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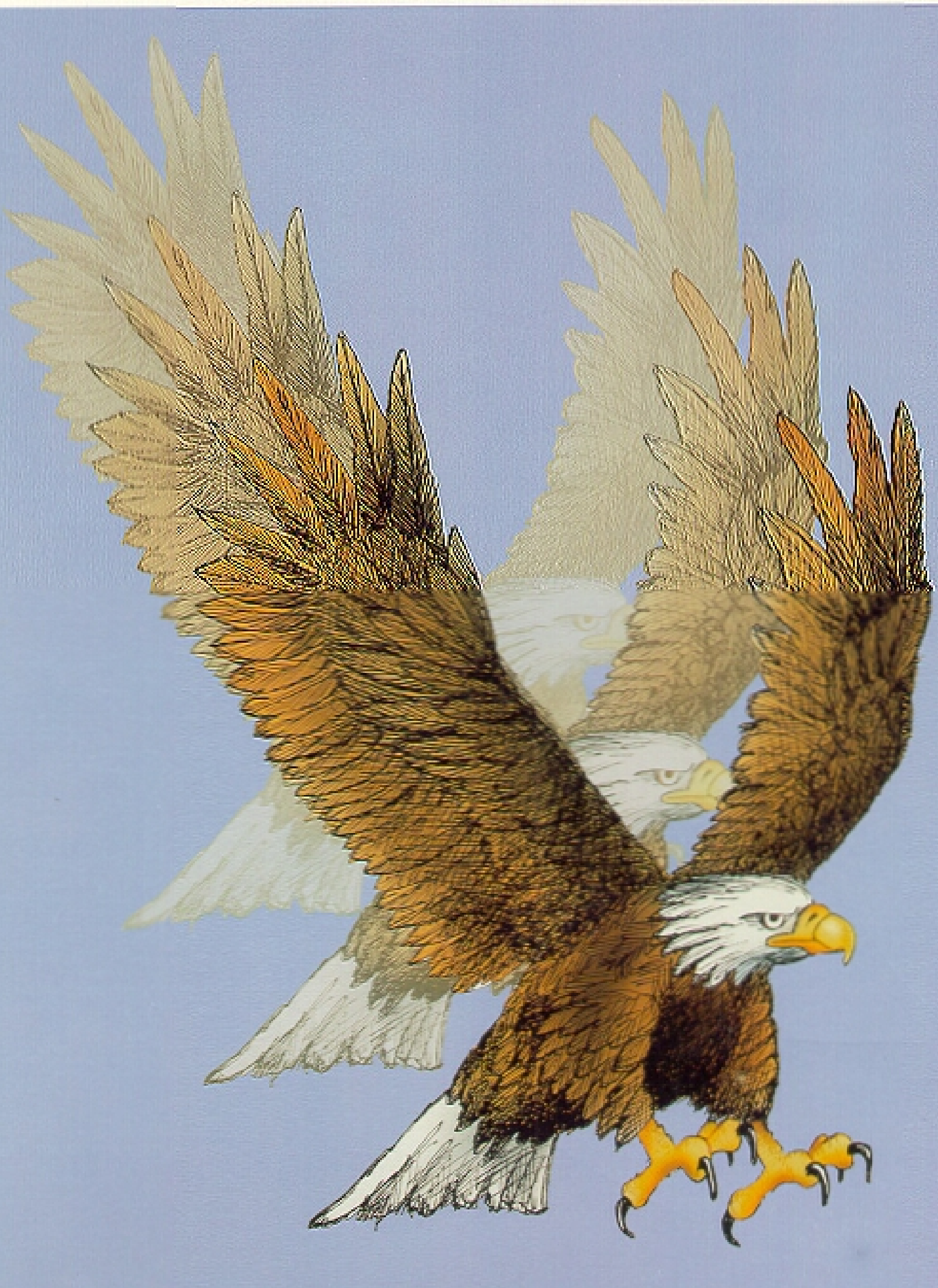
DL128/D
REV 6

Analog/Interface ICs

Device Data

Vol. I



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DL128/D
REV 6

Analog ICs

Device Data

Vol. I

This publication presents technical information for the broad line of Analog and Interface Integrated Circuit products. Complete device specifications are provided in the form of **Data Sheets** which are categorized by product type into ten chapters for easy reference. **Selector Guides** by product family are provided in the beginning of each chapter to enable quick comparisons of performance characteristics. A **Cross Reference** chapter lists Motorola nearest replacement and functional equivalent part numbers for other industry products.

One chapter is devoted showing all of the **Tape and Reel Options**. All **Packaging Information**, including surface mount packages, is provided in another chapter.

Additionally, chapters are provided with information on **Quality and Reliability Assurance** program concepts, high–reliability processing, and abstracts of available **Applications and Product Literature**.

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Data Classification

Product Preview

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Alphanumeric Index and Cross References

In Brief . . .

Motorola Analog and Interface Integrated Circuits cover a much broader range of products than the traditional op amps/ regulators/consumer–image associated with Analog suppliers. Analog circuit technology currently influences the design and architecture of equipment for all major markets. As with other integrated circuit technologies, Analog circuit design techniques and processes have been continually refined and updated to meet the needs of these diversified markets.

Operational amplifiers have utilized JFET inputs for improved performance, plus innovative design and trimming concepts have evolved for improved high performance and precision characteristics. In analog power ICs, basic voltage regulators have been refined to include higher current and voltage levels, low dropout regulators, and more precise three–terminal fixed and adjustable voltages. The power area continues to expand into switching regulators, power supply control and supervisory circuits, motor controllers, and battery charging controllers.

Analog designs also offer a wide array of line drivers, receivers and transceivers for many of the EIA, European, IEEE and IBM interface standards. Peripheral drivers for a variety of devices are also offered. In addition to these key interface functions, hard disk drive read channel circuits, 10BASE–T and Ethernet circuits are also available.

In Data Conversion, a high performance video speed flash converter is available, as well as a variety of CMOS and Sigma–Delta converters. Analog circuit technology has also provided precision low–voltage references for use in Data Conversion and other low temperature drift applications.

A host of special purpose analog devices have also been developed. These circuits find applications in telecommunications, radio, television, automotive, RF communications, and data transmission. These products have reduced the cost of RF communications, and have provided capabilities in telecommunications which make the telephone line convenient for both voice and data communications. Analog developments have also reduced the many discrete components formerly required for consumer functions to a few IC packages and have made significant contributions to the rapidly growing market for electronics in automotive applications.

The table of contents provides a perspective of the many markets served by Analog/Interface ICs and of Motorola's involvement in these areas.

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* = See Communications Device Data (DL136).
\# = Not recommended for new designs.

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* = See Communications Device Data (DL136).
\# = Not recommended for new designs.

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* = See Communications Device Data (DL136).
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* = See Communications Device Data (DL136).
\# = Not recommended for new designs.

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* = See Communications Device Data (DL136).
# = Not recommended for new designs.

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Cross References

The following table represents a cross reference guide for all Analog devices that are manufactured by Motorola. Where the Motorola part number differs from the industry part number, the Motorola device is a “form, fit and function” replacement for the industry part number. However, some differences in characteristics and/or specifications may exist.

Industry Part Number	Motorola Nearest Replacement	Motorola Similar Replacement
75175	SN75175	
9636AT	MC3488AP	
9640PC	MC26S10P#	
9667PC	MC1413P	
9668PC	MC1416P	
AD589J		LM385Z–1.2
AD589K		LM385Z–1.2
AD589L		LM385Z–1.2
AD589M		LM385BZ–1.2
AM201AD		LM201AN
AM201D		LM201AN
AM26LS30P	AM26LS30PC	
AM26LS31CJ	AM26LS31PC#	
AM26LS31CN	AM26LS31PC#	
AM26LS32ACJ	AM26LS32D#	
AM26LS32ACN	AM26LS32PC#	
AM26LS32PC	AM26LS32PC#	
AM723PC	MC1723CP	
AN5150		MC34129P
CA081AE		TL081ACP
CA081E		TL081CP
CA082AE		TL082ACP
CA082E		TL082CP
CA084AE		TL084ACN
CA084E		TL084CN
CA1391E	MC1391P	
CA1458S	MC1458CP1	
CA239AE	LM239AN	
CA239E	LM239N	
CA3026		CA3054
CA3045F		MC3346P
CA3046	MC3346P	
CA3054	CA3054	
CA3058		CA3059
CA3059	CA3059	
CA3079	CA3079	
CA3086F		MC3346P
CA3136A		MC3346P
CA3146		MC3346P
CA339AE	LM339AN	
CA339E	LM339N	
CA723CE	MC1723CP	
CA741CS	MC1741CP1	
CS2842AD	UC2842BD1	
CS2843AD	UC2843BD1	
CS2844D	UC2844BD1	

= Not recommended for new designs.

Industry Part Number	Motorola Nearest Replacement	Motorola Similar Replacement
CS2845D	UC2845BD1	
CS3842AD	UC3842BD1	
CS3843AD	UC3843BD1	
CS3844D	UC3844BD1	
CS3845D	UC3845BD1	
DM8822N		MC1489AP
DS1233M		MC34064P–5
DS1488N	MC1488P	
DS1489AN	MC1489AP	
DS1489N	MC1489P	
DS26LS32N	AM26LS32P#	
DS26S10CN	MC26S10P#	
DS3650N	MC3450P#	
DS8834N		MC8T26AP
DS8835N		MC8T26AP
DS9636ACN	MC3488AP1	
ICL741CLNPA		MC1741CP1
ICL741CLNTY		MC1741CP1
ICL8008CPA		LM301AN
ICL8008CTY		LM301AN
ICL8017CTW		LM301AN
ICL8017MTW		LM301AN
ICL8069CCZR		LM385BZ–1.2
ICL8069DCZR		LM385BZ–1.2
IP33063N	MC33063AP1	
IP34060AN	MC34060AP	
IP34063N	MC34063AP1	
IP3525AN	SG3525AN	
IP3526N	SG3526N	
IP3527AN	SG3527AN	
LM240LAZ–18		MC78L18ACP
LM240LAZ–24		MC78L24ACP
LM240LAZ–5.0		MC78L05ACP
LM240LAZ–6.0		MC78L05ACP
LM240LAZ–8.0		MC78L08ACP
LM249N		MC4741CP
LM2575	LM2575	
LM258D	LM258D	
LM258M	LM258D	
LM258N	LM258N	
LM285Z–1.2	LM285Z–1.2	
LM285Z–2.5	LM285Z–2.5	
LM2901D	LM2901D	
LM2901M	LM2901D	
LM2901N	LM2901N	
LM2902D	LM2902D	

Cross References (continued)

Industry Part Number	Motorola Nearest Replacement	Motorola Similar Replacement
IP494ACJ		TL594IN
IP494ACN		TL594CN
IR3M03A		MC34063AP1
IR3M03AN		MC34063AD
ITT3710		MC1391P
ITT656	MC1413P	
L144AP		LM324N
L203	MC1413P	
L387		MC33267T
LF347BN	LF347BN	
LF347N	LF347N	
LF351BN		MC34001BP
LF351N	LF351N	
LF353AN	MC34002AP	
LF353BN	MC34002BP	
LF353D	LF353D	
LF353N	LF353N	
LF411CD	LF411CD	
LF412CD	LF412CD	
LF441CD	LF441CD	
LF441CN	LF441CN	
LF442CD	LF442CD	
LF442CN	LF442CN	
LF444CD	LF444CD	
LF444CN	LF444CN	
LM11CLN	LM11CLN	
LM11CN	LM11CN	
LM139N	MC1391P	
LM1489AN	MC1489AP	
LM1489N	MC1489P	
LM1496N	MC1496P	
LM1496M	MC1496D	
LM1889		MC1374P
LM1981		MC13020P
LM201AD	LM201AD	
LM201AN	LM201AN	
LM201AP		LM201AN
LM211D	LM211D	
LM211M	LM211D	
LM224D	LM224D	
LM224M	LM224D	
LM224N	LM224N	
LM239AN	LM239AN	
LM239D	LM239D	
LM239M	LM239D	
LM239N	LM239N	
LM240LAZ–12		MC78L12ACP
LM240LAZ–15		MC78L15ACP
LM2902M	LM2902D	
LM2902N	LM2902N	
LM2903D	LM2903D	
LM2903M	LM2903D	

Industry Part Number	Motorola Nearest Replacement	Motorola Similar Replacement
LM2903N	LM2903N	
LM2903P	LM2903N	
LM2904M	LM2904D	
LM2904N	LM2904N	
LM2905N		MC1455P1
LM2931AD–5.0	LM2931AD–5.0	
LM2931AT–5.0	LM2931AT–5.0	
LM2931AZ–5.0	LM2931AZ–5.0	
LM2931CD	LM2931CD	
LM2931CM	LM2931CD	
LM2931CT	LM2931CT	
LM2931D–5.0	LM2931D–5.0	
LM2931D	LM2931D–5.0	
LM2931T–5.0	LM2931T–5.0	
LM2931Z–5.0	LM2931Z–5.0	
LM2935T	LM2935T	
LM293D	LM293D	
LM301AD	LM301AD	
LM301AM	LM301AD	
LM301AN	LM301AN	
LM301AP		LM301AN
LM3045		MC3346P
LM3046N	MC3346P	
LM3054	CA3054	
LM308AD	LM308AD	
LM308AN	LM308AN	
LM308P		MC3356P
LM311D	LM311D	
LM311M	LM311D	
LM311N	LM311N	
LM311P	LM311N	
LM3146A		MC3346P
LM3146		MC3346P
LM317KC	LM317T	
LM317KD		LM317T
LM317LD	LM317LD	
LM317LZ	LM317LZ	
LM317MP		LM317MT
LM317P		LM317T
LM317T	LM317T	
LM3189		MC3356P
LM320LZ–12		MC79L12ACP
LM320LZ–15		MC79L15ACP
LM320LZ–5.0		MC79L05ACP
LM320MP–12		MC7912CT
LM320MP–15		MC7915CT
LM320MP–18		MC7918CT
LM320MP–24		MC7924CT
LM340LAZ–5.0		MC78L05ACP
LM340LAZ–8.0		MC78L08ACP
LM340T–12	LM340T–12	
LM340T–15	LM340T–15	

= Not recommended for new designs.

Cross References (continued)

Industry Part Number	Motorola Nearest Replacement	Motorola Similar Replacement
LM320MP–5.0		MC7905CT
LM320MP–5.2		MC7905.2CT
LM320MP–6.0		MC7906CT
LM320MP–8.0		MC7908CT
LM320T–12		MC7912CT
LM320T–15		MC7915CT
LM320T–5.0		MC7905CT
LM320T–5.2		MC7905.2CT
LM322N		MC1455P1
LM323AT	LM323AT	
LM323T	LM323T	
LM324AD	LM324AD	
LM324AN	LM324AN	
LM324D	LM324D	
LM324M	LM324D	
LM324N	LM324N	
LM337MP		LM337MT
LM337MT	LM337MT	
LM337T	LM337T	
LM339AD	LM339AD	
LM339AM	LM339AD	
LM339AN	LM339AN	
LM339D	LM339D	
LM339N	LM339N	
LM339P		LM339N
LM340AT–12	LM340AT–12	
LM340AT–15	LM340AT–15	
LM340AT–5.0	LM340AT–5.0	
LM340KC–12	LM340T–12	
LM340KC–15	LM340T–15	
LM340LAZ–12		MC78L12ACP
LM340LAZ–18		MC78L18ACP
LM340LAZ–24		MC78L24ACP
LM340T–18	LM340T–18	
LM340T–24	LM340T–24	
LM340T–5.0	LM340T–5.0	
LM340T–6.0	LM340T–6.0	
LM340T–8.0	LM340T–8.0	
LM341P–12		MC78M12CT
LM341P–15		MC78M15CT
LM341P–18		MC78M18CT
LM341P–24		MC78M24CT
LM341P–5.0		MC78M05CT
LM341P–6.0		MC78M06CT
LM341P–8.0		MC78M08CT
LM342P–12		MC78M12CT
LM342P–15		MC78M15CT
LM342P–18		MC78M18CT
LM342P–24		MC78M24CT
LM342P–5.0		MC78M05CT
LM342P–6.0		MC78M06CT
LM342P–8.0		MC78M08CT

Industry Part Number	Motorola Nearest Replacement	Motorola Similar Replacement
LM348D	LM348D	
LM348M	LM348D	
LM349N		MC4741CP
LM350T	LM350T	
LM358AN		LM358N
LM358D	LM358D	
LM358N	LM358N	
LM363AN		MC3450P#
LM363N		MC3450P#
LM385BZ–1.2	LM385BZ–1.2	
LM385BZ–2.5	LM385BZ–2.5	
LM385D–1.2	LM385D–1.2	
LM385D–2.5	LM385D–2.5	
LM385M–1.2	LM385D–1.2	
LM385M–2.5	LM385D–2.5	
LM385Z–1.2	LM385Z–1.2	
LM385Z–2.5	LM385Z–2.5	
LM386N		MC34119P
LM3905N		MC1455P1
LM393AN	LM393AN	
LM393D	LM393D	
LM393JG		LM393N
LM393M	LM393D	
LM393N	LM393N	
LM431ACZ	TL431ACLP	
LM431ACM	TL431ACD	
LM4250CN		MC1776CP1
LM555CN	MC1455P1	
LM556CN	MC3456P	
LM703LN		MC1350P
LM723CN	MC1723CP	
LM741EN		MC1741CP1
LM7805CT	MC7805CT	
LM7812CT	MC7812CT	
LM7815CT	MC7815CT	
LM78L05ACZ	MC78L05ACP	
LM78L05CZ	MC78L05CP	
LM78L08ACZ	MC78L08ACP	
LM78L08CZ	MC78L08CP	
LM78L12ACZ	MC78L12ACP	
LM78L12CZ	MC78L12CP	
LM78L15ACZ	MC78L15ACP	
LM78L15CZ	MC78L15CP	
LM78L18ACZ	MC78L18ACP	
LM78L18CZ	MC78L18CP	
LM78L24ACZ	MC78L24ACP	
LM78L24CZ	MC78L24CP	
LM78M05CP		MC78M05CT
LM78M06CP		MC78M06CT
LM78M12CP		MC78M12CT
LM78M15CP		MC78M15CT
LM7905CT	MC7905CT	

= Not recommended for new designs.

Cross References (continued)

Industry Part Number	Motorola Nearest Replacement	Motorola Similar Replacement
LM7912CT	MC7912CT	
LM7915CT	MC7915CT	
LM79L05ACZ	MC79L05ACP	
LM79L12ACZ	MC79L12ACP	
LM79L15ACZ	MC78L15ACP	
LM79M05CP		MC79M05CT
LM79M12CP		MC79M12CT
LM79M15CP		MC79M15CT
LM833D	LM833D	
LM833N	LM833N	
LM833P	LM833N	
LM837N		MC33079P
LMC6482D		MC33202D
LMC6482P		MC33202P
LMC6484D		MC33204D
LMC6484P		MC33204P
LP2950CZ–3.0	LP2950CZ–3.0	
LP2950CZ–3.3	LP2950CZ–3.3	
LP2950CZ–5.0	LP2950CZ–5.0	
LP2950ACZ–3.0	LP2950ACZ–3.0	
LP2950ACZ–3.3	LP2950ACZ–3.3	
LP2950ACZ–5.0	LP2950ACZ–5.0	
LP2951CM	LP2951CD	
LP2951ACM	LP2951ACD	
LP2951CM–3.0	LP2951CD–3.0	
LP2951CM–3.3	LP2951CD–3.3	
LP2951ACM–3.0	LP2951ACD–3.0	
LP2951ACM–3.3	LP2951ACD–3.3	
LP2951CN	LP2951CN	
LP2951ACN	LP2951ACN	
LP2951CN–3.0	LP2951CN–3.0	
LP2951CN–3.3	LP2951CN–3.3	
LP2951ACN–3.0	LP2951ACN–3.0	
LP2951ACN–3.3	LP2951ACN–3.3	
LT1083		MC34268DT
LT1431CZ	TL431BCLP	
LTC699CN8		MC34064D–5
LTC699IN8		MC33064D–5
MAX809LCPA		MC34064P–5
MB3759	TL494CN	
N5558V	MC1458P1	
N5723A		MC1723CP
N5741A		MC1741CP1
N5741V	MC1741CP1	
N8T26AB	MC8T26AP	
N8T26AN	MC8T26AP	
N8T26B	MC8T26AP	
N8T26N	MC8T26AP	
N8T97B	MC8T97P	
N8T97N	MC8T97P	
N8T98B	MC8T98P	
N8T98N	MC8T98P	

= Not recommended for new designs.

Industry Part Number	Motorola Nearest Replacement	Motorola Similar Replacement
NE550A		MC1723CP
NE555D	MC1455D	
NE555V	MC1455P1	
NE556D	NE556D	
NE5561N		MC34060AP
NE5234D		MC33204D
NE5234P		MC33204P
OP–01P		MC1436P1
RC1458DN	MC1458P1	
RC4136DP		MC3403P
RC4136N		MC3403P
RC4558DN	MC4558CP1	
RC4558P	MC4558CP1	
RC723DB	MC1723CP	
RC741DN	MC1741CP1	
RE5VL47A	MC34164P–5	
RH5RE30AA–T1	MC78LC30HT1	
RH5RE33AA–T1	MC78LC33HT1	
RH5RE40AA–T1	MC78LC40HT1	
RH5RE50AA–T1	MC78LC50HT1	
RN5RG30AA–TR	MC78BC30NTR	
RN5RG33AA–TR	MC78BC33NTR	
RN5RG40AA–TR	MC78BC40NTR	
RN5RG50AA–TR	MC78BC50NTR	
RH5RH301A–T1	MC33466H–30JT1	
RH5RH302B–T1	MC33466H–30LT1	
RH5RH331A–T1	MC33466H–33JT1	
RH5RH332B–T1	MC33466H–33LT1	
RH5RH501A–T1	MC33466H–50JT1	
RH5RH502B–T1	MC33466H–50LT1	
RH5RI301B–T1	MC33463H–30KT1	
RH5RI302B–T1	MC33463H–30LT1	
RH5RI331B–T1	MC33463H–33KT1	
RH5RI332B–T1	MC33463H–33LT1	
RH5RI501B–T1	MC33463H–50KT1	
RH5RI502B–T1	MC33463H–50LT1	
RH5RL30AA–T1	MC78FC30HT1	
RH5RL33AA–T1	MC78FC33HT1	
RH5RL40AA–T1	MC78FC40HT1	
RH5RL50AA–T1	MC78FC50HT1	
RH5VT09AA–T1	MC33464H–09AT1	
RH5VT20AA–T1	MC33464H–20AT1	
RH5VT27AA–T1	MC33464H–27AT1	
RH5VT30AA–T1	MC33464H–30AT1	
RH5VT45AA–T1	MC33464H–45AT1	
RH5VT09CA–T1	MC33464H–09CT1	
RH5VT20CA–T1	MC33464H–20CT1	
RH5VT27CA–T1	MC33464H–27CT1	
RH5VT30CA–T1	MC33464H–30CT1	
RH5VT45CA–T1	MC33464H–45CT1	
RN5RL30AA–TR	MC78FC30NTR	
RN5RL33AA–TR	MC78FC33NTR	

Cross References (continued)

Industry Part Number	Motorola Nearest Replacement	Motorola Similar Replacement
RN5RL40AA–TR	MC78FC40NTR	
RN5RL50AA–TR	MC78FC50NTR	
RN5VD09AA–TR	MC33465N–09ATR	
RN5VD20AA–TR	MC33465N–20ATR	
RN5VD27AA–TR	MC33465N–27ATR	
RN5VD30AA–TR	MC33465N–30ATR	
RN5VD45AA–TR	MC33465N–45ATR	
RN5VD09CA–TR	MC33465N–09CTR	
RN5VD20CA–TR	MC33465N–20CTR	
RN5VD27CA–TR	MC33465N–27CTR	
RN5VD30CA–TR	MC33465N–30CTR	
RN5VD45CA–TR	MC33465N–45CTR	
RN5VT09AA–TR	MC33464N–09ATR	
RN5VT20AA–TR	MC33464N–20ATR	
RN5VT27AA–T4	MC33464N–27ATR	
RN5VT30AA–TR	MC33464N–30ATR	
RN5VT45AA–TR	MC33464N–45ATR	
RN5VT09CA–TR	MC33464N–09CTR	
RN5VT20CA–TR	MC33464N–20CTR	
RN5VT27CA–TR	MC33464N–27CTR	
RN5VT30CA–TR	MC33464N–30CTR	
RN5VT45CA–TR	MC33464N–45CTR	
S–80743AN		MC34164P–3
SA555N	MC1455BP1	
SAA1042		SAA1042V
SG1458M	MC1458P1	
SG1496N	MC1496P	
SG1596J	MC1496BP	
SG201AM	LM201AN	
SG201AN		LM201AN
SG201M	LM201AN	
SG201N		LM201AN
SG224N	LM224N	
SG300N		MC1723CP
SG301AM	LM301AN	
SG301AN		LM301AN
SG308AM	LM308AN	
SG3118AM		LM308AN
SG311M	LM311N	
SG317P	LM317T	
SG317R		LM317T
SG324N	LM324N	
SG337P	LM337T	
SG337R		LM337T
SG3423M		MC3423P1
SG3525AN	SG3525AN	
SG3526N	SG3526N	
SG3527AN	SG3527AN	
SG3561	MC34261P	
SG4250CM		MC1776CP1
SG555CM	MC1455P1	
SG556CN	MC3456P	

= Not recommended for new designs.

Industry Part Number	Motorola Nearest Replacement	Motorola Similar Replacement
SG723CN	MC1723CP	
SG741CM	MC1741CP1	
SG777CN		LM308AN
SG7805ACP	MC7805ACT	
SG7805ACR		MC7805ACT
SG7805ACT		MC7805ACT
SG7805CP	MC7805CT	
SG7806ACP	MC7806ACT	
SG7806ACR		MC7806ACT
SG7806ACT		MC7806ACT
SG7806CP	MC7806CT	
SG7806CR		MC7806CT
SG7808ACP	MC7808ACT	
SG7808ACT		MC7808ACT
SG7808CP	MC7808CT	
SG7808CR		MC7808CT
SG7812ACP	MC7812ACT	
SG7812ACR		MC7812ACT
SG7812ACT		MC7812ACT
SG7812CP	MC7812CT	
SG7812CR		MC7812CT
SG7815ACP	MC7815ACT	
SG7815ACR		MC7815ACT
SG7815ACT		MC7815ACT
SG7815CP	MC7815CT	
SG7815CR		MC7815CT
SG7815CT		MC7815CT
SG7818ACP	MC7818ACT	
SG7818ACR		MC7818ACT
SG7818ACT		MC7818ACT
SG7818CP	MC7818CT	
SG7818CR		MC7818CT
SG7824ACP	MC7824ACT	
SG7824ACR		MC7824ACT
SG7824ACT		MC7824ACT
SG7824CP	MC7824CT	
SG7824CR		MC7824CT
SG7905.2CP	MC7905.2CT	
SG7905.2CR		MC7905.2CT
SG7905.2CT		MC7905.2CT
SG7905ACP	MC7905ACT	
SG7905ACR		MC7905ACT
SG7905ACT		MC7905ACT
SG7905CP	MC7905CT	
SG7905CR		MC7905CT
SG7905CT		MC7905CT
SG7908CP	MC7908CT	
SG7908CR		MC7908CT
SG7908CT		MC7908CT
SG7912ACP	MC7912ACT	
SG7912ACR		MC7912ACT
SG7912ACT		MC7912ACT

Cross References (continued)

Industry Part Number	Motorola Nearest Replacement	Motorola Similar Replacement
SG7912CP	MC7912CT	
SG7912CR		MC7912CT
SG7912CT		MC7912CT
SG79015ACP	MC7915ACT	
SG7915ACR		MC7915ACT
SG7915ACT		MC7915ACT
SG7915CP	MC7915CT	
SG7915CR		MC7915CT
SG7915CT		MC7915CT
SG7918CP	MC7918CT	
SN75LBC086		MC34055DW
SN75121N		MC3481/5P#
SN75126N		MC3481/5P#
SN75150N		MC1488P
SN75154N		MC1489P
SN75174N	MC75174BP	
SN75175N	SN75175N	
SN75188N	MC1488P	
SN75189AN	MC1489AP	
SN75189N	MC1489P	
SN75468N	MC1413P	
SN76591P	MC1391P	
SN76600P	MC1350P	
SSS201AP	LM201AN	
SSS301AP	LM301AN	
TA7504P	MC1741CP1	
TA7506P	LM301AN	
TA75071P		MC34001P
TA75072P		MC34002P
TA75074F		MC34004P
TA75339F	LM339D	
TA75339P	LM339N	
TA75358CF	LM358D	
TA75358CP	LM358N	
TA75393F	LM393D	
TA75393P	LM393N	
TA75458F	MC1458D	
TA75458P	MC1458CP1	
TA75558P	MC4558CP1	
TA7555F	MC1455D	
TA7555P	MC1455P1	
TA75902F	LM324D	
TA76494P		TL494IN
TA78005AP	MC7805CT	
TA78006AP	MC7806CT	
TA78008AP	MC7808CT	
TA78012AP	MC7812CT	
TA78015AP	MC7815CT	
TA78018AP	MC7818CT	
TA78024AP	MC7824CT	
TA78L005AP		MC78L05ACP
TA78L005P		MC78L05CP

= Not recommended for new designs.

Industry Part Number	Motorola Nearest Replacement	Motorola Similar Replacement
TA78L008AP		MC78L08ACP
TA78L008P		MC78L08CP
TA78L012AP		MC78L12ACP
TA78L012P		MC78L12CP
TA78L015AP		MC78L15ACP
TA78L015P		MC78L15CP
TA78L018AP		MC78L18ACP
TA78L018P		MC78L18CP
TA78L024AP		MC78L24ACP
TA78L024P		MC78L24CP
TA78M05P	MC78M05CT	
TA78M06P	MC78M06CT	
TA78M08P	MC78M08CT	
TA78M12P	MC78M12CT	
TA78M18P	MC78M18CT	
TA78M20P	MC78M20CT	
TA78M24P	MC78M24CT	
TA79005P	MC7905CT	
TA79006P	MC7906CT	
TA79008P	MC7908CT	
TA79012P	MC7912CT	
TA79015P	MC7915CT	
TA79018P	MC7918CT	
TA79024P	MC7924CT	
TA79L005P		MC79L05CP
TA79L012P		MC79L12P
TA79L015P		MC79L15P
TA79L018P		MC79L18P
TA79L024P		MC79L24P
TB920		MC1391P
TBA920S		MC1391P
TCF5600	TCF5600	
TD62003P/AP	MC1413P	
TD62479P	MC1374P	
TDA1085C	TDA1085C	
TDA1085		TDA1085C
TDA1185A	TDA1185A#	
TDA4817		MC34261P
TDC1018		MC10324P
TDC1048		MC10319P
TK115	MC33264	
TL022CP		LM358N
TL044CJ		LM324N
TL062ACP	TL062ACP	
TL062CD	TL062CD	
TL062CP	TL062CP	
TL062VP	TL062VP	
TL064ACD	TL064ACD	
TL064ACN	TL064ACN	
TL064CD	TL064CD	
TL064CN	TL064CN	
TL064VN	TL064VN	

Cross References (continued)

Industry Part Number	Motorola Nearest Replacement	Motorola Similar Replacement
TL071ACD	TL071ACD	
TL071ACP	TL071ACP	
TL071CD	TL071CD	
TL071CP	TL071CP	
TL072ACD	TL072ACD	
TL072ACP	TL072ACP	
TL072CD	TL072CD	
TL072CP	TL072CP	
TL074ACN	TL074ACN	
TL074CN	TL074CN	
TL081ACD	TL081ACD	
TL081ACP	TL081ACP	
TL081CD	TL081CD	
TL081CP	TL081CP	
TL082ACP	TL082ACP	
TL082CD	TL082CD	
TL082CP	TL082CP	
TL084ACN	TL084ACN	
TL084CN	TL084CN	
TL431CD	TL431CD	
TL431CLP	TL431CLP	
TL431CP	TL431CP	
TL431ILP	TL431ILP	
TL431IP	TL431IP	
TL494CN	TL494CN	
TL494IN	TL494IN	
TL497CN		MC34063AP1
TL594CN	TL594CN	
TL594IN	TL594IN	
TL780–05CKC	TL780–05CKC	
TL780–12CKC	TL780–12CKC	
TL780–15CKC	TL780–15CKC	
TL7805ACKC	MC7805ACT	
TLC2272D		MC33202D
TLC2272P		MC33202P
TLC2274D		MC33204D
TLC2274P		MC33204P
µA1391PC	MC1391P	
µA1458CP	MC1458CP1	
µA1458CTC	MC1458CP1	
µA1458P	MC1458P1	
µA1458TC	MC1458P1	
µA2240PC		MC1455P1
µA301AT	LM301AN	
µA3026HM		CA3054
µA3045		MC3346P
µA3046DC	MC3346P	
µA3054DC	CA3054	
µA311T	LM311N	
µA317UC	LM317T	
µA3303P	MC3303P	
µA3403P	MC3403P	

= Not recommended for new designs.

Industry Part Number	Motorola Nearest Replacement	Motorola Similar Replacement
µA4136PC		MC4741CP
µA431AWC	TL431CP	
µA4558TC	MC4558CP1	
µA494PC	TL494CN	
µA555TC	MC1455P1	
µA556PC	MC3456P	
µA723CN	MC1723CP	
µA723PC	MC1723CP	
µA741CP	MC1741CP1	
µA742DC		CA3059
µA757DC		MC1350P
µA757DM		MC1350P
µA775PC	LM339N	
µA776TC	MC1776CP1	
µA7805CKC	MC7805CT	
µA7805UC	MC7805CT	
µA7805UV	MC7805BT	
µA7806CKC	MC7806CT	
µA7806UC	MC7806CT	
µA7806UV	MC7806BT	
µA7808CKC	MC7808CT	
µA7808UC	MC7808CT	
µA7808UV	MC7808BT	
µA7812CKC	MC7812CT	
µA7812UC	MC7812CT	
µA7812UV	MC7812BT	
µA7815CKC	MC7815CT	
µA7815UC	MC7815CT	
µA7815UV	MC7815BT	
µA7818CKC	MC7818CT	
µA7818UC	MC7818CT	
µA7818UV	MC7818BT	
µA7824CKC	MC7824CT	
µA7824UC	MC7824CT	
µA7824UV	MC7824BT	
µA78GU1C		LM317T
µA78GUC		LM317T
µA78L05ACLP	MC78L05ACP	
µA78L05AWC		MC78L05ACP
µA78L05CLP	MC78L05CP	
µA78L05WC		MC78L05CP
µA78L08ACLP	MC78L08ACP	
µA78L08AWC		MC78L08ACP
µA78L08CLP	MC78L08CP	
µA78L12ACLP	MC78L12ACP	
µA78L12AWC		MC78L12ACP
µA78L12CLP	MC78L12CP	
µA78L12WC		MC78L12CP
µA78L15ACLP	MC78L15ACP	
µA78L15AWC		MC78L15ACP
µA78L15CLP	MC78L15CP	
µA78L15WC		MC78L15CP

Cross References (continued)

Industry Part Number	Motorola Nearest Replacement	Motorola Similar Replacement
µA78L18AWC		MC78L18ACP
µA78L24AWC	MC78L24ACP	
µA78M05CKC	MC78M05CT	
µA78M05CKD		MC78M05CT
µA78M05UC	MC78M05CT	
µA78M06CKC	MC78M06CT	
µA78M06CKD		MC78M06CT
µA78M06UC	MC78M06CT	
µA78M08CKC	MC78M08CT	
µA78M08CKD		MC78M08CT
µA78M08UC	MC78M08CT	
µA78M12CKC	MC78M12CT	
µA78M12CKD		MC78M12CT
µA78M12UC	MC78M12CT	
µA78M15CKC	MC78M15CT	
µA78M15CKD		MC78M15CT
µA78M15UC	MC78M15CT	
µA78M18UC	MC78M18CT	
µA78M20CKC	MC78M20CT	
µA78M20CKD		MC78M20CT
µA78M20UC	MC78M20CT	
µA78M24CKC	MC78M24CT	
µA78M24CKD		MC78M24CT
µA78M24UC	MC78M24CT	
µA78MGT2C		LM317T
µA78MGU1C		LM317T
µA78MGUC		LM317MT
µA78S40PC	µA78S40PC	
µA78S40PV	µA78S40PV	
µA7905.2CKC	MC7905.2CT	
µA7905CKC	MC7905CT	
µA7905UC	MC7905CT	
µA7906CKC	MC7906CT	
µA7906UC	MC7906CT	
µA7908CKC	MC7908CT	
µA7912CKC	MC7912CT	
µA7912UC	MC7912CT	
µA7915CKC	MC7915CT	
µA7915UC	MC7915CT	
µA7918CKC	MC7918CT	
µA7918UC	MC7918CT	
µA7924CKC	MC7924CT	
µA7924UC	MC7924CT	
µA798TC	MC3458P1	
µA79L05AWC	MC79L05ACP	
µA79L05WC	MC79L05CP	
µA79L12AWC	MC79L12ACP	
µA79L12WC	MC79L12CP	
µA79L15AWC	MC79L15ACP	
µA79L15WC	MC79L15CP	
µA79M05AUC	MC79M05CT	
µA79M05CKC	MC79M05CT	

Industry Part Number	Motorola Nearest Replacement	Motorola Similar Replacement
µA79M06AUC		MC79M06CT
µA79M06CKC		MC79M06CT
µA79M06UC		MC79M06CT
µA79M08AUC		MC79M08CT
µA79M08CKC		MC79M08CT
µA79M08UC		MC79M08CT
µA79M12AUC	MC79M12CT	
µA79M12CKC	MC79M12CT	
µA79M18AUC		MC79M18CT
µA79M18UC		MC79M18CT
µA79M24AUC		MC79M24CT
µA79M24CKC		MC79M24CT
µA79M24UC		MC79M24CT
µA9636ATC	MC3488AP1	
UAA1016B	UAA1016B	
UC2823DW		MC33023DW
UC2823N		MC33023P
UC2823Q		MC33023FN
UC2825DW		MC33025DW
UC2825N		MC33025P
UC2825Q		MC33025FN
UC2842AD	UC2842AD	
UC2842AN	UC2842AN	
UC2842BD	UC2842BD	
UC2842BN	UC2842BN	
UC2842D	UC2842AD	
UC2842N	UC2842AN	
UC2843AD	UC2843AD	
UC2843AN	UC2843AN	
UC2843BD	UC2843BD	
UC2843BN	UC2843BN	
UC2843D	UC2843AD	
UC2843N	UC2843AN	
UC2844BD	UC2844BD	
UC2844BN	UC2844BN	
UC2844D	UC2844D	
UC2844N	UC2844N	
UC2845BD	UC2845BD	
UC2845BN	UC2845BN	
UC2845D	UC2845D	
UC2845N	UC2845N	
UC317T	LM317T	
UC337T	LM337T	
UC3525AN	SG3525AN	
UC3526N	SG3526N	
UC3527AN	SG3527AN	
UC3823DW		MC34023DW
UC3823N		MC34023P
UC3823Q		MC34023FN
UC3825DW		MC34025DW
UC3825N		MC34025P
UC3825Q		MC34025FN

= Not recommended for new designs.

Cross References (continued)

Industry Part Number	Motorola Nearest Replacement	Motorola Similar Replacement
UC3842AD	UC3842AD	
UC3842AN	UC3842AN	
UC3842BD	UC3842BD	
UC3842BN	UC3842BN	
UC3842D	UC3842AD	
UC3842N	UC3842AN	
UC3843AD	UC3843AD	
UC3843AN	UC3843AN	
UC3843BD	UC3843BD	
UC3843BN	UC3843BN	
UC3843D	UC3843AD	
UC3843N	UC3843AN	
UC3844BD	UC3844BD	
UC3844BN	UC3844BN	
UC3844D	UC3844D	
UC3844N	UC3844N	
UC3845BD	UC3845BD	
UC3845BN	UC3845BN	
UC3845D	UC3845D	

Industry Part Number	Motorola Nearest Replacement	Motorola Similar Replacement
UC3845N	UC3845N	
UC494ACN		TL594CN
UC494CN		TL494CN
UCN5816A	MC34142FN	
ULN2003A	MC1413	
ULN2004A	MC1416	
ULN2068BB	ULN2068B#	
ULN2068NE	ULN2068B#	
ULN2151H	MC1741CP1	
ULN2151M		MC1741CP1
ULN2803A	ULN2803A	
ULN2804A	ULN2804A	
ULN8126A	SG3526N	
ULS2151M		MC1741CP1
ULX8161M		MC34060AP
UPD6950C		MC10319P
UVC3101		MC10319P
XR082CP	TL082CP	
XR084CP	TL084CN	

= Not recommended for new designs.

Amplifiers and Comparators

In Brief . . .

For over two decades, Motorola has continually refined and updated integrated circuit technologies, analog circuit design techniques and processes in response to the needs of the marketplace. The enhanced performance of newer operational amplifiers and comparators has come through innovative application of these technologies, designs and processes. Some early designs are still available but are giving way to the new, higher performance operational amplifier and comparator circuits. Motorola has pioneered in JFET inputs, low temperature coefficient input stages, Miller loop compensation, all NPN output stages, dual–doublet frequency compensation and analog “in–the–package” trimming of resistors to produce superior high performance operational amplifiers and comparators, operating in many cases from a single supply with low input offset, low noise, low power, high output swing, high slew rate and high gain–bandwidth product at reasonable cost to the customer.

Present day operational amplifiers and comparators find applications in all market segments including motor controls, instrumentation, aerospace, automotive, telecommunications, medical, and consumer products.

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Operational Amplifiers

Motorola offers a broad line of bipolar operational amplifiers to meet a wide range of applications. From low–cost industry–standard types to high precision circuits, the span encompasses a large range of performance capabilities. These Analog integrated circuits are available as single, dual and quad monolithic devices in a variety of temperature ranges and package styles. Most devices may be obtained in unencapsulated ‘‘chip’’ form as well. For price and delivery information on chips, please contact your Motorola Sales Representative or Distributor.

Table 1. Single Operational Amplifiers

Device	I_{IB} (µA) Max	V_{IO} (mV) Max	TC_{VIO} (µV/°C) Typ	I_{IO} (nA) Max	A_{vol} (V/mV) Min	BW ($A_V = 1$) (MHz) Typ	SR ($A_V = 1$) (V/µs) Typ	Supply Voltage (V)		Description	Suffix/ Package
								Min	Max		
Noncompensated											
Commercial Temperature Range (0°C to +70°C)											
LM301A	0.25	7.5	10	50	25	1.0	0.5	±3.0	±18	General Purpose	N/626, D/751
LM308A	7.0	0.5	5.0	1.0	80	1.0	0.3	±3.0	±18	Precision	N/626, D/751
Industrial Temperature Range (–25°C to +85°C)											
LM201A	0.075	2.0	10	10	50	1.0	0.5	±3.0	±22	General Purpose	N/626, D/751
Internally Compensated											
Commercial Temperature Range (0°C to +70°C)											
LF351	200 pA	10	10	100 pA	25	4.0	13	±5.0	±18	JFET Input	N/626, D/751
LF411C	200 pA	2.0	10	100 pA	25	8.0	25	+5.0	±22	JFET Input, Low Offset, Low Drift	N/626, D/751
LF441C	100 pA	5.0	10	50 pA	25	2.0	6.0	±5.0	±18	Low Power, JFET Input	N/626, D/751
LM11C	100 pA	0.6	2.0	10 pA	250	1.0	0.3	±3.0	±20	Precision	N/626
LM11CL	200 pA	5.0	3.0	25 pA	50	1.0	0.3	±3.0	±20	Precision	N/626
MC1436, C	0.04	10	12	10	70	1.0	2.0	±15	±34	High Voltage	P1/626, D/751
MC1741C	0.5	6.0	15	200	20	1.0	0.5	±3.0	±18	General Purpose	P1/626, D/751
MC1776C	0.003	6.0	15	3.0	100	1.0	0.2	±1.2	±18	µPower, Programmable	P1/626, D/751
MC3476	0.05	6.0	15	25	50	1.0	0.2	±1.5	±18	Low Cost, µPower, Programmable	P1/626
MC34001	200 pA	10	10	100 pA	25	4.0	13	±5.0	±18	JFET Input	P/626, D/751
MC34001B	200 pA	5.0	10	100 pA	50	4.0	13	±5.0	±18	JFET Input	P/626, D/751
MC34071	0.5	5.0	10	75	25	4.5	10	+3.0	+44	High Performance	P/626, D/751
MC34071A	500 nA	3.0	10	50	50	4.5	10	+3.0	+44	Single Supply	P/626, D/751
MC34080B	200 pA	1.0	10	100 pA	25	16	55	±5.0	±22	Decompensated	P/626, D/751
MC34081B	200 pA	1.0	10	100 pA	25	8.0	30	±5.0	±22	High Speed, JFET Input	P/626, D/751
MC34181	0.1 nA	2.0	10	0.05	25	4.0	10	±2.5	±18	Low Power, JFET Input	P/626
TL071AC	200 pA	6.0	10	50 pA	50	4.0	13	±5.0	±18	Low Noise, JFET Input	P/626, D/751
TL071C	200 pA	10	10	50 pA	25	4.0	13	±5.0	±18	Low Noise, JFET Input	P/626, D/751
TL081AC	200 pA	6.0	10	100 pA	50	4.0	13	±5.0	±18	JFET Input	P/626, D/751
TL081C	400 pA	15	10	200 pA	25	4.0	13	±5.0	±18	JFET Input	P/626, D/751
Automotive Temperature Range (–40°C to +85°C)											
MC33071	0.5	5.0	10	75	25	4.5	10	+3.0	+44	High Performance	P/626, D/751
MC33071A	500 nA	3.0	10	50	50	4.5	10	+3.0	+44	Single Supply	P/626, D/751
MC33171	0.1	4.5	10	20	50	1.8	2.1	+3.0	+44	Low Power, Single Supply	P/626, D/751
MC33181	0.1 nA	2.0	10	0.05	25	4.0	10	±2.5	±18	Low Power, JFET Input	P/626, D/751
Extended Automotive Temperature Range (–40°C to +105°C)											
MC33201	250 nA	9.0	2.0	100	50	2.2	1.0	±0.9	±6.0	Low V Rail–to–Rail	P/626, D/751
Military Temperature Range (–55°C to +125°C)											
MC33201	400 nA	9.0	2.0	200	50	2.2	1.0	±0.9	±6.0	Low V Rail–to–Rail	P/626, D/751

Table 2. Dual Operational Amplifiers

Device	I_{IB} (μA) Max	V_{IO} (mV) Max	TC_{VIO} (μV/°C) Typ	I_{IO} (nA) Max	A_{vol} (V/mV) Min	BW (A_V = 1) (MHz) Typ	SR (A_V = 1) (V/μs) Typ	Supply Voltage (V) Min	Max	Description	Suffix/ Package
Internally Compensated											
Commercial Temperature Range (0°C to +70°C)											
LF353	200 pA	10	10	100 pA	25	4.0	13	±5.0	±18	JFET Input	N/626, D/751
LF412C	200 pA	3.0	10	100 pA	25	4.0	13	+5.0	±18	JFET Input, Low Offset, Low Drift	N/626, D/751
LF442C	100 pA	5.0	10	50 pA	25	2.0	6.0	±5.0	±18	Low Power, JFET Input	N/626
LM358	0.25	6.0	7.0	50	25	1.0	0.6	±1.5 +3.0	±18 +36	Single Supply, Low Power Consumption	N/626, D/751
LM833	1.0	5.0	2.0	200	31.6	15	7.0	+2.5	±18	Low Noise, Audio	N/626, D/751
MC/MCT1458	0.5	6.0	10	200	20	1.1	0.8	±3.0	±18	Dual MC1741	P1/626, D/751
MC1458C	0.7	10	10	300	20	1.1	0.8	±3.0	±18	General Purpose	P1/626, D/751
MC3458	0.5	10	7.0	50	20	1.0	0.6	±1.5 +3.0	±18 +36	Split Supplies, Single Supply, Low Crossover Distortion	P1/626, D/751
MC4558AC	0.5	5.0	10	200	50	2.8	1.6	±3.0	±22	High Frequency	P1/626
MC/MCT4558C	0.5	6.0	10	200	20	2.8	1.6	±3.0	±18	High Frequency	P1/626, D/751
MC34002	100 pA	10	10	100 pA	25	4.0	13	±5.0	±18	JFET Input	P/626, D/751
MC34002B	100 pA	5.0	10	70 pA	25	4.0	13	±5.0	±18	JFET Input	P/626, D/751
MC34072	0.5	5.0	10	75	25	4.5	10	+3.0	+44	High Performance	P/626, D/751
MC34072A	500 nA	3.0	10	50	50	4.5	10	+3.0	+44	Single Supply	P/626, D/751
MC34082	200 pA	3.0	10	100 pA	25	8.0	30	±5.0	±22	High Speed, JFET Input	P/626
MC34083B	200 pA	3.0	10	100 pA	25	16	55	±5.0	±22	Decompensated	P/626
MC34182	0.1 nA	3.0	10	0.05	25	4.0	10	±2.5	±18	Low Power, JFET Input	P/626, D/751
TL062AC	200 pA	6.0	10	100 pA	4.0	2.0	6.0	±2.5	±18	Low Power, JFET Input	P/626, D/751
TL062C	200 pA	15	10	200 pA	4.0	2.0	6.0	±2.5	±18	Low Power, JFET Input	P/626, D/751
TL072AC	200 pA	6.0	10	50 pA	50	4.0	13	±5.0	±18	Low Noise, JFET Input	P/626, D/751
TL072C	200 pA	10	10	50 pA	25	4.0	13	±5.0	±18	Low Noise, JFET Input	P/626, D/751
TL082AC	200 pA	6.0	10	100 pA	50	4.0	13	±5.0	±18	JFET Input	P/626, D/751
TL082C	400 pA	15	10	200 pA	25	4.0	13	±5.0	±18	JFET Input	P/626, D/751
Industrial Temperature Range (–25°C to +85°C)											
LM258	0.15	5.0	10	30	50	1.0	0.6	±1.5 +3.0	±18 +36	Split or Single Supply Op Amp	N/626, D/751
Automotive Temperature Range (–40°C to +85°C)											
MC3358	5.0	8.0	10	75	20	1.0	0.6	±1.5 +3.0	±18 +36	Split or Single Supply	P1/626
MC33072	0.50	5.0	10	75	25	4.5	10	+3.0	+44	High Performance	P/626, D/751
MC33072A	500 nA	3.0	10	50	50	4.5	10	+3.0	+44	Single Supply	P/626, D/751
MC33076	0.5	4.0	2.0	70	25	7.4	2.6	±2.0	±18	High Output Current	P1/626, P2/648C, D/751
MC33077	1.0	1.0	2.0	180	150	37	11	±2.5	±18	Low Noise	P/626, D/751
MC33078	750 nA	2.0	2.0	150	31.6	16	7.0	±5.0	±18	Low Noise	N/626, D/751
MC33102											P/626, D/751
(Awake)	600 nA	3.0	1.0	60	25	4.6	1.7	±2.5	±18	Sleep–Mode™ Micropower	
(Sleep)	60 nA	3.0	1.0	6.0	15	0.3	0.1	±2.5	±18		
MC33172	0.10	4.5	10	20	50	1.8	2.1	+3.0	+44	Low Power, Single Supply	P/626, D/751
MC33178	0.5	3.0	2.0	50	50	5.0	2.0	±2.0	±18	High Output Current	P/626, D/751
MC33182	0.1 nA	3.0	10	0.05	25	4.0	10	±2.5	±18	Low Power, JFET Input	P/626, D/751
MC33272A	650 nA	1.0	0.56	25 nA	31.6	5.5	11.5	±1.5	±18	High Performance	P/626, D/751
MC33282	100 pA	200 μV	5.0	50 pA	50	30	12	±2.5	±18	Low Input, Offset JFET	P/626, D/751
TL062V	200 pA	6.0	10	100 pA	4.0	2.0	6.0	±2.5	±18	Low Power, JFET Input	P/626, D/751

Table 2. Dual Operational Amplifiers (continued)

Device	I_{IB} (μA) Max	V_{IO} (mV) Max	TC_{VIO} (μV/°C) Typ	I_{IO} (nA) Max	A_{vol} (V/mV) Min	BW (A_V = 1) (MHz) Typ	SR (A_V = 1) (V/μs) Typ	Supply Voltage (V)		Description	Suffix/ Package
								Min	Max		
Extended Automotive Temperature Range (–40°C to +105°C)											
MC33202	250 nA	11	2.0	100	50	2.2	1.0	±0.9	±6.0	Low V Rail–to–Rail	P/626, D/751
MC33206										Rail–to–Rail with Enable	P/646, D/751A
LM2904	0.25	10	7.0	50	100 typ	1.0	0.6	±1.5 +3.0	±13 +26	Split or Single Supply	N/626, D/751
Extended Automotive Temperature Range (–40°C to +125°C)											
TCA0372	500 nA	15	20	50	30	1.1	1.4	+5.0	+36	Power Op Amp, Single Supply	DP2/648, DW/751G
LM2904V	0.25	13	7.0	50	100 typ	1.0	0.6	±1.5 +3.0	±13 +26	Split or Single Supply	N/626, D/751
Military Temperature Range (–55°C to +125°C)											
MC33202	400 pA	11	2.0	200 pA	50	2.2	1.0	±0.9	±6.0	Low V Rail–to–Rail	P/626, D/751

Table 3. Quad Operational Amplifiers

Device	I_{IB} (μA) Max	V_{IO} (mV) Max	TC_{VIO} (μV/°C) Typ	I_{IO} (nA) Max	A_{vol} (V/mV) Min	BW (A_V = 1) (MHz) Typ	SR (A_V = 1) (V/μs) Typ	Supply Voltage (V)		Description	Suffix/ Package
								Min	Max		
Internally Compensated											
Commercial Temperature Range (0°C to +70°C)											
LF347	200 pA	10	10	100 pA	25	4.0	13	±5.0	±18	JFET Input	N/646
LF347B	200 pA	5.0	10	100 pA	50	4.0	13	±5.0	±18	JFET Input	N/646
LF444C	100 pA	10	10	50 pA	25	2.0	6.0	±5.0	±18	Low Power, JFET Input	N/646, D/751A
LM324, A	0.25	6.0	7.0	50	25	1.0	0.6	±1.5 +3.0	±16 +32	Low Power Consumption	N/646, D/751A
LM348	0.2	6.0	–	50	25	1.0	0.5	±3.0	±18	Quad MC1741	D/751A
LM3900								+3.0	+36		
MC3403	0.5	10	7.0	50	20	1.0	0.6	±1.5 +3.0	±18 +36	No Crossover Distortion	P/646, D/751A
MC4741C	0.5	6.0	15	200	20	1.0	0.5	±3.0	±18	Quad MC1741	P/646, D/751A
MC34004	200 pA	10	10	100 pA	25	4.0	13	±5.0	±18	JFET Input	P/646
MC34004B	200 pA	5.0	10	100 pA	50	4.0	13	±5.0	±18	JFET Input	P/646
MC34074	0.5	5.0	10	75	25	4.5	10	+3.0	+44	High Performance	P/646, D/751A
MC34074A	500 nA	3.0	10	50	50	4.5	10	+3.0	+44	Single Supply	P/646, D/751A
MC34084	200 pA	12	10	100 pA	25	8.0	30	±5.0	±22	High Speed, JFET Input	P/646, DW/751G
MC34085B	200 pA	12	10	100 pA	25	16	55	±5.0	±22	Decompensated	P/646, DW/751G
MC34184	0.1 nA	10	10	0.05	25	4.0	10	±2.5	±18	Low Power, JFET Input	P/646, D/751A
TL064AC	200 pA	6.0	10	100 pA	4.0	2.0	6.0	±2.5	±18	Low Power, JFET Input	N/646, D/751A
TL064C	200 pA	15	10	200 pA	4.0	2.0	6.0	±2.5	±18	Low Power, JFET Input	N/646, D/751A
TL074AC	200 pA	6.0	10	50 pA	50	4.0	13	±5.0	±18	Low Noise, JFET Input	N/646
TL074C	200 pA	10	10	50 pA	25	4.0	13	±5.0	±18	Low Noise, JFET Input	N/646
TL084AC	200 pA	6.0	10	100 pA	50	4.0	13	±5.0	±18	JFET Input	N/646
TL084C	400 pA	15	10	200 pA	25	4.0	13	±5.0	±18	JFET Input	N/646
Industrial Temperature Range (–25°C to +85°C)											
LM224, A	0.15	5.0	7.0	30	50	1.0	0.6	±1.5 +3.0	±16 +32	Split Supplies or Single Supply	N/646, D/751A
Automotive Temperature Range (–40°C to +85°C)											
MC3301/ LM2900	0.3	–	–	–	1.0	4.0	0.6	±2.0 +4.0	±15 +28	Norton Input	P/646 N/646
MC3303	0.5	8.0	10	75	20	1.0	0.6	±1.5 +3.0	±18 +36	Differential General Purpose	P/646, D/751A

Table 3. Quad Operational Amplifiers (continued)

Device	I_{IB} (µA) Max	V_{IO} (mV) Max	TC_{VIO} (µV/°C) Typ	I_{IO} (nA) Max	A_{vol} (V/mV) Min	BW (A_V = 1) (MHz) Typ	SR (A_V = 1) (V/µs) Typ	Supply Voltage (V) Min	Supply Voltage (V) Max	Description	Suffix/ Package
MC33074	0.5	4.5	10	75	25	4.5	10	+3.0	+44	High Performance, Single Supply	P/646, D/751A
MC33074A	500 nA	3.0	10	50	50	4.5	10	+3.0	+44	High Performance	P/646, D/751A
MC33079	750 nA	2.5	2.0	150	31.6	9.0	7.0	±5.0	±18	Low Noise	N/646, D/751A
MC33174	0.1	4.5	10	20	50	1.8	2.1	+3.0	+44	Low Power, Single Supply	P/646, D/751A
MC33179	0.5	3.0	2.0	50	50	5.0	2.0	±2.0	±18	High Output Current	P/646, D/751A
MC33184	0.1 nA	10	10	0.05	25	4.0	10	±2.5	±18	Low Power, JFET Input	P/646, D/751A
MC33274A	650 nA	1.0	0.56	25 nA	31.6	5.5	11.5	±1.5	±18	High Performance	P/646, D/751A
MC33284	100 pA	2.0	5.0	50 pA	50	30	12	±2.5	±18	Low Input, Offset JFET	P/646, D/751A
TL064V	200 pA	9.0	10	100 pA	4.0	2.0	6.0	±2.5	±18	Low Power, JFET Input	N/646, D/751A
Extended Automotive Temperature Range (–40°C to +105°C)											
MC33204	250 nA	13	2.0	100	50	2.2	1.0	±0.9	±6.0	Low V Rail–to–Rail	P/646, D/751A
MC33207					50	2.2		±0.9	±6.0	Rail–to–Rail with Enable	P/648, D/751B
MC33304					25	3.0		+1.8	+12	Sleepmode, Rail–to–Rail	P/646, D/751A
LM2902	0.5	10	–	50	15	1.0	0.6	±1.5 +3.0	±13 +26	Differential Low Power	N/646, D/751A
Extended Automotive Temperature Range (–40°C to +125°C)											
LM2902V	0.5	13	–	50	15	1.0	0.6	±1.5 +3.0	±13 +26	Differential Low Power	N/646, D/751A
Military Temperature Range (–55°C to +125°C)											
MC33204	400 pA	13	2.0	200 pA	50	2.2	1.0	±0.9	±6.0	Low V Rail–to–Rail	P/646, D/751A

High Frequency Amplifiers

A variety of high frequency circuits with features ranging from low cost simplicity to multifunction versatility marks Motorola’s line of integrated amplifiers. Devices described here are intended for industrial and communications applications. For devices especially dedicated to consumer products, i.e., TV and entertainment radio. (See the Consumer Electronics Circuits section.)

AGC Amplifiers

MC1490/MC1350 Family Wideband General Purpose Amplifiers

The MC1490 and MC1350 family are basic building blocks – AGC (Automatic Gain Controlled) RF/Video Amplifiers. These parts are recommended for applications up through 70 MHz. The best high frequency performance may be obtained by using the physically smaller SOIC version (shorter leads) – MC1350D. There are currently no other RF ICs like these, because other manufacturers have dropped their copies. Applications include variable gain video and instrumentation amplifiers, IF (Intermediate Frequency) amplifiers for radio and TV receivers, and transmitter power output control. Many uses will be found in medical instrumentation, remote monitoring, video/graphics processing, and a variety of communications equipment. The family of parts using the same basic die (identical circuit with slightly different test parameters) is listed in the following table.

Table 4. High Frequency Amplifier Specifications

Operating Temperature Range		A_V (dB)	Bandwidth @ MHz	V_{CC}/V_{EE} (Vdc)		Suffix/ Package
–40° to +85°C	0° to +70°C	Typical		Minimum	Maximum	
–	MC1350	50	45	+6.0	+18	P/626, D/751
MC1490	–	50 45 35	10 60 100			P/626

Miscellaneous Amplifiers

Motorola provides several Bipolar and CMOS special purpose amplifiers which fill specific needs. These devices range from low power CMOS programmable amplifiers and comparators to variable–gain bipolar power amplifiers.

MC3405
Dual Operational Amplifier and Dual Voltage Comparator

This device contains two Differential Input Operational Amplifiers and two Comparators; each set capable of single supply operation. This operational amplifier–comparator circuit will find its applications as a general purpose product for automotive circuits and as an industrial ''building block.''

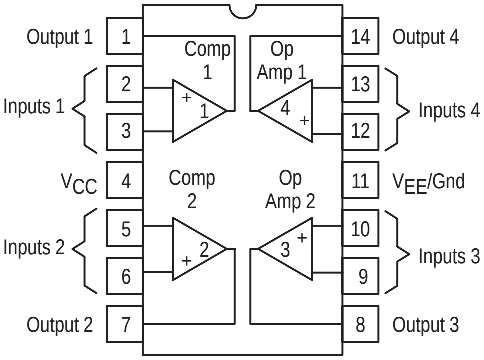


Table 5. Bipolar

Device	I_{IB} (μA) Max	V_{IO} (mV) Max	I_{IO} (nA) Max	A_{vol} (V/mV) Min	Response (μs) Typ	Supply Voltage Single	Supply Voltage Dual	Suffix/ Package
MC3405	0.5	10	50	20	1.3	3.0 to 36	±1.5 to ±18	P/646

MC14573
Quad Programmable Operational Amplifier

MC14575
Dual Programmable Operational Amplifier and Dual Programmable Comparator

MC14576B/MC14577B
Dual Video Amplifiers

Table 6. CMOS

Function	Quantity Per Package	Single Supply Voltage Range	Dual Supply Voltage Range	Frequency Range	Device	Suffix/ Package
Operational Amplifiers	4	3.0 to 15 V	±1.5 to ±7.5 V	DC to 1.0 MHz	MC14573	P/648, D/751B
Operational Amplifiers and Comparators	2 and 2	3.0 to 15 V	±1.5 to ±7.5 V	DC to 1.0 MHz	MC14575	P/648, D/751B
Video Amplifiers	2	5.0 to 12 V(1)	±2.5 to ±6.0 V(2)	Up to 10 MHz	MC14576C MC14577C	P/626, F/904

(1) 5.0 to 10 V for surface mount package.
(2) ±2.5 to ±5.0 V for surface mount package.

Comparators

Table 7. Single Comparators

Device	I_{IB} (µA) Max	V_{IO} (mV) Max	I_{IO} (µA) Max	A_V (V/V) Typ	I_{IO} (mA) Min	Response Time (ns)	Supply Voltage (V)	Description	Temperature Range (°C)	Suffix/ Package
Bipolar										
LM211	0.1	3.0	0.01	200 k	8.0	200	+15, –15	With strobe, will operate from single supply	–25 to +85	D/751
LM311	0.25	7.5	0.05						0 to +70	N/626, D/751
CMOS										
MC14578	1.0 pA	50	–	–	1.1	–	3.5 to 14	Requires only 10 µA from single–ended supply	–30 to +70	P/648, D/751B

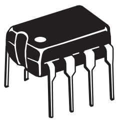
Table 8. Dual Comparators

Device	I_{IB} (µA) Max	V_{IO} (mV) Max	I_{IO} (µA) Max	A_V (V/V) Typ	I_{IO} (mA) Min	Response Time (ns)	Supply Voltage (V)	Description	Temperature Range (°C)	Suffix/ Package
Bipolar										
LM293	0.25	5.0	0.05	200 k	6.0	1300	±1.5 to ±18 or 3.0 to 36	Designed for single or split supply operation, input common mode includes ground (negative supply)	–25 to +85	N/626, D/751
LM393		5.0				1300			0 to +70	
LM393A		2.0				1300			0 to +70	
LM2903		7.0				1500			–40 to +105	
LM2903V		7.0				1500			–40 to +125	
MC3405	0.5	10	0.05	200 k	6.0	1300	±1.5 to ±7.5 or 3.0 to 15	This device contains 2 op amps and 2 comparators in a single package	0 to +70	P/646
CMOS										
MC14575	0.001	30	0.0001	2.0 k	3.0	1000	±1.5 to ±7.5 or 3.0 to 15	This device contains 2 op amps and 2 comparators in a single package	–40 to +85	P/648, D/751B

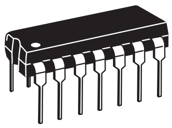
Table 9. Quad Comparators

Device	I_{IB} (µA) Max	V_{IO} (mV) Max	I_{IO} (µA) Max	A_V (V/V) Typ	I_{IO} (mA) Min	Response Time (ns)	Supply Voltage (V)	Description	Temperature Range (°C)	Suffix/ Package
Bipolar										
LM239	0.25	5.0	0.05	200 k	6.0	1300	±1.5 to ±18 or 3.0 to 36	Designed for single or split supply operation, input common mode includes ground (negative supply)	–25 to +85	N/646, D/751A
LM239A		2.0		200 k					–25 to +85	
LM339		5.0		200 k					0 to +70	
LM339A		2.0		200 k					0 to +70	
LM2901		7.0		100 k					–40 to +85	
LM2901V		7.0		100 k					–40 to +125	
MC3302	0.5	20	0.5	100 k					–40 to +85	P/646
MC3431	40	10	1.0 Typ	1.2 k	16	33	+5.0, –5.0	High speed comparator/ sense amplifier	0 to +70	P/648
MC3432		6.0				40				
MC3433		10				40				
CMOS										
MC14574	0.001	30	0.0001	2.0 k	3.0	1000	±1.5 to ±7.5 or 3.0 to 15	Externally programmable power dissipation with 1 or 2 resistors	–40 to +85	P/648, D/751B

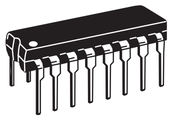
Amplifiers and Comparators Package Overview



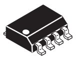
CASE 626
N, P, P1 SUFFIX



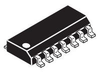
CASE 646
N, P SUFFIX



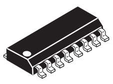
CASE 648, 648C
DP2, P, P2 SUFFIX



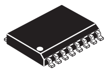
CASE 751
D SUFFIX



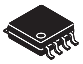
CASE 751A
D SUFFIX



CASE 751B
D SUFFIX



CASE 751G
DW SUFFIX



CASE 904
F SUFFIX

Device Listing and Related Literature

Amplifiers

Amplifiers

Comparators

ADDENDUM

RELATED APPLICATION NOTES

App Note	Title	Related Device
AN587	Analysis and Design of the Op Amp Current Source	**MC1741C**

MOTOROLA

LF347, B
LF351
LF353

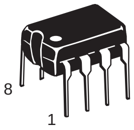
JFET Input Operational Amplifiers

These low cost JFET input operational amplifiers combine two state–of–the–art analog technologies on a single monolithic integrated circuit. Each internally compensated operational amplifier has well matched high voltage JFET input devices for low input offset voltage. The JFET technology provides wide bandwidths and fast slew rates with low input bias currents, input offset currents, and supply currents.

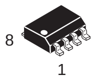
These devices are available in single, dual and quad operational amplifiers which are pin–compatible with the industry standard MC1741, MC1458, and the MC3403/LM324 bipolar devices.

- Input Offset Voltage of 5.0 mV Max (LF347B)
- Low Input Bias Current: 50 pA
- Low Input Noise Voltage: 16 nV/$\sqrt{\text{Hz}}$
- Wide Gain Bandwidth: 4.0 MHz
- High Slew Rate: 13V/µs
- Low Supply Current: 1.8 mA per Amplifier
- High Input Impedance: 10^{12} Ω
- High Common Mode and Supply Voltage Rejection Ratios: 100 dB

FAMILY OF JFET OPERATIONAL AMPLIFIERS

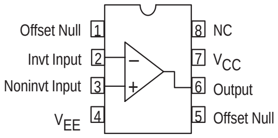


N SUFFIX
PLASTIC PACKAGE
CASE 626

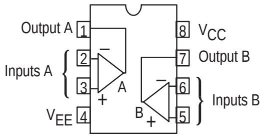


D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

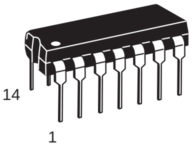
PIN CONNECTIONS



LF351
(Top View)

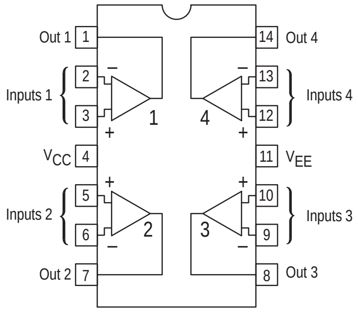


LF353
(Top View)



N SUFFIX
PLASTIC PACKAGE
CASE 646

PIN CONNECTIONS



(Top View)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC} V_{EE}	+18 –18	V
Differential Input Voltage	V_{ID}	±30	V
Input Voltage Range (Note 1)	V_{IDR}	±15	V
Output Short Circuit Duration (Note 2)	t_{SC}	Continuous	
Power Dissipation at T_A = +25°C Derate above T_A =+25°C	P_D $1/\theta_{JA}$	900 10	mW mW/°C
Operating Ambient Temperature Range	T_A	0 to +70	°C
Operating Junction Temperature Range	T_J	115	°C
Storage Temperature Range	T_{stg}	– 65 to +150	°C

NOTES: 1. Unless otherwise specified, the absolute maximum negative input voltage is limited to the negative power supply.
2. Any amplifier output can be shorted to ground indefinitely. However, if more than one amplifier output is shorted simultaneously, maximum junction temperature rating may be exceeded.

ORDERING INFORMATION

Device	Function	Operating Temperature Range	Package
LF351D LF351N	Single Single	T_A = 0° to +70°C	SO–8 Plastic DIP
LF353D LF353N	Dual Dual		SO–8 Plastic DIP
LF347BN LF347N	Quad Quad		Plastic DIP Plastic DIP

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V_{EE} = –15 V, T_A = 25°C, unless otherwise noted.)

Characteristic	Symbol	LF347B			LF347, LF351, LF353			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage (R_S ≤ 10 k, V_{CM} = 0)	V_{IO}							mV
T_A = +25°C		–	1.0	5.0	–	5.0	10	
0°C ≤ T_A ≤ +70°C		–	–	8.0	–	–	13	
Avg. Temperature Coefficient of Input Offset Voltage	$\Delta V_{IO}/\Delta T$							µV/°C
R_S ≤ 10 k, 0°C ≤ T_A ≤ +70°C		–	10	–	–	10	–	
Input Offset Current (V_{CM} = 0, Note 3)	I_{IO}							
T_A = +25°C		–	25	100	–	25	100	pA
0°C ≤ T_A ≤ +70°C		–	–	4.0	–	–	4.0	nA
Input Bias Current (V_{CM} = 0, Note 3)	I_{IB}							
T_A = +25°C		–	50	200	–	50	200	pA
0°C ≤ T_A ≤ +70°C		–	–	8.0	–	–	8.0	nA
Input Resistance	r_i	–	10^{12}	–	–	10^{12}	–	Ω
Common Mode Input Voltage Range	V_{ICR}	±11	+15 –12	–	±11	+15 –12	–	V
Large–Signal Voltage Gain (V_O = ±10 V, R_L = 2.0 k)	A_{VOL}							V/mV
T_A = +25°C		50	100	–	25	100	–	
0°C ≤ T_A ≤ +70°C		25	–	–	15	–	–	
Output Voltage Swing (R_L = 10 k)	V_O	±12	±14	–	±12	±14	–	V
Common Mode Rejection (R_S ≤ 10 k)	CMR	80	100	–	70	100	–	dB
Supply Voltage Rejection (R_S ≤ 10 k)	PSRR	80	100	–	70	100	–	dB
Supply Current	I_D							mA
LF347		–	7.2	11	–	7.2	11	
LF351		–	–	–	–	1.8	3.4	
LF353		–	–	–	–	3.6	6.5	
Short Circuit Current	I_{SC}	–	25	–	–	25	–	mA
Slew Rate (A_V = +1)	SR	–	13	–	–	13	–	V/µs
Gain–Bandwidth Product	BWp	–	4.0	–	–	4.0	–	MHz
Equivalent Input Noise Voltage (R_S = 100 Ω, f = 1000 Hz)	e_n	–	24	–	–	24	–	$nV/\sqrt{Hz}$
Equivalent Input Noise Current (f = 1000 Hz)	i_n	–	0.01	–	–	0.01	–	$pA/\sqrt{Hz}$
Channel Separation (LF347, LF353) 1.0 Hz ≤ f ≤ 20 kHz (Input Referred)	–	–	–120	–	–	–120	–	dB

For Typical Characteristic Performance Curves, refer to MC34001, 34002, 34004 data sheet.

NOTE: 3. Input bias currents of JFET input op amps approximately double for every 10°C rise in junction temperature. To maintain junction temperatures as close to ambient as is possible, pulse techniques are utilized during test.

MOTOROLA

LF411C
LF412C

Low Offset, Low Drift JFET Input Operational Amplifiers

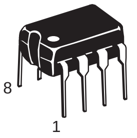
Through innovative design concepts and precision matching this monolithic high speed JFET input operational amplifier family offers very low input offset voltage as well as low temperature coefficient of input offset voltage. The amplifier requires less than 3.4 mA per amplifier of supply current yet exhibits greater than 2.7 MHz of gain bandwidth product and more than 8.0 V/µs slew rate. Through the use of JFET inputs the amplifier has very low input bias currents and low input offset currents. The amplifier utilizes industry standard pinouts which afford the user the opportunity to directly upgrade circuit performance without the need for redesign.

The LF411C and LF412C are available in the industry standard plastic 8–pin DIP and SO–8 surface mount packages, and specified over the commercial temperature range.

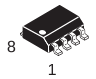
- Low Input Offset Voltage: 2.0 mV Max (Single)
  3.0 mV Max (Dual)
- Low T.C. of Input Offset Voltage: 10 µV/°C
- Low Input Offset Current: 20 pA
- Low Input Bias Current: 60 pA
- Low Input Noise Voltage: 18 nV/$\sqrt{Hz}$
- Low Input Noise Current: 0.01 pA/$\sqrt{Hz}$
- Low Total Harmonic Distortion: 0.05%
- Low Supply Current: 2.5 mA
- High Input Resistance: 10^{12} Ω
- Wide Gain Bandwidth: 8.0 MHz
- High Slew Rate: 25 V/µs (Typ)
- Fast Settling Time: 1.6 µs (to within 0.01%)
- Internally Compensated

SINGLE/DUAL JFET OPERATIONAL AMPLIFIERS

SEMICONDUCTOR TECHNICAL DATA



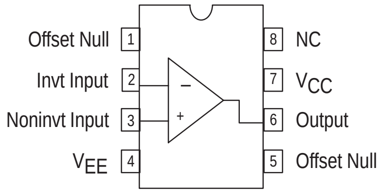
N SUFFIX
PLASTIC PACKAGE
CASE 626



D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

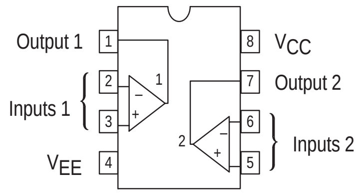
PIN CONNECTIONS

LF411C



(Single, Top View)

LF412C



(Dual, Top View)

ORDERING INFORMATION

Device	Function	Operating Temperature Range	Package
LF411CD	Single	T_A = 0° to +70°C	SO–8
LF411CN			Plastic DIP
LF412CD	Dual		SO–8
LF412CN			Plastic DIP

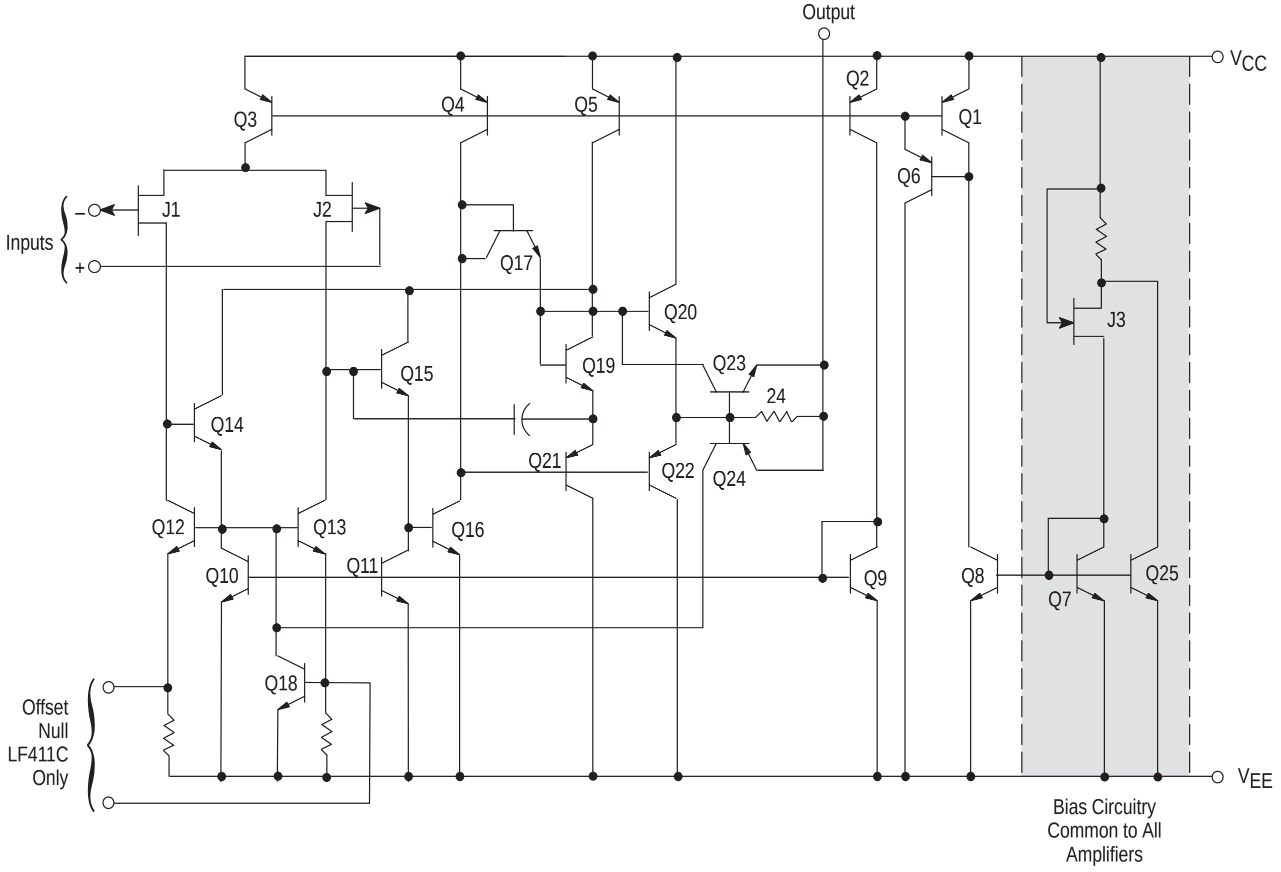
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltages	V_{CC}, $\lvert V_{EE} \rvert$	+18	V
Input Differential Voltage Range (Note 1)	V_{IDR}	±30	V
Input Voltage Range (Note 1)	V_{IR}	±15	V
Output Short Circuit Duration (Note 2)	t_{SC}	Indefinite	sec
Maximum Junction Temperature	T_J	+150	°C
Operating Ambient Temperature Range	T_A	0 to 70	°C
Thermal Resistance (Junction–to–Ambient) LF411CN/412CN LF411CD/412CD	$R_{\theta JA}$	100 180	°C/W
Storage Temperature	T_{stg}	–60 to +150	°C
Maximum Power Dissipation	P_D	(Note 2)	mW

NOTES: 1. Input voltages should not exceed V_{CC} or V_{EE}.
2. Power dissipation must be considered to ensure maximum junction temperature (T_J) is not exceeded.

Representative Schematic Diagram

(Each Amplifier)



ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = –15 V, T_A = 0° to 70°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Offset Voltage (R_S = 10 k Ω, V_{CM} = 0 V, V_O = 0 V)	$\|V_{IO}\|$				mV
LF411		–	0.5	2.0	
LF412		–	1.0	3.0	
Average Temperature Coefficient of Input Offset Voltage	$\Delta V_{IO}\ \Delta T$				µV/°C
(R_S = 10 k Ω, V_{CM} = 0 V, V_O = 0 V)		–	10	–	
Input Offset Current (V_{CM} = 0 V, V_O = 0 V)	I_{IO}				
LF411 T_A = 25°C		–	20	100	pA
T_A = 0° to 70°C		–	–	2.0	nA
LF412 T_A = 25°C		–	25	100	pA
T_A = 0° to 70°C		–	–	2.0	nA
Input Bias Current (V_{CM} = 0 V, V_O = 0 V)	I_{IB}				
LF411 T_A = 25°C		–	0.6	200	pA
T_A = 0° to 70°C		–	–	4.0	nA
LF412 T_A = 25°C		–	0.5	200	pA
T_A = 0° to 70°C		–	–	4.0	nA
Large Signal Voltage Gain (V_O = ±10 V, R_L = 2.0 k Ω)	A_{VOL}				V/mV
LF411 T_A = 25°C		25	80	–	
T_A = 0° to 70°C		15	–	–	
LF412 T_A = 25°C		25	150	–	
T_A = 0° to 70°C		15	–	–	
Output Voltage Swing (V_{ID} = ±1.0 V, R_L = 10 kΩ)					V
LF411	V_O +	+12	+13.9	–	
	V_O –	–	–14.7	–12	
LF412	V_O +	+12	+14.0	–	
	V_O –	–	–14.0	–12	
Common Mode Input Voltage Range (V_O = 0 V)	V_{ICR}				V
LF411		+11	+14	–11	
		–	–14	–	
LF412		+11	+15	–11	
		–	–12	–	
Common Mode Rejection (V_{CM} = ±11 V, R_S ≤ 10 k Ω)	CMR				dB
LF411		70	90	–	
LF412		70	100	–	
Power Supply Rejection (Note 3)	PSR				dB
(V_{CC} V_{EE} = +15 V, –15 V to +5.0 V, –5.0 V)					
LF411		70	86	–	
LF412		70	100	–	
Power Supply Current (V_O = 0 V)	I_D				mA
LF411		–	2.5	3.4	
LF412		–	2.8	6.8	

NOTE: 3. Measured with V_{CC} and V_{EE} simultaneously varied.

AC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = –15 V, T_A = 25°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Slew Rate (V_{in} = –10 V to +10 V, R_L = 2.0 k Ω, A_V = +1.0)	SR				V/µs
LF411		8.0	25	–	
LF412		8.0	13	–	
Gain Bandwidth Product	GBW				MHz
LF411		2.7	8.0	–	
LF412		2.7	4.0	–	
Channel Separation (f = 1.0 Hz to 20 kHz, LF412)	CS	–	–120	–	dB
Differential Input Resistance (V_{CM} = 0 V)	R_{in}	–	10^{12}	–	kΩ
Equivalent Input Voltage Noise (R_S = 100 Ω, f = 1.0 kHz)	e_n				$nV/\sqrt{Hz}$
LF411		–	30	–	
LF412		–	25	–	
Equivalent Input Noise Current (f = 1.0 kHz)	i_n				$pA/\sqrt{Hz}$
LF411		–	0.01	–	
LF412		–	0.01	–	

MOTOROLA

LF441C
LF442C
LF444C

Low Power JFET Input Operational Amplifiers

LOW POWER
JFET INPUT
OPERATIONAL AMPLIFIERS

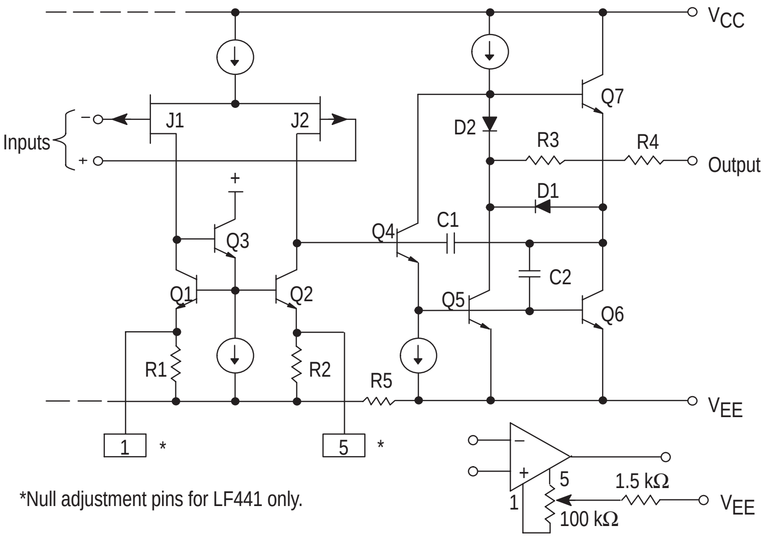
SEMICONDUCTOR
TECHNICAL DATA

These JFET input operational amplifiers are designed for low power applications. They feature high input impedance, low input bias current and low input offset current. Advanced design techniques allow for higher slew rates, gain bandwidth products and output swing. The LF441C device provides for the external null adjustment of input offset voltage.

These devices are specified over the commercial temperature range. All are available in plastic dual in–line and SOIC packages.

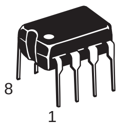
- Low Supply Current: 200 µA/Amplifier
- Low Input Bias Current: 5.0 pA
- High Gain Bandwidth: 2.0 MHz
- High Slew Rate: 6.0 V/µs
- High Input Impedance: 10^{12} Ω
- Large Output Voltage Swing: ±14 V
- Output Short Circuit Protection

Representative Schematic Diagram
(Each Amplifier)

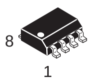


*Null adjustment pins for LF441 only.

LF441C input offset voltage
null adjust circuit

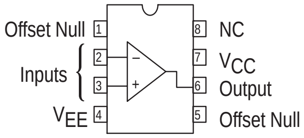


N SUFFIX
PLASTIC PACKAGE
CASE 626

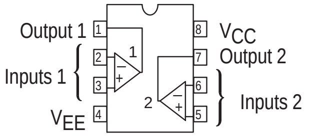


D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

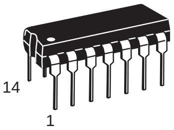
PIN CONNECTIONS



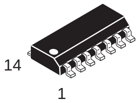
(Single, Top View)



(Dual, Top View)

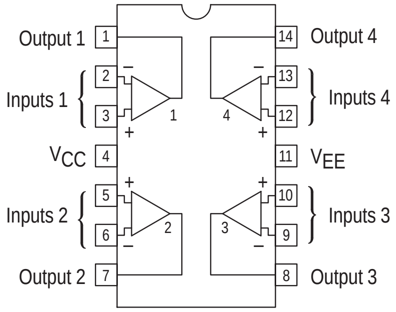


N SUFFIX
PLASTIC PACKAGE
CASE 646



D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO–14)

PIN CONNECTIONS



(Quad, Top View)

ORDERING INFORMATION

Device	Function	Operating Temperature Range	Package
LF441CD LF441CN	Single	T_A = 0° to +70°C	SO–8 Plastic DIP
LF442CD LF442CN	Dual		SO–8 Plastic DIP
LF444CD LF444CN	Quad		SO–14 Plastic DIP

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage (from V_{CC} to V_{EE})	V_S	+36	V
Input Differential Voltage Range (Note 1)	V_{IDR}	±30	V
Input Voltage Range (Notes 1 and 2)	V_{IR}	±15	V
Output Short Circuit Duration (Note 3)	t_{SC}	Indefinite	sec
Operating Junction Temperature (Note 3)	T_J	+150	°C
Storage Temperature Range	T_{stg}	–60 to +150	°C

NOTES:
1. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
2. The magnitude of the input voltage must never exceed the magnitude of the supply or 15 V, whichever is less.
3. Power dissipation must be considered to ensure maximum junction temperature (T_J) is not exceeded (see Figure 1).

DC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = –15 V, T_A = 0° to 70°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Offset Voltage (R_S = 10 kΩ, V_O = 0 V)	V_{IO}				mV
Single: T_A = +25°C		–	3.0	5.0	
T_A = 0° to +70°C		–	–	7.5	
Dual: T_A = +25°C		–	3.0	5.0	
T_A = 0° to +70°C		–	–	7.5	
Quad: T_A = +25°C		–	3.0	10	
T_A = 0° to +70°C		–	–	12	
Average Temperature Coefficient of Offset Voltage (R_S = 10 kΩ, V_O = 0 V)	$\Delta V_{IO}/\Delta T$	–	10	–	µV/°C
Input Offset Current (V_{CM} = 0 V, V_O = 0 V)	I_{IO}				
T_A = +25°C		–	0.5	50	pA
T_A = 0° to +70°C		–	–	1.5	nA
Input Bias Current (V_{CM} = 0 V, V_O = 0 V)	I_{IB}				
T_A = +25°C		–	3.0	100	pA
T_A = 0° to +70°C		–	–	3.0	nA
Common Mode Input Voltage Range (T_A = +25°C)	V_{ICR}	–	+14.5	+11	V
		–11	–12	–	
Large Signal Voltage Gain (V_O = ±10 V, R_L = 10 kΩ)	A_{VOL}				V/mV
T_A = +25°C		25	60	–	
T_A = 0° to +70°C		15	–	–	
Output Voltage Swing (R_L = 10 kΩ)	V_O +	+12	+14	–	V
	V_O –	–	–14	–12	
Common Mode Rejection (R_S ≤ 10 kΩ, V_{CM} = V_{ICR}, V_O = 0 V)	CMR	70	86	–	dB
Power Supply Rejection (R_S = 100 Ω, V_{CM} = 0 V, V_O = 0 V)	PSR	70	84	–	dB
Power Supply Current (No Load, V_O = 0 V)	I_D				µA
Single		–	200	250	
Dual		–	400	500	
Quad		–	800	1000	

AC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = –15 V, T_A = +25°C, unless otherwise noted.)

Characteristic		Symbol	Min	Typ	Max	Unit
Slew Rate (V_{in} = –10 V to +10 V, R_L = 10 kΩ, C_L = 10 pF, A_V = +1.0)		SR	0.6	6.0	–	V/ µs
Settling Time (A_V = –1.0, R_L = 10 kΩ, V_O = 0 V to +10 V)	To within 10 mV To within 1.0 mV	t_S	– –	1.6 2.2	– –	µs
Gain Bandwidth Product (f = 200 kHz)		GBW	0.6	2.0	–	MHz
Equivalent Input Noise Voltage (R_S = 100 Ω, f = 1.0 kHz)		e_n	–	47	–	$nV/\sqrt{Hz}$
Equivalent Input Noise Current (f = 1.0 kHz)		i_n	–	0.01	–	$pA/\sqrt{Hz}$
Input Resistance		R_i	–	10^{12}	–	Ω
Channel Separation (f = 1.0 Hz to 20 kHz)		CS	–	120	–	dB

Figure 1. Maximum Power Dissipation versus Temperature for Package Variations

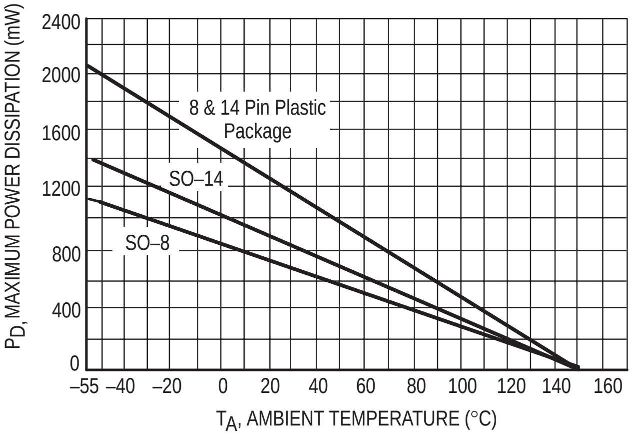


Figure 2. Input Bias Current versus Input Common Mode Voltage

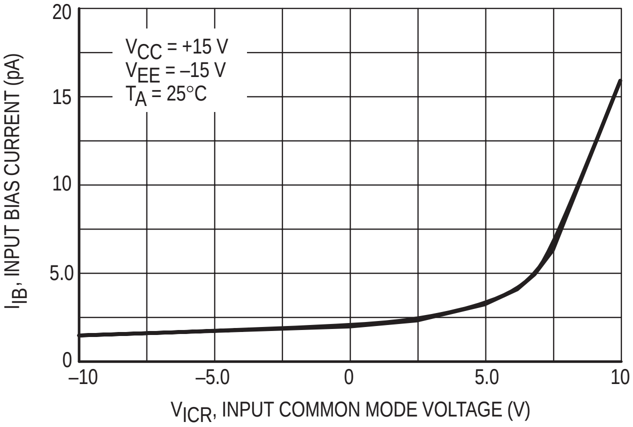


Figure 3. Input Bias Current versus Temperature

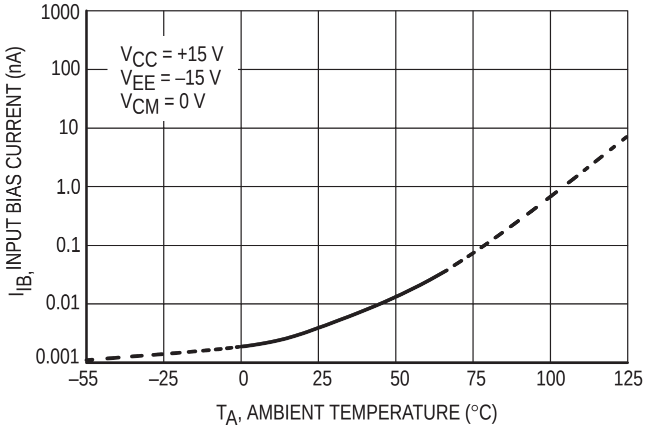


Figure 4. Supply Current versus Supply Voltage

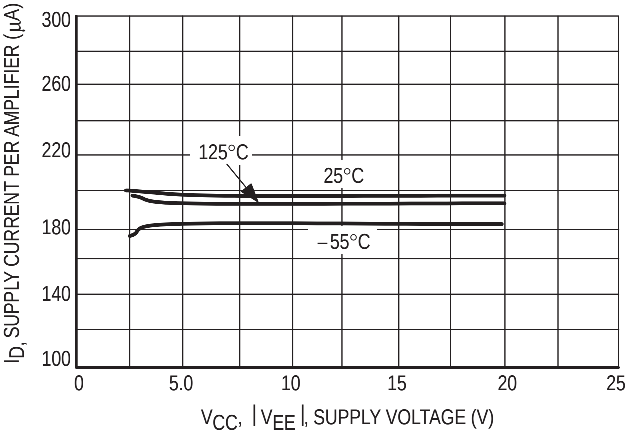


Figure 5. Positive Input Common Mode Voltage Range versus Positive Supply Voltage

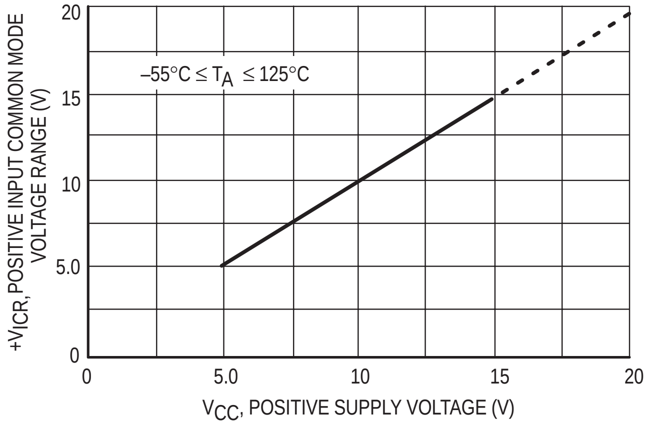


Figure 6. Negative Input Common Mode Voltage Range versus Negative Supply Voltage

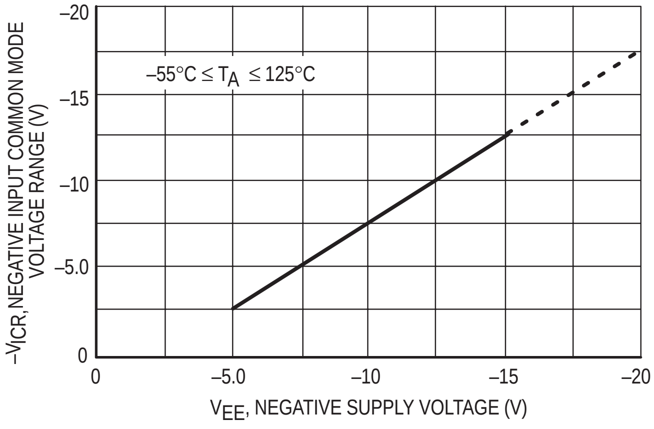


Figure 7. Output Voltage versus Output Source Current

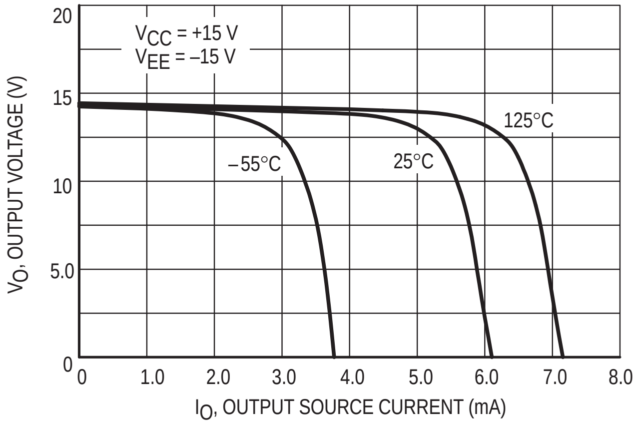


Figure 8. Output Voltage versus Output Sink Current

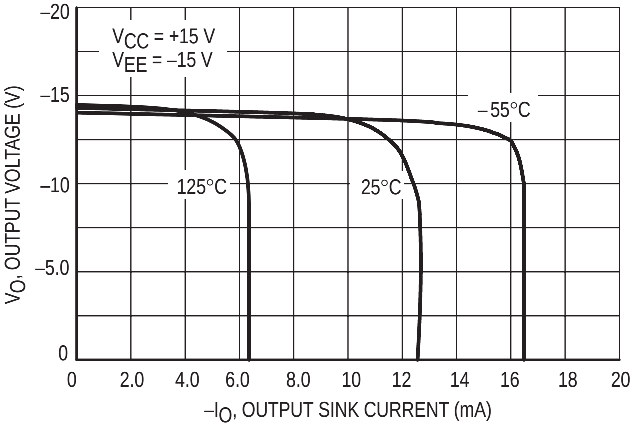


Figure 9. Output Voltage Swing versus Supply Voltage

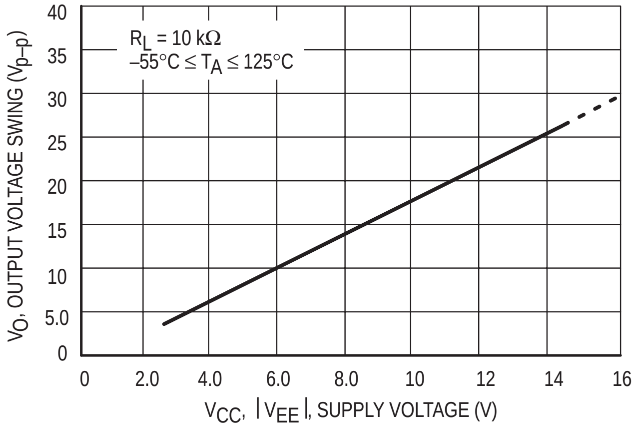


Figure 10. Output Voltage Swing versus Load Resistance

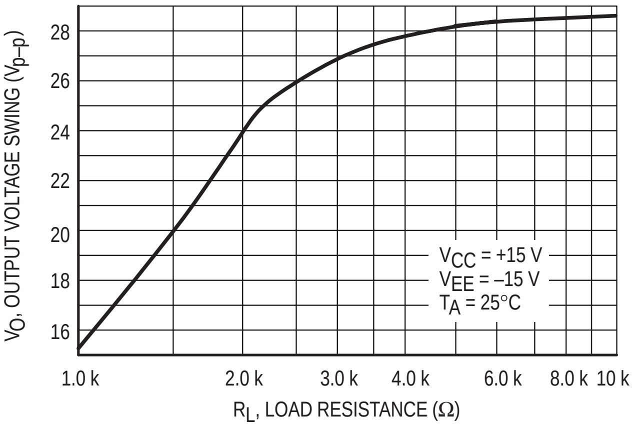


Figure 11. Normalized Gain Bandwidth Product versus Temperature

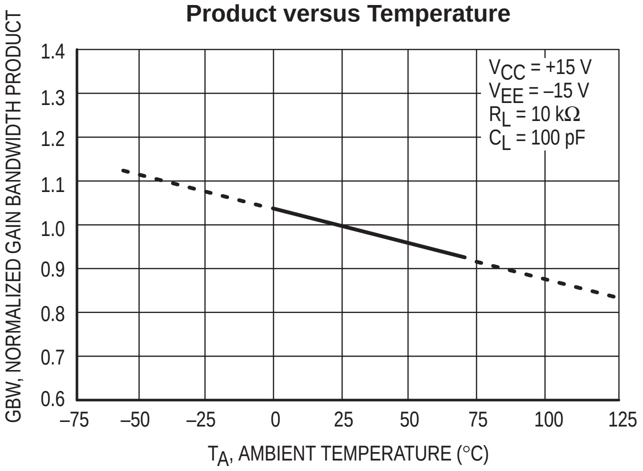


Figure 12. Open Loop Voltage Gain and Phase versus Frequency

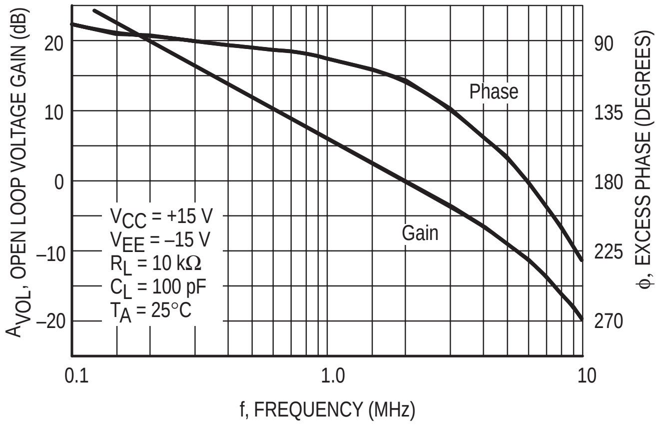


Figure 13. Slew Rate versus Temperature

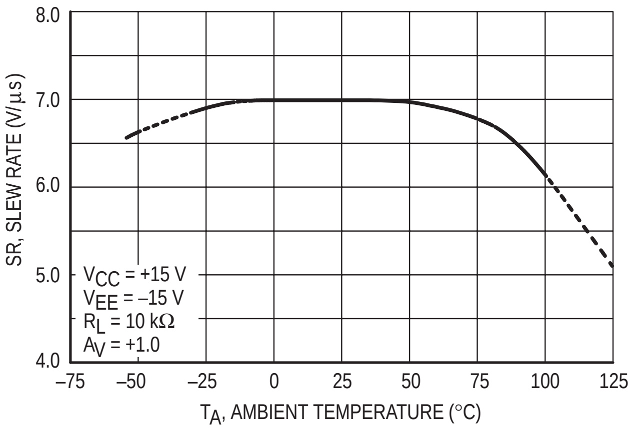


Figure 14. Total Output Distortion versus Frequency

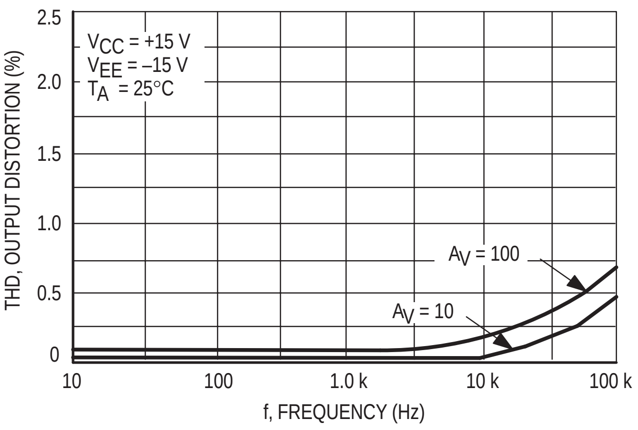


Figure 15. Output Voltage Swing versus Frequency

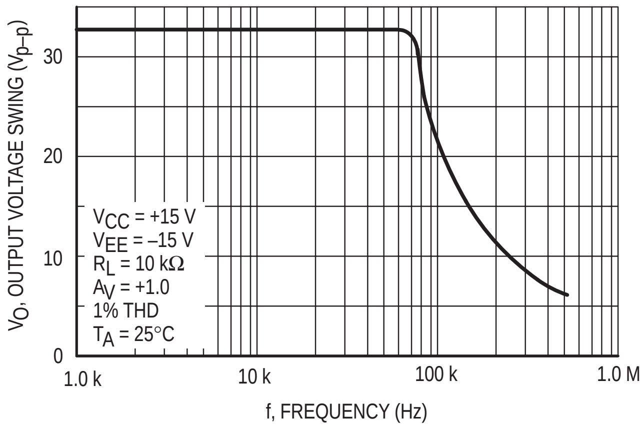
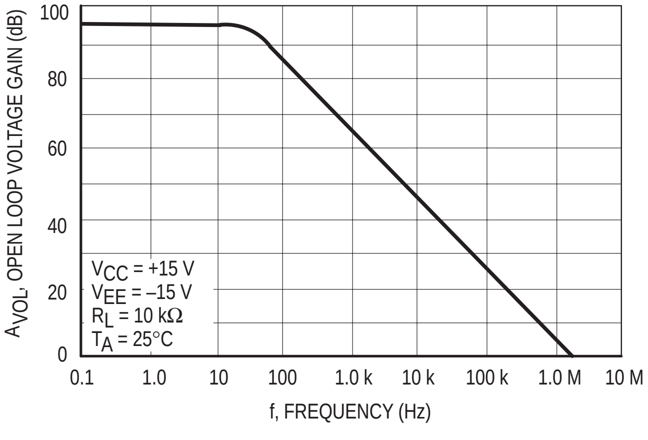


Figure 16. Open Loop Voltage Gain versus Frequency



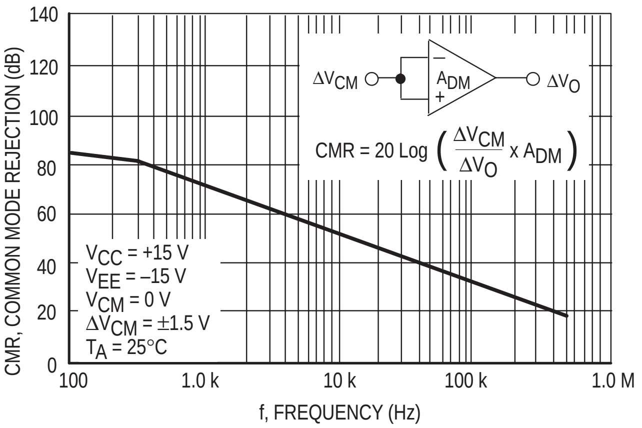


Figure 17. Common Mode Rejection versus Frequency

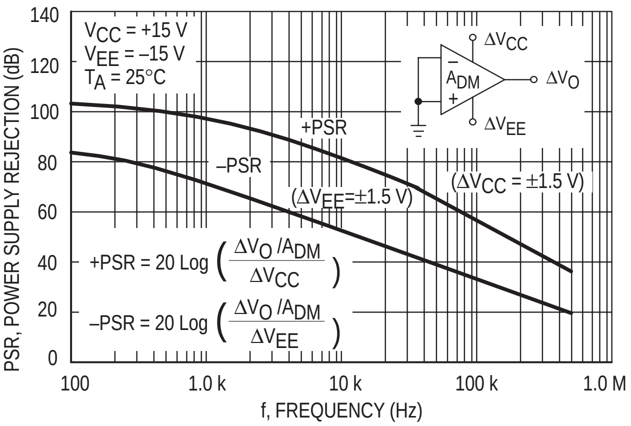


Figure 18. Power Supply Rejection versus Frequency

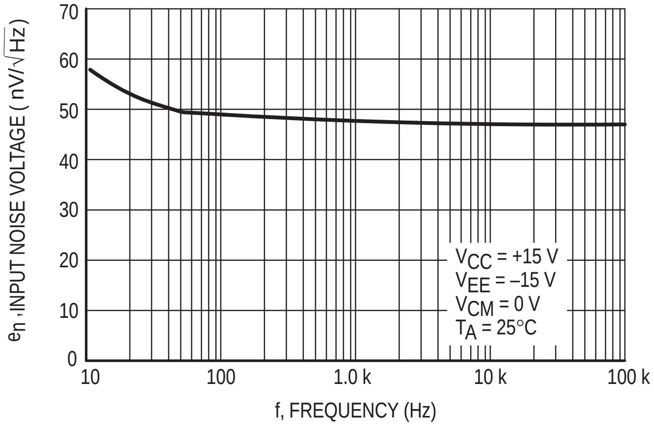


Figure 19. Input Noise Voltage versus Frequency

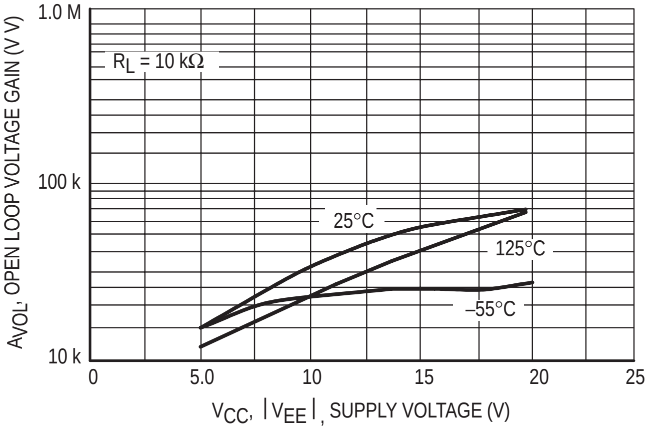


Figure 20. Open Loop Voltage Gain versus Supply Voltage

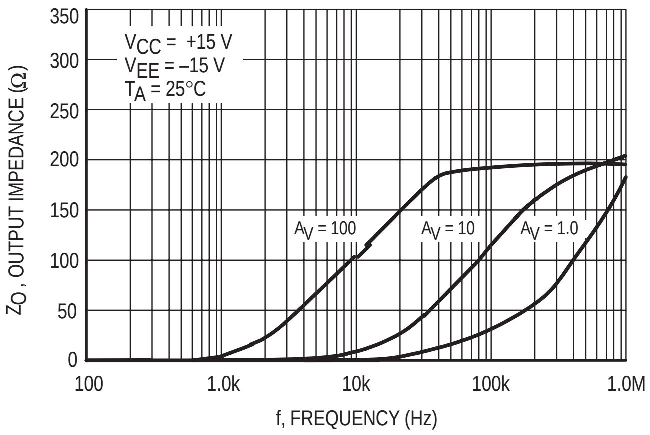


Figure 21. Output Impedance versus Frequency

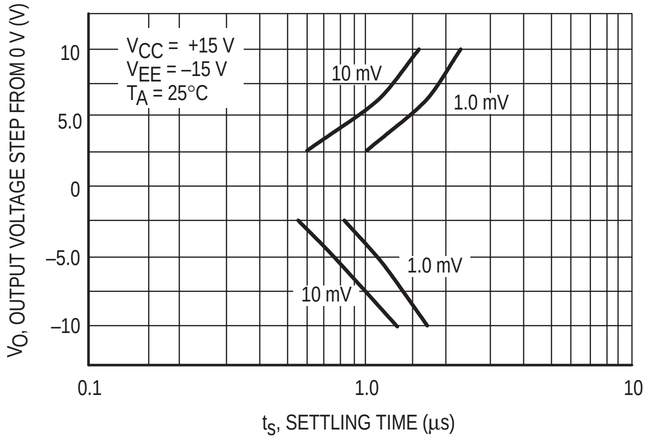


Figure 22. Inverter Settling Time

SMALL SIGNAL RESPONSE

Figure 23. Inverting

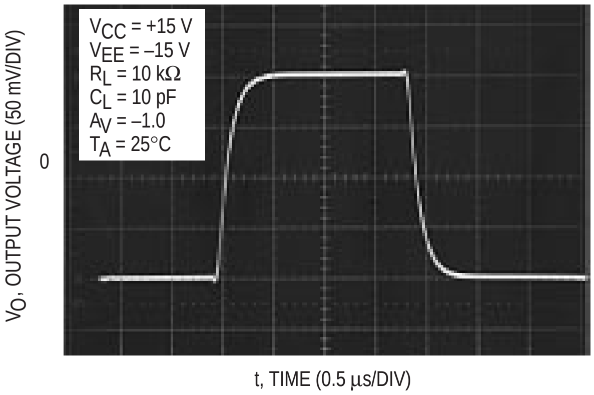
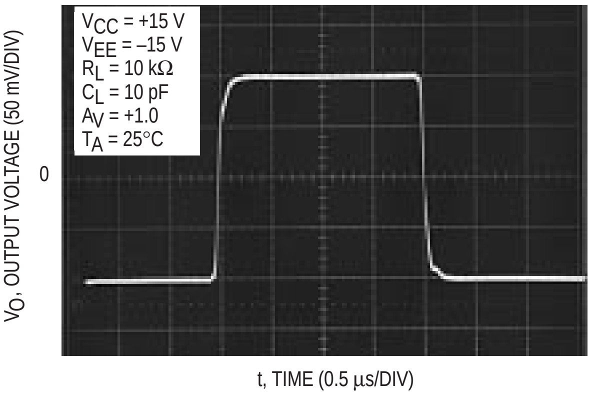


Figure 24. Noninverting



LARGE SIGNAL RESPONSE

Figure 25. Inverting

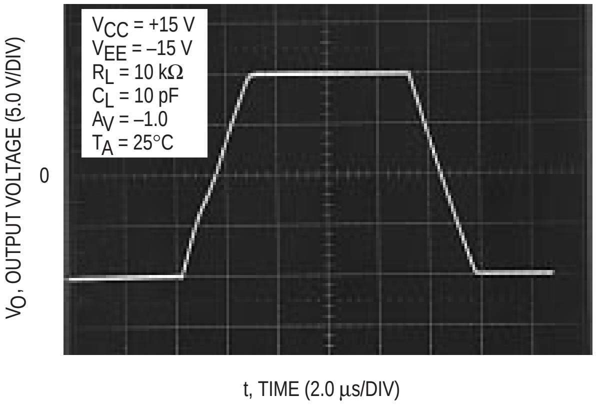
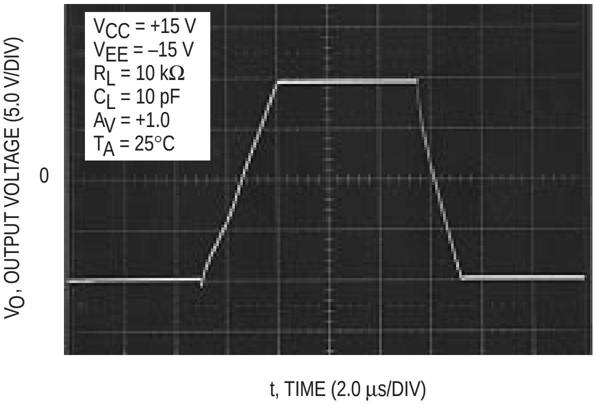


Figure 26. Noninverting



MOTOROLA

LM11C, CL

Precision Operational Amplifiers

PRECISION OPERATIONAL AMPLIFIERS

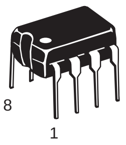
SEMICONDUCTOR TECHNICAL DATA

The LM11C is a precision, low drift operational amplifier providing the best features of existing FET and Bipolar op amps. Implementation of super gain transistors allows reduction of input bias currents by an order of magnitude over earlier devices such as the LM308A. Offset voltage and drift have also been reduced. Although bandwidth and slew rate are not as great as FET devices, input offset voltage, drift and bias current are inherently lower, particularly over temperature. Power consumption is also much lower, eliminating warm–up stabilization time in critical applications.

Offset balancing is provided, with the range determined by an external low resistance potentiometer. Compensation is provided internally, but external compensation can be added for improved stability when driving capacitive loads.

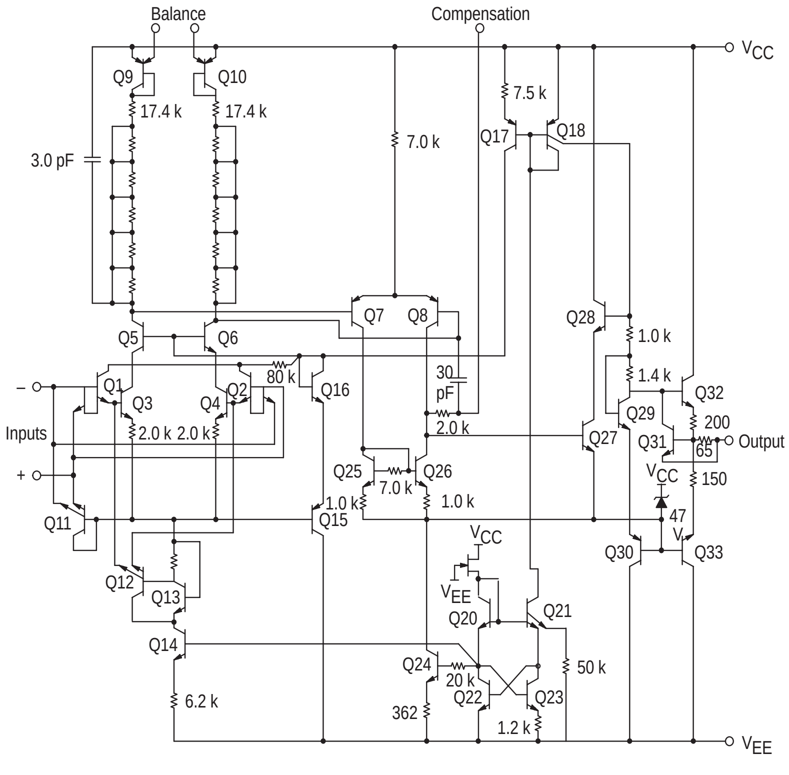
The precision characteristics of the LM11C make this device ideal for applications such as charge integrators, analog memories, electrometers, active filters, light meters and logarithmic amplifiers.

- Low Input Offset Voltage: 100 µV
- Low Input Bias Current: 17 pA
- Low Input Offset Current: 0.5 pA
- Low Input Offset Voltage Drift: 1.0 µV/°C
- Long–Term Stability: 10 µV/year
- High Common Mode Rejection: 130 dB

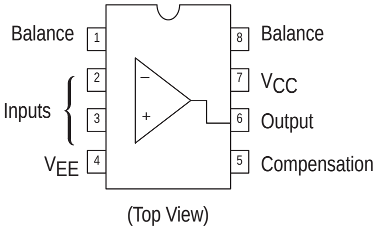


N SUFFIX
PLASTIC PACKAGE
CASE 626

Representative Schematic Diagram



PIN CONNECTIONS



ORDERING INFORMATION

Device	Operating Temperature Range	Package
LM11CN,CLN	T_A = 0° to +70°C	Plastic DIP

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC} to V_{EE}	40	Vdc
Differential Input Current (Note 1)	I_{ID}	±10	mA
Output Short Circuit Duration (Note 2)	t_{SC}	Indefinite	
Power Dissipation (Note 3)	P_D	500	mW
Operating Junction Temperature	T_J	85	°C
Storage Temperature Range	T_{stg}	–55 to +125	°C

ELECTRICAL CHARACTERISTICS (T_J = 25°C, unless otherwise noted [Note 4] .)

Characteristic	Symbol	Min	Typ	Max	Min	Typ	Max	Unit
Input Offset Voltage T_{low} to T_{high}	V_{IO}	– –	0.2 –	0.6 0.8	– –	0.5 –	5.0 6.0	mV
Input Offset Current T_{low} to T_{high}	I_{IO}	– –	1.0 –	10 20	– –	4.0 –	25 50	pA
Input Bias Current T_{low} to T_{high}	I_{IB}	– –	17 –	100 150	– –	17 –	200 300	pA
Input Resistance	r_i	–	10^{11}	–	–	10^{11}	–	Ω
Input Offset Voltage Drift T_{low} to T_{high}	$\Delta V_{IO}/\Delta T$	–	2.0	5.0	–	3.0	–	µV/°C
Input Offset Current Drift T_{low} to T_{high}	$\Delta I_{IO}/\Delta T$	–	10	–	–	50	–	ƒA/°C
Input Bias Current Drift T_{low} to T_{high}	$\Delta I_{IB}/\Delta T$	–	0.8	3.0	–	1.4	–	pA/°C
Large Signal Voltage Gain V_S = ±15 V, V_{out} = ±12 V, I_{out} = ±2.0 mA T_{low} to T_{high} (Note 5) V_S = ±15 V, V_{out} = ±12 V, I_{out} = ±0.5 mA T_{low} to T_{high}	A_{VOL}	 100 50 250 100	 300 – 1200 –	 – – – –	 25 15 50 30	 300 – 800 –	 – – – –	V/mV
Common Mode Rejection V_S = ±15 V, –13 V ≤ V_{CM} ≤ 14 V V_S = ±15 V, –12.5 V ≤ V_{CM} ≤ 14 V, T_{low} to T_{high}	CMR	 110 100	 130 –	 – –	 96 90	 110 –	 – –	dB
Power Supply Rejection ±2.5 V ≤ V_S ≤ ±20 V T_{low} to T_{high}	PSR	 100 96	 118 –	 – –	 84 80	 100 –	 – –	dB
Power Supply Current T_{low} to T_{high}	I_D	– –	0.3 –	0.8 1.0	– –	0.3 –	0.8 1.0	mA
Output Short Circuit Current T_J = 150°C, Output Shorted to Ground	I_{SC}	–	±10	–	–	±10	–	mA

NOTES:
1. The inputs are shunted by back–to–back diodes for over–voltage protection. Excessive current will flow if the input differential voltage is in excess of 1.0 V if no limiting resistance is used. Additionally, a 2.0 kΩ resistance in each input is suggested to prevent possible latch–up initiated by supply reversals.
2. The output is current limited when shorted to ground or any voltages less than the supplies. Continuous overloads will require package dissipation to be considered and heatsinking should be provided when necessary.
3. Devices must be derated based on package thermal resistance (see package outline dimensions).
4. These specifications apply for V_{EE} +2.0 V ≤ V_{CM} ≤ V_{CC} –1.0 V (V_{EE} +2.5 V ≤ V_{CM} ≤ V_{CC} –1.0 V for T_{low} to T_{high}) and ±2.5 V ≤ V_S ≤ ±20 V T_{low} to T_{high}: 0°C ≤ T_J ≤ +70°C for LM11C and LM11C.
5. V_{out} = ±11.5 V, all other conditions unchanged.

Figure 1. Input Bias Current versus Case Temperature

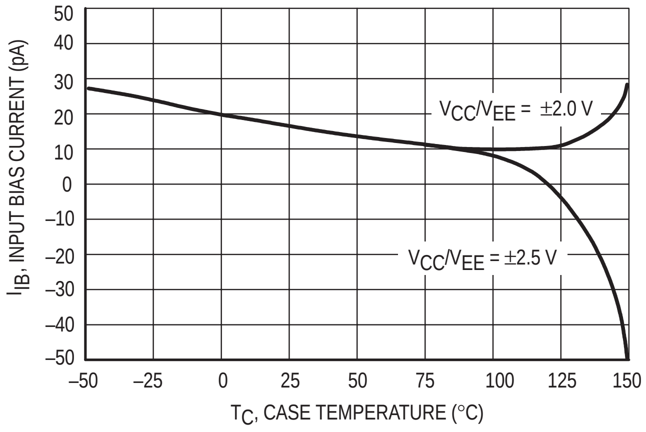


Figure 2. Input Offset Current versus Case Temperature

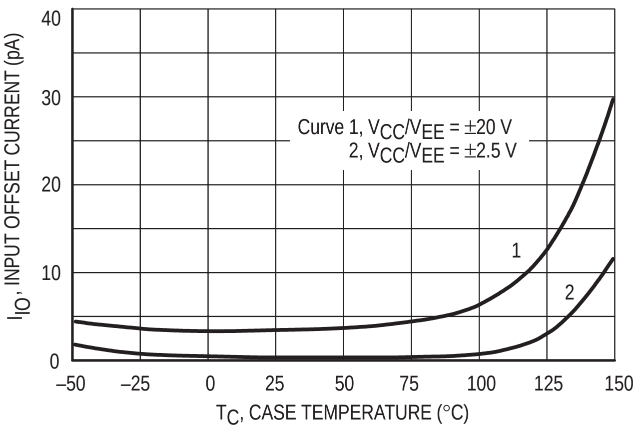


Figure 3. Temperature Coefficient of Input Offset Voltage versus Input Offset Voltage

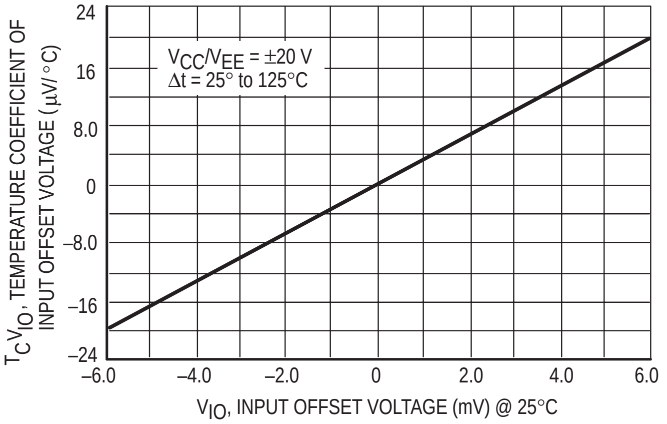


Figure 4. Spectral Noise Density

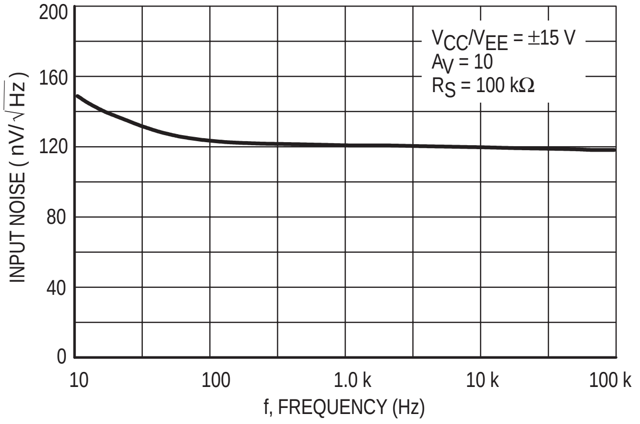


Figure 5. Common Mode Limits versus Temperature

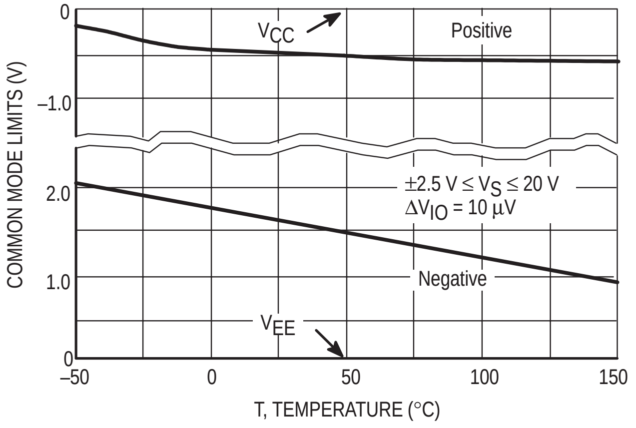


Figure 6. Common Mode Rejection and Slew Limit versus Frequency

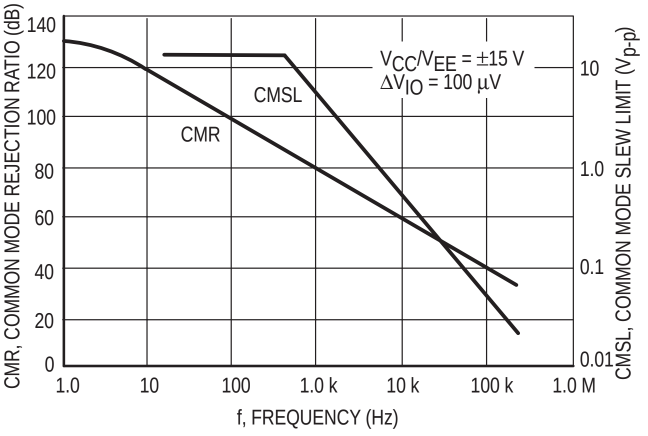


Figure 7. Open Loop Voltage Gain versus Supply Voltage

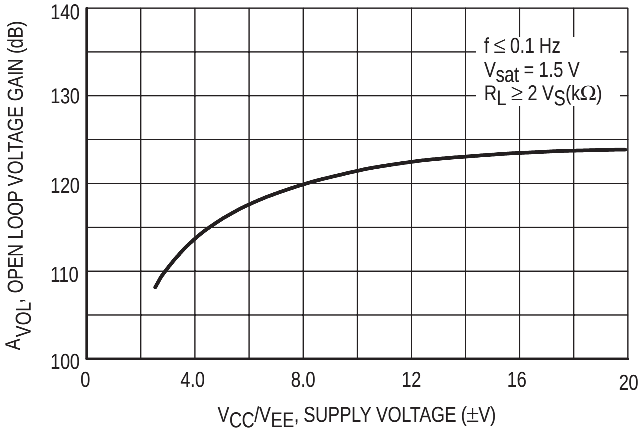


Figure 8. Output Saturation versus Load Current

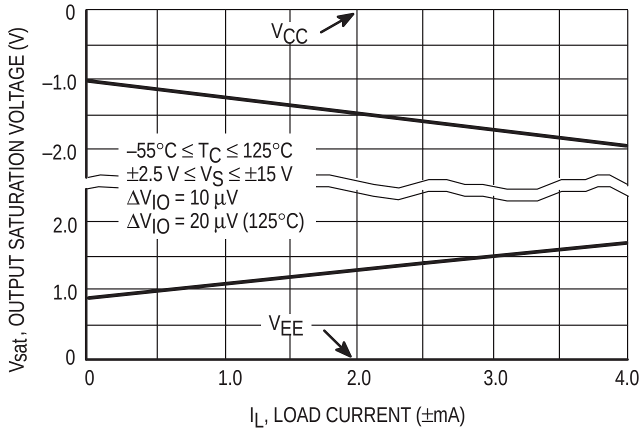


Figure 9. Power Supply Rejection Ratio versus Frequency

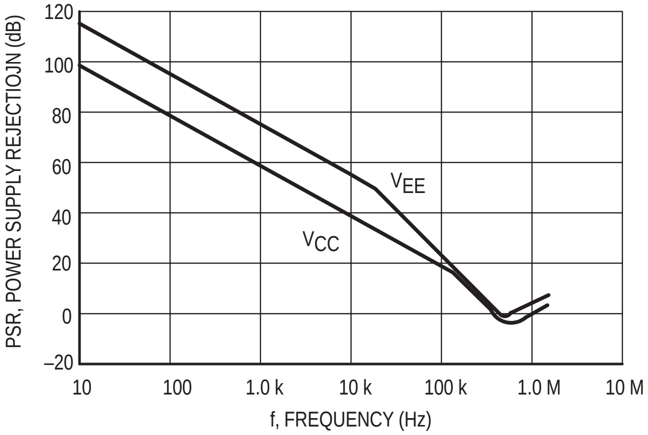


Figure 10. Supply Current versus Supply Voltage

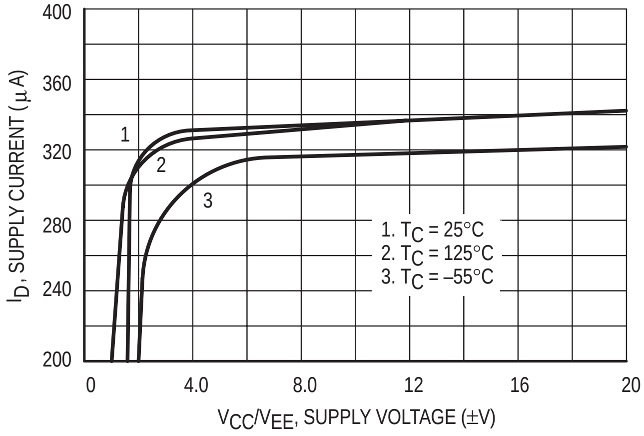


Figure 11. Open Loop Voltage Gain and Phase versus Frequency

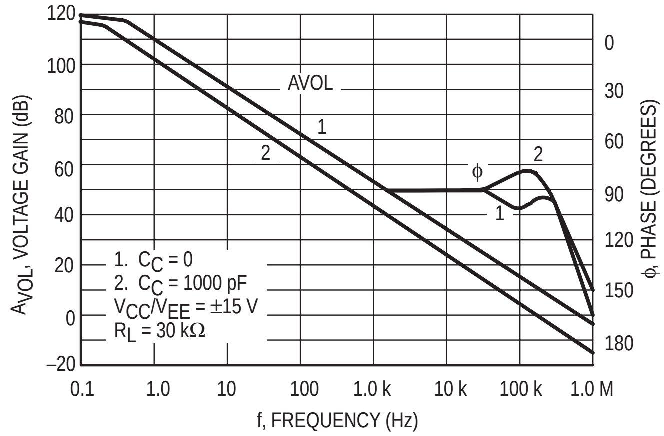


Figure 12. Slew Rate versus External Compensation Capacitor

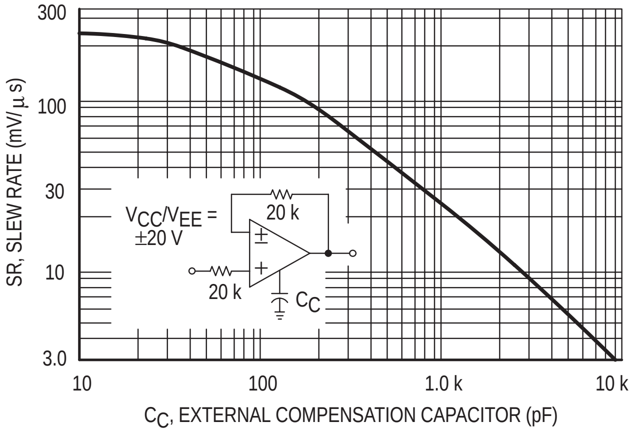
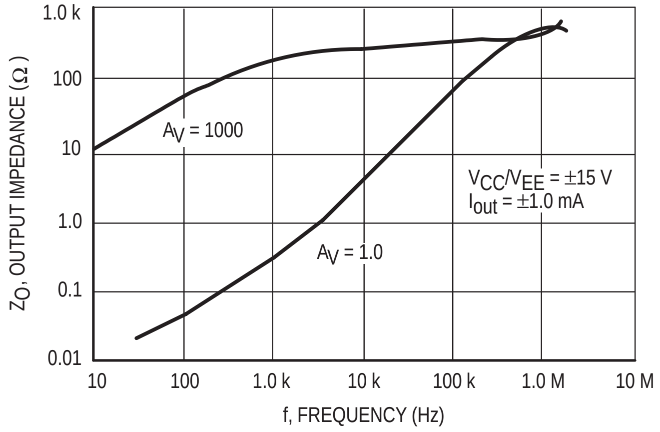


Figure 13. Closed Loop Output Impedance versus Frequency



APPLICATIONS INFORMATION

Due to the extremely low input bias currents of this device, it may be tempting to remove the bias current compensation resistor normally associated with a summing amplifier configuration. Direct connection of the inputs to a low impedance source or ground should be avoided when supply voltages greater than approximately 3.0 V are used. The potential problem involves reversal of one supply which can cause excessive current to flow in the second supply. Possible destruction of the IC could result if the second supply is not current limited to approximately 100 mA or if bypass capacitors greater than 1.0 µF are used in the supply bus.

Disconnecting one supply will generally cause reversal due to loading of the other supply within the IC and in external circuitry. Although the problem can usually be avoided by placing clamp diodes across the power supplies of each printed circuit board, a careful design will include sufficient resistance in the input leads to limit the current to 10 mA if the input leads are pulled to either supply by internal currents. This precaution is not limited only to the LM11C.

The LM11C is capable of resolving picoampere level signals. Leakage currents external to the IC can severely impair the performance of the device. It is important that high quality insulating materials such as teflon be employed. Proper cleaning to remove fluxes and other residues from printed circuit boards, sockets and the device package are necessary to minimize surface leakage.

When operating in high humidity environments or temperatures near 0°C, a surface coating is suggested to set up a moisture barrier.

Leakage effects on printed circuit boards can be reduced by encircling the inputs (both sides of pc board) with a conductive guard ring connected to a low impedance potential nearly the same as that of the inputs.

Guard ring electrical connections for common operational amplifier configurations are illustrated in Figure 14. Electrostatic shielding is suggested in high impedance circuits.

Error voltages in external circuitry can be generated by thermocouple effects. Dissimilar metals along with temperature gradients can set up an error voltage ranging in the hundreds of microvolts. Some of the best thermocouples are junctions of dissimilar metals made up of IC package pins and printed circuit boards. Problems can be avoided by keeping low level circuitry away from heat generating elements.

The LM11C is internally compensated, but external compensation can be added to improve stability, particularly when driving capacitive loads.

Figure 14. Guard Ring Electrical Connections for Common Amplifier Configurations

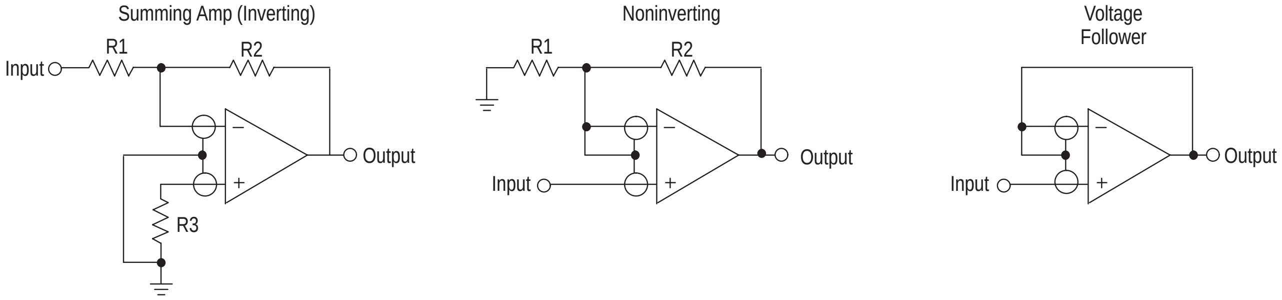
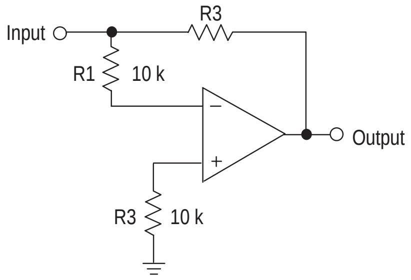
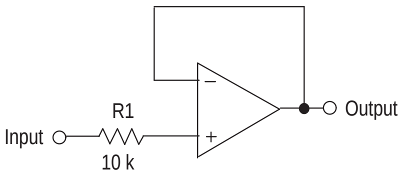


Figure 15. Input Protection for Summing (Inverting) Amplifier



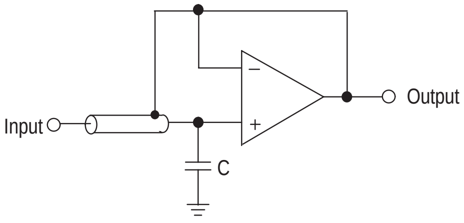
Current is limited by R1 in the event the input is connected to a low impedance source outside the common mode range of the device. Current is controlled by R2 if one supply reverses. R1 and R2 do not affect normal operation.

Figure 16. Input Protection for a Voltage Follower

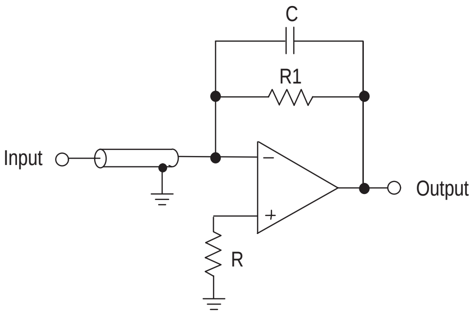


Input current is limited by R1 when the input exceeds supply voltage, power supply is turned off, or output is shorted.

Figure 17. Cable Bootstrapping and Input Shields

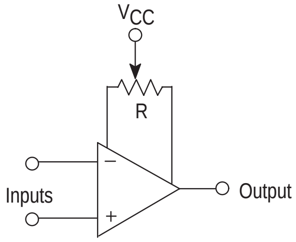


An input shield bootstrapped in a voltage follower reduces input capacitance, leakage, and spurious voltages from cable flexing. A small capacitor from the input to ground will prevent any instability.



In a summing amplifier the input is at virtual ground. Therefore the shield can be grounded. A small feedback capacitor will insure stability.

Figure 18. Adjusting Input Offset Voltage with Balance Potentiometer



Minimum Adjustment Range (mV)	R (Ω)
±0.4	1.0 k
±1.0	3.0 k
±2.0	10 k
±5.0	100 k

Input offset voltage adjustment range is a function of the Balance Potentiometer Resistance as indicated by the table above. The potentiometer is connected between the two “Balance” pins.

MOTOROLA

LM301A
LM201A

Operational Amplifiers

A general purpose operational amplifier that allows the user to choose the compensation capacitor best suited to his needs. With proper compensation, summing amplifier slew rates to 10 V/µs can be obtained.

- Low Input Offset Current: 20 nA Maximum Over Temperature Range
- External Frequency Compensation for Flexibility
- Class AB Output Provides Excellent Linearity
- Output Short Circuit Protection
- Guaranteed Drift Characteristics

Figure 1. Standard Compensation and Offset Balancing Circuit

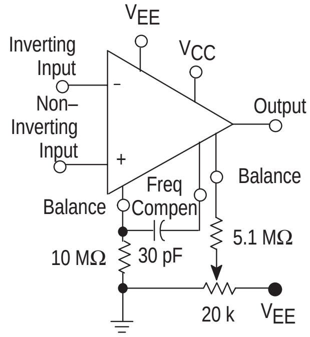
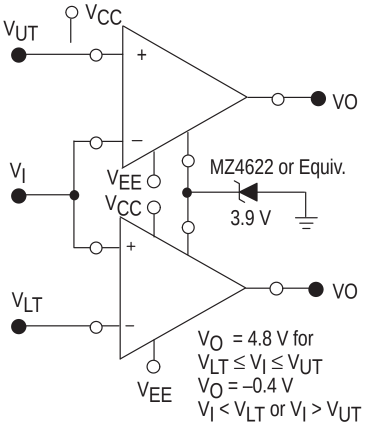
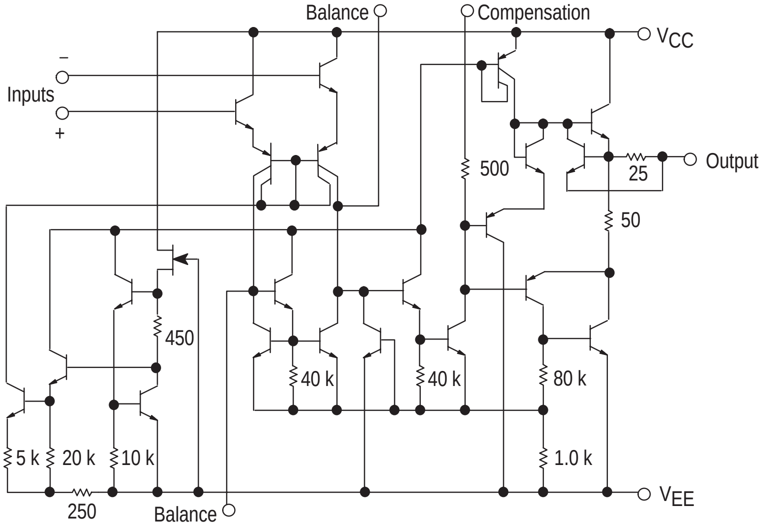


Figure 2. Double–Ended Limit Detector



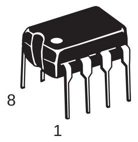
(Pins Not Shown Are Not Connected)

Figure 3. Representative Circuit Schematic

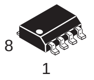


OPERATIONAL AMPLIFIERS

SEMICONDUCTOR TECHNICAL DATA

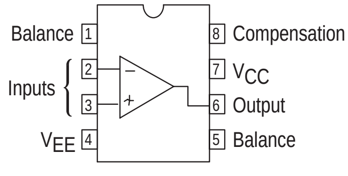


N SUFFIX
PLASTIC PACKAGE
CASE 626



D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
LM301AD LM301AN	T_A = 0° to +70°C	SO–8 Plastic DIP
LM201AD LM201AN	T_A = –25° to +85°C	SO–8 Plastic DIP

MAXIMUM RATINGS

Rating	Symbol	Value		Unit
		LM201A	LM301A	
Power Supply Voltage	V_{CC}, V_{EE}	±22	±18	Vdc
Input Differential Voltage	V_{ID}	←±30→		V
Input Common Mode Range (Note 1)	V_{ICR}	←±15→		V
Output Short Circuit Duration	t_{SC}	←Continuous→		
Power Dissipation (Package Limitation) Plastic Dual–In–Line Package (LM201A/301A) Derate above T_A = +25°C	P_D	 625 5.0	 625 5.0	 mW mW/°C
Operating Ambient Temperature Range	T_A	–25 to +85	0 to +70	°C
Storage Temperature Range	T_{stg}	←–65 to +150→		°C

NOTE: 1. For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.

ELECTRICAL CHARACTERISTICS (T_A = +25°C, unless otherwise noted.) Unless otherwise specified, these specifications apply for supply voltages from ±5.0 V to ±20 V for the LM201A, and from ±5.0 V to ±15 V for the LM301A.

Characteristic	Symbol	LM201A			LM301A			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage (R_S ≤ 50 kΩ)	V_{IO}	–	0.7	2.0	–	2.0	7.5	mV
Input Offset Current	I_{IO}	–	1.5	10	–	3.0	50	nA
Input Bias Current	I_{IB}	–	30	75	–	70	250	nA
Input Resistance	r_i	1.5	4.0	–	0.5	2.0	–	MΩ
Supply Current V_{CC}/V_{EE} = ±20 V V_{CC}/V_{EE} = ±15 V	I_{CC},I_{EE}	 – –	 1.8 –	 3.0 –	 – –	 – 1.8	 – 3.0	mA
Large Signal Voltage Gain (V_{CC}/V_{EE} = ±15 V, V_O = ±10 V, R_L > 2.0 kΩ)	A_V	50	160	–	25	160	–	V/mV

The following specifications apply over the operating temperature range.

Characteristic	Symbol	LM201A Min	LM201A Typ	LM201A Max	LM301A Min	LM301A Typ	LM301A Max	Unit
Input Offset Voltage (R_S ≤ 50 kΩ)	V_{IO}	–	–	3.0	–	–	10	mV
Input Offset Current	I_{IO}	–	–	20	–	–	70	nA
Avg Temperature Coefficient of Input Offset Voltage T_A(min) ≤ T_A ≤ T_A (max)	$\Delta V_{IO}/\Delta T$	–	3.0	15	–	6.0	30	µV/°C
Avg Temperature Coefficient of Input Offset Current +25°C ≤ T_A ≤ T_A (max) T_A(min) ≤ T_A ≤ 25°C	$\Delta I_{IO}/\Delta T$	 – –	 0.01 0.02	 0.1 0.2	 – –	 0.01 0.02	 0.3 0.6	nA/°C
Input Bias Current	I_{IB}	–	–	100	–	–	300	nA
Large Signal Voltage Gain (V_{CC}/V_{EE} = ±15 V, V_O = ±10V, R_L > 2.0 kΩ)	A_{VOL}	25	–	–	15	–	–	V/mV
Input Voltage Range V_{CC}/V_{EE} = ±20 V V_{CC}/V_{EE} = ±15 V	V_{ICR}	 –15 –	 – –	 +15 –	 – –12	 – –	 – +12	V
Common Mode Rejection (R_S ≤ 50 kΩ)	CMR	80	96	–	70	90	–	dB
Supply Voltage Rejection (R_S ≤ 50 kΩ)	PSR	80	96	–	70	96	–	dB
Output Voltage Swing (V_{CC}/V_{EE} = ±15 V, R_L = ±10 kΩ, R_L > 2.0 kΩ)	V_O	±12 ±10	±14 ±13	– –	±12 ±10	±14 ±13	– –	V
Supply Currents (T_A = T_A(max), V_{CC}/V_{EE} = ±20 V)	I_{CC},I_{EE}	–	1.2	2.5	–	–	–	mA

Figure 4. Minimum Input Voltage Range

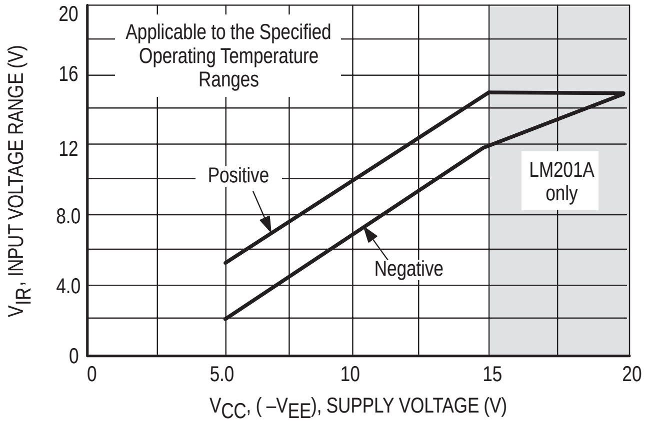


Figure 5. Minimum Output Voltage Swing

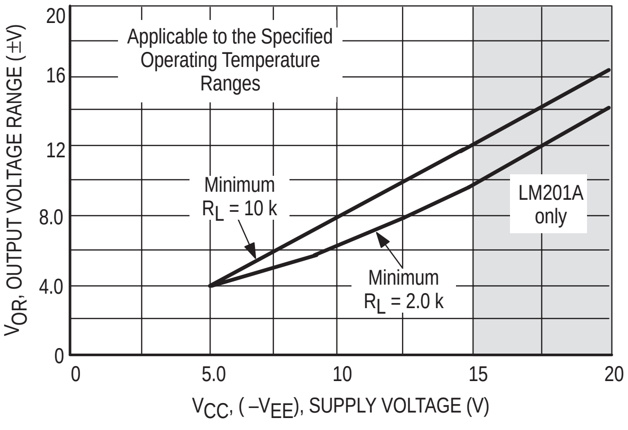


Figure 6. Minimum Voltage Gain

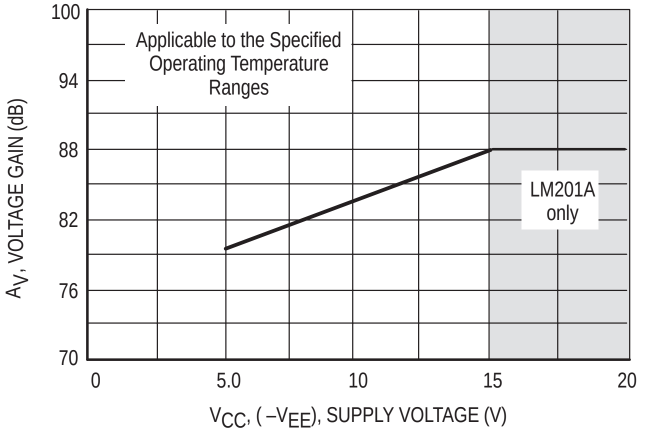


Figure 7. Typical Supply Currents

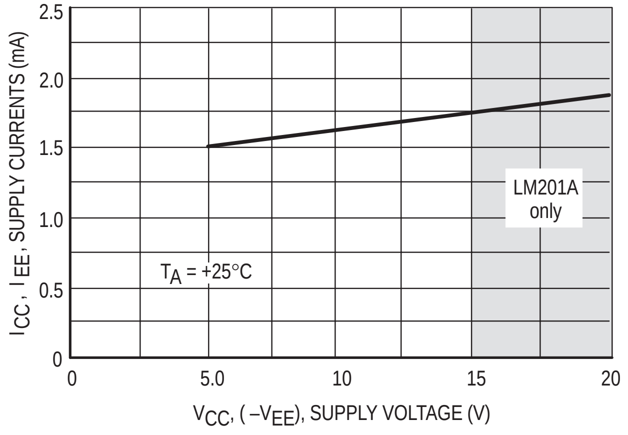


Figure 8. Open Loop Frequency Response

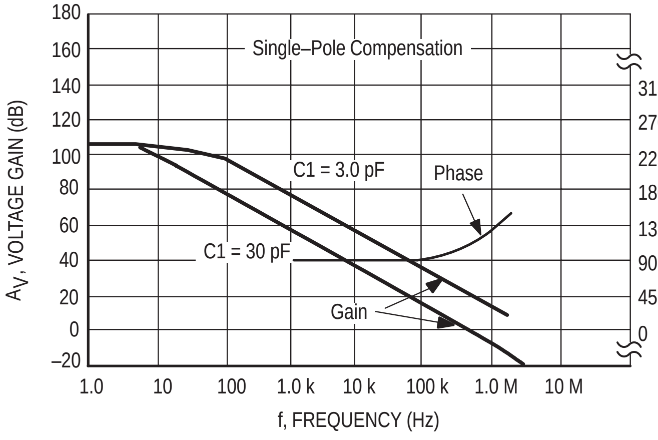


Figure 9. Large Signal Frequency Response

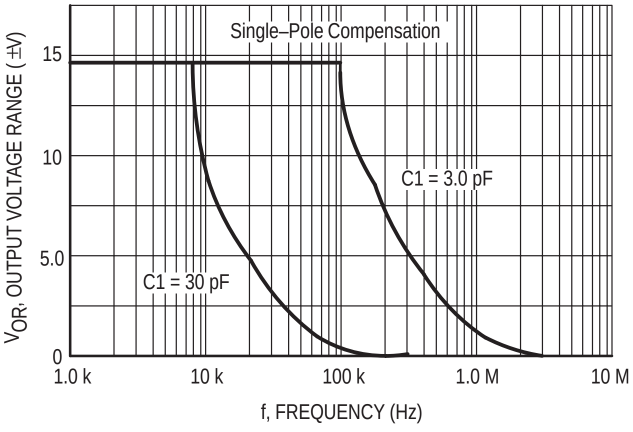


Figure 10. Voltage Follower Pulse Response

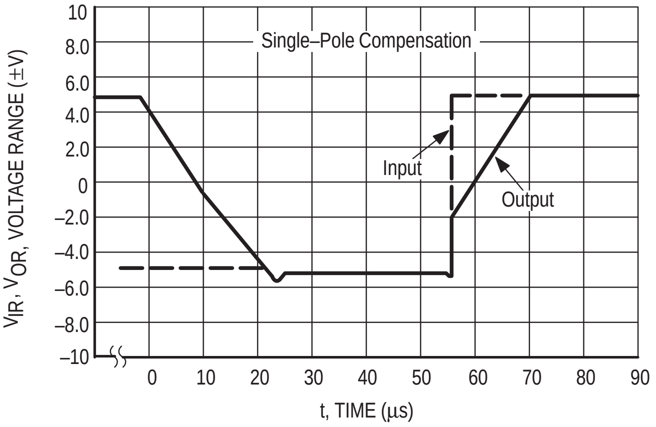


Figure 11. Open Loop Frequency Response

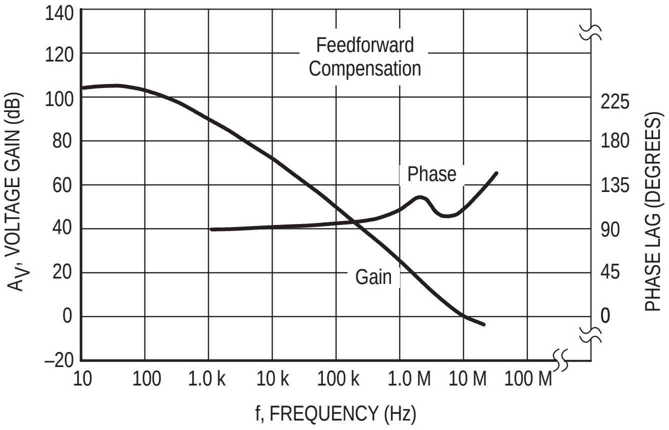


Figure 12. Large Signal Frequency Response

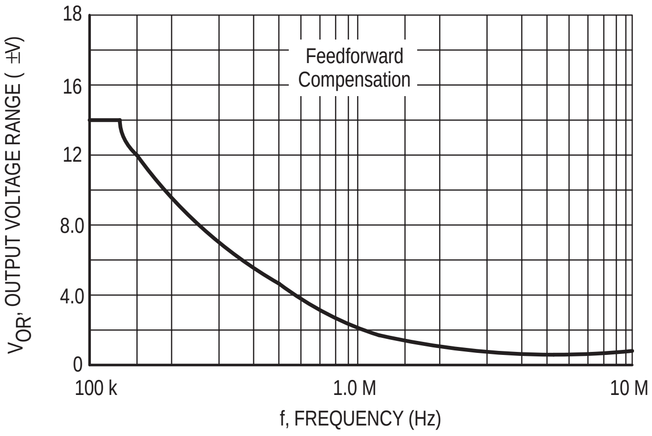


Figure 13. Inverter Pulse Response

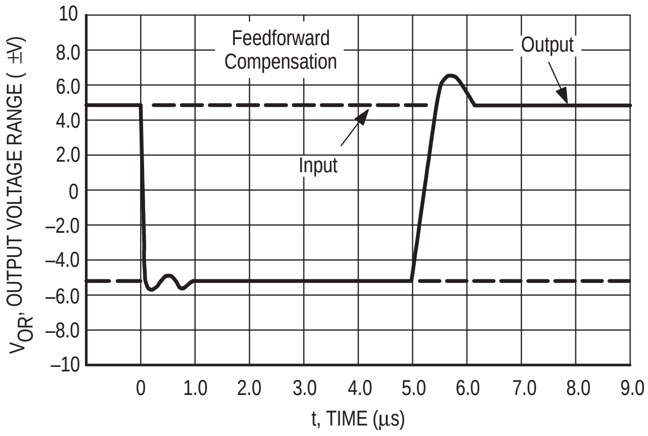


Figure 14. Single–Pole Compensation

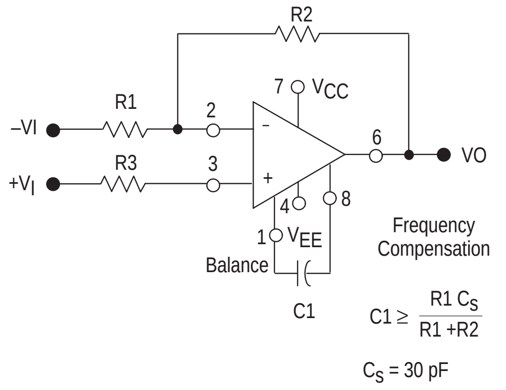
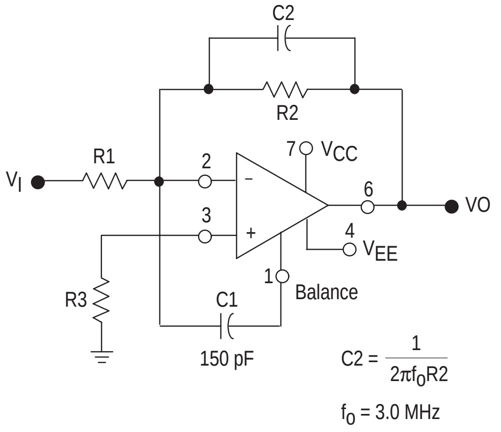


Figure 15. Feedforward Compensation



LM308A

Precision Operational Amplifier

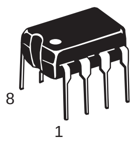
The LM308A operational amplifier provides high input impedance, low input offset and temperature drift, and low noise. These characteristics are made possible by use of a special Super Beta processing technology. This amplifier is particularly useful for applications where high accuracy and low drift performance are essential. In addition high speed performance may be improved by employing feedforward compensation techniques to maximize slew rate without compromising other performance criteria.

The LM308A offers extremely low input offset voltage and drift specifications allowing usage in even the most critical applications without external offset nulling.

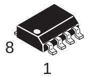
- Operation from a Wide Range of Power Supply Voltages
- Low Input Bias and Offset Currents
- Low Input Offset Voltage and Guaranteed Offset Voltage Drift Performance
- High Input Impedance

SUPER GAIN OPERATIONAL AMPLIFIER

SEMICONDUCTOR TECHNICAL DATA

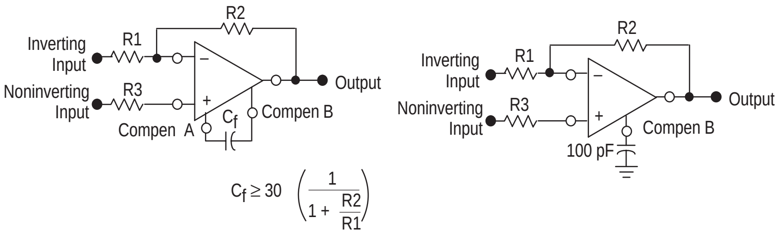


N SUFFIX
PLASTIC PACKAGE
CASE 626



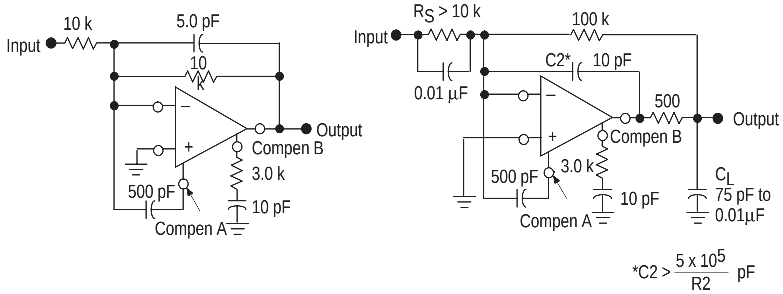
D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

Frequency Compensation



Standard Compensation

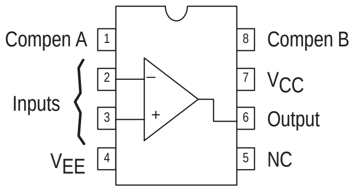
Modified Compensation



Standard Feedforward Compensation

Feedforward Compensations for Decoupling Load Capacitance

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
LM308AN LM308AD	T_A = 0° to +70°C	Plastic DIP SO–8

MAXIMUM RATINGS (T_A = +25°C, unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}, V_{EE}	±18	Vdc
Input Voltage (See Note 1)	V_I	±15	V
Input Differential Current (See Note 2)	I_{ID}	±10	mA
Output Short Circuit Duration	t_{SC}	Indefinite	
Operating Ambient Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Junction Temperature	T_J	+150	°C

NOTES: 1. For supply voltages less than ±15 V, the maximum input voltage is equal to the supply voltage.
2. The inputs are shunted with back–to–back diodes for overvoltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1.0 V is applied between the inputs, unless some limiting resistance is used.

ELECTRICAL CHARACTERISTICS (Unless otherwise noted these specifications apply for supply voltages of +5.0 V ≤ V_{CC} ≤ +15 V and –5.0 V ≥ V_{EE} ≥ –15 V, T_A = +25°C.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Offset Voltage	V_{IO}	–	0.3	0.5	mV
Input Offset Current	I_{IO}	–	0.2	1.0	nA
Input Bias Current	I_{IB}	–	1.5	7.0	nA
Input Resistance	r_i	10	40	–	MΩ
Power Supply Currents (V_{CC} = +15 V, V_{EE} = –15 V)	I_{CC}, I_{EE}	–	±0.3	±0.8	mA
Large Signal Voltage Gain (V_{CC} = +15 V, V_{EE} = –15 V, V_O = ±10 V, R_L ≥ 10 kΩ)	A_{VOL}	80	300	–	V/mV
The following specifications apply over the operating temperature range.					
Input Offset Voltage	V_{IO}	–	–	0.73	mV
Input Offset Current	I_{IO}	–	–	1.5	nA
Average Temperature Coefficient of Input Offset Voltage T_A (min) ≤ T_A ≤ T_A (max)	$\Delta V_{IO}/\Delta T$	–	1.0	5.0	µV/°C
Average Temperature Coefficient of Input Offset Current	$\Delta I_{IO}/\Delta T$	–	2.0	10	pA/°C
Input Bias Current	I_{IB}	–	–	10	nA
Large Signal Voltage Gain (V_{CC} +15 V, V_{EE} = –15 V, V_O = ±10 V, R_L ≥ 10 kΩ)	A_{VOL}	60	–	–	V/mV
Input Voltage Range (V_{CC} = +15 V, V_{EE} = –15 V)	V_{ICR}	±14	–	–	V
Common Mode Rejection (R_S ≤ 50 kΩ)	CMR	96	110	–	dB
Supply Voltage Rejection (R_S ≤ 50 kΩ)	PSR	96	110	–	dB
Output Voltage Range (V_{CC} = +15 V, V_{EE} = –15 V, R_L = 10 kΩ)	V_{OR}	±13	±14	–	V

Figure 1. Input Bias and Input Offset Currents

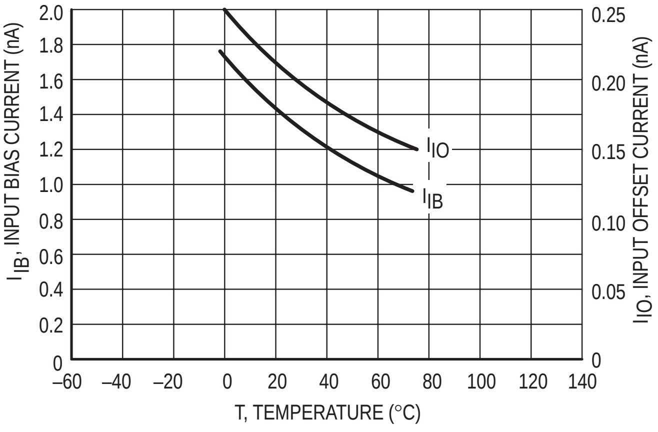


Figure 2. Maximum Equivalent Input Offset Voltage Error versus Input Resistance

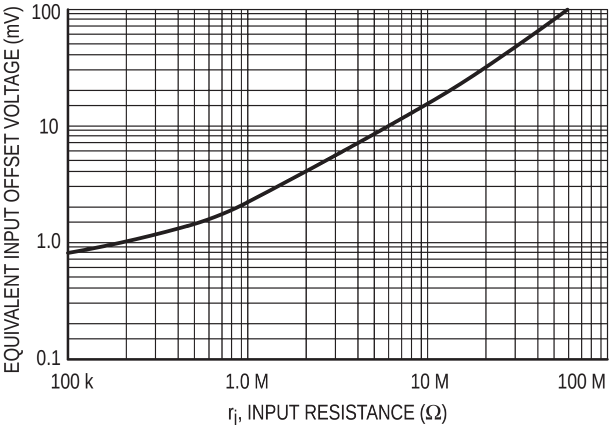


Figure 3. Voltage Gain versus Supply Voltages

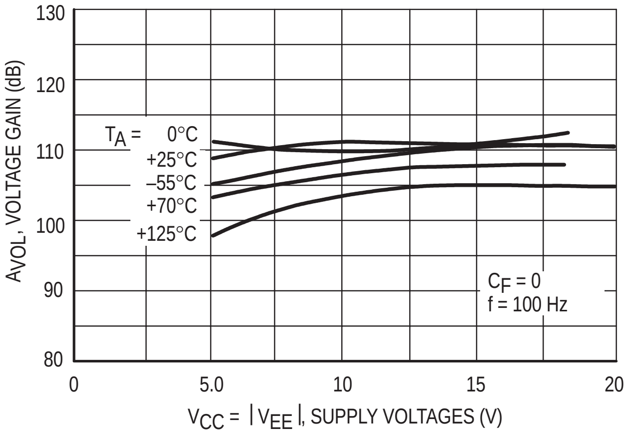


Figure 4. Power Supply Currents versus Power Supply Voltages

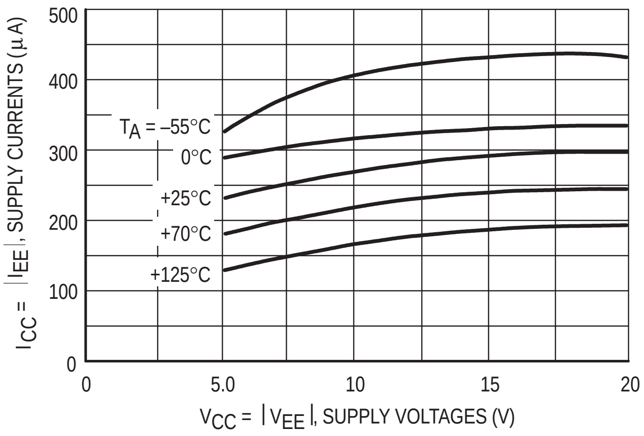


Figure 5. Open Loop Frequency Response

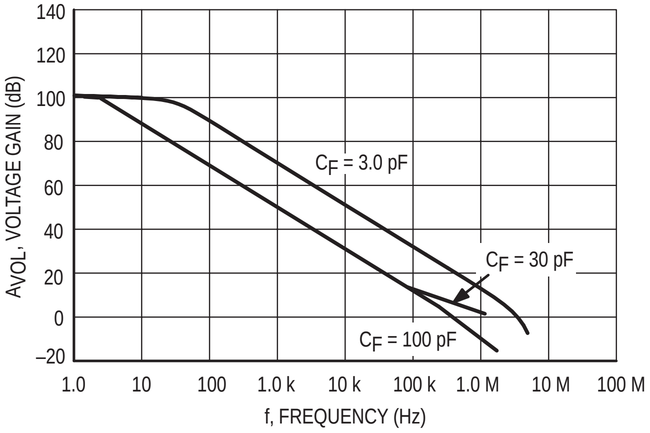
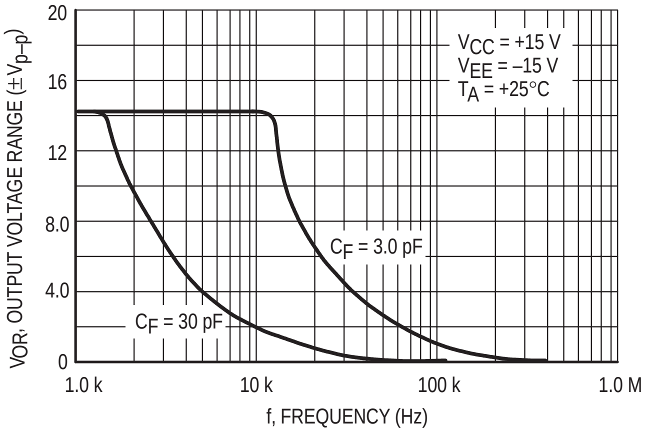


Figure 6. Large Signal Frequency Response



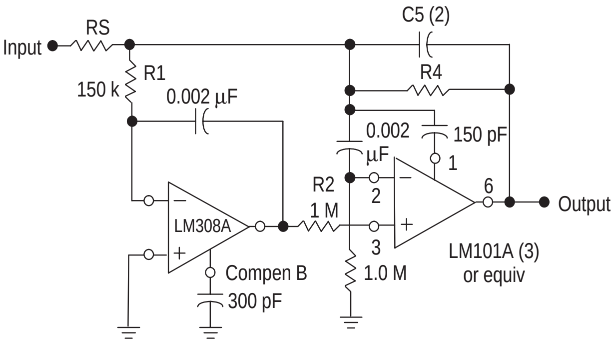
SUGGESTED DESIGN APPLICATIONS

INPUT GUARDING

Special care must be taken in the assembly of printed circuit boards to take full advantage of the low input currents of the LM308A amplifier. Boards must be thoroughly cleaned with alcohol and blown dry with compressed air. After cleaning, the boards should be coated with epoxy or silicone rubber to prevent contamination.

Even with properly cleaned and coated boards, leakage currents may cause trouble at +125°C, particularly since the input pins are adjacent to pins that are at supply potentials. This leakage can be significantly reduced by using guarding to lower the voltage difference between the inputs and adjacent metal runs. The guard, which is a conductive ring surrounding the inputs, is connected to a low–impedance point that is at approximately the same voltage as the inputs. Leakage currents from high voltage pins are then absorbed by the guard.

Figure 7. Fast (1) Summing Amplifier with Low Input Current

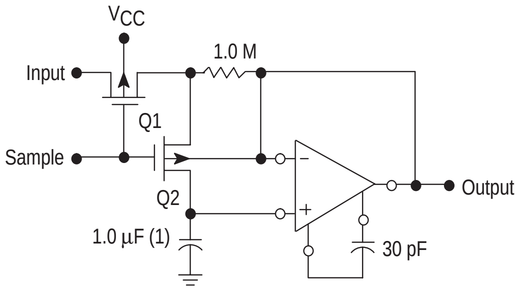


(1) Power Bandwidth: 250 kHz
Small Signal Bandwidth: 3.5 MHz
Slew Rate: 10 V/µs

(2) $C5 = \frac{6 \times 10^{-8}}{R1}$

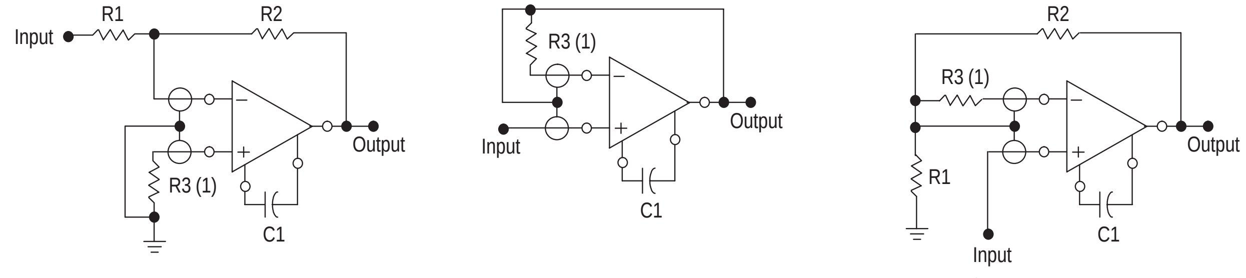
(3) In addition to increasing speed, the LM101A raises high and low frequency gain, increases output drive capability and eliminates thermal feedback.

Figure 8. Sample and Hold



(1) Teflon, Polyethylene or Polycarbonate Dielectric Capacitor

Figure 9. Connection of Input Guards


Inverting Amplifier

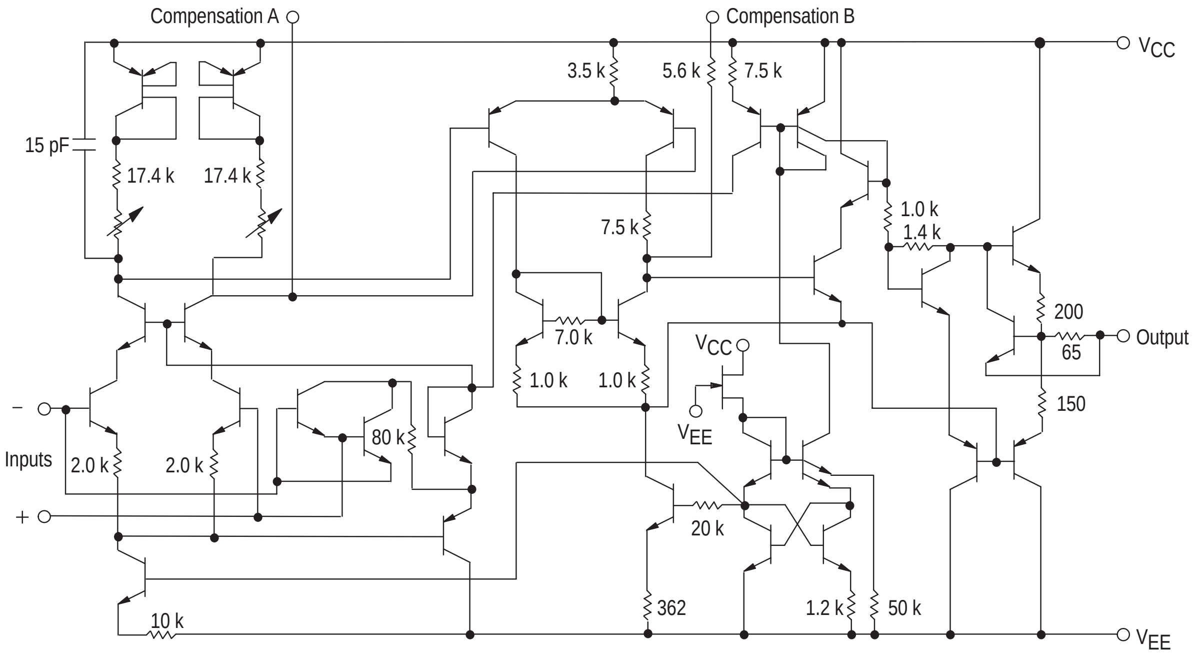
Follower

Noninverting Amplifier

(1) Used to compensate for large source resistances.

Note: $\frac{R1\,R2}{R1 + R2}$ must be an impedance.

Representative Circuit Schematic



MOTOROLA

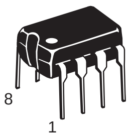
LM311
LM211

Highly Flexible Voltage Comparators

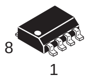
The ability to operate from a single power supply of 5.0 V to 30 V or ±15 V split supplies, as commonly used with operational amplifiers, makes the LM211/LM311 a truly versatile comparator. Moreover, the inputs of the device can be isolated from system ground while the output can drive loads referenced either to ground, the V_{CC} or the V_{EE} supply. This flexibility makes it possible to drive DTL, RTL, TTL, or MOS logic. The output can also switch voltages to 50 V at currents to 50 mA. Thus the LM211/LM311 can be used to drive relays, lamps or solenoids.

HIGH PERFORMANCE VOLTAGE COMPARATORS

SEMICONDUCTOR TECHNICAL DATA



N SUFFIX
PLASTIC PACKAGE
CASE 626



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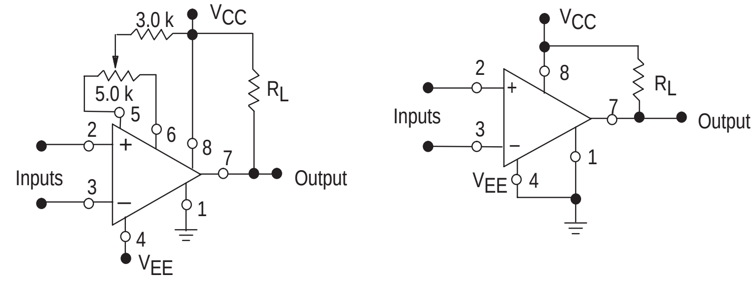
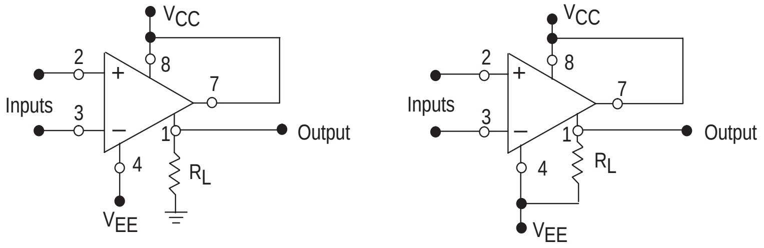
CASE 751
(SO–8)

Typical Comparator Design Configurations



Split Power Supply with Offset Balance

Single Supply

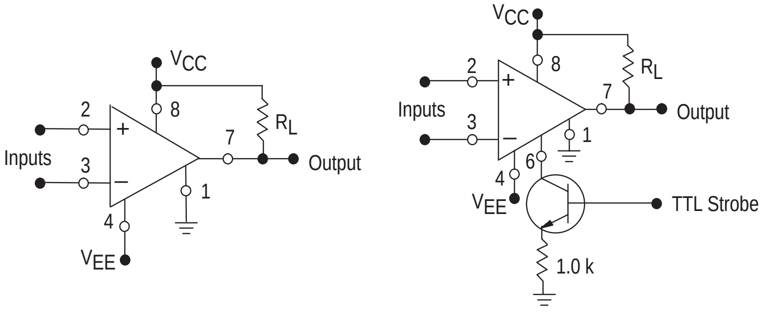


Ground–Referred Load

Input polarity is reversed when Gnd pin is used as an output.

Load Referred to Negative Supply

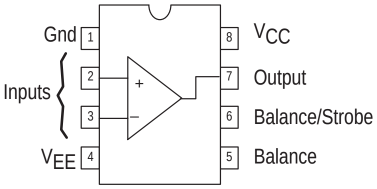
Input polarity is reversed when Gnd pin is used as an output.



Load Referred to Positive Supply

Strobe Capability

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
LM211D	T_A = 25° to +85°C	SO–8
LM311D LM311N	T_A = 0° to +70°C	SO–8 Plastic DIP

MAXIMUM RATINGS (T_A = +25°C, unless otherwise noted.)

Rating	Symbol	LM211	LM311	Unit
Total Supply Voltage	$V_{CC} + \lvert V_{EE} \rvert$	36	36	Vdc
Output to Negative Supply Voltage	$V_O - V_{EE}$	50	40	Vdc
Ground to Negative Supply Voltage	V_{EE}	30	30	Vdc
Input Differential Voltage	V_{ID}	±30	±30	Vdc
Input Voltage (Note 2)	V_{in}	±15	±15	Vdc
Voltage at Strobe Pin	–	V_{CC} to V_{CC}–5	V_{CC} to V_{CC}–5	Vdc
Power Dissipation and Thermal Characteristics				
Plastic DIP	P_D	625		mW
Derate Above T_A = +25°C	$1/\theta_{JA}$	5.0		mW/°C
Operating Ambient Temperature Range	T_A	–25 to +85	0 to +70	°C
Operating Junction Temperature	$T_{J(max)}$	+150	+150	°C
Storage Temperature Range	T_{stg}	–65 to +150	–65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = –15 V, T_A = 25°C, unless otherwise noted [Note 1].)

Characteristic	Symbol	LM211			LM311			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage (Note 3)	V_{IO}							mV
$R_S \leq$ 50 kΩ, T_A = +25°C		–	0.7	3.0	–	2.0	7.5	
$R_S \leq$ 50 kΩ, $T_{low} \leq T_A \leq T_{high}$*		–	–	4.0	–	–	10	
Input Offset Current (Note 3) T_A = +25°C	I_{IO}	–	1.7	10	–	1.7	50	nA
$T_{low} \leq T_A \leq T_{high}$*		–	–	20	–	–	70	
Input Bias Current T_A = +25°C	I_{IB}	–	45	100	–	45	250	nA
$T_{low} \leq T_A \leq T_{high}$*		–	–	150	–	–	300	
Voltage Gain	A_V	40	200	–	40	200	–	V/mV
Response Time (Note 4)		–	200	–	–	200	–	ns
Saturation Voltage	V_{OL}							V
$V_{ID} \leq$ –5.0 mV, I_O = 50 mA, T_A = 25°C		–	0.75	1.5	–	–	–	
$V_{ID} \leq$ –10 mV, I_O = 50 mA, T_A = 25°C		–	–	–	–	0.75	1.5	
$V_{CC} \geq$ 4.5 V, V_{EE} = 0, $T_{low} \leq T_A \leq T_{high}$*								
V_{ID} ∠≤6.0 mV, $I_{sink} \leq$ 8.0 mA		–	0.23	0.4	–	–	–	
V_{ID} ∠≤10 mV, $I_{sink} \leq$ 8.0 mA		–	–	–	–	0.23	0.4	
Strobe ”On” Current (Note 5)	I_S	–	3.0	–	–	3.0	–	mA
Output Leakage Current								
$V_{ID} \geq$ 5.0 mV, V_O= 35 V, T_A = 25°C, I_{strobe}= 3.0 mA		–	0.2	10	–	–	–	nA
$V_{ID} \geq$ 10 mV, V_O= 35 V, T_A = 25°C, I_{strobe}= 3.0 mA		–	–	–	–	0.2	50	nA
$V_{ID} \geq$ 5.0 mV, V_O= 35 V, $T_{low} \leq T_A \leq T_{high}$*		–	0.1	0.5	–	–	–	µA
Input Voltage Range ($T_{low} \leq T_A \leq T_{high}$*)	V_{ICR}	–14.5	–14.7 to 13.8	+13.0	–14.5	–14.7 to 13.8	+13.0	V
Positive Supply Current	I_{CC}	–	+2.4	+6.0	–	+2.4	+7.5	mA
Negative Supply Current	I_{EE}	–	–1.3	–5.0	–	–1.3	–5.0	mA

* T_{low} = –25°C for LM211 T_{high} = +85°C for LM211
= 0°C for LM311 = +70°C for LM311

NOTES:
1. Offset voltage, offset current and bias current specifications apply for a supply voltage range from a single 5.0 V supply up to ±15 V supplies.
2. This rating applies for ±15 V supplies. The positive input voltage limit is 30 V above the negative supply. The negative input voltage limit is equal to the negative supply voltage or 30 V below the positive supply, whichever is less.
3. The offset voltages and offset currents given are the maximum values required to drive the output within a volt of either supply with a 1.0 mA load. Thus, these parameters define an error band and take into account the ”worst case” effects of voltage gain and input impedance.
4. The response time specified is for a 100 mV input step with 5.0 mV overdrive.
5. Do not short the strobe pin to ground; it should be current driven at 3.0 mA to 5.0 mA.

Figure 1. Circuit Schematic

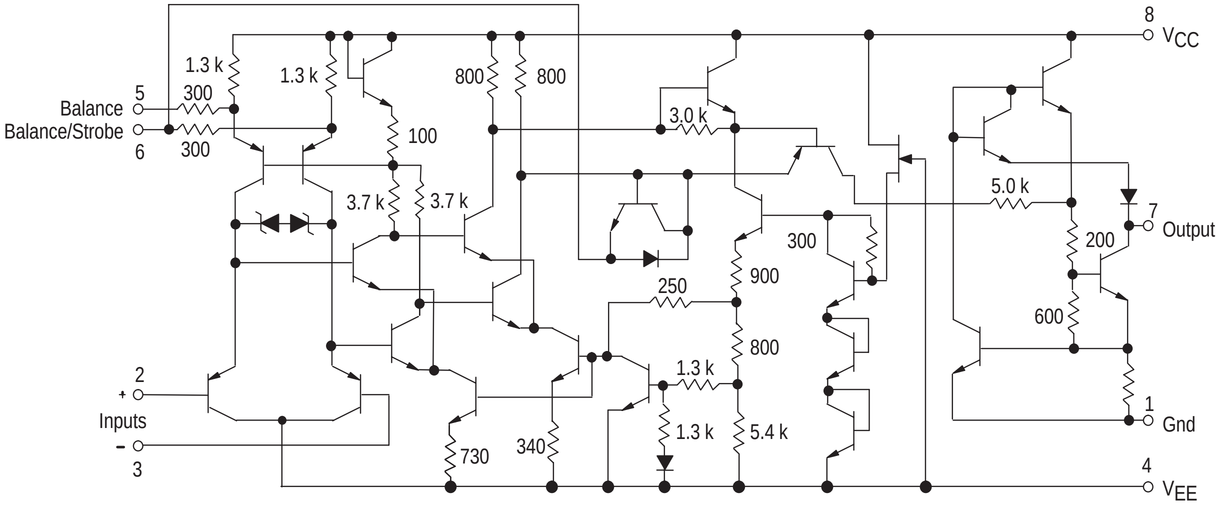


Figure 2. Input Bias Current versus Temperature

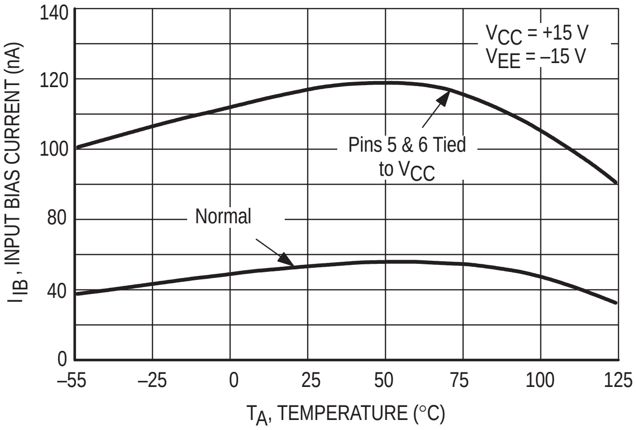


Figure 3. Input Offset Current versus Temperature

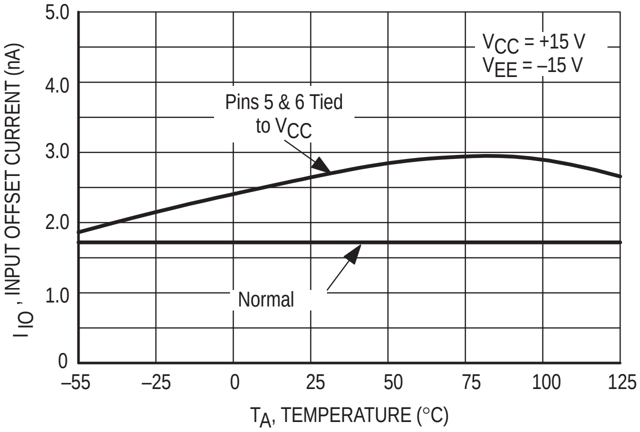


Figure 4. Input Bias Current versus Differential Input Voltage

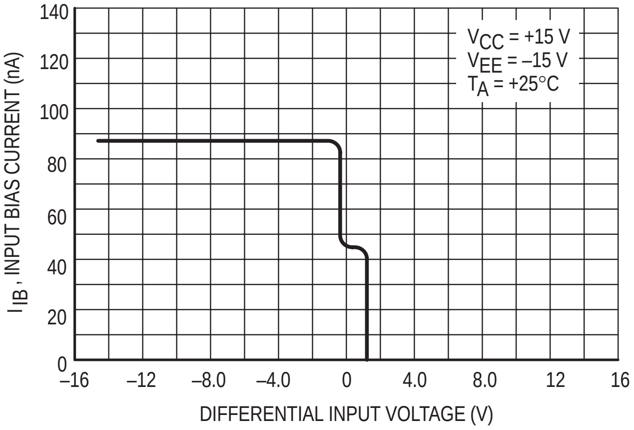


Figure 5. Common Mode Limits versus Temperature

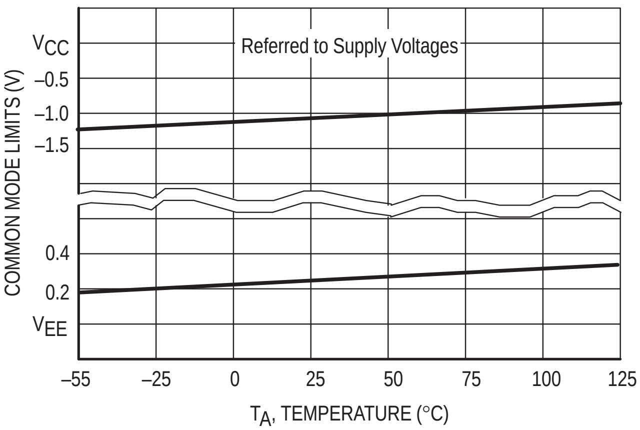


Figure 6. Response Time for Various Input Overdrives

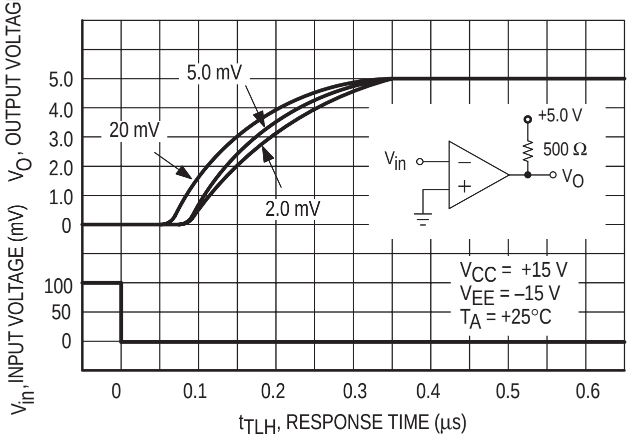


Figure 7. Response Time for Various Input Overdrives

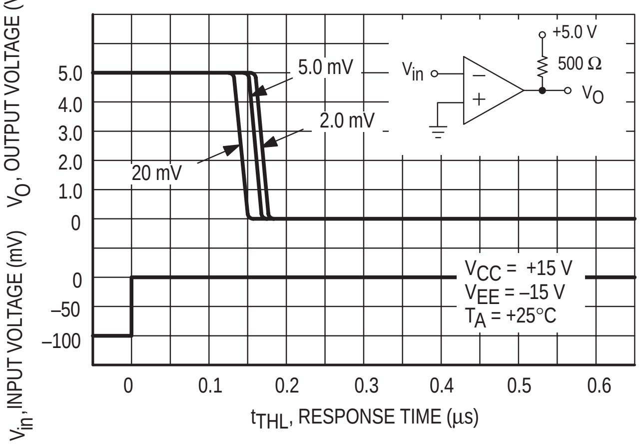


Figure 8. Response Time for Various Input Overdrives

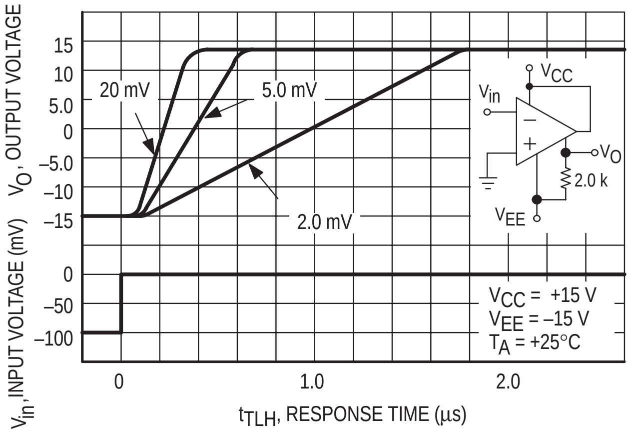


Figure 9. Response Time for Various Input Overdrives

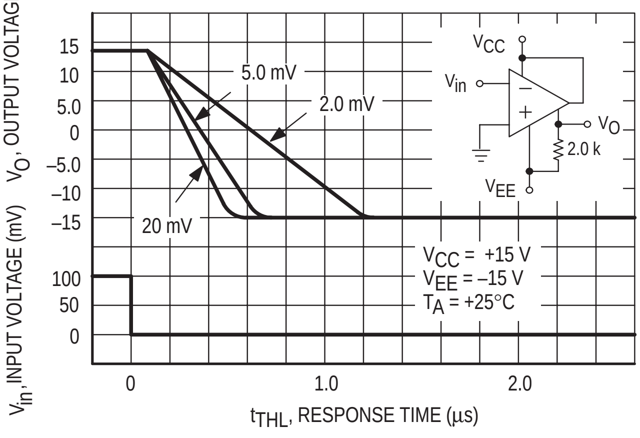


Figure 10. Output Short Circuit Current Characteristics and Power Dissipation

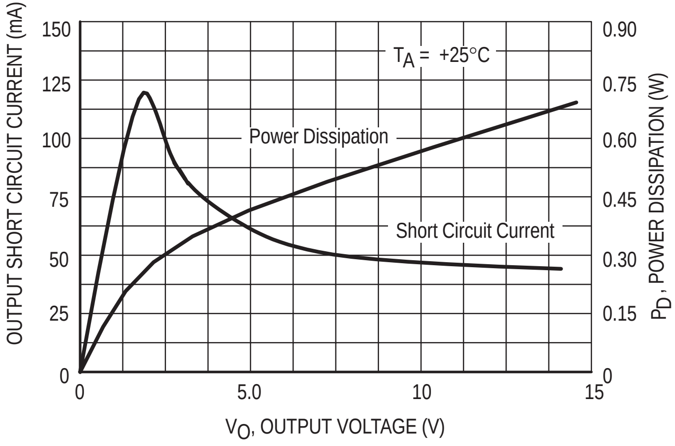


Figure 11. Output Saturation Voltage versus Output Current

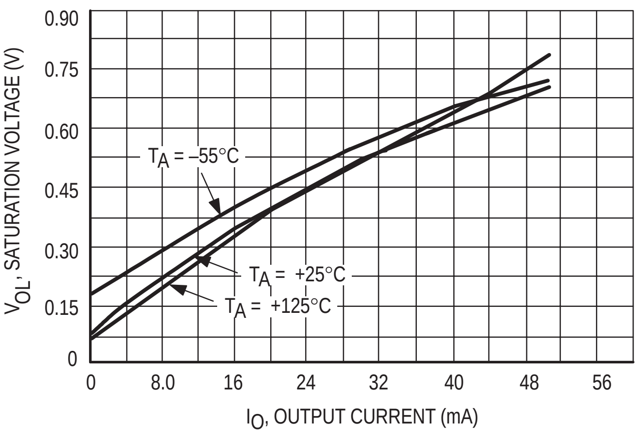


Figure 12. Output Leakage Current versus Temperature

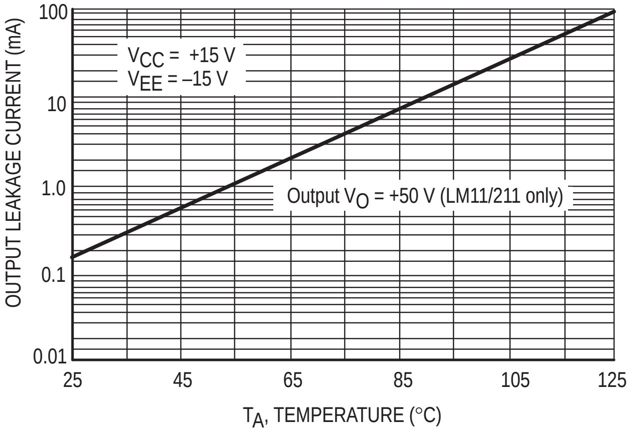


Figure 13. Power Supply Current versus Supply Voltage

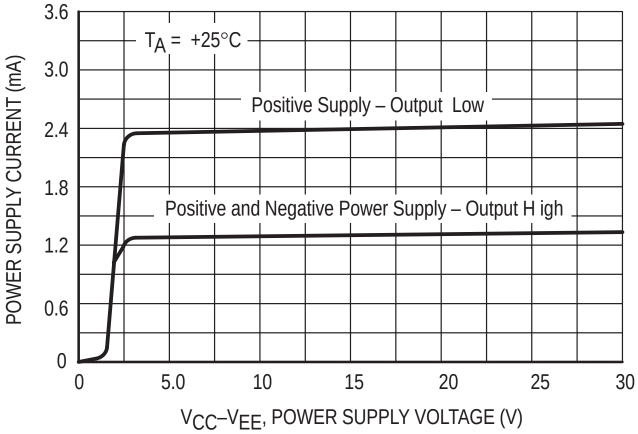
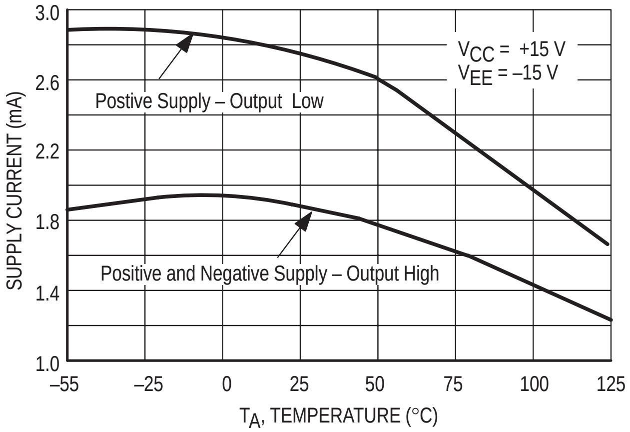


Figure 14. Power Supply Current versus Temperature



APPLICATIONS INFORMATION

Figure 15. Improved Method of Adding Hysteresis Without Applying Positive Feedback to the Inputs

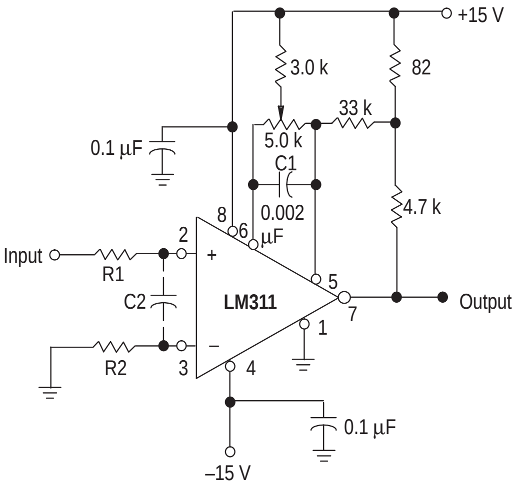
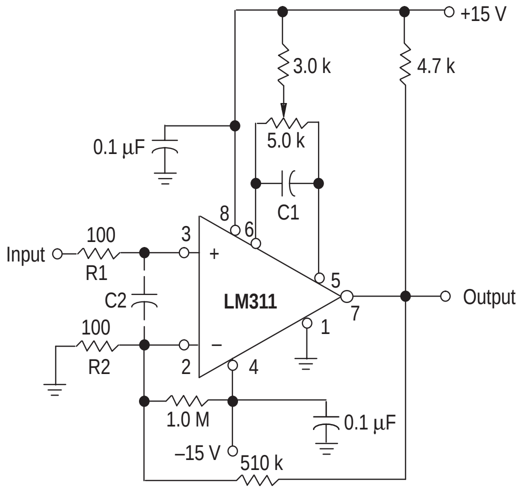


Figure 16. Conventional Technique for Adding Hysteresis



TECHNIQUES FOR AVOIDING OSCILLATIONS IN COMPARATOR APPLICATIONS

When a high speed comparator such as the LM211 is used with high speed input signals and low source impedances, the output response will normally be fast and stable, providing the power supplies have been bypassed (with 0.1 µF disc capacitors), and that the output signal is routed well away from the inputs (Pins 2 and 3) and also away from Pins 5 and 6.

However, when the input signal is a voltage ramp or a slow sine wave, or if the signal source impedance is high (1.0 kΩ to 100 kΩ), the comparator may burst into oscillation near the crossing–point. This is due to the high gain and wide bandwidth of comparators like the LM211 series. To avoid oscillation or instability in such a usage, several precautions are recommended, as shown in Figure 15.

The trim pins (Pins 5 and 6) act as unwanted auxiliary inputs. If these pins are not connected to a trim–pot, they should be shorted together. If they are connected to a trim–pot, a 0.01 µF capacitor (C1) between Pins 5 and 6 will minimize the susceptibility to AC coupling. A smaller capacitor is used if Pin 5 is used for positive feedback as in Figure 15. For the fastest response time, tie both balance pins to V_{CC}.

Certain sources will produce a cleaner comparator output waveform if a 100 pF to 1000 pF capacitor (C2) is connected directly across the input pins. When the signal source is applied through a resistive network, R1, it is usually advantageous to choose R2 of the same value, both for DC and for dynamic (AC) considerations. Carbon, tin–oxide, and metal–film resistors have all been used with good results in comparator input circuitry, but inductive wirewound resistors should be avoided.

When comparator circuits use input resistors (e.g., summing resistors), their value and placement are particularly important. In all cases the body of the resistor should be close to the device or socket. In other words, there should be a very short lead length or printed–circuit foil run between comparator and resistor to radiate or pick up signals. The same applies to capacitors, pots, etc. For example, if R1 = 10 kΩ, as little as 5 inches of lead between the resistors and the input pins can result in oscillations that are very hard to dampen. Twisting these input leads tightly is the best alternative to placing resistors close to the comparator.

Since feedback to almost any pin of a comparator can result in oscillation, the printed–circuit layout should be engineered thoughtfully. Preferably there should be a groundplane under the LM211 circuitry (e.g., one side of a double layer printed circuit board). Ground, positive supply or negative supply foil should extend between the output and the inputs to act as a guard. The foil connections for the inputs should be as small and compact as possible, and should be essentially surrounded by ground foil on all sides to guard against capacitive coupling from any fast high–level signals (such as the output). If Pins 5 and 6 are not used, they should be shorted together. If they are connected to a trim–pot, the trim–pot should be located no more than a few inches away from the LM211, and a 0.01 µF capacitor should be installed across Pins 5 and 6. If this capacitor cannot be used, a shielding printed–circuit foil may be advisable between Pins 6 and 7. The power supply bypass capacitors should be located within a couple inches of the LM211.

A standard procedure is to add hysteresis to a comparator to prevent oscillation, and to avoid excessive noise on the output. In the circuit of Figure 16, the feedback resistor of 510 kΩ from the output to the positive input will cause about 3.0 mV of hysteresis. However, if R2 is larger than 100 Ω, such as 50 kΩ, it would not be practical to simply increase the value of the positive feedback resistor proportionally above 510 kΩ to maintain the same amount of hysteresis.

When both inputs of the LM211 are connected to active signals, or if a high–impedance signal is driving the positive input of the LM211 so that positive feedback would be disruptive, the circuit of Figure 15 is ideal. The positive feedback is applied to Pin 5 (one of the offset adjustment pins). This will be sufficient to cause 1.0 mV to 2.0 mV hysteresis and sharp transitions with input triangle waves from a few Hz to hundreds of kHz. The positive–feedback signal across the 82 Ω resistor swings 240 mV below the positive supply. This signal is centered around the nominal voltage at Pin 5, so this feedback does not add to the offset voltage of the comparator. As much as 8.0 mV of offset voltage can be trimmed out, using the 5.0 kΩ pot and 3.0 kΩ resistor as shown.

Figure 17. Zero–Crossing Detector Driving CMOS Logic

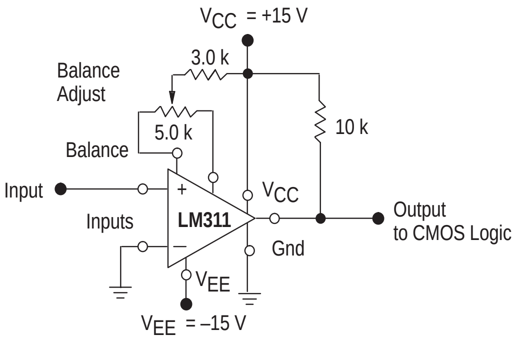
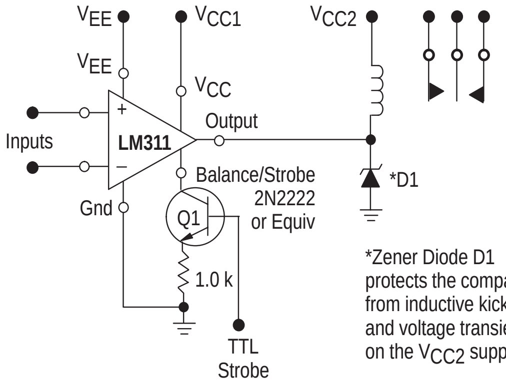


Figure 18. Relay Driver with Strobe Capability



*Zener Diode D1 protects the comparator from inductive kickback and voltage transients on the V_{CC2} supply line.

MOTOROLA

LM324, LM324A, LM224, LM2902, LM2902V

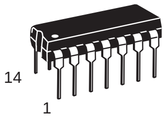
Quad Low Power Operational Amplifiers

The LM324 series are low–cost, quad operational amplifiers with true differential inputs. They have several distinct advantages over standard operational amplifier types in single supply applications. The quad amplifier can operate at supply voltages as low as 3.0 V or as high as 32 V with quiescent currents about one–fifth of those associated with the MC1741 (on a per amplifier basis). The common mode input range includes the negative supply, thereby eliminating the necessity for external biasing components in many applications. The output voltage range also includes the negative power supply voltage.

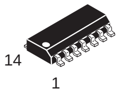
- Short Circuited Protected Outputs
- True Differential Input Stage
- Single Supply Operation: 3.0 V to 32 V
- Low Input Bias Currents: 100 nA Maximum (LM324A)
- Four Amplifiers Per Package
- Internally Compensated
- Common Mode Range Extends to Negative Supply
- Industry Standard Pinouts
- ESD Clamps on the Inputs Increase Ruggedness without Affecting Device Operation

QUAD DIFFERENTIAL INPUT OPERATIONAL AMPLIFIERS

SEMICONDUCTOR TECHNICAL DATA

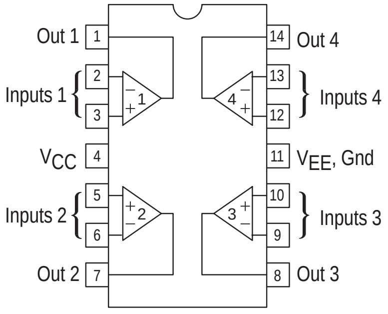


N SUFFIX
PLASTIC PACKAGE
CASE 646
(LM224, LM324,
LM2902 Only)



D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO–14)

PIN CONNECTIONS



(Top View)

MAXIMUM RATINGS (T_A = +25°C, unless otherwise noted.)

Rating	Symbol	LM224 LM324, LM324A	LM2902, LM2902V	Unit
Power Supply Voltages Single Supply Split Supplies	 V_{CC} V_{CC}, V_{EE}	 32 ±16	 26 ±13	Vdc
Input Differential Voltage Range (See Note 1)	V_{IDR}	±32	±26	Vdc
Input Common Mode Voltage Range	V_{ICR}	–0.3 to 32	–0.3 to 26	Vdc
Output Short Circuit Duration	t_{SC}	Continuous		
Junction Temperature	T_J	150		°C
Storage Temperature Range	T_{stg}	–65 to +150		°C
Operating Ambient Temperature Range	T_A	–25 to +85 0 to +70	–40 to +105 –40 to +125	°C

NOTE: 1. Split Power Supplies.

ORDERING INFORMATION

Device	Operating Temperature Range	Package
LM2902D	T_A = –40° to +105°C	SO–14
LM2902N		Plastic DIP
LM2902VD	T_A = –40° to +125°C	SO–14
LM2902VN		Plastic DIP
LM224D	T_A = –25° to +85°C	SO–14
LM224N		Plastic DIP
LM324AD	T_A = 0° to +70°C	SO–14
LM324AN		Plastic DIP
LM324D		SO–14
LM324N		Plastic DIP

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, V_{EE} = Gnd, T_A = 25°C, unless otherwise noted.)

Characteristics	Symbol	LM224			LM324A			LM324			LM2902			LM2902V			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage V_{CC} = 5.0 V to 30 V (26 V for LM2902, V), V_{ICR} = 0 V to V_{CC} –1.7 V, V_O = 1.4 V, R_S = 0 Ω	V_{IO}																mV
T_A = 25°C		–	2.0	5.0	–	2.0	3.0	–	2.0	7.0	–	2.0	7.0	–	2.0	7.0	
$T_A = T_{high}$(1)		–	–	7.0	–	–	5.0	–	–	9.0	–	–	10	–	–	13	
$T_A = T_{low}$(1)		–	–	7.0	–	–	5.0	–	–	9.0	–	–	10	–	–	10	
Average Temperature Coefficient of Input Offset Voltage $T_A = T_{high}$ to T_{low}(1)	$\Delta V_{IO}/\Delta T$	–	7.0	–	–	7.0	30	–	7.0	–	–	7.0	–	–	7.0	–	µV/°C
Input Offset Current	I_{IO}	–	3.0	30	–	5.0	30	–	5.0	50	–	5.0	50	–	5.0	50	nA
$T_A = T_{high}$ to T_{low}(1)		–	–	100	–	–	75	–	–	150	–	–	200	–	–	200	
Average Temperature Coefficient of Input Offset Current $T_A = T_{high}$ to T_{low}(1)	$\Delta I_{IO}/\Delta T$	–	10	–	–	10	300	–	10	–	–	10	–	–	10	–	pA/°C
Input Bias Current	I_{IB}	–	–90	–150	–	–45	–100	–	–90	–250	–	–90	–250	–	–90	–250	nA
$T_A = T_{high}$ to T_{low}(1)		–	–	–300	–	–	–200	–	–	–500	–	–	–500	–	–	–500	
Input Common Mode Voltage Range(2)	V_{ICR}																V
V_{CC} = 30 V (26 V for LM2902, V)		0	–	28.3	0	–	28.3	0	–	28.3	0	–	24.3	0	–	24.3	
V_{CC} = 30 V (26 V for LM2902, V), $T_A = T_{high}$ to T_{low}		0	–	28	0	–	28	0	–	28	0	–	24	0	–	24	
Differential Input Voltage Range	V_{IDR}	–	–	V_{CC}	–	–	V_{CC}	–	–	V_{CC}	–	–	V_{CC}	–	–	V_{CC}	V
Large Signal Open Loop Voltage Gain R_L = 2.0 kΩ, V_{CC} = 15 V, for Large V_O Swing, $T_A = T_{high}$ to T_{low}(1)	A_{VOL}	50 25	100 –	– –	25 15	100 –	– –	25 15	100 –	– –	25 15	100 –	– –	25 15	100 –	– –	V/mV
Channel Separation 10 kHz ≤ f ≤ 20 kHz, Input Referenced	CS	–	–120	–	–	–120	–	–	–120	–	–	–120	–	–	–120	–	dB
Common Mode Rejection, R_S ≤ 10 kΩ	CMR	70	85	–	65	70	–	65	70	–	50	70	–	50	70	–	dB
Power Supply Rejection	PSR	65	100	–	65	100	–	65	100	–	50	100	–	50	100	–	dB
Output Voltage – High Limit ($T_A = T_{high}$ to T_{low})(1)	V_{OH}																V
V_{CC} = 5.0 V, R_L = 2.0 kΩ, T_A = 25°C		3.3	3.5	–	3.3	3.5	–	3.3	3.5	–	3.3	3.5	–	3.3	3.5	–	
V_{CC} = 30 V (26 V for LM2902, V), R_L = 2.0 kΩ		26	–	–	26	–	–	26	–	–	22	–	–	22	–	–	
V_{CC} = 30 V (26 V for LM2902, V), R_L = 10 kΩ		27	28	–	27	28	–	27	28	–	23	24	–	23	24	–	

NOTES: 1. T_{low} = –25°C for LM224 T_{high} = +85°C for LM224
= 0°C for LM324, A = +70°C for LM324, A
= –40°C for LM2902 = +105°C for LM2902
= –40°C for LM2902V = +125°C for LM2902V

2. The input common mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3 V. The upper end of the common mode voltage range is V_{CC} –1.7 V.

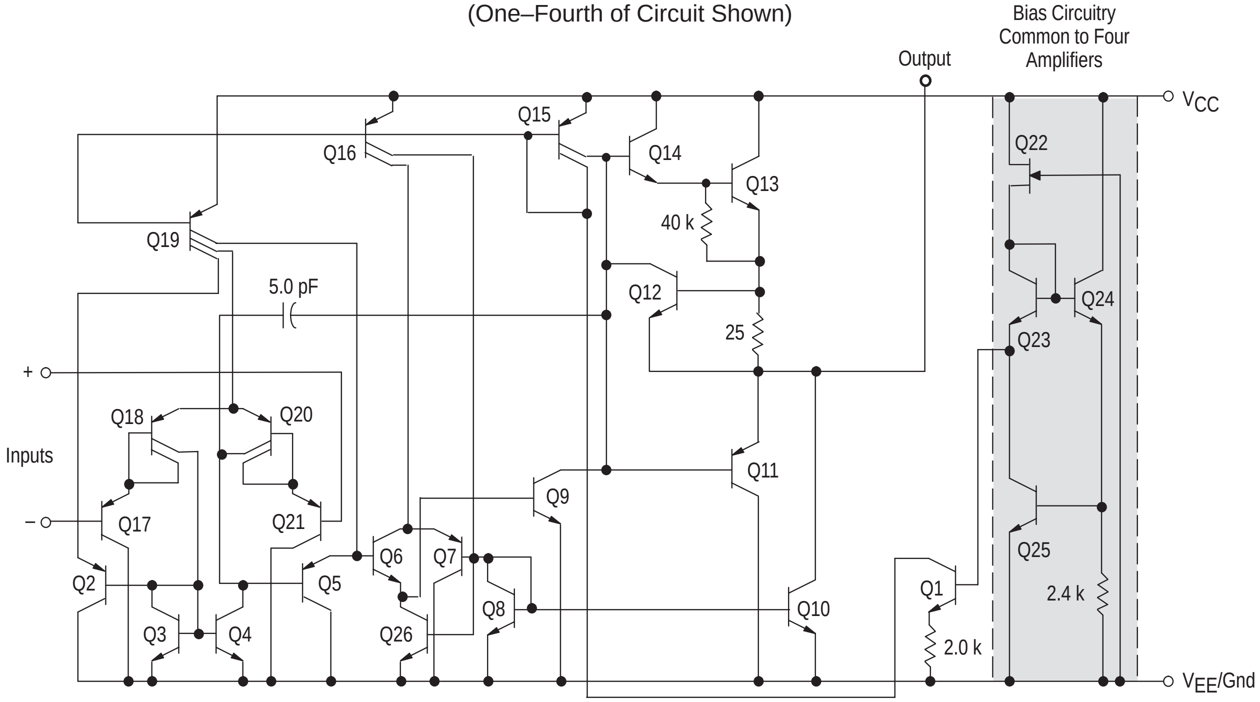
ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, V_{EE} = Gnd, T_A = 25°C, unless otherwise noted.)

Characteristics	Symbol	LM224			LM324A			LM324			LM2902			LM2902V			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Output Voltage – Low Limit, V_{CC} = 5.0 V, R_L = 10 kΩ, T_A = T_{high} to T_{low}(1)	V_{OL}	–	5.0	20	–	5.0	20	–	5.0	20	–	5.0	100	–	5.0	100	mV
Output Source Current (V_{ID} = +1.0 V, V_{CC} = 15 V)	$I_{O\,+}$																mA
T_A = 25°C		20	40	–	20	40	–	20	40	–	20	40	–	20	40	–	
T_A = T_{high} to T_{low}(1)		10	20	–	10	20	–	10	20	–	10	20	–	10	20	–	
Output Sink Current	$I_{O\,-}$																mA
(V_{ID} = –1.0 V, V_{CC} = 15 V) T_A = 25°C		10	20	–	10	20	–	10	20	–	10	20	–	10	20	–	
T_A = T_{high} to T_{low}(1)		5.0	8.0	–	5.0	8.0	–	5.0	8.0	–	5.0	8.0	–	5.0	8.0	–	
(V_{ID} = –1.0 V, V_O = 200 mV, T_A = 25°C)		12	50	–	12	50	–	12	50	–	–	–	–	–	–	–	μA
Output Short Circuit to Ground(3)	I_{SC}	–	40	60	–	40	60	–	40	60	–	40	60	–	40	60	mA
Power Supply Current (T_A = T_{high} to T_{low})(1)	I_{CC}																mA
V_{CC} = 30 V (26 V for LM2902, V), V_O = 0 V, R_L = ∞		–	–	3.0	–	1.4	3.0	–	–	3.0	–	–	3.0	–	–	3.0	
V_{CC} = 5.0 V, V_O = 0 V, R_L = ∞		–	–	1.2	–	0.7	1.2	–	–	1.2	–	–	1.2	–	–	1.2	

NOTES: 1. T_{low} = –25°C for LM224 T_{high} = +85°C for LM224
= 0°C for LM324, A = +70°C for LM324, A
= –40°C for LM2902 = +105°C for LM2902
= –40°C for LM2902V = +125°C for LM2902V

2. The input common mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3 V. The upper end of the common mode voltage range is V_{CC} –1.7 V.

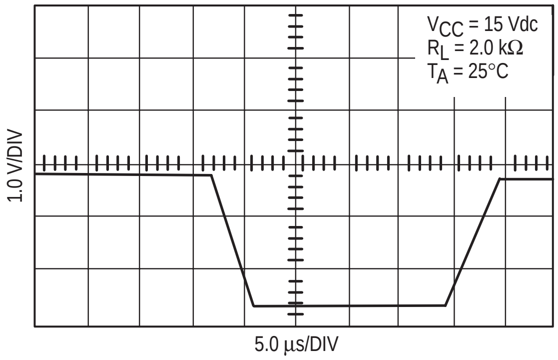
Representative Circuit Diagram
(One–Fourth of Circuit Shown)



CIRCUIT DESCRIPTION

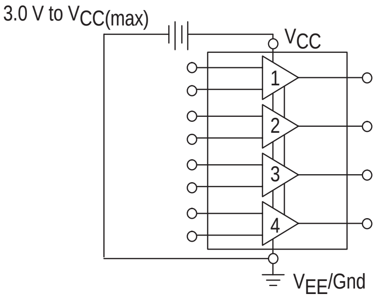
The LM324 series is made using four internally compensated, two–stage operational amplifiers. The first stage of each consists of differential input devices Q20 and Q18 with input buffer transistors Q21 and Q17 and the differential to single ended converter Q3 and Q4. The first stage performs not only the first stage gain function but also performs the level shifting and transconductance reduction functions. By reducing the transconductance, a smaller compensation capacitor (only 5.0 pF) can be employed, thus saving chip area. The transconductance reduction is accomplished by splitting the collectors of Q20 and Q18. Another feature of this input stage is that the input common mode range can include the negative supply or ground, in single supply operation, without saturating either the input devices or the differential to single–ended converter. The second stage consists of a standard current source load amplifier stage.

Large Signal Voltage Follower Response



Each amplifier is biased from an internal–voltage regulator which has a low temperature coefficient thus giving each amplifier good temperature characteristics as well as excellent power supply rejection.

Single Supply



Split Supplies

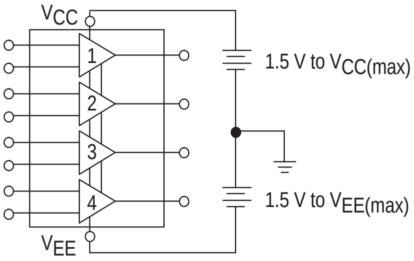


Figure 1. Input Voltage Range

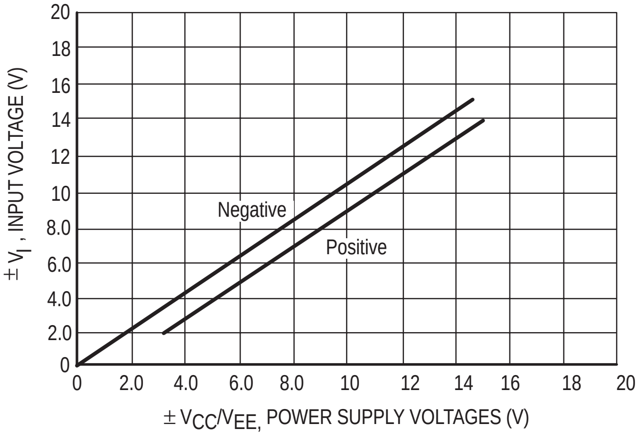


Figure 2. Open Loop Frequency

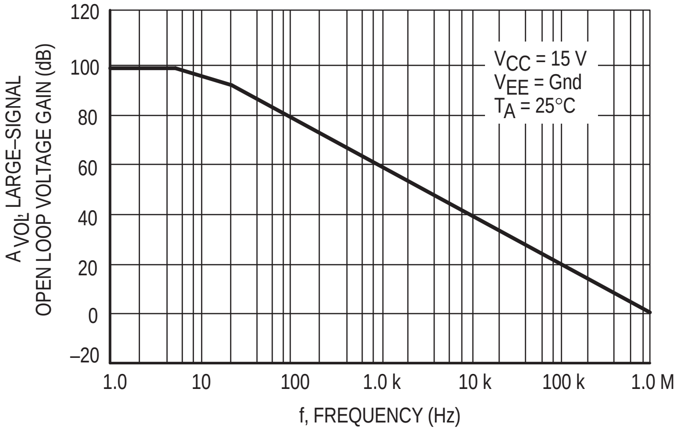


Figure 3. Large–Signal Frequency Response

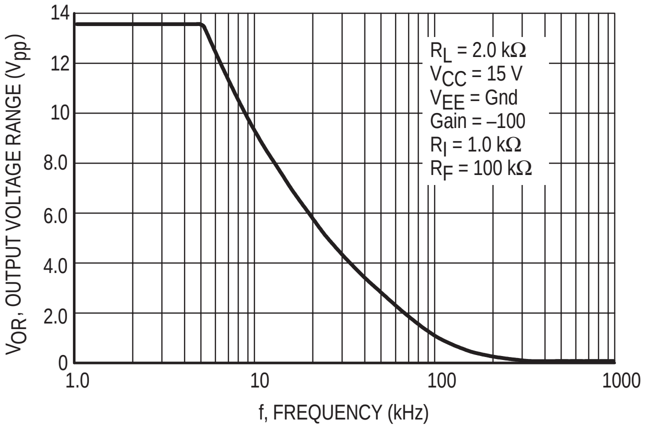


Figure 4. Small–Signal Voltage Follower Pulse Response (Noninverting)

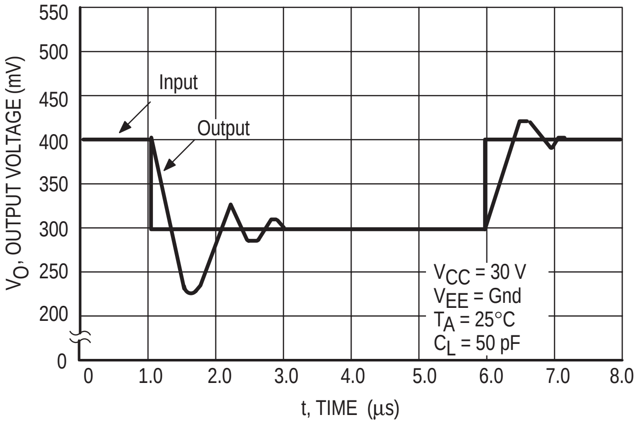


Figure 5. Power Supply Current versus Power Supply Voltage

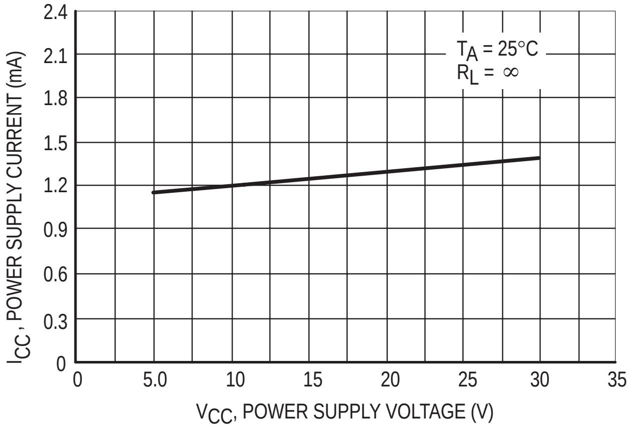


Figure 6. Input Bias Current versus Power Supply Voltage

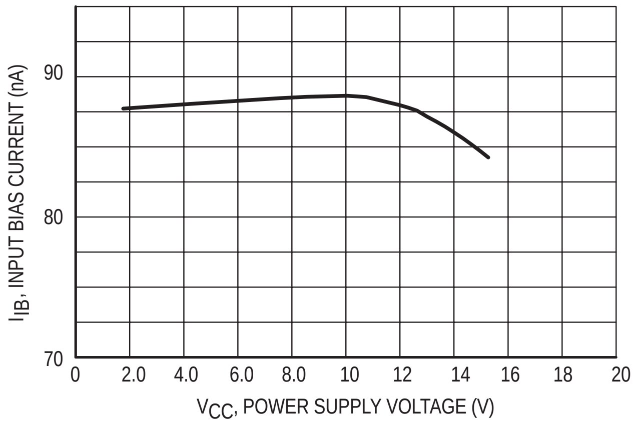


Figure 7. Voltage Reference

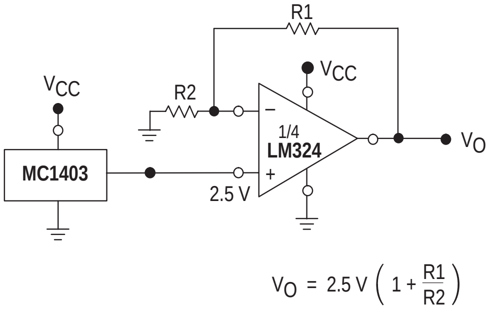


Figure 8. Wien Bridge Oscillator

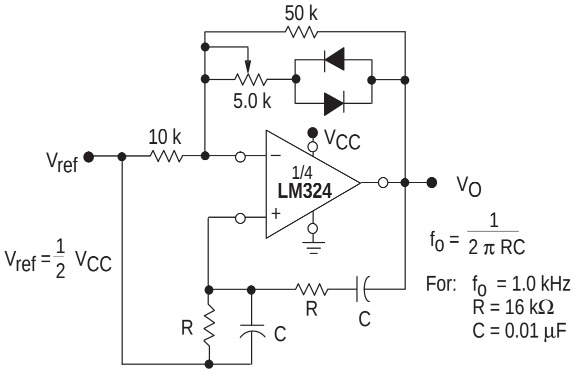


Figure 9. High Impedance Differential Amplifier

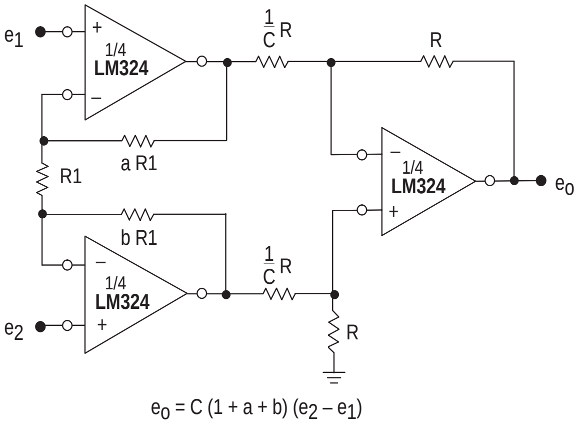


Figure 10. Comparator with Hysteresis

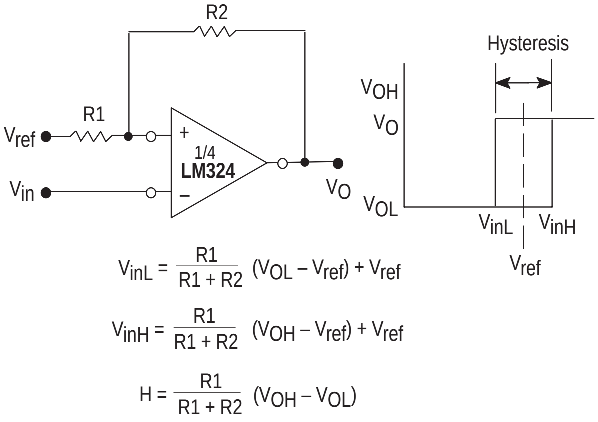


Figure 11. Bi–Quad Filter

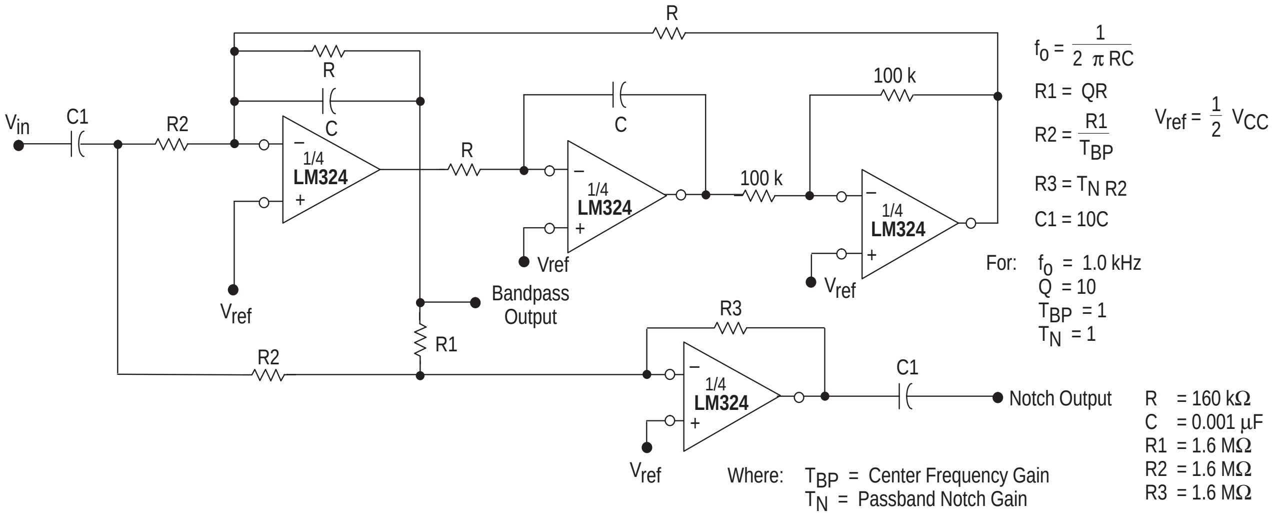
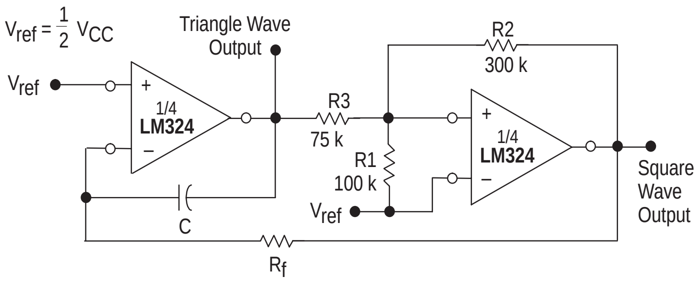
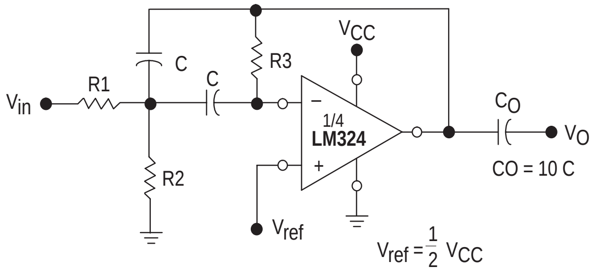


Figure 12. Function Generator



$$f = \frac{R1 + R_C}{4\, C R_f\, R1} \quad \text{if} \quad R3 = \frac{R2\, R1}{R2 + R1}$$

Figure 13. Multiple Feedback Bandpass Filter



Given: f_o = center frequency
$A(f_o)$ = gain at center frequency

Choose value f_o, C

Then: $R3 = \frac{Q}{\pi f_o C}$

$R1 = \frac{R3}{2\, A(f_o)}$

$R2 = \frac{R1\, R3}{4Q^2\, R1 - R3}$

For less than 10% error from operational amplifier, $\frac{Q_o f_o}{BW} < 0.1$

where f_o and BW are expressed in Hz.

If source impedance varies, filter may be preceded with voltage follower buffer to stabilize filter parameters.

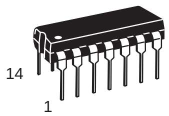
MOTOROLA

LM339, LM339A, LM239, LM239A, LM2901, M2901V, MC3302

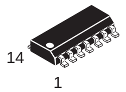
Quad Single Supply Comparators

These comparators are designed for use in level detection, low–level sensing and memory applications in consumer automotive and industrial electronic applications.

- Single or Split Supply Operation
- Low Input Bias Current: 25 nA (Typ)
- Low Input Offset Current: ±5.0 nA (Typ)
- Low Input Offset Voltage: ±1.0 mV (Typ) LM139A Series
- Input Common Mode Voltage Range to Gnd
- Low Output Saturation Voltage: 130 mV (Typ) @ 4.0 mA
- TTL and CMOS Compatible
- ESD Clamps on the Inputs Increase Reliability without Affecting Device Operation



N, P SUFFIX
PLASTIC PACKAGE
CASE 646



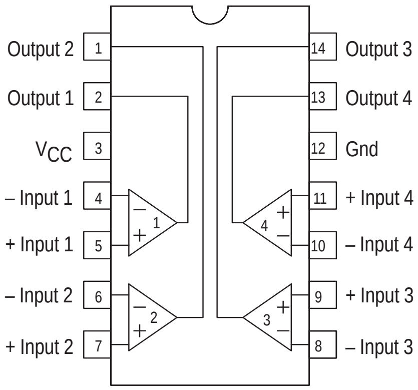
D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO–14)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}		Vdc
LM239, A/LM339A/LM2901, V		+36 or ±18	
MC3302		+30 or ±15	
Input Differential Voltage Range	V_{IDR}		Vdc
LM239, A/LM339A/LM2901, V		36	
MC3302		30	
Input Common Mode Voltage Range	V_{ICMR}	–0.3 to V_{CC}	Vdc
Output Short Circuit to Ground (Note 1)	I_{SC}	Continuous	
Power Dissipation @ T_A = 25°C	P_D		
Plastic Package		1.0	W
Derate above 25°C		8.0	mW/°C
Junction Temperature	T_J	150	°C
Operating Ambient Temperature Range	T_A		°C
LM239, A		–25 to +85	
MC3302		–40 to +85	
LM2901		–40 to +105	
LM2901V		–40 to +125	
LM339, A		0 to +70	
Storage Temperature Range	T_{stg}	–65 to +150	°C

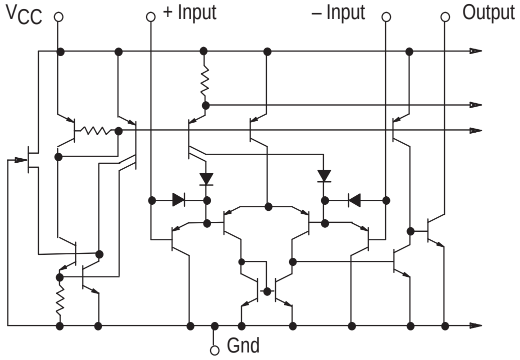
NOTE: 1. The maximum output current may be as high as 20 mA, independent of the magnitude of V_{CC}. Output short circuits to V_{CC} can cause excessive heating and eventual destruction.

PIN CONNECTIONS



(Top View)

Figure 1. Circuit Schematic



NOTE: Diagram shown is for 1 comparator.

ORDERING INFORMATION

Device	Operating Temperature Range	Package
LM239D,AD LM239N,AN	T_A = 25° to +85°C	SO–14 Plastic DIP
LM339D, AD LM339N, AN	T_A = 0° to +70°C	SO–14 Plastic DIP
LM2901D LM2901N	T_A = –40° to +105°C	SO–14 Plastic DIP
LM2901VD LM2901VN	T_A = –40° to +125°C	SO–14 Plastic DIP
MC3302P	T_A = –40° to +85°C	Plastic DIP

ELECTRICAL CHARACTERISTICS (V_{CC} = +5.0 Vdc, T_A = +25°C, unless otherwise noted)

Characteristic	Symbol	LM239A/339A			LM239/339			LM2901/2901V			MC3302			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage (Note 4)	V_{IO}	–	±1.0	±2.0	–	±2.0	±5.0	–	±2.0	±7.0	–	±3.0	±20	mVdc
Input Bias Current (Notes 4, 5) (Output in Analog Range)	I_{IB}	–	25	250	–	25	250	–	25	250	–	25	500	nA
Input Offset Current (Note 4)	I_{IO}	–	±5.0	±50	–	±5.0	±50	–	±5.0	±50	–	±3.0	±100	nA
Input Common Mode Voltage Range	V_{ICMR}	0	–	V_{CC} –1.5	0	–	V_{CC} –1.5	0	–	V_{CC} –1.5	0	–	V_{CC} –1.5	V
Supply Current	I_{CC}													mA
R_L = ∞ (For All Comparators)		–	0.8	2.0	–	0.8	2.0	–	0.8	2.0	–	0.8	2.0	
R_L = ∞, V_{CC} = 30 Vdc		–	1.0	2.5	–	1.0	2.5	–	1.0	2.5	–	1.0	2.5	
Voltage Gain R_L ≥ 15 kΩ, V_{CC} = 15 Vdc	A_{VOL}	50	200	–	50	200	–	25	100	–	25	100	–	V/mV
Large Signal Response Time V_I = TTL Logic Swing, V_{ref} = 1.4 Vdc, V_{RL} = 5.0 Vdc, R_L = 5.1 kΩ	–	–	300	–	–	300	–	–	300	–	–	300	–	ns
Response Time (Note 6) V_{RL} = 5.0 Vdc, R_L = 5.1 kΩ	–	–	1.3	–	–	1.3	–	–	1.3	–	–	1.3	–	µs
Output Sink Current V_I (–) ≥ +1.0 Vdc, V_I(+) = 0, V_O ≤ 1.5 Vdc	I_{Sink}	6.0	16	–	6.0	16	–	6.0	16	–	6.0	16	–	mA
Saturation Voltage V_I(–) ≥ +1.0 Vdc, V_I(+) = 0, I_{sink} ≤ 4.0 mA	V_{sat}	–	130	400	–	130	400	–	130	400	–	130	500	mV
Output Leakage Current V_I(+) ≥ +1.0 Vdc, V_I(–) = 0, V_O = +5.0 Vdc	I_{OL}	–	0.1	–	–	0.1	–	–	0.1	–	–	0.1	–	nA

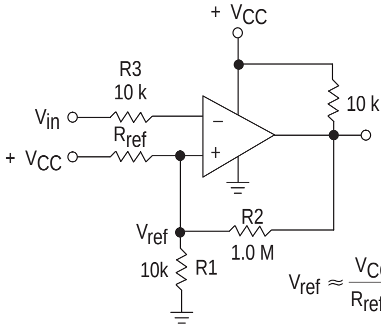
PERFORMANCE CHARACTERISTICS (V_{CC} = +5.0 Vdc, T_A = T_{low} to T_{high} [Note 3])

Characteristic	Symbol	LM239A/339A			LM239/339			LM2901/2901V			MC3302			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage (Note 4)	V_{IO}	–	–	±4.0	–	–	±9.0	–	–	±15	–	–	±40	mVdc
Input Bias Current (Notes 4, 5) (Output in Analog Range)	I_{IB}	–	–	400	–	–	400	–	–	500	–	–	1000	nA
Input Offset Current (Note 4)	I_{IO}	–	–	±150	–	–	±150	–	–	±200	–	–	±300	nA
Input Common Mode Voltage Range	V_{ICMR}	0	–	V_{CC} –2.0	0	–	V_{CC} –2.0	0	–	V_{CC} –2.0	0	–	V_{CC} –2.0	V
Saturation Voltage V_I(–) ≥ +1.0 Vdc, V_I(+) = 0, I_{sink} ≤ 4.0 mA	V_{sat}	–	–	700	–	–	700	–	–	700	–	–	700	mV
Output Leakage Current V_I(+) ≥ +1.0 Vdc, V_I(–) = 0, V_O = 30 Vdc	I_{OL}	–	–	1.0	–	–	1.0	–	–	1.0	–	–	1.0	µA
Differential Input Voltage All V_I ≥ 0 Vdc	V_{ID}	–	–	V_{CC}	–	–	V_{CC}	–	–	V_{CC}	–	–	V_{CC}	Vdc

NOTES: 3. (LM239/239A) T_{low} = –25°C, T_{high} = +85°
(LM339/339A) T_{low} = 0°C, T_{high} = +70°C
(MC3302) T_{low} = –40°C, T_{high} = +85°C
(LM2901) T_{low} = –40°C, T_{high} = +105°
(LM2901V) T_{low} = –40°C, T_{high} = +125°C

4. At the output switch point, $V_O \simeq$ 1.4 Vdc, R_S ≤ 100 Ω 5.0 Vdc ≤ V_{CC} ≤ 30 Vdc, with the inputs over the full common mode range (0 Vdc to V_{CC} –1.5 Vdc).
5. The bias current flows out of the inputs due to the PNP input stage. This current is virtually constant, independent of the output state.
6. The response time specified is for a 100 mV input step with 5.0 mV overdrive. For larger signals, 300 ns is typical.

Figure 2. Inverting Comparator with Hystersis



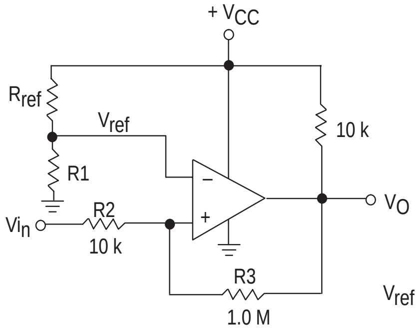
$$V_{ref} \approx \frac{V_{CC}\,R1}{R_{ref} + R1}$$

$$R3 \simeq R1\,//\,R_{ref}\,//\,R2$$

$$V_H = \frac{R1\,//\,R_{ref}}{R1//\,R_{ref} + R2}\,[V_{O(max)} - V_{O(min)}]$$

$$R2 \gg Rref\,//\,R1$$

Figure 3. Noninverting Comparator with Hysteresis



$$V_{ref} = \frac{V_{CC}\,R1}{R_{ref} + R1}$$

$$R2 \approx R1\,//\,R_{ref}$$

Amount of Hysteresis V_H

$$V_H = \frac{R2}{R2 + R3}\,[(V_{O(max)} - V_{O(min)}]$$

Typical Characteristics

(V_{CC} = 15 Vdc, T_A = +25°C (each comparator) unless otherwise noted.)

Figure 4. Normalized Input Offset Voltage

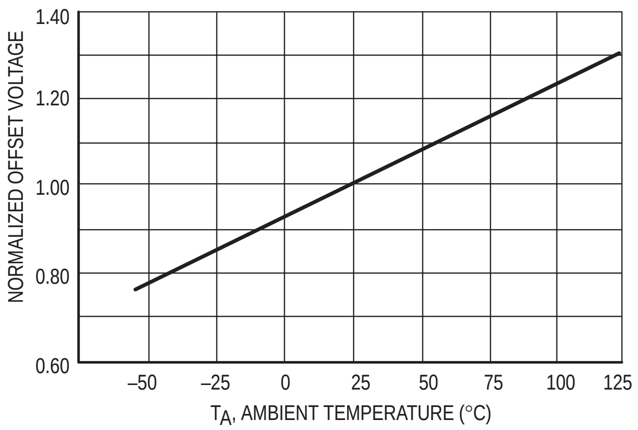


Figure 5. Input Bias Current

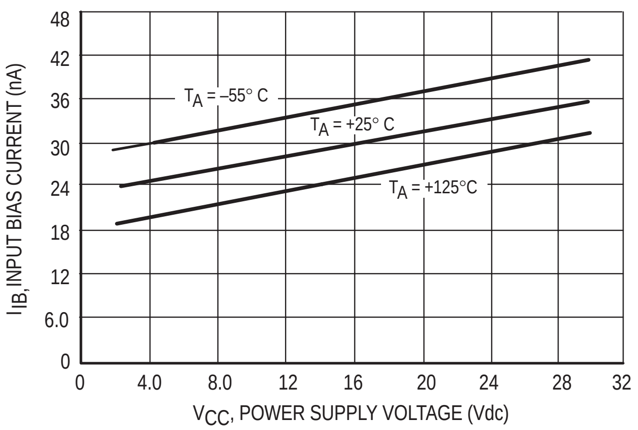


Figure 6. Output Sink Current versus Output Saturation Voltage

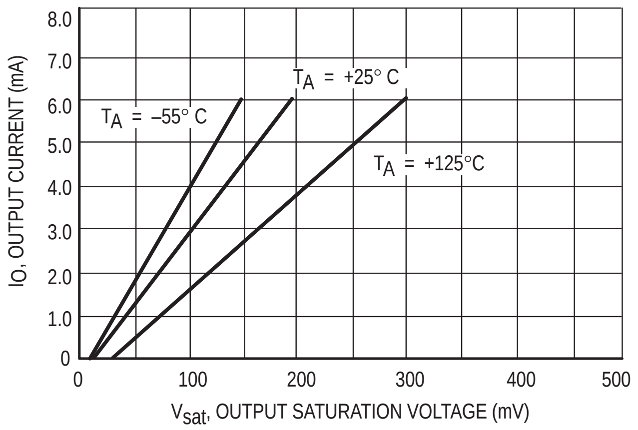
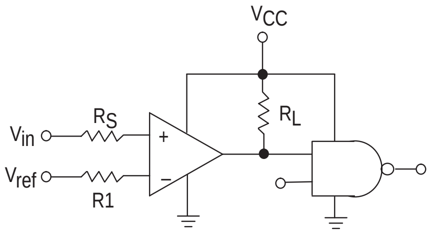


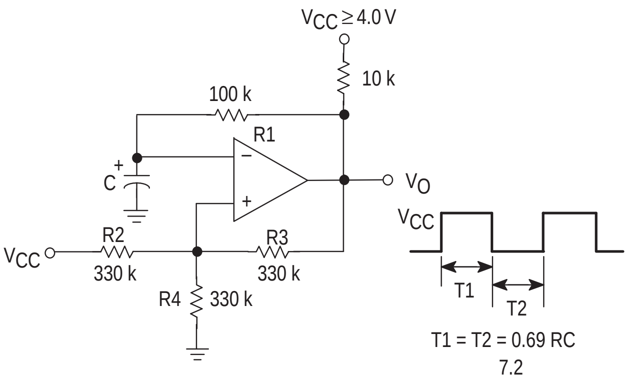
Figure 7. Driving Logic



R_S = Source Resistance
$R1 \simeq R_S$

Logic	Device	V_{CC} (V)	R_L kΩ
CMOS	1/4 MC14001	+15	100
TTL	1/4 MC7400	+5.0	10

Figure 8. Squarewave Oscillator



$T1 = T2 = 0.69\ RC$

$f \approx \dfrac{7.2}{C(\mu F)}$

$R2 = R3 = R4$

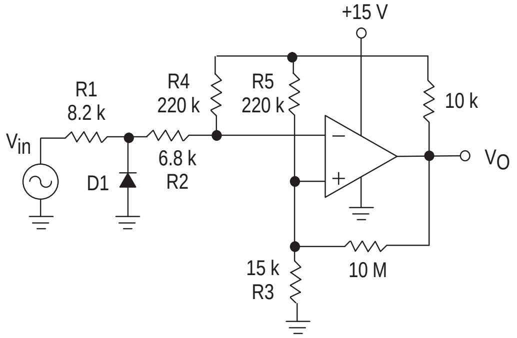
$R1 \approx R2\ //\ R3\ //\ R4$

APPLICATIONS INFORMATION

These quad comparators feature high gain, wide bandwidth characteristics. This gives the device oscillation tendencies if the outputs are capacitively coupled to the inputs via stray capacitance. This oscillation manifests itself during output transitions (V_{OL} to V_{OH}). To alleviate this situation input resistors < 10 kΩ should be used. The addition of positive feedback (< 10 mV) is also recommended. It is good design practice to ground all unused input pins.

Differential input voltages may be larger than supply voltages without damaging the comparator’s inputs. Voltages more negative than –300 mV should not be used.

Figure 9. Zero Crossing Detector (Single Supply)



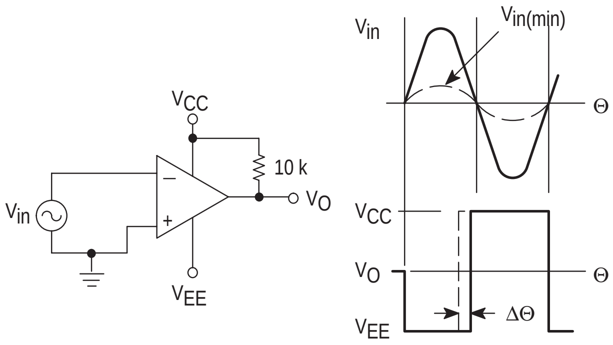
D1 prevents input from going negative by more than 0.6 V.

$R1 + R2 = R3$

$R3 \le \dfrac{R5}{10}$ for small error in zero crossing

Figure 10. Zero Crossing Detector (Split Supplies)

$V_{in(min)} \approx 0.4$ V peak for 1% phase distortion (ΔΘ).



MOTOROLA

LM348

Differential Input Operational Amplifier

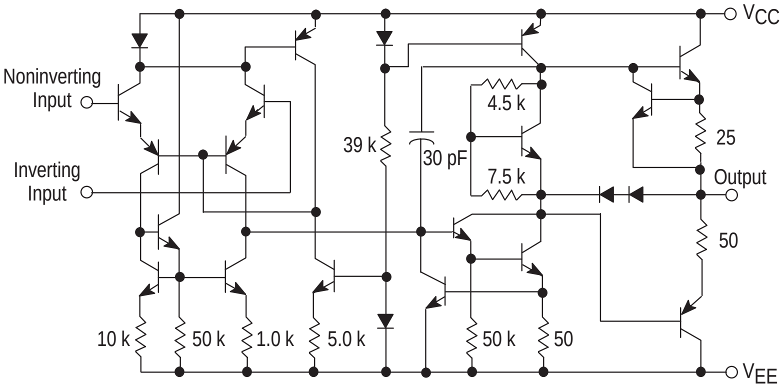
The LM348 is a true quad MC1741. Integrated on a single monolithic chip are four independent, low power operational amplifiers which have been designed to provide operating characteristics identical to those of the industry standard MC1741, and can be applied with no change in circuit performance. In addition, the total supply current for all four amplifiers is comparable to the supply current of a single MC1741. Other features include input offset currents and input bias currents which are much less than the MC1741 industry standard.

The LM348 can be used in applications where amplifier matching or high packing density is important. Other applications include high impedance buffer amplifiers and active filter amplifiers.

- Each Amplifier is Functionally Equivalent to the MC1741
- Low Input Offset and Input Bias Currents
- Class AB Output Stage Eliminates Crossover Distortion
- Pin Compatible with MC3403 and LM324
- True Differential Inputs
- Internally Frequency Compensated
- Short Circuit Protection
- Low Power Supply Current (0.6 mA/Amplifier)

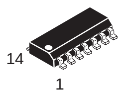
Representative Schematic Diagram

(1/4 of Circuit Shown)



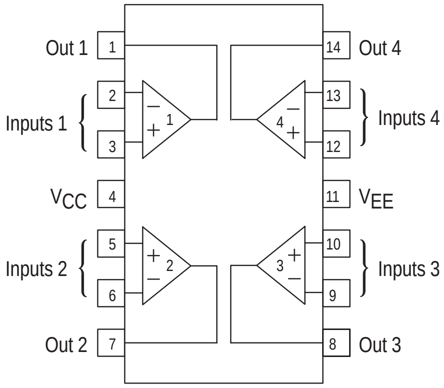
DIFFERENTIAL INPUT OPERATIONAL AMPLIFIER

SEMICONDUCTOR TECHNICAL DATA



D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO–14)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
LM348D	T_A = 0° to +70°C	SO–14

MAXIMUM RATINGS (T_A = +25°C, unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC} V_{EE}	+18 –18	Vdc
Input Differential Voltage	V_{ID}	±36	V
Input Common Mode Voltage	V_{ICM}	±18	V
Output Short Circuit Duration	t_{SC}	Continuous	
Operating Ambient Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	–55 to +125	°C
Junction Temperature	T_J	150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = –15 V, T_A = 25°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Offset Voltage (R_S ≤ 10 k)	V_{IO}	–	1.0	6.0	mV
Input Offset Current Input Bias Current	I_{IO} I_{IB}	– –	4.0 30	50 200	nA
Input Resistance	r_i	0.8	2.5	–	MΩ
Common Mode Input Voltage Range	V_{ICR}	±12	–	–	V
Large Signal Voltage Gain (R_L ≥ 2.0 k, V_O = ±10 V)	A_{VOL}	25	160	–	V/mV
Channel Separation (f = 1.0 Hz to 20 kHz)	–	–	–120	–	dB
Common Mode Rejection (R_S ≤ 10 k) Supply Voltage Rejection (R_S ≤ 10 k)	CMR PSR	70 77	90 96	– –	dB
Output Voltage Swing	V_O				V
(R_L ≥ 10 k)		±12	±13	–	
(R_L ≥ 2.0 k)		±10	±12	–	
Output Short Circuit Current	I_{SC}	–	25	–	mA
Supply Current (All Amplifiers)	I_D	–	2.4	4.5	mA
Small Signal Bandwidth (A_V = 1)	BW	–	1.0	–	MHz
Phase Margin (A_V = 1)	ϕm	–	60	–	Degrees
Slew Rate (A_V = 1)	SR	–	0.5	–	V/µs

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = –15 V, T_A = *T_{high} to T_{low}, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Offset Voltage (R_S ≤ 10 kΩ)	V_{IO}	–	–	7.5	mV
Input Offset Current Input Bias Current	I_{IO} I_{IB}	– –	– –	100 400	nA
Common Mode Input Voltage Range	V_{ICR}	±12	–	–	V
Large Signal Voltage Gain (R_L ≥ 2 k, V_O = ±10 V)	A_{VOL}	15	–	–	V/mV
Common Mode Rejection (R_S ≤ 10 k) Supply Voltage Rejection (R_S ≤ 10 k)	CMR PSR	70 77	90 96	– –	dB
Output Voltage Swing	V_O				V
(R_L ≥ 10 k)		±12	±13	–	
(R_L ≥ 2 k)		±10	±12	–	

* T_{high} = 70°C. T_{low} = 0°C.

NOTE: Any of the amplifier outputs can be shorted to ground indefinitely; however, more than one should not be simultaneously shorted or the maximum junction temperature will be exceeded.

Figure 1. Power Bandwidth (Large Signal Swing versus Frequency)

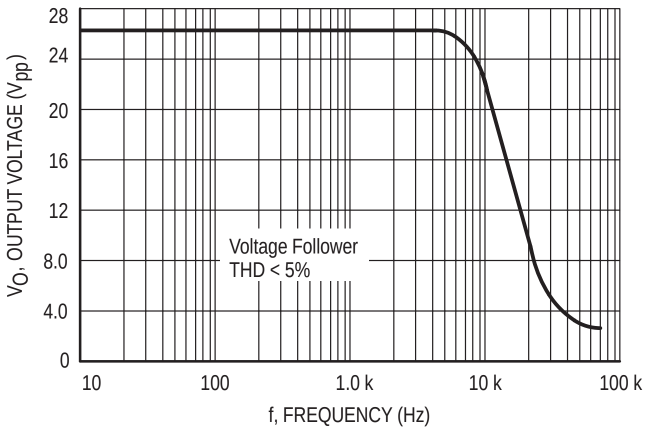


Figure 2. Open Loop Frequency Response

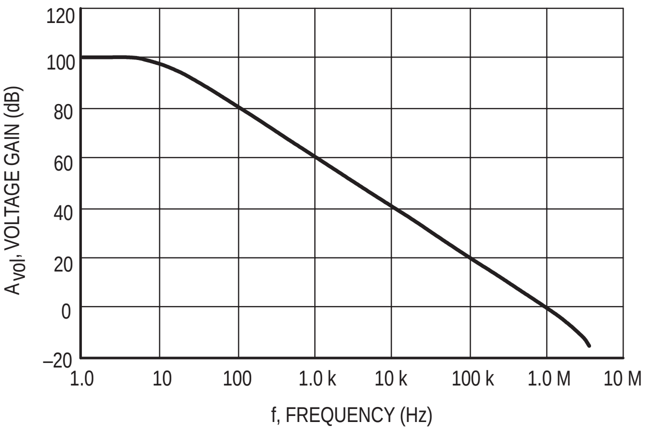


Figure 3. Positive Output Voltage Swing versus Load Resistance

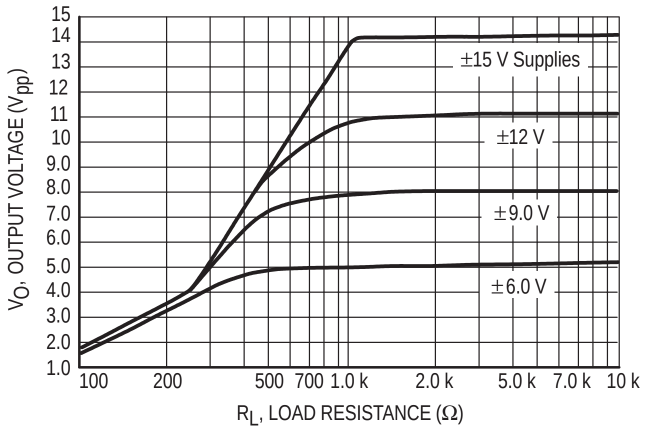


Figure 4. Negative Output Voltage Swing versus Load Resistance

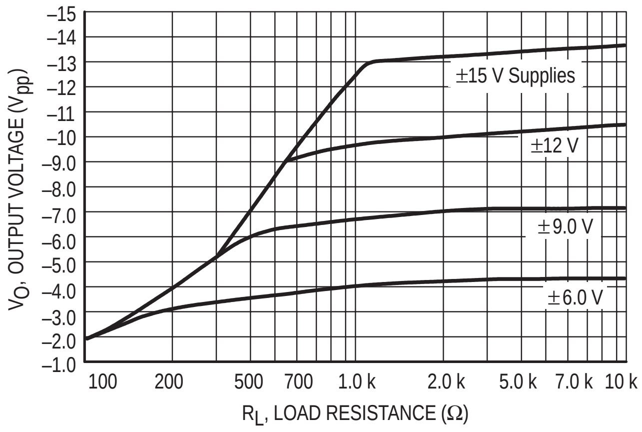


Figure 5. Output Voltage Swing versus Load Resistance (Single Supply Operation)

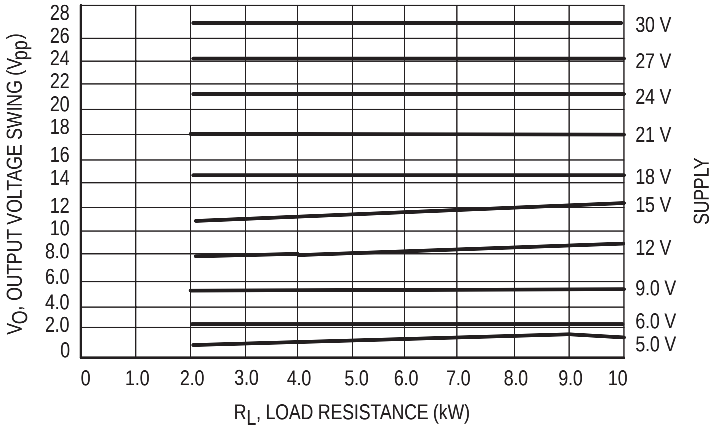


Figure 6. Noninverting Pulse Response

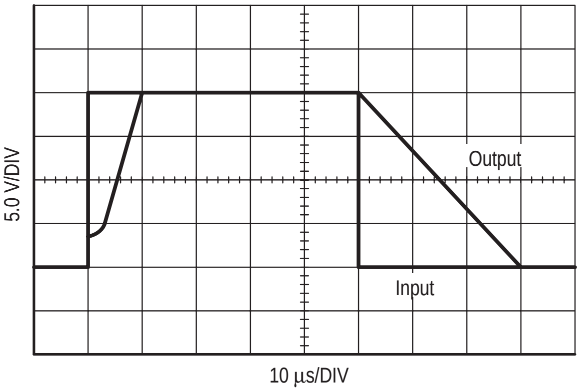
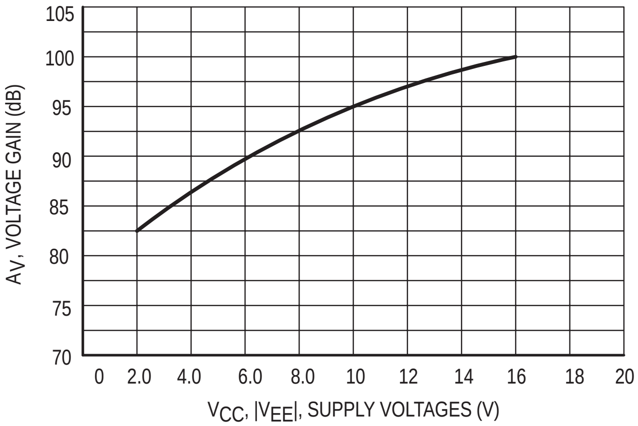
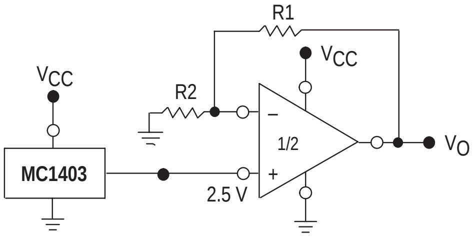


Figure 7. Open Loop Voltage Gain versus Supply Voltage



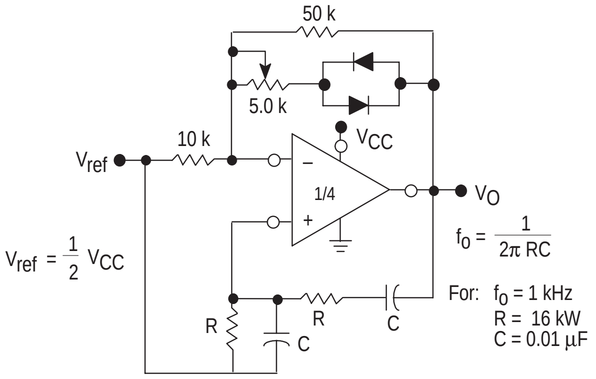
APPLICATIONS INFORMATION

Figure 8. Voltage Reference



$$V_O = 2.5\text{ V}\left(1 + \frac{R1}{R2}\right)$$

Figure 9. Wien Bridge Oscillator

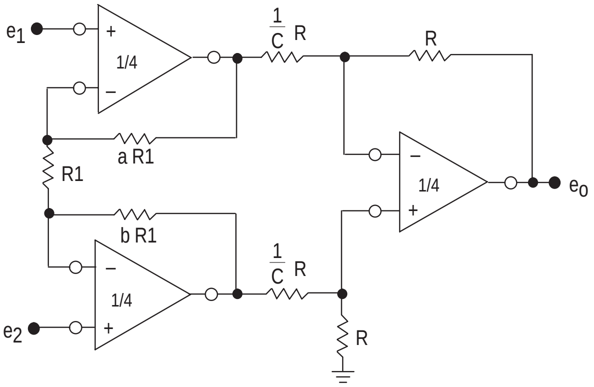


$$V_{ref} = \frac{1}{2} V_{CC}$$

$$f_0 = \frac{1}{2\pi RC}$$

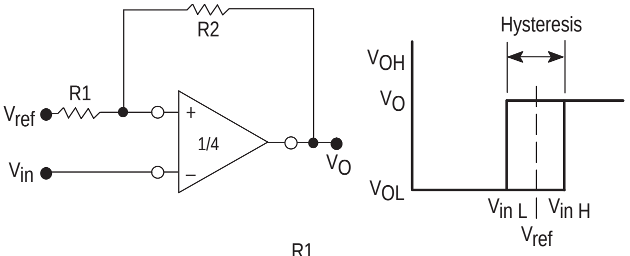
For: $f_0 = 1$ kHz
$R = 16$ kW
$C = 0.01$ µF

Figure 10. High Impedance Differential Amplifier



$$e_0 = C\,(1 + a + b)\ (e_2 - e_1)$$

Figure 11. Comparator with Hysteresis



$$V_{in\,L} = \frac{R1}{R1 + R2}\ (V_{OL} - V_{ref}) + V_{ref}$$

$$V_{in\,H} = \frac{R1}{R1 + R2}\ (V_{OH} - V_{ref}) + V_{ref}$$

$$H = \frac{R1}{R1 + R2}\ (V_{OH} - V_{OL})$$

Figure 12. High Impedance Instrumentation Buffer/Filter

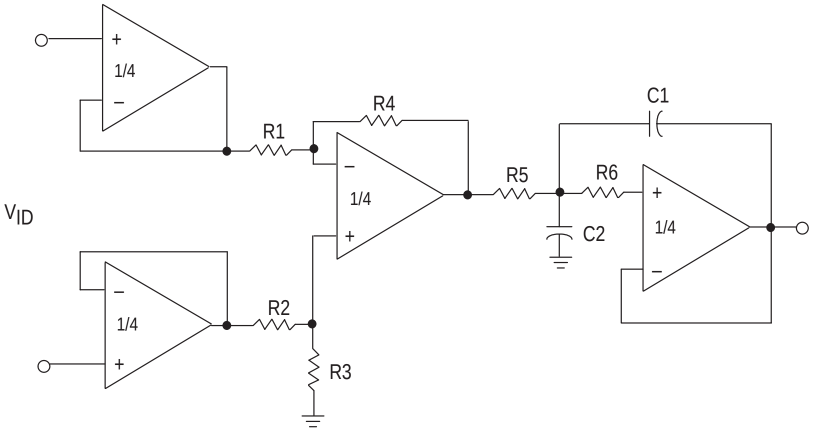
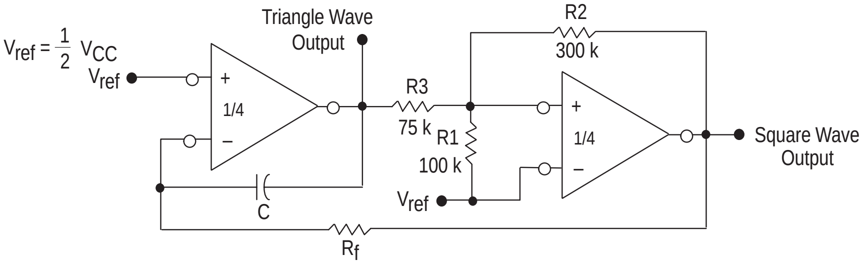
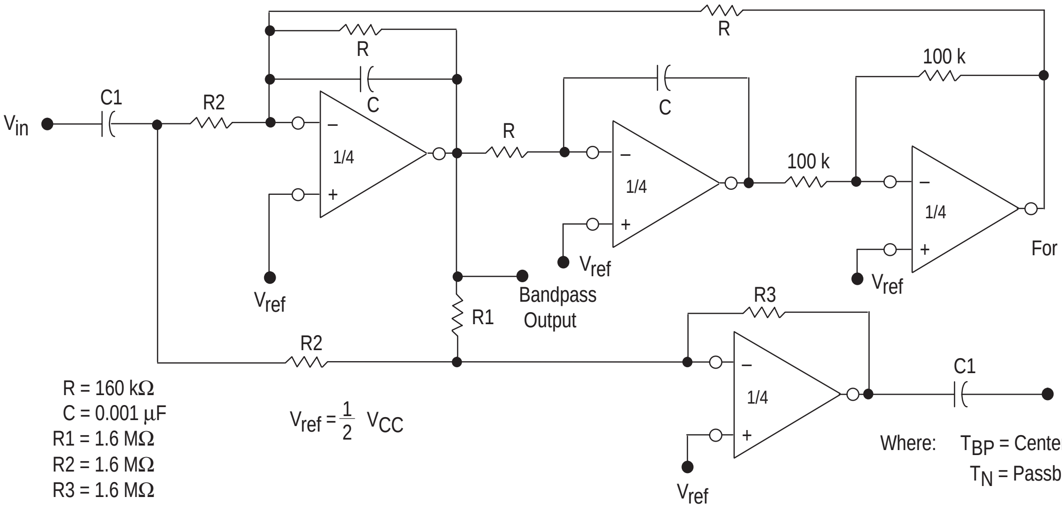


Figure 13. Function Generator



$$f = \frac{R1 + R_C}{4\ CR_f\ R1} \quad \text{if} \quad R3 = \frac{R2\ R1}{R2 + R1}$$

Figure 14. Bi–Quad Filter



R = 160 kΩ
C = 0.001 µF
R1 = 1.6 MΩ
R2 = 1.6 MΩ
R3 = 1.6 MΩ

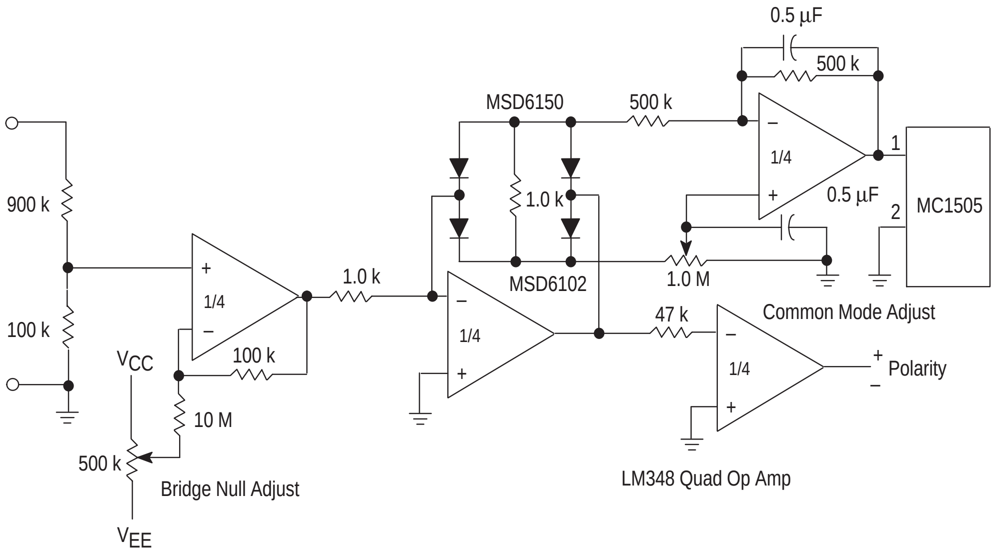
$V_{ref} = \frac{1}{2}\ V_{CC}$

$f_o = \frac{1}{2\ \pi\ RC}$
R1 = QR
$R2 = \frac{R1}{T_{BP}}$
$R3 = T_N\ R2$
C1 = 10C

For : f_o = 1.0 kHz
Q = 10
T_{BP} = 1
T_N = 1

Where: T_{BP} = Center Frequency Gain
T_N = Passband Notch Gain

Figure 15. Absolute Value DVM Front End



MOTOROLA

LM358, LM258, LM2904, LM2904V

Dual Low Power Operational Amplifiers

Utilizing the circuit designs perfected for recently introduced Quad Operational Amplifiers, these dual operational amplifiers feature 1) low power drain, 2) a common mode input voltage range extending to ground/V_{EE}, 3) single supply or split supply operation and 4) pinouts compatible with the popular MC1558 dual operational amplifier. The LM158 series is equivalent to one–half of an LM124.

These amplifiers have several distinct advantages over standard operational amplifier types in single supply applications. They can operate at supply voltages as low as 3.0 V or as high as 32 V, with quiescent currents about one–fifth of those associated with the MC1741 (on a per amplifier basis). The common mode input range includes the negative supply, thereby eliminating the necessity for external biasing components in many applications. The output voltage range also includes the negative power supply voltage.

- Short Circuit Protected Outputs
- True Differential Input Stage
- Single Supply Operation: 3.0 V to 32 V
- Low Input Bias Currents
- Internally Compensated
- Common Mode Range Extends to Negative Supply
- Single and Split Supply Operation
- Similar Performance to the Popular MC1558
- ESD Clamps on the Inputs Increase Ruggedness of the Device without Affecting Operation

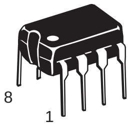
MAXIMUM RATINGS (T_A = +25°C, unless otherwise noted.)

Rating	Symbol	LM258 LM358	LM2904 LM2904V	Unit
Power Supply Voltages Single Supply Split Supplies	 V_{CC} V_{CC}, V_{EE}	 32 ±16	 26 ±13	Vdc
Input Differential Voltage Range (Note 1)	V_{IDR}	±32	±26	Vdc
Input Common Mode Voltage Range (Note 2)	V_{ICR}	–0.3 to 32	–0.3 to 26	Vdc
Output Short Circuit Duration	t_{SC}	Continuous		
Junction Temperature	T_J	150		°C
Storage Temperature Range	T_{stg}	–55 to +125		°C
Operating Ambient Temperature Range LM258 LM358 LM2904 LM2904V	T_A	 –25 to +85 0 to +70 – –	 – – –40 to +105 –40 to +125	°C

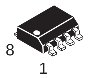
NOTES: 1. Split Power Supplies.
2. For Supply Voltages less than 32 V for the LM258/358 and 26 V for the LM2904, the absolute maximum input voltage is equal to the supply voltage.

DUAL DIFFERENTIAL INPUT OPERATIONAL AMPLIFIERS

SEMICONDUCTOR TECHNICAL DATA

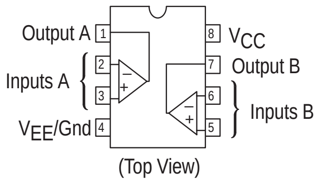


N SUFFIX
PLASTIC PACKAGE
CASE 626



D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

PIN CONNECTIONS



ORDERING INFORMATION

Device	Operating Temperature Range	Package
LM2904D	T_A = –40° to +105°C	SO–8
LM2904N		Plastic DIP
LM2904VD	T_A = –40° to +125°C	SO–8
LM2904VN		Plastic DIP
LM258D	T_A = –25° to +85°C	SO–8
LM258N		Plastic DIP
LM358D	T_A = 0° to +70°C	SO–8
LM358N		Plastic DIP

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, V_{EE} = Gnd, T_A = 25°C, unless otherwise noted.)

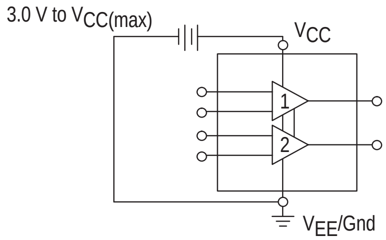
Characteristic	Symbol	LM258			LM358			LM2904			LM2904V			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage V_{CC} = 5.0 V to 30 V (26 V for LM2904, V), V_{IC} = 0 V to V_{CC} –1.7 V, V_O ≃ 1.4 V, R_S = 0 Ω	V_{IO}													mV
T_A = 25°C		–	2.0	5.0	–	2.0	7.0	–	2.0	7.0	–	–	–	
T_A = T_{high} (Note 1)		–	–	7.0	–	–	9.0	–	–	10	–	–	13	
T_A = T_{low} (Note 1)		–	–	2.0	–	–	9.0	–	–	10	–	–	10	
Average Temperature Coefficient of Input Offset Voltage T_A = T_{high} to T_{low} (Note 1)	$\Delta V_{IO}/\Delta T$	–	7.0	–	–	7.0	–	–	7.0	–	–	7.0	–	µV/°C
Input Offset Current	I_{IO}	–	3.0	30	–	5.0	50	–	5.0	50	–	5.0	50	nA
T_A = T_{high} to T_{low} (Note 1)		–	–	100	–	–	150	–	45	200	–	45	200	
Input Bias Current	I_{IB}	–	–45	–150	–	–45	–250	–	–45	–250	–	–45	–250	
T_A = T_{high} to T_{low} (Note 1)		–	–50	–300	–	–50	–500	–	–50	–500	–	–50	–500	
Average Temperature Coefficient of Input Offset Current T_A = T_{high} to T_{low} (Note 1)	$\Delta I_{IO}/\Delta T$	–	10	–	–	10	–	–	10	–	–	10	–	pA/°C
Input Common Mode Voltage Range (Note 2), V_{CC} = 30 V (26 V for LM2904, V)	V_{ICR}	0	–	28.3	0	–	28.3	0	–	24.3	0	–	24.3	V
V_{CC} = 30 V (26 V for LM2904, V), T_A = T_{high} to T_{low}		0	–	28	0	–	28	0	–	24	0	–	24	
Differential Input Voltage Range	V_{IDR}	–	–	V_{CC}	–	–	V_{CC}	–	–	V_{CC}	–	–	V_{CC}	V
Large Signal Open Loop Voltage Gain	A_{VOL}													V/mV
R_L = 2.0 kΩ, V_{CC} = 15 V, For Large V_O Swing,		50	100	–	25	100	–	25	100	–	25	100	–	
T_A = T_{high} to T_{low} (Note 1)		25	–	–	15	–	–	15	–	–	15	–	–	
Channel Separation 1.0 kHz ≤ f ≤ 20 kHz, Input Referenced	CS	–	–120	–	–	–120	–	–	–120	–	–	–120	–	dB
Common Mode Rejection R_S ≤ 10 kΩ	CMR	70	85	–	65	70	–	50	70	–	50	70	–	dB
Power Supply Rejection	PSR	65	100	–	65	100	–	50	100	–	50	100	–	dB
Output Voltage–High Limit (T_A = T_{high} to T_{low}) (Note 1)	V_{OH}													V
V_{CC} = 5.0 V, R_L = 2.0 kΩ, T_A = 25°C		3.3	3.5	–	3.3	3.5	–	3.3	3.5	–	3.3	3.5	–	
V_{CC} = 30 V (26 V for LM2904, V), R_L = 2.0 kΩ		26	–	–	26	–	–	22	–	–	22	–	–	
V_{CC} = 30 V (26 V for LM2904, V), R_L = 10 kΩ		27	28	–	27	28	–	23	24	–	23	24	–	
Output Voltage–Low Limit V_{CC} = 5.0 V, R_L = 10 kΩ, T_A = T_{high} to T_{low} (Note 1)	V_{OL}	–	5.0	20	–	5.0	20	–	5.0	20	–	5.0	20	mV
Output Source Current V_{ID} = +1.0 V, V_{CC} = 15 V	I_{O+}	20	40	–	20	40	–	20	40	–	20	40	–	mA
Output Sink Current	I_{O-}													
V_{ID} = –1.0 V, V_{CC} = 15 V		10	20	–	10	20	–	10	20	–	10	20	–	mA
V_{ID} = –1.0 V, V_O = 200 mV		12	50	–	12	50	–	–	–	–	–	–	–	µA
Output Short Circuit to Ground (Note 3)	I_{SC}	–	40	60	–	40	60	–	40	60	–	40	60	mA
Power Supply Current (T_A = T_{high} to T_{low}) (Note 1)	I_{CC}													mA
V_{CC} = 30 V (26 V for LM2904, V), V_O = 0 V, R_L = ∞		–	1.5	3.0	–	1.5	3.0	–	1.5	3.0	–	1.5	3.0	
V_{CC} = 5 V, V_O = 0 V, R_L = ∞		–	0.7	1.2	–	0.7	1.2	–	0.7	1.2	–	0.7	1.2	

NOTES: 1. T_{low} = –40°C for LM2904 T_{high} = +105°C for LM2904
= –40°C for LM2904V = +125°C for LM2904V
= –25°C for LM258 = +85°C for LM258
= 0°C for LM358 = +70°C for LM358

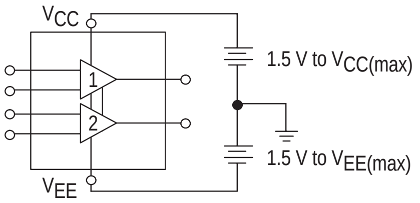
2. The input common mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3 V. The upper end of the common mode voltage range is V_{CC} –1.7 V.

3. Short circuits from the output to V_{CC} can cause excessive heating and eventual destruction. Destructive dissipation can result from simultaneous shorts on all amplifiers.

Single Supply

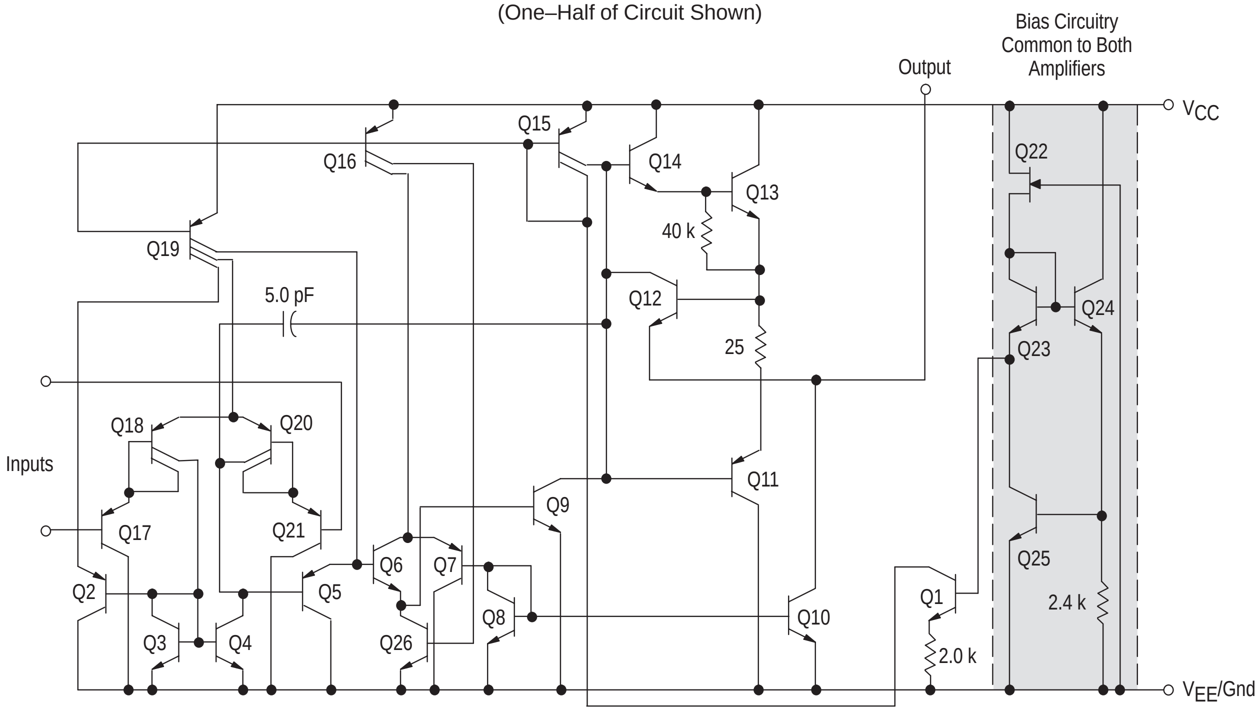


Split Supplies



Representative Schematic Diagram

(One–Half of Circuit Shown)



CIRCUIT DESCRIPTION

The LM258 series is made using two internally compensated, two–stage operational amplifiers. The first stage of each consists of differential input devices Q20 and Q18 with input buffer transistors Q21 and Q17 and the differential to single ended converter Q3 and Q4. The first stage performs not only the first stage gain function but also performs the level shifting and transconductance reduction functions. By reducing the transconductance, a smaller compensation capacitor (only 5.0 pF) can be employed, thus saving chip area. The transconductance reduction is accomplished by splitting the collectors of Q20 and Q18. Another feature of this input stage is that the input common mode range can include the negative supply or ground, in single supply operation, without saturating either the input devices or the differential to single–ended converter. The second stage consists of a standard current source load amplifier stage.

Each amplifier is biased from an internal–voltage regulator which has a low temperature coefficient thus giving each amplifier good temperature characteristics as well as excellent power supply rejection.

Large Signal Voltage Follower Response

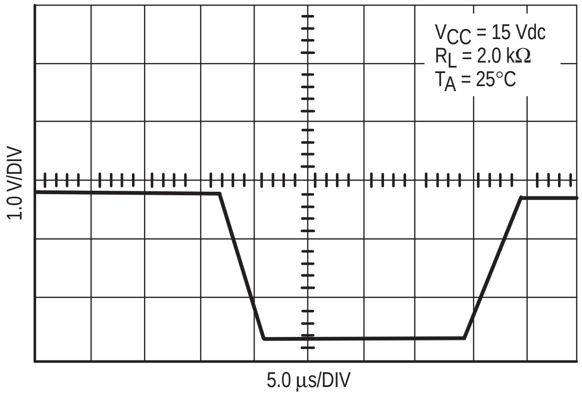


Figure 1. Input Voltage Range

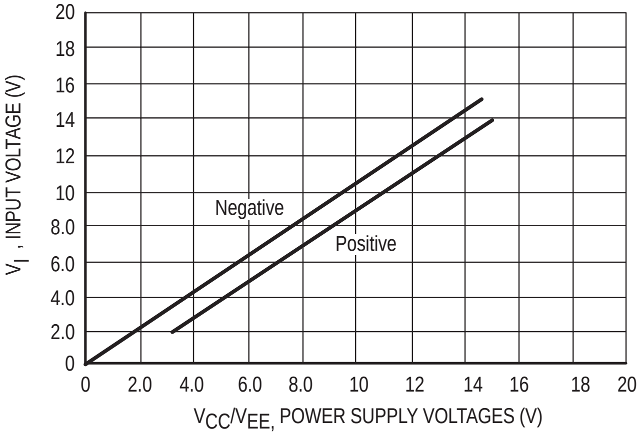


Figure 2. Large–Signal Open Loop Voltage Gain

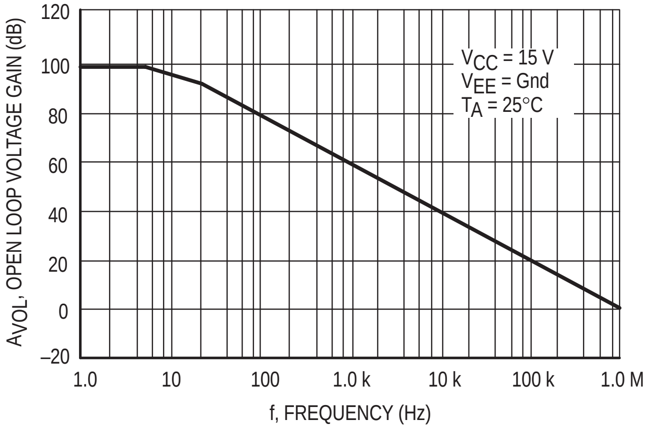


Figure 3. Large–Signal Frequency Response

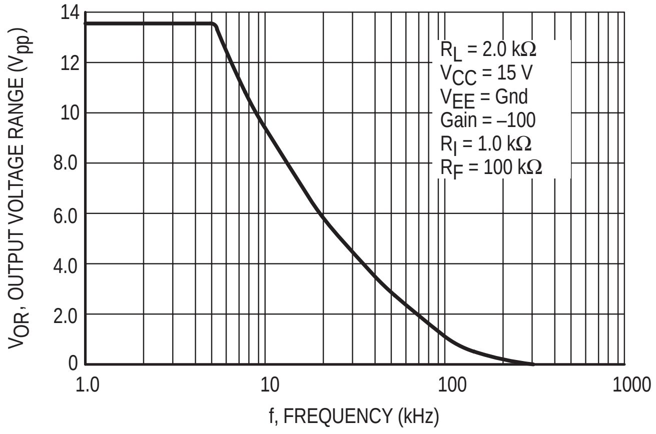


Figure 4. Small Signal Voltage Follower Pulse Response (Noninverting)

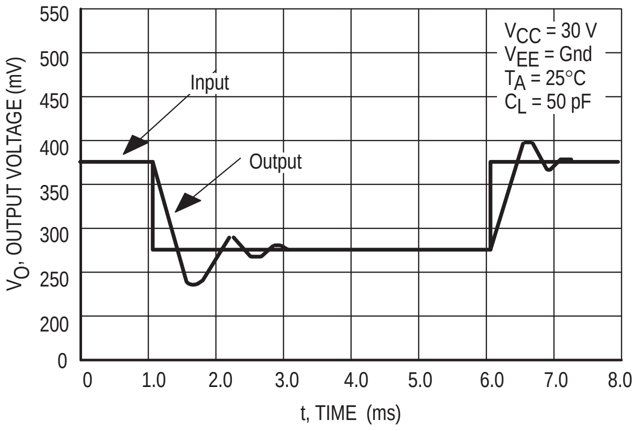


Figure 5. Power Supply Current versus Power Supply Voltage

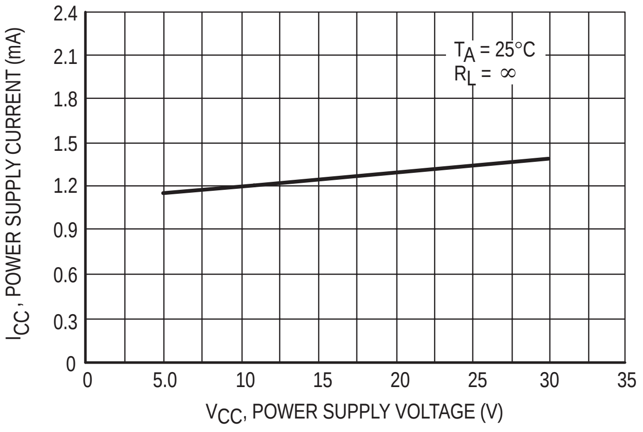


Figure 6. Input Bias Current versus Supply Voltage

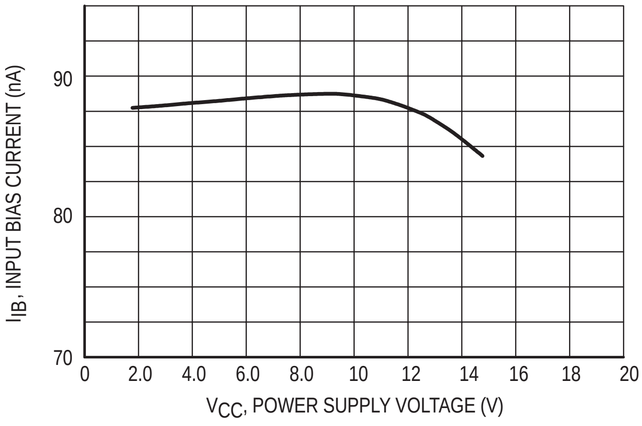
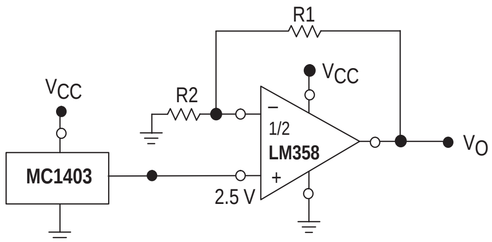
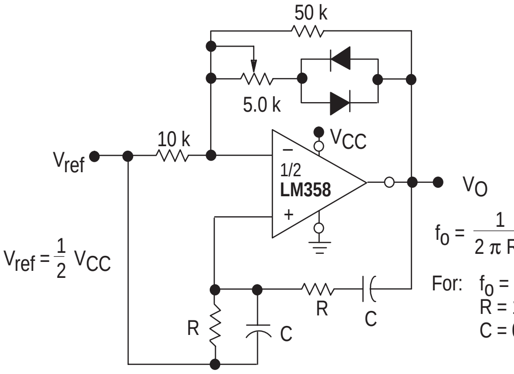


Figure 7. Voltage Reference



$$V_O = 2.5\ V\left(1 + \frac{R1}{R2}\right)$$

Figure 8. Wien Bridge Oscillator

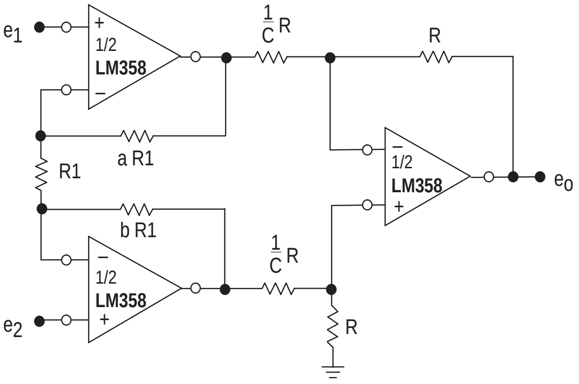


$$V_{ref} = \frac{1}{2} V_{CC}$$

$$f_o = \frac{1}{2\pi RC}$$

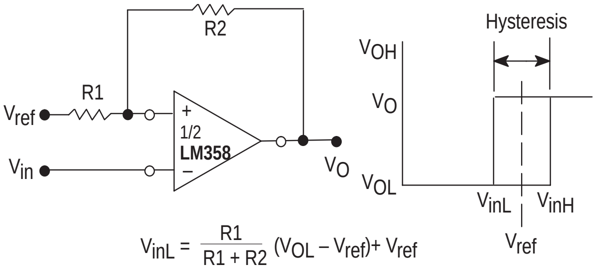
For: $f_o = 1.0$ kHz
$R = 16\ k\Omega$
$C = 0.01\ \mu F$

Figure 9. High Impedance Differential Amplifier



$$e_o = C\,(1 + a + b)\,(e_2 - e_1)$$

Figure 10. Comparator with Hysteresis

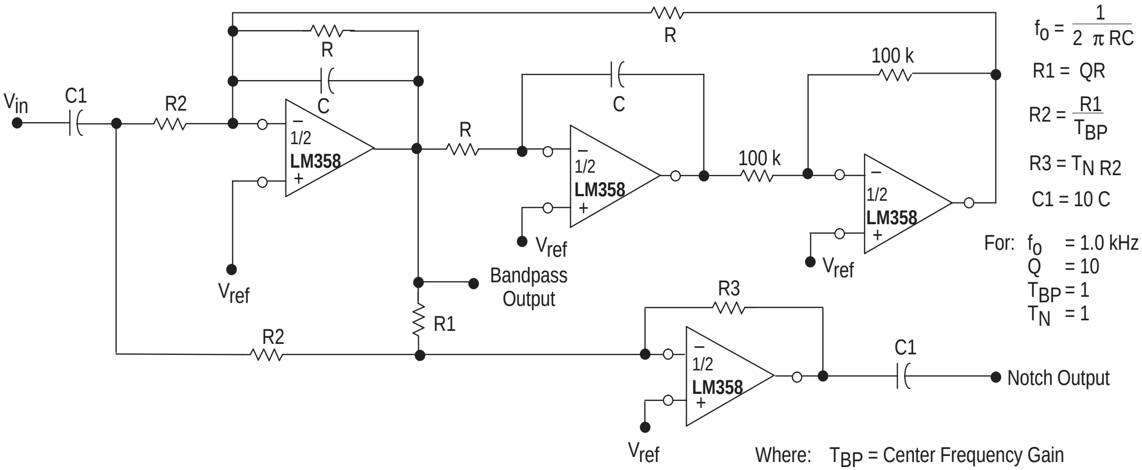


$$V_{inL} = \frac{R1}{R1 + R2}\,(V_{OL} - V_{ref}) + V_{ref}$$

$$V_{inH} = \frac{R1}{R1 + R2}\,(V_{OH} - V_{ref}) + V_{ref}$$

$$H = \frac{R1}{R1 + R2}\,(V_{OH} - V_{OL})$$

Figure 11. Bi–Quad Filter



$$f_o = \frac{1}{2\pi RC}$$

$R1 = QR$

$$R2 = \frac{R1}{T_{BP}}$$

$R3 = T_N\,R2$

$C1 = 10\,C$

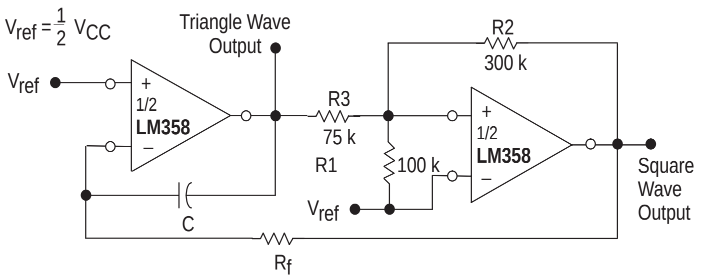
$$V_{ref} = \frac{1}{2} V_{CC}$$

For: $f_o = 1.0$ kHz
$Q = 10$
$T_{BP} = 1$
$T_N = 1$

$R = 160\ k\Omega$
$C = 0.001\ \mu F$
$R1 = 1.6\ M\Omega$
$R2 = 1.6\ M\Omega$
$R3 = 1.6\ M\Omega$

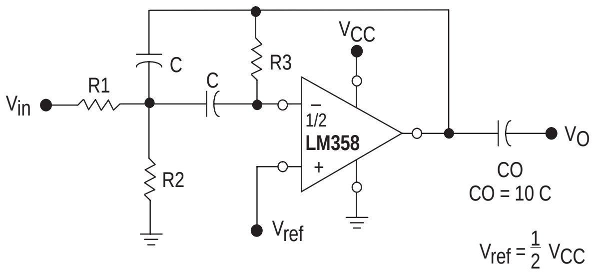
Where: T_{BP} = Center Frequency Gain
T_N = Passband Notch Gain

Figure 12. Function Generator



$$f = \frac{R1 + R_C}{4\ CR_f\ R1} \qquad \text{if, } R3 = \frac{R2\ R1}{R2 + R1}$$

Figure 13. Multiple Feedback Bandpass Filter



Given: f_0 = center frequency
$A(f_0)$ = gain at center frequency

Choose value f_0, C

Then: $R3 = \frac{Q}{\pi f_0 C}$

$R1 = \frac{R3}{2\ A(f_0)}$

$R2 = \frac{R1\ R3}{4Q^2\ R1 - R3}$

For less than 10% error from operational amplifier. $\frac{Q_0\ f_0}{BW} < 0.1$

Where f_0 and BW are expressed in Hz.

If source impedance varies, filter may be preceded with voltage follower buffer to stabilize filter parameters.

MOTOROLA

LM393, LM393A, LM293, LM2903, LM2903V

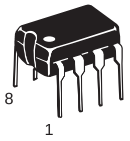
Low Offset Voltage Dual Comparators

SINGLE SUPPLY, LOW POWER DUAL COMPARATORS

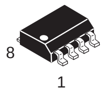
SEMICONDUCTOR TECHNICAL DATA

The LM393 series are dual independent precision voltage comparators capable of single or split supply operation. These devices are designed to permit a common mode range–to–ground level with single supply operation. Input offset voltage specifications as low as 2.0 mV make this device an excellent selection for many applications in consumer automotive, and industrial electronics.

- Wide Single–Supply Range: 2.0 Vdc to 36 Vdc
- Split–Supply Range: ±1.0 Vdc to ±18 Vdc
- Very Low Current Drain Independent of Supply Voltage: 0.4 mA
- Low Input Bias Current: 25 nA
- Low Input Offset Current: 5.0 nA
- Low Input Offset Voltage: 2.0 mV (max) LM393A
  5.0 mV (max) LM293/393
- Input Common Mode Range to Ground Level
- Differential Input Voltage Range Equal to Power Supply Voltage
- Output Voltage Compatible with DTL, ECL, TTL, MOS, and CMOS Logic Levels
- ESD Clamps on the Inputs Increase the Ruggedness of the Device without Affecting Performance

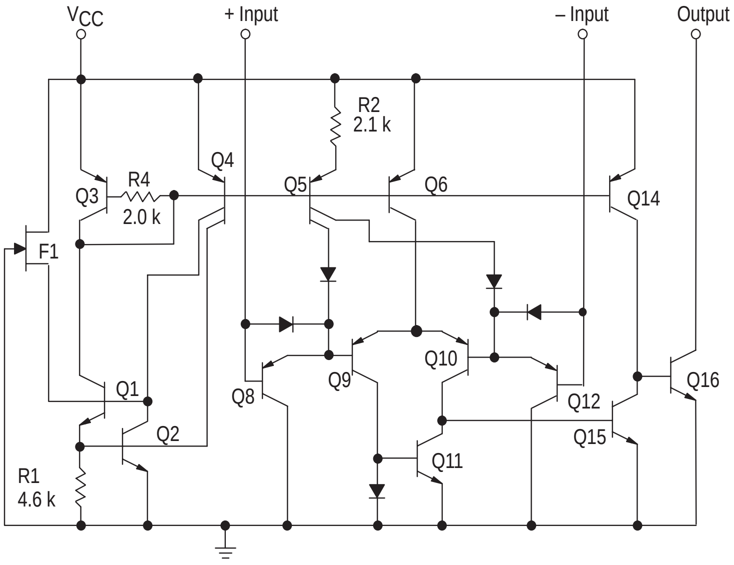


N SUFFIX
PLASTIC PACKAGE
CASE 626

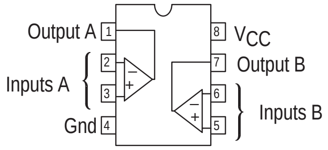


D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

Representative Schematic Diagram
(Diagram shown is for 1 comparator)



PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
LM293D	T_A = –25° to +85°C	SO–8
LM393D	T_A = 0° to +70°C	SO–8
LM393AN,N		Plastic DIP
LM2903D	T_A = –40° to +105°C	SO–8
LM2903N		Plastic DIP
LM2903VD	T_A = –40° to +105°C	SO–8
LM2903VN		Plastic DIP

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	+36 or ±18	Vdc
Input Differential Voltage Range	V_{IDR}	36	Vdc
Input Common Mode Voltage Range	V_{ICR}	–0.3 to +36	Vdc
Output Short Circuit–to–Ground Output Sink Current (Note 1)	I_{SC} I_{Sink}	Continuous 20	mA
Power Dissipation @ T_A = 25°C Derate above 25°C	P_D $1/R_{\theta JA}$	570 5.7	mW mW/°C
Operating Ambient Temperature Range	T_A		°C
LM293		–25 to +85	
LM393, 393A		0 to +70	
LM2903		–40 to +105	
LM2903V		–40 to +125	
Maximum Operating Junction Temperature	$T_{J(max)}$		°C
LM393, 393A, 2903, LM2903V		125	
LM293		150	
Storage Temperature Range	T_{stg}	–65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 Vdc, $T_{low} \le T_A \le T_{high}$,* unless otherwise noted.)

Characteristic	Symbol	LM393A			Unit
		Min	Typ	Max	
Input Offset Voltage (Note 2)	V_{IO}				mV
T_A = 25°C		–	±1.0	±2.0	
$T_{low} \le T_A \le T_{high}$		–	–	4.0	
Input Offset Current	I_{IO}				nA
T_A = 25°C		–	±50	±50	
$T_{low} \le T_A \le T_{high}$		–	–	±150	
Input Bias Current (Note 3)	I_{IB}				nA
T_A = 25°C		–	25	250	
$T_{low} \le T_A \le T_{high}$		–	–	400	
Input Common Mode Voltage Range (Note 4)	V_{ICR}				V
T_A = 25°C		0	–	V_{CC} –1.5	
$T_{low} \le T_A \le T_{high}$		0	–	V_{CC} –2.0	
Voltage Gain $R_L \ge$ 15 kΩ, V_{CC} = 15 Vdc, T_A = 25°C	A_{VOL}	50	200	–	V/mV
Large Signal Response Time V_{in} = TTL Logic Swing, V_{ref} = 1.4 Vdc V_{RL} = 5.0 Vdc, R_L = 5.1 kΩ, T_A = 25°C	–	–	300	–	ns
Response Time (Note 5) V_{RL} = 5.0 Vdc, R_L = 5.1 kΩ, T_A = 25°C	t_{TLH}	–	1.3	–	µs
Input Differential Voltage (Note 6) All $V_{in} \ge$ Gnd or V– Supply (if used)	V_{ID}	–	–	V_{CC}	V
Output Sink Current $V_{in-} \ge$ 1.0 Vdc, V_{in+} = 0 Vdc, $V_O \le$ 1.5 Vdc, T_A = 25°C	I_{Sink}	6.0	16	–	mA
Output Saturation Voltage	V_{OL}				mV
$V_{in-} \ge$ 1.0 Vdc, V_{in+} = 0 Vdc, $I_{Sink} \le$ 4.0 mA, T_A = 25°C		–	150	400	
$T_{low} \le T_A \le T_{high}$		–	–	700	

*T_{low} = 0°C, T_{high} = +70°C for LM393/393A

NOTES:
1. The maximum output current may be as high as 20 mA, independent of the magnitude of V_{CC}, output short circuits to V_{CC} can cause excessive heating and eventual destruction.
2. At output switch point, $V_O \simeq$ 1.4 Vdc, R_S = 0 Ω with V_{CC} from 5.0 Vdc to 30 Vdc, and over the full input common mode range (0 V to V_{CC} = –1.5 V).
3. Due to the PNP transistor inputs, bias current will flow out of the inputs. This current is essentially constant, independent of the output state, there fore, no loading changes will exist on the input lines.
4. Input common mode of either input should not be permitted to go more than 0.3 V negative of ground or minus supply. The upper limit of common mode range is V_{CC} –1.5 V.
5. Response time is specified with a 100 mV step and 5.0 mV of overdrive. With larger magnitudes of overdrive faster response times are obtainable.
6. The comparator will exhibit proper output state if one of the inputs becomes greater than V_{CC}, the other input must remain within the common mode range. The low input state must not be less than –0.3 V of ground or minus supply.

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 Vdc, $T_{low} \le T_A \le T_{high}$,* unless otherwise noted.)

Characteristic	Symbol	LM393A			Unit
		Min	Typ	Max	
Output Leakage Current	I_{OL}				µA
V_{in-} = 0 V, $V_{in+} \ge$ 1.0 Vdc, V_O = 5.0 Vdc, T_A= 25°C		–	0.1	–	
V_{in-} = 0 V, $V_{in+} \ge$ 1.0 Vdc, V_O = 30 Vdc, $T_{low} \le T_A \le T_{high}$		–	–	1.0	
Supply Current	I_{CC}				mA
$R_L = \infty$ Both Comparators, T_A = 25°C		–	0.4	1.0	
$R_L = \infty$ Both Comparators, V_{CC} = 30 V		–	1.0	2.5	

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 Vdc, $T_{low} \le T_A \le T_{high}$, unless otherwise noted.)

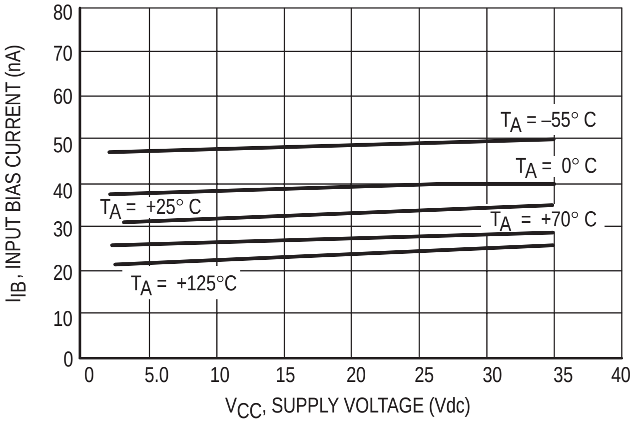
Characteristic	Symbol	LM392, LM393			LM2903, LM2903V			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage (Note 2)	V_{IO}							mV
T_A = 25°C		–	±1.0	±5.0	–	±2.0	±7.0	
$T_{low} \le T_A \le T_{high}$		–	–	9.0	–	9.0	15	
Input Offset Current	I_{IO}							nA
T_A = 25°C		–	±5.0	±50	–	±5.0	±50	
$T_{low} \le T_A \le T_{high}$		–	–	±150	–	±50	±200	
Input Bias Current (Note 3)	I_{IB}							nA
T_A = 25°C		–	25	250	–	25	250	
$T_{low} \le T_A \le T_{high}$		–	–	400	–	200	500	
Input Common Mode Voltage Range (Note 3)	V_{ICR}							V
T_A = 25°C		0	–	V_{CC} –1.5	0	–	V_{CC} –1.5	
$T_{low} \le T_A \le T_{high}$		0	–	V_{CC} –2.0	0	–	V_{CC} –2.0	
Voltage Gain $R_L \ge$ 15 kΩ, V_{CC} = 15 Vdc, T_A = 25°C	A_{VOL}	50	200	–	25	200	–	V/mV
Large Signal Response Time V_{in} = TTL Logic Swing, V_{ref} = 1.4 Vdc V_{RL} = 5.0 Vdc, R_L = 5.1 kΩ, T_A = 25°C	–	–	300	–	–	300	–	ns
Response Time (Note 5) V_{RL} = 5.0 Vdc, R_L = 5.1 kΩ, T_A = 25°C	t_{TLH}	–	1.3	–	–	1.5	–	µs
Input Differential Voltage (Note 6) All $V_{in} \ge$ Gnd or V– Supply (if used)	V_{ID}	–	–	V_{CC}	–	–	V_{CC}	V
Output Sink Current $V_{in} \ge$ 1.0 Vdc, V_{in+} = 0 Vdc, $V_O \le$ 1.5 Vdc T_A = 25°C	I_{Sink}	6.0	16	–	6.0	16	–	mA
Output Saturation Voltage	V_{OL}							mV
$V_{in} \ge$ 1.0 Vdc, V_{in+} = 0, $I_{Sink} \le$ 4.0 mA, T_A = 25°C		–	150	400	–	–	400	
$T_{low} \le T_A \le T_{high}$		–	–	700	–	200	700	
Output Leakage Current	I_{OL}							nA
V_{in-} = 0 V, $V_{in+} \ge$ 1.0 Vdc, V_O = 5.0 Vdc, T_A = 25°C		–	0.1	–	–	0.1	–	
V_{in-} = 0 V, $V_{in+} \ge$ 1.0 Vdc, V_O = 30 Vdc, $T_{low} \le T_A \le T_{high}$		–	–	1000	–	–	1000	
Supply Current	I_{CC}							mA
$R_L = \infty$ Both Comparators, T_A = 25°C		–	0.4	1.0	–	0.4	1.0	
$R_L = \infty$ Both Comparators, V_{CC} = 30 V		–	–	2.5	–	–	2.5	

*T_{low} = 0°C, T_{high} = +70°C for LM393/393A
LM293 T_{low} = –25°C, T_{high} = +85°C
LM2903 T_{low} = –40°C, T_{high} = +105°C
LM2903V T_{low} = –40°C, T_{high} = +125°C

NOTES:
2. At output switch point, $V_O \simeq$ 1.4 Vdc, R_S = 0 Ω with V_{CC} from 5.0 Vdc to 30 Vdc, and over the full input common mode range (0 V to V_{CC} = –1.5 V).
3. Due to the PNP transistor inputs, bias current will flow out of the inputs. This current is essentially constant, independent of the output state, therefore, no loading changes will exist on the input lines.
5. Response time is specified with a 100 mV step and 5.0 mV of overdrive. With larger magnitudes of overdrive faster response times are obtainable.
6. The comparator will exhibit proper output state if one of the inputs becomes greater than V_{CC}, the other input must remain within the common mode range. The low input state must not be less than –0.3 V of ground or minus supply.

LM293/393,A

Figure 1. Input Bias Current versus Power Supply Voltage



LM2903

Figure 2. Input Bias Current versus Power Supply Voltage

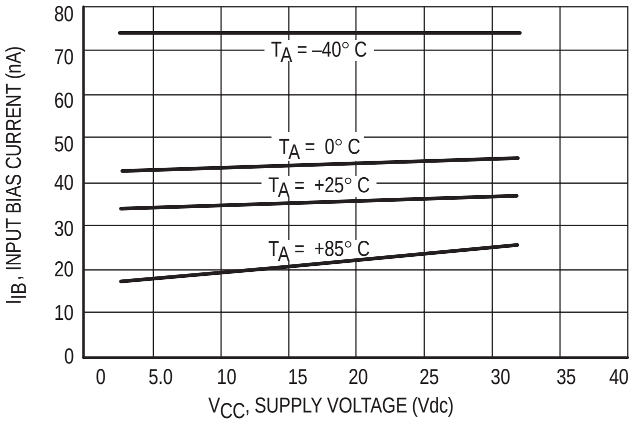


Figure 3. Output Saturation Voltage versus Output Sink Current

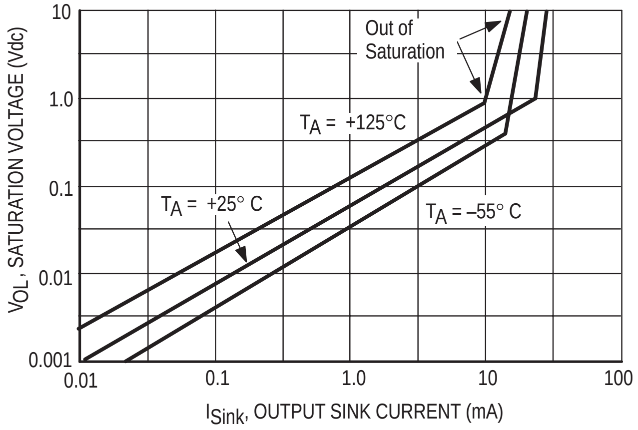


Figure 4. Output Saturation Voltage versus Output Sink Current

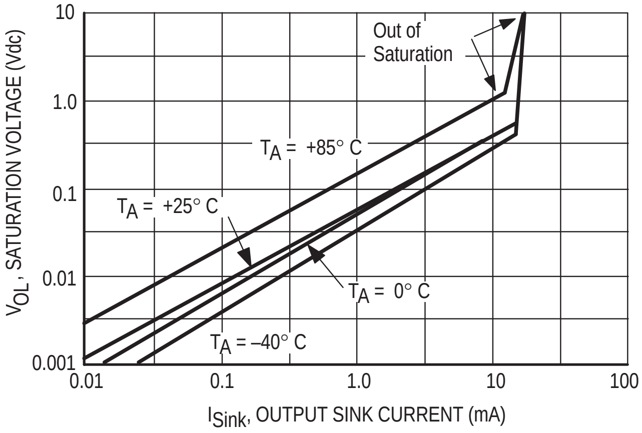


Figure 5. Power Supply Current versus Power Supply Voltage

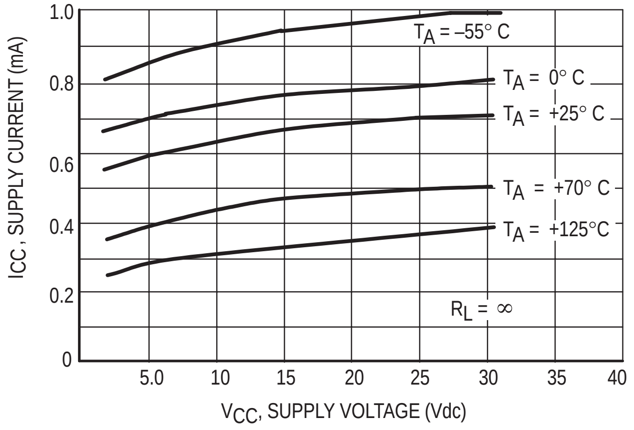
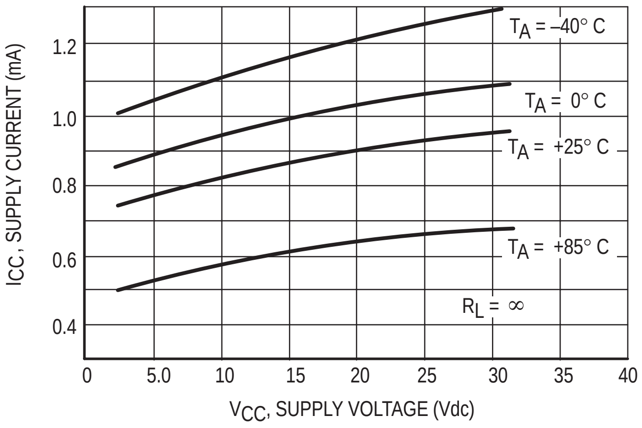


Figure 6. Power Supply Current versus Power Supply Voltage



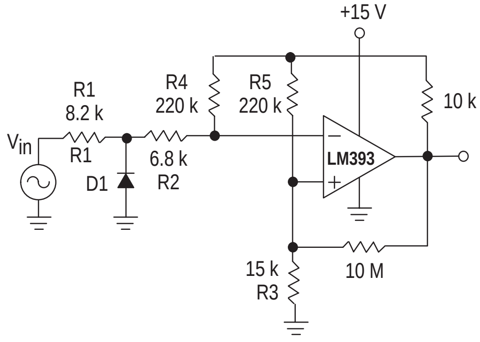
APPLICATIONS INFORMATION

These dual comparators feature high gain, wide bandwidth characteristics. This gives the device oscillation tendencies if the outputs are capacitively coupled to the inputs via stray capacitance. This oscillation manifests itself during output transitions (V_{OL} to V_{OH}). To alleviate this situation, input resistors < 10 kΩ should be used.

The addition of positive feedback (< 10 mV) is also recommended. It is good design practice to ground all unused pins.

Differential input voltages may be larger than supply voltage without damaging the comparator's inputs. Voltages more negative than –0.3 V should not be used.

Figure 7. Zero Crossing Detector (Single Supply)

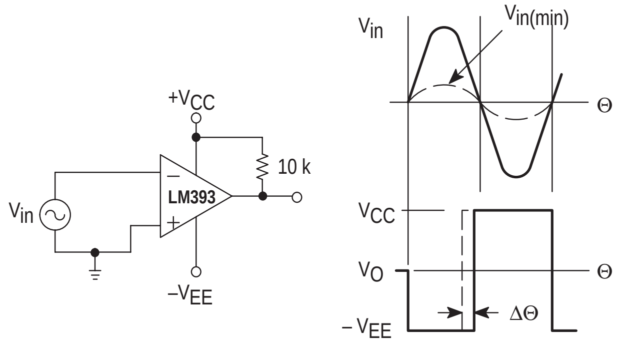


D1 prevents input from going negative by more than 0.6 V.

$$R1 + R2 = R3$$

$$R3 \leq \frac{R5}{10} \text{ for small error in zero crossing.}$$

Figure 8. Zero Crossing Detector (Split Supply)



$V_{in(min)} \approx$ 0.4 V peak for 1% phase distortion (ΔΘ).

Figure 9. Free–Running Square–Wave Oscillator

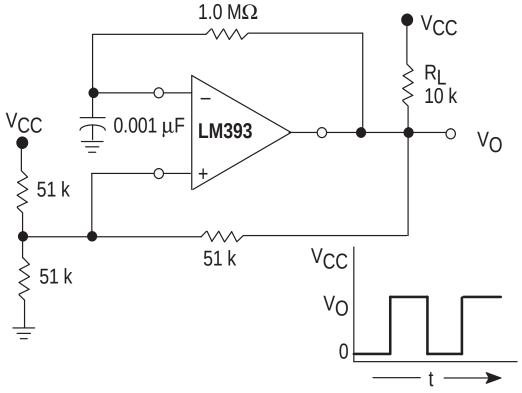
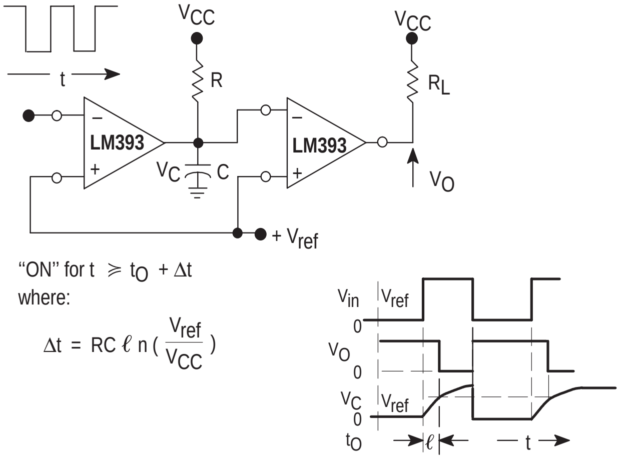


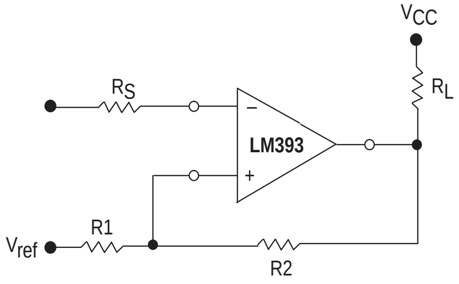
Figure 10. Time Delay Generator



"ON" for t $\geqslant t_O + \Delta t$
where:

$$\Delta t = RC\,\ell n\left(\frac{V_{ref}}{V_{CC}}\right)$$

Figure 11. Comparator with Hysteresis



$$R_S = R1 \,||\, R2$$

$$V_{th1} = V_{ref} + \frac{(V_{CC} - V_{ref})\ R1}{R1 + R2 + R_L}$$

$$V_{th2} = V_{ref} - \frac{(V_{ref} - V_{O}\ \text{Low})\ R1}{R1 + R2}$$

MOTOROLA

LM833

Dual Low Noise, Audio Amplifier

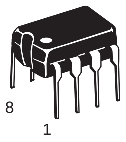
The LM833 is a standard low–cost monolithic dual general–purpose operational amplifier employing Bipolar technology with innovative high–performance concepts for audio systems applications. With high frequency PNP transistors, the LM833 offers low voltage noise (4.5 nV/$\sqrt{Hz}$), 15 MHz gain bandwidth product, 7.0 V/µs slew rate, 0.3 mV input offset voltage with 2.0 µV/°C temperature coefficient of input offset voltage. The LM833 output stage exhibits no deadband crossover distortion, large output voltage swing, excellent phase and gain margins, low open loop high frequency output impedance and symmetrical source/sink AC frequency response.

The LM833 is specified over the automotive temperature range and is available in the plastic DIP and SO–8 packages (P and D suffixes). For an improved performance dual/quad version, see the MC33079 family.

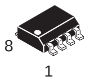
- Low Voltage Noise: 4.5 nV/$\sqrt{Hz}$
- High Gain Bandwidth Product: 15 MHz
- High Slew Rate: 7.0 V/µs
- Low Input Offset Voltage: 0.3 mV
- Low T.C. of Input Offset Voltage: 2.0 µV/°C
- Low Distortion: 0.002%
- Excellent Frequency Stability
- Dual Supply Operation

DUAL OPERATIONAL AMPLIFIER

SEMICONDUCTOR TECHNICAL DATA

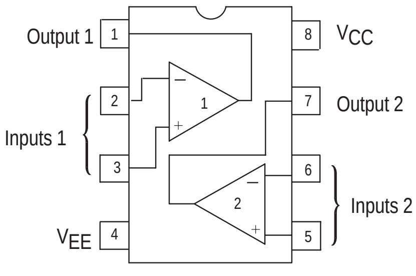


N SUFFIX
PLASTIC PACKAGE
CASE 626



D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

PIN CONNECTIONS



(Top View)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage (V_{CC} to V_{EE})	V_S	+36	V
Input Differential Voltage Range (Note 1)	V_{IDR}	30	V
Input Voltage Range (Note 1)	V_{IR}	±15	V
Output Short Circuit Duration (Note 2)	t_{SC}	Indefinite	
Operating Ambient Temperature Range	T_A	–40 to +85	°C
Operating Junction Temperature	T_J	+150	°C
Storage Temperature	T_{stg}	–60 to +150	°C
Maximum Power Dissipation (Notes 2 and 3)	P_D	500	mW

NOTES: 1. Either or both input voltages must not exceed the magnitude of V_{CC} or V_{EE}.
2. Power dissipation must be considered to ensure maximum junction temperature (T_J) is not exceeded (see power dissipation performance characteristic).
3. Maximum value at $T_A \leq 85°C$.

ORDERING INFORMATION

Device	Operating Temperature Range	Package
LM833N	T_A = – 40° to +85°C	Plastic DIP
LM833D		SO–8

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = –15 V, T_A = 25°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Offset Voltage (R_S = 10 Ω, V_O = 0 V)	V_{IO}	–	0.3	5.0	mV
Average Temperature Coefficient of Input Offset Voltage R_S = 10 Ω, V_O = 0 V, T_A = T_{low} to T_{high}	$\Delta V_{IO}/\Delta T$	–	2.0	–	µV/°C
Input Offset Current (V_{CM} = 0 V, V_O = 0 V)	I_{IO}	–	10	200	nA
Input Bias Current (V_{CM} = 0 V, V_O = 0 V)	I_{IB}	–	300	1000	nA
Common Mode Input Voltage Range	V_{ICR}	– –12	+14 –14	+12 –	V
Large Signal Voltage Gain (R_L = 2.0 kΩ, V_O = ±10 V	A_{VOL}	90	110	–	dB
Output Voltage Swing:					V
R_L = 2.0 kΩ, V_{ID} = 1.0 V	V_{O+}	10	13.7	–	
R_L = 2.0 kΩ, V_{ID} = 1.0 V	V_{O-}	–	–14.1	–10	
R_L = 10 kΩ, V_{ID} = 1.0 V	V_{O+}	12	13.9	–	
R_L = 10 kΩ, V_{ID} = 1.0 V	V_{O-}	–	–14.7	–12	
Common Mode Rejection (V_{in} = ±12 V)	CMR	80	100	–	dB
Power Supply Rejection (V_S = 15 V to 5.0 V, –15 V to –5.0 V)	PSR	80	115	–	dB
Power Supply Current (V_O = 0 V, Both Amplifiers)	I_D	–	4.0	8.0	mA

AC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = –15 V, T_A = 25°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Slew Rate (V_{in} = –10 V to +10 V, R_L = 2.0 kΩ, A_V = +1.0)	S_R	5.0	7.0	–	V/µs
Gain Bandwidth Product (f = 100 kHz)	GBW	10	15	–	MHz
Unity Gain Frequency (Open Loop)	f_U	–	9.0	–	MHz
Unity Gain Phase Margin (Open Loop)	θ_m	–	60	–	Deg
Equivalent Input Noise Voltage (R_S = 100 Ω, f = 1.0 kHz)	e_n	–	4.5	–	$nV/\sqrt{Hz}$
Equivalent Input Noise Current (f = 1.0 kHz)	i_n	–	0.5	–	$pA/\sqrt{Hz}$
Power Bandwidth (V_O = 27 V_{pp}, R_L = 2.0 kΩ, THD ≤ 1.0%)	BWP	–	120	–	kHz
Distortion (R_L = 2.0 kΩ, f = 20 Hz to 20 kHz, V_O = 3.0 V_{rms}, A_V = +1.0)	THD	–	0.002	–	%
Channel Separation (f = 20 Hz to 20 kHz)	C_S	–	–120	–	dB

Figure 1. Maximum Power Dissipation versus Temperature

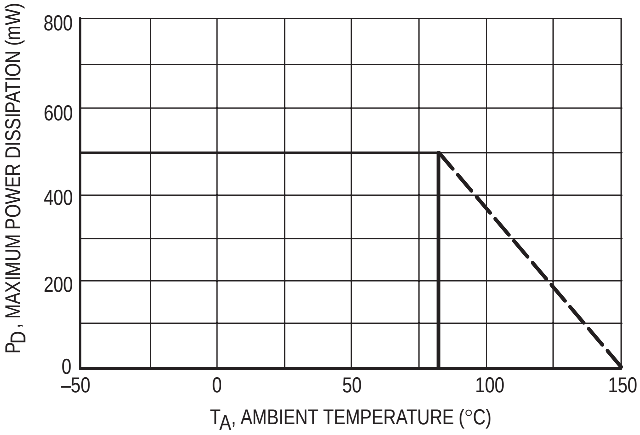


Figure 2. Input Bias Current versus Temperature

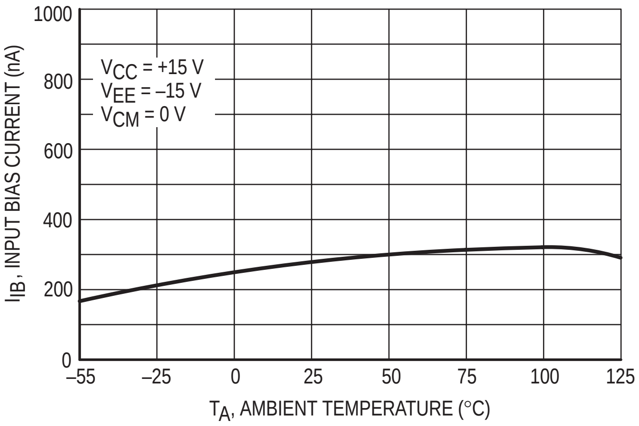


Figure 3. Input Bias Current versus Supply Voltage

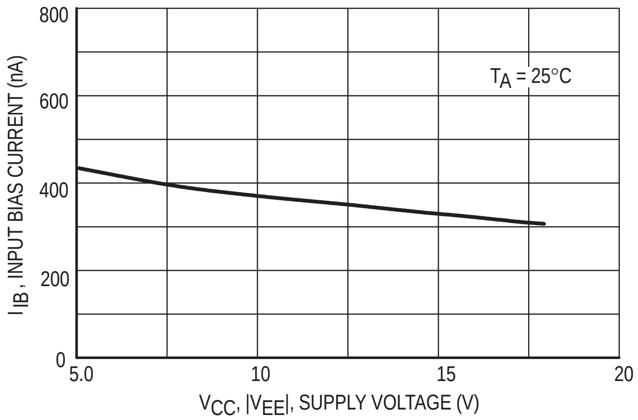


Figure 4. Supply Current versus Supply Voltage

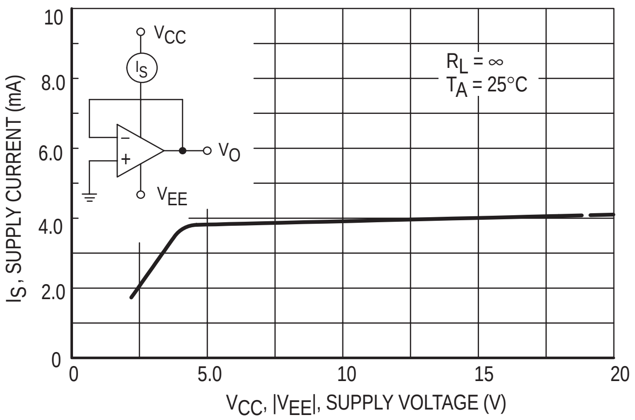


Figure 5. DC Voltage Gain versus Temperature

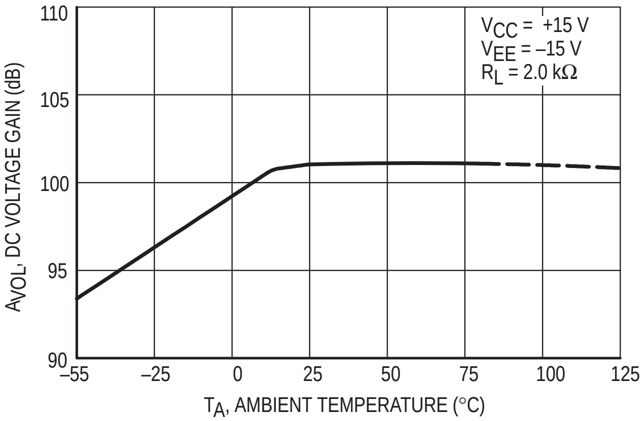


Figure 6. DC Voltage Gain versus Supply Voltage

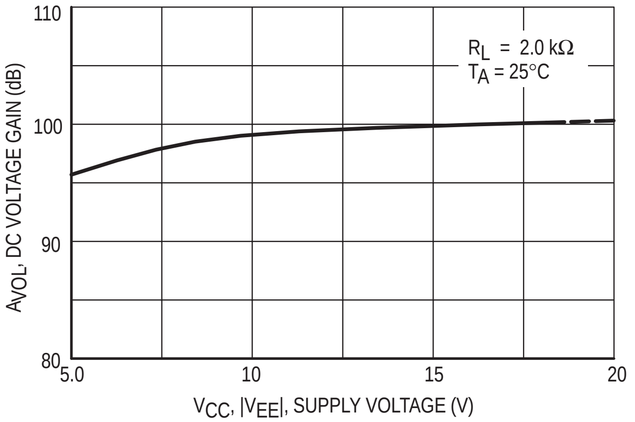


Figure 7. Open Loop Voltage Gain and Phase versus Frequency

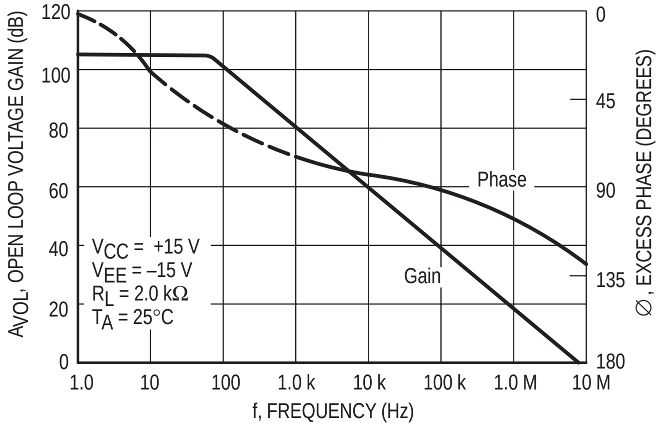


Figure 8. Gain Bandwidth Product versus Temperature

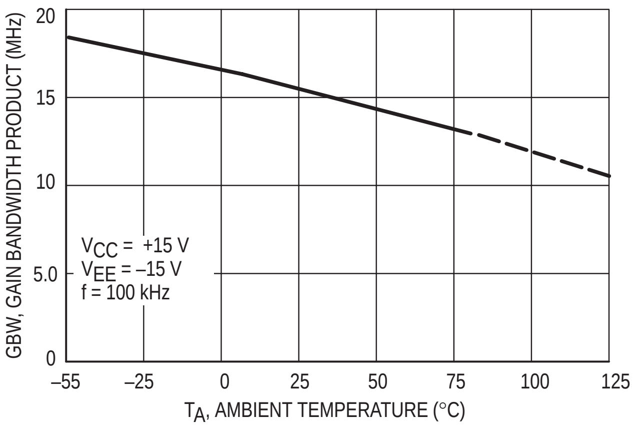


Figure 9. Gain Bandwidth Product versus Supply Voltage

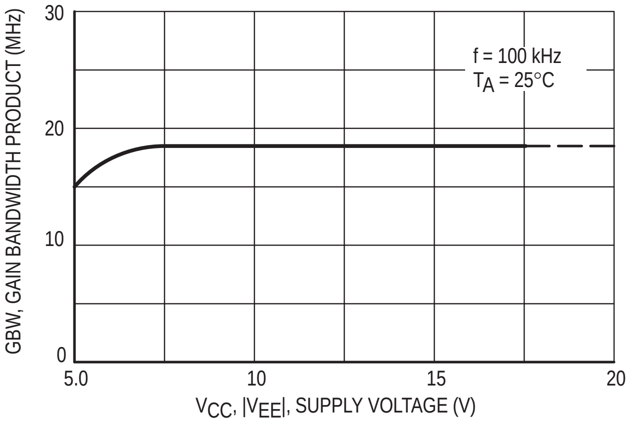


Figure 10. Slew Rate versus Temperature

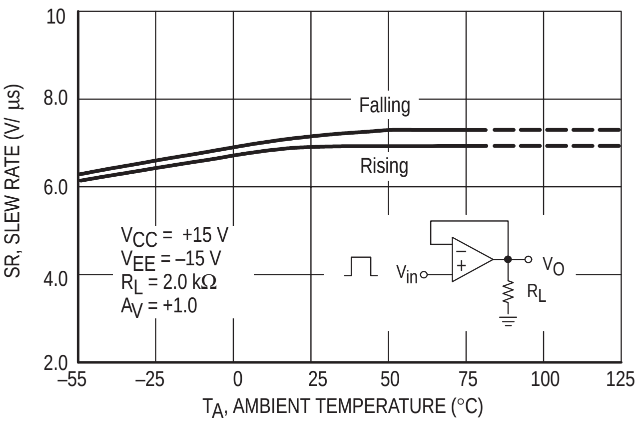


Figure 11. Slew Rate versus Supply Voltage

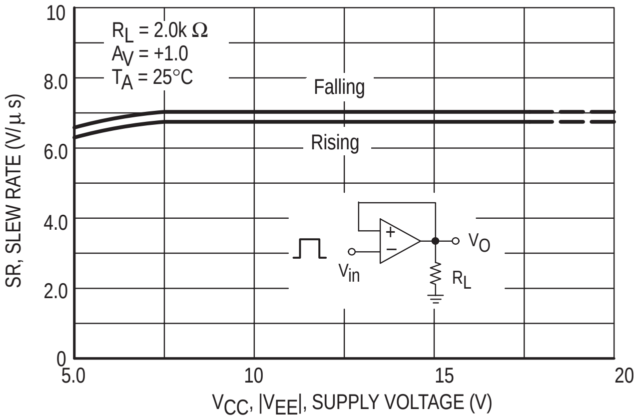


Figure 12. Output Voltage versus Frequency

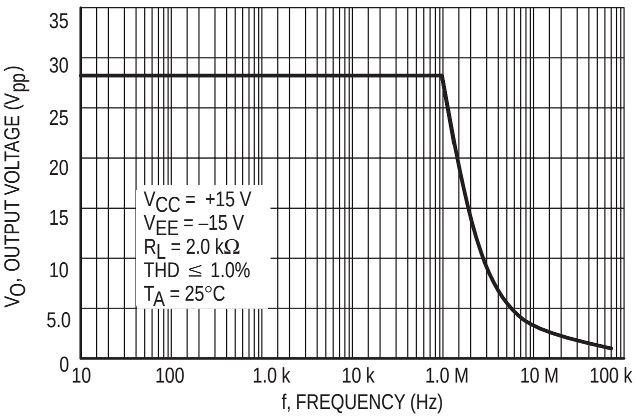


Figure 13. Maximum Output Voltage versus Supply Voltage

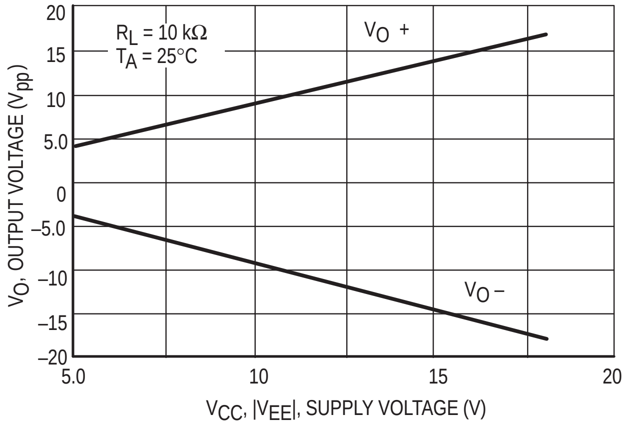


Figure 14. Output Saturation Voltage versus Temperature

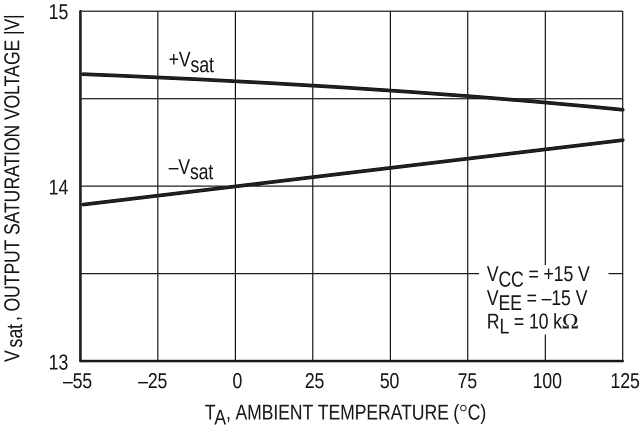


Figure 15. Power Supply Rejection versus Frequency

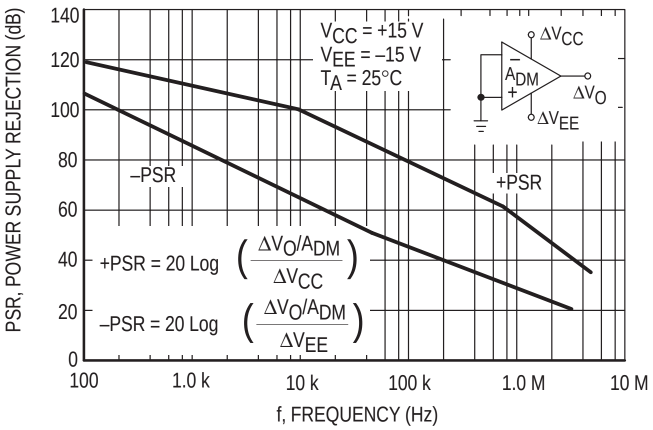


Figure 16. Common Mode Rejection versus Frequency

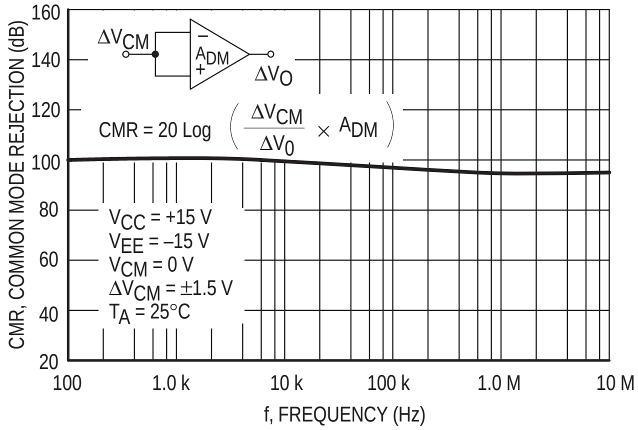


Figure 17. Total Harmonic Distortion versus Frequency

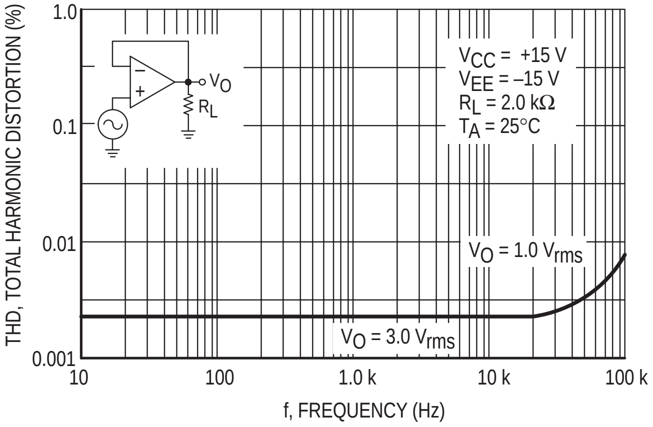


Figure 18. Input Referred Noise Voltage versus Frequency

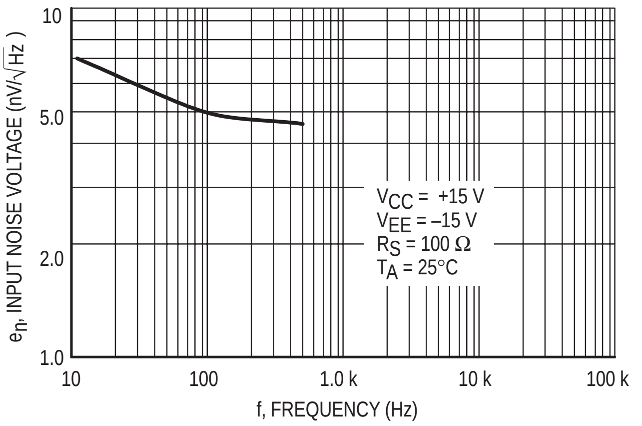


Figure 19. Input Referred Noise Current versus Frequency

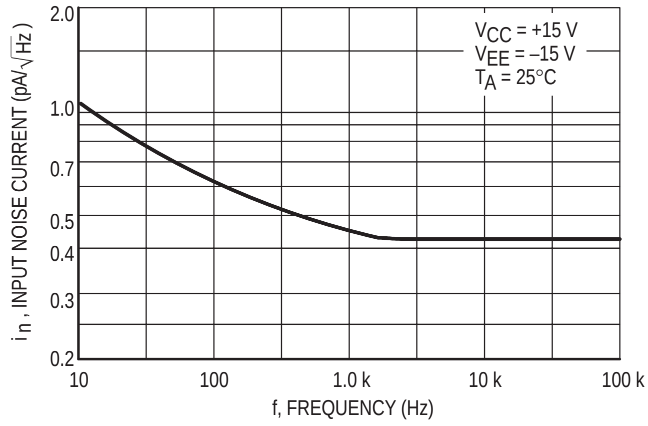


Figure 20. Input Referred Noise Voltage versus Source Resistance

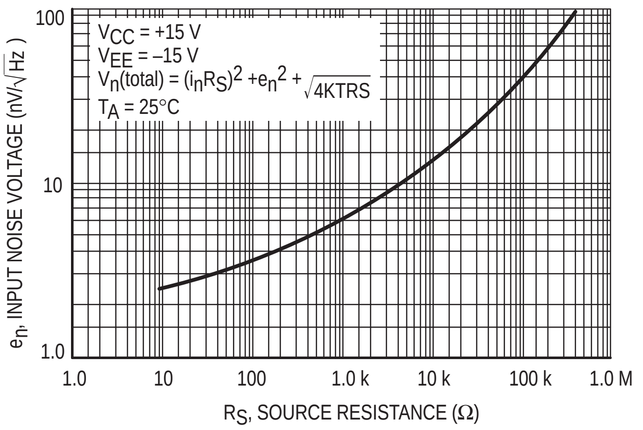


Figure 21. Inverting Amplifier

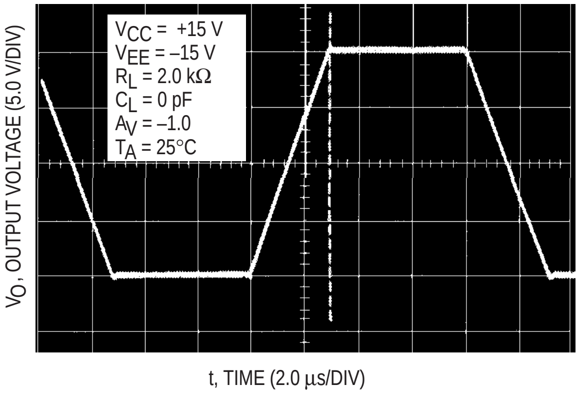


Figure 22. Noninverting Amplifier Slew Rate

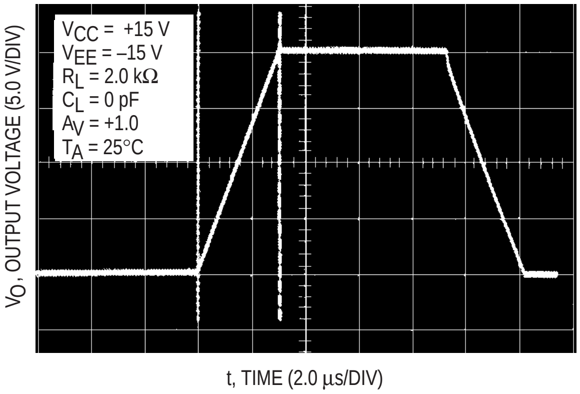
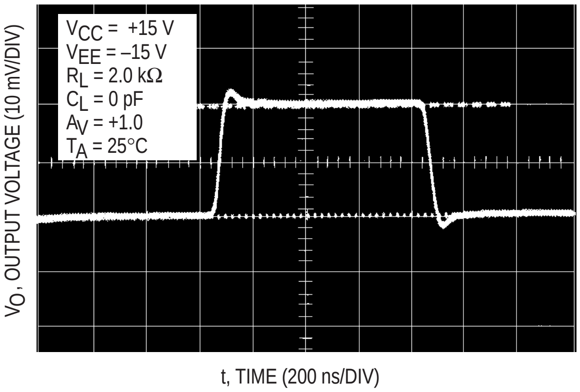


Figure 23. Noninverting Amplifier Overshoot



MC1436, C

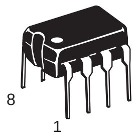
High Voltage, Internally Compensated Operational Amplifiers

The MC1436, C was designed for use as a summing amplifier, integrator, or amplifier with operating characteristics as a function of the external feedback components.

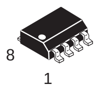
- Output Voltage Swing:
  ±22 $V_{pk(min)}$ (V_{CC} = +28 V, V_{EE} = –28 V)
- Fast Slew Rate: 2.0 V/µs Typ
- Internally Compensated
- Offset Voltage Null Capability
- Input Overvoltage Protection
- A_{VOL}: 500,000 Typ
- Characteristics Independent of Power Supply Voltages:
  (±5.0 Vdc to ±36 Vdc)

OPERATIONAL AMPLIFIERS

SEMICONDUCTOR TECHNICAL DATA



P1 SUFFIX
PLASTIC PACKAGE
CASE 626



D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

PIN CONNECTIONS

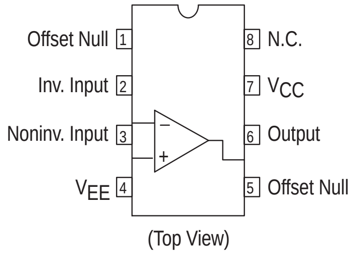


Figure 1. Differential Amplifier with ±20 V Common Mode Input Voltage Range

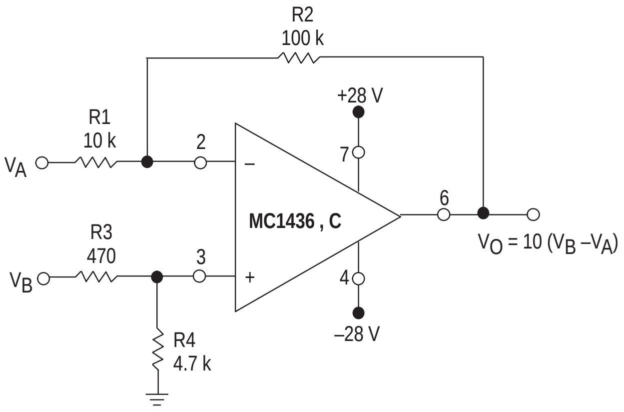
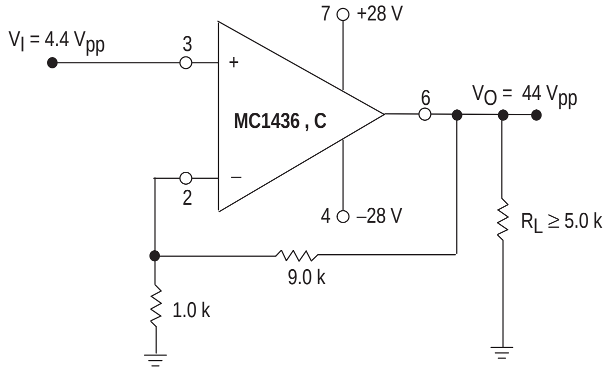


Figure 2. Typical Noninverting X10 Voltage Amplifier



ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC1436CD,D	T_A = 0° to +70°C	SO–8
MC1436CP1,P1		Plastic DIP

MAXIMUM RATINGS (T_A = +25°C, unless otherwise noted.)

Rating	Symbol	MC1436	MC1436C	Unit
Power Supply Voltage	V_{CC} V_{EE}	+34 –34	+30 –30	Vdc
Input Differential Voltage Range	V_{IDR}	Note 2		V
Input Common Mode Voltage Range	V_{ICR}	Note 2		V
Output Short Circuit Duration (V_{CC} = V_{EE} = 28 Vdc, V_O = 0)	t_{SC}	5.0		sec
Power Dissipation (Package Limitation) Derate above T_A = +25°C	P_D	680 4.6		mW mW/°C
Operating Ambient Temperature Range	T_A	0 to +70		°C
Storage Temperature Range	T_{stg}	–65 to +150		°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +28 V, V_{EE} = –28 V, T_A = 25°C, unless otherwise noted.)

Characteristic	Symbol	MC1436			MC1436C			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Bias Current	I_{IB}							nAdc
T_A = +25°C		–	15	40	–	25	90	
T_A = T_{low} to T_{high} (See Note 1)		–	–	55	–	–	–	
Input Offset Current	I_{IO}							nAdc
T_A = +25°C		–	5.0	10	–	10	25	
T_A = +25°C to T_{high}		–	–	14	–	–	–	
T_A = T_{low} to +25°C		–	–	14	–	–	–	
Input Offset Voltage	V_{IO}							mVdc
T_A = +25°C		–	5.0	10	–	5.0	12	
T_A = T_{low} to T_{high}		–	–	14	–	–	–	
Differential Input Impedance (Open loop, f ≤ 5.0 Hz)								
Parallel Input Resistance	rp	–	10	–	–	10	–	MΩ
Parallel Input Capacitance	Cp	–	2.0	–	–	2.0	–	pF
Common Mode Input Impedance (f ≤ 5.0 Hz)	z_{ic}	–	250	–	–	250	–	MΩ
Input Common Mode Voltage Range	V_{ICR}	±22	±25	–	±18	±20	–	Vpk
Equivalent Input Noise Voltage (A_V = 100, R_S = 10 kΩ, f = 1.0 kHz, BW = 1.0 Hz)	e_n	–	50	–	–	50	–	nV/(Hz)$^1/_2$
Common Mode Rejection (DC)	CMR	70	110	–	50	90	–	dB
Large Signal DC Open Loop Voltage Gain	A_{VOL}							V/V
(V_O = ±10 V, R_L = 100 kΩ) T_A = +25°C		70,000	500,000	–	50,000	500,000	–	
T_A = T_{low} to T_{high}		50,000	–	–	–	–	–	
(V_O = ±10 V, R_L = 10 kΩ, T_A = +25°C)		–	200,000	–	–	200,000	–	
Power Bandwidth (Voltage Follower) (A_V = 1, R_L = 5.0 kΩ, THD ≤ 5%, V_O = 40 V_{pp})	BWp	–	23	–	–	23	–	kHz
Unity Gain Crossover Frequency (Open loop)	f_c	–	1.0	–	–	1.0	–	MHz
Phase Margin (Open loop, Unity Gain)	ϕ_m	–	50	–	–	50	–	Degrees
Gain Margin	A_M	–	18	–	–	18	–	dB
Slew Rate (Unity Gain)	SR	–	2.0	–	–	2.0	–	V/µs
Output Impedance (f ≤ 5.0 Hz)	z_O	–	1.0	–	–	1.0	–	kΩ
Short Circuit Output Current	I_{SC}	–	±17	–	–	±19	–	mAdc

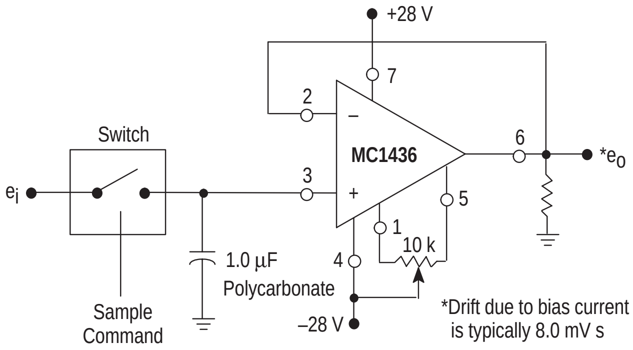
NOTES: 1. T_{low} = 0°C for MC1436,C T_{high} = +70°C for MC1436,C
2. Either or both input voltages must not exceed the magnitude of V_{CC} or V_{EE} + 3.0 V.

ELECTRICAL CHARACTERISTICS (V_{CC} = +28 V, V_{EE} = –28 V, T_A = 25°C, unless otherwise noted.)

Characteristic	Symbol	MC1436			MC1436C			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage Range (R_L = 5.0 kΩ) V_{CC} = +28 Vdc, V_{EE} = –28 Vdc V_{CC} = +36 Vdc, V_{EE} = –36 Vdc	V_O	 ±20 –	 ±22 –	 – –	 ±20 –	 ±22 –	 – –	V_{pk}
Power Supply Rejection V_{EE} = Constant, R_S ≤ 10 kΩ V_{CC} = Constant, R_S ≤ 10 kΩ	 PSR + PSR –	 – –	 35 35	 200 200	 – –	 50 50	 – –	µV/V
Power Supply Current (See Note 2)	I_{CC} I_{EE}	– –	2.6 2.6	5.0 5.0	– –	2.6 2.6	5.0 5.0	mAdc
DC Quiescent Power Consumption (V_O = 0)	P_C	–	146	280	–	146	280	mW

NOTES: 2. V_{CC} = V_{EE} = 5.0 Vdc to 30 Vdc for MC1436
V_{CC} = V_{EE} = 5.0 Vdc to 28 Vdc for MC1436C

Figure 3. Low–Drift Sample and Hold



*Drift due to bias current is typically 8.0 mV s

Figure 4. Power Bandwidth

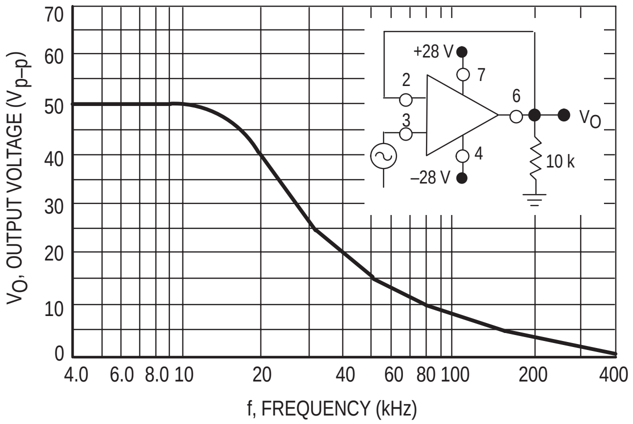


Figure 5. Peak Output Voltage Swing versus Power Supply Voltage

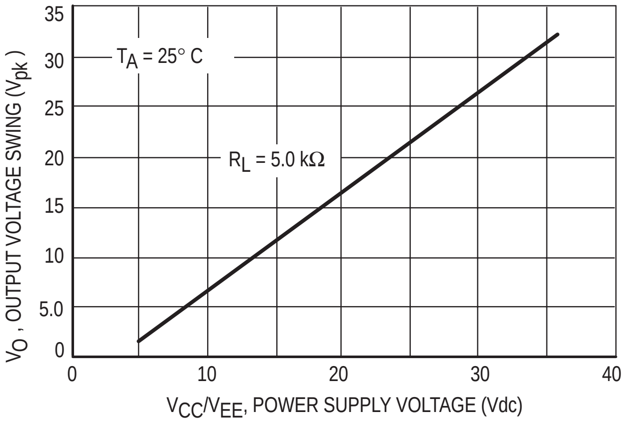


Figure 6. Open Loop Frequency Response

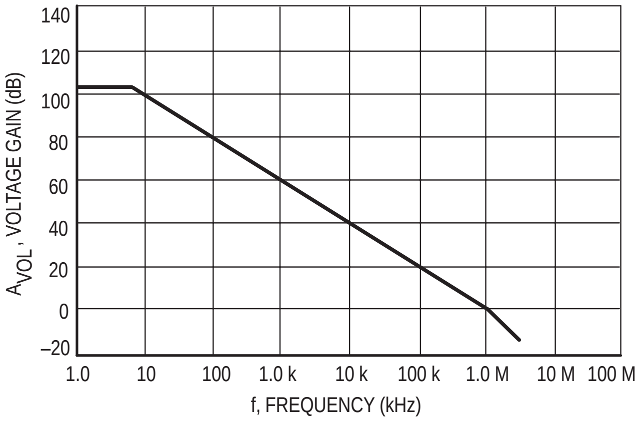


Figure 7. Output Short Circuit Current versus Temperature

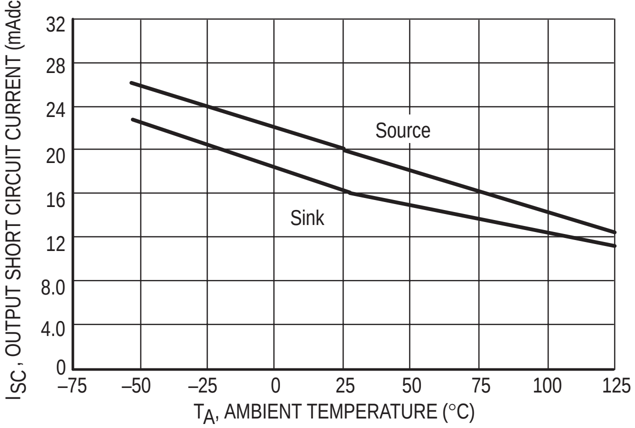


Figure 8. Input Bias Current versus Temperature

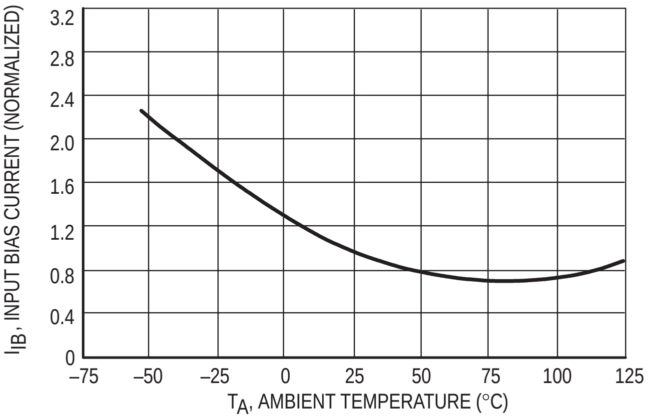
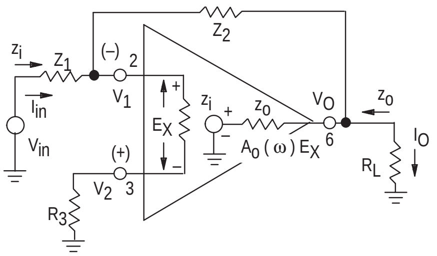


Figure 9. Inverting Feedback Model



$$z_o = z_o \frac{1 + Z_2/Z_1}{A_0(\omega)}$$

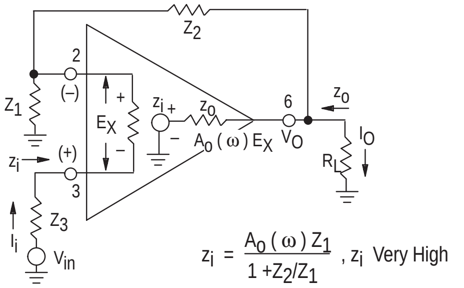
If : $A_0(\omega) \rightarrow \infty$

$$\frac{V_O}{V_i} = -\frac{Z_2}{Z_1}$$

If : $R_3 \ll Z_1$

$$z_i \approx Z_1$$

Figure 10. Noninverting Feedback Model



$$z_i = \frac{A_0(\omega)Z_1}{1 + Z_2/Z_1}, \ z_i \text{ Very High}$$

$$z_0 = z_0 \frac{1 + Z_2/Z_1}{A_0(\omega)} \qquad \frac{V_O}{V_i} = 1 + Z_2/Z_1, \text{ when } A_O(\omega) \rightarrow \infty$$

$Z_0 \rightarrow 0$
$A_0(\omega) \rightarrow \infty$

Figure 11. Audio Amplifier

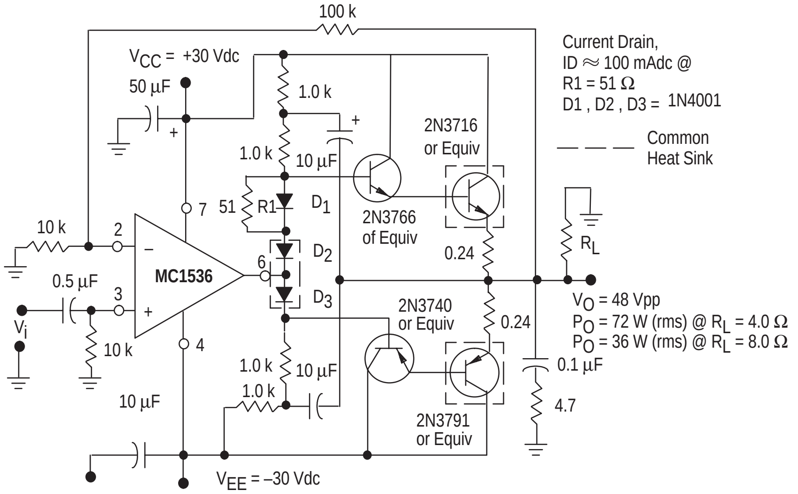
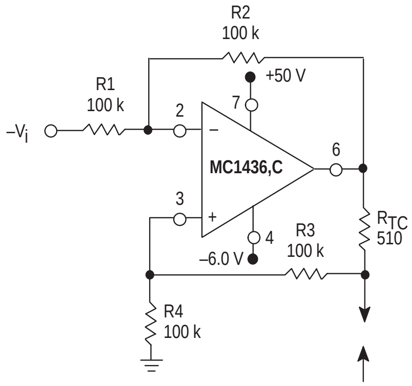


Figure 12. Voltage Controlled Current Source or Transconductance Amplifier with 0 V to 40 V Compliance



$$\frac{I_O}{V_i} = \frac{I}{R_{TC}} = 2.0\ \text{mA/V}$$

$$Z_O = \frac{R1R_{TC}\ (R3 + R4)}{R1\ (R_{TC} + R3) - R2\ R4}$$

Figure 13. Representative Schematic Diagram

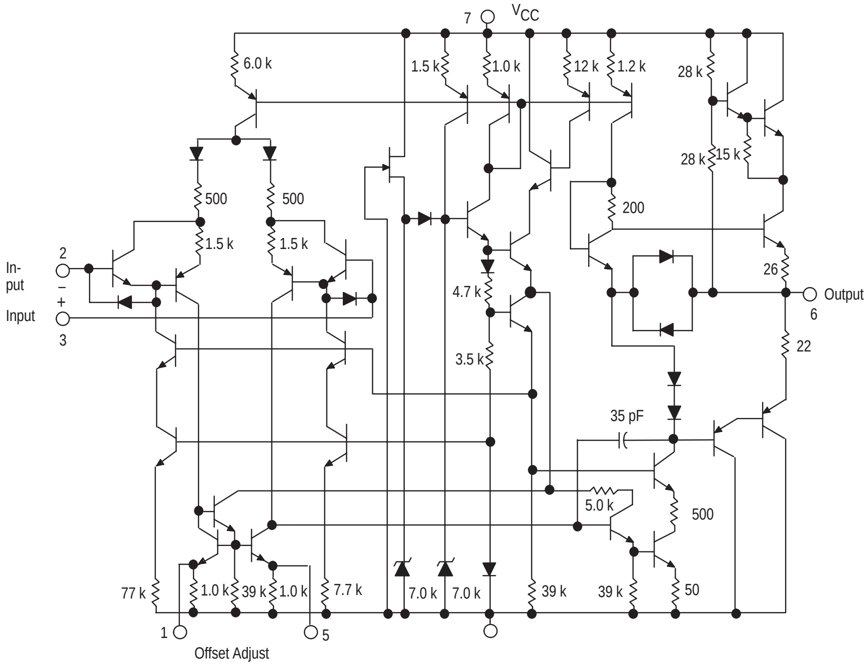
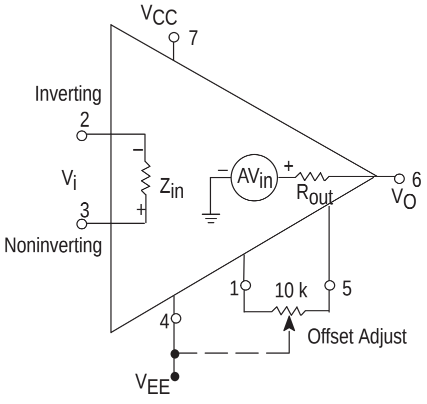


Figure 14. Equivalent Circuit



MOTOROLA

MC1458, C

Internally Compensated, High Performance Dual Operational Amplifiers

The MC1458, C was designed for use as a summing amplifier, integrator, or amplifier with operating characteristics as a function of the external feedback components.

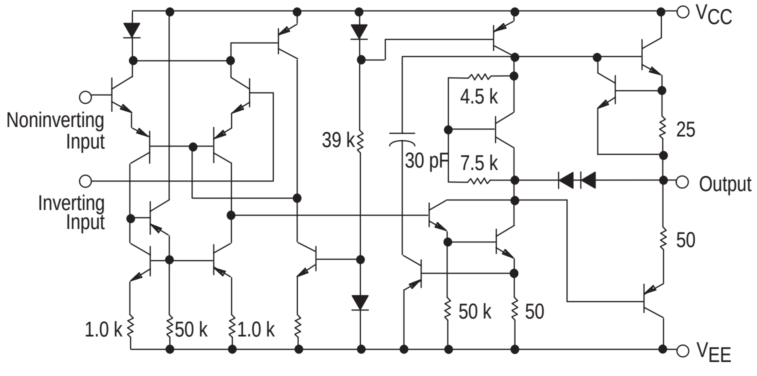
- No Frequency Compensation Required
- Short Circuit Protection
- Wide Common Mode and Differential Voltage Ranges
- Low Power Consumption
- No Latch–Up

MAXIMUM RATINGS (T_A = +25°C, unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC} V_{EE}	+18 –18	Vdc
Input Differential Voltage	V_{ID}	±30	V
Input Common Mode Voltage (Note 1)	V_{ICM}	±15	V
Output Short Circuit Duration (Note 2)	t_{SC}	Continuous	
Operating Ambient Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	–55 to +125	°C
Junction Temperature	T_J	150	°C

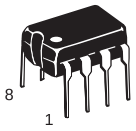
NOTES: 1. For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.
2. Supply voltage equal to or less than 15 V.

Representative Schematic Diagram

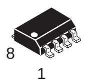


DUAL OPERATIONAL AMPLIFIERS
(DUAL MC1741)

SEMICONDUCTOR TECHNICAL DATA

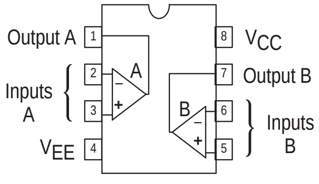


P1 SUFFIX
PLASTIC PACKAGE
CASE 626



D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC1458CD, D	T_A = 0° to +70°C	SO–8
MC1458CP1, P1		Plastic DIP

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = –15 V, T_A = 25°C, unless otherwise noted. (Note 3))

Characteristic	Symbol	MC1458			MC1458C			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage ($R_S \le 10$ k)	V_{IO}	–	2.0	6.0	–	2.0	1.0	mV
Input Offset Current	I_{IO}	–	20	200	–	20	300	nA
Input Bias Current	I_{IB}	–	80	500	–	80	700	nA
Input Resistance	r_i	0.3	2.0	–	–	2.0	–	MΩ
Input Capacitance	C_i	–	1.4	–	–	1.4	–	pF
Offset Voltage Adjustment Range	V_{IOR}	–	±15	–	–	±15	–	mV
Common Mode Input Voltage Range	V_{ICR}	±12	±13	–	±11	±13	–	V
Large Signal Voltage Gain	A_{VOL}							V/mV
(V_O = ±10 V, R_L = 2.0 k)		20	200	–	–	–	–	
(V_O = ±10 V, R_L = 10 k)		–	–	–	20	200	–	
Output Resistance	r_o	–	75	–	–	75	–	Ω
Common Mode Rejection ($R_S \le 10$ k)	CMR	70	90	–	60	90	–	dB
Supply Voltage Rejection ($R_S \le 10$ k)	PSR	–	30	150	–	30	–	µV/V
Output Voltage Swing	V_O							V
($R_S \le 10$ k)		±12	±14	–	±11	±14	–	
($R_S \le 2.0$ k)		±10	±13	–	±9.0	±13	–	
Output Short Circuit Current	I_{SC}	–	20	–	–	20	–	mA
Supply Currents (Both Amplifiers)	I_D	–	2.3	5.6	–	2.3	8.0	mA
Power Consumption	P_C	–	70	170	–	70	240	mW
Transient Response (Unity Gain)								
(V_I = 20 mV, $R_L \ge 2.0$ kΩ, $C_L \le 100$ pF) Rise Time	t_{TLH}	–	0.3	–	–	0.3	–	µs
(V_I = 20 mV, $R_L \ge 2.0$ kΩ, $C_L \le 100$ pF) Overshoot	os	–	15	–	–	15	–	%
(V_I = 10 V, $R_L \ge 2.0$ kΩ, $C_L \le 100$ pF) Slew Rate	SR	–	0.5	–	–	0.5	–	V/µs

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = –15 V, T_A = T_{high} to T_{low}, unless otherwise noted. (Note 3))*

Characteristic	Symbol	MC1458			MC1458C			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage ($R_S \le 10$ kΩ)	V_{IO}	–	–	7.5	–	–	12	mV
Input Offset Current (T_A = 0° to +70°C)	I_{IO}	–	–	300	–	–	400	nA
Input Bias Current (T_A = 0° to +70°C)	I_{IB}	–	–	800	–	–	1000	nA
Output Voltage Swing	V_O							V
($R_S \le 10$ k)		±12	±14	–	–	–	–	
($R_S \le 2$ k)		±10	±13	–	±9.0	±13	–	
Large Signal Voltage Gain	A_{VOL}							V/mV
(V_O = ±10 V, R_L = 2 k)		15	–	–	–	–	–	
(V_O = ±10 V, R_L = 10 k)		–	–	–	15	–	–	

*T_{low} = 0°C for MC1458, C T_{high} = +70°C for MC1458, C

NOTE: 3. Input pins of an unused amplifier must be grounded for split supply operation or biased at least 3.0 V above V_{EE} for single supply operation.

Figure 1. Burst Noise versus Source Resistance

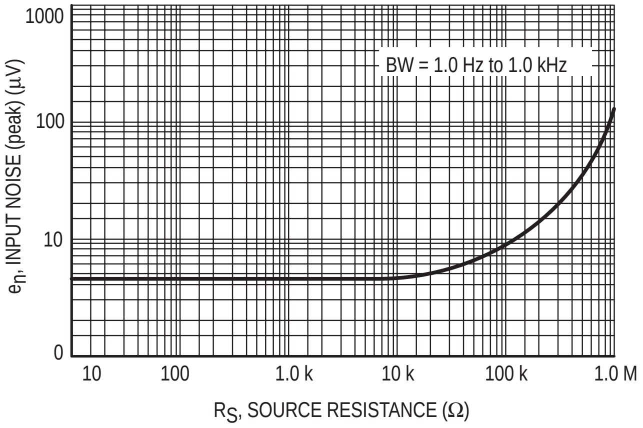


Figure 2. RMS Noise versus Source Resistance

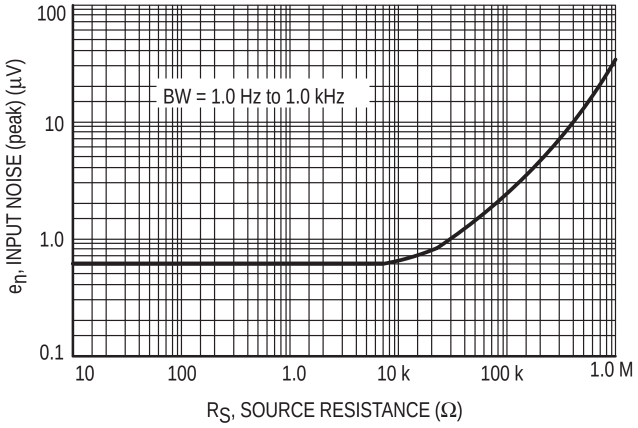


Figure 3. Output Noise versus Source Resistance

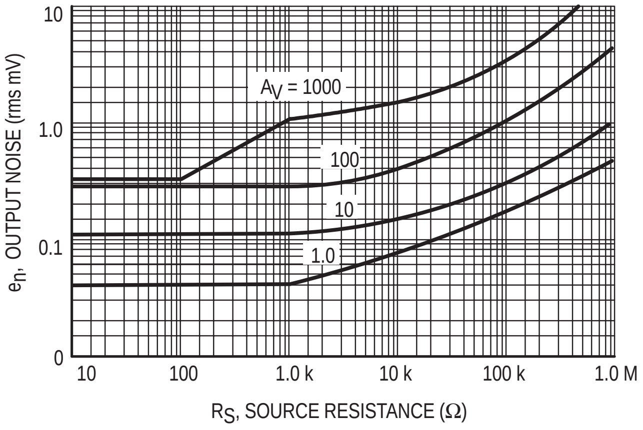


Figure 4. Spectral Noise Density

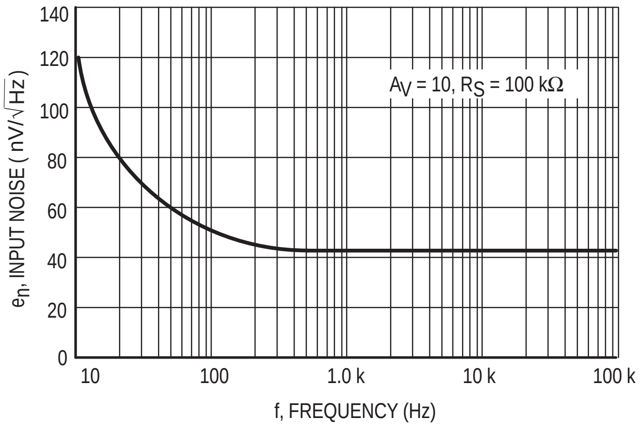
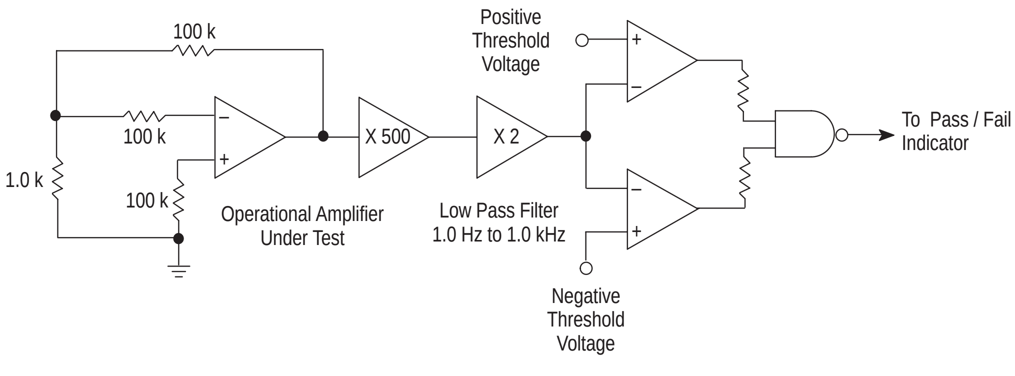


Figure 5. Burst Noise Test Circuit



Unlike conventional peak reading or RMS meters, this system was especially designed to provide the quick response time essential to burst (popcorn) noise testing.

The test time employed is 10 sec and the 20 µV peak limit refers to the operational amplifier input thus eliminating errors in the closed loop gain factor of the operational amplifier .

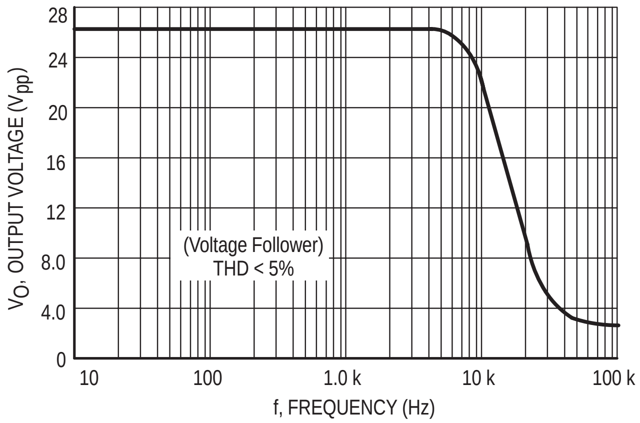


Figure 6. Power Bandwidth (Large Signal Swing versus Frequency)

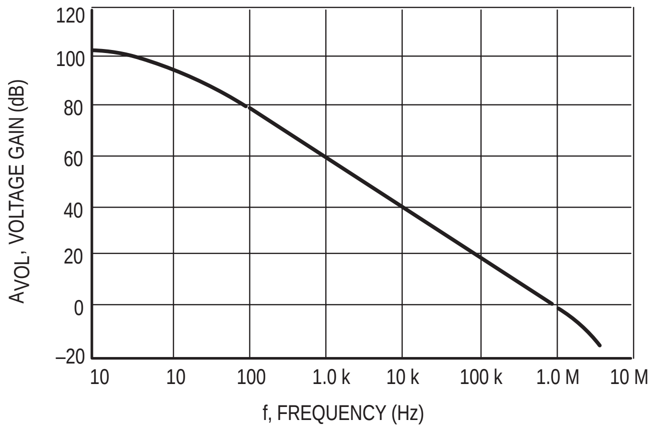


Figure 7. Open Loop Frequency Response

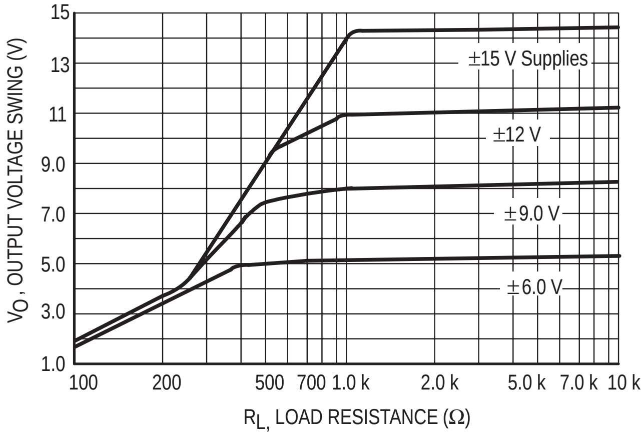


Figure 8. Positive Output Voltage Swing versus Load Resistance

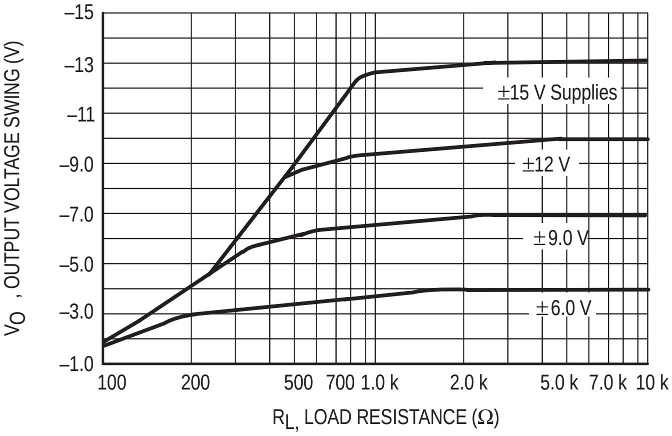


Figure 9. Negative Output Voltage Swing versus Load Resistance

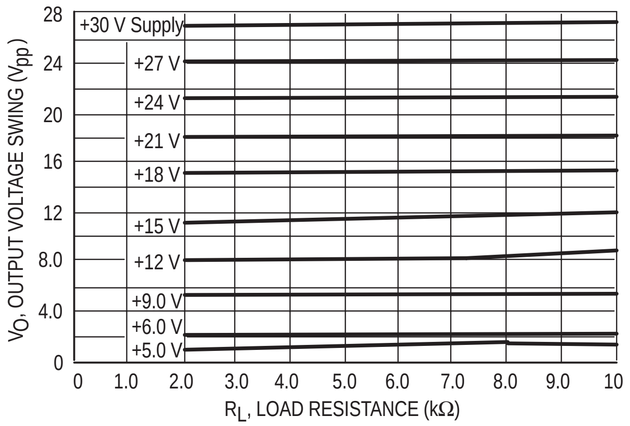


Figure 10. Output Voltage Swing versus Load Resistance (Single Supply Operation)

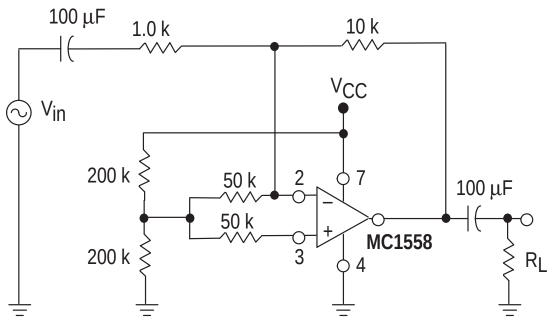


Figure 11. Single Supply Inverting Amplifier

Figure 12. Noninverting Pulse Response

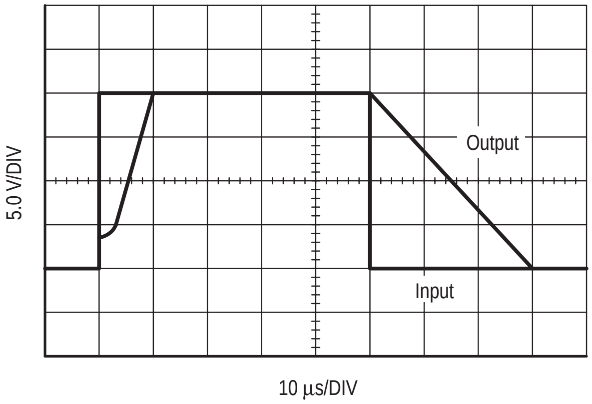


Figure 13. Transient Response Test Circuit

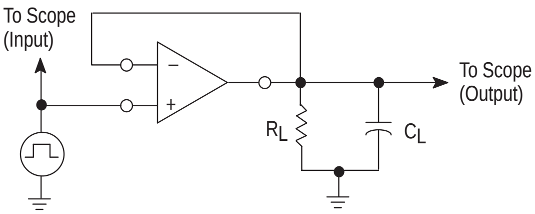


Figure 14. Unused OpAmp

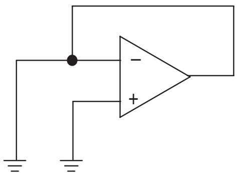
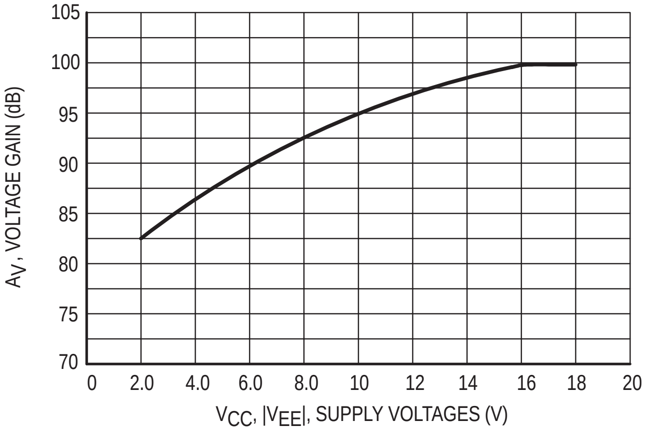


Figure 15. Open Loop Voltage Gain versus Supply Voltage



MOTOROLA

Internally Compensated, High Performance Dual Operational Amplifier

The MCT1458, C was designed for use as a summing amplifier, integrator, or amplifier with operating characteristics as a function of the external feedback components.

- No Frequency Compensation Required
- Short Circuit Protection
- Wide Common Mode and Differential Voltage Ranges
- Low Power Consumption
- No Latch–Up

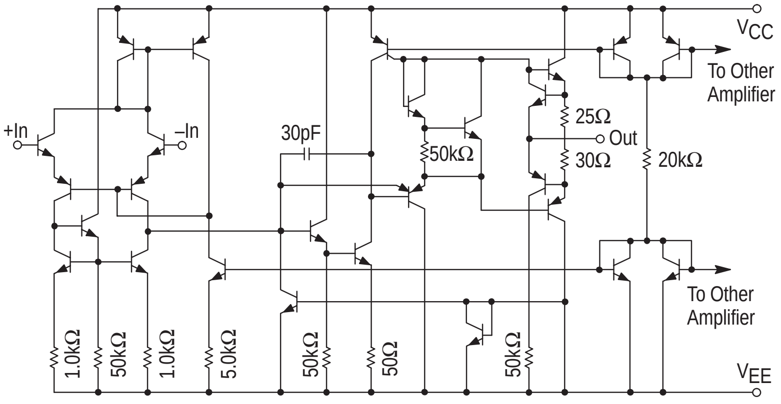
This MCT–prefixed device is intended to be a possible replacement for the similar device with the MC–prefix. Because the MCT device originates from different source material, there may be subtle differences in typical parameter values or characteristic curves. Due to the diversity of potential applications, Motorola can not assure identical performance in all circuits. Motorola recommends that the customer qualify the MCT–prefixed device in each potential application.

MAXIMUM RATINGS (T_A = +25°C, unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC} V_{EE}	+18 –18	Vdc
Input Differential Voltage	V_{ID}	±30	V
Input Common Mode Voltage (Note 1)	V_{ICM}	±15	V
Output Short Circuit Duration (Note 2)	t_{SC}	Continuous	
Operating Ambient Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	–55 to +125	°C
Junction Temperature	T_J	150	°C

NOTES: 1. For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.
2. Supply voltage equal to or less than 15 V.

Representative Schematic Diagram



This device contains 46 active transistors.

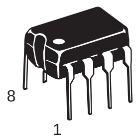
CAUTION: These devices do not have internal ESD protection circuitry and are rated as CLASS 1 devices per the ESD test method in Mil–Std–833D. They should be handled using standard ESD prevention methods to avoid damage to the device.

MCT1458, C

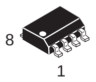
DUAL OPERATIONAL AMPLIFIER

(DUAL MC1741)

SEMICONDUCTOR TECHNICAL DATA

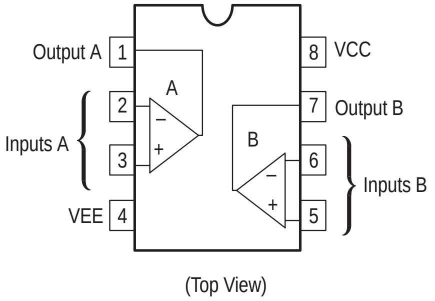


P1 SUFFIX
PLASTIC PACKAGE
CASE 626



D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

PIN CONNECTIONS



ORDERING INFORMATION

Device	Operating Temperature Range	Package
MCT1458CD, D	T_A = 0° to +70°C	SO–8
MCT1458CP1, P1		Plastic

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = –15 V, T_A = 25°C, unless otherwise noted.)

Characteristic	Symbol	MCT1458			MCT1458C			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage ($R_S \le$ 10 k)	V_{IO}	—	2.0	6.0	—	2.0	10	mV
Input Offset Current	I_{IO}	—	20	200	—	20	300	nA
Input Bias Current	I_{IB}	—	80	500	—	80	700	nA
Input Resistance	r_i	0.3	2.0	—	—	2.0	—	MΩ
Input Capacitance	C_i	—	6.0	—	—	6.0	—	pF
Common Mode Input Voltage Range	V_{ICR}	±12	±13	—	±11	±13	—	V
Large Signal Voltage Gain	A_{VOL}							V/mV
(V_O = ±10 V, R_L = 2.0 k)		20	200	—	—	—	—	
(V_O = ±10 V, R_L = 10 k)		—	—	—	20	200	—	
Output Resistance	r_o	—	75	—	—	75	—	Ω
Common Mode Rejection ($R_S \le$ 10 k)	CMR	70	90	—	60	90	—	dB
Supply Voltage Rejection ($R_S \le$ 10 k)	PSR	—	30	150	—	30	—	µV/V
Output Voltage Swing	V_O							V
($R_S \le$ 10 k)		±12	±14	—	±11	±14	—	
($R_S \le$ 2.0 k)		±10	±13	—	±9.0	±13	—	
Output Short Circuit Current	I_{SC}	—	20	—	—	20	—	mA
Supply Currents (Both Amplifiers)	I_D	—	2.3	5.6	—	2.3	8.0	mA
Power Consumption	P_C	—	70	170	—	70	240	mW
Transient Response (Unity Gain)								
(V_I = 20 mV, $R_L \ge$ 2.0 kΩ, $C_L \le$ 100 pF) Rise Time	t_{TLH}	—	0.9	—	—	0.9	—	µs
(V_I = 20 mV, $R_L \ge$ 2.0 kΩ, $C_L \le$ 100 pF) Overshoot	os	—	15	—	—	15	—	%
(V_I = 10 V, $R_L \ge$ 2.0 kΩ, $C_L \le$ 100 pF) Slew Rate	SR	—	0.8	—	—	0.8	—	V/µs

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = –15 V, T_A = T_{high} to T_{low}, unless otherwise noted.)

Characteristic	Symbol	MCT1458			MCT1458C			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage ($R_S \le$ 10 kΩ)	V_{IO}	—	—	7.5	—	—	12	mV
Input Offset Current	I_{IO}							nA
(T_A = 0° to +70°C)		—	—	300	—	—	400	
Input Bias Current	I_{IB}							nA
(T_A = 0° to +70°C)		—	—	800	—	—	1000	
Output Voltage Swing	V_O							V
($R_S \le$ 10 k)		±12	±14	—	—	—	—	
($R_S \le$ 2 k)		±10	±13	—	±9.0	±13	—	
Large Signal Voltage Gain	A_{VOL}							V/mV
(V_O = ±10 V, R_L = 2 k)		15	—	—	—	—	—	
(V_O = ±10 V, R_L = 10 k)		—	—	—	15	—	—	

Figure 1. Power Bandwidth (Large Signal Swing versus Frequency)

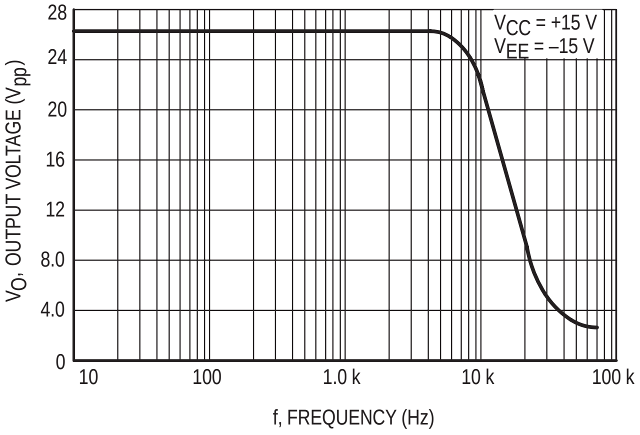


Figure 2. Maximum Output Voltage Swing versus Load Resistance

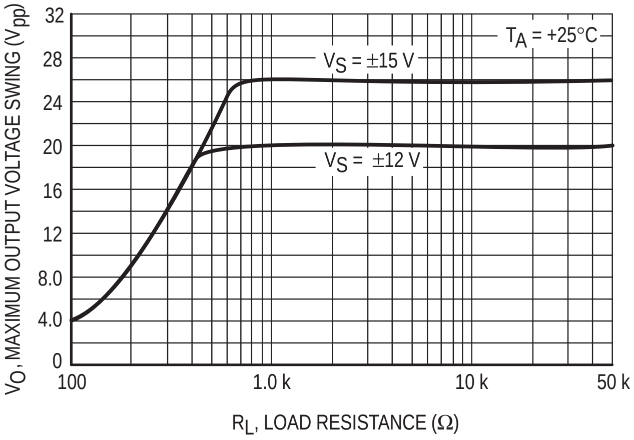


Figure 3. Input Offset Current versus Temperature

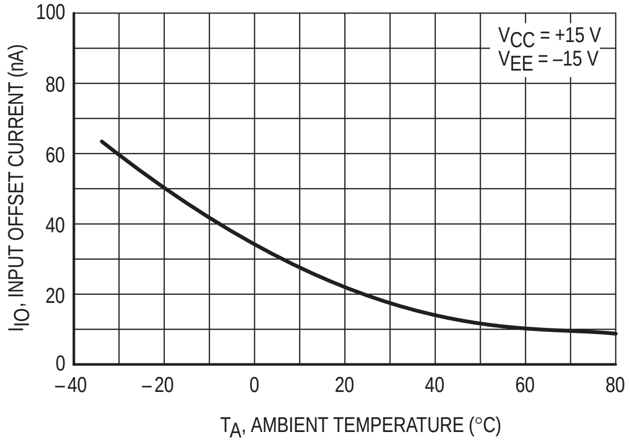


Figure 4. Input Offset Current versus Supply Voltage

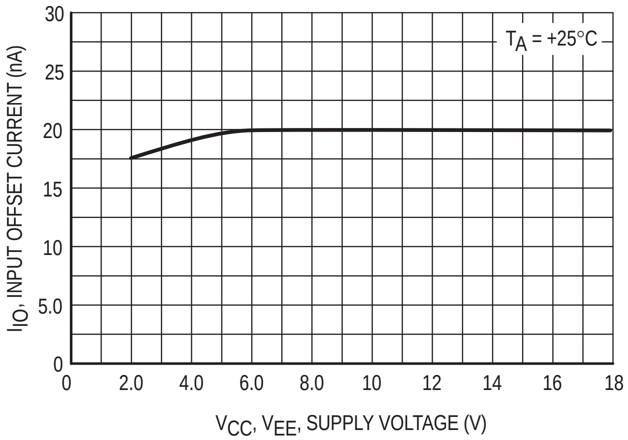


Figure 5. Open Loop Voltage Gain versus Supply Voltage

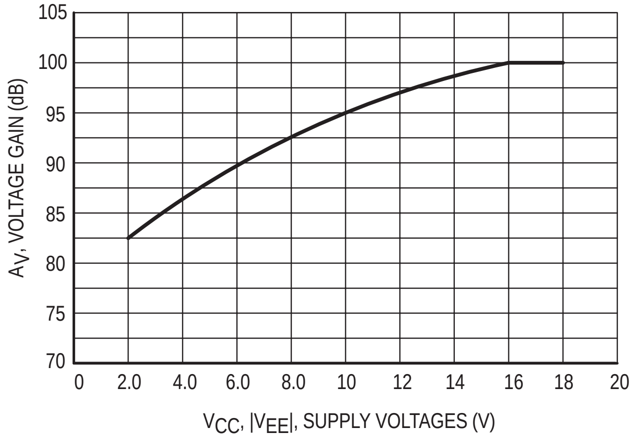
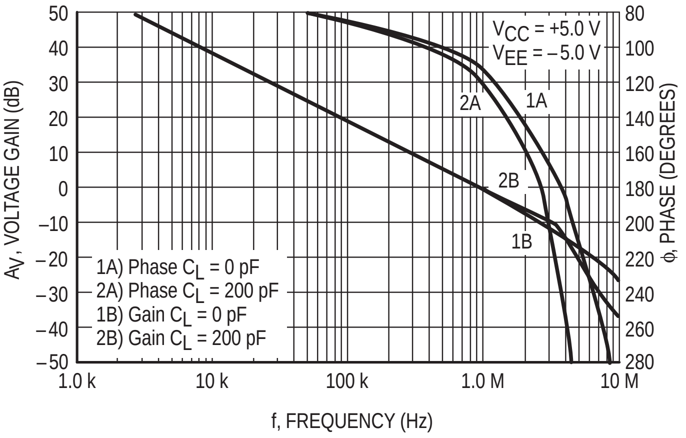


Figure 6. Voltage Gain and Phase versus Frequency



MOTOROLA

MC1490

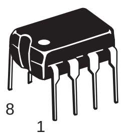
RF/IF/Audio Amplifier

The MC1490 is an integrated circuit featuring wide–range AGC for use in RF/IF amplifiers and audio amplifiers over the temperature range, –40° to +85°C.

- High Power Gain: 50 dB Typ at 10 MHz
  45 dB Typ at 60 MHz
  35 dB Typ at 100 MHz
- Wide Range AGC: 60 dB Min, DC to 60 MHz
- 6.0 V to 15 V Operation, Single Polarity Supply
- See MC1350D for Surface Mount

WIDEBAND AMPLIFIER WITH AGC

SEMICONDUCTOR TECHNICAL DATA



P SUFFIX
PLASTIC PACKAGE
CASE 626

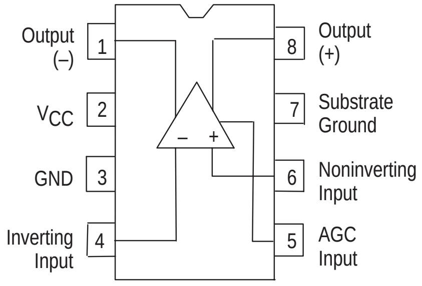
MAXIMUM RATINGS (T_A = +25°C, unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	+18	Vdc
AGC Supply	V_{AGC}	V_{CC}	Vdc
Input Differential Voltage	V_{ID}	5.0	Vdc
Operating Temperature Range	T_A	–40 to +85	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Junction Temperature	T_J	+150	°C

ORDERING INFORMATION

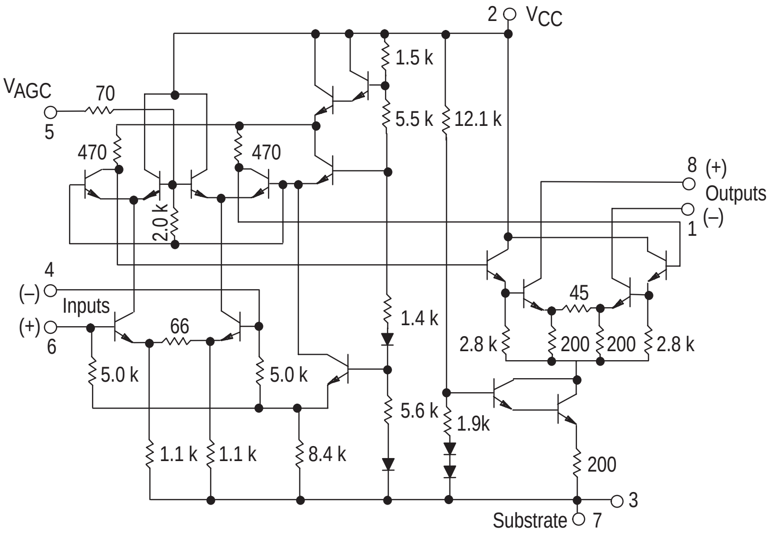
Device	Operating Temperature Range	Package
MC1490P	T_A = –40° to +85°C	Plastic

PIN CONNECTIONS



(Top View)

Representative Schematic Diagram



Pins 3 and 7 should both be connected to circuit ground.

SCATTERING PARAMETERS
(V_{CC} = +12 Vdc, T_A = +25°C, Z_o = 50 Ω)

Parameter	Symbol	f = MHz Typ 30	f = MHz Typ 60	Unit
Input Reflection Coefficient	$\lvert S_{11}\rvert$ θ_{11}	0.95 –7.3	0.93 –16	– deg
Output Reflection Coefficient	$\lvert S_{22}\rvert$ θ_{22}	0.99 –3.0	0.98 –5.5	– deg
Forward Transmission Coefficient	$\lvert S_{21}\rvert$ θ_{21}	16.8 128	14.7 64.3	– deg
Reverse Transmission Coefficient	S_{12} θ_{12}	0.00048 84.9	0.00092 79.2	– deg

ELECTRICAL CHARACTERISTICS (V_{CC} = 12 Vdc, f = 60 MHz, BW = 1.0 MHz, T_A = 25°C)

Characteristic	Figure	Symbol	Min	Typ	Max	Unit
Power Supply Current Drain	–	I_{CC}	–	–	17	mA
AGC Range (AGC) 5.0 V Min to 7.0 V Max	19	M_{AGC}	–60	–	–	dB
Output Stage Current (Sum of Pins 1 and 8)	–	I_O	4.0	–	7.5	mA
Single–Ended Power Gain R_S = R_L = 50 Ω	19	G_P	40	–	–	dB
Noise Figure R_S = 50 Ohms	19	NF	–	6.0	–	dB
Power Dissipation	–	P_D	–	168	204	mW

Figure 1. Unneutralized Power Gain versus Frequency (Tuned Amplifier, See Figure 19)

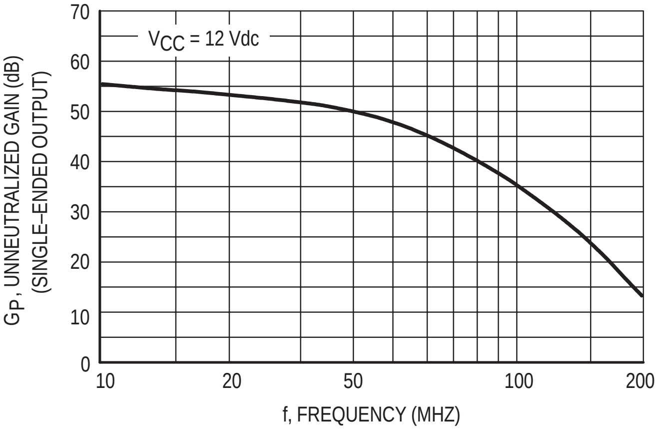


Figure 2. Voltage Gain versus Frequency (Video Amplifier, See Figure 20)

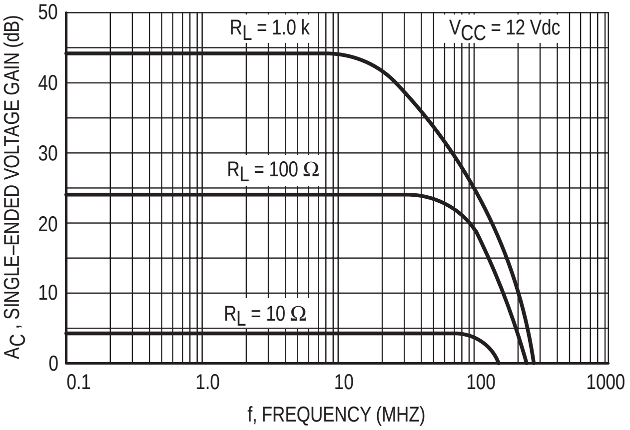


Figure 3. Dynamic Range: Output Voltage versus Input Voltage (Video Amplifier, See Figure 20)

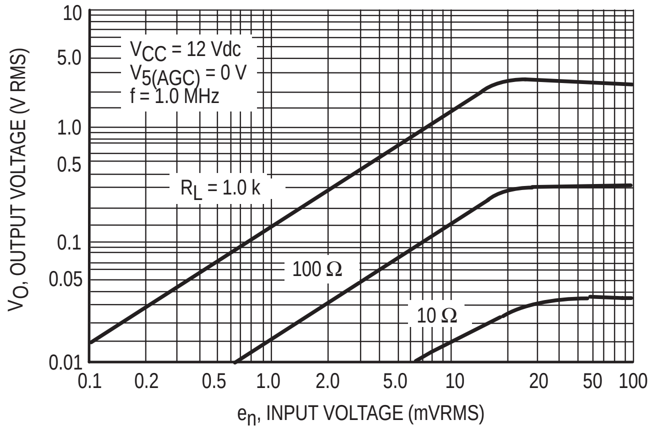


Figure 4. Voltage Gain versus Frequency (Video Amplifier, See Figure 20)

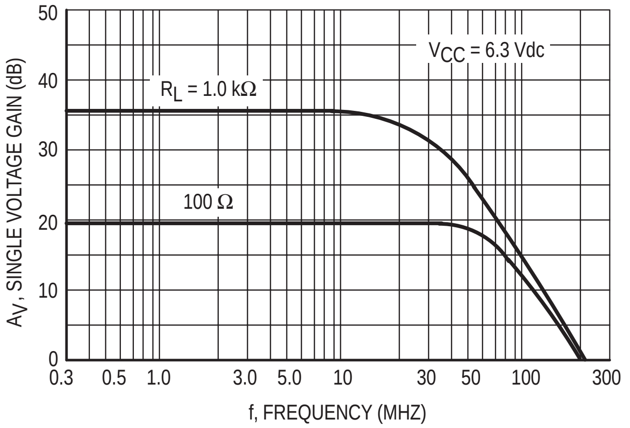


Figure 5. Voltage Gain and Supply Current versus Supply Voltage (Video Amplifier, See Figure 20)

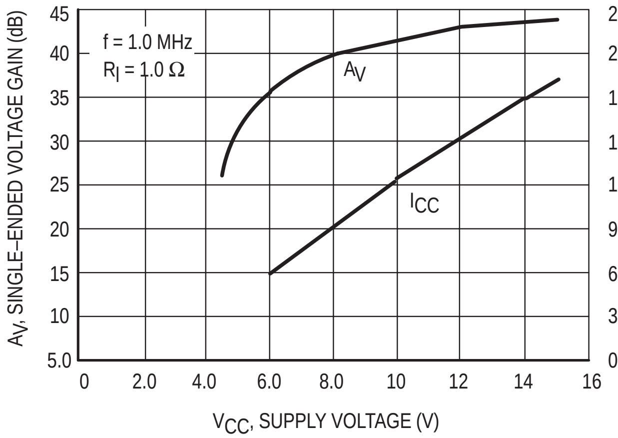


Figure 6. Typical Gain Reduction versus AGC Voltage

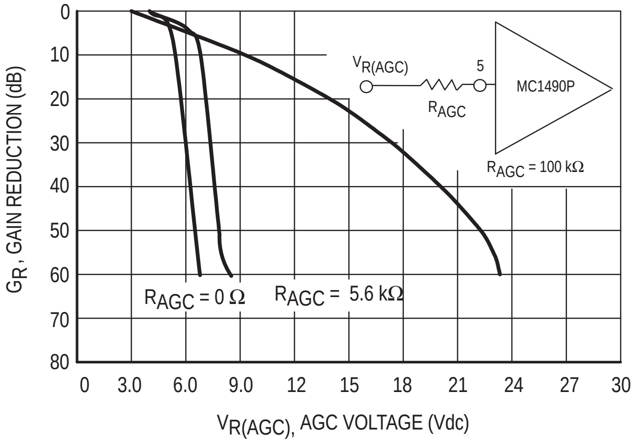


Figure 7. Typical Gain Reduction versus AGC Current

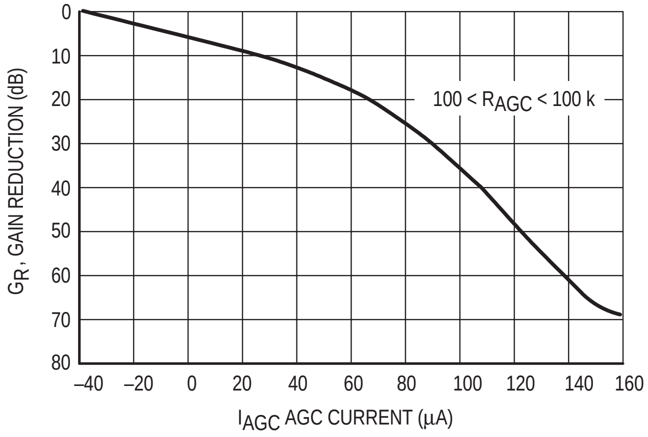


Figure 8. Fixed Tuned Power Gain Reduction versus Temperature (See Test Circuit, Figure 19)

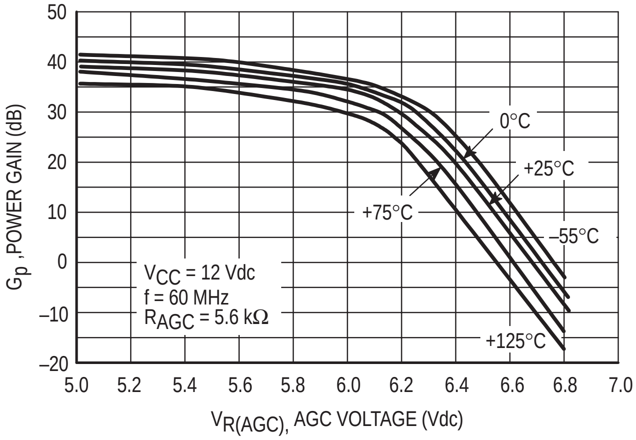


Figure 9. Power Gain versus Supply Voltage (See Test Circuit, Figure 19)

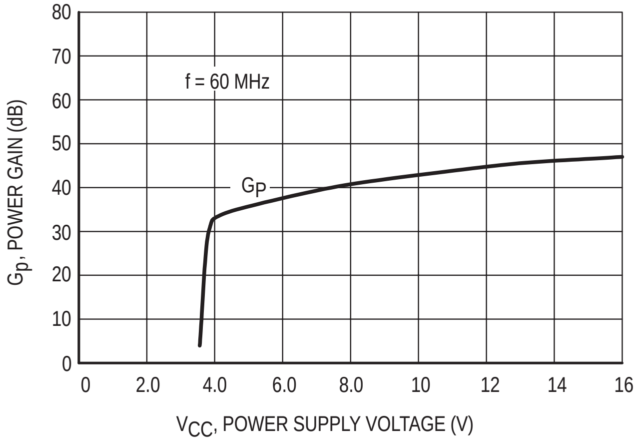


Figure 10. Noise Figure versus Frequency

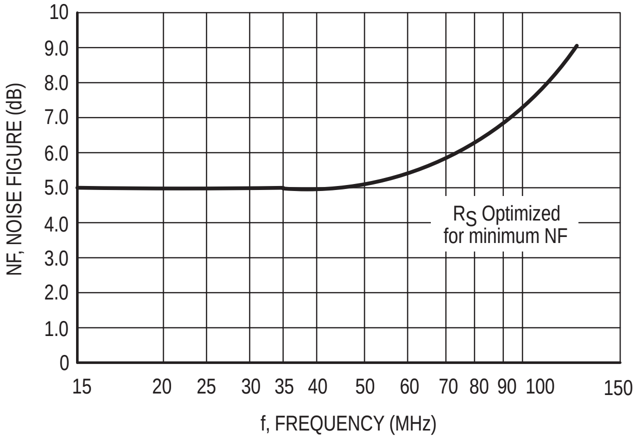


Figure 11. Noise Figure versus Source Resistance

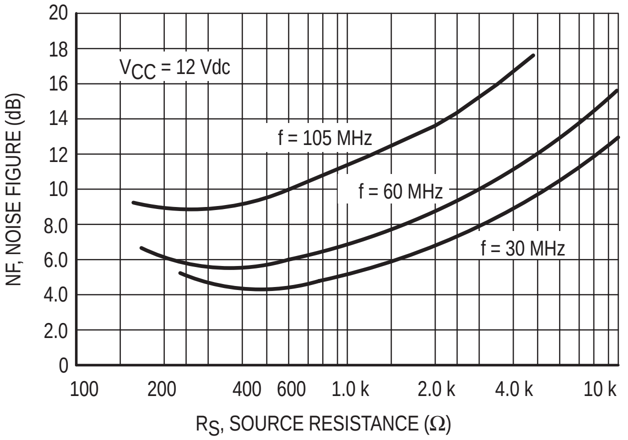


Figure 12. Noise Figure versus AGC Gain Reduction

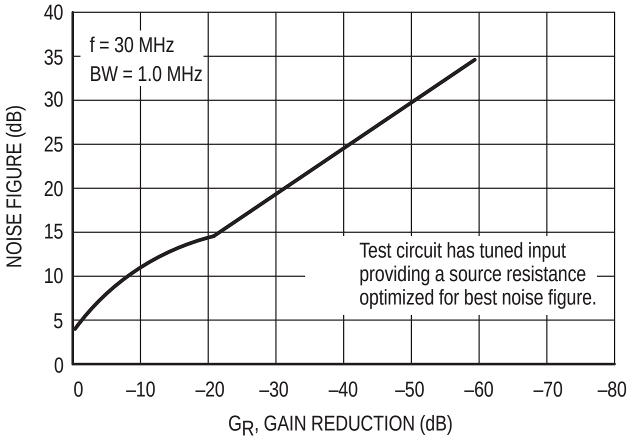


Figure 13. Harmonic Distortion versus AGC Gain Reduction for AM Carrier (For Test Circuit, See Figure 14)

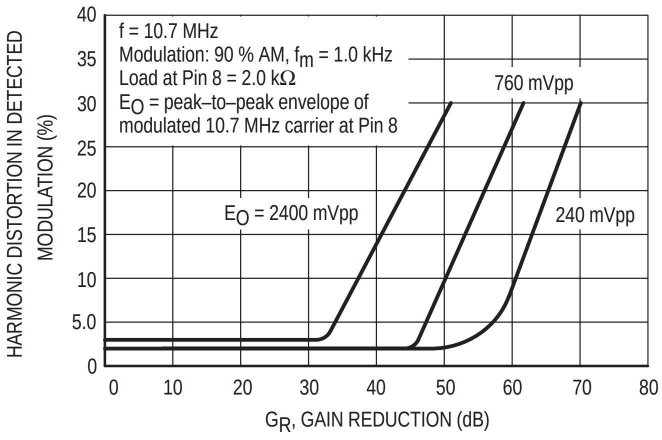
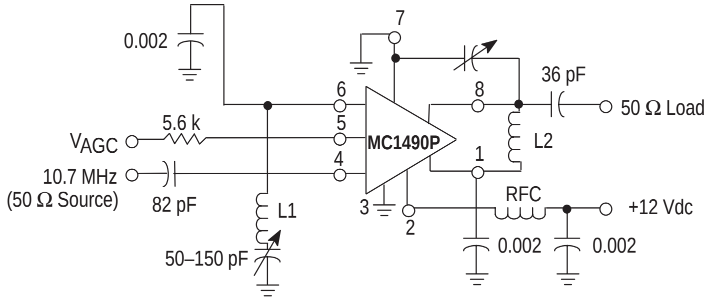


Figure 14. 10.7 MHz Amplifier Gain ≃ 55 dB, BW ≃ 100 kHz



L1 = 24 turns, #22 AWG wire on a T12–44 micro metal Toroid core (–124 pF)

L2 = 20 turns, #22 AWG wire on a T12–44 micro metal Toroid core (–100 pF)

Figure 15. S_{11} and S_{22}, Input and Output Reflection Coefficient

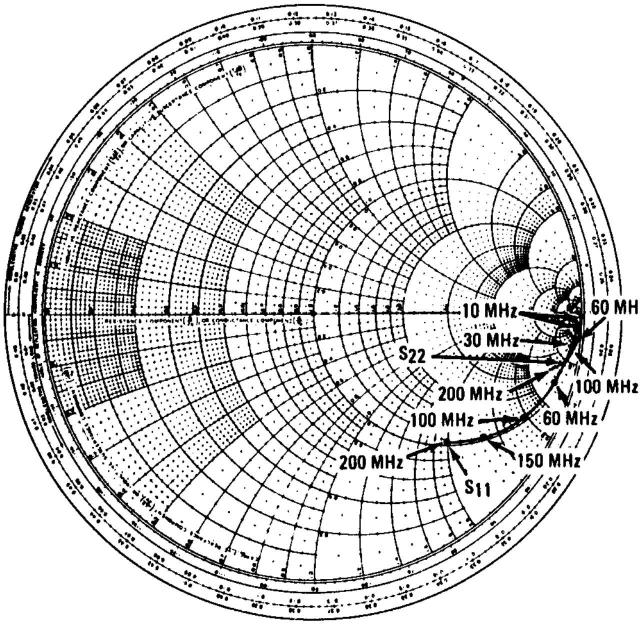


Figure 16. S_{11} and S_{22}, Input and Output Reflection Coefficient

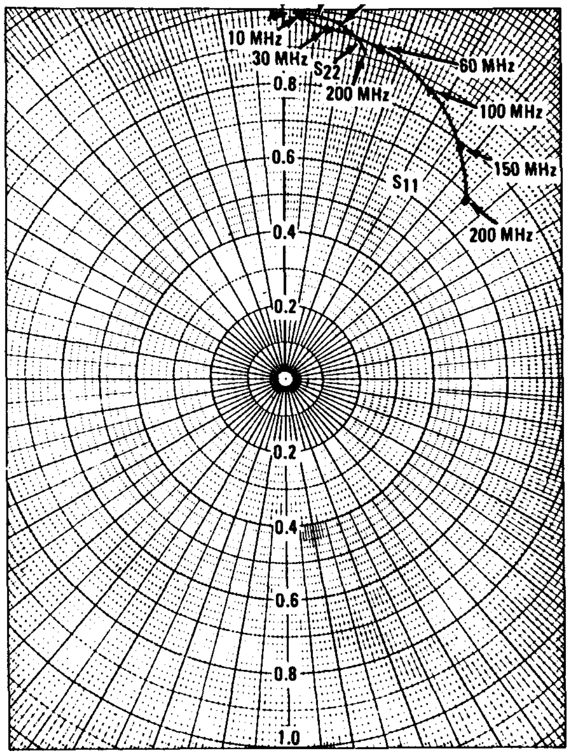


Figure 17. S_{21}, Forward Transmission Coefficient (Gain)

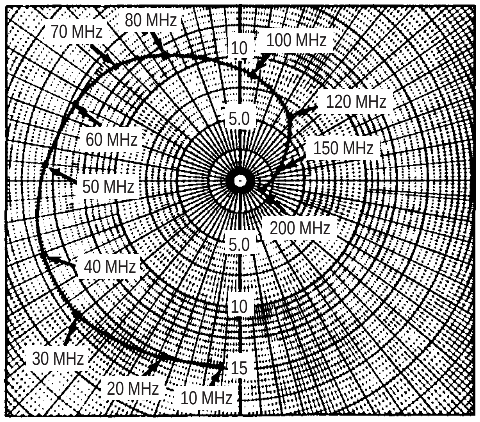


Figure 18. S_{12}, Reverse Transmission Coefficient (Feedback)

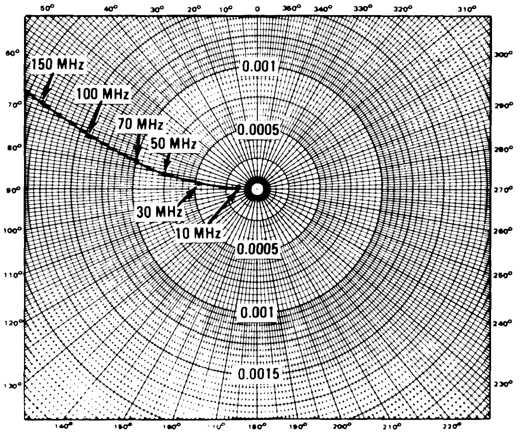
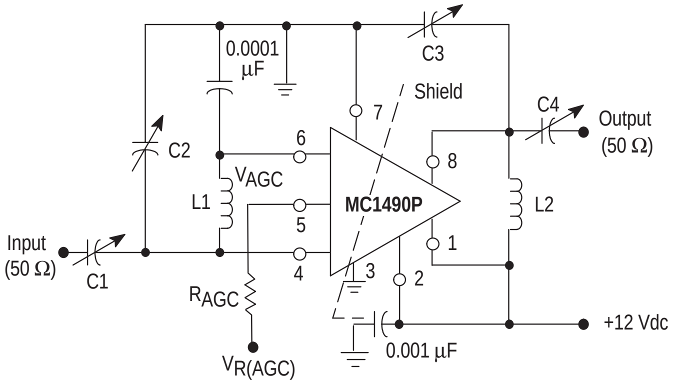


Figure 19. 60 MHz Power Gain Test Circuit



L1 = 7 turns, #20 AWG wire, 5/16″ Dia., 5/8″ long
L2 = 6 turns, #14 AWG wire, 9/16″ Dia., 3/4″ long
C1,C2,C3 = (1–30) pF
C4 = (1–10) pF

Figure 20. Video Amplifier

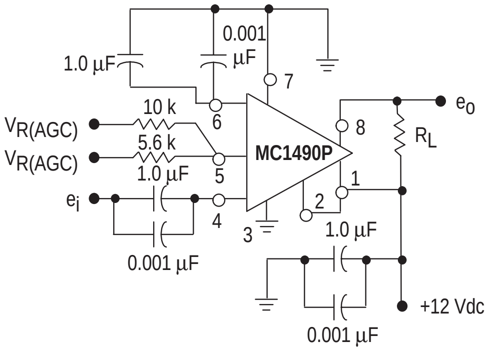
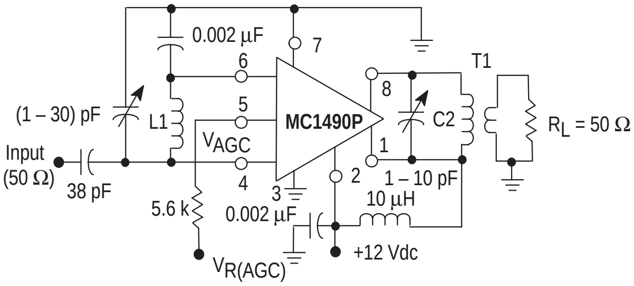
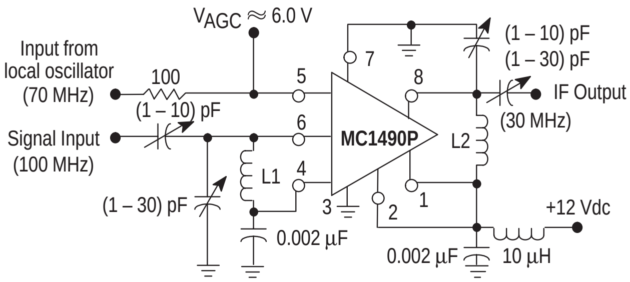


Figure 21. 30 MHz Amplifier (Power Gain = 50 dB, BW ≈ 1.0 MHz)



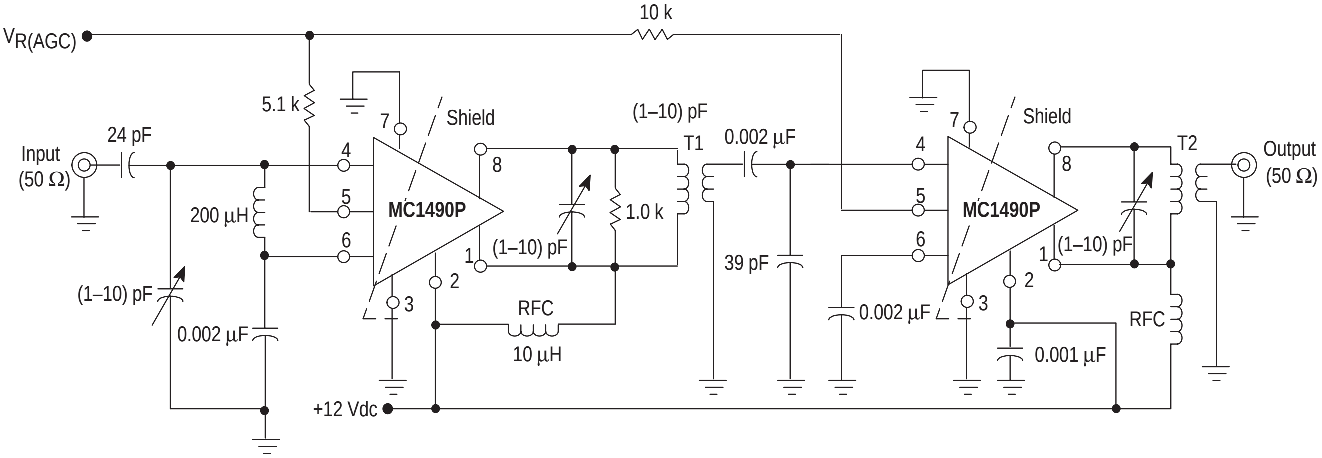
L1 = 12 turns, #22 AWG wire on a Toroid core,
(T37–6 micro metal or equiv).
T1: Primary = 17 turns, #20 AWG wire on a Toroid core, (T44–6).
Secondary = 2 turns, #20 AWG wire.

Figure 22. 100 MHz Mixer



L1 = 5 turns, #16 AWG wire, 1/4″, ID Dia., 5/8″ long
L2 = 16 turns, #20 AWG wire on a Toroid core, (T44–6).

Figure 23. Two–Stage 60 MHz IF Amplifier (Power Gain ≈ 80 dB, BW ≈ 1.5 MHz)



T1: Primary Winding = 15 turns, #22 AWG wire, 1/4″ ID Air Core
Secondary Winding = 4 turns, #22 AWG wire,
Coefficient of Coupling ≈ 1.0

T2: Primary Winding = 10 turns, #22 AWG wire, 1/4″ ID Air Core
Secondary Winding = 2 turns, #22 AWG wire,
Coefficient of Coupling ≈ 1.0

DESCRIPTION OF SPEECH COMPRESSOR

The amplifier drives the base of a PNP transistor operating common–emitter with a voltage gain of approximately 20. The control R1 varies the quiescent Q point of this transistor so that varying amounts of signal exceed the level V_r. Diode D1 rectifies the positive peaks of Q1's output only when these peaks are greater than $V_r \simeq 7.0$ V. The resulting output is filtered by C_X, R_X.

R_X controls the charging time constant or attack time. C_X is involved in both charge and discharge. R2 (the 150 kΩ and input resistance of the emitter–follower Q2) controls the decay time. Making the decay long and attack short is accomplished by making R_X small and R2 large. (A Darlington emitter–follower may be needed if extremely slow decay times are required.)

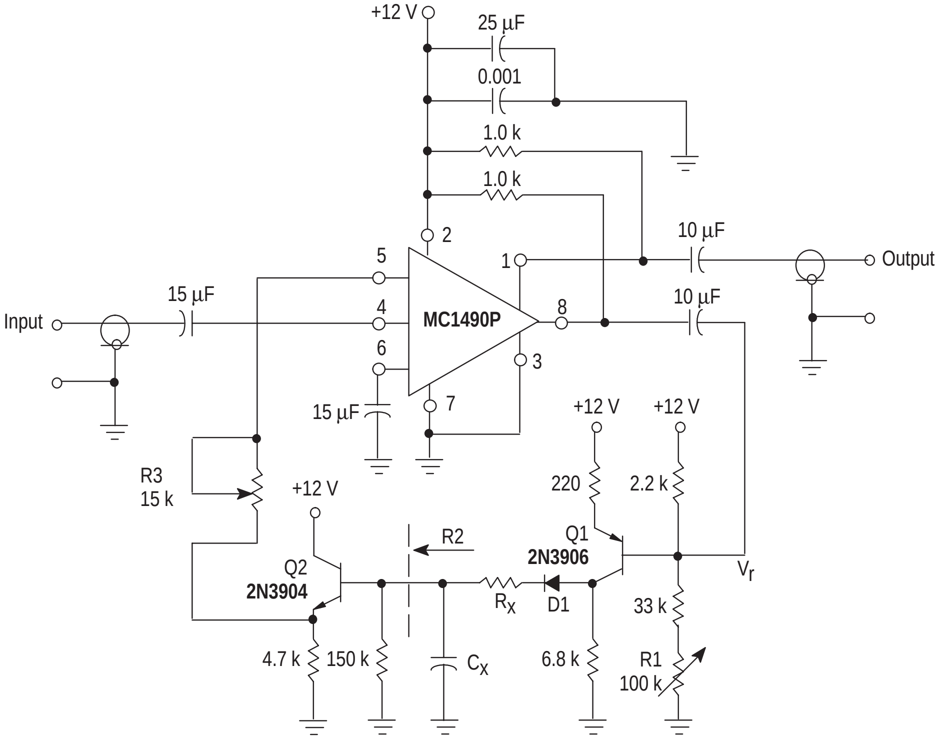
The emitter–follower Q2 drives the AGC Pin 5 of the MC1490P and reduces the gain. R3 controls the slope of signal compression.

Table 1. Distortion versus Frequency

Frequency	Distortion		Distortion	
	10 mV e_i	100 mV e_i	10 mV e_i	100 mV e_i
100 Hz	3.5%	12%	15%	27%
300 Hz	2%	10%	6%	20%
1.0 kHz	1.5%	8%	3%	9%
10 kHz	1.5%	8%	1%	3%
100 kHz	1.5%	8%	1%	3%
	Notes 1 and 2		Notes 3 and 4	

Notes:
(1) Decay = 300 ms
Attack = 20 ms
(2) C_X = 7.5 µF
R_X = 0 (Short)
(3) Decay = 20 ms
Attack = 3.0 ms
(4) C_X = 0.68 µF
R_X = 1.5 kΩ

Figure 24. Speech Compressor



MOTOROLA

MC1741C

Internally Compensated, High Performance Operational Amplifier

The MC1741C was designed for use as a summing amplifier, integrator, or amplifier with operating characteristics as a function of the external feedback components.

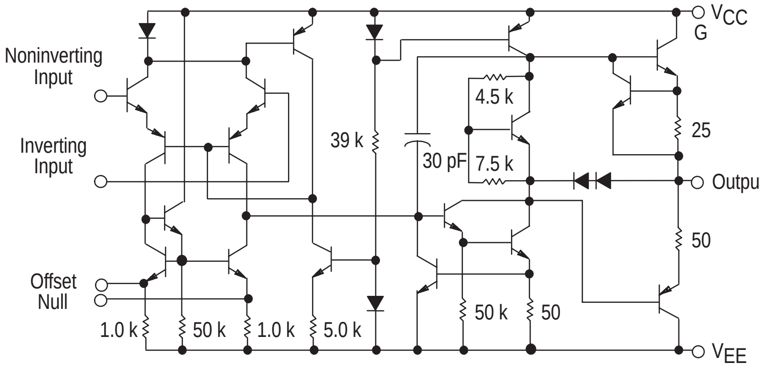
- No Frequency Compensation Required
- Short Circuit Protection
- Offset Voltage Null Capability
- Wide Common Mode and Differential Voltage Ranges
- Low Power Consumption
- No Latch Up

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}, V_{EE}	±18	Vdc
Input Differential Voltage	V_{ID}	±30	V
Input Common Mode Voltage (Note 1)	V_{ICM}	±15	V
Output Short Circuit Duration (Note 2)	t_{SC}	Continuous	
Operating Ambient Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	–55 to +125	°C

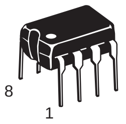
NOTES: 1. For supply voltages less than +15 V, the absolute maximum input voltage is equal to the supply voltage.
2. Supply voltage equal to or less than 15 V.

Equivalent Circuit Schematic
(1/4 of Circuit Shown)

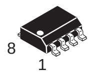


OPERATIONAL AMPLIFIER

SEMICONDUCTOR TECHNICAL DATA

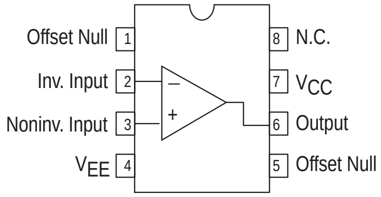


P1 SUFFIX
PLASTIC PACKAGE
CASE 626



D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Alternate	Operating Temperature Range	Package
MC1741CD	–	T_A = 0° to +70°C	SO–8
MC1741CP1	LM741CN µA741TC		Plastic DIP

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = –15 V, T_A = 25°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Offset Voltage ($R_S \le 10$ k)	V_{IO}	–	2.0	6.0	mV
Input Offset Current	I_{IO}	–	20	200	nA
Input Bias Current	I_{IB}	–	80	500	nA
Input Resistance	r_i	0.3	2.0	–	MΩ
Input Capacitance	C_i	–	1.4	–	pF
Offset Voltage Adjustment Range	V_{IOR}	–	±15	–	mV
Common Mode Input Voltage Range	V_{ICR}	±12	±13	–	V
Large Signal Voltage Gain (V_O = ±10 V, $R_L \ge 2.0$ k)	A_{VOL}	20	200	–	V/mV
Output Resistance	r_o	–	75	–	Ω
Common Mode Rejection ($R_S \le 10$ k)	CMR	70	90	–	dB
Supply Voltage Rejection ($R_S \le 10$ k)	PSR	75	–	–	dB
Output Voltage Swing	V_O				V
($R_L \ge 10$ k)		±12	±14	–	
($R_L \ge 2.0$ k)		±10	±13	–	
Output Short Circuit Current	I_{SC}	–	20	–	mA
Supply Current	I_D	–	1.7	2.8	mA
Power Consumption	P_C	–	50	85	mW
Transient Response (Unity Gain, Noninverting)					
(V_I = 20 mV, $R_L \ge$ 2.0 k, $C_L \le 100$ pF) Rise Time	t_{TLH}	–	0.3	–	µs
(V_I = 20 mV, $R_L \ge$ 2.0 k, $C_L \le 100$ pF) Overshoot	os	–	15	–	%
(V_I = 10 V, $R_L \ge$ 2.0 k, $C_L \le 100$ pF) Slew Rate	SR	–	0.5	–	V/µs

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = –15 V, T_A = T_{low} to T_{high}, unless otherwise noted.)*

Characteristic	Symbol	Min	Typ	Max	Unit
Input Offset Voltage ($R_S \le 10$ kΩ)	V_{IO}	–	–	7.5	mV
Input Offset Current (T_A = 0° to +70°C)	I_{IO}	–	–	300	nA
Input Bias Current (T_A = 0° to +70°C)	I_{IB}	–	–	800	nA
Supply Voltage Rejection ($R_S \le 10$ k)	PSR	75	–	–	dB
Output Voltage Swing ($R_L \ge 2.0$ k)	V_O	±10	±13	–	V
Large Signal Voltage Gain ($R_L \ge 2.0$ k, V_O = ±10 V)	A_{VOL}	15	–	–	V/mV

* T_{low} = 0°C T_{high} = 70°C

Figure 1. Burst Noise versus Source Resistance

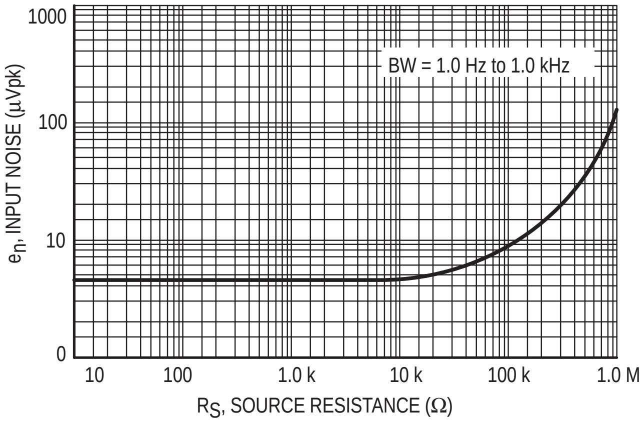


Figure 2. RMS Noise versus Source Resistance

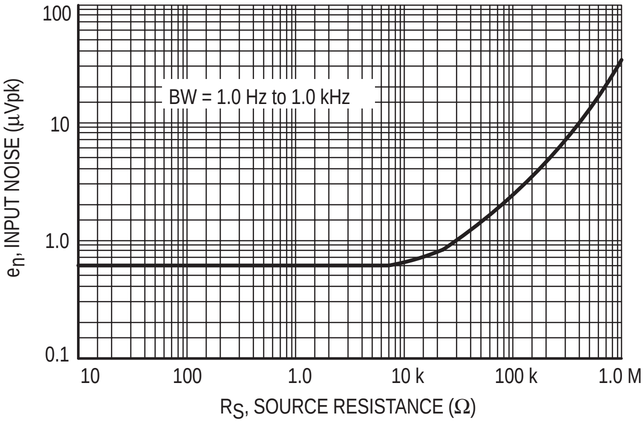


Figure 3. Output Noise versus Source Resistance

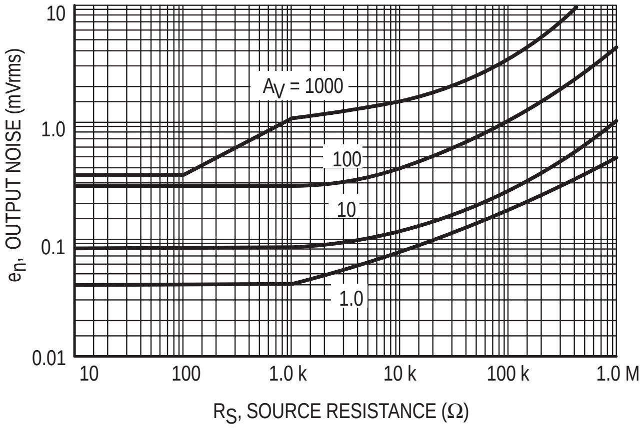


Figure 4. Spectral Noise Density

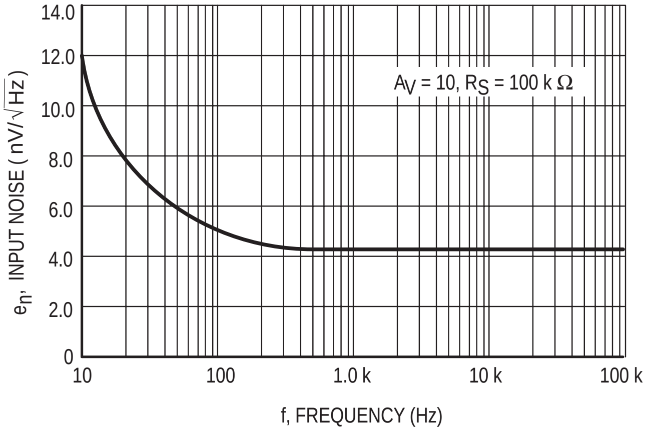
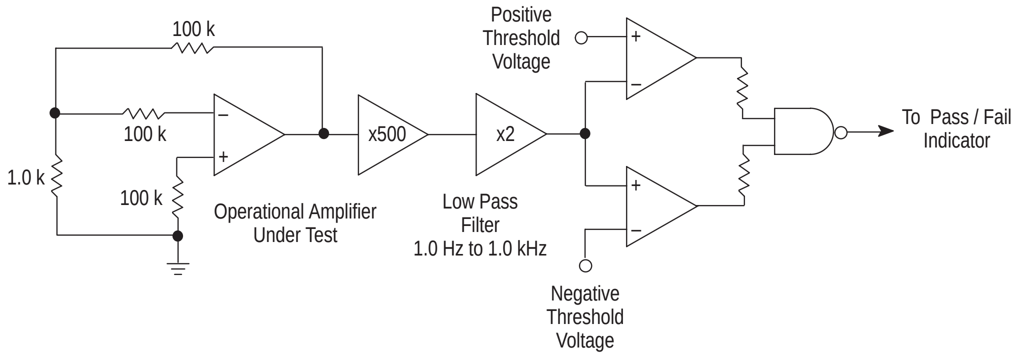


Figure 5. Burst Noise Test Circuit



Unlike conventional peak reading or RMS meters, this system was especially designed to provide the quick response time essential to burst (popcorn) noise testing.

The test time employed is 10 sec and the 20 mV peak limit refers to the operational amplifier input thus eliminating errors in the closed loop gain factor of the operational amplifier.

Figure 6. Power Bandwidth (Large Signal Swing versus Frequency)

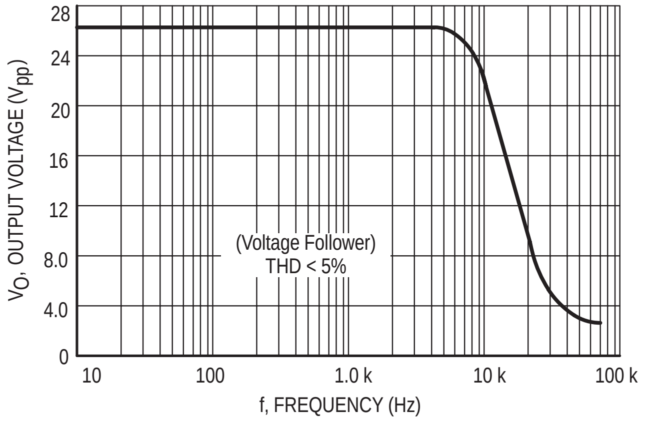


Figure 7. Open Loop Frequency Response

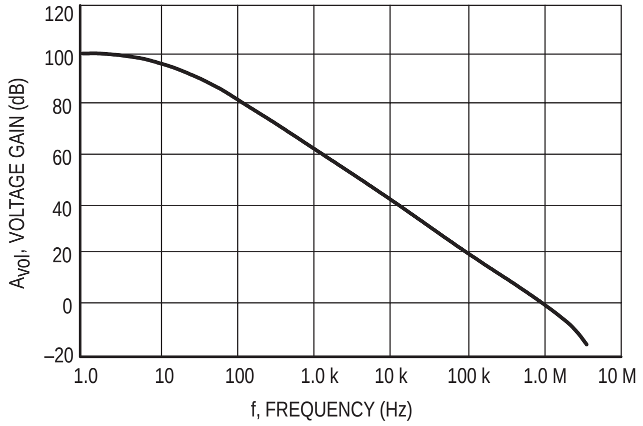


Figure 8. Positive Output Voltage Swing versus Load Resistance

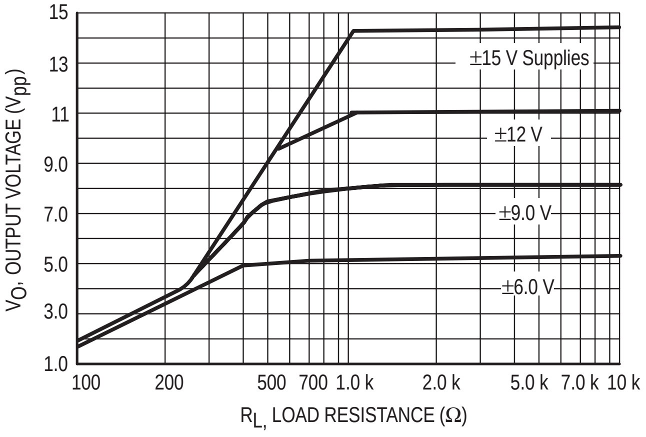


Figure 9. Negative Output Voltage Swing versus Load Resistance

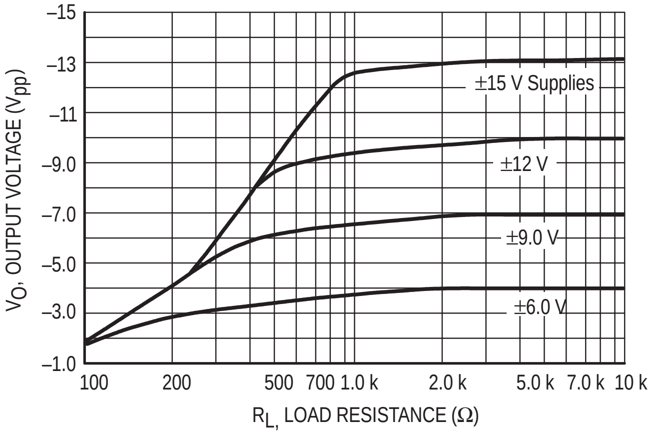


Figure 10. Output Voltage Swing versus Load Resistance (Single Supply Operation)

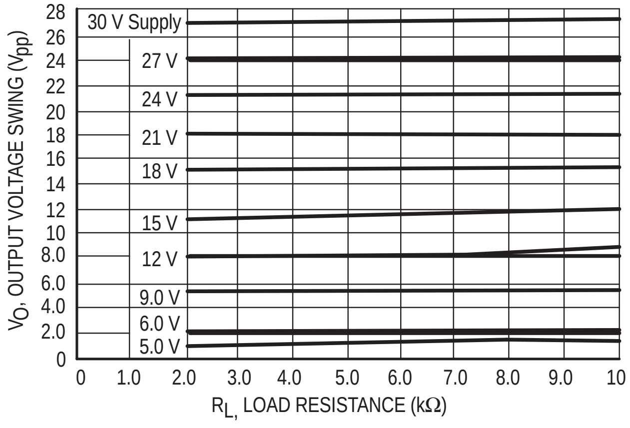


Figure 11. Single Supply Inverting Amplifier

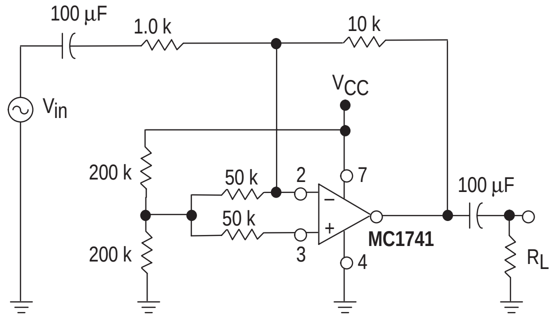


Figure 12. Noninverting Pulse Response

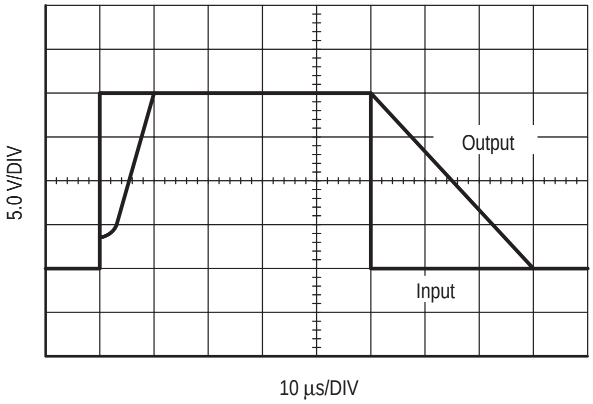


Figure 13. Transient Response Test Circuit

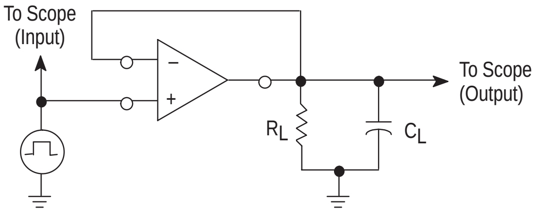
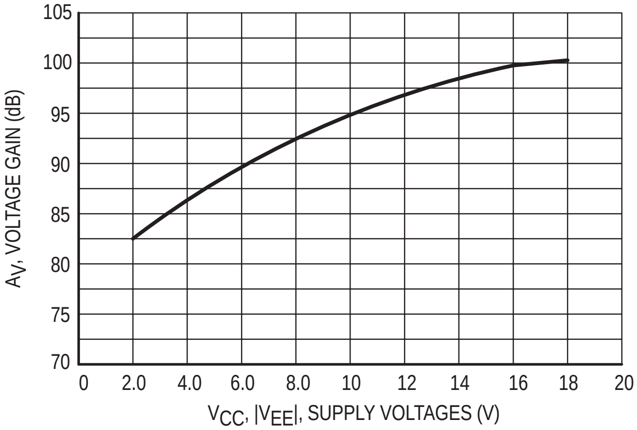


Figure 14. Open Loop Voltage Gain versus Supply Voltage



MOTOROLA

MC1776C

Micropower Programmable Operational Amplifier

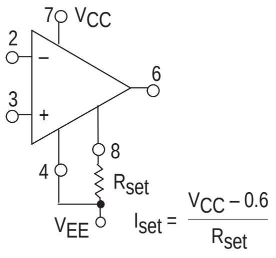
This extremely versatile operational amplifier features low power consumption and high input impedance. In addition, the quiescent currents within the device may be programmed by the choice of an external resistor value or current source applied to the I_{set} input. This allows the amplifier's characteristics to be optimized for input current and power consumption despite wide variations in operating power supply voltages.

- ±1.2 V to ±18 V Operation
- Wide Programming Range
- Offset Null Capability
- No Frequency Compensation Required
- Low Input Bias Currents
- Short Circuit Protection

Resistive Programming

(See Figure 1)

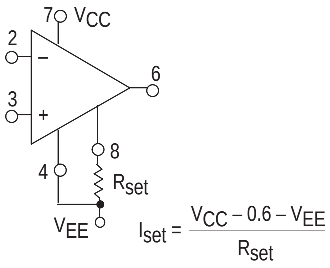
R_{set} to Ground



$$I_{set} = \frac{V_{CC} - 0.6}{R_{set}}$$

R_{set} to Negative Supply

(Recommended for supply voltage less than ±6.0 V)



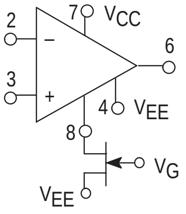
$$I_{set} = \frac{V_{CC} - 0.6 - V_{EE}}{R_{set}}$$

Typical R_{set} Values		
V_{CC}, V_{EE}	I_{set} = 1.5 μA	I_{set} = 15 μA
±6.0 V	3.6 MΩ	360 kΩ
±10 V	6.2 MΩ	620 kΩ
±12 V	7.5 MΩ	750 kΩ
±15 V	10 MΩ	1.0 MΩ

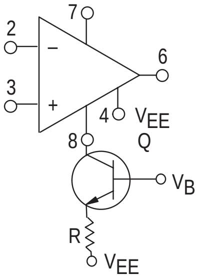
Typical R_{set} Values		
V_{CC}, V_{EE}	I_{set} = 1.5 μA	I_{set} = 15 μA
±1.5 V	1.6 MΩ	160 kΩ
±3.0 V	3.6 MΩ	360 kΩ
±6.0 V	7.5 MΩ	750 kΩ
±15 V	20 MΩ	2.0 MΩ

Active Programming

FET Current Source



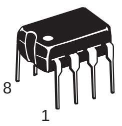
Bipolar Current Source



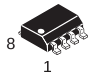
Pins not shown are not connected.

PROGRAMMABLE OPERATIONAL AMPLIFIER

SEMICONDUCTOR TECHNICAL DATA

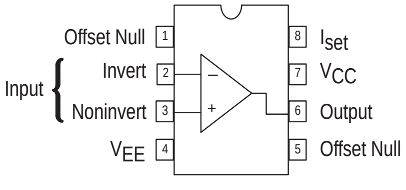


P1 SUFFIX
PLASTIC PACKAGE
CASE 626



D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

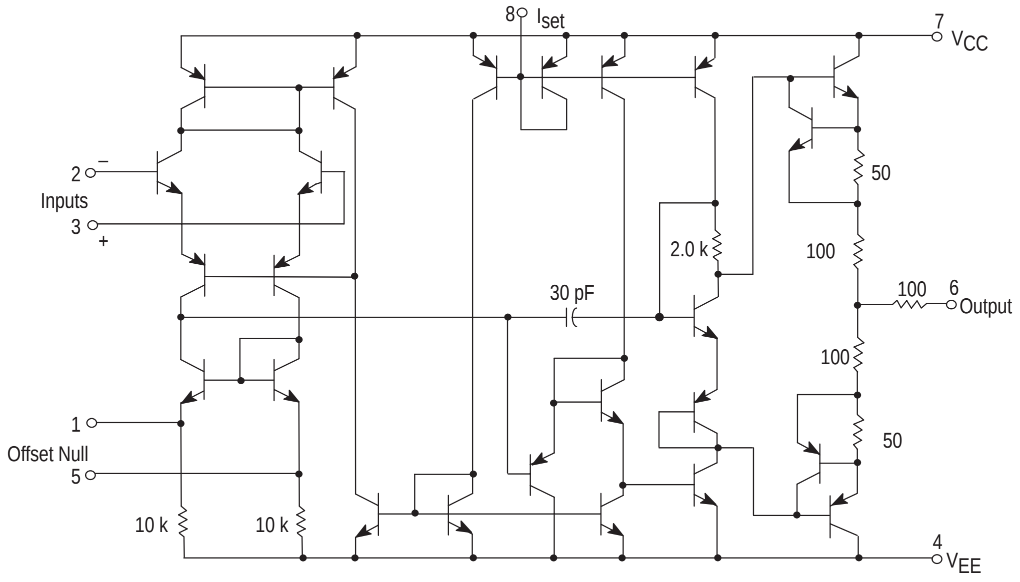
Device	Operating Temperature Range	Package
MC1776CD	T_A = 0° to +70°C	SO–8
MC1776CP1		Plastic DIP

MAXIMUM RATINGS (T_A = +25°C, unless otherwise noted.)

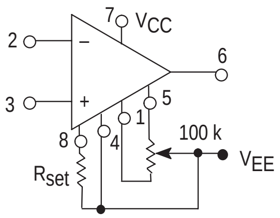
Rating	Symbol	Value	Unit
Power Supply Voltages	V_{CC}, V_{EE}	±18	Vdc
Differential Input Voltage	V_{ID}	±30	Vdc
Common Mode Input Voltage V_{CC} and $\lvert V_{EE}\rvert < 15$ V V_{CC} and $\lvert V_{EE}\rvert \geq 15$ V	V_{ICM}	 V_{CC}, V_{EE} ±15	Vdc
Offset Null to V_{EE} Voltage	$V_{off}–V_{EE}$	±0.5	Vdc
Programming Current	I_{set}	500	µA
Programming Voltage (Voltage from I_{set} Terminal to Ground)	V_{set}	(V_{CC} –2.0 V) to V_{CC}	Vdc
Output Short Circuit Duration (Note 1)	t_{SC}	Indefinite	sec
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Junction Temperature	T_J	150	°C

NOTE 1. May be to ground or either supply voltage. Rating applies up to a case temperature of +125°C or ambient temperature of +70°C and $I_{set} \leq 30$ µA.

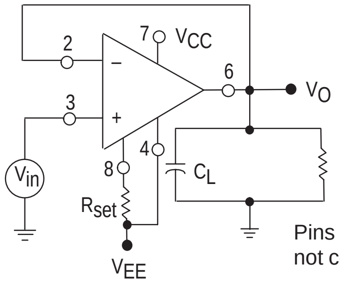
Representative Schematic Diagram



Voltage Offset Null Circuit



Transient Response Test Circuit



Pins not shown are not connected.

ELECTRICAL CHARACTERISTICS (V_{CC} = +3.0 V, V_{EE} = –3.0 V, I_{set} = 1.5 µA, T_A = +25°C, unless otherwise noted.*)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Offset Voltage ($R_S \leq 10$ kΩ)	V_{IO}				mV
T_A = +25°C		–	2.0	6.0	
$T_{low}^* \leq T_A \leq T_{high}^*$		–	–	7.5	
Offset Voltage Adjustment Range	V_{IOR}	–	9.0	–	mV
Input Offset Current	I_{IO}				nA
T_A = +25°C		–	0.7	6.0	
$T_A = T_{high}$		–	–	6.0	
$T_A = T_{low}$		–	–	10	
Input Bias Current	I_{IB}				nA
T_A = +25°C		–	2.0	10	
$T_A = T_{high}$		–	–	10	
$T_A = T_{low}$		–	–	20	
Input Resistance	r_i	–	50	–	MΩ
Input Capacitance	c_i	–	2.0	–	pF
Input Voltage Range	V_{ID}				V
$T_{low} \leq T_A \leq T_{high}$		+1.0	–	–	
Large Signal Voltage Gain	A_{VOL}				V/V
$R_L \geq 75$ kΩ, $V_O = \pm1.0$ V, T_A = +25°C		25 k	200 k	–	
$R_L \geq 75$ kΩ, $V_O = \pm1.0$ V, $T_{low} \leq T_A \leq T_{high}$		25 k	–	–	
Output Voltage Swing	V_O				V
$R_L \geq 75$ kΩ, $T_{low} \leq T_A \leq T_{high}$		±2.0	±2.4	–	
Output Resistance	r_o	–	5.0	–	kΩ
Output Short Circuit Current	I_{SC}	–	3.0	–	mA
Common Mode Rejection	CMR				dB
$R_S \leq 10$ kΩ, $T_{low} \leq T_A \leq T_{high}$		70	86	–	
Supply Voltage Rejection Ratio	PSRR				µV/V
$R_S \leq 10$ kΩ, $T_{low} \leq T_A \leq T_{high}$		–	25	200	
Supply Current	I_{CC}, I_{EE}				µA
T_A = +25°C		–	13	20	
$T_{low} \leq T_A \leq T_{high}$		–	–	25	
Power Dissipation	P_D				µW
T_A = +25°C		–	78	120	
$T_{low} \leq T_A \leq T_{high}$		–	–	150	
Transient Response (Unity Gain)					
V_{in} = 20 mV, $R_L \geq 5.0$ kΩ, C_L = 100 pF					
Rise Time	t_{TLH}	–	3.0	–	µs
Overshoot	os	–	0	–	%
Slew Rate ($R_L \geq 5.0$ kΩ)	S_R	–	0.03	–	V/µs

*T_{low} = 0°C T_{high} = +70°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +3.0 V, V_{EE} = –3.0 V, I_{set} = 15 µA, T_A = +25°C, unless otherwise noted.*)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Offset Voltage ($R_S \leq$ 10 kΩ) T_A = +25°C $T_{low}* \leq T_A \leq T_{high}*$	V_{IO}	 – –	 2.0 –	 6.0 7.5	mV
Offset Voltage Adjustment Range	V_{IOR}	–	18	–	mV
Input Offset Current T_A = +25°C $T_A = T_{high}$ $T_A = T_{low}$	I_{IO}	 – – –	 2.0 – –	 25 25 40	nA
Input Bias Current T_A = +25°C $T_A = T_{high}$ $T_A = T_{low}$	I_{IB}	 – – –	 15 – –	 50 50 100	nA
Input Resistance	r_i	–	5.0	–	MΩ
Input Capacitance	c_i	–	2.0	–	pF
Input Voltage Range $T_{low} \leq T_A \leq T_{high}$	V_{ID}	 ±1.0	 –	 –	V
Large Signal Voltage Gain $R_L \geq$ 5.0 kΩ, V_O = ±1.0 V, T_A = +25°C $R_L \geq$ 5.0 kΩ, V_O = ±1.0 V, $T_{low} \leq T_A \leq T_{high}$	A_{VOL}	 25 k 25 k	 200 k –	 – –	V/V
Output Voltage Swing $R_L \geq$ 5.0 kΩ, $T_{low} \leq T_A \leq T_{high}$	V_O	 ±2.0	 ±2.1	 –	V
Output Resistance	r_o	–	1.0	–	kΩ
Output Short Circuit Current	I_{SC}	–	5.0	–	mA
Common Mode Rejection $R_S \leq$ 10 kΩ, $T_{low} \leq T_A \leq T_{high}$	CMR	 70	 86	 –	dB
Supply Voltage Rejection Ratio $R_S \leq$ 10 kΩ, $T_{low} \leq T_A \leq T_{high}$	PSRR	 –	 25	 200	µV/V
Supply Current T_A = +25°C $T_{low} \leq T_A \leq T_{high}$	I_{CC}, I_{EE}	 – –	 130 –	 170 180	µA
Power Dissipation T_A = +25°C $T_{low} \leq T_A \leq T_{high}$	P_D	 – –	 780 –	 1020 1080	µW
Transient Response (Unity Gain) V_{in} = 20 mV, $R_L \geq$ 5.0 kΩ, C_L = 100 pF Rise Time Overshoot	 t_{TLH} os	 – –	 0.6 5.0	 – –	 µs %
Slew Rate ($R_L \geq$ 5.0 kΩ)	S_R	–	0.35	–	V/µs

*T_{low} = 0°C T_{high} = +70°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = –15 V, I_{set} = 1.5 µA, T_A = +25°C, unless otherwise noted.*)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Offset Voltage ($R_S \le 10$ kΩ)	V_{IO}				mV
T_A = +25°C		–	2.0	6.0	
$T_{low}{}^* \le T_A \le T_{high}{}^*$		–	–	7.5	
Offset Voltage Adjustment Range	V_{IOR}	–	9.0	–	mV
Input Offset Current	I_{IO}				nA
T_A = +25°C		–	0.7	6.0	
$T_A = T_{high}$		–	–	6.0	
$T_A = T_{low}$		–	–	10	
Input Bias Current	I_{IB}				nA
T_A = +25°C		–	2.0	10	
$T_A = T_{high}$		–	–	10	
$T_A = T_{low}$		–	–	20	
Input Resistance	r_i	–	50	–	MΩ
Input Capacitance	c_i	–	2.0	–	pF
Input Voltage Range	V_{ID}				V
$T_{low} \le T_A \le T_{high}$		±10	–	–	
Large Signal Voltage Gain	A_{VOL}				V/V
$R_L \ge 75$ kΩ, $V_O = \pm 10$ V, T_A = +25°C		50 k	400 k	–	
$R_L \ge 75$ kΩ, $V_O = \pm 10$ V, $T_{low} \le T_A \le T_{high}$		50 k	–	–	
Output Voltage Swing	V_O				V
$R_L \ge 75$ kΩ, T_A = +25°C		±12	±14	–	
$R_L \ge 75$ kΩ, $T_{low} \le T_A \le T_{high}$		±10	–	–	
Output Resistance	r_o	–	5.0	–	kΩ
Output Short Circuit Current	I_{SC}	–	3.0	–	mA
Common Mode Rejection	CMR				dB
$R_S \le$ 10 kΩ, $T_{low} \le T_A \le T_{high}$		70	90	–	
Supply Voltage Rejection Ratio	PSRR				µV/V
$R_S \le$ 10 kΩ, $T_{low} \le T_A \le T_{high}$		–	25	200	
Supply Current	I_{CC}, I_{EE}				µA
T_A = +25°C		–	20	30	
$T_{low} \le T_A \le T_{high}$		–	–	35	
Power Dissipation	P_D				mW
T_A = +25°C		–	780	0.9	
$T_{low} \le T_A \le T_{high}$		–	–	1.05	
Transient Response (Unity Gain)					
V_{in} = 20 mV, $R_L \ge$ 5.0 kΩ, C_L = 100 pF					
Rise Time	t_{TLH}	–	1.6	–	µs
Overshoot	os	–	0	–	%
Slew Rate ($R_L \ge$ 5.0 kΩ)	S_R	–	0.1	–	V/µs

*T_{low} = 0°C T_{high} = +70°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = –15 V, I_{set} = 15 µA, T_A = +25°C, unless otherwise noted.*)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Offset Voltage (R_S ≤ 10 kΩ) T_A = +25°C T_{low}* ≤ T_A ≤ T_{high}*	V_{IO}	 – –	 2.0 –	 6.0 7.5	mV
Offset Voltage Adjustment Range	V_{IOR}	–	18	–	mV
Input Offset Current T_A = +25°C T_A = T_{high} T_A = T_{low}	I_{IO}	 – – –	 2.0 – –	 25 25 40	nA
Input Bias Current T_A = +25°C T_A = T_{high} T_A = T_{low}	I_{IB}	 – – –	 15 – –	 50 50 100	nA
Input Resistance	r_i	–	5.0	–	MΩ
Input Capacitance	c_i	–	2.0	–	pF
Input Voltage Range T_{low} ≤ T_A ≤ T_{high}	V_{ID}	 ±10	 –	 –	V
Large Signal Voltage Gain R_L ≥ 5.0 kΩ, V_O = ±10 V, T_A = +25°C R_L ≥ 75 kΩ, V_O = ±10 V, T_{low} ≤ T_A ≤ T_{high}	A_{VOL}	 50 k 50 k	 400 k –	 – –	V/V
Output Voltage Swing R_L ≥ 5.0 kΩ, T_A = +25°C R_L ≥ 75 kΩ, T_{low} ≤ T_A ≤ T_{high}	V_O	 ±10 ±10	 ±13 –	 – –	V
Output Resistance	r_o	–	1.0	–	kΩ
Output Short Circuit Current	I_{SC}	–	12	–	mA
Common Mode Rejection R_S ≤ 10 kΩ, T_{low} ≤ T_A ≤ T_{high}	CMR	 70	 90	 –	dB
Supply Voltage Rejection Ratio R_S ≤ 10 kΩ, T_{low} ≤ T_A ≤ T_{high}	PSRR	 –	 25	 200	µV/V
Supply Current T_A = +25°C T_{low} ≤ T_A ≤ T_{high}	I_{CC}, I_{EE}	 – –	 160 –	 190 200	µA
Power Dissipation T_A = +25°C T_{low} ≤ T_A ≤ T_{high}	P_D	 – –	 – –	 5.7 6.0	µW
Transient Response (Unity Gain) V_{in} = 20 mV, R_L ≥ 5.0 kΩ, C_L = 100 pF Rise Time Overshoot	 t_{TLH} os	 – –	 0.35 10	 – –	 µs %
Slew Rate (R_L ≥ 5.0 kΩ)	S_R	–	0.8	–	V/µs

*T_{low} = 0°C T_{high} = +70°C

Figure 1. Set Current versus Set Resistor

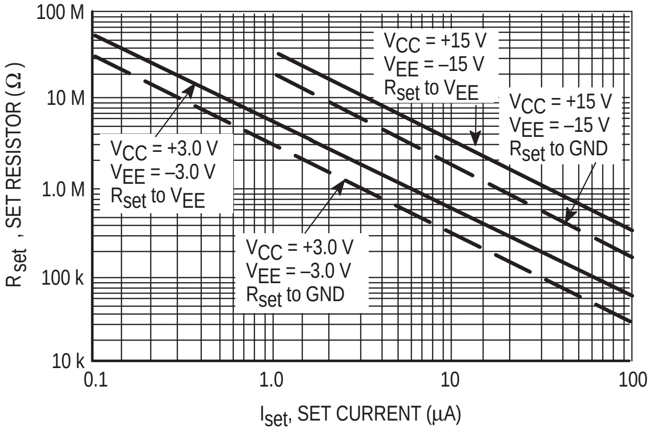


Figure 2. Positive Standby Supply Current versus Set Current

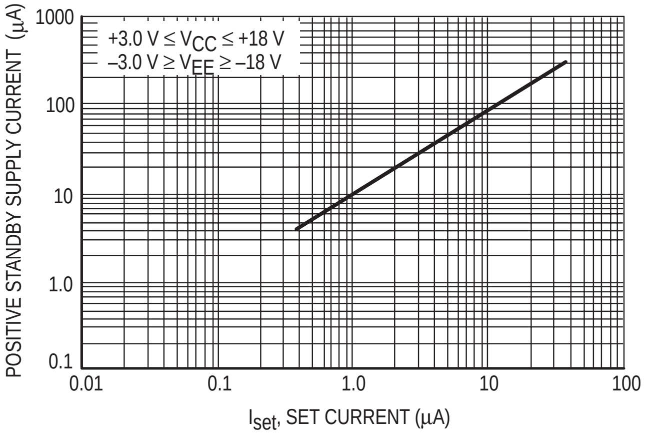


Figure 3. Open Loop Gain versus Set Current

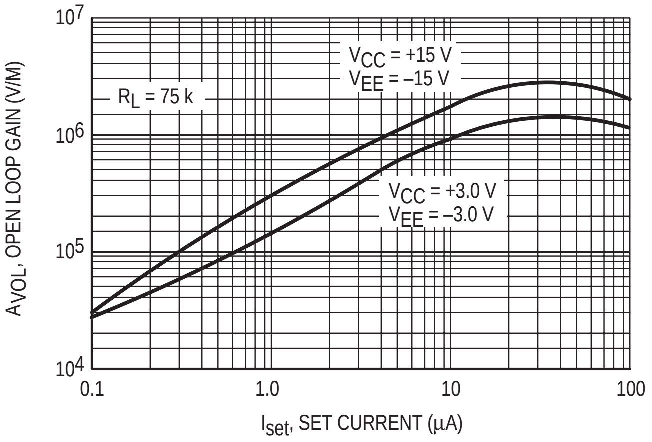


Figure 4. Input Bias Current versus Set Current

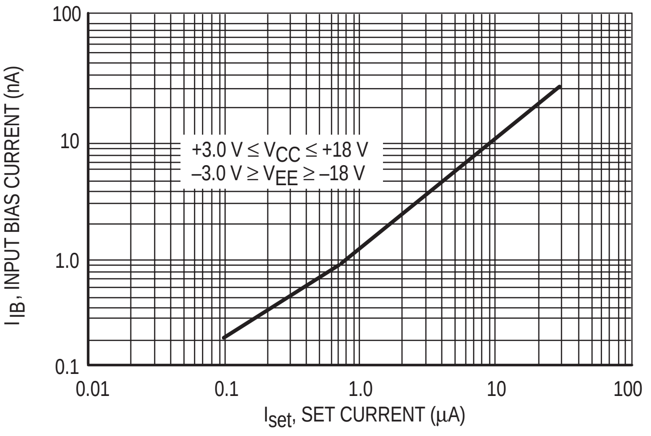


Figure 5. Input Bias Current versus Ambient Temperature

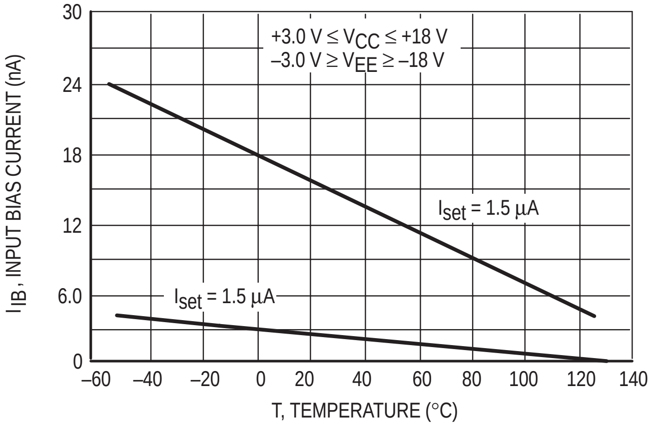


Figure 6. Gain Bandwidth Product versus Set Current

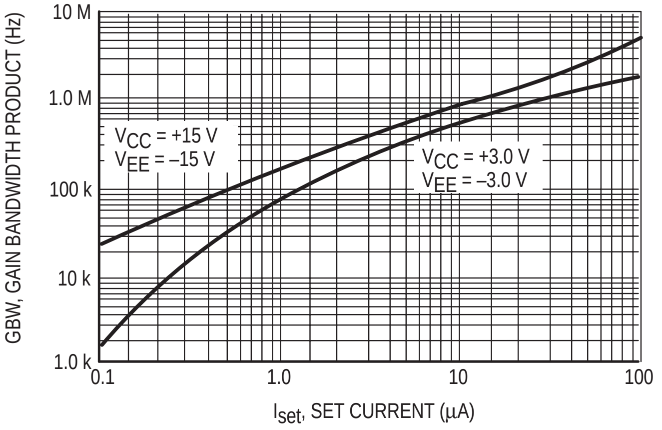


Figure 7. Output Voltage Swing versus Load Resistance

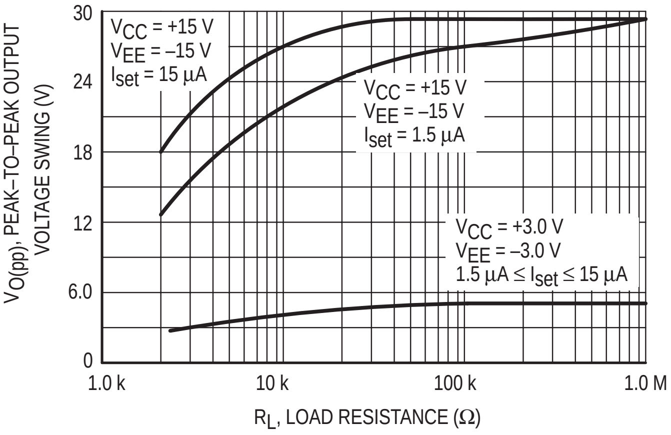


Figure 8. Supply Current versus Ambient Temperature

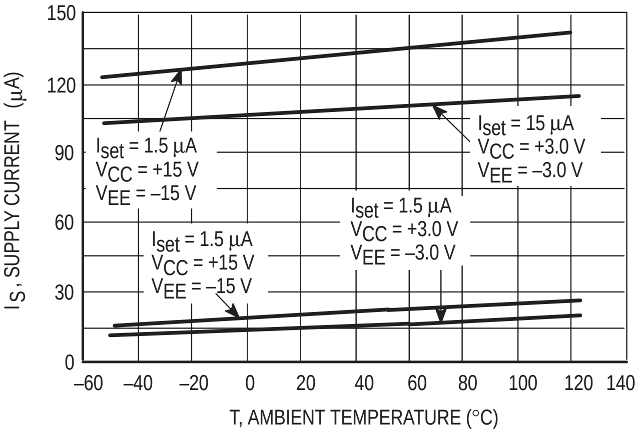


Figure 9. Output Voltage Swing versus Supply Voltage

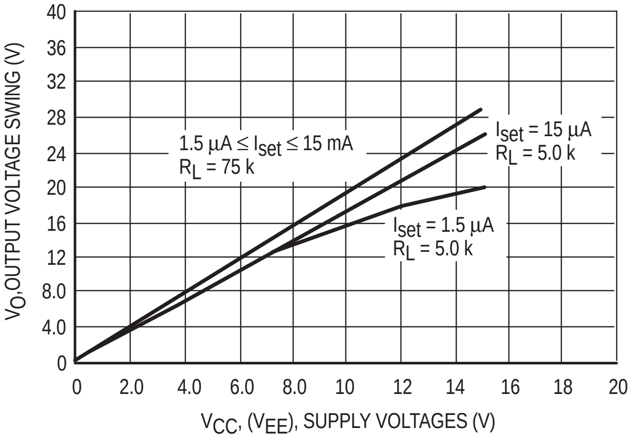


Figure 10. Slew Rate versus Set Current

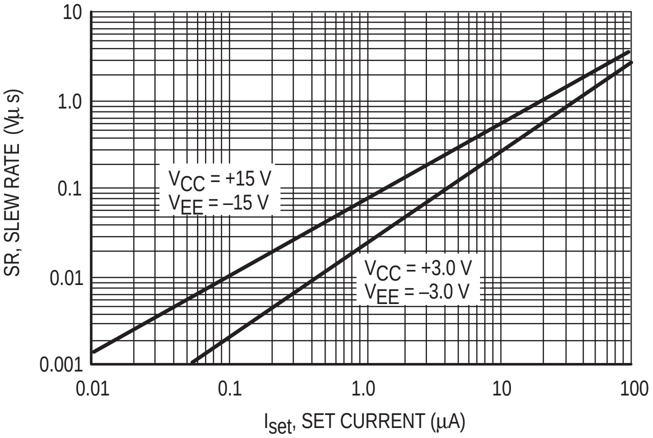


Figure 11. Input Noise Voltage versus Set Current

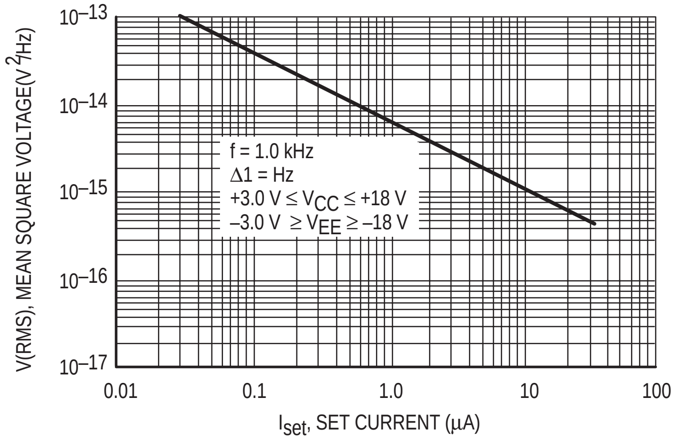


Figure 12. Optimum Source Resistance for Minimum Noise versus Set Current

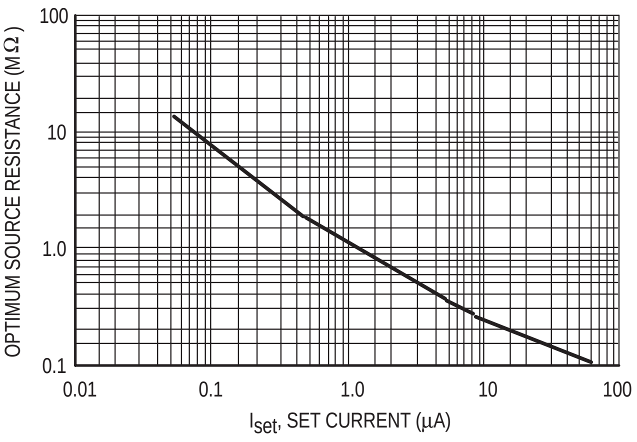
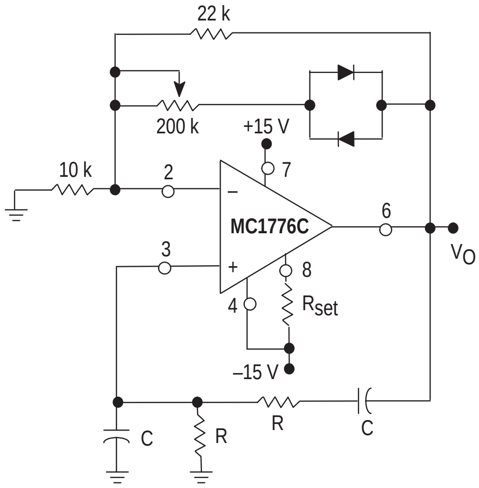


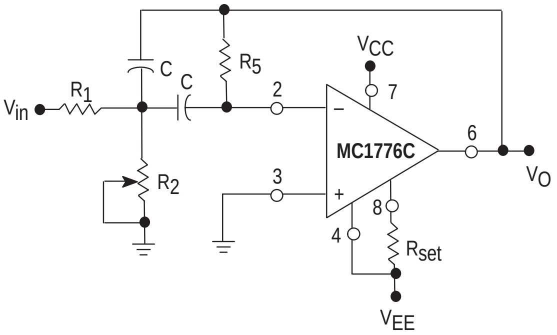
Figure 13. Wien Bridge Oscillator



$$f_0 = \frac{1}{2\pi\ RC} \quad \text{(for } f_0 = 1.0\text{ kHz)}$$

R= 16 kΩ
C = 0.01 µF

Figure 14. Multiple Feedback Bandpass Filter



For a given:
fo = center frequency
A (fo) = Gain at center frequency
Q = quality factor

Choose a value for C, then

$$R_5 = \frac{Q}{\pi f_0 C}$$

$$R_1 = \frac{R5}{2A\ (f_0)}$$

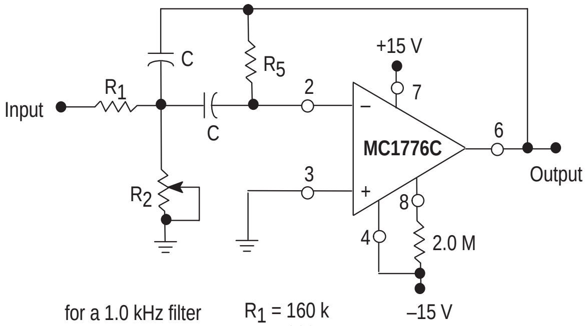
$$R_2 = \frac{R1,R5}{4Q^2\ R1–R5}$$

To obtain less than 10% error from the operational amplifier:

$$\frac{Q_O\ f_0}{GBW} \leq 0.1$$

where f_0 and GBW are expressed in Hz. GBW is available from Figure 6 as a function of Set Current, I_{set}.

Figure 15. Multiple Feedback Bandpass Filter (1.0 kHz)



for a 1.0 kHz filter
with Q = 10
and A (f_0) = 1

R_1 = 160 k
R_2 = 820
R_5 = 300 k
C = 0.01 µF

Figure 16. Gated Amplifier

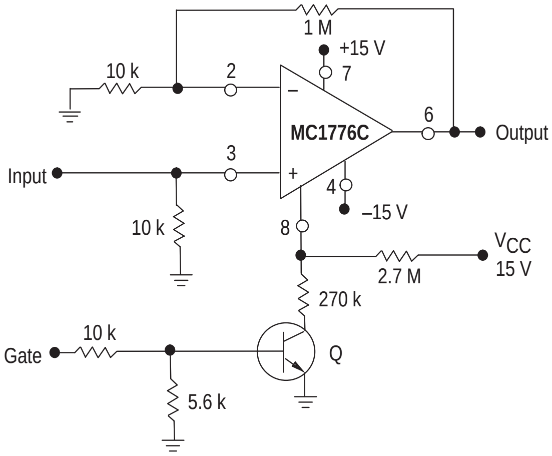
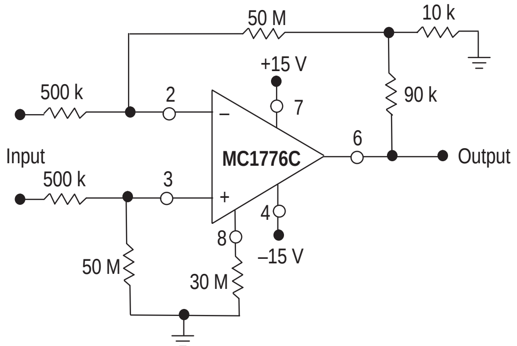


Figure 17. High Input Impedance Amplifier



MC3301, LM2900, LM3900

Quad Single Supply Operational Amplifiers

These internally compensated Norton operational amplifiers are designed specifically for single positive power supply applications found in industrial control systems and automotive electronics. Each device contains four independent amplifiers – making it ideal for applications such as active filters, multi–channel amplifiers, tachometers, oscillators and other similar usage.

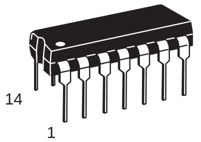
- Single Supply Operation
- Internally Compensated
- Wide Unity Gain Bandwidth: 4.0 MHz Typical
- Low Input Bias Current: 50 nA Typical
- High Open Loop Gain: 1000 V/V Minimum
- Large Output Voltage Swing: (V_{CC} – 1) V_{pp}

MAXIMUM RATINGS

Rating	Symbol	LM2900/ LM3900	MC3301	Unit
Supply Voltage	V_{CC}	+32	+28	V
Input Current (I_{in+} or $I_{in–}$)	I_{in}	5.0		mA
Output Current	I_O	50		mA
Power Dissipation (T_A = +25°C) Derate above T_A = +25°C	P_D $1/R_{\theta JA}$	625 5.0		mW mW/°C
Ambient Temperature Range LM2900 LM3900	T_A	 –40 to +85 0 to +70	 –40 to +85	°C
Storage Temperature Range	T_{stg}	–65 to +150		°C

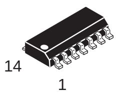
QUAD OPERATIONAL AMPLIFIERS

SEMICONDUCTOR TECHNICAL DATA

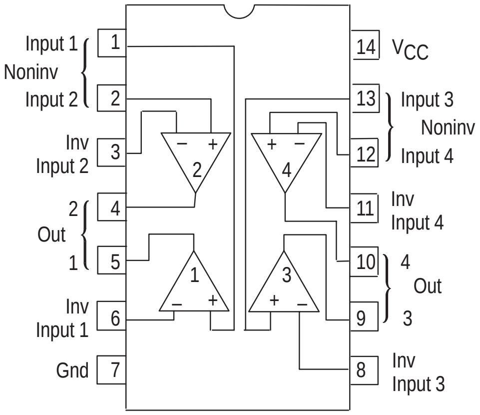


N, P SUFFIX
PLASTIC PACKAGE
CASE 646

D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO–14)



PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
LM3900D	T_A = 0° to +70°C	SO–14
LM3900N		Plastic DIP
LM2900N MC3301P	T_A = – 40° to +85°C	

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 Vdc, R_L = 5.0 kΩ. T_A = +25°C [each amplifier], unless otherwise noted.)

Characteristic	Symbol	LM2900			LM3900			MC3301			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Open Loop Voltage Gain	A_{VOL}										V/mV
f = 100 Hz, R_L = 5.0 k		1.2	2.0	–	1.2	2.0	–	1.2	2.0	–	
$T_A = T_{low}$ to T_{high} (Notes 1, 2)		–	–	–	–	–	–	–	–	–	
Input Resistance (Inverting Input)	r_i	–	1.0	–	–	1.0	–	–	1.0	–	MΩ
Output Resistance	r_o	–	8.0	–	–	8.0	–	–	8.0	–	kΩ
Input Bias Current (Inverting Input)	I_{IB}	–	50	200	–	50	200	–	50	300	nA
$T_A = T_{low}$ to T_{high} (Note 1)		–	–	–	–	–	–	–	–	–	
Slew Rate (C_L = 100 pF, R_L = 2.0 k)	SR										V/µs
Positive Output Swing		–	0.5	–	–	0.5	–	–	0.5	–	
Negative Output Swing		–	20	–	–	20	–	–	20	–	
Unity Gain Bandwidth	BW	–	4.0	–	–	4.0	–	–	4.0	–	MHz
Output Voltage Swing (Note 7)											V
V_{CC} = +15 V, R_L = 2.0 k											
V_{out} High ($I_{in}^{-} = 0$, $I_{in}+ = 0$)	V_{OH}	13.5	14.2	–	13.5	14.2	–	13.5	14.2	–	
V_{out} Low ($I_{in}^{-} = 10\ \mu A$, $I_{in}+ = 0$)	V_{OL}	–	0.03	0.2	–	0.03	0.2	–	0.03	0.2	
V_{CC} = Maximum Rating, $R_L = \infty$											
V_{out} High ($I_{in}^{-} = 0$, $I_{in}+ = 0$)	V_{OH}	–	29.5	–	–	29.5	–	–	25.5	–	
Output Current											mA
Source	I_{Source}	6.0	10	–	6.0	10	–	5.0	10	5.0	
Sink (Note 3)	I_{Sink}	0.5	0.87	–	0.5	0.87	–	0.5	0.87	0.5	
Low Level Output Current	I_{OL}	–	5.0	–	–	5.0	–	–	5.0	–	
$I_{in}^{-} = 5.0\ \mu A$, $V_{OL} = 1.0$ V											
Supply Current (All Four Amplifiers)											mA
Noninverting Inputs Open	I_{DO}	–	6.9	10	–	6.9	10	–	6.9	10	
Noninverting Inputs Grounded	I_{DG}	–	7.8	14	–	7.8	14	–	7.8	14	
Power Supply Rejection (f = 100 Hz)	PSR	–	55	–	–	55	–	–	55	–	dB
Mirror Gain ($T_A = T_{low}$ to T_{high}; Notes 1, 4)	A_i										µA
$I_{in}+ = 20\ \mu A$		0.90	1.0	1.1	0.90	1.0	1.1	0.90	1.0	1.1	
$I_{in}+ = 200\ \mu A$		0.90	1.0	1.1	0.90	1.0	1.1	0.90	1.0	1.1	
Δ Mirror Gain ($T_A = T_{low}$ to T_{high}; Notes 1, 4)	ΔA_i	–	2.0	5.0	–	2.0	5.0	–	2.0	5.0	%
$20\ \mu A \le I_{in}+ \le 200\ \mu A$											
Mirror Current ($T_A = T_{low}$ to T_{high}; Notes 1, 5)		–	10	500	–	10	500	–	10	500	µA
Negative Input Current (Note 6)		–	1.0	–	–	1.0	–	–	1.0	–	mA

NOTES: 1. T_{low} = –40°C for LM2900, MC3301 T_{high} = +85°C for LM2900, MC3301
= 0°C for LM3900 = +70°C for LM3900

2. Open loop voltage gain is defined as voltage gain from the inverting input to the output.
3. Sink current is specified for analog operation. When the device is used as a comparator (non–analog operation) where the inverting input is overdriven, the sink current (low level output current) capability is typically 5.0 mA.
4. This specification indicates the current gain of the current mirror which is used as the noninverting input.
5. Input V_{BE} match between the noninverting and inverting inputs occurs for a mirror current (noninverting input current) of approximately 10 µA.
6. Clamp transistors are included to prevent the input voltages from swinging below ground more than approximately –0.3 V. The negative input currents that may result from large signal overdrive with capacitive input coupling must be limited externally to values of approximately 1.0 mA. If more than one of the input terminals are simultaneously driven negative, maximum currents are reduced. Common mode biasing can be used to prevent negative input voltages.
7. When used as a noninverting amplifier, the minimum output voltage is the V_{BE} of the inverting input transistor.

Figure 1. Open Loop Voltage Gain versus Frequency

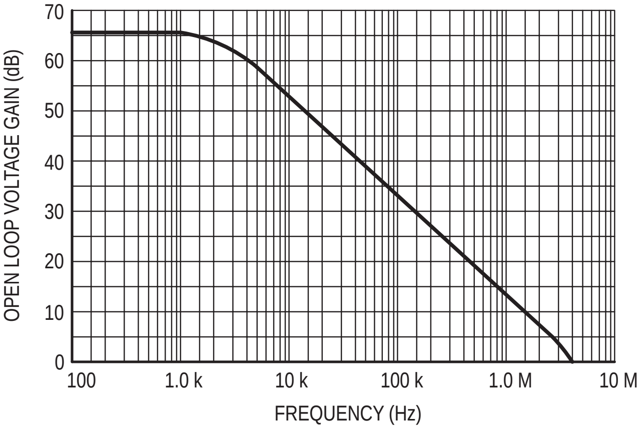


Figure 2. Open Loop Voltage Gain versus Supply Voltage

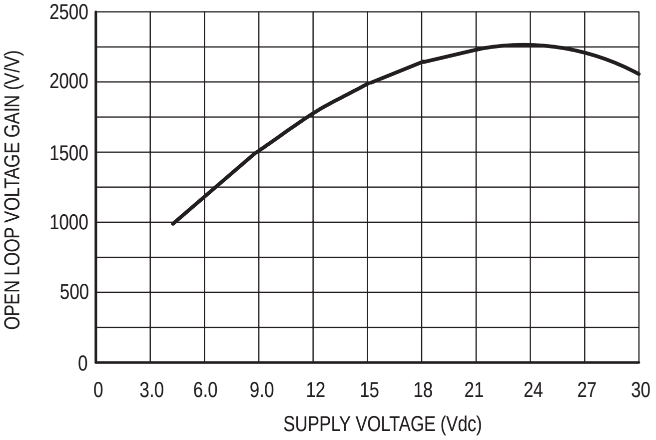


Figure 3. Output Resistance versus Frequency

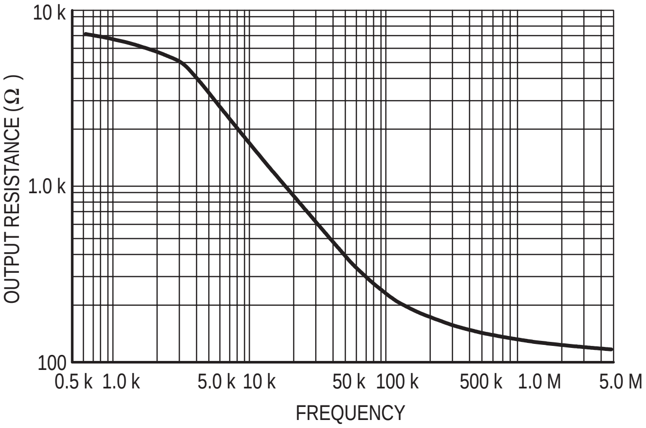


Figure 4. Supply Current versus Supply Voltage

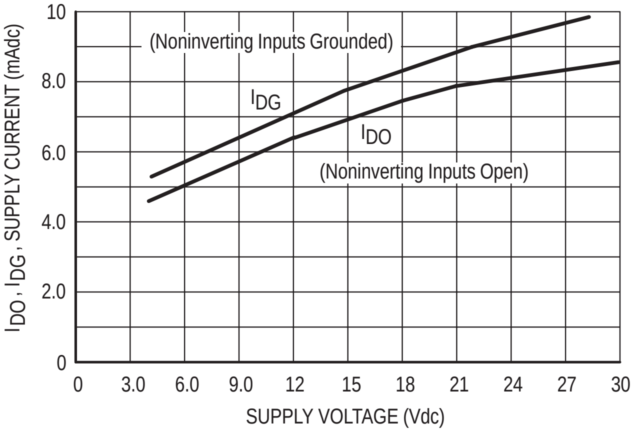


Figure 5. Analog Source Current versus Supply Voltage

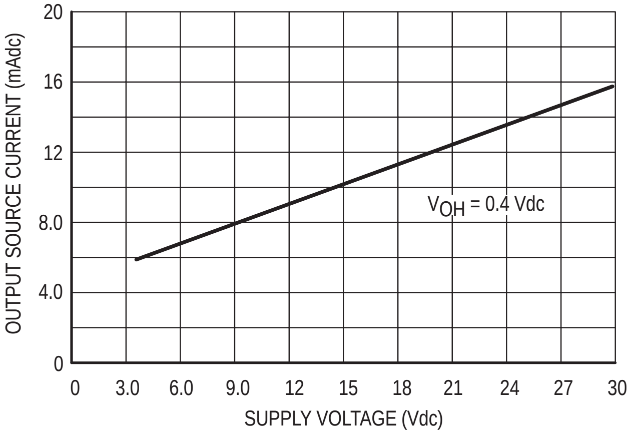
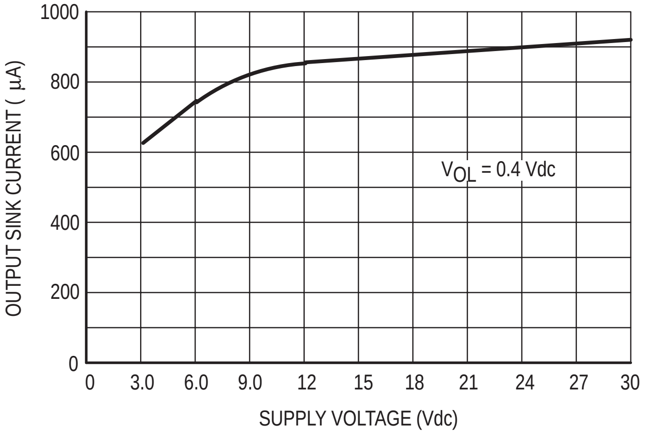


Figure 6. Analog Sink Current versus Supply Voltage

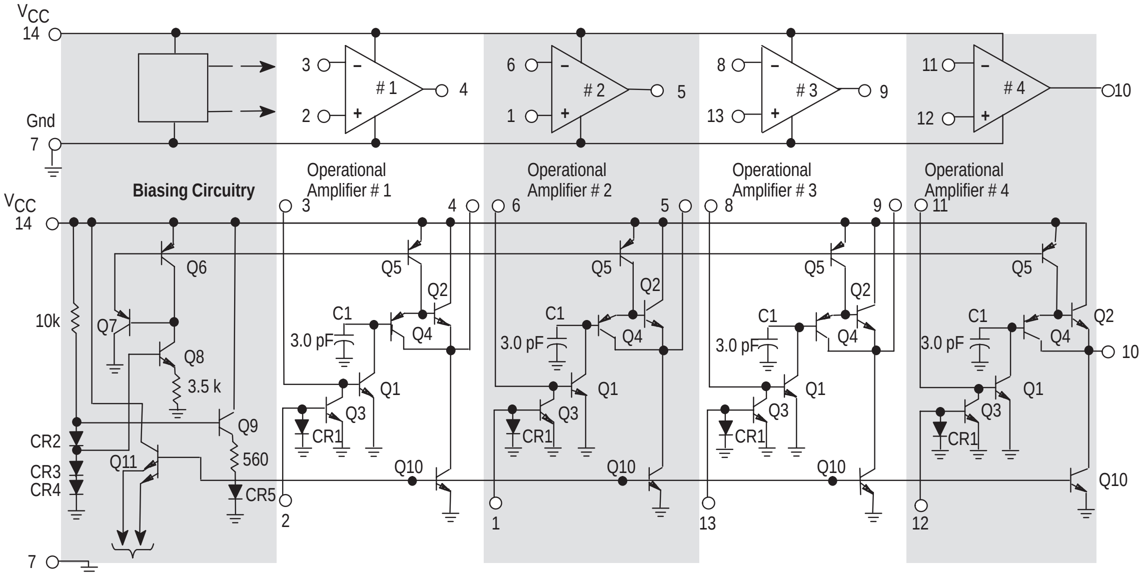


OPERATION AND APPLICATIONS

Basic Amplifier

The basic amplifier is the common emitter stage shown in Figures 7 and 8. The active load I_1 is buffered from the input transistor by a PNP transistor, Q4, and from the output by an NPN transistor, Q2. Q2 is biased Class A by the current source I_2. The magnitude of I_2 (specified I_{sink}) is a limiting factor in capacitively coupled analog operation at the output. The sink of the device can be forced to exceed the specified level by keeping the output DC voltage above ≈ 1.0 V resulting in an increase in the distortion appearing at the output. Closed loop stability is maintained by an on–the–chip 3–pF capacitor shown in Figure 10 on the following page. No external compensation is required.

Figure 7. Block Diagram



Multiple emitter (8) transistor – one emitter connected to each input.

A noninverting input obtained by adding a current mirror as shown in Figure 9. Essentially all current which enters the noninverting input, I_{in}^+, flows through the diode CR1. The voltage drop across CR1 corresponds to this input current magnitude and this same voltage is applied to a matched device, Q3. Thus Q3 is biased to conduct an emitter current equal to I_{in}^+. Since the alpha current gain of Q3 ≈ 1, its collector current is approximately equal to I_{in}^+ also. In operation this current flows through an external feedback resistor which generates the output voltage signal. For inverting applications, the noninverting input is often used to set the DC quiescent level at the output. Techniques for doing this are discussed in the “Normal Design Procedure” section.

Figure 8. A Basic Gain Stage

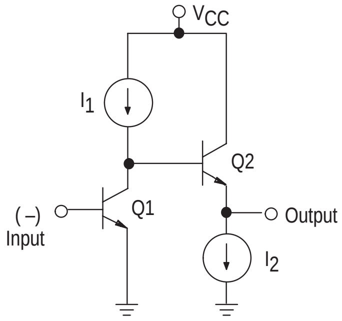
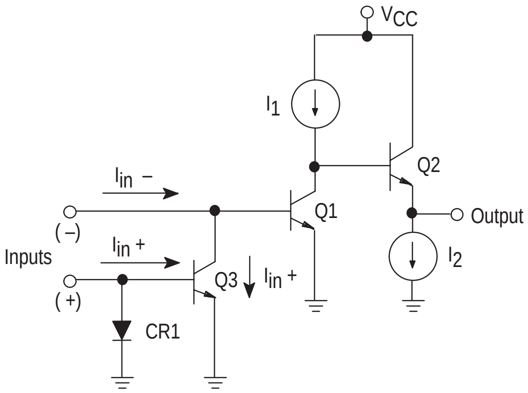


Figure 9. Obtaining A Noninverting Input



Biasing Circuitry

The circuitry common to all four amplifiers is shown in Figure 11. The purpose of this circuitry is to provide biasing voltage for the PNP and NPN current sources used in the amplifiers.

The voltage drops across diodes CR2, CR3 and CR4 are used as references. The voltage across resistor R1 is the sum of the drops across CR4 and CR3 minus the V_{BE} of Q8. The PNP current sources (Q5, etc.) are set to the magnitude V_{BE}/R1 by transistor Q6. Transistor Q7 reduces base current loading. The voltage across resistor R_2 is the sum of the voltage drops across CR2, CR3 and CR4, minus the V_{BE} drops of transistor Q9 and diode CR5; thus the current set is established by CR5 in all the NPN current sources (Q10, etc.). This technique results in current source magnitudes which are relatively independent of the supply voltage. Q11 (Figure 7) provides circuit protection from signals that are negative with respect to ground.

Figure 10. A Basic Operational Amplifier

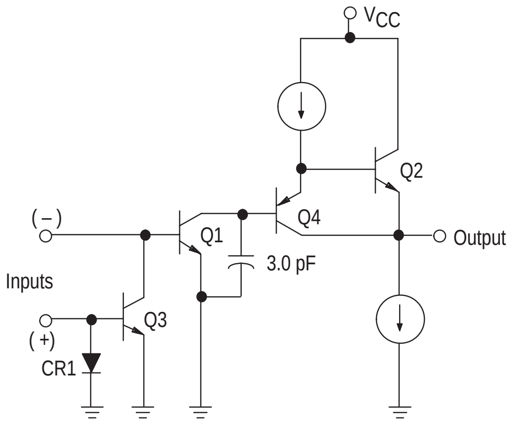
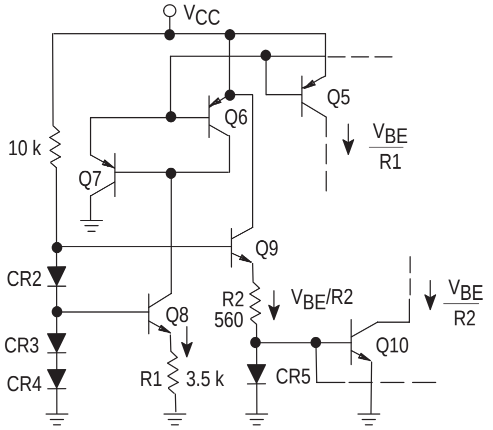


Figure 11. Biasing Circuitry



NORMAL DESIGN PROCEDURE

1. Output Q–Point Biasing
   A. A number of techniques may be devised to bias the quiescent output voltage to an acceptable level. However, in terms of loop gain considerations it is usually desirable to use the noninverting input to effect the biasing, as shown in Figures 12 and 13. The high impedance of the collector of the noninverting "current mirror" transistor helps to achieve the maximum loop gain for any particular configuration. It is desirable that the noninverting input current be in the 10 µA to 200 µA range.

   B. V_{CC} Reference Voltage (see Figures 12 and 13) The noninverting input is normally returned to the V_{CC} voltage (which should be well filtered) through a resistor (R_r) allowing the input current, (I_{in}^+) to be within the range of 10 µA to 200 µA.

   Choosing the feedback resistor (R_f) to be equal to $^1/_2$ R_r will now bias the amplifier output DC level to approximately $V_{CC}/2$. This allows the maximum dynamic range of the output voltage.

   C. Reference Voltage other than V_{CC} (see Figure 14) The biasing resistor (R_r) may be returned to a voltage(V_r) other than V_{CC}. By setting $R_f = R_r$, (still keeping I_{in} +between 10 µA and 200 µA) the output DC level will be equal to V_r. The expression for determining V_{Odc} is:

$$V_{Odc} = \frac{(A_i)(V_r)(R_f)}{R_r} + \left(1 - \frac{R_f}{R_r} A_i\right) \phi$$

   where ϕ is the V_{BE} drop of the input transistors (approximately 0.6 Vdc @ +25°C and assumed equal). A_i is the current mirror gain.

Figure 12. Inverting Amplifier

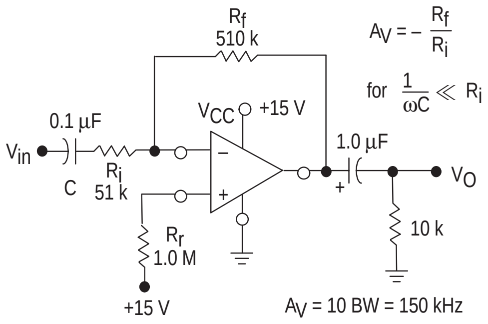
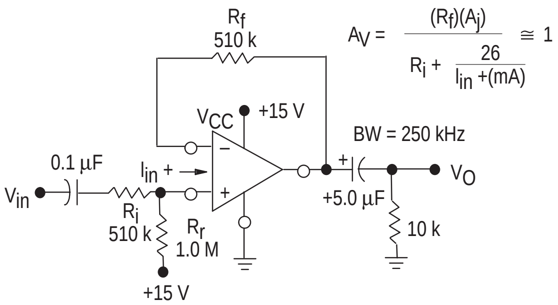


Figure 13. Noninverting Amplifier



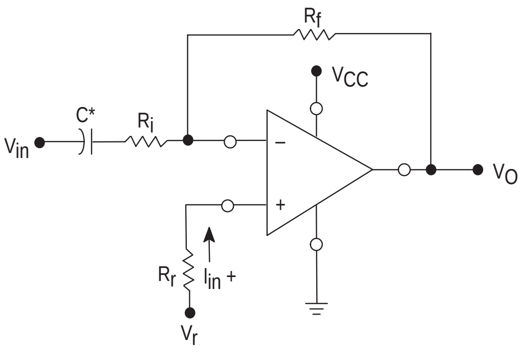
2. Gain Determination
   A. Inverting Amplifier

The amplifier is normally used in the inverting mode. The input may be capacitively coupled to avoid upsetting the DC bias and the output is normally capacitively coupled to eliminate the DC voltage across the load. Note that when the output is capacitively coupled to the load, the value of I_{sink} becomes a limitation with respect to the load driving capabilities of the device if it is direct coupled. In this configuration, the AC gain is determined by the ratio of R_f to R_i, in the same manner as for a conventional operational amplifier:

$$A_V = \frac{R_f}{R_i}$$

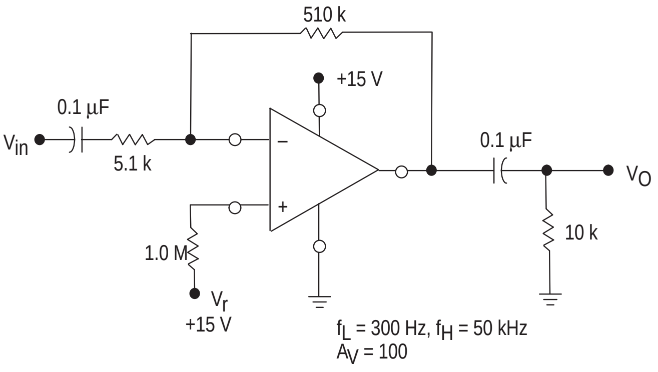
The lower corner frequency is determined by the coupling capacitors to the input and load resistors. The upper corner frequency will usually be determined by the amplifier internal compensation. The amplifier unity gain bandwidth is typically 400 kHz with 20 dB of closed loop gain or 40 kHz with 40 dB of closed loop gain. The exception to this occurs at low gains where the input resistor selected is large. The pole formed by the amplifier input capacitance, stray capacitance and the input resistor may occur before the closed loop gain intercepts the open loop response curve. The inverting input capacity is typically 3.0 pF.

Figure 14. Inverting Amplifier with Arbitrary Reference



*Select for low frequency response.

Figure 15. Inverting Amplifier with A_V = 100 and V_r = V_{CC}



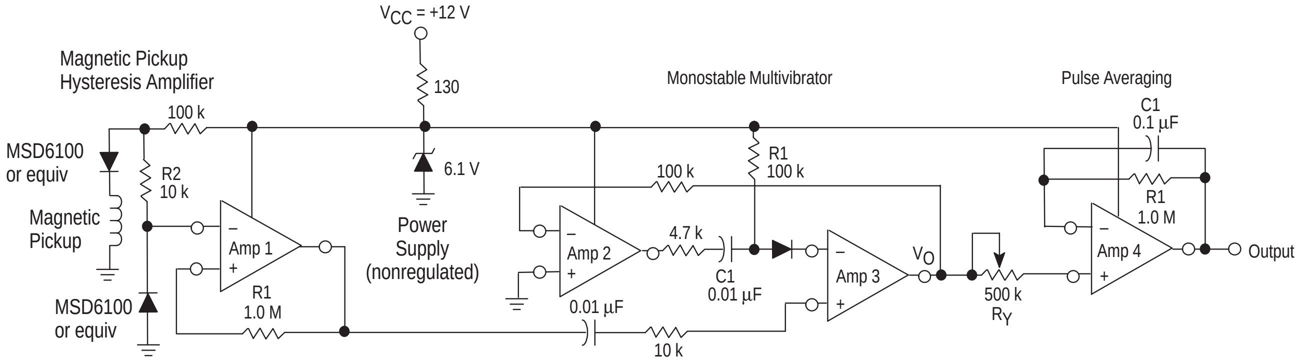
B. Noninverting Amplifier

These devices may be used in the noninverting mode (see Figure 13). The amplifier gain in this configuration is subject to the current mirror gain. In addition, the resistance of the input diode must be included in the value of the input resistor. This resistance is approximately $\frac{26}{I_{in}+}$ Ω, where I_{in}+is input current in milliamperes. The noninverting AC gain expression is given by:

$$A_V = \frac{(R_f)(A_i)}{R_i + \frac{26}{I_{in} + (mA)}}$$

The bandwidth of the noninverting configuration for a given R_f value is essentially independent of the gain chosen. For R_f = 510 kΩ the bandwidth will be in excess of 200 kHz for noninverting of 1, 10, or 100. This is a result of the loop gain remaining constant for these gains since the the input resistor is effectively isolated from the feedback loop.

Figure 16. Tachometer Circuit



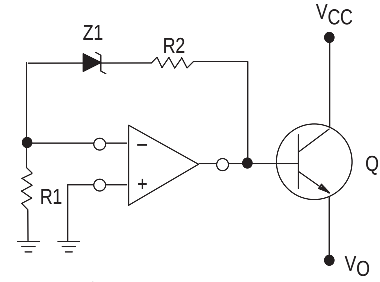
Hysteresis Voltage for Switching

$$V_H = \frac{A_i R2}{R1}(V_{CC} - 1.6)$$

Timing Interval: t ≈ 0.7 R1 C1

$$V_{pp} \cong \frac{(V_O - 0.6) \bullet A_i \bullet t}{R_Y C1}$$

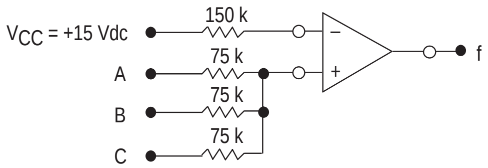
Figure 17. Voltage Regulator



$$V_O = V_{Z1} + 0.6\left(1 + \frac{R2}{R1}\right) - V_{BE\ Q1}$$

Note: For positive T_C zeners R2 and R1 can be selected to give T_C output.

Figure 18. Logic “OR” Gate



f = A + B + C

Figure 19. Logic "NAND" Gate (Large Fan–In)

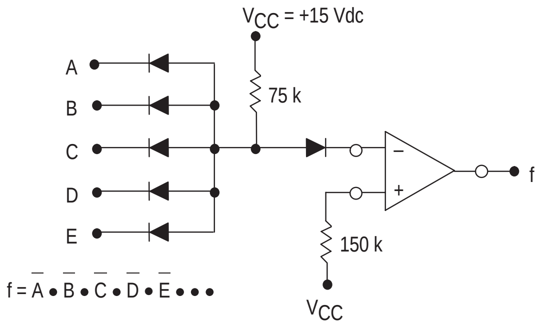


Figure 20. Logic "NOR" Gate

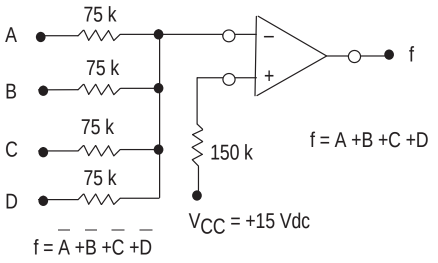


Figure 21. R–S Flip–Flop

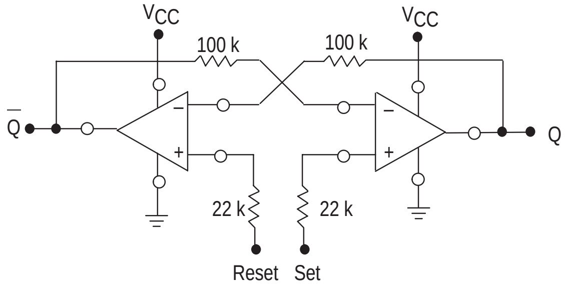


Figure 22. Astable Multivibrator

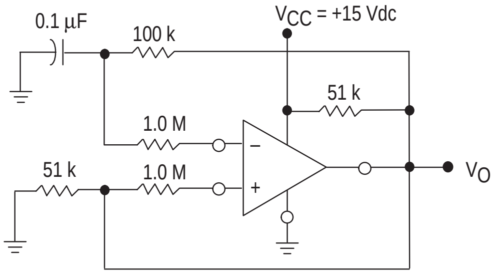


Figure 23. Positive–Edge Differentiator

Output Rise Time ≈ 0.22 ms
Input Change Time Constant ≈ 1.0 ms

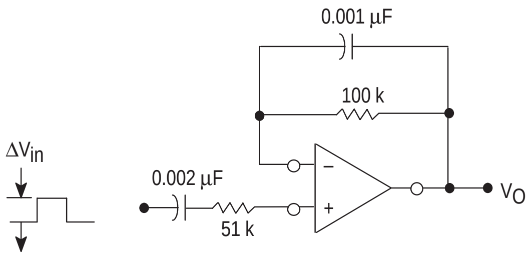
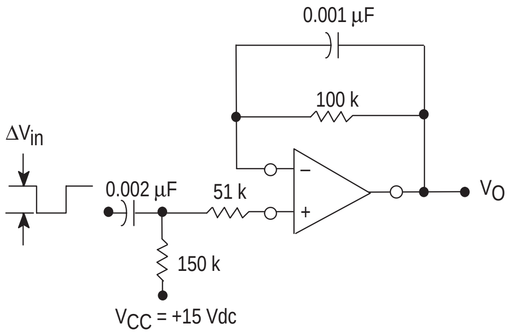
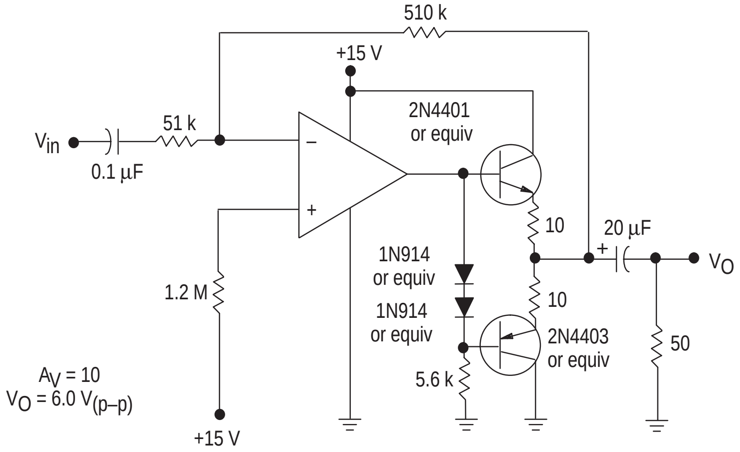


Figure 24. Negative–Edge Differentiator



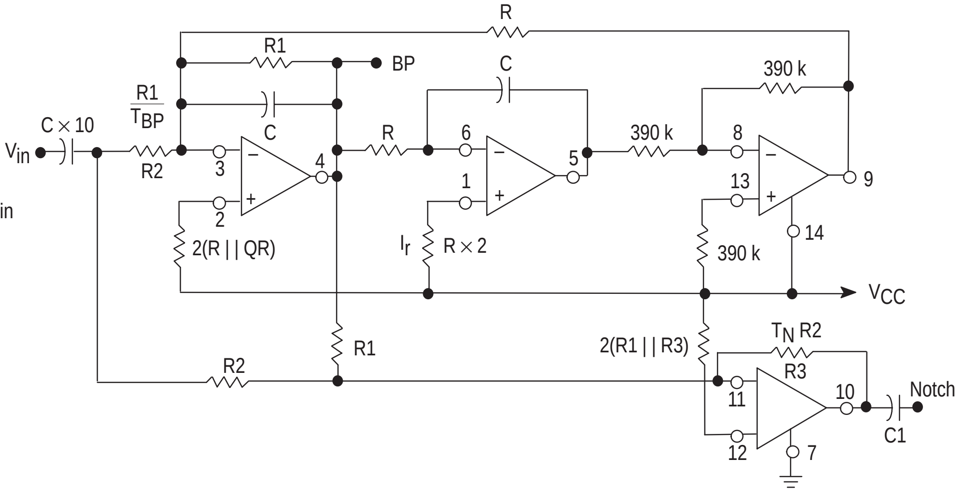
$V_{O(dc)} \approx 7.0$ Vdc
Output Rise Time ≈ 0.22 ms
Input Change Time Constant ≈ 1.0 ms

Figure 25. Amplifier and Driver for a 50 Ω Line



$A_V = 10$
$V_O = 6.0\ V_{(p–p)}$

Figure 26. Basic Bandpass and Notch Filter



T_{BP} = Center Frequency Gain
T_N = Passband Notch Gain

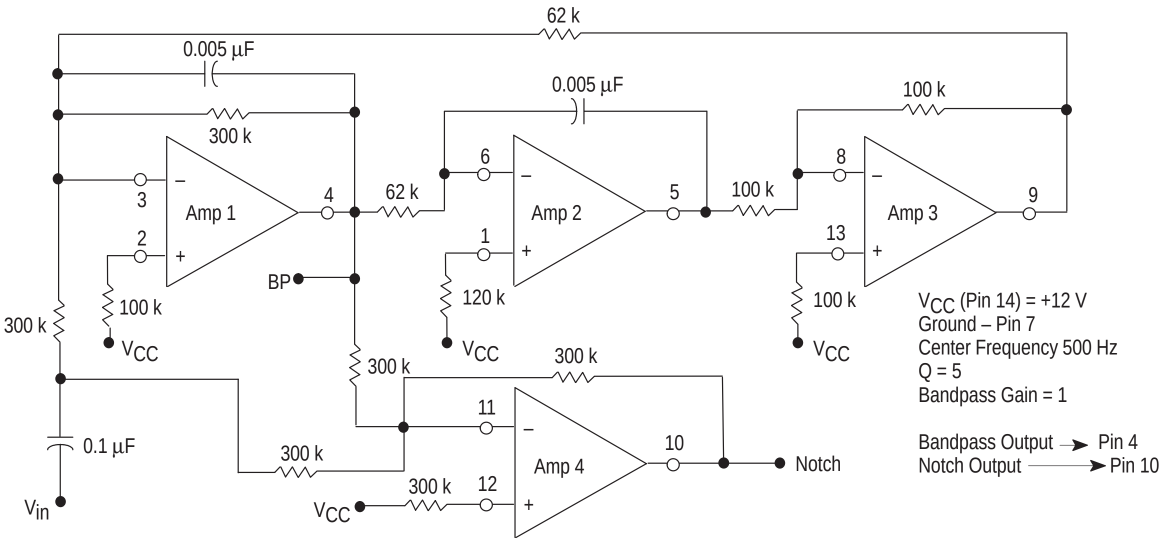
$w_0 = \frac{1}{RC}$

R1 = QR

$R2 = \frac{R1}{T_{BP}}$

$R3 = T_N\ R2$

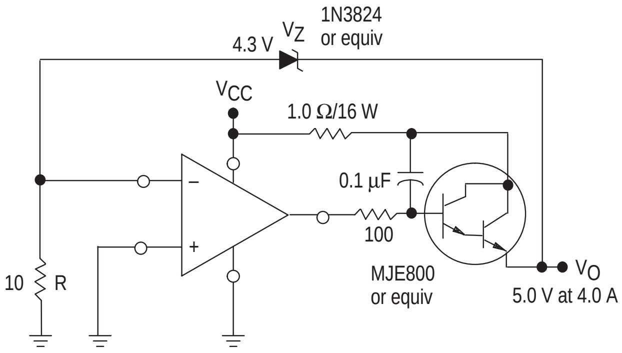
Figure 27. Bandpass and Notch Filter



V_{CC} (Pin 14) = +12 V
Ground – Pin 7
Center Frequency 500 Hz
Q = 5
Bandpass Gain = 1

Bandpass Output → Pin 4
Notch Output → Pin 10

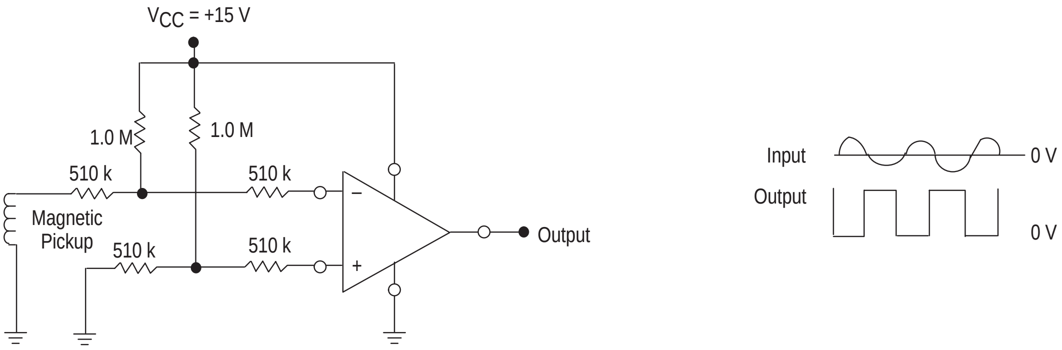
Figure 28. Voltage Regulator



$V_O = V_Z + 0.6$ Vdc

NOTES:
1. R is used to bias the zener.
2. If the zener TC is positive, and equal in magnitude to the negative TC of the input to the operational amplifier (≈2.0 mV/°C), the output is zero–TC. A 7.0 V zener will give approximately zero–TC.

Figure 29. Zero Crossing Detector



MOTOROLA

MC3403
MC3303

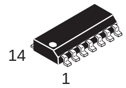
Quad Low Power Operational Amplifiers

QUAD DIFFERENTIAL INPUT OPERATIONAL AMPLIFIERS

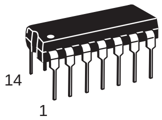
SEMICONDUCTOR
TECHNICAL DATA

The MC3403 is a low cost, quad operational amplifier with true differential inputs. The device has electrical characteristics similar to the popular MC1741C. However, the MC3403 has several distinct advantages over standard operational amplifier types in single supply applications. The quad amplifier can operate at supply voltages as low as 3.0 V or as high as 36 V with quiescent currents about one third of those associated with the MC1741C (on a per amplifier basis). The common mode input range includes the negative supply, thereby eliminating the necessity for external biasing components in many applications. The output voltage range also includes the negative power supply voltage.

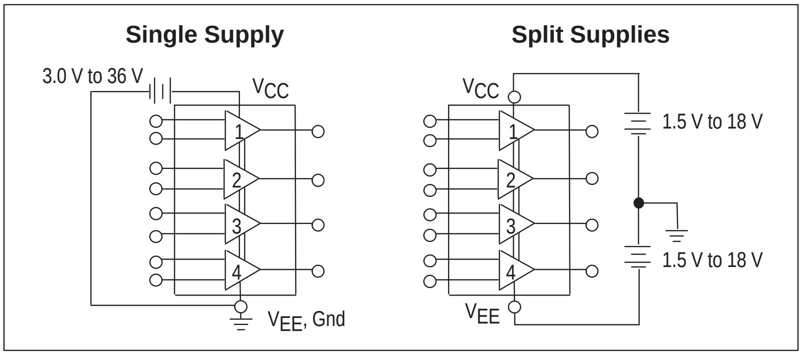
- Short Circuit Protected Outputs
- Class AB Output Stage for Minimal Crossover Distortion
- True Differential Input Stage
- Single Supply Operation: 3.0 V to 36 V
- Split Supply Operation: ±1.5 V to ±18 V
- Low Input Bias Currents: 500 nA Max
- Four Amplifiers Per Package
- Internally Compensated
- Similar Performance to Popular MC1741C
- Industry Standard Pinouts
- ESD Diodes Added for Increased Ruggedness



D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO–14)

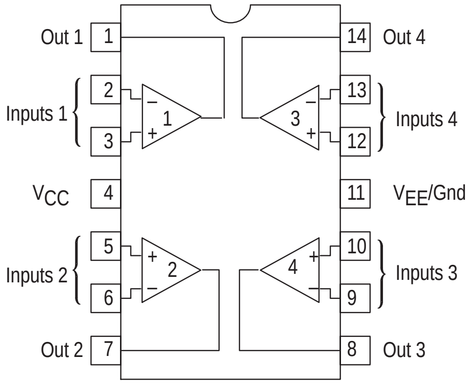


P SUFFIX
PLASTIC PACKAGE
CASE 646



Single Supply **Split Supplies**

PIN CONNECTIONS



(Top View)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltages			Vdc
Single Supply	V_{CC}	36	
Split Supplies	V_{CC}, V_{EE}	±18	
Input Differential Voltage Range (Note 1)	V_{IDR}	±36	Vdc
Input Common Mode Voltage Range (Notes 1, 2)	V_{ICR}	±18	Vdc
Storage Temperature Range	T_{stg}	–55 to +125	°C
Operating Ambient Temperature Range	T_A		°C
MC3303		–40 to +85	
MC3403		0 to +70	
Junction Temperature	T_J	150	°C

NOTES: 1. Split power supplies.
2. For supply voltages less than ±18 V, the absolute maximum input voltage is equal to the supply voltage.

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC3303D MC3303P	T_A = – 40° to +85°C	SO–14 Plastic DIP
MC3403D MC3403P	T_A = 0° to +70°C	SO–14 Plastic DIP

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = –15 V for MC3403; V_{CC} = +14 V, V_{EE} = Gnd for MC3303 T_A = 25°C, unless otherwise noted.)

Characteristic	Symbol	MC3403			MC3303			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage T_A = T_{high} to T_{low} (Note 1)	V_{IO}	– –	2.0 –	10 12	– –	2.0 –	8.0 10	mV
Input Offset Current T_A = T_{high} to T_{low}	I_{IO}	– –	30 –	50 200	– –	30 –	75 250	nA
Large Signal Open Loop Voltage Gain V_O = ±10 V, R_L = 2.0 kΩ T_A = T_{high} to T_{low}	A_{VOL}	 20 15	 200 –	 – –	 20 15	 200 –	 – –	V/mV
Input Bias Current T_A = T_{high} to T_{low}	I_{IB}	– –	–200 –	–500 –800	– –	–200 –	–500 –1000	nA
Output Impedance f = 20 Hz	z_o	–	75	–	–	75	–	Ω
Input Impedance f = 20 Hz	z_i	0.3	1.0	–	0.3	1.0	–	MΩ
Output Voltage Range R_L = 10 kΩ R_L = 2.0 kΩ R_L = 2.0 kΩ, T_A = T_{high} to T_{low}	V_O	 ±12 ±10 ±10	 ±13.5 ±13 –	 – – –	 12 10 10	 12.5 12 –	 – – –	V
Input Common Mode Voltage Range	V_{ICR}	+13 V $-V_{EE}$	+13 V $-V_{EE}$	–	+12 V $-V_{EE}$	+12.5 V $-V_{EE}$	–	V
Common Mode Rejection $R_S \leq 10$ k Ω	CMR	70	90	–	70	90	–	dB
Power Supply Current (V_O = 0) $R_L = \infty$	I_{CC}, I_{EE}	–	2.8	7.0	–	2.8	7.0	mA
Individual Output Short–Circuit Current (Note 2)	I_{SC}	±10	±20	±45	±10	±30	±45	mA
Positive Power Supply Rejection Ratio	PSRR+	–	30	150	–	30	150	µV/V
Negative Power Supply Rejection Ratio	PSRR–	–	30	150	–	30	150	µV/V
Average Temperature Coefficient of Input Offset Current T_A = T_{high} to T_{low}	$\Delta I_{IO}/\Delta T$	–	50	–	–	50	–	pA/°C
Average Temperature Coefficient of Input Offset Voltage T_A = T_{high} to T_{low}	$\Delta V_{IO}/\Delta T$	–	10	–	–	10	–	µV/°C
Power Bandwidth A_V = 1, R_L = 10 kΩ, V_O = 20 V(p–p), THD = 5%	BWp	–	9.0	–	–	9.0	–	kHz
Small–Signal Bandwidth A_V = 1, R_L = 10 kΩ, V_O = 50 mV	BW	–	1.0	–	–	1.0	–	MHz
Slew Rate A_V = 1, V_i = –10 V to +10 V	SR	–	0.6	–	–	0.6	–	V/µs
Rise Time A_V = 1, R_L = 10 kΩ, V_O = 50 mV	t_{TLH}	–	0.35	–	–	0.35	–	µs
Fall Time A_V = 1, R_L = 10 kΩ, V_O = 50 mV	t_{TLH}	–	0.35	–	–	0.35	–	µs
Overshoot A_V = 1, R_L = 10 kΩ, V_O = 50 mV	os	–	20	–	–	20	–	%
Phase Margin A_V = 1, R_L = 2.0 kΩ, V_O = 200 pF	φm	–	60	–	–	60	–	Degrees
Crossover Distortion (V_{in} = 30 mVpp,V_{out}= 2.0 Vpp, f = 10 kHz)	–	–	1.0	–	–	1.0	–	%

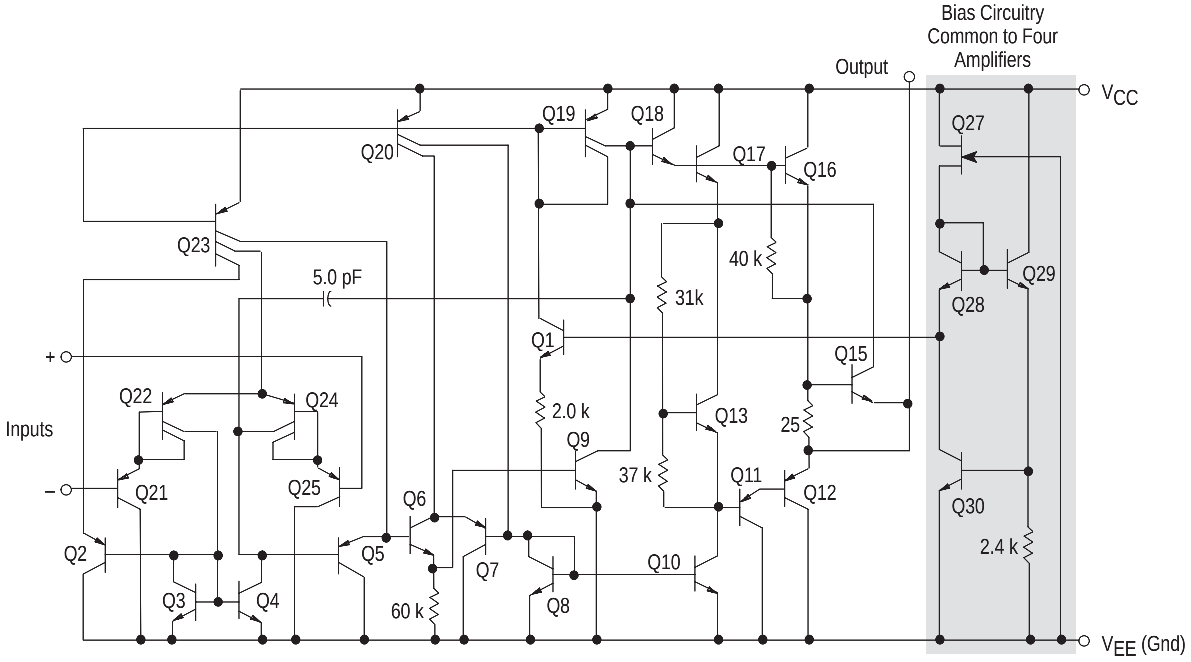
NOTES: 1. T_{high} = +70°C for MC3403, +85°C for MC3303
T_{low} = 0°C for MC3403, –40°C for MC3303
2. Not to exceed maximum package power dissipation.

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, V_{EE} = Gnd, T_A = 25°C, unless otherwise noted.)

Characteristic	Symbol	MC3403			MC3303			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V_{IO}	–	2.0	10	–	–	10	mV
Input Offset Current	I_{IO}	–	30	50	–	–	75	nA
Input Bias Current	I_{IB}	–	–200	–500	–	–	–500	nA
Large Signal Open Loop Voltage Gain R_L = 2.0 kΩ	A_{VOL}	10	200	–	10	200	–	V/mV
Power Supply Rejection Ratio	PSRR	–	–	150	–	–	150	µV/V
Output Voltage Range (Note 3) R_L = 10 kΩ, V_{CC} = 5.0 V R_L = 10 kΩ, 5.0 ≤ V_{CC} ≤ 30 V	V_{OR}	 3.3 V_{CC}–2.0	 3.5 V_{CC}–1.7	 – –	 3.3 V_{CC}–2.0	 3.5 V_{CC}–1.7	 – –	Vpp
Power Supply Current	I_{CC}	–	2.5	7.0	–	2.5	7.0	mA
Channel Separation f = 1.0 kHz to 20 kHz (Input Referenced)	CS	–	–120	–	–	–120	–	dB

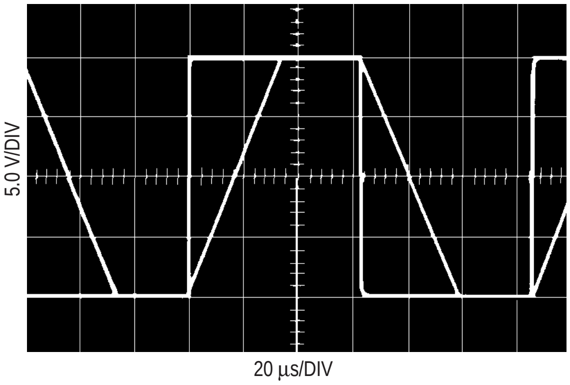
NOTES: 3. Output will swing to ground with a 10 kΩ pull down resistor.

Representative Schematic Diagram
(1/4 of Circuit Shown)



CIRCUIT DESCRIPTION

Inverter Pulse Response



The MC3403/3303 is made using four internally compensated, two–stage operational amplifiers. The first stage of each consists of differential input device Q24 and Q22 with input buffer transistors Q25 and Q21 and the differential to single ended converter Q3 and Q4. The first stage performs not only the first stage gain function but also performs the level shifting and transconductance reduction functions. By reducing the transconductance, a smaller compensation capacitor (only 5.0 pF) can be employed, thus saving chip area. The transconductance reduction is accomplished by splitting the collectors of Q24 and Q22. Another feature of this input stage is that the input common mode range can include the negative supply or ground, in single supply operation, without saturating either the input devices or the differential to single–ended converter. The second stage consists of a standard current source load amplifier stage.

The output stage is unique because it allows the output to swing to ground in single supply operation and yet does not exhibit any crossover distortion in split supply operation. This is possible because Class AB operation is utilized.

Each amplifier is biased from an internal voltage regulator which has a low temperature coefficient, thus giving each amplifier good temperature characteristics as well as excellent power supply rejection.

Figure 1. Sine Wave Response

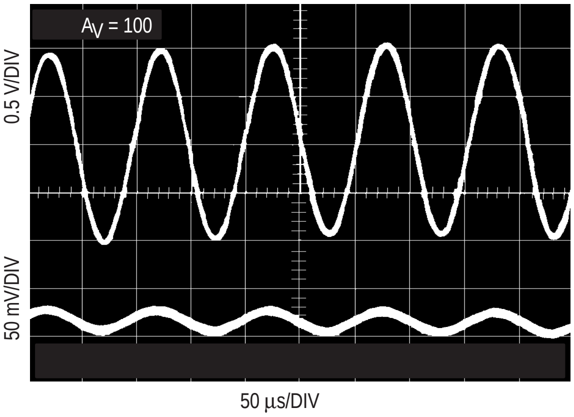


Figure 2. Open Loop Frequency Response

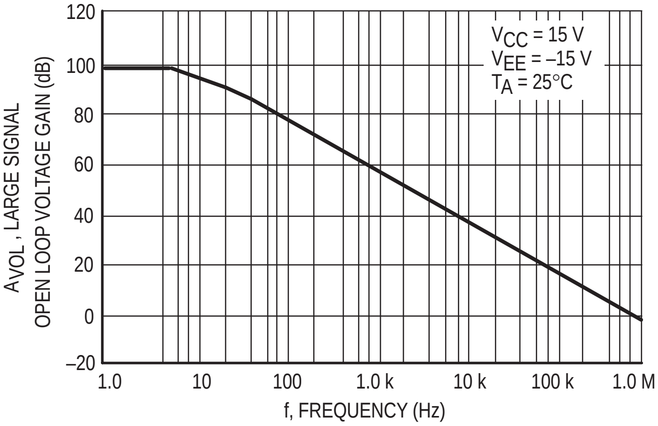


Figure 3. Power Bandwidth

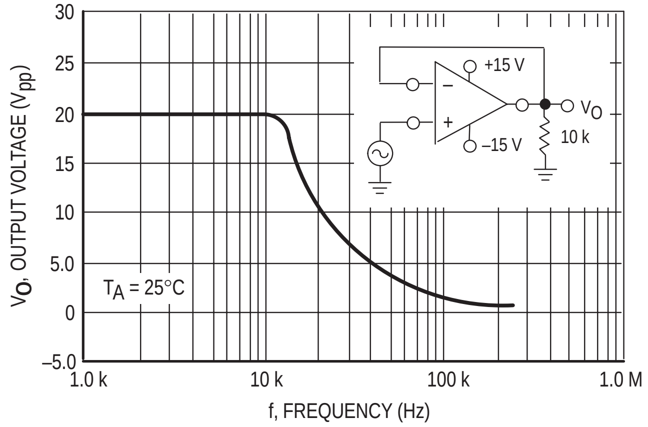


Figure 4. Output Swing versus Supply Voltage

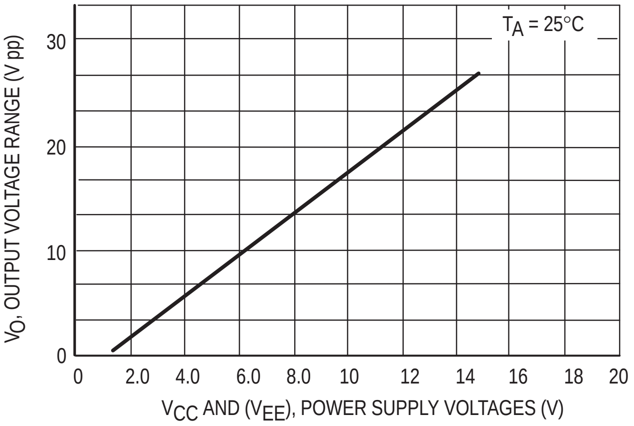


Figure 5. Input Bias Current versus Temperature

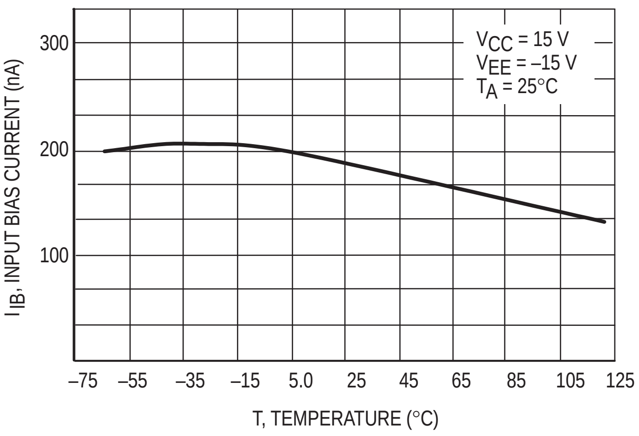


Figure 6. Input Bias Current versus Supply Voltage

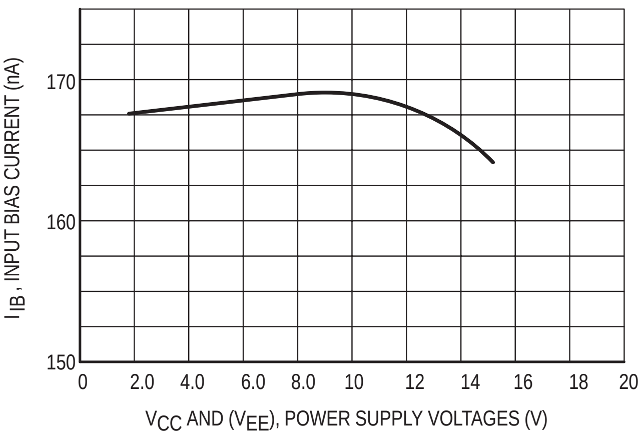


Figure 7. Voltage Reference

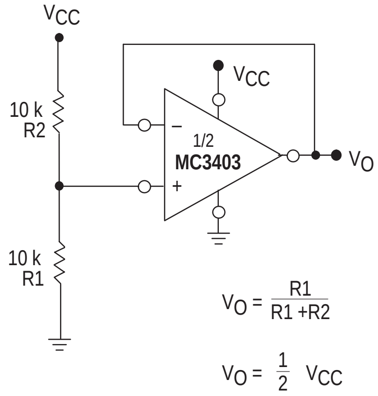


Figure 8. Wien Bridge Oscillator

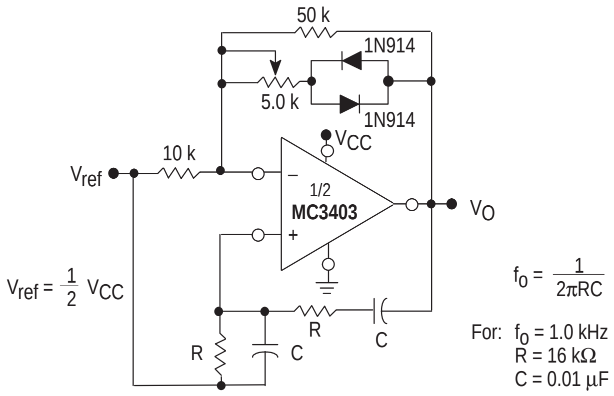
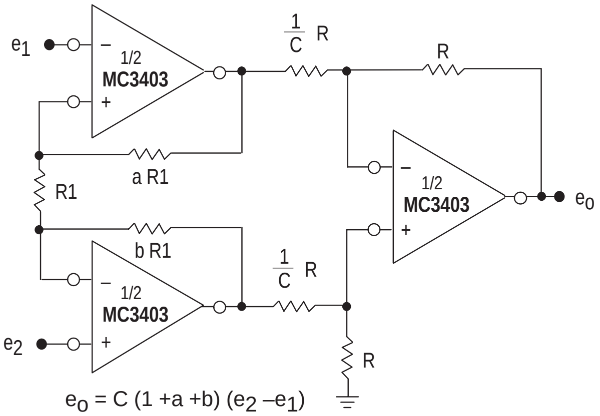
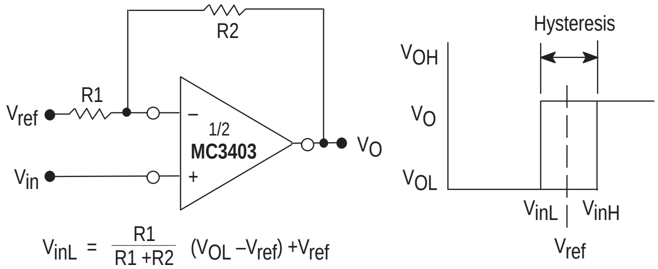


Figure 9. High Impedance Differential Amplifier



$e_o = C\,(1 + a + b)\,(e_2 - e_1)$

Figure 10. Comparator with Hysteresis

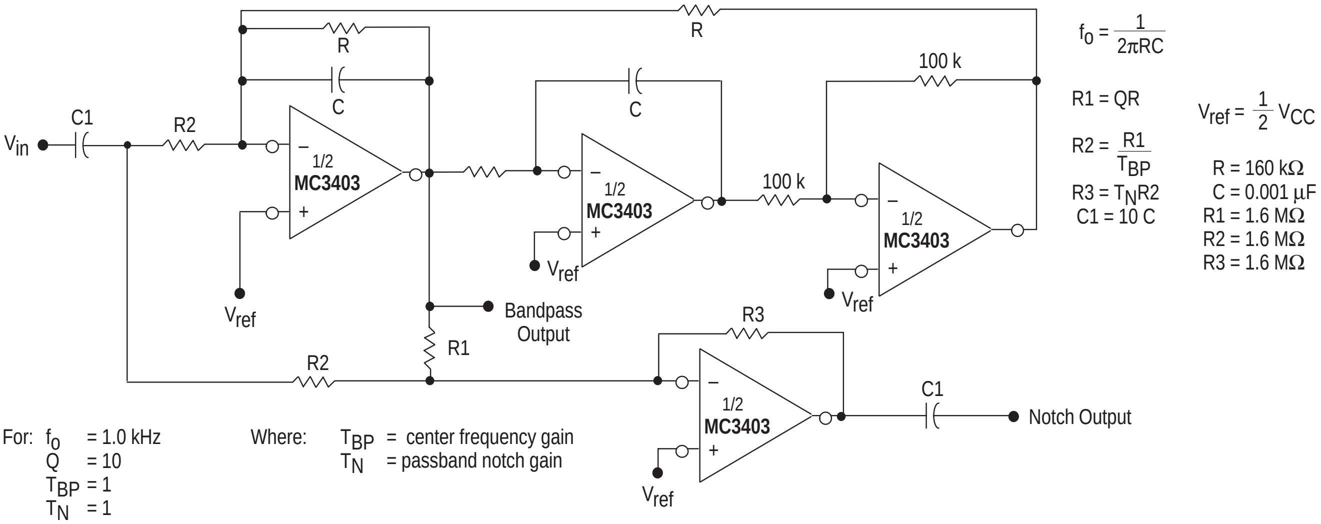


$V_{inL} = \frac{R1}{R1 + R2}(V_{OL} - V_{ref}) + V_{ref}$

$V_{inH} = \frac{R1}{R1 + R2}(V_{OH} - V_{ref}) + V_{ref}$

$V_h = \frac{R1}{R1 + R2}(V_{OH} - V_{OL})$

Figure 11. Bi–Quad Filter



$f_o = \frac{1}{2\pi RC}$

$R1 = QR$

$R2 = \frac{R1}{T_{BP}}$

$R3 = T_N R2$

$C1 = 10\,C$

$V_{ref} = \frac{1}{2} V_{CC}$

$R = 160\ k\Omega$

$C = 0.001\ \mu F$

$R1 = 1.6\ M\Omega$

$R2 = 1.6\ M\Omega$

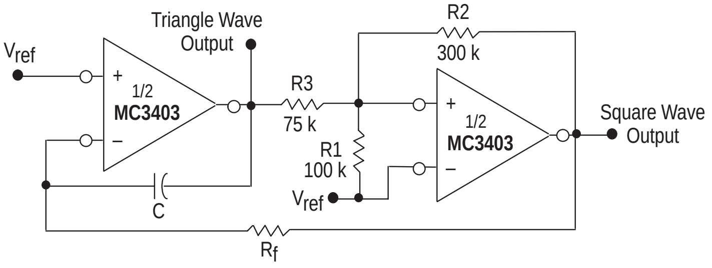
$R3 = 1.6\ M\Omega$

For: $f_o = 1.0$ kHz
$Q = 10$
$T_{BP} = 1$
$T_N = 1$

Where: T_{BP} = center frequency gain
T_N = passband notch gain

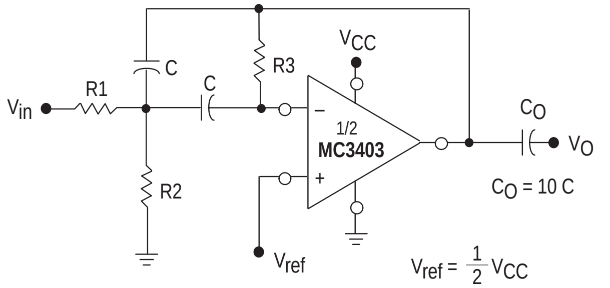
Figure 12. Function Generator

$V_{ref} = \frac{1}{2} V_{CC}$



$f = \frac{R1 + R_C}{4\,CR_f\,R1}$ if $R3 = \frac{R2\,R1}{R2 + R1}$

Figure 13. Multiple Feedback Bandpass Filter



$V_{ref} = \frac{1}{2} V_{CC}$

Given: f_o = center frequency
$A(f_o)$ = gain at center frequency

Choose value f_o, C

Then: $R3 = \frac{Q}{\pi f_o C}$ $R1 = \frac{R3}{2\,A(f_o)}$ $R2 = \frac{R1\,R5}{4Q^2\,R1 - R5}$

For less than 10% error from operational amplifier $\frac{O_o f_o}{BW} < 0.1$ where f_o and BW are expressed in Hz.

If source impedance varies, filter may be preceded with voltage follower buffer to stabilize filter parameters.

MOTOROLA

MC3405

Dual Operational Amplifier and Dual Comparator

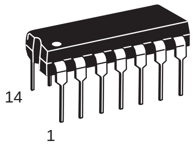
DUAL OPERATIONAL AMPLIFIER / DUAL VOLTAGE COMPARATOR

SEMICONDUCTOR TECHNICAL DATA

The MC3405 contains two differential–input operational amplifiers and two comparators, each set capable of single supply operation. This operational amplifier–comparator circuit fulfills its applications as a general purpose product for automotive and consumer circuits as well as an industrial building block.

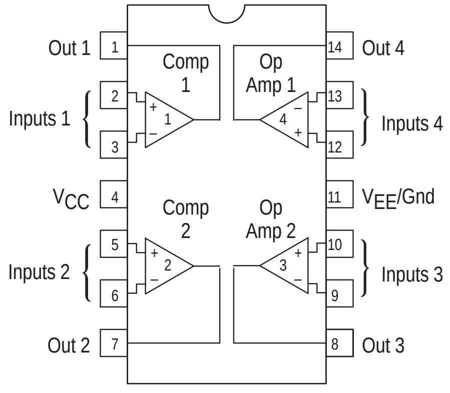
The MC3405 is specified over the commercial operating temperature range of 0° to +70°C.

- Operational Amplifier Equivalent in Performance to MC3403
- Comparator Similar in Performance to LM339
- Single Supply Operation: 3.0 V to 36 V
- Split Supply Operation: ±1.5 V to ±18 V
- Low Supply Current Drain
- Operational Amplifier is Internally Frequency Compensated
- Comparator TTL and CMOS Compatible

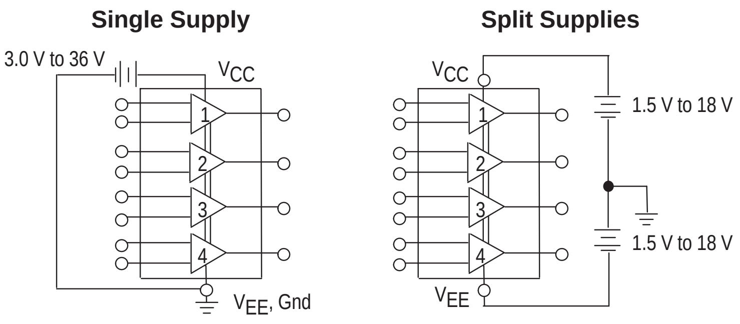


P SUFFIX
PLASTIC PACKAGE
CASE 646

PIN CONNECTIONS



(Top View)



ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC3405P	T_A = 0° to +70°C	Plastic DIP

OPERATIONAL AMPLIFIER SECTION

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage – Single Supply Split Supplies	V_{CC} V_{CC}, V_{EE}	36 ±18	Vdc
Input Differential Voltage Range	V_{IDR}	±36	Vdc
Input Common Mode Voltage Range	V_{ICR}	±18	Vdc
Operating Ambient Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	Tstg	–55 to +125	°C
Operating Junction Temperature Range	T_J	150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, V_{EE} = Gnd, T_A = 25°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Offset Voltage	V_{IO}	–	2.0	10	mV
Input Offset Current	I_{IO}	–	30	50	nA
Input Bias Current	I_{IB}	–	–200	–500	nA
Large–Signal, Open Loop Voltage Gain (R_L = 2.0 kΩ)	A_{VOL}	20	200	–	V/mV
Power Supply Rejection	PSR	–	–	150	µV/V
Output Voltage Range (Note 1)	V_{OR}				V_{pp}
(R_L = 10 kΩ, V_{CC} = 5.0 V)		3.3	3.5	–	
(R_L = 10 kΩ, 5.0 V ≤ V_{CC} ≤ 30 V)		V_{CC} –2.0	V_{CC} –1.7	–	
Power Supply Current (Notes 2 and 3)	I_{CC}	–	2.5	7.0	mA
Channel Separation, f = 1.0 kHz to 20 kHz (Input Referenced)	–	–	–120	–	dB

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = –15 V, T_A = 25°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Offset Voltage	V_{IO}	–	2.0	10	mV
(T_A = T_{low} + T_{high}) (Note 4)		–	–	12	
Average Temperature Coefficient of Input Offset Voltage	$\Delta V_{IO}/\Delta T$	–	15	–	µV/°C
Input Offset Current	I_{IO}	–	–	50	nA
(T_A = T_{low} to T_{high}) (Note 4)		–	–	200	
Input Bias Current	I_{IB}	–	–200	–500	nA
(T_A = T_{low} to T_{high}) (Note 4)		–	–	–800	
Input Common Mode Voltage Range	V_{ICR}	+13 –V_{EE}	–	–	Vdc
Large Signal, Open Loop Voltage Gain	A_{VOL}				V/mV
(V_O = ±10 V, R_L = 2.0 kΩ)		20	200	–	
(T_A = T_{low} to T_{high}) (Note 4)		15	100	–	
Common Mode Rejection	CMR	70	90	–	dB
Power Supply Rejection Ratio	PSRR	–	30	150	µV/V
Output Voltage	V_O				Vdc
(R_L = 10 kΩ)		±12	±13.5	–	
(R_L = 2.0 kΩ)		±10	±13	–	
(R_L = 2.0 kΩ, T_A = T_{low} to T_{high}) (Note 4)		±10	–	–	
Output Short Circuit Current	I_{SC}	±10	±20	±45	mA
Power Supply Current (Notes 2 and 3)	I_{CC}, I_{EE}	–	2.8	7.0	mA
Phase Margin	φm	–	60	–	Degrees
Small–Signal Bandwidth (A_V = 1, R_L = 10 kΩ, V_O = 50 mV)	BW	–	1.0	–	MHz

NOTES: 1. Output will swing to ground.
2. Not to exceed maximum package power dissipation.
3. For operational amplifier and comparator.
4. T_{low} = 0°C, T_{high} = +70°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = –15 V, T_A = 25°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Power Bandwidth (A_V = 1, R_L = 2.0 kΩ, V_O = 20 V_{pp}, THD = 5%)	BWp	–	9.0	–	kHz
Rise Time/Fall Time	t_{TLH}, t_{THL}	–	0.35	–	µs
Overshoot (A_V = 1, R_L = 10 kΩ, V_O = 50 mV)	os	–	20	–	%
Slew Rate	SR	–	0.6	–	V/µs

COMPARATOR SECTION

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage – Single Supply Split Supplies	V_{CC} V_{CC}, V_{EE}	36 ±18	Vdc
Input Differential Voltage Range	V_{IDR}	±36	Vdc
Input Common Mode Voltage Range	V_{ICR}	–0.3 to +36	Vdc
Sink Current	I_{Sink}	20	mA
Operating Ambient Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	Tstg	–55 to +125	°C
Operating Junction Temperature Range	T_J	150	°C

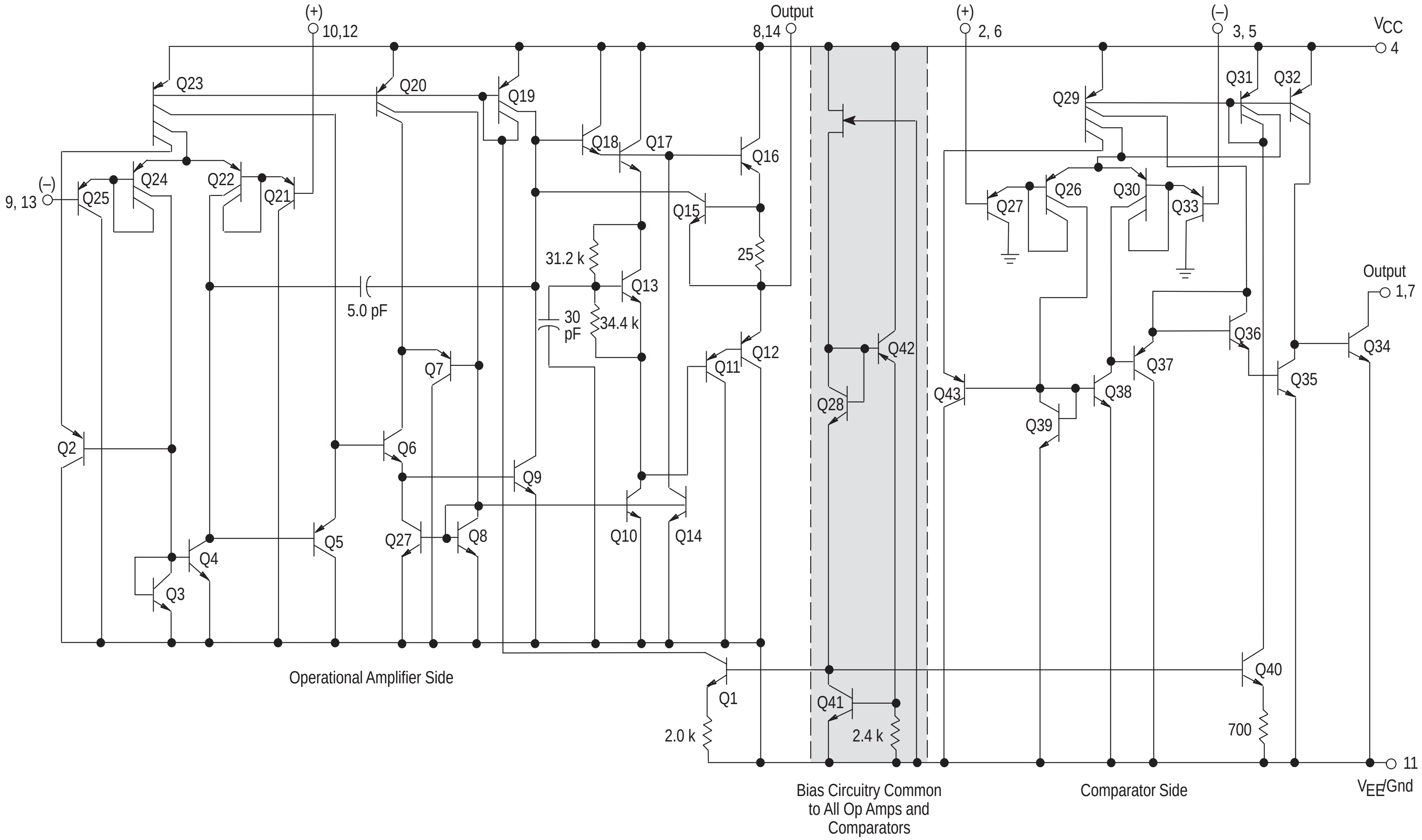
ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, V_{EE} = Gnd, T_A = 25°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Offset Voltage (T_A = T_{low} to T_{high}) (Notes 1 and 2)	V_{IO}	– –	2.0 –	10 12	mV
Average Temperature Coefficient of Input Offset Voltage	$\Delta V_{IO}/\Delta T$	–	15	–	µV/°C
Input Offset Current (T_A = T_{low} to T_{high}) (Note 1)	I_{IO}	– –	50 –	100 200	nA
Input Bias Current (T_A = T_{low} to T_{high}) (Note 1)	I_{IB}	– –	–125 –	–500 –800	nA
Input Common Mode Voltage Range (T_A = T_{low} to T_{high}) (Note 1)	V_{ICR}	0 0	V_{CC} –1.5 V_{CC} –1.7	V_{CC} –1.7 V_{CC} –2.0	Vpp
Input Differential Voltage (All V_{in} ≥ 0 Vdc)	V_{ID}	–	–	36	V
Large–Signal, Open Loop Voltage Gain (R_L = 15 kΩ)	A_{VOL}	–	200	–	V/mV
Output Sink Current (–V_{in} ≥ 1.0 Vdc, +V_{in}= 0, V_O ≤ 1.5 V)	I_{Sink}	6.0	16	–	mA
Low Level Output Voltage (+V_{in}= 0 V, –V_{in}= 1.0 V, I_{Sink} = 4.0 mA) (T_A = T_{low} to T_{high}) (Note 1)	V_{OL}	 – –	 350 –	 500 700	µA
Output Leakage Current (+V_{in} ≥ 1.0 Vdc, –V_{in}= 0, V_O = 5.0 Vdc) (T_A = T_{low} to T_{high}) (Note 1)	I_{OL}	 – –	 0.1 0.1	 1.0 1.0	µA
Large–Signal Response	–	–	300	–	ns
Response Time (Note 3) (V_{RL} = 5.0 Vdc, R_L = 5.1 kΩ)	–	–	1.3	–	µs

NOTES: 1. T_{low} = 0°C, T_{high} = +70°C
2. $V_O \cong$ 1.4 V, R_S = 0 Ω with V_{CC} from 5.0 Vdc to 30 Vdc, and over the input common mode range 0 to V_{CC} –1.7 V.
3. The response time specified is for a 100 mV input step with 5.0 mV overdrive. For larger signals 300 ns is typical.

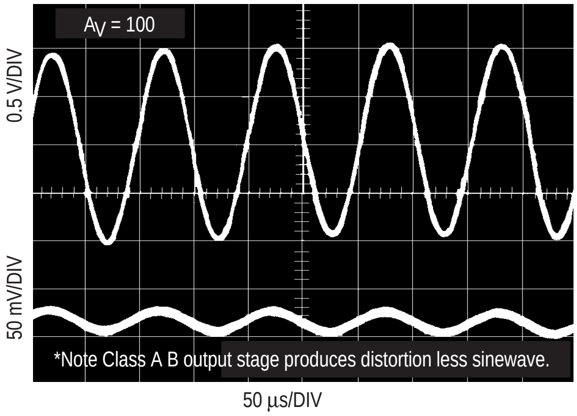
Representative Schematic Diagram

(1/2 of Circuit Shown)



OPERATIONAL AMPLIFIER SECTION

Figure 1. Sine Wave Response



*Note Class A B output stage produces distortion less sinewave.

Figure 2. Open Loop Frequency Response

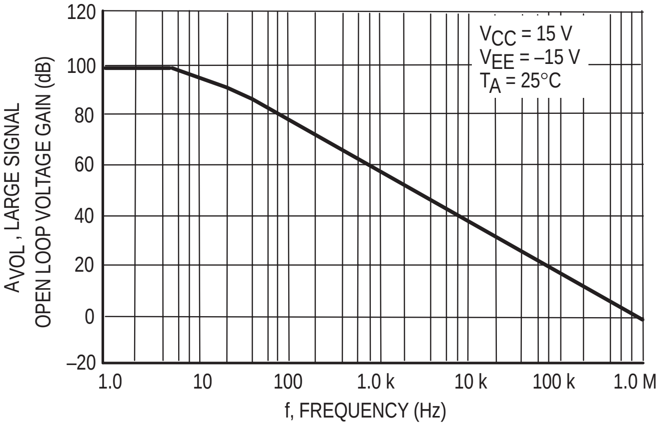


Figure 3. Power Bandwidth

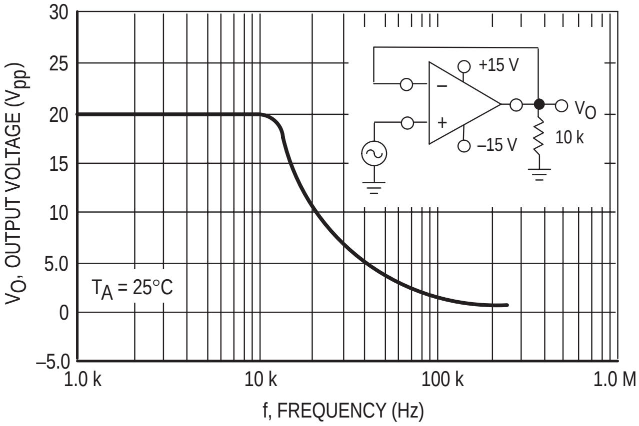


Figure 4. Output Swing versus Supply Voltage

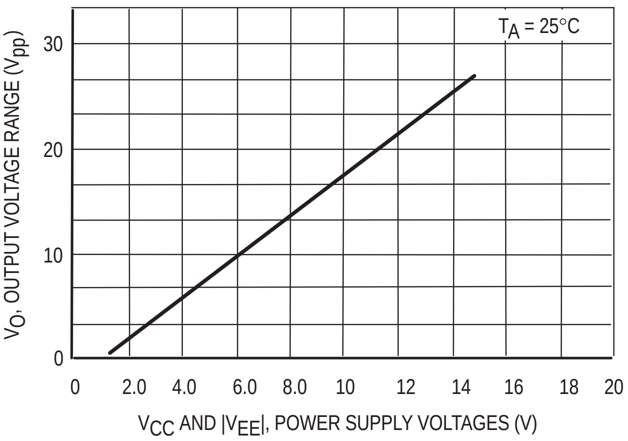


Figure 5. Input Bias Current versus Temperature

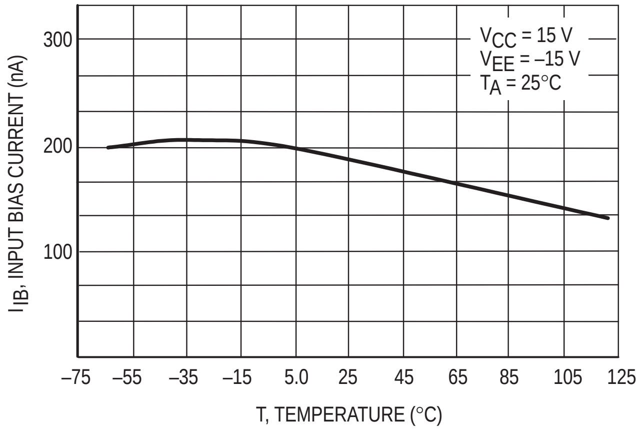
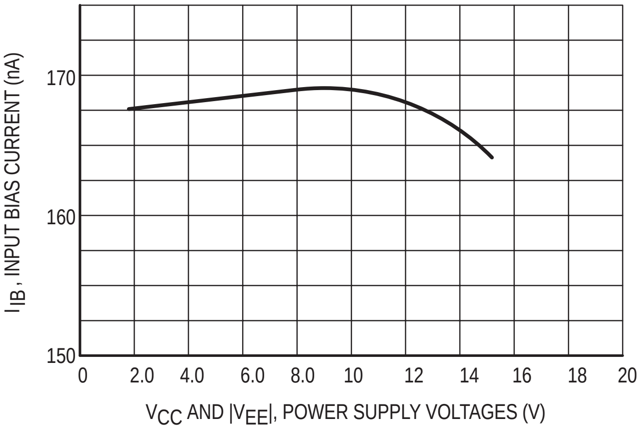


Figure 6. Input Bias Current versus Supply Voltage



COMPARATOR SECTION

Figure 7. Normalized Input Offset Voltage

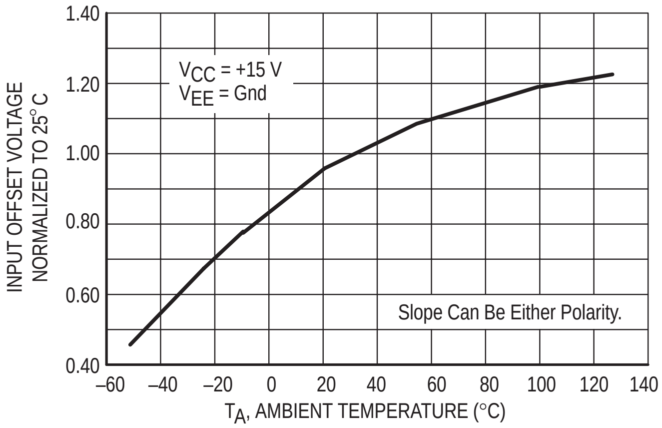


Figure 8. Input Bias Current

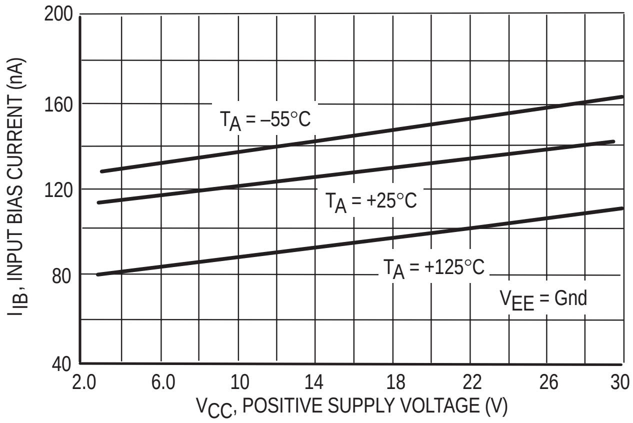


Figure 9. Normalized Input Offset Current

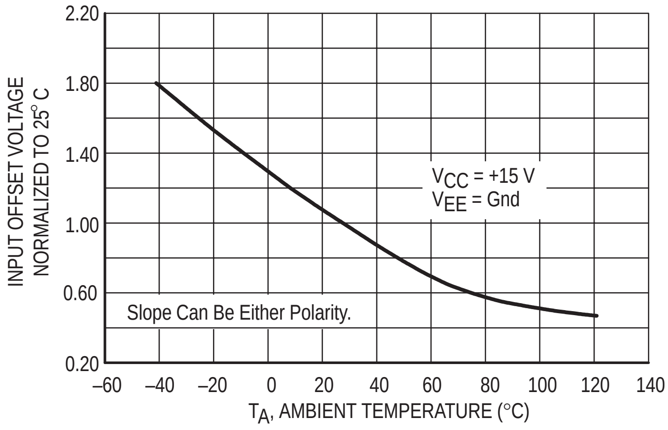


Figure 10. Output Sink Current versus Output Voltage

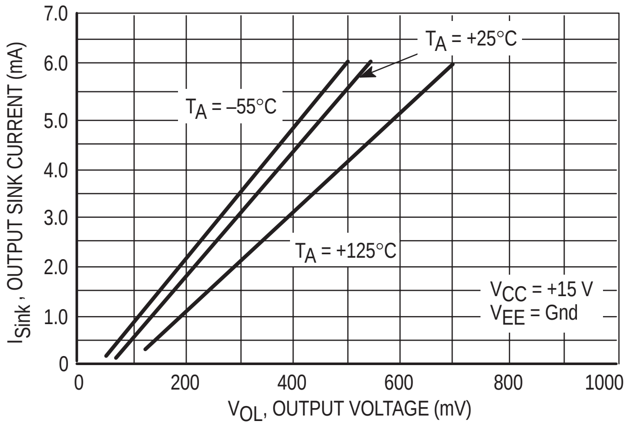
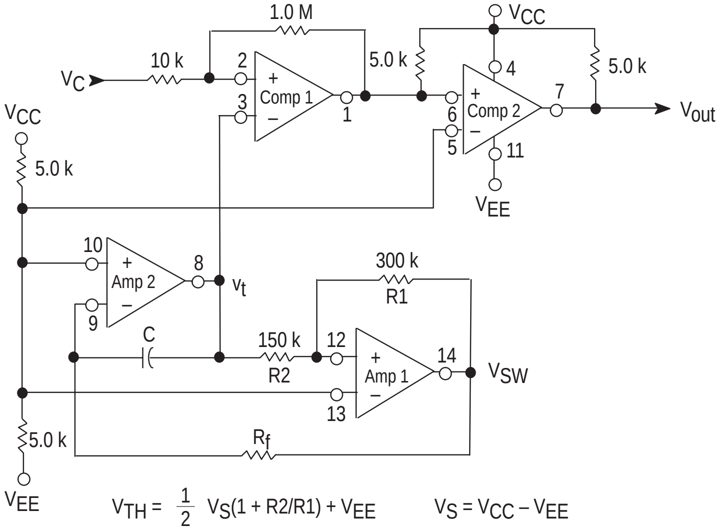
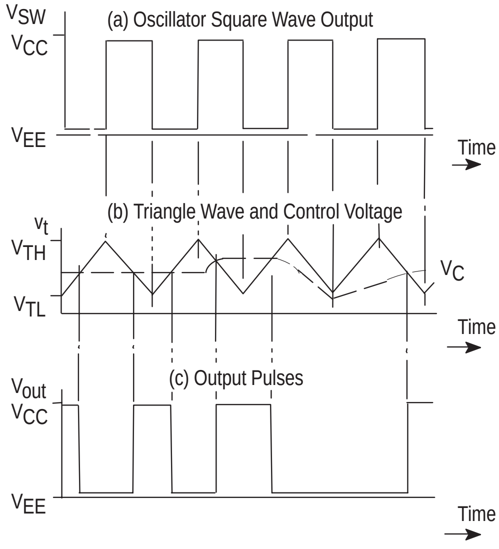


Figure 11. Pulse Width Modulator Schematic and Waveforms





$V_{TH} = \frac{1}{2}\,V_S(1 + R2/R1) + V_{EE}$ $V_S = V_{CC} - V_{EE}$

$V_{TL} = \frac{1}{2}\,V_S(1 - R2/R1) + V_{EE}$

Oscillator Frequency $f = \frac{R1}{4R_fCR2}$

Pulse Width = $\left(\frac{1}{f}\right)\left(\frac{V_c - V_{TL}}{V_{TH} - V_{TL}}\right)$ when: $V_{TL} < V_C < V_{TH}$

Duty Cycle in % = $\left(\frac{V_c - V_{TL}}{V_{TH} - V_{TL}}\right)$ (100)

Figure 12. Window Comparator

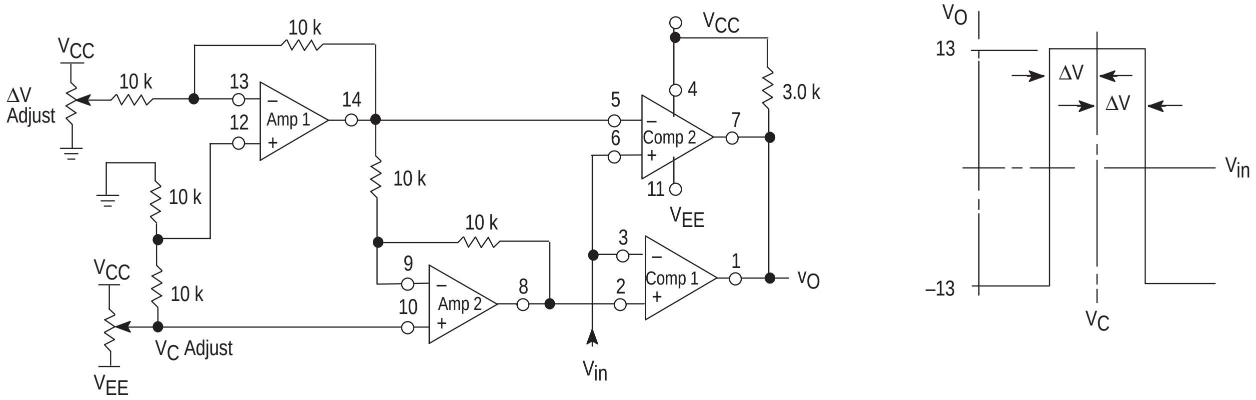
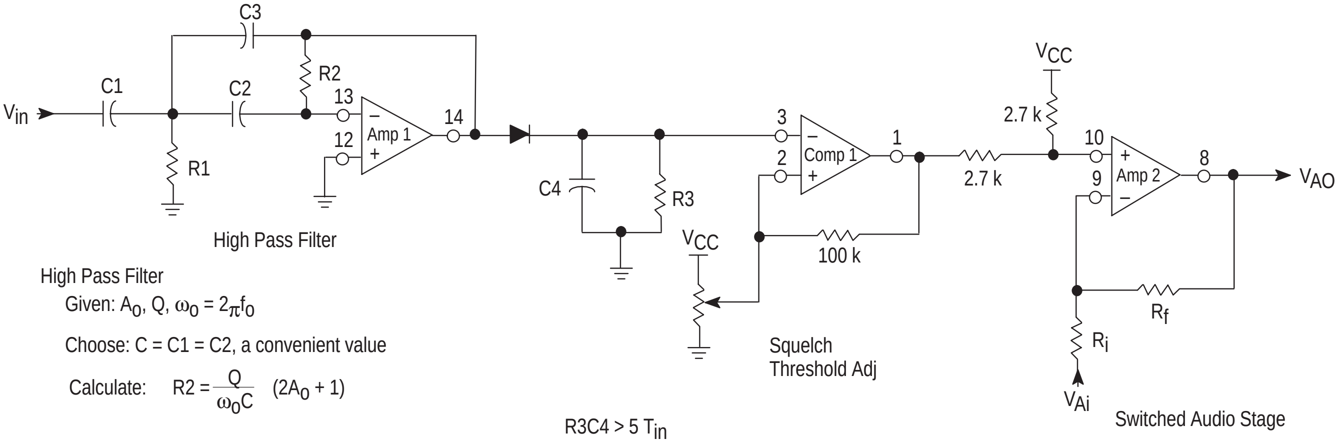


Figure 13. Squelch Circuit for AM or FM



High Pass Filter

Given: A_0, Q, $\omega_0 = 2\pi f_0$

Choose: C = C1 = C2, a convenient value

Calculate: $R2 = \frac{Q}{\omega_0 C}(2A_0 + 1)$

$C3 = \frac{C}{A_0}$

$R1 = \frac{A_0}{Q\omega_0 C(2A_0 + 1)}$

$R3C4 > 5\ T_{in}$

Where : T_{in} is the period of V_{in}

Q = Quality Factor

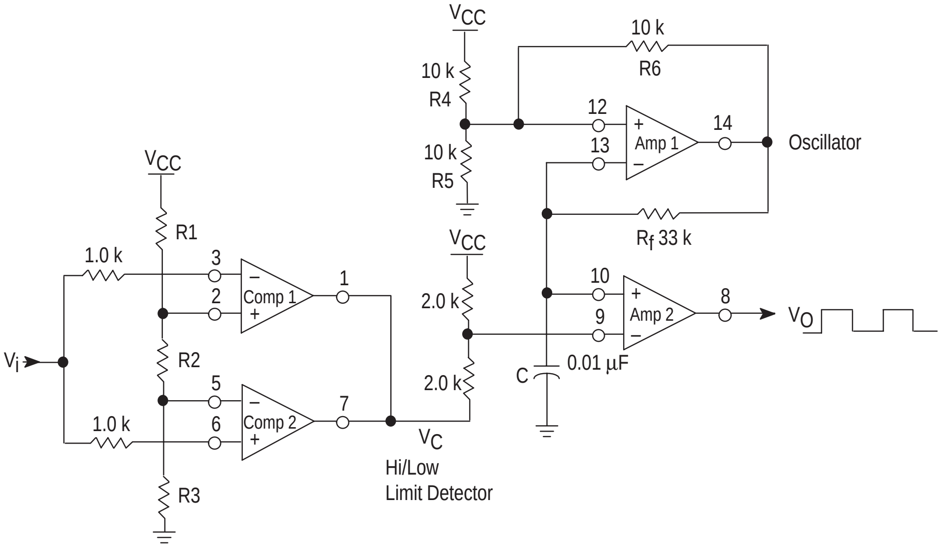
A_0 = High Frequency Gain

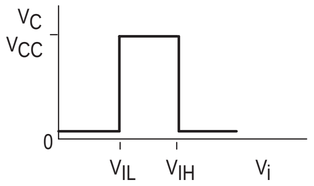
ω_0 = Break Frequency

Gain of Audio Stage

$A_{CI} = \frac{R_f}{R_i}$

Figure 14. High/Low Limit Alarm





$V_{IL} = V_{CC}\ \frac{R3}{R1 + R2 + R3}$

$V_{IH} = V_{CC}\ \frac{R2 + R3}{R1 + R2 + R3}$

Oscillator

If R4 = R5 = R6

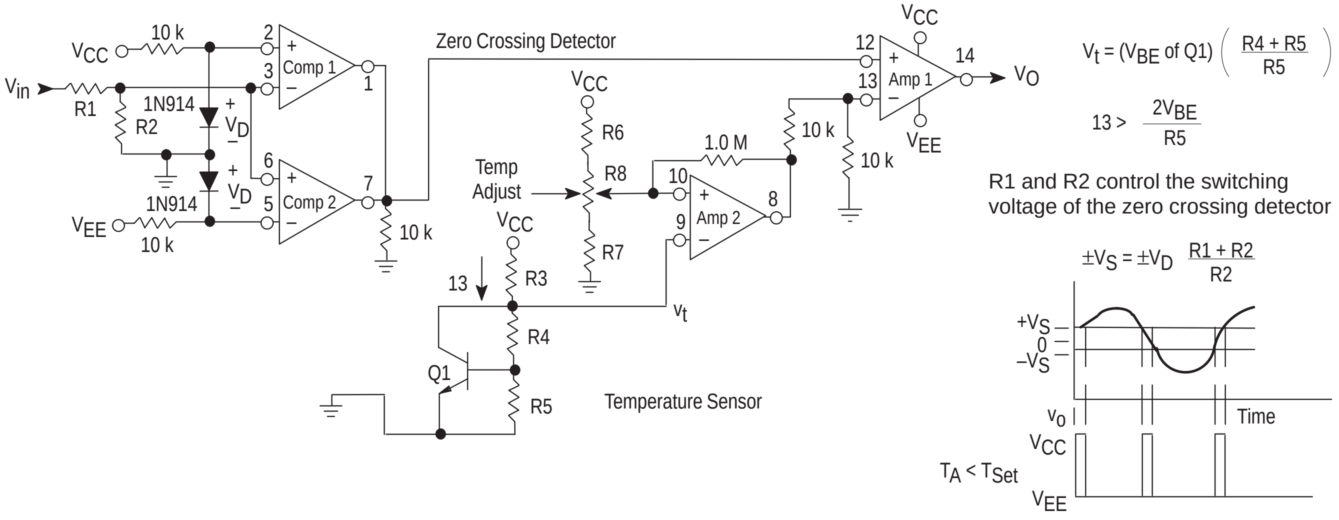
$f = 0.72/R_f C$

As shown, f = 2.2 kHz

V_O will oscillate if $V_{IH} < V_i$, or $V_{IL} > V_i$

V_O will be low if $V_{IL} < V_i < V_{IH}$

Figure 15. Zero Crossing Detector with Temperature Sensor



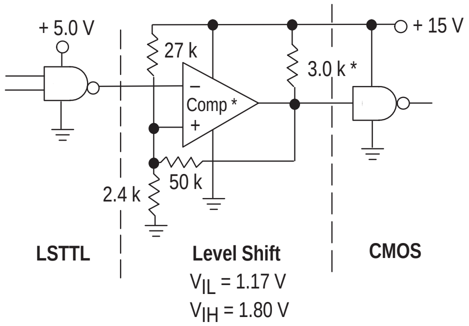
$V_t = (V_{BE}\text{ of Q1})\left(\frac{R4 + R5}{R5}\right)$

$13 > \frac{2V_{BE}}{R5}$

R1 and R2 control the switching voltage of the zero crossing detector

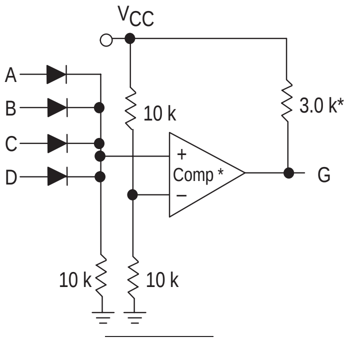
$\pm V_S = \pm V_D \frac{R1 + R2}{R2}$

Figure 16. LSTTL to CMOS Interface with Hysteresis



* The same configuration may be used with an op amp if the 3.0 k resistor is removed.

Figure 17. NOR Gate



$G = \overline{A + B + C + D}$

* The same configuration may be used with an op amp if the 3.0 k resistor is removed.

MOTOROLA

MC3458
MC3358

Dual, Low Power Operational Amplifiers

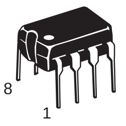
Utilizing the circuit designs perfected for the quad operational amplifiers, these dual operational amplifiers feature: 1) low power drain, 2) a common mode input voltage range extending to ground/V_{EE}, and 3) Single Supply or Split Supply operation.

These amplifiers have several distinct advantages over standard operational amplifier types in single supply applications. They can operate at supply voltages as low as 3.0 V or as high as 36 V with quiescent currents about one–fifth of those associated with the MC1741C (on a per amplifier basis). The common mode input range includes the negative supply, thereby eliminating the necessity for external biasing components in many applications. The output voltage range also includes the negative power supply voltage.

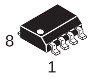
- Short Circuit Protected Outputs
- True Differential Input Stage
- Single Supply Operation: 3.0 V to 36 V
- Low Input Bias Currents
- Internally Compensated
- Common Mode Range Extends to Negative Supply
- Class AB Output Stage for Minimum Crossover Distortion
- Single and Split Supply Operations Available
- Similar Performance to the Popular MC1458

DUAL DIFFERENTIAL INPUT OPERATIONAL AMPLIFIERS

SEMICONDUCTOR TECHNICAL DATA

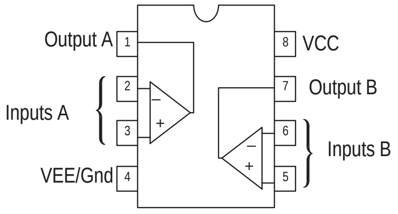


P1 SUFFIX
PLASTIC PACKAGE
CASE 626



D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

PIN CONNECTIONS



(Top View)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltages Single Supply Split Supplies	 V_{CC} V_{CC}, V_{EE}	 36 ±18	Vdc
Input Differential Voltage Range (1)	V_{IDR}	±30	Vdc
Input Common Mode Voltage Range (2)	V_{ICR}	±15	Vdc
Junction Temperature	T_J	150	°C
Storage Temperature Range	T_{stg}	–55 to +125	°C
Operating Ambient Temperature Range MC3458 MC3358	T_A	 0 to +70 –40 to +85	°C

NOTES: 1. Split Power Supplies.
2. For supply voltages less than ±18 V, the absolute maximum input voltage is equal to the supply voltage.

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC3358P1	T_A = –40° to +85°C	Plastic DIP
MC3458D	T_A = 0° to +70°C	SO–8
MC3458P1		Plastic DIP

ELECTRICAL CHARACTERISTICS (For MC3458, V_{CC} = +15 V, V_{EE} = –15 V, T_A = 25°C, unless otherwise noted.)
(For MC3358, V_{CC} = +14 V, V_{EE} = Gnd, T_A = 25°C, unless otherwise noted.)

Characteristic	Symbol	MC3458			MC3358			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage $T_A = T_{high}$ to T_{low} (Note 1)	V_{IO}	– –	2.0 –	10 12	– –	2.0 –	8.0 10	mV
Input Offset Current $T_A = T_{high}$ to T_{low}	I_{IO}	– –	30 –	50 200	– –	30 –	75 250	nA
Large Signal Open Loop Voltage Gain $V_O = \pm10$ V, R_L = 2.0 kΩ, $T_A = T_{high}$ to T_{low}	A_{VOL}	 20 15	 200 –	 – –	 20 15	 200 –	 – –	V/mV
Input Bias Current $T_A = T_{high}$ to T_{low}	I_{IB}	– –	–200 –	–500 –800	– –	–200 –	–500 –1000	nA
Output Impedance, f = 20 Hz	z_O	–	75	–	–	75	–	Ω
Input Impedance, f = 20 Hz	z_I	0.3	1.0	–	0.3	1.0	–	MΩ
Output Voltage Range R_L = 10 kΩ R_L = 2.0 kΩ R_L = 2.0 kΩ, $T_A = T_{high}$ to T_{low}	V_{OR}	 ±12 ±10 ±10	 ±13.5 ±13 –	 – – –	 12 10 10	 12.5 12 –	 – – –	V
Input Common Mode Voltage Range	V_{ICR}	+13 $-V_{EE}$	+13.5 $-V_{EE}$	–	+13 $-V_{EE}$	+13.5 $-V_{EE}$	–	V
Common Mode Rejection Ratio, $R_S \leq 10$ kΩ	CMR	70	90	–	70	90	–	dB
Power Supply Current (V_O = 0) $R_L = \infty$	I_{CC}, I_{EE}	–	1.6	3.7	–	1.6	3.7	mA
Individual Output Short Circuit Current (Note 2)	I_{SC}	±10	±20	±45	±10	±30	±45	mA
Positive Power Supply Rejection Ratio	PSRR+	–	30	150	–	30	150	µV/V
Negative Power Supply Rejection Ratio	PSRR–	–	30	150	–	–	–	µV/V
Average Temperature Coefficient of Input Offset Current, $T_A = T_{high}$ to T_{low}	$\Delta I_{IO}/\Delta T$	–	50	–	–	50	–	pA/°C
Average Temperature Coefficient of Input Offset Current, $T_A = T_{high}$ to T_{low}	$\Delta V_{IO}/\Delta T$	–	10	–	–	10	–	µV/°C
Power Bandwidth A_V = 1, R_L = 2.0 kΩ, V_O = 20 V_{pp}, THD = 5%	BWp	–	9.0	–	–	9.0	–	kHz
Small Signal Bandwidth A_V = 1, R_L = 10 kΩ, V_O = 50 mV	BW	–	1.0	–	–	1.0	–	MHz
Slew Rate A_V = 1, V_I = –10 V to +10 V	SR	–	0.6	–	–	0.6	–	V/µs
Rise Time A_V = 1, R_L = 10 kΩ, V_O = 50 mV	t_{TLH}	–	0.35	–	–	0.35	–	µs
Fall Time A_V = 1, R_L = 10 kΩ, V_O = 50 mV	t_{THL}	–	0.35	–	–	0.35	–	µs
Overshoot A_V = 1, R_L = 10 kΩ, V_O = 50 mV	os	–	20	–	–	20	–	%
Phase Margin A_V = 1, R_L = 2.0 kΩ, C_L = 200 pF	ϕm	–	60	–	–	60	–	Degrees
Crossover Distortion (V_{in} = 30 mV_{pp}, V_{out} = 2.0 V_{pp}, f = 10 kHz)	–	–	1.0	–	–	1.0	–	%

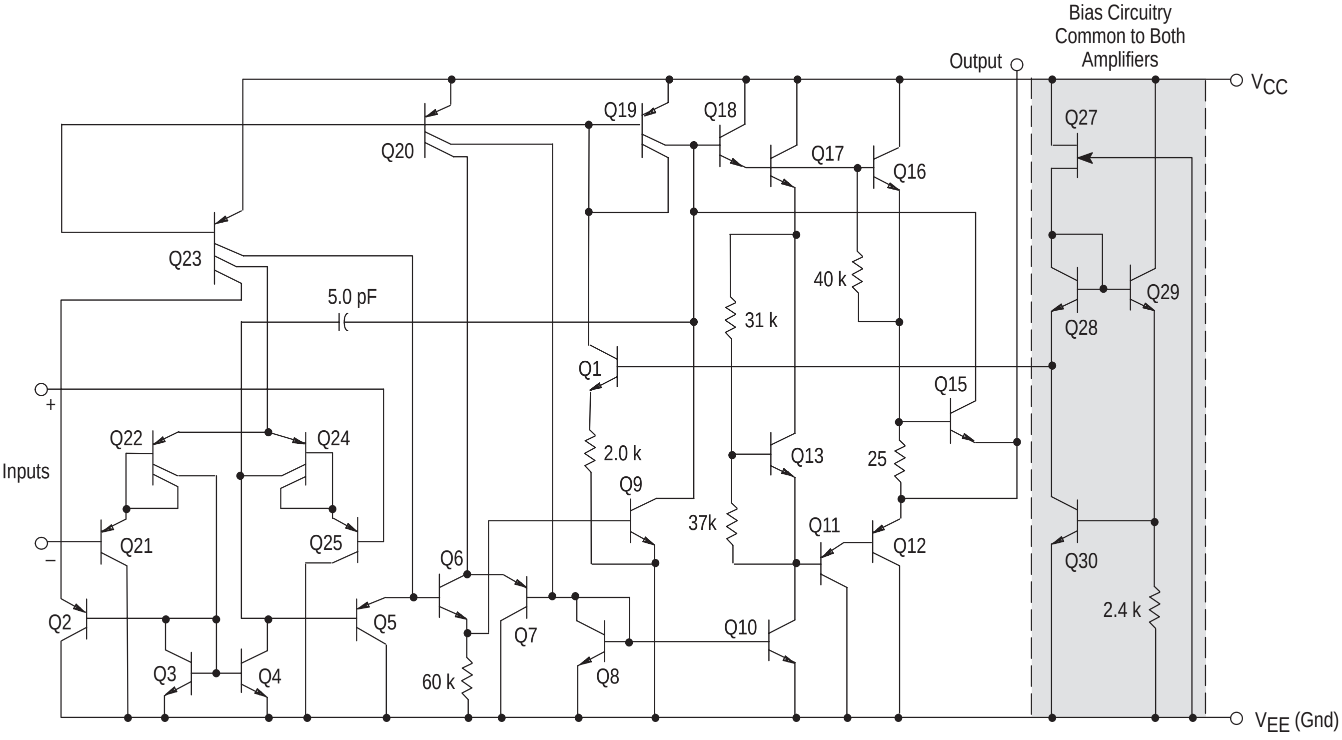
NOTES: 1. T_{high} = 70°C for MC3458, 85°C for MC3358
T_{low} = 0°C for MC3458, –40°C for MC3358
2. Not to exceed maximum package power dissipation.

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, V_{EE} = Gnd, T_A = 25°C, unless otherwise noted.)

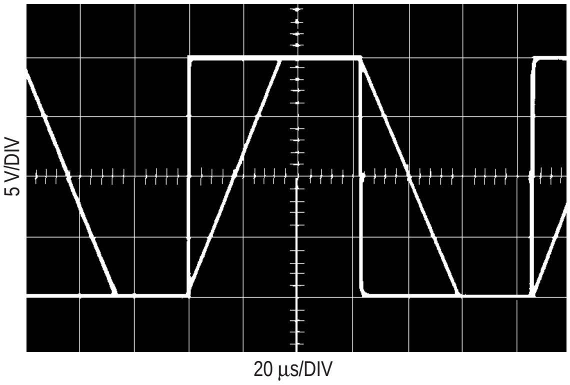
Characteristic	Symbol	MC3458			MC3358			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V_{IO}	–	2.0	5.0	–	2.0	10	mV
Input Offset Current	I_{IO}	–	30	50	–	–	75	nA
Input Bias Current	I_{IB}	–	–200	–500	–	–	–500	nA
Large Signal Open Loop Voltage Gain R_L = 2.0 kΩ,	A_{VOL}	20	200	–	20	200	–	V/mV
Power Supply Rejection Ratio	PSRR	–	–	150	–	–	150	µV/V
Output Voltage Range (Note 3)	V_{OR}							V_{pp}
R_L = 10 kΩ, V_{CC} = 5.0 V		3.3	3.5	–	3.3	3.5	–	
R_L = 10 kΩ, 5.0 V ≤ V_{CC} ≤ 30 V		–	V_{CC} –1.7	–	–	V_{CC} –1.7	–	
Power Supply Current	I_{CC}	–	2.5	7.0	–	2.5	4.0	mA
Channel Separation f = 1.0 kHz to 20 kHz (Input Referenced)	CS	–	–120	–	–	–120	–	dB

NOTE: 3. Output will swing to ground with a 10 kΩ pull down resistor.

Representative Schematic Diagram
(1/2 of Circuit Shown)



Inverter Pulse Response



CIRCUIT DESCRIPTION

The MC3458/3358 is made using two internally compensated, two–stage operational amplifiers. The first stage of each consists of differential input devices Q24 and Q22 with input buffer transistors Q25 and Q21 and the differential to single ended converter Q3 and Q4. The first stage performs not only the first stage gain function but also performs the level shifting and transconductance reduction functions. By reducing the transconductance, a smaller compensation capacitor (only 5.0 pF) can be employed, thus saving chip area. The transconductance reduction is accomplished by splitting the collectors of Q24 and Q22. Another feature of this input stage is that the input Common Mode range can include the negative supply or ground, in single supply operation, without saturating either the input devices or the differential to single–ended converter. The second stage consists of a standard current source load amplifier stage.

The output stage is unique because it allows the output to swing to ground in single supply operation and yet does not exhibit any crossover distortion in split supply operation. This is possible because Class AB operation is utilized.

Each amplifier is biased from an internal voltage regulator which has a low temperature coefficient thus giving each amplifier good temperature characteristics as well as excellent power supply rejection.

Figure 1. Sine Wave Response

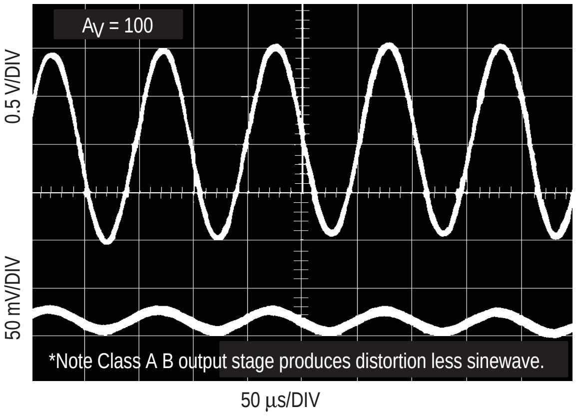


Figure 2. Open Loop Frequency Response

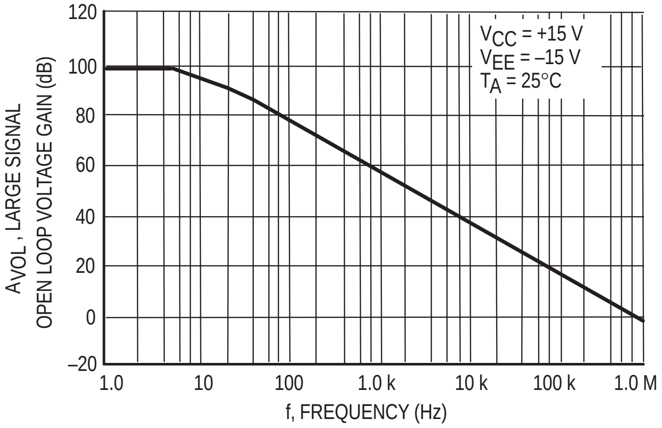


Figure 3. Power Bandwidth

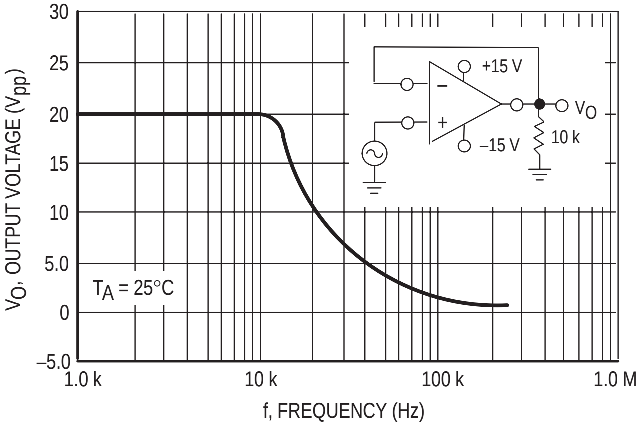


Figure 4. Output Swing versus Supply Voltage

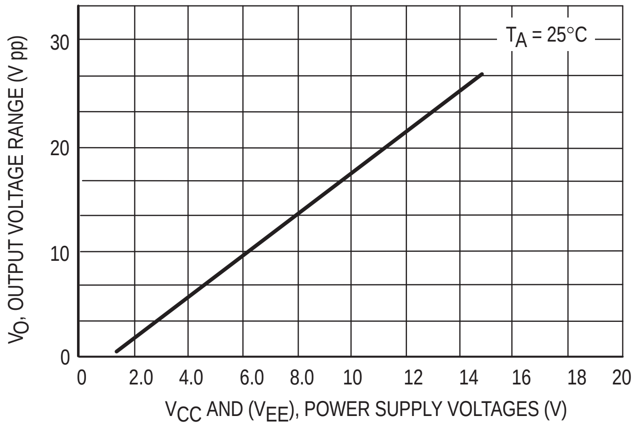


Figure 5. Input Bias Current versus Temperature

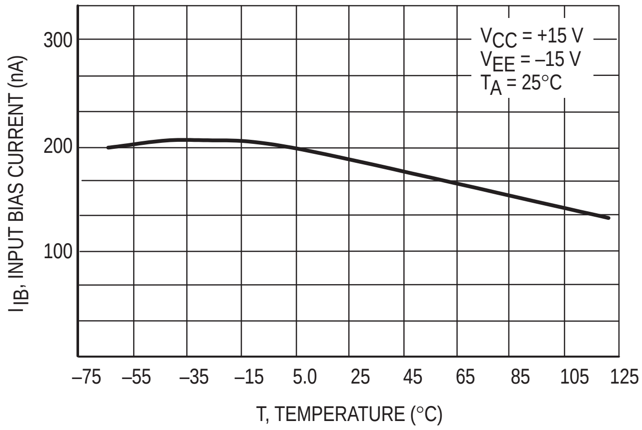


Figure 6. Input Bias Current versus Supply Voltage

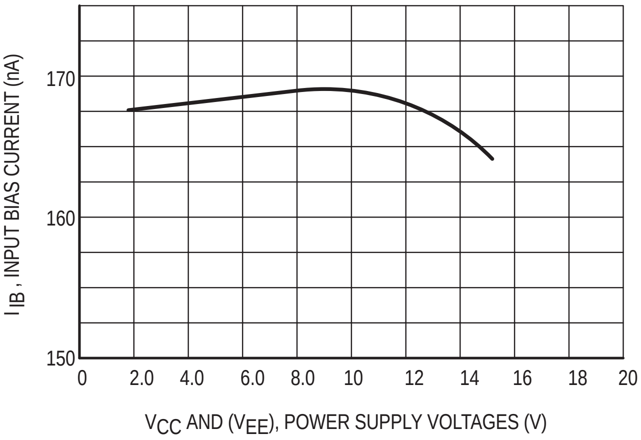


Figure 7. Voltage Reference

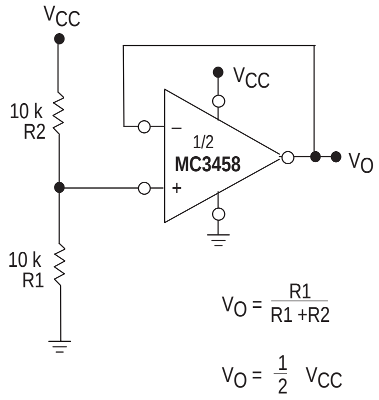


Figure 8. Wien Bridge Oscillator

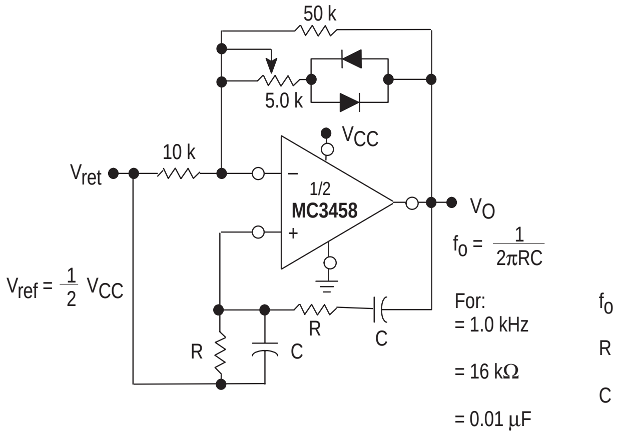


Figure 9. High Impedance Differential Amplifier

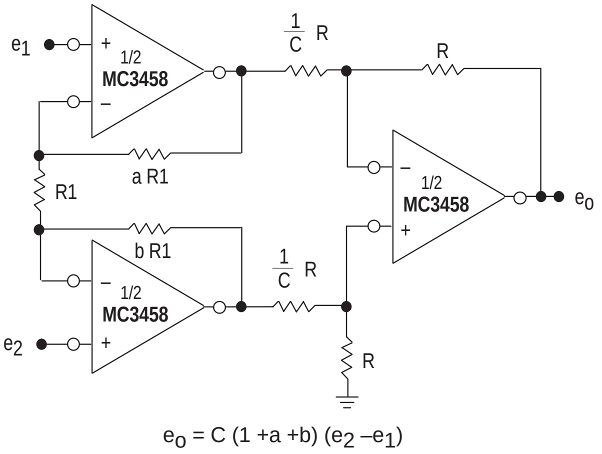


Figure 10. Comparator with Hysteresis

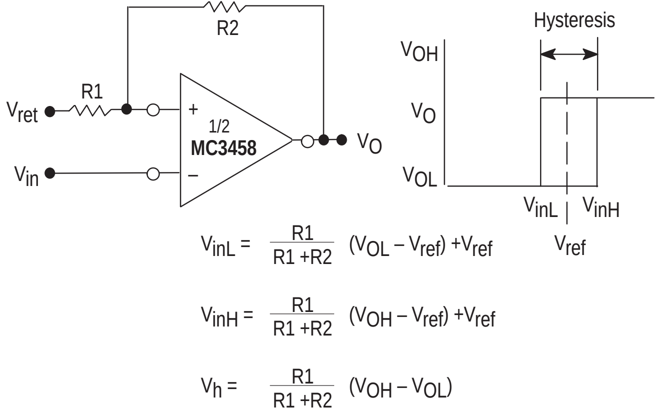


Figure 11. Bi–Quad Filter

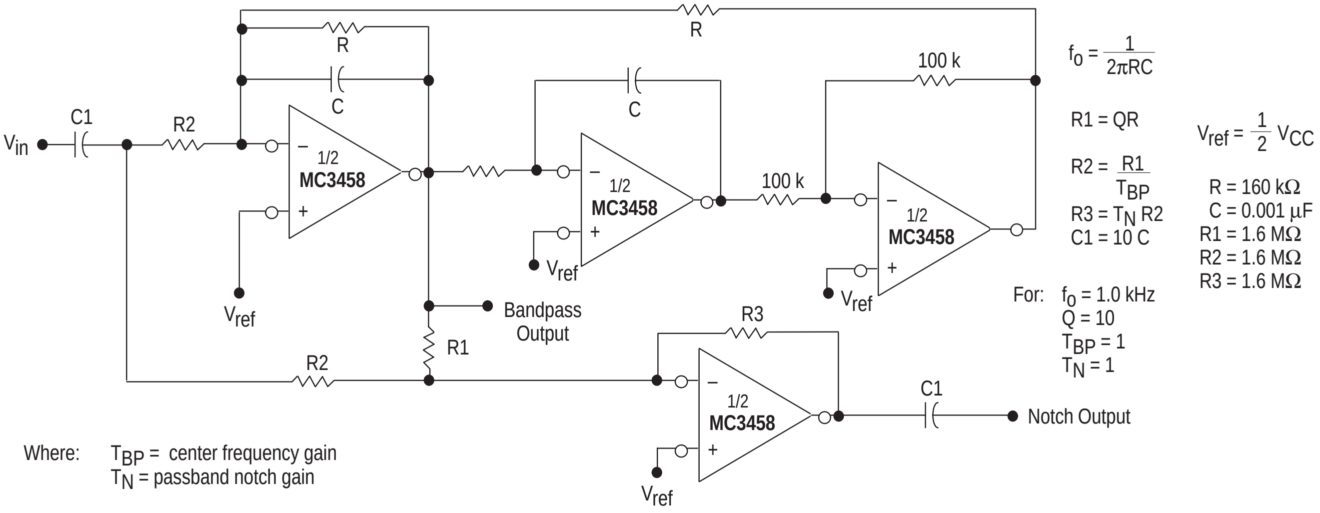
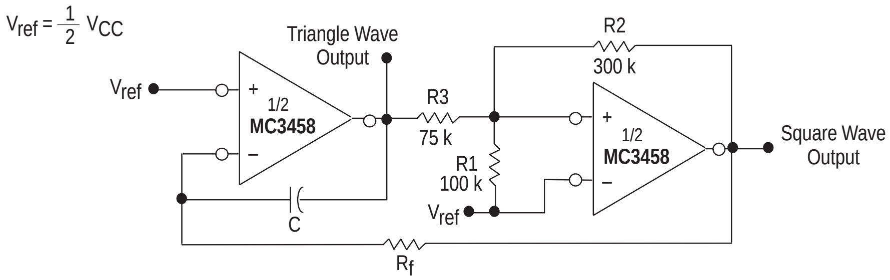
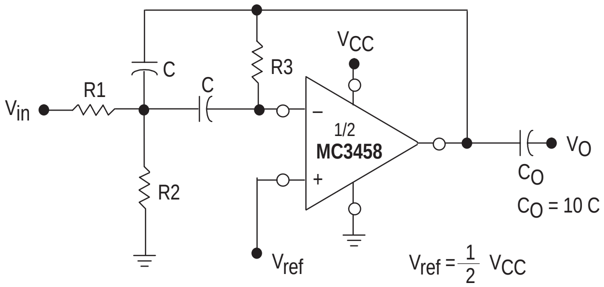


Figure 12. Function Generator



$$f = \frac{R1 + R_C}{4\,CR_f\,R1} \qquad \text{if,} \quad R3 = \frac{R2\,R1}{R2 + R1}$$

Figure 13. Multiple Feedback Bandpass Filter



Given: f_0 = center frequency
$A(f_0)$ = gain at center frequency

Choose value f_0, C.

Then: $R3 = \frac{Q}{\pi f_0 C}$ $\quad R1 = \frac{R3}{2\,A(f_0)}$ $\quad R2 = \frac{R1\,R5}{4Q^2\,R1 - R3}$

For less than 10% error from operational amplifier $\frac{Q_0\,f_0}{BW} < 0.1$

where, f_0 and BW are expressed in Hz.

If source impedance varies, filter may be preceded with voltage follower buffer to stabilize filter parameters.

MOTOROLA

MC3476

Low Cost Programmable Operational Amplifier

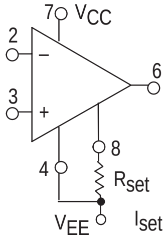
The MC3476 is a low cost selection of the popular industry standard MC1776 programmable operational amplifier. This extremely versatile operational amplifier features low power consumption and high input impedance. In addition, the quiescent currents within the device may be programmed by the choice of an external resistor value or current source applied to the I_{set} input. This allows the amplifier's characteristics to be optimized for input current and power consumption despite wide variations in operating power supply voltages.

- ±6.0 V to ±18 V Operation
- Wide Programming Range
- Offset Null Capability
- No Frequency Compensation Required
- Low Input Bias Currents
- Short Circuit Protection

Resistive Programming

(See Figure 1)

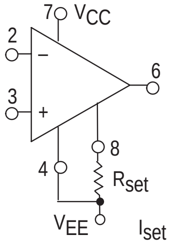
R_{set} to Ground



$$I_{set} = \frac{V_{CC} - 0.6}{R_{set}}$$

R_{set} to Negative Supply

(Recommended for supply voltage less than ±6.0 V)



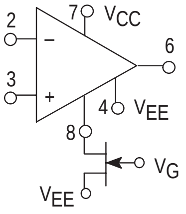
$$I_{set} = \frac{V_{CC} - 0.6 - V_{EE}}{R_{set}}$$

Typical R_{set} Values		
V_{CC}, V_{EE}	I_{set} = 1.5 μA	I_{set} = 15 μA
±6.0 V	3.6 MΩ	360 kΩ
±10 V	6.2 MΩ	620 kΩ
±12 V	7.5 MΩ	750 kΩ
±15 V	10 MΩ	1.0 MΩ

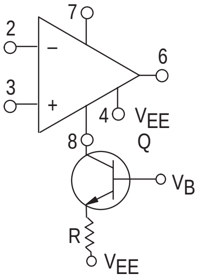
Typical R_{set} Values		
V_{CC}, V_{EE}	I_{set} = 1.5 μA	I_{set} = 15 μA
+1.5 V	1.6 MΩ	160 kΩ
+3.0 V	3.6 MΩ	360 kΩ
+6.0 V	7.5 MΩ	750 kΩ
+15 V	20 MΩ	2.0 MΩ

Active Programming

FET Current Source



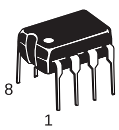
Bipolar Current Source



Pins not shown are not connected.

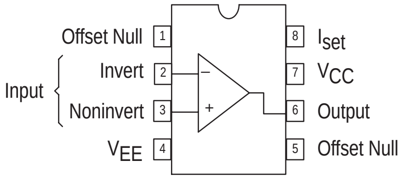
LOW COST PROGRAMMABLE OPERATIONAL AMPLIFIER

SEMICONDUCTOR TECHNICAL DATA



P1 SUFFIX
PLASTIC PACKAGE
CASE 626

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

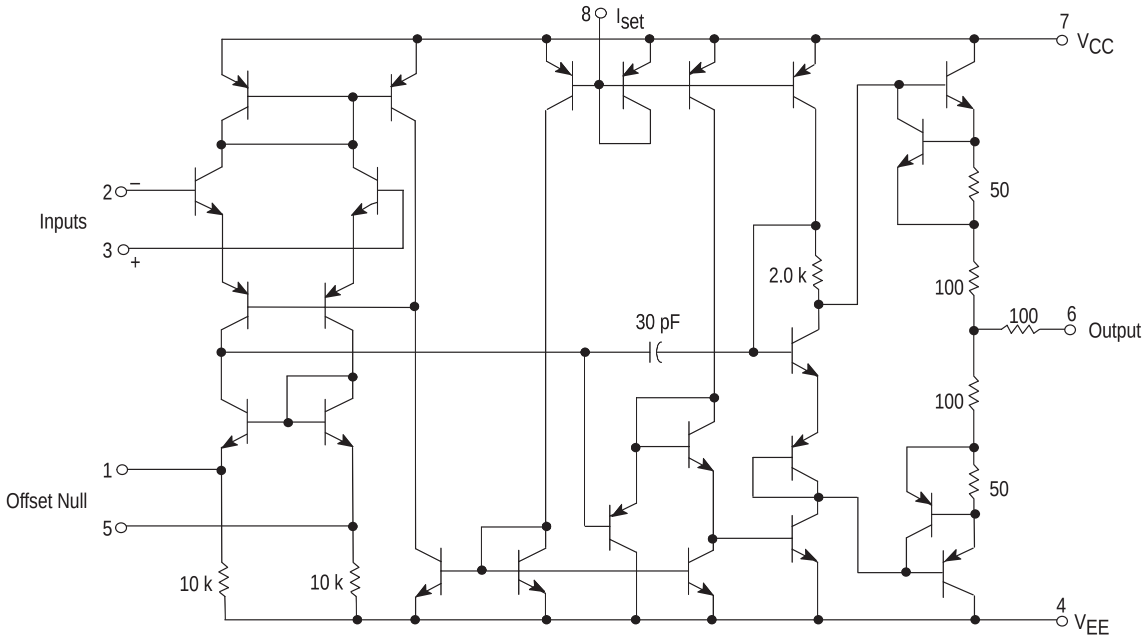
Device	Operating Temperature Range	Package
MC3476P1	T_A = 0° to +70°C	Plastic DIP

MAXIMUM RATINGS (T_A = +25°C, unless otherwise noted.)

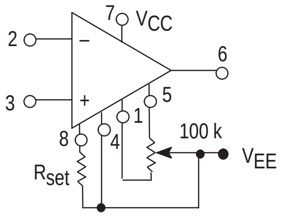
Rating	Symbol	Value	Unit
Power Supply Voltages	V_{CC}, V_{EE}	±18	Vdc
Input Differential Voltage Range	V_{IDR}	±30	Vdc
Input Common Mode Voltage Range	V_{ICR}	V_{CC}, V_{EE}	Vdc
Offset Null to V_{EE} Voltage	$V_{off} – V_{EE}$	±0.5	Vdc
Programming Current	I_{set}	200	µA
Programming Voltage (Voltage from I_{set} Terminal to Ground)	V_{set}	(V_{CC} – 0.6 V) to V_{CC}	Vdc
Output Short Circuit Duration (Note 1)	t_{SC}	Indefinite	sec
Operating Ambient Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	– 55 ot +125	°C
Junction Temperature	T_J	150	°C

NOTES: 1. Short circuit to ground with $I_{set} \le 15$ µA. Rating applies up to ambient temperature of +70°C.

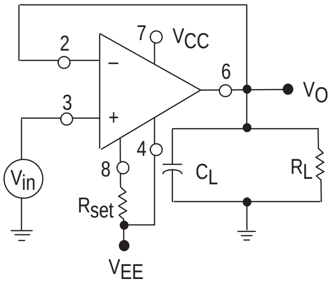
Representative Schematic Diagram



Voltage Offset Null Circuit



Transient Response Test Circuit



Pins not shown are
not connected.

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = – 15 V, I_{set} = 15 µA, T_A = +25°C, unless otherwise noted).

Characteristic	Symbol	Min	Typ	Max	Unit
Input Offset voltage (R_S ≤ 10 kΩ)	V_{IO}				mV
T_A = +25°C		–	2.0	6.0	
0°C ≤ T_A ≤ +70°C		–	–	7.5	
Offset Voltage Adjustment Range	V_{IOR}	–	18	–	mV
Input Offset Current	I_{IO}				nA
T_A = +25°C		–	20	25	
T_A = +70°C		–	–	25	
T_A = 0°C		–	–	40	
Input Bias Current	I_{IB}				nA
T_A = +25°C		–	15	50	
T_A = +70°C		–	–	50	
T_A = 0°C		–	–	100	
Input Resistance	r_i	–	5.0	–	MΩ
Input Capacitance	C_i	–	2.0	–	pF
Input Common Mode Voltage Gain 0°C ≤ T_A ≤ +70°C	V_{ICR}	±10	–	–	V
Large Signal Voltage Gain	A_{VOL}				V/V
R_L ≥ 10 kΩ, V_O = ±10 V, T_A = +25°C		50 k	400 k	–	
R_L ≥ 10 kΩ, V_O = ±10 V, 0°C ≤ T_A ≤ +70°C		25 k	–	–	
Output Voltage Range	V_{OR}				V
R_L ≥ 10 kΩ, T_A = +25°C		±12	±13	–	
R_L ≥ 10 kΩ, 0°C ≤ T_A ≤ +70°C		±12	–	–	
Output Resistance	r_o	–	1.0	–	kΩ
Output Short Circuit Current	I_{SC}	–	12	–	mA
Common Mode Rejection R_S ≤ 10 kΩ, 0°C ≤ T_A ≤ +70°C	CMR	70	90	–	dB
Supply Voltage Rejection Ratio R_S ≤ 10 kΩ, 0°C ≤ T_A ≤ +70°C	PSRR	–	25	200	µV/V
Supply Current	I_{CC}, I_{EE}				µA
T_A = +25°C		–	160	200	
0°C ≤ T_A ≤ +70°C		–	–	225	
Power Dissipation	P_D				mW
T_A = +25°C		–	4.8	6.0	
0°C ≤ T_A ≤ +70°C		–	–	6.75	
Transient Response (Unity Gain)					
V_{in} = 20 mV, R_L ≥ 10 kΩ, C_L = 100 pF					
Rise Time	t_{TLH}	–	0.35	–	µs
Overshoot	os	–	10	–	%
Slew Rate (R_L ≥ 10 kΩ)	SR	–	0.8	–	V/µs

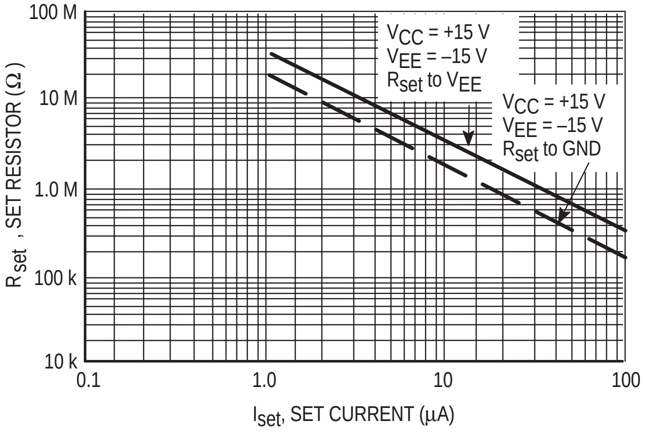


Figure 1. Set Current versus Set Resistor
100 M
10 M
1.0 M
100 k
10 k
R_{set}, SET RESISTOR (Ω)
0.1
1.0
10
100
I_{set}, SET CURRENT (μA)
V_{CC} = +15 V
V_{EE} = –15 V
R_{set} to V_{EE}
V_{CC} = +15 V
V_{EE} = –15 V
R_{set} to GND

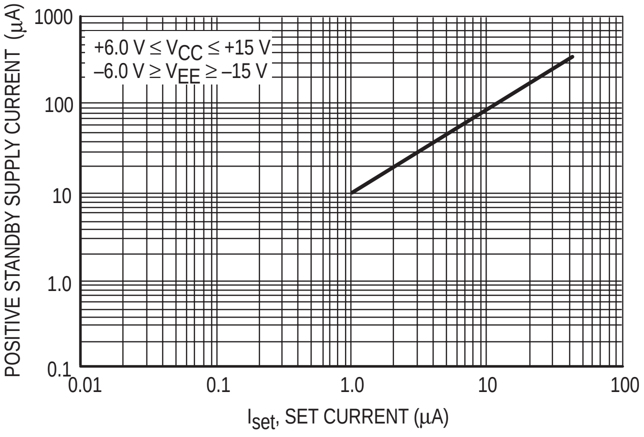


Figure 2. Positive Standby Supply Current versus Set Current
1000
100
10
1.0
0.1
POSITIVE STANDBY SUPPLY CURRENT (μA)
0.01
0.1
1.0
10
100
I_{set}, SET CURRENT (μA)
+6.0 V ≤ V_{CC} ≤ +15 V
–6.0 V ≥ V_{EE} ≥ –15 V

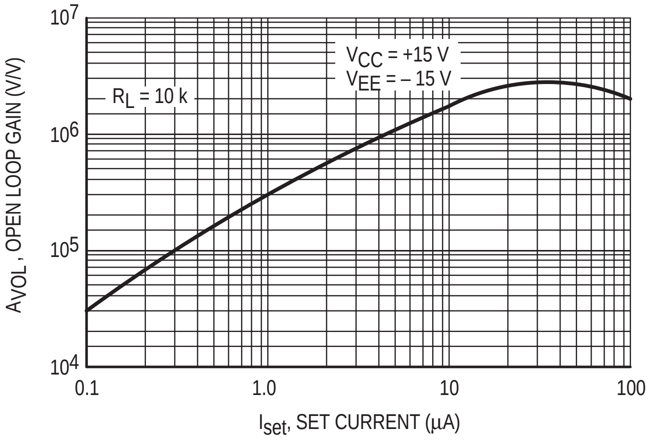


Figure 3. Open Loop versus Set Current
10^7
10^6
10^5
10^4
A_{VOL}, OPEN LOOP GAIN (V/V)
0.1
1.0
10
100
I_{set}, SET CURRENT (μA)
R_L = 10 k
V_{CC} = +15 V
V_{EE} = – 15 V

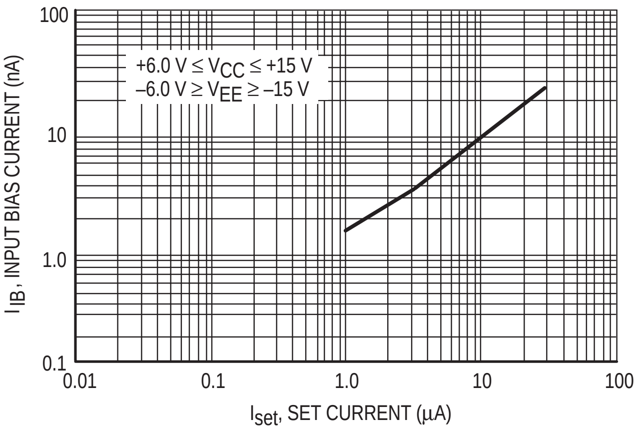


Figure 4. Input Bias Current versus Set Current
100
10
1.0
0.1
I_{IB}, INPUT BIAS CURRENT (nA)
0.01
0.1
1.0
10
100
I_{set}, SET CURRENT (μA)
+6.0 V ≤ V_{CC} ≤ +15 V
–6.0 V ≥ V_{EE} ≥ –15 V

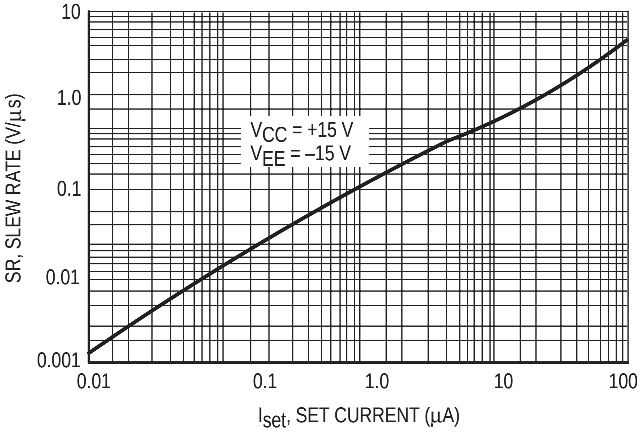


Figure 5. Slew Rate versus Set Current
10
1.0
0.1
0.01
0.001
SR, SLEW RATE (V/μs)
0.01
0.1
1.0
10
100
I_{set}, SET CURRENT (μA)
V_{CC} = +15 V
V_{EE} = –15 V

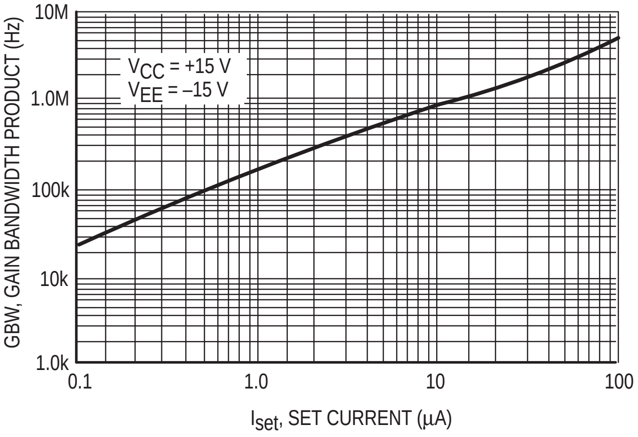


Figure 6. Gain Bandwidth Product versus Set Current
10M
1.0M
100k
10k
1.0k
GBW, GAIN BANDWIDTH PRODUCT (Hz)
0.1
1.0
10
100
I_{set}, SET CURRENT (μA)
V_{CC} = +15 V
V_{EE} = –15 V

Figure 7. Output Voltage Swing versus Load Resistance

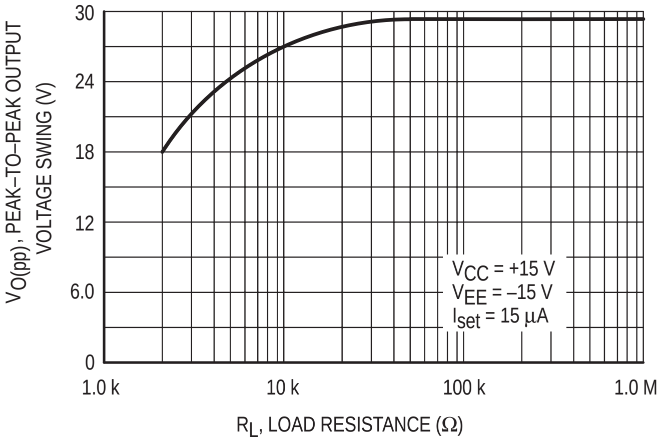
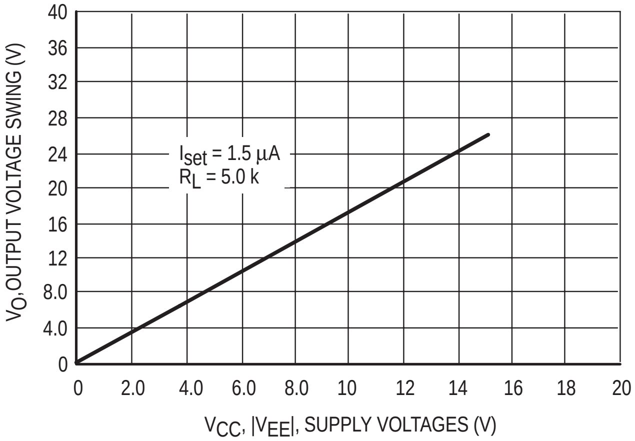


Figure 8. Output Voltage Swing versus Supply Voltage



MOTOROLA

MC4558AC
MC4558C

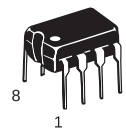
Dual Wide Bandwidth Operational Amplifiers

The MC4558AC, C combine all the outstanding features of the MC1458 and, in addition offer three times the unity gain bandwidth of the industry standard.

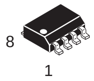
- 2.5 MHz Unity Gain Bandwidth Guaranteed (MC4558AC)
- 2.0 MHz Unity Gain Bandwidth Guaranteed (MC4558C)
- Internally Compensated
- Short Circuit Protection
- Gain and Phase Match between Amplifiers
- Low Power Consumption

DUAL WIDE BANDWIDTH OPERATIONAL AMPLIFIERS

SEMICONDUCTOR TECHNICAL DATA



P1 SUFFIX
PLASTIC PACKAGE
CASE 626



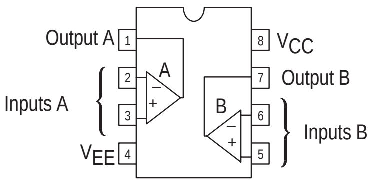
D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

MAXIMUM RATINGS (T_A = +25°C, unless otherwise noted.)

Rating	Symbol	MC4558AC	MC4558C	Unit
Power Supply Voltage	V_{CC} V_{EE}	+22 –22	+18 –18	Vdc
Input Differential Voltage	V_{ID}	±30		V
Input Common Mode Voltage (Note 1)	V_{ICM}	±15		V
Output Short Circuit Duration (Note 2)	t_{SC}	Continuous		
Ambient Temperature Range	T_A	0 to +70		°C
Storage Temperature Range	T_{stg}	–55 to +125		°C
Junction Temperature	T_J	150		°C

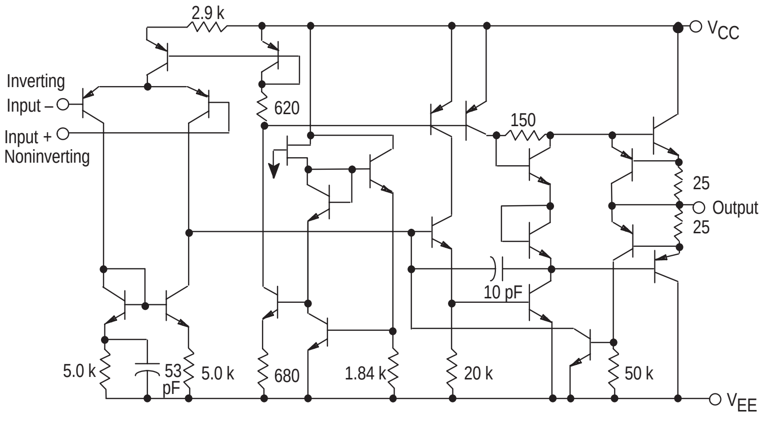
NOTES: 1. For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.
2. Short circuit may be to ground or either supply.

PIN CONNECTIONS



(Top View)

Representative Schematic Diagram
(1/2 of Circuit Shown)



ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC4558CD	T_A = 0° to +70°C	SO–8
MC4558ACP1,CP1		Plastic DIP

FREQUENCY CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = –15 V, T_A = 25°C)

Characteristic	Symbol	MC4558AC			MC4558C			Unit
		Min	Typ	Max	Min	Typ	Max	
Unity Gain Bandwidth	BW	2.5	2.8	–	2.0	2.8	–	MHz

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V, V_{EE} = –15 V, T_A = 25°C, unless otherwise noted.)

Input Offset Voltage (R_S ≤ 10 kΩ)	V_{IO}	–	1.0	5.0	–	2.0	6.0	mV
Input Offset Current	I_{IO}	–	20	200	–	20	200	nA
Input Bias Current (Note 1)	I_{IB}	–	80	500	–	80	500	nA
Input Resistance	r_i	0.3	2.0	–	0.3	2.0	–	MΩ
Input Capacitance	C_i	–	1.4	–	–	1.4	–	pF
Common Mode Input Voltage Range	V_{ICR}	±12	±13	–	±12	±13	–	V
Large Signal Voltage Gain (V_O = ±10 V, R_L = 2.0 kΩ)	A_{VOL}	50	200	–	20	200	–	V/mV
Output Resistance	r_o	–	75	–	–	75	–	Ω
Common Mode Rejection (R_S ≤ 10 kΩ)	CMR	70	90	–	70	90	–	dB
Supply Voltage Rejection Ratio (R_S ≤ 10 kΩ)	PSRR	–	30	150	–	30	150	µV/V
Output Voltage Swing (R_L ≥ 10 kΩ) (R_L ≥ 2.0 kΩ)	V_O	 ±12 ±10	 ±14 ±13	 – –	 ±12 ±10	 ±14 ±13	 – –	V
Output Short Circuit Current	I_{SC}	10	20	40	10	20	40	mA
Supply Currents (Both Amplifiers)	I_D	–	2.3	5.0	–	2.3	5.6	mA
Power Consumption (Both Amplifiers)	P_C	–	70	150	–	70	170	mW
Transient Response (Unity Gain) (V_I = 20 mV, R_L ≥ 2.0 kΩ, C_L ≤ 100 pF) Rise Time (V_I = 20 mV, R_L ≥ 2.0 kΩ, C_L ≤ 100 pF) Overshoot (V_I = 10 V, R_L ≥ 2.0 kΩ, C_L ≤ 100 pF) Slew Rate	 t_{TLH} os SR	 – – 1.5	 0.3 15 1.6	 – – –	 – – 1.0	 0.3 15 1.6	 – – –	 µs % V/µs

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = –15 V, T_A = T_{high} to T_{low}, unless otherwise noted. See Note 2.)

Input Offset Voltage (R_S ≤ 10 kΩ)	V_{IO}	–	1.0	6.0	–	–	7.5	mV
Input Offset Current (T_A = T_{high}) (T_A = T_{low}) (T_A = 0° to +70°C)	I_{IO}	 – – –	 7.0 85 –	 200 500 –	 – – –	 – – –	 – – 300	nA
Input Bias Current (T_A = T_{high}) (T_A = T_{low}) (T_A = 0° to +70°C)	I_{IB}	 – – –	 30 300 –	 500 1500 –	 – – –	 – – –	 – – 800	nA
Common Mode Input Voltage Range	V_{ICR}	±12	±13	–	–	–	–	V
Large Signal Voltage Gain (V_O = ±10 V, R_L = 2.0 kΩ)	A_{VOL}	25	–	–	15	–	–	V/mV
Common Mode Rejection (R_S ≤ 10 kΩ)	CMR	70	90	–	–	–	–	dB
Supply Voltage Rejection Ratio (R_S ≤ 10 kΩ)	PSRR	–	30	150	–	–	–	µV/V
Output Voltage Swing (R_L ≥ 10 kΩ) (R_L ≥ 2.0 kΩ)	V_O	 ±12 ±10	 ±14 ±13	 – –	 ±12 ±10	 ±14 ±13	 – –	V
Supply Currents (Both Amplifiers) (T_A = T_{high}) (T_A = T_{low})	I_D	 – –	 – –	 4.5 6.0	 – –	 – –	 5.0 6.7	mA
Power Consumption (Both Amplifiers) (T_A = T_{high}) (T_A = T_{low})	P_C	 – –	 – –	 135 180	 – –	 – –	 150 200	mW

NOTES: 1. I_{IB} is out of the amplifier due to PNP input transistors.
2. T_{high} = +70°C, T_{low} = 0°C.

Figure 1. Burst Noise versus Source Resistance

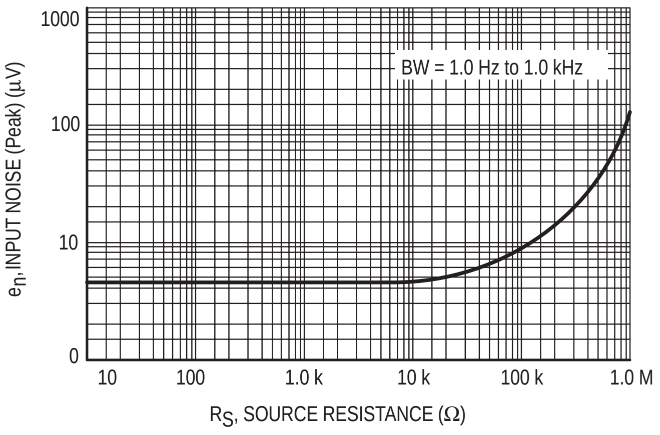


Figure 2. RMS Noise versus Source Resistance

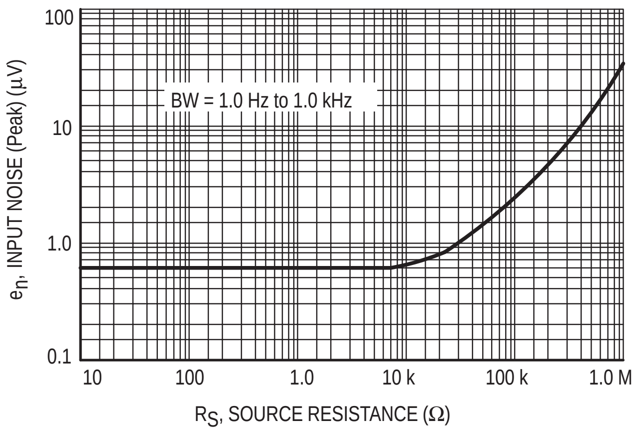


Figure 3. Output Noise versus Source Resistance

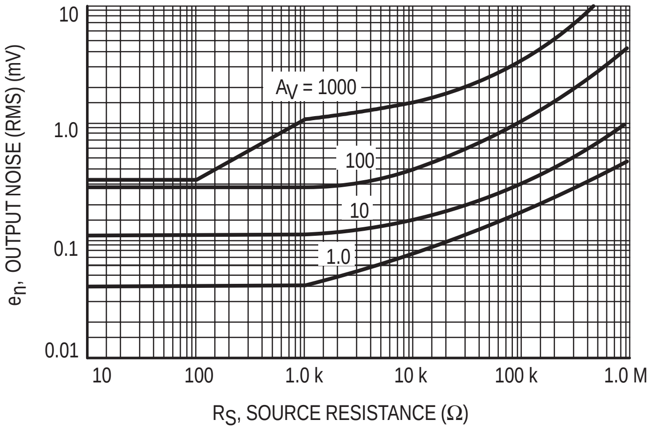


Figure 4. Spectral Noise Density

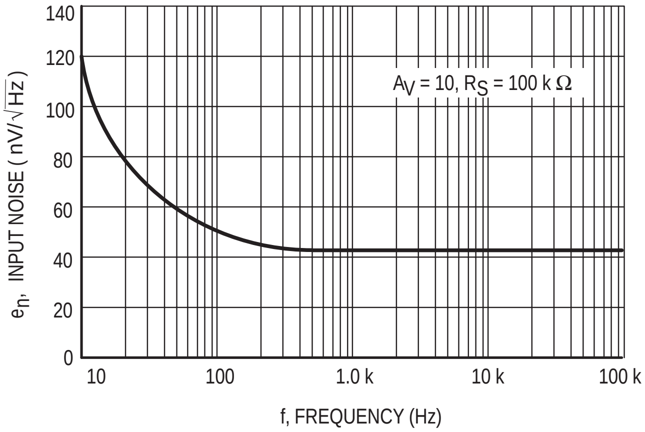
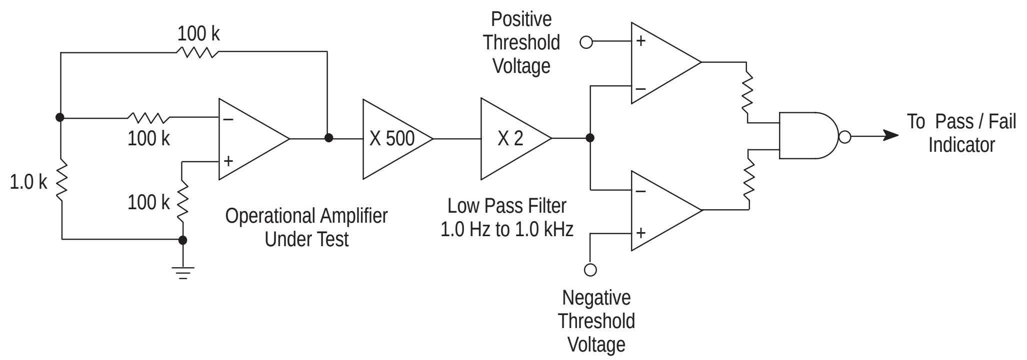


Figure 5. Burst Noise Test Circuit



Unlike conventional peak reading or RMS meters, this system was especially designed to provide the quick response time essential to burst (popcorn) noise testing.

The test time employed is 10 sec and the 20 μV peak limit refers to the operational amplifier input thus eliminating errors in the closed loop gain factor of the operational amplifier.

Figure 6. Open Loop Frequency Response

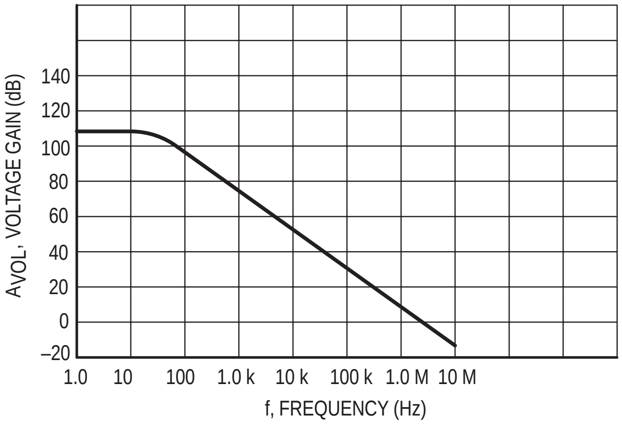


Figure 7. Phase Margin versus Frequency

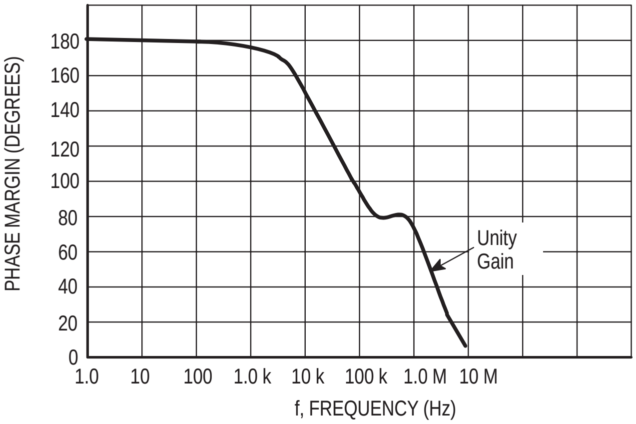


Figure 8. Positive Output Voltage Swing versus Load Resistance

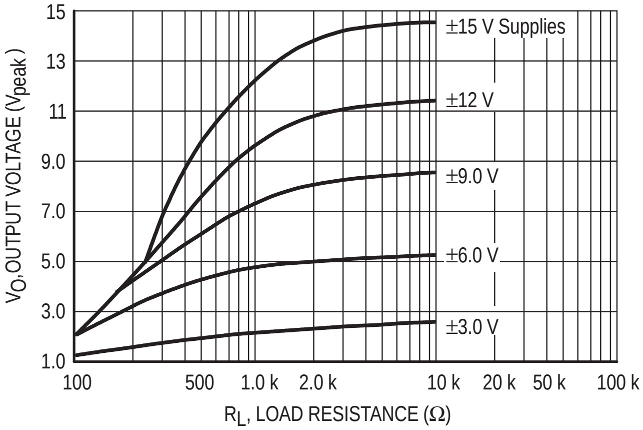


Figure 9. Negative Output Voltage Swing versus Load Resistance

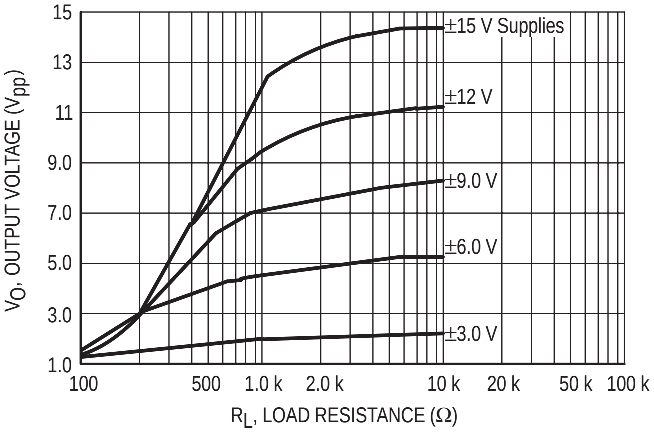


Figure 10. Power Bandwidth (Large Signal Swing versus Frequency)

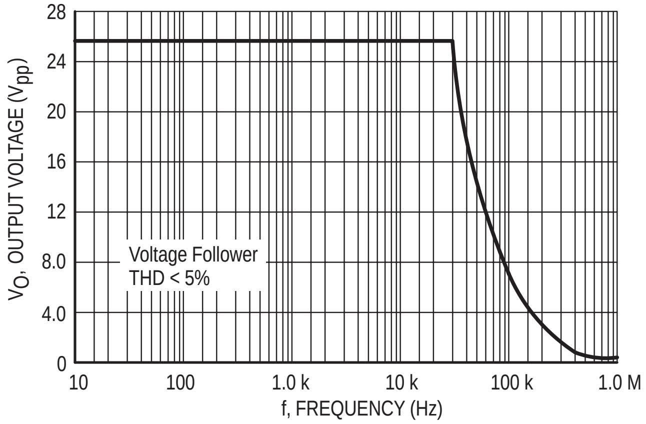
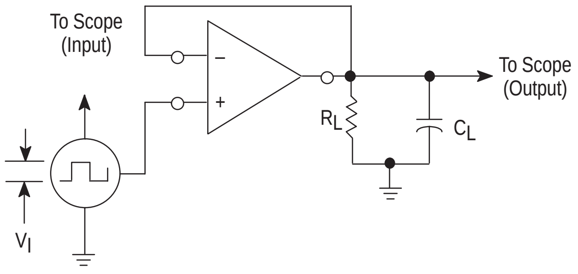


Figure 11. Transient Response Test Circuit



MOTOROLA

MCT4558C

Dual Wide Bandwidth Operational Amplifier

The MCT4558C combines all of the outstanding features of the MC1458 and, in addition, offers three times the unity gain bandwidth of the industry standard.

- 2.0 MHz Unity Gain Bandwidth Guaranteed
- Internally Compensated
- Short Circuit Protection
- Gain and Phase Match Between Amplifiers
- Low Power Consumption

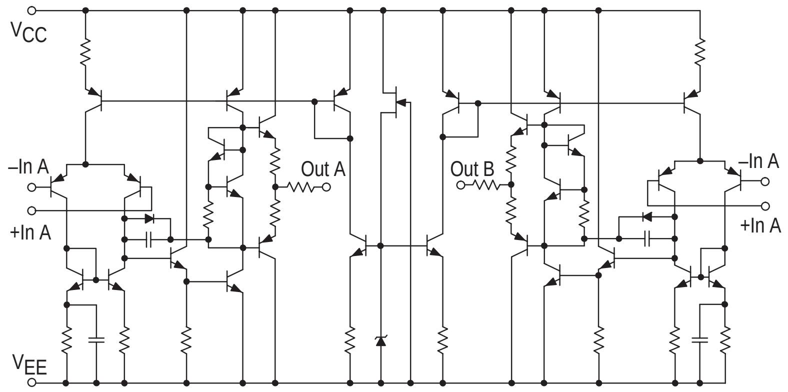
This MCT–prefixed device is intended to be a possible replacement for the similar device with the MC–prefix. Because the MCT device originates from different source material, there may be subtle differences in typical parameter values or characteristic curves. Due to the diversity of potential applications, Motorola can not assure identical performance in all circuits. Motorola recommends that the customer qualify the MCT–prefixed device in each potential application.

MAXIMUM RATINGS (T_A = +25°C, unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltages	V_{CC} V_{EE}	+18 –18	Vdc
Input Differential Voltage	V_{ID}	±30	V
Input Common Mode Voltage (Note 1)	V_{ICM}	±15	V
Output Short Circuit Duration (Note 2)	t_{SC}	Continuous	
Ambient Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	–55 to +125	°C
Junction Temperature	T_J	150	°C

NOTES: 1. For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.
2. Short circuit may be to ground or either supply.

Representative Schematic Diagram

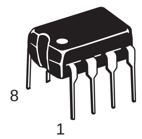


This device contains 29 active transistors.

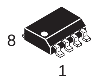
CAUTION: These devices do not have internal ESD protection circuitry and are rated as CLASS 1 devices per the ESD test method in Mil–Std–833D. They should be handled using standard ESD prevention methods to avoid damage to the device.

DUAL WIDE BANDWIDTH OPERATIONAL AMPLIFIER

SEMICONDUCTOR TECHNICAL DATA

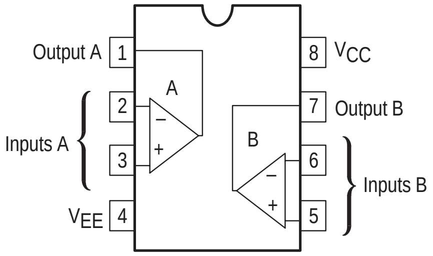


P1 SUFFIX
PLASTIC PACKAGE
CASE 626



D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MCT4558CD	T_A = 0° to +70°C	SO–8
MCT4558CPI		Plastic DIP

FREQUENCY CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = –15 V, T_A = 25°C)

Characteristic	Symbol	Min	Typ	Max	Unit
Unity Gain Bandwidth	BW	2.0	2.8	—	MHz

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V, V_{EE} = –15 V, T_A = 25°C, unless otherwise noted.)

Input Offset Voltage (R_S ≤ 10 kΩ)	V_{IO}	—	2.0	6.0	mV
Input Offset Current	I_{IO}	—	20	200	nA
Input Bias Current (Note 1)	I_{IB}	—	80	500	nA
Common Mode Input Voltage Range	V_{ICR}	±12	±13	—	V
Large Signal Voltage Gain (V_O = ±10 V, R_L = 2.0 kΩ)	A_{VOL}	20	200	—	V/mV
Common Mode Rejection (R_S ≤ 10 kΩ)	CMR	70	90	—	dB
Supply Voltage Rejection Ratio (R_S ≤ 10 kΩ)	PSRR	—	30	150	µV/V
Output Voltage Swing	V_O				
(R_L ≥ 10 kΩ)		±12	±14	—	V
(R_L ≥ 2.0 kΩ)		±10	±13	—	
Output Short Circuit Current	I_{SC}	10	20	75	mA
Supply Currents (Both Amplifiers)	I_D	—	4.0	5.6	mA
Power Consumption (Both Amplifiers)	P_C	—	70	170	mW
Transient Response (Unity Gain)					
(V_I = 20 mV, R_L ≥ 2.0 kΩ, C_L ≤ 100 pF) Rise Time	t_{TLH}	—	0.3	—	µs
(V_I = 20 mV, R_L ≥ 2.0 kΩ, C_L ≤ 100 pF) Overshoot	os	—	15	—	%
(V_I = 10 V, R_L ≥ 2.0 kΩ, C_L ≤ 100 pF) Slew Rate	SR	1.0	1.8	—	V/µs

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = –15 V, T_A = T_{high} to T_{low}, [Note 2] unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Offset Voltage (R_S ≤ 10 kΩ)	V_{IO}	—	—	7.5	mV
Input Offset Current (T_A = 0° to +70°C)	I_{IO}	—	—	300	nA
Input Bias Current (T_A = 0° to +70°C)	I_{IB}	—	—	800	nA
Large Signal Voltage Gain (V_O = ±10 V, R_L = 2.0 kΩ)	A_{VOL}	15	—	—	V/mV
Output Voltage Swing	V_O				V
(R_L ≥ 10 kΩ)		±12	±14	—	
(R_L ≥ 2.0 kΩ)		±10	±13	—	
Supply Currents (Both Amplifiers)	I_D				mA
(T_A = T_{high})		—	—	5.0	
(T_A = T_{low})		—	—	6.7	
Power Consumption (Both Amplifiers)	P_C				mW
(T_A = T_{high})		—	—	150	
(T_A = T_{low})		—	—	200	

NOTES: 1. I_{IB} is out of the amplifier due to PNP input transistors.
2. T_{low} = 0°C T_{high} = +70°C

Figure 1. Power Bandwidth (Large Signal Swing versus Frequency)

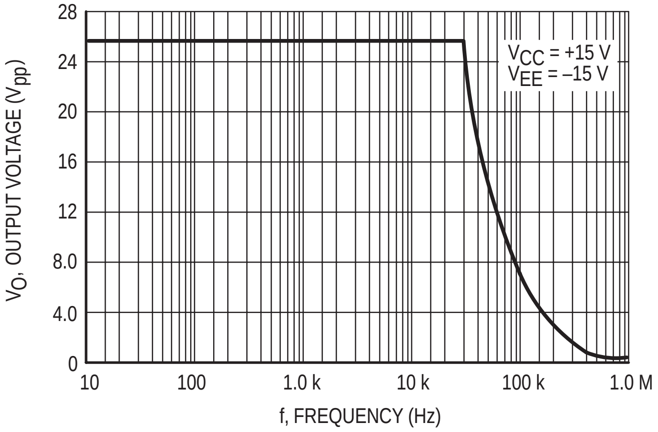


Figure 2. Maximum Output Voltage Swing versus Load Resistance

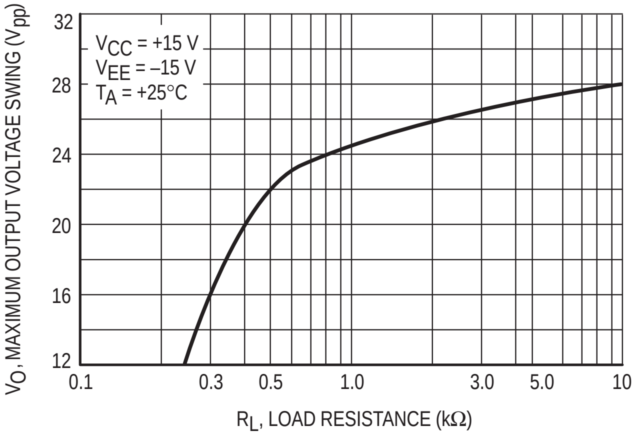


Figure 3. Equivalent Input Noise Voltage versus Frequency

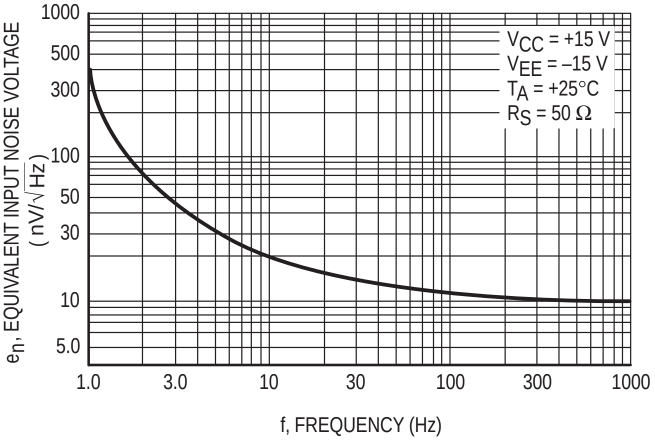


Figure 4. Input Bias Current versus Ambient Temperature

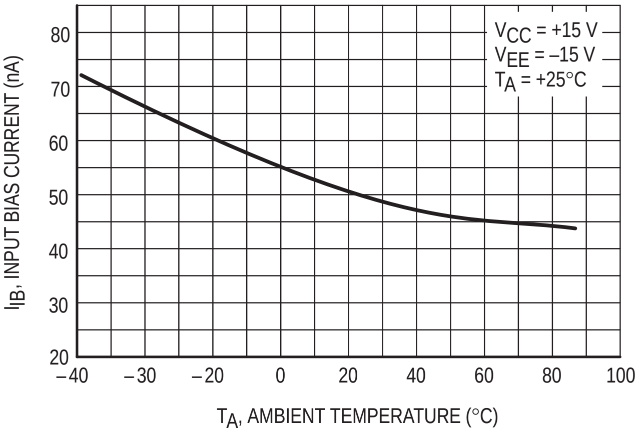


Figure 5. Voltage Gain and Phase versus Frequency

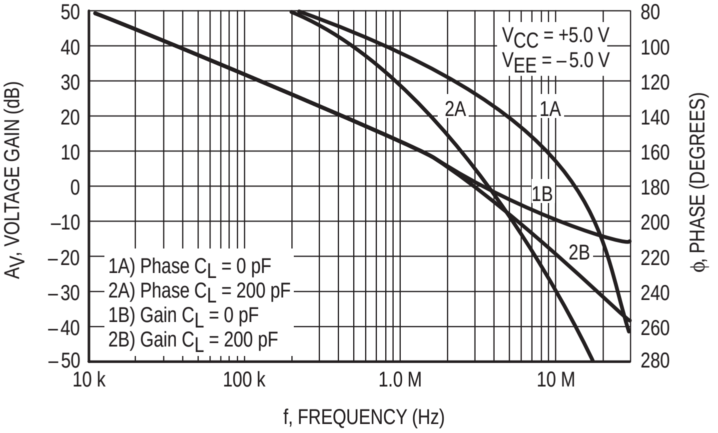
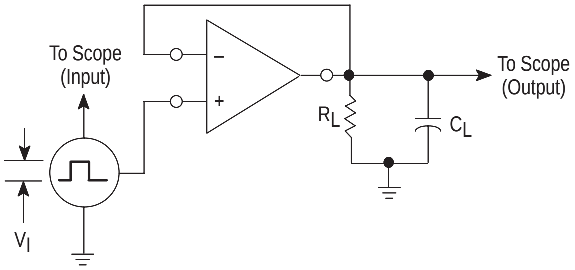


Figure 6. Transient Response Test Circuit



MOTOROLA

MC4741C

Differential Input Operational Amplifier

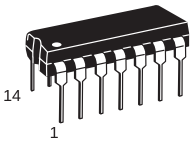
The MC4741C is a true quad MC1741. Integrated on a single monolithic chip are four independent, low power operational amplifiers which have been designed to provide operating characteristics identical to those of the industry standard MC1741, and can be applied with no change in circuit performance.

The MC4741C can be used in applications where amplifier matching or high packing density is important. Other applications include high impedance buffer amplifiers and active filter amplifiers.

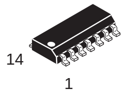
- Each Amplifier is Functionally Equivalent to the MC1741
- Class AB Output Stage Eliminates Crossover Distortion
- True Differential Inputs
- Internally Frequency Compensated
- Short Circuit Protection
- Low Power Supply Current (0.6 mA/Amplifier)

DIFFERENTIAL INPUT OPERATIONAL AMPLIFIER
(QUAD MC1741)

SEMICONDUCTOR TECHNICAL DATA

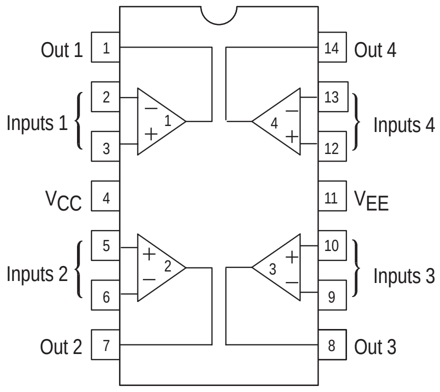


P SUFFIX
PLASTIC PACKAGE
CASE 646



D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO–14)

PIN CONNECTIONS

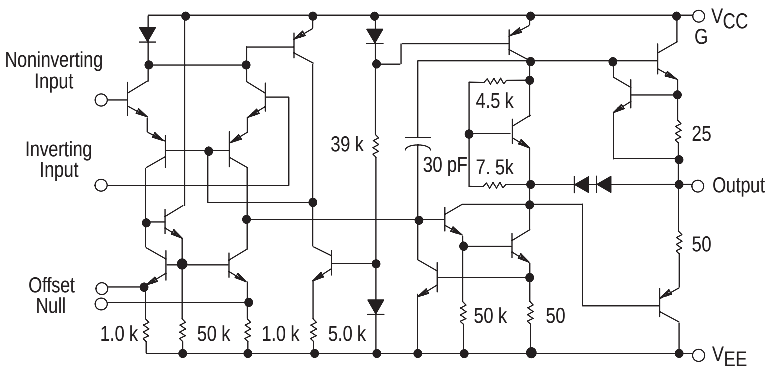


(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC4741CD	T_A = 0° to +70°C	SO–14
MC4741CP		Plastic DIP

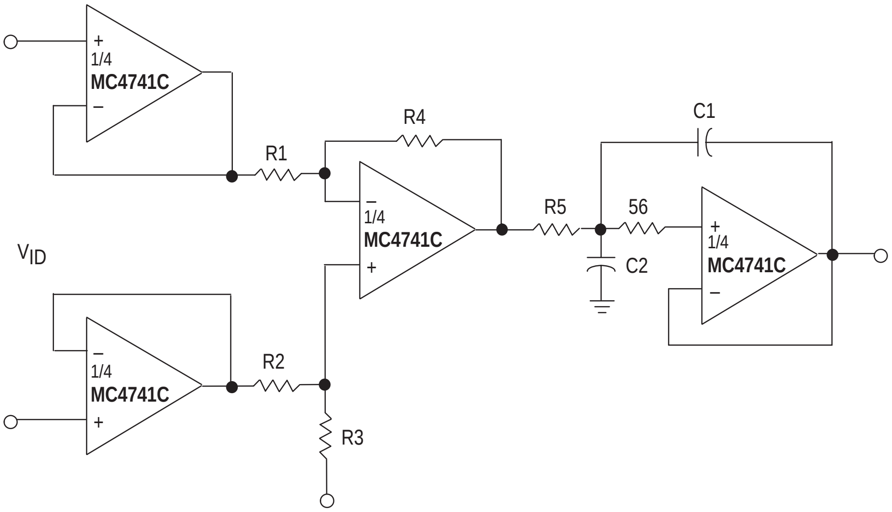
Representative Schematic Diagram
(1/4 of Circuit Shown)



MAXIMUM RATINGS (T_A = +25°C, unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC} V_{EE}	+18 –18	Vdc
Input Differential Voltage	V_{ID}	±36	V
Input Common Mode Voltage	V_{ICM}	±18	V
Output Short Circuit Duration	t_{SC}	Continuous	
Operating Ambient Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	–55 to +125	°C
Junction Temperature	T_J	150	°C

High Impedance Instrumentation Buffer/Filter



ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = –15 V, T_A = 25°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Offset Voltage (R_S ≤ 10 k)	V_{IO}	–	2.0	6.0	mV
Input Offset Current	I_{IO}	–	20	200	nA
Input Bias Current	I_{IB}	–	80	500	nA
Input Resistance	r_i	0.3	2.0	–	MΩ
Input Capacitance	C_i	–	1.4	–	pF
Offset Voltage Adjustment Range	V_{IOR}	–	±15	–	mV
Common Mode Input Voltage Range	V_{ICR}	±12	±13	–	V
Large Signal Voltage Gain (V_O = ±10 V, R_L ≥ 2.0 k)	A_V	20	200	–	V/mV
Output Resistance	r_o	–	75	–	Ω
Common Mode Rejection (R_S ≤ 10 k)	CMR	70	90	–	dB
Supply Voltage Rejection Ratio (R_S ≤ 10 k)	PSRR	–	30	150	µV/V
Output Voltage Swing	V_O				V
(R_L ≥ 10 k)		±12	±14	–	
(R_L ≥ 2 k)		±10	±13	–	
Output Short Circuit Current	I_{SC}	–	20	–	mA
Supply Current – (All Amplifiers)	I_D	–	3.5	7.0	mA
Power Consumption (All Amplifiers)	P_C	–	105	210	mW
Transient Response (Unity Gain – Non–Inverting)					
(V_I = 20 mV, R_L ≥ 2 kΩ, C_L ≤ 100 pF) Rise Time	t_{TLH}	–	0.3	–	µs
(V_I = 20 mV, R_L ≥ 2 kΩ, C_L ≤ 100 pF) Overshoot	os	–	15	–	%
(V_I = 10 V, R_L ≥ 2 kΩ, C_L ≤ 100 pF) Slew Rate	SR	–	0.5	–	V/µs

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = –15 V, T_A = * T_{high} to T_{low}, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Offset Voltage (R_S ≤ 10 kΩ)	V_{IO}	–	–	7.5	mV
Input Offset Current (T_A = 0° to + 70°C)	I_{IO}	–	–	300	nA
Input Bias Current (T_A = 0° to + 70°C)	I_{IB}	–	–	800	nA
Large Signal Voltage Gain (R_L ≥ 2k, V_{OUT} = ±10 V)	A_V	15	–	–	V/mV
Output Voltage Swing (R_L ≥ 2 k)	V_O	±10	±13	–	V

* T_{high} = 70°C T_{low} = –0°C

Figure 1. Power Bandwidth (Large Signal Swing versus Frequency)

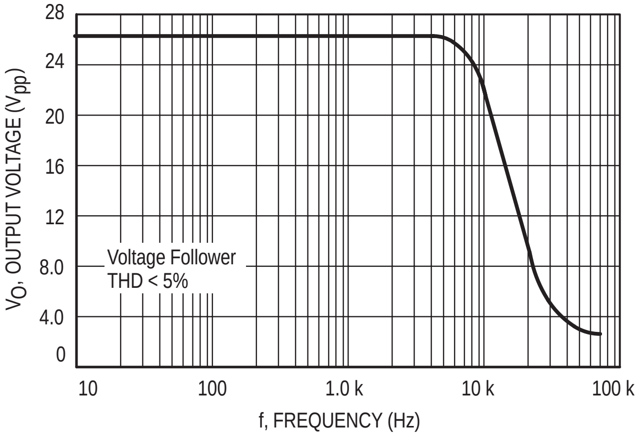


Figure 2. Open Loop Frequency Response

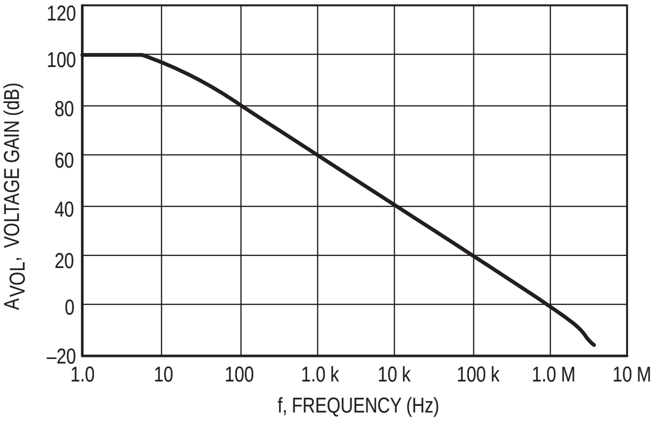


Figure 3. Positive Output Voltage Swing versus Load Resistance

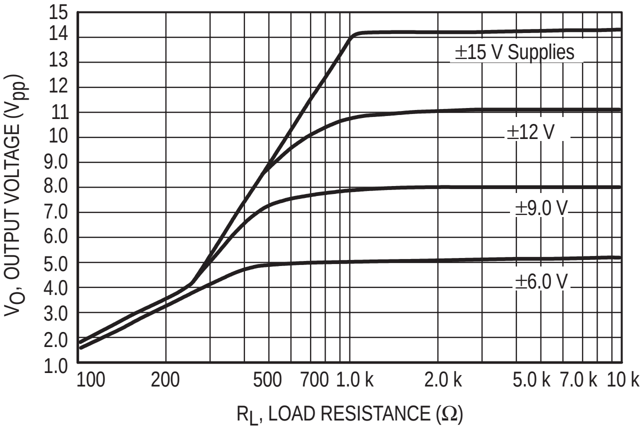


Figure 4. Negative Output Voltage Swing versus Load Resistance

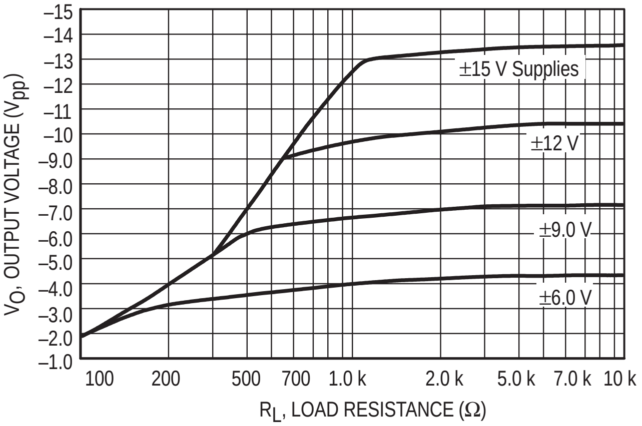


Figure 5. Output Voltage Swing versus Load Resistance (Single Supply Operation)

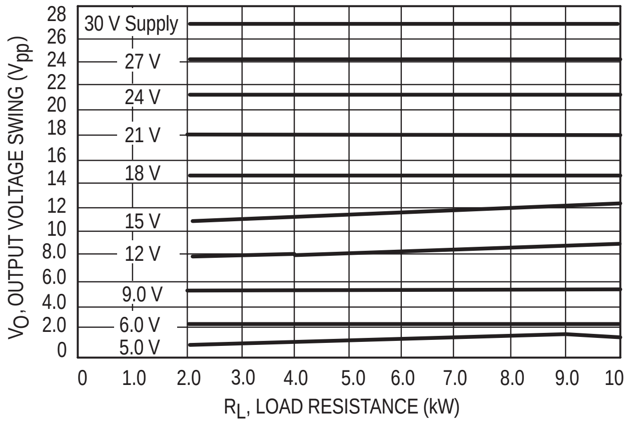


Figure 6. Noninverting Pulse Response

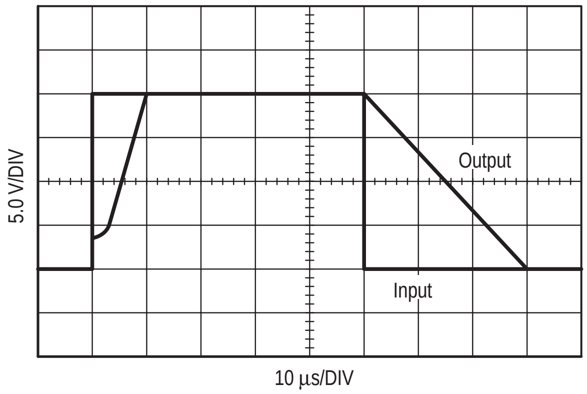


Figure 7. Bi–Quad Filter

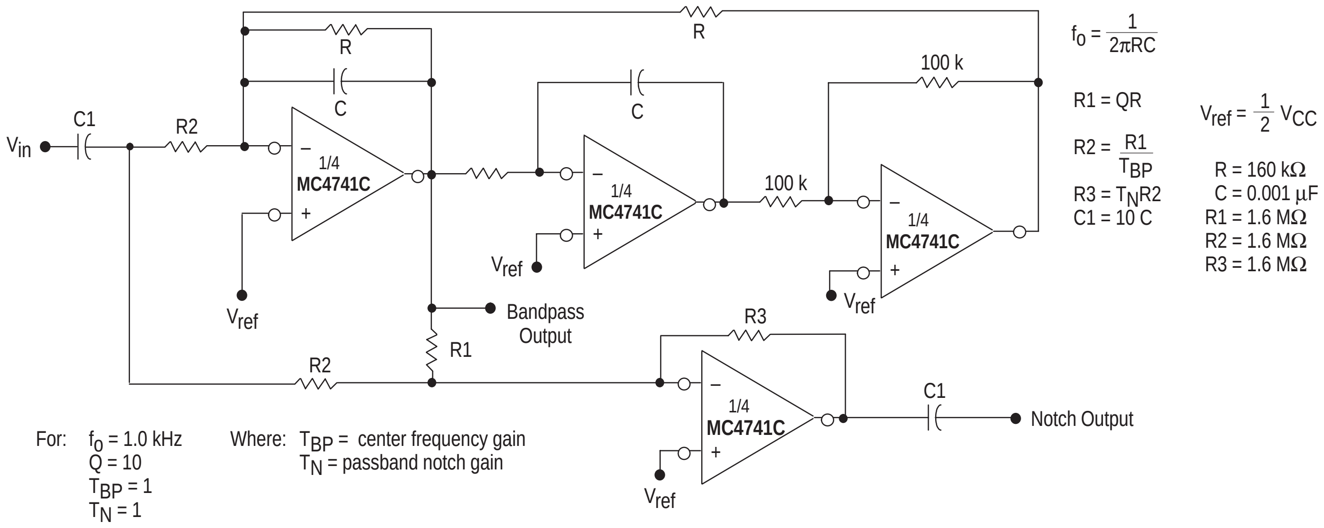


Figure 8. Open Loop Voltage Gain versus Supply Voltage

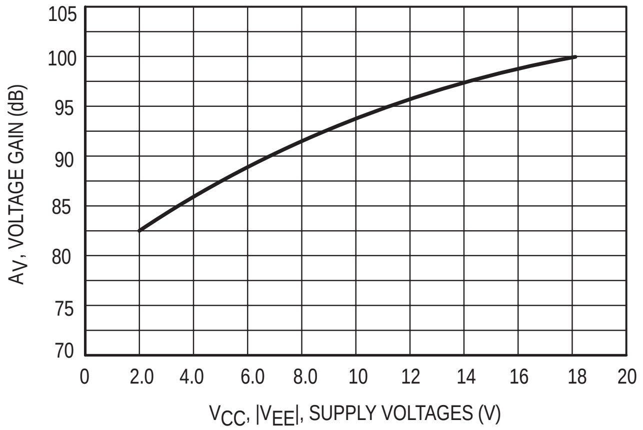


Figure 9. Transient Response Test Circuit

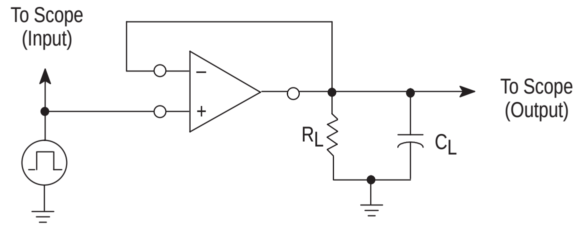
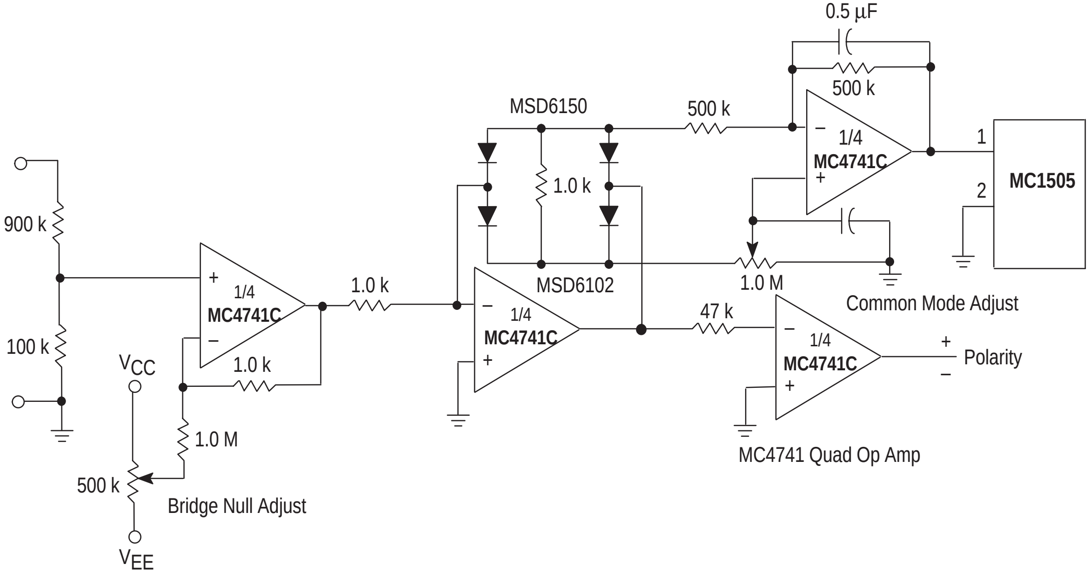


Figure 10. Absolute Value DVM Front End



MOTOROLA

MC33076

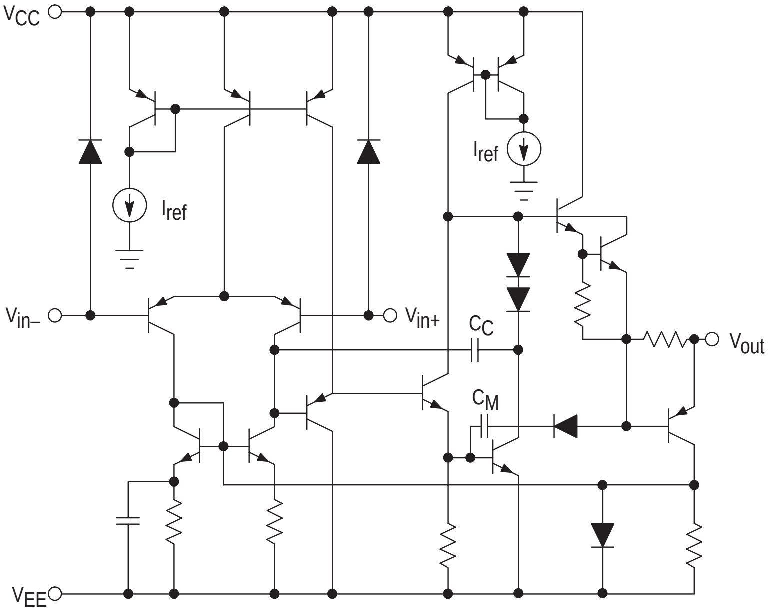
Dual High Output Current, Low Power, Low Noise Bipolar Operational Amplifier

The MC33076 operational amplifier employs bipolar technology with innovative high performance concepts for audio and industrial applications. This device uses high frequency PNP input transistors to improve frequency response. In addition, the amplifier provides high output current drive capability while minimizing the drain current. The all NPN output stage exhibits no deadband crossover distortion, large output voltage swing, excellent phase and gain margins, low open loop high frequency output impedance and symmetrical source and sink AC frequency performance.

The MC33076 is tested over the automotive temperature range and is available in an 8–pin SOIC package (D suffix) and in both the standard 8 pin DIP and 16–pin DIP packages for high power applications.

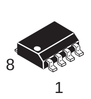
- 100 Ω Output Drive Capability
- Large Output Voltage Swing
- Low Total Harmonic Distortion
- High Gain Bandwidth: 7.4 MHz
- High Slew Rate: 2.6 V/µs
- Dual Supply Operation: ±2.0 V to ±18 V
- High Output Current: ISC = 250 mA typ
- Similar Performance to MC33178

Equivalent Circuit Schematic
(Each Amplifier)

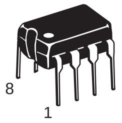


DUAL HIGH OUTPUT CURRENT OPERATIONAL AMPLIFIER

SEMICONDUCTOR TECHNICAL DATA

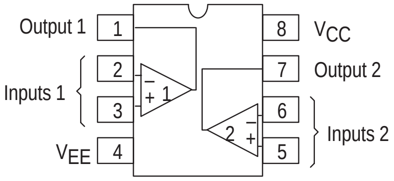


D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

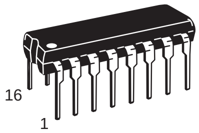


P1 SUFFIX
PLASTIC PACKAGE
CASE 626

PIN CONNECTIONS

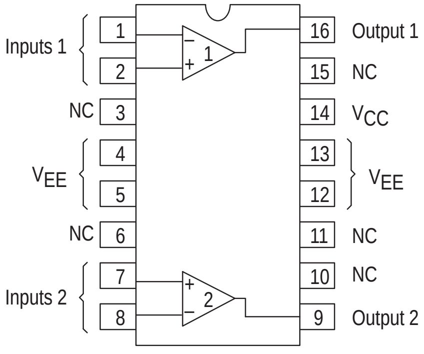


(8 Pin Pkg, Top View)



P2 SUFFIX
PLASTIC PACKAGE
CASE 648C
DIP (12+2+2)

PIN CONNECTIONS



(16 Pin Pkg, Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC33076D	T_A = –40° to +85°C	SO–8
MC33076P1		Plastic DIP
MC33076P2		Power Plastic

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage (Note 2)	V_{CC} to V_{EE}	+36	V
Input Differential Voltage Range	V_{IDR}	(Note 1)	V
Input Voltage Range	V_{IR}	(Note 1)	V
Output Short Circuit Duration (Note 2)	t_{SC}	5.0	sec
Maximum Junction Temperature	T_J	+150	°C
Storage Temperature	T_{stg}	–60 to +150	°C
Maximum Power Dissipation	P_D	(Note 2)	mW

NOTES: 1. Either or both input voltages should not exceed V_{CC} or V_{EE}.
2. Power dissipation must be considered to ensure maximum junction temperature (T_J) is not exceeded (see power dissipation performance characteristic, Figure 1). See applications section for further information.

DC ELECTRICAL CHARACTERICISTICS (V_{CC} = +15 V, V_{EE} = –15 V, T_A = 25°C, unless otherwise noted.)

Characteristics	Figure	Symbol	Min	Typ	Max	Unit
Input Offset Voltage (R_S = 50 Ω, V_{CM} = 0 V) (V_S = ±2.5 V to ±15 V) T_A = +25°C T_A = –40° to +85°C	2	$\lvert V_{IO}\rvert$	 — —	 0.5 0.5	 4.0 5.0	mV
Input Offset Voltage Temperature Coefficient (R_S = 50 Ω, V_{CM} = 0 V) T_A = –40° to +85°C		$\Delta V_{IO}/\Delta T$	 —	 2.0	 —	µV/°C
Input Bias Current (V_{CM} = 0 V) T_A = +25°C T_A = –40° to +85°C	3, 4	I_{IB}	 — —	 100 —	 500 600	nA
Input Offset Current (V_{CM} = 0 V) T_A = +25°C T_A = –40° to +85°C		$\lvert I_{IO}\rvert$	 — —	 5.0 —	 70 100	nA
Common Mode Input Voltage Range	5	V_{ICR}	–13	–14 +14	 13	V
Large Signal Voltage Gain (V_O = –10 V to +10 V) (T_A = +25°C) R_L = 100 Ω R_L = 600 Ω (T_A = –40° to +85°C) R_L = 600 Ω	6	A_{VOL}	 25 50 25	 — 200 —	 — — —	kV/V
Output Voltage Swing (V_{ID} = ±1.0 V) (V_{CC} = +15 V, V_{EE} = –15 V) R_L = 100 Ω R_L = 100 Ω R_L = 600 Ω R_L = 600 Ω (V_{CC} = +2.5 V, V_{EE} = –2.5 V) R_L = 100 Ω R_L = 100 Ω	7, 8, 9	 V_{O+} V_{O-} V_{O+} V_{O-} V_{O+} V_{O-}	 10 — 13 — 1.2 —	 +11.7 –11.7 +13.8 –13.8 +1.66 –1.74	 — –10 — –13 — –1.2	V
Common Mode Rejection (V_{in} = ±13 V)	10	CMR	80	116	—	dB
Power Supply Rejection (V_{CC}/V_{EE} = +15 V/–15 V, +5.0 V/–15 V, +15 V/–5.0 V)	11	PSR	 80	 120	 —	dB

DC ELECTRICAL CHARACTERICISTICS (V_{CC} = +15 V, V_{EE} = –15 V, T_A = 25°C, unless otherwise noted.)

Characteristics	Figure	Symbol	Min	Typ	Max	Unit
Output Short Circuit Current (V_{ID} = ±1.0 V Output to Gnd)	12, 13	I_{SC}				mA
(V_{CC} = +15 V, V_{EE} = –15 V)						
Source			190	+250	—	
Sink			—	–280	–215	
(V_{CC} = +2.5 V, V_{EE} = –2.5 V)						
Source			63	+94	—	
Sink			—	–80	–46	
Power Supply Current per Amplifier (V_O = 0 V)	14	I_D				mA
(V_S = ±2.5 V to ±15 V)						
T_A = +25°C			—	2.2	2.8	
T_A = –40° to +85°C			—	—	3.3	

AC ELECTRICAL CHARACTERICISTICS (V_{CC} = +15 V, V_{EE} = –15 V, T_A = 25°C, unless otherwise noted.)

Characteristics	Figure	Symbol	Min	Typ	Max	Unit
Slew Rate (V_{in} = –10 V to +10 V, R_L = 100 Ω, C_L = 100 pF, A_V = +1)	15	SR	1.2	2.6	—	V/µs
Gain Bandwidth Product (f = 20 kHz)	16	GBW	4.0	7.4	—	MHz
Unity Gain Frequency (Open Loop) (R_L = 600 Ω, C_L = 0 pF)	—	f_U	—	3.5	—	MHz
Gain Margin (R_L = 600 Ω, C_L = 0 pF)	19, 20	A_m	—	15	—	dB
Phase Margin (R_L = 600 Ω, C_L = 0 pF)	19, 20	$\varnothing_m$	—	52	—	Deg
Channel Separation (f = 100 Hz to 20 kHz)	21	CS	—	–120	—	dB
Power Bandwidth (V_O = 20 V_{pp}, R_L = 600 Ω, THD ≤ 1%)	—	BW_p	—	32	—	kHz
Total Harmonic Distortion (R_L = 600 Ω, V_O = 2.0 V_{pp}, A_V = +1)	22	THD				%
f = 1.0 kHz			—	0.0027	—	
f = 10 kHz			—	0.011	—	
f = 20 kHz			—	0.022	—	
Open Loop Output Impedance (V_O = 0 V, f = 2.5 MHz, A_V = 10)	23	$\|Z_O\|$	—	75	—	Ω
Differential Input Resistance (V_{CM} = 0 V)	—	R_{in}	—	200	—	kΩ
Differential Input Capacitance (V_{CM} = 0 V)	—	C_{in}	—	10	—	pF
Equivalent Input Noise Voltage (R_S = 100 Ω)	24	e_n				nV/$\sqrt{Hz}$
f = 10 Hz			—	7.5		
f = 1.0 kHz			—	5.0	—	
Equivalent Input Noise Current	—	i_n				pA/$\sqrt{Hz}$
f = 10 Hz			—	0.33	—	
f = 1.0 kHz			—	0.15	—	

Figure 1. Maximum Power Dissipation versus Temperature

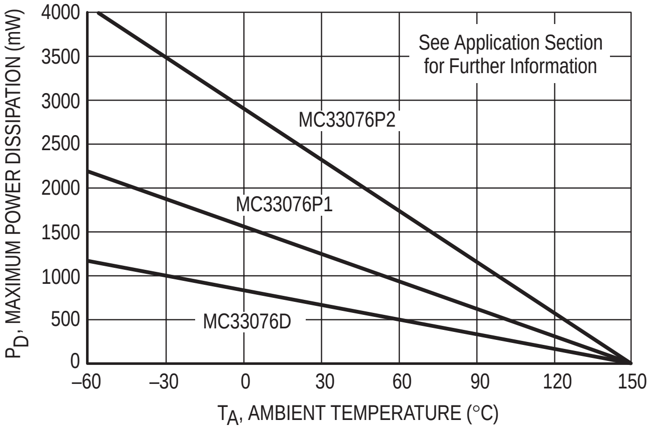


Figure 2. Distribution of Input Offset Voltage

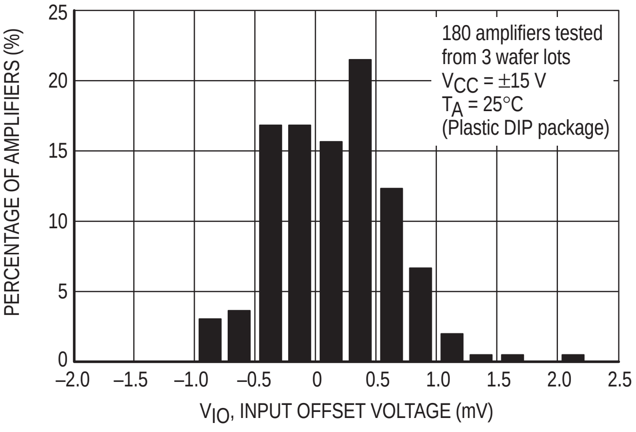


Figure 3. Input Bias Current versus Common Mode Voltage

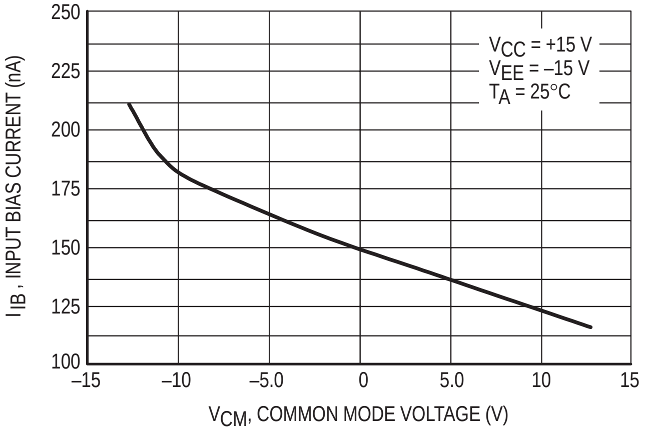


Figure 4. Input Bias Current versus Temperature

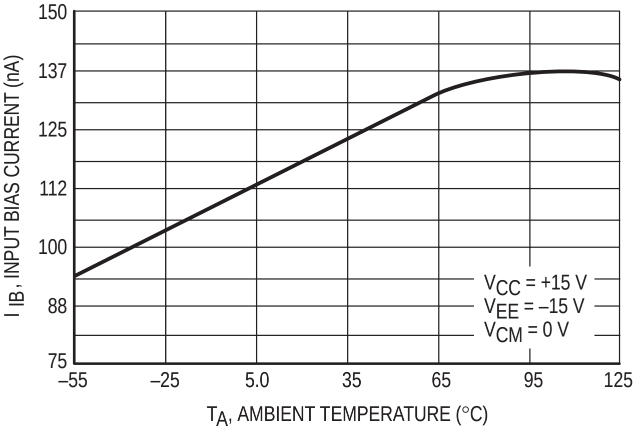


Figure 5. Input Common Mode Voltage Range versus Temperature

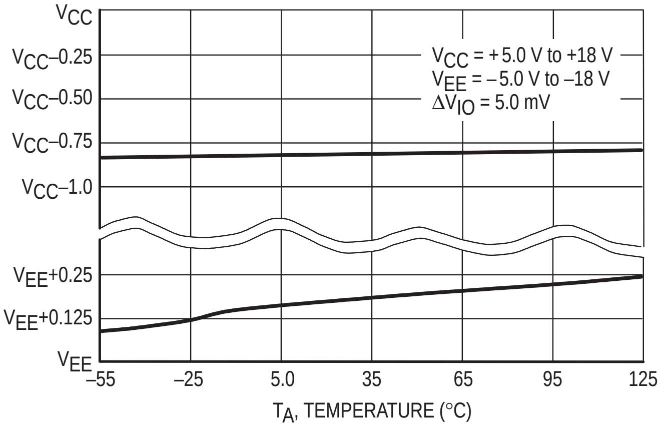


Figure 6. Open Loop Voltage Gain versus Temperature

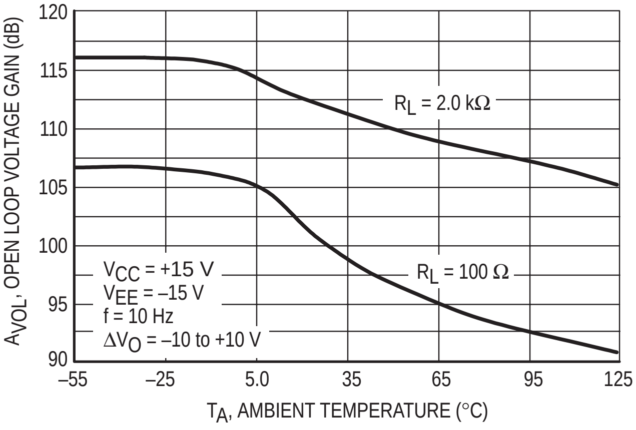


Figure 7. Output Voltage Swing versus Supply Voltage

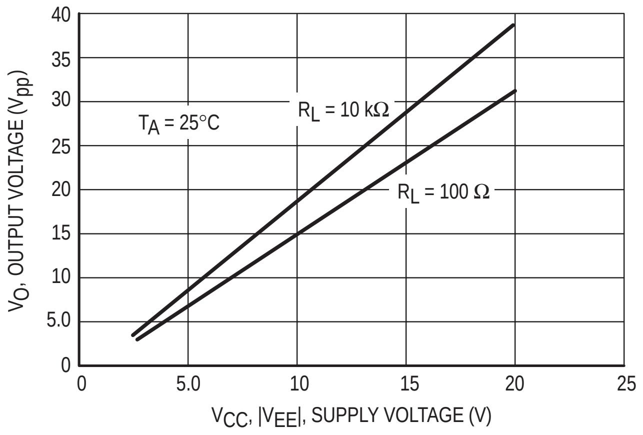


Figure 8. Maximum Peak–to–Peak Output Voltage Swing versus Load Resistance

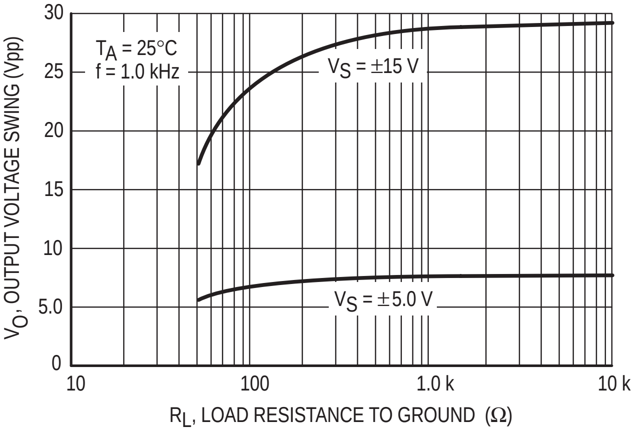


Figure 9. Output Voltage versus Frequency

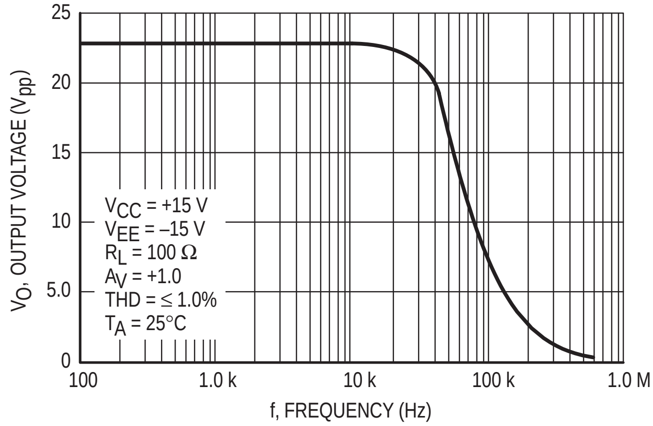


Figure 10. Common Mode Rejection versus Frequency Over Temperature

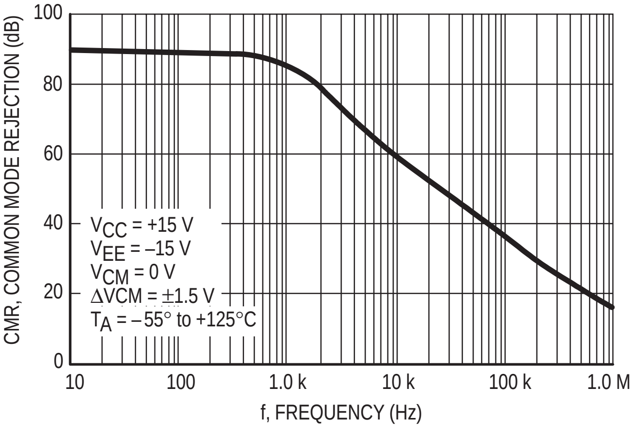


Figure 11. Power Supply Rejection versus Frequency Over Temperature

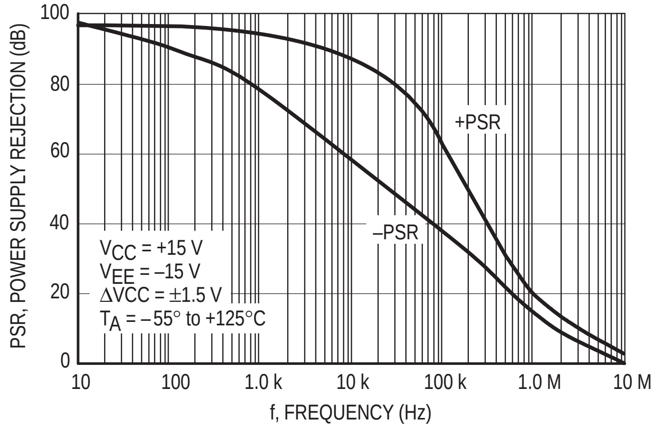


Figure 12. Output Short Circuit Current versus Output Voltage

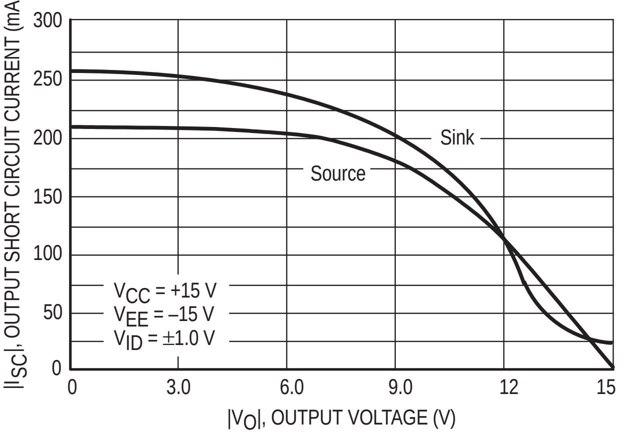


Figure 13. Output Short Circuit Current versus Temperature

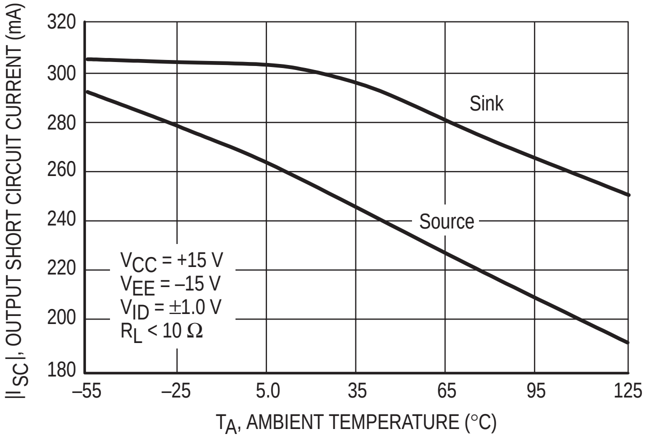


Figure 14. Supply Current versus Supply Voltage with No Load

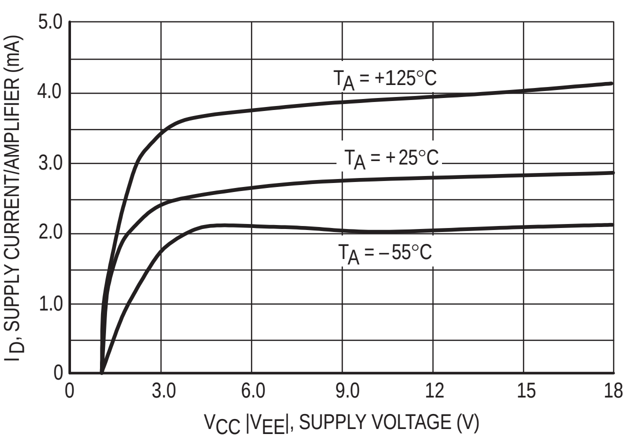


Figure 15. Slew Rate versus Temperature

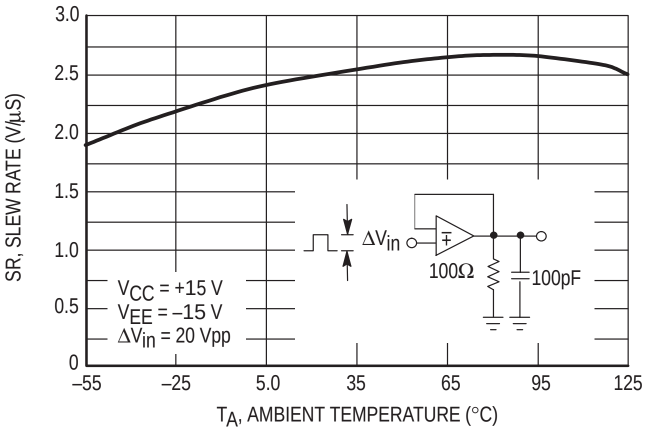


Figure 16. Gain Bandwidth Product versus Temperature

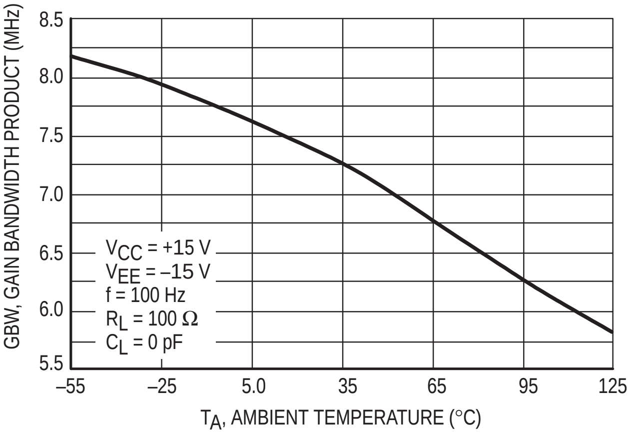


Figure 17. Voltage Gain and Phase versus Frequency

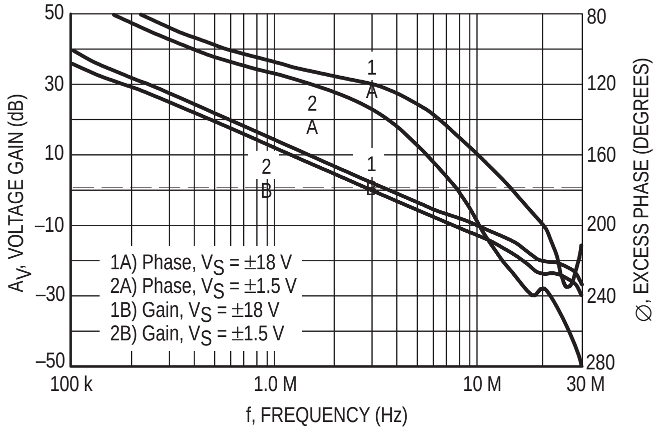


Figure 18. Voltage Gain and Phase versus Frequency

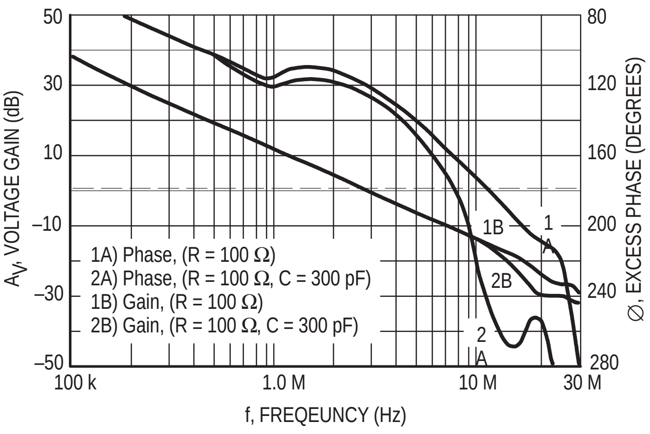


Figure 19. Phase Margin and Gain Margin versus Differential Source Resistance

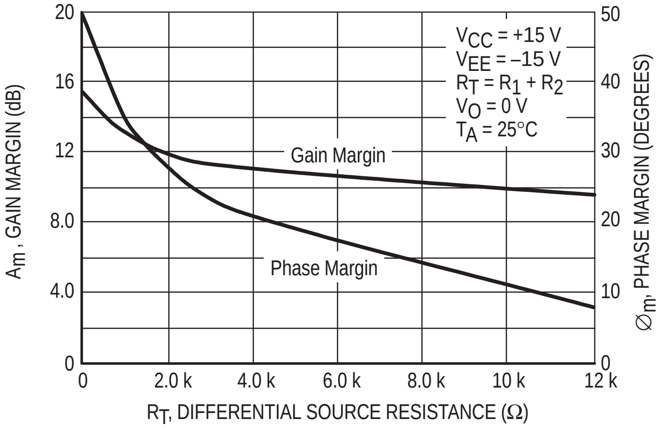


Figure 20. Open Loop Gain Margin and Phase Margin versus Output Load Capacitance

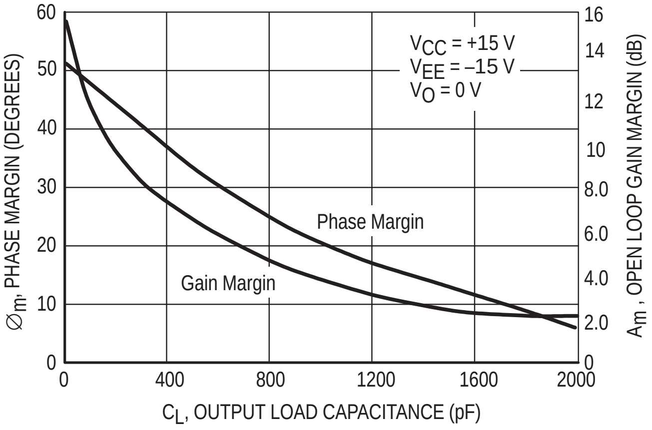


Figure 21. Channel Separation versus Frequency

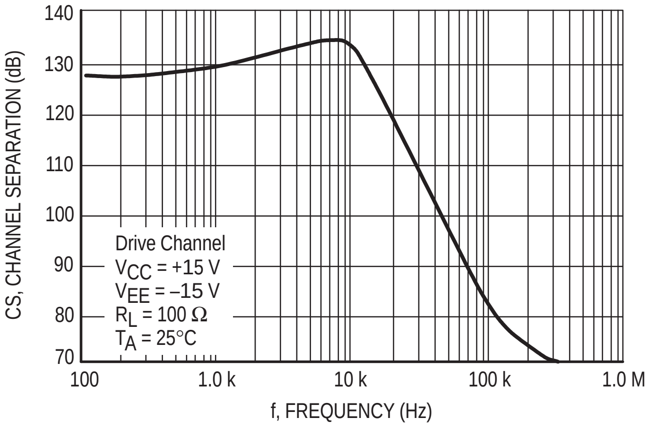


Figure 22. Total Harmonic Distortion versus Frequency

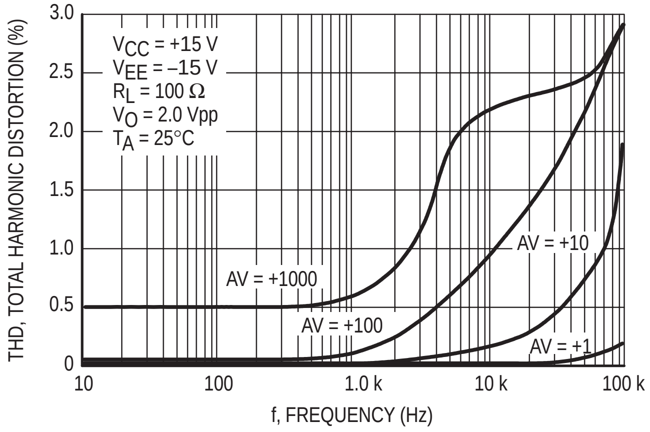


Figure 23. Output Impedance versus Frequency

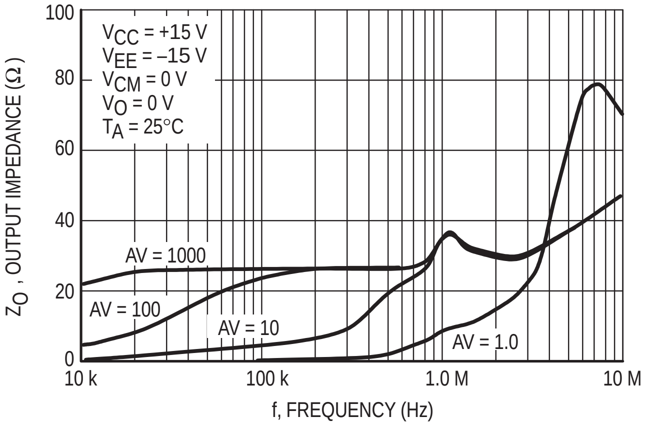


Figure 24. Input Referred Noise Voltage versus Frequency

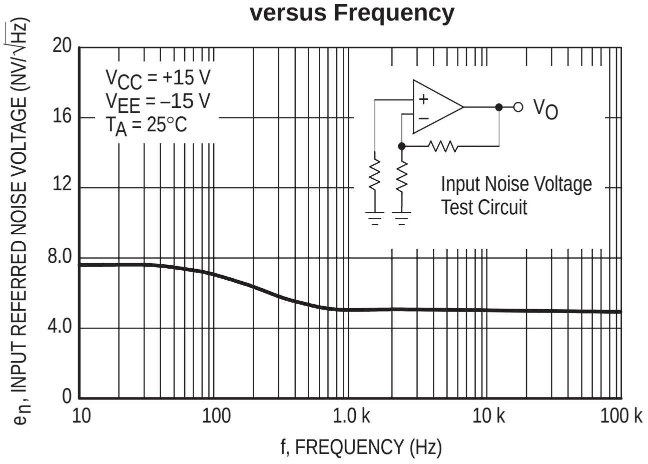


Figure 25. Percent Overshoot versus Load Capacitance

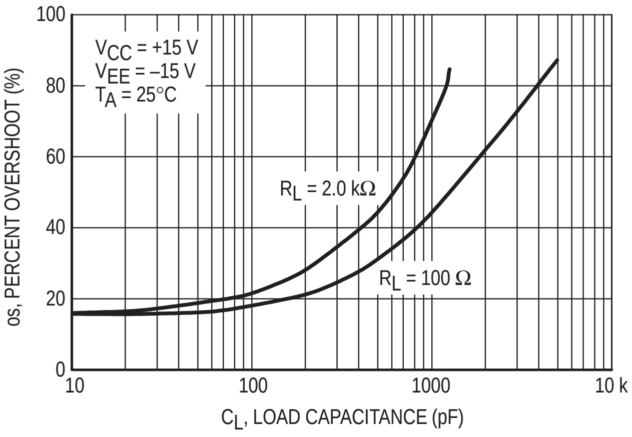
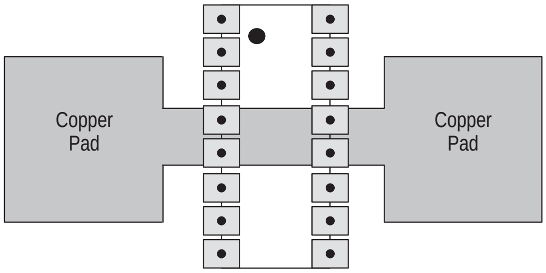


Figure 26. PC Board Heatsink Example



APPLICATIONS INFORMATION

The MC33076 dual operational amplifier is available in the standard 8–pin plastic dual–in–line (DIP) and surface mount packages, and also in a 16–pin batwing power package. To enhance the power dissipation capability of the power package, Pins 4, 5, 12, and 13 are tied together on the leadframe, giving it an ambient thermal resistance of 52°C/W typically, in still air. The junction–to–ambient thermal resistance ($R_{\theta JA}$) can be decreased further by using a copper padb on the printed circuit board (as shown in Figure 26) to draw the heat away from the package. *Care must be taken not to exceed the maximum junction temperature or damage to the device may occur.*

MOTOROLA

MC33077

Dual, Low Noise Operational Amplifier

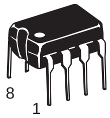
DUAL, LOW NOISE OPERATIONAL AMPLIFIER

SEMICONDUCTOR TECHNICAL DATA

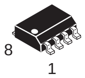
The MC33077 is a precision high quality, high frequency, low noise monolithic dual operational amplifier employing innovative bipolar design techniques. Precision matching coupled with a unique analog resistor trim technique is used to obtain low input offset voltages. Dual–doublet frequency compensation techniques are used to enhance the gain bandwidth product of the amplifier. In addition, the MC33077 offers low input noise voltage, low temperature coefficient of input offset voltage, high slew rate, high AC and DC open loop voltage gain and low supply current drain. The all NPN transistor output stage exhibits no deadband cross–over distortion, large output voltage swing, excellent phase and gain margins, low open loop output impedance and symmetrical source and sink AC frequency performance.

The MC33077 is tested over the automotive temperature range and is available in plastic DIP and SO–8 packages (P and D suffixes).

- Low Voltage Noise: $4.4\ \text{nV}/\sqrt{\text{Hz}}$ @ 1.0 kHz
- Low Input Offset Voltage: 0.2 mV
- Low TC of Input Offset Voltage: 2.0 µV/°C
- High Gain Bandwidth Product: 37 MHz @ 100 kHz
- High AC Voltage Gain: 370 @ 100 kHz
  1850 @ 20 kHz
- Unity Gain Stable: with Capacitance Loads to 500 pF
- High Slew Rate: 11 V/µs
- Low Total Harmonic Distortion: 0.007%
- Large Output Voltage Swing: +14 V to –14.7 V
- High DC Open Loop Voltage Gain: 400 k (112 dB)
- High Common Mode Rejection: 107 dB
- Low Power Supply Drain Current: 3.5 mA
- Dual Supply Operation: ±2.5 V to ±18 V

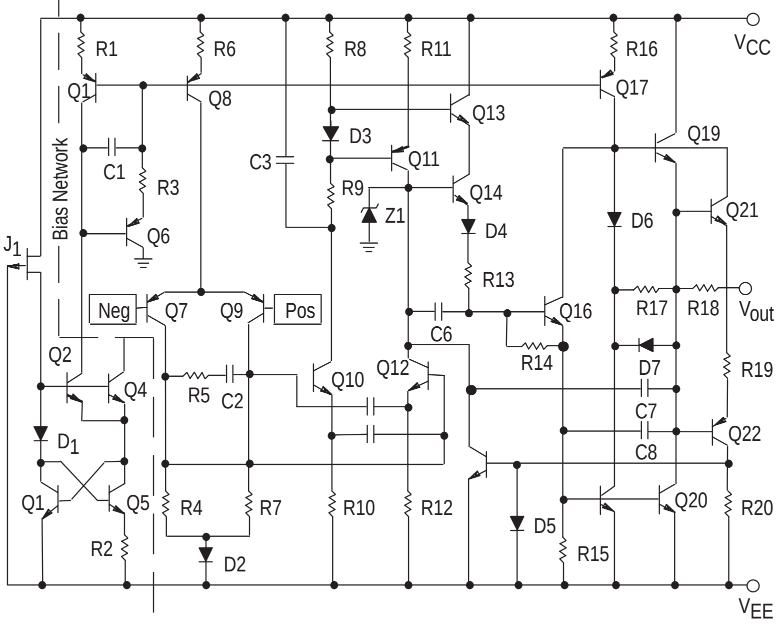


P SUFFIX
PLASTIC PACKAGE
CASE 626

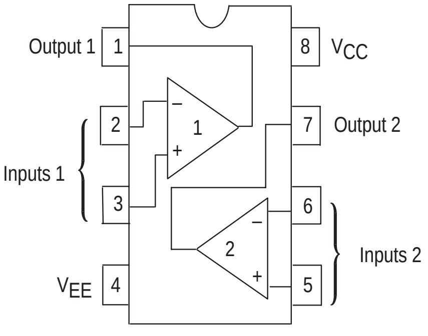


D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

Representative Schematic Diagram (Each Amplifier)



PIN CONNECTIONS



(Dual, Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC33077D	T_A = – 40° to +85°C	SO–8
MC33077P		Plastic DIP

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage (V_{CC} to V_{EE})	V_S	+36	V
Input Differential Voltage Range	V_{IDR}	(Note 1)	V
Input Voltage Range	V_{IR}	(Note 1)	V
Output Short Circuit Duration (Note 2)	t_{SC}	Indefinite	sec
Maximum Junction Temperature	T_J	+150	°C
Storage Temperature	T_{stg}	–60 to +150	°C
Maximum Power Dissipation	P_D	(Note 2)	mW

NOTES: 1. Either or both input voltages should not exceed V_{CC} or V_{EE} (See Applications Information).
2. Power dissipation must be considered to ensure maximum junction temperature (T_J) is not exceeded (See power dissipation performance characteristic, Figure 1).

DC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = –15 V, T_A = 25°C, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Input Offset Voltage (R_S = 10 Ω, V_{CM} = 0 V, V_O = 0 V)	$\|V_{IO}\|$				mV
T_A = +25°C		—	0.13	1.0	
T_A = –40° to +85°C		—	—	1.5	
Average Temperature Coefficient of Input Offset Voltage R_S = 10 Ω, V_{CM} = 0 V, V_O = 0 V, T_A = –40° to +85°C	$\Delta V_{IO}/\Delta T$	—	2.0	—	µV/°C
Input Bias Current (V_{CM} = 0 V, V_O = 0 V)	I_{IB}				nA
T_A = +25°C		—	280	1000	
T_A = –40° to +85°C		—	—	1200	
Input Offset Current (V_{CM} = 0 V, V_O = 0 V)	I_{IO}				nA
T_A = +25°C		—	15	180	
T_A = –40° to +85°C		—	—	240	
Common Mode Input Voltage Range (ΔV_{IO} ,= 5.0 mV, V_O = 0 V)	V_{ICR}	±13.5	±14	—	V
Large Signal Voltage Gain (V_O = ±1.0 V, R_L = 2.0 kΩ)	A_{VOL}				V/V
T_A = +25°C		150 k	400 k	—	
T_A = –40° to +85°C		125 k	—	—	
Output Voltage Swing (V_{ID} = ±1.0 V)					V
R_L = 2.0 kΩ	V_{O+}	+13.0	+13.6	—	
R_L = 2.0 kΩ	V_{O-}	—	–14.1	–13.5	
R_L = 10 kΩ	V_{O+}	+13.4	+14.0	—	
R_L = 10 kΩ	V_{O-}	—	–14.7	–14.3	
Common Mode Rejection (V_{in} = ±13 V)	CMR	85	107	—	dB
Power Supply Rejection (Note 3) V_{CC}/V_{EE} = +15 V/ –15 V to +5.0 V/ –5.0 V	PSR	80	90	—	dB
Output Short Circuit Current (V_{ID} = ±1.0 V, Output to Ground)	I_{SC}				mA
Source		+10	+26	+60	
Sink		–20	–33	+60	
Power Supply Current (V_O = 0 V, All Amplifiers)	I_D				mA
T_A = +25°C		—	3.5	4.5	
T_A = –40° to +85°C		—	—	4.8	

NOTE: 3. Measured with V_{CC} and V_{EE} simultaneously varied.

AC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = –15 V, T_A = 25°C, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Slew Rate (V_{in} = –10 V to +10 V, R_L = 2.0 kΩ, C_L = 100 pF, A_V = +1.0)	SR	8.0	11	—	V/µs
Gain Bandwidth Product (f = 100 kHz)	GBW	25	37	—	MHz
AC Voltage Gain (R_L = 2.0 kΩ, V_O = 0 V)	A_{VO}				V/V
f = 100 kHz		—	370	—	
f = 20 kHz		—	1850	—	
Unity Gain Frequency (Open Loop)	f_U	—	7.5	—	MHz
Gain Margin (R_L = 2.0 kΩ, C_L = 10 pF)	A_m	—	10	—	dB
Phase Margin (R_L = 2.0 kΩ, C_L = 10 pF)	$\varnothing_m$	—	55	—	Degrees
Channel Separation (f = 20 Hz to 20 kHz, R_L = 2.0 kΩ, V_O = 10 V_{pp})	CS	—	–120	—	dB
Power Bandwidth (V_O = 27$_{p–p}$, R_L = 2.0 kΩ, THD ≤ 1%)	BW_p	—	200	—	kHz
Distortion (R_L = 2.0 kΩ)	THD				%
A_V = +1.0, f = 20 Hz to 20 kHz					
V_O = 3.0 V_{rms}		—	0.007	—	
A_V = 2000, f = 20 kHz					
V_O = 2.0 V_{pp}		—	0.215	—	
V_O = 10 V_{pp}		—	0.242	—	
A_V = 4000, f = 100 kHz					
V_O = 2.0 V_{pp}		—	0.3.19	—	
V_O = 10 V_{pp}		—	0.316	—	
Open Loop Output Impedance (V_O = 0 V, f = f_U)	$\|Z_O\|$	—	36	—	Ω
Differential Input Resistance (V_{CM} = 0 V)	R_{in}	—	270	—	kΩ
Differential Input Capacitance (V_{CM} = 0 V)	C_{in}	—	15	—	pF
Equivalent Input Noise Voltage (R_S = 100 Ω)	e_n				nV/$\sqrt{Hz}$
f = 10 Hz		—	6.7	—	
f = 1.0 kHz		—	4.4	—	
Equivalent Input Noise Current (f = 1.0 kHz)	i_n				pA/$\sqrt{Hz}$
f = 10 Hz		—	1.3	—	
f = 1.0 kHz		—	0.6	—	

Figure 1. Maximum Power Dissipation versus Temperature

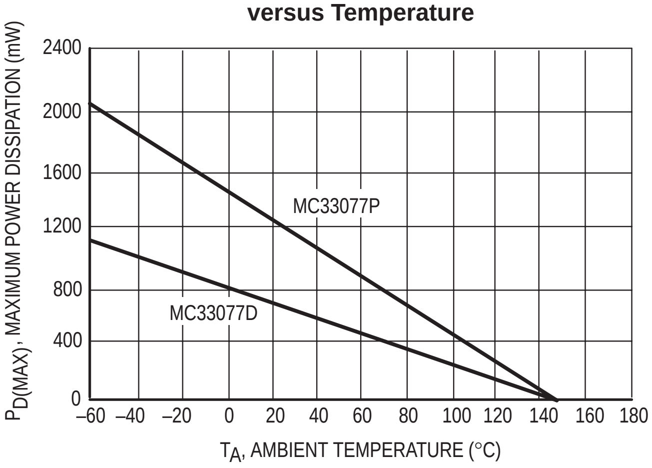


Figure 2. Input Bias Current versus Supply Voltage

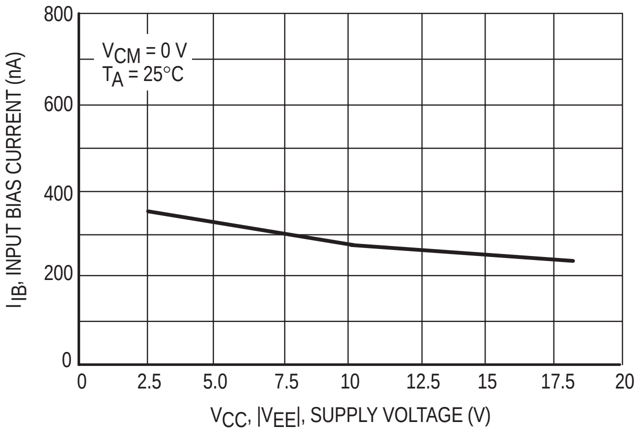


Figure 3. Input Bias Current versus Temperature

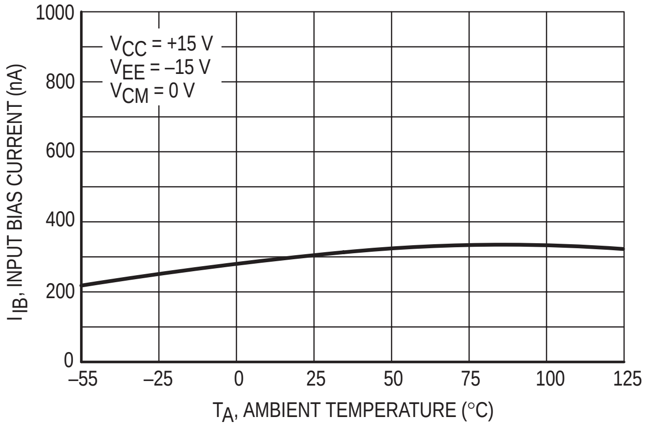


Figure 4. Input Offset Voltage versus Temperature

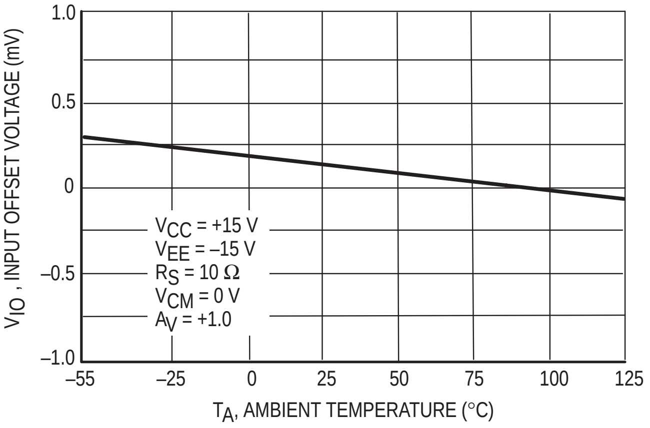


Figure 5. Input Bias Current versus Common Mode Voltage

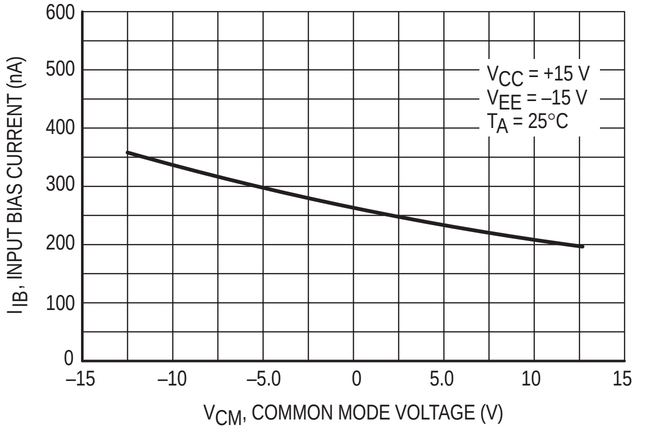


Figure 6. Input Common Mode Voltage Range versus Temperature

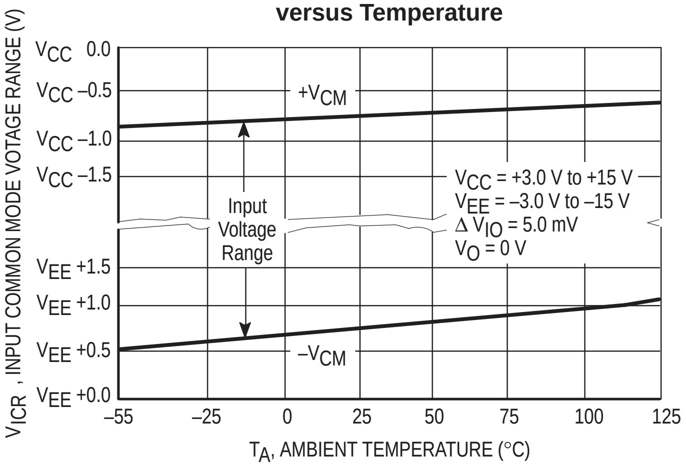


Figure 7. Output Saturation Voltage versus Load Resistance to Ground

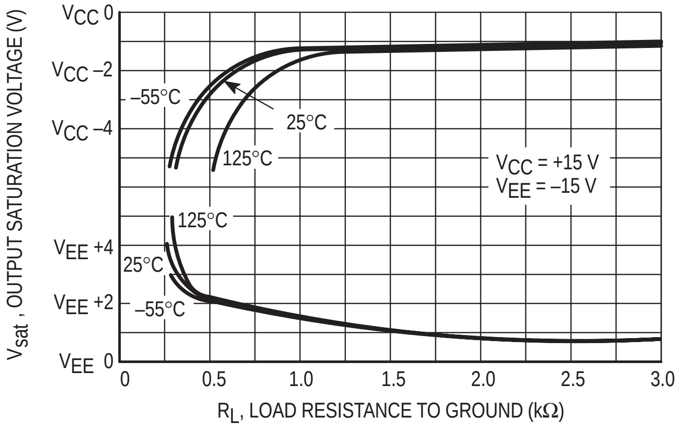


Figure 8. Output Short Circuit Current versus Temperature

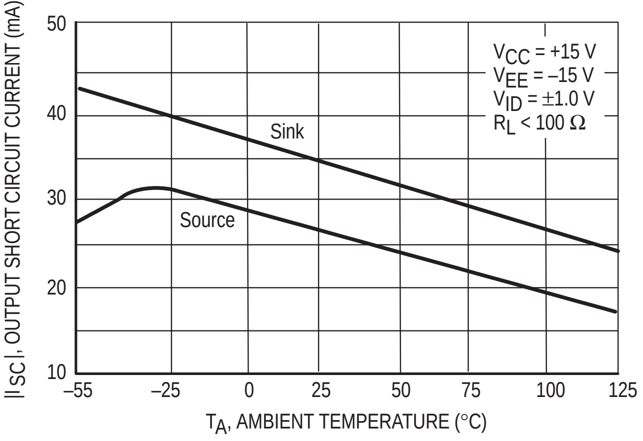


Figure 9. Supply Current versus Temperature

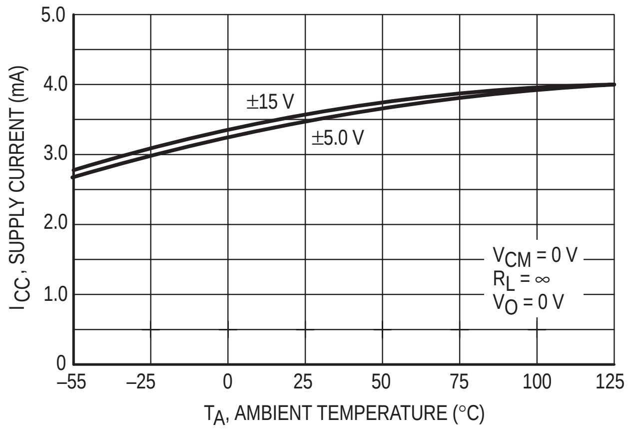


Figure 10. Common Mode Rejection versus Frequency

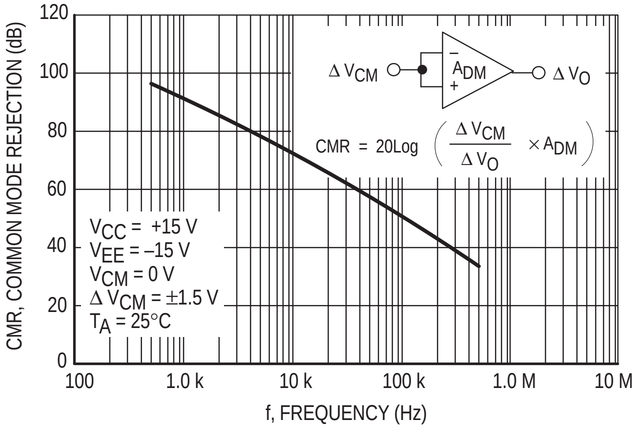


Figure 11. Power Supply Rejection versus Frequency

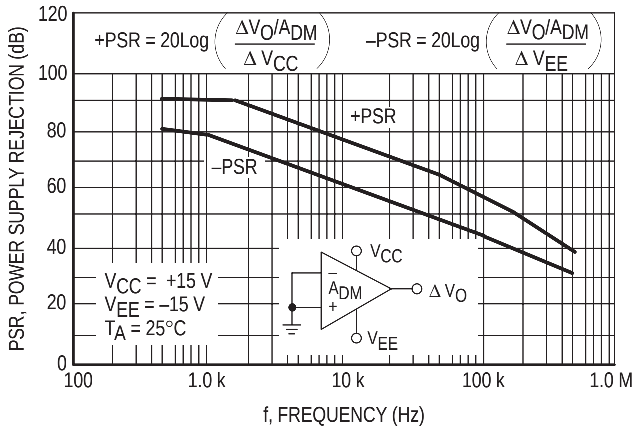


Figure 12. Gain Bandwidth Product versus Supply Voltage

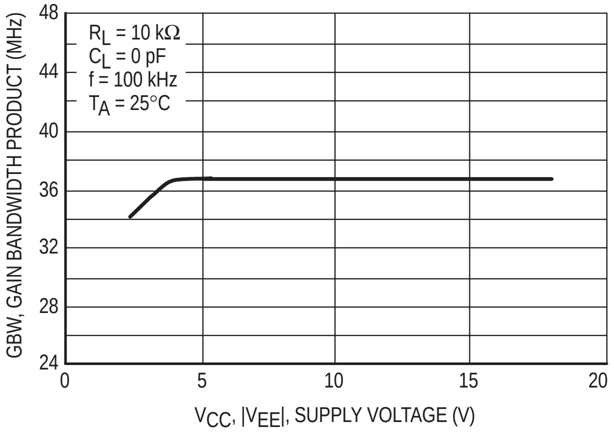


Figure 13. Gain Bandwidth Product versus Temperature

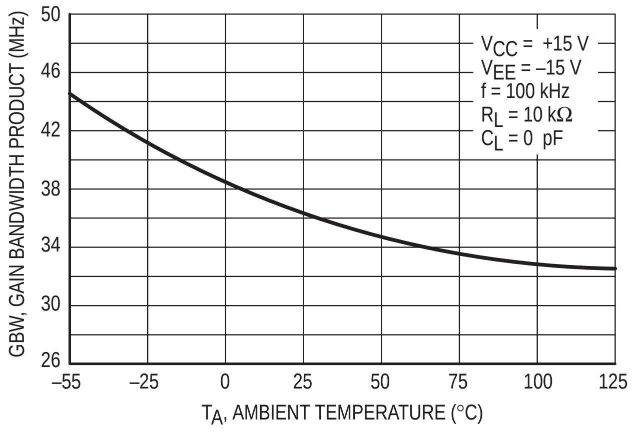


Figure 14. Maximum Output Voltage versus Supply Voltage

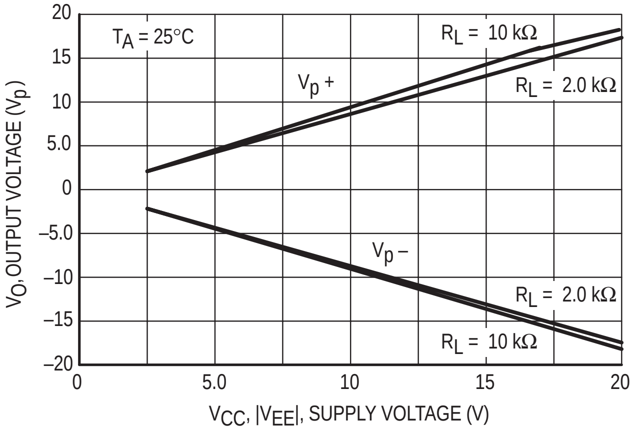


Figure 15. Output Voltage versus Frequency

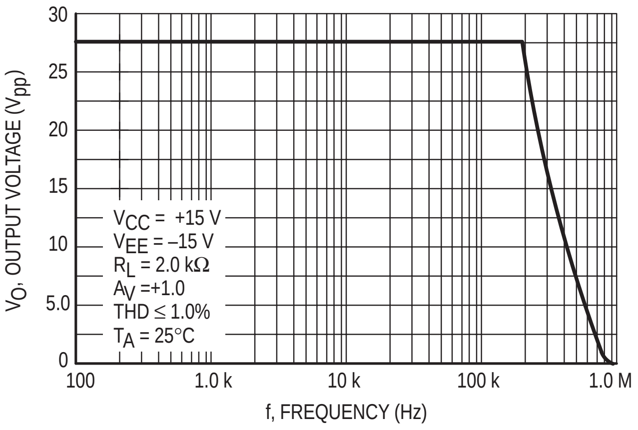


Figure 16. Open Loop Voltage Gain versus Supply Voltage

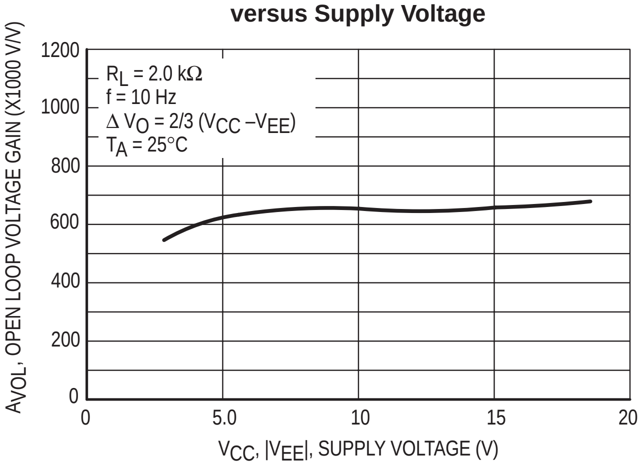


Figure 17. Open Loop Voltage Gain versus Temperature

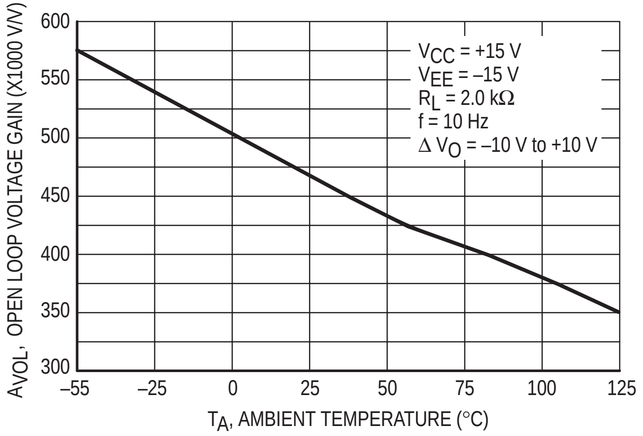


Figure 18. Output Impedance versus Frequency

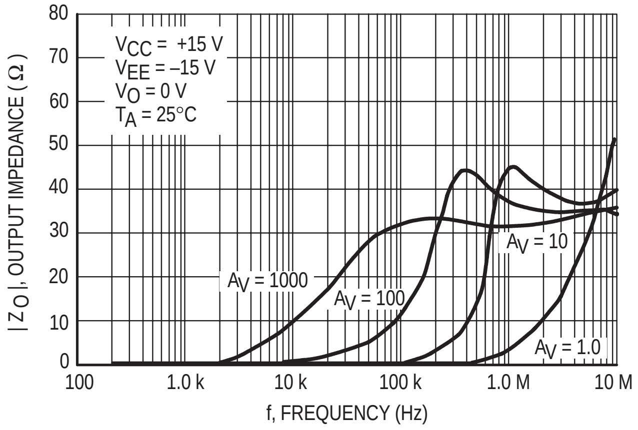


Figure 19. Channel Separation versus Frequency

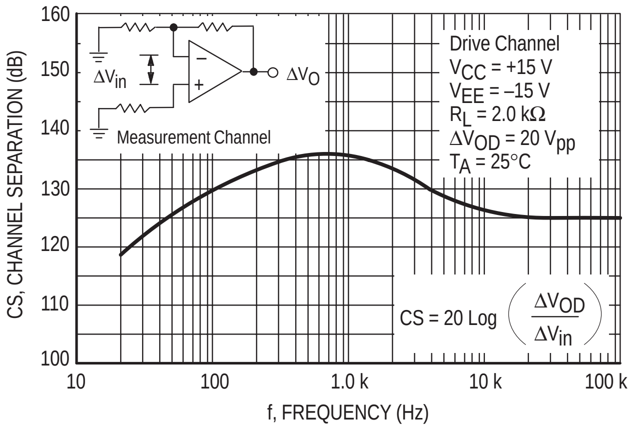


Figure 20. Total Harmonic Distortion versus Frequency

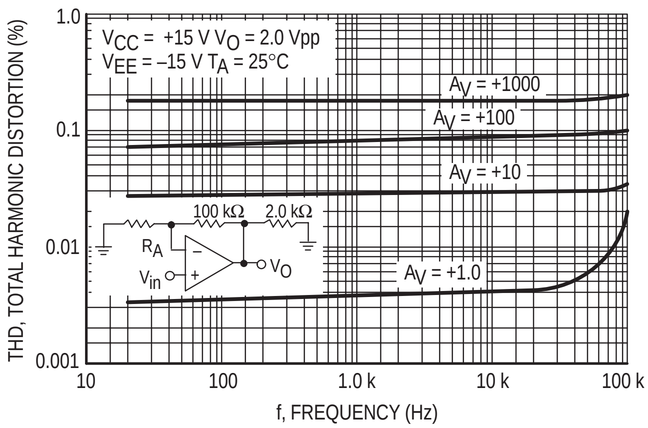


Figure 21. Total Harmonic Distortion versus Frequency

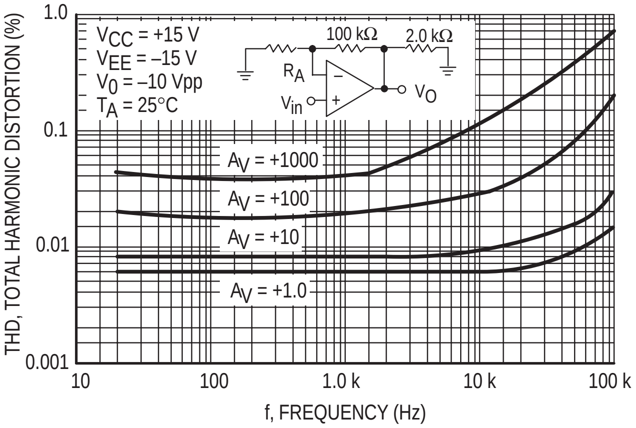


Figure 22. Total Harmonic Distortion versus Output Voltage

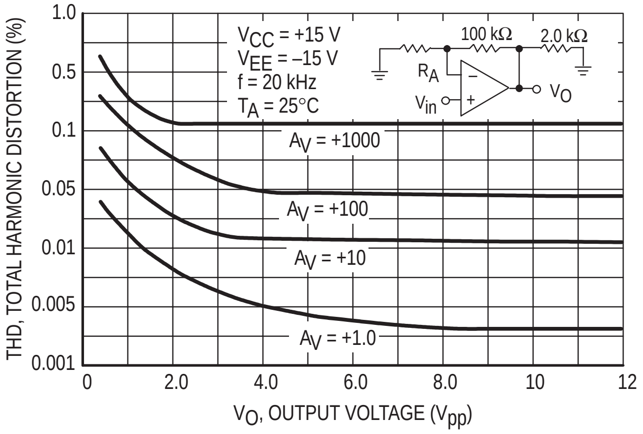


Figure 23. Slew Rate versus Supply Voltage

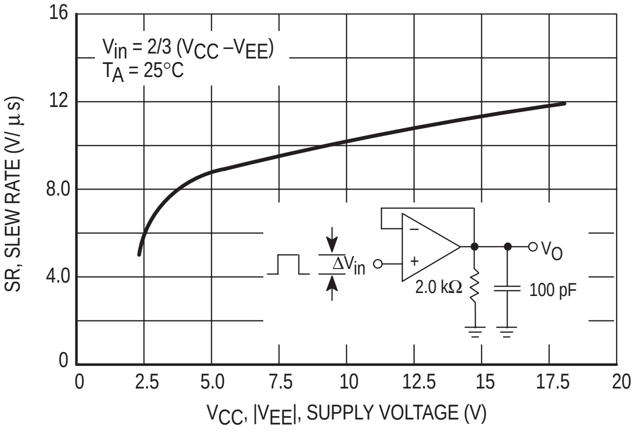


Figure 24. Slew Rate versus Temperature

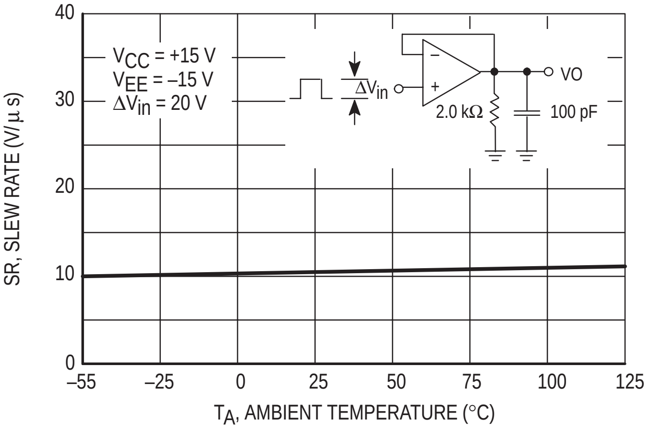


Figure 25. Voltage Gain and Phase versus Frequency

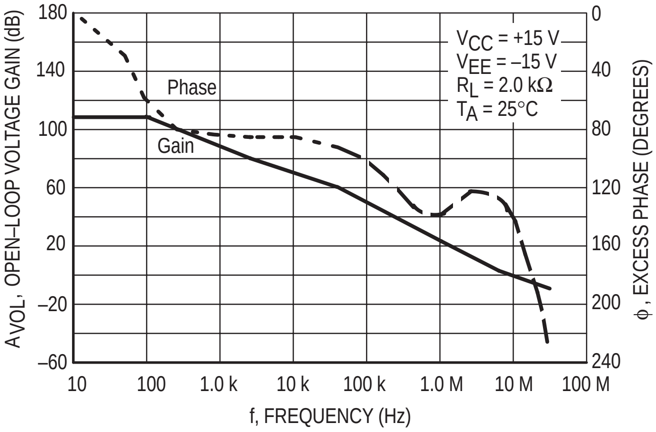


Figure 26. Open Loop Gain Margin and Phase Margin versus Output Load Capacitance

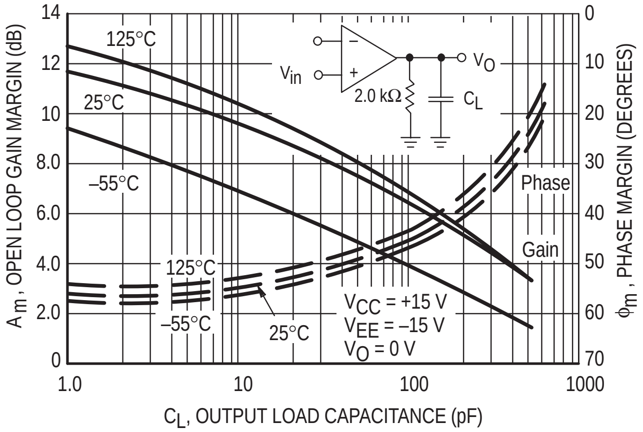


Figure 27. Phase Margin versus Output Voltage

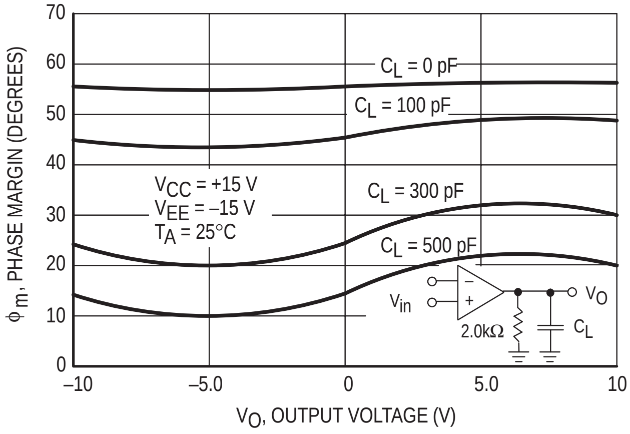


Figure 28. Overshoot versus Output Load Capacitance

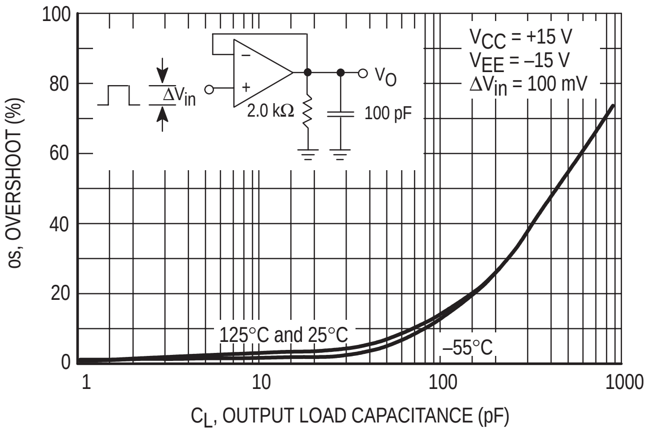


Figure 29. Input Referred Noise Voltage and Current versus Frequency

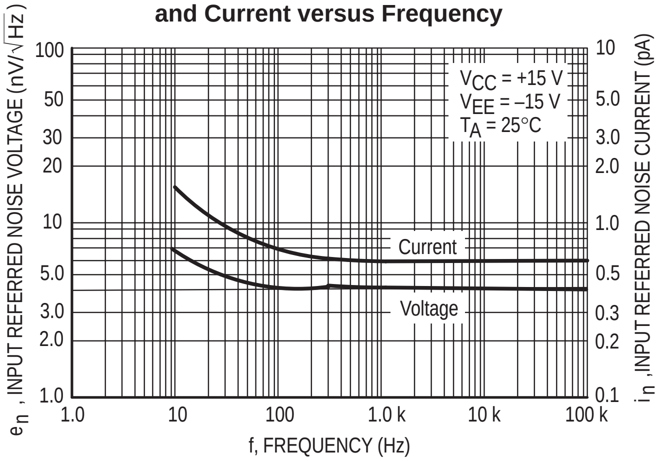


Figure 30. Total Input Referred Noise Voltage versus Source Resistant

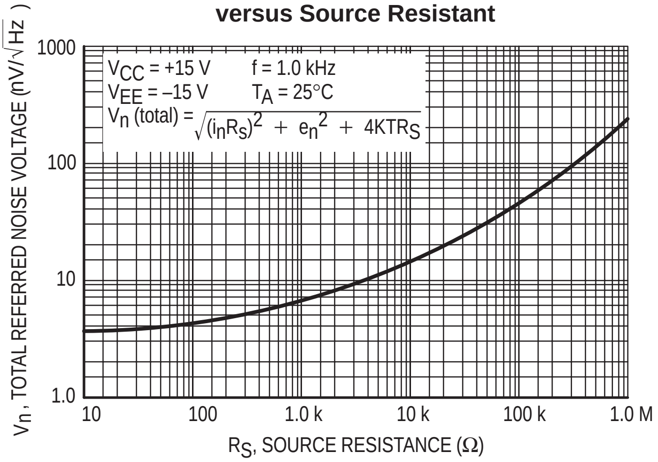


Figure 31. Phase Margin and Gain Margin versus Differential Source Resistance

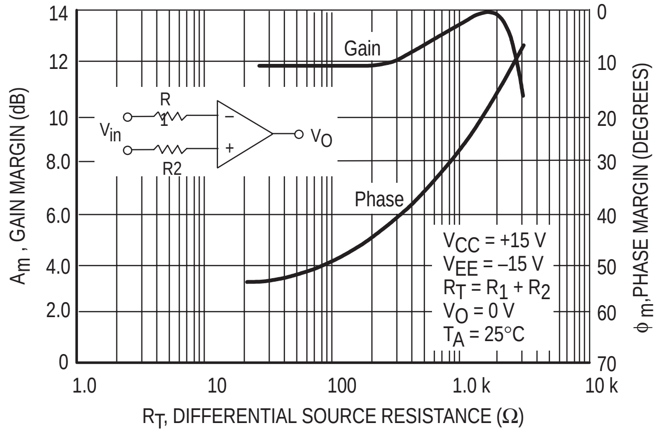


Figure 32. Inverting Amplifer Slew Rate

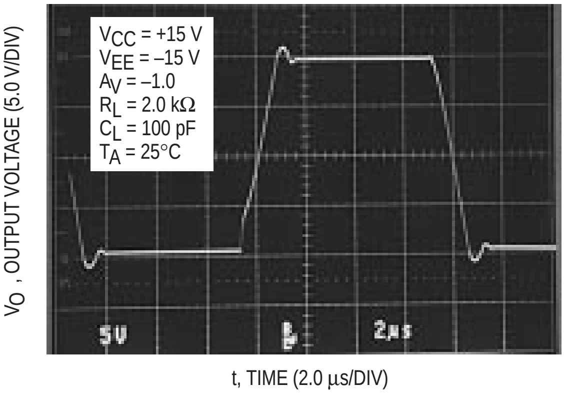


Figure 33. Noninverting Amplifier Slew Rate

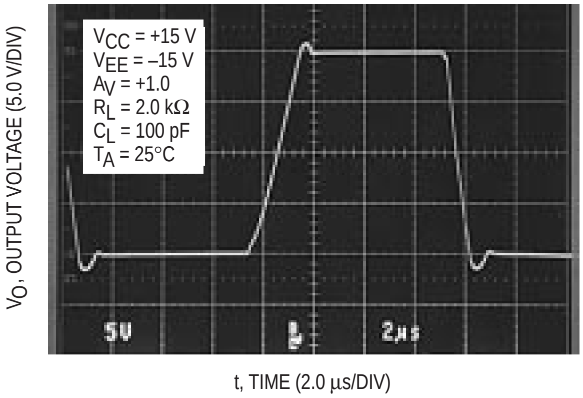


Figure 34. Noninverting Amplifier Overshoot

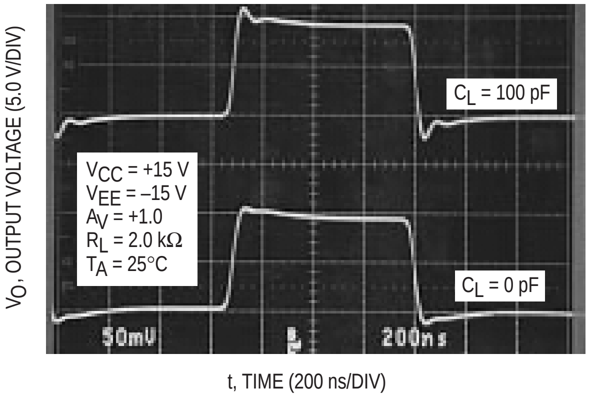
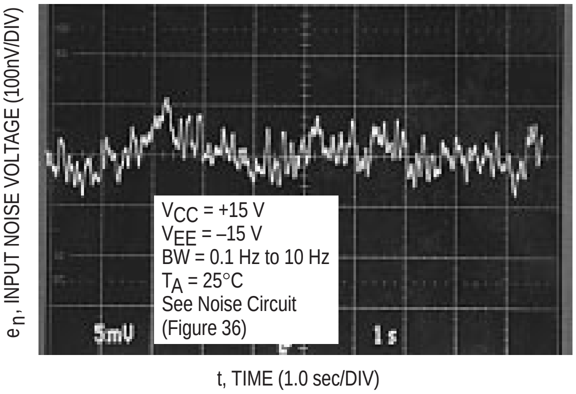


Figure 35. Low Frequency Noise Voltage versus Time



APPLICATIONS INFORMATION

The MC33077 is designed primarily for its low noise, low offset voltage, high gain bandwidth product and large output swing characteristics. Its outstanding high frequency gain/phase performance make it a very attractive amplifier for high quality preamps, instrumentation amps, active filters and other applications requiring precision quality characteristics.

The MC33077 utilizes high frequency lateral PNP input transistors in a low noise bipolar differential stage driving a compensated Miller integration amplifier. Dual–doublet frequency compensation techniques are used to enhance the gain bandwidth product. The output stage uses an all NPN transistor design which provides greater output voltage swing and improved frequency performance over more conventional stages by using both PNP and NPN transistors (Class AB). This combination produces an amplifier with superior characteristics.

Through precision component matching and innovative current mirror design, a lower than normal temperature coefficient of input offset voltage (2.0 μV/°C as opposed to 10 μV/°C), as well as low input offset voltage, is accomplished.

The minimum common mode input range is from 1.5 V below the positive rail (V_{CC}) to 1.5 V above the negative rail (V_{EE}). The inputs will typically common mode to within 1.0 V of both negative and positive rails though degradation in offset voltage and gain will be experienced as the common mode voltage nears either supply rail. In practice, though not recommended, the input voltage may exceed V_{CC} by approximately 30 V and decrease below the V_{EE} by approximately 0.6 V without causing permanent damage to the device. If the input voltage on either or both inputs is less than approximately 0.6 V, excessive current may flow, if not limited, causing permanent damage to the device.

The amplifier will not latch with input source currents up to 20 mA, though in practice, source currents should be limited to 5.0 mA to avoid any parametric damage to the device. If both inputs exceed V_{CC}, the output will be in the high state and phase reversal may occur. No phase reversal will occur if the voltage on one input is within the common mode range and the voltage on the other input exceeds V_{CC}. Phase reversal may occur if the input voltage on either or both inputs is less than 1.0 V above the negative rail. Phase reversal will be experienced if the voltage on either or both inputs is less than V_{EE}.

Through the use of dual–doublet frequency compensation techniques, the gain bandwidth product has been greatly enhanced over other amplifiers using the conventional single pole compensation. The phase and gain error of the amplifier remains low to higher frequencies for fixed amplifier gain configurations.

With the all NPN output stage, there is minimal swing loss to the supply rails, producing superior output swing, no crossover distortion and improved output phase symmetry with output voltage excursions (output phase symmetry being the amplifiers ability to maintain a constant phase relation independent of its output voltage swing). Output phase symmetry degradation in the more conventional PNP and NPN transistor output stage was primarily due to the inherent cut–off frequency mismatch of the PNP and NPN transistors used (typically 10 MHz and 300 MHz, respectively), causing considerable phase change to occur as the output voltage changes. By eliminating the PNP in the output, such phase change has been avoided and a very significant improvement in output phase symmetry as well as output swing has been accomplished.

The output swing improvement is most noticeable when operation is with lower supply voltages (typically 30% with ± 5.0 V supplies). With a 10 k load, the output of the amplifier can typically swing to within 1.0 V of the positive rail (V_{CC}), and to within 0.3 V of the negative rail (V_{EE}), producing a 28.7 V_{pp} signal from ±15 V supplies. Output voltage swing can be further improved by using an output pull–up resistor referenced to the V_{CC}. Where output signals are referenced to the positive supply rail, the pull–up resistor will pull the output to V_{CC} during the positive swing, and during the negative swing, the NPN output transistor collector will pull the output very near V_{EE}. This configuration will produce the maximum attainable output signal from given supply voltages. The value of load resistance used should be much less than any feedback resistance to avoid excess loading and allow easy pull–up of the output.

Output impedance of the amplifier is typically less than 50 Ω at frequencies less than the unity gain crossover frequency (see Figure 18). The amplifier is unity gain stable with output capacitance loads up to 500 pF at full output swing over the –55° to +125°C temperature range. Output phase symmetry is excellent with typically 4°C total phase change over a 20 V output excursion at 25°C with a 2.0 kΩ and 100 pF load. With a 2.0 kΩ resistive load and no capacitance loading, the total phase change is approximately one degree for the same 20 V output excursion. With a 2.0 kΩ and 500 pF load at 125°C, the total phase change is typically only 10°C for a 20 V output excursion (see Figure 27).

As with all amplifiers, care should be exercised to insure that one does not create a pole at the input of the amplifier which is near the closed loop corner frequency. This becomes a greater concern when using high frequency amplifiers since it is very easy to create such a pole with relatively small values of resistance on the inputs. If this does occur, the amplifier's phase will degrade severely causing the amplifier to become unstable. Effective source resistances, acting in conjunction with the input capacitance of the amplifier, should be kept to a minimum to avoid creating such a pole at the input (see Figure 31). There is minimal effect on stability where the created input pole is much greater than the closed loop corner frequency. Where amplifier stability is affected as a result of a negative feedback resistor in conjunction with the amplifier's input capacitance, creating a pole near the closed loop corner frequency, lead capacitor compensation techniques (lead capacitor in parallel with the feedback resistor) can be employed to improve stability. The feedback resistor and lead capacitor RC time constant should be larger than that of the uncompensated input pole frequency. Having a high resistance connected to the noninverting input of the amplifier can create a like instability problem. Compensation for this condition can be accomplished by adding a lead capacitor in parallel with the noninverting input resistor of such a value as to make the RC time constant larger than the RC time constant of the uncompensated input resistor acting in conjunction with the amplifiers input capacitance.

For optimum frequency performance and stability, careful component placement and printed circuit board layout should be exercised. For example, long unshielded input or output leads may result in unwanted input output coupling. In order to reduce the input capacitance, the body of resistors connected to the input pins should be physically close to the input pins. This not only minimizes the input pole creation for optimum frequency response, but also minimizes extraneous signal "pickup" at this node. Power supplies should be decoupled with adequate capacitance as close as possible to the device supply pin.

In addition to amplifier stability considerations, input source resistance values should be low to take full advantage of the low noise characteristics of the amplifier. Thermal noise (Johnson Noise) of a resistor is generated by thermally–charged carriers randomly moving within the resistor creating a voltage. The rms thermal noise voltage in a resistor can be calculated from:

$$E_{nr} = \sqrt{4k\,TR \times BW}$$

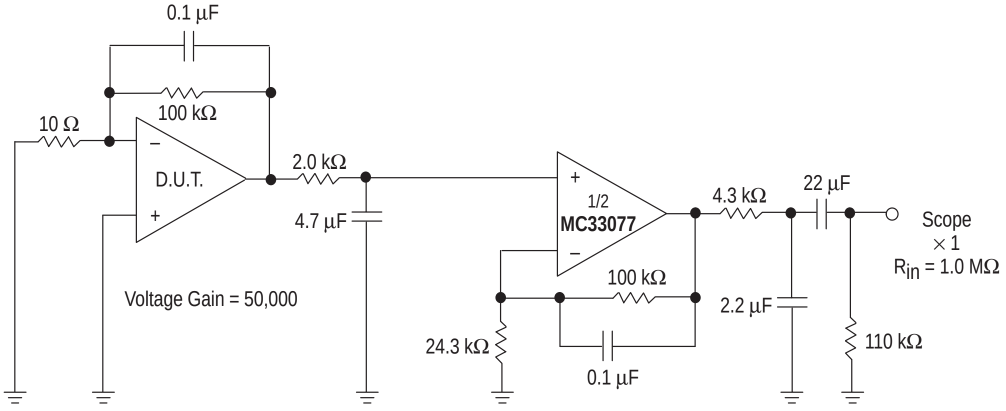
where:

k = Boltzmann's Constant (1.38×10^{-23} joules/k)
T = Kelvin temperature
R = Resistance in ohms
BW = Upper and lower frequency limit in Hertz.

By way of reference, a 1.0 kΩ resistor at 25°C will produce a 4.0 $nV/\sqrt{Hz}$ of rms noise voltage. If this resistor is connected to the input of the amplifier, the noise voltage will be gained–up in accordance to the amplifier's gain configuration. For this reason, the selection of input source resistance for low noise circuit applications warrants serious consideration. The total noise of the amplifier, as referred to its inputs, is typically only 4.4 $nV/\sqrt{Hz}$ at 1.0 kHz.

The output of any one amplifier is current limited and thus protected from a direct short to ground, However, under such conditions, it is important not to allow the amplifier to exceed the maximum junction temperature rating. Typically for ±15 V supplies, any one output can be shorted continuously to ground without exceeding the temperature rating.

Figure 36. Voltage Noise Test Circuit
(0.1 Hz to 10 Hz$_{p-p}$)



Note: All capacitors are non–polarized.

MOTOROLA

MC33078
MC33079

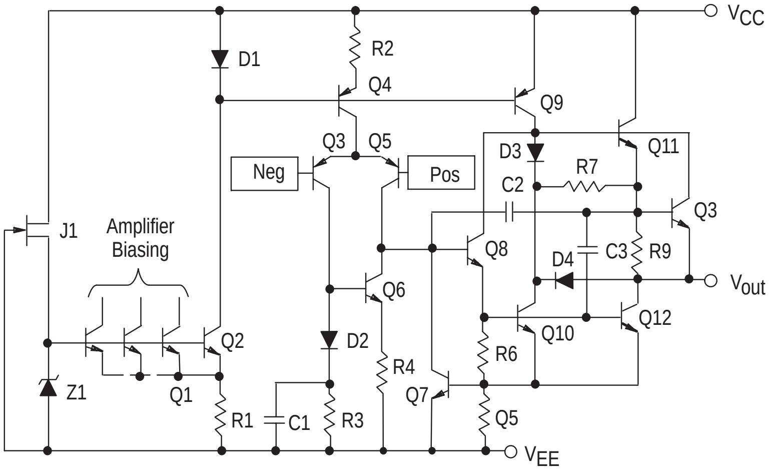
Dual/Quad Low Noise Operational Amplifiers

The MC33078/9 series is a family of high quality monolithic amplifiers employing Bipolar technology with innovative high performance concepts for quality audio and data signal processing applications. This family incorporates the use of high frequency PNP input transistors to produce amplifiers exhibiting low input voltage noise with high gain bandwidth product and slew rate. The all NPN output stage exhibits no deadband crossover distortion, large output voltage swing, excellent phase and gain margins, low open loop high frequency output impedance and symmetrical source and sink AC frequency performance.

The MC33078/9 family offers both dual and quad amplifier versions, tested over the automotive temperature range and available in the plastic DIP and SOIC packages (P and D suffixes).

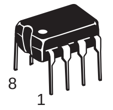
- Dual Supply Operation: ±5.0 V to ±18 V
- Low Voltage Noise: 4.5 nV/$\sqrt{\text{Hz}}$
- Low Input Offset Voltage: 0.15 mV
- Low T.C. of Input Offset Voltage: 2.0 µV/°C
- Low Total Harmonic Distortion: 0.002%
- High Gain Bandwidth Product: 16 MHz
- High Slew Rate: 7.0 V/µs
- High Open Loop AC Gain: 800 @ 20 kHz
- Excellent Frequency Stability
- Large Output Voltage Swing: +14.1 V/ –14.6 V
- ESD Diodes Provided on the Inputs

Representative Schematic Diagram
(Each Amplifier)

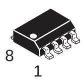


DUAL/QUAD LOW NOISE OPERATIONAL AMPLIFIERS

DUAL

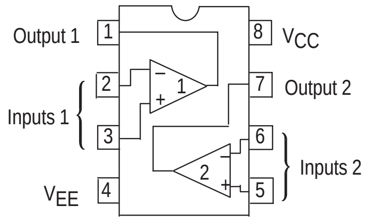


P SUFFIX
PLASTIC PACKAGE
CASE 626



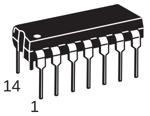
D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

PIN CONNECTIONS

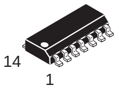


(Dual, Top View)

QUAD

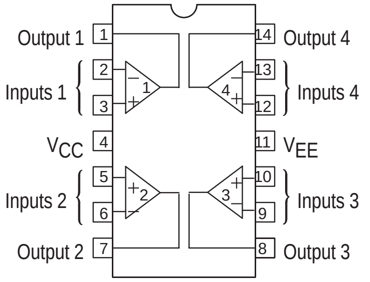


P SUFFIX
PLASTIC PACKAGE
CASE 646



D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO–14)

PIN CONNECTIONS



(Quad, Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC33078D	T_A = –40° to +85°C	SO–8
MC33078P		Plastic DIP
MC33079D		SO–14
MC33079P		Plastic DIP

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage (V_{CC} to V_{EE})	V_S	+36	V
Input Differential Voltage Range	V_{IDR}	(Note 1)	V
Input Voltage Range	V_{IR}	(Note 1)	V
Output Short Circuit Duration (Note 2)	t_{SC}	Indefinite	sec
Maximum Junction Temperature	T_J	+150	°C
Storage Temperature	T_{stg}	–60 to +150	°C
Maximum Power Dissipation	P_D	(Note 2)	mW

NOTES: 1. Either or both input voltages must not exceed the magnitude of V_{CC} or V_{EE}.
2. Power dissipation must be considered to ensure maximum junction temperature (T_J) is not exceeded (see Figure 1).

DC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = –15 V, T_A = 25°C, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Input Offset Voltage (R_S = 10 Ω, V_{CM} = 0 V, V_O = 0 V) (MC33078) T_A = +25°C T_A = –40° to +85°C (MC33079) T_A = +25°C T_A = –40° to +85°C	$\|V_{IO}\|$	 — — — —	 0.15 — 0.15 —	 2.0 3.0 2.5 3.5	mV
Average Temperature Coefficient of Input Offset Voltage R_S = 10 Ω, V_{CM} = 0 V, V_O = 0 V, T_A = T_{low} to T_{high}	$\Delta V_{IO}/\Delta T$	—	2.0	—	µV/°C
Input Bias Current (V_{CM} = 0 V, V_O = 0 V) T_A = +25°C T_A = –40° to +85°C	I_{IB}	 — —	 300 —	 750 800	nA
Input Offset Current (V_{CM} = 0 V, V_O = 0 V) T_A = +25°C T_A = –40° to +85°C	I_{IO}	 — —	 25 —	 150 175	nA
Common Mode Input Voltage Range (ΔV_{IO} = 5.0 mV, V_O = 0 V)	V_{ICR}	±13	±14	—	V
Large Signal Voltage Gain (V_O = ±10 V, R_L = 2.0 kΩ) T_A = +25°C T_A = –40° to +85°C	A_{VOL}	 90 85	 110 —	 — —	dB
Output Voltage Swing (V_{ID} = ±1.0V) R_L = 600 Ω R_L = 600 Ω R_L = 2.0 kΩ R_L = 2.0 kΩ R_L = 10 kΩ R_L = 10 kΩ	 V_O+ V_O- V_O+ V_O- V_O+ V_O-	 — — +13.2 — +13.5 —	 +10.7 –11.9 +13.8 –13.7 +14.1 –14.6	 — — — –13.2 — –14	V
Common Mode Rejection (V_{in} = ±13V)	CMR	80	100	—	dB
Power Supply Rejection (Note 3) V_{CC}/V_{EE} = +15 V/ –15 V to +5.0 V/ –5.0 V	PSR	80	105	—	dB
Output Short Circuit Current (V_{ID} = 1.0 V, Output to Ground) Source Sink	I_{SC}	 +15 –20	 +29 –37	 — —	mA
Power Supply Current (V_O = 0 V, All Amplifiers) (MC33078) T_A = +25°C T_A = –40° to +85°C (MC33079) T_A = +25°C T_A = –40° to +85°C	I_D	 — — — —	 4.1 — 8.4 —	 5.0 5.5 10 11	mA

NOTE: 3. Measured with V_{CC} and V_{EE} differentially varied simultaneously.

AC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = –15 V, T_A = 25°C, unless otherwise noted.)

Characteristics		Symbol	Min	Typ	Max	Unit
Slew Rate (V_{in} = –10 V to +10 V, R_L = 2.0 kΩ, C_L = 100 pF A_V = +1.0)		SR	5.0	7.0	—	V/µs
Gain Bandwidth Product (f = 100 kHz)		GBW	10	16	—	MHz
Unity Gain Frequency (Open Loop)		f_U	—	9.0	—	MHz
Gain Margin (R_L = 2.0 kΩ)	C_L = 0 pF C_L = 100 pF	A_m	— —	–11 –6.0	—	dB
Phase Margin (R_L = 2.0 kΩ)	C_L = 0 pF C_L = 100 pF	ϕ_m	— —	55 40	—	Degrees
Channel Separation (f = 20 Hz to 20 kHz)		CS	—	–120	—	dB
Power Bandwidth (V_O = 27 V_{pp}, R_L = 2.0 kΩ, THD ≤ 1.0%)		BW_p	—	120	—	kHz
Distortion (R_L = 2.0 kΩ, f = 20 Hz to 20 kHz, V_O = 3.0 V_{rms}, A_V = +1.0)		THD	—	0.002	—	%
Open Loop Output Impedance (V_O = 0 V, f = 9.0 MHz)		$\lvert Z_O \rvert$	—	37	—	Ω
Differential Input Resistance (V_{CM} = 0 V)		R_{IN}	—	175	—	kΩ
Differential Input Capacitance (V_{CM} = 0 V)		C_{IN}	—	12	—	pF
Equivalent Input Noise Voltage (R_S = 100 Ω, f = 1.0 kHz)		e_n	—	4.5	—	$\mathrm{nV}/\sqrt{\mathrm{Hz}}$
Equivalent Input Noise Current (f = 1.0 kHz)		i_n	—	0.5	—	$\mathrm{pA}/\sqrt{\mathrm{Hz}}$

Figure 1. Maximum Power Dissipation versus Temperature

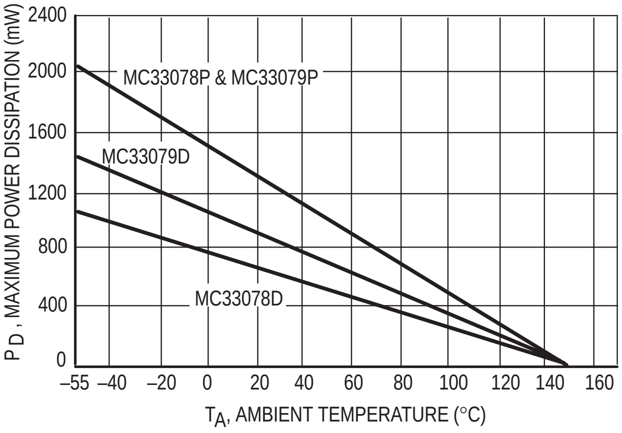


Figure 2. Input Bias Current versus Supply Voltage

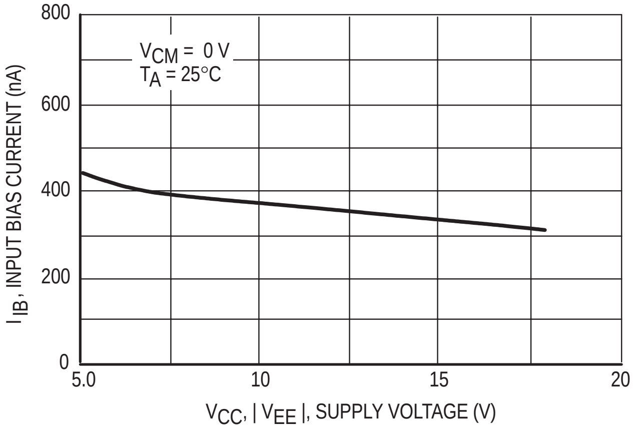


Figure 3. Input Bias Current versus Temperature

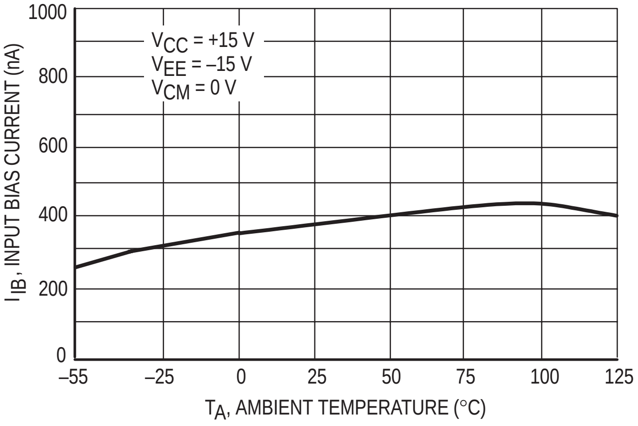


Figure 4. Input Offset Voltage versus Temperature

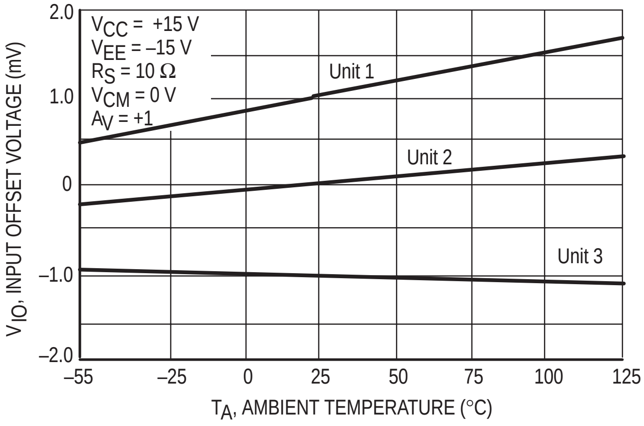


Figure 5. Input Bias Current versus Common Mode Voltage

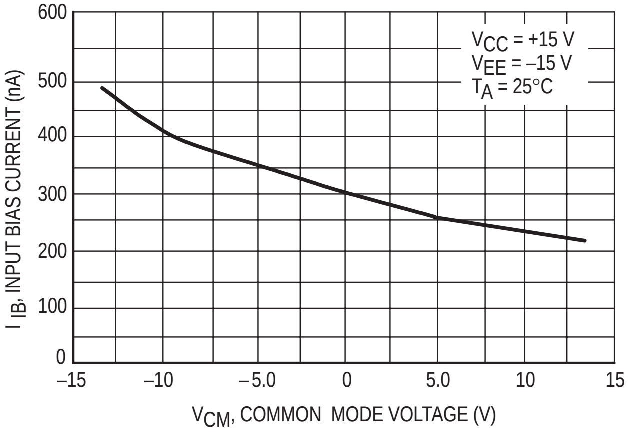


Figure 6. Input Common Mode Voltage Range versus Temperature

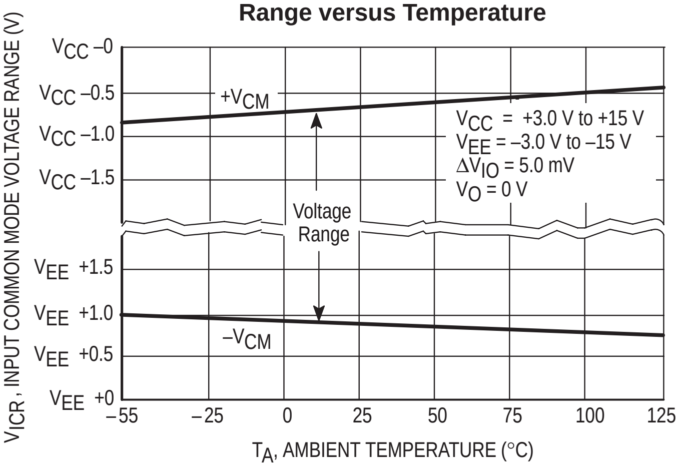


Figure 7. Output Saturation Voltage versus Load Resistance to Ground

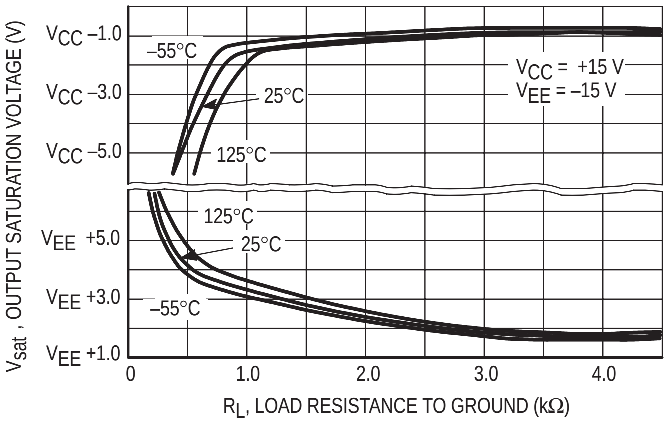


Figure 8. Output Short Circuit Current versus Temperature

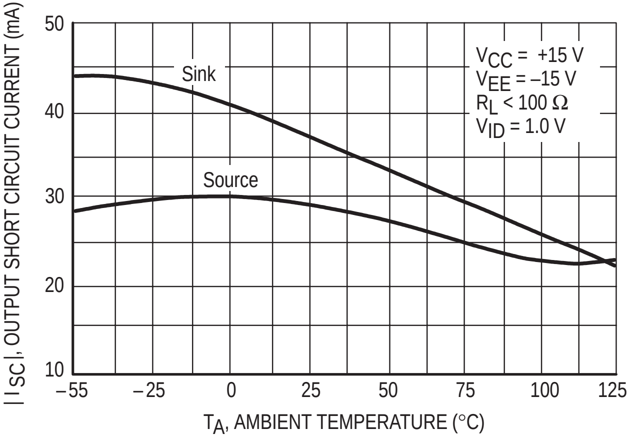


Figure 9. Supply Current versus Temperature

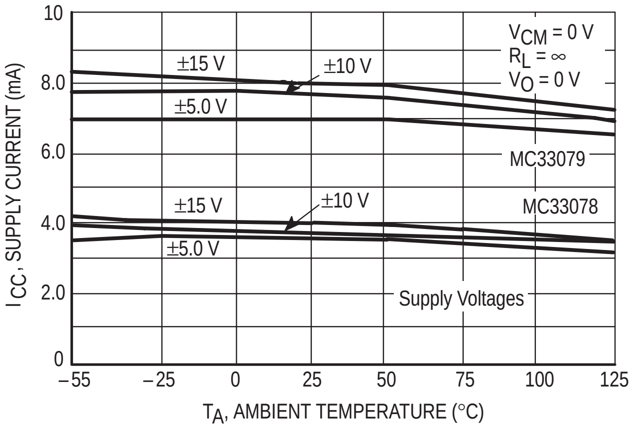


Figure 10. Common Mode Rejection versus Frequency

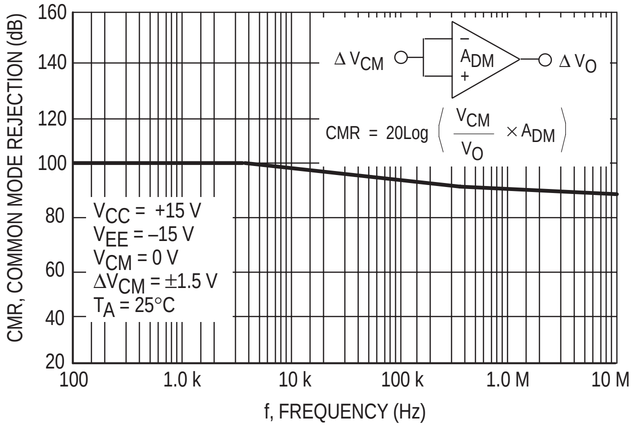


Figure 11. Power Supply Rejection versus Frequency

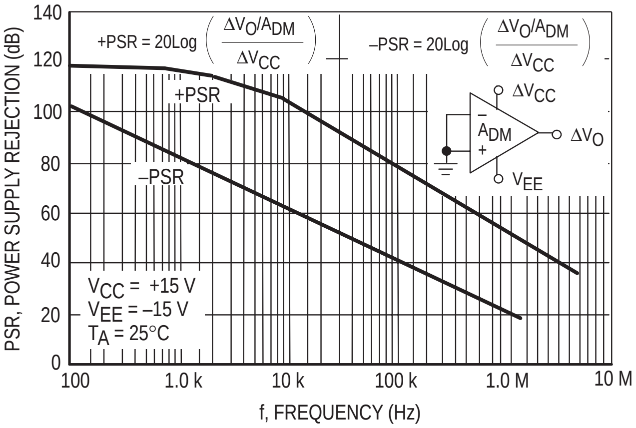


Figure 12. Gain Bandwidth Product versus Supply Voltage

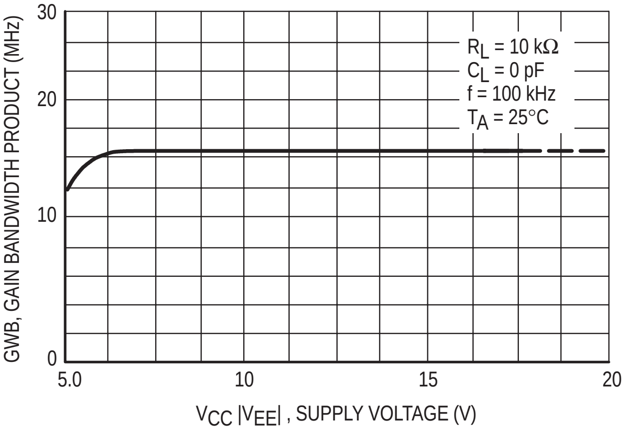


Figure 13. Gain Bandwidth Product versus Temperature

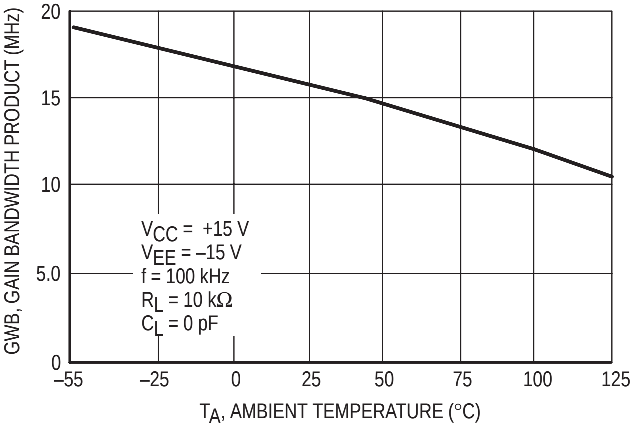


Figure 14. Maximum Output Voltage versus Supply Voltage

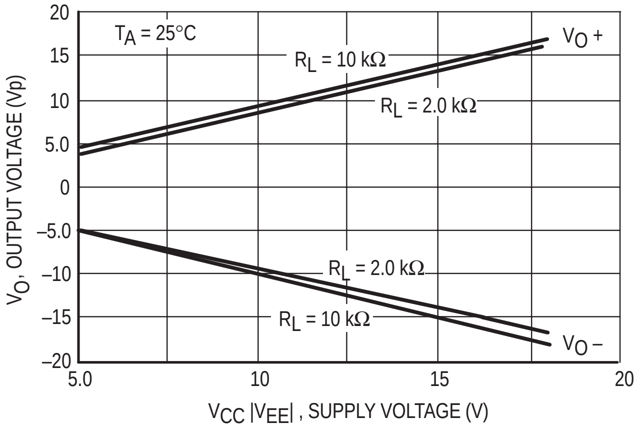


Figure 15. Output Voltage versus Frequency

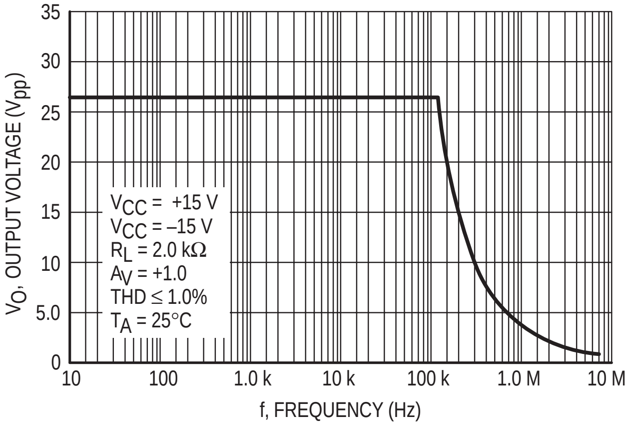


Figure 16. Open Loop Voltage Gain versus Supply Voltage

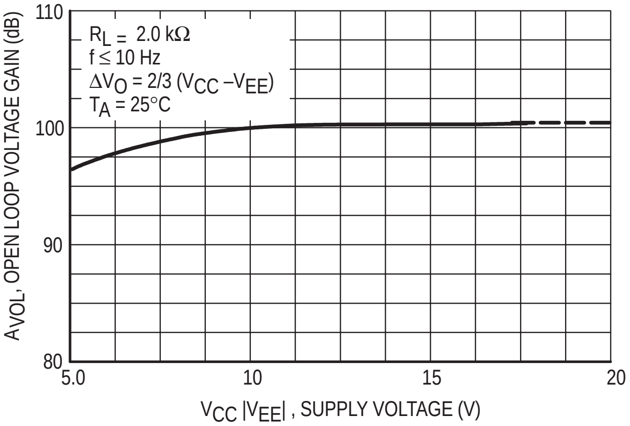


Figure 17. Open Loop Voltage Gain versus Temperature

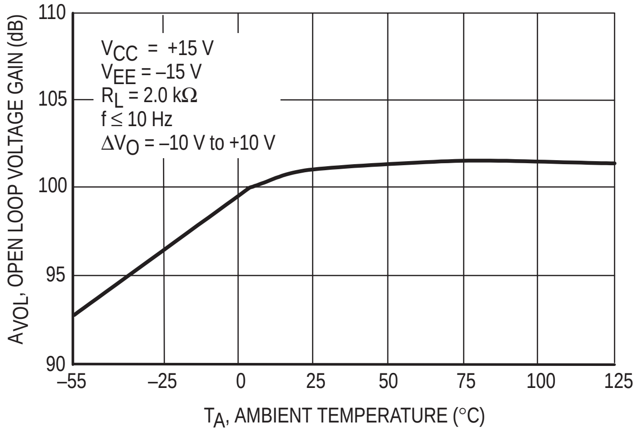


Figure 18. Output Impedance versus Frequency

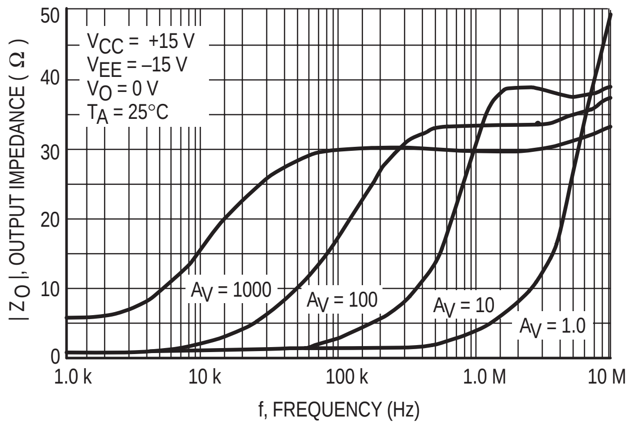


Figure 19. Channel Separation versus Frequency

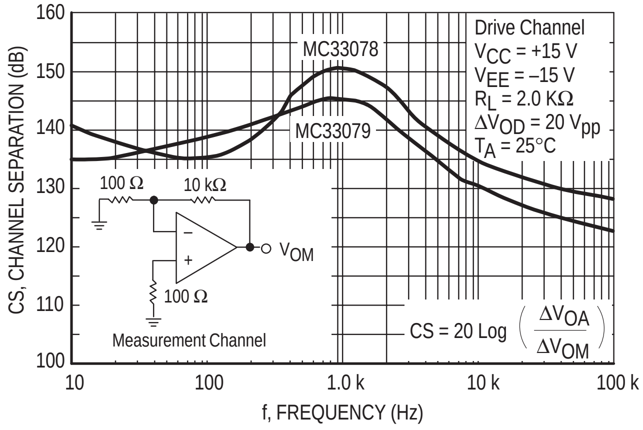


Figure 20. Total Harmonic Distortion versus Frequency

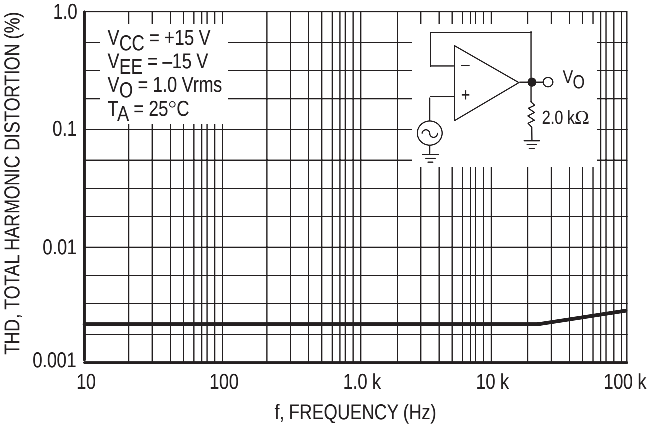


Figure 21. Total Harmonic Distortion versus Output Voltage

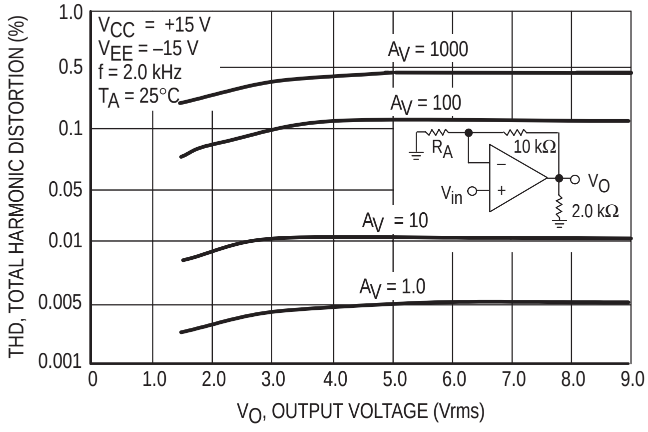


Figure 22. Slew Rate versus Supply Voltage

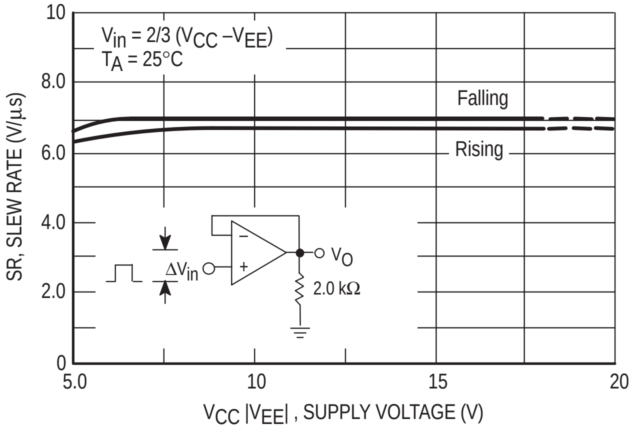


Figure 23. Slew Rate versus Temperature

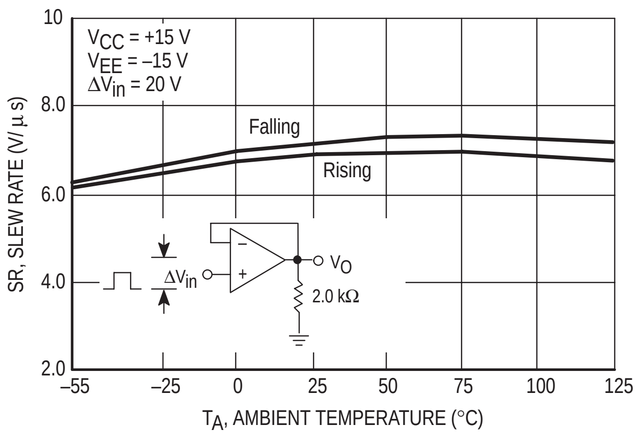


Figure 24. Voltage Gain and Phase versus Frequency

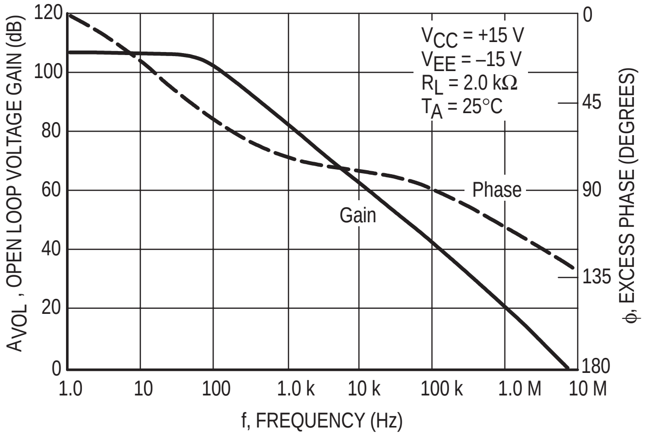


Figure 25. Open Loop Gain Margin and Phase Margin versus Load Capacitance

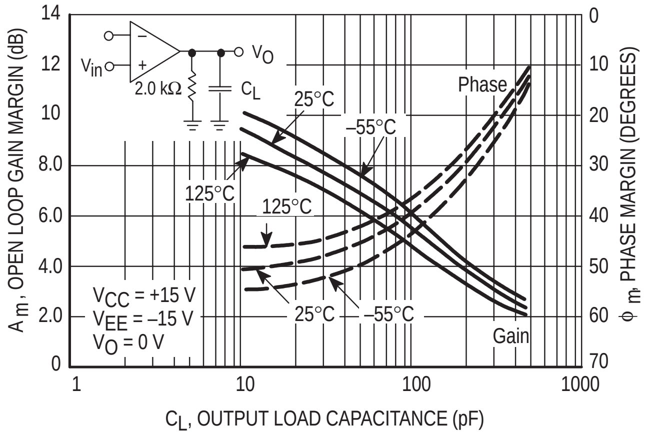


Figure 26. Overshoot versus Output Load Capacitance

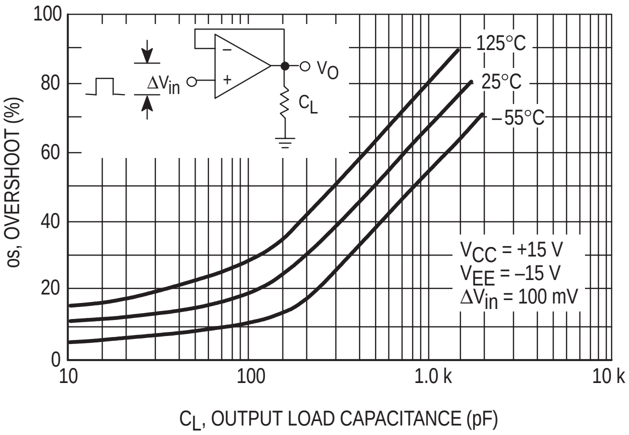


Figure 27. Input Referred Noise Voltage and Current versus Frequency

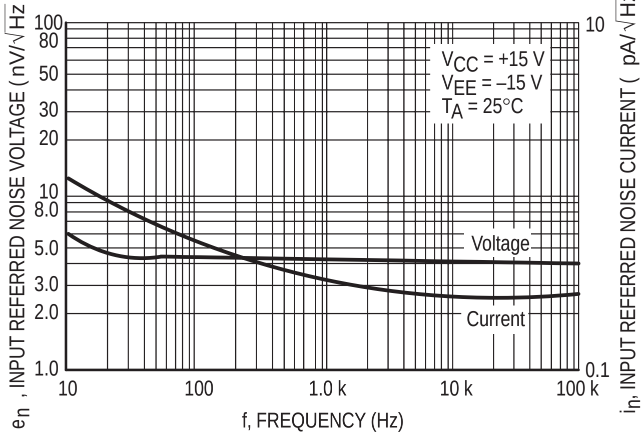


Figure 28. Total Input Referred Noise Voltage versus Source Resistance

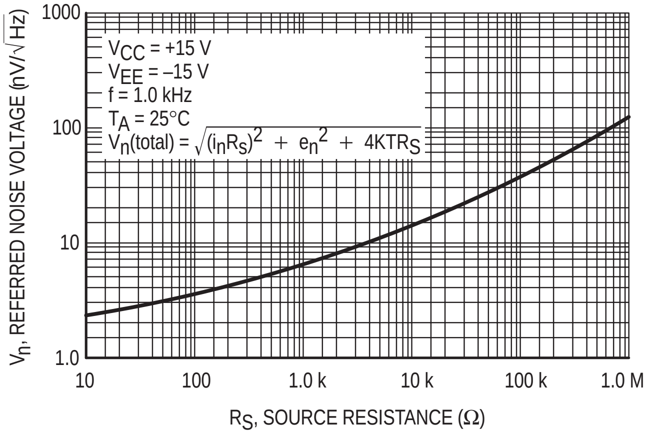


Figure 29. Phase Margin and Gain Margin versus Differential Source Resistance

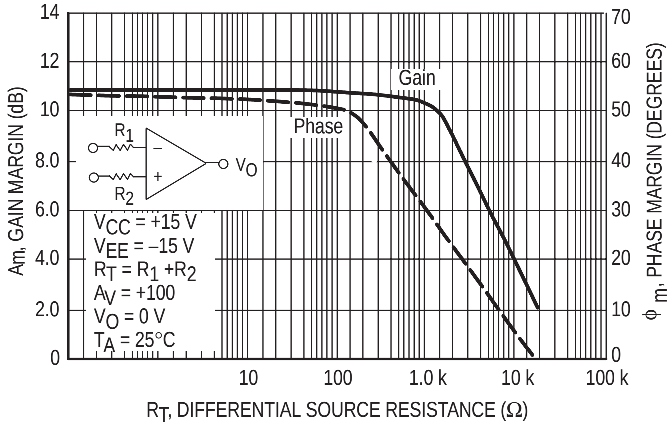


Figure 30. Inverting Amplifier Slew Rate

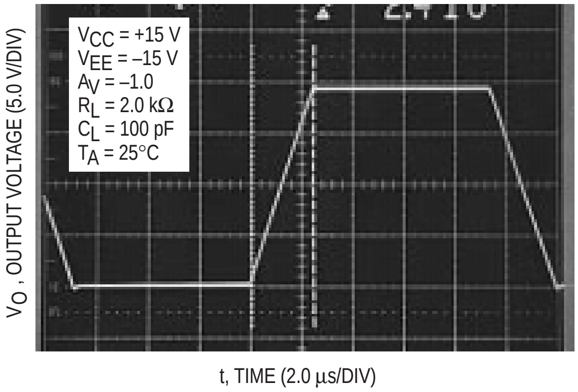


Figure 31. Noninverting Amplifier Slew Rate

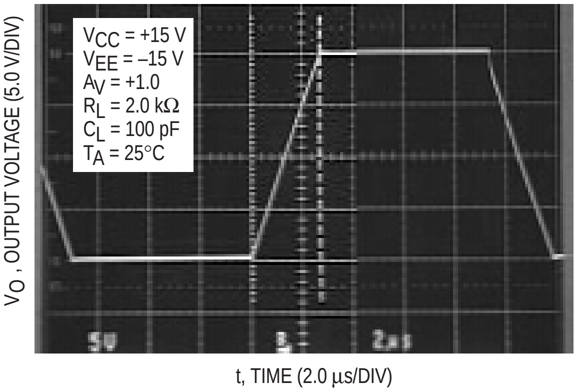


Figure 32. Noninverting Amplifier Overshoot

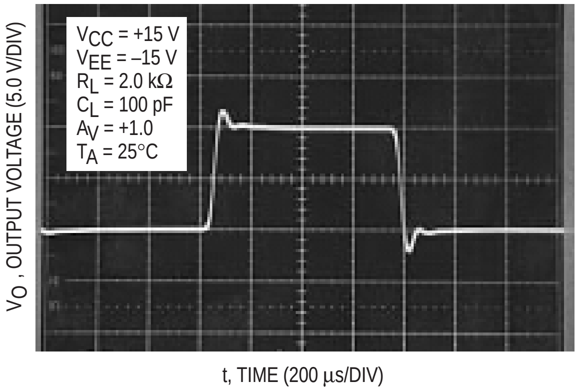


Figure 33. Low Frequency Noise Voltage versus Time

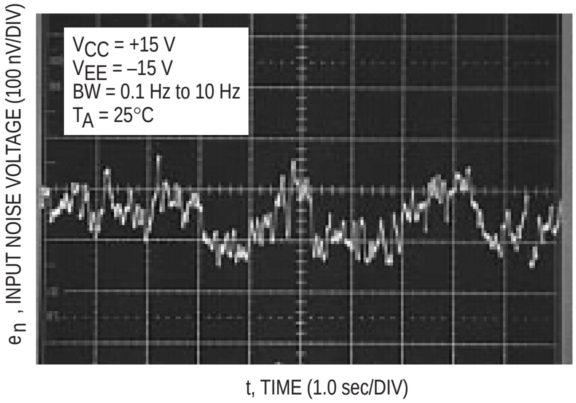
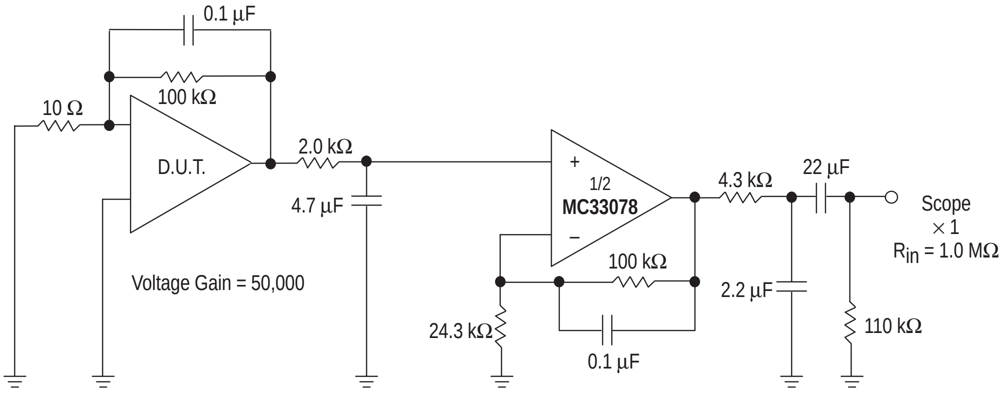


Figure 34. Voltage Noise Test Circuit (0.1 Hz to 10 Hz$_{p-p}$)



Note: All capacitors are non–polarized.

MOTOROLA

Sleep-Mode™ Two-State, Micropower Operational Amplifier

The MC33102 dual operational amplifier is an innovative design concept employing Sleep–Mode technology. Sleep–Mode amplifiers have two separate states, a sleepmode and an awakemode. In sleepmode, the amplifier is active and waiting for an input signal. When a signal is applied causing the amplifier to source or sink 160 µA (typically) to the load, it will automatically switch to the awakemode which offers higher slew rate, gain bandwidth, and drive capability.

- Two States: “Sleepmode” (Micropower) and “Awakemode” (High Performance)
- Switches from Sleepmode to Awakemode in 4.0 µs when Output Current Exceeds the Threshold Current (R_L = 600 Ω)
- Independent Sleepmode Function for Each Op Amp
- Standard Pinouts – No Additional Pins or Components Required
- Sleepmode State – Can Be Used in the Low Current Idle State as a Fully Functional Micropower Amplifier
- Automatic Return to Sleepmode when Output Current Drops Below Threshold
- No Deadband/Crossover Distortion; as Low as 1.0 Hz in the Awakemode
- Drop–in Replacement for Many Other Dual Op Amps
- ESD Clamps on Inputs Increase Reliability without Affecting Device Operation

TYPICAL SLEEPMODE/AWAKEMODE PERFORMANCE

Characteristic	Sleepmode (Typical)	Awakemode (Typical)	Unit
Low Current Drain	45	750	µA
Low Input Offset Voltage	0.15	0.15	mV
High Output Current Capability	0.15	50	mA
Low T.C. of Input Offset Voltage	1.0	1.0	µV/°C
High Gain Bandwidth (@ 20 kHz)	0.33	4.6	MHz
High Slew Rate	0.16	1.7	V/µs
Low Noise (@ 1.0 kHz)	28	9.0	$nV/\sqrt{Hz}$

MAXIMUM RATINGS

Ratings	Symbol	Value	Unit
Supply Voltage (V_{CC} to V_{EE})	V_S	+36	V
Input Differential Voltage Range Input Voltage Range	V_{IDR} V_{IR}	(Note 1)	V
Output Short Circuit Duration (Note 2)	t_{SC}	(Note 2)	sec
Maximum Junction Temperature Storage Temperature	T_J T_{stg}	+150 –65 to +150	°C
Maximum Power Dissipation	P_D	(Note 2)	mW

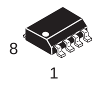
NOTES: 1. Either or both input voltages should not exceed V_{CC} or V_{EE}.
2. Power dissipation must be considered to ensure maximum junction temperature (T_J) is not exceeded (refer to Figure 1).

MC33102

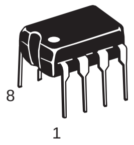
DUAL SLEEP–MODE OPERATIONAL AMPLIFIER

SEMICONDUCTOR TECHNICAL DATA

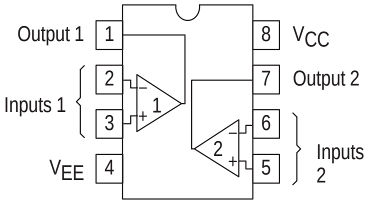
D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)



P SUFFIX
PLASTIC PACKAGE
CASE 626



PIN CONNECTIONS

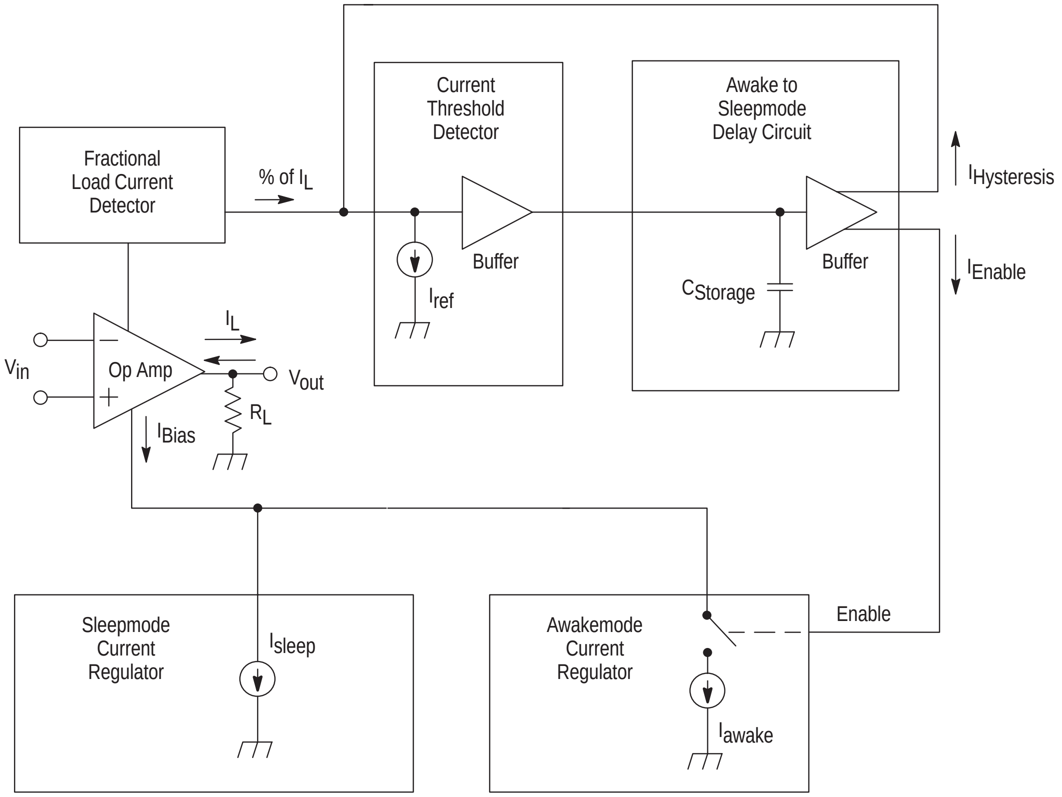


(Dual, Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC33102D	T_A = – 40° to +85°C	SO–8
MC33102P		Plastic DIP

Simplified Block Diagram



DC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = –15 V, T_A = 25°C, unless otherwise noted.)

Characteristics	Figure	Symbol	Min	Typ	Max	Unit
Input Offset Voltage (R_S = 50 Ω, V_{CM} = 0 V, V_O = 0 V)	2	$\|V_{IO}\|$				mV
Sleepmode						
T_A = +25°C			—	0.15	2.0	
T_A = –40° to +85°C			—	—	3.0	
Awakemode						
T_A = +25°C			—	0.15	2.0	
T_A = –40° to +85°C			—	—	3.0	
Input Offset Voltage Temperature Coefficient (R_S = 50 Ω, V_{CM} = 0 V, V_O = 0 V)	3	$\Delta V_{IO}/\Delta T$				µV/°C
T_A = –40° to +85°C (Sleepmode and Awakemode)			—	1.0	—	
Input Bias Current (V_{CM} = 0 V, V_O = 0 V)	4, 6	I_{IB}				nA
Sleepmode						
T_A = +25°C			—	8.0	50	
T_A = –40° to +85°C			—	—	60	
Awakemode						
T_A = +25°C			—	100	500	
T_A = –40° to +85°C			—	—	600	
Input Offset Current (V_{CM} = 0 V, V_O = 0 V)	—	$\|I_{IO}\|$				nA
Sleepmode						
T_A = +25°C			—	0.5	5.0	
T_A = –40° to +85°C			—	—	6.0	
Awakemode						
T_A = +25°C			—	5.0	50	
T_A = –40° to +85°C			—	—	60	

DC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = –15 V, T_A = 25°C, unless otherwise noted.)

Characteristics	Figure	Symbol	Min	Typ	Max	Unit
Common Mode Input Voltage Range	5	V_{ICR}				V
(ΔV_{IO} = 5.0 mV, V_O = 0 V)						
Sleepmode and Awakemode			–13	–14.8	—	
			—	+14.2	+13	
Large Signal Voltage Gain	7	A_{VOL}				kV/V
Sleepmode (RL = 1.0 MΩ)						
T_A = +25°C			25	200	—	
T_A = –40° to +85°C			15	—	—	
Awakemode (V_O = ±10 V, R_L = 600 Ω)						
T_A = +25°C			50	700	—	
T_A = –40° to +85°C			25	—	—	
Output Voltage Swing (V_{ID} = ±1.0 V)	8, 9, 10					V
Sleepmode (V_{CC} = +15 V, V_{EE} = –15 V)						
R_L = 1.0 MΩ		V_{O+}	+13.5	+14.2	—	
R_L = 1.0 MΩ		V_{O-}	—	–14.2	–13.5	
Awakemode (V_{CC} = +15 V, V_{EE} = –15 V)						V
R_L = 600 Ω		V_{O+}	+12.5	+13.6	—	
R_L = 600 Ω		V_{O-}	—	–13.6	–12.5	
R_L = 2.0 kΩ		V_{O+}	+13.3	+14	—	
R_L = 2.0 kΩ		V_{O-}	—	–14	–13.3	
Awakemode (V_{CC} = +2.5 V, V_{EE} = –2.5 V)						
R_L = 600 Ω		V_{O+}	+1.1	+1.6	—	
R_L = 600 Ω		V_{O-}	—	–1.6	–1.1	
Common Mode Rejection (V_{CM} = ±13 V)	11	CMR				dB
Sleepmode and Awakemode			80	90	—	
Power Supply Rejection (V_{CC}/V_{EE} = +15 V/–15 V, 5.0 V/–15 V, +15 V/–5.0 V)	12	PSR				dB
Sleepmode and Awakemode			80	100	—	
Output Transition Current	13, 14					µA
Sleepmode to Awakemode (Source/Sink)		$\lvert I_{TH1}\rvert$				
(V_S = ±15 V)			200	160	—	
(V_S = ±2.5 V)			250	200	—	
Awakemode to Sleepmode (Source/Sink)		$\lvert I_{TH2}\rvert$				
(V_S = ±15 V)			—	142	90	
(V_S = ±2.5 V)			—	180	140	
Output Short Circuit Current (Awakemode)	15, 16	$\lvert I_{SC}\rvert$				mA
(V_{ID} = ±1.0 V, Output to Ground)						
Source			50	110	—	
Sink			50	110	—	
Power Supply Current (per Amplifier) (A_{CL} = 1, V_O = 0V)	17	I_D				µA
Sleepmode (V_S = ±15 V)						
T_A = +25°C			—	45	65	
T_A = –40° to +85°C			—	48	70	
Sleepmode (V_S = ±2.5 V)						
T_A = +25°C			—	38	65	
T_A = –40° to +85°C			—	42	—	
Awakemode (V_S = ±15 V)						
T_A = +25°C			—	750	800	
T_A = –40° to +85°C			—	800	900	

AC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = –15 V, T_A = 25°C, unless otherwise noted.)

Characteristics	Figure	Symbol	Min	Typ	Max	Unit
Slew Rate (V_{in} = –5.0 V to +5.0 V, C_L = 50 pF, A_V = 1.0)	18	SR				V/µs
Sleepmode (R_L = 1.0 MΩ)			0.10	0.16	—	
Awakemode (R_L = 600 Ω)			1.0	1.7	—	
Gain Bandwidth Product	19	GBW				MHz
Sleepmode (f = 10 kHz)			0.25	0.33	—	
Awakemode (f = 20 kHz)			3.5	4.6	—	
Sleepmode to Awakemode Transition Time (A_{CL} = 0.1, V_{in} = 0 V to +5.0 V)	20, 21	t_{tr1}				µs
R_L = 600 Ω			—	4.0	—	
R_L = 10 kΩ			—	15	—	
Awakemode to Sleepmode Transition Time	22	t_{tr2}	—	1.5	—	sec
Unity Gain Frequency (Open Loop)		f_U				kHz
Sleepmode (R_L = 100 kΩ, C_L = 0 pF)			—	200	—	
Awakemode (R_L = 600 Ω, C_L = 0 pF)			—	2500	—	
Gain Margin	23, 25	A_M				dB
Sleepmode (R_L = 100 kΩ, C_L = 0 pF)			—	13	—	
Awakemode (R_L = 600 Ω, C_L = 0 pF)			—	12	—	
Phase Margin	24, 26	$\varnothing_M$				Degrees
Sleepmode (R_L = 100 kΩ, C_L = 0 pF)			—	60	—	
Awakemode (R_L = 600 Ω, C_L = 0 pF)			—	60	—	
Channel Separation (f = 100 Hz to 20 kHz)	29	CS				dB
Sleepmode and Awakemode			—	120	—	
Power Bandwidth (Awakemode) (V_O = 10 V_{pp}, R_L = 100 kΩ, THD ≤ 1%)		BW_P	—	20	—	kHz
Total Harmonic Distortion (V_O = 2.0 V_{pp}, A_V = 1.0)	30	THD				%
Awakemode (R_L = 600 Ω)						
f = 1.0 kHz			—	0.005	—	
f = 10 kHz			—	0.016	—	
f = 20 kHz			—	0.031	—	
DC Output Impedance (V_O = 0 V, A_V = 10, I_Q = 10 µA)	31	R_O				Ω
Sleepmode			—	1.0 k	—	
Awakemode			—	96	—	
Differential Input Resistance (V_{CM} = 0 V)		R_{in}				MΩ
Sleepmode			—	1.3	—	
Awakemode			—	0.17	—	
Differential Input Capacitance (V_{CM} = 0 V)		C_{in}				pF
Sleepmode			—	0.4	—	
Awakemode			—	4.0	—	
Equivalent Input Noise Voltage (f = 1.0 kHz, R_S = 100 Ω)	32	e_n				$nV/\sqrt{Hz}$
Sleepmode			—	28	—	
Awakemode			—	9.0	—	
Equivalent Input Noise Current (f = 1.0 kHz)	33	i_n				$pA/\sqrt{Hz}$
Sleepmode			—	0.01	—	
Awakemode			—	0.05	—	

Figure 1. Maximum Power Dissipation versus Temperature

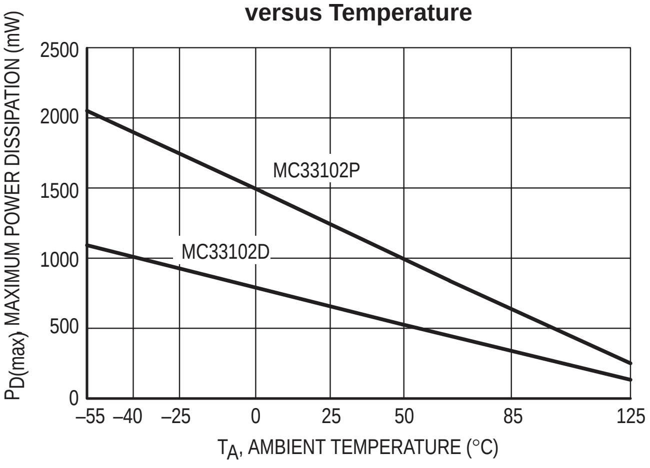


Figure 2. Distribution of Input Offset Voltage (MC33102D Package)

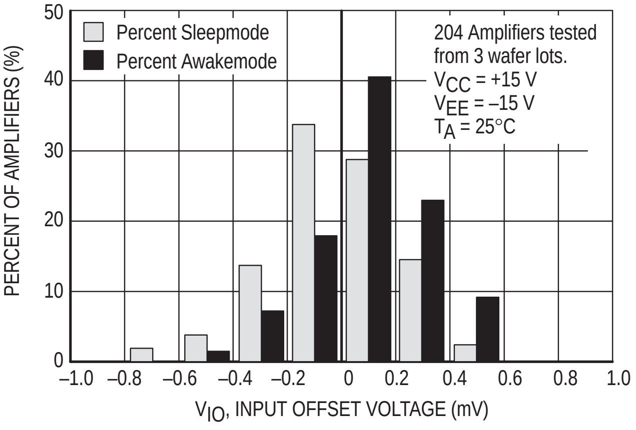


Figure 3. Input Offset Voltage Temperature Coefficient Distribution (MC33102D Package)

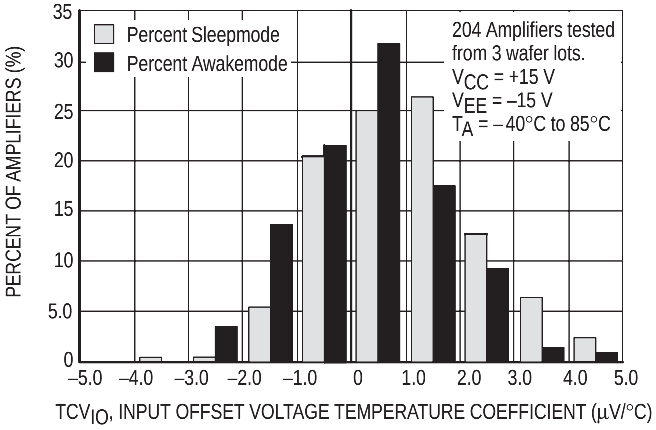


Figure 4. Input Bias Current versus Common Mode Input Voltage

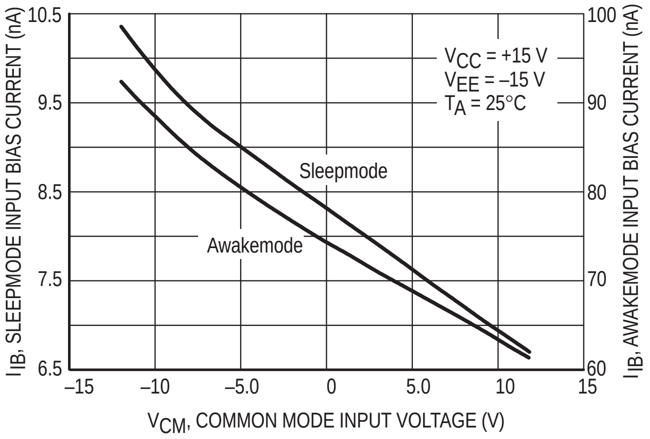


Figure 5. Input Common Mode Voltage Range versus Temperature

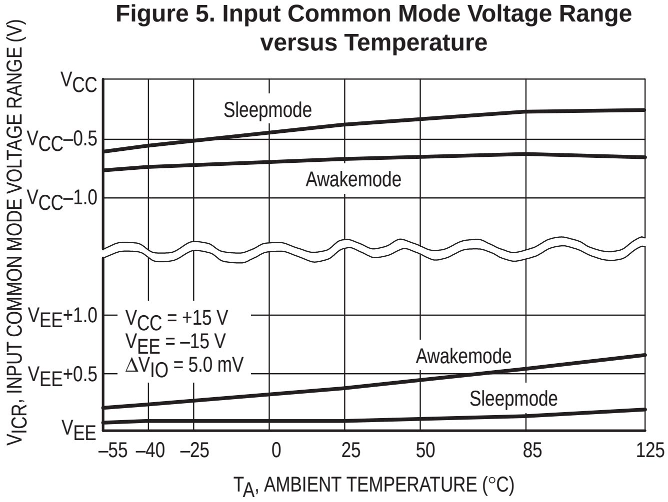


Figure 6. Input Bias Current versus Temperature

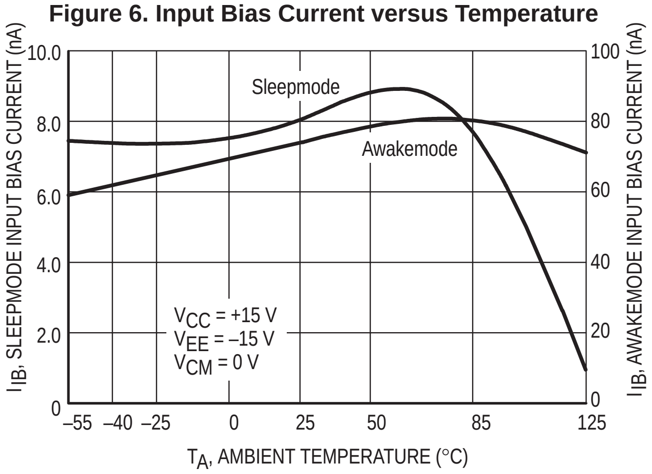


Figure 7. Open Loop Voltage Gain versus Temperature

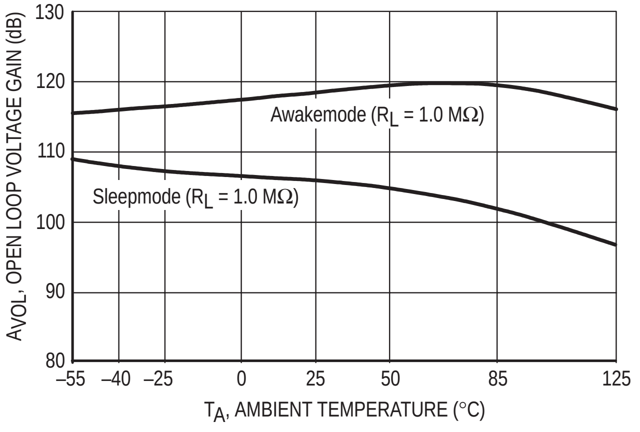


Figure 8. Output Voltage Swing versus Supply Voltage

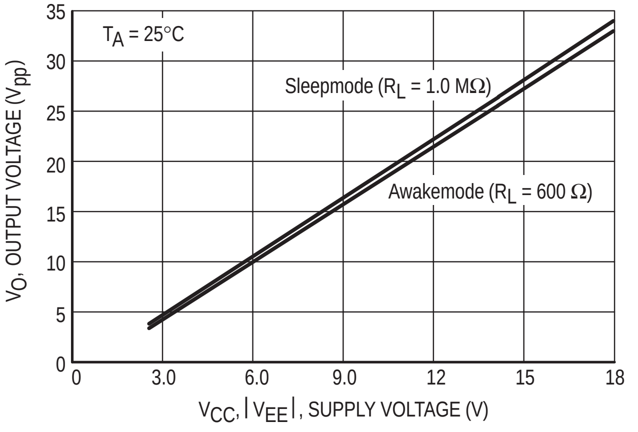


Figure 9. Output Voltage versus Frequency

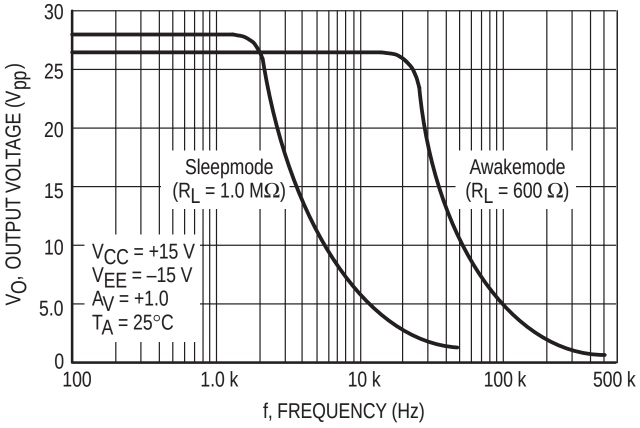


Figure 10. Maximum Peak–to–Peak Output Voltage Swing versus Load Resistance

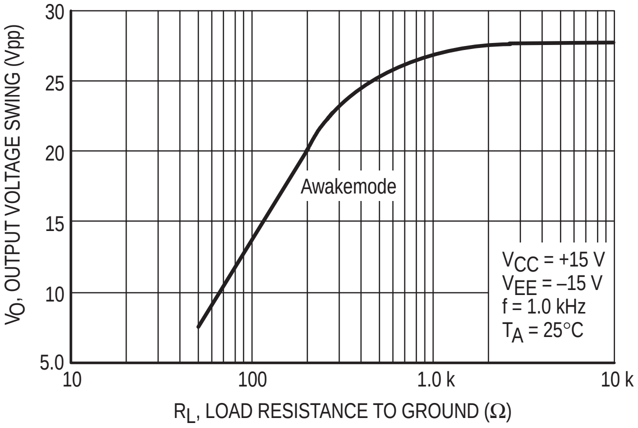


Figure 11. Common Mode Rejection versus Frequency

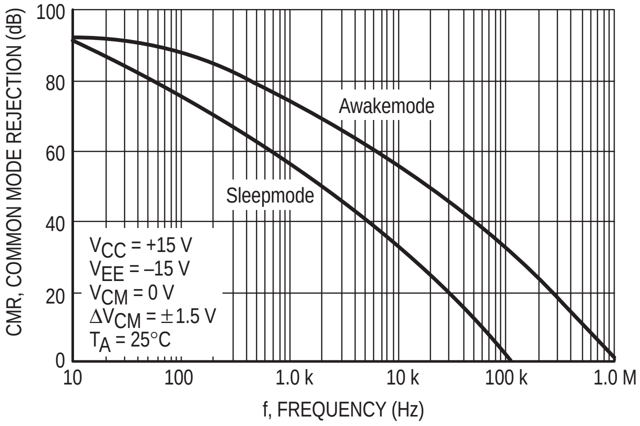


Figure 12. Power Supply Rejection versus Frequency

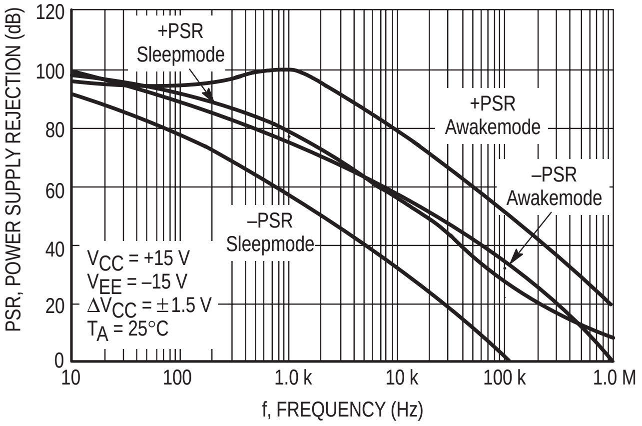


Figure 13. Sleepmode to Awakemode Current Threshold versus Supply Voltage

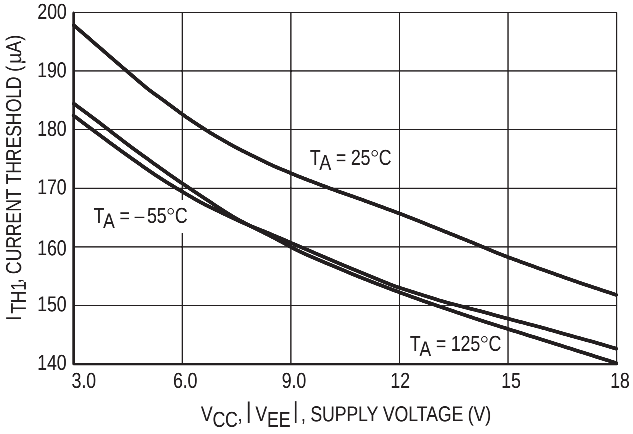


Figure 14. Awakemode to Sleepmode Current Threshold versus Supply Voltage

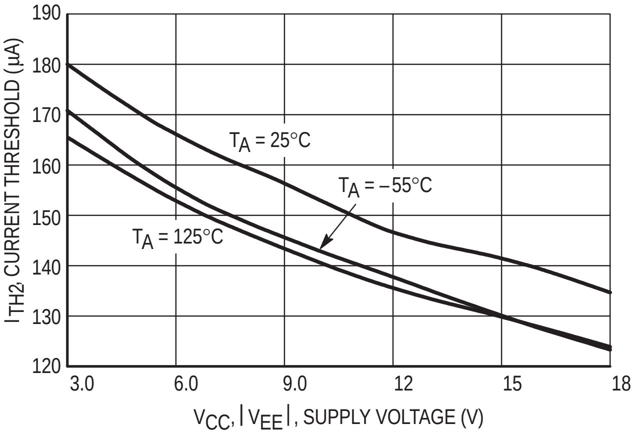


Figure 15. Output Short Circuit Current versus Output Voltage

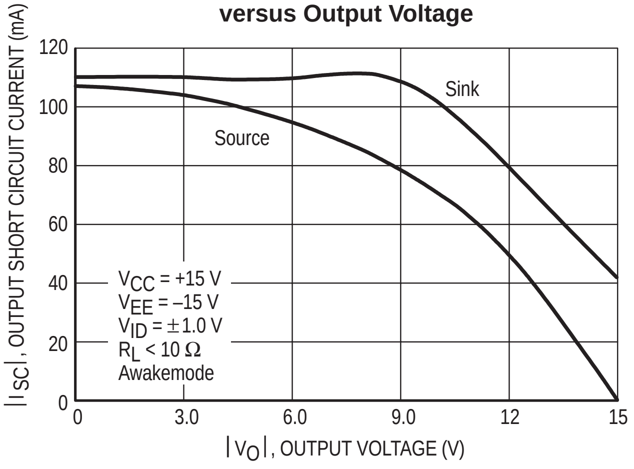


Figure 16. Output Short Circuit Current versus Temperature

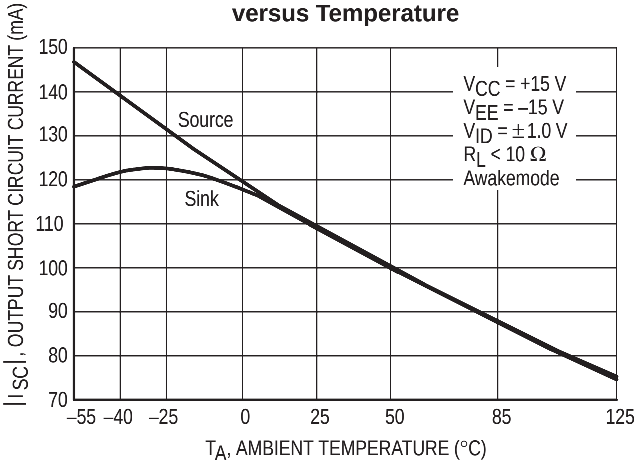


Figure 17. Power Supply Current Per Amplifier versus Temperature

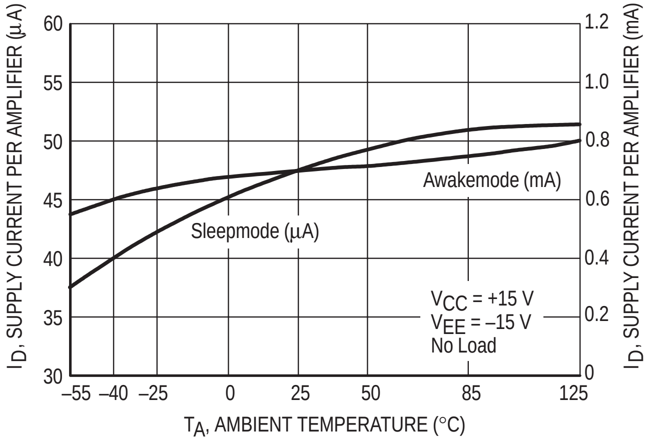


Figure 18. Slew Rate versus Temperature

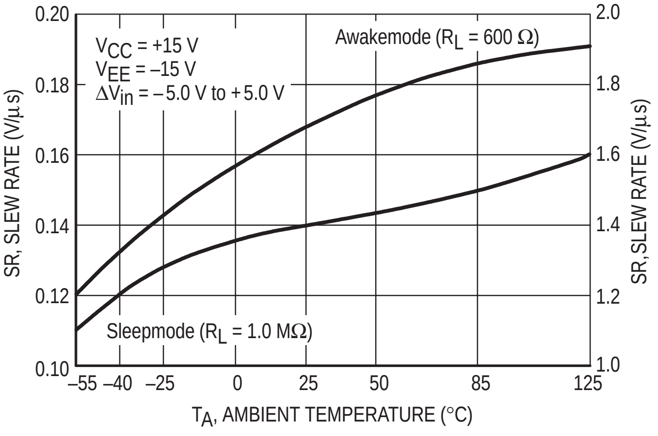


Figure 19. Gain Bandwidth Product versus Temperature

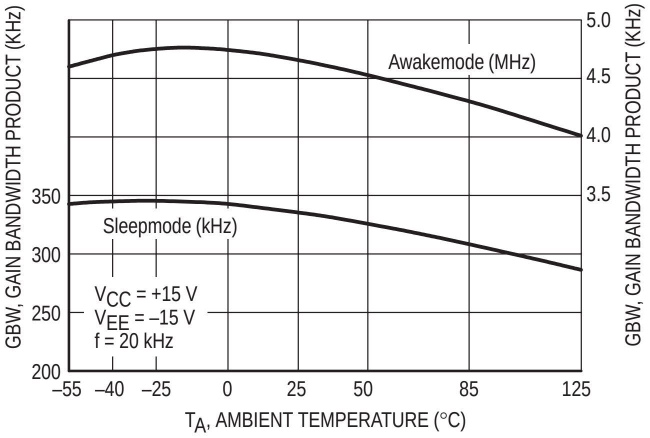


Figure 20. Sleepmode to Awakemode Transition Time

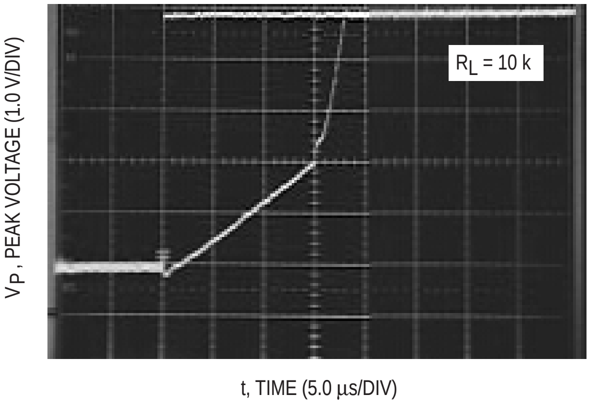


Figure 21. Sleepmode to Awakemode Transition Time

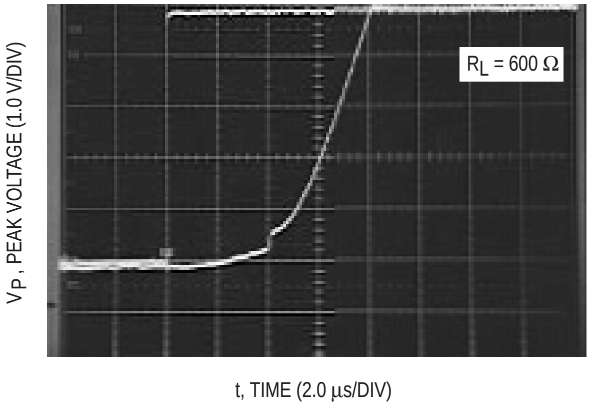


Figure 22. Awakemode to Sleepmode Transition Time versus Supply Voltage

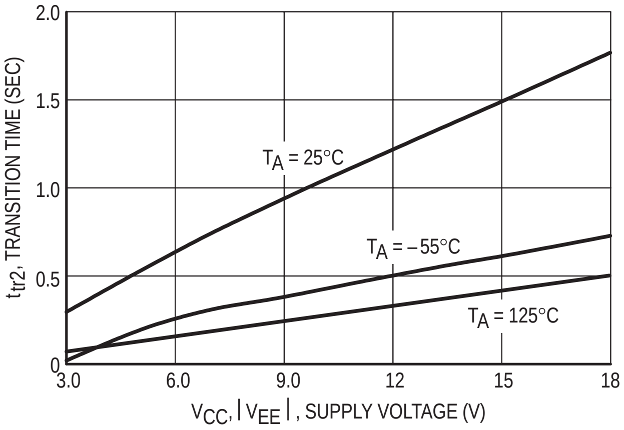


Figure 23. Gain Margin versus Differential Source Resistance

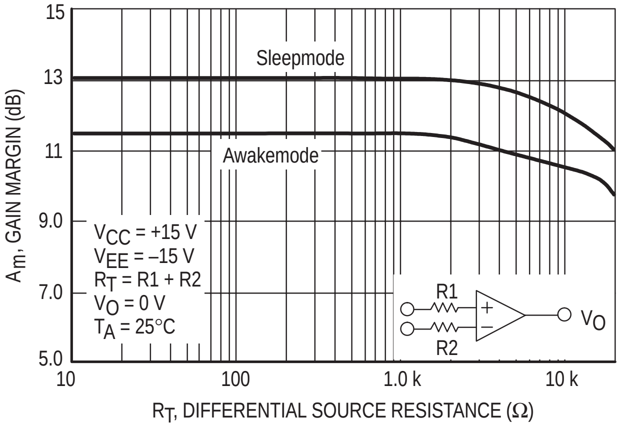


Figure 24. Phase Margin versus Differential Source Resistance

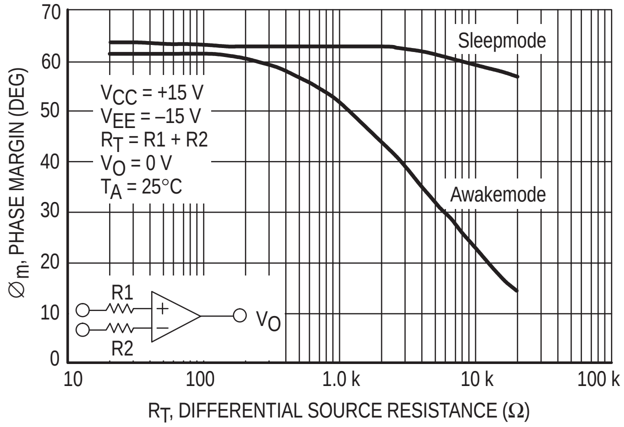


Figure 25. Open Loop Gain Margin versus Output Load Capacitance

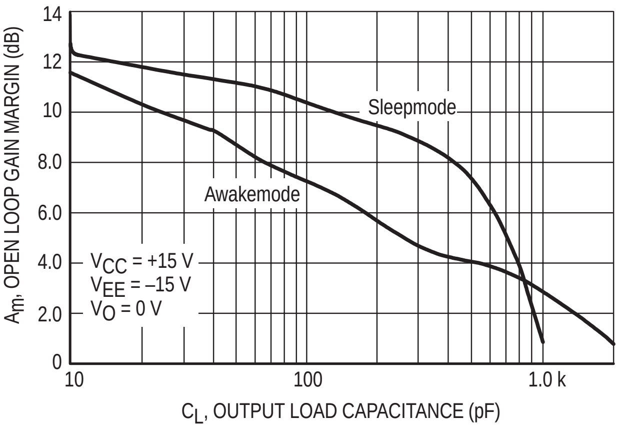


Figure 26. Phase Margin versus Output Load Capacitance

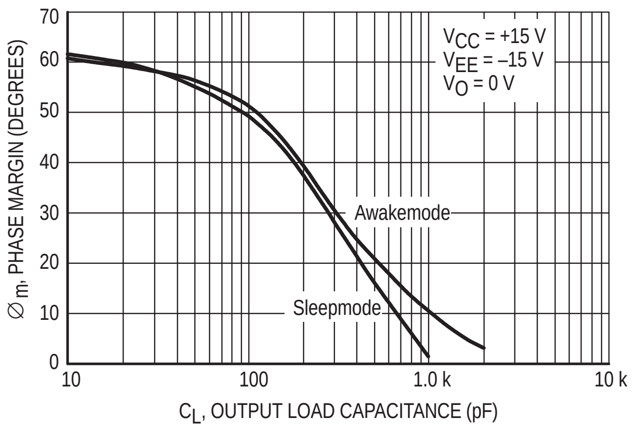


Figure 27. Sleepmode Voltage Gain and Phase versus Frequency

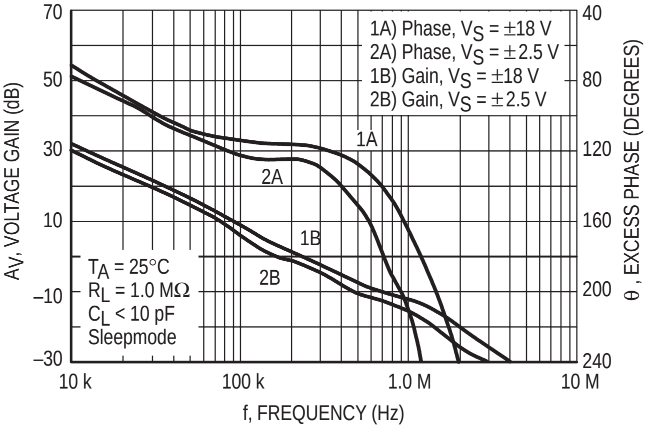


Figure 28. Awakemode Voltage Gain and Phase versus Frequency

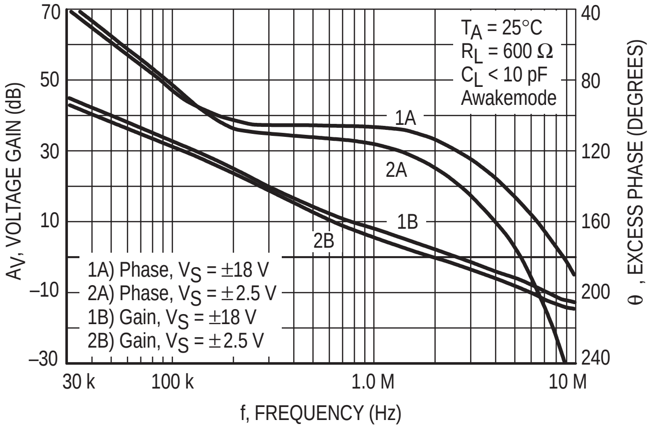


Figure 29. Channel Separation versus Frequency

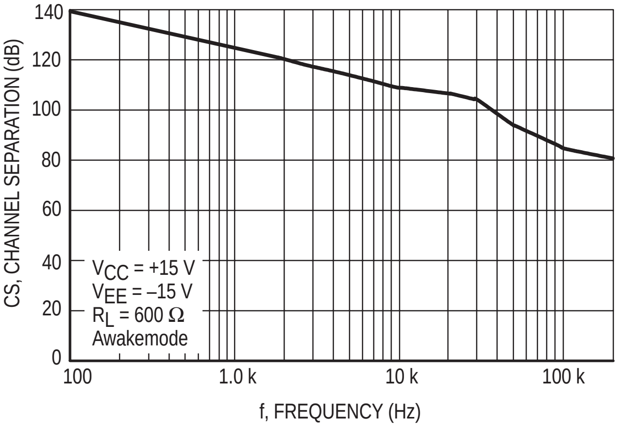


Figure 30. Total Harmonic Distortion versus Frequency

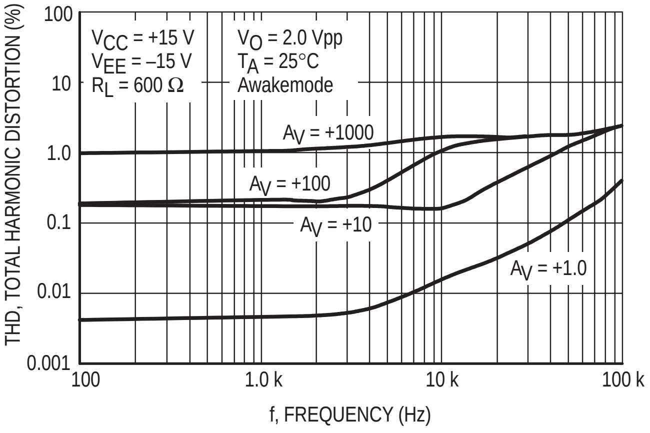


Figure 31. Awakemode Output Impedance versus Frequency

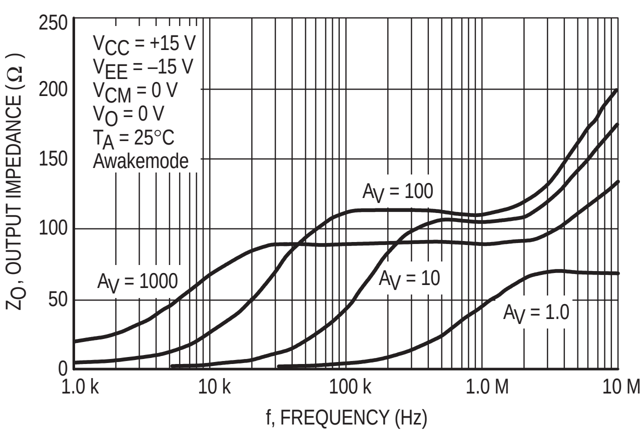


Figure 32. Input Referred Noise Voltage versus Frequency

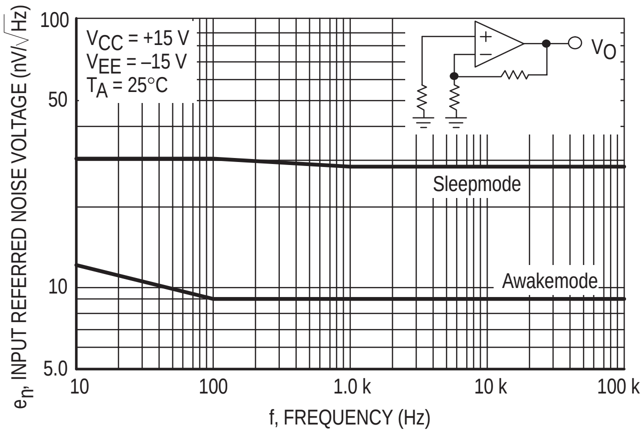


Figure 33. Current Noise versus Frequency

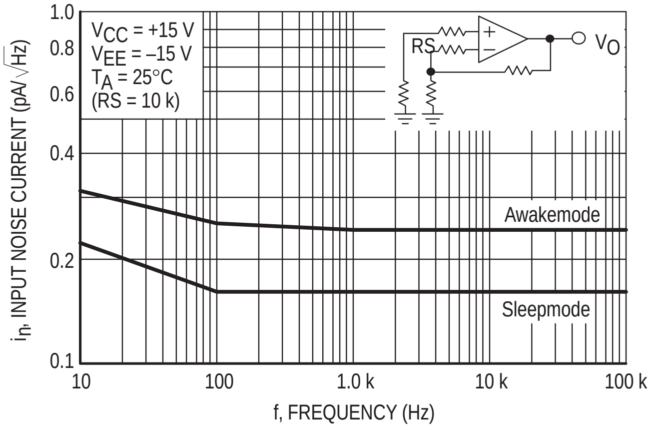


Figure 34. Percent Overshoot versus Load Capacitance

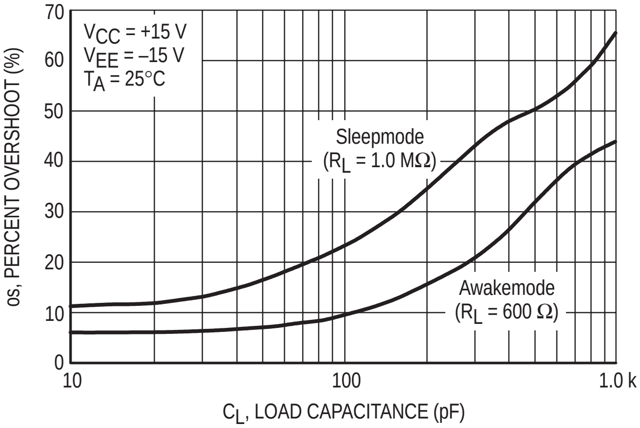


Figure 35. Sleepmode Large Signal Transient Response

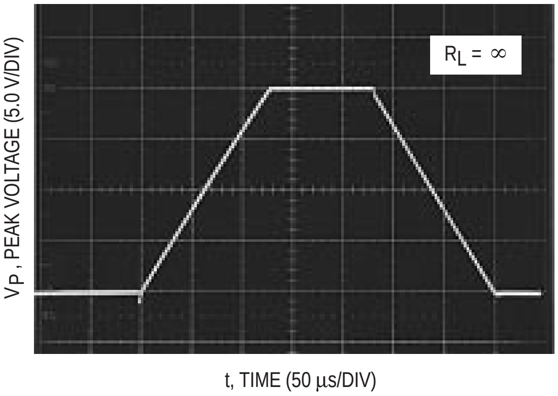


Figure 36. Awakemode Large Signal Transient Response

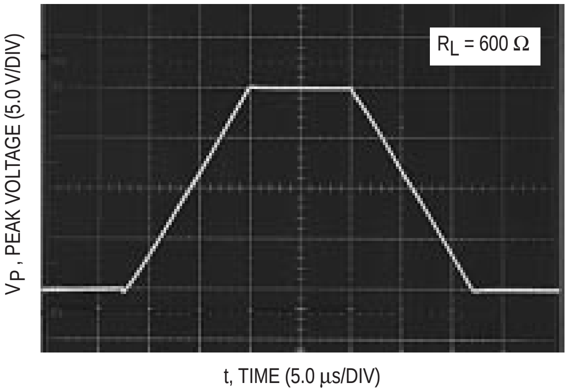


Figure 37. Sleepmode Small Signal Transient Response

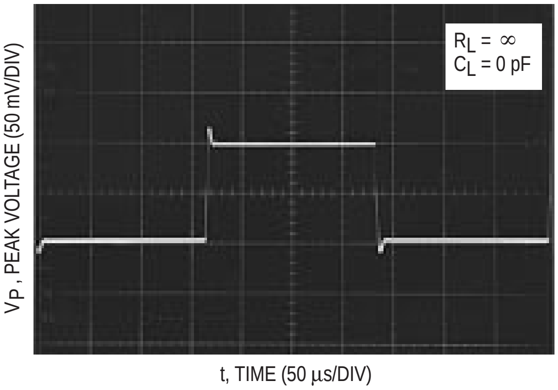
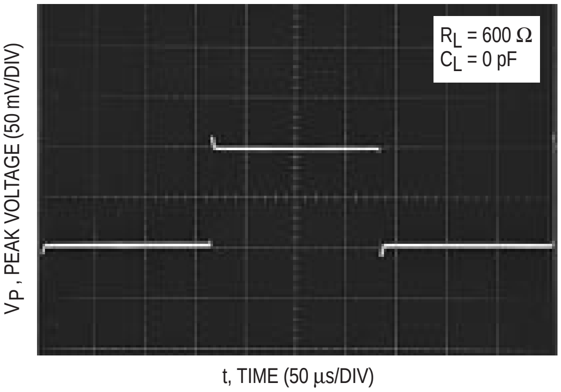


Figure 38. Awakemode Small Signal Transient Response



CIRCUIT INFORMATION

The MC33102 was designed primarily for applications where high performance (which requires higher current drain) is required only part of the time. The two–state feature of this op amp enables it to conserve power during idle times, yet be powered up and ready for an input signal. Possible applications include laptop computers, automotive, cordless phones, baby monitors, and battery operated test equipment. Although most applications will require low power consumption, this device can be used in any application where better efficiency and higher performance is needed.

The Sleep–Mode™ amplifier has two states; a sleepmode and an awakemode. In the sleepmode state, the amplifier is active and functions as a typical micropower op amp. When a signal is applied to the amplifier causing it to source or sink sufficient current (see Figure 13), the amplifier will automatically switch to the awakemode. See Figures 20 and 21 for transition times with 600 Ω and 10 kΩ loads.

The awakemode uses higher drain current to provide a high slew rate, gain bandwidth, and output current capability. In the awakemode, this amplifier can drive 27 Vpp into a 600 Ω load with $V_S = \pm 15$ V.

An internal delay circuit is used to prevent the amplifier from returning to the sleepmode at every zero crossing. This delay circuit also eliminates the crossover distortion commonly found in micropower amplifiers. This amplifier can process frequencies as low as 1.0 Hz without the amplifier returning to sleepmode, depending on the load.

The first stage PNP differential amplifier provides low noise performance in both the sleep and awake modes, and an all NPN output stage provides symmetrical source and sink AC frequency response.

APPLICATIONS INFORMATION

The MC33102 will begin to function at power supply voltages as low as $V_S = \pm 1.0$ V at room temperature. (At this voltage, the output voltage swing will be limited to a few hundred millivolts.) The input voltages must range between V_{CC} and V_{EE} supply voltages as shown in the maximum rating table. Specifically, **allowing the input to go more negative than 0.3 V below V_{EE} may cause product damage.** Also, exceeding the input common mode voltage range on either input may cause phase reversal, even if the inputs are between V_{CC} and V_{EE}.

When power is initially applied, the part may start to operate in the awakemode. This is because of the currents generated due to charging of internal capacitors. When this occurs and the sleepmode state is desired, the user will have to wait approximately 1.5 seconds before the device will switch back to the sleepmode. To prevent this from occurring, ramp the power supplies from 1.0 V to full supply. Notice that the device is more prone to switch into the awakemode when V_{EE} is adjusted than with a similar change in V_{CC}.

The amplifier is designed to switch from sleepmode to awakemode whenever the output current exceeds a preset current threshold (I_{TH}) of approximately 160 µA. As a result, the output switching threshold voltage (V_{ST}) is controlled by the output loading resistance (R_L). This loading can be a load resistor, feedback resistors, or both. Then:

$$V_{ST} = (160\ \mu A) \times R_L$$

Large valued load resistors require a large output voltage to switch, but reduce unwanted transitions to the awakemode. For instance, in cases where the amplifier is connected with a large closed loop gain (A_{CL}), the input offset voltage (V_{IO}) is multiplied by the gain at the output and could produce an output voltage exceeding V_{ST} with no input signal applied.

Small values of R_L allow rapid transition to the awakemode because most of the transition time is consumed slewing in the sleepmode until V_{ST} is reached (see Figures 20, 21). The output switching threshold voltage V_{ST} is higher for larger values of R_L, requiring the amplifier to slew longer in the slower sleepmode state before switching to the awakemode.

The transition time (t_{tr1}) required to switch from sleep to awake mode is:

$$t_{tr1} = t_D = I_{TH} (R_L/SR_{sleepmode})$$

Where: t_D = Amplifier delay (<1.0 μs)
I_{TH} = Output threshold current for more transition (160 μA)
R_L = Load resistance
$SR_{sleepmode}$ = Sleepmode slew rate (0.16 V/μs)

Although typically 160 μA, I_{TH} varies with supply voltage and temperature. In general, any current loading on the output which causes a current greater than I_{TH} to flow will switch the amplifier into the awakemode. This includes transition currents such as those generated by charging load capacitances. In fact, the maximum capacitance that can be driven while attempting to remain in the sleepmode is approximately 1000 pF.

$$\begin{aligned} C_{L(max)} &= I_{TH}/SR_{sleepmode} \\ &= 160\ \mu A/(0.16\ V/\mu s) \\ &= 1000\ pF \end{aligned}$$

Any electrical noise seen at the output of the MC33102 may also cause the device to transition to the awakemode. To minimize this problem, a resistor may be added in series with the output of the device (inserted as close to the device as possible) to isolate the op amp from both parasitic and load capacitance.

The awakemode to sleepmode transition time is controlled by an internal delay circuit, which is necessary to prevent the amplifier from going to sleep during every zero crossing. This time is a function of supply voltage and temperature as shown in Figure 22.

Gain bandwidth product (GBW) in both modes is an important system design consideration when using a sleepmode amplifier. The amplifier has been designed to obtain the maximum GBW in both modes. “Smooth” AC transitions between modes with no noticeable change in the amplitude of the output voltage waveform will occur as long as the closed loop gains (A_{CL}) in both modes are substantially equal at the frequency of operation. For smooth AC transitions:

$$(A_{CLsleepmode})\ (BW) < GBW_{sleepmode}$$

Where: $A_{CLsleepmode}$ = Closed loop gain in the sleepmode
BW = The required system bandwidth or operating frequency

TESTING INFORMATION

To determine if the MC33102 is in the awakemode or the sleepmode, the power supply currents (I_D+ and I_D–) must be measured. When the magnitude of **either** power supply current exceeds 400 μA, the device is in the awakemode. When the magnitudes of both supply currents are less than 400 μA, the device is in the sleepmode. Since the total supply current is typically ten times higher in the awakemode than the sleepmode, the two states are easily distinguishable.

The measured value of I_D+ equals the I_D of both devices (for a dual op amp) plus the output source current of device A and the output source current of device B. Similarly, the measured value of I_D– is equal to the I_D– of both devices plus the output sink current of each device. I_{out} is the sum of the currents caused by both the feedback loop and load resistance. The total I_{out} needs to be subtracted from the measured I_D to obtain the correct I_D of the dual op amp.

An accurate way to measure the awakemode I_{out} current on automatic test equipment is to remove the I_{out} current on both Channel A and B. Then measure the I_D values before the device goes back to the sleepmode state. The transition will take typically 1.5 seconds with ±15 V power supplies.

The large signal sleepmode testing in the characterization was accomplished with a 1.0 MΩ load resistor which ensured the device would remain in sleepmode despite large voltage swings.

MOTOROLA

MC33171
MC33172
MC33174

Low Power, Single Supply Operational Amplifiers

Quality bipolar fabrication with innovative design concepts are employed for the MC33171/72/74 series of monolithic operational amplifiers. These devices operate at 180 µA per amplifier and offer 1.8 MHz of gain bandwidth product and 2.1 V/µs slew rate without the use of JFET device technology. Although this series can be operated from split supplies, it is particularly suited for single supply operation, since the common mode input voltage includes ground potential (V_{EE}). With a Darlington input stage, these devices exhibit high input resistance, low input offset voltage and high gain. The all NPN output stage, characterized by no deadband crossover distortion and large output voltage swing, provides high capacitance drive capability, excellent phase and gain margins, low open loop high frequency output impedance and symmetrical source/sink AC frequency response.

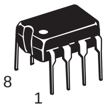
The MC33171/72/74 are specified over the industrial/ automotive temperature ranges. The complete series of single, dual and quad operational amplifiers are available in plastic as well as the surface mount packages.

- Low Supply Current: 180 µA (Per Amplifier)
- Wide Supply Operating Range: 3.0 V to 44 V or ±1.5 V to ±22 V
- Wide Input Common Mode Range, Including Ground (V_{EE})
- Wide Bandwidth: 1.8 MHz
- High Slew Rate: 2.1 V/µs
- Low Input Offset Voltage: 2.0 mV
- Large Output Voltage Swing: –14.2 V to +14.2 V (with ±15 V Supplies)
- Large Capacitance Drive Capability: 0 pF to 500 pF
- Low Total Harmonic Distortion: 0.03%
- Excellent Phase Margin: 60°C
- Excellent Gain Margin: 15 dB
- Output Short Circuit Protection
- ESD Diodes Provide Input Protection for Dual and Quad

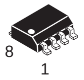
ORDERING INFORMATION

Op Amp Function	Device	Operating Temperature Range	Package
Single	MC33171D MC33171P	T_A = –40° to +85°C T_A = –40° to +85°C	SO–8 Plastic DIP
Dual	MC33172D MC33172P	T_A = –40° to +85°C T_A = –40° to +85°C	SO–8 Plastic DIP
Quad	MC33174D MC33174P	T_A = –40° to +85°C T_A = –40° to +85°C	SO–14 Plastic DIP

DUAL

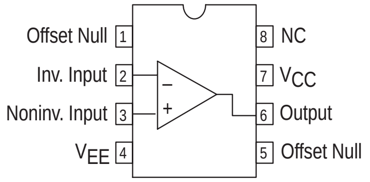


P SUFFIX
PLASTIC PACKAGE
CASE 626

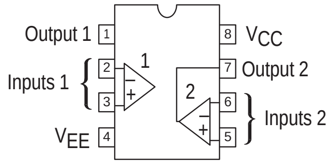


D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

PIN CONNECTIONS

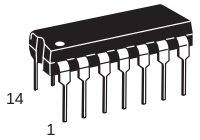


(Single, Top View)

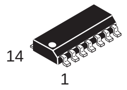


(Top View)

QUAD

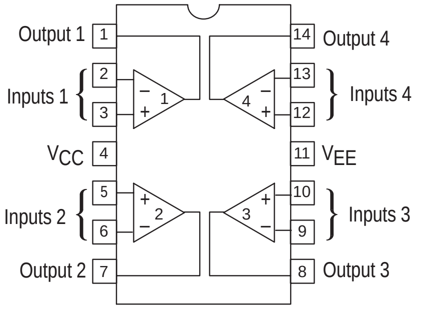


P SUFFIX
PLASTIC PACKAGE
CASE 646



D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO–14)

PIN CONNECTIONS



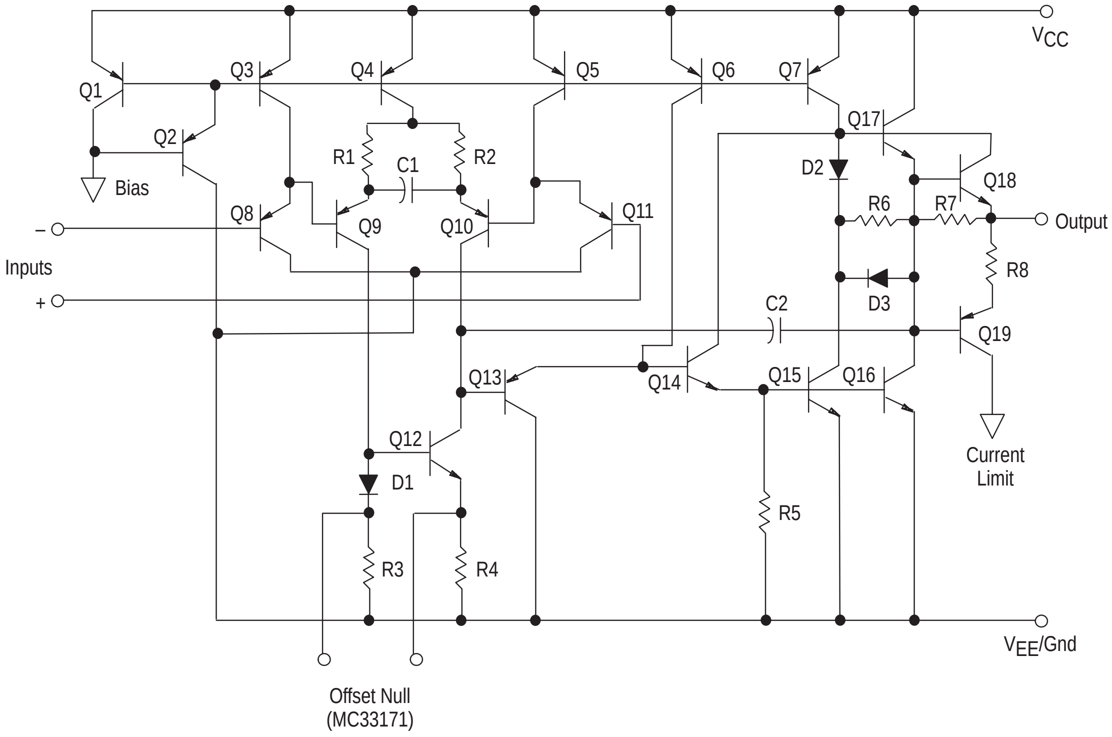
(Top View)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}/V_{EE}	±22	V
Input Differential Voltage Range	V_{IDR}	(Note 1)	V
Input Voltage Range	V_{IR}	(Note 1)	V
Output Short Circuit Duration (Note 2)	t_{SC}	Indefinite	sec
Operating Ambient Temperature Range	T_A	–40 to +85	°C
Operating Junction Temperature	T_J	+150	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

NOTES: 1. Either or both input voltages must not exceed the magnitude of V_{CC} or V_{EE}.
2. Power dissipation must be considered to ensure maximum junction temperature (T_J) is not exceeded.

Representative Schematic Diagram
(Each Amplifier)



DC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = –15 V, R_L connected to ground, T_A = T_{low} to T_{high} [Note 3], unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Input Offset Voltage (V_{CM} = 0 V)	V_{IO}				mV
V_{CC} = +15 V, V_{EE} = –15 V, T_A = +25°C		—	2.0	4.5	
V_{CC} = +5.0 V, V_{EE} = 0 V, T_A = +25°C		—	2.5	5.0	
V_{CC} = +15 V, V_{EE} = –15 V, T_A = T_{low} to T_{high}		—	—	6.5	
Average Temperature Coefficient of Offset Voltage	$\Delta V_{IO}/\Delta T$	—	10	—	µV/°C
Input Bias Current (V_{CM} = 0 V)	I_{IB}				nA
T_A = +25°C		—	20	100	
T_A = T_{low} to T_{high}		—	—	200	
Input Offset Current (V_{CM} = 0 V)	I_{IO}				nA
T_A = +25°C		—	5.0	20	
T_A = T_{low} to T_{high}		—	—	40	
Large Signal Voltage Gain (V_O = ±10 V< R_L = 10 k)	A_{VOL}				V/mV
T_A = +25°C		50	500	—	
T_A = T_{low} to T_{high}		25	—	—	
Output Voltage Swing	V_{OH}				V
V_{CC} = +5.0 V, V_{EE} = 0 V, R_L = 10 k, T_A = +25°C		3.5	4.3	—	
V_{CC} = +15 V, V_{EE} = –15 V, R_L = 10 k, T_A = +25°C		13.6	14.2	—	
V_{CC} = +15 V, V_{EE} = –15 V, R_L = 10 k, T_A = T_{low} to T_{high}		13.3	—	—	
V_{CC} = +5.0 V, V_{EE} = 0 V, R_L = 10 k, T_A = +25°C	V_{OL}	—	0.05	0.15	
V_{CC} = +15 V, V_{EE} = –15 V, R_L = 10 k, T_A = +25°C		—	–14.2	–13.6	
V_{CC} = +15 V, V_{EE} = –15 V, R_L = 10 k, T_A = T_{low} to T_{high}		—	—	–13.3	
Output Short Circuit (T_A = +25°C)	I_{SC}				mA
Input Overdrive = 1.0 V, Output to Ground					
Source		3.0	5.0	—	
Sink		15	27	—	
Input Common Mode Voltage Range	V_{ICR}				V
T_A = +25°C		V_{EE} to (V_{CC} –1.8)			
T_A = T_{low} to T_{high}		V_{EE} to (V_{CC} –2.2)			
Common Mode Rejection Ratio (R_S ≤ 10 k) T_A = +25°C	CMRR	80	90	—	dB
Power Supply Rejection Ratio (R_S = 100 Ω) T_A = +25°C	PSRR	80	100	—	dB
Power Supply Current (Per Amplifier)	I_D				µA
V_{CC} = +5.0 V, V_{EE} = 0 V, T_A = +25°C		—	180	250	
V_{CC} = +15 V, V_{EE} = –15 V, T_A = +25°C		—	220	250	
V_{CC} = +15 V, V_{EE} = –15 V, T_A = T_{low} to T_{high}		—	—	300	

NOTE: 3. T_{low} = –40°C T_{high} = +85°C

AC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = –15 V, R_L connected to ground, T_A = +25°C, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Slew Rate (V_{in} = –10 V to +10 V, R_L = 10 k, C_L = 100 pF) A_V +1 A_V –1	SR	 1.6 —	 2.1 2.1	 — —	V/µs
Gain Bandwidth Product (f = 100 kHz)	GBW	1.4	1.8	—	MHz
Power Bandwidth A_V = +1.0 R_L = 10 k, V_O = 20 V_{pp}, THD = 5%	BWp	—	35	—	kHz
Phase Margin R_L = 10 k R_L = 10 k, C_L = 100 pF	ϕ_m	 — —	 60 45	 — —	Degrees
Gain Margin R_L = 10 k R_L = 10 k, C_L = 100 pF	A_m	 — —	 15 5.0	 — —	dB
Equivalent Input Noise Voltage R_S = 100 Ω, f = 1.0 kHz	e_n	—	32	—	nV/$\sqrt{Hz}$
Equivalent Input Noise Current (f = 1.0 kHz)	I_n	—	0.2	—	pA/$\sqrt{Hz}$
Differential Input Resistance V_{cm} = 0 V	R_{in}	—	300	—	MΩ
Input Capacitance	C_i	—	0.8	—	pF
Total Harmonic Distortion A_V = +10, R_L = 10 k, 2.0 V_{pp} ≤ V_O ≤ 20 V_{pp}, f = 10 kHz	THD	—	0.03	—	%
Channel Separation (f = 10 kHz)	CS	—	120	—	dB
Open Loop Output Impedance (f = 1.0 MHz)	z_o	—	100	—	Ω

Figure 1. Input Common Mode Voltage Range versus Temperature

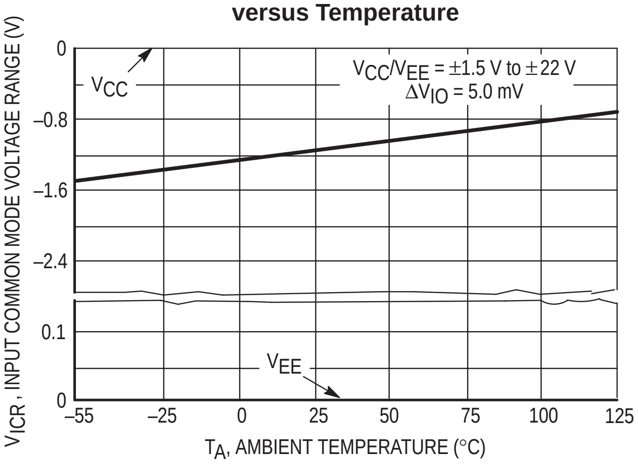


Figure 2. Split Supply Output Saturation versus Load Current

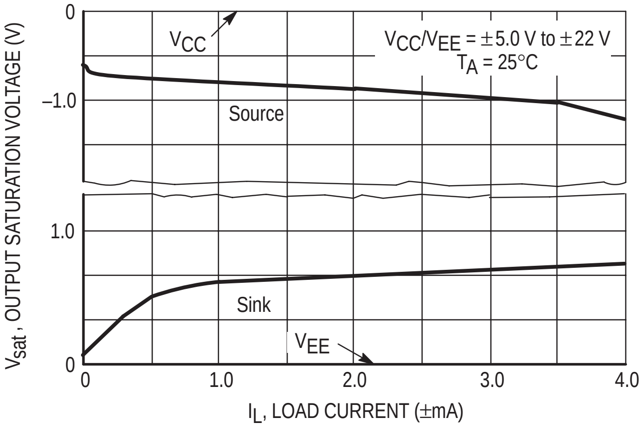


Figure 3. Open Loop Voltage Gain and Phase versus Frequency

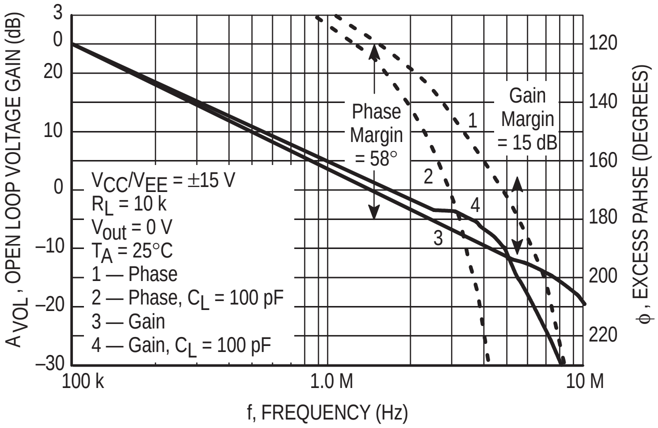


Figure 4. Phase Margin and Percent Overshoot versus Load Capacitance

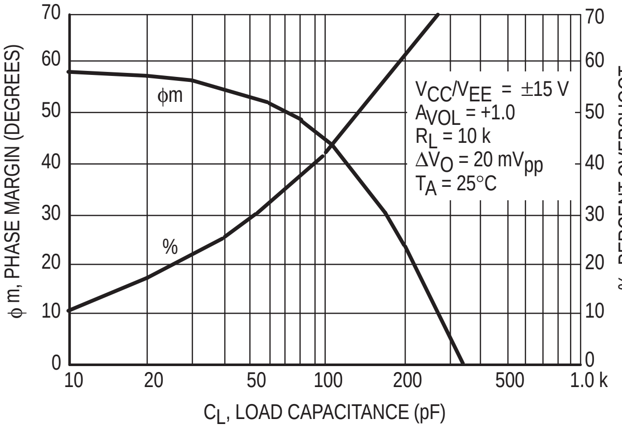


Figure 5. Normalized Gain Bandwidth Product and Slew Rate versus Temperature

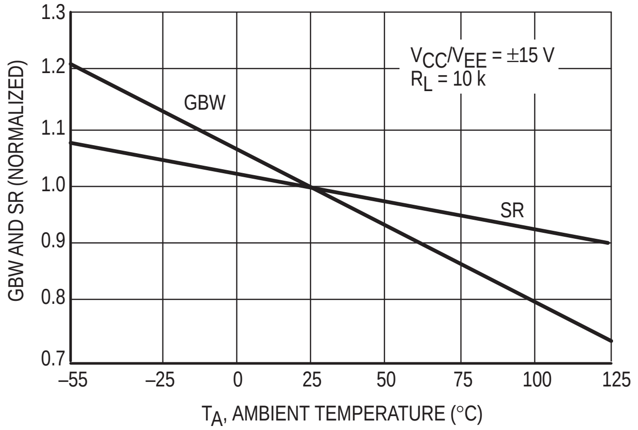


Figure 6. Small and Large Signal Transient Response

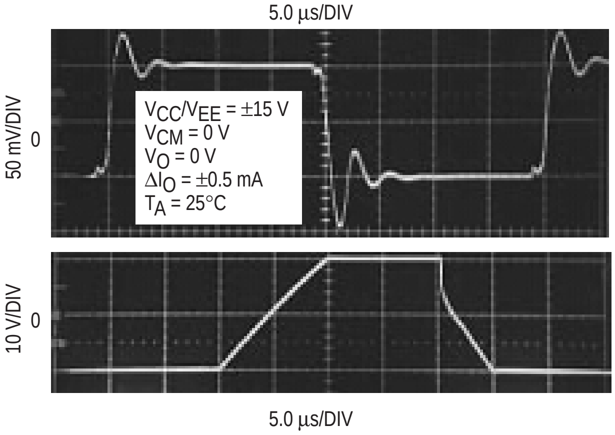


Figure 7. Output Impedance and Frequency

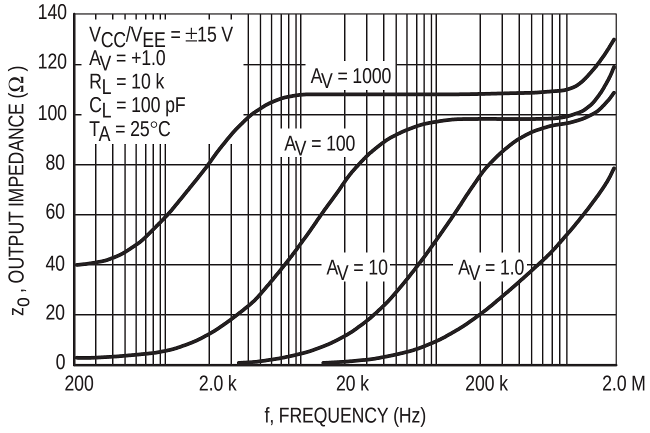
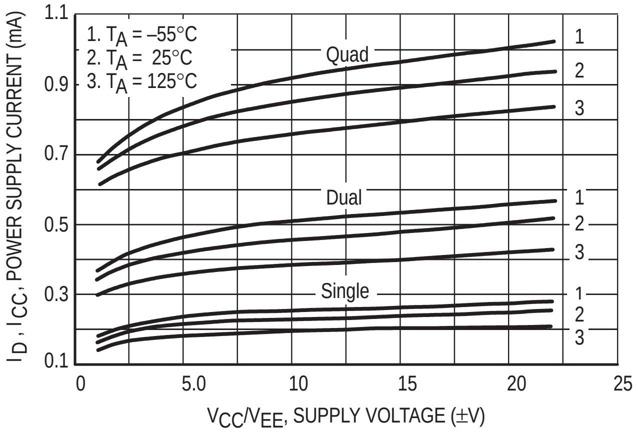


Figure 8. Supply Current versus Supply Voltage



APPLICATIONS INFORMATION – CIRCUIT DESCRIPTION/PERFORMANCE FEATURES

Although the bandwidth, slew rate, and settling time of the MC33171/72/74 amplifier family is similar to low power op amp products utilizing JFET input devices, these amplifiers offer additional advantages as a result of the PNP transistor differential inputs and an all NPN transistor output stage.

Because the input common mode voltage range of this input stage includes the V_{EE} potential, single supply operation is feasible to as low as 3.0 V with the common mode input voltage at ground potential.

The input stage also allows differential input voltages up to ±44 V, provided the maximum input voltage range is not exceeded. Specifically, the input voltages must range between V_{CC} and V_{EE} supply voltages as shown by the maximum rating table. In practice, although *not recommended,* the input voltages can exceed the V_{CC} voltage by approximately 3.0 V and decrease below the V_{EE} voltage by 0.3 V without causing product damage, although output phase reversal may occur. It is also possible to source up to 5.0 mA of current from V_{EE} through either inputs' clamping diode without damage or latching, but phase reversal may again occur. If at least one input is within the common mode input voltage range and the other input is within the maximum input voltage range, no phase reversal will occur. If both inputs exceed the upper common mode input voltage limit, the output will be forced to its lowest voltage state.

Since the input capacitance associated with the small geometry input device is substantially lower (0.8 pF) than that of a typical JFET (3.0 pF), the frequency response for a given input source resistance is greatly enhanced. This becomes evident in D–to–A current to voltage conversion applications where the feedback resistance can form a pole with the input capacitance of the op amp. This input pole creates a 2nd Order system with the single pole op amp and is therefore detrimental to its settling time. In this context, lower input capacitance is desirable especially for higher values of feedback resistances (lower current DACs). This input pole can be compensated for by creating a feedback zero with a capacitance across the feedback resistance, if necessary, to reduce overshoot. For 10 kΩ of feedback resistance, the MC33171/72/74 family can typically settle to within 1/2 LSB of 8 bits in 4.2 µs, and within 1/2 LSB of 12 bits in 4.8 µs for a 10 V step. In a standard inverting unity gain fast settling configuration, the symmetrical slew rate is typically ± 2.1 V/µs. In the classic noninverting unity gain configuration the typical output positive slew rate is also 2.1 V/µs, and the corresponding negative slew rate will usually exceed the positive slew rate as a function of the fall time of the input waveform.

The all NPN output stage, shown in its basic form on the equivalent circuit schematic, offers unique advantages over the more conventional NPN/PNP transistor Class AB output stage. A 10 kΩ load resistance can typically swing within 0.8 V of the positive rail (V_{CC}) and negative rail (V_{EE}), providing a 28.4 Vpp swing from ±15 V supplies. This large output swing becomes most noticeable at lower supply voltages.

The positive swing is limited by the saturation voltage of the current source transistor Q7, the V_{BE} of the NPN pull–up transistor Q17, and the voltage drop associated with the short circuit resistance, R5. For sink currents less than 0.4 mA, the negative swing is limited by the saturation voltage of the pull–down transistor Q15, and the voltage drop across R4 and R5. For small valued sink currents, the above voltage drops are negligible, allowing the negative swing voltage to approach within millivolts of V_{EE}. For sink currents (> 0.4 mA), diode D3 clamps the voltage across R4. Thus the negative swing is limited by the saturation voltage of Q15, plus the forward diode drop of D3 (≈V_{EE} +1.0 V). Therefore an unprecedented peak–to–peak output voltage swing is possible for a given supply voltage as indicated by the output swing specifications.

If the load resistance is referenced to V_{CC} instead of ground for single supply applications, the maximum possible output swing can be achieved for a given supply voltage. For light load currents, the load resistance will pull the output to V_{CC} during the positive swing and the output will pull the load resistance near ground during the negative swing. The load resistance value should be much less than that of the feedback resistance to maximize pull–up capability.

Because the PNP output emitter–follower transistor has been eliminated, the MC33171/72/74 family offers a 15 mA minimum current sink capability, typically to an output voltage of (V_{EE} +1.8 V). In single supply applications the output can directly source or sink base current from a common emitter NPN transistor for current switching applications.

In addition, the all NPN transistor output stage is inherently faster than PNP types, contributing to the bipolar amplifier's improved gain bandwidth product. The associated high frequency low output impedance (200 Ω typ @ 1.0 MHz) allows capacitive drive capability from 0 pF to 400 pF without oscillation in the noninverting unity gain configuration. The 60°C phase margin and 15 dB gain margin, as well as the general gain and phase characteristics, are virtually independent of the source/sink output swing conditions. This allows easier system phase compensation, since output swing will not be a phase consideration. The AC characteristics of the MC33171/72/74 family also allow excellent active filter capability, especially for low voltage single supply applications.

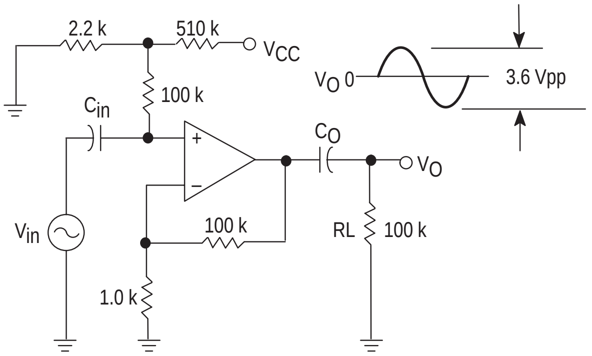
Although the single supply specification is defined at 5.0 V, these amplifiers are functional to at least 3.0 V @ 25°C. However slight changes in parametrics such as bandwidth, slew rate, and DC gain may occur.

If power to this integrated circuit is applied in reverse polarity, or if the IC is installed backwards in a socket, large unlimited current surges will occur through the device that may result in device destruction.

As usual with most high frequency amplifiers, proper lead dress, component placement and PC board layout should be exercised for optimum frequency performance. For example, long unshielded input or output leads may result in unwanted input/output coupling. In order to preserve the relatively low input capacitance associated with these amplifiers, resistors connected to the inputs should be immediately adjacent to the input pin to minimize additional stray input capacitance. This not only minimizes the input pole for optimum frequency response, but also minimizes extraneous "pick up" at this node. Supply decoupling with adequate capacitance immediately adjacent to the supply pin is also important, particularly over temperature, since many types of decoupling capacitors exhibit great impedance changes over temperature.

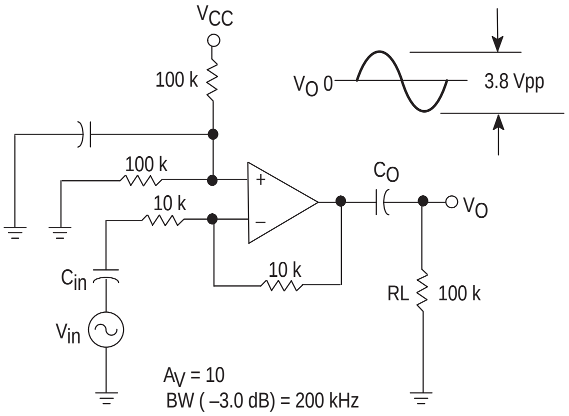
The output of any one amplifier is current limited and thus protected from a direct short to ground. However, under such conditions, it is important not to allow the device to exceed the maximum junction temperature rating. Typically for ±15 V supplies, any one output can be shorted continuously to ground without exceeding the maximum temperature rating.

Figure 9. AC Coupled Noninverting Amplifier with Single +5.0 V Supply



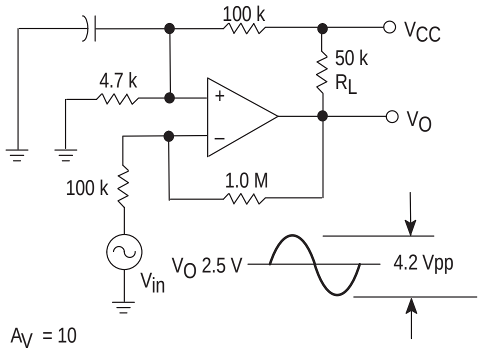
$A_V = 101$
BW (–3.0 dB) = 20 kHz

Figure 10. AC Coupled Inverting Amplifier with Single +5.0 V Supply



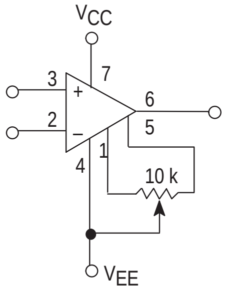
$A_V = 10$
BW (–3.0 dB) = 200 kHz

Figure 11. DC Coupled Inverting Amplifier Maximum Output Swing with Single +5.0 V Supply



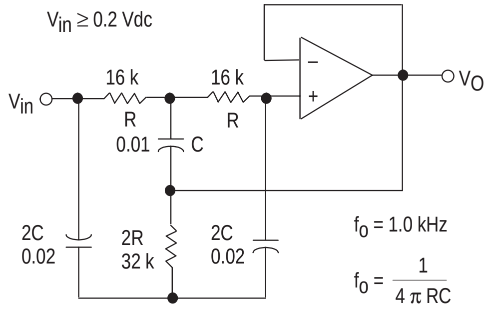
$A_V = 10$
BW (–3.0 dB) = 200 kHz

Figure 12. Offset Nulling Circuit



Offset Nulling range is approximately ±80 mV with a 10 k potentiometer, MC33171 only.

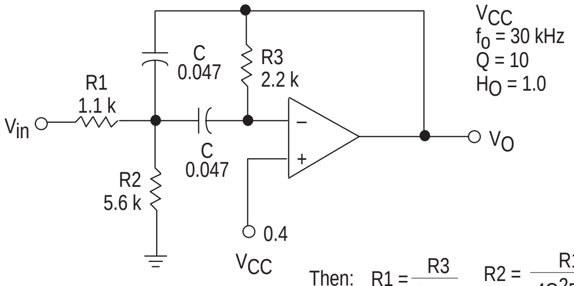
Figure 13. Active High–Q Notch Filter



$f_0 = 1.0$ kHz

$$f_0 = \frac{1}{4\,\pi\, RC}$$

Figure 14. Active Bandpass Filter



$f_0 = 30$ kHz
$Q = 10$
$H_O = 1.0$

Then: $R1 = \frac{R3}{2\,H_O}$ $R2 = \frac{R1\,R3}{4Q^2 R1 - R3}$

$R3 = \frac{Q}{\pi\, f_0 C}$ $\frac{Q_0\ f_0}{GBW} < 0.1$

Given f_0 = center frequency
A_0 = Gain at center frequency
Choose Value f_0, Q, A_0, C
For less than 10% error for operational amplifier, where f_0 and GBW are expressed in Hz.

MOTOROLA

MC33178
MC33179

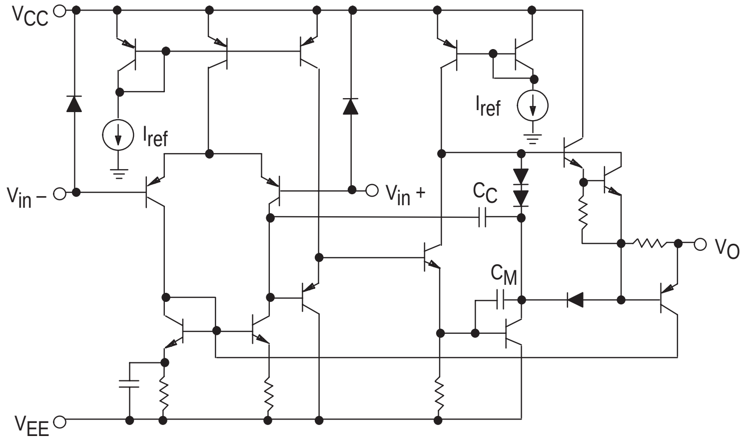
High Output Current Low Power, Low Noise Bipolar Operational Amplifiers

The MC33178/9 series is a family of high quality monolithic amplifiers employing Bipolar technology with innovative high performance concepts for quality audio and data signal processing applications. This device family incorporates the use of high frequency PNP input transistors to produce amplifiers exhibiting low input offset voltage, noise and distortion. In addition, the amplifier provides high output current drive capability while consuming only 420 µA of drain current per amplifier. The NPN output stage used, exhibits no deadband crossover distortion, large output voltage swing, excellent phase and gain margins, low open–loop high frequency output impedance, symmetrical source and sink AC frequency performance.

The MC33178/9 family offers both dual and quad amplifier versions, tested over the vehicular temperature range, and are available in DIP and SOIC packages.

- 600 Ω Output Drive Capability
- Large Output Voltage Swing
- Low Offset Voltage: 0.15 mV (Mean)
- Low T.C. of Input Offset Voltage: 2.0 µV/°C
- Low Total Harmonic Distortion: 0.0024% (@ 1.0 kHz w/600 Ω Load)
- High Gain Bandwidth: 5.0 MHz
- High Slew Rate: 2.0 V/µs
- Dual Supply Operation: ±2.0 V to ±18 V
- ESD Clamps on the Inputs Increase Ruggedness without Affecting Device Performance

Representative Schematic Diagram (Each Amplifier)

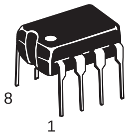


ORDERING INFORMATION

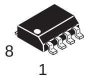
Op Amp Function	Fully Compensated	Operating Temperature Range	Package
Dual	MC33178D MC33178P	T_A = –40° to +85°C	SO–8 Plastic DIP
Quad	MC33179D MC33179P		SO–14 Plastic DIP

HIGH OUTPUT CURRENT LOW POWER, LOW NOISE OPERATIONAL AMPLIFIERS

DUAL

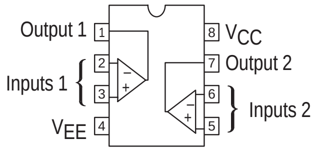


P SUFFIX
PLASTIC PACKAGE
CASE 626



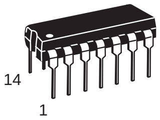
D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

PIN CONNECTIONS

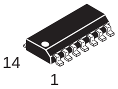


(Top View)

QUAD

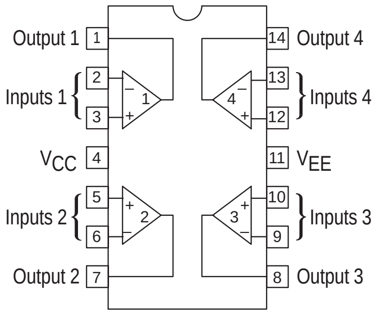


P SUFFIX
PLASTIC PACKAGE
CASE 646



D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO–14)

PIN CONNECTIONS



(Top View)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage (V_{CC} to V_{EE})	V_S	+36	V
Input Differential Voltage Range	V_{IDR}	(Note 1)	V
Input Voltage Range	V_{IR}	(Note 1)	V
Output Short Circuit Duration (Note 2)	t_{SC}	Indefinite	sec
Maximum Junction Temperature	T_J	+150	°C
Storage Temperature Range	T_{stg}	–60 to +150	°C
Maximum Power Dissipation	P_D	(Note 2)	mW

NOTES: 1. Either or both input voltages should not exceed V_{CC} or V_{EE}.
2. Power dissipation must be considered to ensure maximum junction temperature (T_J) is not exceeded. (See power dissipation performance characteristic, Figure 1.)

DC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = –15 V, T_A = 25°C, unless otherwise noted.)

Characteristics	Figure	Symbol	Min	Typ	Max	Unit
Input Offset Voltage (R_S = 50 Ω, V_{CM} = 0 V, V_O = 0 V)	2	$\lvert V_{IO}\rvert$				mV
(V_{CC} = +2.5 V, V_{EE} = –2.5 V to V_{CC} = +15 V, V_{EE} = –15 V)						
T_A = +25°C			—	0.15	3.0	
T_A = –40° to +85°C			—	—	4.0	
Average Temperature Coefficient of Input Offset Voltage	2	$\Delta V_{IO}/\Delta T$				µV/°C
(R_S = 50 Ω, V_{CM} = 0 V, V_O = 0 V)						
T_A = –40° to +85°C			—	2.0	—	
Input Bias Current (V_{CM} = 0 V, V_O = 0 V)	3, 4	I_{IB}				nA
T_A = +25°C			—	100	500	
T_A = –40° to +85°C			—	—	600	
Input Offset Current (V_{CM} = 0 V, V_O = 0 V)		$\lvert I_{IO}\rvert$				nA
T_A = +25°C			—	5.0	50	
T_A = –40° to +85°C			—	—	60	
Common Mode Input Voltage Range	5	V_{ICR}	–13	–14	—	V
(ΔV_{IO} = 5.0 mV, V_O = 0 V)			—	+14	+13	
Large Signal Voltage Gain (V_O = –10 V to +10 V, R_L = 600 Ω)	6, 7	A_{VOL}				V/V
T_A = +25°C			50 k	200 k	—	
T_A = –40° to +85°C			25 k	—	—	
Output Voltage Swing (V_{ID} = ±1.0 V)	8, 9, 10					V
(V_{CC} = +15 V, V_{EE} = –15 V)						
R_L = 300 Ω		V_O+	—	+12	—	
R_L = 300 Ω		V_O–	—	–12	—	
R_L = 600 Ω		V_O+	+12	+13.6	—	
R_L = 600 Ω		V_O–	—	–13	–12	
R_L = 2.0 kΩ		V_O+	+13	+14	—	
R_L = 2.0 kΩ		V_O–	—	–13.8	–13	
(V_{CC} = +2.5 V, V_{EE} = –2.5 V)						
R_L = 600 Ω		V_O+	1.1	1.6	—	
R_L = 600 Ω		V_O–	—	–1.6	–1.1	
Common Mode Rejection (V_{in} = ±13 V)	11	CMR	80	110	—	dB
Power Supply Rejection	12	PSR	80	110	—	dB
V_{CC}/V_{EE} = +15 V/ –15 V, +5.0 V/ –15 V, +15 V/ –5.0 V						
Output Short Circuit Current (V_{ID} = ±1.0 V, Output to Ground)	13, 14	I_{SC}				mA
Source (V_{CC} = 2.5 V to 15 V)			+50	+80	—	
Sink (V_{EE} = –2.5 V to –15 V)			–50	–100	—	
Power Supply Current (V_O = 0 V)	15	I_D				mA
(V_{CC} = 2.5 V, V_{EE} = –2.5 V to V_{CC} = +15 V, V_{EE} = –15 V)						
MC33178 (Dual)						
T_A = +25°C			—	—	1.4	
T_A = –40° to +85°C			—	—	1.6	
MC33179 (Quad)						
T_A = +25°C			—	1.7	2.4	
T_A = –40° to +85°C			—	—	2.6	

AC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = –15 V, T_A = 25°C, unless otherwise noted.)

Characteristics	Figure	Symbol	Min	Typ	Max	Unit
Slew Rate (V_{in} = –10 V to +10 V, R_L = 2.0 kΩ, C_L = 100 pF, A_V = +1.0 V)	16, 31	SR	1.2	2.0	—	V/µs
Gain Bandwidth Product (f = 100 kHz)	17	GBW	2.5	5.0	—	MHz
AC Voltage Gain (R_L = 600 Ω, V_O = 0 V, f = 20 kHz)	18, 19	A_{VO}	—	50	—	dB
Unity Gain Frequency (Open–Loop) (R_L = 600 Ω, C_L = 0 pF)		f_U	—	3.0	—	MHz
Gain Margin (R_L = 600 Ω, C_L = 0 pF)	20, 22, 23	A_m	—	15	—	dB
Phase Margin (R_L = 600 Ω, C_L = 0 pF)	21, 22, 23	ϕ_m	—	60	—	Degrees
Channel Separation (f = 100 Hz to 20 kHz)	24	CS	—	–120	—	dB
Power Bandwidth (V_O = 20 V_{pp}, R_L = 600 Ω, THD ≤ 1.0%)		BW_p	—	32	—	kHz
Distortion (R_L = 600 Ω,, V_O = 2.0 V_{pp}, A_V = +1.0 V)	25	THD				%
(f = 1.0 kHz)			—	0.0024	—	
(f = 10 kHz)			—	0.014	—	
(f = 20 kHz)			—	0.024	—	
Open Loop Output Impedance (V_O = 0 V, f = 3.0 MHz, A_V = 10 V)	26	$\lvert Z_O \rvert$	—	150	—	Ω
Differential Input Resistance (V_{CM} = 0 V)		R_{in}	—	200	—	kΩ
Differential Input Capacitance (V_{CM} = 0 V)		C_{in}	—	10	—	pF
Equivalent Input Noise Voltage (R_S = 100 Ω,)	27	e_n				$nV/\sqrt{Hz}$
f = 10 Hz			—	8.0	—	
f = 1.0 kHz			—	7.5	—	
Equivalent Input Noise Current	28	i_n				$pA/\sqrt{Hz}$
f = 10 Hz			—	0.33	—	
f = 1.0 kHz			—	0.15	—	

Figure 1. Maximum Power Dissipation versus Temperature

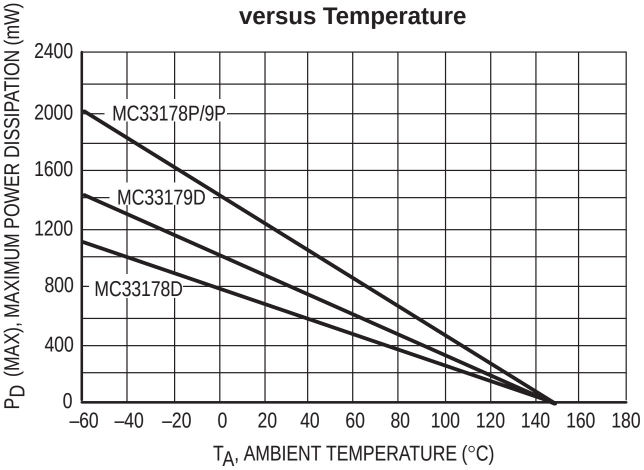


Figure 2. Input Offset Voltage versus Temperature for 3 Typical Units

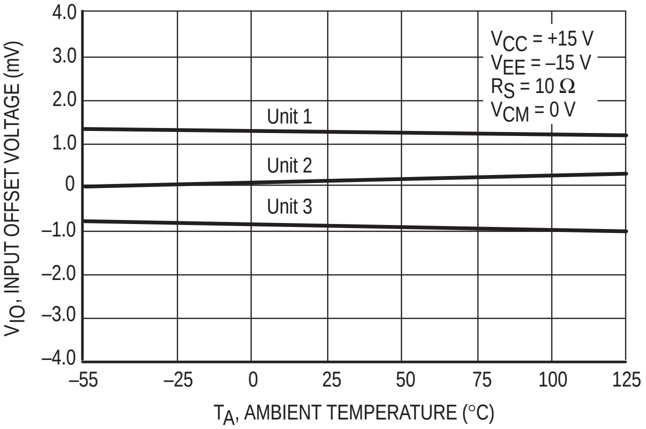


Figure 3. Input Bias Current versus Common Mode Voltage

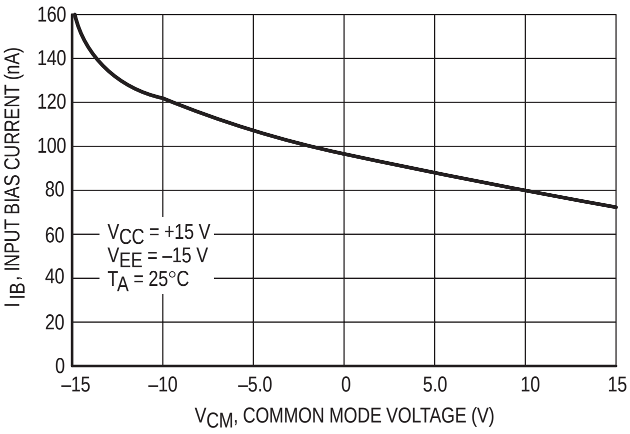


Figure 4. Input Bias Current versus Temperature

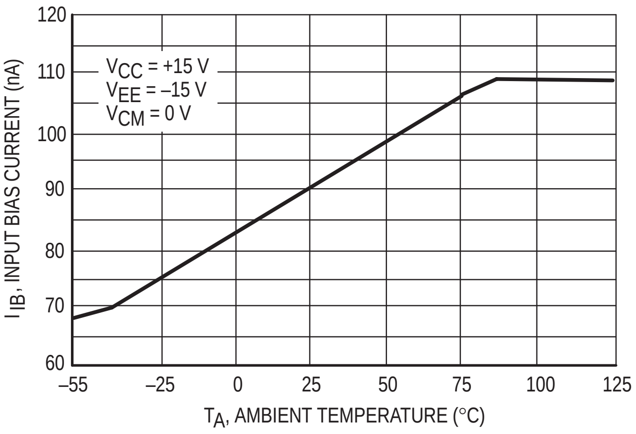


Figure 5. Input Common Mode Voltage Range versus Temperature

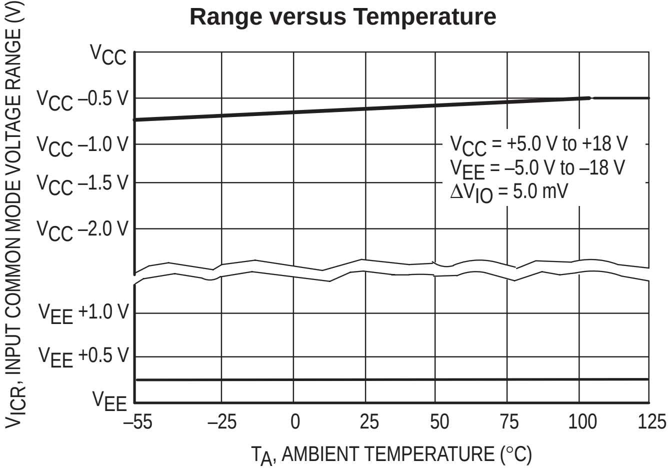


Figure 6. Open Loop Voltage Gain versus Temperature

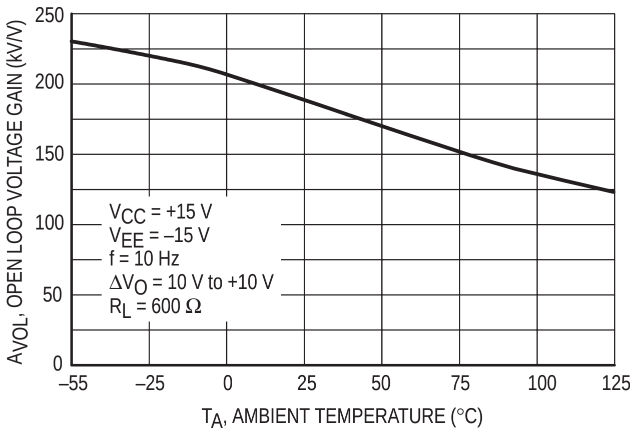


Figure 7. Voltage Gain and Phase versus Frequency

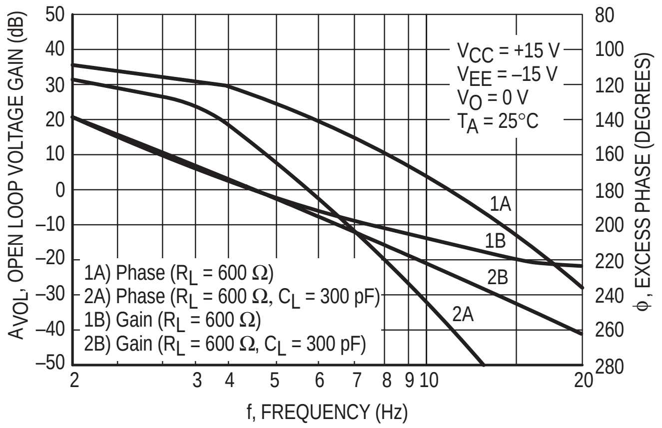


Figure 8. Output Voltage Swing versus Supply Voltage

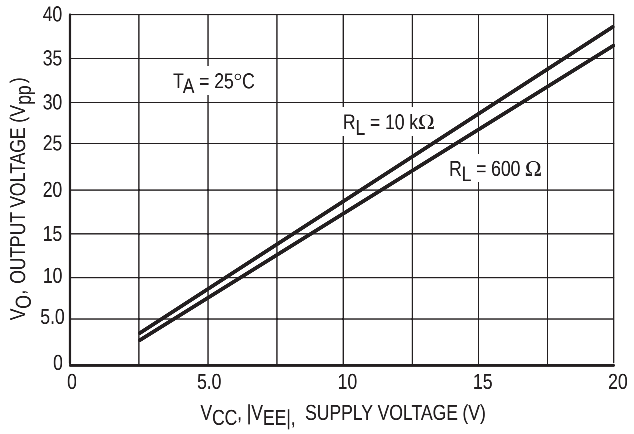


Figure 9. Output Saturation Voltage versus Load Current

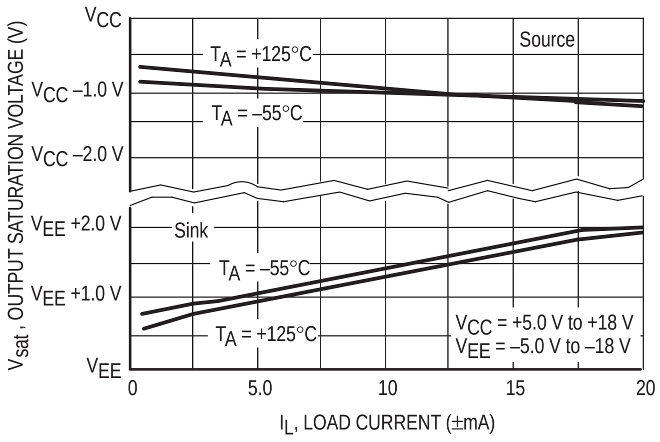


Figure 10. Output Voltage versus Frequency

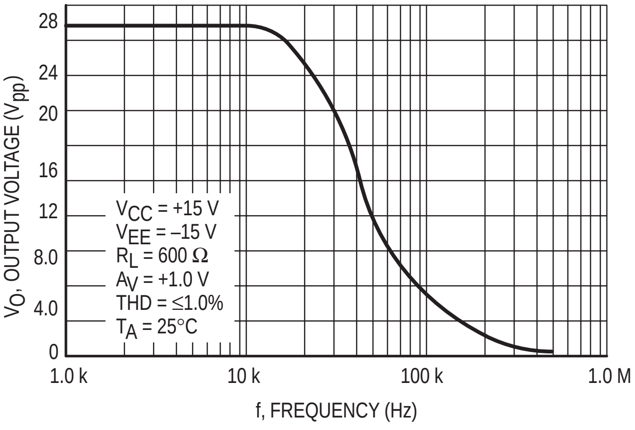


Figure 11. Common Mode Rejection versus Frequency Over Temperature

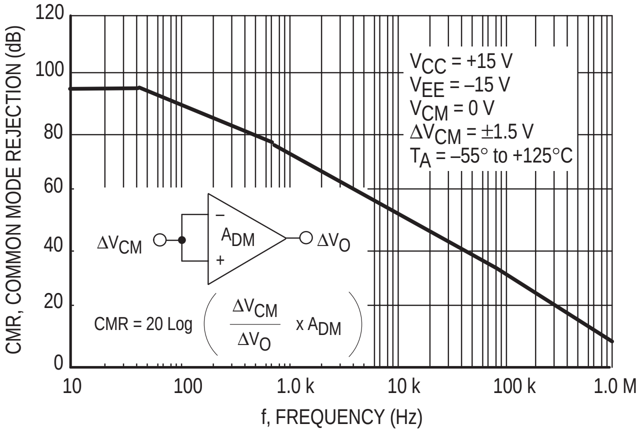


Figure 12. Power Supply Rejection versus Frequency Over Temperature

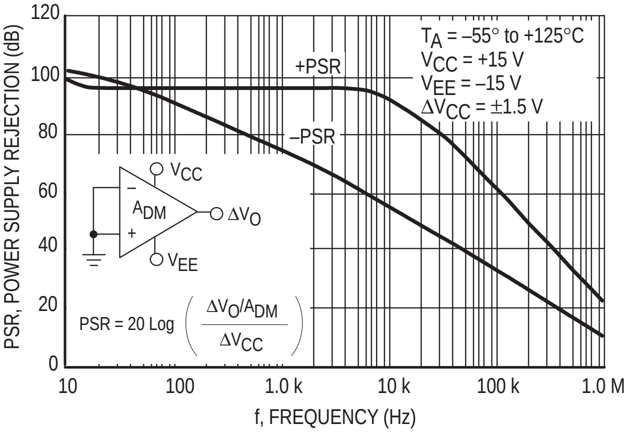


Figure 13. Output Short Circuit Current versus Output Voltage

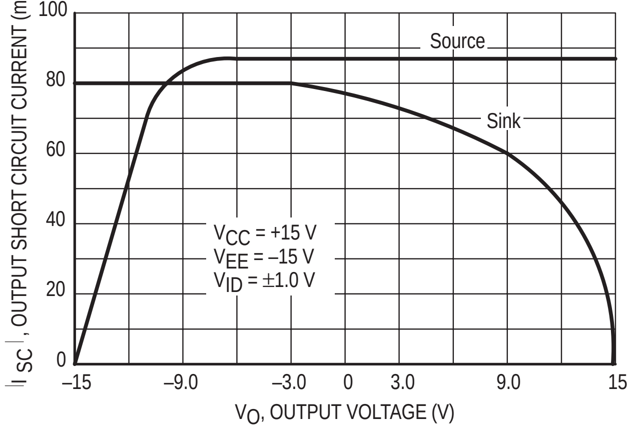


Figure 14. Output Short Circuit Current versus Temperature

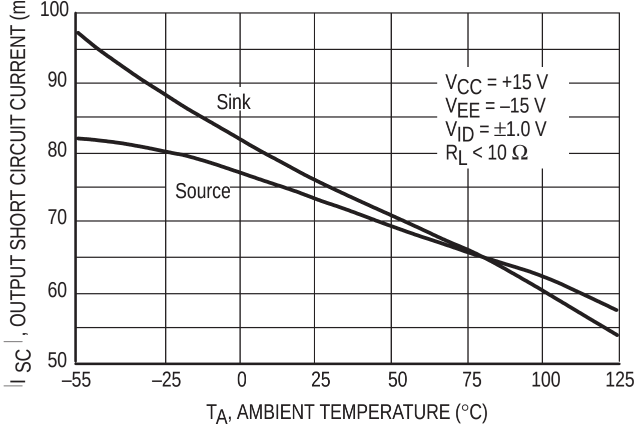


Figure 15. Supply Current versus Supply Voltage with No Load

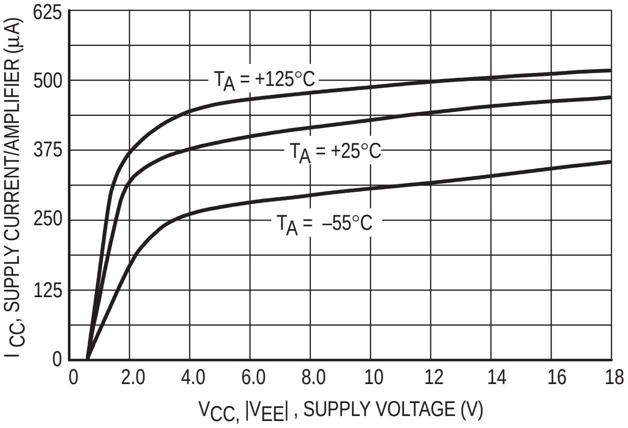


Figure 16. Normalized Slew Rate versus Temperature

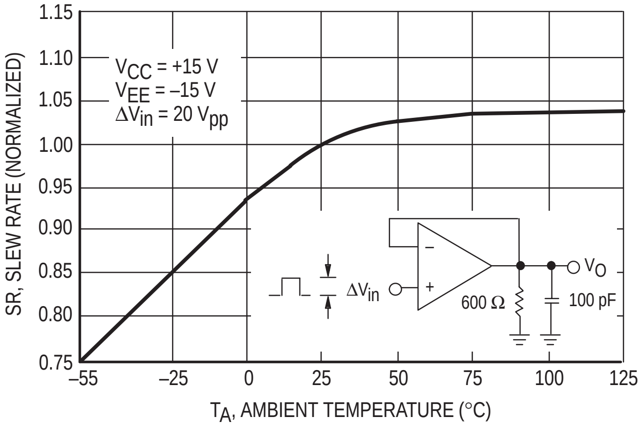


Figure 17. Gain Bandwidth Product versus Temperature

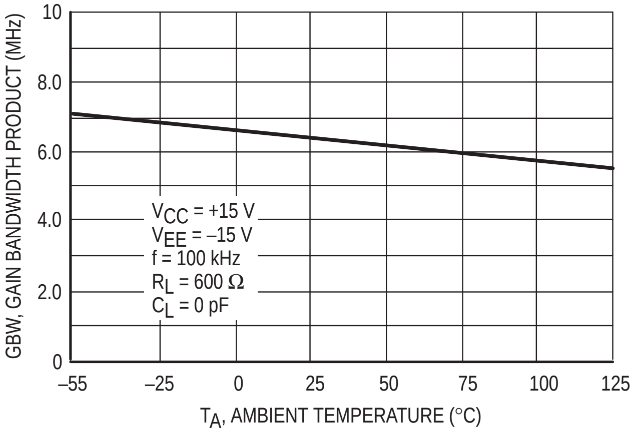


Figure 18. Voltage Gain and Phase versus Frequency

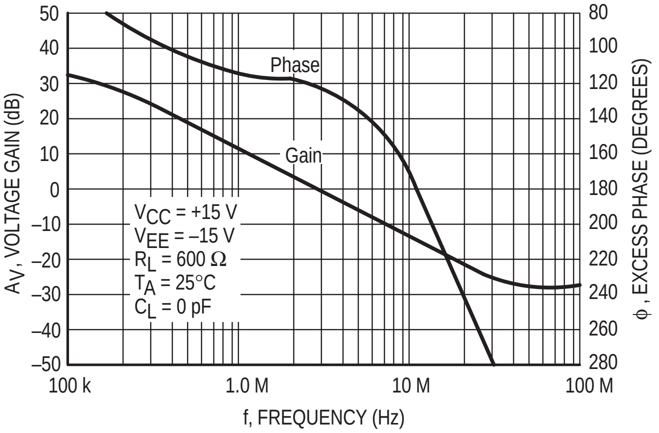


Figure 19. Voltage Gain and Phase versus Frequency

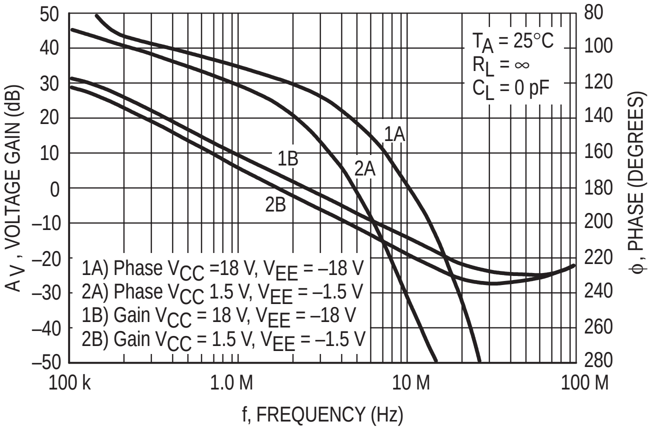


Figure 20. Open Loop Gain Margin versus Temperature

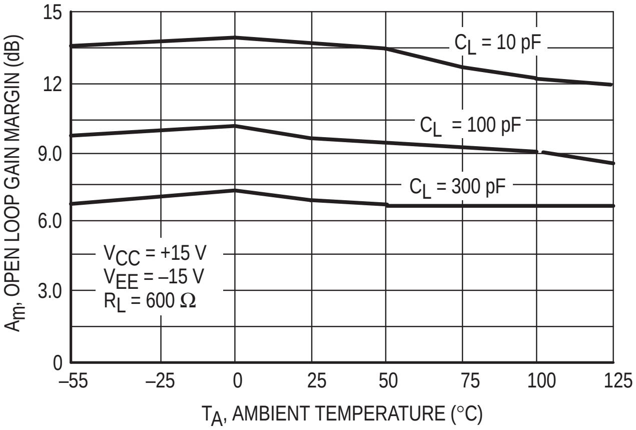


Figure 21. Phase Margin versus Temperature

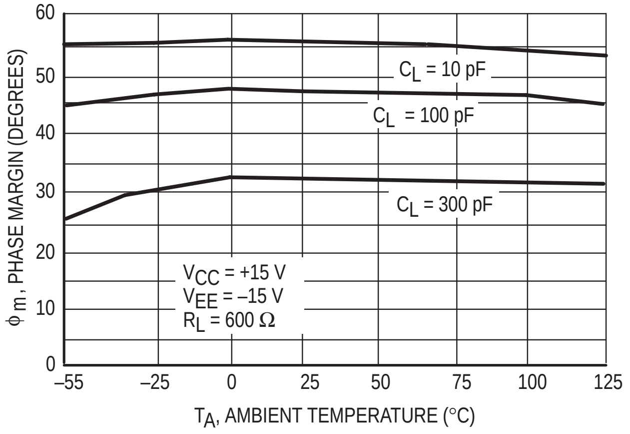


Figure 22. Phase Margin and Gain Margin versus Differential Source Resistance

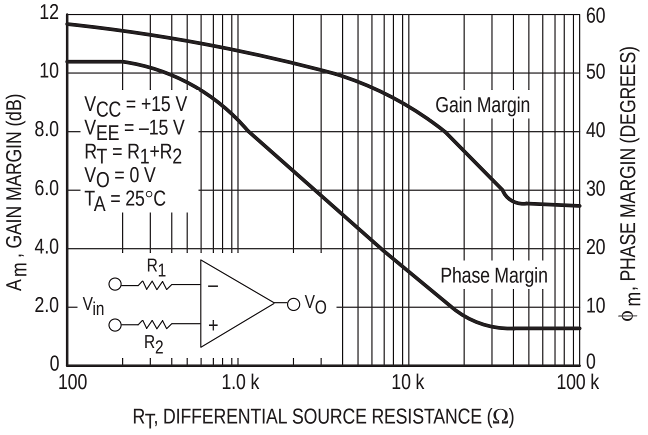


Figure 23. Open Loop Gain Margin and Phase Margin versus Output Load Capacitance

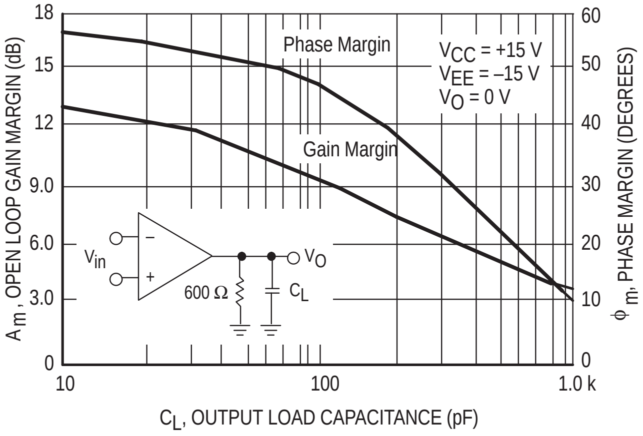


Figure 24. Channel Separation versus Frequency

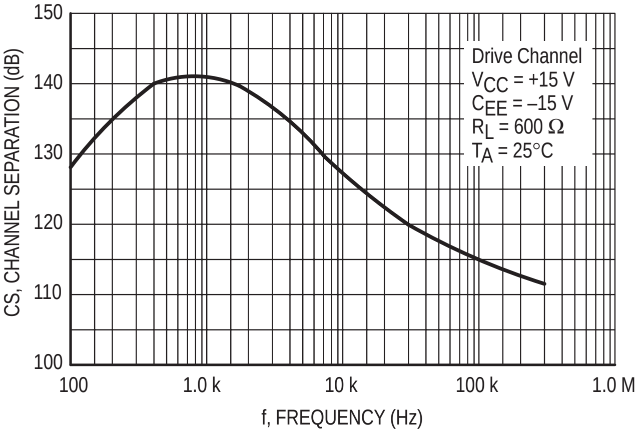


Figure 25. Total Harmonic Distortion versus Frequency

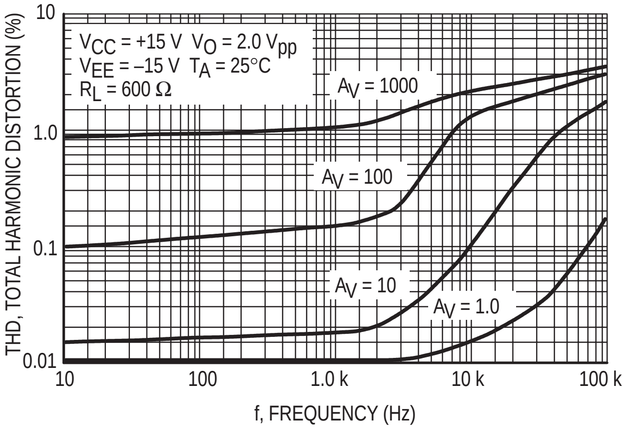


Figure 26. Output Impedance versus Frequency

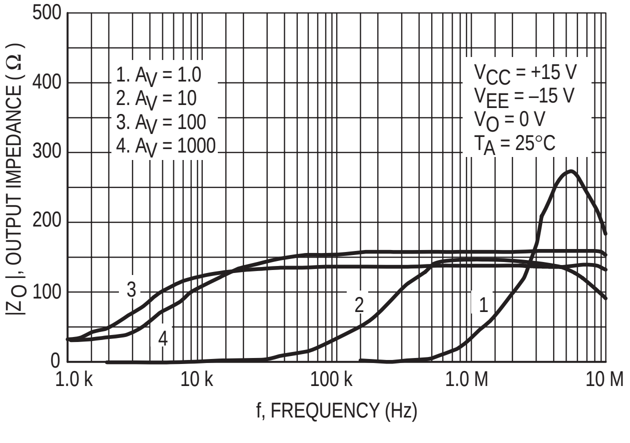


Figure 27. Input Referred Noise Voltage versus Frequency

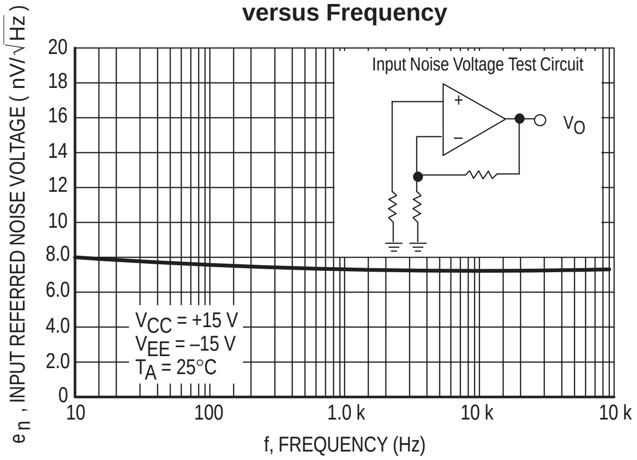


Figure 28. Input Referred Noise Current versus Frequency

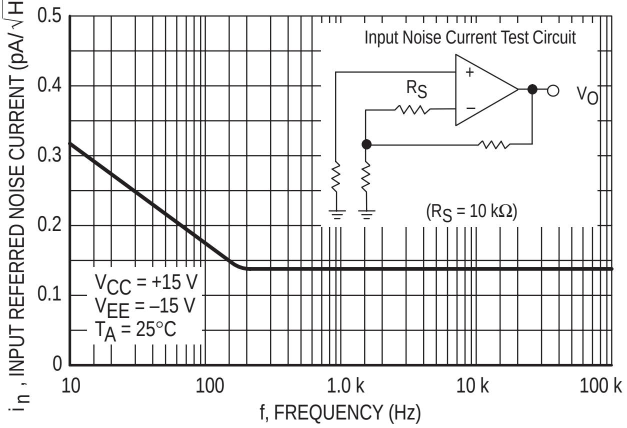


Figure 29. Percent Overshoot versus Load Capacitance

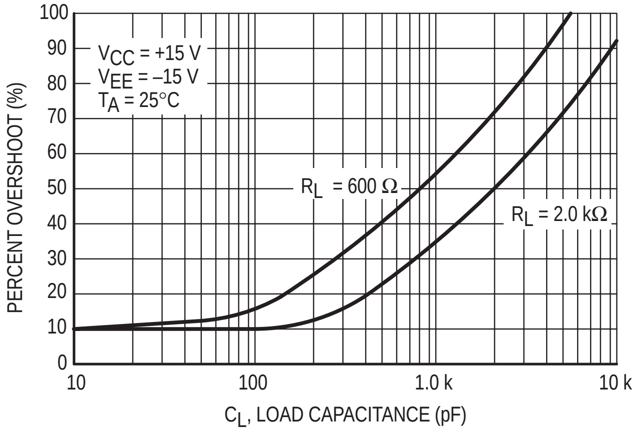


Figure 30. Noninverting Amplifier Slew Rate

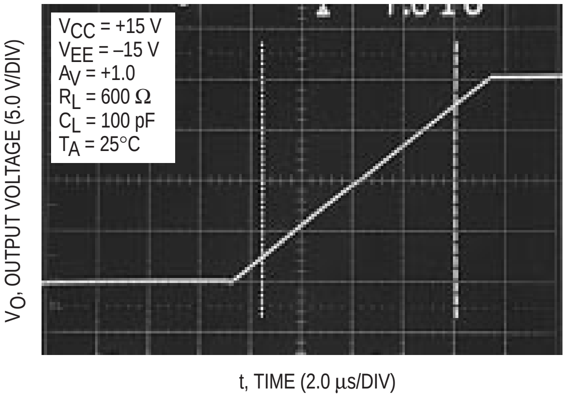


Figure 31. Small Signal Transient Response

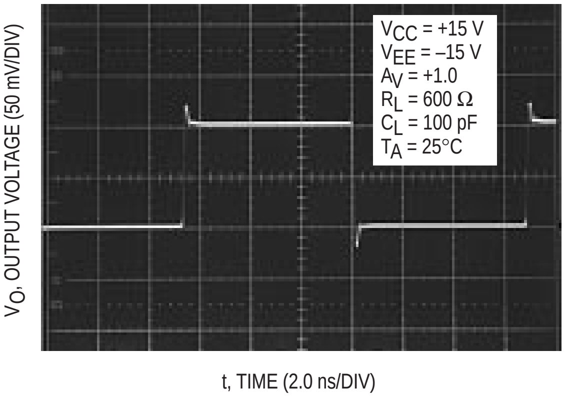


Figure 32. Large Signal Transient Response

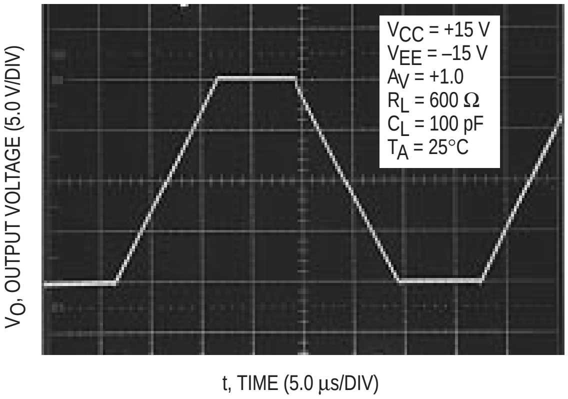
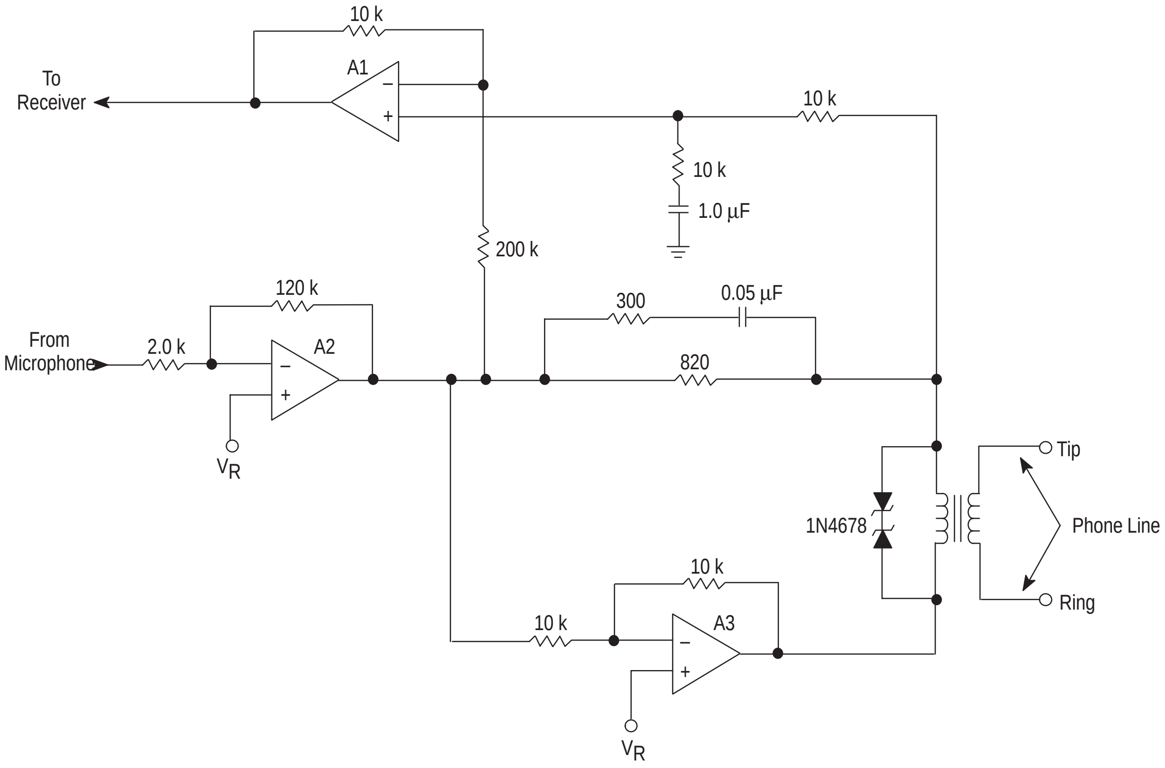


Figure 33. Telephone Line Interface Circuit



APPLICATION INFORMATION

This unique device uses a boosted output stage to combine a high output current with a drain current lower than similar bipolar input op amps. Its 60° phase margin and 15 dB gain margin ensure stability with up to 1000 pF of load capacitance (see Figure 23). The ability to drive a minimum 600 Ω load makes it particularly suitable for telecom applications. Note that in the sample circuit in Figure 33 both A2 and A3 are driving equivalent loads of approximately 600 Ω.

The low input offset voltage and moderately high slew rate and gain bandwidth product make it attractive for a variety of other applications. For example, although it is not single supply (the common mode input range does not include ground), it is specified at +5.0 V with a typical common mode rejection of 110 dB. This makes it an excellent choice for use with digital circuits. The high common mode rejection, which is stable over temperature, coupled with a low noise figure and low distortion, is an ideal op amp for audio circuits.

The output stage of the op amp is current limited and therefore has a certain amount of protection in the event of a short circuit. However, because of its high current output, it is especially important not to allow the device to exceed the maximum junction temperature, particularly with the MC33179 (quad op amp). Shorting more than one amplifier could easily exceed the junction temperature to the extent of causing permanent damage.

Stability

As usual with most high frequency amplifiers, proper lead dress, component placement, and PC board layout should be exercised for optimum frequency performance. For example, long unshielded input or output leads may result in unwanted input/output coupling. In order to preserve the relatively low input capacitance associated with these amplifiers, resistors connected to the inputs should be immediately adjacent to the input pin to minimize additional stray input capacitance. This not only minimizes the input pole frequency for optimum frequency response, but also minimizes extraneous “pick up” at this node. Supplying decoupling with adequate capacitance immediately adjacent to the supply pin is also important, particularly over temperature, since many types of decoupling capacitors exhibit great impedance changes over temperature.

Additional stability problems can be caused by high load capacitances and/or a high source resistance. Simple compensation schemes can be used to alleviate these effects.

If a high source of resistance is used (R1 > 1.0 kΩ), a compensation capacitor equal to or greater than the input capacitance of the op amp (10 pF) placed across the feedback resistor (see Figure 34) can be used to neutralize that pole and prevent outer loop oscillation. Since the closed loop transient response will be a function of that capacitance, it is important to choose the optimum value for that capacitor. This can be determined by the following Equation:

$$C_C = (1 + [R1/R2])^2 \times C_L (Z_O/R_2) \qquad (1)$$

where: Z_O is the output impedance of the op amp.

For moderately high capacitive loads (500 pF < C_L < 1500 pF) the addition of a compensation resistor on the order of 20 Ω between the output and the feedback loop will help to decrease miller loop oscillation (see Figure 35). For high capacitive loads (C_L > 1500 pF), a combined compensation scheme should be used (see Figure 36). Both the compensation resistor and the compensation capacitor affect the transient response and can be calculated for optimum performance. The value of C_C can be calculated using Equation (1). The Equation to calculate R_C is as follows:

$$R_C = Z_O \times R1/R2 \qquad (2)$$

Figure 34. Compensation for High Source Impedance

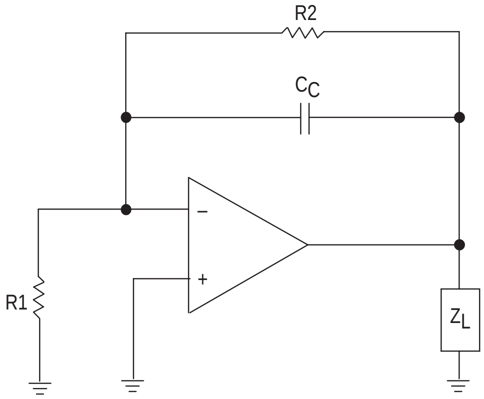


Figure 35. Compensation Circuit for Moderate Capacitive Loads

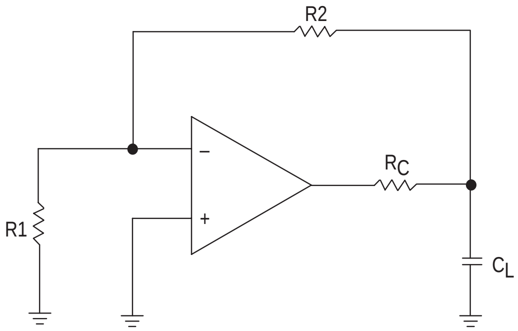
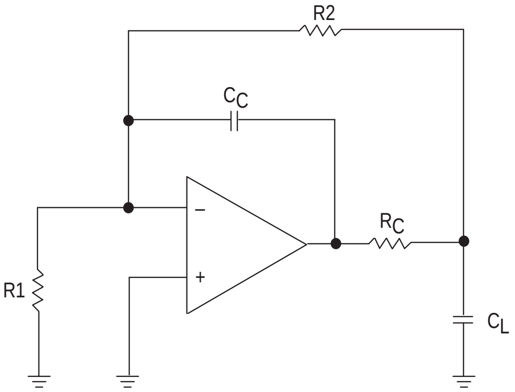


Figure 36. Compensation Circuit for High Capacitive Loads



MOTOROLA

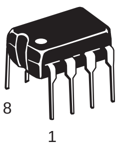
MC33201
MC33202
MC33204

Rail-to-Rail Operational Amplifiers

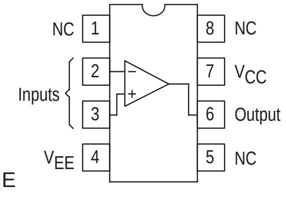
The MC33201/2/4 family of operational amplifiers provide rail–to–rail operation on both the input and output. The inputs can be driven as high as 200 mV beyond the supply rails without phase reversal on the outputs, and the output can swing within 50 mV of each rail. This rail–to–rail operation enables the user to make full use of the supply voltage range available. It is designed to work at very low supply voltages (± 0.9 V) yet can operate with a supply of up to +12 V and ground. Output current boosting techniques provide a high output current capability while keeping the drain current of the amplifier to a minimum. Also, the combination of low noise and distortion with a high slew rate and drive capability make this an ideal amplifier for audio applications.

- Low Voltage, Single Supply Operation (+1.8 V and Ground to +12 V and Ground)
- Input Voltage Range Includes both Supply Rails
- Output Voltage Swings within 50 mV of both Rails
- No Phase Reversal on the Output for Over–driven Input Signals
- High Output Current (I_{SC} = 80 mA, Typ)
- Low Supply Current (I_D = 0.9 mA, Typ)
- 600 Ω Output Drive Capability
- Extended Operating Temperature Ranges (–40° to +105°C and –55° to +125°C)
- Typical Gain Bandwidth Product = 2.2 MHz
- Offered in New TSSOP Package Including Standard SOIC and DIP Packages

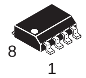
LOW VOLTAGE RAIL–TO–RAIL OPERATIONAL AMPLIFIERS



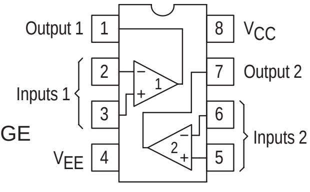
P SUFFIX
PLASTIC PACKAGE
CASE 626



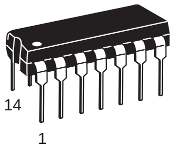
(Single, Top View)



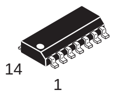
D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)



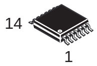
(Dual, Top View)



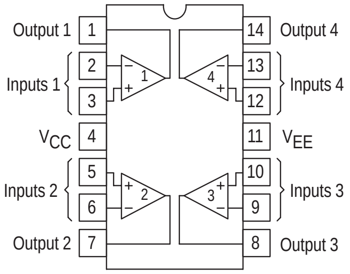
P SUFFIX
PLASTIC PACKAGE
CASE 646



D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO–14)



DTB SUFFIX
PLASTIC PACKAGE
CASE 948G
(TSSOP–14)



(Quad, Top View)

ORDERING INFORMATION

Operational Amplifier Function	Device	Operating Temperature Range	Package
Single	MC33201D	T_A= –40 ° to +105°C	SO–8
	MC33201P		Plastic DIP
	MC33201VD	T_A = –55 ° to +125°C	SO–8
	MC33201VP		Plastic DIP
Dual	MC33202D	T_A= –40 ° to +105°C	SO–8
	MC33202P		Plastic DIP
	MC33202VD	T_A = –55 ° to +125°C	SO–8
	MC33202VP		Plastic DIP
Quad	MC33204D	T_A= –40 ° to +105°C	SO–14
	MC33204DTB		TSSOP–14
	MC33204P		Plastic DIP
	MC33204VD	T_A = –55 ° to +125°C	SO–14
	MC33204VDTB		TSSOP–14
	MC33204VP		Plastic DIP

DC ELECTRICAL CHARACTERISTICS (T_A = 25°C)

Characteristic	V_{CC} = 2.0 V	V_{CC} = 3.3 V	V_{CC} = 5.0 V	Unit
Input Offset Voltage				mV
V_{IO} (max)				
MC33201	± 8.0	± 8.0	± 6.0	
MC33202	±10	±10	± 8.0	
MC33204	±12	±12	±10	
Output Voltage Swing				
V_{OH} (R_L = 10 kΩ)	1.9	3.15	4.85	V_{min}
V_{OL} (R_L = 10 kΩ)	0.10	0.15	0.15	V_{max}
Power Supply Current per Amplifier (I_D)	1.125	1.125	1.125	mA

Specifications at V_{CC} = 3.3 V are guaranteed by the 2.0 V and 5.0 V tests. V_{EE} = Gnd.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage (V_{CC} to V_{EE})	V_S	+13	V
Input Differential Voltage Range	V_{IDR}	(Note 1)	V
Common Mode Input Voltage Range (Note 2)	V_{CM}	V_{CC} + 0.5 V to V_{EE} – 0.5 V	V
Output Short Circuit Duration	t_s	(Note 3)	sec
Maximum Junction Temperature	T_J	+150	°C
Storage Temperature	T_{stg}	– 65 to +150	°C
Maximum Power Dissipation	P_D	(Note 3)	mW

NOTES: 1. The differential input voltage of each amplifier is limited by two internal parallel back–to–back diodes. For additional differential input voltage range, use current limiting resistors in series with the input pins.

2. The input common mode voltage range is limited by internal diodes connected from the inputs to both supply rails. Therefore, the voltage on either input must not exceed either supply rail by more than 500 mV.

3. Power dissipation must be considered to ensure maximum junction temperature (T_J) is not exceeded. (See Figure 2)

DC ELECTRICAL CHARACTERISTICS (V_{CC} = + 5.0 V, V_{EE} = Ground, T_A = 25°C, unless otherwise noted.)

Characteristic	Figure	Symbol	Min	Typ	Max	Unit
Input Offset Voltage (V_{CM} 0 V to 0.5 V, V_{CM} 1.0 V to 5.0 V)	3	$\vert V_{IO}\vert$				mV
MC33201: T_A = + 25°C			–	–	6.0	
T_A = – 40° to +105°C			–	–	9.0	
T_A = – 55° to +125°C			–	–	13	
MC33202: T_A = + 25°C			–	–	8.0	
T_A = – 40° to +105°C			–	–	11	
T_A = – 55° to +125°C			–	–	14	
MC33204: T_A = + 25°C			–	–	10	
T_A = – 40° to +105°C			–	–	13	
T_A = – 55° to +125°C			–	–	17	
Input Offset Voltage Temperature Coefficient (R_S = 50 Ω)	4	$\Delta V_{IO}/\Delta T$				µV/°C
T_A = – 40° to +105°C			–	2.0	–	
T_A = – 55° to +125°C			–	2.0	–	
Input Bias Current (V_{CM} = 0 V to 0.5 V, V_{CM} = 1.0 V to 5.0 V)	5, 6	$\vert I_{IB}\vert$				nA
T_A = + 25°C			–	80	200	
T_A = – 40° to +105°C			–	100	250	
T_A = – 55° to +125°C			–	–	500	
Input Offset Current (V_{CM} = 0 V to 0.5 V, V_{CM} = 1.0 V to 5.0 V)	–	$\vert I_{IO}\vert$				nA
T_A = + 25°C			–	5.0	50	
T_A = – 40° to +105°C			–	10	100	
T_A = – 55° to +125°C			–	–	200	
Common Mode Input Voltage Range	–	V_{ICR}	V_{EE}	–	V_{CC}	V

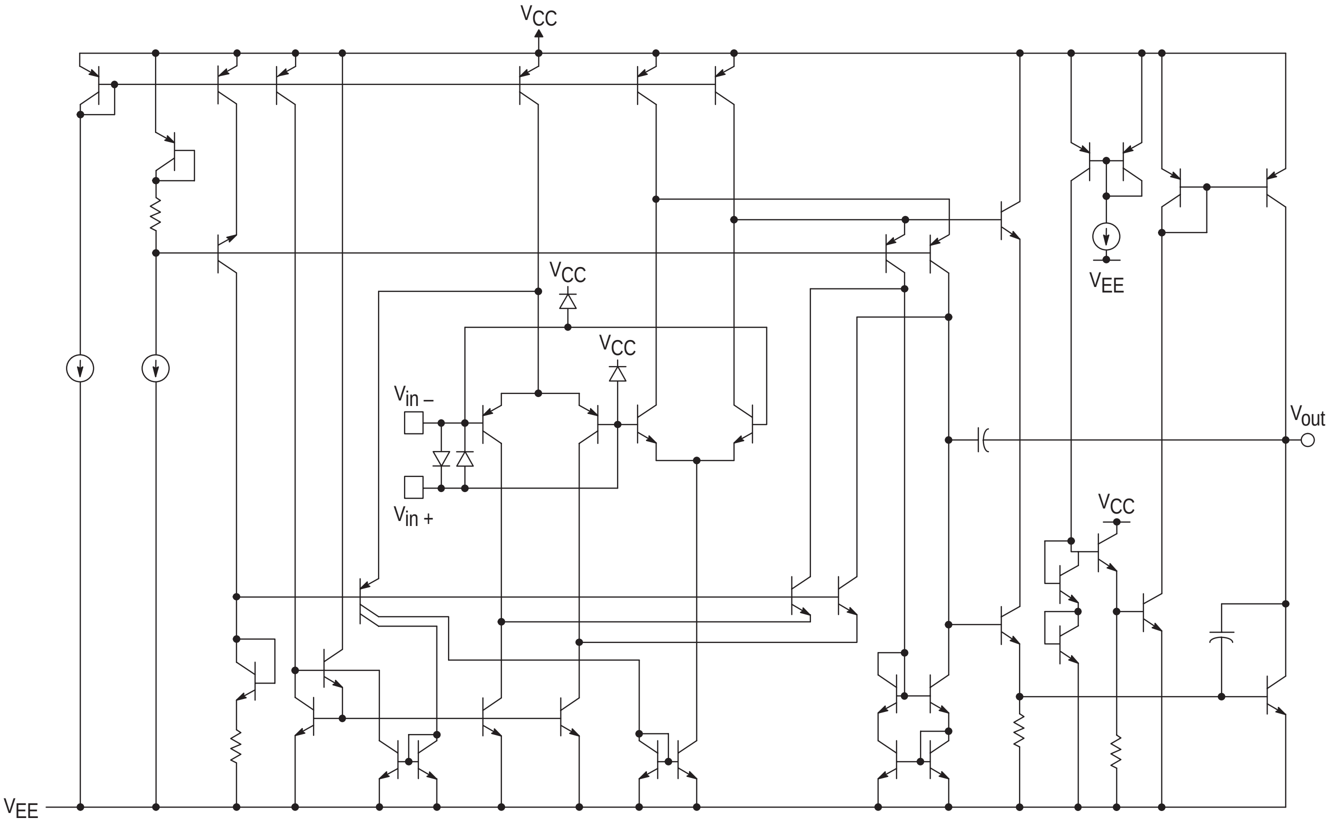
DC ELECTRICAL CHARACTERISTICS (continued) (V_{CC} = + 5.0 V, V_{EE} = Ground, T_A = 25°C, unless otherwise noted.)

Characteristic	Figure	Symbol	Min	Typ	Max	Unit
Large Signal Voltage Gain (V_{CC} = + 5.0 V, V_{EE} = – 5.0 V)	7	A_{VOL}				kV/V
R_L = 10 kΩ			50	300	–	
R_L = 600 Ω			25	250	–	
Output Voltage Swing (V_{ID} = ± 0.2 V)	8, 9, 10					V
R_L = 10 kΩ		V_{OH}	4.85	4.95	–	
R_L = 10 kΩ		V_{OL}	–	0.05	0.15	
R_L = 600 Ω		V_{OH}	4.75	4.85	–	
R_L = 600 Ω		V_{OL}	–	0.15	0.25	
Common Mode Rejection (V_{in} = 0 V to 5.0 V)	11	CMR	60	90	–	dB
Power Supply Rejection Ratio	12	PSRR				µV/V
V_{CC}/V_{EE} = 5.0 V/Gnd to 3.0 V/Gnd			500	25	–	
Output Short Circuit Current (Source and Sink)	13, 14	I_{SC}	50	80	–	mA
Power Supply Current per Amplifier (V_O = 0 V)	15	I_D				mA
T_A = – 40° to +105°C			–	0.9	1.125	
T_A = – 55° to +125°C			–	0.9	1.125	

AC ELECTRICAL CHARACTERISTICS (V_{CC} = + 5.0 V, V_{EE} = Ground, T_A = 25°C, unless otherwise noted.)

Characteristic	Figure	Symbol	Min	Typ	Max	Unit
Slew Rate	16, 26	SR				V/µs
(V_S = ± 2.5 V, V_O = – 2.0 V to + 2.0 V, R_L = 2.0 kΩ, A_V = +1.0)			0.5	1.0	–	
Gain Bandwidth Product (f = 100 kHz)	17	GBW	–	2.2	–	MHz
Gain Margin (R_L = 600 Ω, C_L = 0 pF)	20, 21, 22	A_M	–	12	–	dB
Phase Margin (R_L = 600 Ω, C_L = 0 pF)	20, 21, 22	$\varnothing_M$	–	65	–	Deg
Channel Separation (f = 1.0 Hz to 20 kHz, A_V = 100)	23	CS	–	90	–	dB
Power Bandwidth (V_O = 4.0 V_{pp}, R_L = 600 Ω, THD ≤ 1 %)		BW_P	–	28	–	kHz
Total Harmonic Distortion (R_L = 600 Ω, V_O = 1.0 V_{pp}, A_V = 1.0)	24	THD				%
f = 1.0 kHz			–	0.002	–	
f = 10 kHz			–	0.008	–	
Open Loop Output Impedance		$\lvert Z_O \rvert$				Ω
(V_O = 0 V, f = 2.0 MHz, A_V = 10)			–	100	–	
Differential Input Resistance (V_{CM} = 0 V)		R_{in}	–	200	–	kΩ
Differential Input Capacitance (V_{CM} = 0 V)		C_{in}	–	8.0	–	pF
Equivalent Input Noise Voltage (R_S = 100 Ω)	25	e_n				nV/$\sqrt{Hz}$
f = 10 Hz			–	25	–	
f = 1.0 kHz			–	20	–	
Equivalent Input Noise Current	25	i_n				pA/$\sqrt{Hz}$
f = 10 Hz			–	0.8	–	
f = 1.0 kHz			–	0.2	–	

Figure 1. Circuit Schematic
(Each Amplifier)



This device contains 70 active transistors (each amplifier).

Figure 2. Maximum Power Dissipation versus Temperature

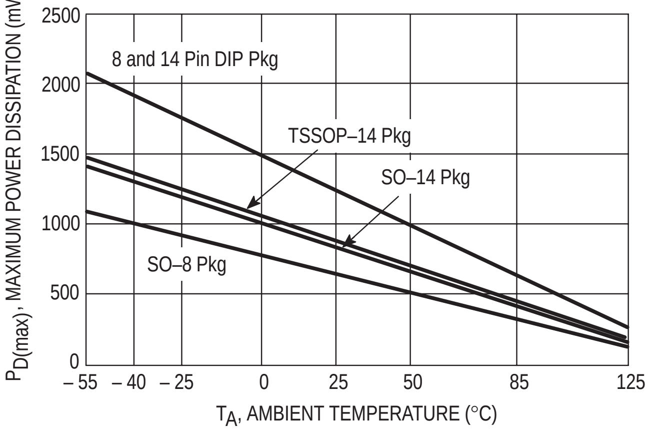


Figure 3. Input Offset Voltage Distribution

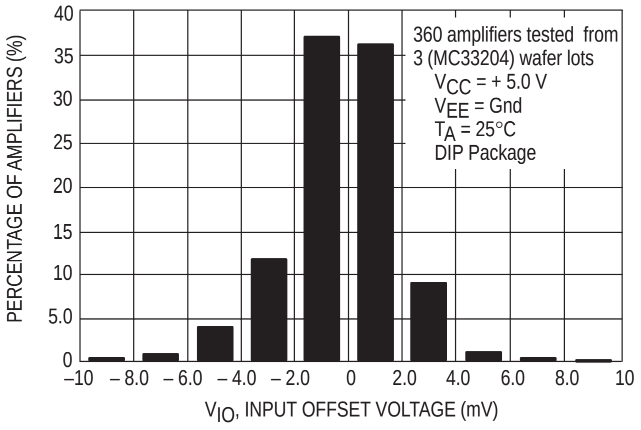


Figure 4. Input Offset Voltage Temperature Coefficient Distribution

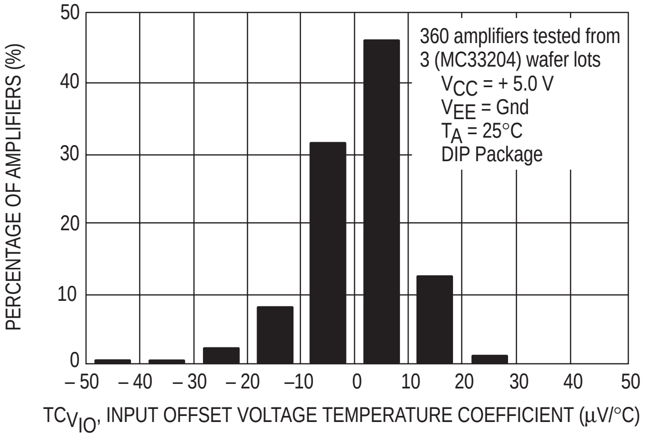


Figure 5. Input Bias Current versus Temperature

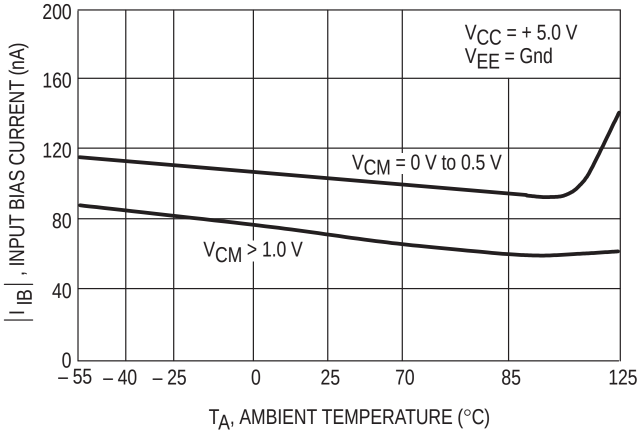


Figure 6. Input Bias Current versus Common Mode Voltage

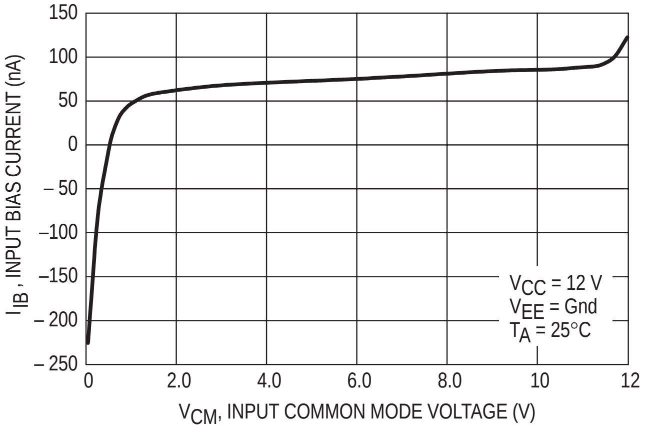


Figure 7. Open Loop Voltage Gain versus Temperature

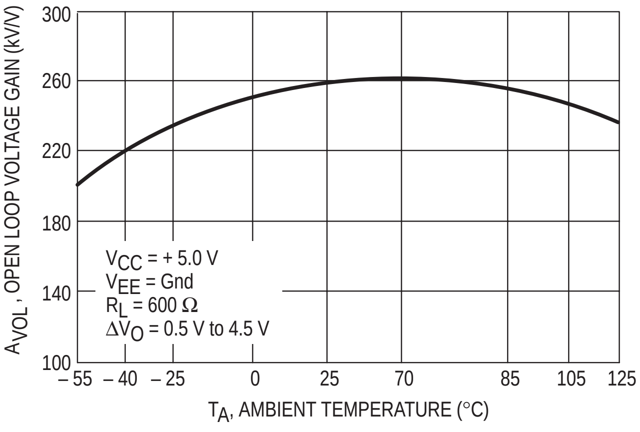


Figure 8. Output Voltage Swing versus Supply Voltage

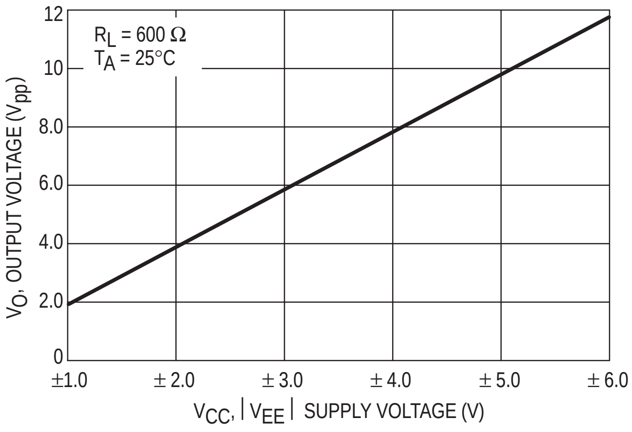


Figure 9. Output Saturation Voltage versus Load Current

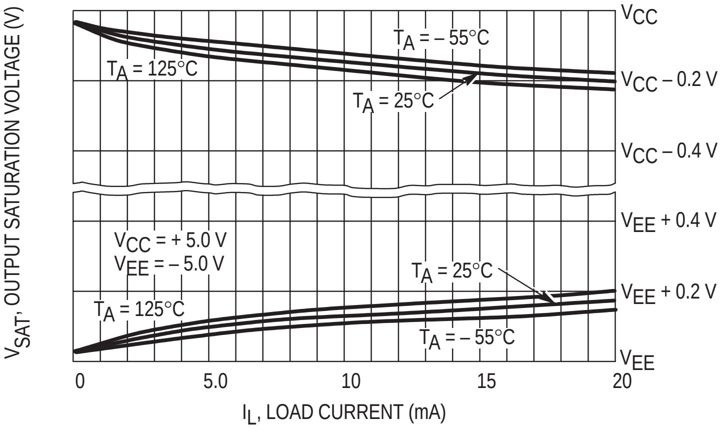


Figure 10. Output Voltage versus Frequency

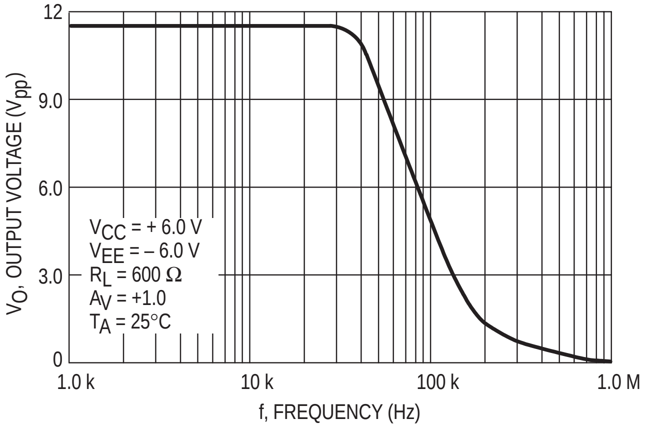


Figure 11. Common Mode Rejection versus Frequency

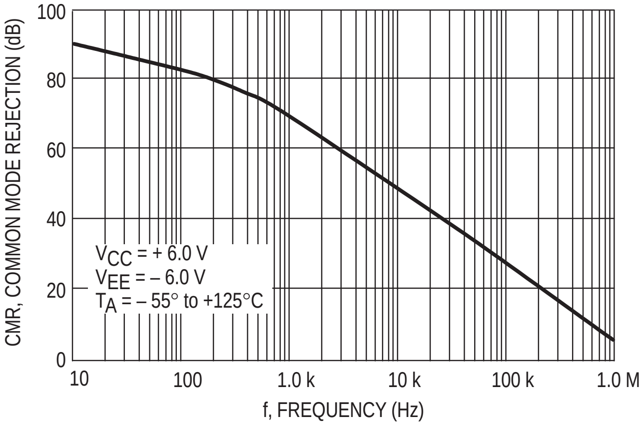


Figure 12. Power Supply Rejection versus Frequency

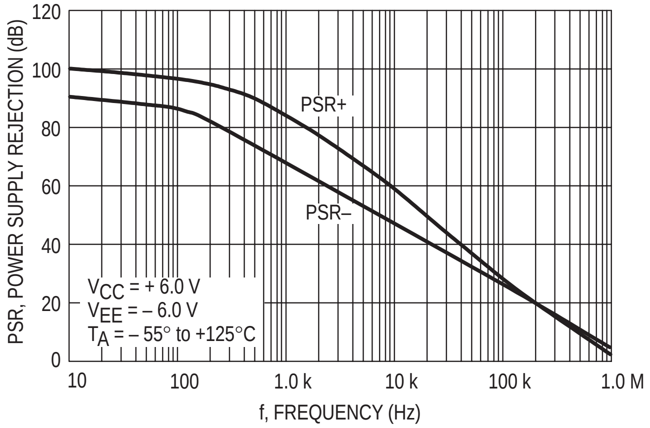


Figure 13. Output Short Circuit Current versus Output Voltage

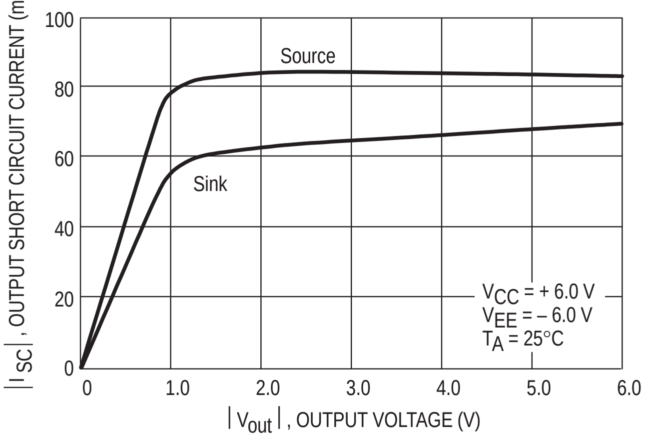


Figure 14. Output Short Circuit Current versus Temperature

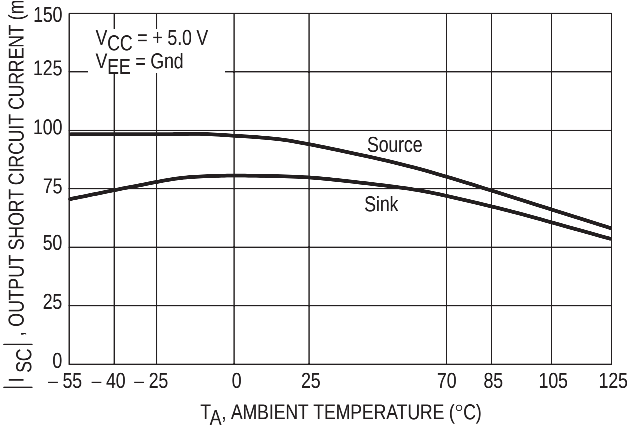


Figure 15. Supply Current per Amplifier versus Supply Voltage with No Load

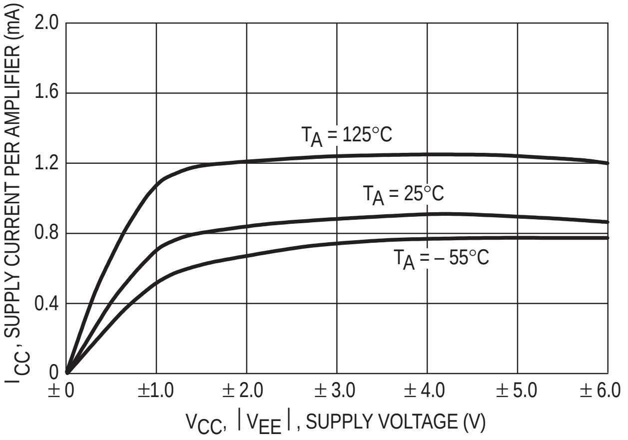


Figure 16. Slew Rate versus Temperature

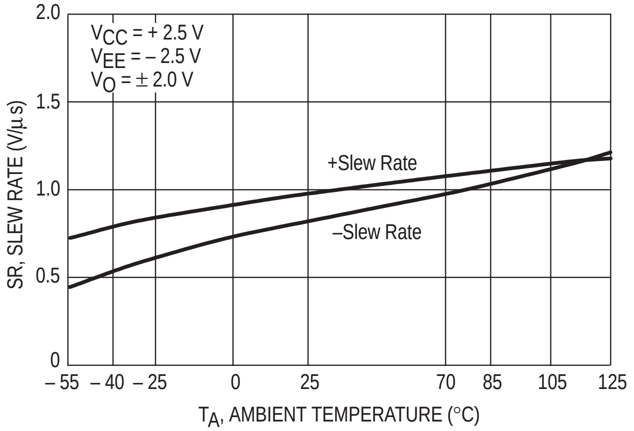


Figure 17. Gain Bandwidth Product versus Temperature

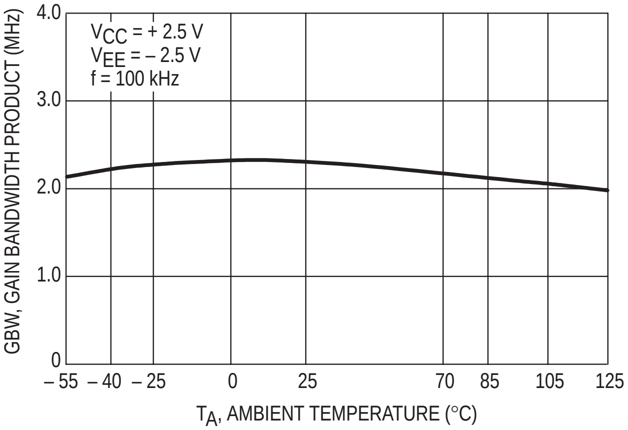


Figure 18. Voltage Gain and Phase versus Frequency

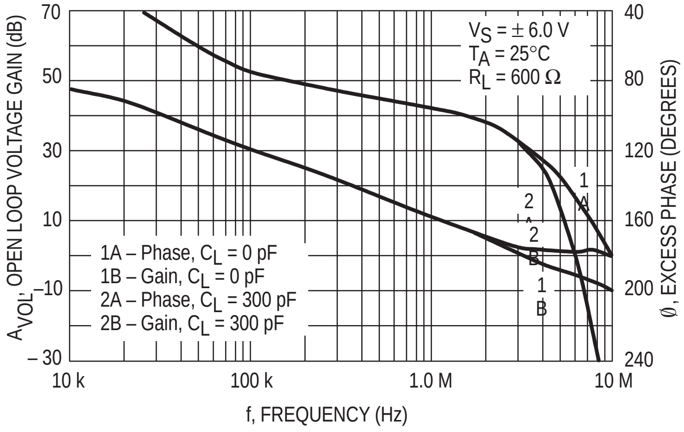


Figure 19. Voltage Gain and Phase versus Frequency

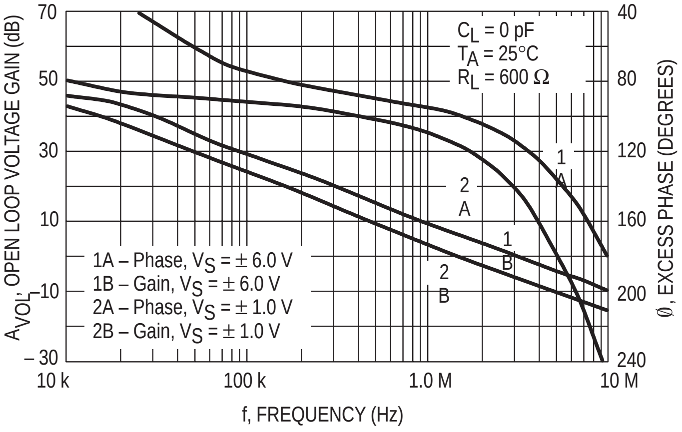


Figure 20. Gain and Phase Margin versus Temperature

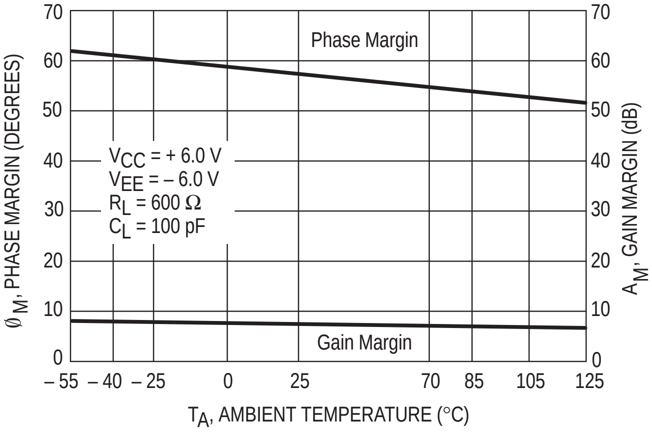


Figure 21. Gain and Phase Margin versus Differential Source Resistance

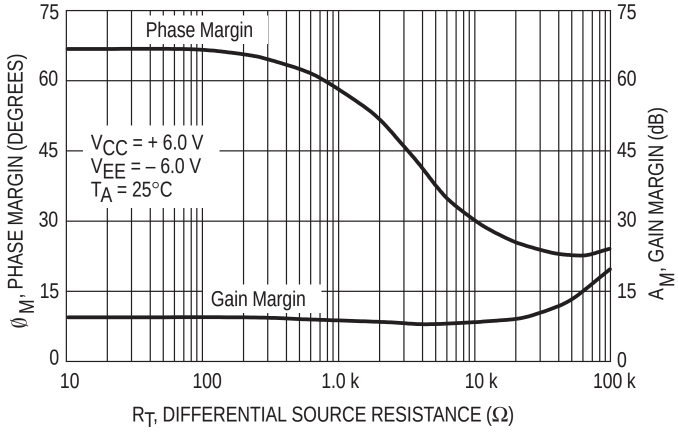


Figure 22. Gain and Phase Margin versus Capacitive Load

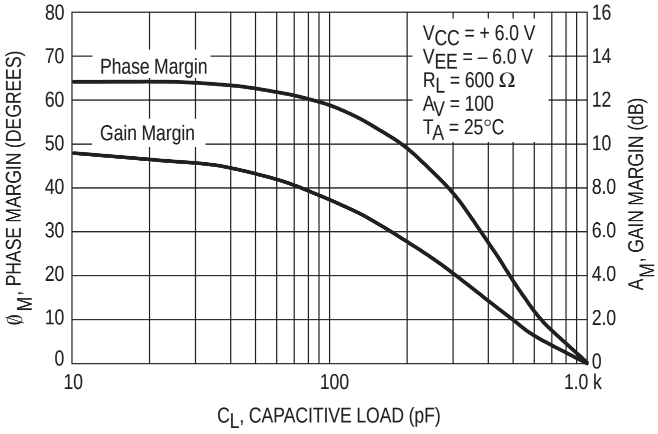


Figure 23. Channel Separation versus Frequency

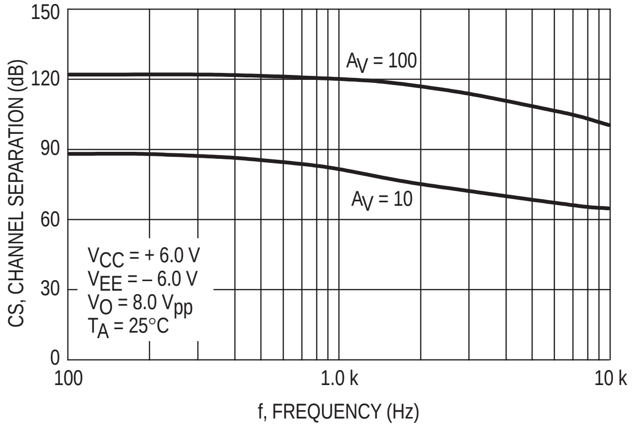


Figure 24. Total Harmonic Distortion versus Frequency

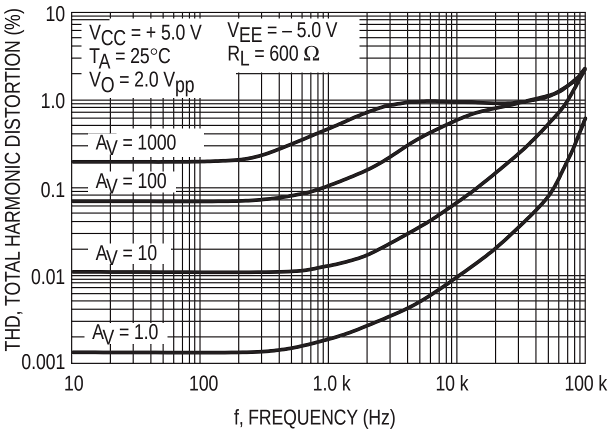
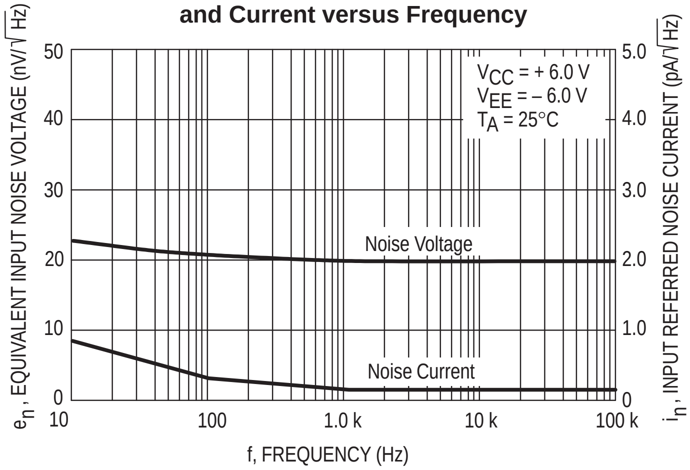


Figure 25. Equivalent Input Noise Voltage and Current versus Frequency



General Information

The MC33201/2/4 family of operational amplifiers are unique in their ability to swing rail–to–rail on both the input and the output with a completely bipolar design. This offers low noise, high output current capability and a wide common mode input voltage range even with low supply voltages. Operation is guaranteed over an extended temperature range and at supply voltages of 2.0 V, 3.3 V and 5.0 V and ground.

Since the common mode input voltage range extends from V_{CC} to V_{EE}, it can be operated with either single or split voltage supplies. The MC33201/2/4 are guaranteed not to latch or phase reverse over the entire common mode range, however, the inputs should not be allowed to exceed maximum ratings.

Circuit Information

Rail–to–rail performance is achieved at the input of the amplifiers by using parallel NPN–PNP differential input stages. When the inputs are within 800 mV of the negative rail, the PNP stage is on. When the inputs are more than 800 mV greater than V_{EE}, the NPN stage is on. This switching of input pairs will cause a reversal of input bias currents (see Figure 6). Also, slight differences in offset voltage may be noted between the NPN and PNP pairs. Cross–coupling techniques have been used to keep this change to a minimum.

In addition to its rail–to–rail performance, the output stage is current boosted to provide 80 mA of output current, enabling the op amp to drive 600 Ω loads. Because of this high output current capability, care should be taken not to exceed the 150°C maximum junction temperature.

Figure 26. Noninverting Amplifier Slew Rate

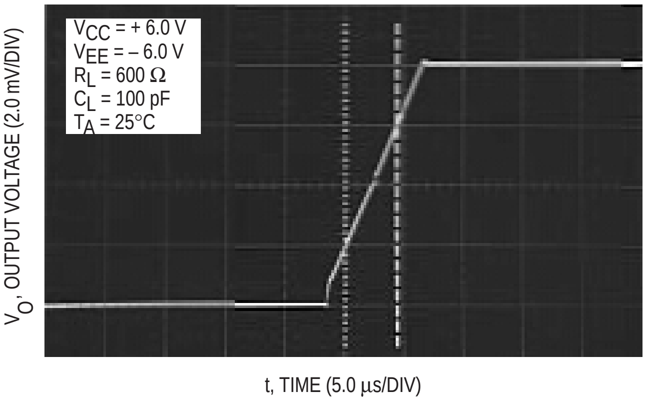


Figure 27. Small Signal Transient Response

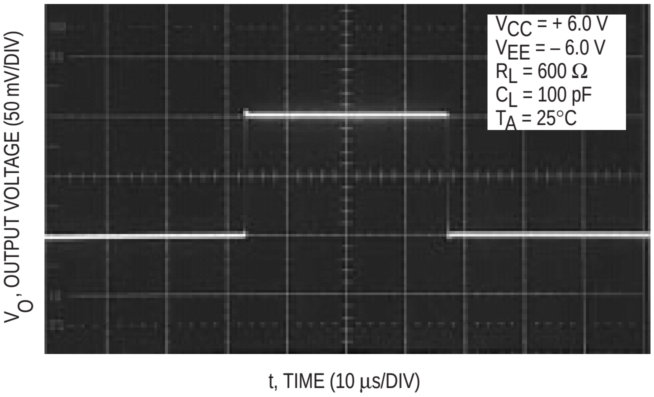
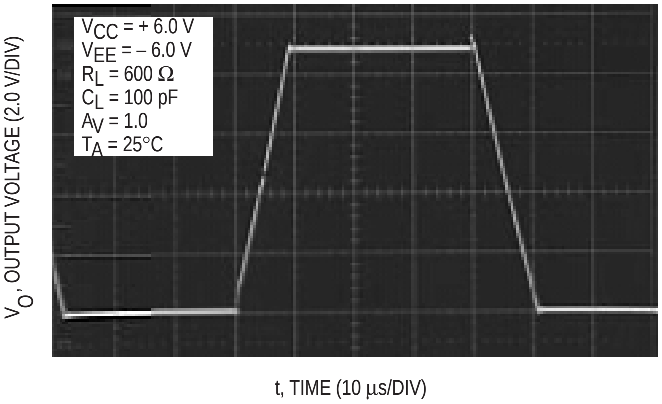


Figure 28. Large Signal Transient Response



MOTOROLA

MC33206
MC33207

Advance Information

Rail-To-Rail Operational Amplifiers with Enable Feature

The MC33206/7 family of operational amplifiers provide rail–to–rail operation on both the input and output. The inputs can be driven as high as 200 mV beyond the supply rails without phase reversal on the outputs and the output can swing within 50 mV of each rail. This rail–to–rail operation enables the user to make full use of the supply voltage range available. It is designed to work at very low supply voltages (±0.9 V) yet can operate with a single supply of up to 12 V and ground. Output current boosting techniques provide a high output current capability while keeping the drain current of the amplifier to a minimum.

The MC33206/7 has an enable mode that can be controlled externally. The typical supply current in the standby mode is <1.0 µA (V_{Enable} = Gnd). The addition of an enable function makes this amplifier an ideal choice for power sensitive applications, battery powered equipment (instrumentation and monitoring), portable telecommunication, and sample–and–hold applications.

- Standby Mode (I_D ≤1.0 µA, Typ)
- Low Voltage, Single Supply Operation
  (1.8 V and Ground to 12 V and Ground)
- Rail–to–Rail Input Common Mode Voltage Range
- Output Voltage Swings within 50 mV of both Rails
- No Phase Reversal on the Output for Over–Driven Input Signals
- High Output Current (I_{SC} = 80 mA, Typ)
- Low Supply Current (I_D = 0.9 mA, Typ)
- 600 Ω Output Drive Capability
- Typical Gain Bandwidth Product = 2.2 MHz

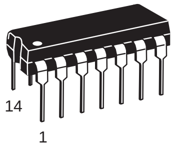
ORDERING INFORMATION

Operational Amplifier Function	Device	Operating Temperature Range	Package
Dual	MC33206D	T_A= –40 ° to +105°C	SO–14
	MC33206P		Plastic DIP
Quad	MC33207D		SO–16
	MC33207P		Plastic DIP

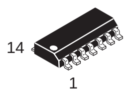
LOW VOLTAGE
RAIL–TO–RAIL
OPERATIONAL AMPLIFIERS

SEMICONDUCTOR
TECHNICAL DATA

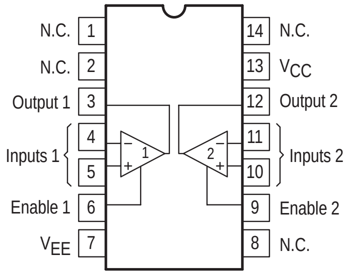
MC33206



P SUFFIX
PLASTIC PACKAGE
CASE 646

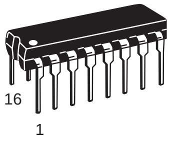


D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO–14)

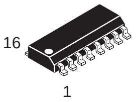


(Dual, Top View)

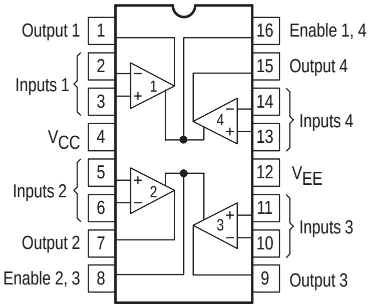
MC33207



P SUFFIX
PLASTIC PACKAGE
CASE 648



D SUFFIX
PLASTIC PACKAGE
CASE 751B
(SO–16)



(Quad, Top View)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage (V_{CC} to V_{EE})	V_S	13	V
ESD Protection Voltage at any Pin Human Body Model	V_{ESD}	2,000	V
Voltage at any Device Pin	V_{DP}	$V_S \pm 0.5$	V
Input Differential Voltage Range	V_{IDR}	(Note 1)	V
Common Mode Input Voltage Range (Note 2)	V_{CM}	$V_{CC} + 0.5$ to $V_{EE} – 0.5$	V
Output Short Circuit Duration (Note 3)	t_s	(Note 3)	sec
Maximum Junction Temperature	T_J	+150	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Maximum Power Dissipation	P_D	(Note 3)	mW

NOTES:
1. The differential input voltage of each amplifier is limited by two internal parallel back–to–back diodes. For additional differential input voltage range, use current limiting resistors in series with the input pins.
2. The common–mode input voltage range of each amplifier is limited by diodes connected from the inputs to both power supply rails. Therefore, the voltage on either input must not exceed either supply rail by more than 500 mV.
3. Power dissipation must be considered to ensure maximum junction temperature (T_J) is not exceeded.
4. ESD data available upon request.

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, V_{EE} = 0 V, V_{Enable} = 5.0 V, T_A = 25°C, unless otherwise noted.)

Characteristic	Figure	Symbol	Min	Typ	Max	Unit
Input Offset Voltage (V_{CM} 0 to 0.5 V, V_{CM} 1.0 to 5.0 V)	–	V_{IO}				mV
MC33206: T_A = 25°C			–	0.5	8.0	
T_A = –40° to +105°C			–	1.0	11	
MC33207: T_A = 25°C			–	0.5	10	
T_A = –40° to +105°C			–	1.0	13	
Input Offset Voltage Temperature Coefficient (R_S = 50 Ω) T_A = –40° to +105°C	–	$\Delta V_{IO}/\Delta T$	–	2.0	–	µV/°C
Input Bias Current (V_{CM} = 0 to 0.5 V, V_{CM} = 1.0 to 5.0 V)	–	$\lvert I_{IB} \rvert$				nA
T_A = 25°C			–	80	200	
T_A = –40° to +105°C			–	100	250	
Input Offset Current (V_{CM} = 0 to 0.5 V, V_{CM} = 1.0 to 5.0 V)	–	$\lvert I_{IO} \rvert$				nA
T_A = 25°C			–	5.0	50	
T_A = –40° to +105°C			–	10	100	
Common Mode Input Voltage Range	–	V_{ICR}	– V_{EE}	$V_{CC} + 0.2$ $V_{EE} – 0.2$	V_{CC} –	V
Large Signal Voltage Gain (V_{CC} = 5.0 V, V_{EE} = –5.0 V)	–	A_{VOL}				kV/V
R_L = 10 kΩ			50	300	–	
R_L = 600 Ω			25	250	–	
Output Voltage Swing (V_{ID} = ±0.2 V)	–					V
R_L = 10 kΩ		V_{OH}	4.85	4.95	–	
R_L = 10 kΩ		V_{OL}	–	0.05	0.15	
R_L = 600 Ω		V_{OH}	4.75	4.85	–	
R_L = 600 Ω		V_{OL}	–	0.15	0.25	
Common Mode Rejection (V_{in} = 0 to 5.0 V)	–	CMR	60	90	–	dB
Power Supply Rejection Ratio V_{CC}/V_{EE} = 5.0 V/Gnd to 3.0 V/Gnd	–	PSRR PSR	– 66	25 92	500 –	µV/V dB
Output Short Circuit Current (Source and Sink)	–	I_{SC}	50	80	–	mA

DC ELECTRICAL CHARACTERISTICS (continued) (V_{CC} = 5.0 V, V_{EE} = 0 V, V_{Enable} = 5.0 V, T_A = 25°C, unless otherwise noted.)

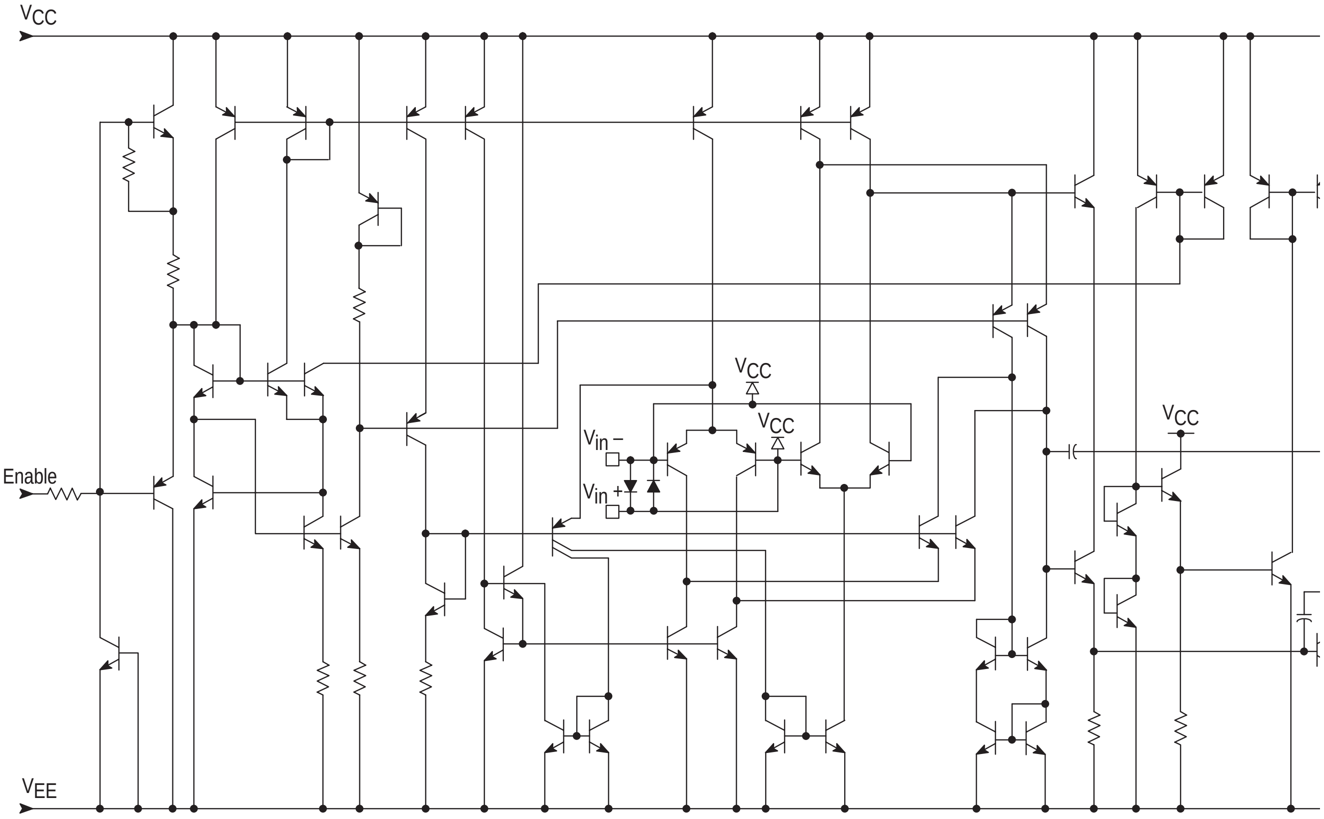
Characteristic	Figure	Symbol	Min	Typ	Max	Unit
Power Supply Current (V_O = 2.5 V, T_A = –40° to +105°C, per Amplifier)	–	I_D				
MC33206: V_{Enable} = 5.0 Vdc			–	0.8	1.125	mA
V_{Enable} = Gnd (Standby)			–	0.5	6.0	μA
MC33207: V_{Enable} = 5.0 Vdc			–	1.5	2.25	mA
V_{Enable} = Gnd (Standby)			–	0.5	6.0	μA
Enable Input Voltage (per Amplifier)	–	V_{Enable}				V
Enabled – Amplifier “On”			–	V_{EE} + 1.8	–	
Disabled – Amplifier “Off” (Standby)			–	V_{EE} + 0.3	–	
Enable Input Current (Note 5) (per Amplifier)	–	I_{Enable}				μA
V_{Enable} = 12 V			–	2.5	–	
V_{Enable} = 5.0 V			–	2.2	–	
V_{Enable} = 1.8 V			–	0.8	–	
V_{Enable} = Gnd			–	0	–	

NOTE: 5. External control circuitry must provide for an initial turn–off transient of <10 μA.

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, V_{EE} = 0 V, V_{Enable} = 5.0 V, T_A = 25°C, unless otherwise noted.)

Characteristic	Figure	Symbol	Min	Typ	Max	Unit
Slew Rate (V_S = ±2.5 V, V_O = –2.0 to +2.0 V, R_L = 2.0 kΩ, A_V = 1.0)	–	SR	0.5	1.0	–	V/μs
Gain Bandwidth Product (f = 100 kHz)	–	GBW	–	2.2	–	MHz
Phase Margin (R_L = 600 Ω, C_L = 0 pF)	–	$\emptyset_M$	–	65	–	Deg
Gain Margin (R_L = 600 Ω, C_L = 0 pF)	–	A_M	–	12	–	dB
Channel Separation (f = 1.0 Hz to 20 kHz, A_V = 100)	–	CS	–	90	–	dB
Power Bandwidth (V_O = 4.0 Vpp, R_L = 600 Ω, THD ≤ 1%)	–	BW_P	–	28	–	kHz
Total Harmonic Distortion (R_L = 600 Ω, V_O = 1.0 Vpp, A_V = 1.0)	–	THD				%
f = 1.0 kHz			–	0.002	–	
f = 10 kHz			–	0.008	–	
Open Loop Output Impedance (V_O = 0 V, f = 2.0 MHz, A_V = 10)	–	$\lvert Z_O \rvert$	–	100	–	Ω
Differential Input Resistance (V_{CM} = 0 V)	–	R_{in}	–	200	–	kΩ
Differential Input Capacitance (V_{CM} = 0 V)	–	C_{in}	–	8.0	–	pF
Equivalent Input Noise Voltage (R_S = 100 Ω)	–	e_n				$nV/\sqrt{Hz}$
f = 10 Hz			–	25	–	
f = 1.0 kHz			–	20	–	
Equivalent Input Noise Current	–	i_n				$pA/\sqrt{Hz}$
f = 10 Hz			–	0.8	–	
f = 1.0 kHz			–	0.2	–	
Time Delay for Device to Turn On	–	t_{on}	–	10	–	μs
Time Delay for Device to Turn Off	–	t_{off}	–	2.0	–	μs

Figure 1. Circuit Schematic
(Each Amplifier)



This device contains 96 active transistors (each amplifier).

Figure 2. Maximum Power Dissipation versus Temperature

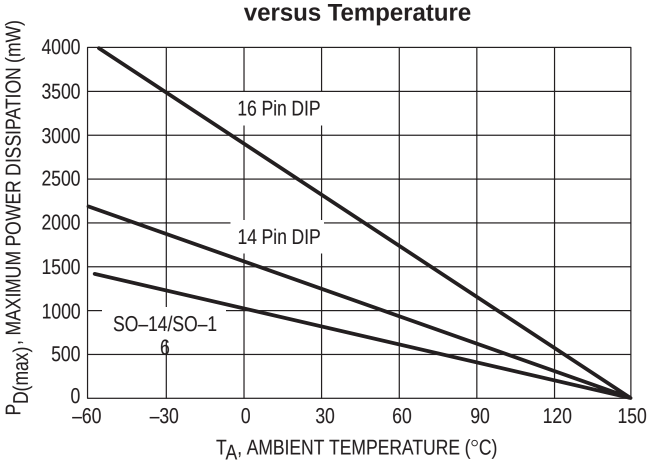


Figure 3. Input Offset Voltage Distribution

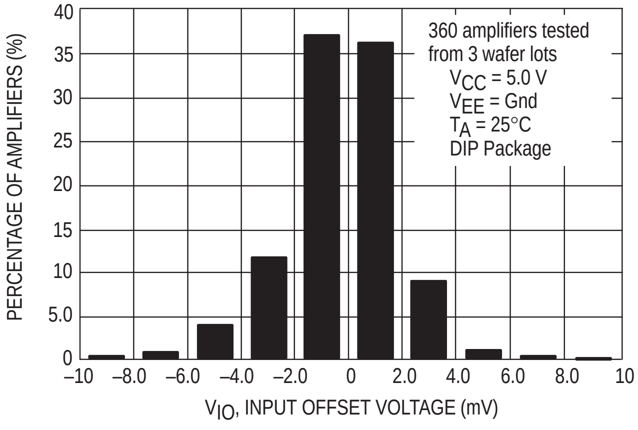


Figure 4. Input Offset Voltage Temperature Coefficient Distribution

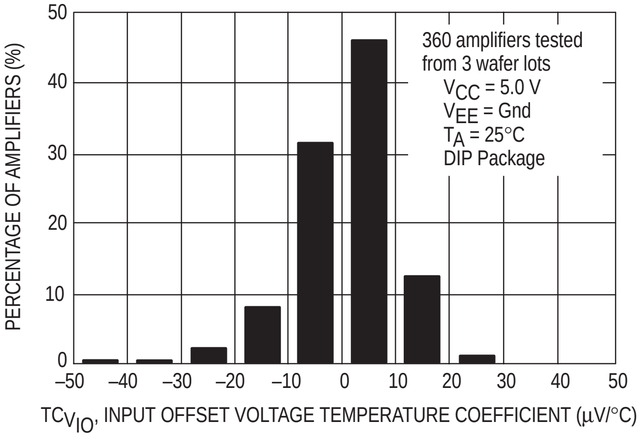


Figure 5. Input Bias Current versus Temperature

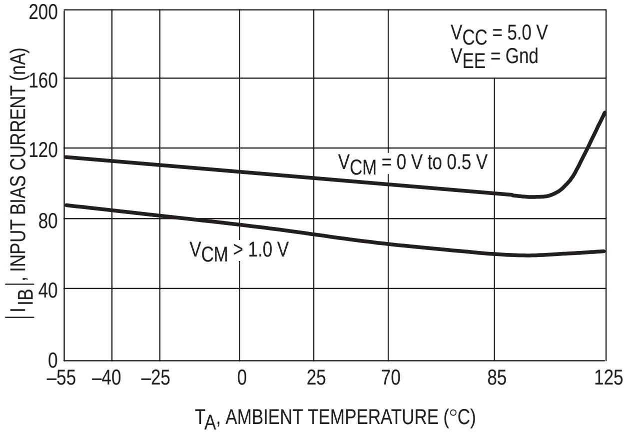


Figure 6. Input Bias Current versus Common Mode Voltage

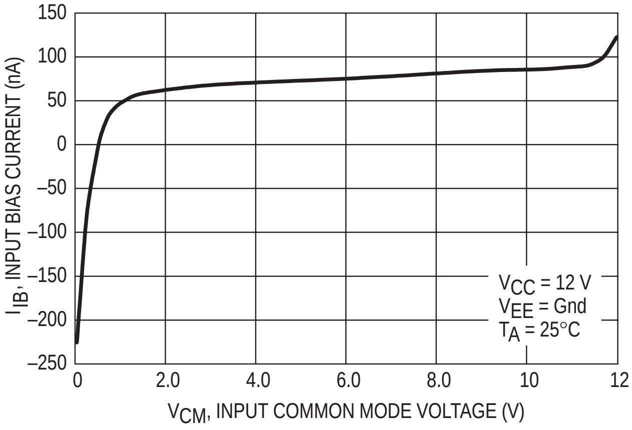


Figure 7. Open Loop Voltage Gain versus Temperature

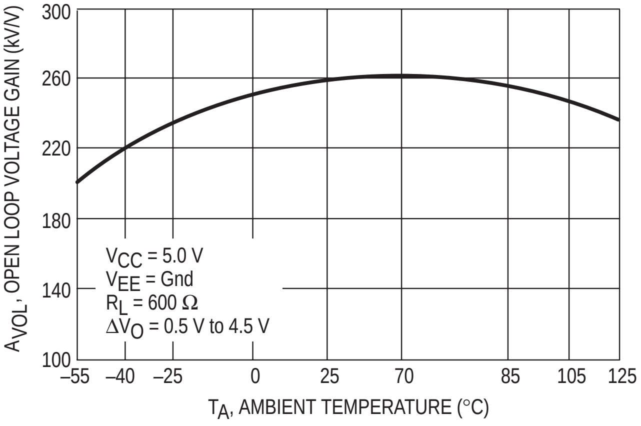


Figure 8. Output Voltage Swing versus Supply Voltage

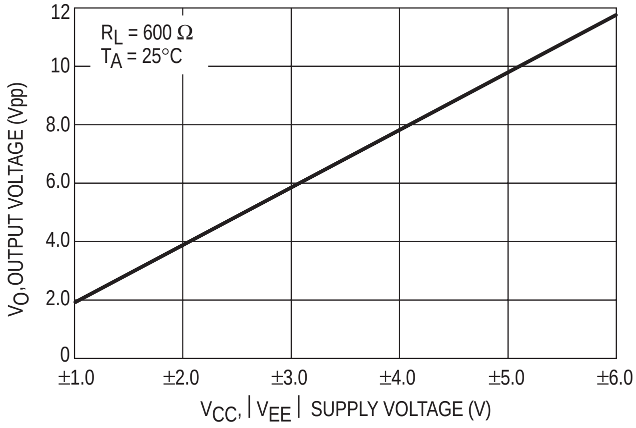


Figure 9. Output Saturation Voltage versus Load Current

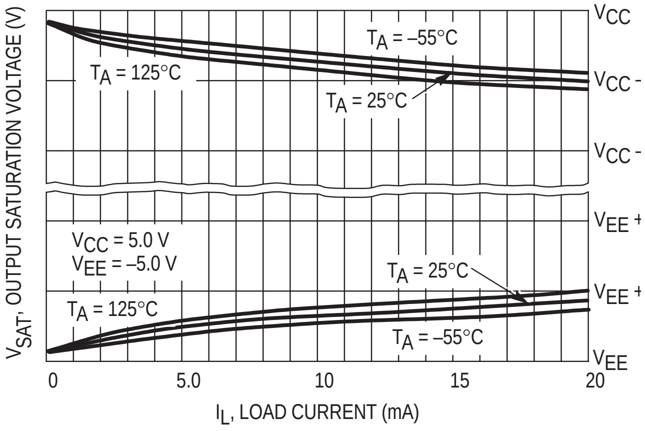


Figure 10. Output Voltage versus Frequency

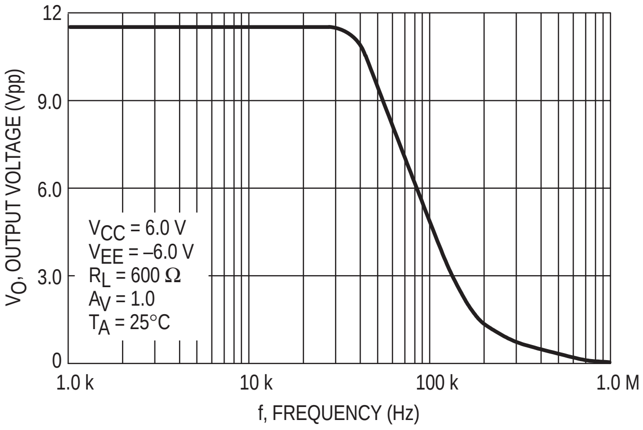


Figure 11. Common Mode Rejection versus Frequency

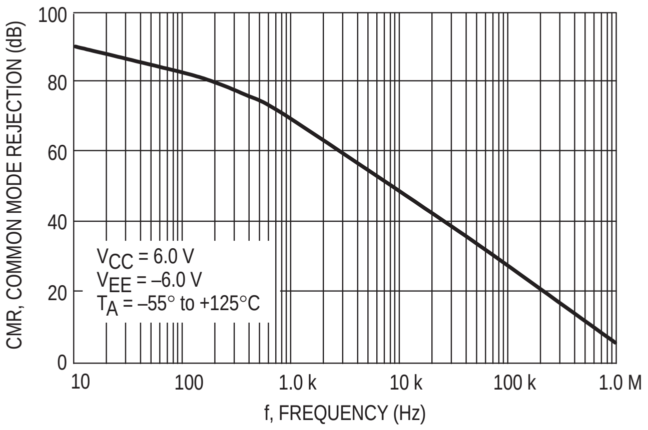


Figure 12. Power Supply Rejection versus Frequency

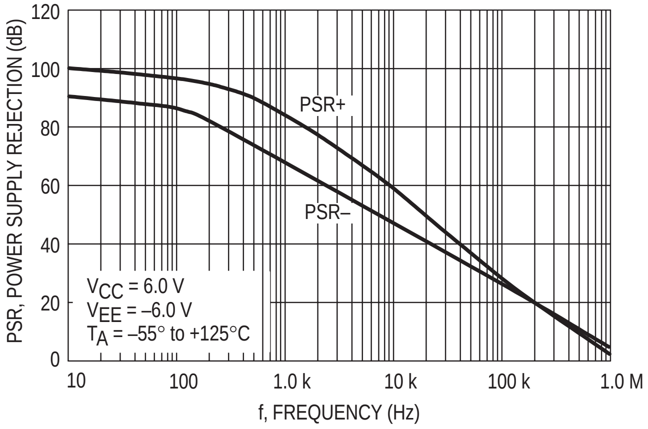


Figure 13. Output Short Circuit Current versus Output Voltage

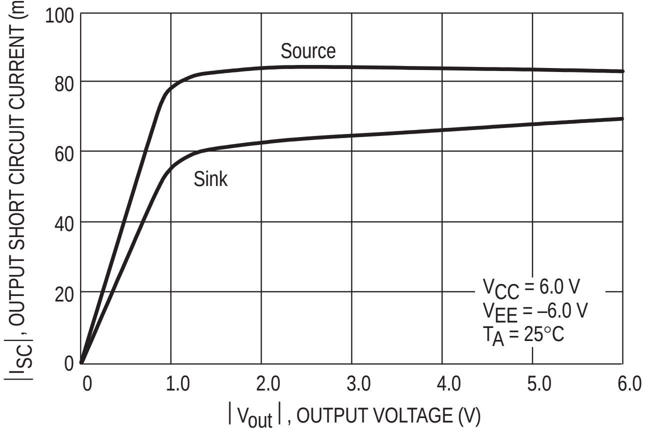


Figure 14. Output Short Circuit Current versus Temperature

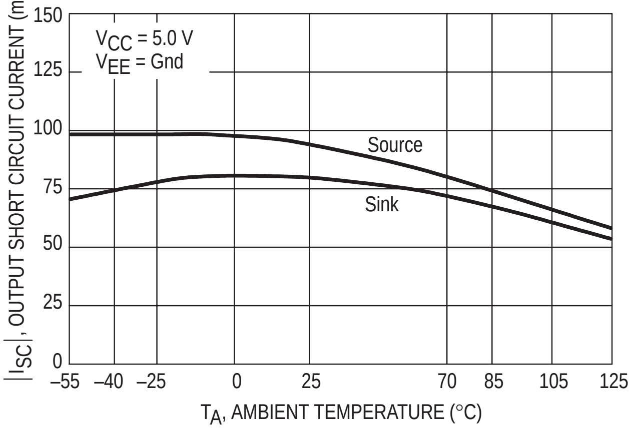


Figure 15. Supply Current per Amplifier versus Supply Voltage with No Load

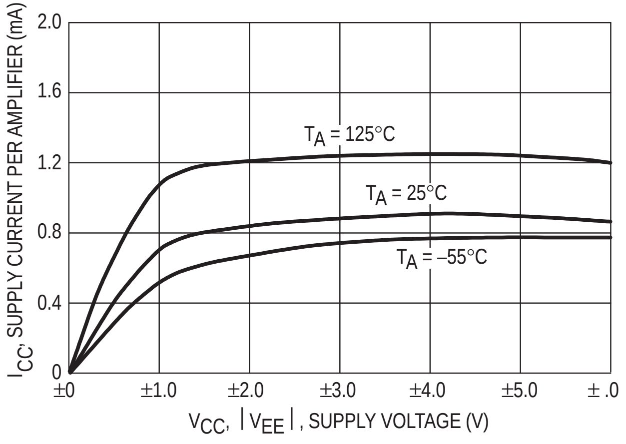


Figure 16. Slew Rate versus Temperature

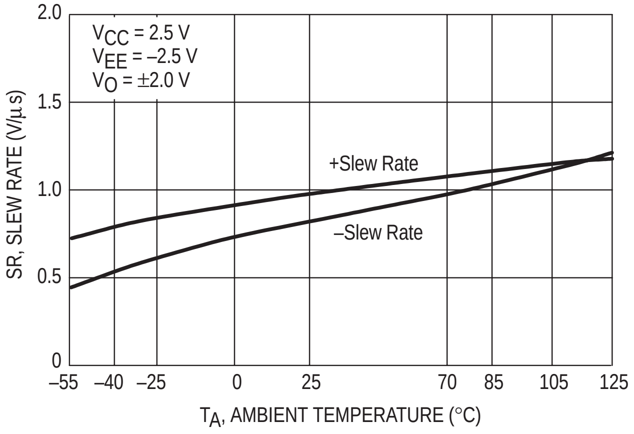


Figure 17. Gain Bandwidth Product versus Temperature

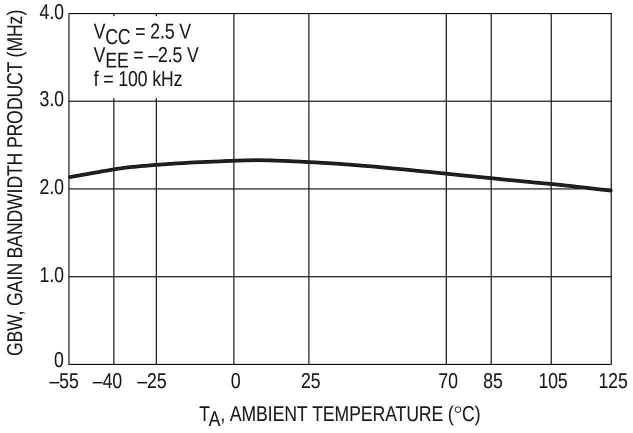


Figure 18. Voltage Gain and Phase versus Frequency

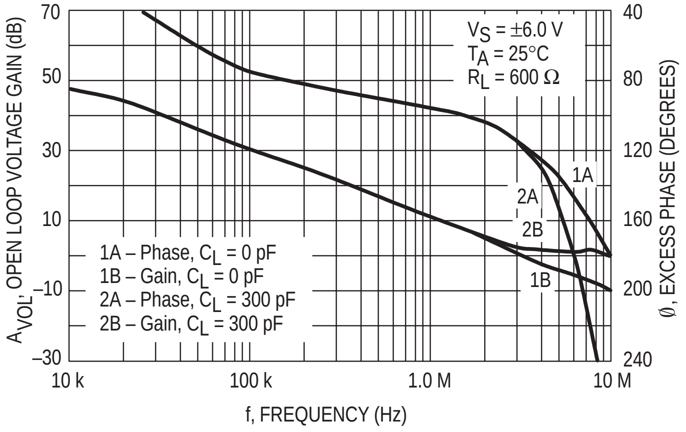


Figure 19. Voltage Gain and Phase versus Frequency

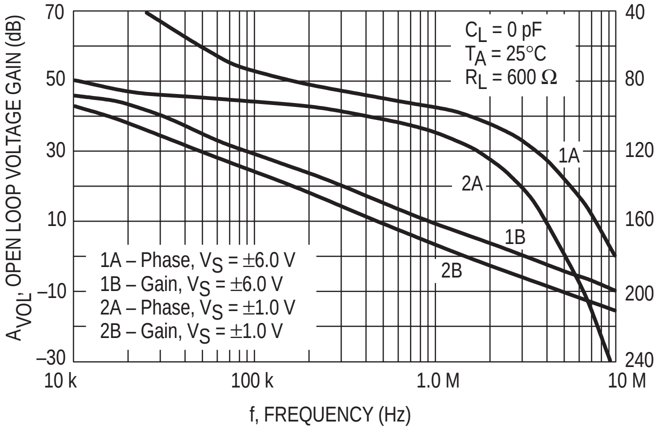


Figure 20. Gain and Phase Margin versus Temperature

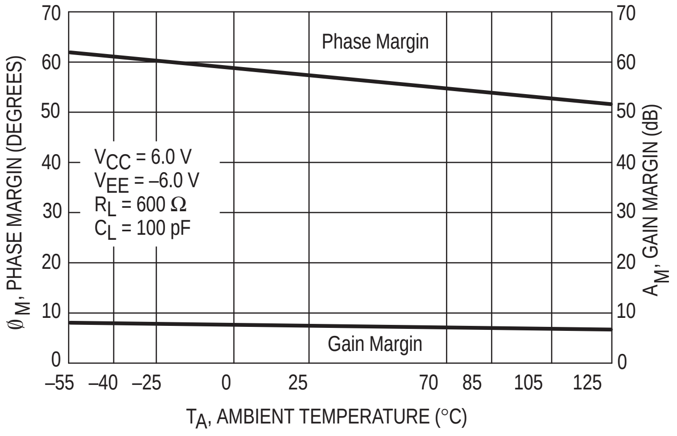


Figure 21. Gain and Phase Margin versus Differential Source Resistance

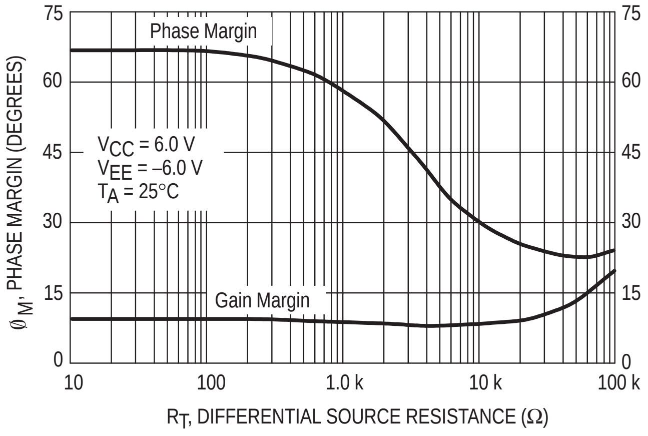


Figure 22. Gain and Phase Margin versus Capacitive Load

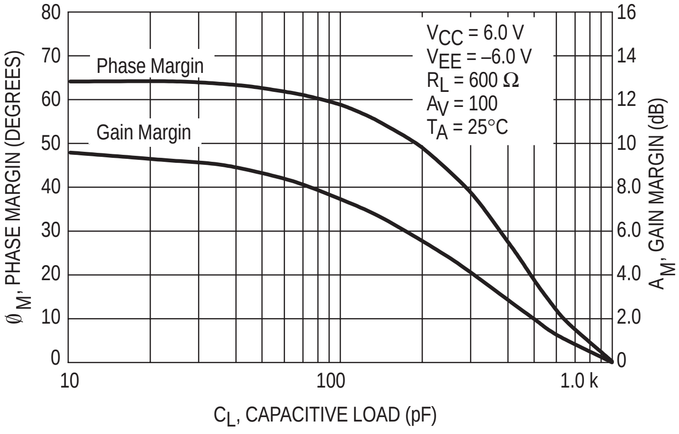


Figure 23. Output Voltage versus Load Resistance

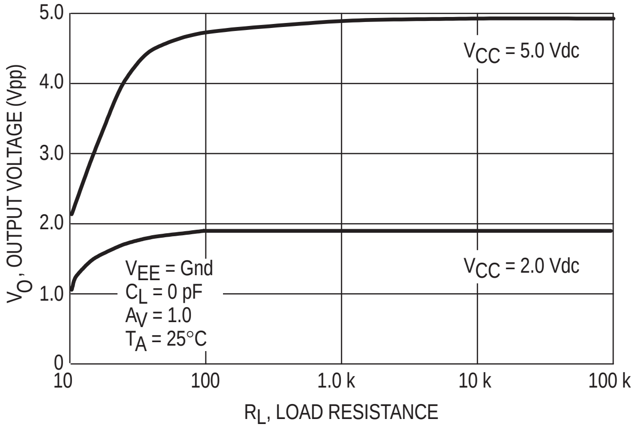


Figure 24. Channel Separation versus Frequency

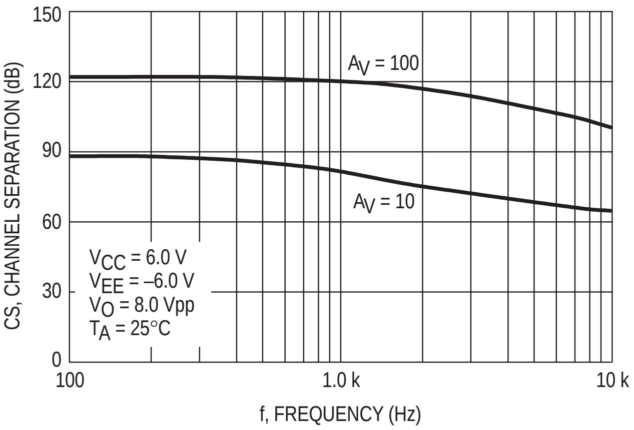


Figure 25. Total Harmonic Distortion versus Frequency

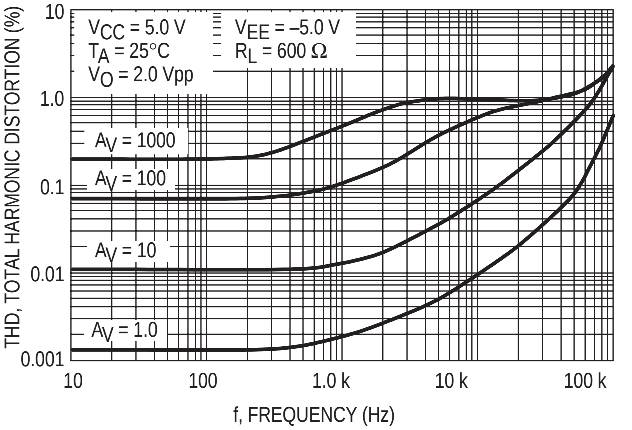
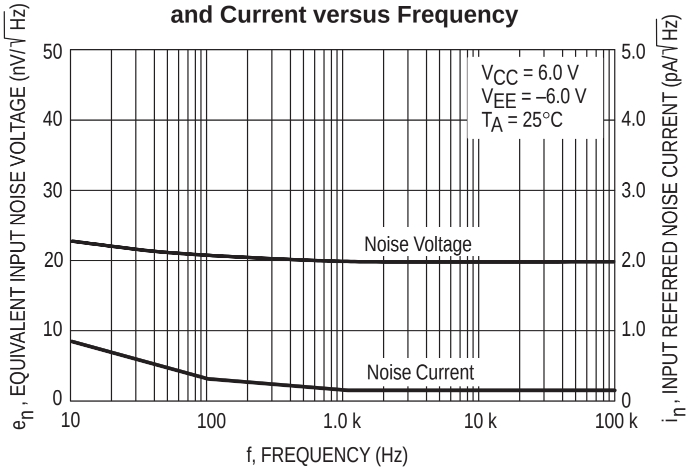


Figure 26. Equivalent Input Noise Voltage and Current versus Frequency



GENERAL INFORMATION

The MC33206/7 family of operational amplifiers are unique in their ability to swing rail–to–rail on both the input and the output with a completely bipolar design. This offers low noise, high output current capability and a wide common mode input voltage range even with low supply voltages. Operation is guaranteed over an extended temperature range and at supply voltages of 2.0 V, 3.3 V and 5.0 V and ground.

Since the common mode input voltage range extends from V_{CC} to V_{EE}, it can be operated with either single or split voltage supplies. The MC33206/7 are guaranteed not to latch or phase reverse over the entire common mode range, however, the inputs should not be allowed to exceed maximum ratings.

CIRCUIT INFORMATION

Rail–to–rail performance is achieved at the input of the amplifiers by using parallel NPN–PNP differential input stages. When the inputs are within 800 mV of the negative rail, the PNP stage is on. When the inputs are more than 800 mV greater than V_{EE}, the NPN stage is on. This switching of input pairs will cause a reversal of input bias currents (see Figure 6). Also, slight differences in offset voltage may be noted between the NPN and PNP pairs. Cross–coupling techniques have been used to keep this change to a minimum.

In addition to its rail–to–rail performance, the output stage is current boosted to provide 80 mA of output current, enabling the op amp to drive 600 Ω loads. Because of this high output current capability, care should be taken not to exceed the 150°C maximum junction temperature.

Enable Function

The MC33206/07 enable pins allow the user to externally control the device. (Refer to the Pin Diagram on the first page of this data sheet for enable pin connections.) If the enable pins are pulled low (Gnd) each amplifier (MC33206) and amplifier pair (MC33207) will be disabled. When the enable pins are at a logic high ($V_{Enable} \geq V_{EE} = 1.8$ V) the amplifiers will turn "on". Refer to the data sheet characteristics for the required levels needed to change logical state.

The time to change states (from device "on" to "off" and "off" to "on") is defined as the time delay. The Circuit in Figure 27 is used to measure t_{on} and t_{off}. Typical t_{on} and t_{off} measurements are shown in Figures 28 and 29. When the device is turned off (V_{Enable} = Gnd) an internal regulator is shut off disabling the amplifier.

Figure 27. Test Circuit for t_{on} and t_{off}

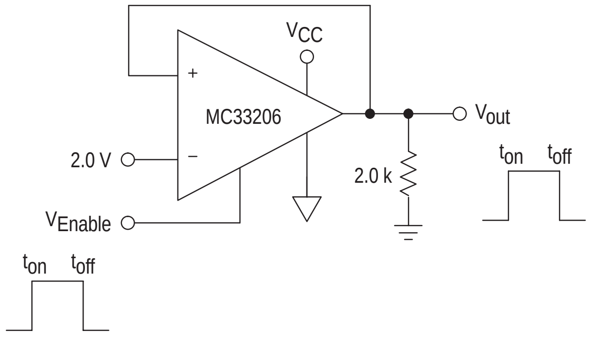


Figure 28. t_{on} Response

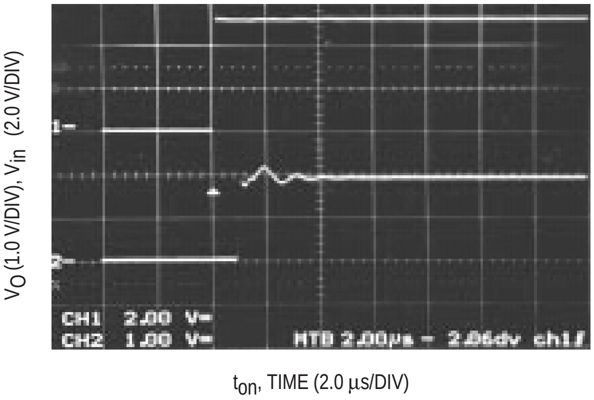
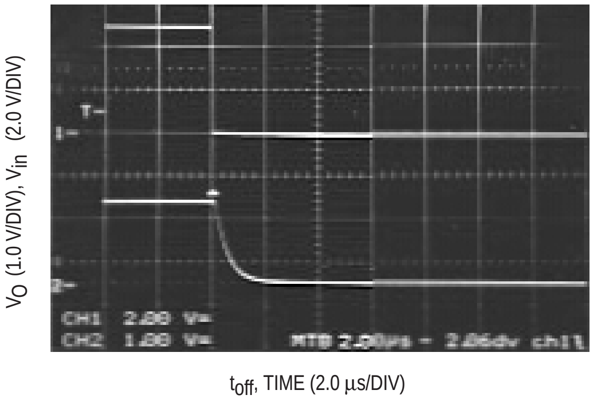


Figure 29. t_{off} Response



Low Voltage Operation

The MC33206/07 will operate at supply voltages down to 1.8 V and ground. Since this device is a rail–to–rail on both the input and output, one can be assured of continued operation in battery applications when battery voltages drop to low voltage levels. This is called End of Discharge (see Figure 30). Now, the user can select a minimum quantity of batteries best suited for the particular design depending on the type of battery chosen. This will minimize part count in many designs.

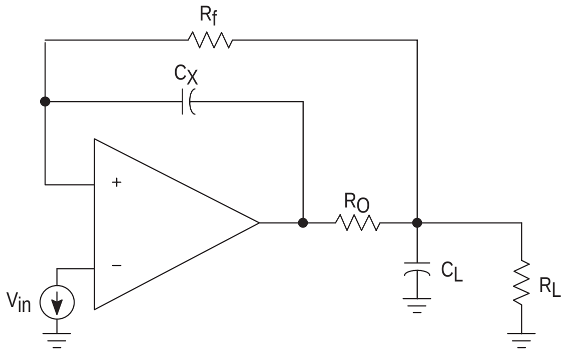
Figure 30. Typical Battery Characteristics

Type	Operating Voltage	End of Discharge
Alkaline	1.5 V	0.9 V
NiCd	1.2 V	1.0 V
NiMh	1.2 V	1.0 V
Silver Oxide	1.6 V	1.3 V
Lithium Ion	3.6 V	2.5 V

Compensating for Output Capacitance

The combination of device output impedance and increasing capacitive loading will cause phase delay (reducing the phase margin) in any amplifier (Figure 22). If the loading is excessive, the resulting response can be circuit oscillation. In other words, an amplifier can become unstable when the phase becomes greater than 180 degrees before the open loop gain drops to unity gain. Figures 18 and 19 show this situation as frequency increases for a given load. The MC33206/7 can typically drive up to 300 pF loads at unity gain without oscillating.

Figure 31. Capacitive Loads Compensation



There are several ways to compensate for this phenomena. Adding series resistance to the output is one way, but not an ideal solution. A dc voltage error will occur at the output. A better design solution to compensate for higher capacitive loads would be to use the circuit in Figure 31. This design helps to counteract the loss of phase margin by taking the high frequency output signal and feeding it back into the amplifier inverting input. This technique helps to overcome oscillation due to a highly capacitive load. Keep in mind that compensation will have the affect of lowering the Gain Bandwidth Product (GPW). The values of C_X and R0, are determined experimentally. Typical C_X and C_L will be the same value.

SPICE Model

If a SPICE Macromodel is desired for the MC33206/07, the user can define the characteristics from the following information. Obtain the SPICE Macromodel for the MC33204 Rail–to–Rail Operational Amplifier (device is the same as the MC33207). For the Enable feature of the MC33207, simulate it as a bipolar switch. The Macromodel does not include an input capacitance between the inverting and noninverting inputs. This capacitor is called C_{in}. Add 3.0 to 5.0 pF if stability analysis is required.

Figure 32. Noninverting Amplifier Slew Rate

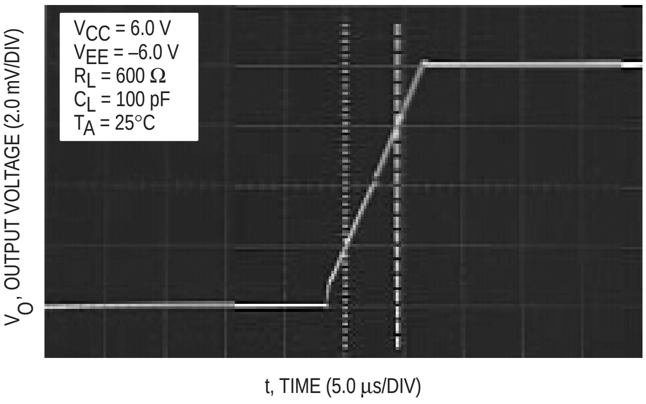


Figure 33. Small Signal Transient Response

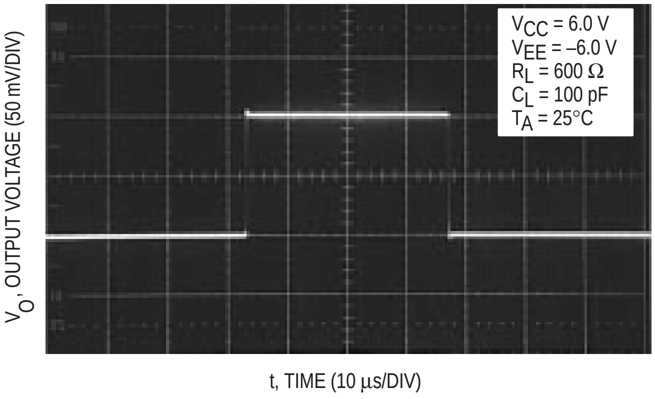
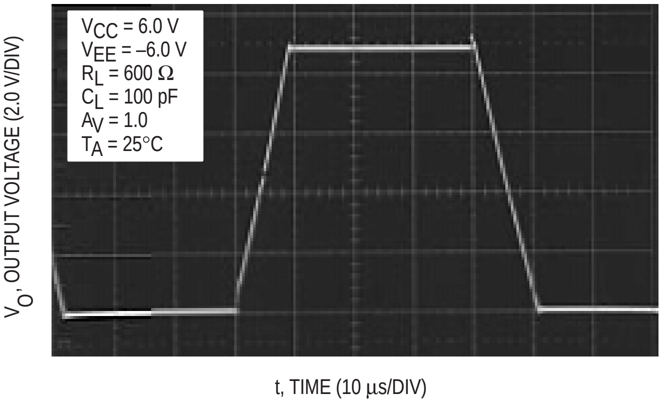


Figure 34. Large Signal Transient Response



MOTOROLA

MC33272A
MC33274A

Single Supply, High Slew Rate Low Input Offset Voltage, Bipolar Operational Amplifiers

The MC33272/74 series of monolithic operational amplifiers are quality fabricated with innovative Bipolar design concepts. This dual and quad operational amplifier series incorporates Bipolar inputs along with a patented Zip–R–Trim element for input offset voltage reduction. The MC33272/74 series of operational amplifiers exhibits low input offset voltage and high gain bandwidth product. Dual–doublet frequency compensation is used to increase the slew rate while maintaining low input noise characteristics. Its all NPN output stage exhibits no deadband crossover distortion, large output voltage swing, and an excellent phase and gain margin. It also provides a low open loop high frequency output impedance with symmetrical source and sink AC frequency performance.

The MC33272/74 series is specified over –40° to +85°C and are available in plastic DIP and SOIC surface mount packages.

- Input Offset Voltage Trimmed to 100 µV (Typ)
- Low Input Bias Current: 300 nA
- Low Input Offset Current: 3.0 nA
- High Input Resistance: 16 MΩ
- Low Noise: 18 nV/ $\sqrt{\text{Hz}}$ @ 1.0 kHz
- High Gain Bandwidth Product: 24 MHz @ 100 kHz
- High Slew Rate: 10 V/µs
- Power Bandwidth: 160 kHz
- Excellent Frequency Stability
- Unity Gain Stable: w/Capacitance Loads to 500 pF
- Large Output Voltage Swing: +14.1 V/ –14.6 V
- Low Total Harmonic Distortion: 0.003%
- Power Supply Drain Current: 2.15 mA per Amplifier
- Single or Split Supply Operation: +3.0 V to +36 V or ±1.5 V to ±18 V
- ESD Diodes Provide Added Protection to the Inputs

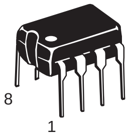
ORDERING INFORMATION

Op Amp Function	Device	Operating Temperature Range	Package
Dual	MC33272AD	T_A = –40° to +85°C	SO–8
	MC33272AP		Plastic DIP
Quad	MC33274AD		SO–14
	MC33274AP		Plastic DIP

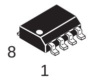
HIGH PERFORMANCE OPERATIONAL AMPLIFIERS

SEMICONDUCTOR TECHNICAL DATA

DUAL

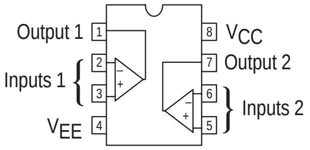


P SUFFIX
PLASTIC PACKAGE
CASE 626



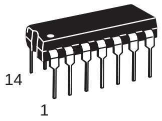
D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

PIN CONNECTIONS

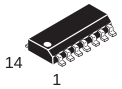


(Top View)

QUAD

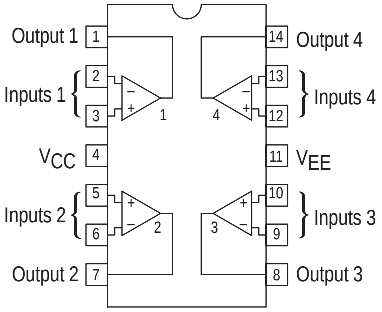


P SUFFIX
PLASTIC PACKAGE
CASE 646



D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO–14)

PIN CONNECTIONS



(Top View)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC} to V_{EE}	+36	V
Input Differential Voltage Range	V_{IDR}	(Note 1)	V
Input Voltage Range	V_{IR}	(Note 1)	V
Output Short Circuit Duration (Note 2)	t_{SC}	Indefinite	sec
Maximum Junction Temperature	T_J	+150	°C
Storage Temperature	T_{stg}	–60 to +150	°C
Maximum Power Dissipation	P_D	(Note 2)	mW

NOTES: 1. Either or both input voltages should not exceed V_{CC} or V_{EE}.
2. Power dissipation must be considered to ensure maximum junction temperature (T_J) is not exceeded (see Figure 2).

DC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = –15 V, T_A = 25°C, unless otherwise noted.)

Characteristics	Figure	Symbol	Min	Typ	Max	Unit
Input Offset Voltage (R_S = 10 Ω, V_{CM} = 0 V, V_O = 0 V)	3	$\|V_{IO}\|$				mV
(V_{CC} = +15 V, V_{EE} = –15 V)						
T_A = +25°C			—	0.1	1.0	
T_A = –40° to +85°C			—	—	1.8	
(V_{CC} = 5.0 V, V_{EE} = 0)						
T_A = +25°C			—	—	2.0	
Average Temperature Coefficient of Input Offset Voltage	3	$\Delta V_{IO}/\Delta T$				µV/°C
R_S = 10 Ω, V_{CM} = 0 V, V_O = 0 V, T_A = –40° to +85°C			—	2.0	—	
Input Bias Current (V_{CM} = 0 V, V_O = 0 V)	4, 5	I_{IB}				nA
T_A = +25°C			—	300	650	
T_A = –40° to +85°C			—	—	800	
Input Offset Current (V_{CM} = 0 V, V_O = 0 V)		$\|I_{IO}\|$				nA
T_A = +25°C			—	3.0	65	
T_A = –40° to +85°C			—	—	80	
Common Mode Input Voltage Range (ΔV_{IO} = 5.0 mV, V_O = 0 V)	6	V_{ICR}				V
T_A = +25°C			V_{EE} to (V_{CC} –1.8)			
Large Signal Voltage Gain (V_O = 0 V to 10 V, R_L = 2.0 kΩ)	7	A_{VOL}				dB
T_A = +25°C			90	100	—	
T_A = –40° to +85°C			86	—	—	
Output Voltage Swing (V_{ID} = ±1.0 V)	8, 9, 12					V
(V_{CC} = +15 V, V_{EE} = –15 V)						
R_L = 2.0 kΩ		V_O+	13.4	13.9	—	
R_L = 2.0 kΩ		V_O-	—	–13.9	–13.5	
R_L = 10 kΩ		V_O+	13.4	14	—	
R_L = 10 kΩ		V_O-	—	–14.7	–14.1	
(V_{CC} = 5.0 V, V_{EE} = 0 V)	10, 11					
R_L = 2.0 kΩ		V_{OL}	—	—	0.2	
R_L = 2.0 kΩ		V_{OH}	3.7	—	5.0	
Common Mode Rejection (V_{in} = +13.2 V to –15 V)	13	CMR	80	100	—	dB
Power Supply Rejection	14, 15	PSR				dB
V_{CC}/V_{EE} = +15 V/ –15 V, +5.0 V/ –15 V, +15 V/ –5.0 V			80	105	—	
Output Short Circuit Current (V_{ID} = 1.0 V, Output to Ground)	16	I_{SC}				mA
Source			+25	+37	—	
Sink			–25	–37	—	
Power Supply Current Per Amplifier (V_O = 0 V)	17	I_{CC}				mA
(V_{CC} = +15 V, V_{EE} = –15 V)						
T_A = +25°C			—	2.15	2.75	
T_A = –40° to +85°C			—	—	3.0	
(V_{CC} = 5.0 V, V_{EE} = 0 V)						
T_A = +25°C			—	—	2.75	

AC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = –15 V, T_A = 25°C, unless otherwise noted.)

Characteristics	Figure	Symbol	Min	Typ	Max	Unit
Slew Rate (V_{in} = –10 V to +10 V, R_L = 2.0 kΩ, C_L = 100 pF, A_V = +1.0 V)	18, 33	SR	8.0	10	—	V/µs
Gain Bandwidth Product (f = 100 kHz)	19	GBW	17	24	—	MHz
AC Voltage Gain (R_L = 2.0 kΩ, V_O = 0 V, f = 20 kHz)	20, 21, 22	A_{VO}	—	65	—	dB
Unity Gain Frequency (Open Loop)		f_U	—	5.5	—	MHz
Gain Margin (R_L = 2.0 kΩ, C_L = 0 pF)	23, 24, 26	A_m	—	12	—	dB
Phase Margin (R_L = 2.0 kΩ, C_L = 0 pF)	23, 25, 26	ϕ_m	—	55	—	Degrees
Channel Separation (f = 20 Hz to 20 kHz)	27	CS	—	–120	—	dB
Power Bandwidth (V_O = 20 V_{pp}, R_L = 2.0 kΩ, THD ≤ 1.0%)		BW_P	—	160	—	kHz
Total Harmonic Distortion (R_L = 2.0 kΩ, f = 20 Hz to 20 kHz, V_O = 3.0 V_{rms}, A_V = +1.0)	28	THD	—	0.003	—	%
Open Loop Output Impedance (V_O = 0 V, f = 6.0 MHz)	29	$\lvert Z_O \rvert$	—	35	—	Ω
Differential Input Resistance (V_{CM} = 0 V)		R_{IN}	—	16	—	MΩ
Differential Input Capacitance (V_{CM} = 0 V)		C_{IN}	—	3.0	—	pF
Equivalent Input Noise Voltage (R_S = 100 Ω, f = 1.0 kHz)	30	e_n	—	18	—	$nV/\sqrt{Hz}$
Equivalent Input Noise Current (f = 1.0 kHz)	31	i_n	—	0.5	—	$pA/\sqrt{Hz}$

Figure 1. Equivalent Circuit Schematic
(Each Amplifier)

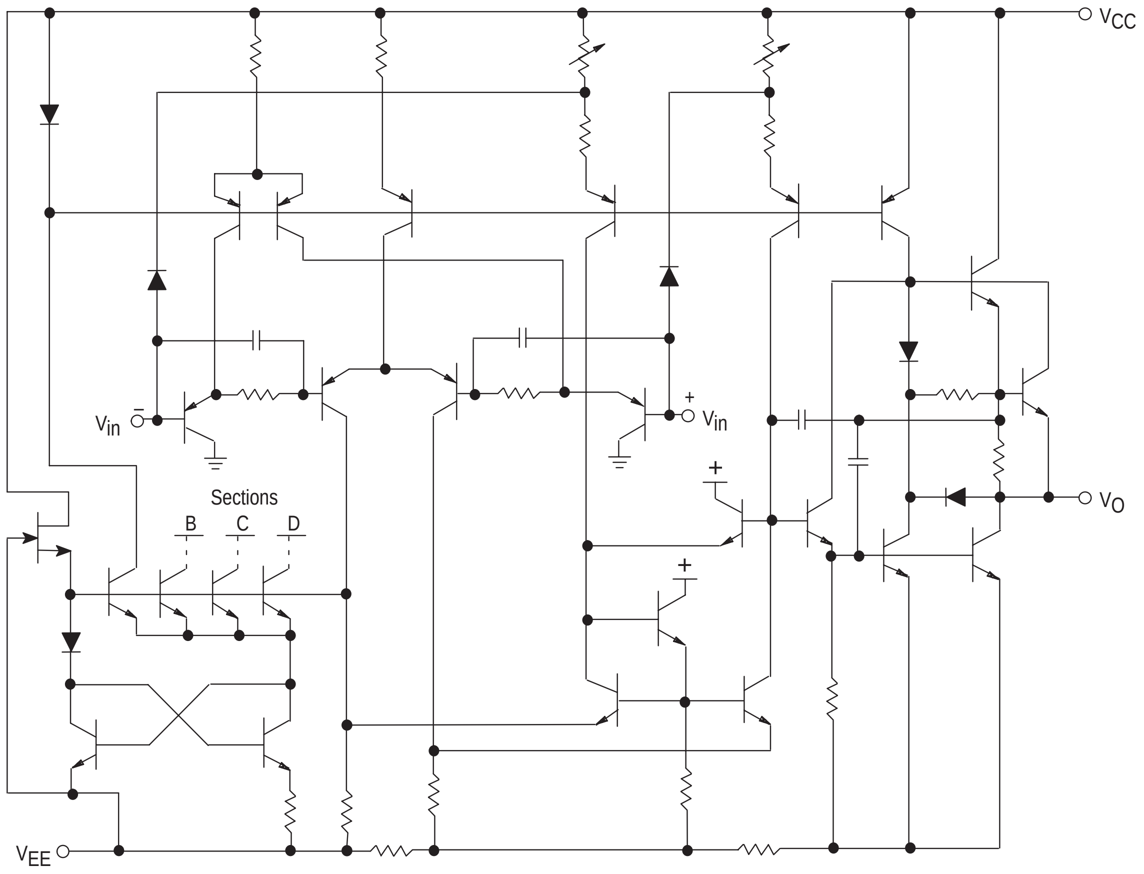


Figure 2. Maximum Power Dissipation versus Temperature

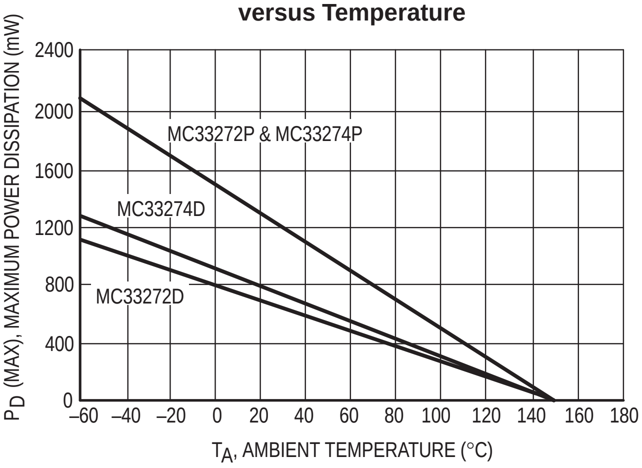


Figure 3. Input Offset Voltage versus Temperature for Typical Units

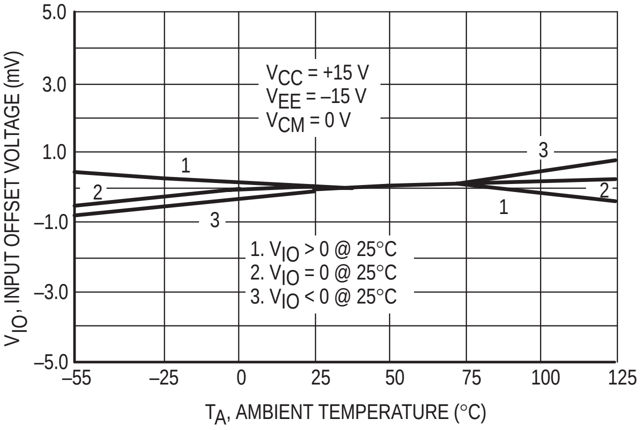


Figure 4. Input Bias Current versus Common Mode Voltage

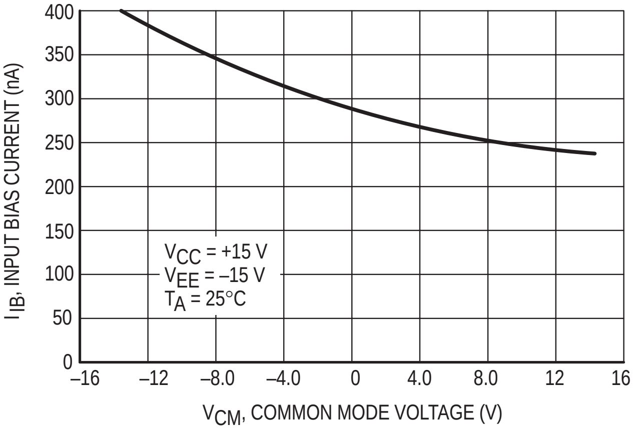


Figure 5. Input Bias Current versus Temperature

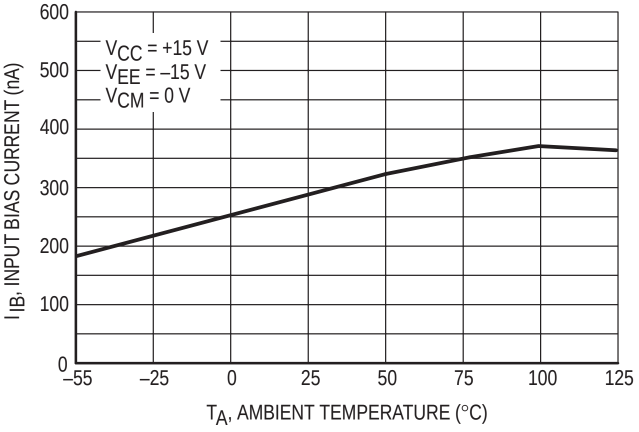


Figure 6. Input Common Mode Voltage Range versus Temperature

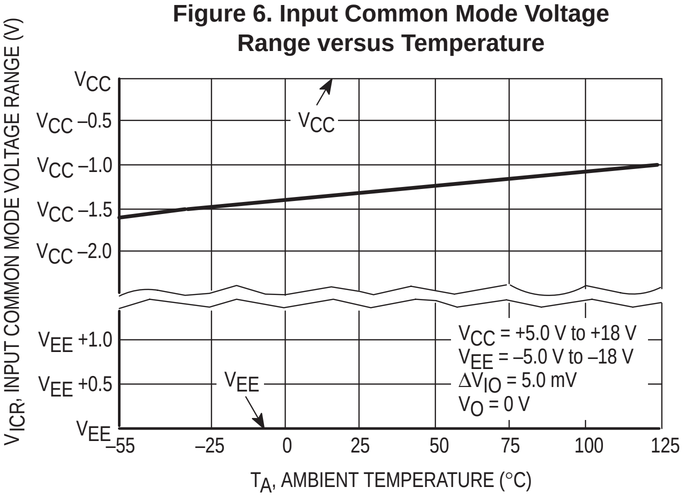


Figure 7. Open Loop Voltage Gain versus Temperature

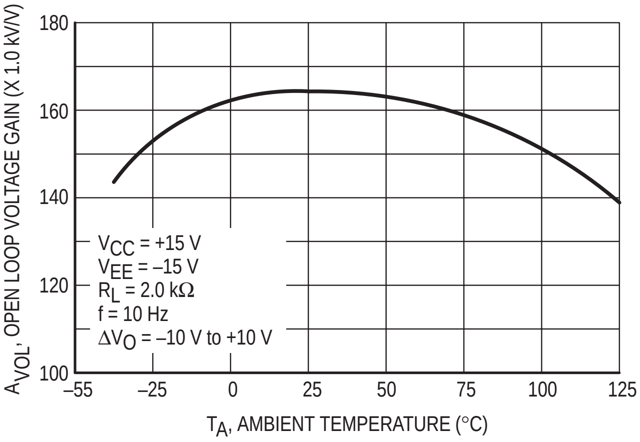


Figure 8. Split Supply Output Voltage Swing versus Supply Voltage

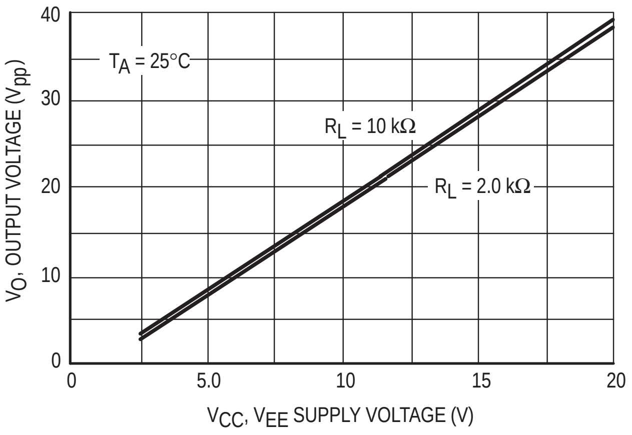


Figure 9. Split Supply Output Saturation Voltage versus Load Current

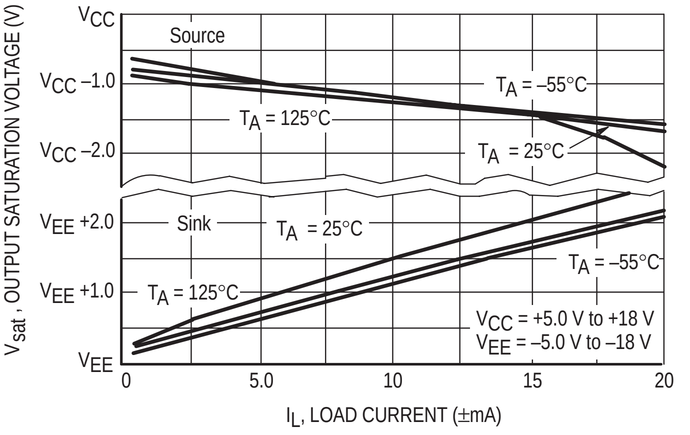


Figure 10. Single Supply Output Saturation Voltage versus Load Resistance to Ground

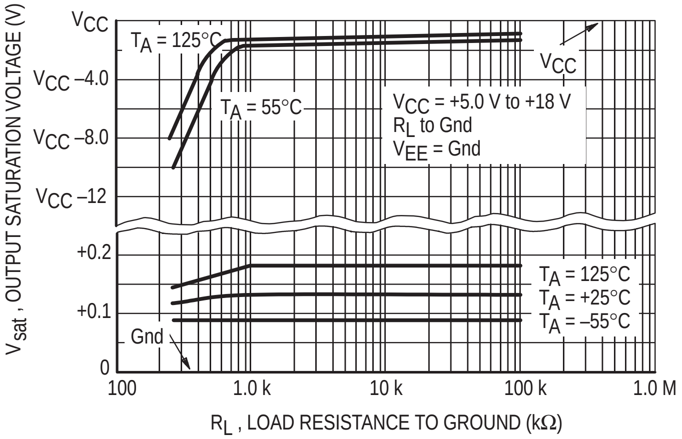


Figure 11. Single Supply Output Saturation Voltage versus Load Resistance to V_{CC}

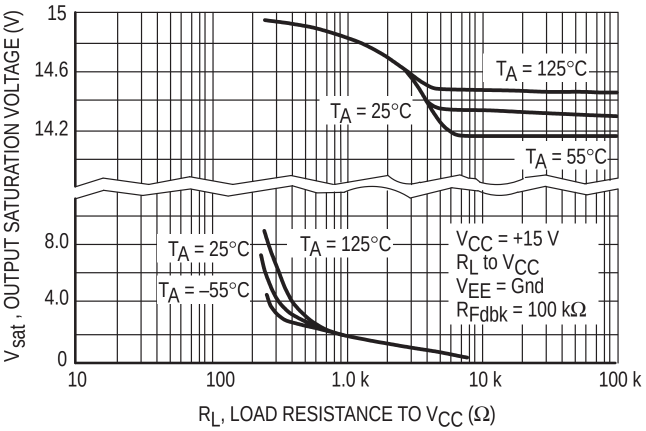


Figure 12. Output Voltage versus Frequency

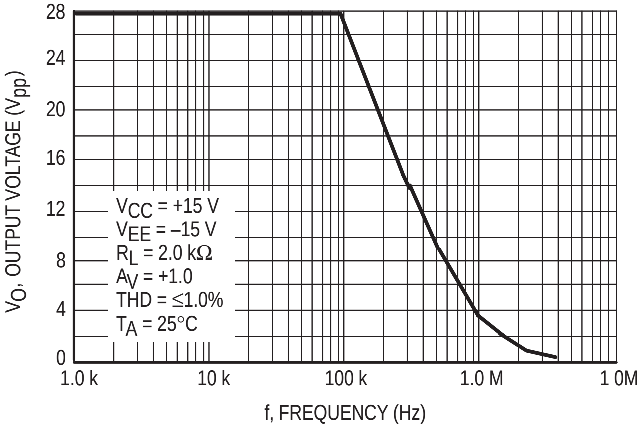


Figure 13. Common Mode Rejection versus Frequency

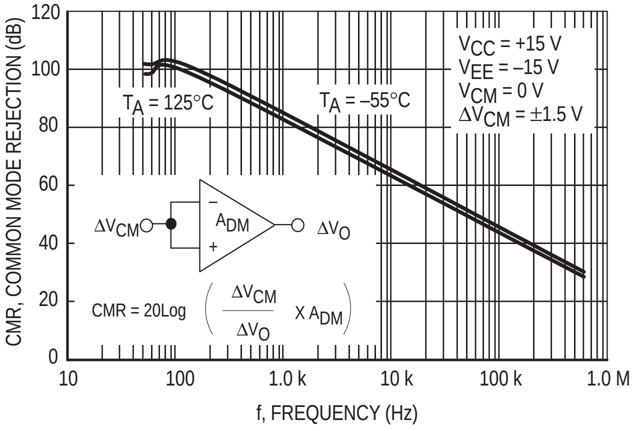


Figure 14. Positive Power Supply Rejection versus Frequency

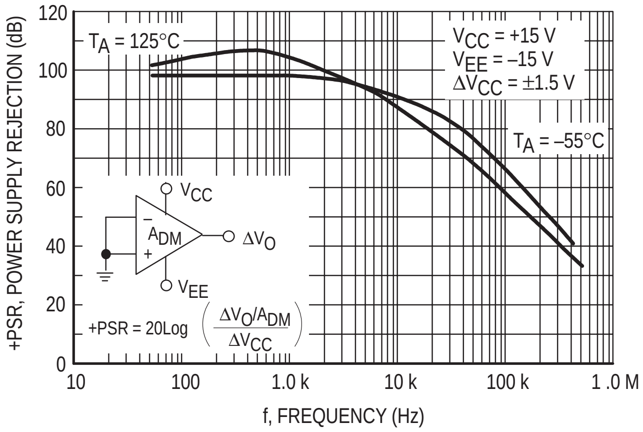


Figure 15. Negative Power Supply Rejection versus Frequency

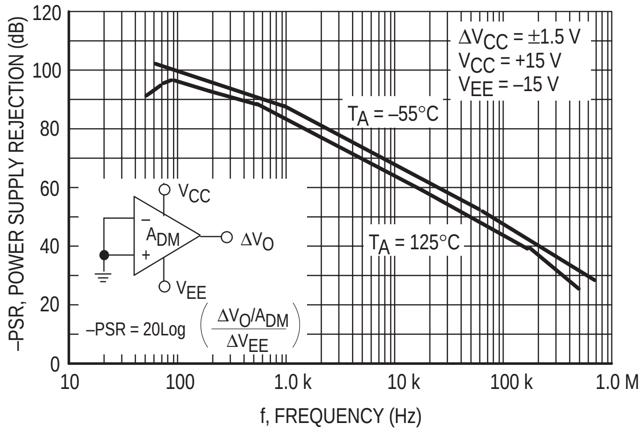


Figure 16. Output Short Circuit Current versus Temperature

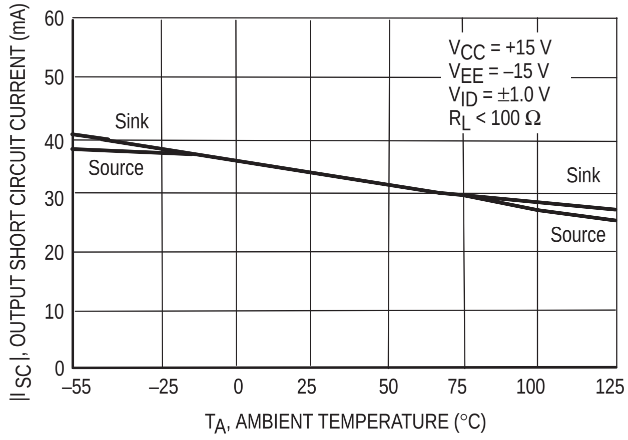


Figure 17. Supply Current versus Supply Voltage

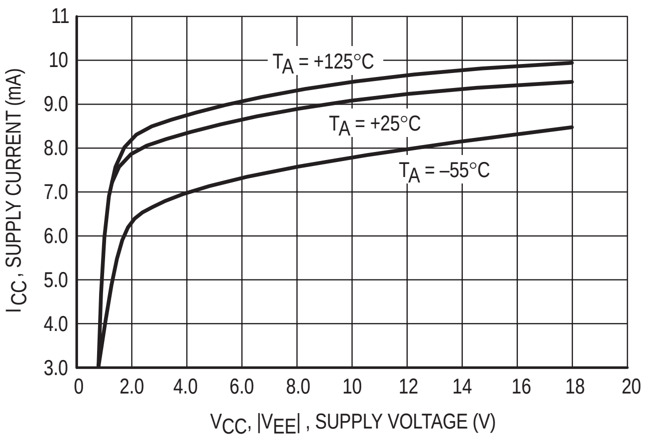


Figure 18. Normalized Slew Rate versus Temperature

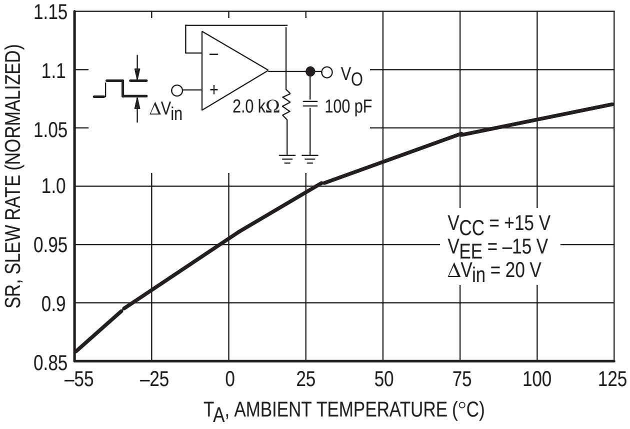


Figure 19. Gain Bandwidth Product versus Temperature

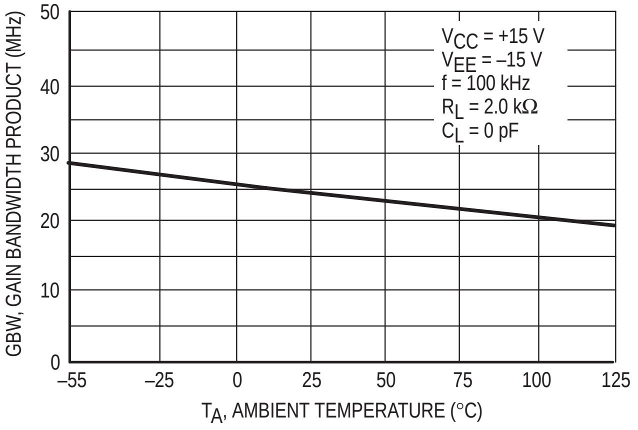


Figure 20. Voltage Gain and Phase versus Frequency

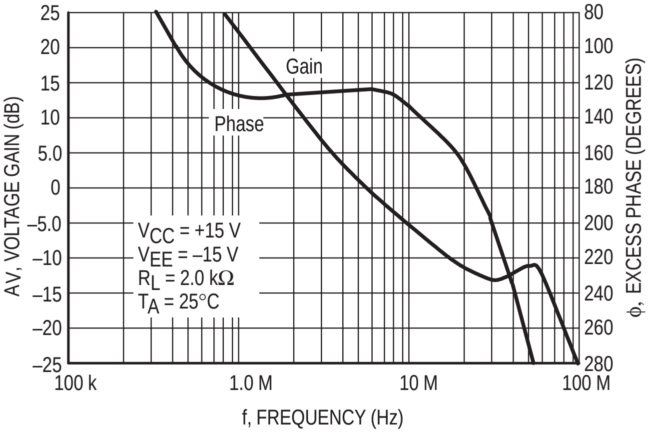


Figure 21. Gain and Phase versus Frequency

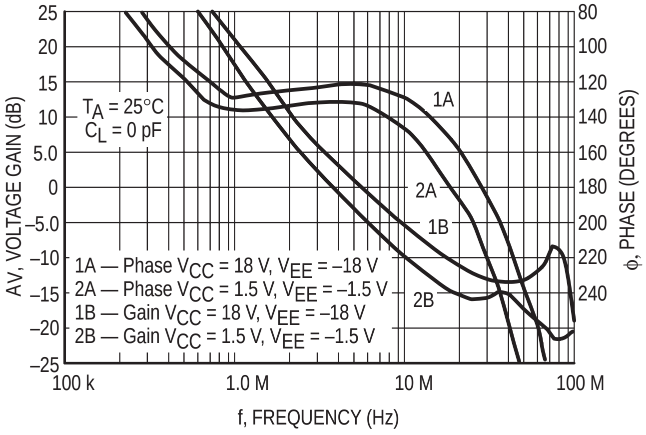


Figure 22. Open Loop Voltage Gain and Phase versus Frequency

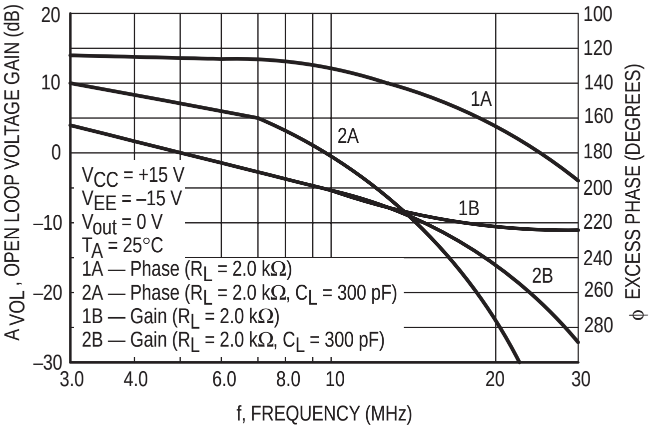


Figure 23. Open Loop Gain Margin and Phase Margin versus Output Load Capacitance

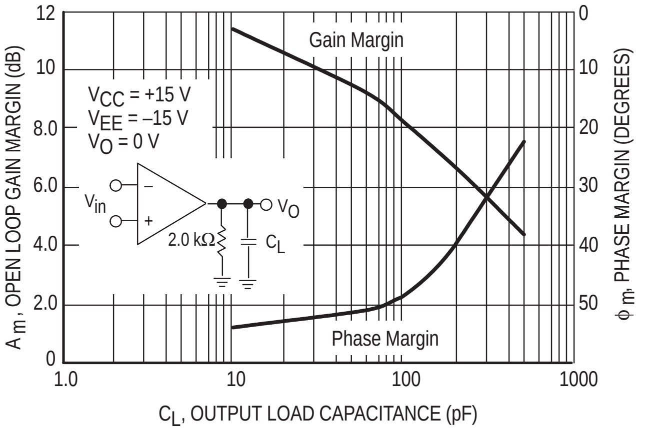


Figure 24. Open Loop Gain Margin versus Temperature

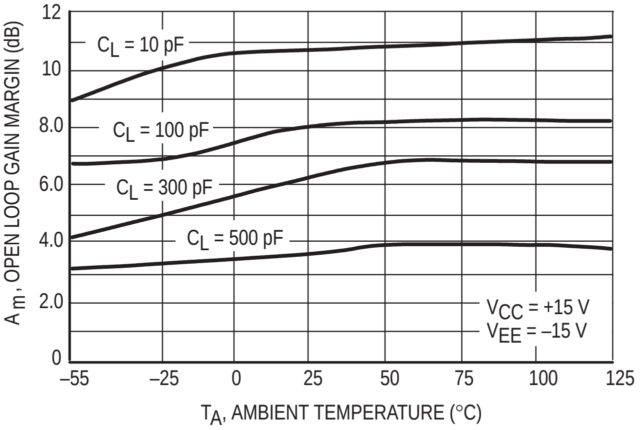


Figure 25. Phase Margin versus Temperature

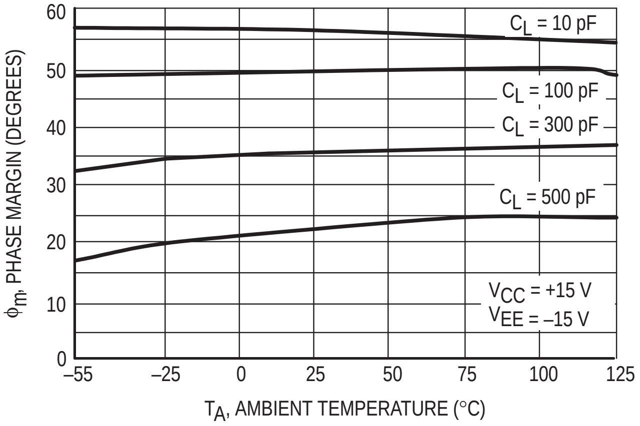


Figure 26. Phase Margin and Gain Margin versus Differential Source Resistance

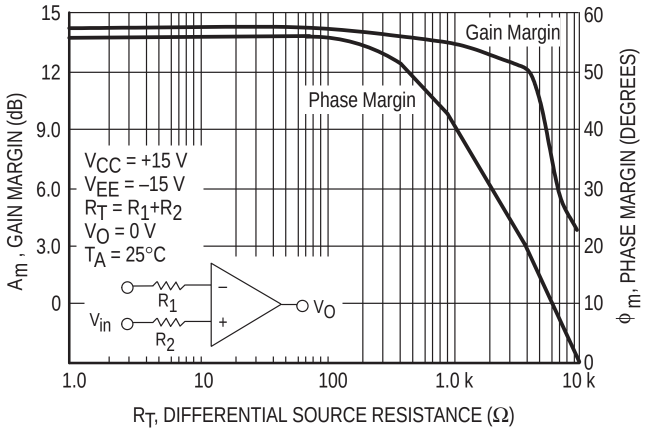


Figure 27. Channel Separation versus Frequency

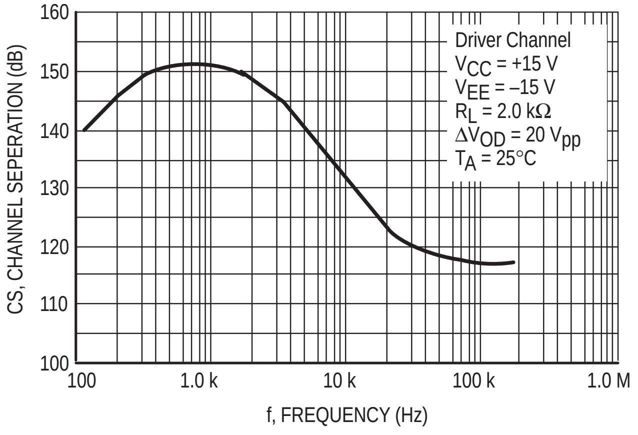


Figure 28. Total Harmonic Distortion versus Frequency

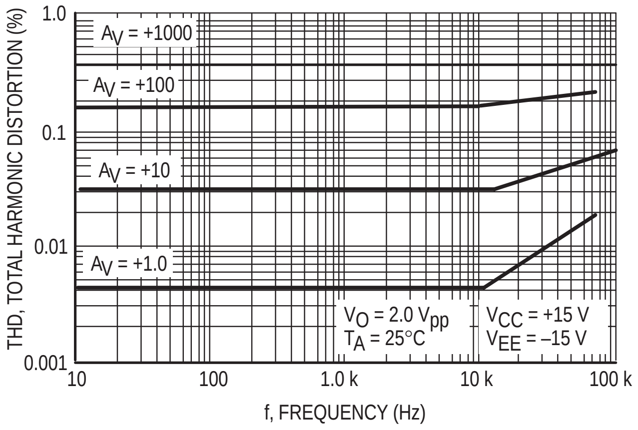


Figure 29. Output Impedance versus Frequency

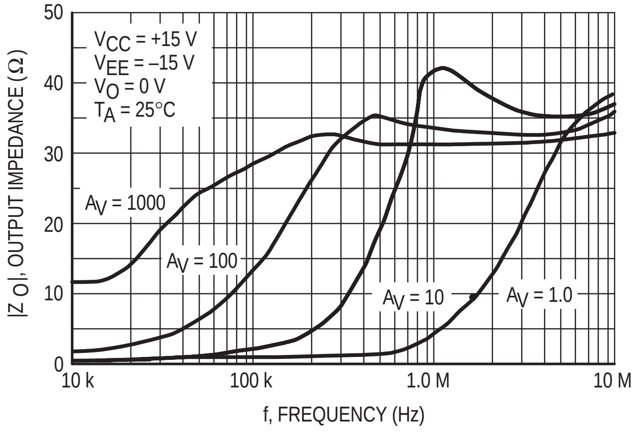


Figure 30. Input Referred Noise Voltage versus Frequency

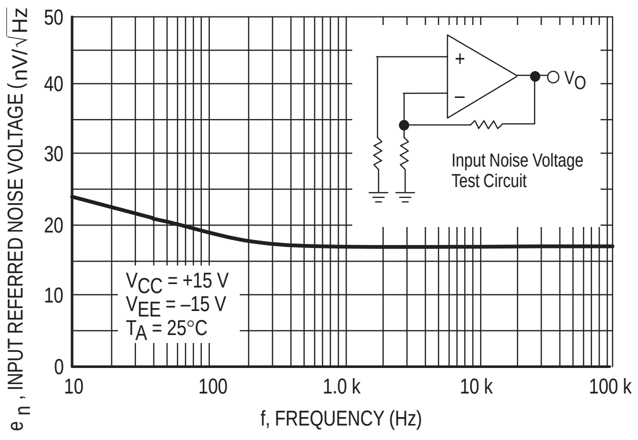


Figure 31. Input Referred Noise Current versus Frequency

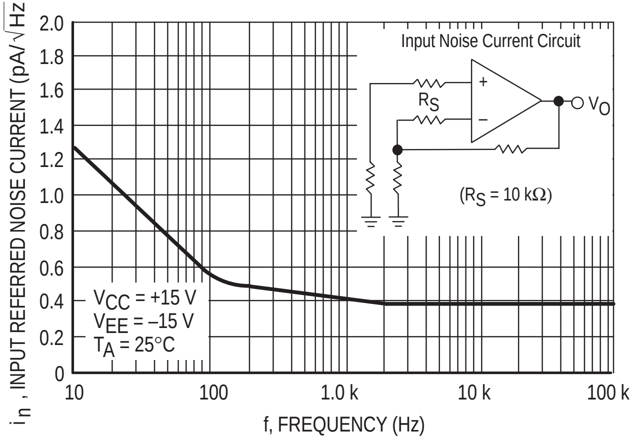


Figure 32. Percent Overshoot versus Load Capacitance

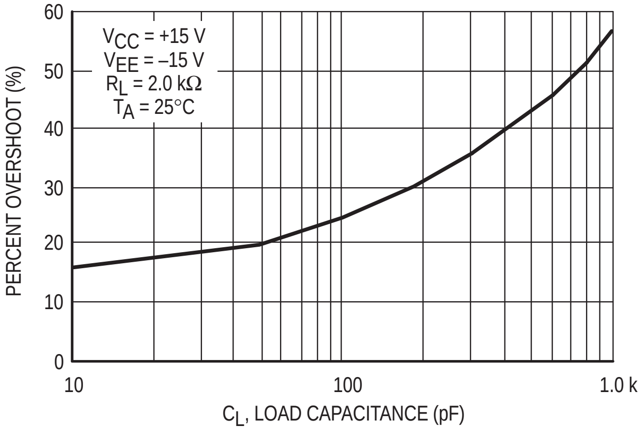


Figure 33. Noninverting Amplifier Slew Rate for the MC33274

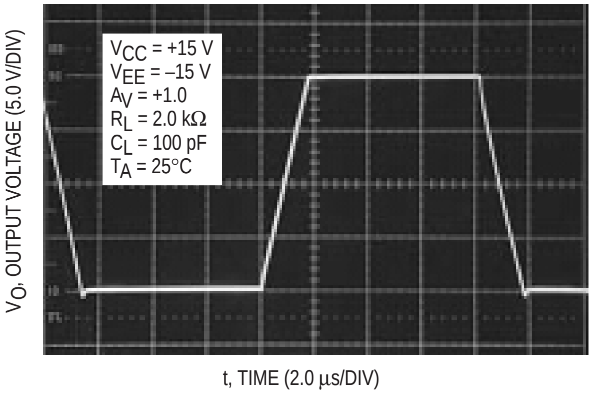


Figure 34. Noninverting Amplifier Overshoot for the MC33274

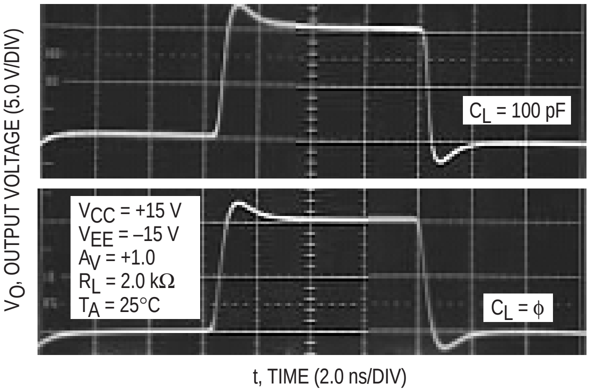


Figure 35. Small Signal Transient Response for MC33274

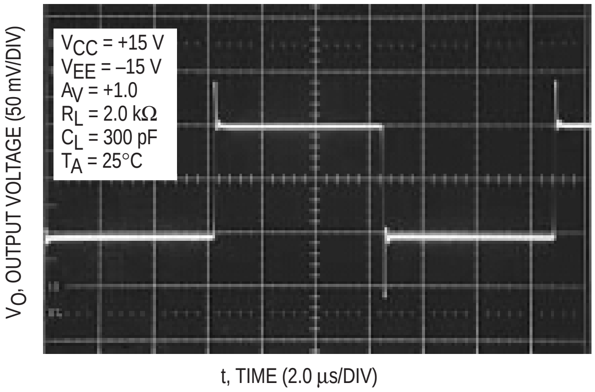
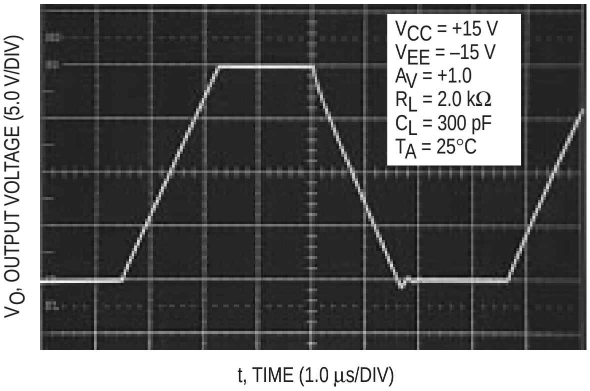


Figure 36. Large Signal Transient Response for MC33274



MOTOROLA

MC33282
MC33284

Low Input Offset, High Slew Rate, Wide Bandwidth, JFET Input Operational Amplifiers

The MC33282/284 series of high performance operational amplifiers are quality fabricated with innovative bipolar and JFET design concepts. This dual and quad amplifier series incorporates JFET inputs along with a patented Zip–R–Trim® element for input offset voltage reduction. These devices exhibit low input offset voltage, low input bias current, high gain bandwidth and high slew rate. Dual–doublet frequency compensation is incorporated to produce high quality phase/gain performance. In addition, the MC33282/284 series exhibit low input noise characteristics for JFET input amplifiers. Its all NPN output stage exhibits no deadband crossover distortion and a large output voltage swing. They also provide a low open loop high frequency output impedance with symmetrical source and sink AC frequency performance.

The MC33282/284 series are specified over –40° to +85°C and are available in plastic DIP and SOIC surface mount packages.

- Low Input Offset Voltage: Trimmed to 200 μV
- Low Input Bias Current: 30 pA
- Low Input Offset Current: 6.0 pA
- High Input Resistance: 10^{12} Ω
- Low Noise: 18 nV $\sqrt{\text{Hz}}$ @ 1.0 kHz
- High Gain Bandwidth Products: 35 MHz @ 100 kHz
- High Slew Rate: 15 V/μs
- Power Bandwidth: 175 kHz
- Unity Gain Stable: w/Capacitance Loads to 300 pF
- Large Output Voltage Swing: +14.1 V/–14.6 V
- Low Total Harmonic Distortion: 0.003%
- Power Supply Drain Current: 2.15 mA per Amplifier
- Dual Supply Operation: ±2.5 V to ±18 V (Max)

ORDERING INFORMATION

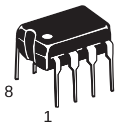
Op Amp Function	Device	Operating Temperature Range	Package
Dual	MC33282D	T_A = –40° to +85°C	SOP–8
	MC33282P		Plastic DIP
Quad	MC33284D		SO–14
	MC33284P		Plastic DIP

Zip–R–Trim is a registered trademark of Motorola Inc.

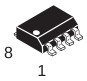
HIGH PERFORMANCE OPERATIONAL AMPLIFIERS

SEMICONDUCTOR
TECHNICAL DATA

DUAL

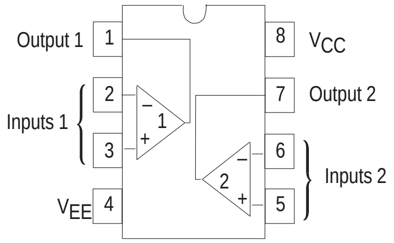


P SUFFIX
PLASTIC PACKAGE
CASE 626



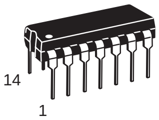
D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

PIN CONNECTIONS

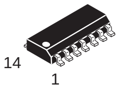


(Top View)

QUAD

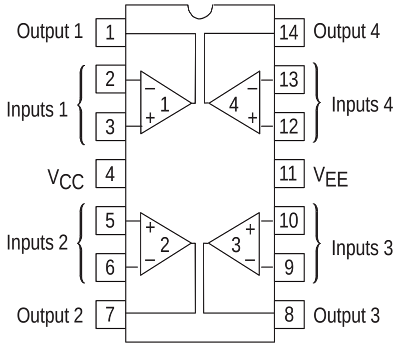


P SUFFIX
PLASTIC PACKAGE
CASE 646



D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO–14)

PIN CONNECTIONS



(Top View)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage (V_{CC} to V_{EE})	V_S	+36	V
Input Differential Voltage Range	V_{IDR}	(Note 1)	V
Input Voltage Range	V_{IR}	(Note 1)	V
Output Short Circuit Duration (Note 2)	t_{SC}	Indefinite	sec
Maximum Junction Temperature	T_J	+150	°C
Storage Temperature	T_{stg}	– 60 to +150	°C
Maximum Power Dissipation	P_D	(Note 2)	mW

NOTES: 1. Either or both input voltages should not exceed V_{CC} or V_{EE}.
2. Power dissipation must be considered to ensure maximum junction temperature (T_J) is not exceeded (see Figure 2).

DC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = –15 V, T_A = 25°C, unless otherwise noted.)

Characteristics	Symbol	Figure	Min	Typ	Max	Unit
Input Offset Voltage (R_S = 10 Ω, V_{CM} = 0 V, V_O = 0 V)	$\lvert V_{IO}\rvert$	3				mV
T_A = +25°C			—	0.2	2.0	
T_A = –40° to +85°C			—	—	4.0	
Average Temperature Coefficient of Input Offset Voltage	$\lvert\Delta V_{IO}\rvert/\Delta T$	3				µV/°C
R_S = 10 Ω, V_{CM} = 0 V, V_O = 0 V, T_A = T_{low} to T_{high}			—	15	—	
Input Bias Current (V_{CM} = 0 V, V_O = 0 V)	I_{IB}	4, 5				
T_A = +25°C			–200	30	200	pA
T_A = –40° to +85°C			–2.0	—	2.0	nA
Input Offset Current (V_{CM} = 0 V, V_O = 0 V)	I_{IO}					
T_A = +25°C			–100	6.0	100	pA
T_A = –40° to +85°C			–1.0	—	1.0	nA
Common Mode Input Voltage Range	V_{ICR}	6	–11	–12	—	V
(ΔV_{IO} = 5.0 mV, V_O = 0 V)			—	+14	+11	
Large Signal Voltage Gain (V_O = ±10 V, R_L = 2.0 kΩ)	A_{VOL}	7				V/mV
T_A = +25°C			50	200	—	
T_A = –40° to +85°C			25	—	—	
Output Voltage Swing (V_{ID} = ±1.0 V)		8, 9, 10				V
R_L = 2.0 kΩ	V_O+		13.2	+13.7	—	
R_L = 2.0 kΩ	V_O–		—	–13.9	–13.2	
R_L = 10 kΩ	V_O+		13.7	+14.1	—	
R_L = 10 kΩ	V_O–		—	–14.6	–14.3	
Common Mode Rejection (V_{in} = ±11 V)	CMR	11	70	90	—	dB
Power Supply Rejection	PSR	12				dB
V_{CC}/V_{EE} = +15 V/–15 V, +5.0 V/–15 V, +15 V/–5.0 V			75	100	—	
Output Short Circuit Current (V_{ID} = 1.0 V, output to ground)	I_{SC}	13, 14				mA
Source			15	+21	—	
Sink			—	–27	–15	
Power Supply Current (V_O = 0 V, per amplifier)	I_D	15				mA
T_A = +25°C			—	2.15	2.75	
T_A = –40° to +85°C			—	—	3.0	

AC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = –15 V, T_A = 25°C, unless otherwise noted.)

Characteristics	Symbol	Figure	Min	Typ	Unit
Slew Rate (V_{in} = –10 V to +10 V, R_L = 2.0 kΩ, C_L = 100 pF, A_V = +1.0)	SR	16, 28, 29	8.0	15	V/μs
Gain Bandwidth Product (f = 100 kHz)	GBW	17	20	35	MHz
AC Voltage Gain (R_L = 2.0 kΩ, V_O = 0 V, f = 20 kHz)	A_{VO}	18, 21	—	1750	V/V
Unity Gain Frequency (Open Loop)	f_U		—	5.5	MHz
Gain Margin (R_L = 2.0 kΩ, C_L = 0 pF)	A_m	19, 20	—	15	dB
Phase Margin (R_L = 2.0 kΩ, C_L = 0 pF)	ϕ_m	19, 20	—	40	Degrees
Channel Separation (f = 20 Hz to 20 kHz)	CS	22	—	–120	dB
Power Bandwidth (V_O = 20 V_{pp}, R_L = 2.0 kΩ, THD ≤ 1.0%)	BW_P		—	175	kHz
Distortion (R_L = 2.0 kΩ, f = 20 Hz to 20 kHz, V_O = 3.0 V_{rms}, A_V = +1.0)	THD	23	—	0.003	%
Open Loop Output Impedance (V_O = 0 V, f = 9.0 MHz)	$\lvert Z_O \rvert$	24	—	37	Ω
Differential Input Resistance (V_{CM} = 0 V)	R_{in}		—	10^{12}	Ω
Differential Input Capacitance (V_{CM} = 0 V)	C_{in}		—	5.0	pF
Equivalent Input Noise Voltage (R_S = 100 Ω, f = 1.0 kHz)	e_n	25	—	18	$\mathrm{nV}/\sqrt{\mathrm{Hz}}$
Equivalent Input Noise Current (f = 1.0 kHz)	i_n		—	0.01	$\mathrm{pA}/\sqrt{\mathrm{Hz}}$

Figure 1. Equivalent Circuit Schematic
(Each Amplifier)

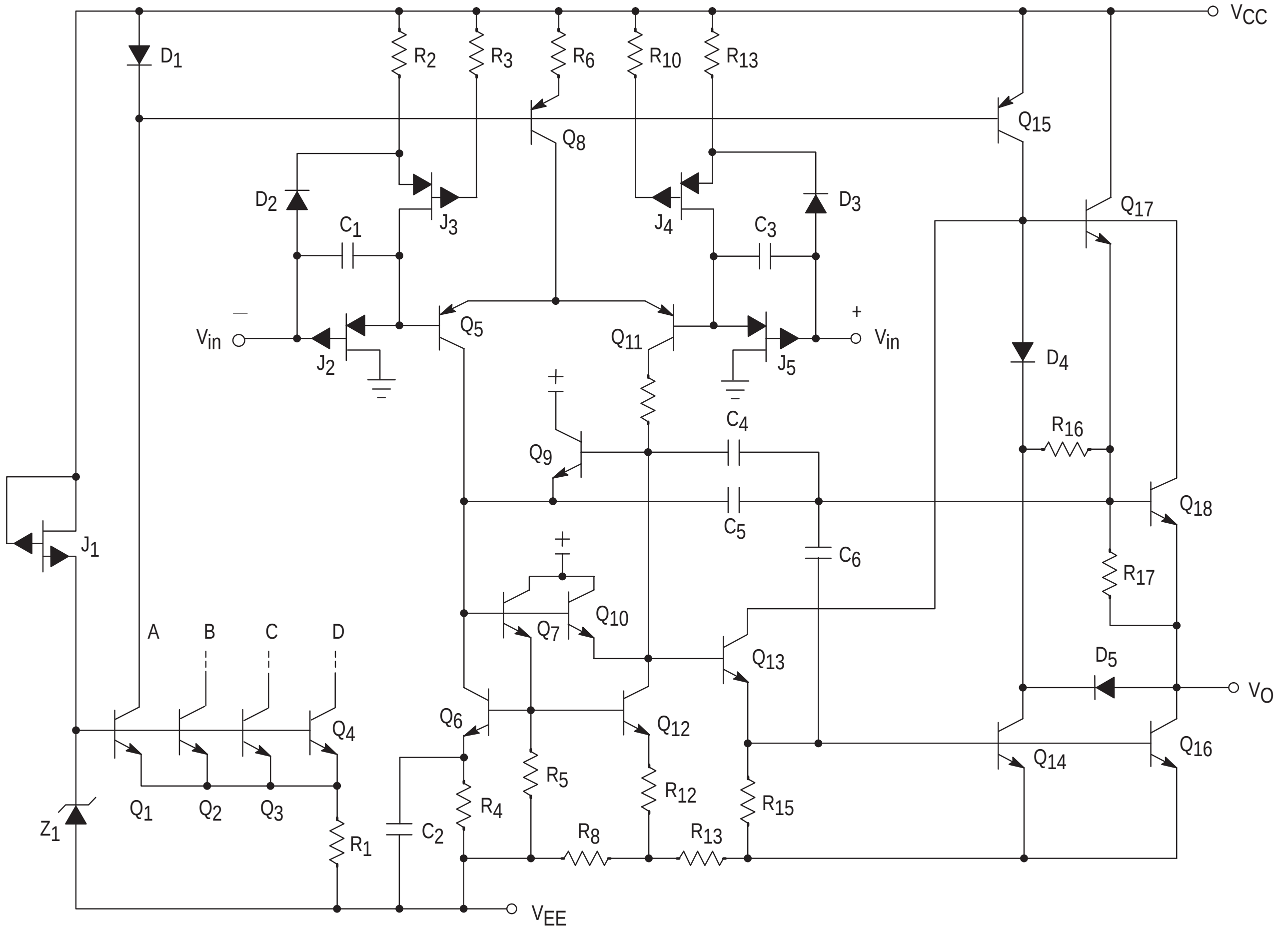


Figure 2. Maximum Power Dissipation versus Temperature

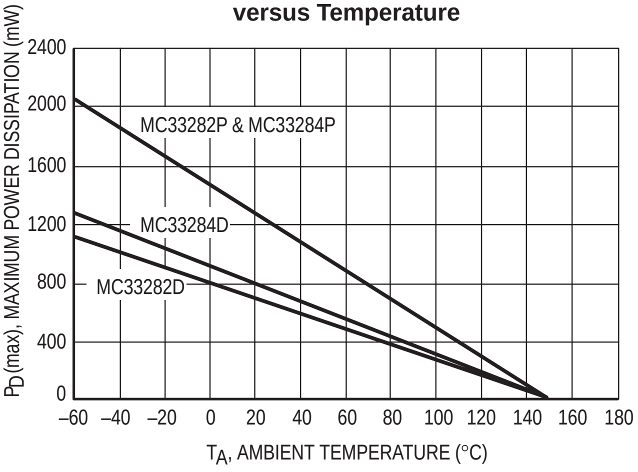


Figure 3. Input Offset Voltage versus Temperature for Typical Units

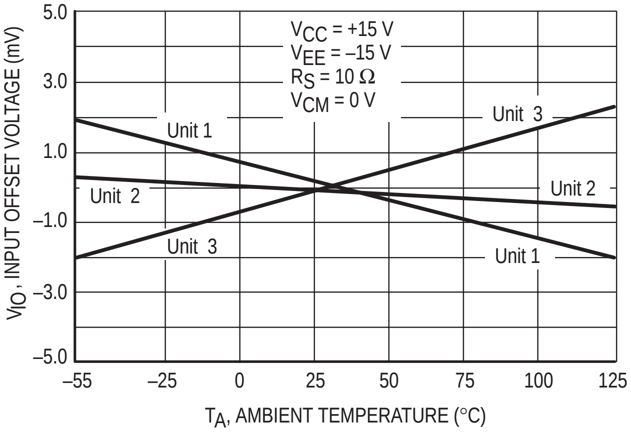


Figure 4. Input Bias Current versus Temperature

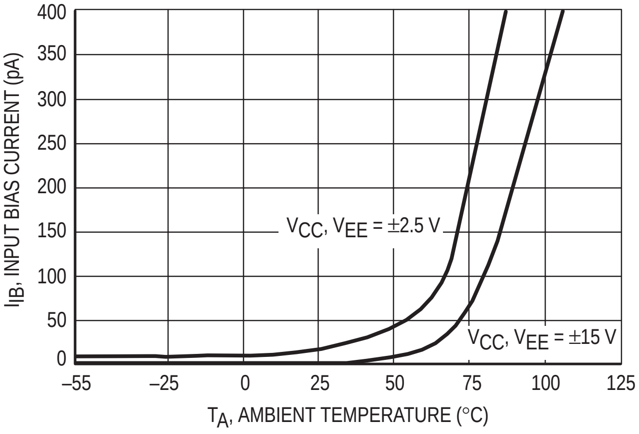


Figure 5. Input Bias Current versus Common Mode Voltage

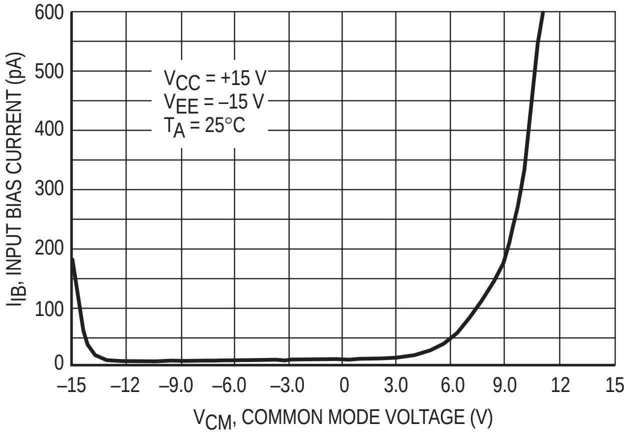


Figure 6. Input Common Mode Voltage Range versus Temperature

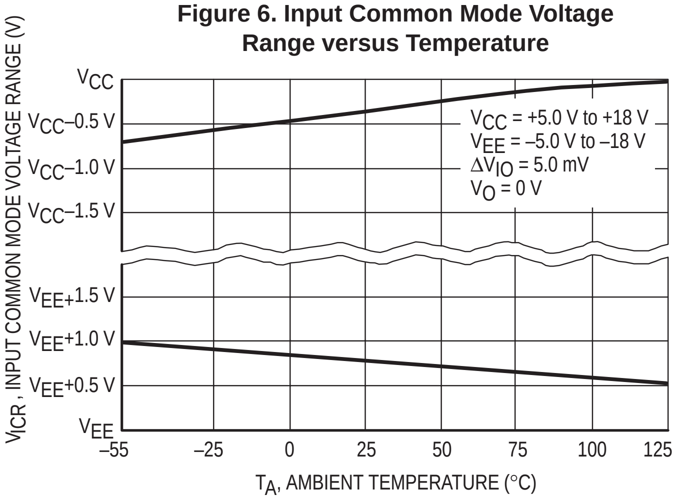


Figure 7. Open Loop Voltage Gain versus Temperature

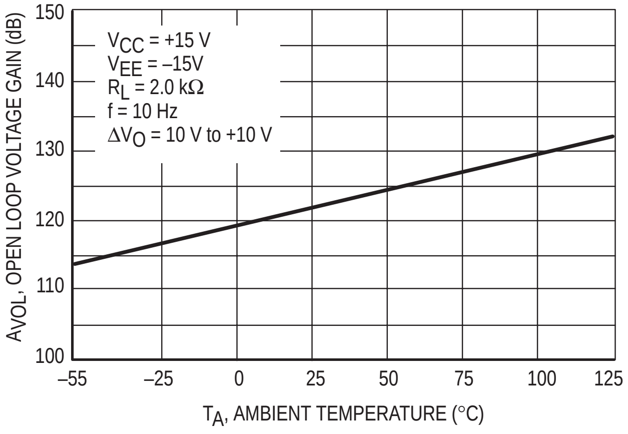


Figure 8. Output Voltage Swing versus Supply Voltage

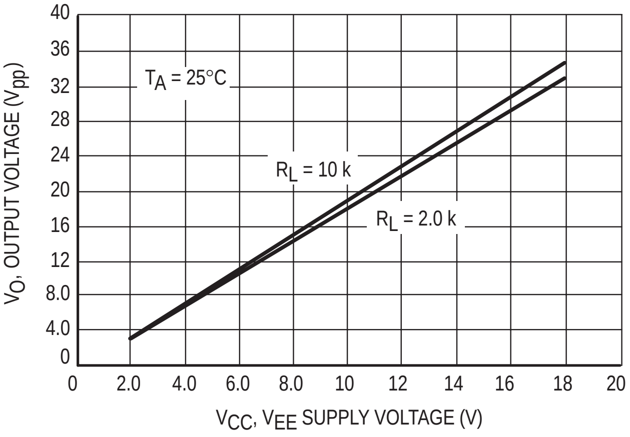


Figure 9. Output Voltage versus Frequency

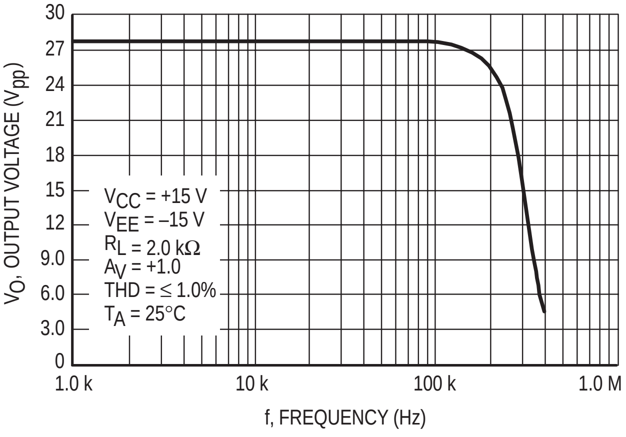


Figure 10. Output Saturation Voltage versus Load Current

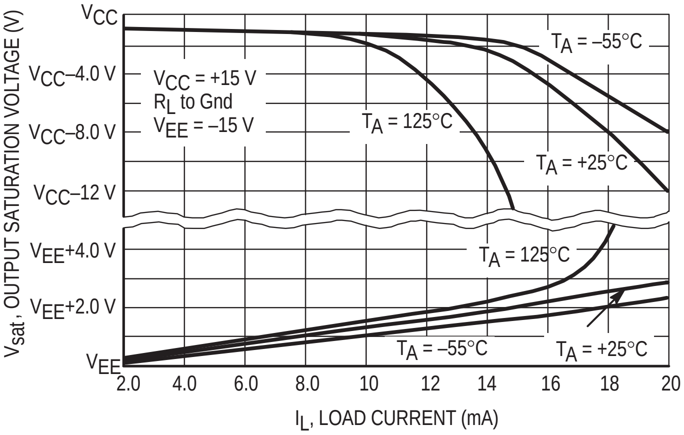


Figure 11. Common Mode Rejection versus Frequency

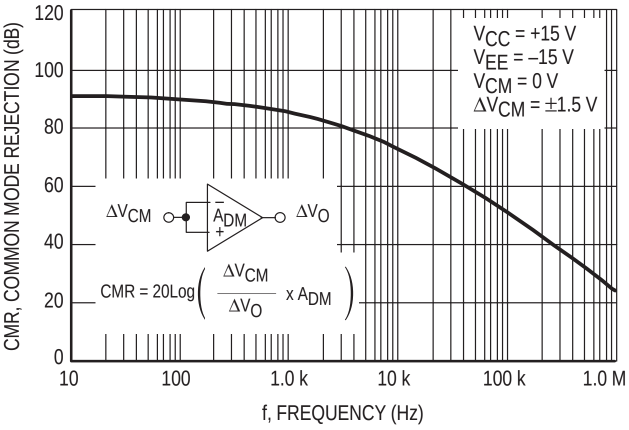


Figure 12. Positive Power Supply Rejection versus Frequency

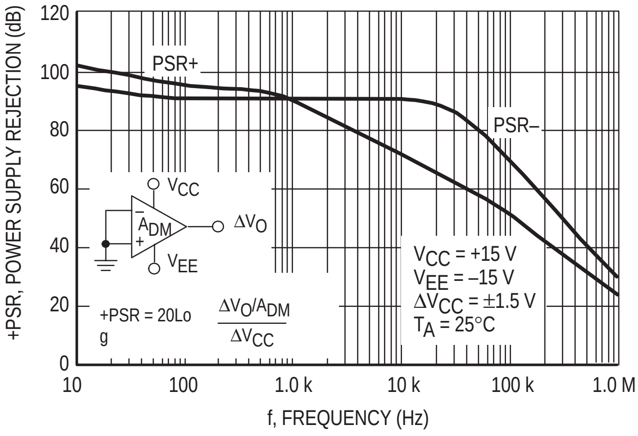


Figure 13. Output Short Circuit Source Current versus Temperature

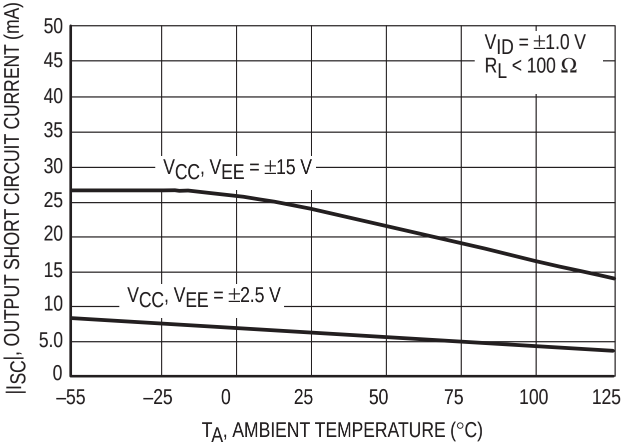


Figure 14. Output Short Circuit Sink Current versus Temperature

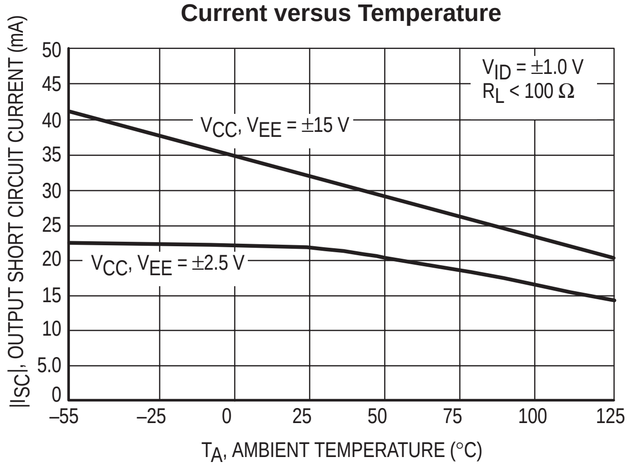


Figure 15. Power Supply Current versus Supply Voltage

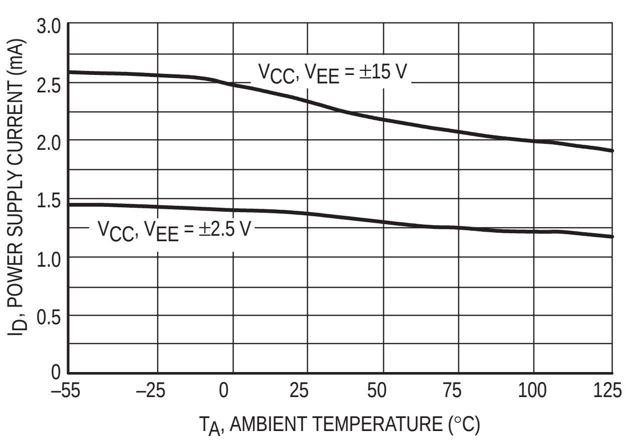


Figure 16. Slew Rate versus Temperature

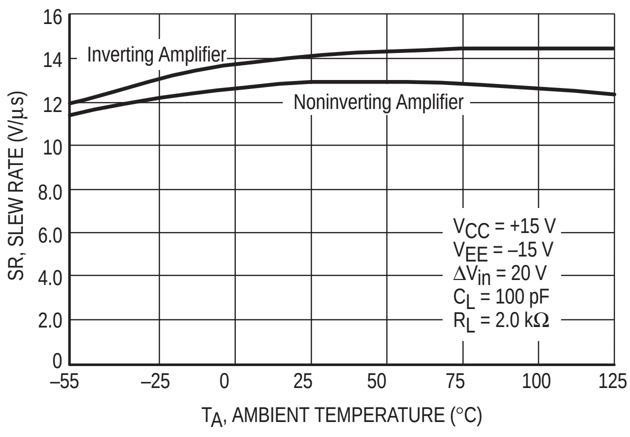


Figure 17. Gain Bandwidth Product versus Temperature

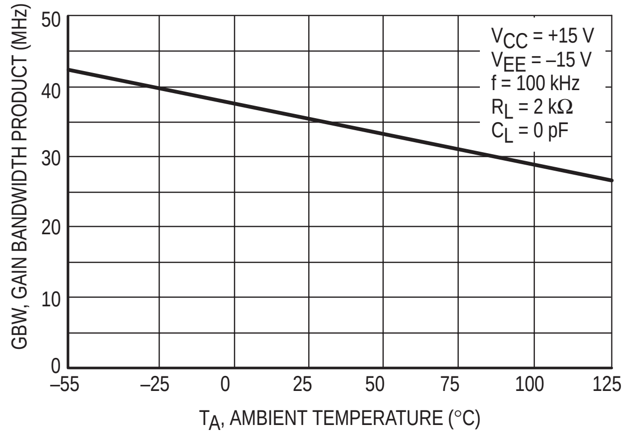


Figure 18. Gain and Phase versus Frequency

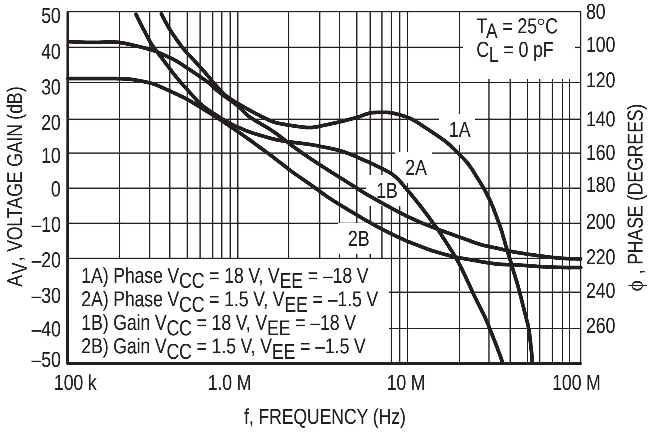
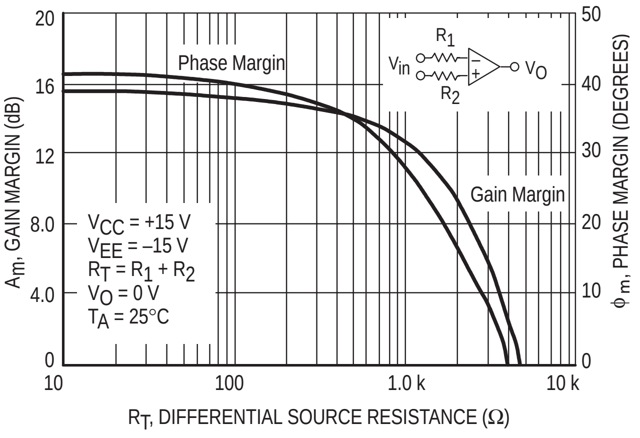


Figure 19. Phase Margin and Gain Margin versus Differential Source Resistance



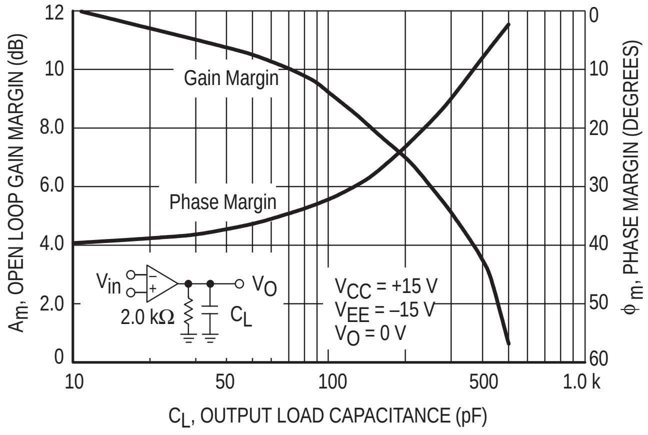


Figure 20. Open Loop Gain and Phase Margin versus Output Load Capacitance

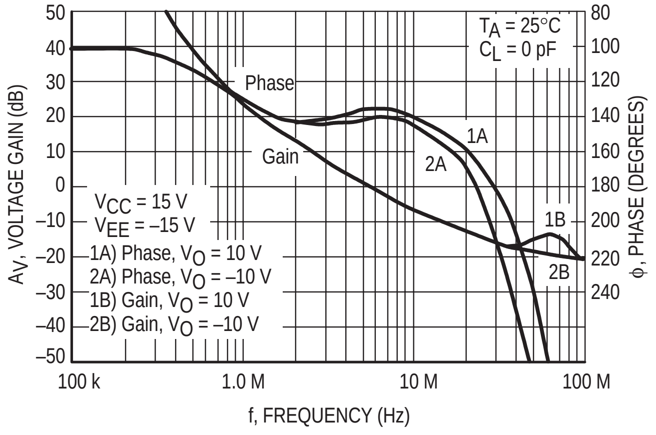


Figure 21. Gain and Phase versus Frequency

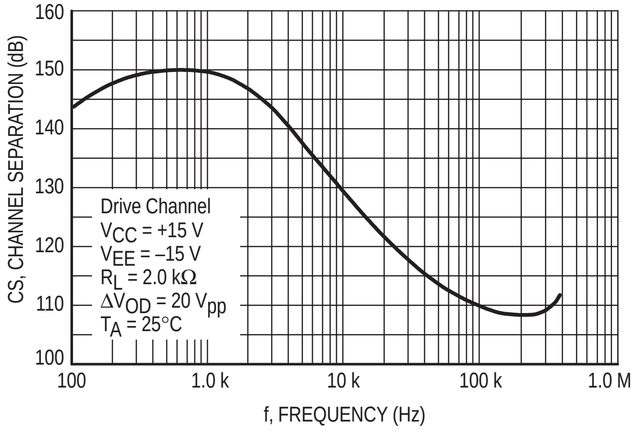


Figure 22. Channel Separation versus Frequency

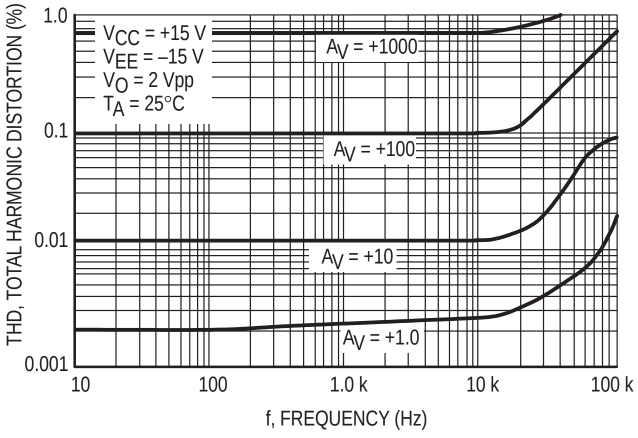


Figure 23. Total Harmonic Distortion versus Frequency

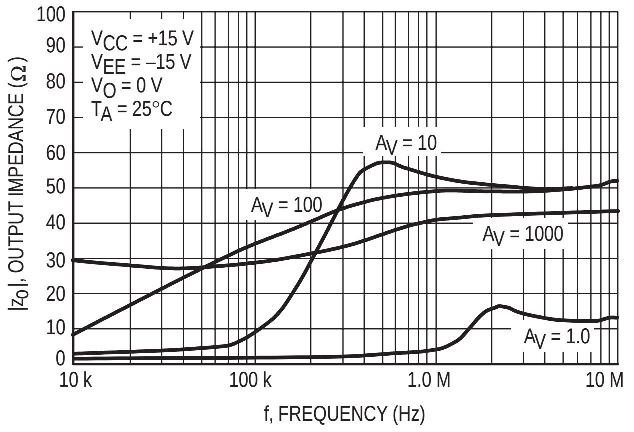


Figure 24. Output Impedance versus Frequency

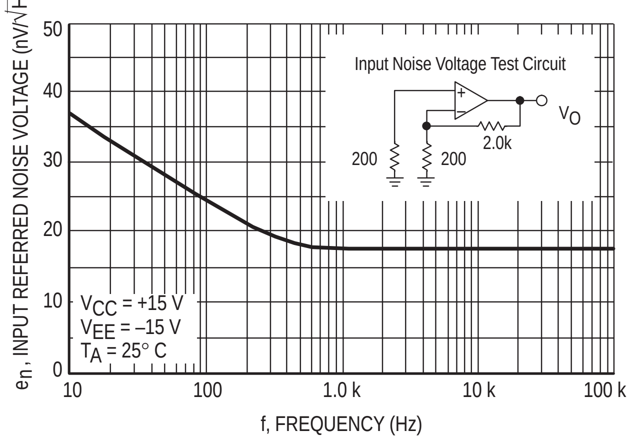


Figure 25. Input Referred Noise Voltage versus Frequency

Figure 26. Percent Overshoot versus Load Capacitance

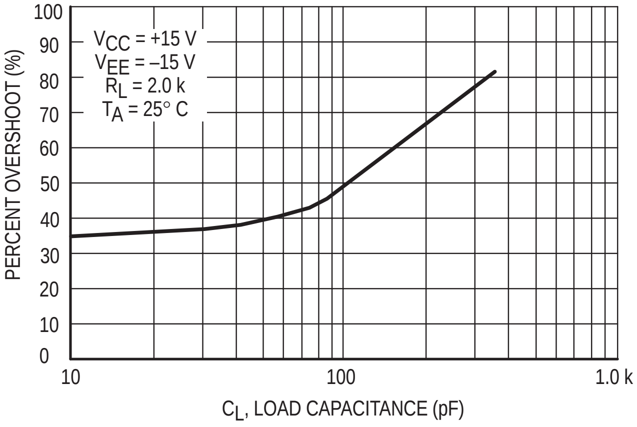


Figure 27. Noninverting Amplifier Overshoot

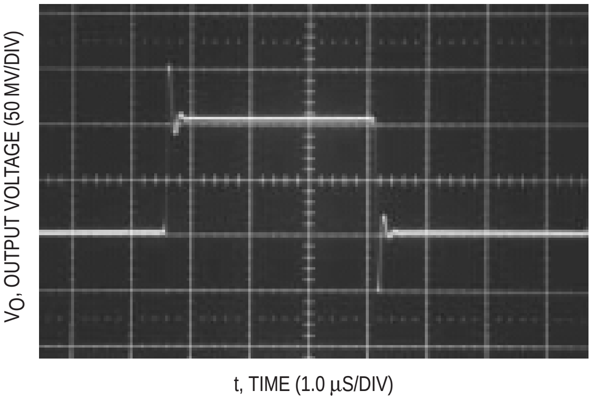


Figure 28. Noninverting Amplifier Slew Rate

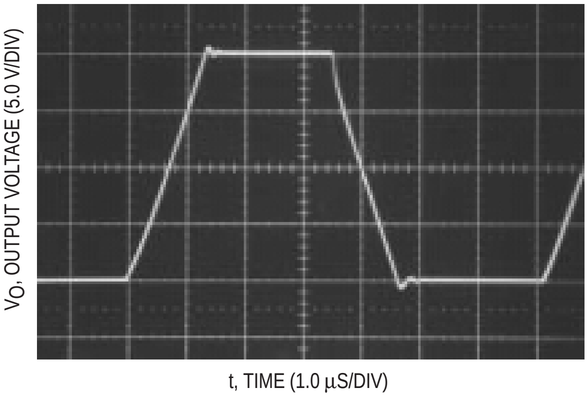
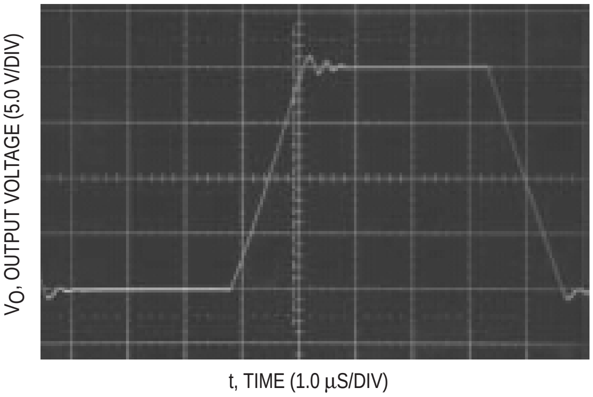


Figure 29. Inverting Amplifier Slew Rate



MOTOROLA

MC33304

Low Voltage Rail-To-Rail Sleep-Mode™ Operational Amplifier

The MC33304 is a monolithic bipolar operational amplifier. This low voltage rail–to–rail amplifier has both a rail–to–rail input and output stage, with high output current capability. This amplifier also employs Sleep–Mode technology. In sleepmode, the micropower amplifier is active and waiting for an input signal. When a signal is applied, causing the amplifier to source or sink ≥200 µA (typically) to the load, it will automatically switch to the awakemode (supplying up to 70 mA to the load). When the output current drops below 90 µA, the amplifier automatically returns to the sleepmode.

Excellent performance can be achieved as an audio amplifier. This is due to the amplifier's low noise and low distortion. A delay circuit is incorporated to prevent crossover distortion.

- Ideal for Battery Applications
- Full Output Signal (No Distortion) for Battery Applications Down to ±0.9 VDC.
- Single Supply Operation (+1.8 to +12 V)
- Rail–To–Rail Performance on Both the Input and Output
- Output Voltages Swings Typically within 100 mV of Both Rails (R_L = 1.0 mΩ)
- Two States: "Sleepmode" (Micropower, I_D = 110 µA/Amp) and "Awakemode" (High Performance, I_D = 1200 µA/Amp)
- Automatic Return to Sleepmode when Output Current Drops Below Threshold, Allowing a Fully Functional Micropower Amplifier
- Independent Sleepmode Function for Each Amplifier
- No Phase Reversal on the Output for Overdriven Input Signals
- High Output Current (70 mA typically)
- 600 Ω Drive Capability
- Standard Pinouts; No Additional Pins or Components Required
- Drop–In Replacement for Many Other Quad Operational Amplifiers
- Similar to MC33201, MC33202 and MC33204 Family
- The MC33304 Amplifier is Offered in the Plastic DIP or SOIC Package (P and D Suffixes)

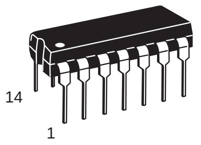
TYPICAL DC ELECTRICAL CHARACTERISTICS (T_A = 25°C)

Characteristic	V_{CC} = 2.0 V	V_{CC} = 3.3 V	V_{CC} = 5.0 V	Unit
Input Offset Voltage $V_{IO(max)}$ MC33304	±10	±10	±10	mV
Output Voltage Swing				
V_{OH} (R_L = 600 Ω)	1.85	3.10	4.75	V_{min}
V_{OL} (R_L = 600 Ω)	0.15	0.15	0.15	V_{max}
Power Supply Current per Amplifier (I_D)				
Awakemode	1.625	1.625	1.625	mA
Sleepmode	140	140	140	µA

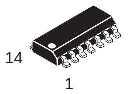
Specifications are for reference only and not necessarily guaranteed. V_{EE} = Gnd.

RAIL–TO–RAIL SLEEP–MODE OPERATIONAL AMPLIFIER

SEMICONDUCTOR TECHNICAL DATA

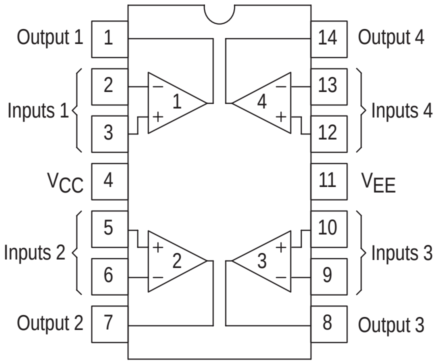


P SUFFIX
PLASTIC PACKAGE
CASE 646



D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO–14)

PIN CONNECTIONS



(Quad, Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC33304D	T_A = – 40° to +105°C	SO–14
MC33304P		Plastic DIP

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage (V_{CC} to V_{EE})	V_S	+16	V
ESD Protection Voltage at Any Pin Human Body Model	V_{ESD}	 2000	V
Voltage at Any Device Pin (Note 2)	V_{DP}	$V_S \pm 0.5$	V
Input Differential Voltage Range	V_{IDR}	(Notes 1 & 2)	V
Output Short Circuit Duration	t_s	Indefinite (Note 3)	sec
Maximum Junction Temperature	T_J	+150	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Maximum Power Dissipation	P_D	(Note 5)	mW

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_S				V
Single Supply		1.8	–	12	
Split Supplies		±0.9	–	±6.0	
Input Voltage Range, Sleepmode and Awakemode	V_{ICR}	V_{EE}	–	V_{CC}	V
Ambient Operating Temperature Range	T_A	–40	–	+105	°C

DC ELECTRICAL CHARACTERISTICS (V_{CC} = +5.0 V, V_{EE} = Gnd, T_A = 25°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Offset Voltage (V_{CM} = 0 V, V_O = 0 V) (Note 4) Sleepmode and Awakemode	V_{IO}				mV
T_A = 25°C		–10	0.7	+10	
T_A = –40° to +105°C		–13	–	+13	
Average Temperature Coefficient of Input Offset Voltage (R_S = 50 Ω, V_{CM} = 0 V, V_O = 0 V)	$\Delta V_{IO}/\Delta T$				µV/°C
T_A = –40° to +105°C, Sleepmode and Awakemode		–	2.0	–	
Input Bias Current (V_{CM} = 0 V, V_O = 0 V) (Note 4) Awakemode	$\lvert I_{IB}\rvert$				nA
T_A = 25°C		–	90	+200	
T_A = –40° to +105°C		–	–	+500	
Input Offset Current (V_{CM} = 0 V, V_O = 0 V) (Note 4) Awakemode	$\lvert I_{IO}\rvert$				nA
T_A = 25°C		–	3.1	+50	
T_A = –40° to +105°C		–	–	+100	
Large Signal Voltage Gain (V_{CC} = +5.0 V, V_{EE} = –5.0 V) Awakemode, R_L = 600 Ω	A_{VOL}				dB
T_A = 25°C		90	116	–	
T_A = –40° to +105°C		85	–	–	
Power Supply Rejection Ratio, Awakemode	PSRR	65	90	–	dB
Output Short Circuit Current (Awakemode) (V_{ID} = ±0.2 V)	I_{SC}				mA
Source		–200	–89	–50	
Sink		+50	+89	+200	
Output Transition Current, Source/Sink					µA
Sleepmode to Awakemode, V_{CC} = +1.0 V, V_{EE} = –1.0 V	$\lvert I_{TH1}\rvert$	–	–	200	
Awakemode to Sleepmode, V_{CC} = +5.0 V, V_{EE} –5.0 V	$\lvert I_{TH2}\rvert$	90	–	–	

DC ELECTRICAL CHARACTERISTICS (continued) (V_{CC} = +5.0 V, V_{EE} = Gnd, T_A = 25°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage Swing (V_{ID} = ±0.2 V)					V
Sleepmode					
V_{CC} = +5.0 V, V_{EE} = 0 V, R_L = 1.0 MΩ	V_{OH}	4.90	4.97	–	
V_{CC} = 0 V, V_{EE} = –5.0 V, R_L = 1.0 MΩ	V_{OL}	–	–4.96	–4.90	
V_{CC} = +2.0 V, V_{EE} = 0 V, R_L = 1.0 MΩ	V_{OH}	1.90	1.98	–	
V_{CC} = 0 V, V_{EE} = –2.0 V, R_L = 1.0 MΩ	V_{OL}	–	–1.97	–1.90	
Awakemode					
V_{CC} = +5.0 V, V_{EE} = 0 V, R_L = 600 Ω	V_{OH}	4.75	4.86	–	
V_{CC} = 0 V, V_{EE} = –5.0 V, R_L = 600 Ω	V_{OL}	–	–4.85	–4.75	
V_{CC} = +2.0 V, V_{EE} = 0 V, R_L = 600 Ω	V_{OH}	1.85	1.91	–	
V_{CC} = 0 V, V_{EE} = –2.0 V, R_L = 600 Ω	V_{OL}	–	–1.90	–1.85	
V_{CC} = +2.5 V, V_{EE} = –2.5 V, R_L = 600 Ω	V_{OH}	–	2.41	–	
V_{CC} = +2.5 V, V_{EE} = –2.5 V, R_L = 600 Ω	V_{OL}	–	–2.40	–	
Common Mode Rejection Ratio	CMRR	60	90	–	dB
Power Supply Current (per Amplifier)	I_D				µA
Sleepmode					
V_{CC} = +2.0 V, V_{EE} = 0 V T_A = +25°C		–	85	–	
V_{CC} = +2.5 V, V_{EE} = –2.5 V T_A = +25°C		–	110	140	
T_A = –40° to +105°C		–	–	150	
V_{CC} = +12 V, V_{EE} = 0 V T_A = +25°C		–	125	–	
Awakemode					
V_{CC} = +2.5 V, V_{EE} = –2.5 V T_A = +25°C		–	1200	1625	
T_A = –40° to +105°C		–	–	1750	
Thermal Resistance	θ_{JA}				°C/W
SOIC		–	145	–	
Plastic DIP		–	75	–	

AC ELECTRICAL CHARACTERISTICS (V_{CC} = +6.0 V, V_{EE} = –6.0 V, R_L = 600 Ω, T_A = 25°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Slew Rate (V_{CC} = +2.5 V, V_{EE} = –2.5 V, A_V = +1.0) (Note 6)	SR				V/µs
Awakemode		0.5	0.89	–	
Gain Bandwidth Product (f = 100 kHz)	GBW				MHz
Awakemode		–	2.2	–	
Gain Margin (C_L = 0 pF)	A_m				dB
Awakemode		–	6.0	–	
Sleepmode (R_L = 1.0 kΩ)		–	9.0	–	
Phase Margin (R_L = 1.0 kΩ, V_O = 0 V, C_L = 0 pF)	ϕ_m				Deg
Awakemode		–	40	–	
Sleepmode		–	60	–	
Sleepmode to Awakemode Transition Time	t_{tr1}				µsec
R_L = 600 Ω		–	4.0	–	
R_L = 10 k		–	12	–	
Awakemode to Sleepmode Transition Time	t_{tr2}	–	1.5	–	sec
Channel Separation (f = 1.0 kHz)	CS				dB
Awakemode		–	100	–	

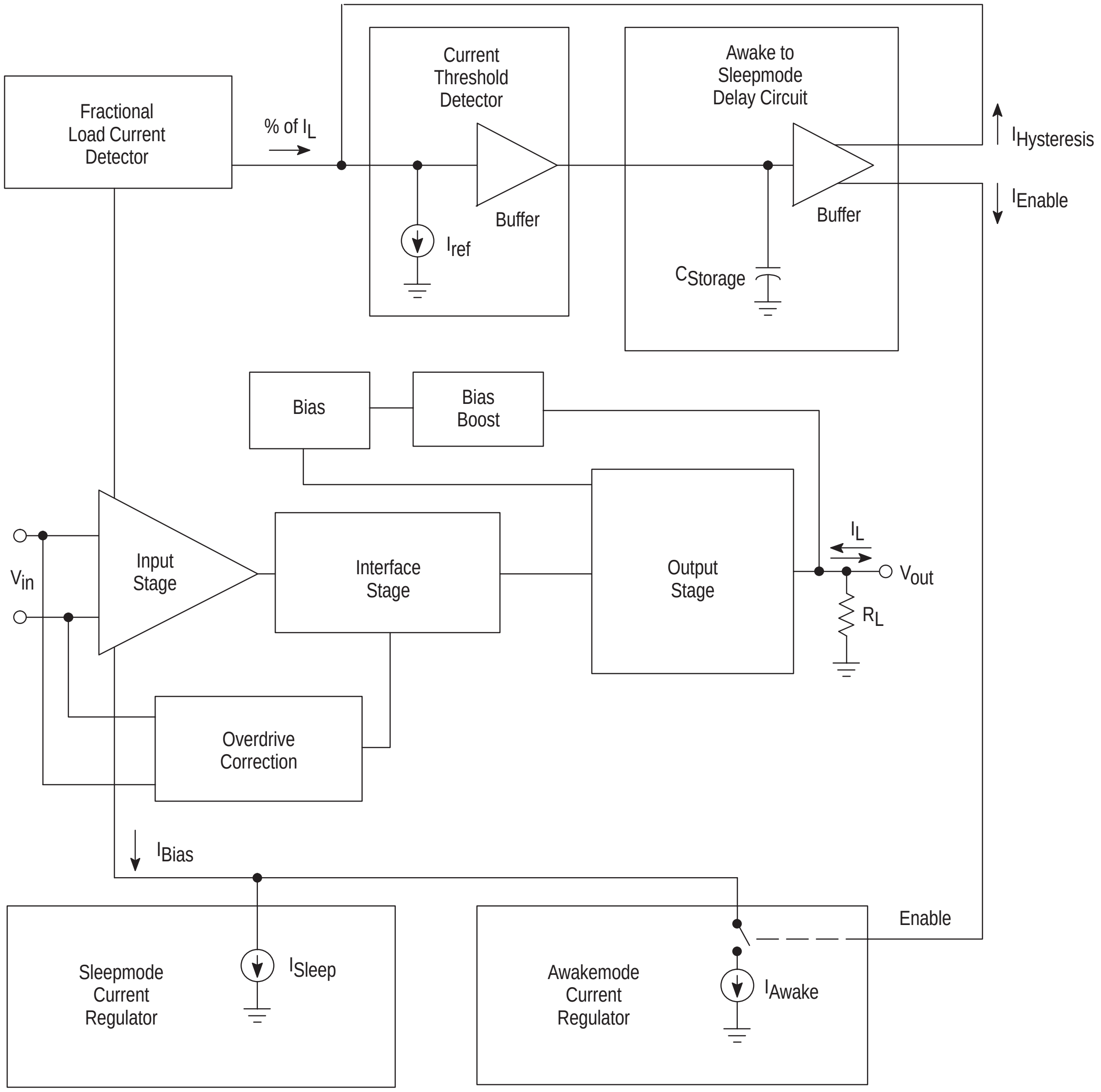
NOTES:
1. The differential input voltage of each amplifier is limited by two internal diodes. The diodes are connected across the inputs in parallel and opposite to each other. For more differential input voltage range, use current limiting resistors in series with the input pins.
2. The common–mode input voltage range of each amplifier is limited by diodes connected from the inputs to both power supply rails. Therefore, the voltage on either input must not exceed supply rail by more than ±500 mV.
3. Simultaneous short circuits of two or more amplifiers to the positive or negative rail can exceed the power dissipation ratings and cause eventual failure of the device.
4. Rail–to–rail performance is achieved at the input of the amplifier by using parallel NPN–PNP differential stages. When the inputs are near the negative rail ($V_{EE} < V_{CM} <$ 800 mV), the PNP stage is on. When the inputs are above 800 mV (i.e. 800 mV $< V_{CM} < V_{CC}$), the NPN stage is on. This switching of the input pairs will cause a reversal of input bias current. Slight changes in the input offset voltage will be noted between the NPN and PNP pairs. Cross–coupling techniques have been used to keep this change to a minimum.
5. Power dissipation must be considered to ensure maximum junction (T_J) is not exceeded. (See Figure 2)
6. When connected as a voltage follower and used in transient conditions, a current limiting resistor may be needed between the output and the inverting input. This is because of the back to back diodes clamped across the inputs. The value of this resistor should be between 1.0 kΩ and 10 kΩ. If the amplifier does not become slew rate limited and is processing low frequency waveforms, then no resistor would be necessary. (The output could be tied directly to the negative input.)

AC ELECTRICAL CHARACTERISTICS (continued) (V_{CC} = +6.0 V, V_{EE} = –6.0 V, R_L = 600 Ω, T_A = 25°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Power Bandwidth (V_O = 4.0 V_{pp}, R_L = 2.0 kΩ, THD ≤ 1.0%)	BW_p				kHz
Awakemode		–	28	–	
Distortion (V_O = 2.0 V_{pp}, A_V = +1.0)	THD				%
Awakemode (f = 10 kHz)		–	0.009	–	
Sleepmode (f = 1.0 kHz, R_L = Infinite)		–	0.007	–	
Open Loop Output Impedance (V_O = 0 V, f = 2.0 MHz, A_V = +10, I_Q = 10 μA)	$\lvert Z_O \rvert$				Ω
Awakemode		–	100	–	
Sleepmode		–	1000	–	
Differential Input Impedance (V_{CM} = 0 V)	R_{IN}				kΩ
Awakemode		–	200	–	
Sleepmode		–	1300	–	
Differential Input Capacitance (V_{CM} = 0 V)	C_{IN}				pF
Awakemode		–	8.0	–	
Sleepmode		–	0.4	–	
Equivalent Input Noise Voltage (R_S = 100 Ω, f = 1.0 kHz)	e_n				$nV/\sqrt{Hz}$
Awakemode		–	15	–	
Sleepmode		–	60	–	
Equivalent Input Noise Current (f = 1.0 kHz)	i_n				$pA/\sqrt{Hz}$
Awakemode		–	0.22	–	
Sleepmode		–	0.20	–	

NOTES:
1. The differential input voltage of each amplifier is limited by two internal diodes. The diodes are connected across the inputs in parallel and opposite to each other. For more differential input voltage range, use current limiting resistors in series with the input pins.
2. The common–mode input voltage range of each amplifier is limited by diodes connected from the inputs to both power supply rails. Therefore, the voltage on either input must not exceed supply rail by more than ±500 mV.
3. Simultaneous short circuits of two or more amplifiers to the positive or negative rail can exceed the power dissipation ratings and cause eventual failure of the device.
4. Rail–to–rail performance is achieved at the input of the amplifier by using parallel NPN–PNP differential stages. When the inputs are near the negative rail ($V_{EE} < V_{CM} <$ 800 mV), the PNP stage is on. When the inputs are above 800 mV (i.e. 800 mV $< V_{CM} < V_{CC}$), the NPN stage is on. This switching of the input pairs will cause a reversal of input bias current. Slight changes in the input offset voltage will be noted between the NPN and PNP pairs. Cross–coupling techniques have been used to keep this change to a minimum.
5. Power dissipation must be considered to ensure maximum junction (T_J) is not exceeded. (See Figure 2)
6. When connected as a voltage follower and used in transient conditions, a current limiting resistor may be needed between the output and the inverting input. This is because of the back to back diodes clamped across the inputs. The value of this resistor should be between 1.0 kΩ and 10 kΩ. If the amplifier does not become slew rate limited and is processing low frequency waveforms, then no resistor would be necessary. (The output could be tied directly to the negative input.)

Figure 1. Equivalent Circuit Block Diagram (Each Amplifier)



There are 515 active components for the entire quad device.

DEVICE DESCRIPTION

The MC33304 will begin to function at power supply voltages as low as $V_S = \pm 0.8$ V. The device has the ability to swing rail–to–rail on both the input and the output. Since the common mode input voltage range extends from V_{CC} to V_{EE}, it can be operated with either single or split voltage supplies. The MC33304 is guaranteed not to latch up or phase reverse over the entire common mode range. However, the output could go into phase reversal state if input voltage is set higher than $+V_{CC}$ or $-V_{EE}$.

When power is initially applied, the part may start to operate in the awakemode. This occurs because of bias currents being generated from the charging of the internal capacitors. When this occurs, the user will have to wait approximately 1.5 seconds before the device will switch back to the sleepmode.

The amplifier is designed to switch from sleepmode to awakemode whenever the output current exceeds a preset current threshold (I_{TH}) of approximately 200 μA. As a result, the output switching threshold voltage (V_{ST}) is controlled by the output loading resistance (R_L). Large valued load resistors require a large output voltage to switch, but reduce unwanted transitions to the awakemode.

Most of the transition time is consumed slewing in the sleepmode until V_{ST} is reached, therefore, small values of R_L allow rapid transition to the awakemode. The output switching threshold voltage (V_{ST}) is higher for the larger values of R_L, requiring the amplifier to slew longer in the slower sleepmode state before switching to the awakemode.

Although typically 200 μA, I_{TH} varies with supply voltage, temperature and the load resistance. Generally, any current loading on the ouput which causes a current greater than I_{TH} to flow will switch the amplifier into the awakemode. This includes transition currents like those generated by charging load capacitances. In fact, the maximum capacitance that can be driven while attempting to remain in the sleepmode is approximately 300 pF.

The awakemode to sleepmode transition time is controlled by an internal delay circuit, which is necessary to prevent the amplifier from going to sleep during every zero crossing of the output waveform. This delay circuit also eliminates the crossover distortion commonly found in micropower amplifiers.

The MC33304 rail–to–rail sleepmode operational amplifier is unique in its ability to swing rail–to–rail on both the input and output using a bipolar design. This offers a low noise and wide common mode input voltage range. Since the common mode input voltage range extends from V_{CC} to V_{EE}, it can be operated with either single or split voltage supplies.

Rail–to–rail performance is achieved at the input of the amplifiers by using parallel NPN–PNP differential input stages. When the inputs are within 800 mV of the negative rail, the PNP stage is on. When the inputs are more than 800 mV above V_{EE}, the NPN stage is on. This switching of input pairs will cause a reversal of input bias currents. Also, slight differences in offset voltage may be noted between the NPN and PNP pairs. Cross–coupling techniques have been used to keep this change to a minimum.

In addition to the rail–to–rail performance, the output stage is current boosted to provide enough output current to drive 600 Ω loads. Because of this high current capability, care should be taken not to exceed the 150°C maximum junction temperature specification.

Figure 2. Maximum Power Dissipation versus Temperature

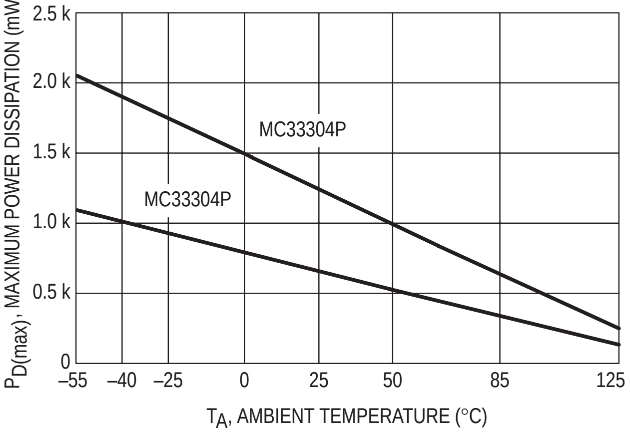


Figure 3. Input Bias Current versus Temperature

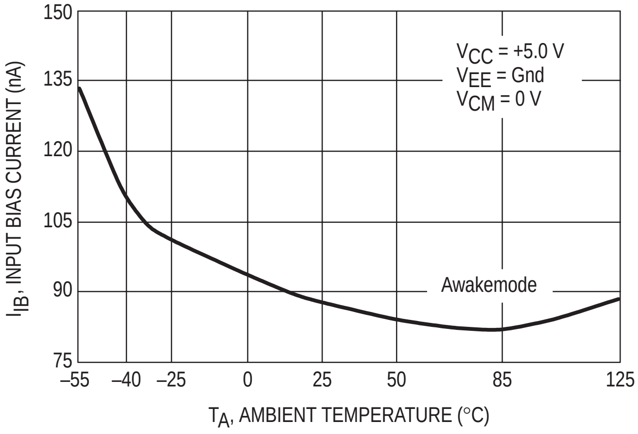


Figure 4. Input Bias Current versus Common Mode Input Voltage

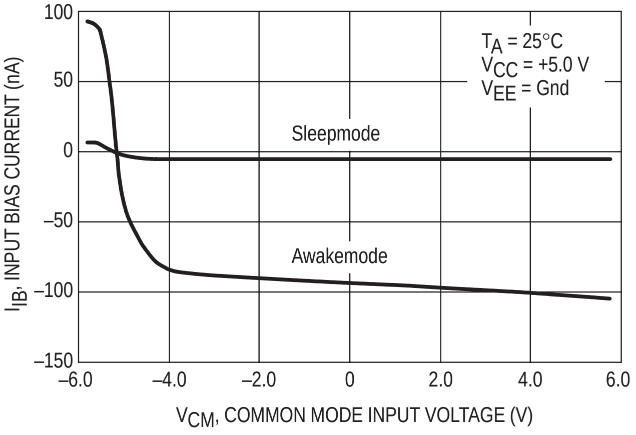


Figure 5. Open Loop Voltage Gain versus Temperature

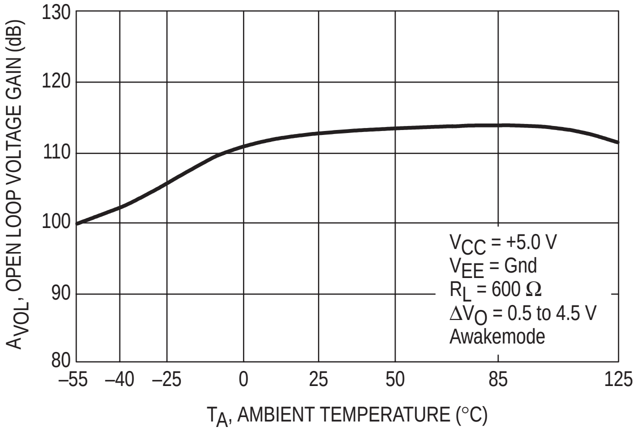


Figure 6. Output Voltage Swing versus Supply Voltage

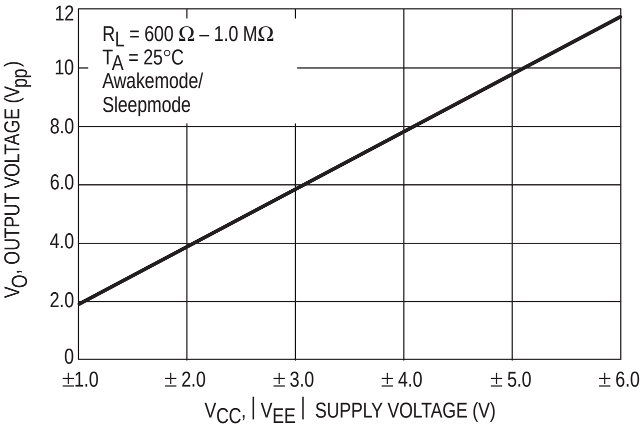


Figure 7. Output Voltage versus Frequency

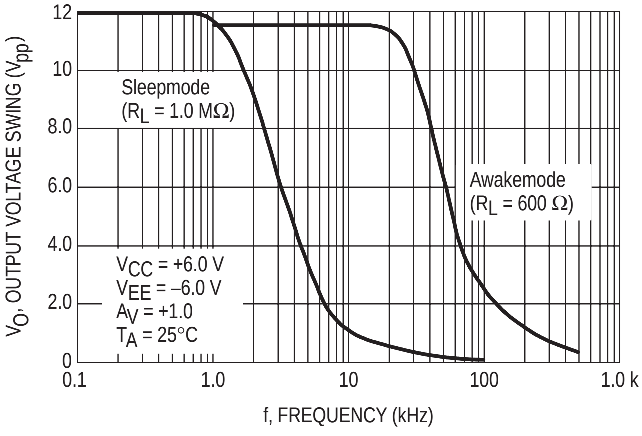


Figure 8. Maximum Peak–to–Peak Output Voltage Swing versus Load Resistance

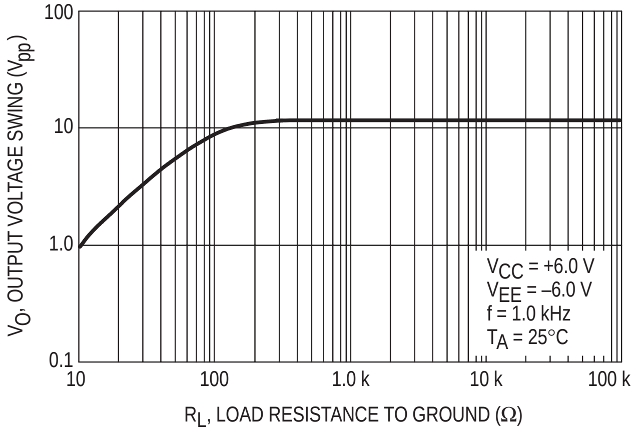


Figure 9. Common Mode Rejection versus Frequency

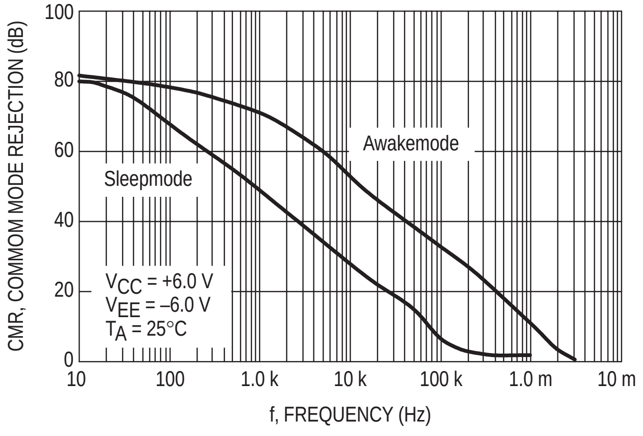


Figure 10. Power Supply Rejection versus Frequency

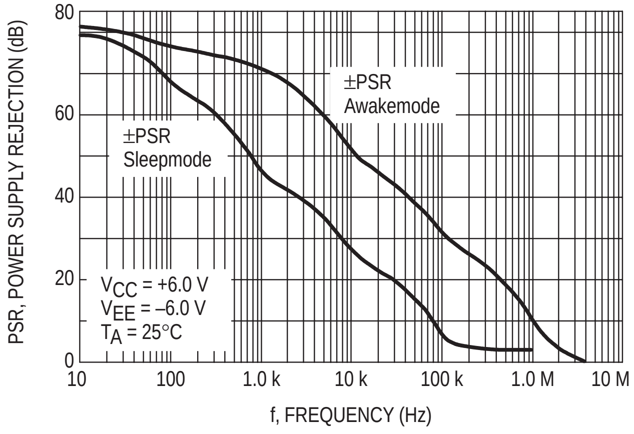


Figure 11. Awakemode to Sleepmode Current Threshold versus Supply Voltage

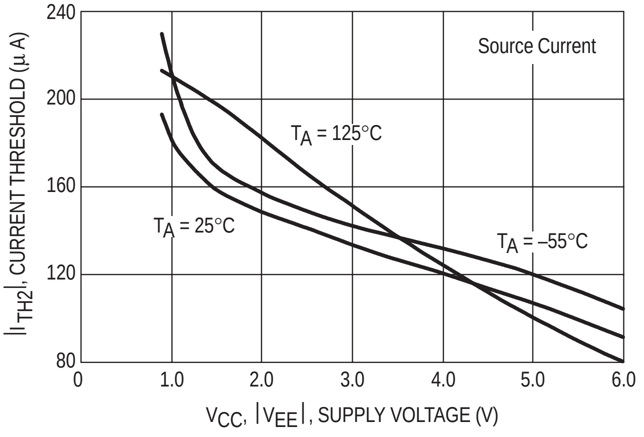


Figure 12. Sleepmode to Awakemode Current Threshold versus Supply Voltage

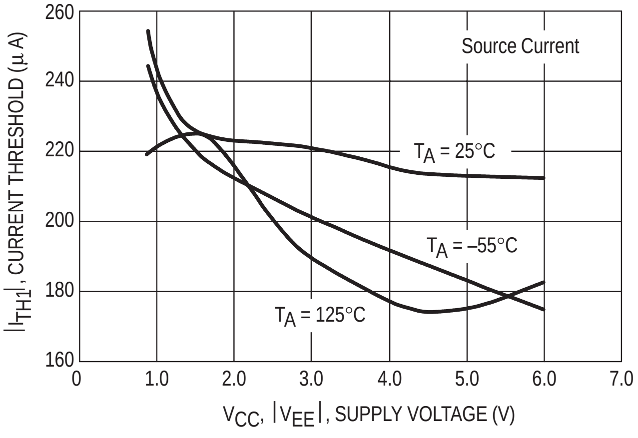


Figure 13. Output Short Circuit Current versus Output Voltage

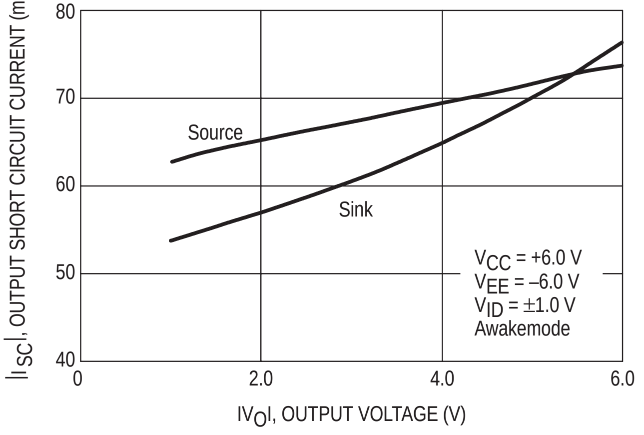


Figure 14. Output Short Circuit Current versus Temperature

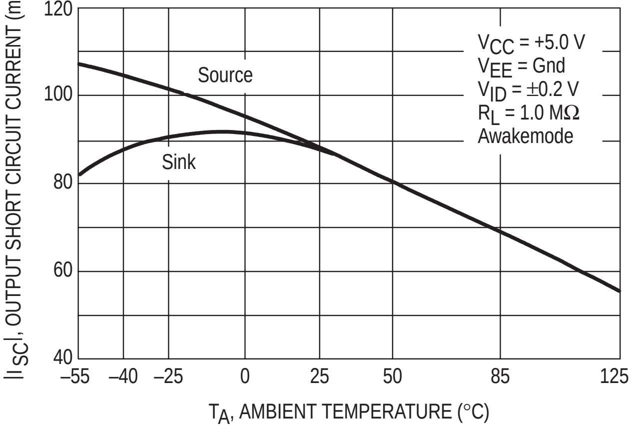


Figure 15. Supply Current versus Supply Voltage with Load

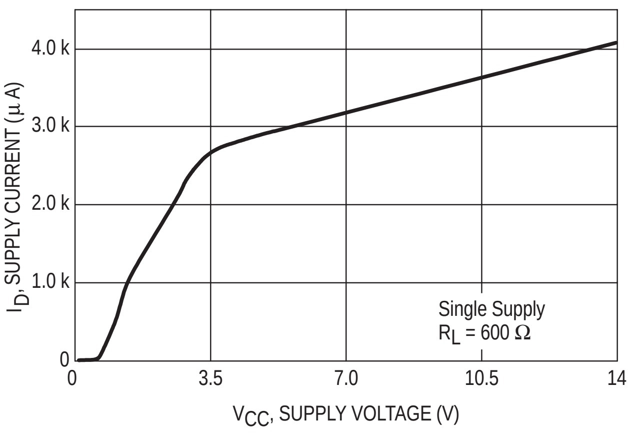


Figure 16. Supply Current versus Supply Voltage

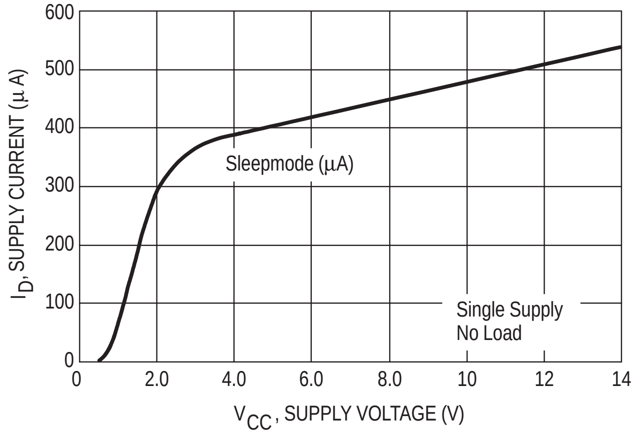


Figure 17. Slew Rate versus Temperature

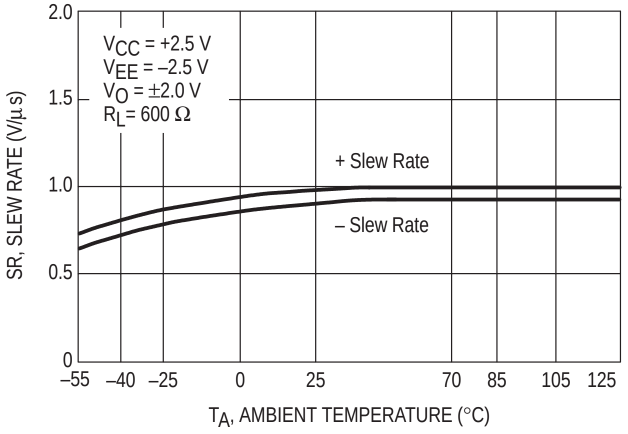


Figure 18. Gain Bandwidth Product versus Temperature

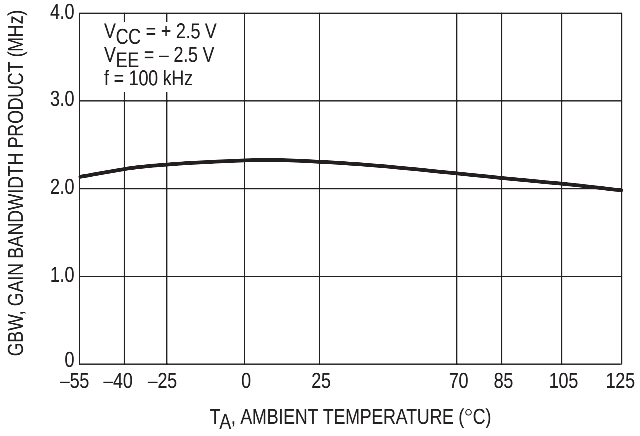


Figure 19. Gain Margin versus Differential Source Resistance

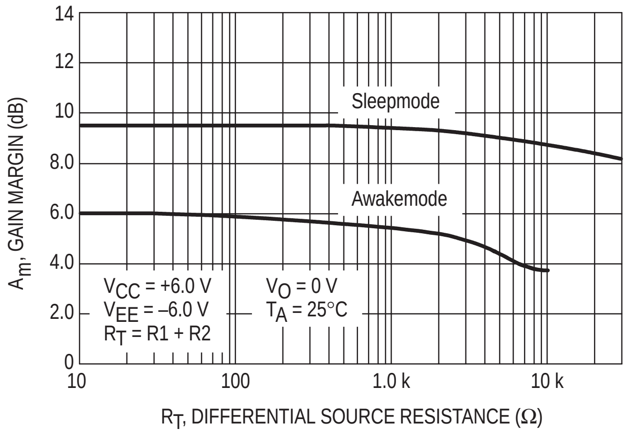


Figure 20. Phase Margin versus Differential Source Resistance

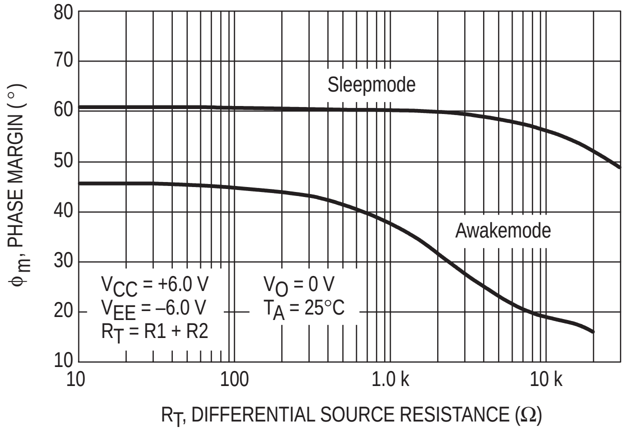


Figure 21. Gain Margin versus Output Load Capacitance

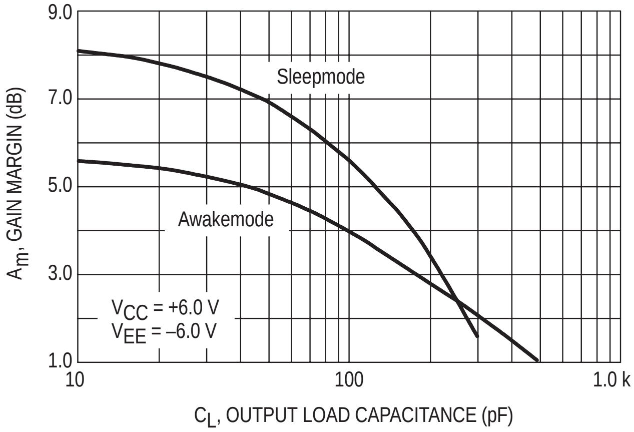


Figure 22. Phase Margin versus Output Load Capacitance

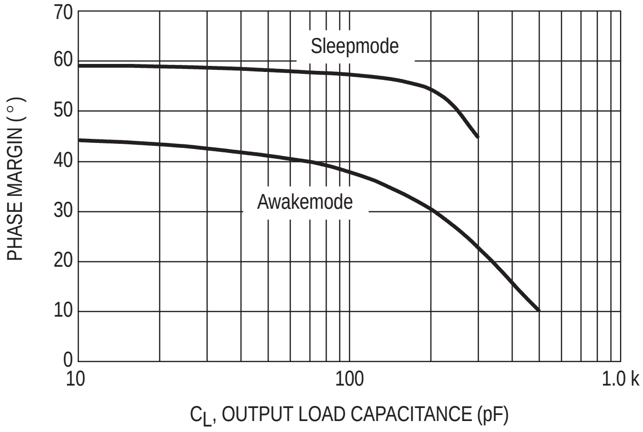


Figure 23. Channel Separation versus Frequency

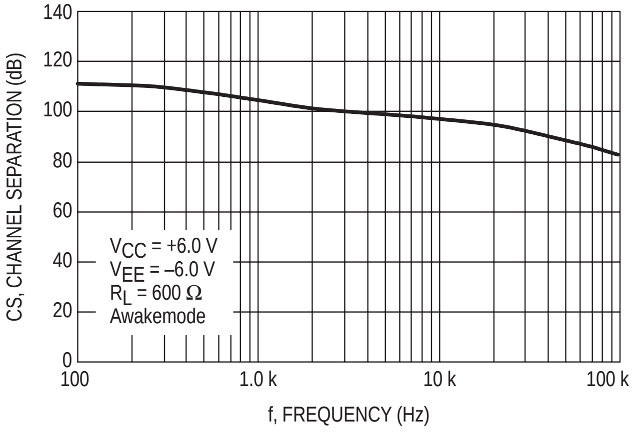


Figure 24. Total Harmonic Distortion versus Frequency

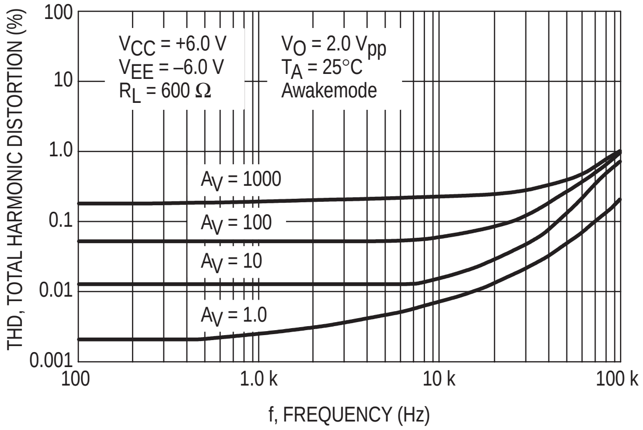


Figure 25. Input Referred Noise Voltage versus Frequency

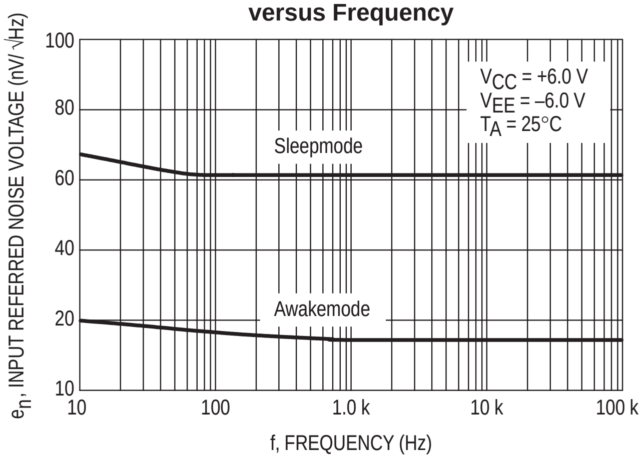


Figure 26. Current Noise versus Frequency

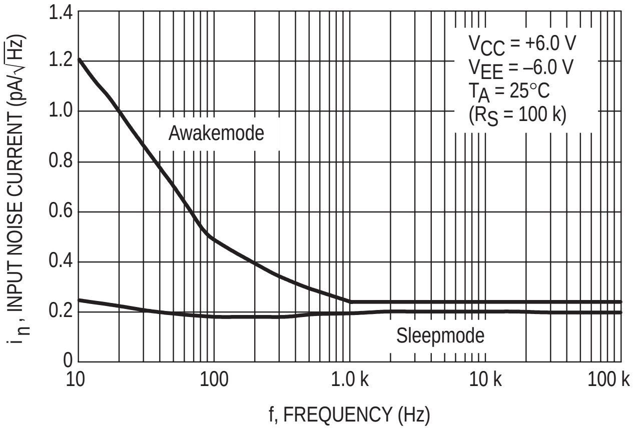
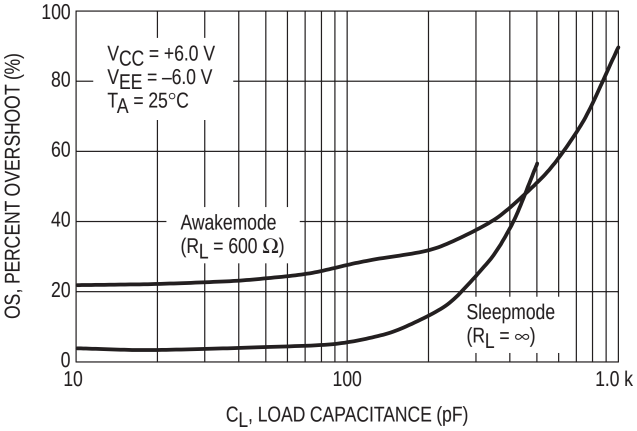


Figure 27. Percent Overshoot versus Load Capacitance



MOTOROLA

MC34001, B
MC34002, B
MC34004, B

JFET Input Operational Amplifiers

These low cost JFET input operational amplifiers combine two state–of–the–art analog technologies on a single monolithic integrated circuit. Each internally compensated operational amplifier has well matched high voltage JFET input devices for low input offset voltage. The BIFET technology provides wide bandwidths and fast slew rates with low input bias currents, input offset currents, and supply currents.

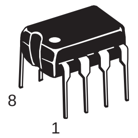
The Motorola BIFET family offers single, dual and quad operational amplifiers which are pin–compatible with the industry standard MC1741, MC1458, and the MC3403/LM324 bipolar devices. The MC34001/34002/34004 series are specified from 0° to +70°C.

- Input Offset Voltage Options of 5.0 mV and 10 mV Maximum
- Low Input Bias Current: 40 pA
- Low Input Offset Current: 10 pA
- Wide Gain Bandwidth: 4.0 MHz
- High Slew Rate: 13 V/µs
- Low Supply Current: 1.4 mA per Amplifier
- High Input Impedance: $10^{12}\ \Omega$
- High Common Mode and Supply Voltage Rejection Ratios: 100 dB
- Industry Standard Pinouts

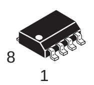
ORDERING INFORMATION

Op Amp Function	Device	Operating Temperature Range	Package
Single	MC34001BD, D	T_A = 0° to+ 70°C	SO–8
	MC34001BP, P		Plastic DIP
Dual	MC34002BD, D	T_A = 0° to +70°C	SO–8
	MC34002BP, P		Plastic DIP
Quad	MC34004BP, P	T_A = 0° to +70°C	Plastic DIP

JFET INPUT OPERATIONAL AMPLIFIERS

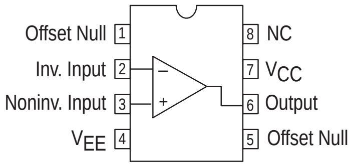


P SUFFIX
PLASTIC PACKAGE
CASE 626

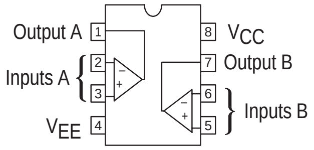


D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

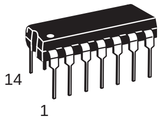
PIN CONNECTIONS



MC34001 (Top View)

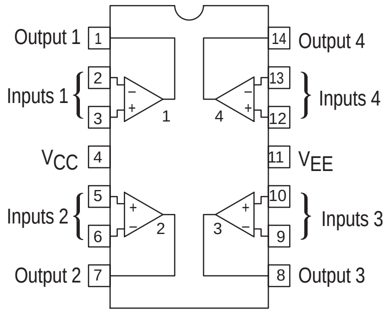


MC34002 (Top View)



P SUFFIX
PLASTIC PACKAGE
CASE 646

PIN CONNECTIONS



MC34004 (Top View)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}, V_{EE}	±18	V
Differential Input Voltage (Note 1)	V_{ID}	±30	V
Input Voltage Range	V_{IDR}	±16	V
Open Short Circuit Duration	t_{SC}	Continuous	
Operating Ambient Temperature Range	T_A	0 to +70	°C
Operating Junction Temperature	T_J	150	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

NOTES: 1. Unless otherwise specified, the absolute maximum negative input voltage is equal to the negative power supply.

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = –15 V, T_A = 25°C, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Input Offset Voltage ($R_S \le 10$ k)	V_{IO}				mV
MC3400XB		—	3.0	5.0	
MC3400X		—	5.0	10	
Average Temperature Coefficient of Input Offset Voltage $R_S \le 10$ k, $T_A = T_{low}$ to T_{high} (Note 2)	$\Delta V_{IO}/\Delta T$	—	10	—	µV/°C
Input Offset Current ($V_{CM} = 0$) (Note 3)	I_{IO}				pA
MC3400XB		—	25	100	
MC3400X		—	25	100	
Input Bias Current ($V_{CM} = 0$) (Note 3)	I_{IB}				pA
MC3400XB		—	50	200	
MC3400X		—	50	200	
Input Resistance	r_i	—	10^{12}	—	Ω
Common Mode Input Voltage Range	V_{ICR}	±11 —	+15 –12	— —	V
Large Signal Voltage Gain (V_O = ±10 V, R_L = 2.0 k)	A_{VOL}				V/mV
MC3400XB		50	150	—	
MC3400X		25	100	—	
Output Voltage Swing	V_O				V
($R_L \ge 10$ k)		±12	±14	—	
($R_L \ge 2.0$ k)		±10	±13	—	
Common Mode Rejection Ratio ($R_S \le 10$ k)	CMRR				dB
MC3400XB		80	100	—	
MC3400X		70	100	—	
Supply Voltage Rejection Ratio ($R_S \le 10$ k) (Note 4)	PSRR				dB
MC3400XB		80	100	—	
MC3400X		70	100	—	
Supply Current (Each Amplifier)	I_D				mA
MC3400XB		—	1.4	2.5	
MC3400X		—	1.4	2.7	
Slew Rate ($A_V = 1.0$)	SR	—	13	—	V/µs
Gain–Bandwidth Product	GBW	—	4.0	—	MHz
Equivalent Input Noise Voltage (R_S = 100 Ω, f = 1000 Hz)	e_n	—	25	—	$nV/\sqrt{Hz}$
Equivalent Input Noise Current (f = 1000 Hz)	i_n	—	0.01	—	$pA/\sqrt{Hz}$

NOTES: 2. T_{low} = 0°C for MC34001/34001B; MC34002; MC34004/34004B — T_{high} = +70°C for MC34001/34001B; MC34002; MC34004/34004B

3. The input bias currents approximately double for every 10°C rise in junction temperature, T_J. Due to limited test time, the input bias currents are correlated to junction temperature. Use of a heatsink is recommended if input bias current is to be kept to a minimum.

4. Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously, in accordance with common practice.

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = –15 V, T_A = T_{low} to T_{high} [Note 2].)

Characteristics	Symbol	Min	Typ	Max	Unit
Input Offset Voltage (R_S ≤ 10 k)	V_{IO}				mV
MC3400XB		—	—	7.0	
MC3400X		—	—	13	
Input Offset Current (V_{CM} = 0) (Note 3)	I_{IO}				nA
MC3400XB		—	—	4.0	
MC3400X		—	—	4.0	
Input Bias Current (V_{CM} = 0) (Note 3)	I_{IB}				nA
MC3400XB		—	—	8.0	
MC3400X		—	—	8.0	
Common Mode Input Voltage Range	V_{ICR}	±11	—	—	V
Large Signal (V_O = ±10 V, R_L = 2.0 k)	A_{VOL}				V/mV
MC3400XB		25	—	—	
MC3400X		15	—	—	
Output Voltage Swing	V_O				V
(R ≥ 10 k)		±12	—	—	
(R ≥ 2.0 k)		±10	—	—	
Common Mode Rejection Ratio (R_S ≤ 10 k)	CMRR				dB
MC3400XB		80	—	—	
MC3400X		70	—	—	
Supply Voltage Rejection Ratio (R_S ≤ 10 k) (Note 4)	PSRR				dB
MC3400XB		80	—	—	
MC3400X		70	—	—	
Supply Current (Each Amplifier)	I_D				mA
MC3400XB		—	—	2.8	
MC3400X		—	—	3.0	

NOTES: 2. T_{low} = 0°C for MC34001/34001B T_{high} = +70°C for MC34001/34001B
MC34002 MC34002
MC34004/34004B MC34004/34004B

3. The input bias currents approximately double for every 10°C rise in junction temperature, T_J. Due to limited test time, the input bias currents are correlated to junction temperature. Use of a heatsink is recommended if input bias current is to be kept to a minimum.
4. Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously, in accordance with common practice.

Figure 1. Input Bias Current versus Temperature

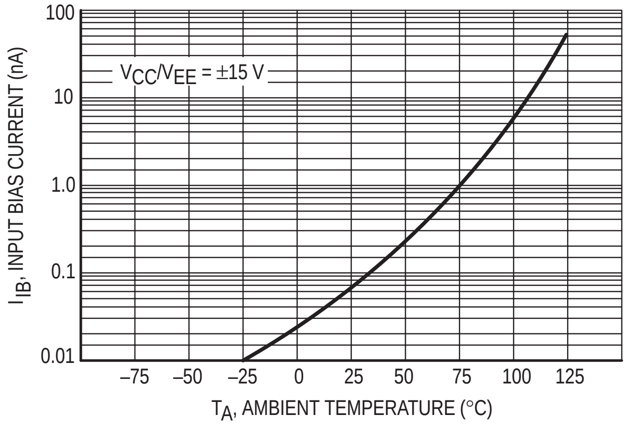


Figure 2. Output Voltage Swing versus Frequency

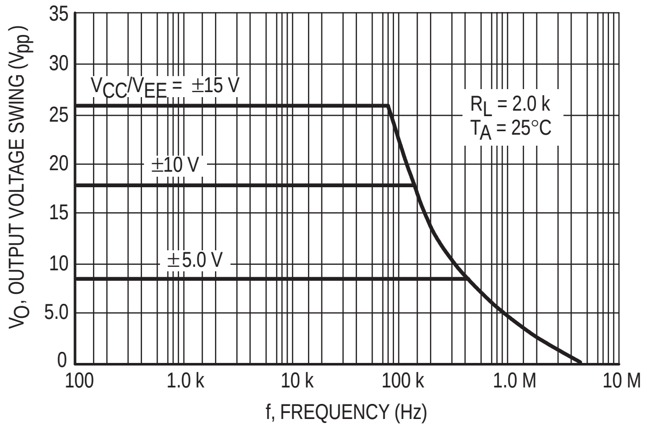


Figure 3. Output Voltage Swing versus Load Resistance

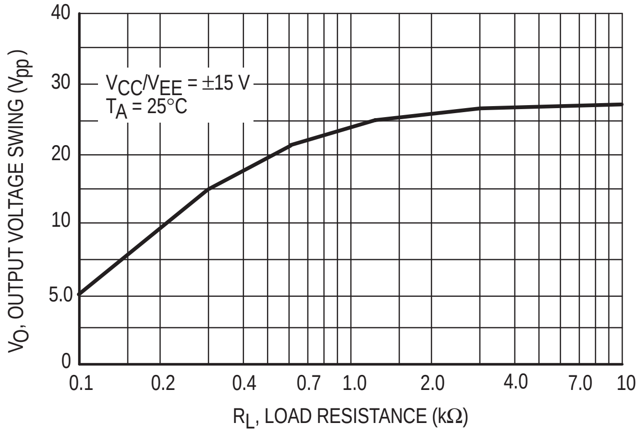


Figure 4. Output Voltage Swing versus Supply Voltage

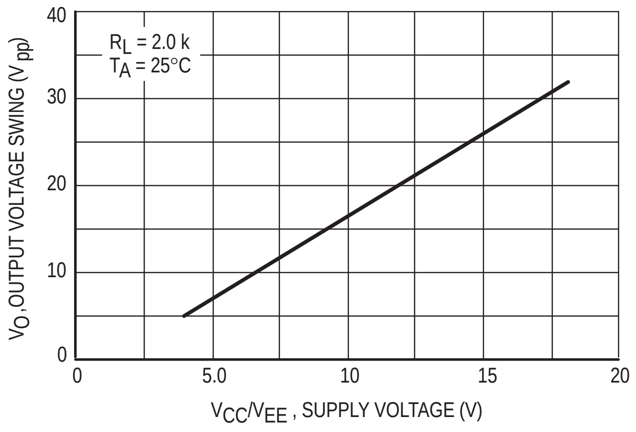


Figure 5. Output Voltage Swing versus Temperature

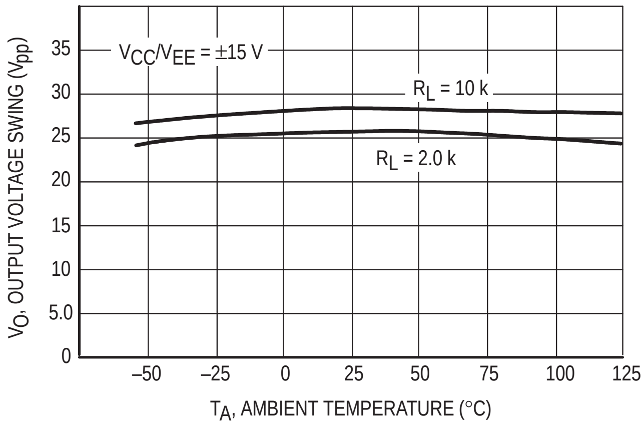


Figure 6. Supply Current per Amplifier versus Temperature

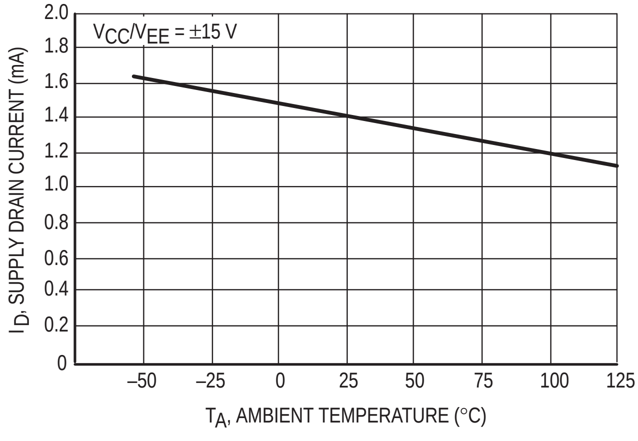


Figure 7. Large–Signal Voltage Gain and Phase Shift versus Frequency

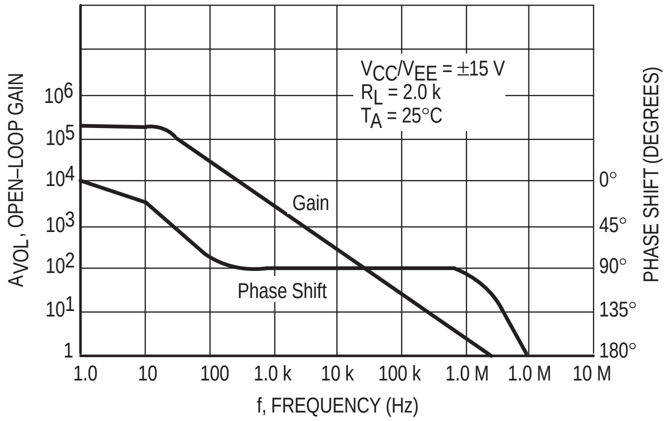


Figure 8. Large–Signal Voltage Gain versus Temperature

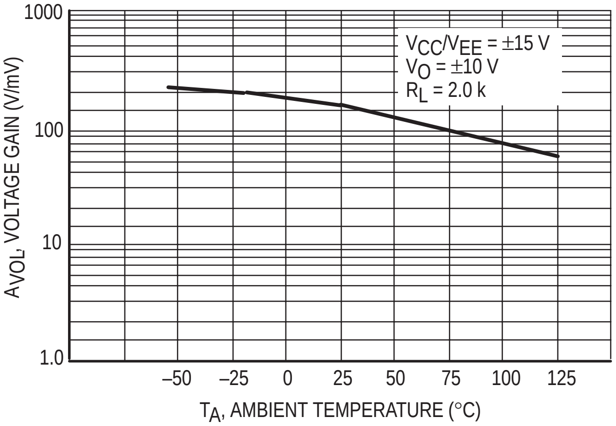


Figure 9. Normalized Slew Rate versus Temperature

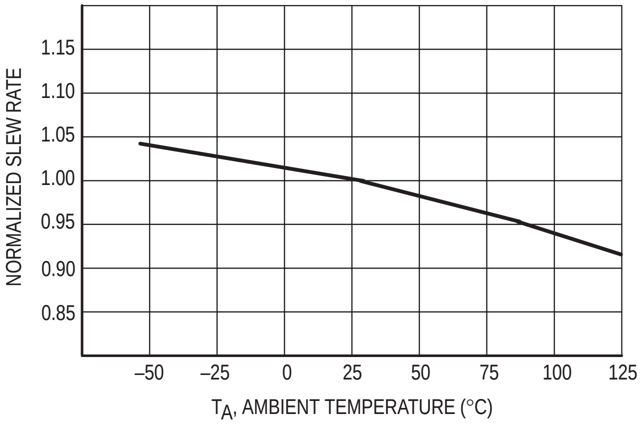


Figure 10. Equivalent Input Noise Voltage versus Frequency

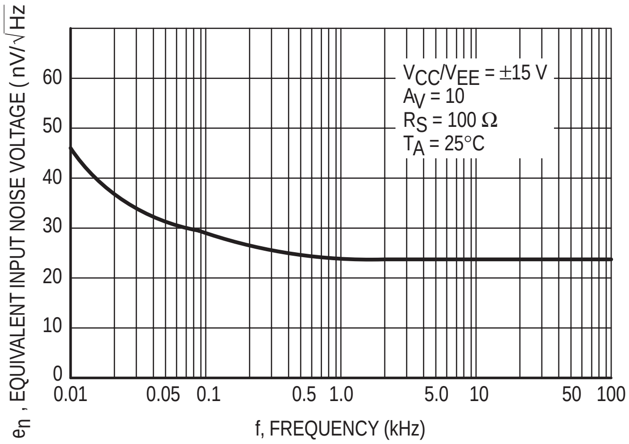
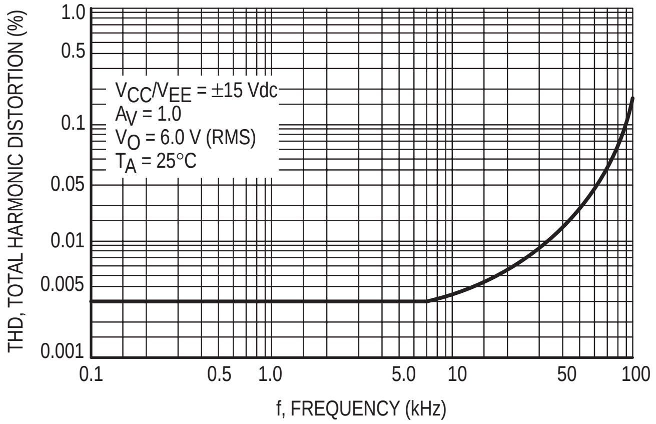


Figure 11. Total Harmonic Distortion versus Frequency



Representative Circuit Schematic
(Each Amplifier)

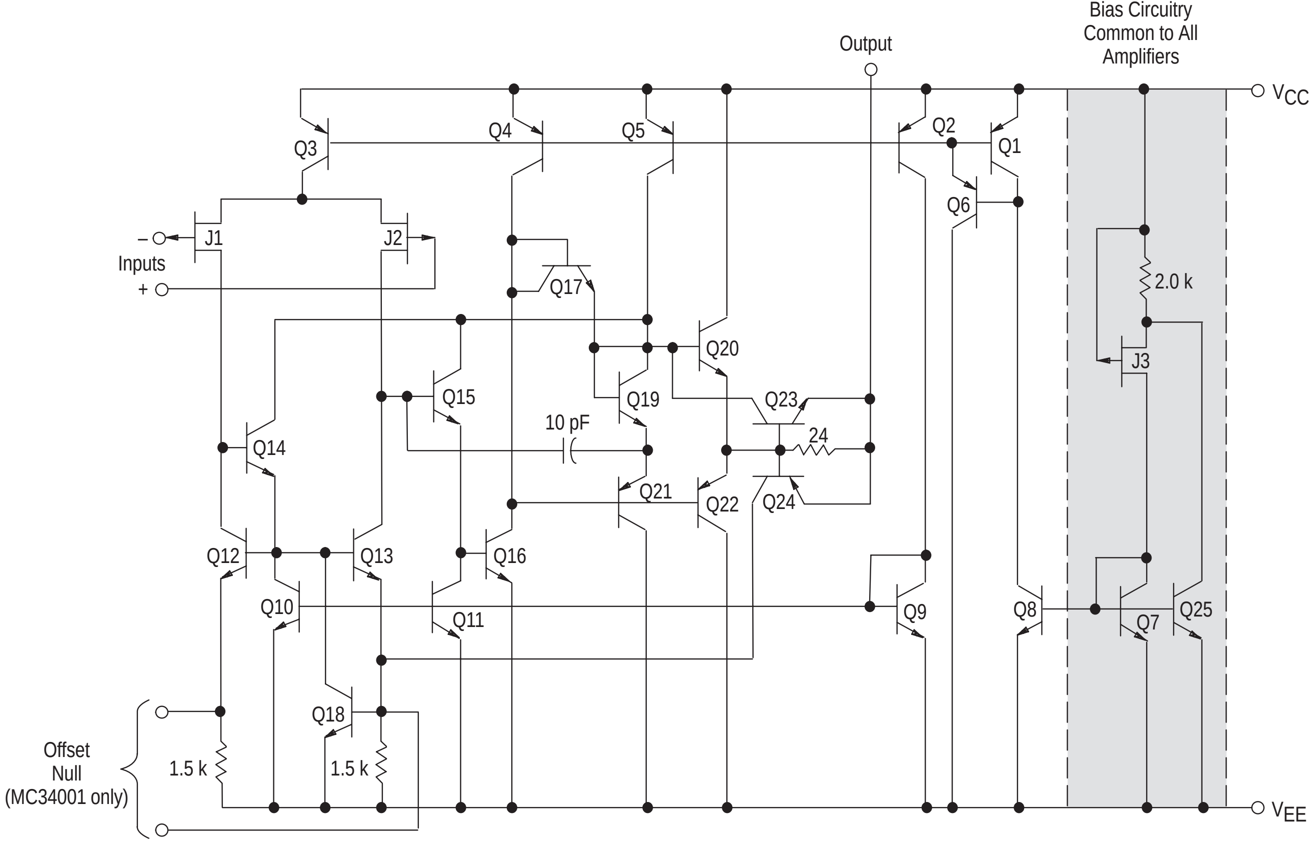
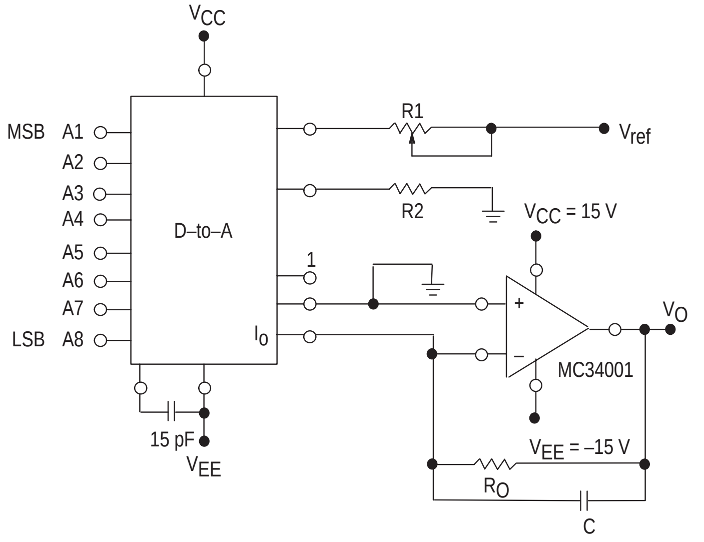


Figure 12. Output Current to Voltage Transformation for a D–to–A Converter



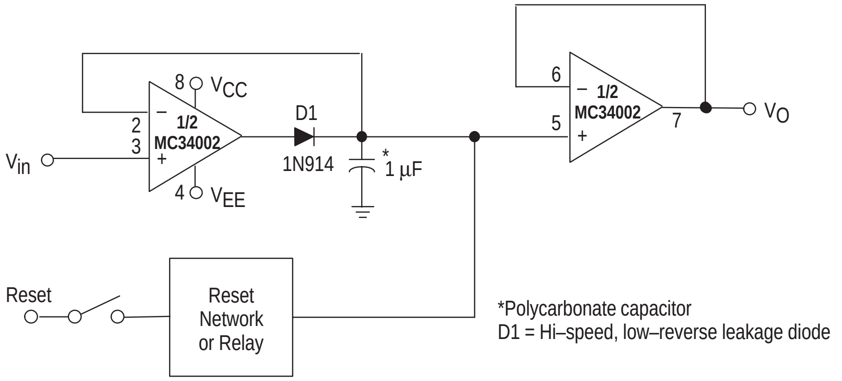
Settling time to within 1/2 LSB is approximately 4.0 µs from the time all bits are switched (C = 68 pF).

The value of C may be selected to minimize overshoot and ringing.

Theoretical V_O

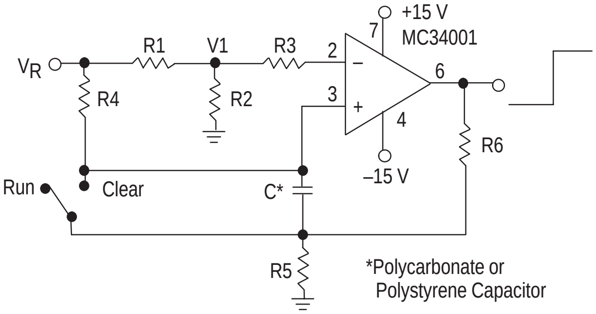
$$V_O = \frac{V_{ref}}{R1}(R_O)\left[\frac{A1}{2} + \frac{A2}{4} + \frac{A3}{8} + \frac{A4}{16} + \frac{A5}{32} + \frac{A6}{64} + \frac{A7}{128} + \frac{A8}{256}\right]$$

Figure 13. Positive Peak Detector



*Polycarbonate capacitor
D1 = Hi–speed, low–reverse leakage diode

Figure 14. Long Interval RC Timer

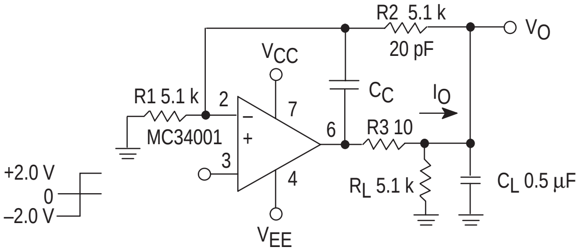


*Polycarbonate or
Polystyrene Capacitor

Time (t) = R4 Cn (V_R/V_R–V_I), $R_3 = R_4$, $R_5 = 0.1\ R_6$
If R1 = R2: t = 0.693 R4C

Design Example: 100 Second Timer
V_R = 10 V C = l.0 µF R3 = R4 = 144 M
R6 = 20 k R5 = 2.0 k R1 = R2 = 1.0 k

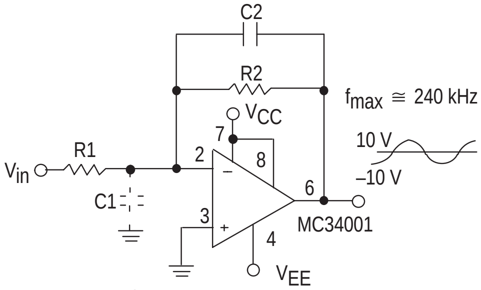
Figure 15. Isolating Large Capacitive Loads



Overshoot < 10%
t_S = 10 µs
When driving large C_L, the V_O slew rate is determined by C_L and $I_{O(max)}$:

$$\frac{\Delta V_O}{\Delta t} = \frac{I_O}{C_L} = \frac{0.02}{0.5}\ \text{V/µs} = 0.04\ \text{V/µs (with } C_L \text{ shown)}$$

Figure 16. Wide BW, Low Noise, Low Drift Amplifier



Power BW: $f_{max} = \frac{S_r}{2\pi\ Vp} \cong 240$ kHz

Parasitic input capacitance (C1 ≅ 3.0 pF plus any additional layout capacitance) interacts with feedback elements and creates undesirable high–frequency pole. To compensate add C2 such that: R2C2 ≅ R1C1.

MOTOROLA

MC34071,2,4,A
MC33071,2,4,A

High Slew Rate, Wide Bandwidth, Single Supply Operational Amplifiers

Quality bipolar fabrication with innovative design concepts are employed for the MC33071/72/74, MC34071/72/74 series of monolithic operational amplifiers. This series of operational amplifiers offer 4.5 MHz of gain bandwidth product, 13 V/µs slew rate and fast setting time without the use of JFET device technology. Although this series can be operated from split supplies, it is particularly suited for single supply operation, since the common mode input voltage range includes ground potential (V_{EE}). With A Darlington input stage, this series exhibits high input resistance, low input offset voltage and high gain. The all NPN output stage, characterized by no deadband crossover distortion and large output voltage swing, provides high capacitance drive capability, excellent phase and gain margins, low open loop high frequency output impedance and symmetrical source/sink AC frequency response.

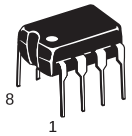
The MC33071/72/74, MC34071/72/73 series of devices are available in standard or prime performance (A Suffix) grades and are specified over the commercial, industrial/vehicular or military temperature ranges. The complete series of single, dual and quad operational amplifiers are available in plastic DIP and SOIC surface mount packages.

- Wide Bandwidth: 4.5 MHz
- High Slew Rate: 13 V/µs
- Fast Settling Time: 1.1 µs to 0.1%
- Wide Single Supply Operation: 3.0 V to 44 V
- Wide Input Common Mode Voltage Range: Includes Ground (V_{EE})
- Low Input Offset Voltage: 3.0 mV Maximum (A Suffix)
- Large Output Voltage Swing: –14.7 V to +14 V (with ±15 V Supplies)
- Large Capacitance Drive Capability: 0 pF to 10,000 pF
- Low Total Harmonic Distortion: 0.02%
- Excellent Phase Margin: 60°
- Excellent Gain Margin: 12 dB
- Output Short Circuit Protection
- ESD Diodes/Clamps Provide Input Protection for Dual and Quad

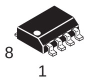
ORDERING INFORMATION

Op Amp Function	Device	Operating Temperature Range	Package
Single	MC34071P, AP MC34071D, AD	T_A = 0° to +70°C	Plastic DIP SO–8
	MC33071P, AP MC33071D, AD	T_A = –40° to +85°C	Plastic DIP SO–8
Dual	MC34072P, AP MC34072D, AD	T_A = 0° to +70°C	Plastic DIP SO–8
	MC33072P, AP MC33072D, AD	T_A = –40° to +85°C	Plastic DIP SO–8
Quad	MC34074P, AP MC34074D, AD	T_A = 0° to +70°C	Plastic DIP SO–14
	MC33074P, AP MC33074D, AD	T_A = –40° to +85°C	Plastic DIP SO–14

HIGH BANDWIDTH SINGLE SUPPLY OPERATIONAL AMPLIFIERS

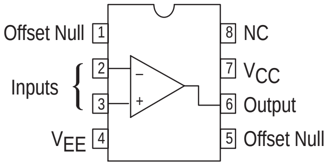


P SUFFIX
PLASTIC PACKAGE
CASE 626

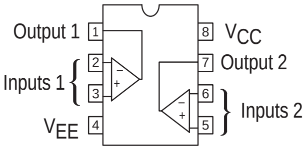


D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

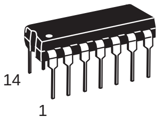
PIN CONNECTIONS



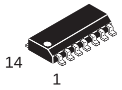
(Single, Top View)



(Dual, Top View)

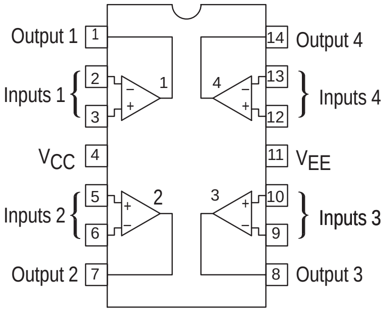


P SUFFIX
PLASTIC PACKAGE
CASE 646



D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO–14)

PIN CONNECTIONS



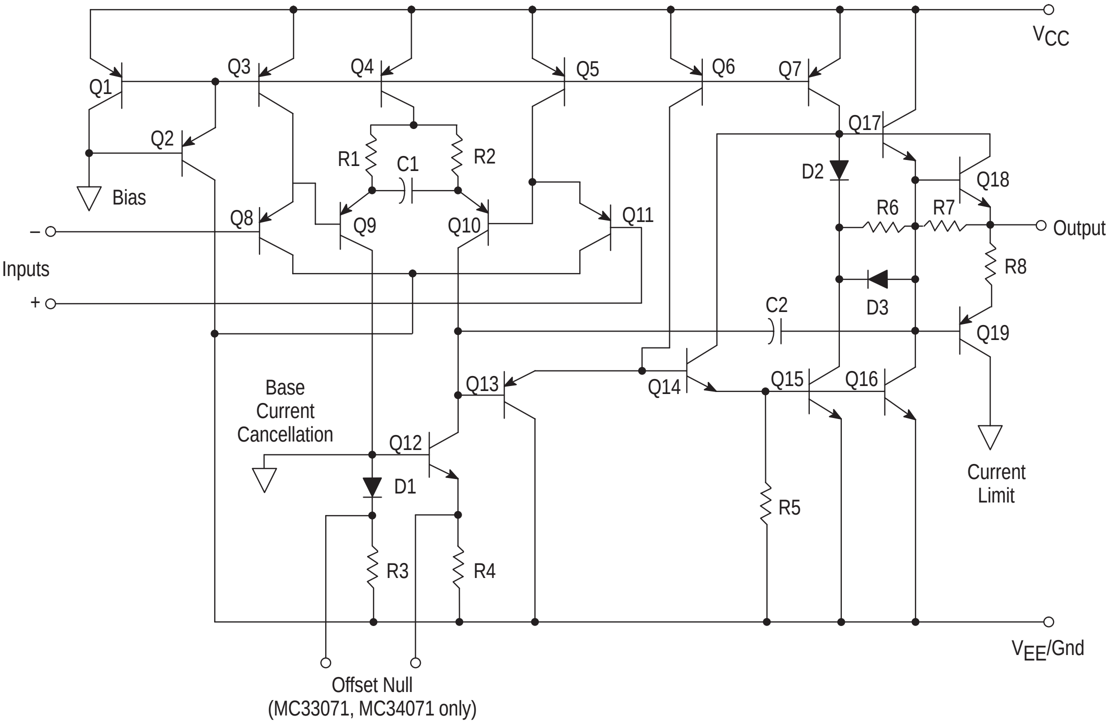
(Quad, Top View)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage (from V_{EE} to V_{CC})	V_S	+44	V
Input Differential Voltage Range	V_{IDR}	Note 1	V
Input Voltage Range	V_{IR}	Note 1	V
Output Short Circuit Duration (Note 2)	t_{SC}	Indefinite	sec
Operating Junction Temperature	T_J	+150	°C
Storage Temperature Range	T_{stg}	–60 to +150	°C

NOTES: 1. Either or both input voltages should not exceed the magnitude of V_{CC} or V_{EE}.
2. Power dissipation must be considered to ensure maximum junction temperature (T_J) is not exceeded (see Figure 1).

Representative Schematic Diagram
(Each Amplifier)



ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = –15 V, R_L = connected to ground, unless otherwise noted. See Note 3 for T_A = T_{low} to T_{high})

		A Suffix			Non–Suffix			
Characteristics	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
Input Offset Voltage (R_S = 100 Ω, V_{CM} = 0 V, V_O = 0 V)	V_{IO}							mV
V_{CC} = +15 V, V_{EE} = –15 V, T_A = +25°C		—	0.5	3.0	—	1.0	5.0	
V_{CC} = +5.0 V, V_{EE} = 0 V, T_A = +25°C		—	0.5	3.0	—	1.5	5.0	
V_{CC} = +15 V, V_{EE} = –15 V, T_A = T_{low} to T_{high}		—	—	5.0	—	—	7.0	
Average Temperature Coefficient of Input Offset Voltage R_S = 10 Ω, V_{CM} = 0 V, V_O = 0 V, T_A = T_{low} to T_{high}	$\Delta V_{IO}/\Delta T$	—	10	—	—	10	—	µV/°C
Input Bias Current (V_{CM} = 0 V, V_O = 0 V)	I_{IB}							nA
T_A = +25°C		—	100	500	—	100	500	
T_A = T_{low} to T_{high}		—	—	700	—	—	700	
Input Offset Current (V_{CM} = 0 V, V_O = 0V)	I_{IO}							nA
T_A = +25°C		—	6.0	50	—	6.0	75	
T_A = T_{low} to T_{high}		—	—	300	—	—	300	
Input Common Mode Voltage Range	V_{ICR}							V
T_A = +25°C		V_{EE} to (V_{CC} –1.8)			V_{EE} to (V_{CC} –1.8)			
T_A = T_{low} to T_{high}		V_{EE} to (V_{CC} –2.2)			V_{EE} to (V_{CC} –2.2)			
Large Signal Voltage Gain (V_O = ±10 V, R_L = 2.0 kΩ)	A_{VOL}							V/mV
T_A = +25°C		50	100	—	25	100	—	
T_A = T_{low} to T_{high}		25	—	—	20	—	—	
Output Voltage Swing (V_{ID} = ±1.0 V)	V_{OH}							V
V_{CC} = +5.0 V, V_{EE} = 0 V, R_L = 2.0 kΩ, T_A = +25°C		3.7	4.0	—	3.7	4.0	—	
V_{CC} = +15 V, V_{EE} = –15 V, R_L = 10 kΩ, T_A = +25°C		13.6	14	—	13.6	14	—	
V_{CC} = +15 V, V_{EE} = –15 V, R_L = 2.0 kΩ, T_A = T_{low} to T_{high}		13.4	—	—	13.4	—	—	
V_{CC} = +5.0 V, V_{EE} = 0 V, R_L = 2.0 kΩ, T_A = +25°C	V_{OL}	—	0.1	0.3	—	0.1	0.3	V
V_{CC} = +15 V, V_{EE} = –15 V, R_L = 10 kΩ, T_A = +25°C		—	–14.7	–14.3	—	–14.7	–14.3	
V_{CC} = +15 V, V_{EE} = –15 V, R_L = 2.0 kΩ, T_A = T_{low} to T_{high}		—	—	–13.5	—	—	–13.5	
Output Short Circuit Current (V_{ID} = 1.0 V, V_O = 0 V, T_A = 25°C)	I_{SC}							mA
Source		10	30	—	10	30	—	
Sink		20	30	—	20	30	—	
Common Mode Rejection R_S ≤ 10 kΩ, V_{CM} = V_{ICR}, T_A = 25°C	CMR	80	97	—	70	97	—	dB
Power Supply Rejection (R_S = 100 Ω) V_{CC}/V_{EE} = +16.5 V/–16.5 V to +13.5 V/–13.5 V, T_A = 25°C	PSR	80	97	—	70	97	—	dB
Power Supply Current (Per Amplifier, No Load)	I_D							mA
V_{CC} = +5.0 V, V_{EE} = 0 V, V_O = +2.5 V, T_A = +25°C		—	1.6	2.0	—	1.6	2.0	
V_{CC} = +15 V, V_{EE} = –15 V, V_O = 0 V, T_A = +25°C		—	1.9	2.5	—	1.9	2.5	
V_{CC} = +15 V, V_{EE} = –15 V, V_O = 0 V, T_A = T_{low} to T_{high}		—	—	2.8	—	—	2.8	

NOTES: 3. T_{low} = –40°C for MC33071, 2, 4, /A
= 0°C for MC34071, 2, 4, /A
T_{high} = +85°C for MC33071, 2, 4, /A
= +70°C for MC34071, 2, 4, /A

AC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = –15 V, R_L = connected to ground. T_A = +25°C, unless otherwise noted.)

		A Suffix			Non–Suffix			
Characteristics	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
Slew Rate (V_{in} = –10 V to +10 V, R_L = 2.0 kΩ, C_L = 500 pF) A_V = +1.0 A_V = –1.0	SR	 8.0 —	 10 13	 — —	 8.0 —	 10 13	 — —	V/µs
Setting Time (10 V Step, A_V = –1.0) To 0.1% (+1/2 LSB of 9–Bits) To 0.01% (+1/2 LSB of 12–Bits)	t_s	 — —	 1.1 2.2	 — —	 — —	 1.1 2.2	 — —	µs
Gain Bandwidth Product (f = 100 kHz)	GBW	3.5	4.5	—	3.5	4.5	—	MHz
Power Bandwidth A_V = +1.0, R_L = 2.0 kΩ, V_O = 20 V_{pp}, THD = 5.0%	BW	—	160	—	—	160	—	kHz
Phase margin R_L = 2.0 kΩ R_L = 2.0 kΩ, C_L = 300 pF	f_m	 — —	 60 40	 — —	 — —	 60 40	 — —	Deg
Gain Margin R_L = 2.0 kΩ R_L = 2.0 kΩ, C_L = 300 pF	A_m	 — —	 12 4.0	 — —	 — —	 12 4.0	 — —	dB
Equivalent Input Noise Voltage R_S = 100 Ω, f = 1.0 kHz	e_n	—	32	—	—	32	—	$nV/\sqrt{Hz}$
Equivalent Input Noise Current f = 1.0 kHz	i_n	—	0.22	—	—	0.22	—	$pA/\sqrt{Hz}$
Differential Input Resistance V_{CM} = 0 V	R_{in}	—	150	—	—	150	—	MΩ
Differential Input Capacitance V_{CM} = 0 V	C_{in}	—	2.5	—	—	2.5	—	pF
Total Harmonic Distortion A_V = +10, R_L = 2.0 kΩ, 2.0 $V_{pp} \le V_O \le$ 20 V_{pp}, f = 10 kHz	THD	—	0.02	—	—	0.02	—	%
Channel Separation (f = 10 kHz)	—	—	120	—	—	120	—	dB
Open Loop Output Impedance (f = 1.0 MHz)	$\|Z_O\|$	—	30	—	—	30	—	W

Figure 1. Power Supply Configurations

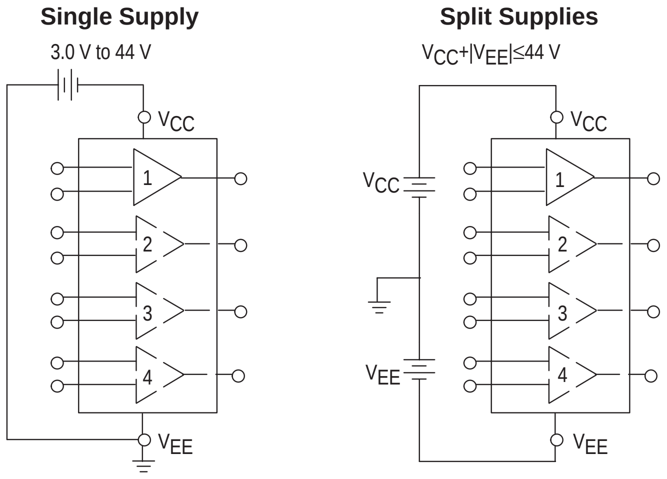
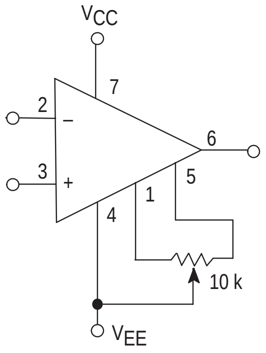

Single Supply
Split Supplies

Figure 2. Offset Null Circuit



Offset nulling range is approximately ±80 mV with a 10 k potentiometer (MC33071, MC34071 only).

Figure 3. Maximum Power Dissipation versus Temperature for Package Types

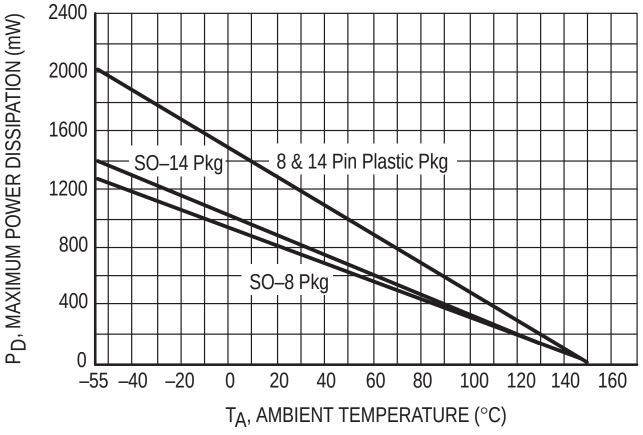


Figure 4. Input Offset Voltage versus Temperature for Representative Units

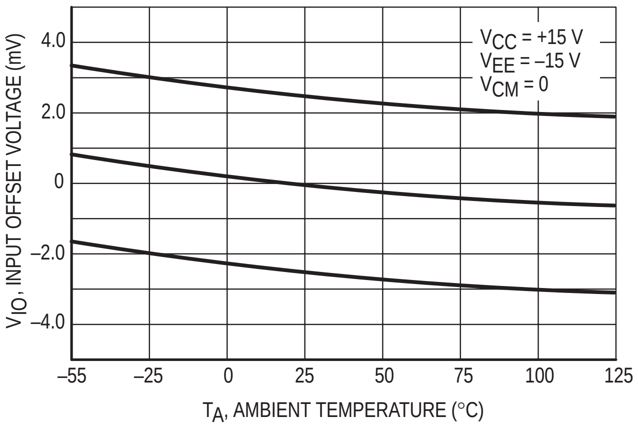


Figure 5. Input Common Mode Voltage Range versus Temperature

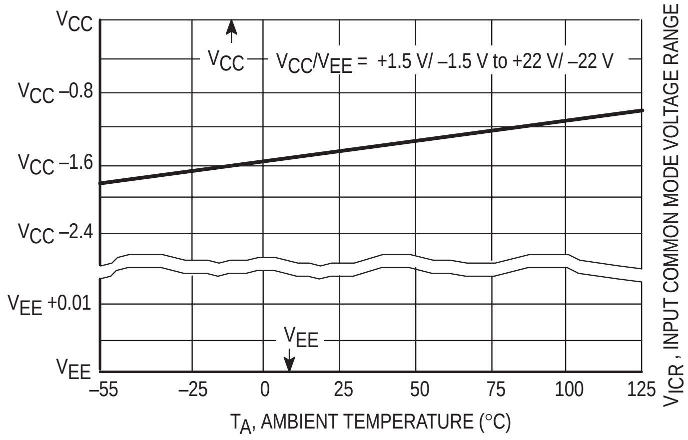


Figure 6. Normalized Input Bias Current versus Temperature

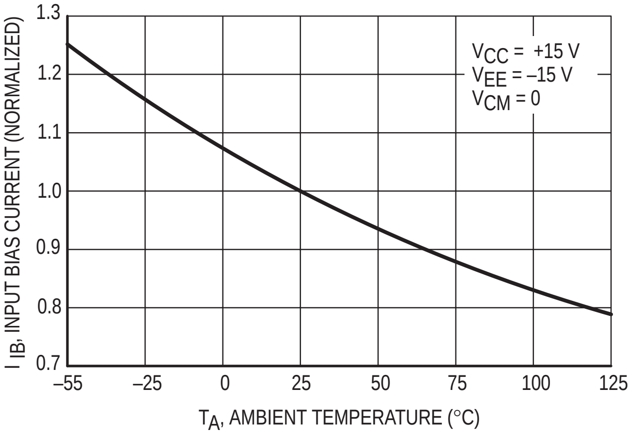


Figure 7. Normalized Input Bias Current versus Input Common Mode Voltage

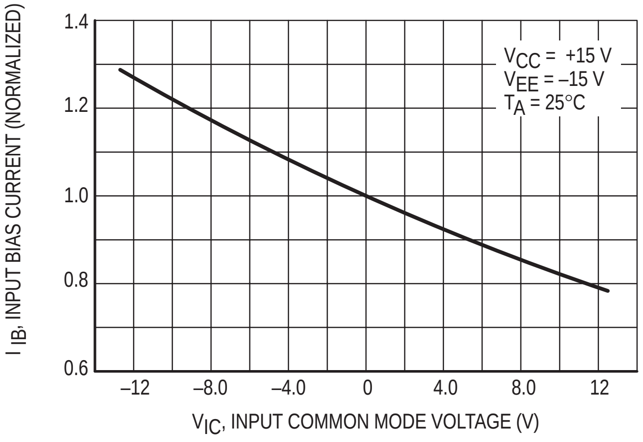


Figure 8. Split Supply Output Voltage Swing versus Supply Voltage

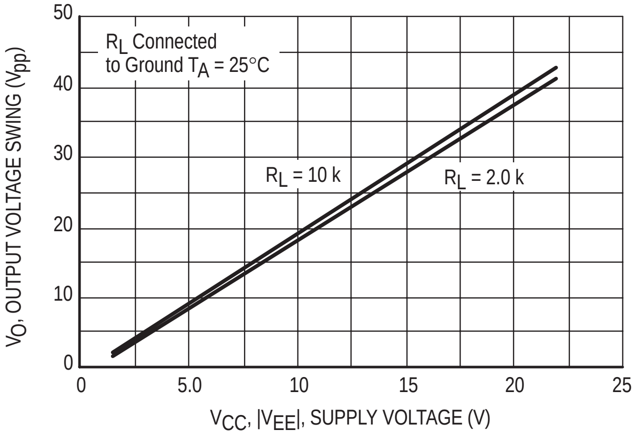


Figure 9. Single Supply Output Saturation versus Load Resistance to V_{CC}

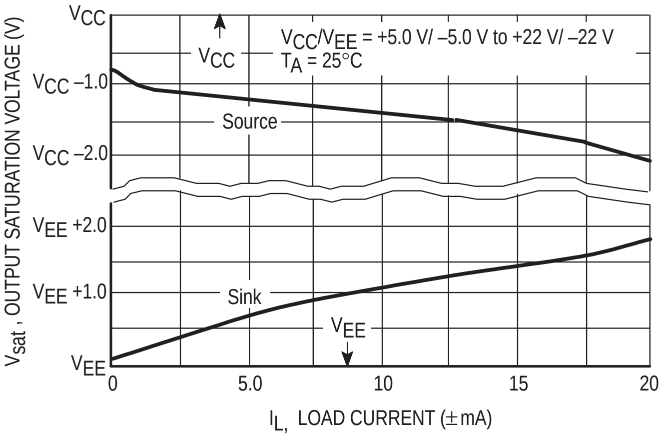


Figure 10. Split Supply Output Saturation versus Load Current

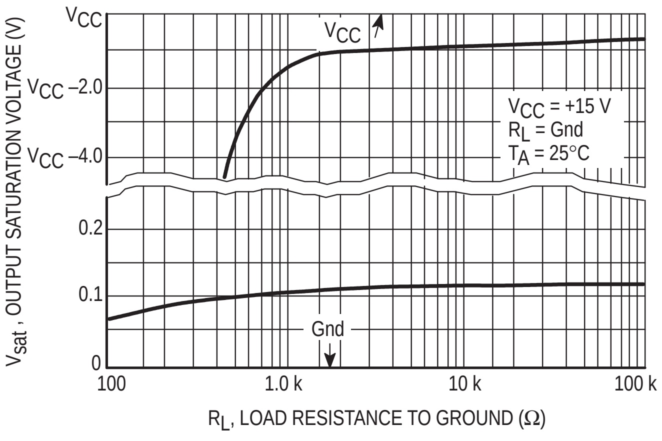


Figure 11. Single Supply Output Saturation versus Load Resistance to Ground

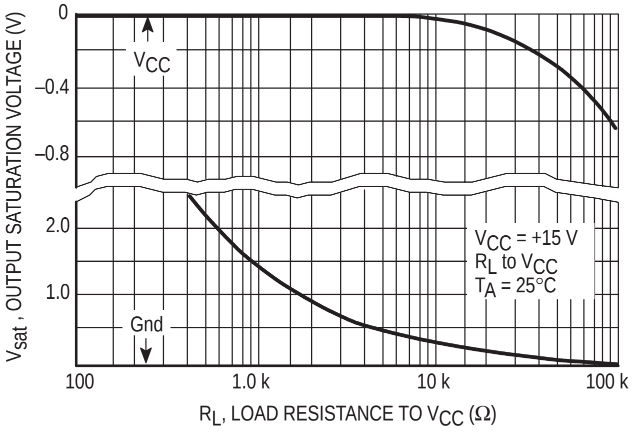


Figure 12. Output Short Circuit Current versus Temperature

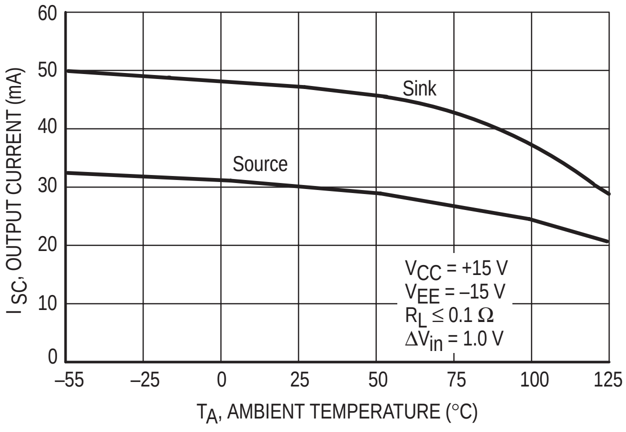


Figure 13. Output Impedance versus Frequency

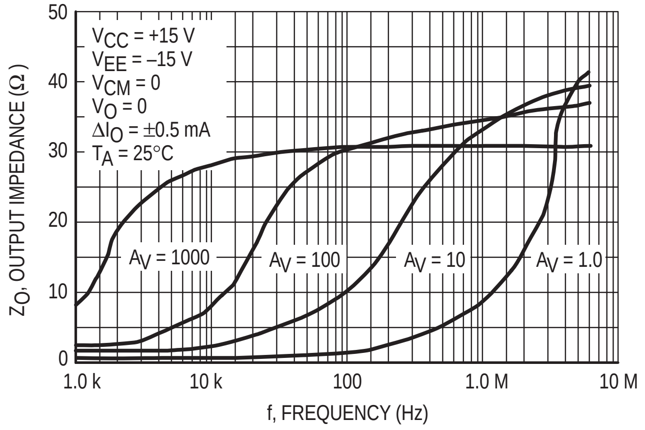


Figure 14. Output Voltage Swing versus Frequency

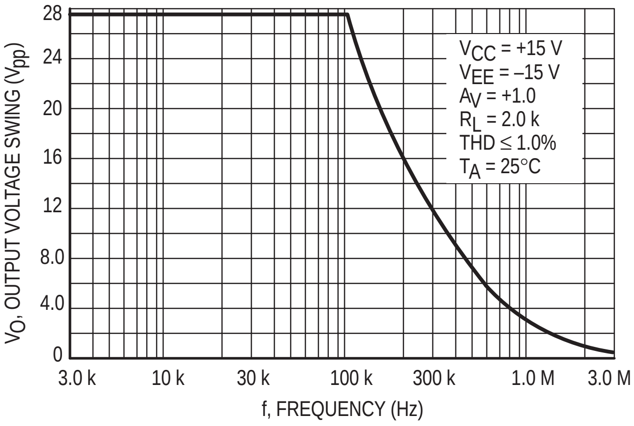


Figure 15. Total Harmonic Distortion versus Frequency

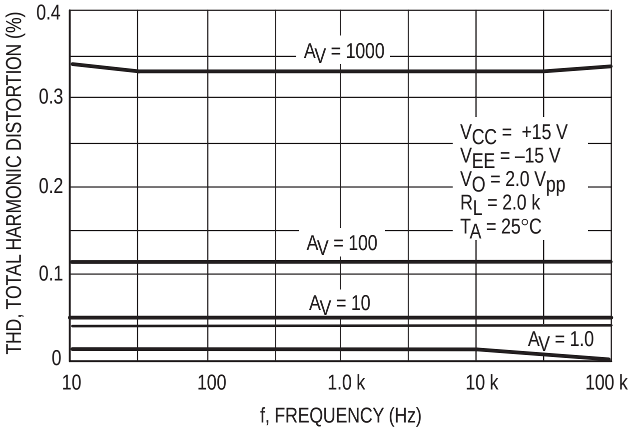


Figure 16. Total Harmonic Distortion versus Output Voltage Swing

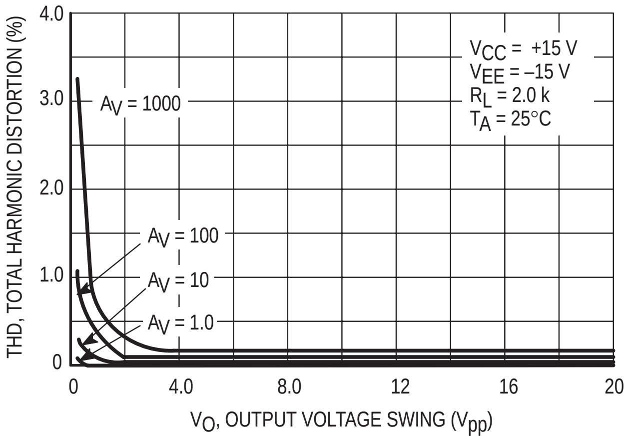


Figure 17. Open Loop Voltage Gain versus Temperature

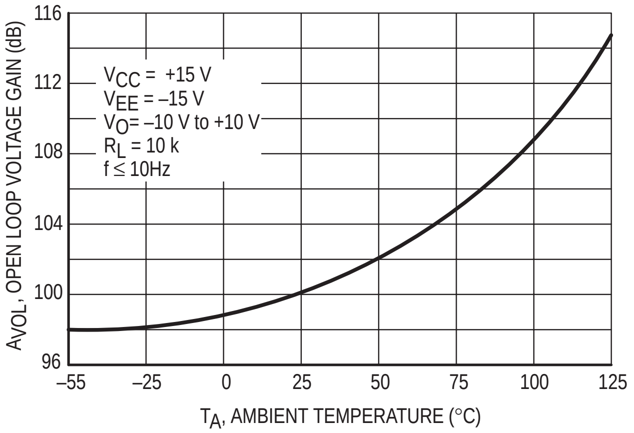


Figure 18. Open Loop Voltage Gain and Phase versus Frequency

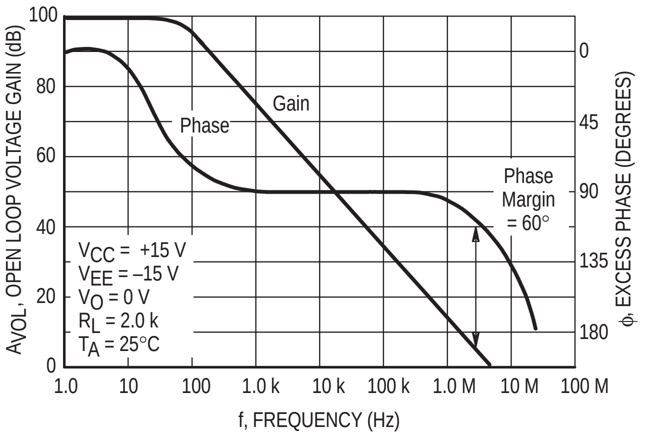


Figure 19. Open Loop Voltage Gain and Phase versus Frequency

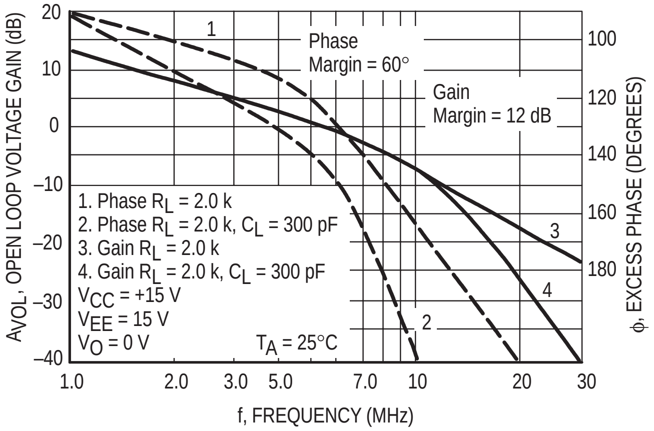


Figure 20. Normalized Gain Bandwidth Product versus Temperature

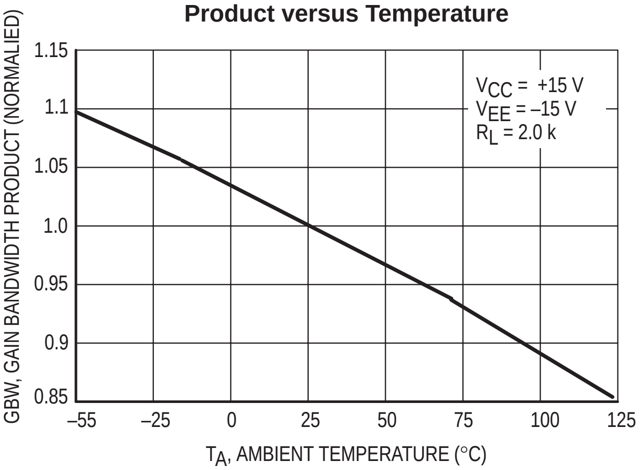


Figure 21. Percent Overshoot versus Load Capacitance

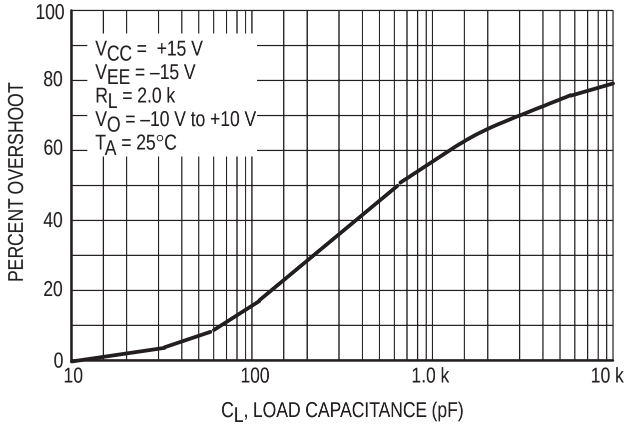


Figure 22. Phase Margin versus Load Capacitance

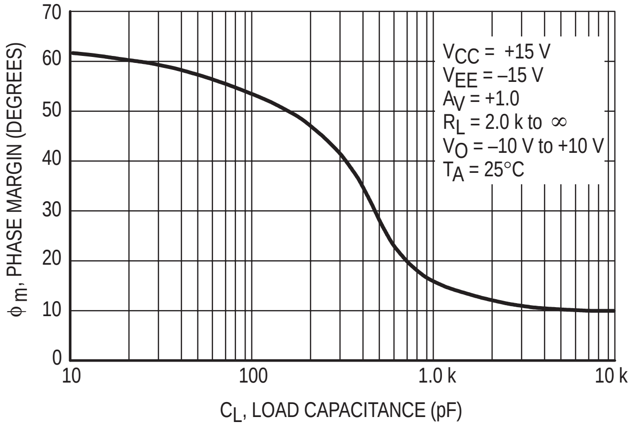


Figure 23. Gain Margin versus Load Capacitance

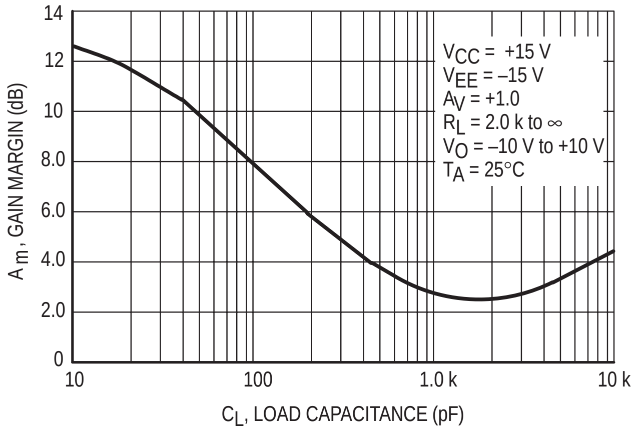


Figure 24. Phase Margin versus Temperature

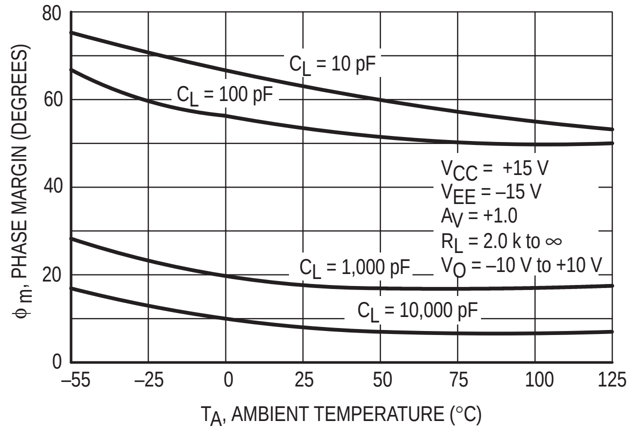


Figure 25. Gain Margin versus Temperature

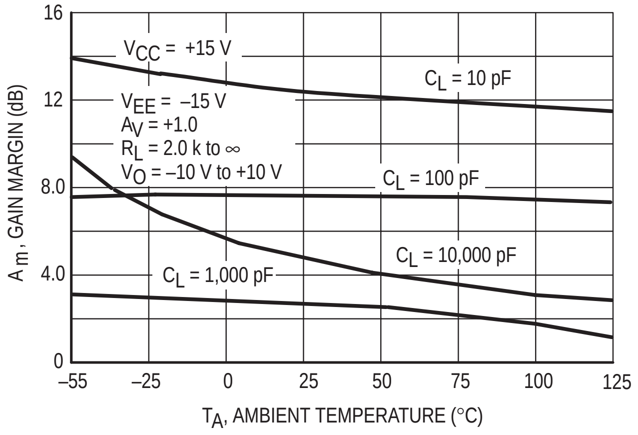


Figure 26. Phase Margin and Gain Margin versus Differential Source Resistance

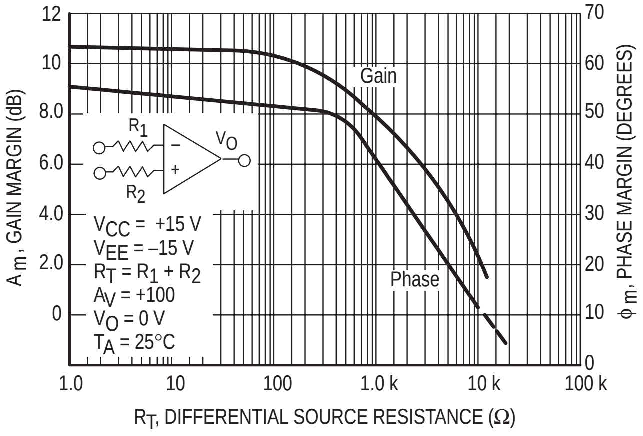


Figure 27. Normalized Slew Rate versus Temperature

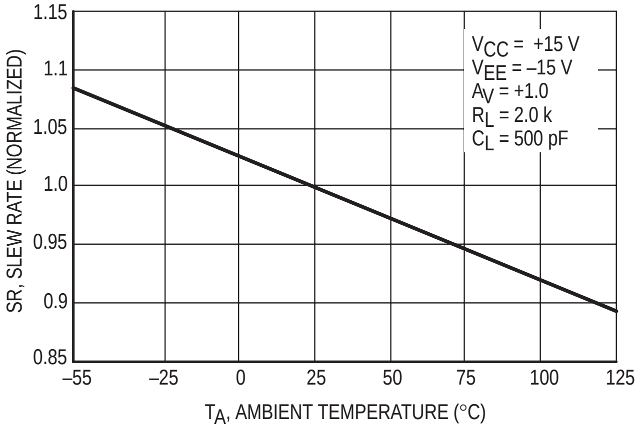


Figure 28. Output Settling Time

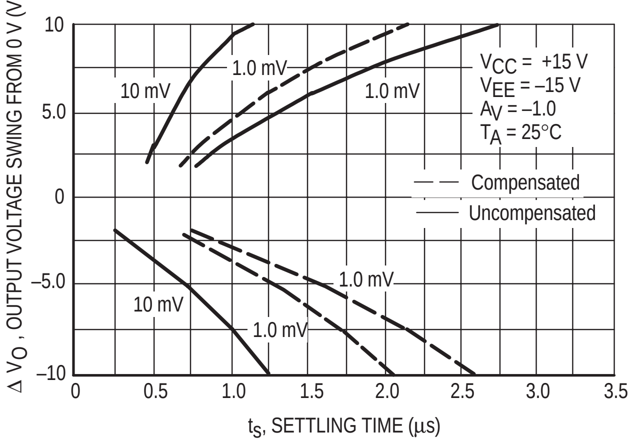


Figure 29. Small Signal Transient Response

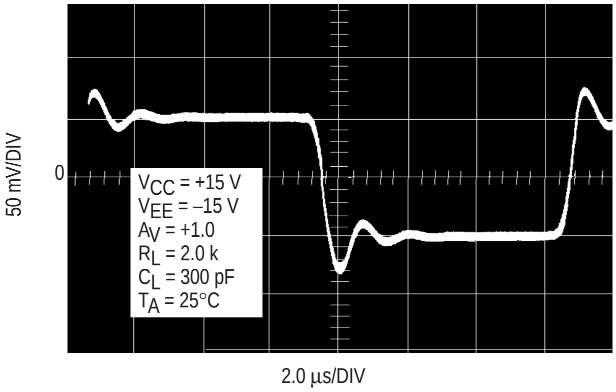


Figure 30. Large Signal Transient Reponse

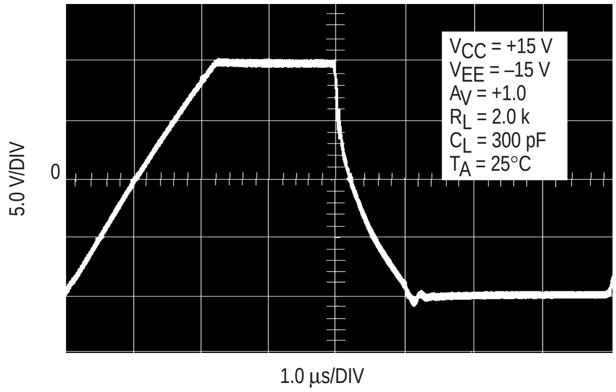


Figure 31. Common Mode Rejection versus Frequency

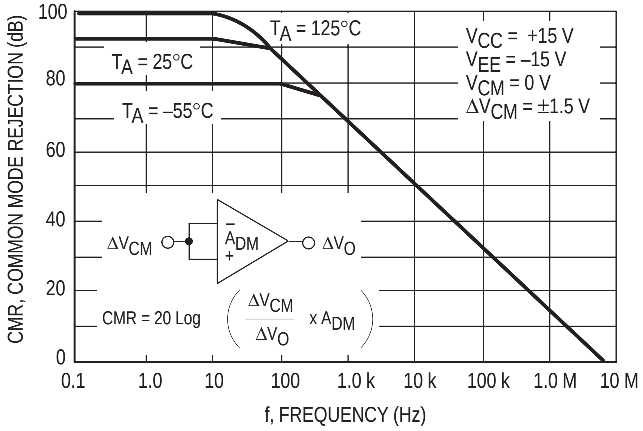


Figure 32. Power Supply Rejection versus Frequency

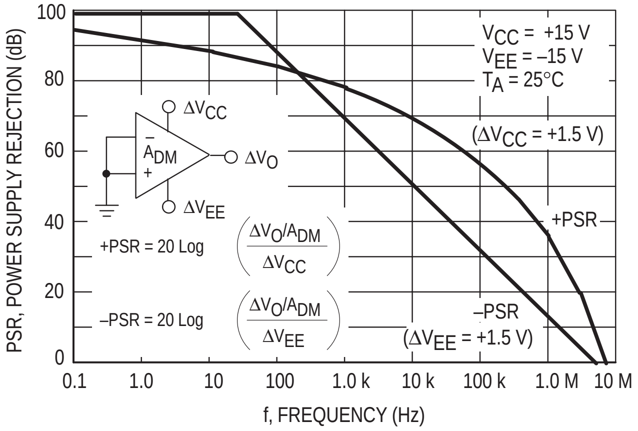


Figure 33. Supply Current versus Supply Voltage

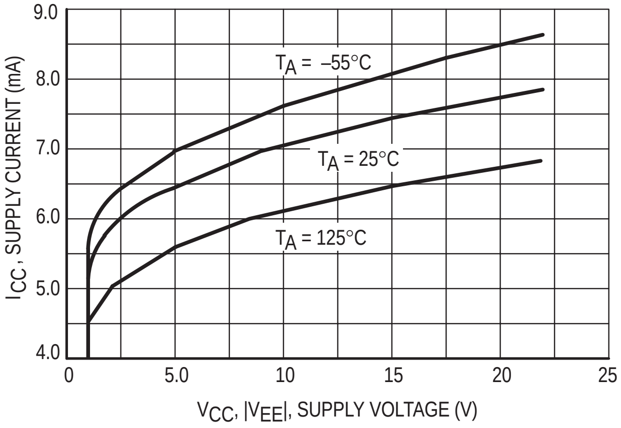


Figure 34. Power Supply Rejection versus Temperature

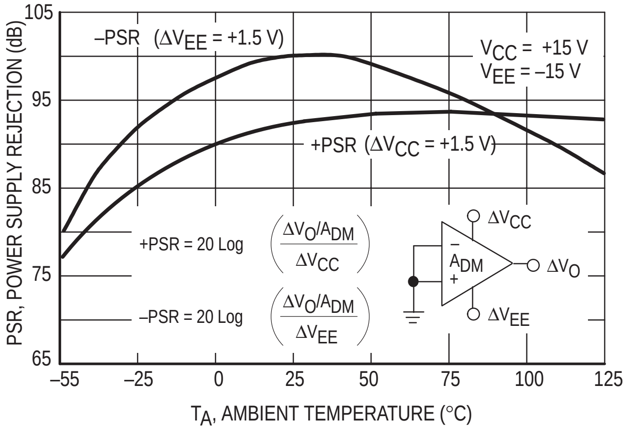


Figure 35. Channel Separation versus Frequency

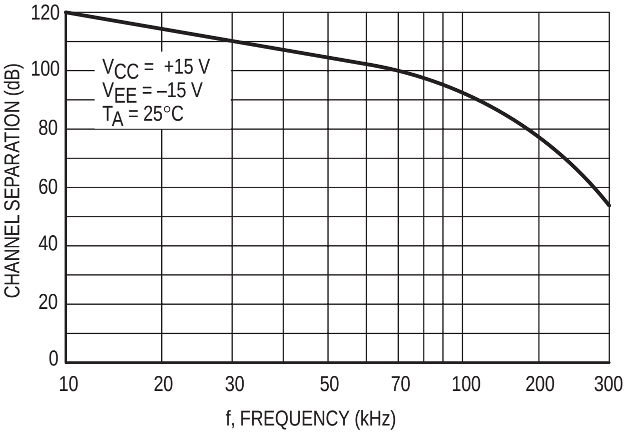
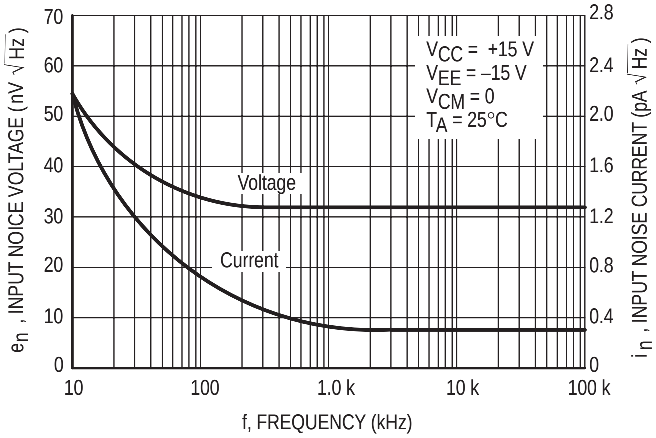


Figure 36. Input Noise versus Frequency



APPLICATIONS INFORMATION
CIRCUIT DESCRIPTION/PERFORMANCE FEATURES

Although the bandwidth, slew rate, and settling time of the MC34071 amplifier series are similar to op amp products utilizing JFET input devices, these amplifiers offer other additional distinct advantages as a result of the PNP transistor differential input stage and an all NPN transistor output stage.

Since the input common mode voltage range of this input stage includes the V_{EE} potential, single supply operation is feasible to as low as 3.0 V with the common mode input voltage at ground potential.

The input stage also allows differential input voltages up to ±44 V, provided the maximum input voltage range is not exceeded. Specifically, the input voltages must range between V_{EE} and V_{CC} supply voltages as shown by the maximum rating table. In practice, although not recommended, the input voltages can exceed the V_{CC} voltage by approximately 3.0 V and decrease below the V_{EE} voltage by 0.3 V without causing product damage, although output phase reversal may occur. It is also possible to source up to approximately 5.0 mA of current from V_{EE} through either inputs clamping diode without damage or latching, although phase reversal may again occur.

If one or both inputs exceed the upper common mode voltage limit, the amplifier output is readily predictable and may be in a low or high state depending on the existing input bias conditions.

Since the input capacitance associated with the small geometry input device is substantially lower (2.5 pF) than the typical JFET input gate capacitance (5.0 pF), better frequency response for a given input source resistance can be achieved using the MC34071 series of amplifiers. This performance feature becomes evident, for example, in fast settling D–to–A current to voltage conversion applications where the feedback resistance can form an input pole with the input capacitance of the op amp. This input pole creates a 2nd order system with the single pole op amp and is therefore detrimental to its settling time. In this context, lower input capacitance is desirable especially for higher values of feedback resistances (lower current DACs). This input pole can be compensated for by creating a feedback zero with a capacitance across the feedback resistance, if necessary, to reduce overshoot. For 2.0 kΩ of feedback resistance, the MC34071 series can settle to within 1/2 LSB of 8 bits in 1.0 µs, and within 1/2 LSB of 12–bits in 2.2 µs for a 10 V step. In a inverting unity gain fast settling configuration, the symmetrical slew rate is ±13 V/µs. In the classic noninverting unity gain configuration, the output positive slew rate is +10 V/µs, and the corresponding negative slew rate will exceed the positive slew rate as a function of the fall time of the input waveform.

Since the bipolar input device matching characteristics are superior to that of JFETs, a low untrimmed maximum offset voltage of 3.0 mV prime and 5.0 mV downgrade can be economically offered with high frequency performance characteristics. This combination is ideal for low cost precision, high speed quad op amp applications.

The all NPN output stage, shown in its basic form on the equivalent circuit schematic, offers unique advantages over the more conventional NPN/PNP transistor Class AB output stage. A 10 kΩ load resistance can swing within 1.0 V of the positive rail (V_{CC}), and within 0.3 V of the negative rail (V_{EE}), providing a 28.7 V_{pp} swing from ±15 V supplies. This large output swing becomes most noticeable at lower supply voltages.

The positive swing is limited by the saturation voltage of the current source transistor Q_7, and V_{BE} of the NPN pull up transistor Q_{17}, and the voltage drop associated with the short circuit resistance, R_7. The negative swing is limited by the saturation voltage of the pull–down transistor Q_{16}, the voltage drop I_LR_6, and the voltage drop associated with resistance R_7, where I_L is the sink load current. For small valued sink currents, the above voltage drops are negligible, allowing the negative swing voltage to approach within millivolts of V_{EE}. For large valued sink currents (>5.0 mA), diode D3 clamps the voltage across R_6, thus limiting the negative swing to the saturation voltage of Q_{16}, plus the forward diode drop of D3 ($\approx V_{EE}$ +1.0 V). Thus for a given supply voltage, unprecedented peak–to–peak output voltage swing is possible as indicated by the output swing specifications.

If the load resistance is referenced to V_{CC} instead of ground for single supply applications, the maximum possible output swing can be achieved for a given supply voltage. For light load currents, the load resistance will pull the output to V_{CC} during the positive swing and the output will pull the load resistance near ground during the negative swing. The load resistance value should be much less than that of the feedback resistance to maximize pull up capability.

Because the PNP output emitter–follower transistor has been eliminated, the MC34071 series offers a 20 mA minimum current sink capability, typically to an output voltage of (V_{EE} +1.8 V). In single supply applications the output can directly source or sink base current from a common emitter NPN transistor for fast high current switching applications.

In addition, the all NPN transistor output stage is inherently fast, contributing to the bipolar amplifier's high gain bandwidth product and fast settling capability. The associated high frequency low output impedance (30 Ω typ @ 1.0 MHz) allows capacitive drive capability from 0 pF to 10,000 pF without oscillation in the unity closed loop gain configuration. The 60° phase margin and 12 dB gain margin as well as the general gain and phase characteristics are virtually independent of the source/sink output swing conditions. This allows easier system phase compensation, since output swing will not be a phase consideration. The high frequency characteristics of the MC34071 series also allow excellent high frequency active filter capability, especially for low voltage single supply applications.

Although the single supply specifications is defined at 5.0 V, these amplifiers are functional to 3.0 V @ 25°C although slight changes in parametrics such as bandwidth, slew rate, and DC gain may occur.

If power to this integrated circuit is applied in reverse polarity or if the IC is installed backwards in a socket, large unlimited current surges will occur through the device that may result in device destruction.

Special static precautions are not necessary for these bipolar amplifiers since there are no MOS transistors on the die.

As with most high frequency amplifiers, proper lead dress, component placement, and PC board layout should be exercised for optimum frequency performance. For example, long unshielded input or output leads may result in unwanted input–output coupling. In order to preserve the relatively low input capacitance associated with these amplifiers, resistors connected to the inputs should be immediately adjacent to the input pin to minimize additional stray input capacitance. This not only minimizes the input pole for optimum frequency response, but also minimizes extraneous “pick up” at this node. Supply decoupling with adequate capacitance immediately adjacent to the supply pin is also important, particularly over temperature, since many types of decoupling capacitors exhibit great impedance changes over temperature.

The output of any one amplifier is current limited and thus protected from a direct short to ground. However, under such conditions, it is important not to allow the device to exceed the maximum junction temperature rating. Typically for ±15 V supplies, any one output can be shorted continuously to ground without exceeding the maximum temperature rating.

(Typical Single Supply Applications V_{CC} = 5.0 V)

Figure 37. AC Coupled Noninverting Amplifer

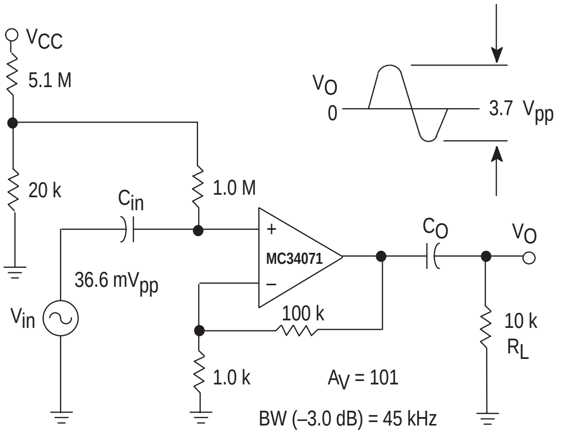


Figure 39. DC Coupled Inverting Amplifer Maximum Output Swing

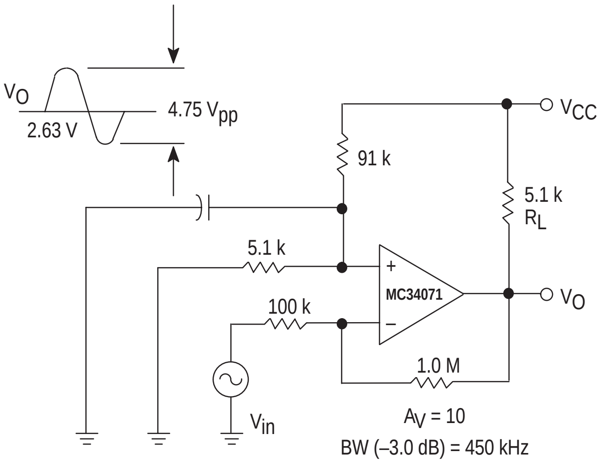


Figure 41. Active High–Q Notch Filter

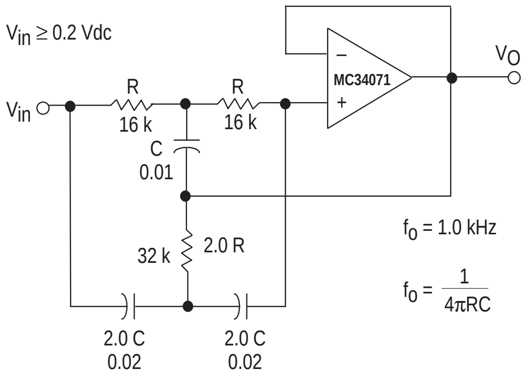


Figure 38. AC Coupled Inverting Amplifier

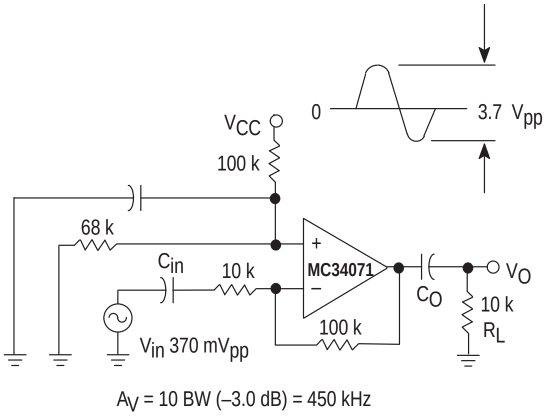


Figure 40. Unity Gain Buffer TTL Driver

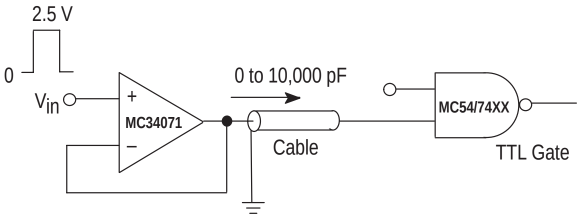
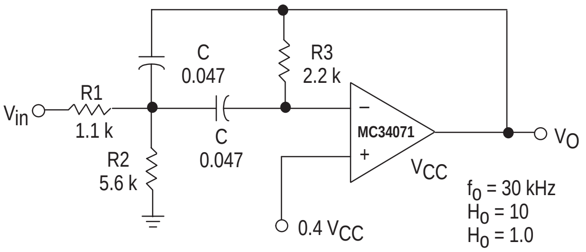


Figure 42. Active Bandpass Filter



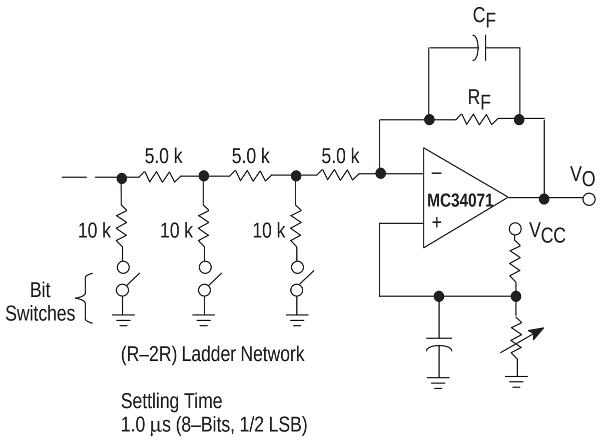
Given f_0 = Center Frequency
A_O = Gain at Center Frequency
Choose Value f_0, Q, A_0, C

Then:
$R3 = \frac{Q}{\pi f_0 C}$ $R1 = \frac{R3}{2H_0}$ $R2 = \frac{R1\,R3}{4Q^2R1-R3}$

For less than 10% error from operational amplifier $\frac{Q_0 f_0}{GBW} < 0.1$

where f_0 and GBW are expressed in Hz.
GBW = 4.5 MHz Typ.

Figure 43. Low Voltage Fast D/A Converter



(R–2R) Ladder Network

Settling Time
1.0 µs (8–Bits, 1/2 LSB)

Figure 44. High Speed Low Voltage Comparator

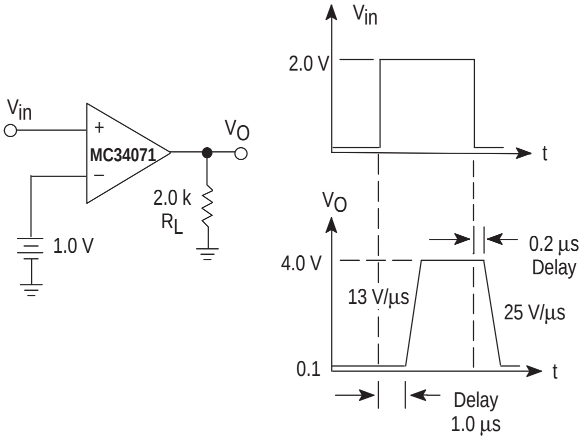


Figure 45. LED Driver

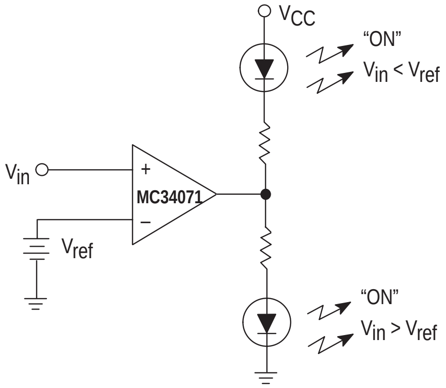
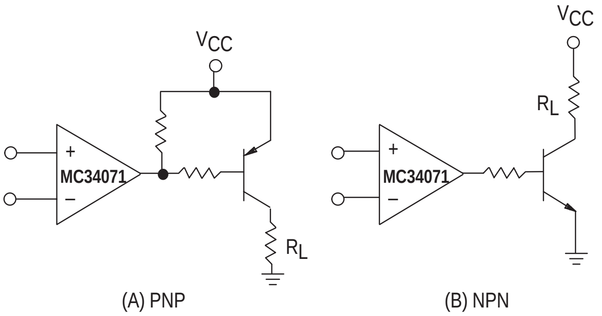


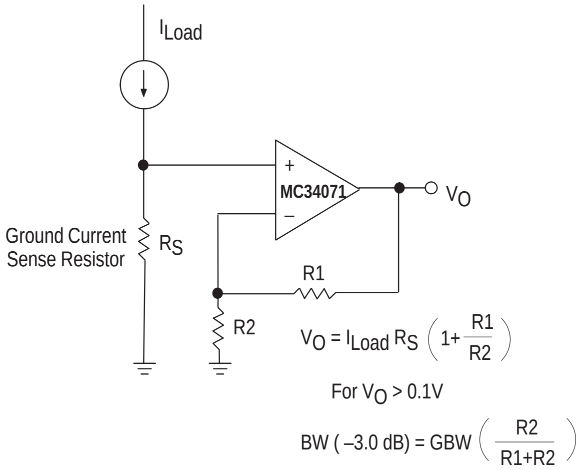
Figure 46. Transistor Driver



(A) PNP

(B) NPN

Figure 47. AC/DC Ground Current Monitor

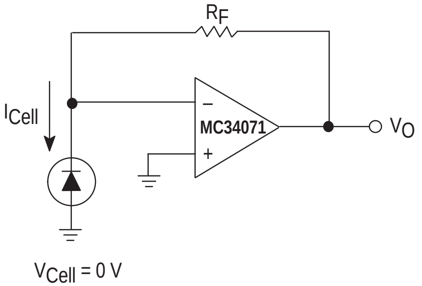


$$V_O = I_{Load}\, R_S \left(1 + \frac{R1}{R2}\right)$$

For $V_O > 0.1V$

$$BW\ (-3.0\ dB) = GBW \left(\frac{R2}{R1+R2}\right)$$

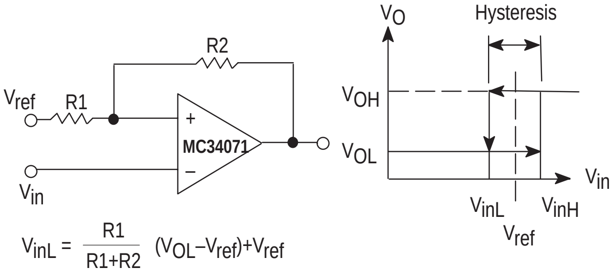
Figure 48. Photovoltaic Cell Amplifier



$V_{Cell} = 0\ V$

$V_O = I_{Cell}\, R_F$
$V_O > 0.1\ V$

Figure 49. Low Input Voltage Comparator with Hysteresis

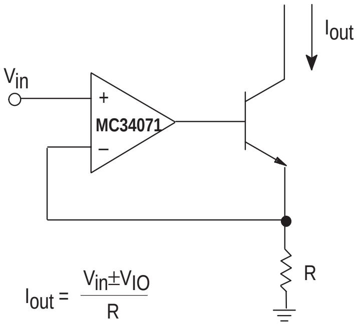


$$V_{inL} = \frac{R1}{R1+R2}(V_{OL}-V_{ref})+V_{ref}$$

$$V_{inH} = \frac{R1}{R1+R2}(V_{OH}-V_{ref})+V_{ref}$$

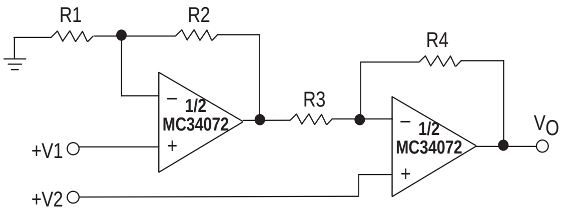
$$V_H = \frac{R1}{R1+R}(V_{OH}-V_{OL})$$

Figure 50. High Compliance Voltage to Sink Current Converter



$$I_{out} = \frac{V_{in} \pm V_{IO}}{R}$$

Figure 51. High Input Impedance Differential Amplifier

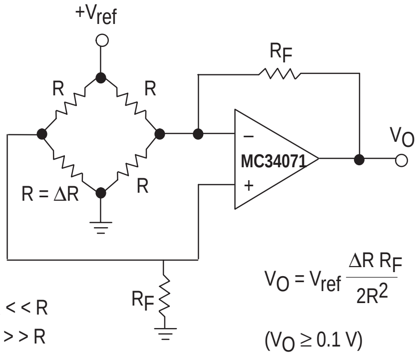


$$\frac{R2}{R1} = \frac{R4}{R3} \text{ (Critical to CMRR)}$$

$$V_O = 1\left(+\frac{R4}{R3}\right)\left(V2-V1\ \frac{R4}{R3}\right)$$

For $(V2 \geq V1), V > 0$

Figure 52. Bridge Current Amplifier



$\Delta R << R$

$R_F >> R$

$$V_O = V_{ref}\frac{\Delta R\ R_F}{2R^2}$$

$(V_O \geq 0.1\text{ V})$

Figure 53. Low Voltage Peak Detector

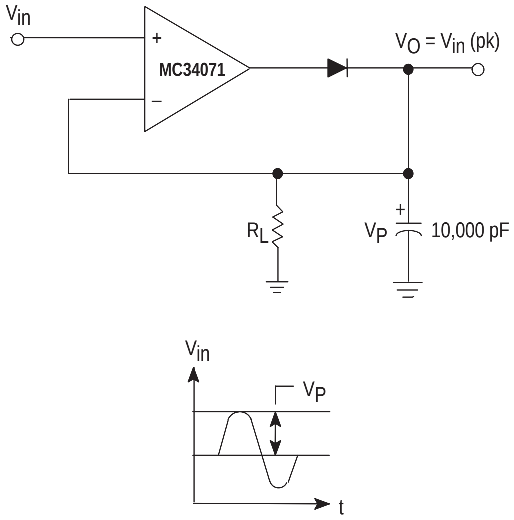
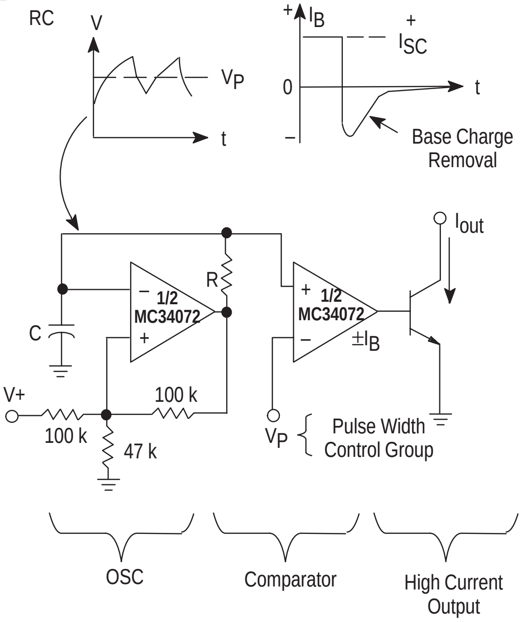


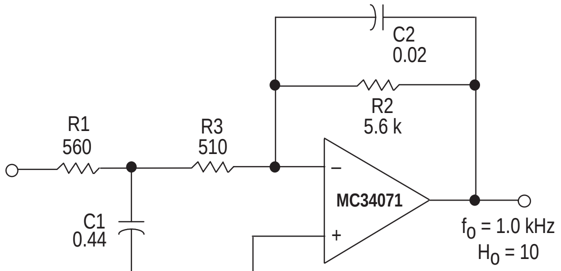
Figure 54. High Frequency Pulse Width Modulation

$$f_{OSC} \cong \frac{0.85}{RC}$$



GENERAL ADDITIONAL APPLICATIONS INFORMATION $V_S = \pm 15.0$ V

Figure 55. Second Order Low–Pass Active Filter

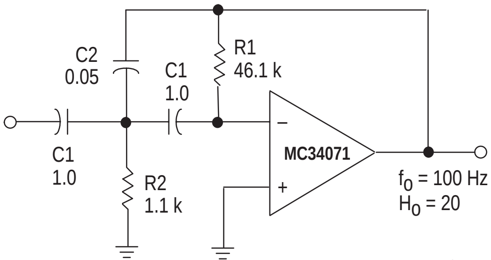


Choose: f_O, H_O, C2

Then: $C1 = 2C2\,(H_O+1)$

$R2 = \frac{\sqrt{2}}{4\pi f_O C2}$ $R3 = \frac{R2}{H_O+1}$ $R1 = \frac{R2}{H_O}$

Figure 56. Second Order High–Pass Active Filter



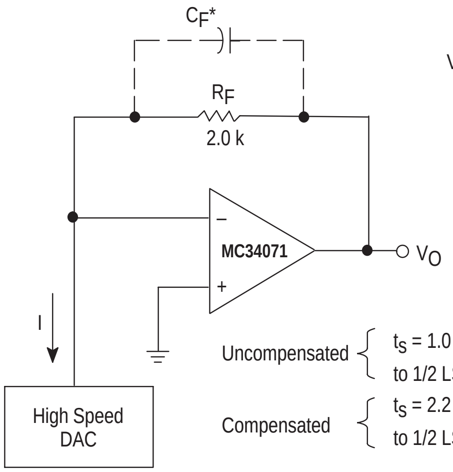
Choose: f_O, H_O, C1

Then: $R1 = \frac{H_O+0.5}{\pi f_O C1 \sqrt{2}}$

$R2 = \frac{\sqrt{2}}{2\pi f_O C1\,(1/H_O+2)}$

$C2 = \frac{C}{H_O}$

Figure 57. Fast Settling Inverter



V_O = 10 V
Step

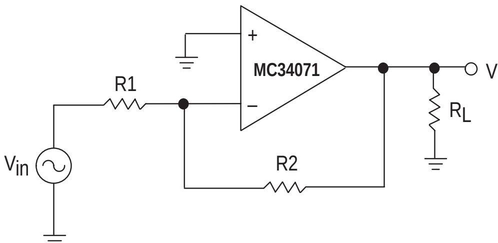
Uncompensated { t_s = 1.0 µs
to 1/2 LSB (8–Bits)

Compensated { t_s = 2.2 µs
to 1/2 LSB (12–Bits)

SR = 13 V/µs

*Optional Compensation

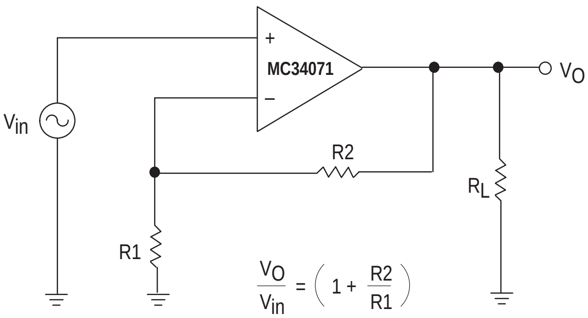
Figure 58. Basic Inverting Amplifier



$\frac{V_O}{V_{in}} = \frac{R2}{R1}$ BW (–3.0 dB) = GBW $\left[\frac{R1}{R1+R2}\right]$

SR = 13 V/µs

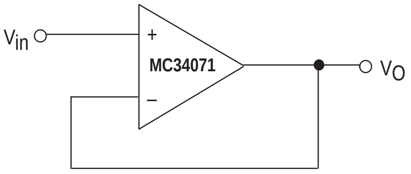
Figure 59. Basic Noninverting Amplifier



$\frac{V_O}{V_{in}} = \left(1 + \frac{R2}{R1}\right)$

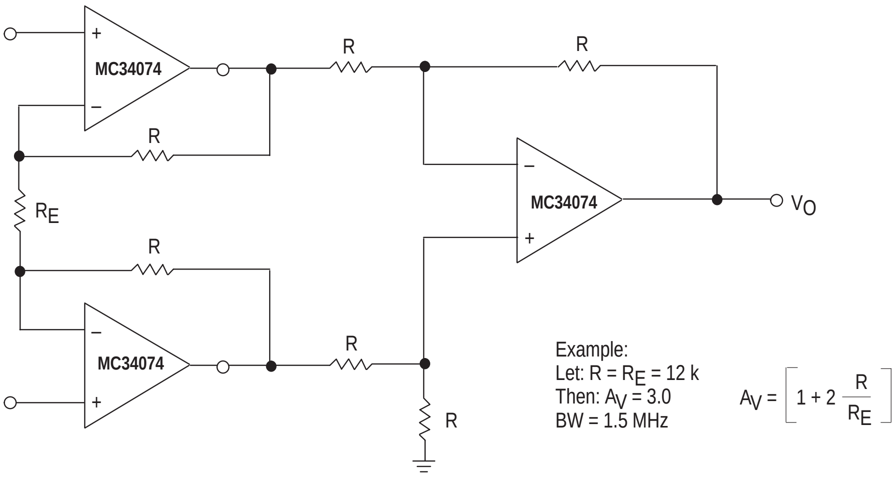
BW (–3.0 dB) = GBW $\left[\frac{R1}{R1+R2}\right]$

Figure 60. Unity Gain Buffer (A_V = +1.0)



BW_p = 200 kHz
V_O = 20 V_{pp}
SR = 10 V/µs

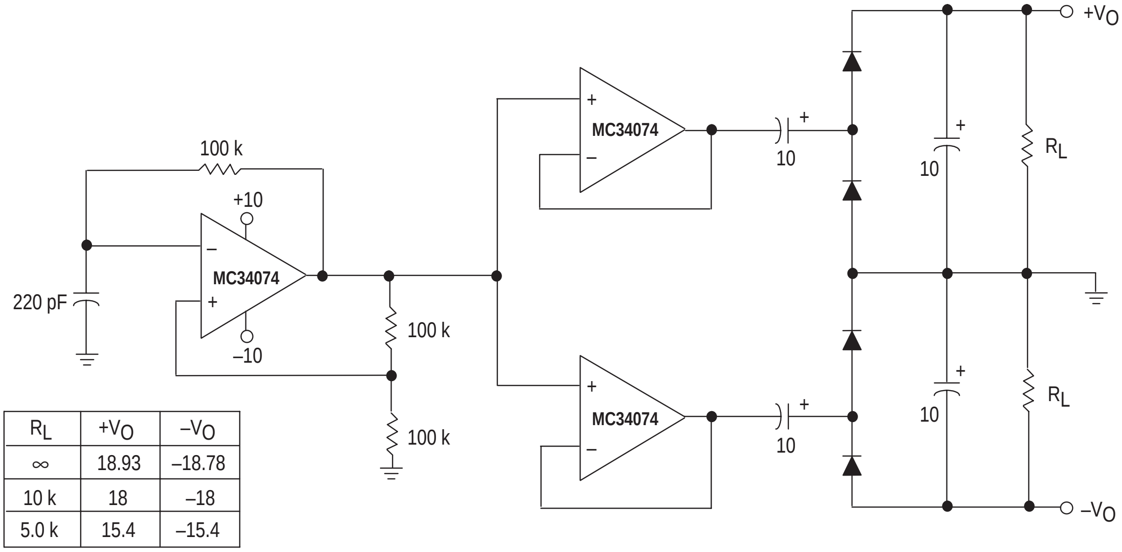
Figure 61. High Impedance Differential Amplifier



Example:
Let: $R = R_E = 12$ k
Then: $A_V = 3.0$
BW = 1.5 MHz

$$A_V = \left[1 + 2\frac{R}{R_E}\right]$$

Figure 62. Dual Voltage Doubler



R_L	$+V_O$	$-V_O$
∞	18.93	–18.78
10 k	18	–18
5.0 k	15.4	–15.4

MOTOROLA

High Slew Rate, Wide Bandwidth, JFET Input Operational Amplifiers

These devices are a new generation of high speed JFET input monolithic operational amplifiers. Innovative design concepts along with JFET technology provide wide gain bandwidth product and high slew rate. Well–matched JFET input devices and advanced trim techniques ensure low input offset errors and bias currents. The all NPN output stage features large output voltage swing, no deadband crossover distortion, high capacitive drive capability, excellent phase and gain margins, low open loop output impedance, and symmetrical source/sink AC frequency response.

This series of devices is available in fully compensated or decompensated ($A_{VCL} \leq 2$) and is specified over a commercial temperature range. They are pin compatible with existing Industry standard operational amplifiers, and allow the designer to easily upgrade the performance of existing designs.

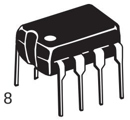
- Wide Gain Bandwidth: 8.0 MHz for Fully Compensated Devices
  16 MHz for Decompensated Devices
- High Slew Rate: 25 V/μs for Fully Compensated Devices
  50 V/μs for Decompensated Devices
- High Input Impedance: $10^{12}\Omega$
- Input Offset Voltage: 0.5 mV Maximum (Single Amplifier)
- Large Output Voltage Swing: –14.7 V to +14 V for $V_{CC}/V_{EE} = \pm15$ V
- Low Open Loop Output Impedance: 30 Ω @ 1.0 MHz
- Low THD Distortion: 0.01%
- Excellent Phase/Gain Margins: 55°/7.6 dB for Fully Compensated Devices

ORDERING INFORMATION

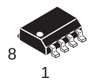
Op Amp Function	Fully Compensated	$A_{VCL} \geq 2$ Compensated	Operating Temperature Range	Package
Single	MC34081BD	MC34080BD	T_A = 0° to +70°C	SO–8
	MC34081BP	MC34080BP		Plastic DIP
Dual	MC34082P	MC34083BP		Plastic DIP
Quad	MC34084DW	MC34085BDW	T_A = 0° to +70°C	SO–16L
	MC34084P	MC34085BP		Plastic DIP

MC34080 thru MC34085

HIGH PERFORMANCE JFET INPUT OPERATIONAL AMPLIFIERS

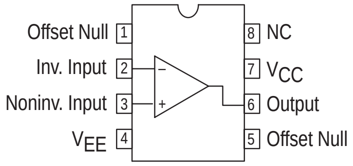


P SUFFIX
PLASTIC PACKAGE
CASE 626

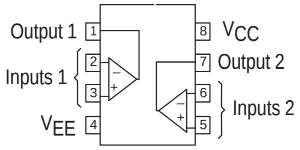


D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

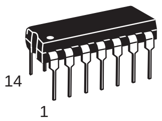
PIN CONNECTIONS



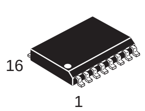
(Single, Top View)



(Dual, Top View)

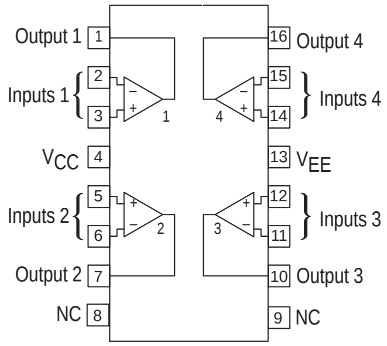


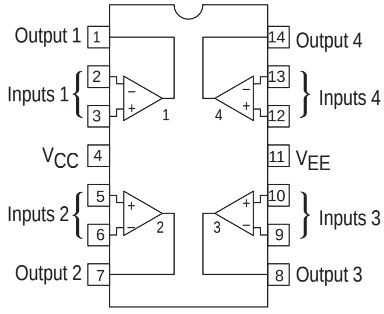
P SUFFIX
PLASTIC PACKAGE
CASE 646



DW SUFFIX
PLASTIC PACKAGE
CASE 751G
(SO–16L)

PIN CONNECTIONS





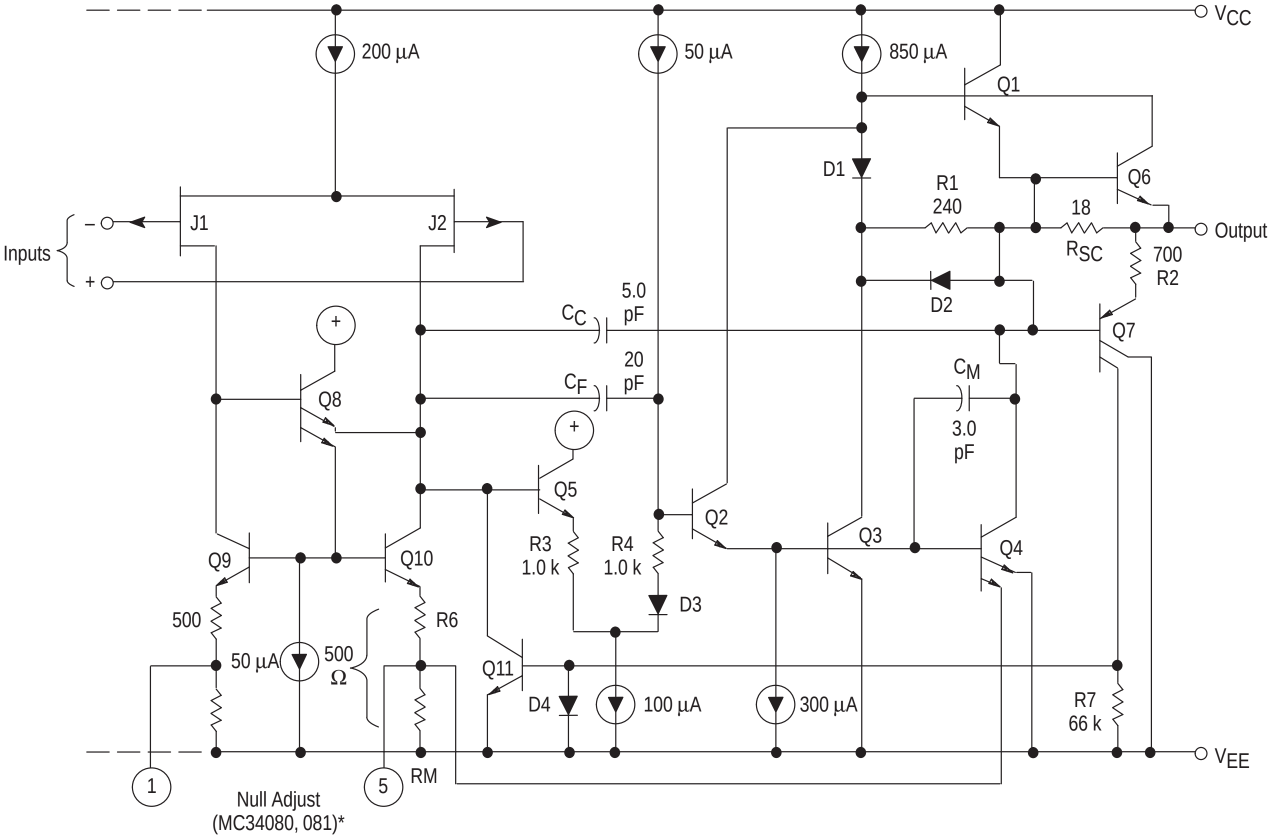
(Quad, Top View)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage (from V_{CC} to V_{EE})	V_S	+44	V
Input Differential Voltage Range	V_{IDR}	(Note 1)	V
Input Voltage Range	V_{IR}	(Note 1)	V
Output Short Circuit Duration (Note 2)	t_{SC}	Indefinite	sec
Operating Ambient Temperature Range	T_A	0 to +70	°C
Operating Junction Temperature	T_J	+125	°C
Storage Temperature Range	T_{stg}	– 65 to +165	°C

NOTES: 1. Either or both input voltages must not exceed the magnitude of V_{CC} or V_{EE}.
2. Power dissipation must be considered to ensure maximum junction temperature (T_J) is not exceeded.

Representative Schematic Diagram
(Each Amplifier)



*Pins 1 & 5 (MC34080,081) should *not* be directly grounded or connected to V_{CC}.

DC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = – 15 V, T_A = T_{low} to T_{high} [Note 3], unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Input Offset Voltage (Note 4)	V_{IO}				mV
Single					
T_A = +25°C		—	0.5	2.0	
T_A = 0° to +70°C (MC34080B, MC34081B)		—	—	4.0	
Dual					
T_A = +25°C		—	1.0	3.0	
T_A = 0° to +70°C (MC34082, MC34083)		—	—	5.0	
Quad					
T_A = +25°C		—	6.0	12	
T_A = 0° to +70°C (MC34084, MC34085)		—	—	14	
Average Temperature Coefficient of Offset Voltage	$\Delta V_{IO}/\Delta T$	—	10	—	µV/°C
Input Bias Current (V_{CM} = 0 Note 5)	I_{IB}				
T_A = +25°C		—	0.06	0.2	nA
T_A = 0° to +70°C		—	—	4.0	
Input Offset Current (V_{CM} = 0 Note 5)	I_{IO}				
T_A = +25°C		—	0.02	0.1	nA
T_A = 0° to +70°C		—	—	2.0	
Large Signal Voltage Gain (V_O = ±10 V, R_L = 2.0 k)	A_{VOL}				V/mV
T_A = +25°C		25	80	—	
T_A = T_{low} to T_{high}		15	—	—	
Output Voltage Swing	V_{OH}				V
R_L = 2.0 k, T_A = +25°C		13.2	13.7	—	
R_L = 10 k, T_A = +25°C		13.4	13.9	—	
R_L = 10 k, T_A = T_{low} to T_{high}		13.4	—	—	
R_L = 2.0 k, T_A = +25°C	V_{OL}	—	–14.1	–13.5	
R_L = 10 k, T_A = +25°C		—	–14.7	–14.1	
R_L = 10 k, T_A = T_{low} to T_{high}		—	—	–14.0	
Output Short Circuit Current (T_A = +25°C)	I_{SC}				mA
Input Overdrive = 1.0 V, Output to Ground					
Source		20	31	—	
Sink		20	28	—	
Input Common Mode Voltage Range T_A = +25°C	V_{ICR}	(V_{EE} +4.0) to (V_{CC} – 2.0)			V
Common Mode Rejection Ratio (R_S ≤ 10 k, T_A = +25°C)	CMRR	70	90	—	dB
Power Supply Rejection Ratio (R_S = 100 Ω, T_A = 25°C)	PSRR	70	86	—	dB
Power Supply Current	I_D				mA
Single					
T_A = +25°C		—	2.5	3.4	
T_A = T_{low} to T_{high}		—	—	4.2	
Dual					
T_A = +25°C		—	4.9	6.0	
T_A = T_{low} to T_{high}		—	—	7.5	
Quad					
T_A = +25°C		—	9.7	11	
T_A = T_{low} to T_{high}		—	—	13	

NOTES: (continued)

3. T_{low} = 0°C for MC34080B, MC34081B, MC34084, MC34085 — T_{high} = +70°C for MC34080B, MC34081B, MC34084, MC34085

3. T_{low} =	0°C for	MC34080B	T_{high} =	+70°C for	MC34080B
		MC34081B			MC34081B
		MC34084			MC34084
		MC34085			MC34085

4. See application information for typical changes in input offset voltage due to solderability and temperature cycling.
5. Limits at T_A = +25°C are guaranteed by high temperature (T_{high}) testing.

AC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = – 15 V, T_A = +25°C, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Slew Rate (V_{in} = –10 V to +10 V, R_L = 2.0 kΩ, C_L = 100 pF) Compensated A_V = +1.0 A_V = –1.0 Decompensated A_V = +2.0 A_V = –1.0	SR	 20 — 35 —	 25 30 50 50	 — — — —	V/µs
Settling Time (10 V Step, A_V = –1.0) To 0.10% (±1/2 LSB of 9–Bits) To 0.01% (±1/2 LSB of 12–Bits)	t_s	 — —	 0.72 1.6	 — —	µs
Gain Bandwidth Product (f = 200 kHz) Compensated Decompensated	GBW	 6.0 12	 8.0 16	 — —	MHz
Power Bandwidth (R_L = 2.0 k, V_O = 20 V_{pp}, THD = 5.0%) Compensated A_V = +1.0 Decompensated A_V = – 1.0	BWp	 — —	 400 800	 — —	kHz
Phase Margin (Compensated) R_L = 2.0 k R_L = 2.0 k, C_L = 100 pF	ϕ_m	 — —	 55 39	 — —	Degrees
Gain Margin (Compensated) R_L = 2.0 k R_L = 2.0 k, C_L = 100 pF	A_m	 — —	 7.6 4.5	 — —	dB
Equivalent Input Noise Voltage R_S = 100 Ω, f = 1.0 kHz	e_n	—	30	—	$nV/\sqrt{Hz}$
Equivalent Input Noise Current (f = 1.0 kHz)	I_n	—	0.01	—	$pA/\sqrt{Hz}$
Input Capacitance	C_i	—	5.0	—	pF
Input Resistance	r_i	—	10^{12}	—	Ω
Total Harmonic Distortion A_V = +10, R_L = 2.0 k, 2.0 ≤ V_O ≤ 20 V_{pp}, f = 10 kHz	THD	—	0.05	—	%
Channel Separation (f = 10 kHz)	—	—	120	—	dB
Open Loop Output Impedance (f = 1.0 MHz)	Z_o	—	35	—	Ω

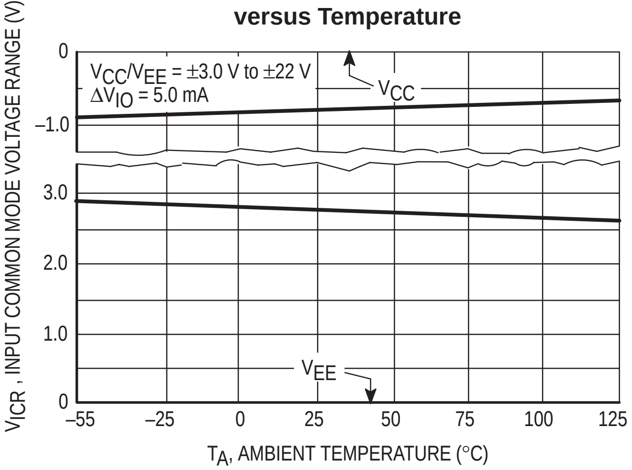


Figure 1. Input Common Mode Voltage Range versus Temperature

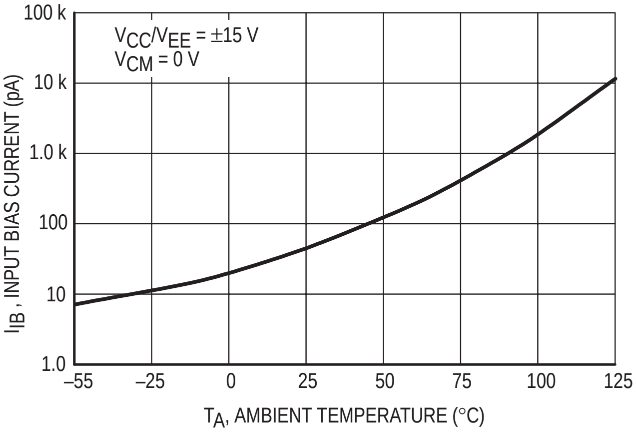


Figure 2. Input Bias Current versus Temperature

Figure 3. Input Bias Current versus Input Common Mode Voltage

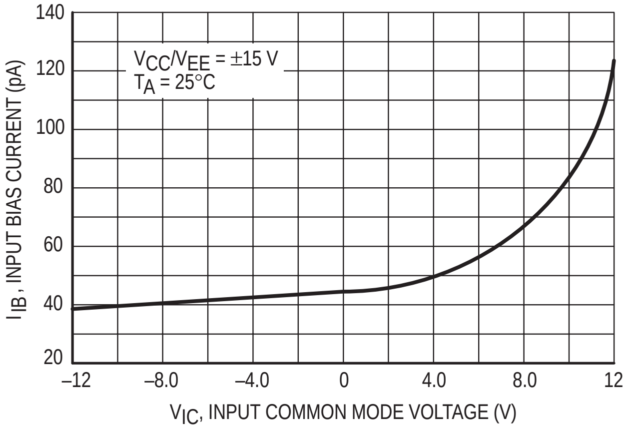


Figure 4. Output Voltage Swing versus Supply Voltage

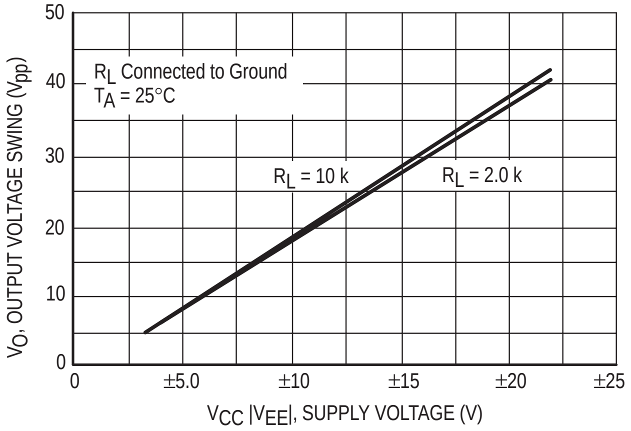


Figure 5. Output Saturation versus Load Current

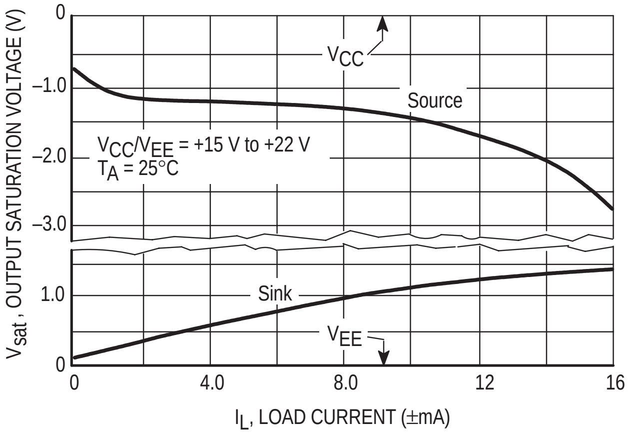


Figure 6. Output Saturation vesus Load Resistance to Ground

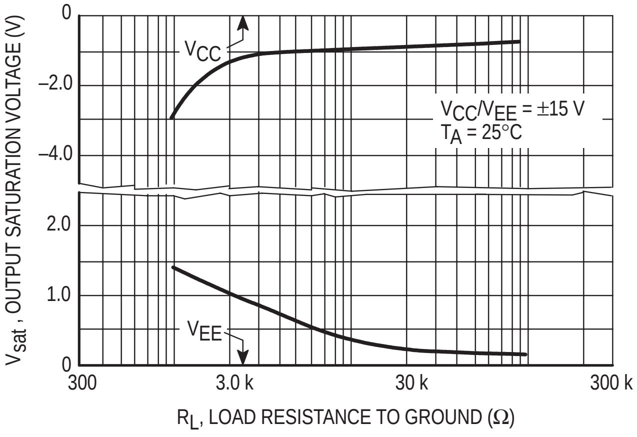


Figure 7. Output Saturation versus Load Resistance to V_{CC}

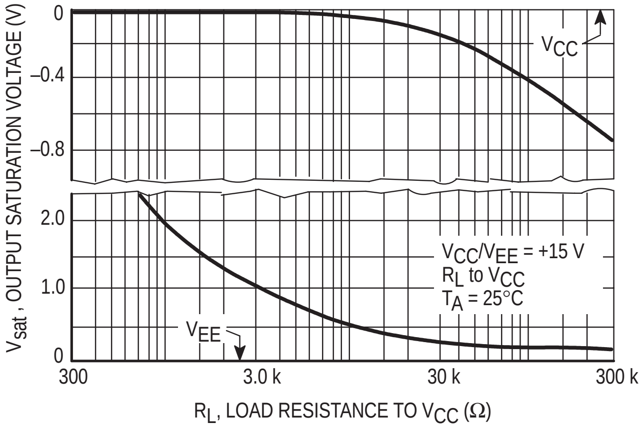


Figure 8. Output Short Circuit Current versus Temperature

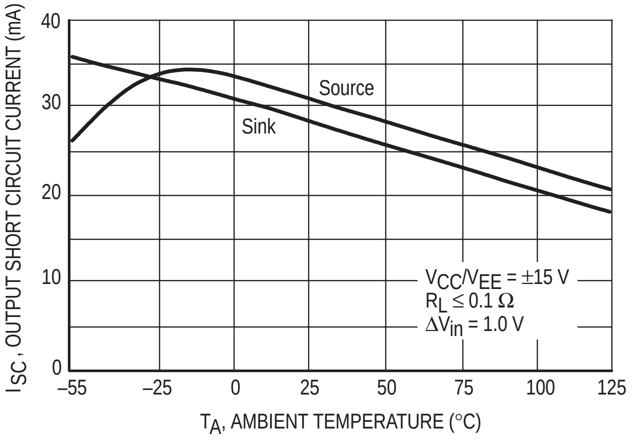


Figure 9. Output Impedance versus Frequency

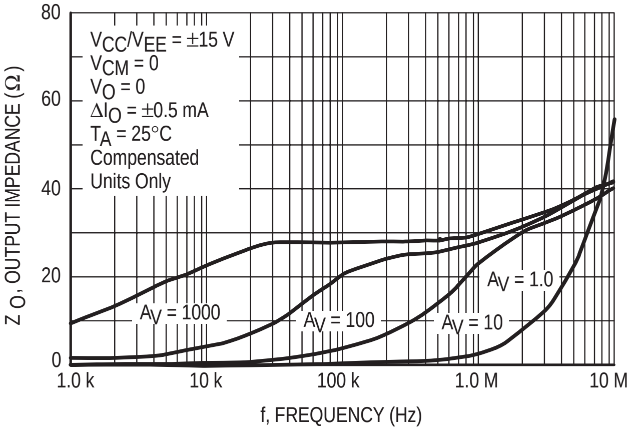


Figure 10. Output Impedance versus Frequency

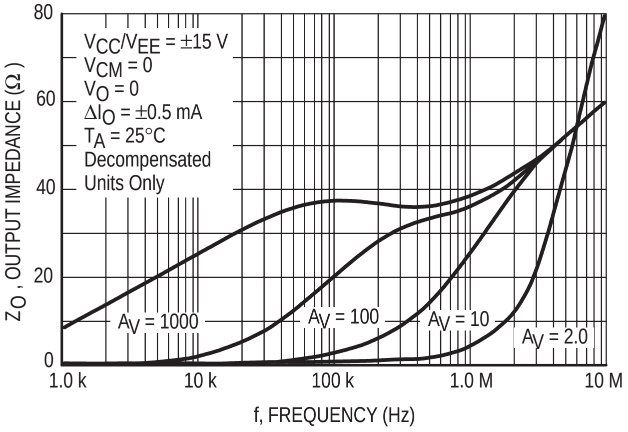


Figure 11. Output Voltage Swing versus Frequency

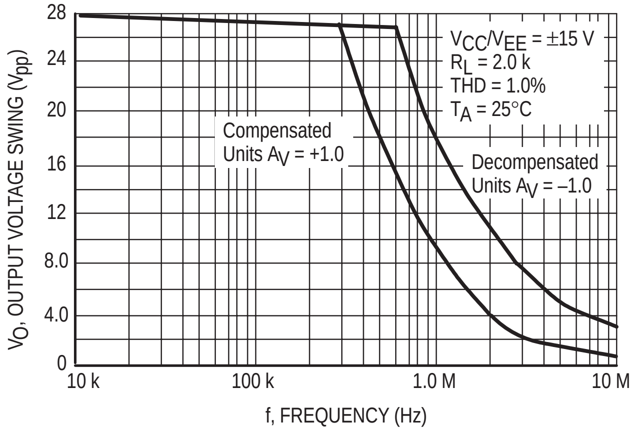


Figure 12. Output Distortion versus Frequency

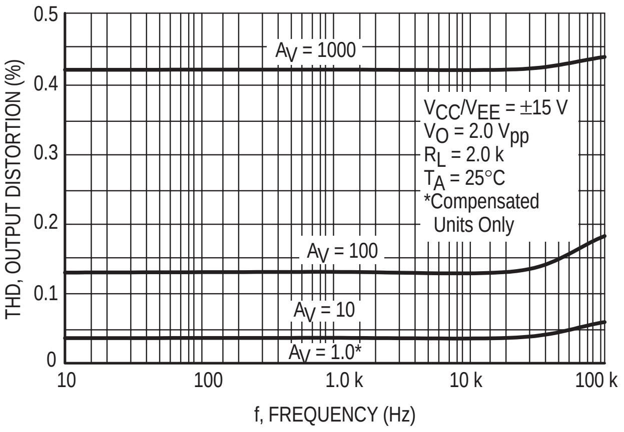


Figure 13. Open Loop Voltage Gain versus Temperature

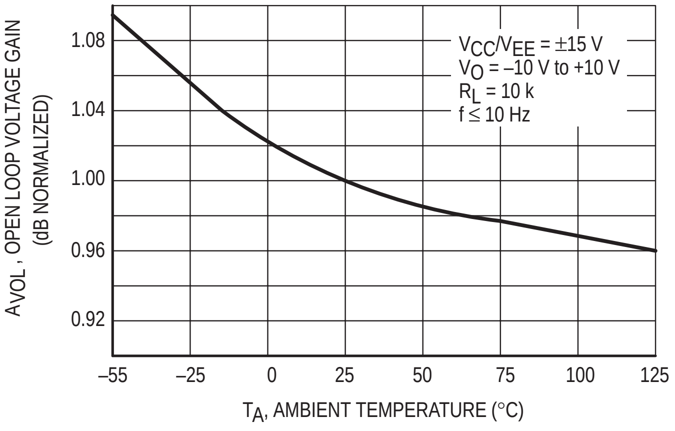


Figure 14. Open Loop Voltage Gain and Phase versus Frequency

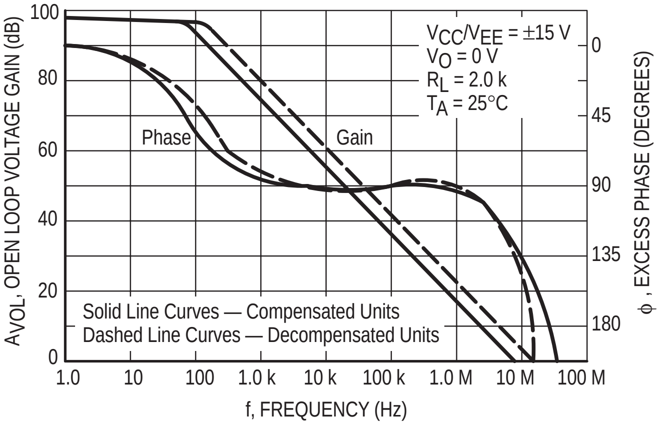


Figure 15. Open Loop Voltage Gain and Phase versus Frequency

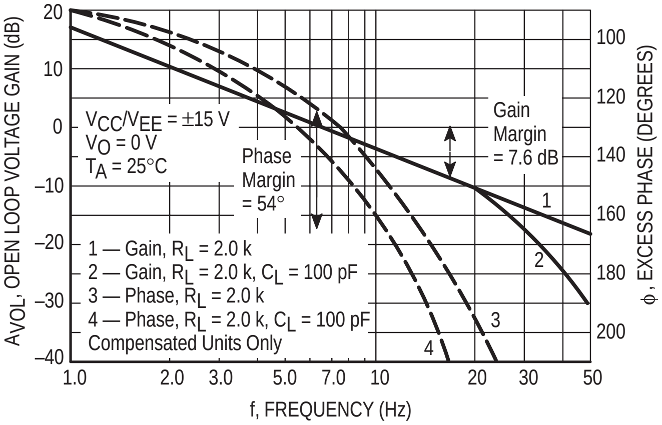


Figure 16. Open Loop Voltage Gain and Phase versus Frequency

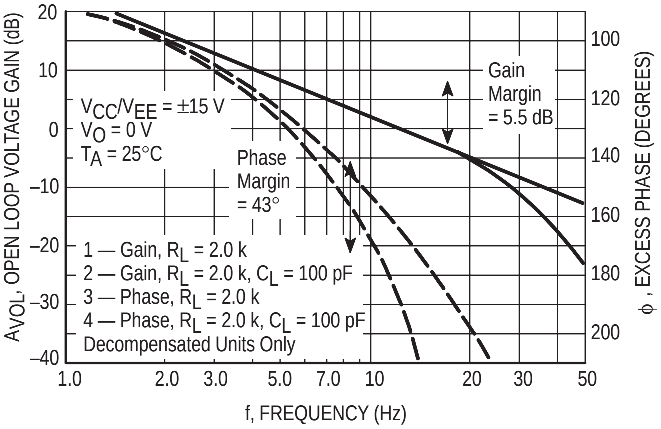


Figure 17. Normalized Gain Bandwidth Product versus Temperature

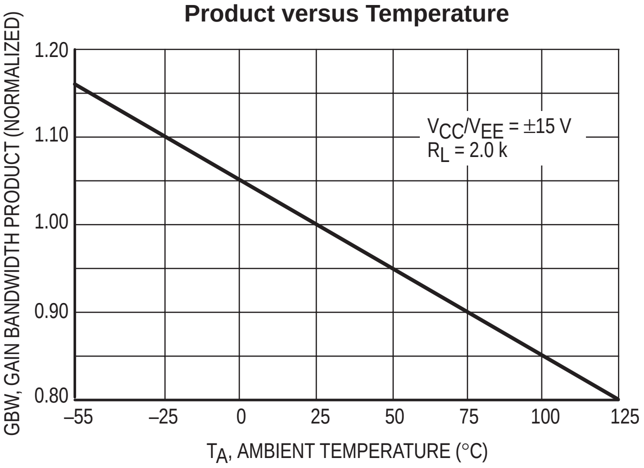


Figure 18. Percent Overshoot versus Load Capacitance

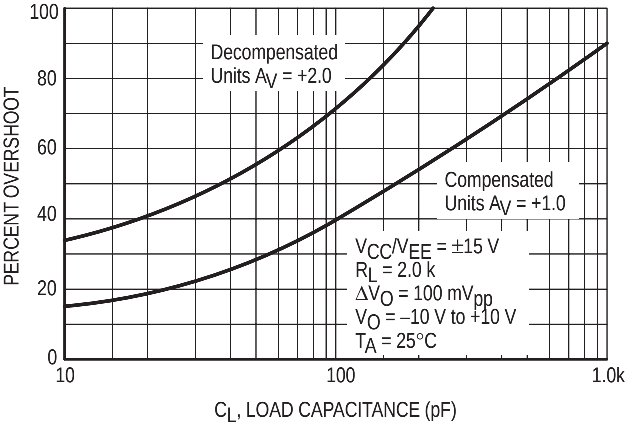


Figure 19. Phase Margin versus Load Capacitance

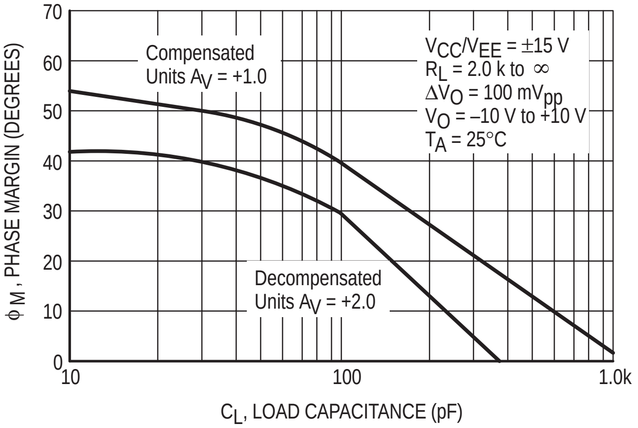


Figure 20. Gain Margin versus Load Capacitance

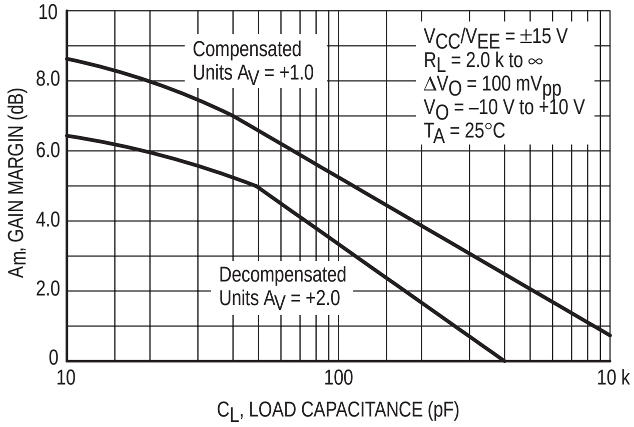


Figure 21. Phase Margin versus Temperature

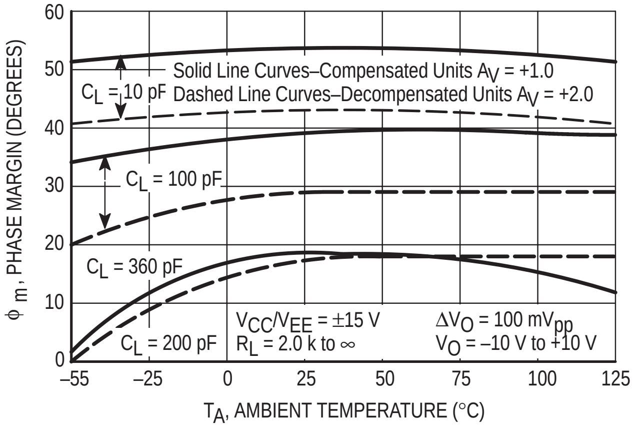


Figure 22. Gain Margin versus Temperature

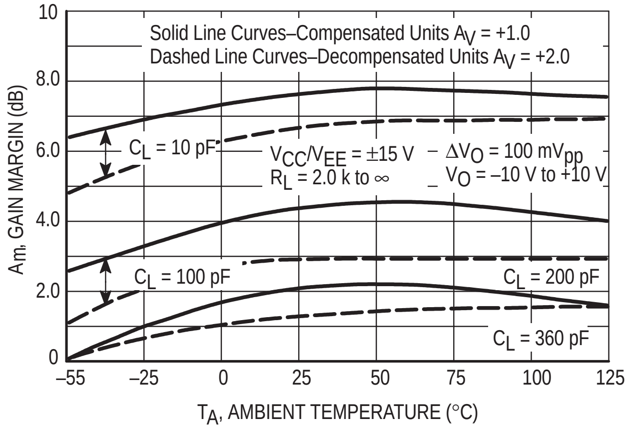
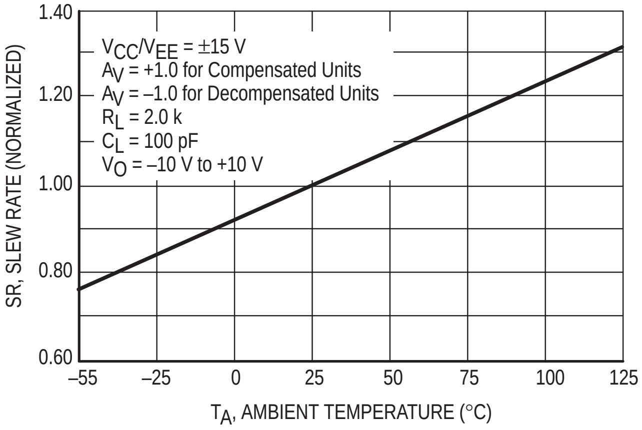


Figure 23. Normalized Slew Rate versus Temperature



MC34084 Transient Response

$A_V = +1.0$, $R_L = 2.0$ k, $V_{CC}/V_{EE} = \pm 15$ V, $T_A = 25°C$

Figure 24. Small Signal

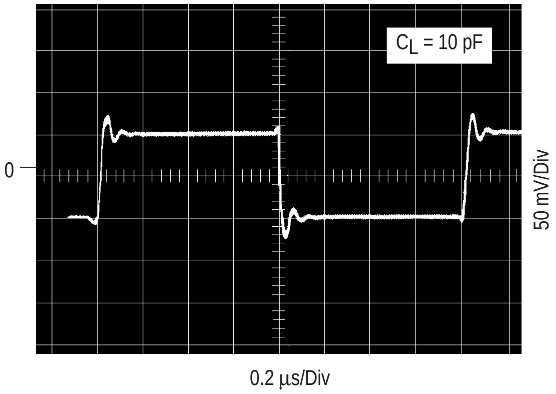
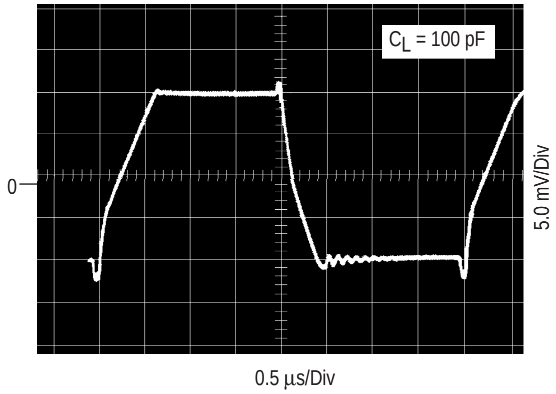


Figure 25. Large Signal



MC34085 Transient Response

$A_V = +2.0$, $R_L = 2.0$ k, $V_{CC}/V_{EE} = \pm 15$ V, $T_A = 25°C$

Figure 26. Small Signal

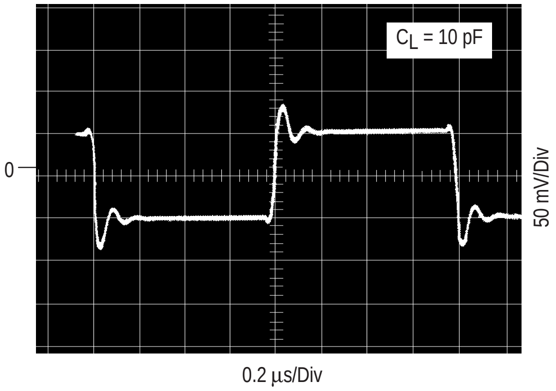


Figure 27. Large Signal

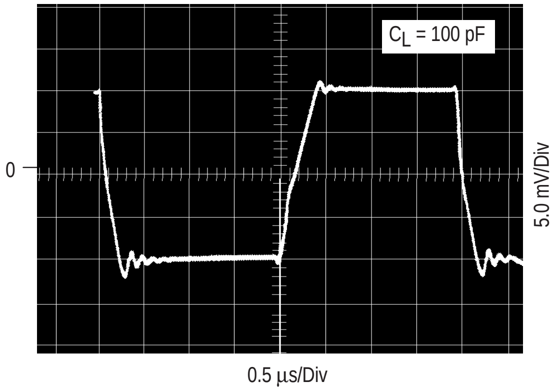


Figure 28. Common Mode Rejection Ratio versus Frequency

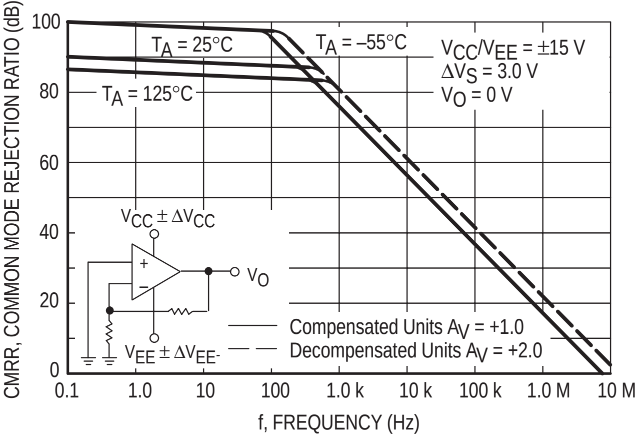


Figure 29. Power Supply Rejection Ratio versus Frequency

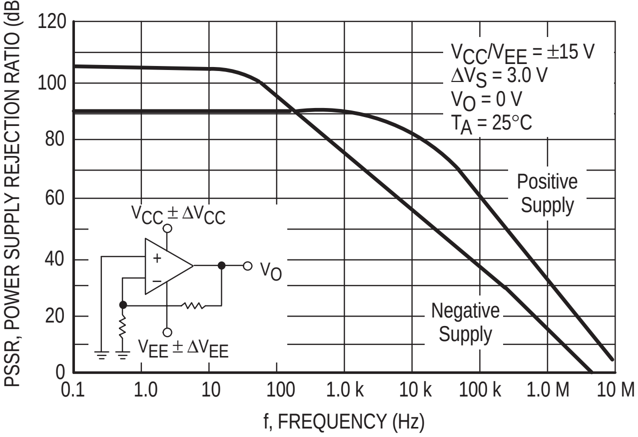


Figure 30. Power Supply Rejection Ratio versus Temperature

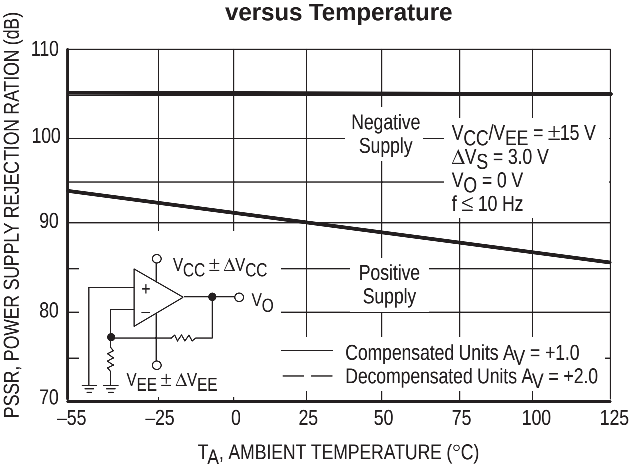


Figure 31. Normalized Supply Current versus Supply Voltage

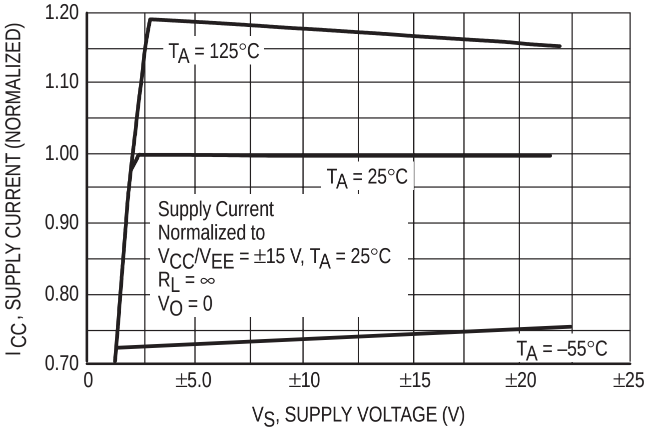


Figure 32. Channel Separation versus Frequency

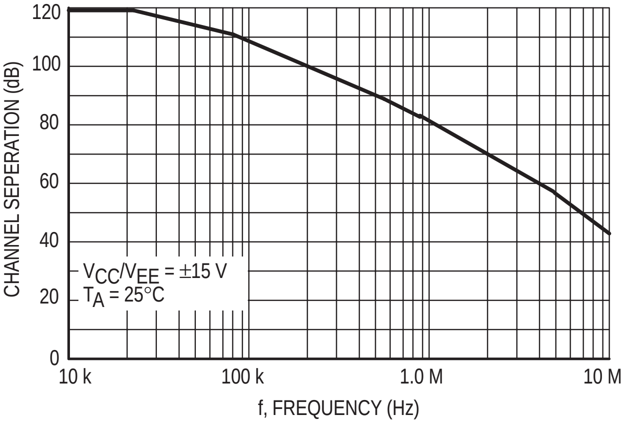
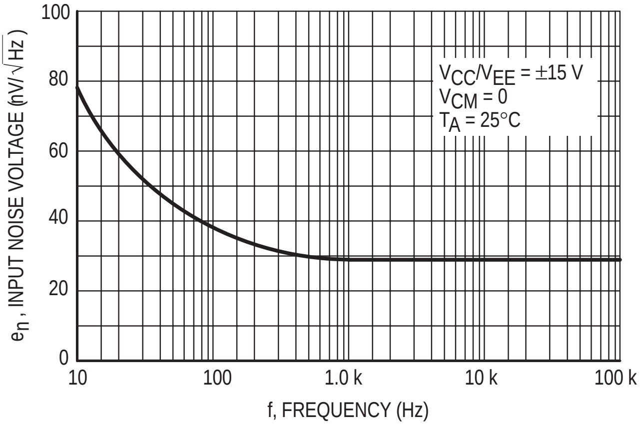


Figure 33. Spectral Noise Density



APPLICATIONS INFORMATION

The bandwidth and slew rate of the MC34080 series is nearly double that of currently available general purpose JFET op–amps. This improvement in AC performance is due to the P–channel JFET differential input stage driving a compensated miller integration amplifier in conjunction with an all NPN output stage.

The all NPN output stage offers unique advantages over the more conventional NPN/PNP transistor Class AB output stage. With a 10 k load resistance, the op amp can typically swing within 1.0 V of the positive rail (V_{CC}), and within 0.3 V of the negative rail (V_{EE}), providing a 28.7 p–p swing from ±15 V supplies. This large output swing becomes most noticeable at lower supply voltages. If the load resistance is referenced to V_{CC} instead of ground, the maximum possible output swing can be achieved for a given supply voltage. For light load currents, the load resistance will pull the output to V_{CC} during the positive swing and the NPN output transistor will pull the output very near V_{EE} during the negative swing. The load resistance value should be much less than that of the feedback resistance to maximize pull–up capability.

The all NPN transistor output stage is also inherently fast, contributing to the operation amplifier's high gain–bandwidth product and fast settling time. The associated high frequency output impedance is 50 Ω (typical) at 8.0 MHz. This allows driving capacitive loads from 0 pF to 300 pF without oscillations over the military temperature range, and over the full range of output swing. The 55°C phase margin and 7.6 dB gain margin as well as the general gain and phase characteristics are virtually independent of the sink/source output swing conditions. The high frequency characteristics of the MC34080 series is especially useful for active filter applications.

The common mode input range is from 2.0 V below the positive rail (V_{CC}) to 4.0 V above the negative rail (V_{EE}). The amplifier remains active if the inputs are biased at the positive rail. This may be useful for some applications in that single supply operation is possible with a single negative supply. However, a degradation of offset voltage and voltage gain may result.

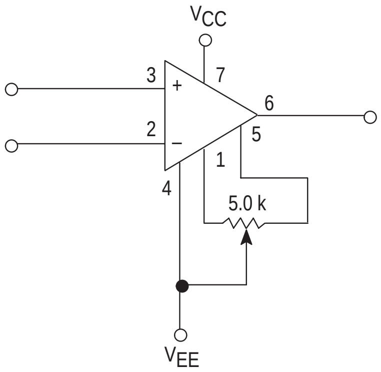
Phase reversal does not occur if either the inverting or noninverting input (or both) exceeds the positive common mode limit. If either input (or both) exceeds the negative common mode limit, the output will be in the high state. The input stage also allows a differential up to ±44 V, provided the maximum input voltage range is not exceeded. The supply voltage operating range is from ±5.0 V to ±22 V.

For optimum frequency performance and stability, careful component placement and printed circuit board layout should be exercised. For example, long unshielded input or output leads may result in unwanted input–output coupling. In order to reduce the input capacitance, resistors connected to the input pins should be physically close to these pins. This not only minimizes the input pole for optimum frequency response, but also minimizes extraneous "pickup" at this node.

Supply decoupling with adequate capacitance close to the supply pin is also important, particularly over temperature, since many types of decoupling capacitors exhibit large impedance changes over temperature.

Primarily due to the JFET inputs of the op amp, the input offset voltage may change due to temperature cycling and board soldering. After 20 temperature cycles (– 55° to 165°C), the typical standard deviation for input offset voltage is 559 µV in the plastic packages. With respect to board soldering (260°C, 10 seconds), the typical standard deviation for input offset voltage is 525 µV in the plastic package. Socketed devices should be used over a minimal temperature range for optimum input offset voltage performance.

Figure 34. Offset Nulling Circuit



MOTOROLA

MC34181,2,4
MC33181,2,4

Low Power, High Slew Rate, Wide Bandwidth, JFET Input Operational Amplifiers

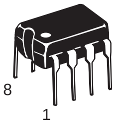
Quality bipolar fabrication with innovative design concepts are employed for the MC33181/2/4, MC34181/2/4 series of monolithic operational amplifiers. This JFET input series of operational amplifiers operates at 210 µA per amplifier and offers 4.0 MHz of gain bandwidth product and 10 V/µs slew rate. Precision matching and an innovative trim technique of the single and dual versions provide low input offset voltages. With a JFET input stage, this series exhibits high input resistance, low input offset voltage and high gain. The all NPN output stage, characterized by no deadband crossover distortion and large output voltage swing, provides high capacitance drive capability, excellent phase and gain margins, low open loop high frequency output impedance and symmetrical source/sink AC frequency response.

The MC33181/2/4, MC34181/2/4 series of devices are specified over the commercial or industrial/vehicular temperature ranges. The complete series of single, dual and quad operational amplifiers are available in the plastic DIP as well as the SOIC surface mount packages.

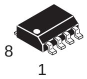
- Low Supply Current: 210 µA (Per Amplifier)
- Wide Supply Operating Range: ±1.5 V to ±18 V
- Wide Bandwidth: 4.0 MHz
- High Slew Rate: 10 V/µs
- Low Input Offset Voltage: 2.0 mV
- Large Output Voltage Swing: –14 V to +14 V (with ±15 V Supplies)
- Large Capacitance Drive Capability: 0 pF to 500 pF
- Low Total Harmonic Distortion: 0.04%
- Excellent Phase Margin: 67°
- Excellent Gain Margin: 6.7 dB
- Output Short Circuit Protection
- Offered in New TSSOP Package Including the Standard SOIC and DIP Packages

ORDERING INFORMATION

Op Amp Function	Device	Operating Temperature Range	Package
Single	MC34181P MC34181D	T_A = 0° to +70°C	Plastic DIP SO–8
	MC33181P MC33181D	T_A = –40° to +85°C	Plastic DIP SO–8
Dual	MC34182P MC34182D	T_A = 0° to +70°C	Plastic DIP SO–8
	MC33182P MC33182D	T_A = –40° to +85°C	Plastic DIP SO–8
Quad	MC34184P MC34184D MC34184DTB	T_A = 0° to +70°C	Plastic DIP SO–14 TSSOP–14
	MC33184P MC33184D MC33184DTB	T_A = –40° to +85°C	Plastic DIP SO–14 TSSOP–14

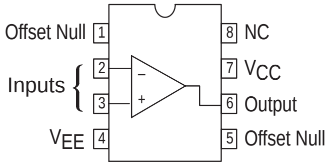


P SUFFIX
PLASTIC PACKAGE
CASE 626

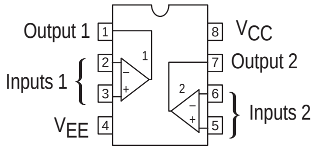


D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

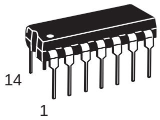
PIN CONNECTIONS



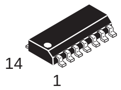
(Single, Top View)



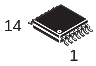
(Dual, Top View)



P SUFFIX
PLASTIC PACKAGE
CASE 646

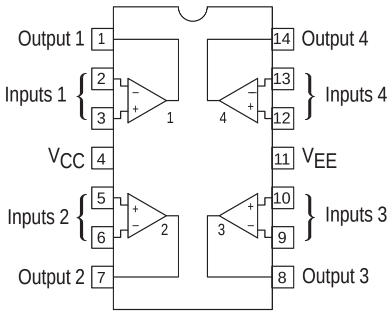


D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO–14)



DTB SUFFIX
PLASTIC PACKAGE
CASE 948G
(TSSOP–14)

PIN CONNECTIONS



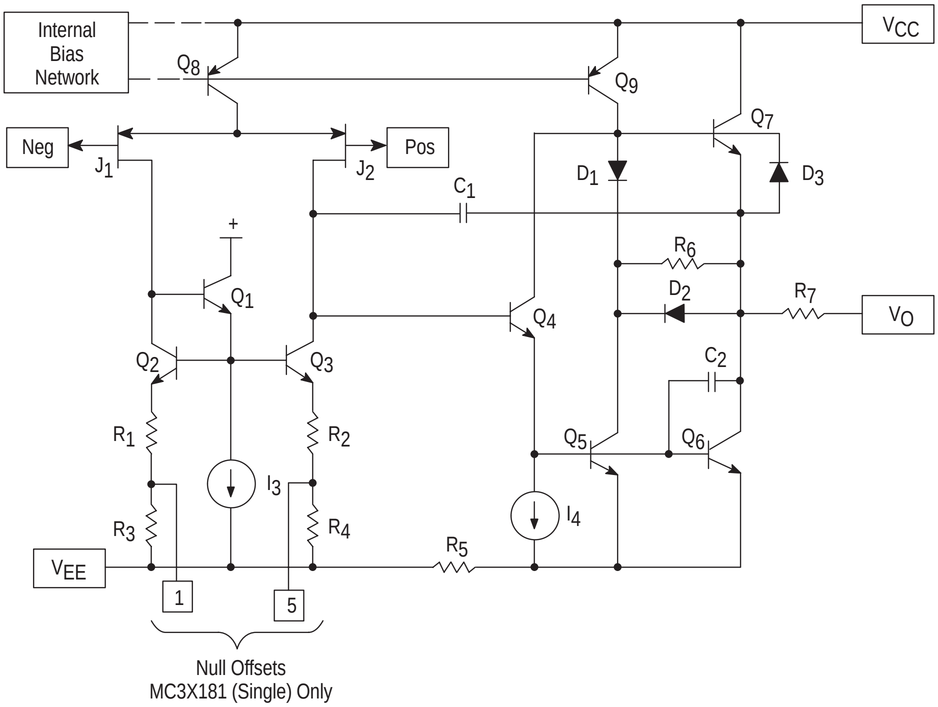
(Quad, Top View)

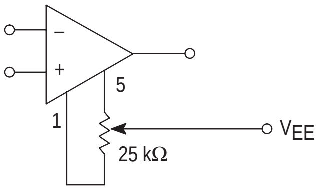
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage (from V_{CC} to V_{EE})	V_S	+36	V
Input Differential Voltage Range	V_{IDR}	Note 1	V
Input Voltage Range	V_{IR}	Note 1	V
Output Short Circuit Duration (Note 2)	t_{SC}	Indefinite	sec
Operating Junction Temperature	T_J	+150	°C
Storage Temperature Range	T_{stg}	–60 to +150	°C

NOTES: 1. Either or both input voltages should not exceed the magnitude of V_{CC} or V_{EE}.
2. Power dissipation must be considered to ensure maximum junction temperature (T_J) is not exceeded (see Figure 1).

Representative Schematic Diagram
(Each Amplifier)





MC3X181 Input Offset Voltage Null CIrcuit

DC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = –15 V, T_A = 25°C, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Input Offset Voltage (R_S = 50 Ω, V_O = 0 V)	V_{IO}				mV
Single					
T_A = +25°C		—	0.5	2.0	
T_A = 0° to +70°C (MC34181)		—	—	3.0	
T_A = –40° to +85°C (MC33181)		—	—	3.5	
Dual					
T_A = +25°C		—	1.0	3.0	
T_A = 0° to +70°C (MC34182)		—	—	4.0	
T_A = –40° to +85°C (MC33182)		—	—	4.5	
Quad					
T_A = +25°C		—	4.0	10	
T_A = 0° to +70°C (MC34184)		—	—	11	
T_A = –40° to +85°C (MC33184)		—	—	11.5	
Average Temperature Coefficient of V_{IO} (R_S = 50 Ω, V_O = 0V)	$\Delta V_{IO}/\Delta T$	—	10	—	µV/°C
Input Offset Current (V_{CM} = 0 V, V_O = 0V)	I_{IO}				nA
T_A = +25°C		—	0.001	0.05	
T_A = 0° to +70°C		—	—	1.0	
T_A = –40° to +85°C		—	—	2.0	
Input Bias Current (V_{CM} = 0 V, V_O = 0V)	I_{IB}				nA
T_A = +25°C		—	0.003	0.1	
T_A = 0° to +70°C		—	—	2.0	
T_A = –40° to +85°C		—	—	4.0	
Input Common Mode Voltage Range	V_{ICR}	(V_{EE} +4.0 V) to (V_{CC} –2.0 V)			V
Large Signal Voltage Gain (R_L = 10 kΩ, V_O = ±10 V)	A_{VOL}				V/mV
T_A = +25°C		25	60	—	
T_A = T_{low} to T_{high}		15	—	—	
Output Voltage Swing (V_{ID} = 1.0 V, R_L = 10 kΩ)	V_O+	+13.5	+14	—	V
T_A = +25°C	V_O-	—	–14	–13.5	
Common Mode Rejection (R_S = 50 Ω, V_{CM} = V_{ICR}, V_O = 0 V)	CMR	70	86	—	dB
Power Supply Rejection (R_S = 50 Ω, V_{CM} = 0 V, V_O = 0 V)	PSR	70	84	—	dB
Output Short Circuit Current (V_{ID} = 1.0 V, Output to Ground)	I_{SC}				mA
Source		3.0	8.0	—	
Sink		8.0	11	—	
Power Supply Current (No Load, V_O = 0 V)	I_D				µA
Single					
T_A = +25°C		—	210	250	
T_A = T_{low} to T_{high}		—	—	250	
Dual					
T_A = +25°C		—	420	500	
T_A = T_{low} to T_{high}		—	—	500	
Quad					
T_A = +25°C		—	840	1000	
T_A = T_{low} to T_{high}		—	—	1000	

AC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = –15 V, T_A = 25°C, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Slew Rate (V_{in} = –10 V to +10 V, R_L = 10 kΩ, C_L = 100 pF) A_V = +1.0 A_V = –1.0	SR	 7.0 —	 10 10	 — —	V/µs
Settling Time (A_V = –1.0, R_L = 10 kΩ, V_O = 0 V to +10 V Step) To Within 0.10% To Within 0.01%	t_s	 — —	 1.1 1.5	 — —	µs
Gain Bandwidth Product (f = 100 kHz)	GBW	3.0	4.0	—	MHz
Power Bandwidth (A_V = +1.0, R_L = 10 kΩ, V_O = 20 V_{pp}, THD = 5.0%)	BW_p	—	120	—	kHz
Phase Margin (–10 V < V_O < +10 V) R_L = 10 kΩ R_L = 10 kΩ, C_L = 100 pF	f_m	 — —	 67 34	 — —	Degrees
Gain Margin (–10 V < V_O < +10 V) R_L = 10 kΩ R_L = 10 kΩ, C_L = 100 pF	A_m	 — —	 6.7 3.4	 — —	dB
Equivalent Input Noise Voltage R_S = 100 Ω, f = 1.0 kHz	e_n	—	38	—	$nV/\sqrt{Hz}$
Equivalent Input Noise Current f = 1.0 kHz	i_n	—	0.01	—	$pA/\sqrt{Hz}$
Differential Input Capacitance	C_i	—	3.0	—	pF
Differential Input Resistance	R_i	—	10^{12}	—	W
Total Harmonic Distortion A_V = 10, R_L = 10 kΩ, 2.0 V_{pp} < V_O < 20 V_{pp}, f = 1.0 kHz	THD	—	0.04	—	%
Channel Separation (R_L = 10 kΩ, –10 V < V_O < +10 V, 0 Hz < f < 10 kHz)	—	—	120	—	dB
Open Loop Output Impedance (f = 1.0 MHz)	$\lvert Z_o \rvert$	—	200	—	Ω

Figure 1. Maximum Power Dissipation versus Temperature for Package Variations

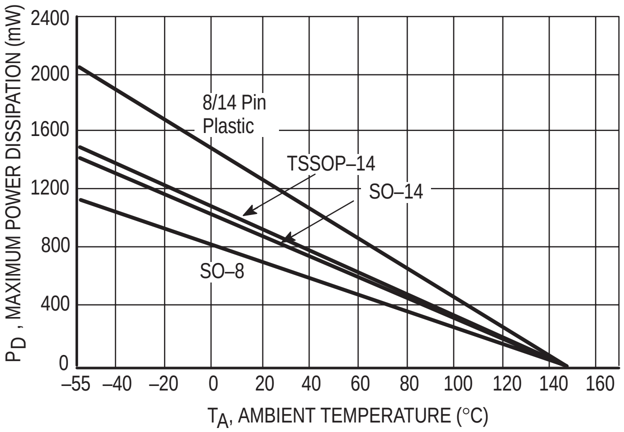


Figure 2. Input Common Mode Voltage Range versus Temperature

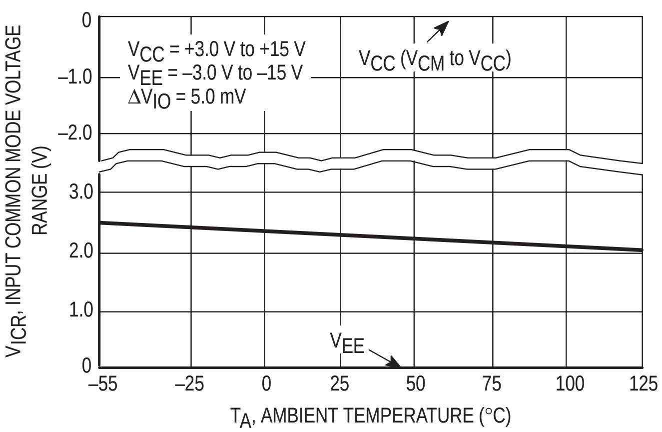


Figure 3. Input Bias Current versus Temperature

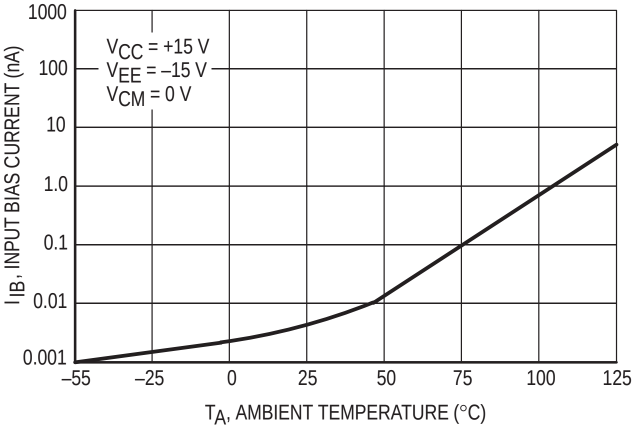


Figure 4. Input Bias Current versus Input Common Mode Voltage

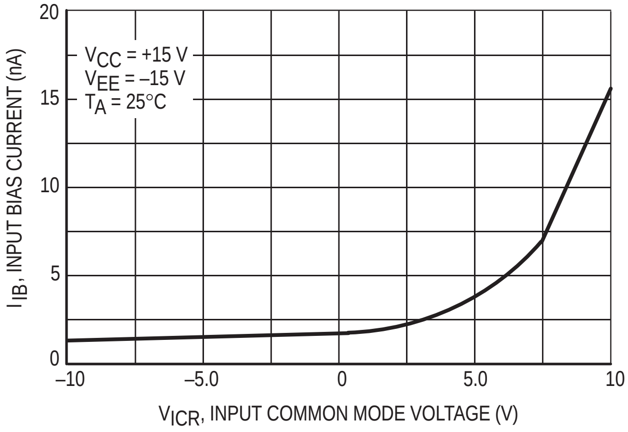


Figure 5. Output Voltage Swing versus Supply Voltage

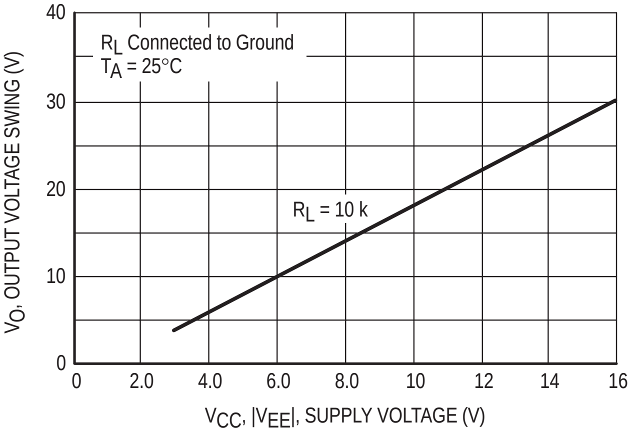


Figure 6. Output Saturation Voltage versus Load Current

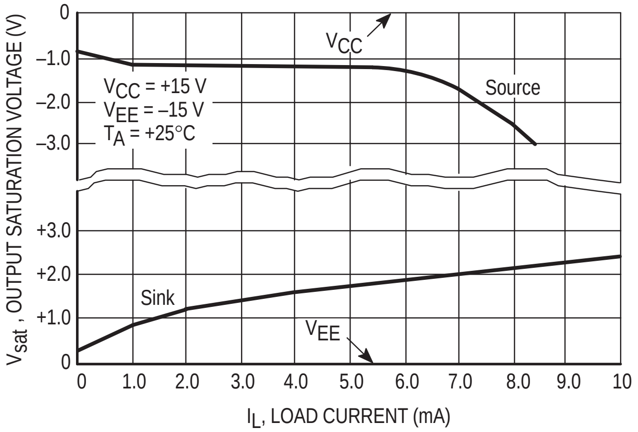


Figure 7. Output Saturation Voltage versus Load Resistance to Ground

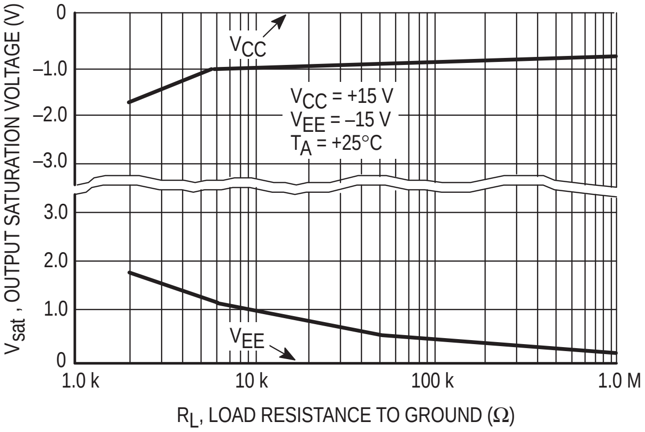


Figure 8. Output Saturation Voltage versus Load Resistance to V_{CC}

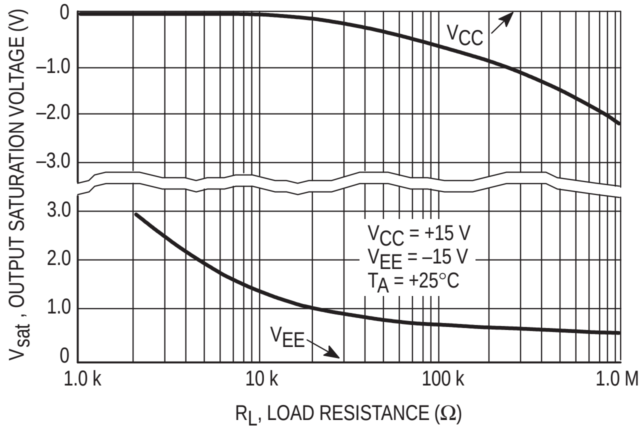


Figure 9. Output Short Circuit Current versus Temperature

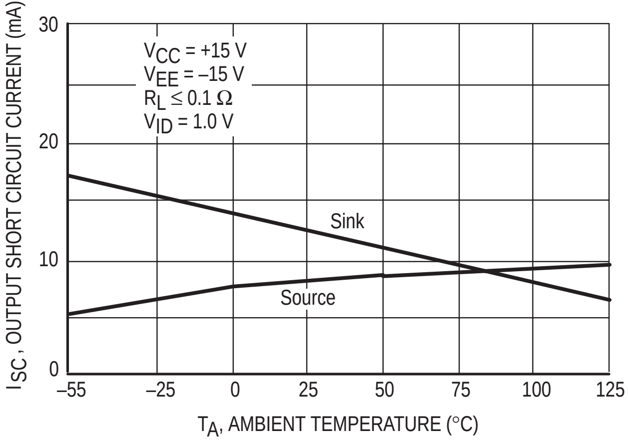


Figure 10. Output Impedance versus Frequency

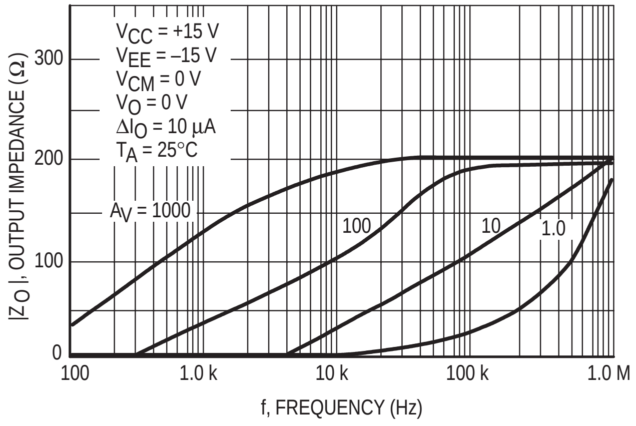


Figure 11. Output Voltage Swing versus Frequency

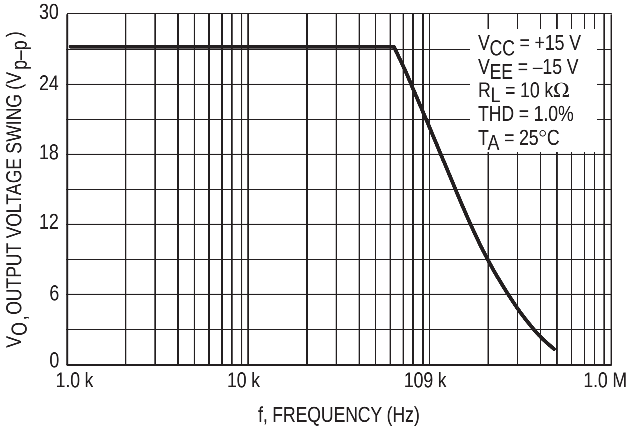


Figure 12. Output Distortion versus Frequency

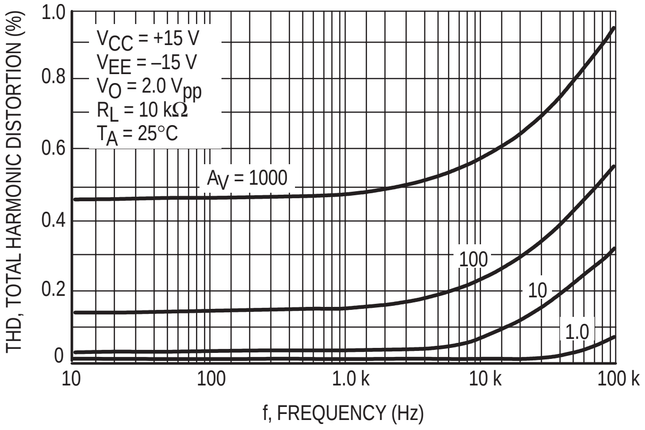


Figure 13. Open Loop Voltage Gain versus Temperature

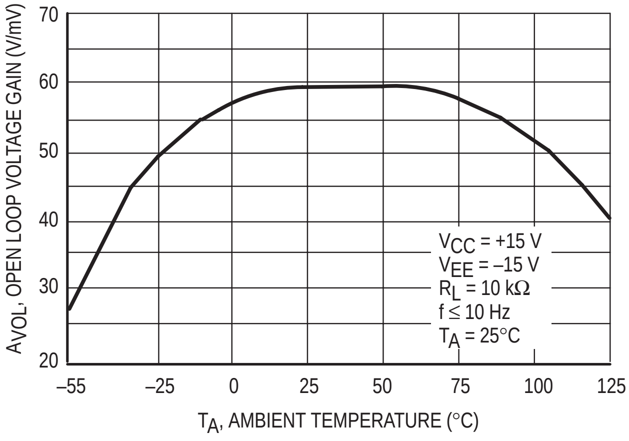


Figure 14. Open Loop Voltage Gain and Phase versus Frequency

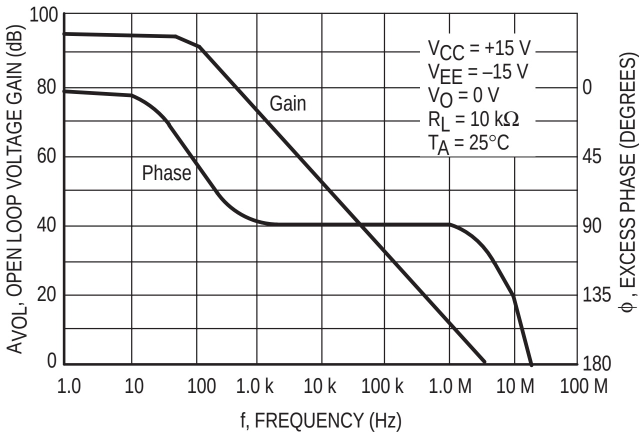


Figure 15. Normalized Gain Bandwidth Product versus Temperature

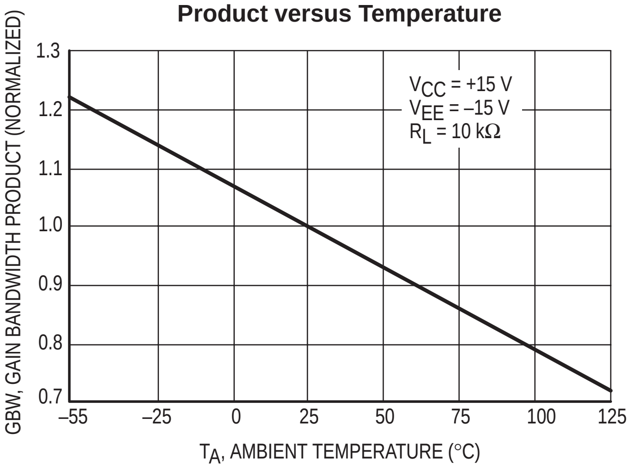


Figure 16. Output Voltage Overshoot versus Load Capacitance

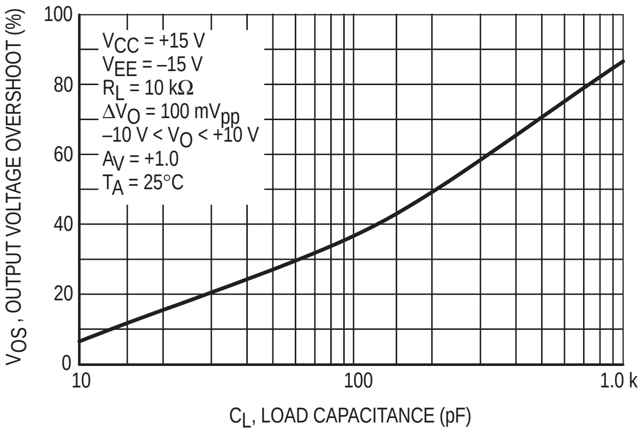


Figure 17. Phase Margin versus Load Capacitance

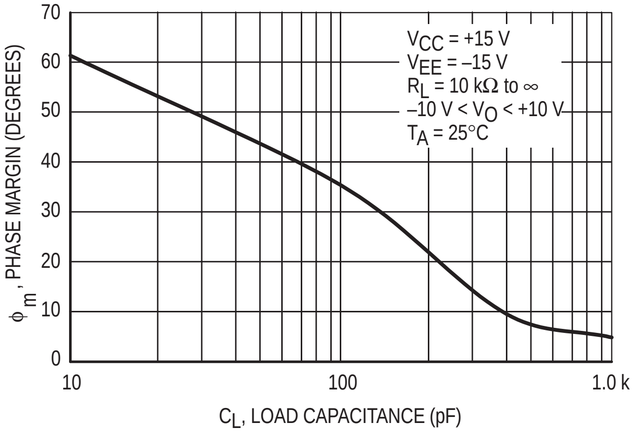


Figure 18. Gain Margin versus Load Capacitance

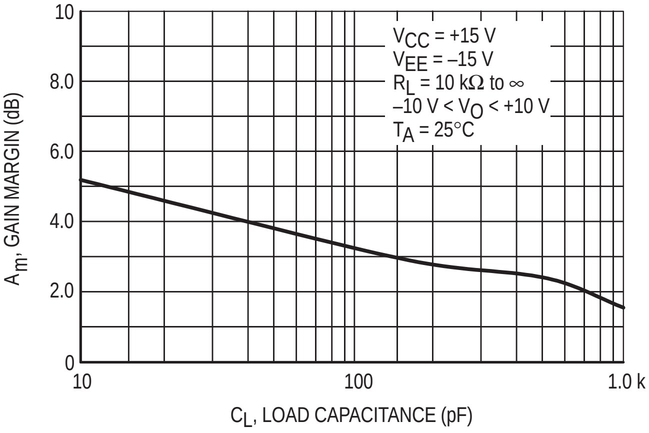


Figure 19. Phase Margin versus Temperature

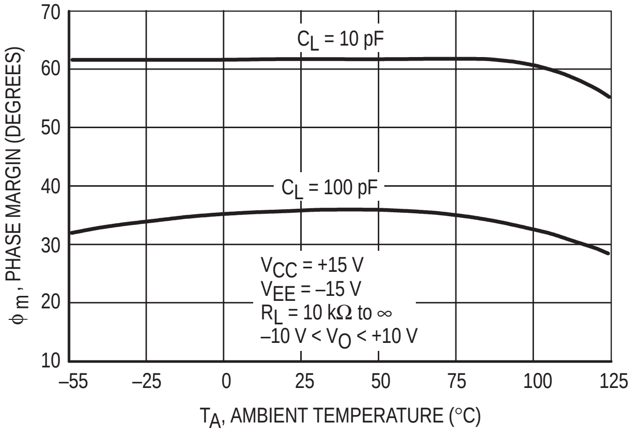


Figure 20. Gain Margin versus Temperature

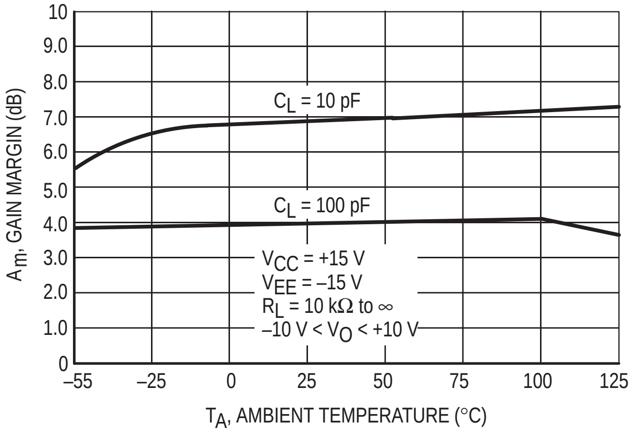


Figure 21. Normalized Slew Rate versus Temperature

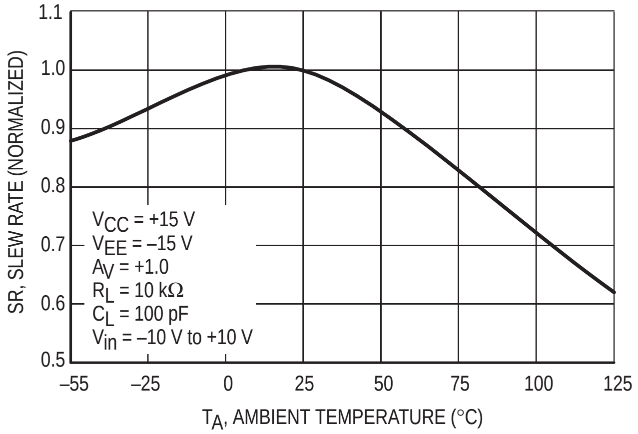


Figure 22. Common Mode Rejection versus Frequency

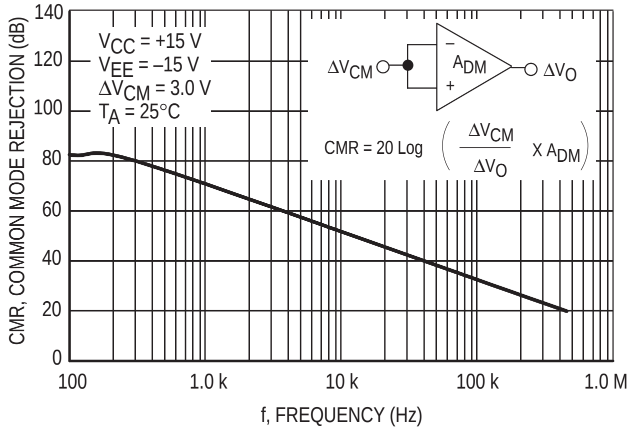


Figure 23. Input Noise Voltage versus Frequency

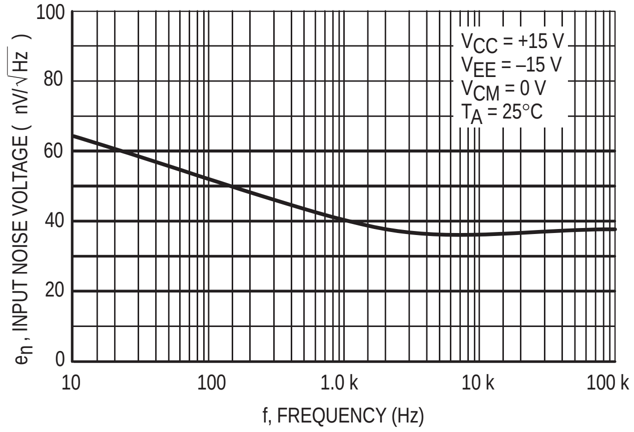


Figure 24. Power Supply Rejection versus Temperature

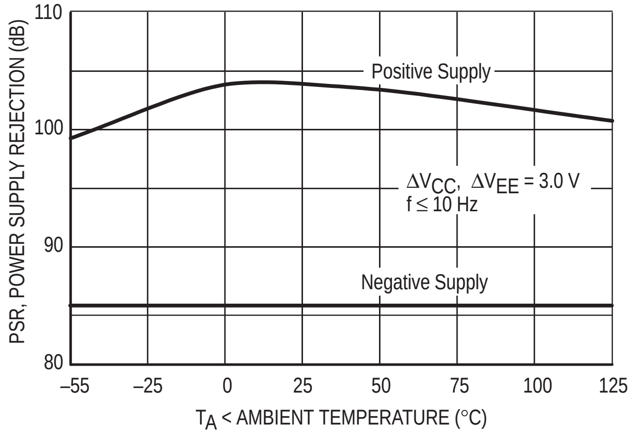


Figure 25. Power Supply Rejection versus Frequency

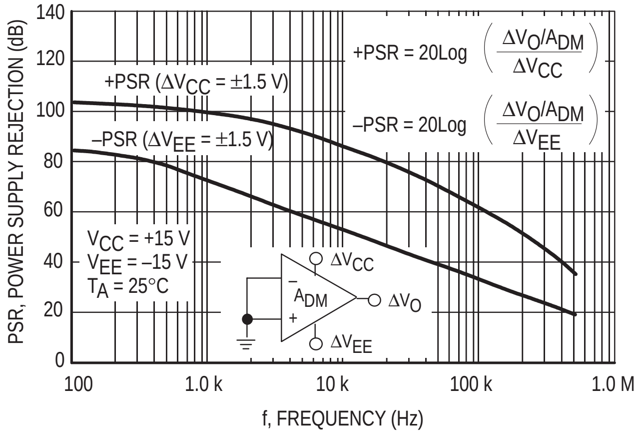


Figure 26. Normalized Supply Current versus Supply Voltage

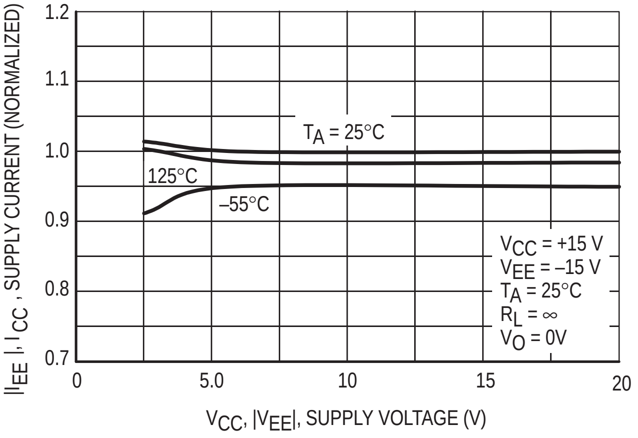


Figure 27. Channel Separation versus Frequency

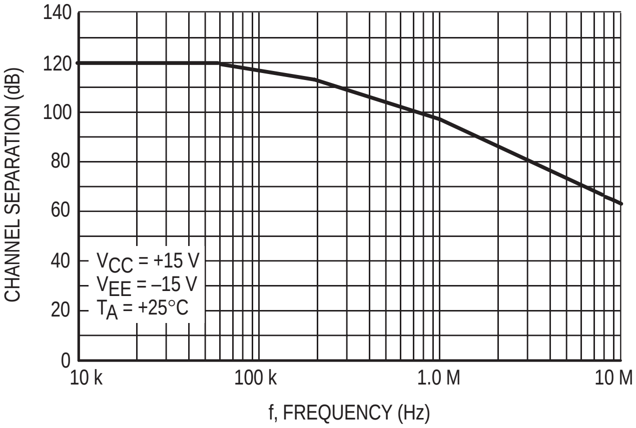


Figure 28. Transient Response

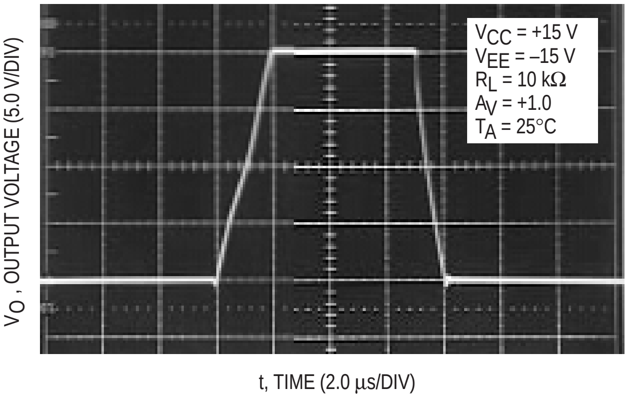
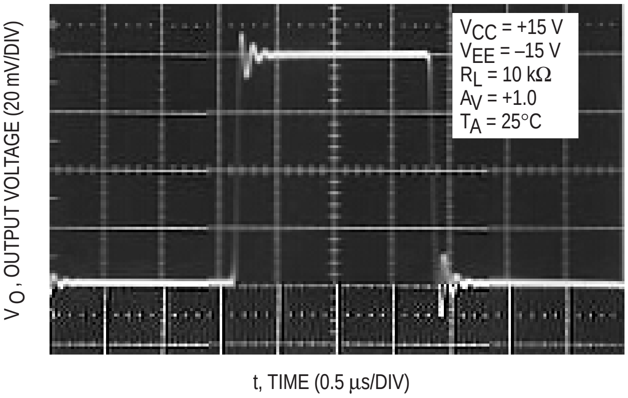


Figure 29. Small Signal Transient Reponse



MOTOROLA

TCA0372

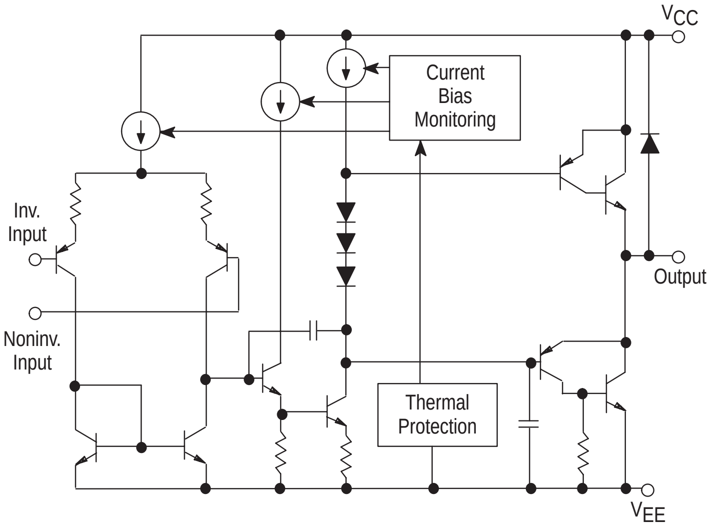
Advance Information

Dual Power Operational Amplifier

The TCA0372 is a monolithic circuit intended for use as a power operational amplifier in a wide range of applications, including servo amplifiers and power supplies. No deadband crossover distortion provides better performance for driving coils.

- Output Current to 1.0 A
- Slew Rate of 1.3 V/µs
- Wide Bandwidth of 1.1 MHz
- Internal Thermal Shutdown
- Single or Split Supply Operation
- Excellent Gain and Phase Margins
- Common Mode Input Includes Ground
- Zero Deadband Crossover Distortion

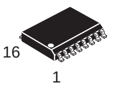
Representative Block Diagram

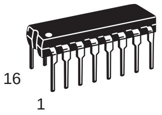


ORDERING INFORMATION

Device	Operating Temperature Range	Package
TCA0372DW	T_J = –40° to +150°C	SOP (12+2+2) L
TCA0372DP1		Plastic DIP
TCA0372DP2		Plastic DIP

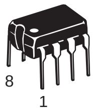
DW SUFFIX
PLASTIC PACKAGE
CASE 751G
SOP (12+2+2)L





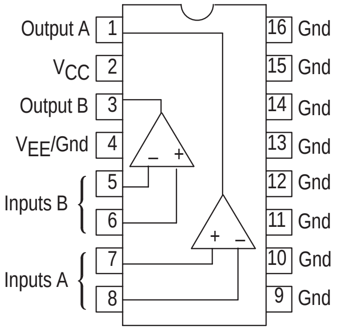
DP2 SUFFIX
PLASTIC PACKAGE
CASE 648

DP1 SUFFIX
PLASTIC PACKAGE
CASE 626



PIN CONNECTIONS

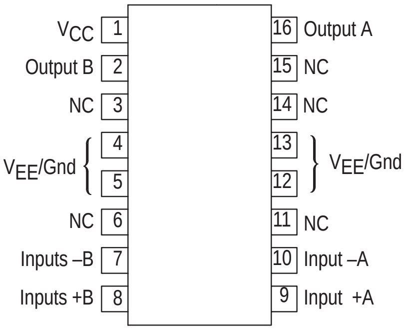
TCA0372DP2



(Top View)

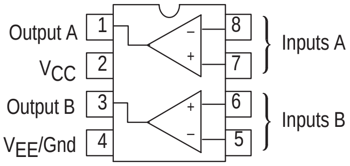
*Pins 4 and 9 to 16 are internally connected.

TCA0372DW



(Top View)

TCA0372DP1



(Top View)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage (from V_{CC} to V_{EE})	V_S	40	V
Input Differential Voltage Range	V_{IDR}	(Note 1)	V
Input Voltage Range	V_{IR}	(Note 1)	V
Junction Temperature (Note 2)	T_J	+150	°C
Storage Temperature Range	T_{stg}	–55 to +150	°C
DC Output Current	I_O	1.0	A
Peak Output Current (Nonrepetitive)	$I_{(max)}$	1.5	A

DC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = –15 V, R_L connected to ground, T_J = –40° to +125°C.)

Characteristics	Symbol	Min	Typ	Max	Unit
Input Offset Voltage (V_{CM} = 0)	V_{IO}				mV
T_J = +25°C		—	1.0	15	
T_J, T_{low} to T_{high}		—	—	20	
Average Temperature Coefficient of Offset Voltage	$\Delta V_{IO}/\Delta T$	—	20	—	μV/°C
Input Bias Current (V_{CM} = 0)	I_{IB}	—	100	500	nA
Input Offset Current (V_{CM} = 0)	I_{IO}	—	10	50	nA
Large Signal Voltage Gain V_O = ±10 V, R_L = 2.0 k	A_{VOL}	30	100	—	V/mV
Output Voltage Swing (I_L = 100 mA)	V_{OH}				V
T_J = +25°C		14.0	14.2	—	
T_J = T_{low} to T_{high}		13.9	—	—	
T_J = +25°C	V_{OL}	—	–14.2	–14.0	
T_J = T_{low} to T_{high}		—	—	–13.9	
Output Voltage Swing (I_L = 1.0 A)	V_{OH}				V
V_{CC} = +24 V, V_{EE} = 0 V, T_J = +25°C		22.5	22.7	—	
V_{CC} = +24 V, V_{EE} = 0 V, T_J = T_{low} to T_{high}		22.5	—	—	
V_{CC} = +24 V, V_{EE} = 0 V, T_J = +25°C	V_{OL}	—	1.3	1.5	
V_{CC} = +24 V, V_{EE} = 0 V, T_J = T_{low} to T_{high}		—	—	1.5	
Input Common Mode Voltage Range	V_{ICR}				V
T_J = +25°C		V_{EE} to (V_{CC} –1.0)			
T_J = T_{low} to T_{high}		V_{EE} to (V_{CC} –1.3)			
Common Mode Rejection Ratio (R_S = 10 k)	CMRR	70	90	—	dB
Power Supply Rejection Ratio (R_S = 100 Ω)	PSRR	70	90	—	dB
Power Supply Current	I_D				mA
T_J = +25°C		—	5.0	10	
T_J = T_{low} to T_{high}		—	—	14	

NOTES: 1. Either or both input voltages should not exceed the magnitude of V_{CC} or V_{EE}.
2. Power dissipation must be considered to ensure maximum junction temperature (T_J) is not exceeded.

AC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = –15 V, R_L connected to ground, T_J = +25°C, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Slew Rate (V_{in} = –10 V to +10 V, R_L = 2.0 k, C_L = 100 pF) A_V = –1.0, T_J = T_{low} to T_{high}	SR	1.0	1.4	—	V/μs
Gain Bandwidth Product (f = 100 kHz, C_L = 100 pF, R_L = 2.0 k)	GBW				MHz
T_J = 25°C		0.9	1.4	—	
T_J = T_{low} to T_{high}		0.7	—	—	
Phase Margin T_J = T_{low} to T_{high} R_L = 2.0 k, C_L = 100 pF	ϕ_m	—	65	—	Degrees
Gain Margin R_L = 2.0 k, C_L = 100 pF	A_m	—	15	—	dB
Equivalent Input Noise Voltage R_S = 100 Ω, f = 1.0 to 100 kHz	e_n	—	22	—	$nV/\sqrt{Hz}$
Total Harmonic Distortion A_V = –1.0, R_L = 50 Ω, V_O = 0.5 VRMS, f = 1.0 kHz	THD	—	0.02	—	%

NOTE: In case V_{EE} is disconnected before V_{CC}, a diode between V_{EE} and Ground is recommended to avoid damaging the device.

Figure 1. Supply Current versus Suppy Voltage with No Load

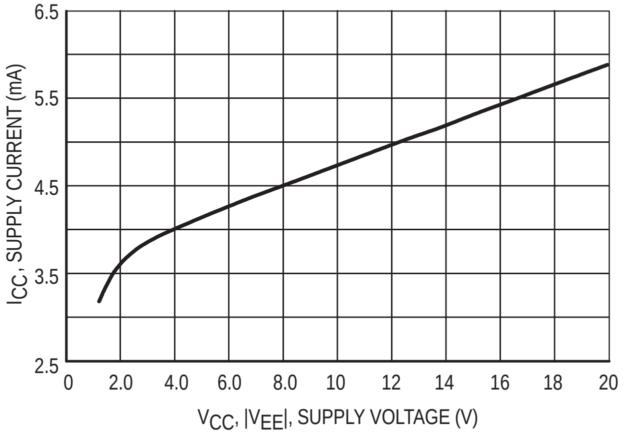


Figure 2. Output Saturation Voltage versus Load Current

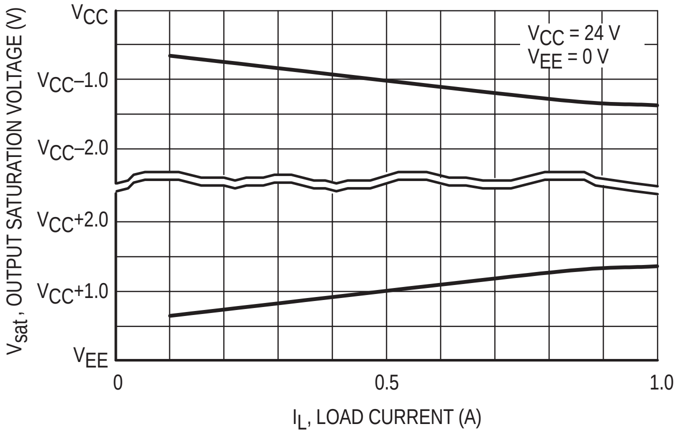


Figure 3. Voltage Gain and Phase versus Frequency

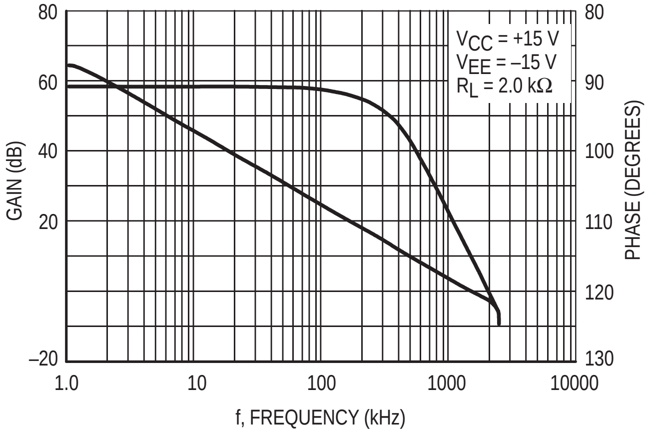


Figure 4. Phase Margin versus Output Load Capacitance

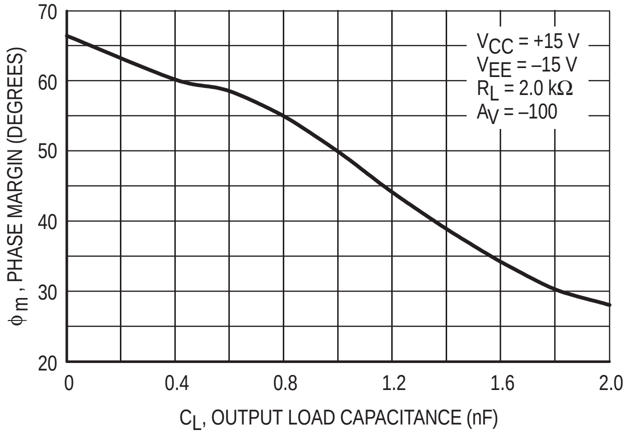


Figure 5. Small Signal Transient Response

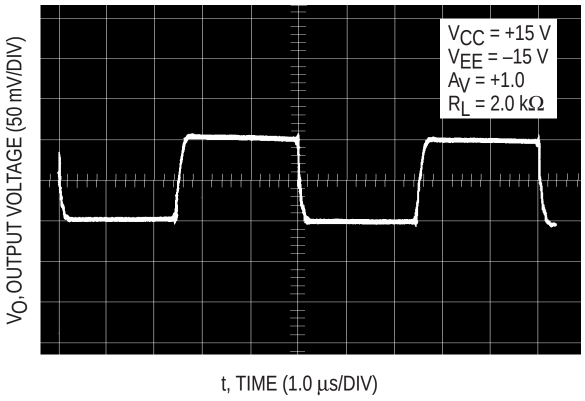


Figure 6. Large Signal Transient Response

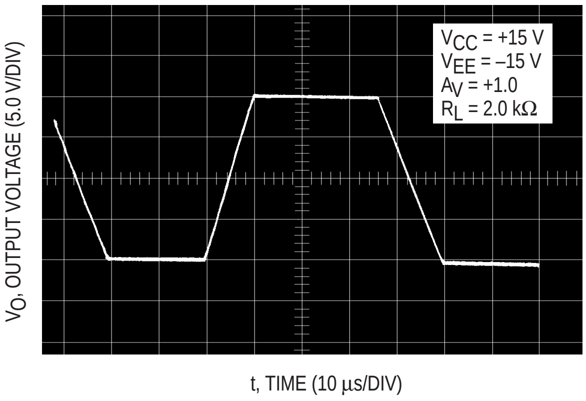


Figure 7. Sine Wave Reponse

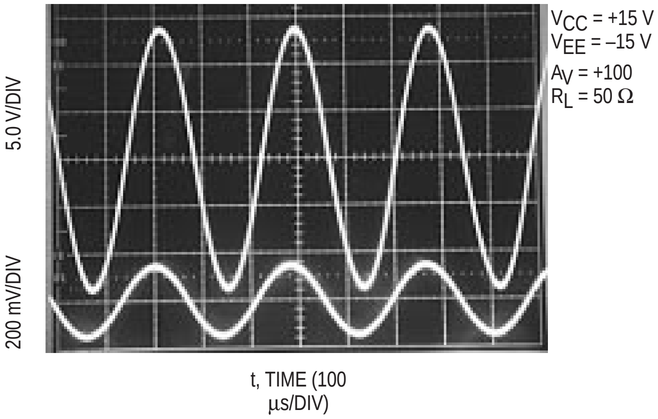
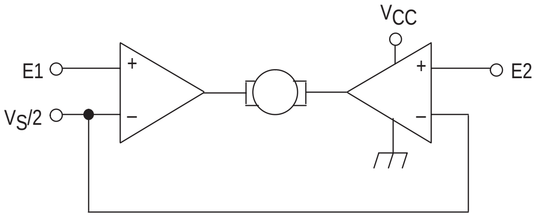
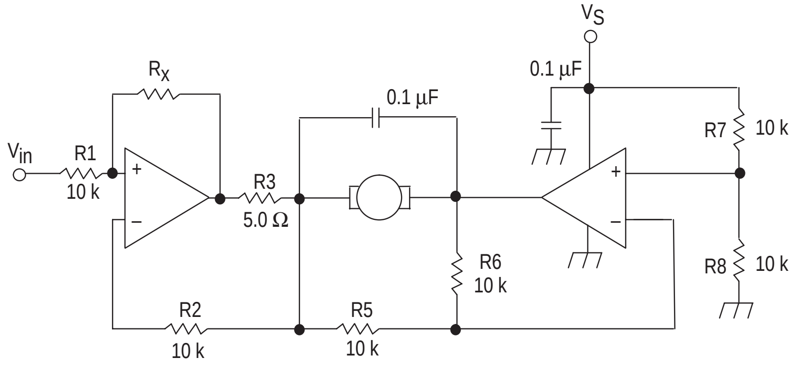


Figure 8. Bidirectional DC Motor Control with Microprocessor–Compatible Inputs



V_S = Logic Supply Voltage
Must Have $V_{CC} > V_S$
E1, E2 = Logic Inputs

Figure 9. Bidirectional Speed Control of DC Motors



For circuit stability, ensure that $R_X > \frac{2R3 \cdot R1}{R_M}$ where, R_M = internal resistance of motor.

The voltage available at the terminals of the motor is: $V_M = 2\left(V_1 - \frac{V_S}{2}\right) + |R_o| \cdot I_M$

where, $|R_o| = \frac{2R3 \cdot R1}{R_X}$ and I_M is the motor current.

THERMAL INFORMATION

The maximum power consumption an integrated circuit can tolerate at a given operating ambient temperature can be found from the equation:

$$P_{D(TA)} = \frac{T_{J(max)} - T_A}{R_{\theta JA}\ (typ)}$$

where, $P_{D(TA)}$ = power dissipation allowable at a given operating ambient temperature.

This must be greater than the sum of the products of the supply voltages and supply currents at the worst case operating condition.

$T_{J(max)}$ = Maximum operating junction temperature as listed in the maximum ratings section.
T_A = Maximum desired operating ambient temperature.
$R_{\theta JA(typ)}$ = Typical thermal resistance junction–to–ambient.

MOTOROLA

TL062
TL064

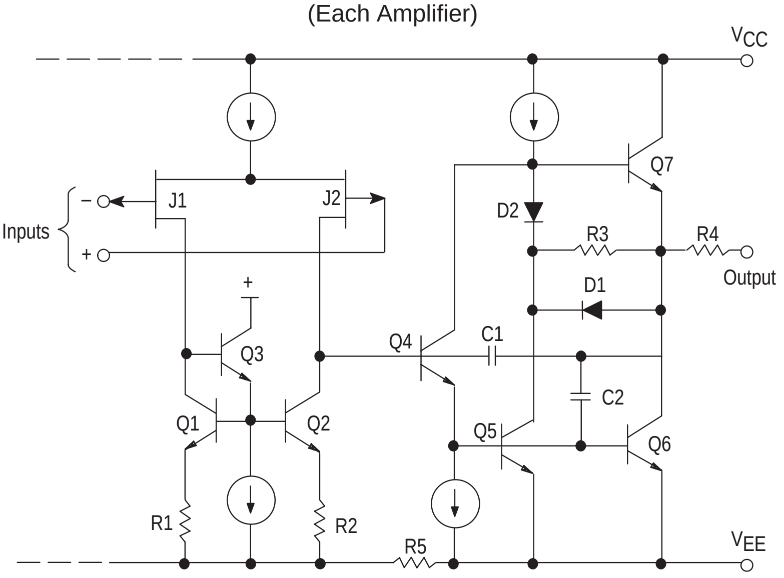
Low Power JFET Input Operational Amplifiers

These JFET input operational amplifiers are designed for low power applications. They feature high input impedance, low input bias current and low input offset current. Advanced design techniques allow for higher slew rates, gain bandwidth products and output swing.

The commercial and vehicular devices are available in Plastic dual in–line and SOIC packages.

- Low Supply Current: 200 µA/Amplifier
- Low Input Bias Current: 5.0 pA
- High Gain Bandwidth: 2.0 MHz
- High Slew Rate: 6.0 V/µs
- High Input Impedance: 10^{12} Ω
- Large Output Voltage Swing: ±14 V
- Output Short Circuit Protection

Representative Schematic Diagram
(Each Amplifier)



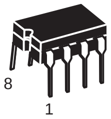
ORDERING INFORMATION

Op Amp Function	Device	Operating Temperature Range	Package
Dual	TL062CD, ACD TL062CP, ACP	T_A = 0° to +70°C	SO–8 Plastic DIP
	TL062VD TL062VP	T_A = –40° to +85°C	SO–8 Plastic DIP
Quad	TL064CD, ACD TL064CN, ACN	T_A = 0° to +70°C	SO–14 Plastic DIP
	TL064VD TL064VN	T_A = –40° to +85°C	SO–14 Plastic DIP

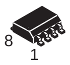
LOW POWER JFET INPUT OPERATIONAL AMPLIFIERS

SEMICONDUCTOR TECHNICAL DATA

DUAL

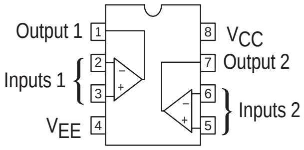


P SUFFIX
PLASTIC PACKAGE
CASE 626



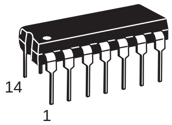
D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

PIN CONNECTIONS

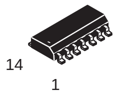


(Top View)

QUAD

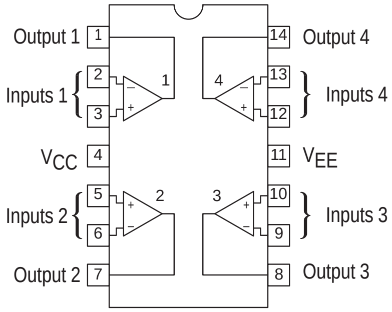


N SUFFIX
PLASTIC PACKAGE
CASE 646



D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO–14)

PIN CONNECTIONS



(Top View)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage (from V_{CC} to V_{EE})	V_S	+36	V
Input Differential Voltage Range (Note 1)	V_{IDR}	±30	V
Input Voltage Range (Notes 1 and 2)	V_{IR}	±15	V
Output Short Circuit Duration (Note 3)	t_{SC}	Indefinite	sec
Operating Junction Temperature	T_J	+150	°C
Storage Temperature Range	T_{stg}	–60 to +150	°C

NOTES: 1. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
2. The magnitude of the input voltage must never exceed the magnitude of the supply or 15 V, whichever is less.
3. Power dissipation must be considered to ensure maximum junction temperature (T_J) is not exceeded. (See Figure 1.)

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = –15 V, T_A = 0° to +70°C, unless otherwise noted.)

Characteristics	Symbol	TL062AC TL064AC			TL062C TL064C			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage (R_S = 50 Ω, V_O = 0V)	V_{IO}							mV
T_A = 25°C		—	3.0	6.0	—	3.0	15	
T_A = 0° to +70°C		—	—	7.5	—	—	20	
Average Temperature Coefficient for Offset Voltage (R_S = 50 Ω, V_O = 0 V)	$\Delta V_{IO}/\Delta T$	—	10	—	—	10	—	µV/°C
Input Offset Current (V_{CM} = 0 V, V_O = 0 V)	I_{IO}							
T_A = 25°C		—	0.5	100	—	0.5	200	pA
T_A = 0° to +70°C		—	—	2.0	—	—	2.0	nA
Input Bias Current (V_{CM} = 0 V, V_O = 0 V)	I_{IB}							
T_A = 25°C		—	3.0	200	—	3.0	200	pA
T_A = 0° to +70°C		—	—	2.0	—	—	10	nA
Input Common Mode Voltage Range	V_{ICR}	—	+14.5	+11.5	—	+14.5	+11	V
T_A = 25°C		–11.5	–12.0	—	–11	–12.0	—	
Large Signal Voltage Gain (R_L = 10 kΩ, V_O = ±10 V)	A_{VOL}							V/mV
T_A = 25°C		4.0	58	—	3.0	58	—	
T_A = 0° to +70°C		4.0	—	—	3.0	—	—	
Output Voltage Swing (R_L = 10 kΩ, V_{ID} = 1.0 V)								V
T_A = 25°C	V_O+	+10	+14	—	+10	+14	—	
	V_O-	—	–14	–10	—	–14	–10	
T_A = 0° to +70°C	V_O+	+10	—	—	+10	—	—	
	V_O-	—	—	–10	—	—	–10	
Common Mode Rejection (R_S = 50 Ω, V_{CM} = V_{ICR} min, V_O = 0 V, T_A = 25°C)	CMR	80	84	—	70	84	—	dB
Power Supply Rejection (R_S = 50 Ω, V_{CM} = 0 V, V_O = 0, T_A = 25°C)	PSR	80	86	—	70	86	—	dB
Power Supply Current (each amplifier) (No Load, V_O = 0 V, T_A = 25°C)	I_D	—	200	250	—	200	250	µA
Total Power Dissipation (each amplifier) (No Load, V_O = 0 V, T_A = 25°C)	P_D	—	6.0	7.5	—	6.0	7.5	mW

DC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = –15 V, T_A = T_{low} to T_{high} [Note 4], unless otherwise noted.)

Characteristics	Symbol	TL062V			TL064V			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage (R_S = 50 Ω, V_O = 0V)	V_{IO}							mV
T_A = 25°C		—	3.0	6.0	—	3.0	9.0	
T_A = T_{low} to T_{high}		—	—	9.0	—	—	15	
Average Temperature Coefficient for Offset Voltage (R_S = 50 Ω, V_O = 0 V)	$\Delta V_{IO}/\Delta T$	—	10	—	—	10	—	µV/°C
Input Offset Current (V_{CM} = 0 V, V_O = 0 V)	I_{IO}							
T_A = 25°C		—	5.0	100	—	5.0	100	pA
T_A = T_{low} to T_{high}		—	—	20	—	—	20	nA
Input Bias Current (V_{CM} = 0 V, V_O = 0 V)	I_{IB}							
T_A = 25°C		—	30	200	—	30	200	pA
T_A = T_{low} to T_{high}		—	—	50	—	—	50	nA
Input Common Mode Voltage Range (T_A = 25°C)	V_{ICR}	— –11.5	+14.5 –12.0	+11.5 —	— –11.5	+14.5 –12.0	+11.5 —	V
Large Signal Voltage Gain (R_L = 10 kΩ, V_O = ±10 V)	A_{VOL}							V/mV
T_A = 25°C		4.0	58	—	4.0	58	—	
T_A = T_{low} to T_{high}		4.0	—	—	4.0	—	—	
Output Voltage Swing (R_L = 10 kΩ, V_{ID} = 1.0 V)								V
T_A = 25°C	V_O+	+10	+14	—	+10	+14	—	
	V_O-	—	–14	–10	—	–14	–10	
T_A = T_{low} to T_{high}	V_O+	+10	—	—	+10	—	—	
	V_O-	—	—	–10	—	—	–10	
Common Mode Rejection (R_S = 50 Ω, V_{CM} = V_{ICR} min, V_O = 0, T_A = 25°C)	CMR	80	84	—	80	84	—	dB
Power Supply Rejection (R_S = 50 Ω, V_{CM} = 0 V, V_O = 0, T_A = 25°C)	PSR	80	86	—	80	86	—	dB
Power Supply Current (each amplifier) (No Load, V_O = 0 V, T_A = 25°C)	I_D	—	200	250	—	200	250	µA
Total Power Dissipation (each amplifier) (No Load, V_O = 0 V, T_A = 25°C)	P_D	—	6.0	7.5	—	6.0	7.5	mW

NOTE: 4. T_{low} = –40°C T_{high} = +85°C for TL062,4V

AC ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = –15 V, T_A = +25°C, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Slew Rate (V_{in} = –10 V to +10 V, R_L = 10 kΩ, C_L = 100 pF, A_V = +1.0)	SR	2.0	6.0	—	V/µs
Rise Time (V_{in} = 20 mV, R_L = 10 kΩ, C_L = 100 pF, A_V = +1.0)	t_r	—	0.1	—	µs
Overshoot (V_{in} = 20 mV, R_L = 10 kΩ, C_L = 100 pF, A_V = +1.0)	OS	—	10	—	%
Settling Time (V_{CC} = +15 V, V_{EE} = –15 V, A_V = –1.0, R_L = 10 kΩ, V_O = 0 V to +10 V step)	t_S				µs
To within 10 mV		—	1.6	—	
To within 1.0 mV		—	2.2	—	
Gain Bandwidth Product (f = 200 kHz)	GBW	—	2.0	—	MHz
Equivalent Input Noise (R_S = 100 Ω, f = 1.0 kHz)	e_n	—	47	—	$nV/\sqrt{Hz}$
Input Resistance	R_i	—	10^{12}	—	W
Channel Separation (f = 10 kHz)	CS	—	120	—	dB

Figure 1. Maximum Power Dissipation versus Temperature for Package Variations

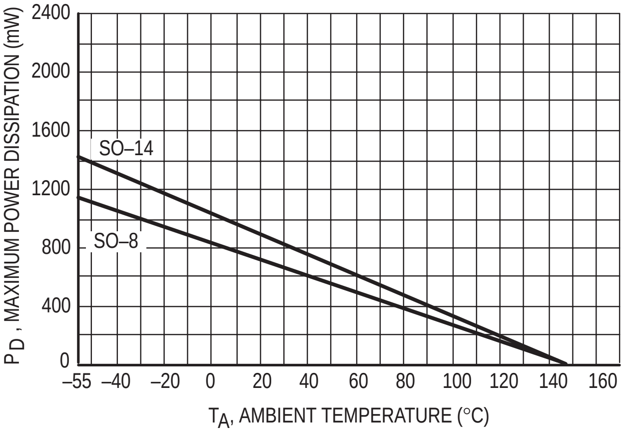


Figure 2. Output Voltage Swing versus Supply Voltage

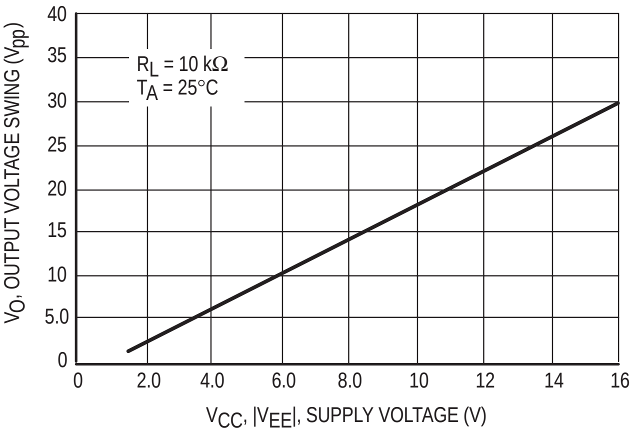


Figure 3. Output Voltage Swing versus Temperature

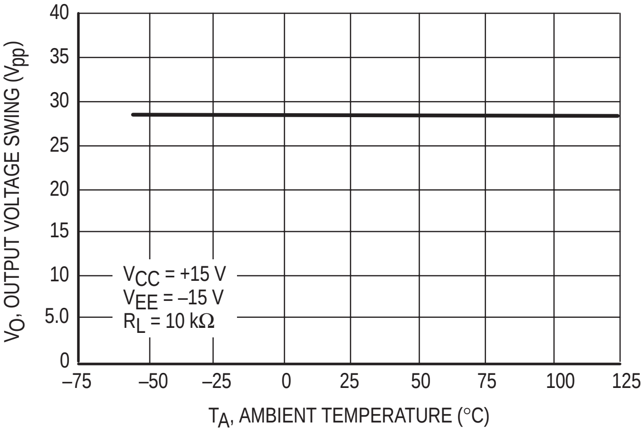


Figure 4. Output Voltage Swing versus Load Resistance

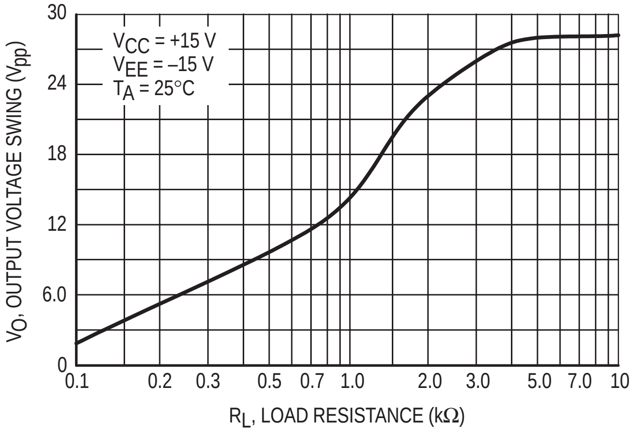


Figure 5. Output Voltage Swing versus Frequency

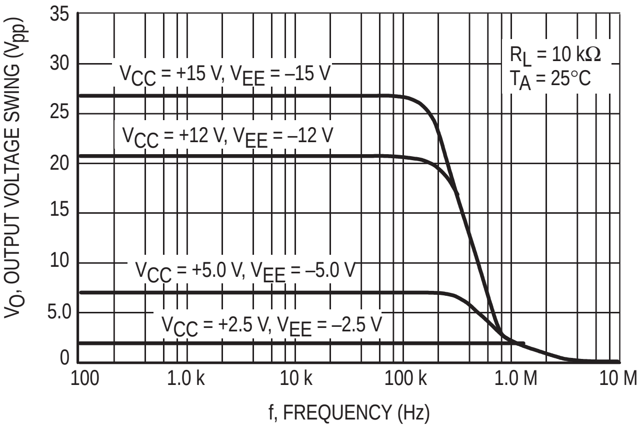


Figure 6. Large Signal Voltage Gain versus Temperature

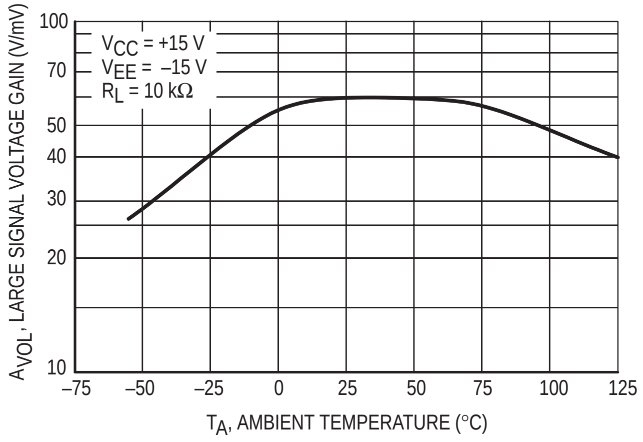


Figure 7. Open Loop Voltage Gain and Phase versus Frequency

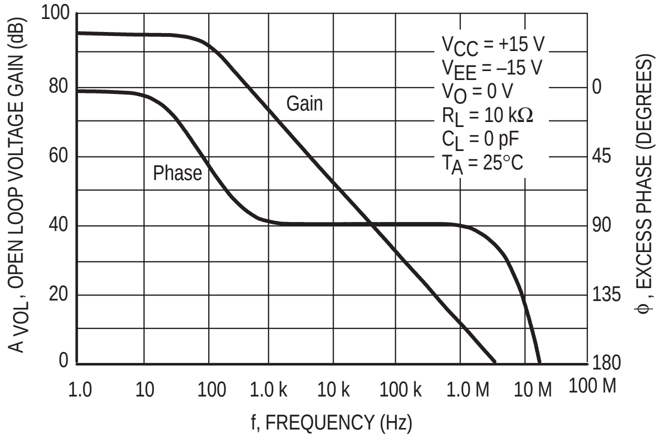


Figure 8. Supply Current per Amplifier versus Supply Voltage

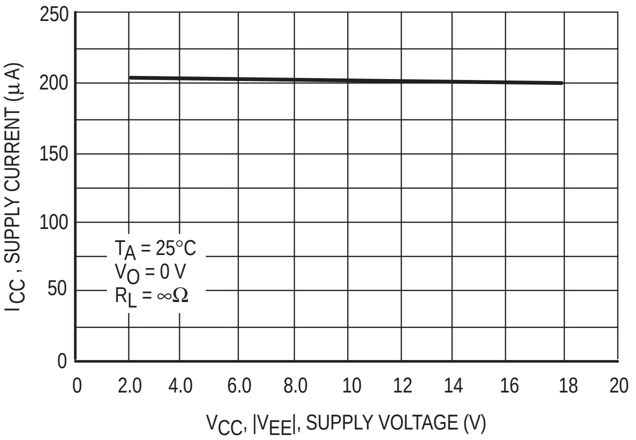


Figure 9. Supply Current per Amplifier versus Temperature

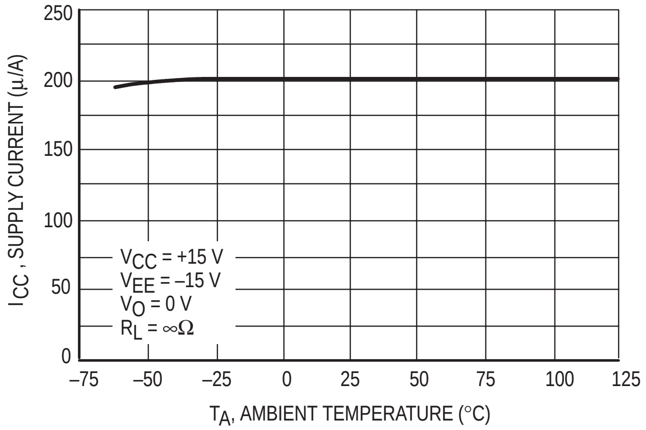


Figure 10. Total Power Dissipation versus Temperature

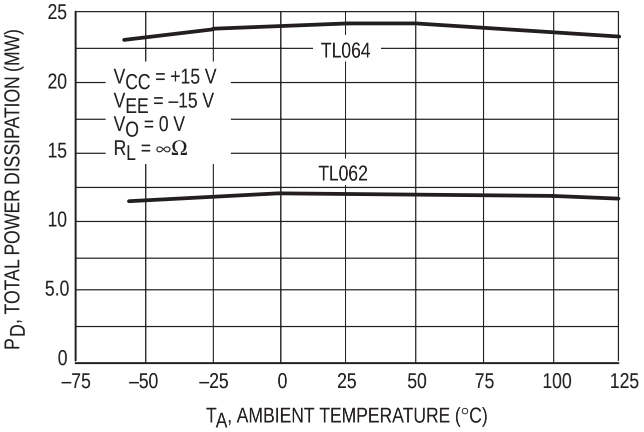


Figure 11. Common Mode Rejection versus Temperature

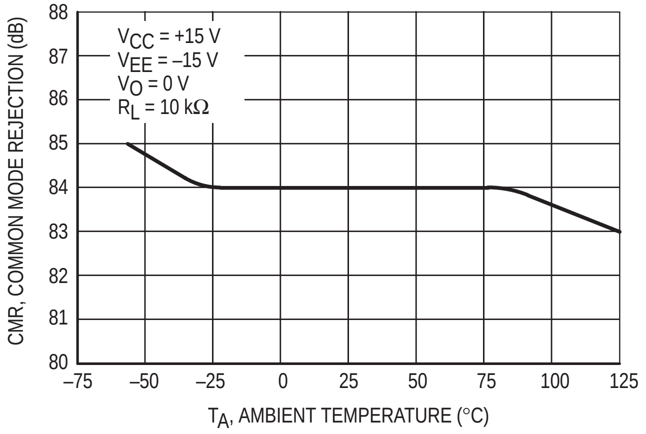


Figure 12. Common Mode Rejection versus Frequency

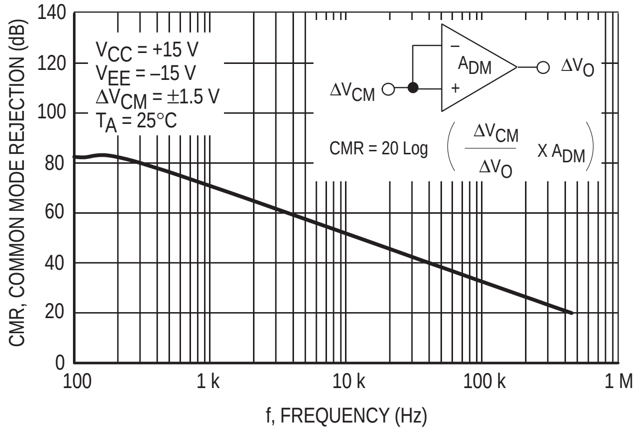


Figure 13. Power Supply Rejection versus Frequency

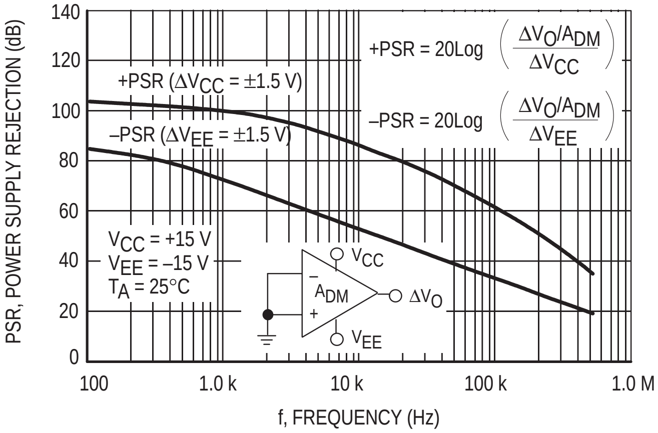


Figure 14. Normalized Gain Bandwidth Product, Slew Rate and Phase Margin versus Temperature

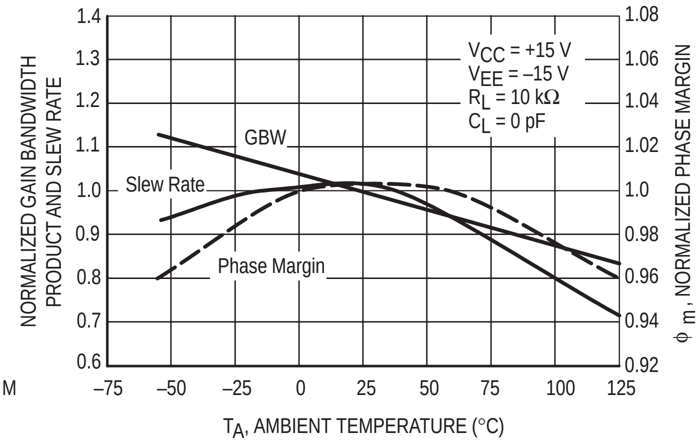


Figure 15. Input Bias Current versus Temperature

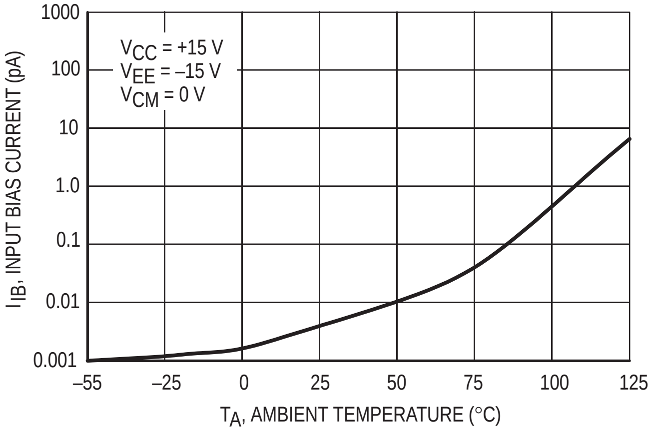


Figure 16. Input Noise Voltage versus Frequency

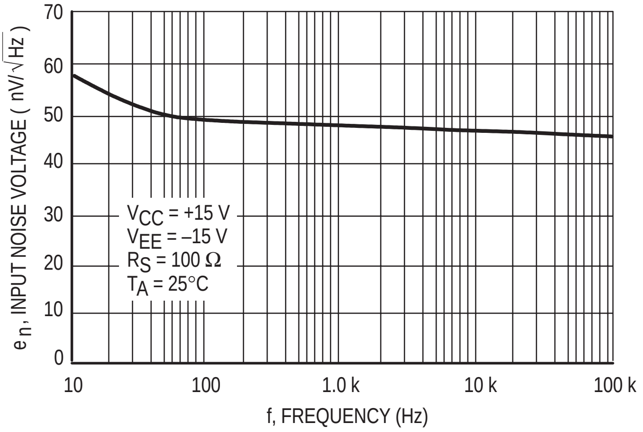


Figure 17. Small Signal Response

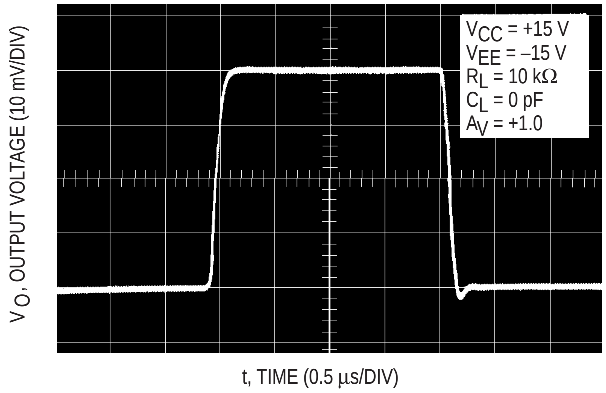


Figure 18. Large Signal Response

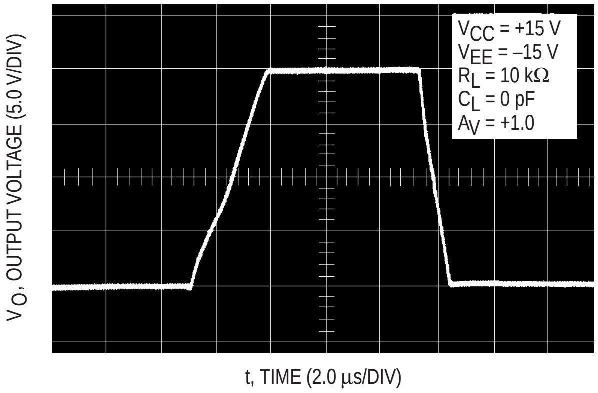


Figure 19. AC Amplifier

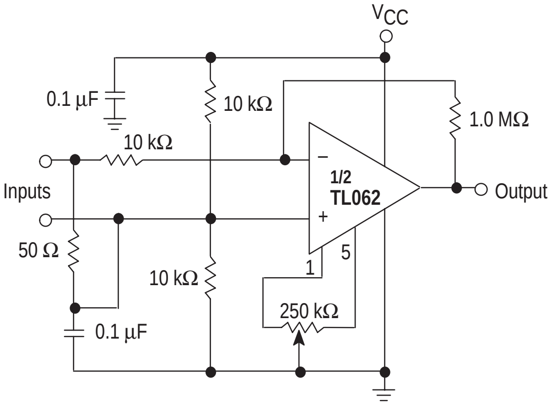


Figure 20. High–Q Notch Filter

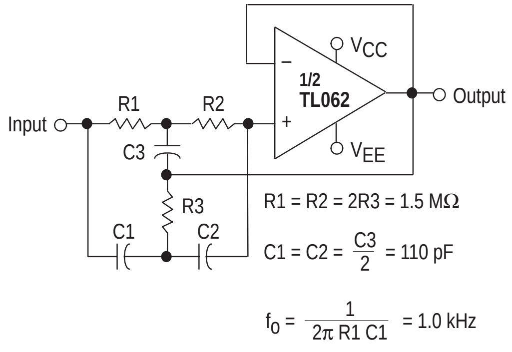


Figure 21. Instrumentation Amplifier

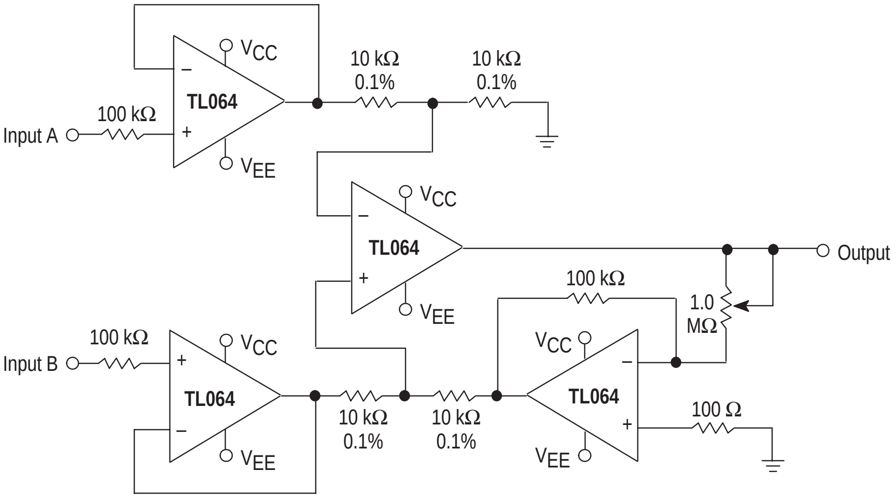


Figure 22. 0.5 Hz Square–Wave Oscillator

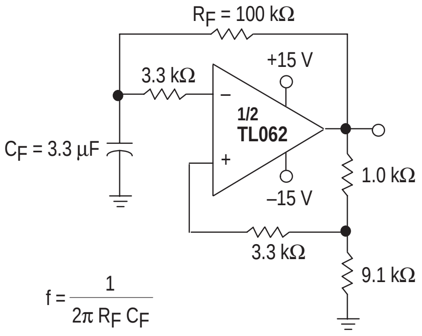
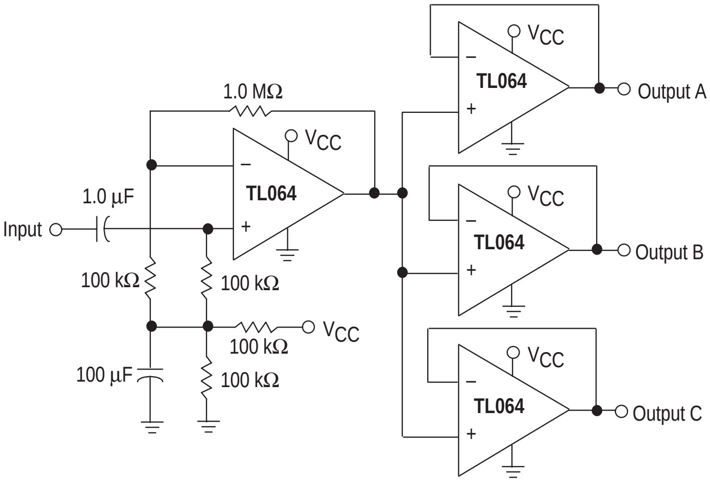


Figure 23. Audio Distribution Amplifier



TL071C,AC
TL072C,AC
TL074C,AC

Low Noise, JFET Input Operational Amplifiers

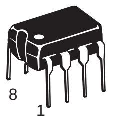
These low noise JFET input operational amplifiers combine two state–of–the–art analog technologies on a single monolithic integrated circuit. Each internally compensated operational amplifier has well matched high voltage JFET input device for low input offset voltage. The BIFET technology provides wide bandwidths and fast slew rates with low input bias currents, input offset currents, and supply currents. Moreover, the devices exhibit low noise and low harmonic distortion, making them ideal for use in high fidelity audio amplifier applications.

These devices are available in single, dual and quad operational amplifiers which are pin–compatible with the industry standard MC1741, MC1458, and the MC3403/LM324 bipolar products.

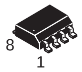
- Low Input Noise Voltage: 18 nV/$\sqrt{Hz}$ Typ
- Low Harmonic Distortion: 0.01% Typ
- Low Input Bias and Offset Currents
- High Input Impedance: 10^{12} Ω Typ
- High Slew Rate: 13 V/µs Typ
- Wide Gain Bandwidth: 4.0 MHz Typ
- Low Supply Current: 1.4 mA per Amp

LOW NOISE, JFET INPUT OPERATIONAL AMPLIFIERS

SEMICONDUCTOR TECHNICAL DATA

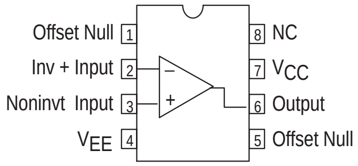


P SUFFIX
PLASTIC PACKAGE
CASE 626

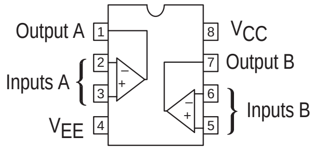


D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

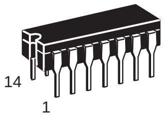
PIN CONNECTIONS



TL071 (Top View)

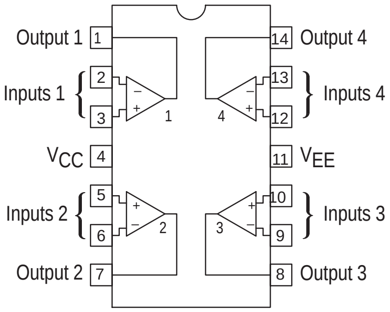


TL072 (Top View)



N SUFFIX
PLASTIC PACKAGE
CASE 646
(TL074 Only)

PIN CONNECTIONS



TL074 (Top View)

ORDERING INFORMATION

Op Amp Function	Device	Operating Temperature Range	Package
Single	TL071ACD, CD	T_A = 0° to +70°C	SO–8
	TL071ACP, CP		Plastic DIP
Dual	TL072ACD, CD	T_A = 0° to +70°C	SO–8
	TL072ACP, CP		Plastic DIP
Quad	TL074ACN, CN	T_A = 0° to +70°C	Plastic DIP

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC} V_{EE}	+18 –18	V
Differential Input Voltage	V_{ID}	±30	V
Input Voltage Range (Note 1)	V_{IDR}	±15	V
Output Short Circuit Duration (Note 2)	t_{SC}	Continuous	
Power Dissipation Plastic Package (N, P) Derate above T_A = +47°C	 P_D $1/\theta_{JA}$	 680 10	 mW mW/°C
Operating Ambient Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

NOTES: 1. The magnitude of the input voltage must not exceed the magnitude of the supply voltage or 15 V, whichever is less.

2. The output may be shorted to ground or either supply. Temperature and/or supply voltages must be limited to ensure that power dissipation ratings are not exceeded.

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = –15 V, T_A = T_{high} to T_{low} [Note 3])

Characteristics	Symbol	Min	Typ	Max	Unit
Input Offset Voltage ($R_S \le$ 10 k, V_{CM} = 0)	V_{IO}				mV
TL071C, TL072C		—	—	13	
TL074C		—	—	13	
TL07_AC		—	—	7.5	
Input Offset Current (V_{CM} = 0) (Note 4)	I_{IO}				nA
TL07_C		—	—	2.0	
TL07_AC		—	—	2.0	
Input Bias Current (V_{CM} = 0) (Note 4)	I_{IB}				nA
TL07_C		—	—	7.0	
TL07_AC		—	—	7.0	
Large–Signal Voltage Gain (V_O = ±10 V, $R_L \ge$ 2.0 k)	A_{VOL}				V/mV
TL07_C		15	—	—	
TL07_AC		25	—	—	
Output Voltage Swing (Peak–to–Peak)	V_O				V
($R_L \ge$ 10 k)		24	—	—	
($R_L \ge$ 2.0 k)		20	—	—	

NOTES: 3. T_{low} = 0°C for TL071C,AC TL072C,AC TL074C,AC T_{high} = +70°C for TL071C,AC TL072C,AC TL074C,AC

4. Input Bias currents of JFET input op amps approximately double for every 10°C rise in junction temperature as shown in Figure 3. To maintain junction temperature as close to ambient temperature as possible, pulse techniques must be used during testing.

Figure 1. Unity Gain Voltage Follower

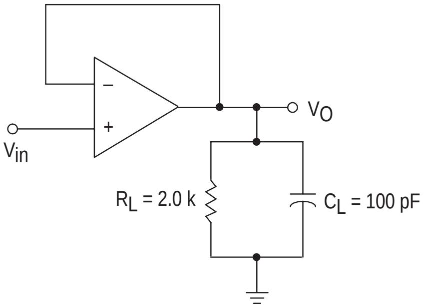
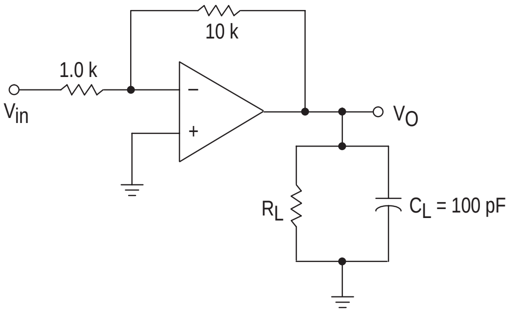


Figure 2. Inverting Gain of 10 Amplifier



ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = –15 V, T_A = 25°C, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Input Offset Voltage ($R_S \leq$ 10 k, V_{CM} = 0)	V_{IO}				mV
TL071C, TL072C		—	3.0	10	
TL074C		—	3.0	10	
TL07_AC		—	3.0	6.0	
Average Temperature Coefficient of Input Offset Voltage R_S = 50 Ω, $T_A = T_{low}$ to T_{high} (Note 3)	$\Delta V_{IO}/\Delta T$	—	10	—	µV/°C
Input Offset Current (V_{CM} = 0) (Note 4)	I_{IO}				pA
TL07_C		—	5.0	50	
TL07_AC		—	5.0	50	
Input Bias Current (V_{CM} = 0) (Note 4)	I_{IB}				pA
TL07_C		—	30	200	
TL07_AC		—	30	200	
Input Resistance	r_i	—	10^{12}	—	Ω
Common Mode Input Voltage Range	V_{ICR}				V
TL07_C		±10	+15, –12	—	
TL07_AC		±11	+15, –12	—	
Large–Signal Voltage Gain (V_O = ±10 V, $R_L \geq$ 2.0 k)	A_{VOL}				V/mV
TL07_C		25	150	—	
TL07_AC		50	150	—	
Output Voltage Swing (Peak–to–Peak) (R_L = 10 k)	V_O	24	28	—	V
Common Mode Rejection Ratio ($R_S \leq$ 10 k)	CMRR				dB
TL07_C		70	100	—	
TL07_AC		80	100	—	
Supply Voltage Rejection Ratio ($R_S \leq$ 10 k)	PSRR				dB
TL07_C		70	100	—	
TL07_AC		80	100	—	
Supply Current (Each Amplifier)	I_D	—	1.4	2.5	mA
Unity Gain Bandwidth	BW	—	4.0	—	MHz
Slew Rate (See Figure 1) V_{in} = 10 V, R_L = 2.0 k, C_L = 100 pF	SR	—	13	—	v/µs
Rise Time (See Figure 1)	t_r	—	0.1	—	µs
Overshoot (V_{in} = 20 mV, R_L = 2.0 k, C_L = 100 pF)	OS	—	10	—	%
Equivalent Input Noise Voltage R_S = 100 Ω, f = 1000 Hz	e_n	—	18	—	$nV/\sqrt{Hz}$
Equivalent Input Noise Current R_S = 100 Ω, f = 1000 Hz	i_n	—	0.01	—	$pA/\sqrt{Hz}$
Total Harmonic Distortion V_O (RMS) = 10 V, $R_S \leq$ 1.0 k, $R_L \geq$ 2.0 k, f = 1000 Hz	THD	—	0.01	—	%
Channel Separation A_V = 100	CS	—	120	—	dB

NOTES: 3. T_{low} = 0°C for TL071C,AC
TL072C,AC
TL074C,AC

T_{high} = +70°C for TL071C,AC
TL072C,AC
TL074C,AC

4. Input Bias currents of JFET input op amps approximately double for every 10°C rise in junction temperature as shown in Figure 3. To maintain junction temperature as close to ambient temperature as possible, pulse techniques must be used during testing.

Figure 3. Input Bias Current versus Temperature

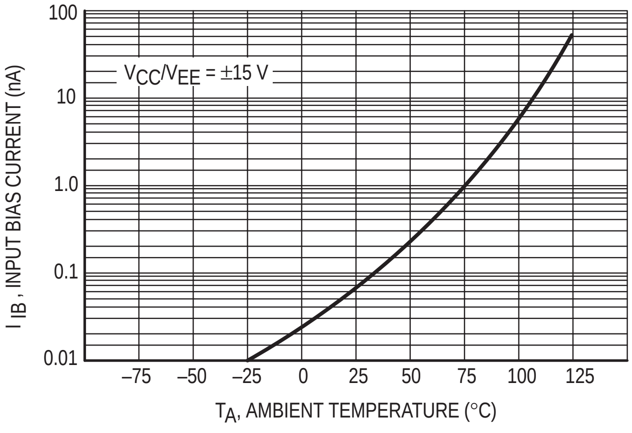


Figure 4. Output Voltage Swing versus Frequency

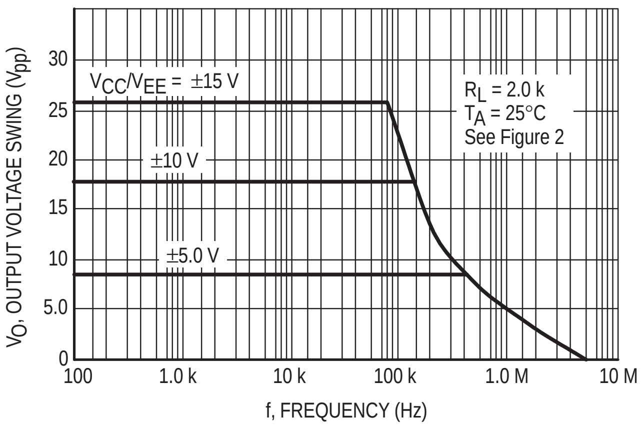


Figure 5. Output Voltage Swing versus Load Resistance

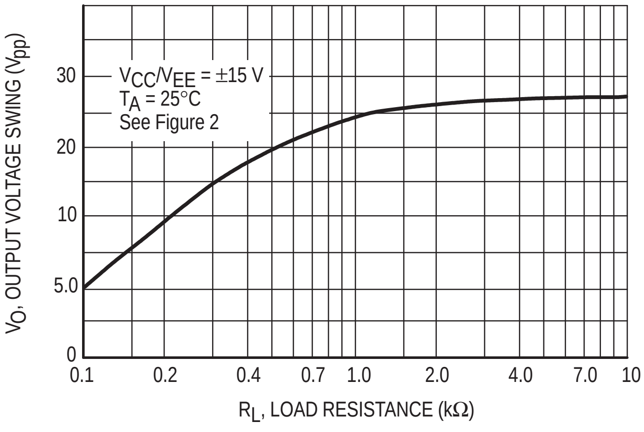


Figure 6. Output Voltage Swing versus Supply Voltage

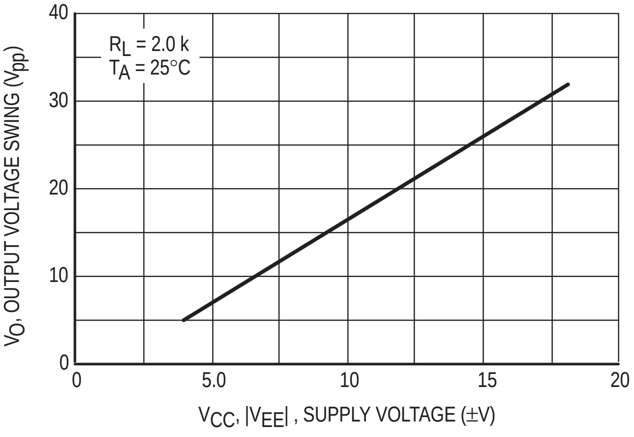


Figure 7. Output Voltage Swing versus Temperature

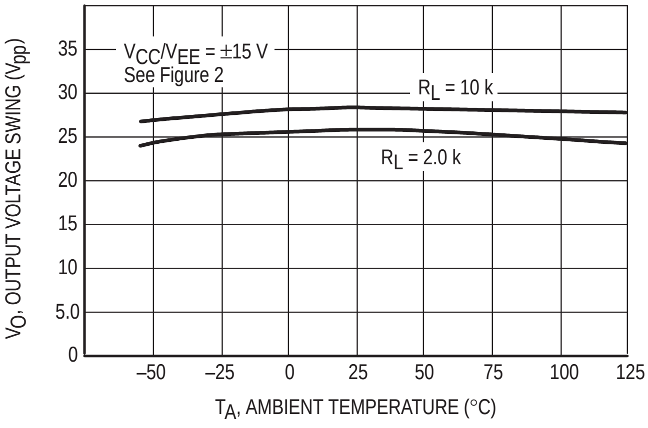


Figure 8. Supply Current per Amplifier versus Temperature

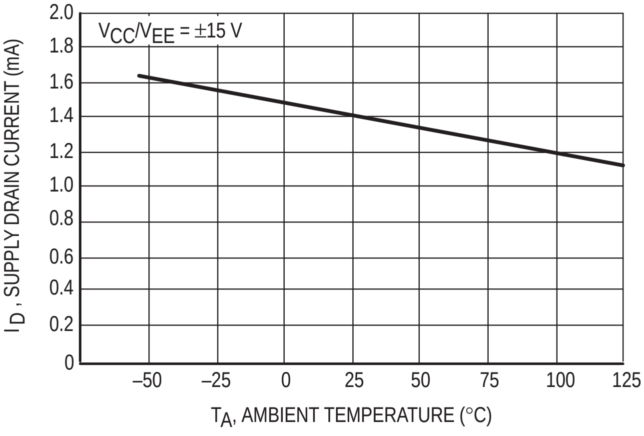


Figure 9. Large Signal Voltage Gain and Phase Shift versus Frequency

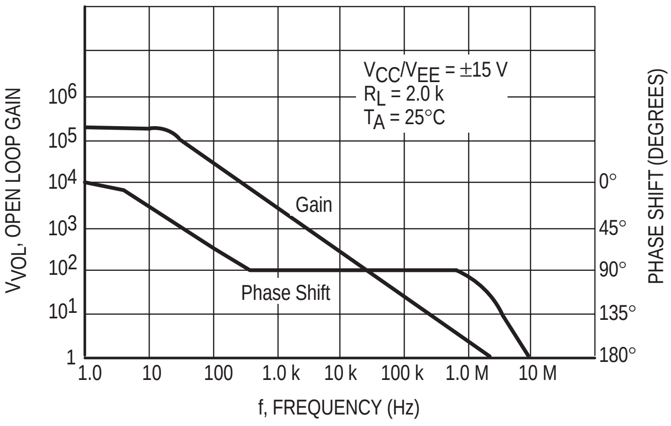


Figure 10. Large Signal Voltage Gain versus Temperature

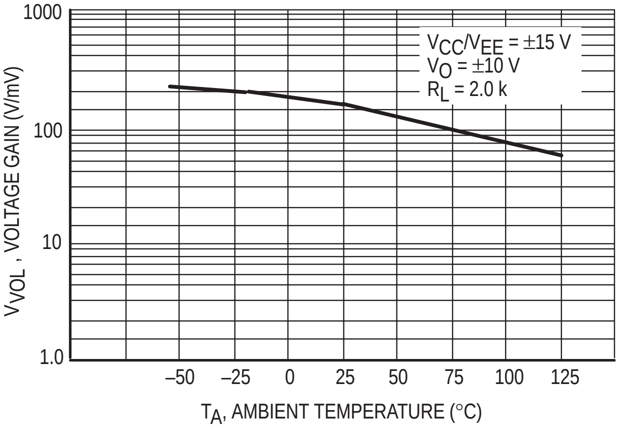


Figure 11. Normalized Slew Rate versus Temperature

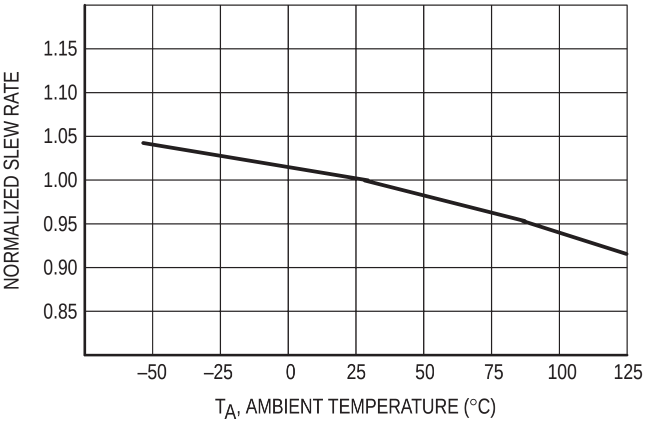


Figure 12. Equivalent Input Noise Voltage versus Frequency

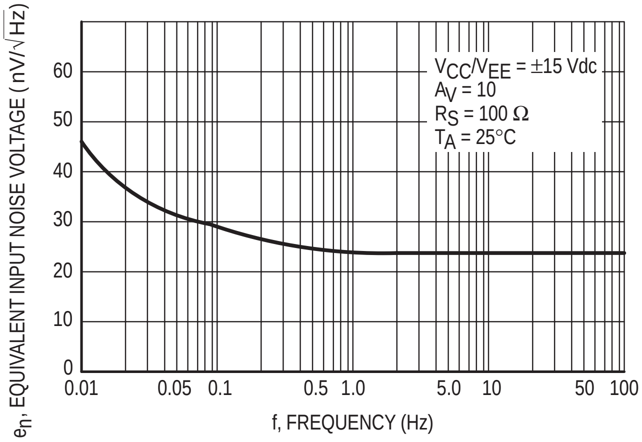
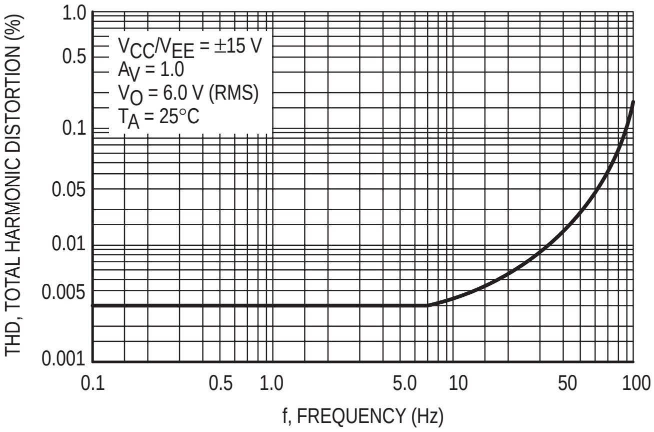


Figure 13. Total Harmonic Distortion versus Frequency



Representative Schematic Diagram

(Each Amplifier)

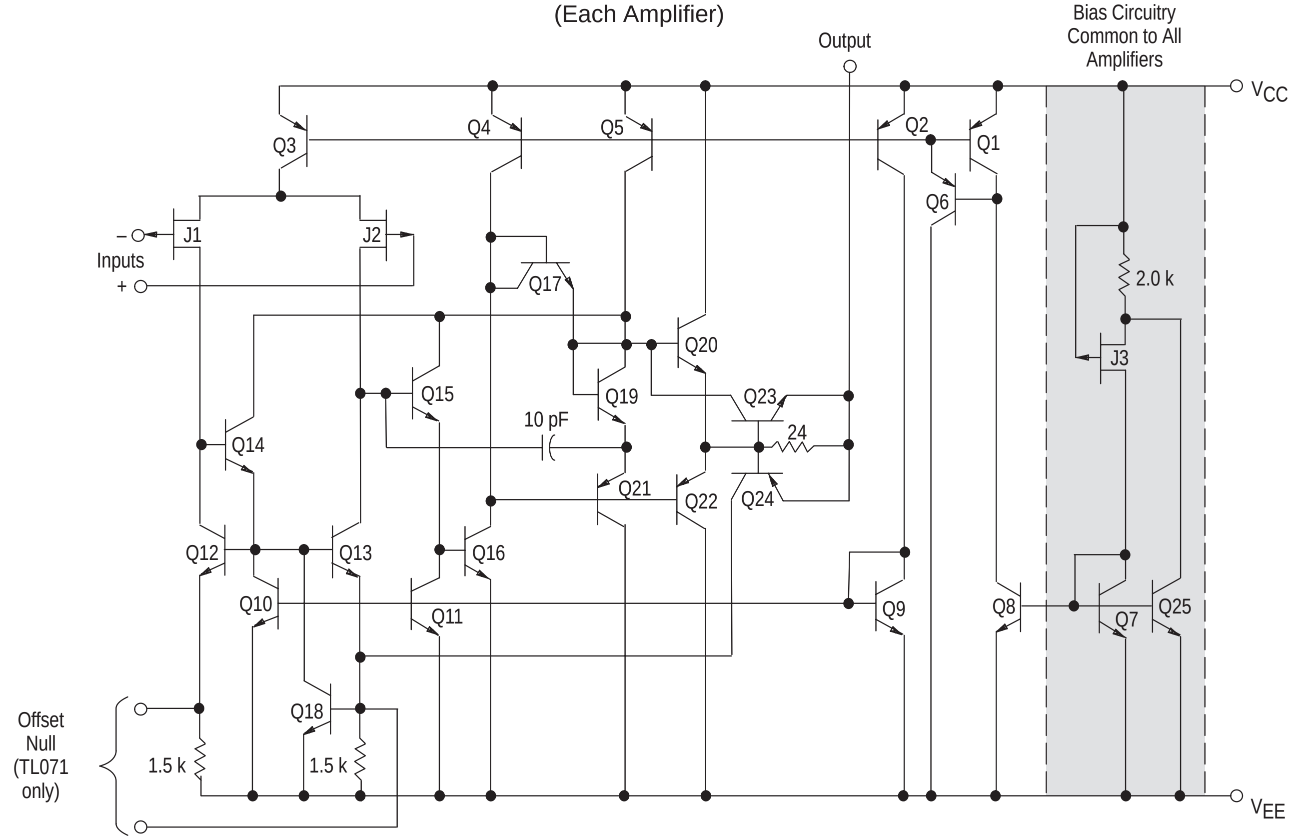
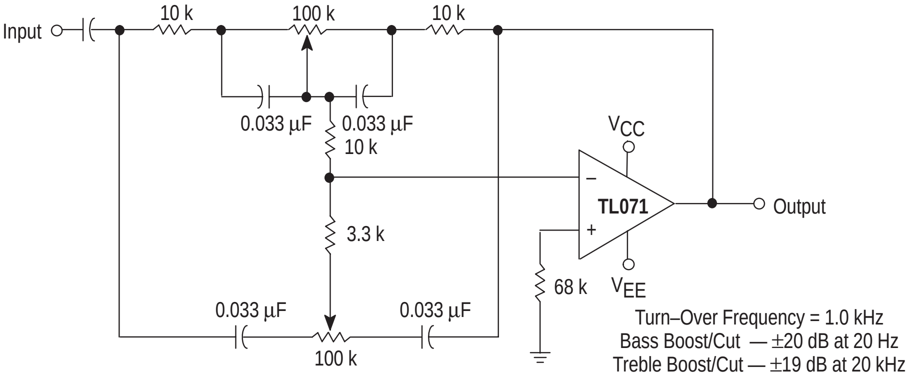
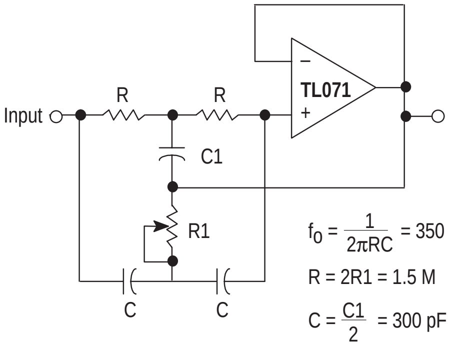


Figure 14. Audio Tone Control Amplifier



Turn–Over Frequency = 1.0 kHz
Bass Boost/Cut — ±20 dB at 20 Hz
Treble Boost/Cut — ±19 dB at 20 kHz

Figure 15. High Q Notch Filter



$f_0 = \frac{1}{2\pi RC} = 350$ Hz

R = 2R1 = 1.5 M

$C = \frac{C1}{2} = 300$ pF

MOTOROLA

TL081C,AC
TL082C,AC
TL084C,AC

JFET Input Operational Amplifiers

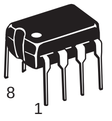
JFET INPUT OPERATIONAL AMPLIFIERS

SEMICONDUCTOR
TECHNICAL DATA

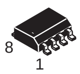
These low–cost JFET input operational amplifiers combine two state–of–the–art linear technologies on a single monolithic integrated circuit. Each internally compensated operational amplifier has well matched high voltage JFET input devices for low input offset voltage. The BIFET technology provides wide bandwidths and fast slew rates with low input bias currents, input offset currents, and supply currents.

These devices are available in single, dual and quad operational amplifiers which are pin–compatible with the industry standard MC1741, MC1458, and the MC3403/LM324 bipolar products.

- Input Offset Voltage Options of 6.0 mV and 15 mV Max
- Low Input Bias Current: 30 pA
- Low Input Offset Current: 5.0 pA
- Wide Gain Bandwidth: 4.0 MHz
- High Slew Rate: 13 V/µs
- Low Supply Current: 1.4 mA per Amplifier
- High Input Impedance: 10^{12} Ω

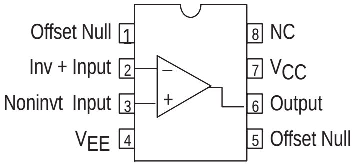


P SUFFIX
PLASTIC PACKAGE
CASE 626

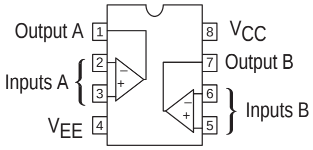


D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

PIN CONNECTIONS

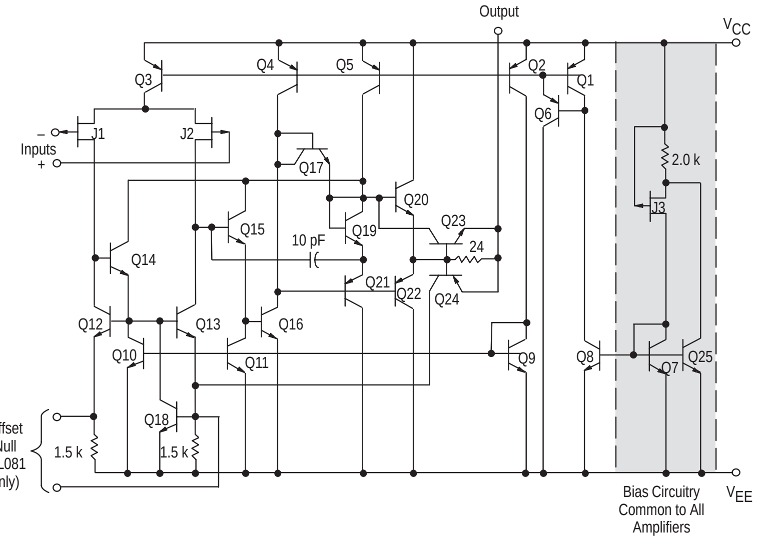


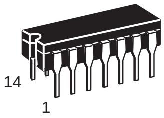
TL081 (Top View)



TL082 (Top View)

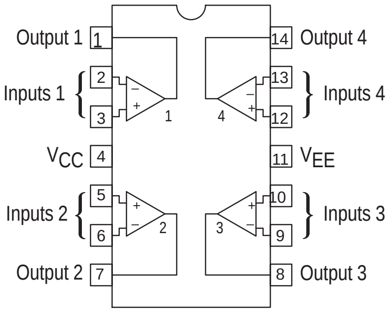
Representative Circuit Schematic (Each Amplifier)





N SUFFIX
PLASTIC PACKAGE
CASE 646

PIN CONNECTIONS



TL084 (Top View)

ORDERING INFORMATION

Op Amp Function	Device	Operating Temperature Range	Package
Single	TL081ACD, CD	T_A = 0° to +70°C	SO–8
	TL081ACP, CP		Plastic DIP
Dual	TL082ACD, CD	T_A = 0° to +70°C	SO–8
	TL082ACP, CP		Plastic DIP
Quad	TL084ACN, CN	T_A = 0° to +70°C	Plastic DIP

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC} V_{EE}	+18 –18	V
Differential Input Voltage	V_{ID}	±30	V
Input Voltage Range (Note 1)	V_{IDR}	±15	V
Output Short Circuit Duration (Note 2)	t_{SC}	Continuous	
Power Dissipation Plastic Package (N, P) Derate above T_A = +47°C	 P_D $1/\theta_{JA}$	 680 10	 mW mW/°C
Operating Ambient Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

NOTES: 1. The magnitude of the input voltage must not exceed the magnitude of the supply voltage or 15 V, whichever is less.

2. The output may be shorted to ground or either supply. Temperature and/or supply voltages must be limited to ensure that power dissipation ratings are not exceeded.

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = –15 V, T_A = T_{low} to T_{high} [Note 3].)

Characteristics	Symbol	Min	Typ	Max	Unit
Input Offset Voltage (R_S ≤ 10 k, V_{CM} = 0)	V_{IO}				mV
TL081C, TL082C		—	—	20	
TL084C		—	—	20	
TL08_AC		—	—	7.5	
Input Offset Current (V_{CM} = 0) (Note 4)	I_{IO}				nA
TL08_C		—	—	5.0	
TL08_AC		—	—	3.0	
Input Bias Current (V_{CM} = 0) (Note 4)	I_{IB}				nA
TL08_C		—	—	10	
TL08_AC		—	—	7.0	
Large–Signal Voltage Gain (V_O= ±10 V,R_L ≥ 2.0 k)	A_{VOL}				V/mV
TL08_C		15	—	—	
TL08_AC		25	—	—	
Output Voltage Swing (Peak–to–Peak)	V_O				V
(R_L ≥ 10 k)		24	—	—	
(R_L ≥ 2.0 k)		20	—	—	

NOTES: 3. T_{low} = 0°C for TL081AC,C
TL082AC,C
TL084AC,C

T_{high} = +70°C for TL081AC
TL082AC,C
TL084AC,C

4. Input Bias currents of JFET input op amps approximately double for every 10°C rise in Junction Temperature as shown in Figure 3. To maintain junction temperature as close to ambient temperature as possible, pulse techniques must be used during testing.

Figure 1. Unity Gain Voltage Follower

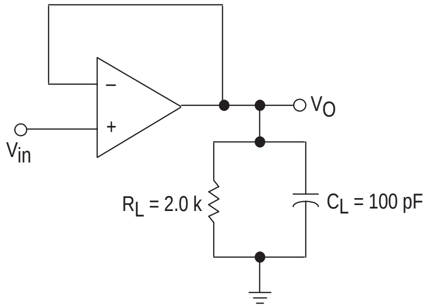
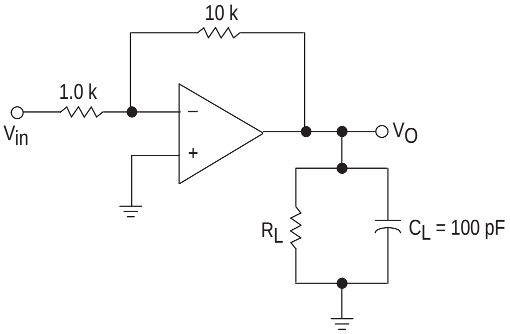


Figure 2. Inverting Gain of 10 Amplifier



ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = –15 V, T_A = +25°C, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Input Offset Voltage ($R_S \le$ 10 k, V_{CM} = 0) TL081C, TL082C TL084C TL08_AC	V_{IO}	 — — —	 5.0 5.0 3.0	 15 15 6.0	mV
Average Temperature Coefficient of Input Offset Voltage R_S = 50 Ω, T_A = T_{low} to T_{high} (Note 3)	$\Delta V_{IO}/\Delta T$	—	10	—	μV/°C
Input Offset Current (V_{CM} = 0) (Note 4) TL08_C TL08_AC	I_{IO}	 — —	 5.0 5.0	 200 100	pA
Input Bias Current (V_{CM} = 0) (Note 4) TL08_C TL08_AC	I_{IB}	 — —	 30 30	 400 200	pA
Input Resistance	r_i	—	10^{12}	—	Ω
Common Mode Input Voltage Range TL08_C TL08_AC	V_{ICR}	 ±10 ±11	 +15, –12 +15, –12	 — —	V
Large Signal Voltage Gain (V_O = ±10 V, $R_L \ge$ 2.0 k) TL08_C TL08_AC	A_{VOL}	 25 50	 150 150	 — —	V/mV
Output Voltage Swing (Peak–to–Peak) (R_L = 10 k)	V_O	24	28	—	V
Common Mode Rejection Ratio ($R_S \le$ 10 k) TL08_C TL08_AC	CMRR	 70 80	 100 100	 — —	dB
Supply Voltage Rejection Ratio ($R_S \le$ 10 k) TL08_C TL08_AC	PSRR	 70 80	 100 100	 — —	dB
Supply Current (Each Amplifier)	I_D	—	1.4	2.8	mA
Unity Gain Bandwidth	BW	—	4.0	—	MHz
Slew Rate (See Figure 1) V_{in} = 10 V, R_L = 2.0 k, C_L = 100 pF	SR	—	13	—	V/μs
Rise Time (See Figure 1)	t_r	—	0.1	—	μs
Overshoot (V_{in} = 20 mV, R_L = 2.0 k, C_L = 100 pF)	OS	—	10	—	%
Equivalent Input Noise Voltage R_S = 100 Ω, f = 1000 Hz	e_n	—	25	—	$nV/\sqrt{Hz}$
Channel Separation A_V = 100	CS	—	120	—	dB

NOTES: 3. T_{low} = 0°C for TL081AC,C
TL082AC,C
TL084AC,C

T_{high} = +70°C for TL081AC
TL082AC,C
TL084AC,C

4. Input Bias currents of JFET input op amps approximately double for every 10°C rise in Junction Temperature as shown in Figure 3. To maintain junction temperature as close to ambient temperature as possible, pulse techniques must be used during testing.

Figure 3. Input Bias Current versus Temperature

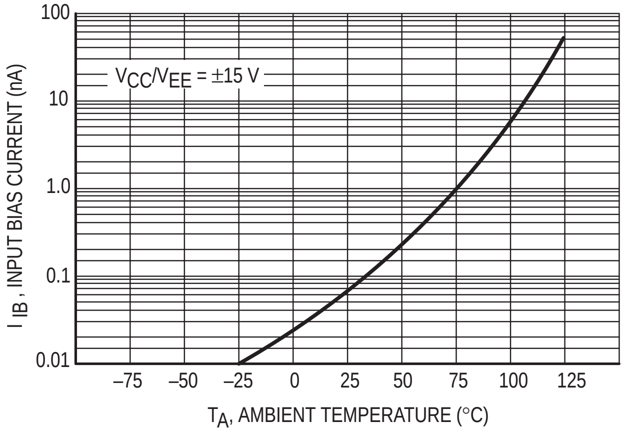


Figure 4. Output Voltage Swing versus Frequency

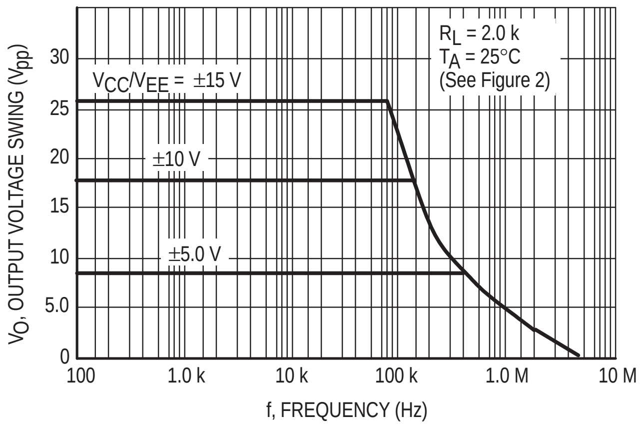


Figure 5. Output Voltage Swing versus Load Resistance

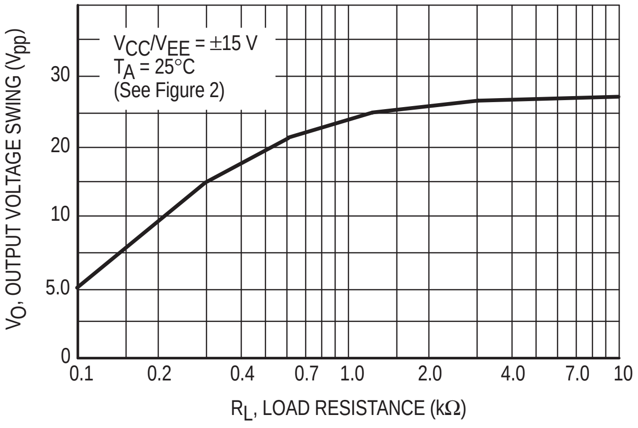


Figure 6. Output Voltage Swing versus Supply Voltage

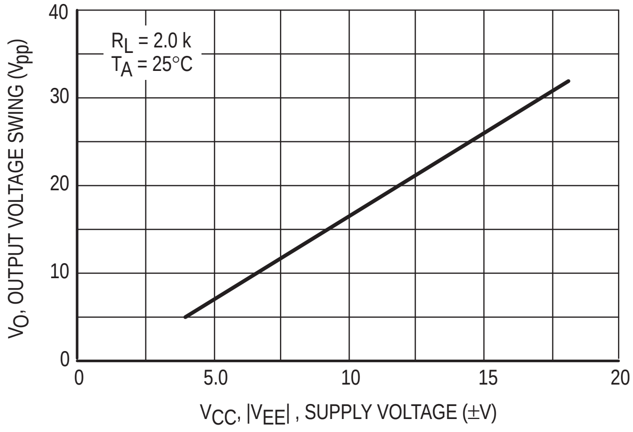


Figure 7. Output Voltage Swing versus Temperature

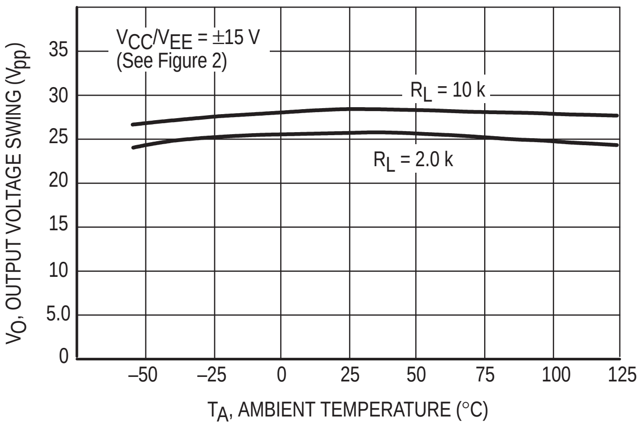


Figure 8. Supply Current per Amplifier versus Temperature

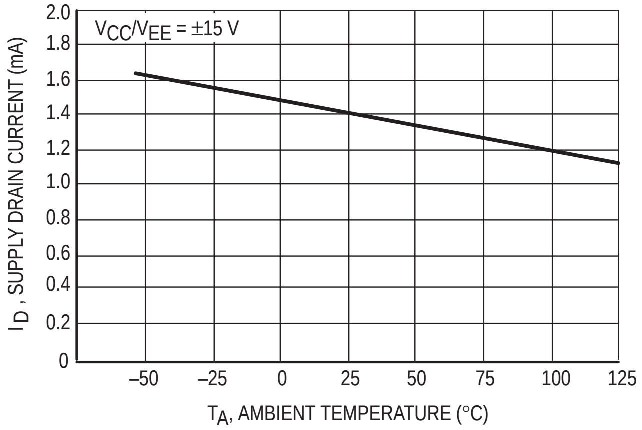


Figure 9. Large Signal Voltage Gain and Phase Shift versus Frequency

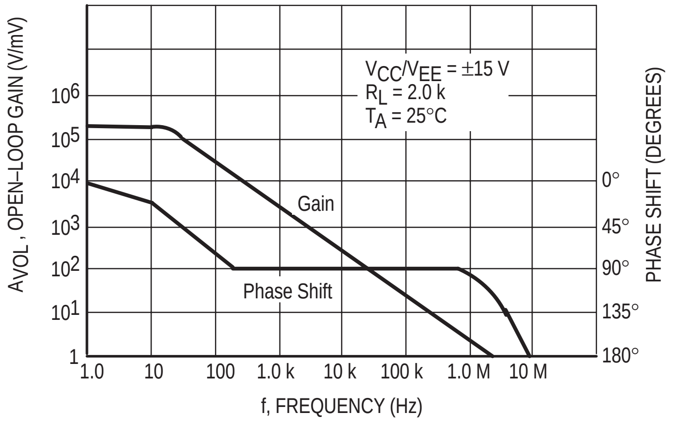


Figure 10. Large Signal Voltage Gain versus Temperature

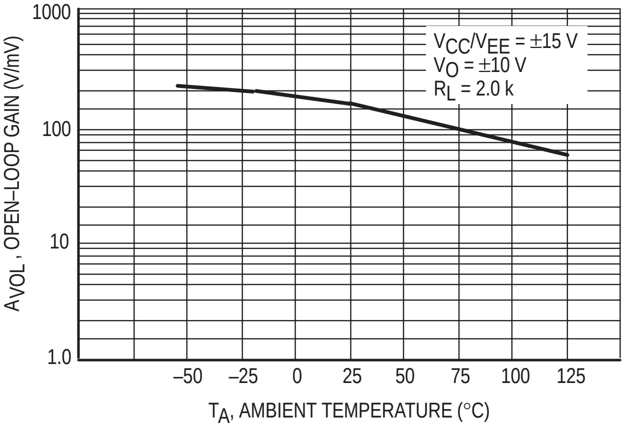


Figure 11. Normalized Slew Rate versus Temperature

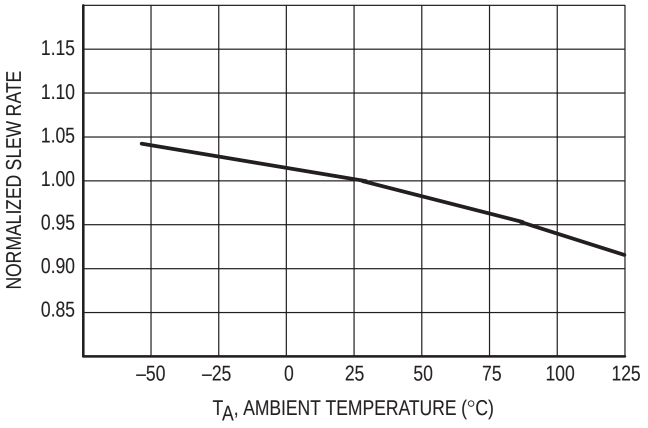


Figure 12. Equivalent Input Noise Voltage versus Frequency

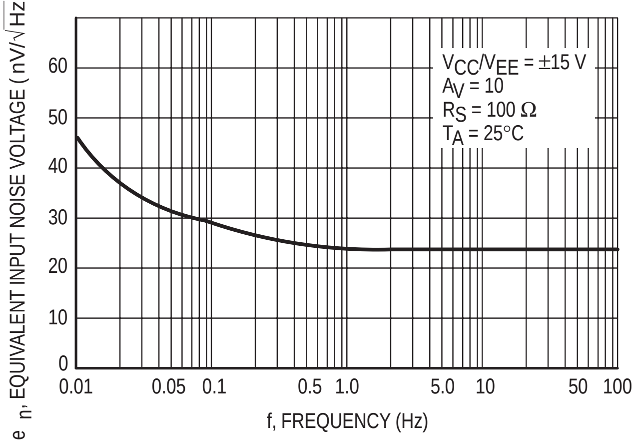


Figure 13. Total Harmonic Distortion versus Frequency

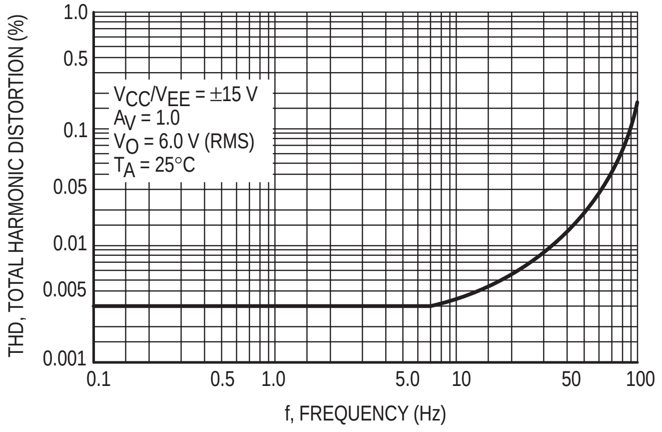
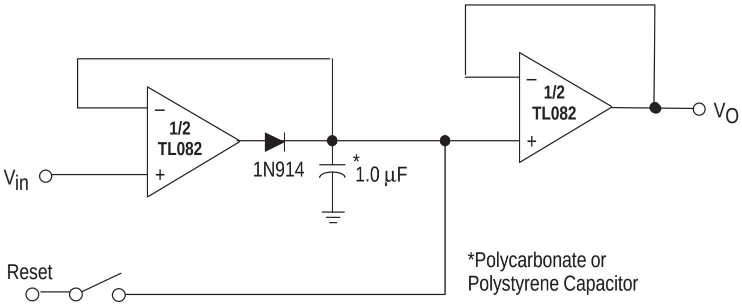
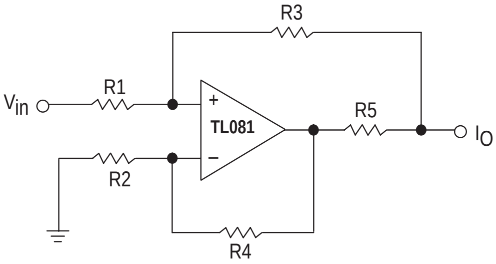


Figure 14. Positive Peak Detector



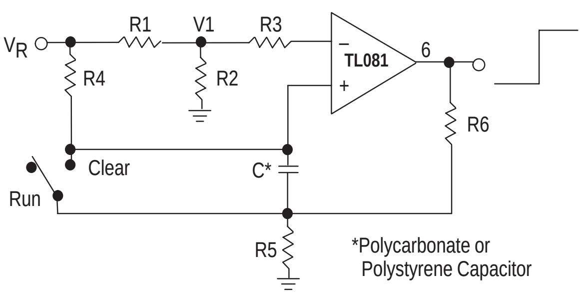
*Polycarbonate or
Polystyrene Capacitor

Figure 15. Voltage Controlled Current Source



If R1 through R4 > > R5 then $I_{out} = \frac{V_{in}}{R5}$

Figure 16. Long Interval RC Timer

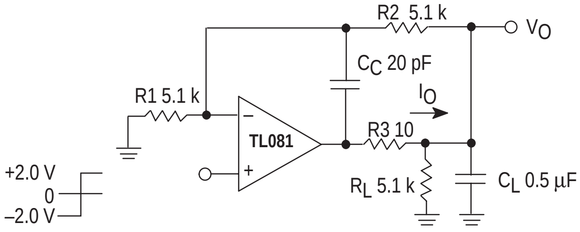


*Polycarbonate or
Polystyrene Capacitor

Time (t) = R4 Cℓn ($V_R/V_R–V_I$), $R_3 = R_4$, $R_5 = 0.1\ R_6$
If R1 = R2: t = 0.693 R4C

Design Example: 100 Second Timer
V_R = 10 V C = 1.0 mF R3 = R4 = 144 M
R6 = 20 k R5 = 2.0 k R1 = R2 = 1.0 k

Figure 17. Isolating Large Capacitive Loads



- Overshoot $< 10\%$
- t_S = 10 µs
- When driving large C_L, the V_O slew rate is determined by C_L and $I_{O(max)}$:

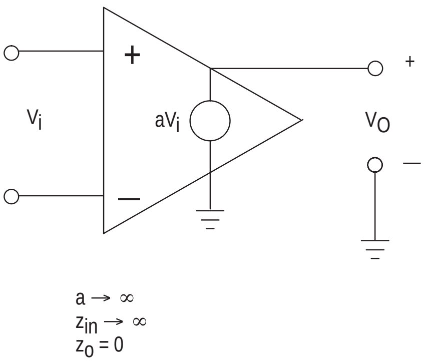
$$\frac{\Delta V_O}{\Delta t} = \frac{I_O}{C_L} \cong \frac{0.02}{0.5}\ \text{V/µs} = 0.04\ \text{V/µs (with } C_L \text{ shown)}$$

Addendum
Operational Amplifier Application Information

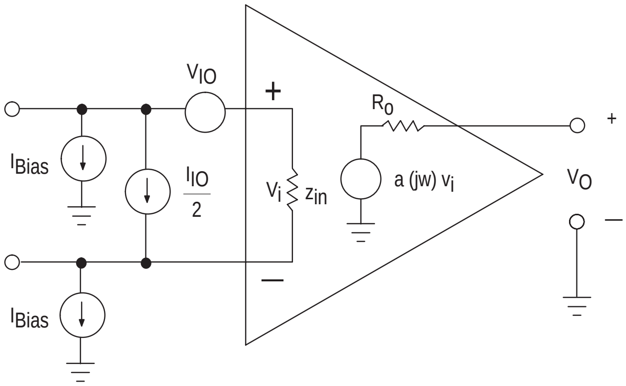
The Ideal Operational Amplifier

An ideal op amp has infinite input impedance, infinite gain, and zero output impedance. Its output is proportional to the differential voltage between the inputs. In reality, slight mismatches between the inputs create an error voltage and current, the input impedance is finite, requiring a small bias current, and gain and operating frequency are limited.

Ideal Op Amp



Equivalent Circuit for Actual Op Amp



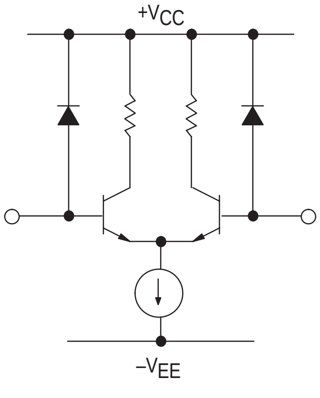
ESD Protection

Newer Motorola devices are equipped with either electrostatic discharge (ESD) diodes or CEO clamps on the inputs to increase their reliability. ESD diodes are connected with the anode attached to the input and the cathode to V_{CC}. During normal operation, the diode should be transparent to the user. However, if the input exceeds V_{CC} by more than a diode drop, the ESD diode will be forward biased and will provide a current path from the input to V_{CC}. Unless the current is limited externally the device could be damaged from overheating.

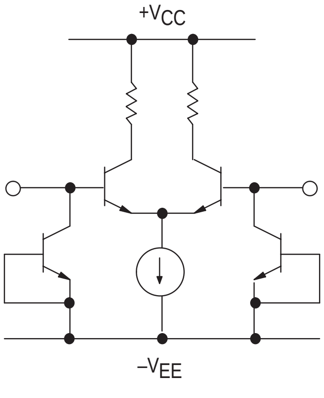
An alternate scheme uses a CEO transistor clamp with the collector connected to the input and the emitter and base connected to V_{EE}. This ESD protection method is totally transparent to the user. Although it is not recommended that the inputs be allowed to exceed V_{CC}, the CEO clamp will not affect device operation. The inputs should never exceed V_{EE}, with or without ESD protection. Single supply op amps are particularly sensitive to damage in a reverse bias condition.

If ESD protection is used on an amplifier, the ESD scheme used will be identified in the data sheet.

ESD Diodes



CEO Clamps



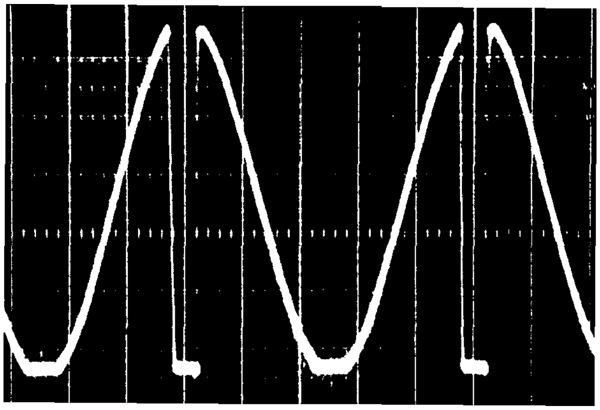
JFET Inputs versus Bipolar Inputs

Although JFET input op amps are generally associated with high speed, there are now bipolar input op amps with comparable slew rates. JFETS do offer higher input impedance and lower input bias current than a typical bipolar input. But for the lowest noise and offset voltage, a bipolar input op amp is a better choice. A bipolar input is also required for true single supply operation. Any op amp can be operated with one supply. But the common mode input voltage range of a single supply op amp includes ground.

Phase Reversal

Most op amp data sheets describe both a maximum input voltage and a minimum common mode input voltage range for the device. The input voltage limit given in the Maximum Ratings Table is considered to be the highest voltage that can be applied without damaging the device. It does not guarantee the device will function normally or within the given electrical specifications. The input common mode voltage range (V_{ICR}), on the other hand, provides the maximum input voltage (for the conditions listed) for normal operation. Exceeding the input common mode range may cause the device to exceed the electrical specifications, latch or go into phase reversal. (As shown in figure at right.)

In a latch condition, the op amp output goes to one of the supply rails, and will remain in that state until the power is removed and reapplied with the error condition corrected. In phase reversal, a normal output low would be seen as an output high, but phase reversal will self correct once the input drops below a certain level. The input voltage required for phase reversal to occur varies, but it is usually seen if the input voltage approaches or exceeds the supply voltage. As you can see in the figure the output is clipping on the negative peaks, and phase reversing on the positive peaks. But as the input drops on the negative going part of the waveform, the output returns the the correct state without powering down the device.



Thermal Considerations

Thermal resistance (θ_{JA}) information is given on most packages in the back of the data book. Low power op amps can handle a short circuit current condition indefinitely. Since some of the higher current drive op amps can deliver a hundred milliamps to an amp in a short circuit condition, extra care is needed to ensure that the maximum junction temperature of the part is not exceeded.

$T_J = T_A + P_D Q_{JA}$

T_J = Junction Temperature (Should not exceed 150°C)

T_A = Ambient Temperature

P_D = Power Dissipation

Q_A = Package Thermal Impedance

Stability and Compensation

Most op amps are internally compensated, enabling them to be used in a unity gain configuration. Uncompensated or decompensated amplifiers have a higher slew rate if no external compensation capacitor is used, but must either be used in a gain of 2 or more or with positive feedback to ensure stable operation. When externally compensating an amplifier, use a capacitor equal or greater than the value recommended in the data sheet. Since the external loop affects the stability of the op amp, the amplifier needs to be evaluated in the circuit and over temperature to determine the minimum amount of compensation required.

Insufficient compensation will cause a high frequency oscillation — higher than the unity gain frequency of the device. This high frequency oscillation is indicative of an instability in the Miller loop, internal to the device. Lower frequency oscillation (below the unity gain frequency of the amplifier) is generally caused by an instability in the outer loop.

The two primary causes of low frequency oscillation are capacitive loading on the output and high differential source resistance. Capacitive loading, which can be either distributed capacitance or an actual load capacitor, can be a problem with as little as 100 pF. Sensitivity to load capacitance varies from op amp to op amp and is not always given in the data sheets. To compensate for capacitive loading, add a small resistor in series with the output. Depending on the load and the external loop, 10 Ω to 100 Ω is generally sufficient (see Figure A). For high capacitive loading, (C_L>1500 pF) a capacitor in the feedback loop may also be necessary (see Figure B).

Keeping the differential source resistance low not only limits the noise generated in the circuit, but avoids stability problems as well. Most op amps are stable with a source resistance of up to 2 kΩ, but will vary from op amp to op amp. The differential source resistance (which includes any feedback resistance) combines with the input capacitance of the op amp to create a low frequency pole. The higher the resistance, the more likely you are to have an oscillation problem. Adding a small capacitor in parallel with the feedback resistor may solve the problem (see Figure C). The capacitor should be greater than the input capacitance of the op amp which is typically about 10 pF.

Figure A. Compensation Circuit for Moderate Capacitive Loads

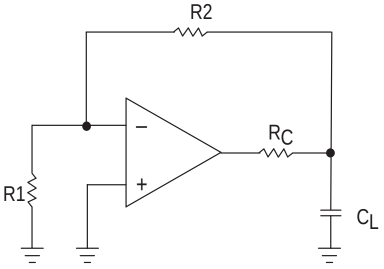


Figure B. Compensation Circuit for High Capacitive Loads

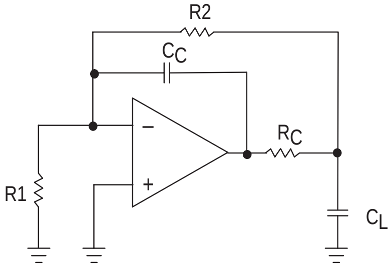
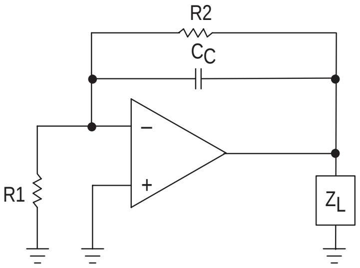


Figure C. Compensation for High Source Impedance



Layout Considerations

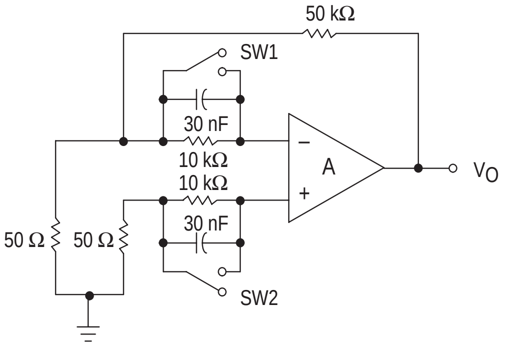
Higher frequency op amps may require special attention to layout. Since most layout problems are not reflected in computer simulations, it is worth it to follow proper layout rules consistently. Some suggestions:

- *Always* bypass the supply pins with at least 0.01 µF to ground, whether or not it is a high frequency application. Some amplifiers have a much lower power supply rejection with respect to the negative supply than to the positive supply due to the internal compensation. A larger bypass capacitor from V_{EE} to ground may be used to prevent high frequency transients from appearing on the output. Generally 10 µF to 20 µF is sufficient.
- Make sure you have a good ground plane.
- Keep AC and DC grounds separate.
- Don't use proto boards or wire wrap for high frequency circuits.
- Use appropriate external components — avoid electrolytics in high frequency paths.
- Keep high frequency paths short (including the leads on discrete components).
- Ground the inputs of unused op amps.

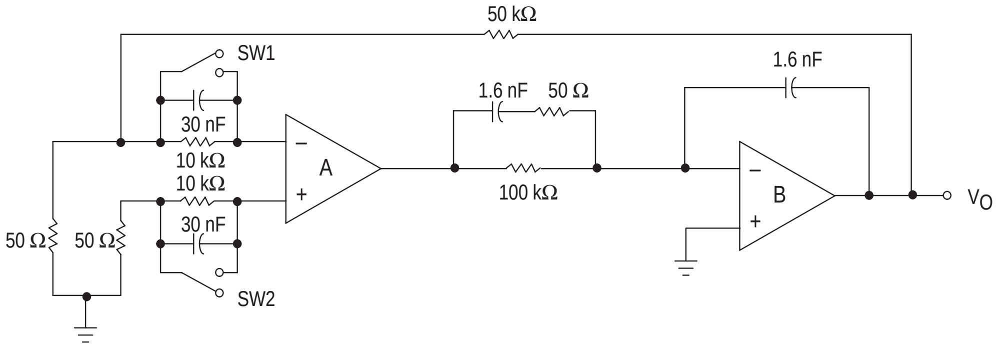
Test Information

The following circuit can be used to test V_{IO}, I_{IO}, and I_{IB}. Op Amp A is the device under test, and Op Amp B is a buffer amplifier which reduces CMRR errors and improves the accuracy of the measurement. The 30 nF capacitors across the 10k Ω source resistors are for stability and may not be needed.

A) Without Buffer Amplifier



B) With Buffer Amplifier



V_{IO} can be measured directly with SW1 and SW2 closed.

To determine I_{IB-}:

- Measure V_{IO} with both switches close,
- Open SW1 only; Measure V_{IO1}

To determine I_{IB+}:

- Close SW1 and open SW2; Measure V_{IO2}

  I_{IO} equals the difference between I_{IB+} and I_{IB-}

GLOSSARY

Input Offset Voltage (V_{IO}) — The voltage which must be applied between the inputs of an op amp to obtain a zero output voltage. For an ideal op amp, V_{IO} would be zero. Some vendors abbreviate it V_{OS}.

Input Bias Current (I_{IB}) — The current flowing in or out of both inputs of an op amp. JFET input op amps provide the lowest input bias current; typically in the picoamp range. A bipolar input op amp is typically in nanoamps. I_{IB} is highly sensitive to slight process variations and can vary an order of magnitude.

Input Offset Current (I_{IO}) — Ideally, the bias currents on the two inputs are equal. The input offset current is the difference between the two currents when the output is at zero volts. Sometimes abbreviated I_{OS}. This should not be confused with the output short circuit current (I_{SC}).

Input Common Mode Voltage Range (V_{ICR}) — The maximum input voltage range for normal operation within given specifications. Exceeding the input common mode range generally will not damage the inputs if the maximum ratings are not exceeded. However, V_{IO} may not meet the specification given in the data sheet, and phase reversal may occur as the input voltage approaches V_{CC} or V_{EE}. Sometimes abbreviated V_{CM}.

Common Mode Rejection Ratio (CMR or CMRR) — CMRR is defined as the ratio of the common mode gain to the differential mode gain. It is also equal to the ratio of the input common mode voltage to the peak–to–peak change in V_{IO}. Measures the ability of an op amp to reject a signal present at both inputs simultaneously. May be given in dB or volts per volt.

Power Supply Rejection Ratio (PSR or PSRR) — The ratio of the change in V_{IO} to the change in power supply voltage. Measures the immunity of the amplifier to changes in power supply voltage.

Output Short Circuit Current (I_{SC}) — The maximum current an amplifier can deliver into a short circuit. Care must be exercised to ensure the maximum junction temperature of the device is not exceeded to prevent damage to the device.

Supply Current (I_D or I_{CC}) — The operating current required with no load and with the output at zero volts.

Slew Rate (SR) — The rate of change of the output voltage in response to a large amplitude pulse applied to the input. The slew rate determines the power bandwidth of the device.

Gain Bandwidth Product (GBW) — The product of the closed–loop gain times the frequency response at a given frequency. For an op amp with a single pole roll–off, the gain bandwidth product is equal to the unity gain frequency.

Phase Margin (ϕ_M) — 180° minus the phase shift at the unity gain frequency of the device. The phase margin must be positive for unconditionally stable operation. Phase margin (and stability) are affected by the external circuit, particularly the capacitive loading on the output and the differential source resistance on the input.

Channel Separation (CS) — A measurement of the immunity of one op amp to a signal present on another amplifier in a dual or quad.

Power Bandwidth (BWP) — The frequency at which the output starts to clip or distort at maximum peak–to–peak input voltage.

Power Supply Circuits

In Brief . . .

In most electronic systems, some form of voltage regulation is required. In the past, the task of voltage regulator design was tediously accomplished with discrete devices, and the results were quite often complex and costly. Today, with bipolar monolithic regulators, this task has been significantly simplified. The designer now has a wide choice of fixed, low V_{Diff} and adjustable type voltage regulators. These devices incorporate many built–in protection features, making them virtually immune to the catastrophic failures encountered in older discrete designs.

The switching power supply continues to increase in popularity and is one of the fastest growing markets in the world of power conversion. They offer the designer several important advantages over linear series–pass regulators. These advantages include significant advancements in the areas of size and weight reduction, improved efficiency, and the ability to perform voltage step–up, step–down, and voltage–inverting functions. Motorola offers a diverse portfolio of full featured switching regulator control circuits which meet the needs of today's modern compact electronic equipment.

Power supplies, MPU/MCU–based systems, industrial controls, computer systems and many other product applications are requiring power supervisory functions which monitor voltages to ensure proper system operation. Motorola offers a wide range of power supervisory circuits that fulfill these needs in a cost effective and efficient manner. MOSFET drivers are also provided to enhance the drive capabilities of first generation switching regulators or systems designed with CMOS/TTL logic devices. These drivers can also be used in dc–to–dc converters, motor controllers or virtually any other application requiring high speed operation of power MOSFETs.

Page

Linear Voltage Regulators

Fixed Output

These low cost monolithic circuits provide positive and/or negative regulation at currents from 100 mA to 3.0 A. They are ideal for on–card regulation employing current limiting and thermal shutdown. Low V_{Diff} devices are offered for battery powered systems.

Although designed primarily as fixed voltage regulators, these devices can be used with external components to obtain adjustable voltages and currents.

Table 1. Linear Voltage Regulators

Device	V_{out}	25°C Tol. ±%	V_{in} Max	V_{in}–V_{out} Diff. Typ.	Reg_{line} Max (% V_{out})	Reg_{load} Max (% V_{out})	Typ. Temp. Coefficient $\frac{\text{mV } (V_{out})}{°C}$	Suffix/ Package
Fixed Voltage, 3–Terminal Regulators, 0.1 Amperes								
LM2931*/A–5.0*	5.0	5.0/3.8	40	0.16	0.6	1.0	0.2	D/751, D2T/936, DT, DT–1, T/221A, Z
LP2950C*/AC*	3.0	0.5	30	0.38	0.2/0.1	0.2/0.1	0.04	DT–3.0, Z–3.0
	3.3							DT–3.3, Z–3.3
	5.0							DT–5.0, Z–5.0
MC78LXXC/AC/AB*	5.0, 8.0, 9.0	8.0/4.0	30	1.7	4.0/3.0	1.2	0.2	D/751, P/29
MC78LXXC/AC/AB*	12, 15, 18	8.0/4.0	35	1.7	2.0	1.0	0.2	D/751, P/29
MC78L24C/AC/AB*	24	8.0/4.0	40	1.7	2.0	1.0	0.2	D/751, P/29
MC79L05C/AC/AB*	–5.0	8.0/4.0	30	1.7	4.0/3.0	1.2	0.2	D/751, P/29
MC79LXXC/AC/AB*	–(12, 15, 18)	8.0/4.0	35	1.7	2.0	1.0	0.2	D/751, P/29
MC79L24C/AC/AB*	–24	8.0/4.0	40	1.7	2.0	1.0	0.2	D/751, P/29
MC33160**	5.0	5.0	40	2.0	0.8	1.0	–	P/626
Fixed Voltage, 3–Terminal Regulators, 0.5 Amperes								
MC78MXXB*/C	5.0, 6.0, 8.0, 12	4.0	35	2.0	1.0	2.0	±0.04	DT, DT–1, T/221A
MC78MXXB*/C	15, 18	4.0	35	2.0	1.0	2.0	±0.04	DT, DT–1, T/221A
MC78MXXB*/C	20, 24	4.0	40	2.0	0.25	2.0	±0.04	DT, DT–1, T/221A
MC79MXXB*/C	–(5.0, 8.0, 12, 15)	4.0	35	1.1	1.0	2.0	–0.07 to ±0.04	DT, DT–1, T/221A
MC33267*	5.05	2.0	40	0.58	1.0	1.0	–	D2T/936A, T/314D, TV
Fixed Voltage, 3–Terminal Medium Dropout Regulators, 0.8 Amperes								
MC33269–XX*	3.3, 5.0, 12	1.0	20	1.0	0.3	1.0	–	D/751, DT, T/221A
MC34268	2.85	1.0	15	0.95	0.3	1.0	–	D/751, DT

Unless otherwise noted, T_J = 0° to +125°C

* T_J = –40° to +125°C

** T_A = –40° to +85°C

Table 1. Linear Voltage Regulators **(continued)**

Device	V_{out}	25°C Tol. ±%	V_{in} Max	V_{in}–V_{out} Diff. Typ.	Reg_{line} Max (% V_{out})	Reg_{load} Max (% V_{out})	Typ. Temp. Coefficient mV (V_{out})/°C	Suffix/ Package
Fixed Voltage, 3–Terminal Regulators, 1.0 Amperes								
MC78XXB*/C/AC	5.0, 6.0, 8.0, 12, 18	4.0/2.0	35	2.0	2.0/1.0	2.0	–0.06 to –0.22	D2T/936, T/221A
MC7824B*/C/AC	24	4.0/2.0	40	2.0	2.0/1.0	2.0/0.4	0.125	D2T/936, T/221A
MC79XXC/AC	–(5.0, 5.2, 6.0)	4.0/2.0	35	2.0	2.0/1.0	2.0	–0.2	D2T/936, T/221A
MC79XXC/AC	–(8.0, 12, 15, 18)	4.0/2.0	35	2.0	2.0/1.0	2.0/1.25	–0.12 to –0.06	D2T/936, T/221A
MC7924C	–24	4.0	40	2.0	1.0	2.0	–0.04	D2T/936, T/221A
LM340/A–XX	5.0, 6.0, 12, 15, 18	4.0/2.0	35	1.7	1.0/0.2	1.0/0.5	±0.12	T/221A
LM340–24	24	4.0	40	1.7	1.0	1.0	±0.12	T/221S
TL780–XXC	5.0, 12, 15	1.0	35	2.0	0.10	0.5	0.012	KC
Fixed Voltage, 3–Terminal Regulators, 3.0 Amperes								
MC78TXXC/AC	5.0, 8.0, 12	4.0/2.0	35	2.5	0.5	0.6	0.04	T/221A
MC78T15C/AC	15	4.0/2.0	40	2.5	0.5	0.6	0.04	T/221A
LM323/A	5.0	4.0/2.0	20	2.3	0.5/0.3	2.0/1.0	±0.2	T/221A

Unless otherwise noted, T_J = 0° to +125°C
* T_J = –40° to +125°C
** T_A = –40° to +85°C

Table 2. Fixed Voltage Medium and Low Dropout Regulators

Device	V_{out}	25°C Tol. ±%	I_O (mA) Max	V_{in} Max	V_{in}–V_{out} Diff. Typ.	Reg_{line} Max (% V_{out})	Reg_{load} Max (% V_{out})	Typ. Temp. Coefficient mV (V_{out})/°C	Suffix/ Package
Fixed Voltage, Medium Dropout Regulators									
MC33267*	5.05	2.0	500	40	0.58	1.0	1.0	–	D2T/936A, T/314D, TV
MC34268	2.85	1.0	800	15	0.95	0.3	1.0		D/751, DT
MC33269–XX*	3.3, 5.0, 12			20	1.0				D/751, DT, T/221A
Fixed Voltage, Low Dropout Regulators									
LM2931*/A*	5.0	5.0/3.8	100	37	0.16	1.12	1.0	±2.5	D/751, D2T/936A, DT, DT–1, T/221A, Z
LP2950C*/AC*	3.0	1.0/0.5	100	30	0.38	0.2/0.1	0.2/0.1	0.2	DT–3.0, Z–3.0
	3.3								DT–3.3, Z–3.3
	5.0								DT–5.0, Z–5.0

Unless otherwise noted, T_J = 0° to +125°C
* T_J = –40° to +125°C

Table 2. Fixed Voltage Medium and Low Dropout Regulators (continued)

Device	V_{out}	25°C Tol. ±%	I_O (mA) Max	V_{in} Max	V_{in}–V_{out} Diff. Typ.	Reg_{line} Max (% V_{out})	Reg_{load} Max (% V_{out})	Typ. Temp. Coefficient $\frac{\text{mV } (V_{out})}{°\text{C}}$	Suffix/ Package
Fixed Voltage, Low Dropout Regulators									
LP2951C*/AC*	3.0	1.0/0.5	100	28.75	0.38	0.04/0.02	0.04/0.02	±1.0	D–3.0/751, DM–3.0/ 846A, N–3.0/626
	3.3								D–3.3/751, DM–3.3/ 846A, N–3.3/626
	5.0								D/751, DM/846A, N/626
LM2935*	5.0/5.0	5.0/5.0	500/10	60	0.45/0.55	1.0	1.0	–	D2T/936A, T/314D, TH, TV

Unless otherwise noted, T_J = 0° to +125°C

* T_J = –40° to +125°C

Adjustable Output

Motorola offers a broad line of adjustable output voltage regulators with a variety of output current capabilities. Adjustable voltage regulators provide users the capability of stocking a single integrated circuit offering a wide range of output voltages for industrial and communications applications. The three–terminal devices require only two external resistors to set the output voltage.

Table 3. Adjustable Output Regulators

Device	V_{out}	I_O (mA) Max	V_{in} Max	V_{in}–V_{out} Diff. Typ.	Reg_{line} Max (% V_{out})	Reg_{load} Max (% V_{out})	Typ. Temp. Coefficient $\frac{\text{mV } (V_{out})}{°\text{C}}$	Suffix/ Package
Adjustable Regulators								
LM317L/B*	2.0–37	100	40	1.9	0.07	1.5	±0.35	D/751, Z
LM2931C*	3.0–24	100	37	0.16	1.12	1.0	±2.5	D/751, D2T/936A, T/314D, TH, TV
LP2951C*/AC*	1.25–29	100	28.75	0.38	0.04/0.02	0.04/0.02	±1.0	D–3.0/751, DM–3.0/ 846A, N–3.0/626
								D–3.3/751, DM–3.3/ 846A, N–3.3/626
								D/751, DM/846A, N/626
MC1723C#	2.0–37	150	38	2.5	0.5	0.2	±0.033	D/751, P/646

Unless otherwise noted, T_J = 0° to +125°C

* T_J = –40° to +125°C

\# T_A = 0° to +70°C

Table 3. Adjustable Output Regulators (continued)

Device	V_{out}	I_O (mA) Max	V_{in} Max	V_{in}–V_{out} Diff. Typ.	Reg_{line} Max (% V_{out})	Reg_{load} Max (% V_{out})	Typ. Temp. Coefficient mV (V_{out}) / °C	Suffix/ Package
Adjustable Regulators								
LM317M/B*	1.2–37	500	40	2.1	0.04	0.5	±0.35	DT, DT–1, T/221A
LM337M/B*	–(1.2–37)	500	40	1.9	0.07	1.5	±0.3	T/221A
MC33269*	1.25–19	800	18.75	1.0	0.3	0.5	±0.4	D/751, DT, T/221A
LM317/B*	1.2–37	1500	40	2.25	0.07	1.5	±0.35	D2T/936, T/221A
LM337/B*	–(1.2–37)	1500	40	2.3	0.07	1.5	±0.3	D2T/936, T/221A
LM350/B*	1.2–33	3000	35	2.7	0.07	1.5	±0.5	T/221A

Unless otherwise noted, T_J = 0° to +125°C
* T_J = –40° to +125°C
\# T_A = 0° to +70°C

Micropower Voltage Regulators for Portable Applications

80 mA Micropower Voltage Regulator

MC78LC00H, N

T_A = –30° to +80°C, Case 1213, 1212

The MC78LC00 series voltage regulators are specifically designed for use as a power source for video instruments, handheld communication equipment, and battery powered equipment.

The MC78LC00 series features an ultra–low quiescent of 1.1 µA and a high accuracy output voltage. Each device contains a voltage reference, an error amplifier, a driver transistor and resistors for setting the output voltage. These devices are available in either SOT–89, 3 pin, or SOT–23, 5 pin, surface mount packages.

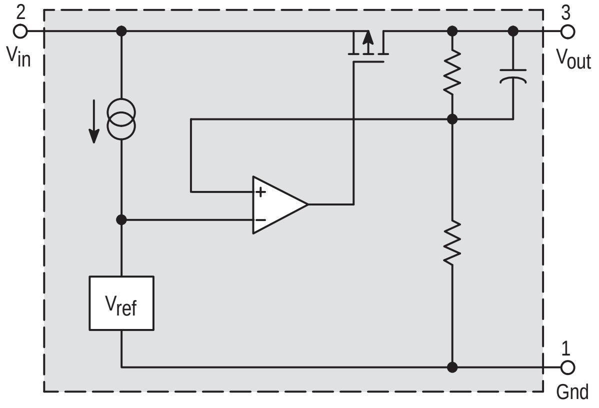
MC78LC00 Series Features:

- Low Quiescent Current of 1.1 µA Typical
- Low Dropout Voltage (30 mV Typical)
- Excellent Line Regulation (0.1%)
- High Accuracy Output Voltage (±2.5%)
- Wide Output Voltage Range (2.0 V to 6.0 V)
- Output Current for Low Power (80 mA Typical)
- Two Surface Mount Packages (SOT–89, 3 Pin, or SOT–23, 5 Pin)

ORDERING INFORMATION

Device	Output Voltage	Operating Temperature Range	Package
MC78LC30HT1 MC78LC33HT1 MC78LC40HT1 MC78LC50HT1	3.0 3.3 4.0 5.0	T_A = –30° to +80°C	SOT–89
MC78LC30NTR MC78LC33NTR MC78LC40NTR MC78LC50NTR	3.0 3.3 4.0 5.0		SOT–23

Other voltages from 2.0 to 6.0 V, in 0.1 V increments, are available upon request. Consult your local Motorola sales office for information.



120 mA Micropower Voltage Regulator

MC78FC00H

T_A = –30° to +80°C, Case 1213

The MC78FC00 series voltage regulators are specifically designed for use as a power source for video instruments, handheld communication equipment, and battery powered equipment.

The MC78FC00 series voltage regulator ICs feature a high accuracy output voltage and ultra–low quiescent current. Each device contains a voltage reference unit, an error amplifier, a driver transistor, and resistors for setting output voltage, and a current limit circuit. These devices are available in SOT–89 surface mount packages, and allow construction of an efficient, constant voltage power supply circuit.

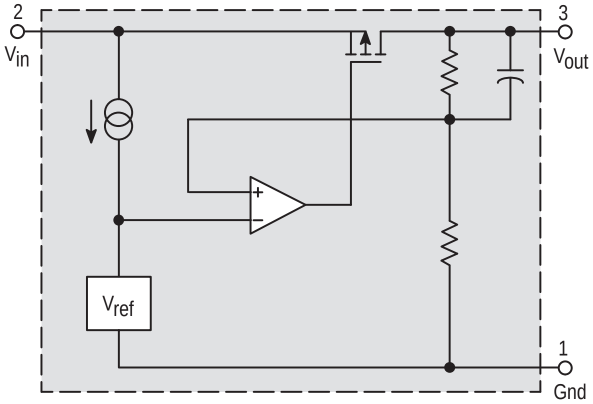
MC78FC00 Series Features:

- Ultra–Low Quiescent Current of 1.1 µA Typical
- Ultra–Low Dropout Voltage (0.5 V Typical)
- Large Output Current (120 mA Typical)
- Excellent Line Regulation (0.1%)
- Wide Operating Voltage Range (2.0 V to 10 V)
- High Accuracy Output Voltage (±2.5%)
- Wide Output Voltage Range (2.0 V to 6.0 V)
- Surface Mount Package (SOT–89)

ORDERING INFORMATION

Device	Output Voltage	Operating Temperature Range	Package
MC78FC30HT1	3.0	T_A = –30° to +80°C	SOT–89
MC78FC33HT1	3.3		
MC78FC40HT1	4.0		
MC78FC50HT1	5.0		

Other voltages from 2.0 to 6.0 V, in 0.1 V increments, are available upon request. Consult your local Motorola sales office for information.



Micropower Voltage Regulator for External Power Transistor

MC78BC00N

T_A = –30° to +80°C, Case 1212

The MC78BC00 voltage regulators are specifically designed to be used with an external power transistor to deliver high current with high voltage accuracy and low quiescent current.

The MC78BC00 series are devices suitable for constructing regulators with ultra–low dropout voltage and output current in the range of several tens of mA to hundreds of mA. These devices have a chip enable function, which minimizes the standby mode current drain. Each of these devices contains a voltage reference unit, an error amplifier, a driver transistor and resistors. These devices are available in the SOT–23, 5 pin surface mount packages.

These devices are ideally suited for battery powered equipment, and power sources for hand–held audio instruments, communication equipment and domestic appliances.

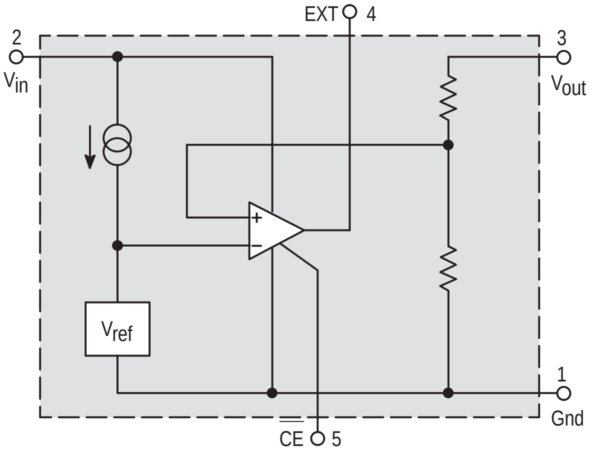
MC78BC00 Series Features:

- Ultra–Low Supply Current (50 µA)
- Standby Mode (0.2 µA)
- Ultra–Low Dropout Voltage (0.1 V with External Transistor and I_O = 100 mA)
- Excellent Line Regulation (Typically 0.1%/V)
- High Accuracy Output Voltage (±2.5%)

ORDERING INFORMATION

Device	Output Voltage	Operating Temperature Range	Package
MC78BC30NTR	3.0	T_A = –30° to +80°C	SOT–23
MC78BC33NTR	3.3		
MC78BC40NTR	4.0		
MC78BC50NTR	5.0		

Other voltages from 2.0 to 6.0 V, in 0.1 V increments, are available upon request. Consult your local Motorola sales office for information.



Micropower Voltage Regulators for Portable Applications (continued)

Micropower Voltage Regulators with On/Off Control

MC33264D, DM

T_A = –40° to +85°C, Case 751, 846A

The MC33264 series are micropower low dropout voltage regulators available in SO–8 and Micro–8 surface mount packages and a wide range of output voltages. These devices feature a very low quiescent current (100 µA in the ON mode; 0.1 µA in the OFF mode), and are capable of supplying output currents up to 100 mA. Internal current and thermal limiting protection is provided.

Additionally, the MC33264 has either active HIGH or active LOW control (Pins 2 and 3) that allows a logic level signal to turn–off or turn–on the regulator output.

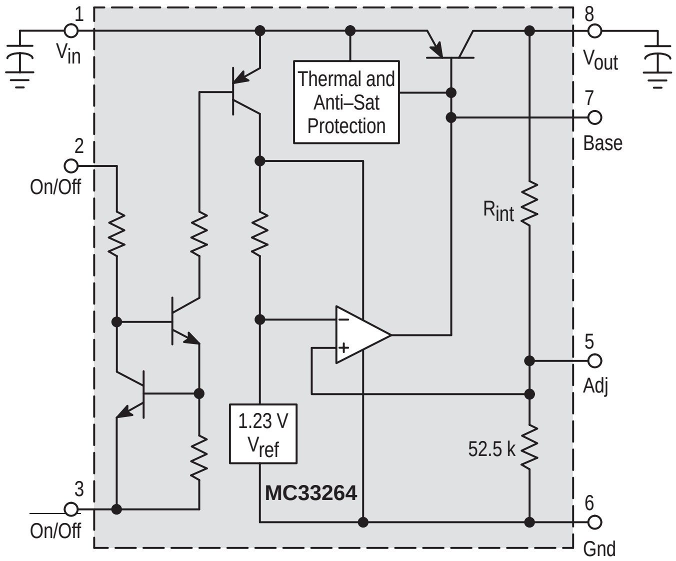
Due to the low input–to–output voltage differential and bias current specifications, these devices are ideally suited for battery powered computer, consumer, and industrial equipment where an extension of useful battery life is desirable.

MC33264 Features:

- Low Quiescent Current (0.3 µA in OFF Mode; 95 µA in ON Mode)
- Low Input–to–Output Voltage Differential of 47 mV at 10 mA, and 131 mV at 50 mA
- Multiple Output Voltages Available
- Extremely Tight Line and Load Regulation
- Stable with Output Capacitance of Only
  0.33 µF for 5.0 V, 6.0 V and 4.75 V Output Voltages
  0.22 µF for 2.8 V, 3.0 V and 3.3 V Output Voltages
- Internal Current and Thermal Limiting
- Logic Level ON/OFF Control
- Functionally Equivalent to TK115XXMC and LP2980

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC33264D–2.8	T_A = –40° to +85°C	SO–8
MC33264D–3.0		
MC33264D–3.3		
MC33264D–3.8		
MC33264D–4.0		
MC33264D–4.75		
MC33264D–5.0		
MC33264DM–2.8		Micro–8
MC33264DM–3.0		
MC33264DM–3.3		
MC33264DM–3.8		
MC33264DM–4.0		
MC33264DM–4.75		
MC33264DM–5.0		



Special Regulators

Voltage Regulator/Supervisory

Table 4. Voltage Regulator/Supervisory

	V_{out} (V)		I_O (mA) Max	V_{in} (V)		Reg_{line} (mV) Max	Reg_{load} (mV) Max	T_A (°C)	Suffix/ Package
Device	Min	Max		Min	Max				
MC33128*	2.9	3.1	35	3.2	7.0	n/a	30	–30 to +60	D/751B
	2.9	3.1	60				40		
	2.9	3.1	20				25		
	–2.65	–2.35	1.0				20		
MC34160	4.75	5.25	100	7.0	40	40	50	0 to +70	P/648C, DW/751G
MC33160								–40 to +85	
MC33267	4.9	5.2	500	6.0	26	50	50	–40 to +105	T/314D, TH, TV
MC33169*	4.7	6.4	–	2.7	9.5	–	–	–40 to +85	DTB/948G
	6.4	7.0							
	–2.35	–2.65							

* These ICs are intended for powering cellular phone GaAs power amplifiers and can be used for other portable applications as well.

Microprocessor Voltage Regulator and Supervisory Circuit

MC34160P, DW

T_A = 0° to +70°C, Case 648C, 751G

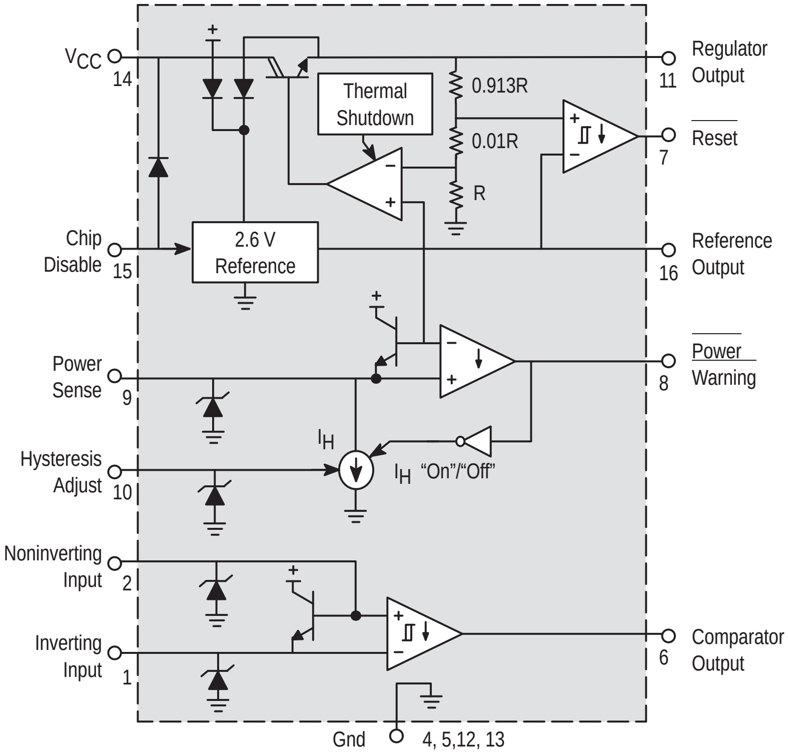
MC33160P, DW

T_A = –40° to +85°C, Case 648C, 751G

The MC34160 series is a voltage regulator and supervisory circuit containing many of the necessary monitoring functions required in microprocessor based systems. It is specifically designed for appliance and industrial applications offering the designer a cost effective solution with minimal external components. These integrated circuits feature a 5.0 V, 100 mA regulator with short circuit current limiting, pinned out 2.6 V bandgap reference, low voltage reset comparator, power warning comparator with programmable hysteresis, and an uncommitted comparator ideally suited for microprocessor line synchronization.

Additional features include a chip disable input for low standby current, and internal thermal shutdown for over temperature protection.

These devices are contained in a 16 pin dual–in–line heat tab plastic package for improved thermal conduction.



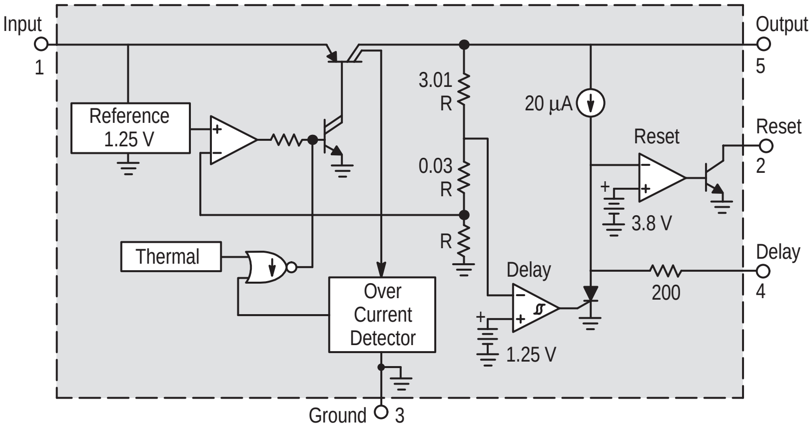
Low Dropout Regulator

MC33267T, TV

T_J = –40° to +105°C, Case 314D, 314B

The MC33267 is a positive fixed 5.0 V regulator that is specifically designed to maintain proper voltage regulation with an extremely low input–to–output voltage differential. This device is capable of supplying output currents in excess of 500 mA and contains internal current limiting and thermal shutdown protection. Also featured is an on–chip power–up reset circuit that is ideally suited for use in microprocessor based systems. Whenever the regulator output voltage is below nominal, the reset output is held low. A programmable time delay is initiated after the regulator has reached its nominal level and upon timeout, the reset output is released.

Due to the low dropout voltage specifications, the MC33267 is ideally suited for use in battery powered industrial and consumer equipment where an extension of useful battery life is desirable. This device is contained in an economical five lead TO–220 type package.



Voltage Regulator/Supervisory (continued)

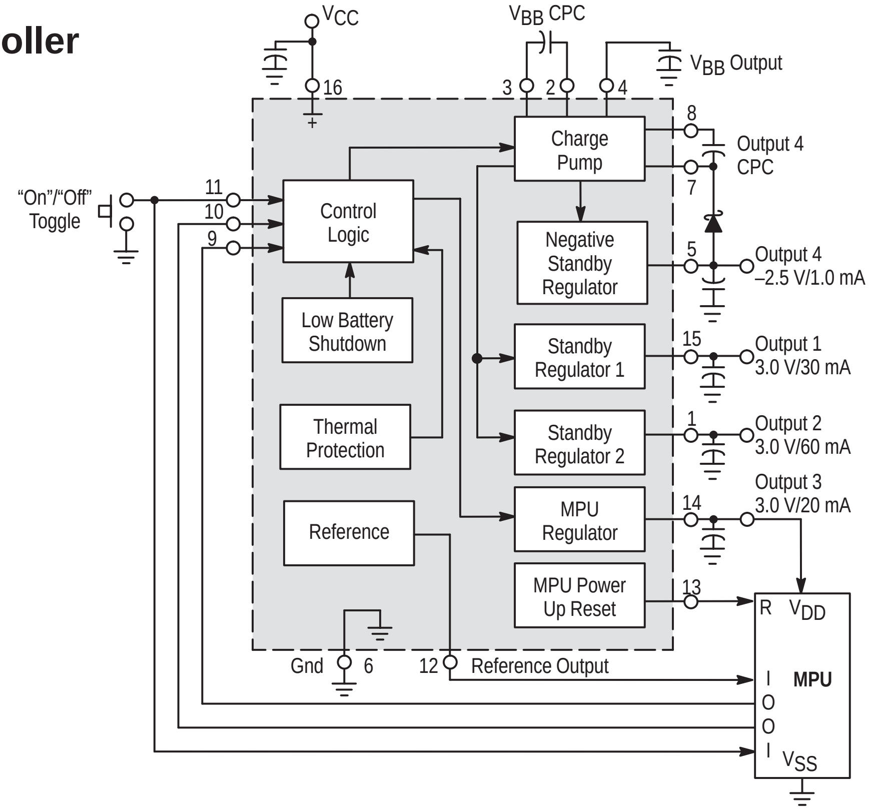
Power Management Controller

MC33128D

T_A = –30° to +60°C, Case 751B

The MC33128 is a power management controller specifically designed for use in battery powered cellular telephone and pager applications. This device contains all of the active functions required to interface the user to the system electronics via a microprocessor. This integrated circuit consists of a low dropout voltage regulator with power–up reset for MPU power, two low dropout voltage regulators for independant powering of analog and digital circuitry, and a negative charge pump voltage regulator for full depletion of gallium arsenide MESFETs.

Also included are protective system shutdown features consisting of a battery latch that is activated upon battery insertion, low battery voltage shutdown, and a thermal over temperature detector. This device is available in a 16–pin narrow body surface mount plastic package.



GaAs Power Amplifier Support IC

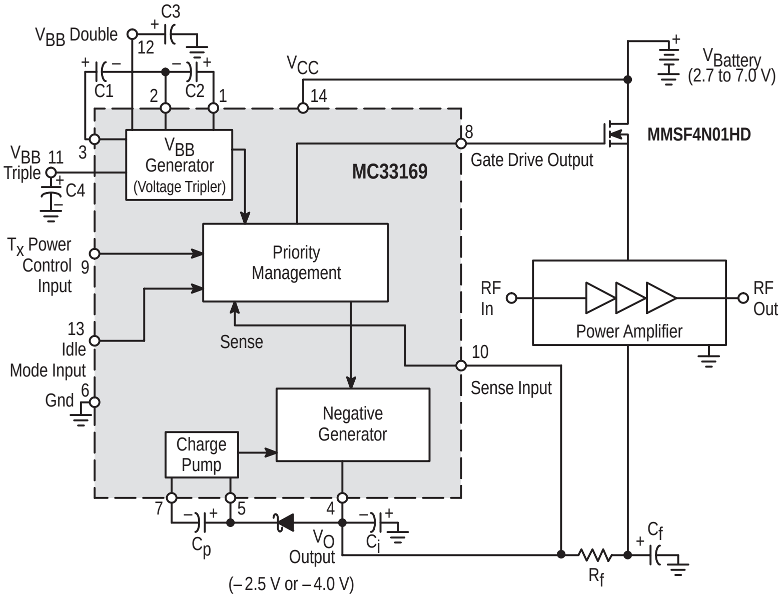
MC33169DTB

T_A = –40° to +85°C, Case 948G

The MC33169 is a support IC for GaAs Power Amplifier Enhanced FETs used in hand portable telephones such as GSM, PCN and DECT. This device provides negative voltages for full depletion of Enhanced MESFETs as well as a priority management system of drain switching, ensuring that the negative voltage is always present before turning "on" the Power Amplifier. Additional features include an idle mode input and a direct drive of the N–Channel drain switch transistor.

This product is available in two versions, –2.5 and –4.0 V. The –4.0 V version is intended for supplying RF modules for GSM and DCS1800 applications, whereas the –2.5 V version is dedicated for DECT and PHS systems.

- Negative Regulated Output for Full Depletion of GaAs MESFETs
- Drain Switch Priority Management Circuit
- CMOS Compatible Inputs
- Idle Mode Input (Standby Mode) for Very Low Current Consumption
- Output Signal Directly Drives N–Channel FET
- Low Startup and Operating Current



SCSI Regulator

Table 5. SCSI Regulator

Device	V_{out} (V)		I_{sink} (mA)	V_{in} (V)		Reg_{line} (%)	Reg_{load} (%)	T_J (°C)	Suffix/ Package
	Min	Max		Min	Max				
MC34268	2.81	2.89	800	3.9	20	0.3	0.5	150	D/751, DT

SCSI–2 Active Terminator Regulator

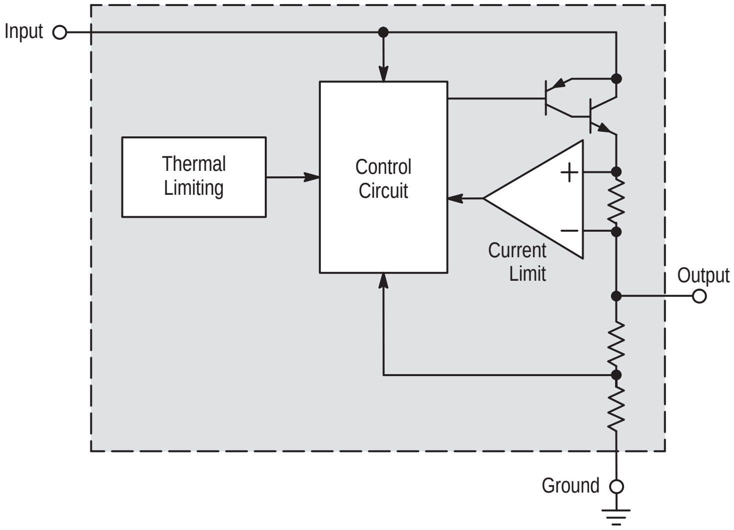
MC34268D, DT

T_J = 0° to +125°C, Case 751, 369A

The MC34268 is a medium current, low dropout positive voltage regulator specifically designed for use in SCSI–2 active termination circuits. This device offers the circuit designer an economical solution for precision voltage regulation, while keeping power losses to a minimum. The regulator consists of a 1.0 V dropout composite PNP/NPN pass transistor, current limiting, and thermal limiting. These devices are packaged in the 8–pin SOP–8 and 3–pin DPAK surface mount power packages.

Applications include active SCSI–2 terminators and post regulation of switching power supplies.

- 2.85 V Output Voltage for SCSI–2 Active Termination
- 1.0 V Dropout
- Output Current in Excess of 800 mA
- Thermal Protection
- Short Circuit Protection
- Output Trimmed to 1.4% Tolerance
- No Minimum Load Required
- Space Saving DPAK and SOP–8 Surface Mount Power Packages



Switching Regulator Control Circuits

These devices contain the primary building blocks which are required to implement a variety of switching power supplies. The product offerings fall into three major categories consisting of single–ended and double–ended controllers, plus single–ended ICs with on–chip power switch transistors. These circuits operate in voltage, current or resonant modes and are designed to drive many of the standard switching topologies. The single–ended configurations include buck, boost, flyback and forward converters. The double–ended devices control push–pull, half bridge and full bridge configurations.

Table 6. Single–Ended Controllers

These single–ended voltage and current mode controllers are designed for use in buck, boost, flyback, and forward converters. They are cost effective in applications that range from 0.1 to 200 W power output.

I_O (mA) Max	Minimum Operating Voltage Range (V)	Operating Mode	Reference (V)	Maximum Useful Oscillator Frequency (kHz)	Device	T_A (°C)	Suffix/ Package
500 (Uncommitted Drive Output)	7.0 to 40	Voltage	5.0 ± 1.5%	200	MC34060A	0 to +70	D/751A
							P/646
					MC33060A	–40 to +85	D/751A
							P/646
1000 (Totem Pole MOSFET Drive Output)	4.2 to 12	Current	1.25 ± 2.0%	300	MC34129	0 to +70	D/751A
							P/646
					MC33129	–40 to +85	D/751A
							P/646
	11.5 to 30		5.0 ± 2.0%	500	UC3842A	0 to +70	D/751A
							N/626
	11 to 30		5.0 ± 1.0%		UC2842A	–25 to +85	D/751A
							N/626
	8.2 to 30		5.0 ± 2.0%		UC3843A	0 to +70	D/751A
							N/626
			5.0 ± 1.0%		UC2843A	–25 to +85	D/751A
							N/626
	11.5 to 30		5.0 ± 2.0%	500 (50% Duty Cycle Limit)	UC3844	0 to +70	D/751A
							N/626
	11 to 30		5.0 ± 1.0%		UC2844	–25 to +85	D/751A
							N/626
	8.2 to 30		5.0 ± 2.0%		UC3845	0 to +70	D/751A
							N/626
			5.0 ± 1.0%		UC2845	–25 to +85	D/751A
							N/626
	11.5 to 30		5.0 ± 2.0%	500 (Improved Oscillator Specifications with Frequency Guaranteed at 250 kHz)	UC3842B	0 to +70	D/751A
							D1/751
							N/626
					UC3842BV	–40 to +105	D/751A
							D1/751
							N/626

Table 6. Single–Ended Controllers (continued)

These single–ended voltage and current mode controllers are designed for use in buck, boost, flyback, and forward converters. They are cost effective in applications that range from 0.1 to 200 W power output.

I_O (mA) Max	Minimum Operating Voltage Range (V)	Operating Mode	Reference (V)	Maximum Useful Oscillator Frequency (kHz)	Device	T_A (°C)	Suffix/ Package
1000 (Totem Pole MOSFET Drive Output)	11 to 30	Current	5.0 ± 1.0%	500 (Improved Oscillator Specifications with Frequency Guaranteed at 250 kHz)	UC2842B	–25 to +85	D/751A
							D1/751
							N/626
	8.2 to 30		5.0 ± 2.0%		UC3843B	0 to +70	D/751A
							D1/751
							N/626
					UC3843BV	–40 to +105	D/751A
							D1/751
							N/626
			5.0 ± 1.0%		UC2843B	–25 to +85	D/751A
							D1/751
							N/626
	11.5 to 30		5.0 ± 2.0%	500 (50% Duty Cycle Limit)	UC3844B	0 to +70	D/751A
							D1/751
							N/626
					UC3844BV	–40 to +105	D/751A
							D1/751
							N/626
	11 to 30		5.0 ± 1.0%		UC2844B	–25 to +85	D/751A
							D1/751
							N/626
	8.2 to 30		5.0 ± 2.0%		UC3845B	0 to +70	D/751A
							D1/751
							N/626
					UC3845BV	–40 to +105	D/751A
							D1/751
							N/626
			5.0 ± 1.0%		UC2845B	–25 to +85	D/751A
							D1/751
							N/626
1000 Source 1500 Sink (Split Totem Pole Bipolar Drive Output)	11 to 18		5.0 ± 6.0%		MC44602		P2/648C
2000 (Totem Pole MOSFET Drive Output)	9.2 to 30	Current or Voltage	5.1 ± 1.0%	1000	MC34023	0 to +70	DW/751G
							FN/775
							P/648
					MC33023	–40 to +105	DW/751G
							FN/775
							P/648

Table 7. Single–Ended Controllers with On–Chip Power Switch

These monolithic power switching regulators contain all the active functions required to implement standard dc–to–dc converter configurations with a minimum number of external components.

I_O (mA) Max	Minimum Operating Voltage Range (V)	Operating Mode	Reference (V)	Maximum Useful Oscillator Frequency (kHz)	Device	T_A (°C)	Suffix/ Package
1500 (Uncommitted Power Switch)	2.5 to 40	Voltage	1.25 ± 5.2%(1)	100	µA78S40	0 to +70	PC/648
						–40 to +85	PV/648
			1.25 ± 2.0%		MC34063A	0 to +70	D/751
							P1/626
					MC33063A	–40 to +85	D/751
							P1/626
						–40 to +125	D/751
1500 (Uncommitted Power Switch)	3.0 to 65	Voltage	1.25 ± 2.0% and 5.05 ± 3.0%	100	MC34165	0 to +70	P/648C, DW/751G
					MC33165	–40 to +85	
3400 (Uncommitted Power Switch)	2.5 to 40				MC34163	0 to +70	
					MC33163	–40 to +85	
3400(2) (Dedicated Emitter Power Switch)	7.5 to 40		5.05 ± 2.0%	72 ± 12% Internally Fixed	MC34166	0 to +70	D2T/936A, TH, TV, T/314D
					MC33166	–40 to +85	
5500(3) (Dedicated Emitter Power Switch)					MC34167	0 to +70	
					MC33167	–40 to +85	

(1) Tolerance applies over the specified operating temperature range.
(2) Guaranteed minimum, typically 4300 mA.
(3) Guaranteed minimum, typically 6500 mA.

Table 8. Easy Switcher™ Single–Ended Controllers with On–Chip Power Switch

The Easy Switcher™ series is ideally suited for easy, convenient design of a step–down switching regulator (buck converter), with a minimum number of external components.

I_O (mA) Max	Minimum Operating Voltage Range (V)	Operating Mode	Oscillator Frequency (kHz)	Output Voltage (V)	Device	T_J (°C)	Suffix/ Package
1000	4.75 to 40	Voltage	52 Fixed Internal	3.3	LM2575T–3.3	–40 to +125	T/314D
	8.0 to 40			5.0	LM2575T–5		
	15 to 40			12	LM2575T–12		
	18 to 40			15	LM2575T–15		
	8.0 to 40			1.23 to 37	LM2575T–Adj		
	4.75 to 40			3.3	LM2575TV–3.3		TV/314B
	8.0 to 40			5.0	LM2575TV–5		
	15 to 40			12	LM2575TV–12		
	18 to 40			15	LM2575TV–15		
	8.0 to 40			1.23 to 37	LM2575TV–Adj		
	4.75 to 40			3.3	LM2575D2T–3.3		D2T/936A
	8.0 to 40			5.0	LM2575D2T–5		
	15 to 40			12	LM2575D2T–12		
	18 to 40			15	LM2575D2T–15		
	8.0 to 40			1.23 to 37	LM2575D2T–Adj		

Table 9. Very High Voltage Single–Ended Controller with On–Chip Power Switch

This monolithic high voltage switching regulator is specifically designed to operate from a rectified ac line voltage source. Included are an on–chip high voltage power switch, active off–line startup circuitry and a full featured PWM controller with fault protection.

Power Switch Maximum Rating		**Startup Input Max (V)**	**Operating Mode**	**Feedback Threshold (V)**	**Maximum Useful Oscillator Frequency (kHz)**	**Device**	**T_J (°C)**	**Suffix/ Package**
V_{DS} (V)	**I_{DS} (mA)**							
500	2000	250	Voltage	2.6 ± 3.1%	1000	MC33362	–25 to +125	DW/751N, P/648E
700	1000	450				MC33363		
700	1000	450				MC33363A		

Table 10. Double–Ended Controllers

These double–ended voltage, current and resonant mode controllers are designed for use in push–pull, half–bridge, and full–bridge converters. They are cost effective in applications that range from 100 to 2000 watts power output.

I_O (mA) Max	**Minimum Operating Voltage Range (V)**	**Operating Mode**	**Reference (V)**	**Maximum Useful Oscillator Frequency (kHz)**	**Device**	**T_A (°C)**	**Suffix/ Package**
500 (Uncommitted Drive Outputs)	7.0 to 40	Voltage	5.0 ± 5.0%(1)	200	TL494	0 to +70	CN/648
						–25 to +85	IN/648
			5.0 ± 1.5%	300	TL594	0 to +70	CN/648
						–25 to +85	IN/648
± 500 (Totem Pole MOSFET Drive Outputs)	8.0 to 40		5.1 ± 2.0%	400	SG3525A	0 to +70	N/648
					SG3527A		N/648
± 200 (Totem Pole MOSFET Drive Outputs)			5.0 ± 2.0%		SG3526	0 to +125(2)	N/707
±1500 (Totem Pole MOSFET Drive Outputs)	9.6 to 20	Resonant (Zero Current)	5.1 ± 2.0%	1000	MC34066	0 to +70	DW/751G
							P/648
					MC33066	–40 to +85	DW/751G
							P/648
		Resonant (Zero Voltage)		2000	MC34067	0 to +70	DW/751G
							P/648
					MC33067	–40 to +85	DW/751G
							P/648
2000 (Totem Pole MOSFET Drive Outputs)	9.2 to 30	Current or Voltage	5.1 ± 1.0%	1000	MC34025	0 to +70	DW/751G
							FN/775
							P/648
					MC33025	–40 to +105	DW/751G
							FN/775
							P/648

(1) Tolerance applies over the specified operating temperature range.
(2) Junction Temperature Range.

CMOS Micropower DC–to–DC Converters

Variable Frequency Micropower DC–to–DC Converter

MC33463H

T_A = –30° to +80°C, Case 1213

The MC33463 series are micropower switching voltage regulators, specifically designed for handheld and laptop applications, to provide regulated output voltages using a minimum of external parts. A wide choice of output voltages are available. These devices feature a very low quiescent bias current of 4.0 μA typical.

The MC33463H–XXLT1 series features a highly accurate voltage reference, an oscillator, a variable frequency modulation (VFM) controller, a driver transistor (Lx), an error amplifier and feedback resistive divider.

The MC33463H–XXLT1 is identical to the MC33463H–XXKT1, except that a drive pin (EXT) for an external transistor is provided.

Due to the low bias current specifications, these devices are ideally suited for battery powered computer, consumer, and industrial equipment where an extension of useful battery life is desirable.

MC33463 Series Features:

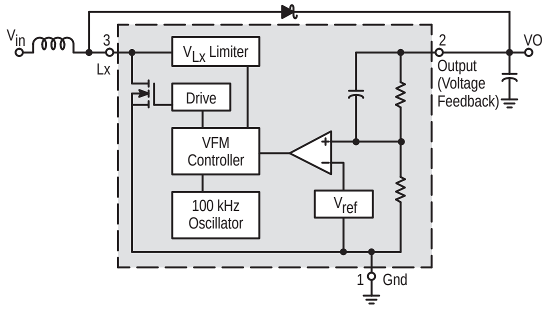
- Low Quiescent Bias Current of 4.0 μA
- High Output Voltage Accuracy of ±2.5%
- Low Startup Voltage of 0.9 V at 1.0 mA
- Surface Mount Package

ORDERING INFORMATION

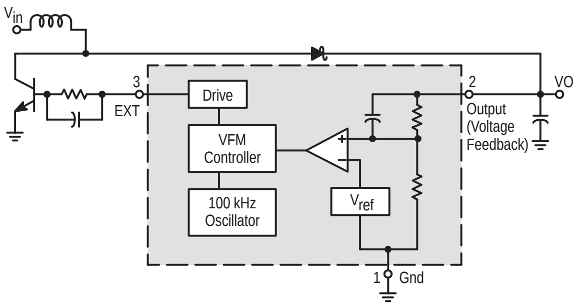
Device	Output Voltage	Type	Operating Temperature Range	Package (Tape/Reel)
MC33463H–30KT1	3.0	Int. Switch	T_A = –30° to +80°C	SOT–89 (Tape)
MC33463H–33KT1	3.3			
MC33463H–50KT1	5.0			
MC33463H–30LT1	3.0	Ext. Switch Drive		SOT–89 (Tape)
MC33463H–33LT1	3.3			
MC33463H–50LT1	5.0			

Other voltages from 2.5 V to 7.5 V, in 0.1 V increments are available upon request. Consult your local Motorola sales office for information.

MC33463H–XXKT1



MC33463H–XXLT1



Fixed Frequency PWM Micropower DC–to–DC Converter

MC33466H

T_A = –30° to +80°C, Case 1213

The MC33466 series are micropower switching voltage regulators, specifically designed for handheld and laptop applications, to provide regulated output voltages using a minimum of external parts. A wide choice of output voltages are available. These devices feature a very low quiescent bias current of 15 µA typical.

The MC33466H–XXJT1 series features a highly accurate voltage reference, an oscillator, a pulse width modulation (PWM) controller, a driver transistor (Lx), an error amplifier and feedback resistive divider.

The MC33466H–XXLT1 is identical to the MC33466H–XXJT1, except that a drive pin (EXT) for an external transistor is provided.

Due to the low bias current specifications, these devices are ideally suited for battery powered computer, consumer, and industrial equipment where an extension of useful battery life is desirable.

MC33466 Series Features:

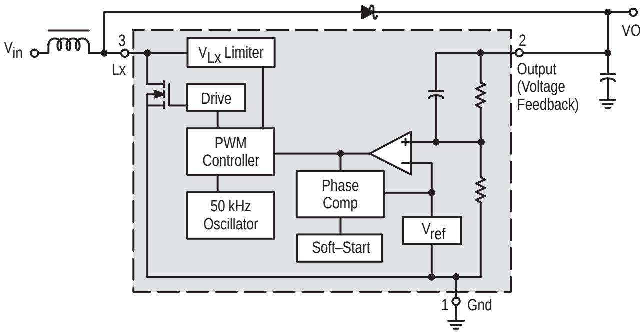
- Low Quiescent Bias Current of 15 µA
- High Output Voltage Accuracy of ±2.5%
- Low Startup Voltage of 0.9 V at 1.0 mA
- Soft–Start = 500 µs
- Surface Mount Package

ORDERING INFORMATION

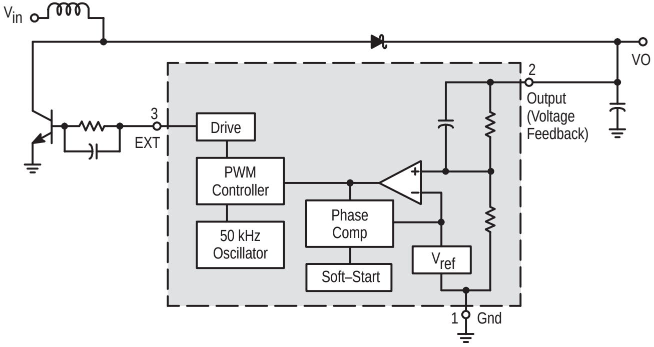
Device	Output Voltage	Type	Operating Temperature Range	Package (Tape/Reel)
MC33466H–30JT1 MC33466H–33JT1 MC33466H–50JT1	3.0 3.3 5.0	Int. Switch	T_A = –30° to +80°C	SOT–89 (Tape)
MC33466H–30LT1 MC33466H–33LT1 MC33466H–50LT1	3.0 3.3 5.0	Ext. Switch Drive		SOT–89 (Tape)

Other voltages from 2.5 V to 7.5 V, in 0.1 V increments are available upon request. Consult your local Motorola sales office for information.

MC33466H–XXJT1



MC33466H–XXLT1



Single–Ended GreenLine™ Controllers

Mixed Frequency Mode GreenLine™ PWM Controller:

Fixed Frequency, Variable Frequency, Standby Mode

MC44603P, DW

T_A = –25° to +85°C, Case 648, 751G

The MC44603 is an enhanced high performance controller that is specifically designed for off–line and dc–to–dc converter applications. This device has the unique ability of automatically changing operating modes if the converter output is overloaded, unloaded, or shorted, offering the designer additional protection for increased system reliability. The MC44603 has several distinguishing features when compared to conventional SMPS controllers. These features consist of a foldback facility for overload protection, a standby mode when the converter output is slightly loaded, a demagnetization detection for reduced switching stresses on transistor and diodes, and a high current totem pole output ideally suited for driving a power MOSFET. It can also be used for driving a bipolar transistor in low power converters (< 150 W). It is optimized to operate in discontinuous mode but can also operate in continuous mode. Its advanced design allows use in current mode or voltage mode control applications.

Current or Voltage Mode Controller

- Operation up to 250 kHz Output Switching Frequency
- Inherent Feed Forward Compensation
- Latching PWM for Cycle–by–Cycle Current Limiting
- Oscillator with Precise Frequency Control

High Flexibility

- Externally Programmable Reference Current
- Secondary or Primary Sensing
- Synchronization Facility
- High Current Totem Pole Output
- Undervoltage Lockout with Hysteresis

Safety/Protection Features

- Overvoltage Protection Against Open Current and Open Voltage Loop
- Protection Against Short Circuit on Oscillator Pin
- Fully Programmable Foldback
- Soft–Start Feature
- Accurate Maximum Duty Cycle Setting
- Demagnetization (Zero Current Detection) Protection
- Internally Trimmed Reference

GreenLine Controller: Low Power Consumption in Standby Mode

- Low Startup and Operating Current
- Fully Programmable Standby Mode
- Controlled Frequency Reduction in Standby Mode
- Low dV/dT for Low EMI Radiations

High Safety Standby Ladder Mode GreenLine™ PWM Controller

MC44604P

T_A = –25° to +85°C, Case 648

The MC44604 is an enhanced high performance controller that is specifically designed for off–line and dc–to–dc converter applications.

The MC44604 is a modification of the MC44603. The MC44604 offers enhanced safety and reliable power management in its protection features (foldback, overvoltage detection, soft–start, accurate demagnetization detection). Its high current totem pole output is also ideally suited for driving a power MOSFET but can also be used for driving a bipolar transistor in low power converters (< 150 W).

In addition, the MC44604 offers a new efficient way to reduce the standby operating power by means of a patented standby ladder mode operation of the converter significantly reducing the converter consumption in standby mode.

Current or Voltage Mode Controller

- Operation Up to 250 kHz Output Switching Frequency
- Inherent Feed Forward Compensation
- Latching PWM for Cycle–by–Cycle Current Limiting
- Oscillator with Precise Frequency Control

High Flexibility

- Externally Programmable Reference Current
- Secondary or Primary Sensing
- High Current Totem Pole Output
- Undervoltage Lockout with Hysteresis

Safety/Protection Features

- Overvoltage Protection Facility Against Open Loop
- Protection Against Short Circuit on Oscillator Pin
- Fully Programmable Foldback
- Soft–Start Feature
- Accurate Maximum Duty Cycle Setting
- Demagnetization (Zero Current Detection) Protection
- Internally Trimmed Reference

GreenLine™ Controller:

- Low Startup and Operating Current
- Patented Standby Ladder Mode for Low Standby Losses
- Low dV/dT for Low EMI

High Safety Latched Mode GreenLine™ PWM Controller for (Multi)Synchronized Applications

MC44605P

T_A = –25° to +85°C, Case 648

The MC44605 is a high performance current mode controller that is specifically designed for off–line converters. The MC44605 has several distinguishing features that make it particularly suitable for multisynchronized monitor applications.

The MC44605 synchronization arrangement enables operation from 16 kHz up to 130 kHz. This product was optimized to operate with universal ac mains voltage from 80 V to 280 V, and its high current totem pole output makes it ideally suited for driving a power MOSFET.

The MC44605 protections provide well controlled, safe power management. Safety enhancements detect four different fault conditions and provide protection through a disabling latch.

Current or Voltage Mode Controller

- Current Mode Operation Up to 250 kHz Output Switching Frequency
- Inherent Feed Forward Compensation
- Latching PWM for Cycle–by–Cycle Current Limiting
- Oscillator with Precise Frequency Control
- Externally Programmable Reference Current
- Secondary or Primary Sensing (Availability of Error Amplifier Output)
- Synchronization Facility
- High Current Totem Pole Output
- Undervoltage Lockout with Hysteresis
- Low Output dV/dT for Low EMI
- Low Startup and Operating Current

Safety/Protection Features

- Soft–Start Feature
- Demagnetization (Zero Current Detection) Protection
- Overvoltage Protection Facility Against Open Loop
- EHT Overvoltage Protection (E.H.T.OVP): Protection Against Excessive Amplitude Synchronization Pulses
- Winding Short Circuit Detection (W.S.C.D.)
- Limitation of the Maximum Input Power (M.P.L.): Calculation of Input Power for Overload Protection
- Over Heating Detection (O.H.D.): to Prevent the Power Switch from Excessive Heating

Latched Disabling Mode

- When one of the following faults is detected: EHT overvoltage, Winding Short Circuit (WSCD), excessive input power (M.P.L.), power switch over heating (O.H.D.), a counter is activated
- If the counter is activated for a time that is long enough, the circuit gets definitively disabled. The latch can only be reset by removing and then re–applying power

Very High Voltage Switching Regulator

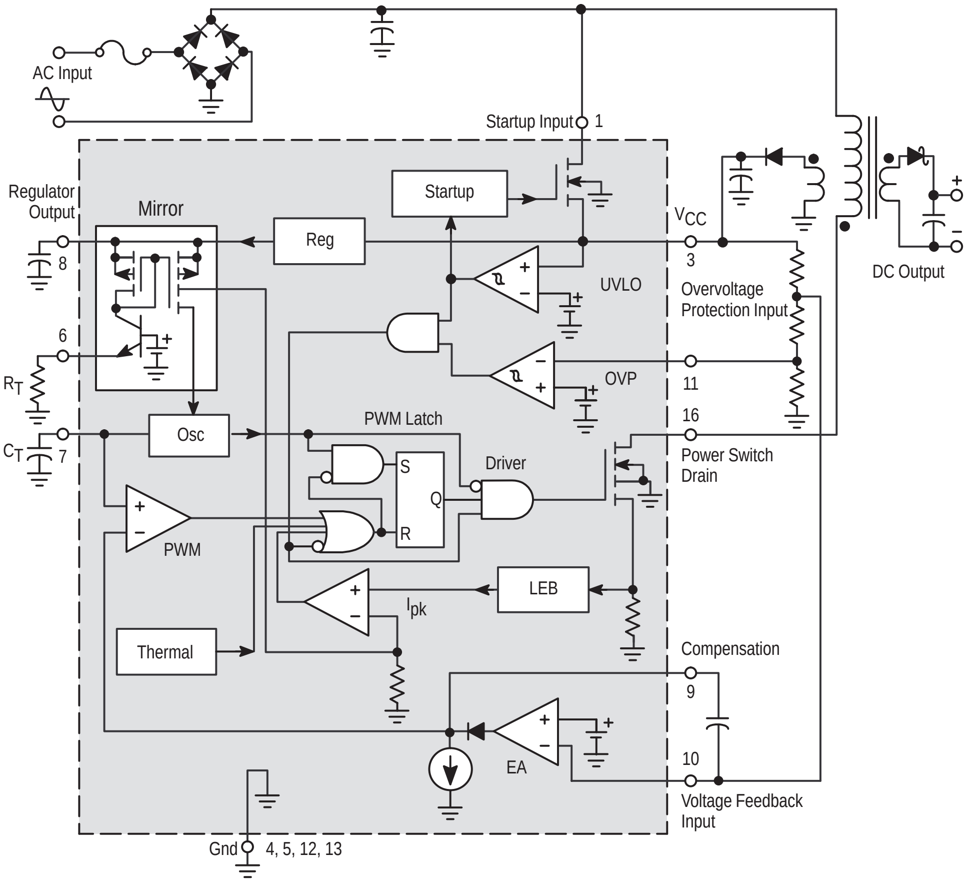
MC33362DW, P

T_J = –25° to +125°C, Case 751N, 658E

The MC33362 is a monolithic high voltage switching regulator that is specifically designed to operate from a rectified 120 VAC line source. This integrated circuit features an on–chip 500 V/2.0 A SenseFET power switch, 250 V active off–line startup FET, duty cycle controlled oscillator, current limiting comparator with a programmable threshold and leading edge blanking, latching pulse width modulator for double pulse suppression, high gain error amplifier, and a trimmed internal bandgap reference. Protective features include cycle–by–cycle current limiting, input undervoltage lockout with hysteresis, output overvoltage protection, and thermal shutdown. This device is available in a 16–lead dual–in–line and wide body surface mount packages.

- On–Chip 500 V, 2.0 A SenseFET Power Switch
- Rectified 120 VAC Line Source Operation
- On–Chip 250 V Active Off–Line Startup FET
- Latching PWM for Double Pulse Suppression
- Cycle–By–Cycle Current Limiting
- Input Undervoltage Lockout with Hysteresis
- Output Overvoltage Protection Comparator
- Trimmed Internal Bandgap Reference
- Internal Thermal Shutdown

20 W Off–Line Converter



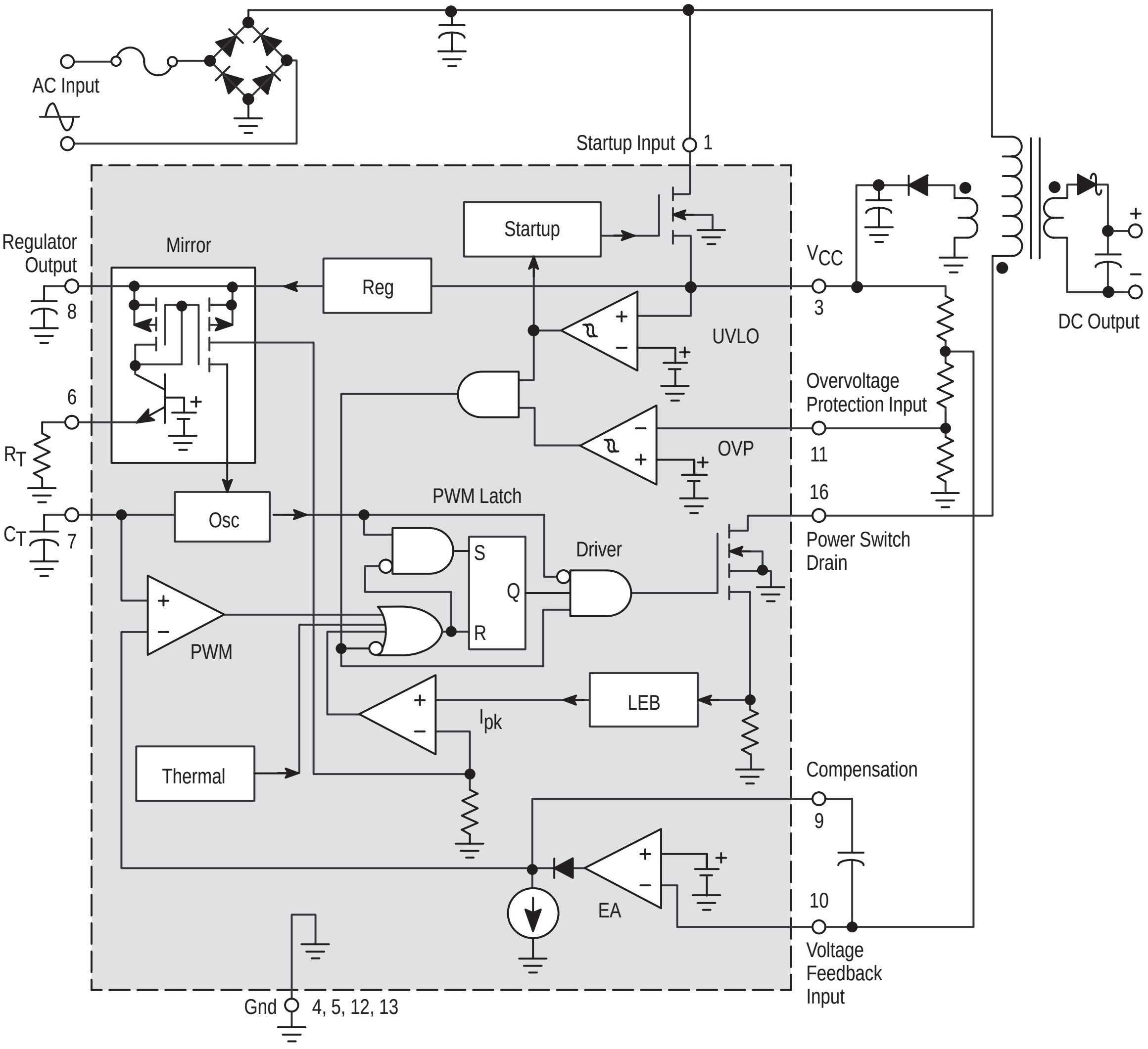
Very High Voltage Switching Regulator

MC33363DW, P, MC33363ADW, P

T_J = –25° to +125°C, Case 751N, 648E

The MC33363 is a monolithic high voltage switching regulator that is specifically designed to operate from a rectified 240 Vac line source. This integrated circuit features an on–chip 700 V/1.0 A (1.5 A in MC33363A) SenseFET power switch, 450 V active off–line startup FET, duty cycle controlled oscillator, current limiting comparator with a programmable threshold and leading edge blanking, latching pulse width modulator for double pulse suppression, high gain error amplifier, and a trimmed internal bandgap reference. Protective features include cycle–by–cycle current limiting, input undervoltage lockout with hysteresis, output overvoltage protection, and thermal shutdown. This device is available in a 16–lead wide body surface mount package.

- On–Chip 700 V, 1.0 A SenseFET Power Switch
- On–Chip 700 V, 1.5 A SenseFET Power Switch in MC33363A
- Rectified 240 Vac Line Source Operation
- On–Chip 450 V Active Off–Line Startup FET
- Latching PWM for Double Pulse Suppression
- Cycle–By–Cycle Current Limiting
- Input Undervoltage Lockout with Hysteresis
- Output Overvoltage Protection Comparator
- Trimmed Internal Bandgap Reference
- Internal Thermal Shutdown



Critical Conduction SMPS Controller

MC33364D, D1, D2

T_J = –25° to +125°C, Case 751, 751B

The MC33364 series are variable frequency SMPS controllers that operate in the critical conduction mode. They are optimized for low power, high density power supplies requiring minimum board area, reduced component count, and low power dissipation. Each narrow body SOIC package provides a small footprint. Integration of the high voltage startup saves approximately 0.7 W of power compared to resistor bootstrapped circuits.

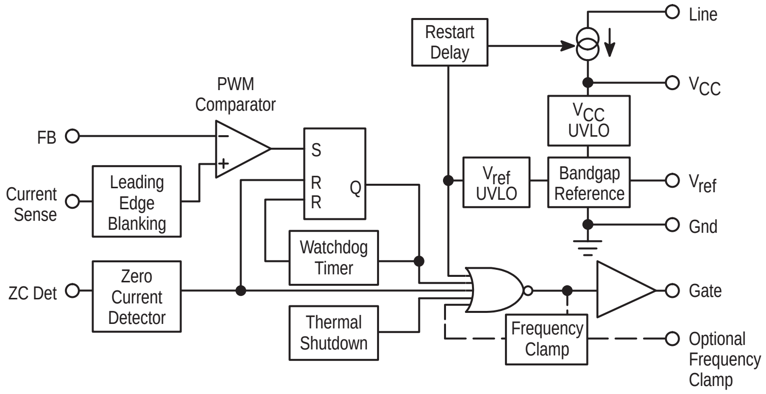
Each MC33364 features an on–board reference, UVLO function, a watchdog timer to initiate output switching, a zero current detector to ensure critical conduction operation, a current sensing comparator, leading edge blanking, and a CMOS driver. Protection features include the ability to shut down switching, and cycle–by–cycle current limiting.

The MC33364D1 is available in a surface mount SO–8 package. It has an internal 144 kHz frequency clamp. For loads which have a low power operating condition, the frequency clamp limits the maximum operating frequency, preventing excessive switching losses and EMI radiation.

The MC33364D2 is available in the SO–8 package without an internal frequency clamp.

The MC33364D is available in the SO–16 package. It has an internal 144 kHz frequency clamp which is pinned out, so that the designer can adjust the clamp frequency by connecting appropriate values of resistance and capacitance.

- Lossless Off–Line Startup
- Leading Edge Blanking for Noise Immunity
- Watchdog Timer to Initiate Switching
- Minimum Number of Support Components
- Shutdown Capability
- Over Temperature Protection
- Optional Frequency Clamp



Special Switching Regulator Controllers

These high performance dual channel controllers are optimized for off–line, ac–to–dc power supplies and dc–to–dc converters in the flyback topology. They also have undervoltage lockout voltages which are optimized for off–line and lower voltage dc–to–dc converters, respectively. Applications include desktop computers, peripherals, televisions, games, and various consumer appliances.

Table 11. Dual Channel Controllers

I_O (mA) Max	Minimum Operating Voltage Range (V)	Operating Mode	Reference (V)	Maximum Useful Oscillator Frequency (kHz)	Device	T_A (°C)	Suffix/ Package
500	4.0	Voltage	1.25 ± 2.0%	700	MC34270	0 to +70	FB/873A
					MC34271		
±1000 (Totem Pole MOSFET Drive Outputs)	11 to 15.5	Current	5.0 ± 2.6%	500	MC34065	0 to +70	DW/751G
							P/648
					MC33065	–40 to +85	DW/751G
							P/648
	11 to 20				MC34065	0 to +70	DW–H/751G
							P–H/648
					MC33065	–40 to +85	DW–H/751G
							P–H/648
	8.4 to 20				MC34065	0 to +70	DW–L/751G
							P–L/648
					MC33065	–40 to +85	DW–L/751G
							P–L/648

Table 12. Universal Microprocessor Power Supply Controllers

A versatile power supply control circuit for microprocessor–based systems, this device is mainly intended for automotive applications and battery powered instruments. The circuit provides a power–on reset delay and a Watchdog feature for orderly microprocessor operation.

Regulated Outputs	Output Current (mA)	V_{CC} (V)		Reference (V)	Key Supervisory Features	Device	T_A (°C)	Package
		Min	Max					
E^2PROM Programmable Output: 24 V (Write Mode) 5.0 V (Read Mode)	150 peak	6.0	35	2.5 ± 3.2%	MPU Reset and Watchdog Circuit	TCF5600 TCA5600	–40 to +85	707

Table 13. Power Factor Controllers

I_O (mA) Max	Minimum Operating Voltage Range (V)	Maximum Startup Voltage (V)	Reference (V)	Features	Device	T_A (°C)	Suffix/ Package
± 500 (Totem Pole MOSFET Drive Outputs)	9.0 to 30	30	2.5 ± 1.4%	Undervoltage Lockout, Internal Startup Timer	MC34261	0 to +70	D/751
							P/626
					MC33261	–40 to +85	D/751
							P/626
				Overvoltage Comparator, Undervoltage Lockout, Internal Startup Timer	MC34262	0 to +85	D/751
							P/626
					MC33262	–40 to +105	D/751
							P/626
1500 (CMOS Totem Pole MOSFET Drive Outputs)	9.0 to 16	500	5.0 ± 1.5%	Off–Line High Voltage Startup Overvoltage Comparator, Undervoltage Lockout, Timer, Low Load Detect	MC33368	–25 to +125	D/751K

Power Factor Controllers

MC34262D, P

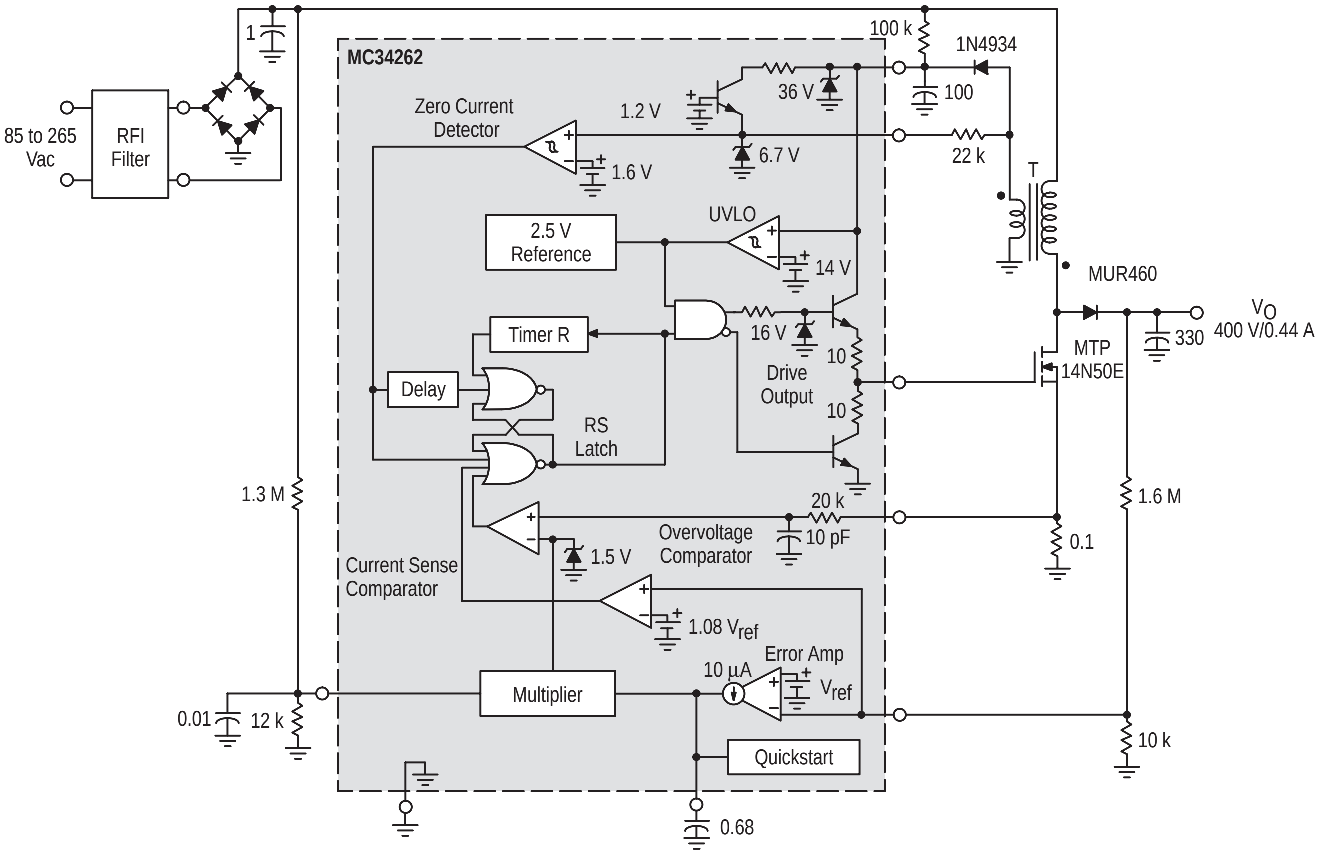
T_A = 0° to +85°C, Case 751, 626

MC33262D, P

T_A = –40° to +105°C, Case 751, 626

The MC34262, MC33262 series are active power factor controllers specifically designed for use as a preconverter in electronic ballast and in off–line power converter applications. These integrated circuits feature an internal startup timer for stand alone applications, a one quadrant multiplier for near unity power factor, zero current detector to ensure critical conduction operation, transconductance error amplifier, quickstart circuit for enhanced startup, trimmed internal bandgap reference, current sensing comparator, and a totem pole output ideally suited for driving a power MOSFET.

Also included are protective features consisting of an overvoltage comparator to eliminate runaway output voltage due to load removal, input undervoltage lockout with hysteresis, cycle–by–cycle current limiting, multiplier output clamp that limits maximum peak switch current, an RS latch for single pulse metering, and a drive output high state clamp for MOSFET gate protection. These devices are available in dual–in–line and surface mount plastic packages.



Power Factor Controllers (continued)

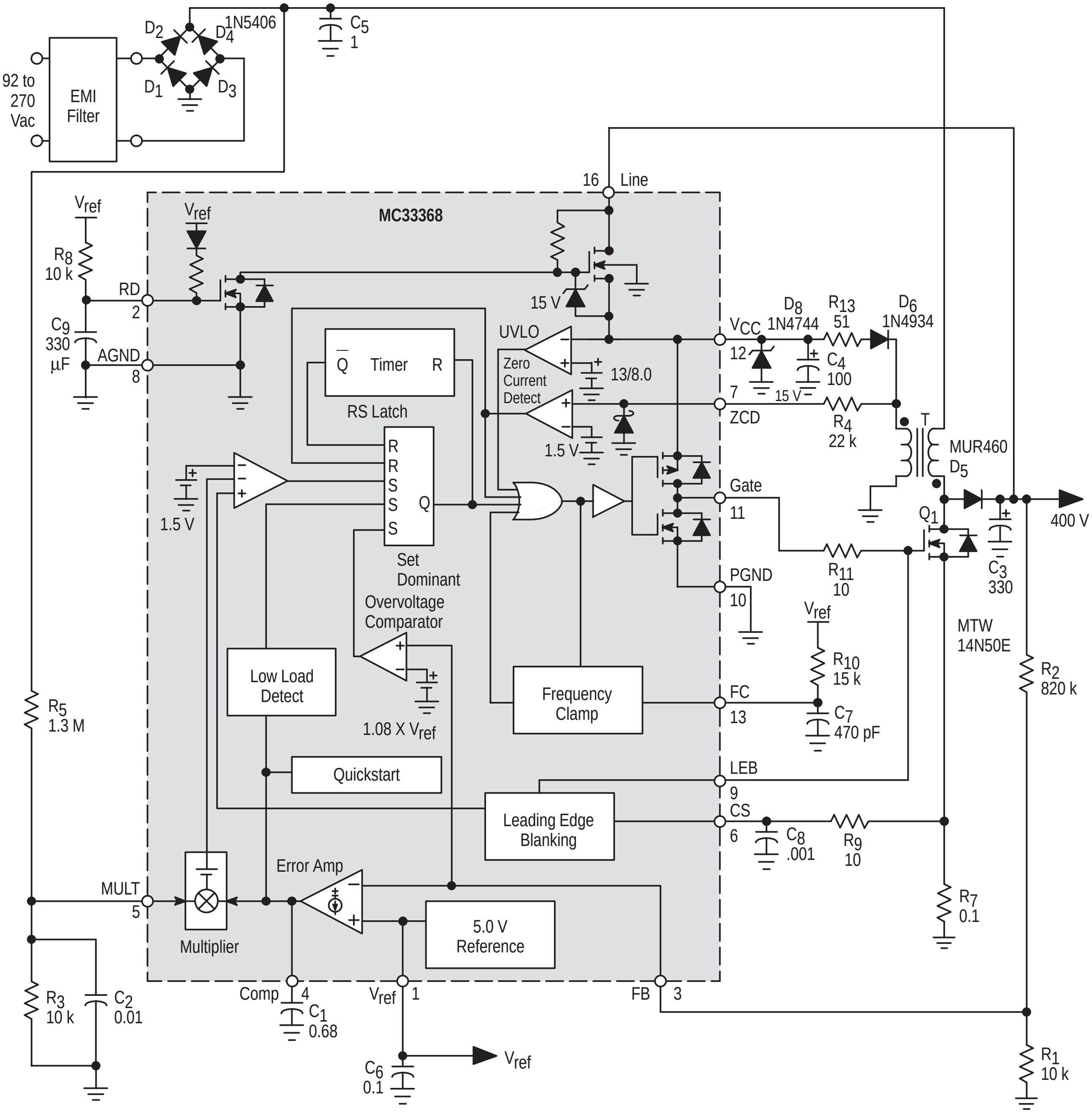
MC33368D

T_J = –25° to +125°C, Case 751K

The MC33368 is an active power factor controller that functions as a boost preconverter in off–line power supply applications. MC33368 is optimized for low power, high density power supplies requiring minimum board area, reduced component count, and low power dissipation. The narrow body SOIC package provides a small footprint. Integration of the high voltage startup saves approximately 0.7 W of power compared to resistor bootstrapped circuits.

The MC33368 features a watchdog timer to initiate output switching, a one quadrant multiplier to force the line current to follow the instantaneous line voltage, a zero current detector to ensure critical conduction operation, a transconductance error amplifier, a current sensing comparator, a 5.0 V reference, an undervoltage lockout (UVLO) circuit which monitors the V_{CC} supply voltage, and a CMOS driver for driving MOSFETs. The MC33368 also includes a programmable output switching frequency clamp. Protection features include an output overvoltage comparator to minimize overshoot, a restart delay timer, and cycle–by–cycle current limiting.

- Lossless Off–Line Startup
- Output Overvoltage Comparator
- Leading Edge Blanking (LEB) for Noise Immunity
- Watchdog Timer to Initiate Switching
- Restart Delay Timer



Supervisory Circuits

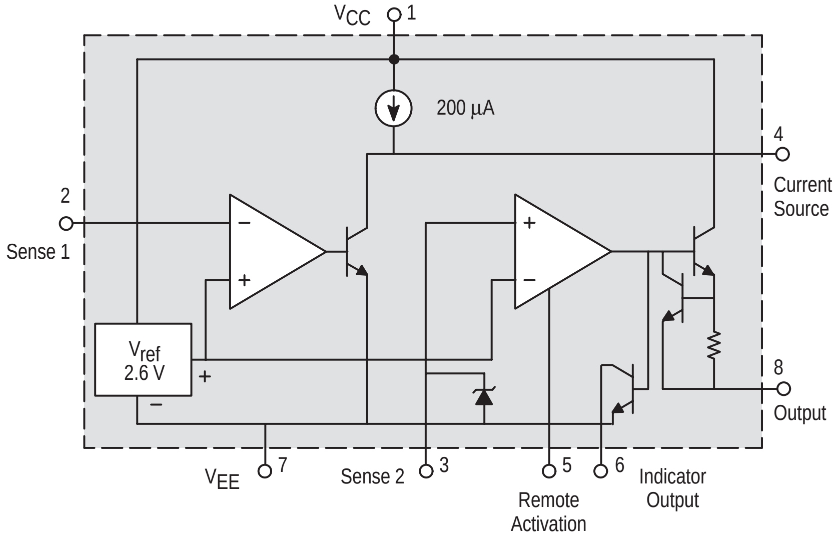
A variety of Power Supervisory Circuits are offered. Overvoltage sensing circuits which drive ‘‘Crowbar’’ SCRs are provided in several configurations from a low cost three–terminal version to 8–pin devices which provide pin–programmable trip voltages or additional features, such as an indicator output drive and remote activation capability. An over/undervoltage protection circuit is also offered.

Overvoltage Crowbar Sensing Circuit

MC3423P1, D

T_A = 0° to +70°C, Case 626, 751

This device can protect sensitive circuitry from power supply transients or regulator failure when used with an external ‘‘Crowbar’’ SCR. The device senses voltage and compares it to an internal 2.6 V reference. Overvoltage trip is adjustable by means of an external resistive voltage divider. A minimum duration before trip is programmable with an external capacitor. Other features include a 300 mA high current output for driving the gate of a ‘‘Crowbar’’ SCR, an open–collector indicator output and remote activation capability.

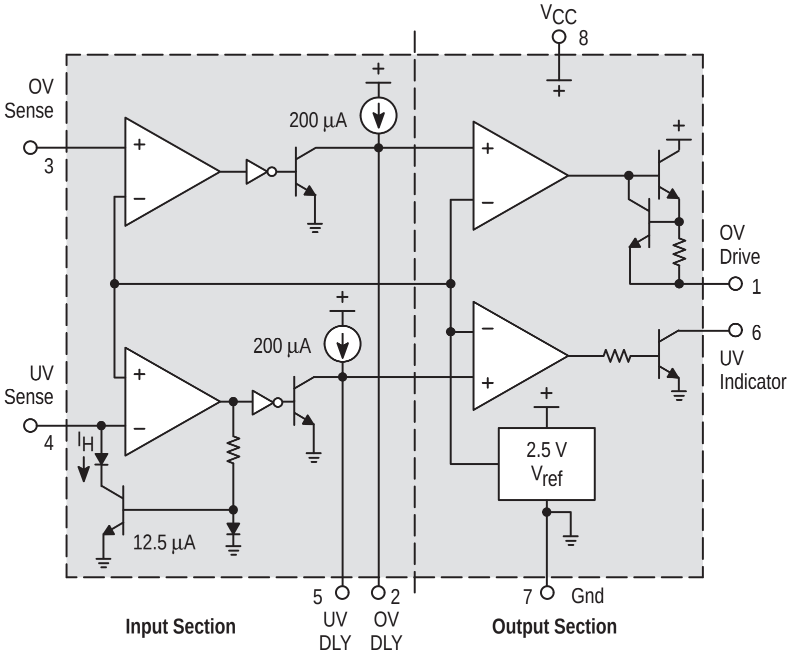


Over/Undervoltage Protection Circuit

MC3425P1

T_A = 0° to +70°C, Case 626

The MC3425 is a power supply supervisory circuit containing all the necessary functions required to monitor over and undervoltage fault conditions. This device features dedicated over and undervoltage sensing channels with independently programmable time delays. The overvoltage channel has a high current drive output for use in conjunction with an external SCR ‘‘Crowbar’’ for shutdown. The undervoltage channel input comparator has hysteresis which is externally programmable, and an open–collector output for fault indication.



CMOS Micropower Undervoltage Sensing Circuits

MC33464H, N

T_A = –30° to +80°C, Case 1213, 1212

The MC33464 series are micropower undervoltage sensing circuits that are specifically designed for use with battery powered microprocessor based systems, where extended battery life is required. A choice of several threshold voltages from 0.9 V to 4.5 V are available. These devices feature a very low quiescent bias current of 0.8 μA typical.

The MC33464 series features a highly accurate voltage reference, a comparator with precise thresholds and built–in hysteresis to prevent erratic reset operation, a choice of output configurations between open drain or complementary MOS, and guaranteed operation below 1.0 V with extremely low standby current. These devices are available in either SOT–89 3–pin or SOT–23 5–pin surface mount packages.

Applications include direct monitoring of the MPU/logic power supply used in portable, appliance, automotive and industrial equipment.

MC33464 Features:

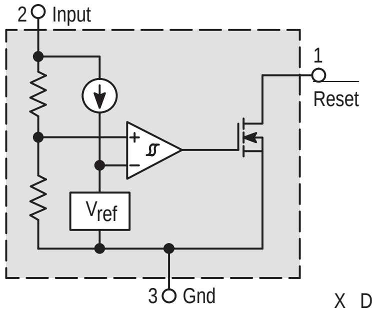
- Extremely Low Standby Current of 0.8 μA at V_{in} = 1.5 V
- Wide Input Voltage Range (0.7 V to 10 V)
- Monitors Power Supply Voltages from 1.1 V to 5.0 V
- High Accuracy Detector Threshold (±2.5%)
- Two Reset Output Types (Open Drain or Complementary Drive)
- Two Surface Mount Packages (SOT–89 or SOT–23 5–Pin)

ORDERING INFORMATION

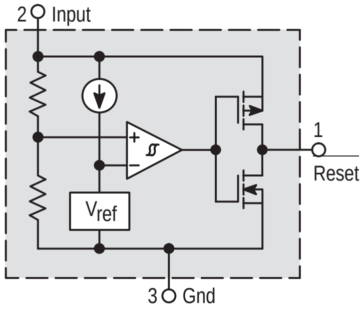
Device	Threshold Voltage	Type	Operating Temperature Range	Package (Qty/Reel)
MC33464H–09AT1	0.9	Open Drain Reset	T_A = –30° to +80°C	SOT–89 (1000)
MC33464H–20AT1	2.0			
MC33464H–27AT1	2.7			
MC33464H–30AT1	3.0			
MC33464H–45AT1	4.5			
MC33464H–09CT1	0.9	Compl. MOS Reset		
MC33464H–20CT1	2.0			
MC33464H–27CT1	2.7			
MC33464H–30CT1	3.0			
MC33464H–45CT1	4.5			
MC33464N–09ATR	0.9	Open Drain Reset		SOT–23 (3000)
MC33464N–20ATR	2.0			
MC33464N–27ATR	2.7			
MC33464N–30ATR	3.0			
MC33464N–45ATR	4.5			
MC33464N–09CTR	0.9	Compl. MOS Reset		
MC33464N–20CTR	2.0			
MC33464N–27CTR	2.7			
MC33464N–30CTR	3.0			
MC33464N–45CTR	4.5			

Other voltages from 0.9 to 6.0 V, in 0.1 V increments, are available upon request. Consult your local Motorola sales office for information.

MC33464X–YYATZ
Open Drain Configuration



MC33464X–YYCTZ
Complementary Drive Configuration



X Denotes Package Type
YY Denotes Threshold Voltage
TZ Denotes Taping Type

CMOS Micropower Undervoltage Sensing Circuits with Output Delay

MC33465N

T_A = –30° to +80°C, Case 1212

The MC33465 series are micropower undervoltage sensing circuits that are specifically designed for use with battery powered microprocessor based systems, where extended battery life is required. A choice of several threshold voltages from 0.9 V to 4.5 V are available. This device features a very low quiescent bias current of 1.0 µA typical.

The MC33465 series features a highly accurate voltage reference, a comparator with precise thresholds and built–in hysteresis to prevent erratic reset operation, a choice of output configurations between open drain or complementary MOS, a time delayed output, which can be programmed by the system designer, and guaranteed operation below 1.0 V with extremely low standby current. This device is available in a SOT–23 5–pin surface mount packages.

Applications include direct monitoring of the MPU/logic power supply used in portable, appliance, automotive and industrial equipment.

MC33465 Features:

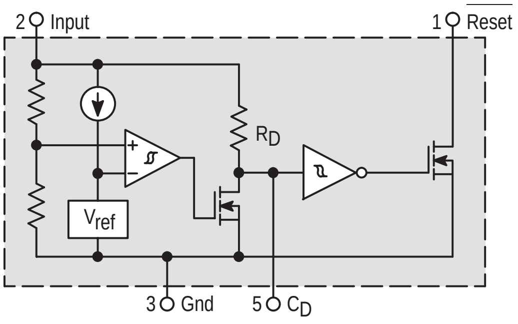
- Extremely Low Standby Current of 1.0 µA at V_{in} = 3.5 V
- Wide Input Voltage Range (0.7 V to 10 V)
- Monitors Power Supply Voltages from 1.1 V to 5.0 V
- High Accuracy Detector Threshold (±2.5%)
- Two Reset Output Types (Open Drain or Complementary Drive)
- Programmable Output Delay by External Capacitor (100 ms typ. with 0.15 µF)
- Surface Mount Package (SOT–23 5–Pin)
- Convenient Tape and Reel (3000 per Reel)

ORDERING INFORMATION

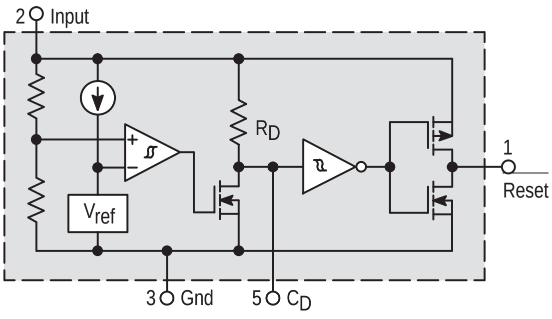
Device	Threshold Voltage	Type	Operating Temperature Range	Package
MC33465N–09ATR	0.9	Open Drain Reset	T_A = –30° to +80°C	SOT–23
MC33465N–20ATR	2.0			
MC33465N–27ATR	2.7			
MC33465N–30ATR	3.0			
MC33465N–45ATR	4.5			
MC33465N–09CTR	0.9	Compl. MOS Reset		
MC33465N–20CTR	2.0			
MC33465N–27CTR	2.7			
MC33465N–30CTR	3.0			
MC33465N–45CTR	4.5			

Other voltages from 0.9 to 6.0 V, in 0.1 V increments, are available upon request. Consult your local Motorola sales office for information.

MC33465N–YYATZ
Open Drain Configuration



MC33465N–YYCTZ
Complementary Drive Configuration



YY Denotes Threshold Voltage
TZ Denotes Taping Type

Undervoltage Sensing Circuit

MC34064P–5, D–5, DM–5
T_A = 0° to +70°C, Case 29, 751, 846A

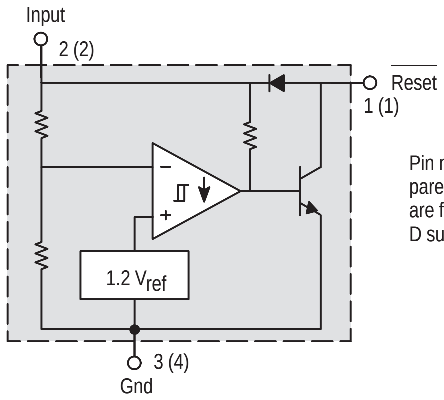
MC33064P–5, D–5, DM–5
T_A = –40° to +85°C, Case 29, 751, 846A

MC34164P–3, P–5, D–3, D–5, DM–3, DM–5
T_A = 0° to +70°C, Case 29, 751, 846A

MC33164P–3, P–5, D–3, D–5, DM–3, DM–5
T_A = –40° to +85°C, Case 29, 751, 846A

The MC34064 and MC34164 are two families of undervoltage sensing circuits specifically designed for use as reset controllers in microprocessor–based systems. They offer the designer an economical solution for low voltage detection with a single external resistor. Both parts feature a trimmed bandgap reference, and a comparator with precise thresholds and built–in hysteresis to prevent erratic reset operation.

The two families of undervoltage sensing circuits taken together, cover the needs of the most commonly specified power supplies used in MCU/MPU systems. Key parameter specifications of the MC34164 family were chosen to complement the MC34064 series. The table summarizes critical parameters of both families. The MC34064 fulfills the needs of a 5.0 V ± 5% system and features a tighter hysteresis specification. The MC34164 series covers 5.0 V ± 10% and 3.0 V ± 5% power supplies with significantly lower power consumption, making them ideal for applications where extended battery life is required such as consumer products or hand held equipment.



Pin numbers in parenthesis are for the D suffix package.

Applications include direct monitoring of the 5.0 V MPU/logic power supply used in appliance, automotive, consumer, and industrial equipment.

The MC34164 is specifically designed for battery powered applications where low bias current (1/25th of the MC34064's) is an important characteristic.

Table 14. Undervoltage Sense/Reset Controller Features

MC34X64 devices are specified to operate from 0° to +70°C, and MC33X64 devices operate from –40° to +85°C.

Device	Standard Power Supply Supported	Typical Threshold Voltage (V)	Typical Hysteresis Voltage (V)	Minimum Output Sink Current (mA)	Power Supply Input Voltage Range (V)	Maximum Quiescent Input Current	Suffix/ Package
MC34064/MC33064	5.0 V ± 5%	4.6	0.02	10	1.0 to 10	500 µA @ V_{in} = 5.0 V	P–5/29
							D–5/751
							DM–5/846A
MC34164/MC33164	5.0 V ± 10%	4.3	0.09	7.0	1.0 to 12	20 µA @ V_{in} = 5.0 V	P–5/29
							D–5/751
							DM–5/846A
MC34164/MC33164	3.0 V ± 5%	2.7	0.06	6.0	1.0 to 12	15 µA @ V_{in} = 3.0 V	P–3/29
							D–3/751
							DM–3/846A

Universal Voltage Monitor

MC34161P, D

T_A = 0° to +70°C, Case 626, 751

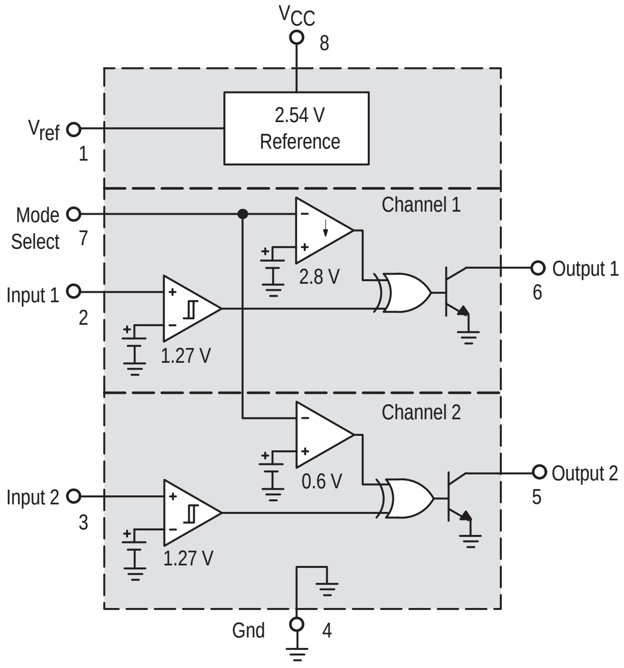
MC33161P, D

T_A = –40° to +85°C, Case 626, 751

The MC34161, MC33161 series are universal voltage monitors intended for use in a wide variety of voltage sensing applications. These devices offer the circuit designer an economical solution for positive and negative voltage detection. The circuit consists of two comparator channels each with hysteresis, a unique Mode Select Input for channel programming, a pinned out 2.54 V reference, and two open collector outputs capable of sinking in excess of 10 mA. Each comparator channel can be configured as either inverting or noninverting by the Mode Select Input. This allows over, under, and window detection of positive and negative voltages. The minimum supply voltage needed for these devices to be fully functional is 2.0 V for positive voltage sensing and 4.0 V for negative voltage sensing.

Applications include direct monitoring of positive and negative voltages used in appliance, automotive, consumer, and industrial equipment.

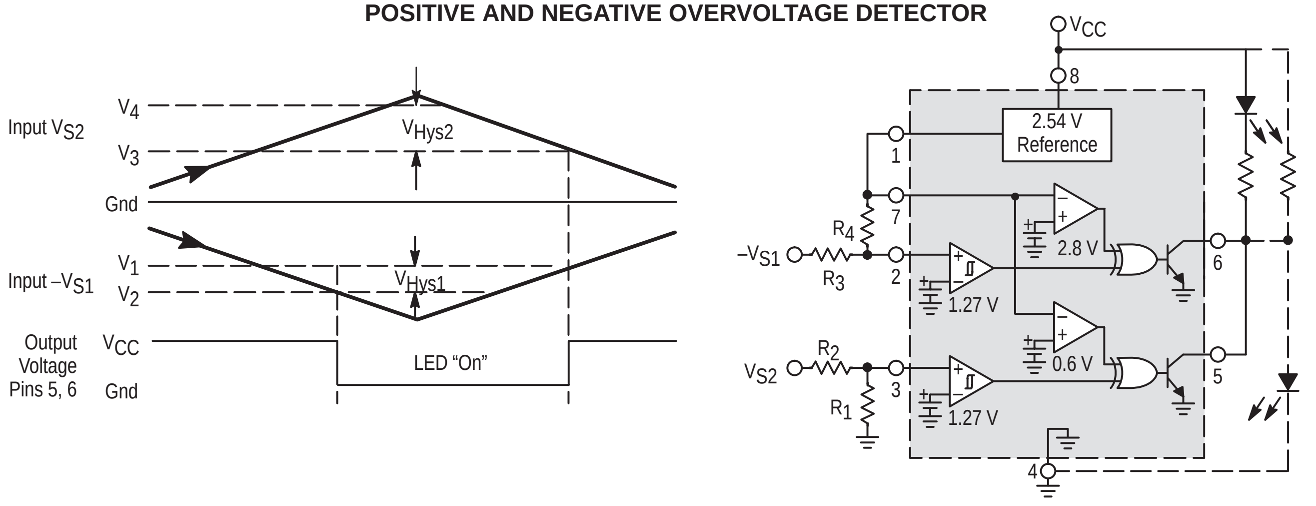
- Unique Mode Select Input Allows Channel Programming
- Over, Under, and Window Voltage Detection
- Positive and Negative Voltage Detection
- Fully Functional at 2.0 V for Positive Voltage Sensing and 4.0 V for Negative Voltage Sensing
- Pinned Out 2.54 V Reference with Current Limit Protection
- Low Standby Current
- Open Collector Outputs for Enhanced Device Flexibility



TRUTH TABLE

Mode Select Pin 7	Input 1 Pin 2	Output 1 Pin 6	Input 2 Pin 3	Output 2 Pin 5	Comments
GND	0 1	0 1	0 1	0 1	Channels 1 & 2: Noninverting
V_{ref}	0 1	0 1	0 1	1 0	Channel 1: Noninverting Channel 2: Inverting
V_{CC} (>2.0 V)	0 1	1 0	0 1	1 0	Channels 1 & 2: Inverting

POSITIVE AND NEGATIVE OVERVOLTAGE DETECTOR



Battery Management Circuits

Battery Charger ICs

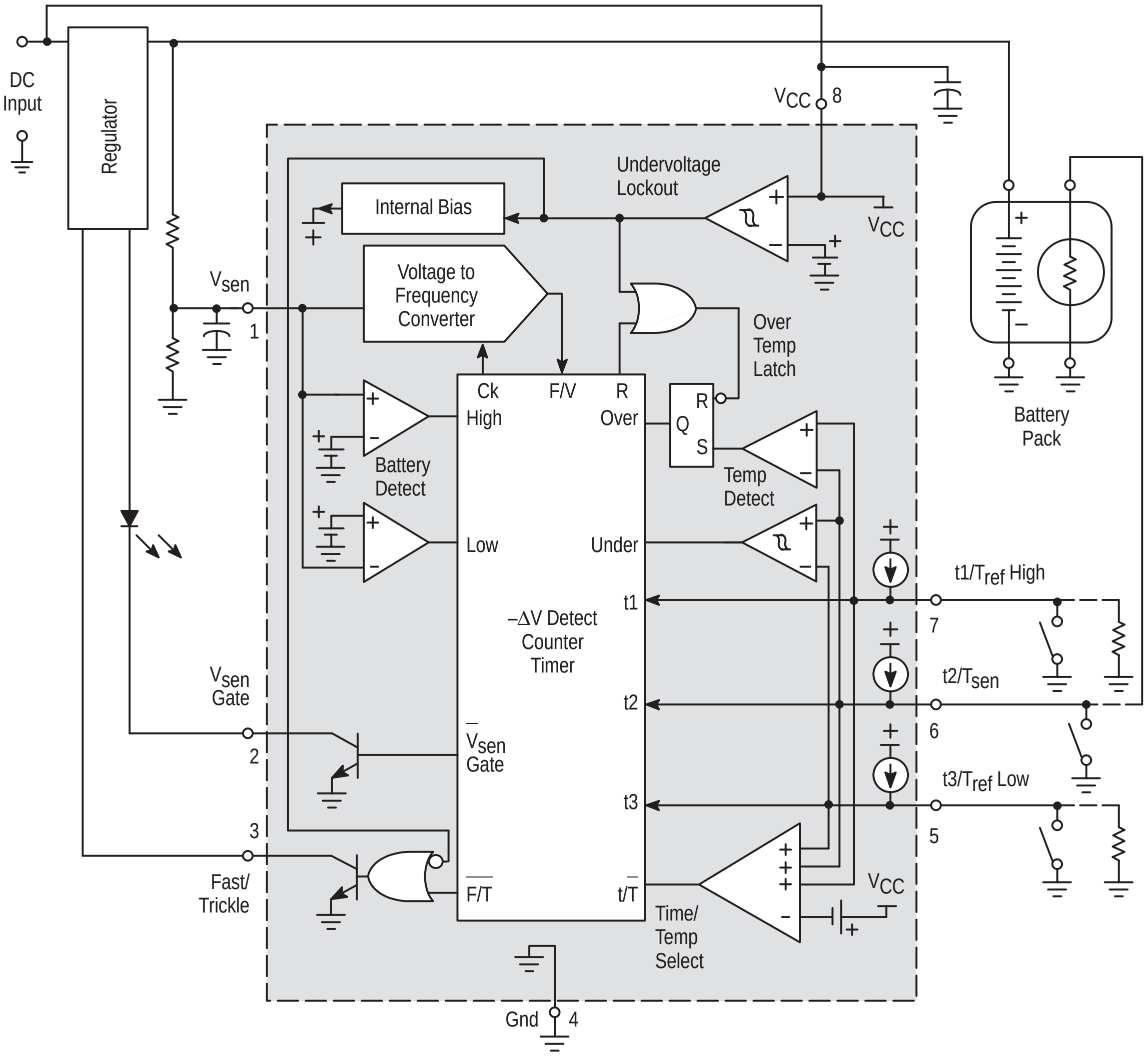
Battery Fast Charge Controller

MC33340P, D

T_A = –25° to +85°C, Case 626, 751

The MC33340 is a monolithic control IC that is specifically designed as a fast charge controller for Nickel Cadmium (NiCd) and Nickel Metal Hydride (NiMH) batteries. This device features negative slope voltage detection as the primary means for fast charge termination. Accurate detection is ensured by an output that momentarily interrupts the charge current for precise voltage sampling. An additional secondary backup termination method can be selected that consists of either a programmable time or temperature limit. Protective features include battery over and undervoltage detection, latched over temperature detection, and power supply input undervoltage lockout with hysteresis. Provisions for entering a rapid test mode are available for enhanced end product testing. This device is available in an economical 8–lead surface mount package.

- Negative Slope Voltage Detection
- Accurate Zero Current Battery Voltage Sensing
- Programmable 1 to 4 Hour Fast Charge Time Limit
- Programmable Over/Under Temperature Detection
- Battery Over and Undervoltage Fast Charge Protection
- Rapid System Test Mode
- Power Supply Input Undervoltage Lockout with Hysteresis
- Operating Voltage Range of 3.0 V to 18 V



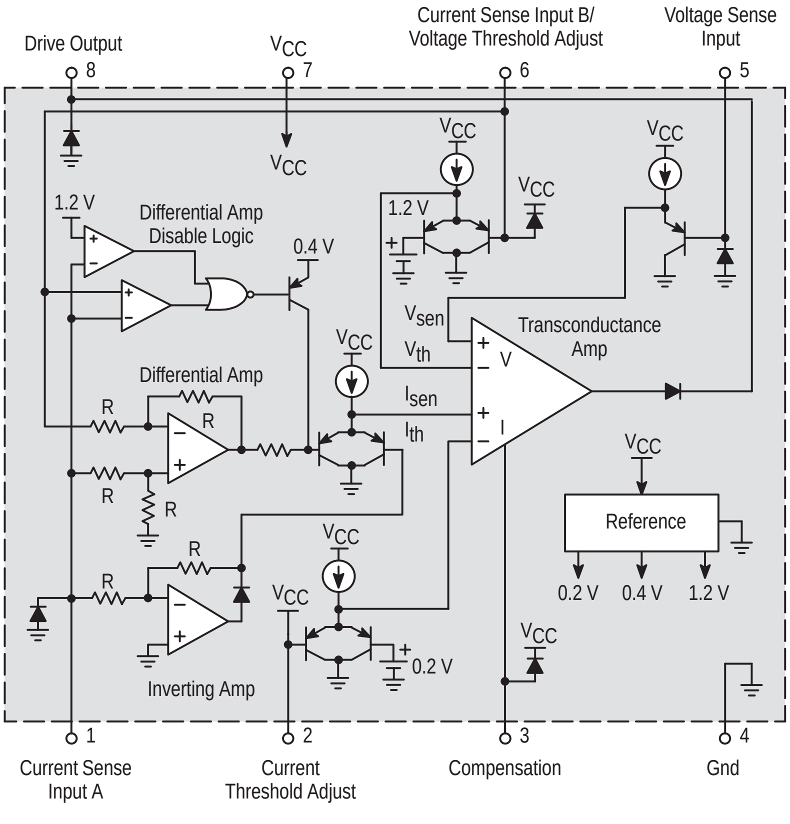
Power Supply
Battery Charger
Regulation Control Circuit

MC33341P, D

T_A = –40° to +85°C, Case 626, 751

The MC33341 is a monolithic regulation control circuit that is specifically designed to close the voltage and current feedback loops in power supply and battery charger applications. This device features the unique ability to perform source high–side, load high–side, source low–side, and load low–side current sensing, each with either an internally fixed or externally adjustable threshold. The various current sensing modes are accomplished by a means of selectively using the internal differential amplifier, inverting amplifier, or a direct input path. Positive voltage sensing is performed by an internal voltage amplifier. The voltage amplifier threshold is internally fixed and can be externally adjusted in all low–side current sensing applications. An active high drive output is provided to directly interface with economical optoisolators for isolated output power systems. This device is available in 8–lead dual–in–line and surface mount packages.

- Differential Amplifier for High–Side Source and Load Current Sensing
- Inverting Amplifier for Source Return Low–Side Current Sensing
- Noninverting Input Path for Load Low–Side Current Sensing
- Fixed or Adjustable Current Threshold in all Current Sensing Modes
- Positive Voltage Sensing in all Current Sensing Modes
- Fixed Voltage Threshold in all Current Sensing Modes
- Adjustable Voltage Threshold in all Low–Side Current Sensing Modes
- Output Driver Directly Interfaces with Economical Optoisolators
- Operating Voltage Range of 2.3 V to 18 V



Battery Pack ICs

Lithium Battery Protection Circuit for One to Four Cell Battery Packs

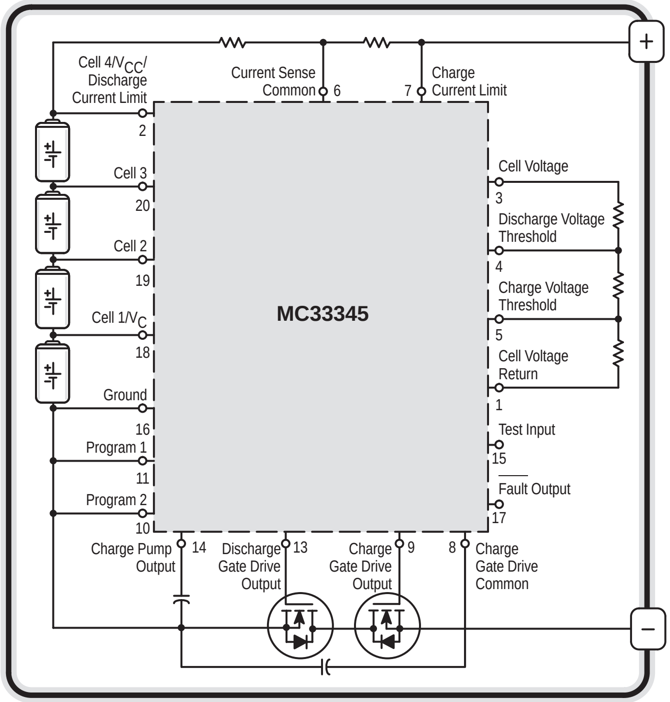
MC33345DW, DTB

T_A = –25° to +85°C, Case 751D, 948E

The MC33345 is a monolithic lithium battery protection circuit that is designed to enhance the useful operating life of one to four cell rechargeable battery packs. Cell protection features consist of independently programmable charge and discharge limits for both voltage and current with a delayed current shutdown, cell voltage balancing with on–chip balancing resistors, and a virtually zero current sleepmode state when the cells are discharged. Additional features include an on–chip charge pump for reduced MOSFET losses while charging or discharging a low cell voltage battery pack, and the programmability for a one to four cell battery pack. This protection circuit requires a minimum number of external components and is targeted for inclusion within the battery pack. The MC33345 is available in standard and low profile 20 lead surface mount packages.

- Independently Programmable Charge and Discharge Limits for Both Voltage and Current
- Charge and Discharge Current Limit Detection with Delayed Shutdown
- Cell Voltage Balancing
- On–Chip Balancing Resistors
- Virtually Zero Current Sleepmode State when Cells are Discharged
- Charge Pump for Reduced Losses with a Low Cell Voltage Battery Pack
- Programmable for One, Two, Three or Four Cell Applications
- Minimum External Components for Inclusion within the Battery Pack
- Available in Low Profile Surface Mount Packages

Typical Four Cell Smart Battery Pack



Battery Pack ICs (continued)

Lithium Battery Protection Circuit for Three or Four Cell Battery Packs

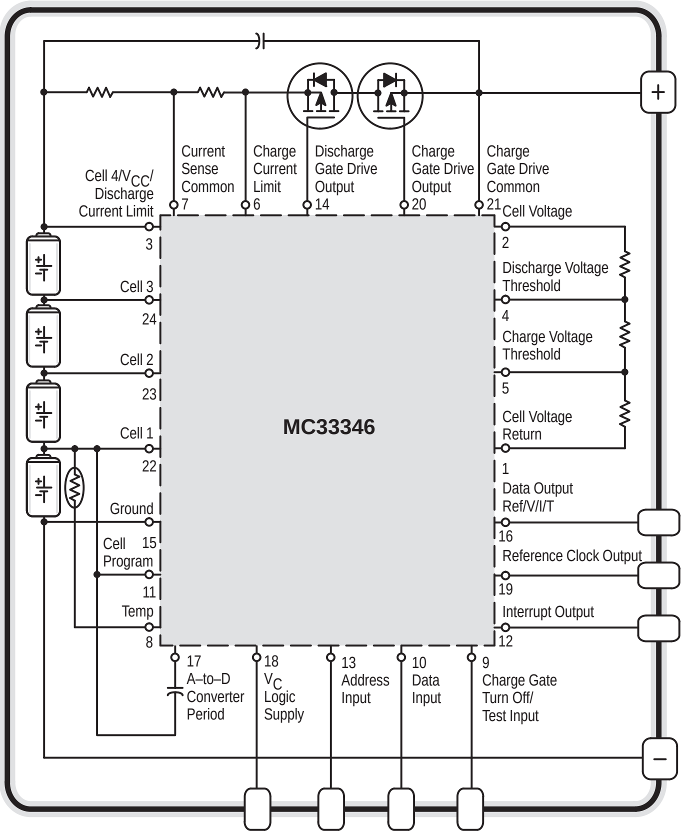
MC33346DW, DTB

T_A = –40° to +85°C, Case 751E, 948H

The MC33346 is a monolithic lithium battery protection circuit that is designed to enhance the useful operating life of three or four cell rechargeable battery packs. Cell protection features consist of independently programmable charge and discharge limits for both voltage and current with a delayed current shutdown, cell voltage balancing with on–chip balancing resistors, and virtually zero current sleepmode state when the cells are discharged. Additional features consists of a six wire microcontroller interface bus that can selectively provide a pulse output that represents the internal reference voltage, cell voltage, cell current and temperature, as well as control the states of four internal balancing and two external MOSFET switches. A microcontroller time reference output is available for gas gauge implementation. This protection circuit requires a minimum number of external components and is targeted for inclusion within the battery pack. The MC33346 is available in standard and low profile 24 lead surface mount packages.

- Independently Programmable Charge and Discharge Limits for Both Voltage and Current
- Delayed Current Shutdown
- Cell Voltage Balancing with On–Chip Resistors
- Six Wire Microcontroller Interface Bus
- Data Output for Reference, Voltage, Current, and Temperature
- Microcontroller Time Reference Output for Gas Gauging
- Virtually Zero Current Sleepmode State when Cells are Discharged
- Programmable for Three or Four Cell Applications
- Minimum External Components for Inclusion within the Battery Pack
- Available in Low Profile Surface Mount Packages

Typical Four Cell Smart Battery Pack



Lithium Battery Protection Circuit for One or Two Cell Battery Packs

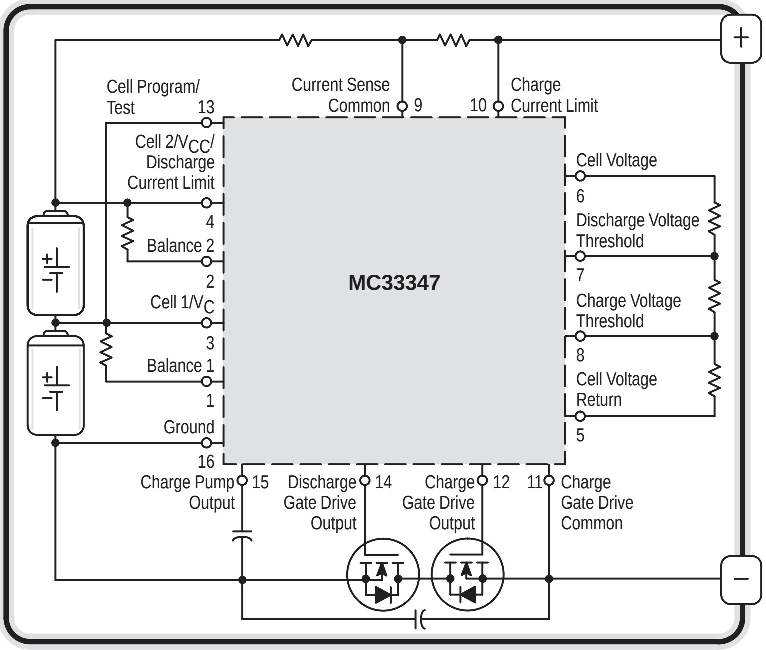
MC33347D, DTB

T_A = –25° to +85°C, Case 751B, 948F

The MC33347 is a monolithic lithium battery protection circuit that is designed to enhance the useful operating life of one or two cell rechargeable battery packs. Cell protection features consist of independently programmable charge and discharge limits for both voltage and current with a delayed current shutdown, continuous cell voltage balancing with the choice of on–chip or external balancing resistors, and a virtually zero current sleepmode state when the cells are discharged. Additional features include an on–chip charge pump for reduced MOSFET losses while charging or discharging a low cell voltage battery pack, and the programmability for one or two cell battery pack. This protection circuit requires a minimum number of external components and is targeted for inclusion within the battery pack. This MC33347 is avaialble in standard and low profile 16 lead surface mount packages.

- Independently Programmable Charge and Discharge Limits for Both Voltage and Current
- Charge and Discharge Current Limit Detection with Delayed Shutdown
- Continuous Cell Voltage Balancing
- On–Chip or External Balancing Resistors
- Virtually Zero Current Sleepmode State when Cells are Discharged
- Charge Pump for Reduced Losses with a Low Cell Voltage Battery Pack
- Programmable for One or Two Cell Applications
- Minimum External Components for Inclusion within the Battery Pack
- Available in Low Profile Surface Mount Packages

Typical Two Cell Smart Battery Pack



Battery Pack ICs (continued)

Lithium Battery Protection Circuit for One Cell Battery Packs

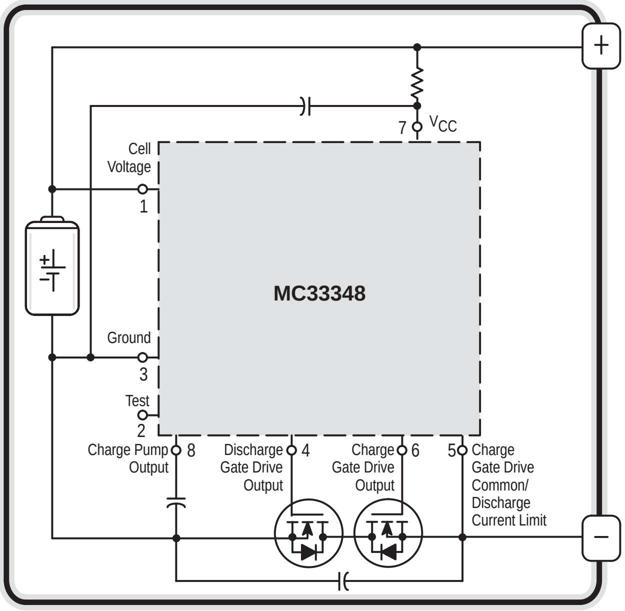
MC33348D, DM

T_A = –25° to +85°C, Case 751, 846A

The MC33348 is a monolithic lithium battery protection circuit that is designed to enhance the useful operating life of one cell rechargeable battery pack. Cell protection features consist of internally trimmed charge and discharge voltage limits, discharge current limit detection with a delayed shutdown, and a virtually zero current sleepmode state when the cell is discharged. An additional feature includes an on–chip charge pump for reduced MOSFET losses while charging or discharging a low cell voltage battery pack. This protection circuit requires a minimum number of external components and is targeted for inclusion within the battery pack. This MC33348 is available in standard and micro 8 lead surface mount packages.

- Internally Trimmed Charge and Discharge Voltage Limits
- Discharge Current Limit Detection with Delayed Shutdown
- Virtually Zero Current Sleepmode State when Cells are Discharged
- Charge Pump for Reduced Losses with a Low Cell Voltage Battery Pack
- Dedicated for One Cell Applications
- Minimum Components for Inclusion within the Battery Pack
- Available in Low Profile Surface Mount Packages

Typical One Cell Smart Battery Pack



ORDERING INFORMATION

Device	Charge Overvoltage Threshold (V)	Charge Overvoltage Hysteresis (mV)	Discharge Undervoltage Threshold (V)	Discharge Current Limit Threshold (mV)	Operating Temperature Range	Package
MC33348D–1	4.20	300	2.25	400	T_A = –25° to +85°C	SO–8
MC33348D–2				200		
MC33348D–3	4.25		2.28	400		
MC33348D–4				200		
MC33348D–5	4.35		2.30	400		
MC33348D–6				200		
MC33348DM–1	4.20		2.25	400		Micro–8
MC33348DM–2				200		
MC33348DM–3	4.25		2.28	400		
MC33348DM–4				200		
MC33348DM–5	4.35		2.30	400		
MC33348DM–6				200		

NOTE: Additional threshold limit options can be made available. Consult your local Motorola sales office for information.

MOSFET/IGBT Drivers

High Speed Dual Drivers

(Inverting)

MC34151P, D

T_A = 0° to +70°C, Case 626, 751

MC33151P, D

T_A = –40° to +85°C, Case 626, 751

(Noninverting)

MC34152P, D

T_A = 0° to +70°C, Case 626, 751

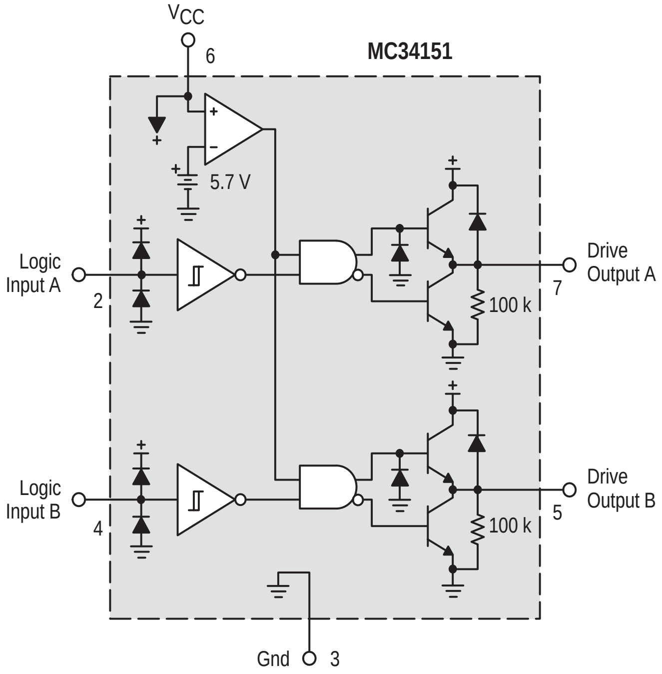
MC33152P, D

T_A = –40° to +85°C, Case 626, 751

These two series of high speed dual MOSFET driver ICs are specifically designed for applications requiring low current digital circuitry to drive large capacitive loads at high slew rates. Both series feature a unique undervoltage lockout function which puts the outputs in a defined low state in an undervoltage condition. In addition, the low “on” state resistance of these bipolar drivers allows significantly higher output currents at lower supply voltages than with competing drivers using CMOS technology.

The MC34151 series is pin–compatible with the MMH0026 and DS0026 dual MOS clock drivers, and can be used as drop–in replacements to upgrade system performance. The MC34152 noninverting series is a mirror image of the inverting MC34151 series.

These devices can enhance the drive capabilities of first generation switching regulators or systems designed with CMOS/TTL logic devices. They can be used in dc–to–dc converters, motor controllers, capacitor charge pump converters, or virtually any other application requiring high speed operation of power MOSFETs.



Single IGBT Driver

MC33153P, D

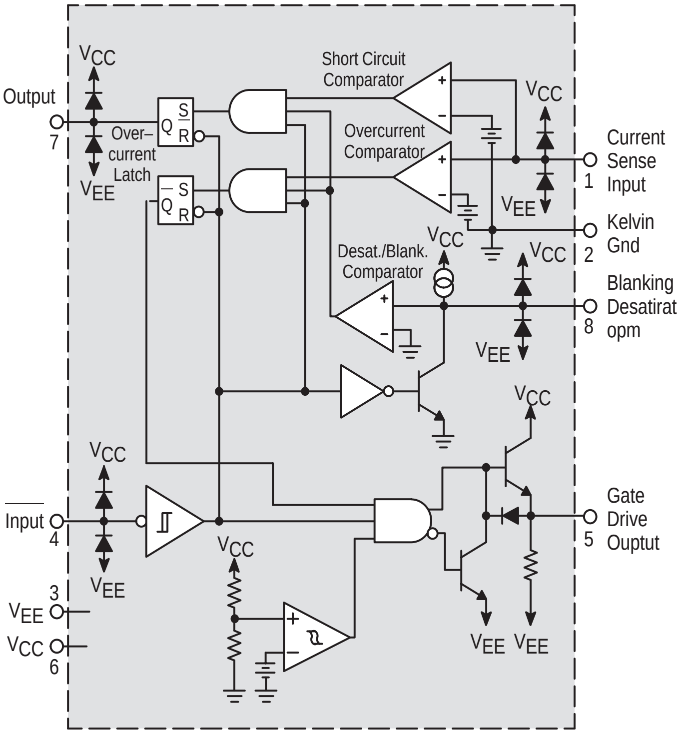
T_A = –40° to +105°C, Case 626, 751

The MC33153 is specifically designed to drive the gate of an IGBT used for ac induction motors. It can be used with discrete IGBTs and IBGT modules up to 100 A.

Typical applications are ac induction motor control, brushless dc motor control, and uninterruptable power supplies.

These devices are available in dual–in–line and surface mount packages and include the following features:

- High Current Output Stage : 1.0 A Source – 2.0 A Sink
- Protection Circuits for Both Conventional and SenseIGBTs
- Current Source for Blanking Timing
- Protection Against Overcurrent and Short Circuit
- Undervoltage Lockout Optimized for IGBT’s
- Negative Gate Drive Capability



MOSFET/IGBT Drivers (continued)

Single IGBT Gate Driver

MC33154D, P

T_A = –40° to +85°C, Case 626, 751

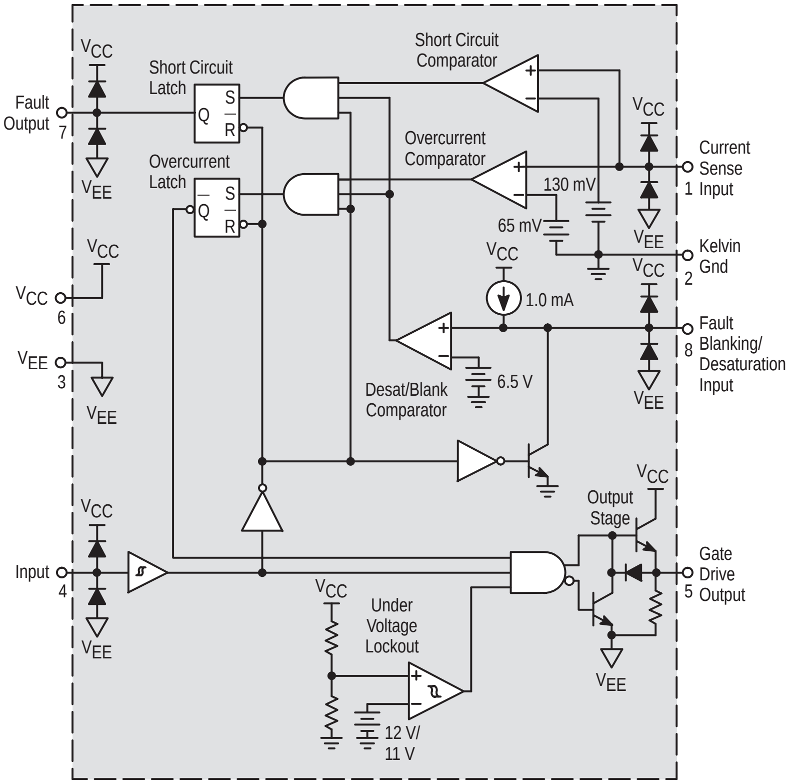
The MC33154 is specifically designed as an IGBT driver for high power applications including ac induction motor control, brushless dc motor control and uninterruptible power supplies.

The MC33154 is similar to the MC33153, except that the output drive is in–phase with the logic input, the output source current drive is four times higher and the supply voltage rating is higher.

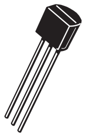
Although designed for driving discrete and module IGBTs, this device offers a cost effective solution for driving power MOSFETs and Bipolar Transistors.

These devices are available in dual–in–line and surface mount packages and include the following features:

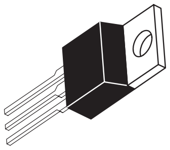
- High Current Output Stage: 4.0 A Source/2.0 A Sink
- Protection Circuits for Both Conventional and Sense IGBTs
- Programmable Fault Blanking Time
- Protection against Overcurrent and Short Circuit
- Undervoltage Lockout Optimzed for IGBTs
- Negative Gate Drive Capability
- Cost Effectively Drives Power MOSFETs and Bipolar Transistors



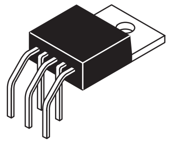
Power Supply Circuits Package Overview



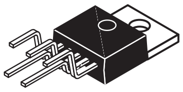
CASE 29
P, Z SUFFIX



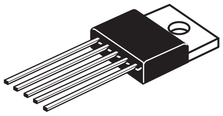
CASE 221A
T, KC SUFFIX



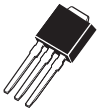
CASE 314A
TH SUFFIX



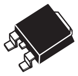
CASE 314B
TV SUFFIX



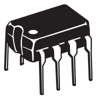
CASE 314D
T SUFFIX



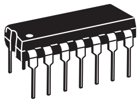
CASE 369
DT–1 SUFFIX



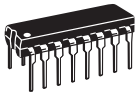
CASE 369A
DT SUFFIX



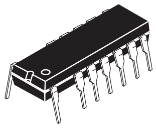
CASE 626
N, P, P1 SUFFIX



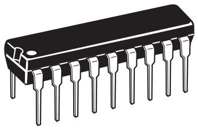
CASE 646
P SUFFIX



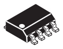
CASES 648, 648C
N, P, P2 SUFFIX



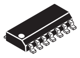
CASE 648E
P SUFFIX



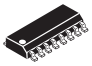
CASE 707
N SUFFIX



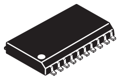
CASE 751
D, D1, D2 SUFFIX



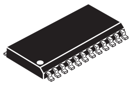
CASE 751A
D SUFFIX



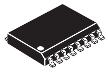
CASE 751B
D SUFFIX



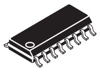
CASE 751D
DW SUFFIX



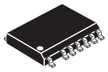
CASE 751E
DW SUFFIX



CASE 751G
DW SUFFIX

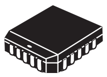


CASE 751K
D SUFFIX



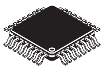
CASE 751N
DW SUFFIX

Power Supply Circuits Package Overview (continued)

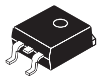


CASE 775
FN SUFFIX

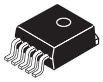
CASE 846A
DM SUFFIX



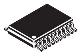
CASE 873A
FB SUFFIX



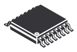
CASE 936
D2T SUFFIX



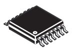
CASE 936A
D2T SUFFIX



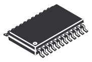
CASE 948E
DTB SUFFIX



CASE 948F
DTB SUFFIX



CASE 948G
DTB SUFFIX



CASE 948H
DTB SUFFIX

CASE 1212
N SUFFIX

CASE 1213
H SUFFIX

Device Listing and Related Literature

Linear Voltage Regulators

Switching Regulator Control

Switching Regulator Control (continued)

Device	**Function**	**Page**
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TL594	Precision Switchmode Pulse Width Modulation Control Circuit	3–726
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UC3844, 45, UC2844, 45	High Performance Current Mode Controllers	3–769
UC3844B, 45B, UC2844B, 45B	High Performance Current Mode Controllers	3–782
μA78S40	Universal Switching Regulator Subsystem	3–796

Special Switching Regulator Controllers

MC34270, 34271	Liquid Crystal Display and Backlight Integrated Controller	3–641
MC44602	High Performance Current Mode Controller	3–651
MC44603	Mixed Frequency Mode GreenLine PWM Controller	3–667
MC44604	High Safety Standby Ladder Mode GreenLine PWM Controller	3–689
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MC34160, 33160	Microprocessor Voltage Regulator and Supervisory Circuit	3–530
MC34161, 33161	Universal Voltage Monitors	3–537
MC34164, 33164	Micropower Undervoltage Sensing Circuits	3–564

ADDENDUM

RELATED APPLICATION NOTES

App Note	Title	Related Device
AN703	Designing Digitally–Controlled Power Supplies	**MC1723C**
AN719	A New Approach to Switching Regulators	**General**
AN1040	Mounting Techniques for Power Semiconductors	**LM317, LM337, MC7800, MC78M00, MC7900, MC79M00**
AN1065	Use of the MC68HC68T1 Real–Time Clock with Multiple Time Bases	**MC34164, MC33164**
AN1315	An Evaluation System Interfacing the MPX2000 Series Pressure Sensors to a Microprocessor	**MC34064, MC33064**
AN920	Theory and Applications of the MC34063 and µA78S40 Switching Regulator Control CIrcuits	**µA78S40**
AN976	A New High Performance Current–Mode Controller Teams Up with Current Sensing Power MOSFETs	**MC34129**
AN983	A Simplified Power Supply Design Using the TL494 Control Circuit	**TL494**
ANE424	50 W Current Mode Controlled Offline Switchmode Power Supply	**UC3842A, UC2842A UC3843A, UC2843A**

LM317

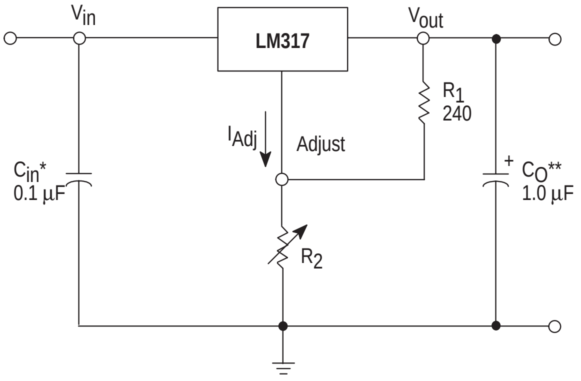
Three-Terminal Adjustable Output Positive Voltage Regulator

The LM317 is an adjustable 3–terminal positive voltage regulator capable of supplying in excess of 1.5 A over an output voltage range of 1.2 V to 37 V. This voltage regulator is exceptionally easy to use and requires only two external resistors to set the output voltage. Further, it employs internal current limiting, thermal shutdown and safe area compensation, making it essentially blow–out proof.

The LM317 serves a wide variety of applications including local, on card regulation. This device can also be used to make a programmable output regulator, or by connecting a fixed resistor between the adjustment and output, the LM317 can be used as a precision current regulator.

- Output Current in Excess of 1.5 A
- Output Adjustable between 1.2 V and 37 V
- Internal Thermal Overload Protection
- Internal Short Circuit Current Limiting Constant with Temperature
- Output Transistor Safe–Area Compensation
- Floating Operation for High Voltage Applications
- Available in Surface Mount D^{2}PAK, and Standard 3–Lead Transistor Package
- Eliminates Stocking many Fixed Voltages

Standard Application



* C_{in} is required if regulator is located an appreciable distance from power supply filter.
** C_O is not needed for stability, however, it does improve transient response.

$$V_{out} = 1.25\ V\left(1+\frac{R_2}{R_1}\right)+I_{Adj}\,R_2$$

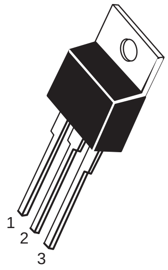
Since I_{Adj} is controlled to less than 100 µA, the error associated with this term is negligible in most applications.

THREE–TERMINAL ADJUSTABLE POSITIVE VOLTAGE REGULATOR

SEMICONDUCTOR TECHNICAL DATA

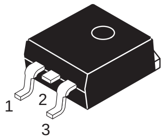
T SUFFIX
PLASTIC PACKAGE
CASE 221A

Heatsink surface
connected to Pin 2.



Pin 1. Adjust
2. V_{out}
3. V_{in}

D2T SUFFIX
PLASTIC PACKAGE
CASE 936
(D^{2}PAK)



Heatsink surface (shown as terminal 4 in case outline drawing) is connected to Pin 2.

ORDERING INFORMATION

Device	Operating Temperature Range	Package
LM317BD2T	T_J = –40° to +125°C	Surface Mount
LM317BT		Insertion Mount
LM317D2T	T_J = 0° to +125°C	Surface Mount
LM317T		Insertion Mount

MAXIMUM RATINGS

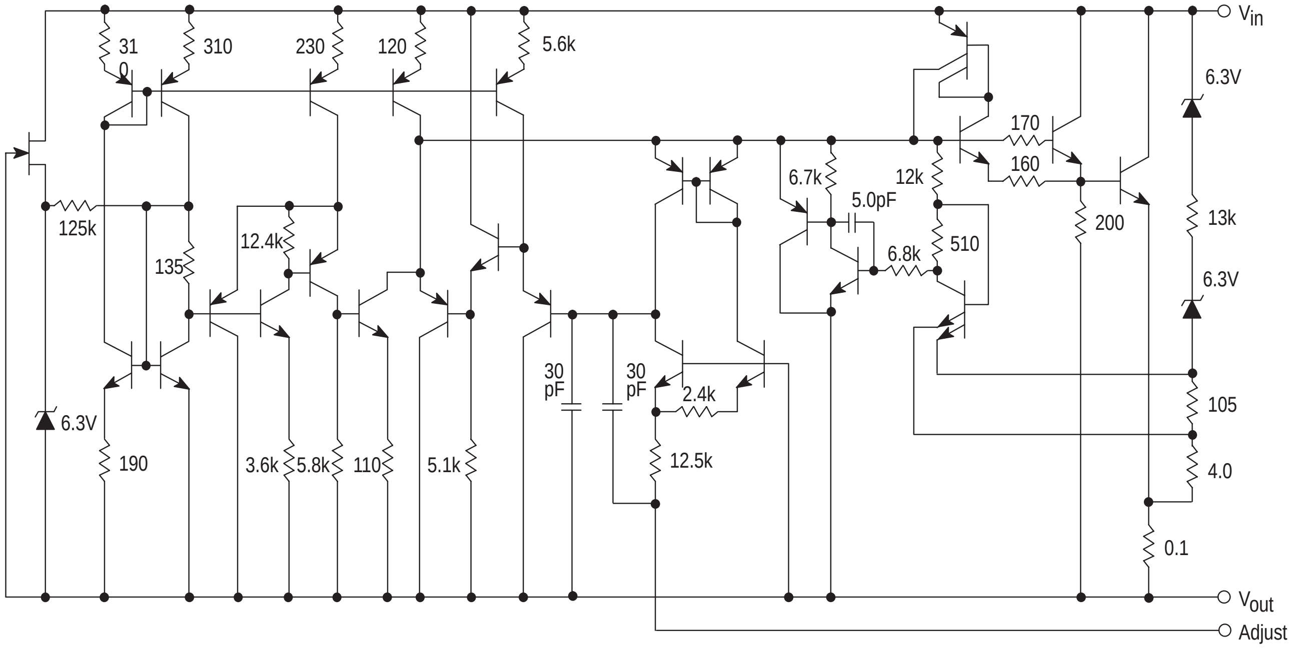
Rating	Symbol	Value	Unit
Input–Output Voltage Differential	$V_I–V_O$	40	Vdc
Power Dissipation			
Case 221A			
T_A = +25°C	P_D	Internally Limited	W
Thermal Resistance, Junction–to–Ambient	θ_{JA}	65	°C/W
Thermal Resistance, Junction–to–Case	θ_{JC}	5.0	°C/W
Case 936 (D^2PAK)			
T_A = +25°C	P_D	Internally Limited	W
Thermal Resistance, Junction–to–Ambient	θ_{JA}	70	°C/W
Thermal Resistance, Junction–to–Case	θ_{JC}	5.0	°C/W
Operating Junction Temperature Range	T_J	–40 to +125	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

ELECTRICAL CHARACTERISTICS ($V_I–V_O$ = 5.0 V; I_O = 0.5 A for D2T and T packages; $T_J = T_{low}$ to T_{high} [Note 1]; I_{max} and P_{max} [Note 2]; unless otherwise noted.)

Characteristics	Figure	Symbol	Min	Typ	Max	Unit
Line Regulation (Note 3), T_A = +25°C, 3.0 V ≤ $V_I–V_O$ ≤ 40 V	1	Reg_{line}	–	0.01	0.04	%/V
Load Regulation (Note 3), T_A = +25°C, 10 mA ≤ I_O ≤ I_{max}	2	Reg_{load}				
V_O ≤ 5.0 V			–	5.0	25	mV
V_O ≥ 5.0 V			–	0.1	0.5	% V_O
Thermal Regulation, T_A = +25°C (Note 6), 20 ms Pulse		Reg_{therm}	–	0.03	0.07	% V_O/W
Adjustment Pin Current	3	I_{Adj}	–	50	100	µA
Adjustment Pin Current Change, 2.5 V ≤ $V_I–V_O$ ≤ 40 V, 10 mA ≤ I_L ≤ I_{max}, P_D ≤ P_{max}	1, 2	ΔI_{Adj}	–	0.2	5.0	µA
Reference Voltage, 3.0 V ≤ $V_I–V_O$ ≤ 40 V, 10 mA ≤ I_O ≤ I_{max}, P_D ≤ P_{max}	3	V_{ref}	1.2	1.25	1.3	V
Line Regulation (Note 3), 3.0 V ≤ $V_I–V_O$ ≤ 40 V	1	Reg_{line}	–	0.02	0.07	% V
Load Regulation (Note 3), 10 mA ≤ I_O ≤ I_{max}	2	Reg_{load}				
V_O ≤ 5.0 V			–	20	70	mV
V_O ≥ 5.0 V			–	0.3	1.5	% V_O
Temperature Stability (T_{low} ≤ T_J ≤ T_{high})	3	T_S	–	0.7	–	% V_O
Minimum Load Current to Maintain Regulation ($V_I–V_O$ = 40 V)	3	I_{Lmin}	–	3.5	10	mA
Maximum Output Current	3	I_{max}				A
$V_I–V_O$ ≤ 15 V, P_D ≤ P_{max}, T Package			1.5	2.2	–	
$V_I–V_O$ = 40 V, P_D ≤ P_{max}, T_A = +25°C, T Package			0.15	0.4	–	
RMS Noise, % of V_O, T_A = +25°C, 10 Hz ≤ f ≤ 10 kHz		N	–	0.003	–	% V_O
Ripple Rejection, V_O = 10 V, f = 120 Hz (Note 4)	4	RR				dB
Without C_{Adj}			–	65	–	
C_{Adj} = 10 µF			66	80	–	
Long–Term Stability, $T_J = T_{high}$ (Note 5), T_A = +25°C for Endpoint Measurements	3	S	–	0.3	1.0	%/1.0 k Hrs.
Thermal Resistance Junction to Case, T Package		$R_{\theta JC}$	–	5.0	–	°C/W

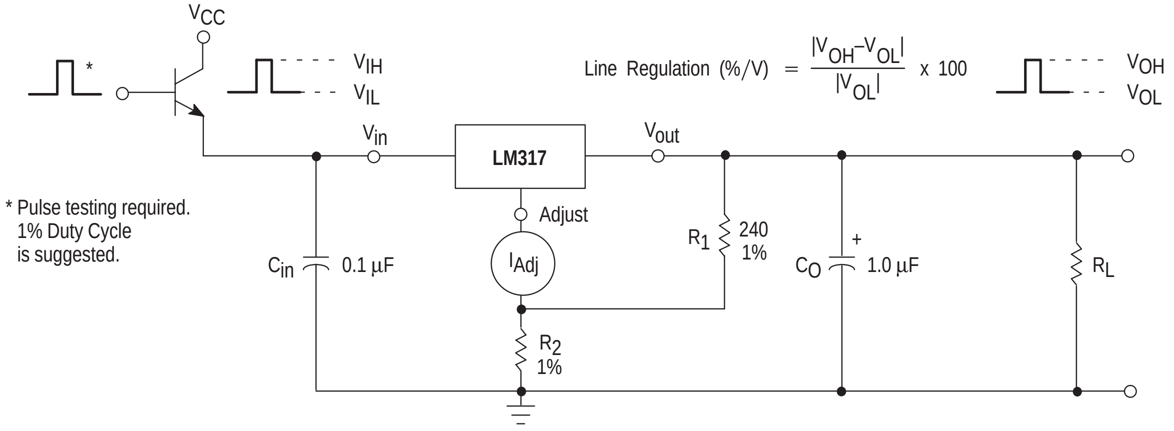
NOTES:
1. T_{low} to T_{high} = 0° to +125°C, for LM317T, D2T. T_{low} to T_{high} = –40° to +125°C, for LM317BT, BD2T.
2. I_{max} = 1.5 A, P_{max} = 20 W
3. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.
4. C_{Adj}, when used, is connected between the adjustment pin and ground.
5. Since Long–Term Stability cannot be measured on each device before shipment, this specification is an engineering estimate of average stability from lot to lot.
6. Power dissipation within an IC voltage regulator produces a temperature gradient on the die, affecting individual IC components on the die. These effects can be minimized by proper integrated circuit design and layout techniques. Thermal Regulation is the effect of these temperature gradients on the output voltage and is expressed in percentage of output change per watt of power change in a specified time.

Representative Schematic Diagram



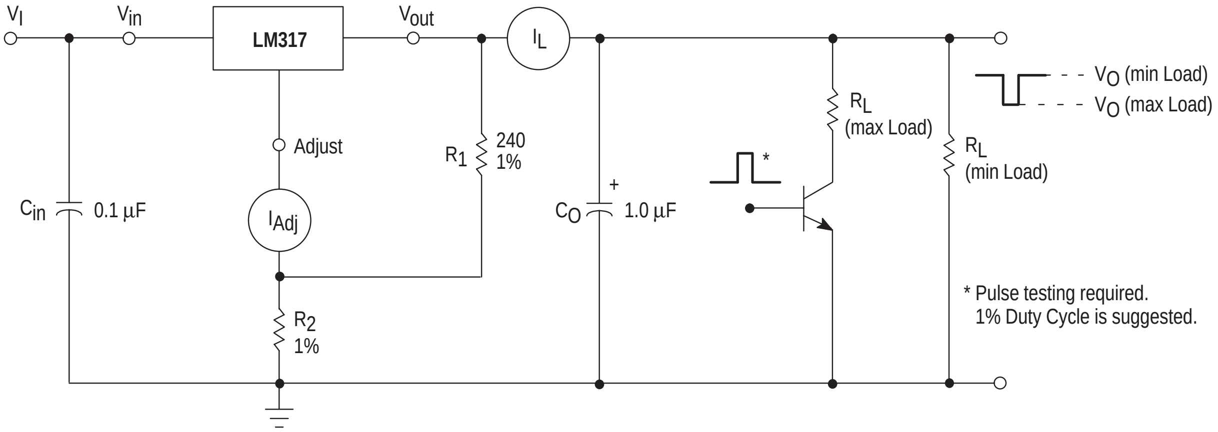
This device contains 29 active transistors.

Figure 1. Line Regulation and ΔI_{Adj}/Line Test Circuit



* Pulse testing required.
1% Duty Cycle
is suggested.

Figure 2. Load Regulation and ΔI_{Adj}/Load Test Circuit

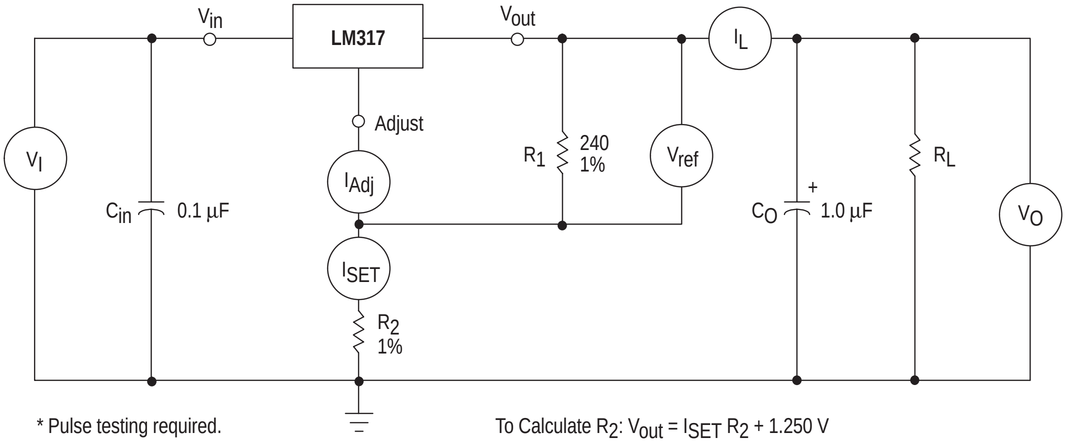


* Pulse testing required.
1% Duty Cycle is suggested.

Load Regulation (mV) = V_O (min Load) – V_O (max Load)

$$\text{Load Regulation } (\%\ V_O) = \frac{V_O \text{ (min Load)} - V_O \text{ (max Load)}}{V_O \text{ (min Load)}} \times 100$$

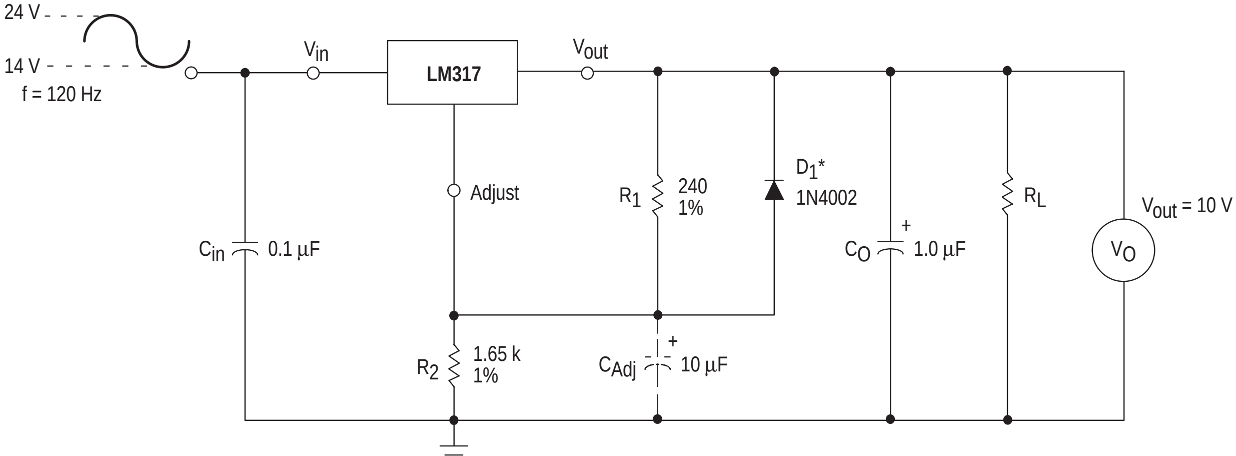
Figure 3. Standard Test Circuit



* Pulse testing required.
1% Duty Cycle is suggested.

To Calculate R_2: $V_{out} = I_{SET} R_2 + 1.250$ V
Assume $I_{SET} = 5.25$ mA

Figure 4. Ripple Rejection Test Circuit



* D_1 Discharges C_{Adj} if output is shorted to Ground.

Figure 5. Load Regulation

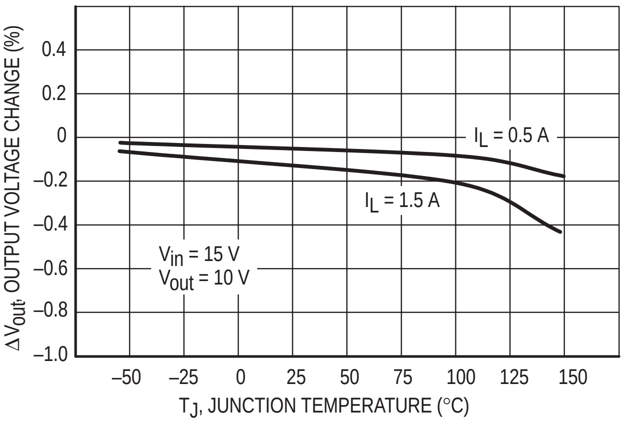


Figure 6. Current Limit

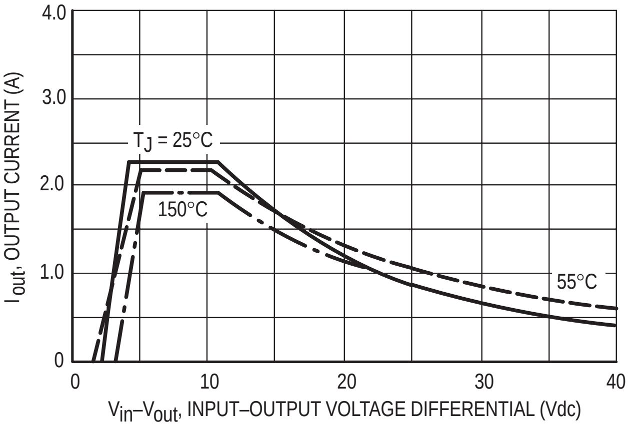


Figure 7. Adjustment Pin Current

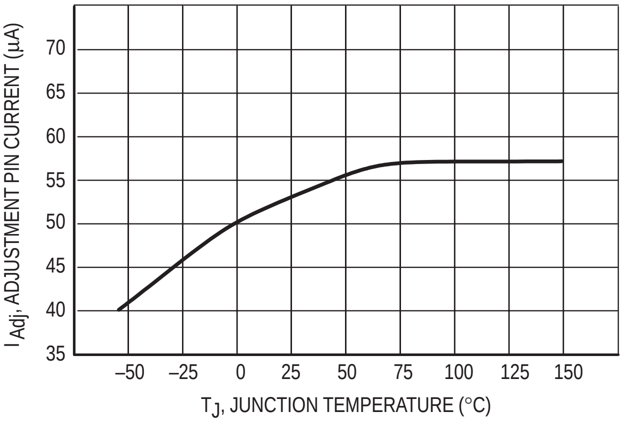


Figure 8. Dropout Voltage

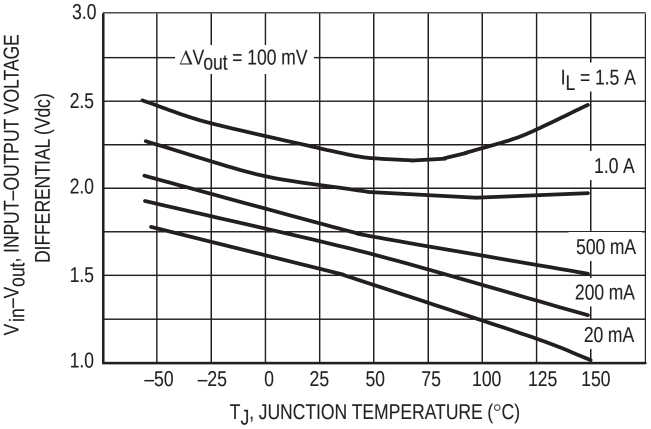


Figure 9. Temperature Stability

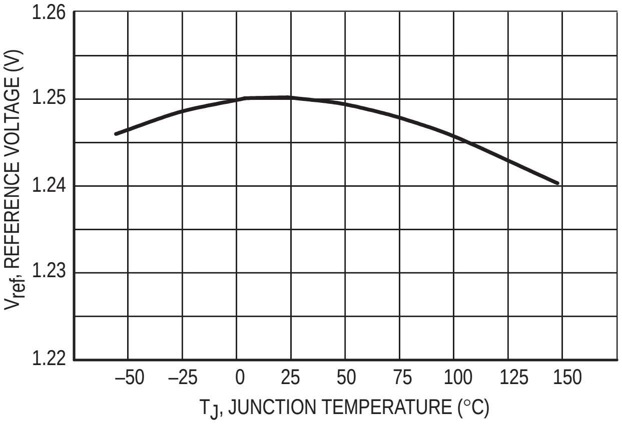


Figure 10. Minimum Operating Current

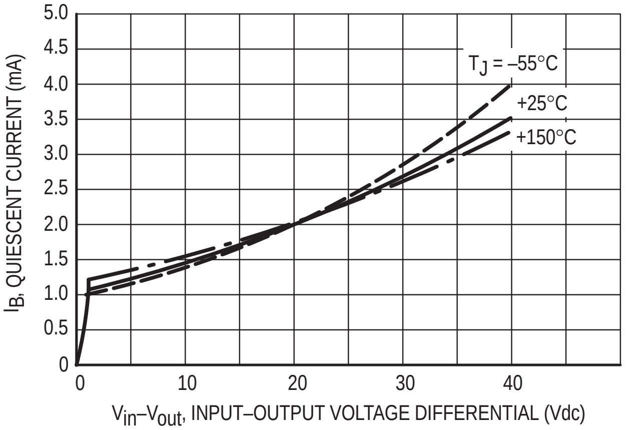


Figure 11. Ripple Rejection versus Output Voltage

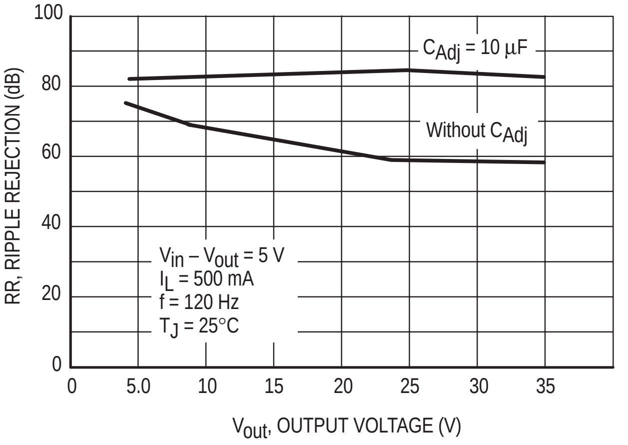


Figure 12. Ripple Rejection versus Output Current

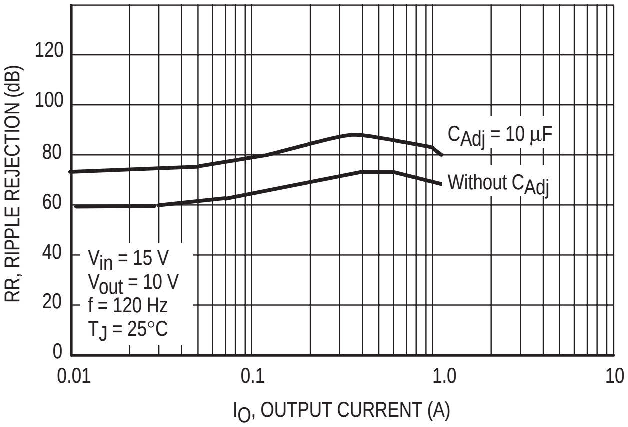


Figure 13. Ripple Rejection versus Frequency

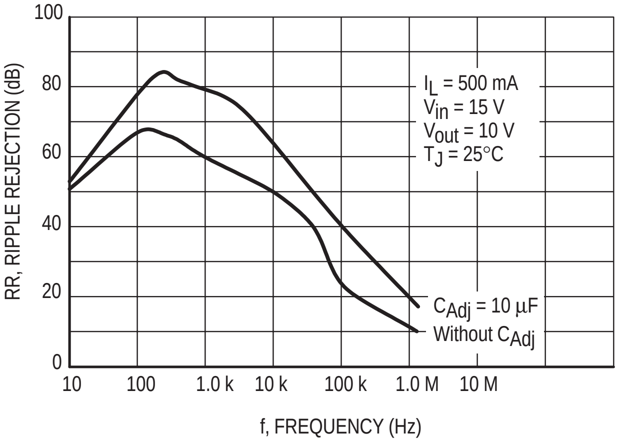


Figure 14. Output Impedance

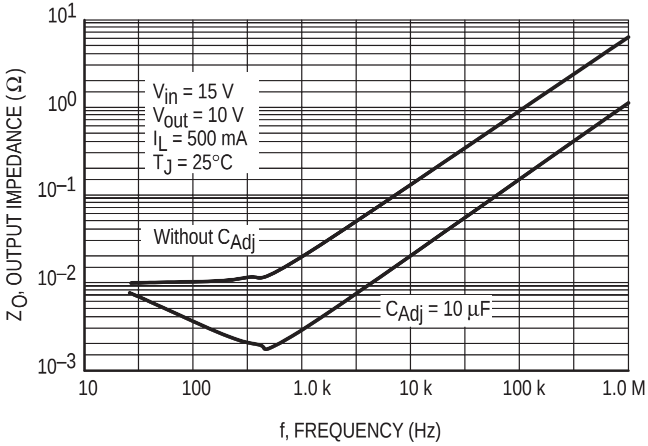


Figure 15. Line Transient Response

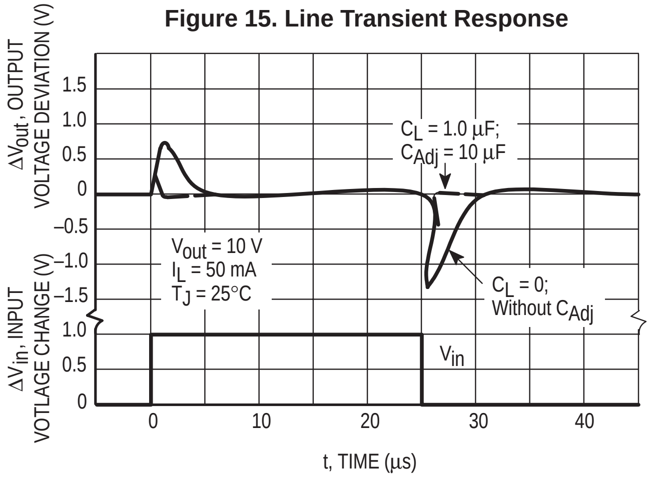
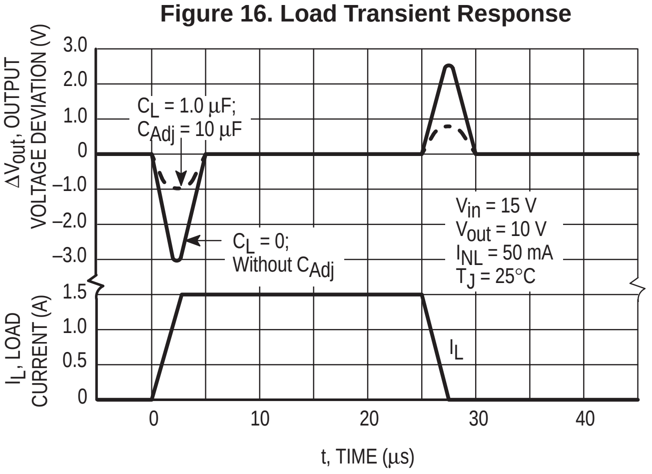


Figure 16. Load Transient Response



APPLICATIONS INFORMATION

Basic Circuit Operation

The LM317 is a 3–terminal floating regulator. In operation, the LM317 develops and maintains a nominal 1.25 V reference (V_{ref}) between its output and adjustment terminals. This reference voltage is converted to a programming current (I_{PROG}) by R_1 (see Figure 17), and this constant current flows through R_2 to ground.

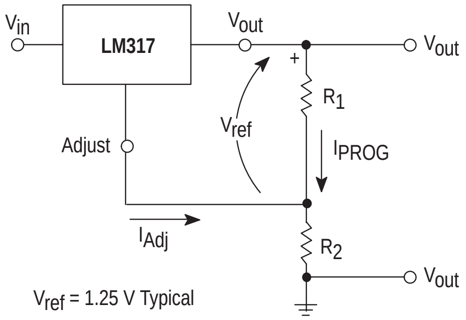
The regulated output voltage is given by:

$$V_{out} = V_{ref}\left(1 + \frac{R_2}{R_1}\right) + I_{Adj} R_2$$

Since the current from the adjustment terminal (I_{Adj}) represents an error term in the equation, the LM317 was designed to control I_{Adj} to less than 100 µA and keep it constant. To do this, all quiescent operating current is returned to the output terminal. This imposes the requirement for a minimum load current. If the load current is less than this minimum, the output voltage will rise.

Since the LM317 is a floating regulator, it is only the voltage differential across the circuit which is important to performance, and operation at high voltages with respect to ground is possible.

Figure 17. Basic Circuit Configuration



Load Regulation

The LM317 is capable of providing extremely good load regulation, but a few precautions are needed to obtain maximum performance. For best performance, the programming resistor (R_1) should be connected as close to the regulator as possible to minimize line drops which effectively appear in series with the reference, thereby degrading regulation. The ground end of R_2 can be returned near the load ground to provide remote ground sensing and improve load regulation.

External Capacitors

A 0.1 µF disc or 1.0 µF tantalum input bypass capacitor (C_{in}) is recommended to reduce the sensitivity to input line impedance.

The adjustment terminal may be bypassed to ground to improve ripple rejection. This capacitor (C_{Adj}) prevents ripple from being amplified as the output voltage is increased. A 10 µF capacitor should improve ripple rejection about 15 dB at 120 Hz in a 10 V application.

Although the LM317 is stable with no output capacitance, like any feedback circuit, certain values of external capacitance can cause excessive ringing. An output capacitance (C_O) in the form of a 1.0 µF tantalum or 25 µF aluminum electrolytic capacitor on the output swamps this effect and insures stability.

Protection Diodes

When external capacitors are used with any IC regulator it is sometimes necessary to add protection diodes to prevent the capacitors from discharging through low current points into the regulator.

Figure 18 shows the LM317 with the recommended protection diodes for output voltages in excess of 25 V or high capacitance values (C_O > 25 µF, C_{Adj} > 10 µF). Diode D_1 prevents C_O from discharging thru the IC during an input short circuit. Diode D_2 protects against capacitor C_{Adj} discharging through the IC during an output short circuit. The combination of diodes D_1 and D_2 prevents C_{Adj} from discharging through the IC during an input short circuit.

Figure 18. Voltage Regulator with Protection Diodes

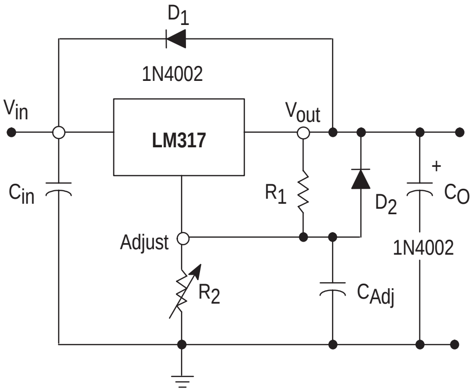


Figure 19. D²PAK Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length

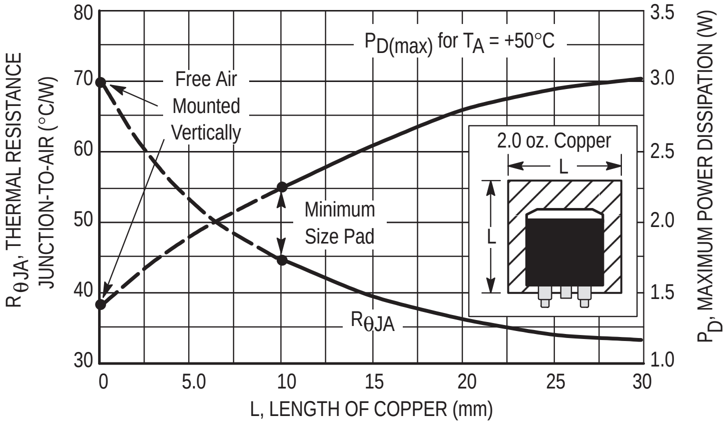
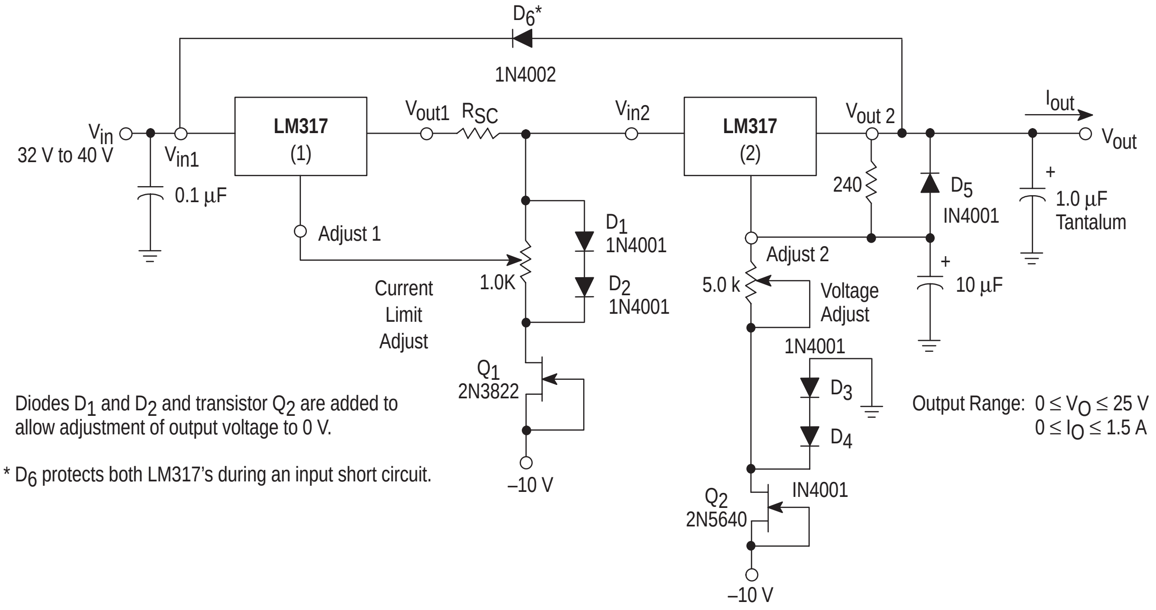


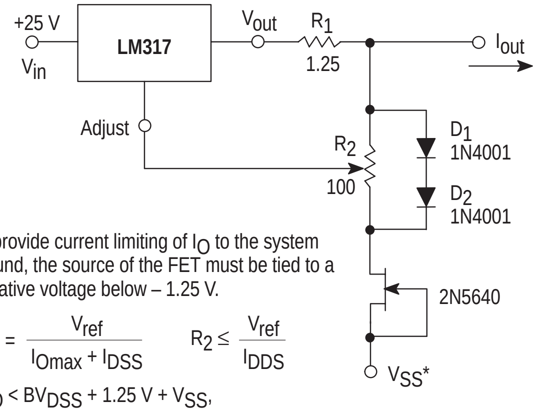
Figure 20. “Laboratory” Power Supply with Adjustable Current Limit and Output Voltage



Diodes D_1 and D_2 and transistor Q_2 are added to allow adjustment of output voltage to 0 V.

* D_6 protects both LM317’s during an input short circuit.

Figure 21. Adjustable Current Limiter

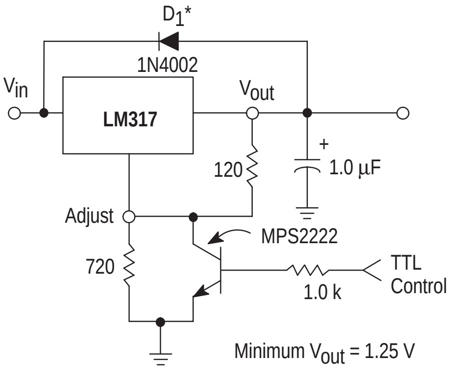


* To provide current limiting of I_O to the system ground, the source of the FET must be tied to a negative voltage below – 1.25 V.

$R_1 = \frac{V_{ref}}{I_{Omax} + I_{DSS}}$ $R_2 \le \frac{V_{ref}}{I_{DDS}}$

$V_O < BV_{DSS} + 1.25\ V + V_{SS}$,
$I_{Lmin} - I_{DSS} < I_O < 1.5$ A.
As shown $0 < I_O < 1.0$ A.

Figure 22. 5.0 V Electronic Shutdown Regulator



* D_1 protects the device during an input short circuit.

Figure 23. Slow Turn–On Regulator

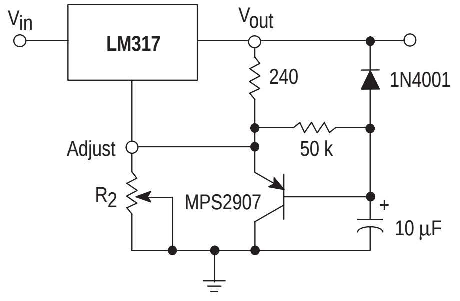
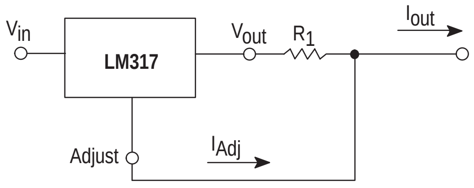


Figure 24. Current Regulator



$$I_{out} = \left(\frac{V_{ref}}{R_1}\right) + I_{Adj}$$

$$= \frac{1.25\ V}{R_1}$$

$10\ mA \le I_{out} \le 1.5$ A

MOTOROLA

LM317L

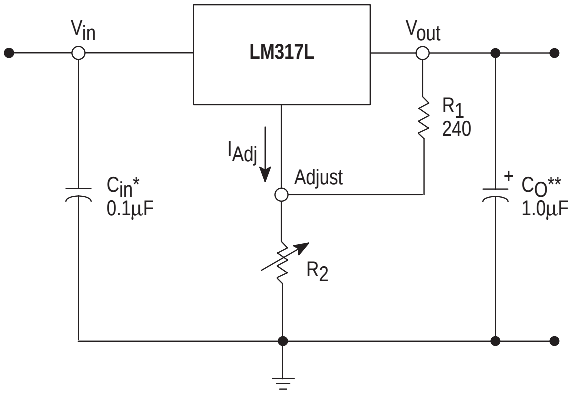
Three-Terminal Adjustable Output Positive Voltage Regulator

The LM317L is an adjustable 3–terminal positive voltage regulator capable of supplying in excess of 100 mA over an output voltage range of 1.2 V to 37 V. This voltage regulator is exceptionally easy to use and requires only two external resistors to set the output voltage. Further, it employs internal current limiting, thermal shutdown and safe area compensation, making them essentially blow–out proof.

The LM317L serves a wide variety of applications including local, on card regulation. This device can also be used to make a programmable output regulator, or by connecting a fixed resistor between the adjustment and output, the LM317L can be used as a precision current regulator.

- Output Current in Excess of 100 mA
- Output Adjustable Between 1.2 V and 37 V
- Internal Thermal Overload Protection
- Internal Short Circuit Current Limiting
- Output Transistor Safe–Area Compensation
- Floating Operation for High Voltage Applications
- Standard 3–Lead Transistor Package
- Eliminates Stocking Many Fixed Voltages

Simplified Application



* C_{in} is required if regulator is located an appreciable distance from power supply filter.

** C_O is not needed for stability, however, it does improve transient response.

$$V_{out} = 1.25\ V\left(1 + \frac{R_2}{R_1}\right) + I_{Adj}\,R_2$$

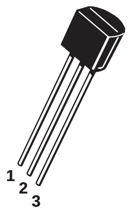
Since I_{Adj} is controlled to less than 100 µA, the error associated with this term is negligible in most applications.

LOW CURRENT THREE–TERMINAL ADJUSTABLE POSITIVE VOLTAGE REGULATOR

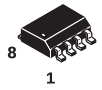
SEMICONDUCTOR TECHNICAL DATA

Z SUFFIX
PLASTIC PACKAGE
CASE 29

Pin 1. Adjust
2. V_{out}
3. V_{in}



D SUFFIX
PLASTIC PACKAGE
CASE 751
(SOP–8*)



Pin 1. V_{in}
2. V_{out}
3. V_{out}
4. Adjust
5. N.C.
6. V_{out}
7. V_{out}
8. N.C.

* SOP–8 is an internally modified SO–8 package. Pins 2, 3, 6 and 7 are electrically common to the die attach flag. This internal lead frame modification decreases package thermal resistance and increases power dissipation capability when appropriately mounted on a printed circuit board. SOP–8 conforms to all external dimensions of the standard SO–8 package.

ORDERING INFORMATION

Device	Operating Temperature Range	Package
LM317LD	T_J = 0° to +125°C	SOP–8
LM317LZ		Plastic
LM317LBD	T_J = –40° to +125°C	SOP–8
LM317LBZ		Plastic

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input–Output Voltage Differential	$V_I–V_O$	40	Vdc
Power Dissipation	P_D	Internally Limited	W
Operating Junction Temperature Range	T_J	–40 to +125	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

ELECTRICAL CHARACTERISTICS ($V_I–V_O$ = 5.0 V; I_O = 40 mA; $T_J = T_{low}$ to T_{high} [Note 1]; I_{max} and P_{max} [Note 2]; unless otherwise noted.)

			LM317L, LB			
Characteristics	Figure	Symbol	Min	Typ	Max	Unit
Line Regulation (Note 3) T_A = 25°C, 3.0 V ≤ $V_I – V_O$ ≤ 40 V	1	Reg_{line}	–	0.01	0.04	%/V
Load Regulation (Note 3), T_A = 25°C 10 mA ≤ I_O ≤ I_{max} – LM317L	2	Reg_{load}				
V_O ≤ 5.0 V			–	5.0	25	mV
V_O ≥ 5.0 V			–	0.1	0.5	% V_O
Adjustment Pin Current	3	I_{Adj}	–	50	100	µA
Adjustment Pin Current Change 2.5 V ≤ $V_I – V_O$ ≤ 40 V, $P_D ≤ P_{max}$ 10 mA ≤ I_O ≤ I_{max} – LM317L	1, 2	ΔI_{Adj}	–	0.2	5.0	µA
Reference Voltage 3.0 V ≤ $V_I – V_O$ ≤ 40 V, $P_D ≤ P_{max}$ 10 mA ≤ I_O ≤ I_{max} – LM317L	3	V_{ref}	1.20	1.25	1.30	V
Line Regulation (Note 3) 3.0 V ≤ $V_I – V_O$ ≤ 40 V	1	Reg_{line}	–	0.02	0.07	%/V
Load Regulation (Note 3) 10 mA ≤ I_O ≤ I_{max} – LM317L	2	Reg_{load}				
V_O ≤ 5.0 V			–	20	70	mV
V_O ≥ 5.0 V			–	0.3	1.5	% V_O
Temperature Stability ($T_{low} ≤ T_J ≤ T_{high}$)	3	T_S	–	0.7	–	% V_O
Minimum Load Current to Maintain Regulation ($V_I – V_O$ = 40 V)	3	I_{Lmin}	–	3.5	10	mA
Maximum Output Current	3	I_{max}				mA
$V_I – V_O$ ≤ 6.25 V, $P_D ≤ P_{max}$, Z Package			100	200	–	
$V_I – V_O$ ≤ 40 V, $P_D ≤ P_{max}$, T_A = 25°C, Z Package			–	20	–	
RMS Noise, % of V_O T_A = 25°C, 10 Hz ≤ f ≤ 10 kHz		N	–	0.003	–	% V_O
Ripple Rejection (Note 4)	4	RR				dB
V_O = 1.2 V, f = 120 Hz			60	80	–	
C_{Adj} = 10 µF, V_O = 10.0 V			–	80	–	
Long Term Stability, $T_J = T_{high}$ (Note 5) T_A = 25°C for Endpoint Measurements	3	S	–	0.3	1.0	%/1.0 k Hrs.
Thermal Resistance, Junction–to–Case Z Package		$R_{\theta JC}$	–	83	–	°C/W
Thermal Resistance, Junction–to–Air Z Package		$R_{\theta JA}$	–	160	–	°C/W

NOTES:
1. T_{low} to T_{high} = 0° to +125°C for LM317L –40° to +125°C for LM317LB
2. I_{max} = 100 mA P_{max} = 625 mW
3. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.
4. C_{Adj}, when used, is connected between the adjustment pin and ground.
5. Since Long–Term Stability cannot be measured on each device before shipment, this specification is an engineering estimate of average stability from lot to lot.

Representative Schematic Diagram

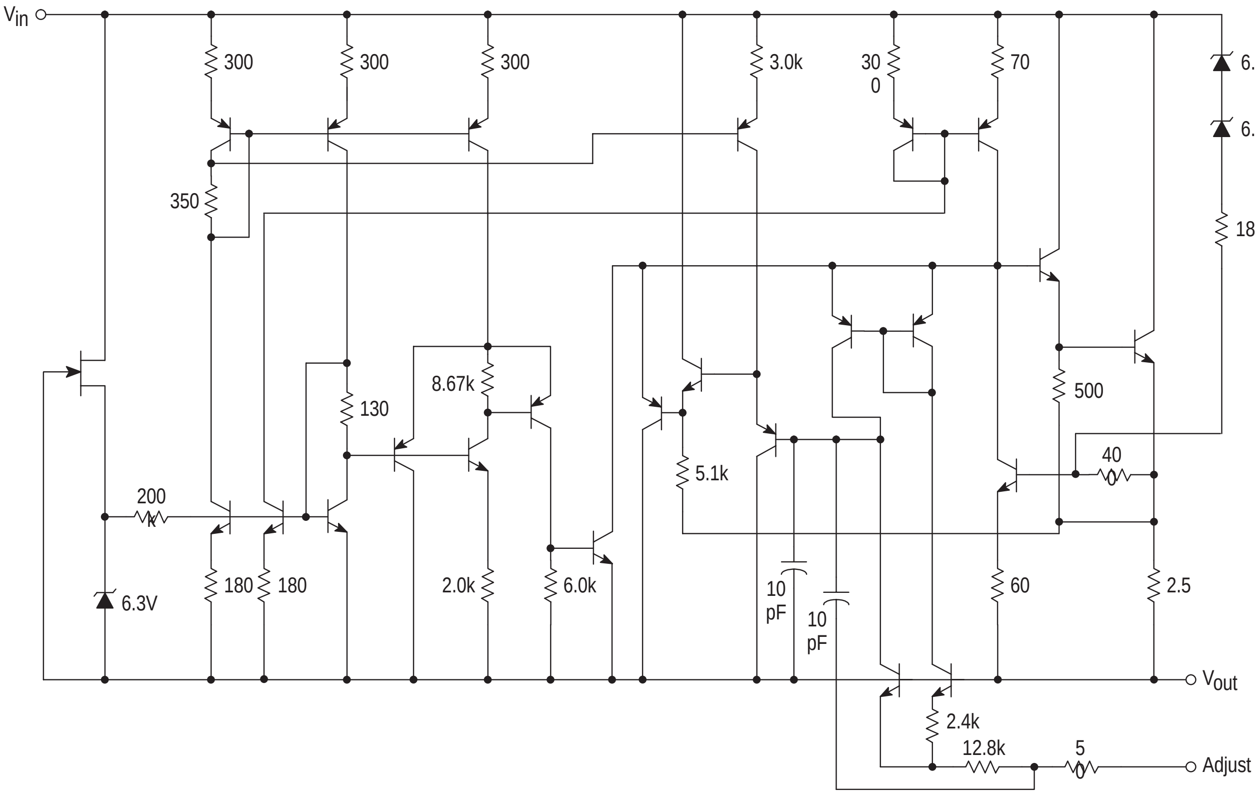
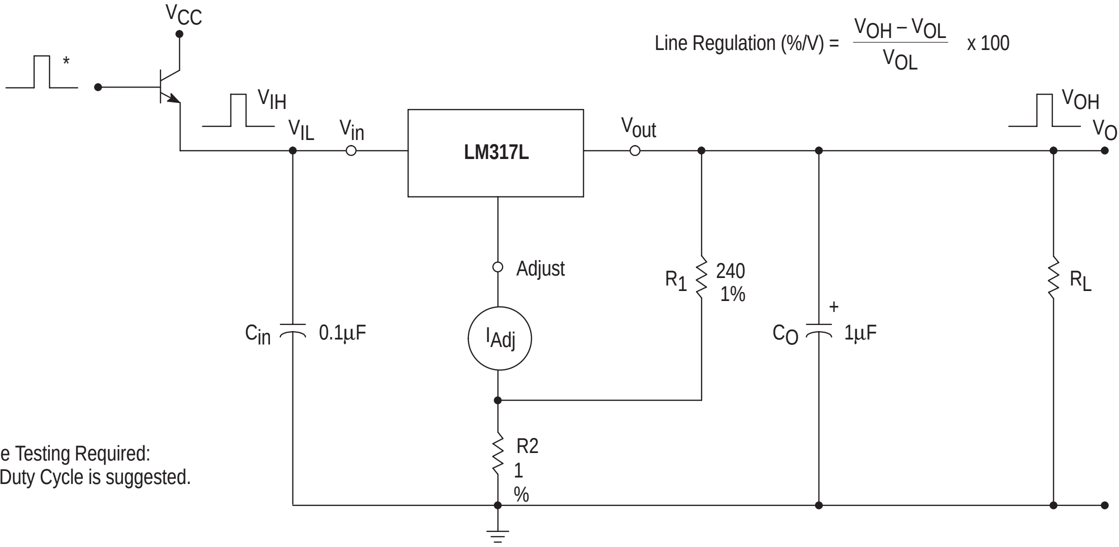


Figure 1. Line Regulation and ΔI_{Adj}/Line Test Circuit



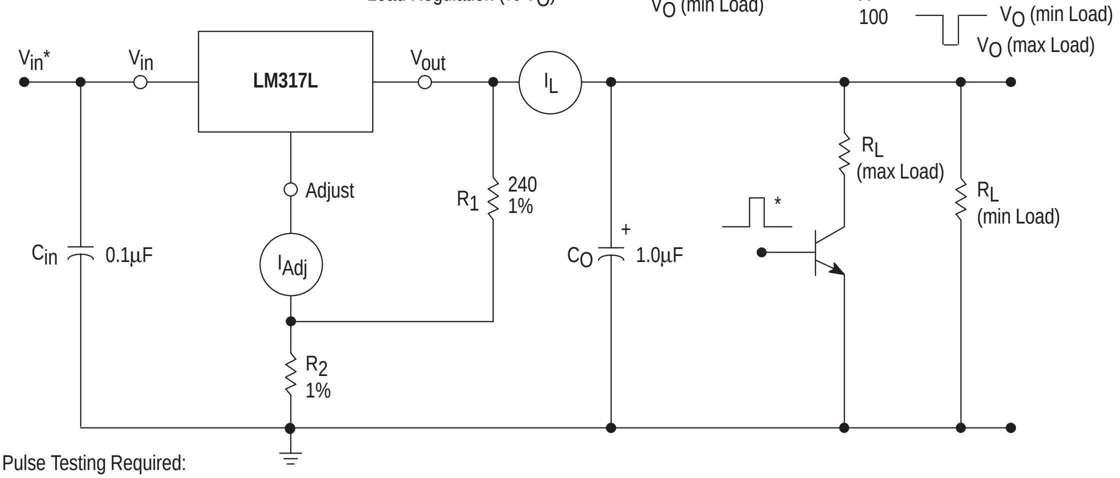
$$\text{Line Regulation (\%/V)} = \frac{V_{OH} - V_{OL}}{V_{OL}} \times 100$$

* Pulse Testing Required:
1% Duty Cycle is suggested.

Figure 2. Load Regulation and ΔI_{Adj}/Load Test Circuit

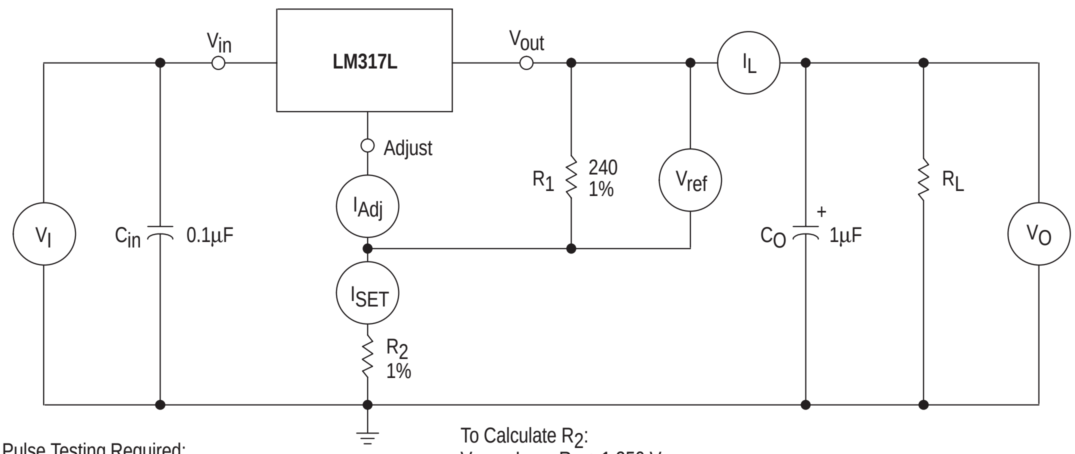
Load Regulation (mV) = V_O (min Load) $-V_O$ (max Load)

Load Regulation (% V_O) = $\frac{V_O \text{ (min Load)} - V_O \text{ (max Load)}}{V_O \text{ (min Load)}}$ X 100



* Pulse Testing Required:
1% Duty Cycle is suggested.

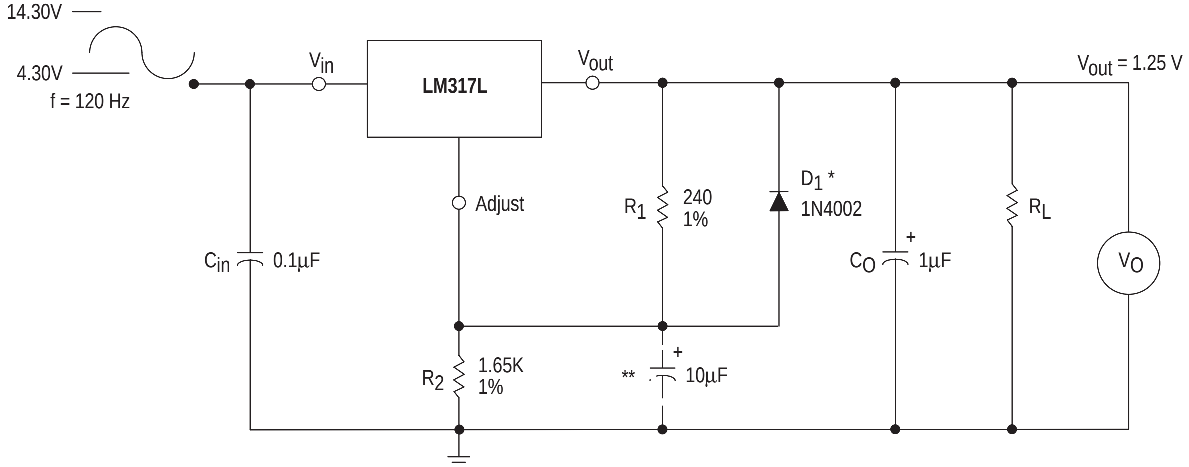
Figure 3. Standard Test Circuit



Pulse Testing Required:
1% Duty Cycle is suggested.

To Calculate R_2:
$V_{out} = I_{SET} R_2 + 1.250$ V
Assume I_{SET} = 5.25 mA

Figure 4. Ripple Rejection Test Circuit



* D_1 Discharges C_{Adj} if Output is Shorted to Ground.

**C_{Adj} provides an AC ground to the adjust pin.

Figure 5. Load Regulation

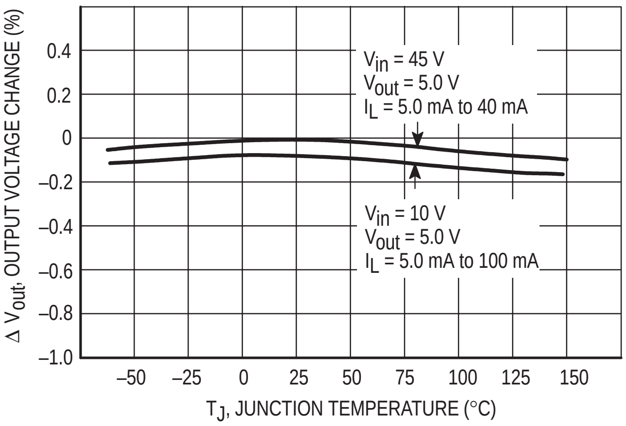


Figure 6. Ripple Rejection

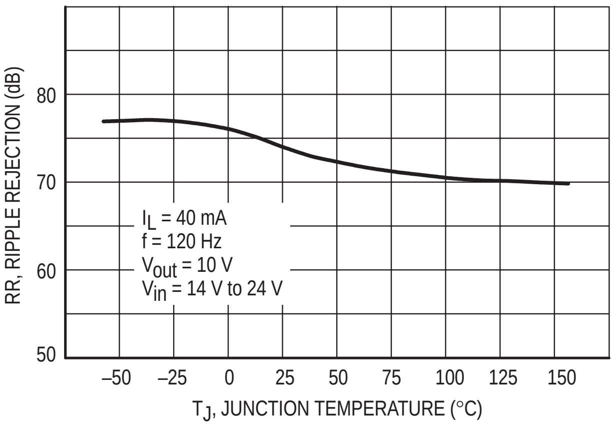


Figure 7. Current Limit

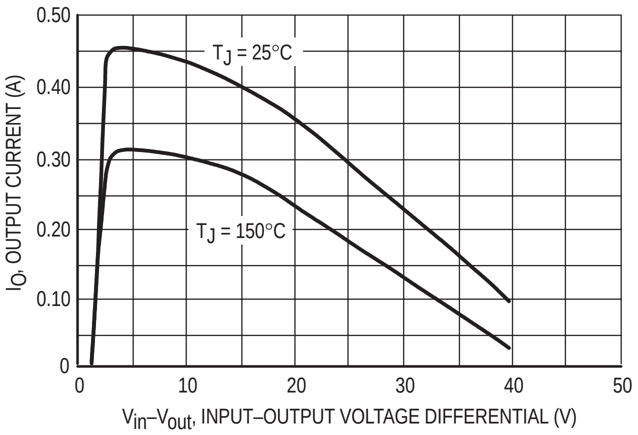


Figure 8. Dropout Voltage

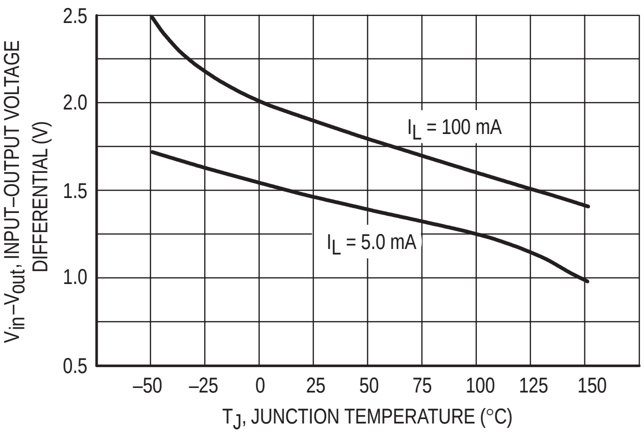


Figure 9. Minimum Operating Current

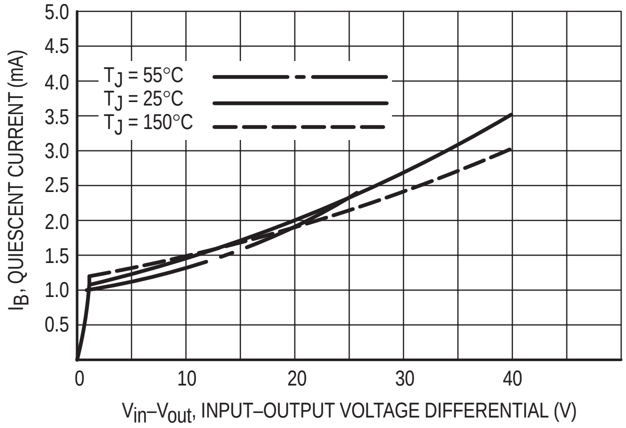


Figure 10. Ripple Rejection versus Frequency

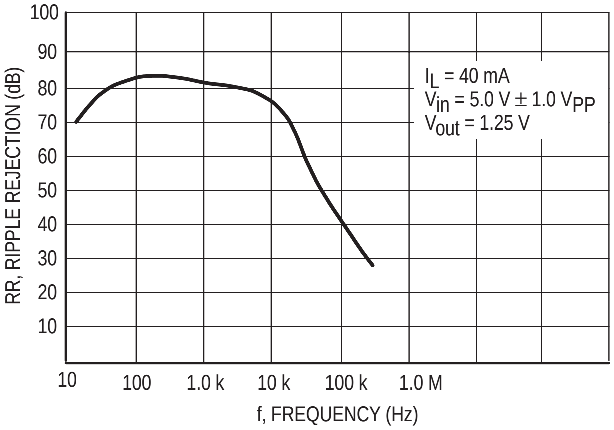


Figure 11. Temperature Stability

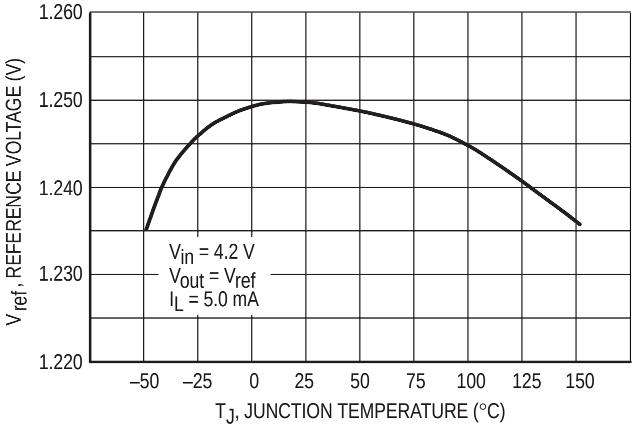


Figure 12. Adjustment Pin Current

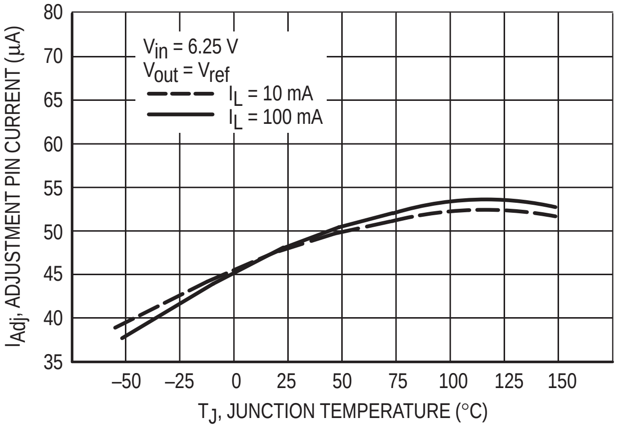


Figure 13. Line Regulation

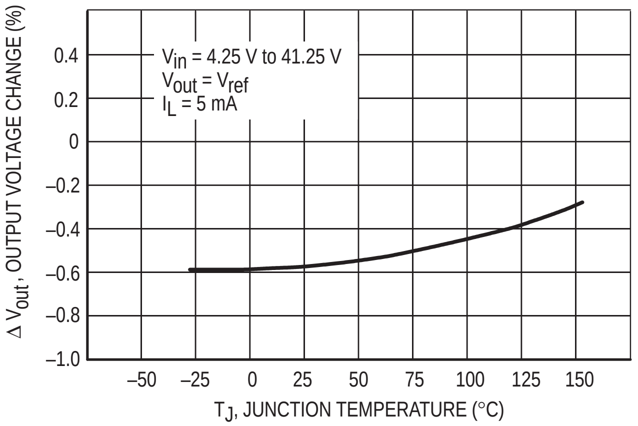


Figure 14. Output Noise

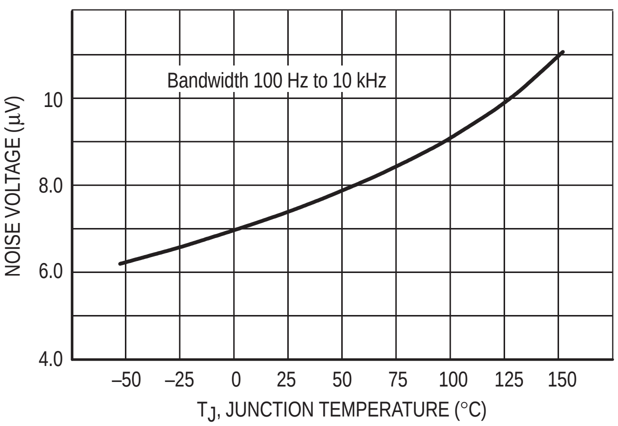


Figure 15. Line Transient Response

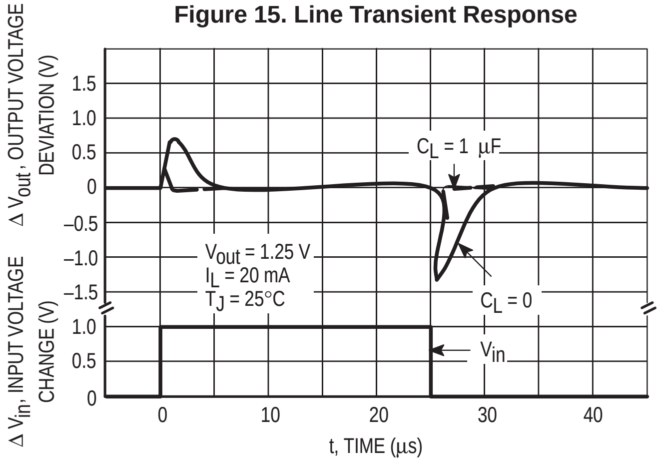
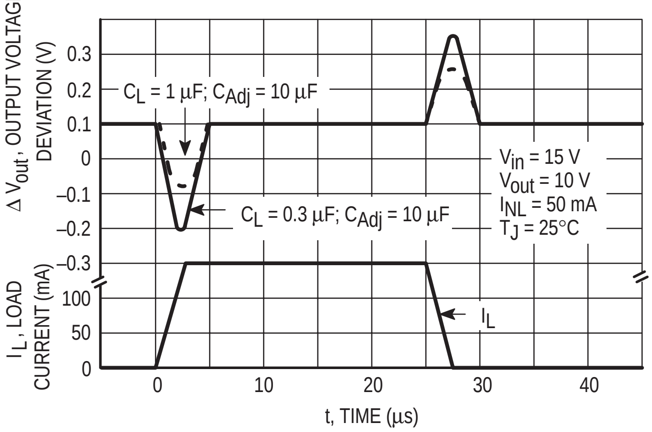


Figure 16. Load Transient Response



APPLICATIONS INFORMATION

Basic Circuit Operation

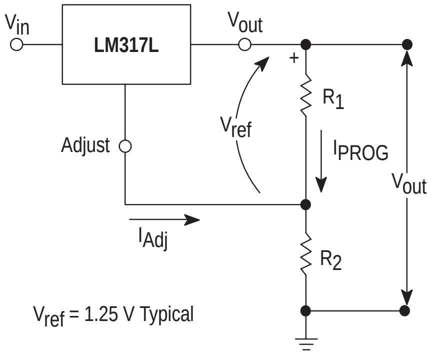
The LM317L is a 3–terminal floating regulator. In operation, the LM317L develops and maintains a nominal 1.25 V reference (V_{ref}) between its output and adjustment terminals. This reference voltage is converted to a programming current (I_{PROG}) by R_1 (see Figure 13), and this constant current flows through R_2 to ground. The regulated output voltage is given by:

$$V_{out} = V_{ref} \left(1 + \frac{R_2}{R_1}\right) + I_{Adj} R_2$$

Since the current from the adjustment terminal (I_{Adj}) represents an error term in the equation, the LM317L was designed to control I_{Adj} to less than 100 µA and keep it constant. To do this, all quiescent operating current is returned to the output terminal. This imposes the requirement for a minimum load current. If the load current is less than this minimum, the output voltage will rise.

Since the LM317L is a floating regulator, it is only the voltage differential across the circuit which is important to performance, and operation at high voltages with respect to ground is possible.

Figure 17. Basic Circuit Configuration



Load Regulation

The LM317L is capable of providing extremely good load regulation, but a few precautions are needed to obtain maximum performance. For best performance, the programming resistor (R1) should be connected as close to the regulator as possible to minimize line drops which effectively appear in series with the reference, thereby degrading regulation. The ground end of R2 can be returned near the load ground to provide remote ground sensing and improve load regulation.

External Capacitors

A 0.1 µF disc or 1.0 µF tantalum input bypass capacitor (C_{in}) is recommended to reduce the sensitivity to input line impedance.

The adjustment terminal may be bypassed to ground to improve ripple rejection. This capacitor (C_{Adj}) prevents ripple from being amplified as the output voltage is increased. A 10 µF capacitor should improve ripple rejection about 15 dB at 120 Hz in a 10 V application.

Although the LM317L is stable with no output capacitance, like any feedback circuit, certain values of external capacitance can cause excessive ringing. An output capacitance (C_O) in the form of a 1.0 µF tantalum or 25 µF aluminum electrolytic capacitor on the output swamps this effect and insures stability.

Protection Diodes

When external capacitors are used with any IC regulator it is sometimes necessary to add protection diodes to prevent the capacitors from discharging through low current points into the regulator.

Figure 14 shows the LM317L with the recommended protection diodes for output voltages in excess of 25 V or high capacitance values (C_O > 10 µF, C_{Adj} > 5.0 µF). Diode D_1 prevents C_O from discharging thru the IC during an input short circuit. Diode D_2 protects against capacitor C_{Adj} discharging through the IC during an output short circuit. The combination of diodes D_1 and D_2 prevents C_{Adj} from discharging through the IC during an input short circuit.

Figure 18. Voltage Regulator with Protection Diodes

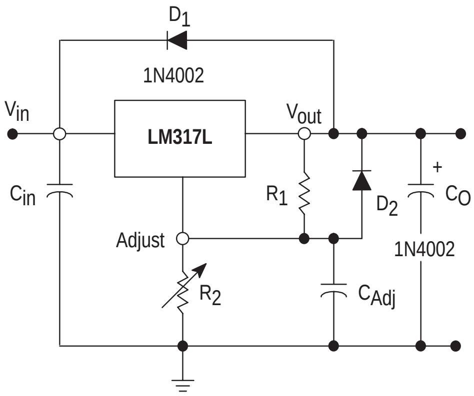
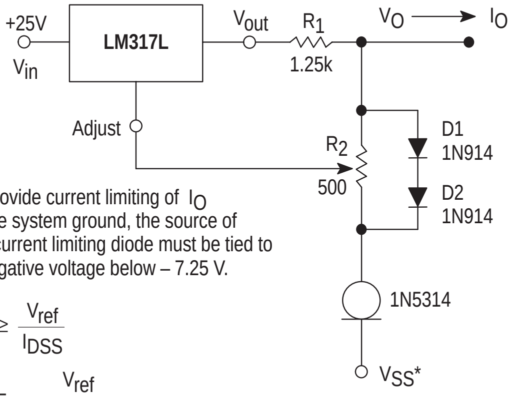


Figure 19. Adjustable Current Limiter



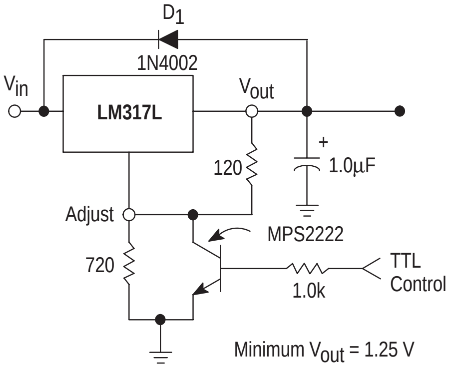
* To provide current limiting of I_O to the system ground, the source of the current limiting diode must be tied to a negative voltage below – 7.25 V.

$$R_2 \geq \frac{V_{ref}}{I_{DSS}}$$

$$R_1 = \frac{V_{ref}}{I_{Omax} + I_{DSS}}$$

$V_O < P_{OV} + 1.25\ V + V_{SS}$
$I_{Lmin} – I_P < I_O < 100\ mA – I_P$
As shown $O < I_O < 95\ mA$

Figure 20. 5 V Electronic Shutdown Regulator



Minimum $V_{out} = 1.25\ V$

D_1 protects the device during an input short circuit.

Figure 21. Slow Turn–On Regulator

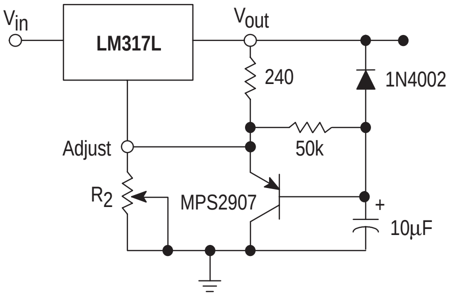
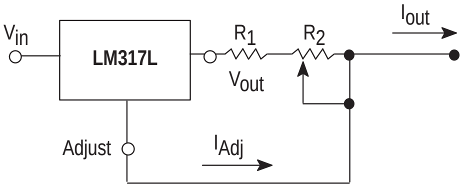


Figure 22. Current Regulator



$$I_{outmax} = \left(\frac{V_{ref}}{R_1}\right) + I_{Adj} \cong \frac{1.25\ V}{R_1}$$

$$I_{outmax} = \left(\frac{V_{ref}}{R_1 + R_2}\right) + I_{Adj} \cong \frac{1.25\ V}{R_1 + R_2}$$

$5.0\ mA < I_{out} < 100\ mA$

MOTOROLA

LM317M

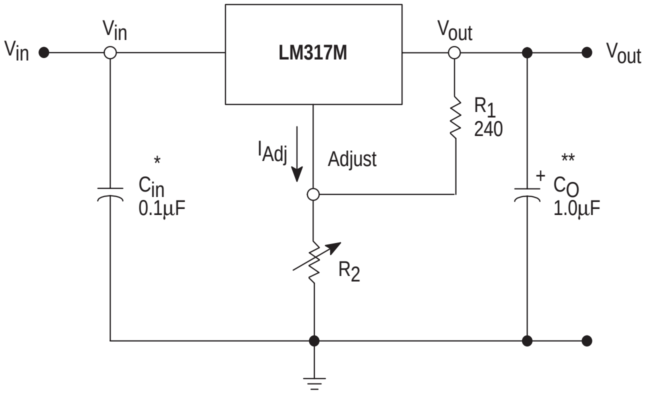
Three-Terminal Adjustable Output Positive Voltage Regulator

The LM317M is an adjustable three–terminal positive voltage regulator capable of supplying in excess of 500 mA over an output voltage range of 1.2 V to 37 V. This voltage regulator is exceptionally easy to use and requires only two external resistors to set the output voltage. Further, it employs internal current limiting, thermal shutdown and safe area compensation, making it essentially blow–out proof.

The LM317M serves a wide variety of applications including local, on–card regulation. This device also makes an especially simple adjustable switching regulator, a programmable output regulator, or by connecting a fixed resistor between the adjustment and output, the LM317M can be used as a precision current regulator.

- Output Current in Excess of 500 mA
- Output Adjustable between 1.2 V and 37 V
- Internal Thermal Overload Protection
- Internal Short Circuit Current Limiting
- Output Transistor Safe–Area Compensation
- Floating Operation for High Voltage Applications
- Eliminates Stocking Many Fixed Voltages

Simplified Application



* = C_{in} is required if regulator is located an appreciable distance from power supply filter.
** = C_O is not needed for stability, however, it does improve transient response.

$$V_{out} = 1.25\ \text{V}\left(1 + \frac{R_2}{R_1}\right) + I_{Adj}\,R_2$$

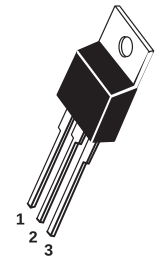
Since I_{Adj} is controlled to less than 100 µA, the error associated with this term is negligible in most applications.

MEDIUM CURRENT THREE–TERMINAL ADJUSTABLE POSITIVE VOLTAGE REGULATOR

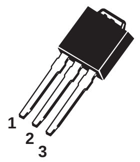
SEMICONDUCTOR TECHNICAL DATA

T SUFFIX
PLASTIC PACKAGE
CASE 221A

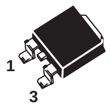
Heatsink surface
connected to Pin 2



(All 3 Packages)
Pin 1. Adjust
2. V_{out}
3. V_{in}



DT–1 SUFFIX
PLASTIC PACKAGE
CASE 369
(DPAK)



DT SUFFIX
PLASTIC PACKAGE
CASE 369A
(DPAK)

Heatsink Surface (shown as terminal 4 in case outline drawing) is connected to Pin 2.

ORDERING INFORMATION

Device	Operating Temperature Range	Package
LM317MT	T_J = 0° to +125°C	Plastic Power
LM317MBT#	T_J = –40° to +125°C	Plastic Power
LM317MDT LM317MDT–1	T_J = 0° to 125°C	DPAK

\# Automotive temperature range selections are available with special test conditions and additional tests. Contact your local Motorola sales office for information.

MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted.)

Rating	Symbol	Value	Unit
Input–Output Voltage Differential	$V_I–V_O$	40	Vdc
Power Dissipation (Package Limitation) (Note 1)			
Plastic Package, T Suffix			
T_A = 25°C	P_D	Internally Limited	
Thermal Resistance, Junction–to–Air	θ_{JA}	70	°C/W
Thermal Resistance, Junction–to–Case	θ_{JC}	5.0	°C/W
Plastic Package, DT Suffix			
T_A = 25°C	P_D	Internally Limited	
Thermal Resistance, Junction–to–Air	θ_{JA}	92	°C/W
Thermal Resistance, Junction–to–Case	θ_{JC}	5.0	°C/W
Operating Junction Temperature Range	T_J	–40 to +125	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

NOTE: 1. Figure 23 provides thermal resistance versus pc board pad size.

ELECTRICAL CHARACTERISTICS ($V_I–V_O$ = 5.0 V; I_O = 0.1 A, $T_J = T_{low}$ to T_{high} [Note 1], unless otherwise noted.)

Characteristics	Figure	Symbol	Min	Typ	Max	Unit
Line Regulation (Note 2) T_A = 25°C, 3.0 V ≤ $V_I–V_O$ ≤ 40 V	1	Reg_{line}	–	0.01	0.04	%/V
Load Regulation (Note 2) T_A = 25°C, 10 mA ≤ I_O ≤ 0.5 A	2	Reg_{load}				
V_O ≤ 5.0 V			–	5.0	25	mV
V_O ≥ 5.0 V			–	0.1	0.5	% V_O
Adjustment Pin Current	3	I_{Adj}	–	50	100	µA
Adjustment Pin Current Change 2.5 V ≤ $V_I–V_O$ ≤ 40 V, 10 mA ≤ I_L ≤ 0.5 A, $P_D \le P_{max}$	1,2	ΔI_{Adj}	–	0.2	5.0	µA
Reference Voltage 3.0 V ≤ $V_I–V_O$ ≤ 40 V, 10 mA ≤ I_O ≤ 0.5 A, $P_D \le P_{max}$	3	V_{ref}	1.20	1.25	1.30	V
Line Regulation (Note 2) 3.0 V ≤ $V_I–V_O$ ≤ 40 V	1	Reg_{line}	–	0.02	0.07	%/V
Load Regulation (Note 2) 10 mA ≤ I_O ≤ 0.5 A	2	Reg_{load}				
V_O ≤ 5.0 V			–	20	70	mV
V_O ≥ 5.0 V			–	0.3	1.5	% V_O
Temperature Stability ($T_{low} \le T_J \le T_{high}$)	3	T_S	–	0.7	–	% V_O
Minimum Load Current to Maintain Regulation ($V_I–V_O$ = 40 V)	3	I_{Lmin}	–	3.5	10	mA
Maximum Output Current	3	I_{max}				A
$V_I–V_O$ ≤ 15 V, $P_D \le P_{max}$			0.5	0.9	–	
$V_I–V_O$ = 40 V, $P_D \le P_{max}$, T_A = 25°C			0.15	0.25	–	
RMS Noise, % of V_O T_A= 25°C, 10 Hz ≤ f ≤ 10 kHz	–	N	–	0.003	–	% V_O
Ripple Rejection, V_O = 10 V, f = 120 Hz (Note 3)	4	RR				dB
Without C_{Adj}			–	65	–	
C_{Adj} = 10 µF			66	80	–	
Long–Term Stability, $T_J = T_{high}$ (Note 4) T_A= 25°C for Endpoint Measurements	3	S	–	0.3	1.0	%/1.0 k Hrs.

NOTES: 1. T_{low} to T_{high} = 0° to +125°C; P_{max} = 7.5 W for LM317M T_{low} to T_{high} = –40° to +125°C; P_{max} = 7.5 W for LM317MB
2. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.
3. C_{Adj}, when used, is connected between the adjustment pin and ground.
4. Since Long–Term Stability cannot be measured on each device before shipment, this specification is an engineering estimate of average stability from lot to lot.

Representative Schematic Diagram

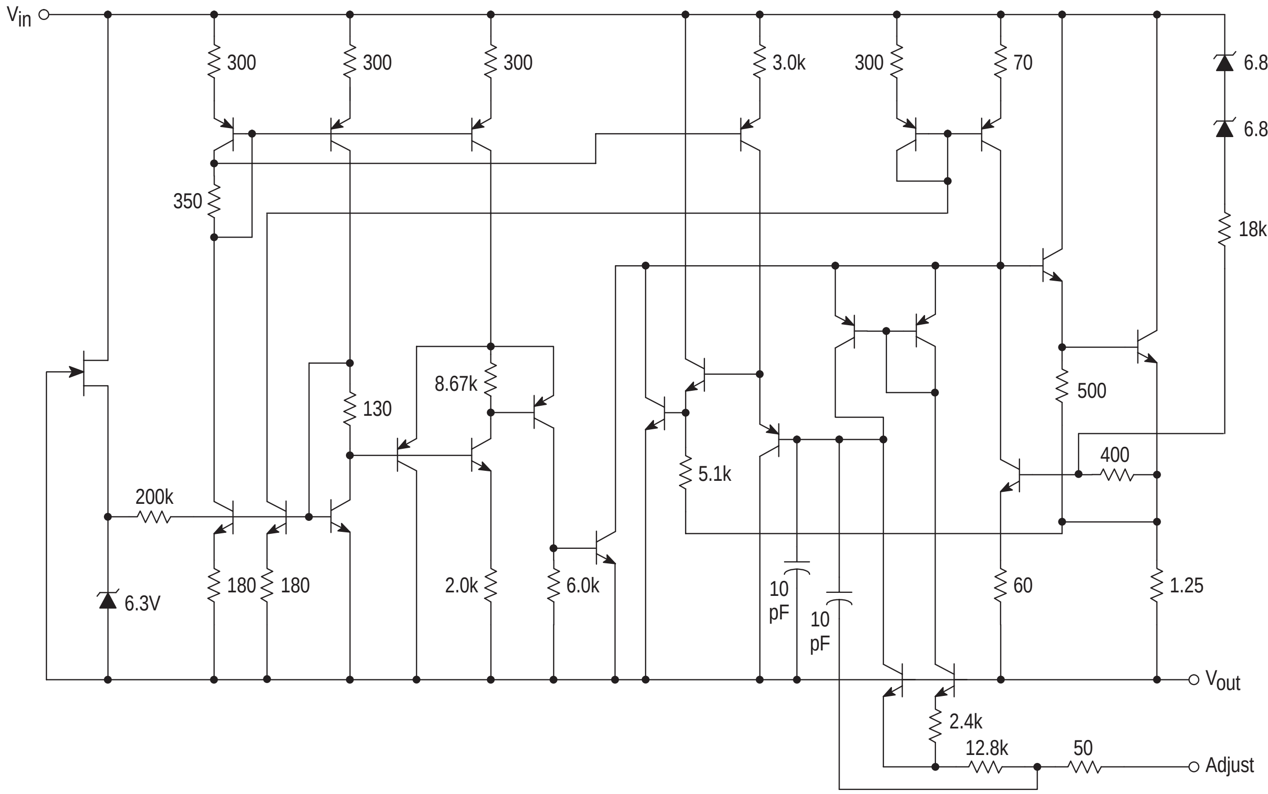
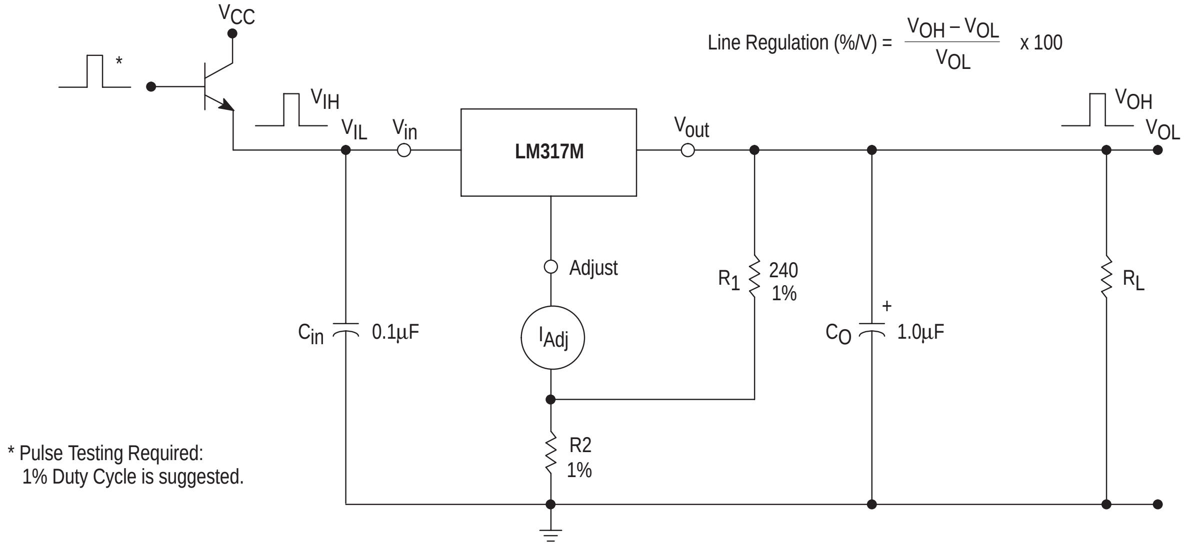


Figure 1. Line Regulation and ΔI_{Adj}/Line Test Circuit



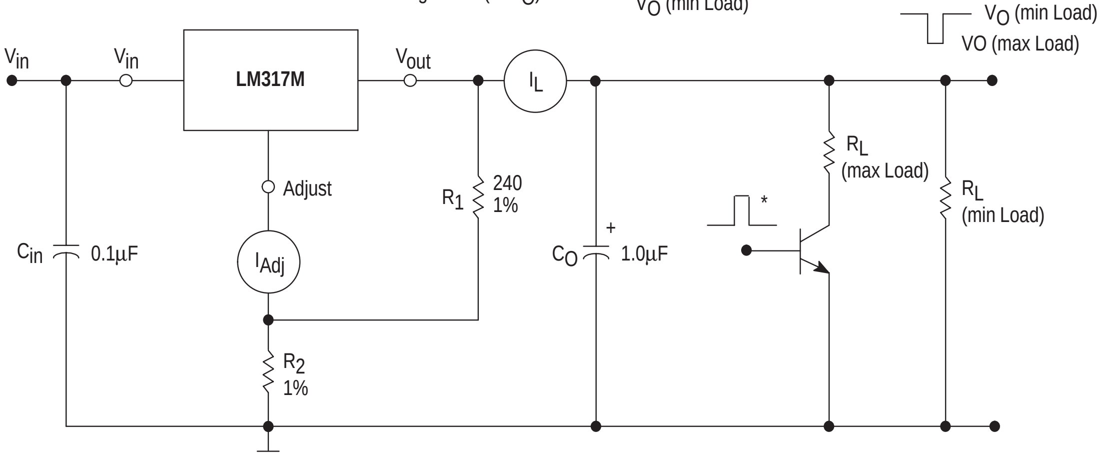
$$\text{Line Regulation (\%/V)} = \frac{V_{OH} - V_{OL}}{V_{OL}} \times 100$$

* Pulse Testing Required:
1% Duty Cycle is suggested.

Figure 2. Load Regulation and ΔI_{Adj}/Load Test Circuit

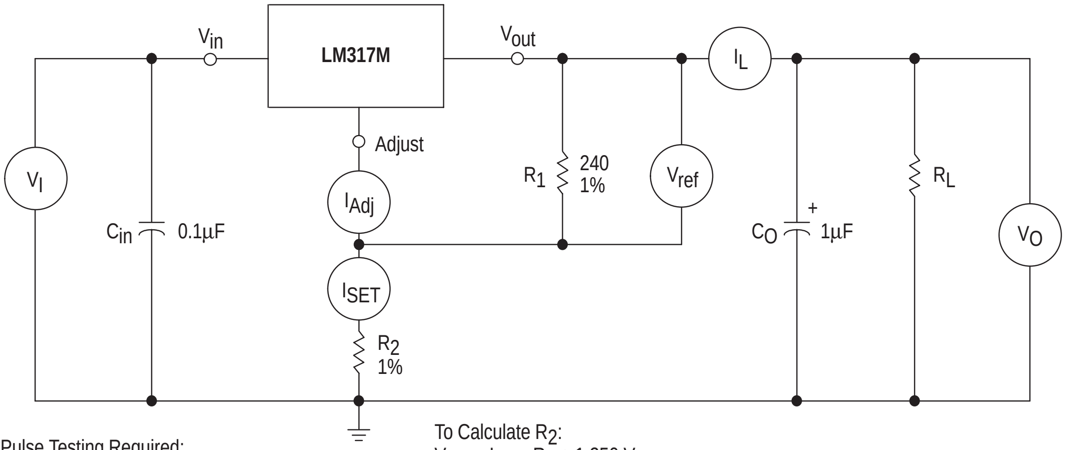
Load Regulation (mV) = V_O (min Load) $-V_O$ (max Load)

$$\text{Load Regulation } (\% V_O) = \frac{V_O \text{ (min Load)} - V_O \text{ (max Load)}}{V_O \text{ (min Load)}} \times 100$$



* Pulse Testing Required:
1% Duty Cycle is suggested.

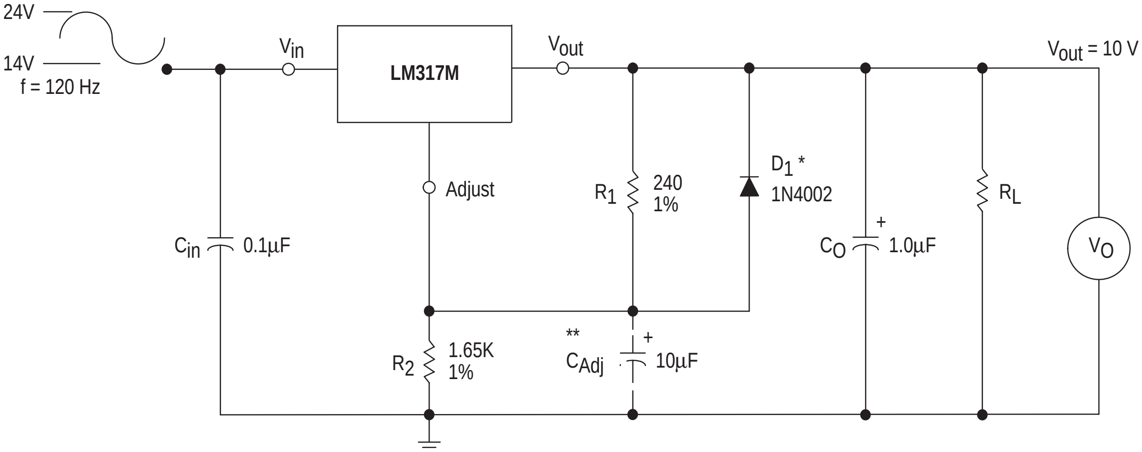
Figure 3. Standard Test Circuit



*Pulse Testing Required:
1% Duty Cycle is suggested.

To Calculate R_2:
$V_{out} = I_{SET} R_2 + 1.250$ V
Assume $I_{SET} = 5.25$ mA

Figure 4. Ripple Rejection Test Circuit



* D_1 Discharges C_{Adj} if Output is Shorted to Ground.
**C_{Adj} provides an AC ground to the adjust pin.

Figure 5. Load Regulation

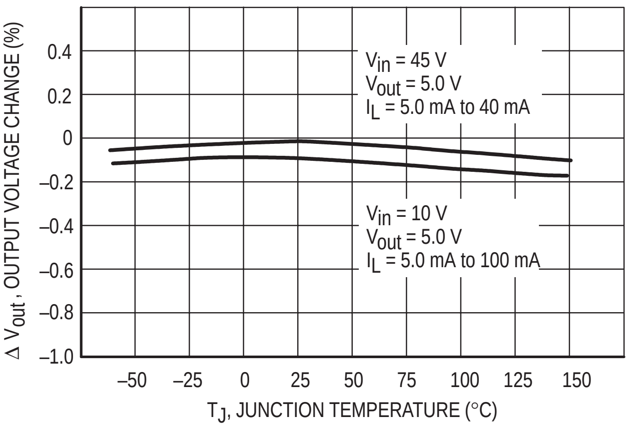


Figure 6. Ripple Rejection

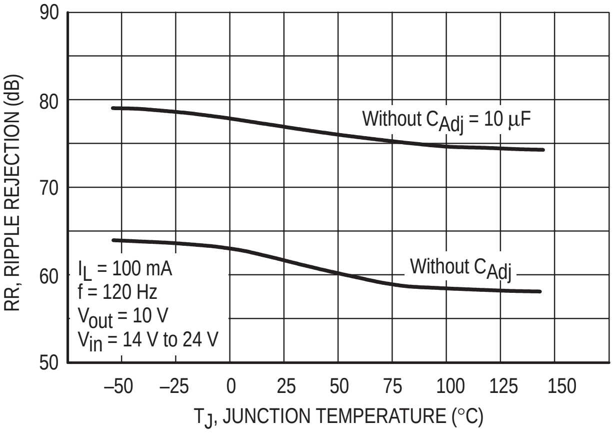


Figure 7. Current Limit

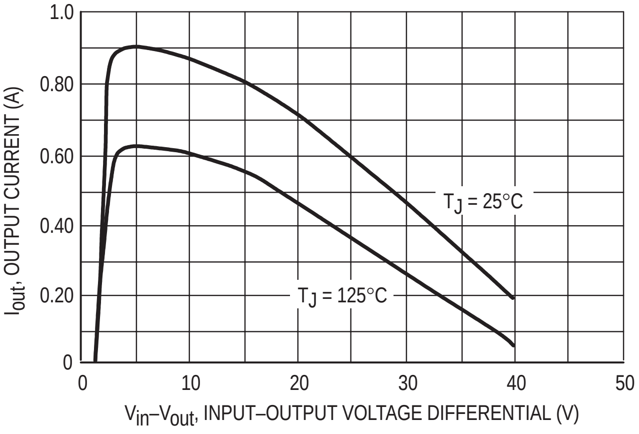


Figure 8. Dropout Voltage

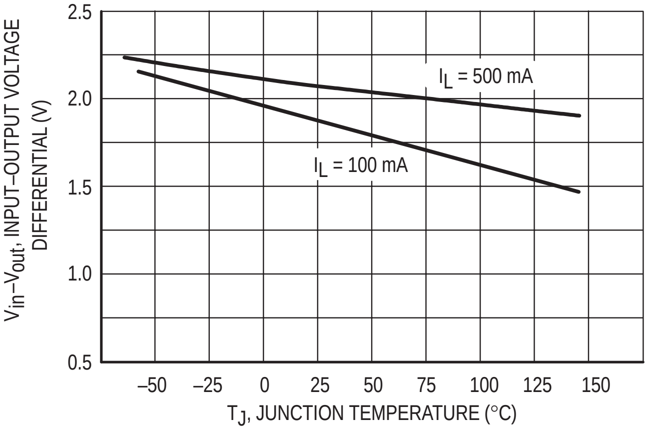


Figure 9. Minimum Operating Current

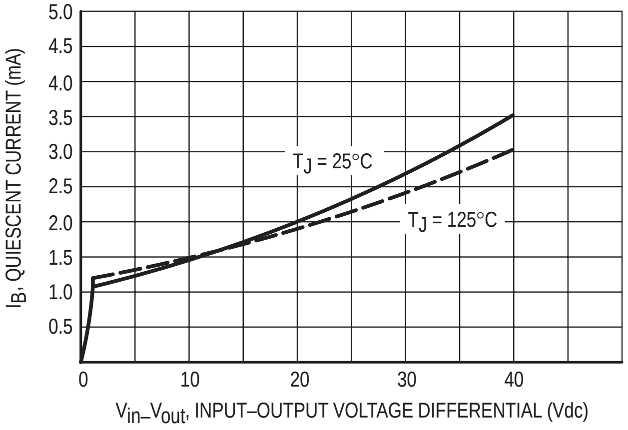


Figure 10. Ripple Rejection versus Frequency

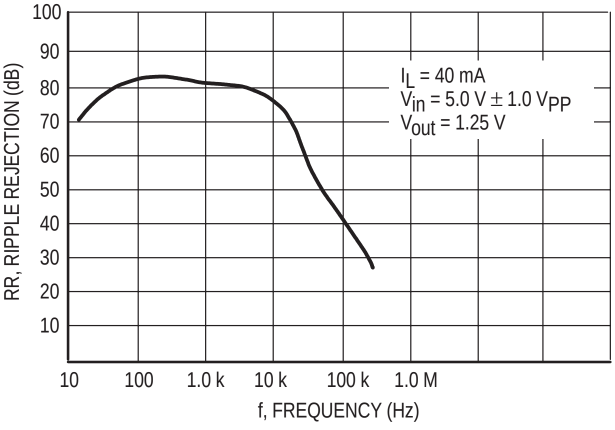


Figure 11. Temperature Stability

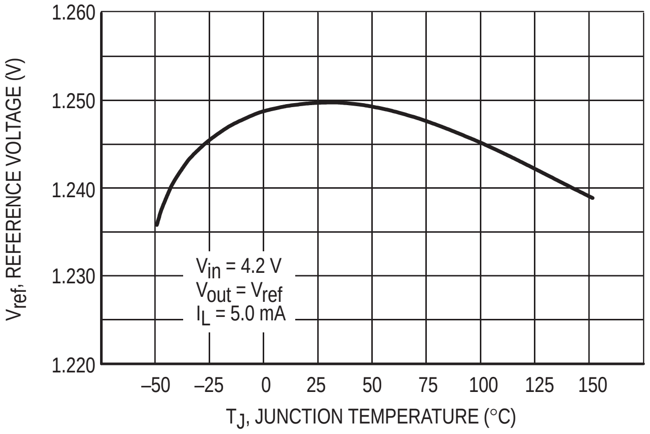


Figure 12. Adjustment Pin Current

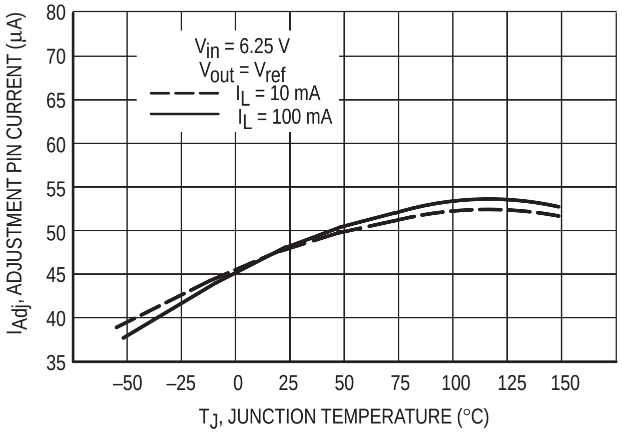


Figure 13. Line Regulation

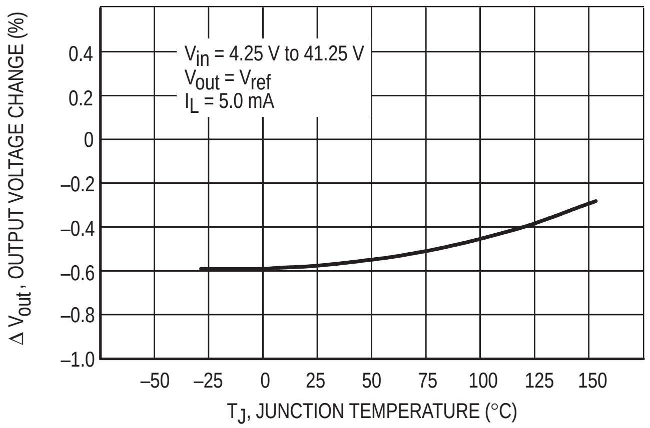


Figure 14. Output Noise

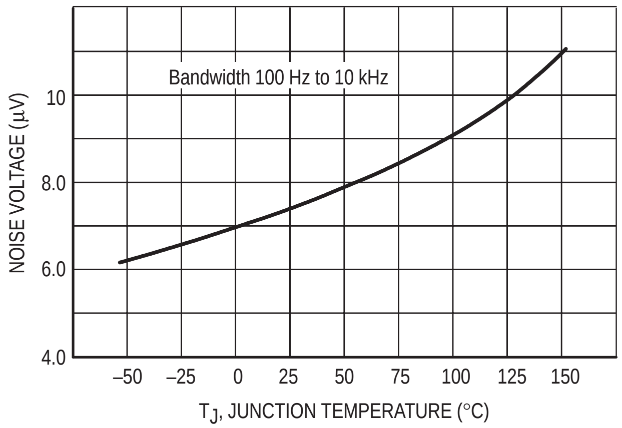


Figure 15. Line Transient Response

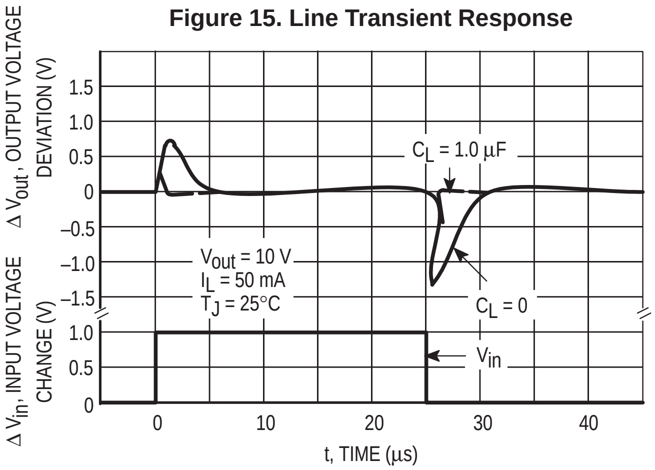
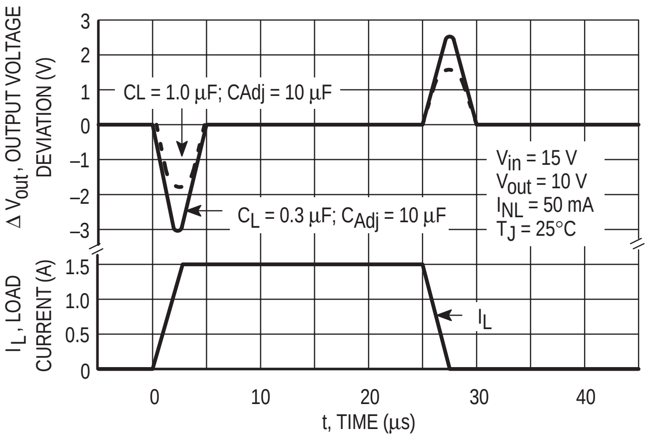


Figure 16. Load Transient Response



APPLICATIONS INFORMATION

Basic Circuit Operation

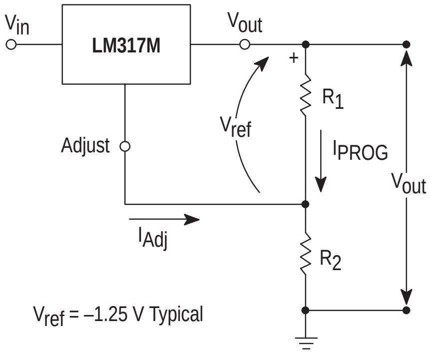
The LM317M is a three–terminal floating regulator. In operation, the LM317M develops and maintains a nominal 1.25 V reference (V_{ref}) between its output and adjustment terminals. This reference voltage is converted to a programming current (I_{PROG}) by R_1 (see Figure 17), and this constant current flows through R_2 to ground. The regulated output voltage is given by:

$$V_{out} = V_{ref}\left(1 + \frac{R_2}{R_1}\right) + I_{Adj}\,R_2$$

Since the current from the terminal (I_{Adj}) represents an error term in the equation, the LM317M was designed to control I_{Adj} to less than 100 μA and keep it constant. To do this, all quiescent operating current is returned to the output terminal. This imposes the requirement for a minimum load current. If the load current is less than this minimum, the output voltage will rise.

Since the LM317M is a floating regulator, it is only the voltage differential across the circuit which is important to performance, and operation at high voltages with respect to ground is possible.

Figure 17. Basic Circuit Configuration



Load Regulation

The LM317M is capable of providing extremely good load regulation, but a few precautions are needed to obtain maximum performance. For best performance, the programming resistor (R_1) should be connected as close to the regulator as possible to minimize line drops which effectively appear in series with the reference, thereby degrading regulation. The ground end of R_2 can be returned near the load ground to provide remote ground sensing and improve load regulation.

External Capacitors

A 0.1 μF disc or 1.0 μF tantalum input bypass capacitor (C_{in}) is recommended to reduce the sensitivity to input line impedance.

The adjustment terminal may be bypassed to ground to improve ripple rejection. This capacitor (C_{Adj}) prevents ripple from being amplified as the output voltage is increased. A 10 μF capacitor should improve ripple rejection about 15 dB at 120 Hz in a 10 V application.

Although the LM317M is stable with no output capacitance, like any feedback circuit, certain values of external capacitance can cause excessive ringing. An output capacitance (C_O) in the form of a 1.0 μF tantalum or 25 μF aluminum electrolytic capacitor on the output swamps this effect and insures stability.

Protection Diodes

When external capacitors are used with any IC regulator it is sometimes necessary to add protection diodes to prevent the capacitors from discharging through low current points into the regulator.

Figure 18 shows the LM317M with the recommended protection diodes for output voltages in excess of 25 V or high capacitance values (C_O > 25 μF, C_{Adj} > 5.0 μF). Diode D_1 prevents C_O from discharging thru the IC during an input short circuit. Diode D_2 protects against capacitor C_{Adj} discharging through the IC during an output short circuit. The combination of diodes D_1 and D_2 prevents C_{Adj} from discharging through the IC during an input short circuit.

Figure 18. Voltage Regulator with Protection Diodes

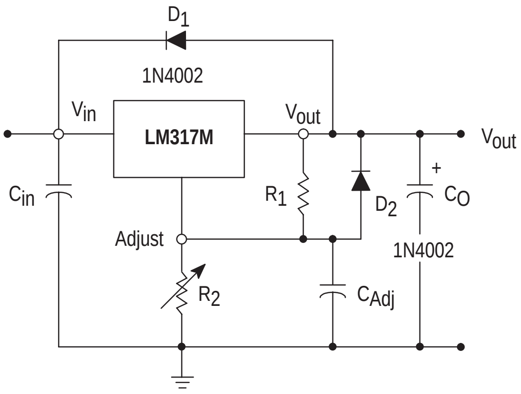
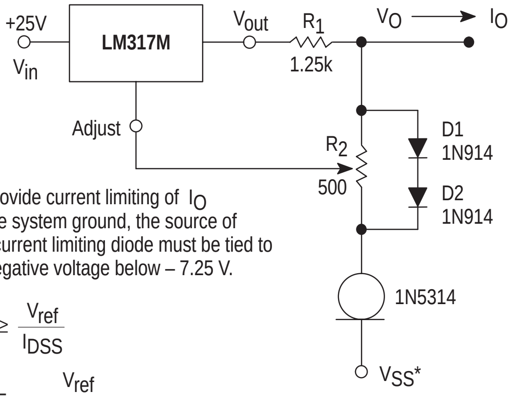


Figure 19. Adjustable Current Limiter



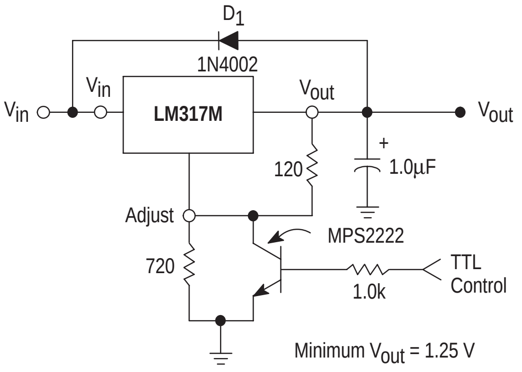
* To provide current limiting of I_O to the system ground, the source of the current limiting diode must be tied to a negative voltage below – 7.25 V.

$$R_2 \geq \frac{V_{ref}}{I_{DSS}}$$

$$R_1 = \frac{V_{ref}}{I_{Omax} + I_{DSS}}$$

$V_O < P_{OV} + 1.25\text{ V} + V_{SS}$
$I_{Lmin} - I_P < I_O < 500\text{ mA} - I_P$
As shown $O < I_O < 495\text{ mA}$

Figure 20. 5 V Electronic Shutdown Regulator



Minimum $V_{out} = 1.25$ V

D_1 protects the device during an input short circuit.

Figure 21. Slow Turn–On Regulator

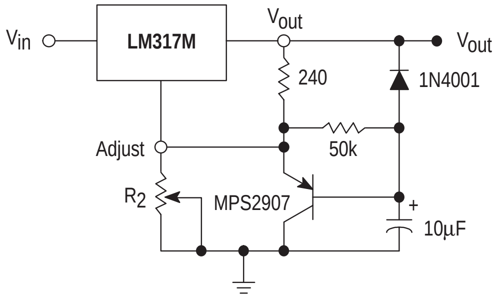
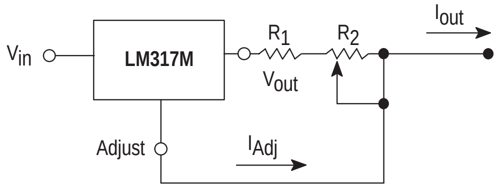


Figure 22. Current Regulator

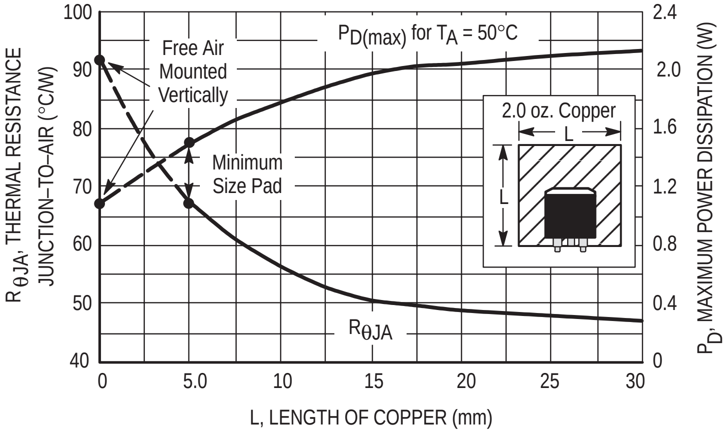


$$I_{outmax} = \left(\frac{V_{ref}}{R_1}\right) + I_{Adj} \cong \frac{1.25\text{ V}}{R_1}$$

$$I_{outmax} = \left(\frac{V_{ref}}{R_1 + R_2}\right) + I_{Adj} \cong \frac{1.25\text{ V}}{R_1 + R_2}$$

$5.0\text{ mA} < I_{out} < 100\text{ mA}$

Figure 23. DPAK Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length



LM323, A

Positive Voltage Regulators

The LM323,A are monolithic integrated circuits which supply a fixed positive 5.0 V output with a load driving capability in excess of 3.0 A. These three–terminal regulators employ internal current limiting, thermal shutdown, and safe–area compensation. The A–suffix is an improved device with superior electrical characteristics and a 2% output voltage tolerance. These regulators are offered with a 0° to +125°C temperature range in a low cost plastic power package.

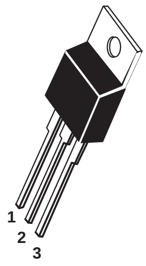
Although designed primarily as a fixed voltage regulator, these devices can be used with external components to obtain adjustable voltages and currents. These devices can be used with a series pass transistor to supply up to 15 A at 5.0 V.

- Output Current in Excess of 3.0 A
- Available with 2% Output Voltage Tolerance
- No External Components Required
- Internal Thermal Overload Protection
- Internal Short Circuit Current Limiting
- Output Transistor Safe–Area Compensation
- Thermal Regulation and Ripple Rejection Have Specified Limits

3–AMPERE, 5 VOLT POSITIVE VOLTAGE REGULATORS

SEMICONDUCTOR TECHNICAL DATA

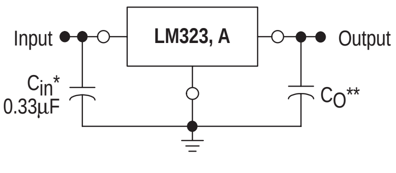
T SUFFIX
PLASTIC PACKAGE
CASE 221A



Pin 1. Input
2. Ground
3. Output

Heatsink surface is connected to Pin 2.

Simplified Application



A common ground is required between the input and the output voltages. The input voltage must remain typically 2.5 V above the output voltage even during the low point on the input ripple voltage.

* C_{in} is required if regulator is located an appreciable distance from power supply filter. (See Applications Information for details.)
** C_O is not needed for stability; however, it does improve transient response.

ORDERING INFORMATION

Device	Output Voltage Tolerance	Operating Temperature Range	Package
LM323T	4%	T_J = 0° to +125°C	Plastic Power
LM323AT	2%		

MAXIMUM RATINGS

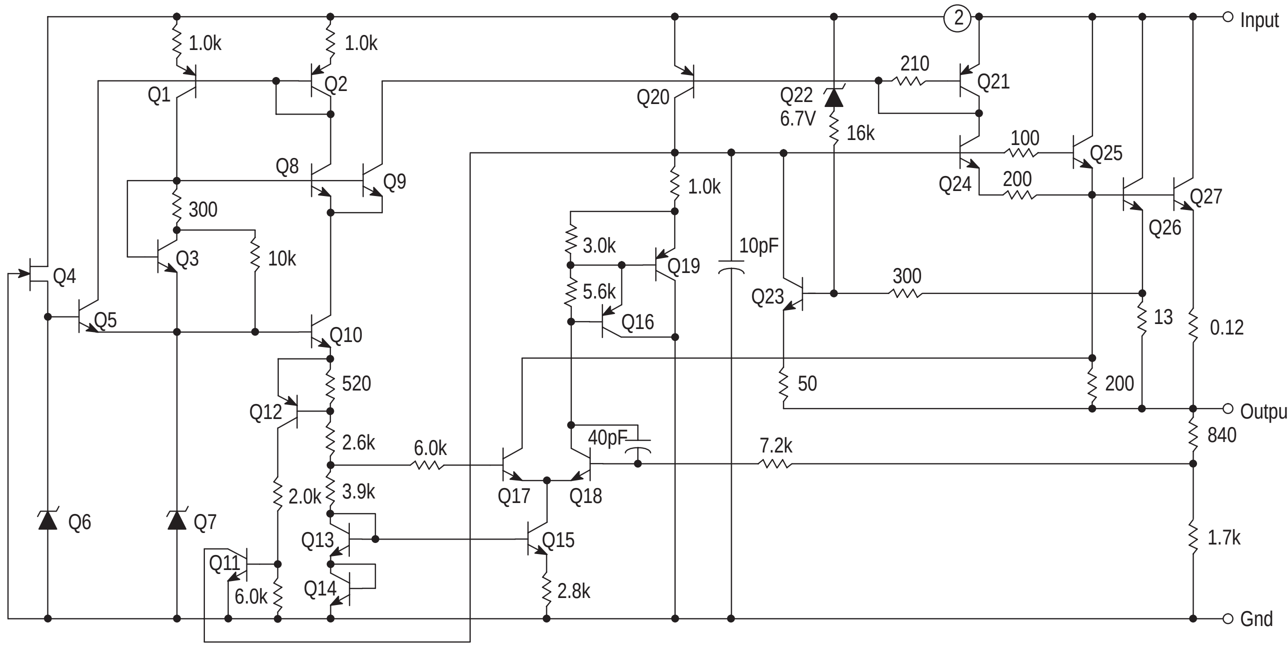
Rating	Symbol	Value	Unit
Input Voltage	V_{in}	20	Vdc
Power Dissipation	P_D	Internally Limited	W
Operating Junction Temperature Range	T_J	0 to +125	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Lead Temperature (Soldering, 10 s)	T_{solder}	300	°C

ELECTRICAL CHARACTERISTICS ($T_J = T_{low}$ to T_{high} [Note 1], unless otherwise noted.)

Characteristics	Symbol	LM323A			LM323			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (V_{in} = 7.5 V, 0 ≤ I_{out} ≤ 3.0 A, T_J = 25°C)	V_O	4.9	5.0	5.1	4.8	5.0	5.2	V
Output Voltage (7.5 V ≤ V_{in} ≤ 15 V, 0 ≤ I_{out} ≤ 3.0 A, P ≤ P_{max}) (Note 2)	V_O	4.8	5.0	5.2	4.75	5.0	5.25	V
Line Regulation (7.5 V ≤ V_{in} ≤ 15 V, T_J = 25°C) (Note 3)	Reg_{line}	–	1.0	15	–	1.0	25	mV
Load Regulation (V_{in} = 7.5 V, 0 ≤ I_{out} ≤ 3.0 A, T_J = 25°C) (Note 3)	Reg_{load}	–	10	50	–	10	100	mV
Thermal Regulation (Pulse = 10 ms, P = 20 W, T_A = 25°C)	Reg_{therm}	–	0.001	0.01	–	0.002	0.03	$\%V_O$/W
Quiescent Current (7.5 V ≤ V_{in} ≤ 15 V, 0 ≤ I_{out} ≤ 3.0 A)	I_B	–	3.5	10	–	3.5	20	mA
Output Noise Voltage (10 Hz ≤ f ≤ 100 kHz, T_J = 25°C)	V_N	–	40	–	–	40	–	μV_{rms}
Ripple Rejection (8.0 V ≤ V_{in} ≤ 18 V, I_{out} = 2.0A, f = 120 Hz, T_J = 25°C)	RR	66	75	–	62	75	–	dB
Short Circuit Current Limit (V_{in} = 15 V, T_J = 25°C) (V_{in} = 7.5 V, T_J = 25°C)	I_{SC}	 – –	 4.5 5.5	 – –	 – –	 4.5 5.5	 – –	A
Long Term Stability	S	–	–	35	–	–	35	mV
Thermal Resistance, Junction–to–Case (Note 4)	$R_{\Theta JC}$	–	2.0	–	–	2.0	–	°C/W

NOTES: 1. T_{low} to T_{high} = 0° to +125°C
2. Although power dissipation is internally limited, specifications apply only for P ≤ P_{max} = 25 W.
3. Load and line regulation are specified at constant junction temperature. Pulse testing is required with a pulse width ≤ 1.0 ms and a duty cycle ≤ 5%.
4. Without a heatsink, the thermal resistance ($R_{\theta JA}$ is 65°C/W). With a heatsink, the effective thermal resistance can approach the specified values of 2.0°C/W, depending on the efficiency of the heatsink.

Representative Schematic Diagram



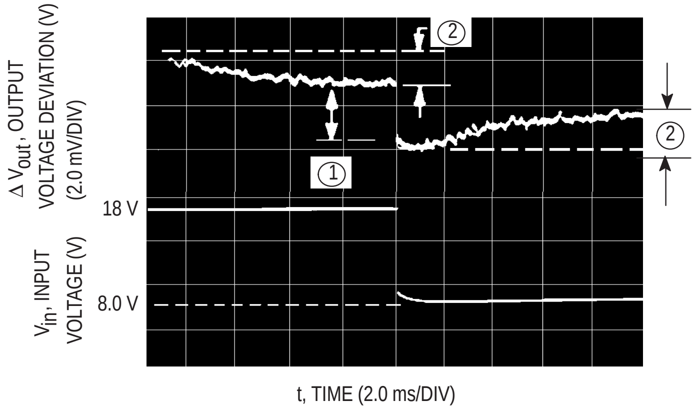
VOLTAGE REGULATOR PERFORMANCE

The performance of a voltage regulator is specified by its immunity to changes in load, input voltage, power dissipation, and temperature. Line and load regulation are tested with a pulse of short duration (< 100 µs) and are strictly a function of electrical gain. However, pulse widths of longer duration (> 1.0 ms) are sufficient to affect temperature gradients across the die. These temperature gradients can cause a change in the output voltage, in addition to changes by line and load regulation. Longer pulse widths and thermal gradients make it desirable to specify thermal regulation.

Thermal regulation is defined as the change in output voltage caused by a change in dissipated power for a specified time, and is expressed as a percentage output voltage change per watt. The change in dissipated power can be caused by a change in either input voltage or the load current. Thermal regulation is a function of IC layout and die attach techniques, and usually occurs within 10 ms of a change in power dissipation. After 10 ms, additional changes in the output voltage are due to the temperature coefficient of the device.

Figure 1 shows the line and thermal regulation response of a typical LM323A to a 20 W input pulse. The variation of the output voltage due to line regulation is labeled À and the thermal regulation component is labeled Á. Figure 2 shows the load and thermal regulation response of a typical LM323A to a 20 W load pulse. The output voltage variation due to load regulation is labeled À and the thermal regulation component is labeled Á.

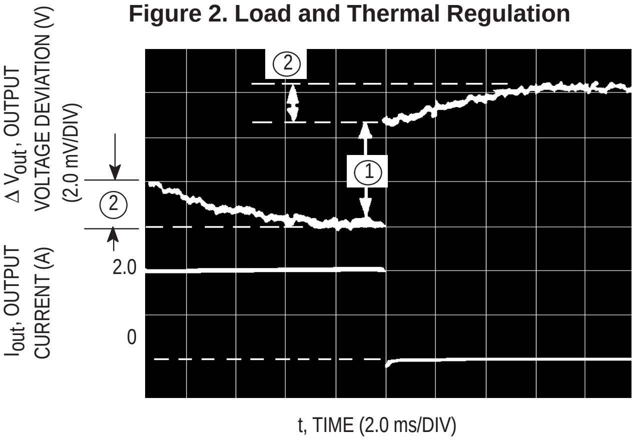
Figure 1. Line and Thermal Regulation



V_{out} = 5.0 V
V_{in} = 8.0 V → 18 V → 8.0 V
I_{out} = 2.0 A

① = Reg_{line} = 2.4 mV
② = Reg_{therm} = 0.0015% V_O/W

Figure 2. Load and Thermal Regulation



V_{out} = 5.0 V
V_{in} = 15 V
I_{out} = 0 A → 2.0 A → 0 A

① = Reg_{line} = 5.4 mV
② = Reg_{therm} = 0.0015% V_O/W

Figure 3. Temperature Stability

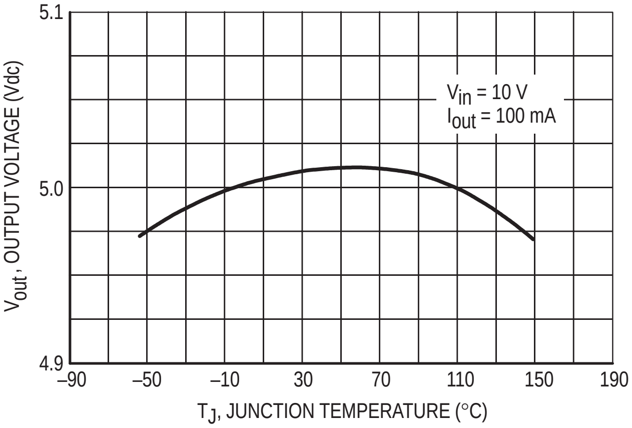


Figure 4. Output Impedance

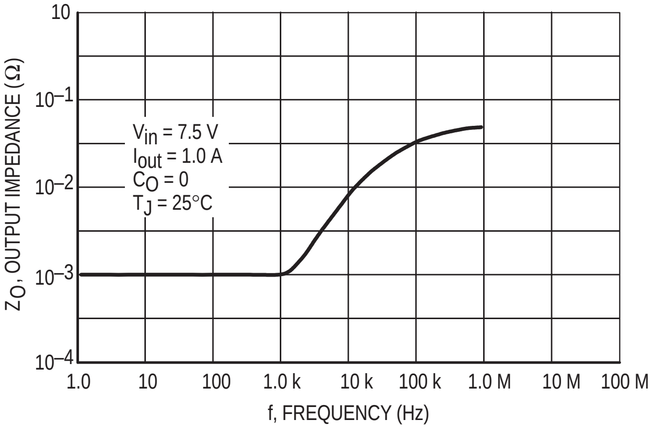


Figure 5. Ripple Rejection versus Frequency

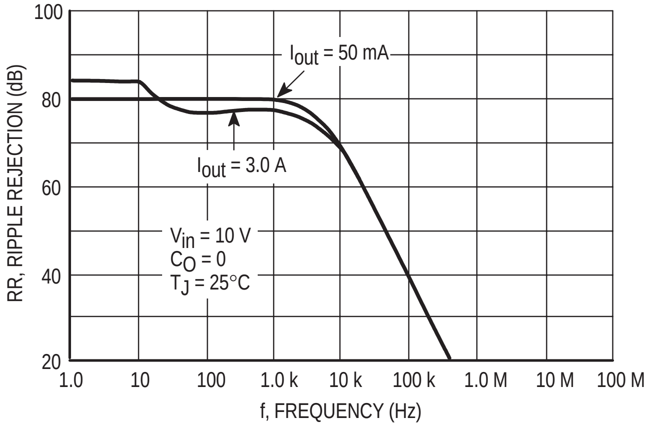


Figure 6. Ripple Rejection versus Output Current

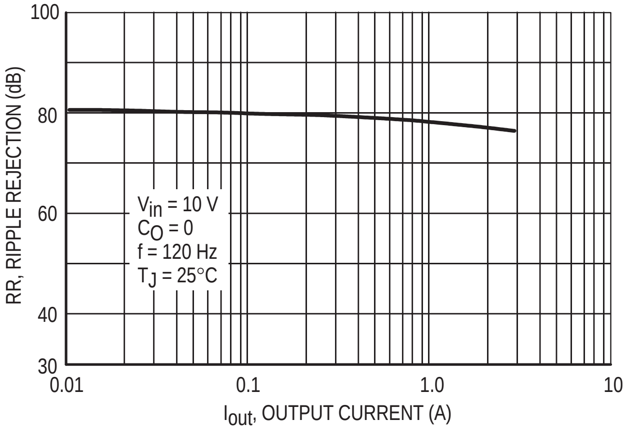


Figure 7. Quiescent Current versus Input Voltage

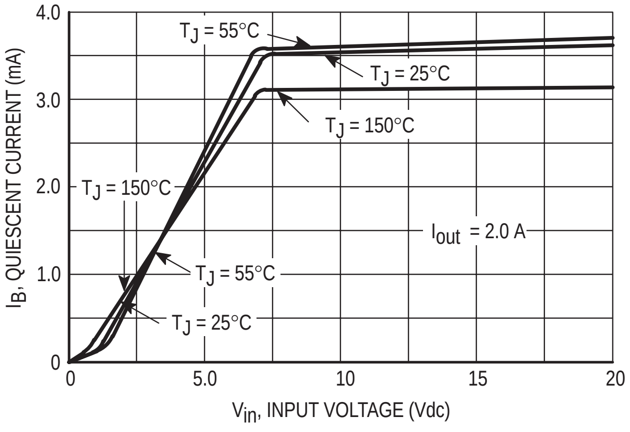
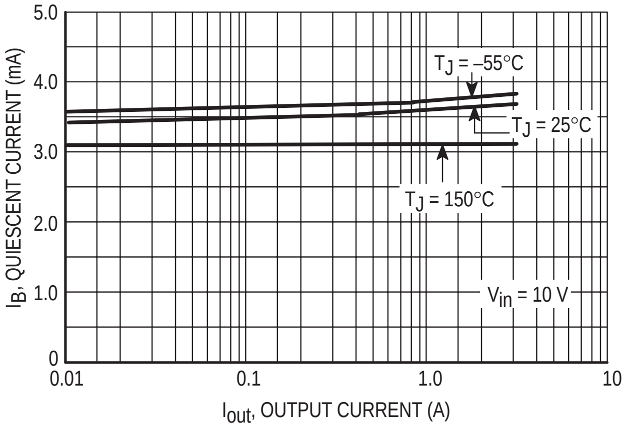


Figure 8. Quiescent Current versus Output Current



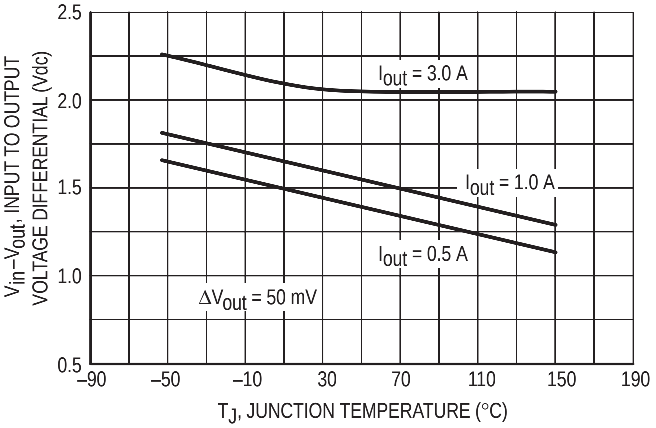


Figure 9. Dropout Voltage

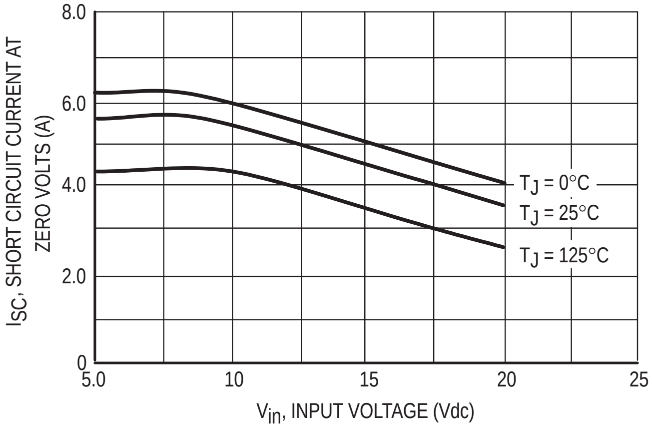


Figure 10. Short Circuit Current

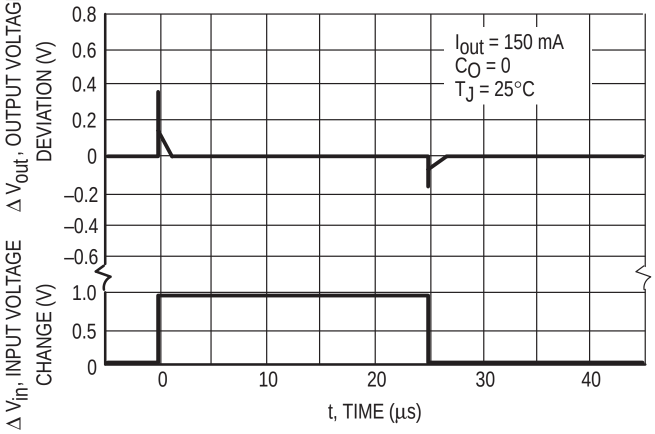


Figure 11. Line Transient Response

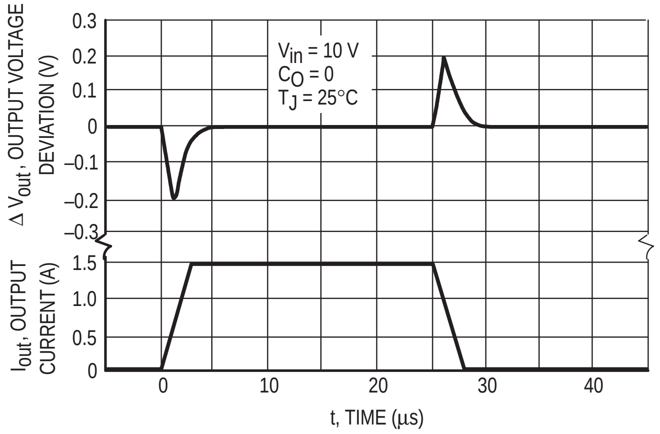


Figure 12. Load Transient Response

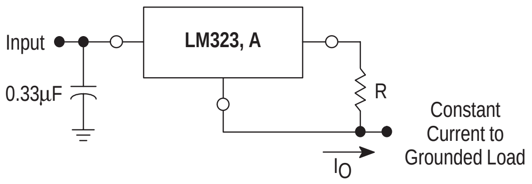
APPLICATIONS INFORMATION

Design Considerations

The LM323,A series of fixed voltage regulators are designed with Thermal Overload Protection that shuts down the circuit when subjected to an excessive power overload condition, Internal Short Circuit Protection that limits the maximum current the circuit will pass, and Output Transistor Safe–Area Compensation that reduces the output short circuit current as the voltage across the pass transistor is increased.

In many low current applications, compensation capacitors are not required. However, it is recommended that the regulator input be bypassed with a capacitor if the regulator is connected to the power supply filter with long wire lengths, or if the output load capacitance is large. An input bypass capacitor should be selected to provide good high–frequency characteristics to insure stable operation under all load conditions. A 0.33 µF or larger tantalum, mylar, or other capacitor having low internal impedance at high frequencies should be chosen. The bypass capacitor should be mounted with the shortest possible leads directly across the regulator's input terminals. Normally good construction techniques should be used to minimize ground loops and lead resistance drops since the regulator has no external sense lead.

Figure 13. Current Regulator



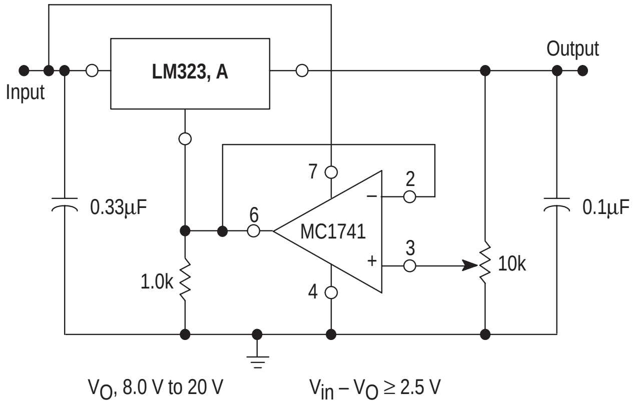
The LM323,A regulator can also be used as a current source when connected as above. Resistor R determines the current as follows:

$$I_O = \frac{5.0\ V}{R} + I_B$$

$\Delta I_B \cong$ 0.7 mA over line, load and temperature changes
$I_B \cong$ 3.5 mA

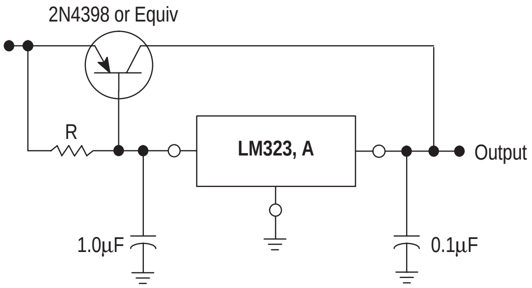
For example, a 2.0 A current source would require R to be a 2.5 Ω, 15 W resistor and the output voltage compliance would be the input voltage less 7.5 V.

Figure 14. Adjustable Output Regulator



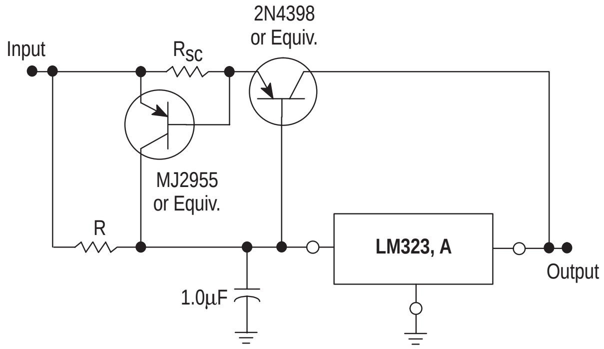
The addition of an operational amplifier allows adjustment to higher or intermediate values while retaining regulation characteristics. The minimum voltage obtainable with this arrangement is 3.0 V greater than the regulator voltage.

Figure 15. Current Boost Regulator



The LM323, A series can be current boosted with a PNP transistor. The 2N4398 provides current to 15 A. Resistor R in conjuction with the V_{BE} of the PNP determines when the pass transistor begins conducting; this circuit is not short circuit proof. Input–output differential voltage minimum is increased by the V_{BE} of the pass transistor.

Figure 16. Current Boost with Short Circuit Protection



The circuit of Figure 16 can be modified to provide supply protection against short circuits by adding a short circuit sense resistor, R_{SC}, and an additional PNP transistor. The current sensing PNP must be able to handle the short circuit current of the three–terminal regulator. Therefore, an 8.0 A power transistor is specified.

MOTOROLA

LM337

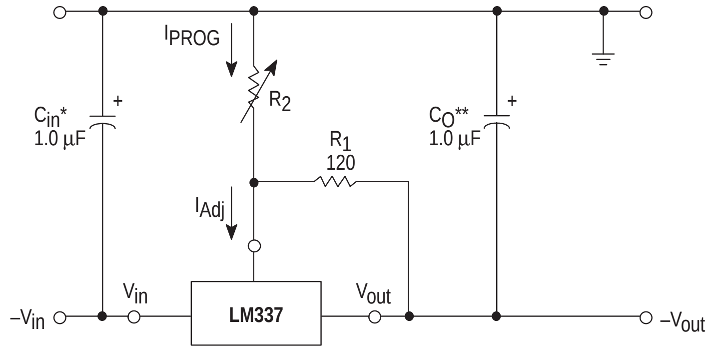
Three-Terminal Adjustable Output Negative Voltage Regulator

The LM337 is an adjustable 3–terminal negative voltage regulator capable of supplying in excess of 1.5 A over an output voltage range of –1.2 V to –37 V. This voltage regulator is exceptionally easy to use and requires only two external resistors to set the output voltage. Further, it employs internal current limiting, thermal shutdown and safe area compensation, making it essentially blow–out proof.

The LM337 serves a wide variety of applications including local, on card regulation. This device can also be used to make a programmable output regulator, or by connecting a fixed resistor between the adjustment and output, the LM337 can be used as a precision current regulator.

- Output Current in Excess of 1.5 A
- Output Adjustable between –1.2 V and –37 V
- Internal Thermal Overload Protection
- Internal Short Circuit Current Limiting Constant with Temperature
- Output Transistor Safe–Area Compensation
- Floating Operation for High Voltage Applications
- Eliminates Stocking many Fixed Voltages
- Available in Surface Mount D^2PAK and Standard 3–Lead Transistor Package

Standard Application



*C_{in} is required if regulator is located more than 4 inches from power supply filter. A 1.0 µF solid tantalum or 10 µF aluminum electrolytic is recommended.

**C_O is necessary for stability. A 1.0 µF solid tantalum or 10 µF aluminum electrolytic is recommeded.

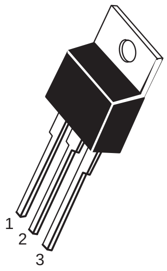
$$V_{out} = -1.25\ V\left(1 + \frac{R_2}{R_1}\right)$$

THREE–TERMINAL ADJUSTABLE NEGATIVE VOLTAGE REGULATOR

SEMICONDUCTOR TECHNICAL DATA

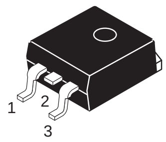
T SUFFIX
PLASTIC PACKAGE
CASE 221A

Heatsink surface connected to Pin 2.



Pin 1. Adjust
2. V_{in}
3. V_{out}

D2T SUFFIX
PLASTIC PACKAGE
CASE 936
(D^2PAK)



Heatsink surface (shown as terminal 4 in case outline drawing) is connected to Pin 2.

ORDERING INFORMATION

Device	Operating Temperature Range	Package
LM337BD2T	T_J = –40° to +125°C	Surface Mount
LM337BT		Insertion Mount
LM337D2T	T_J = 0° to +125°C	Surface Mount
LM337T		Insertion Mount

MAXIMUM RATINGS

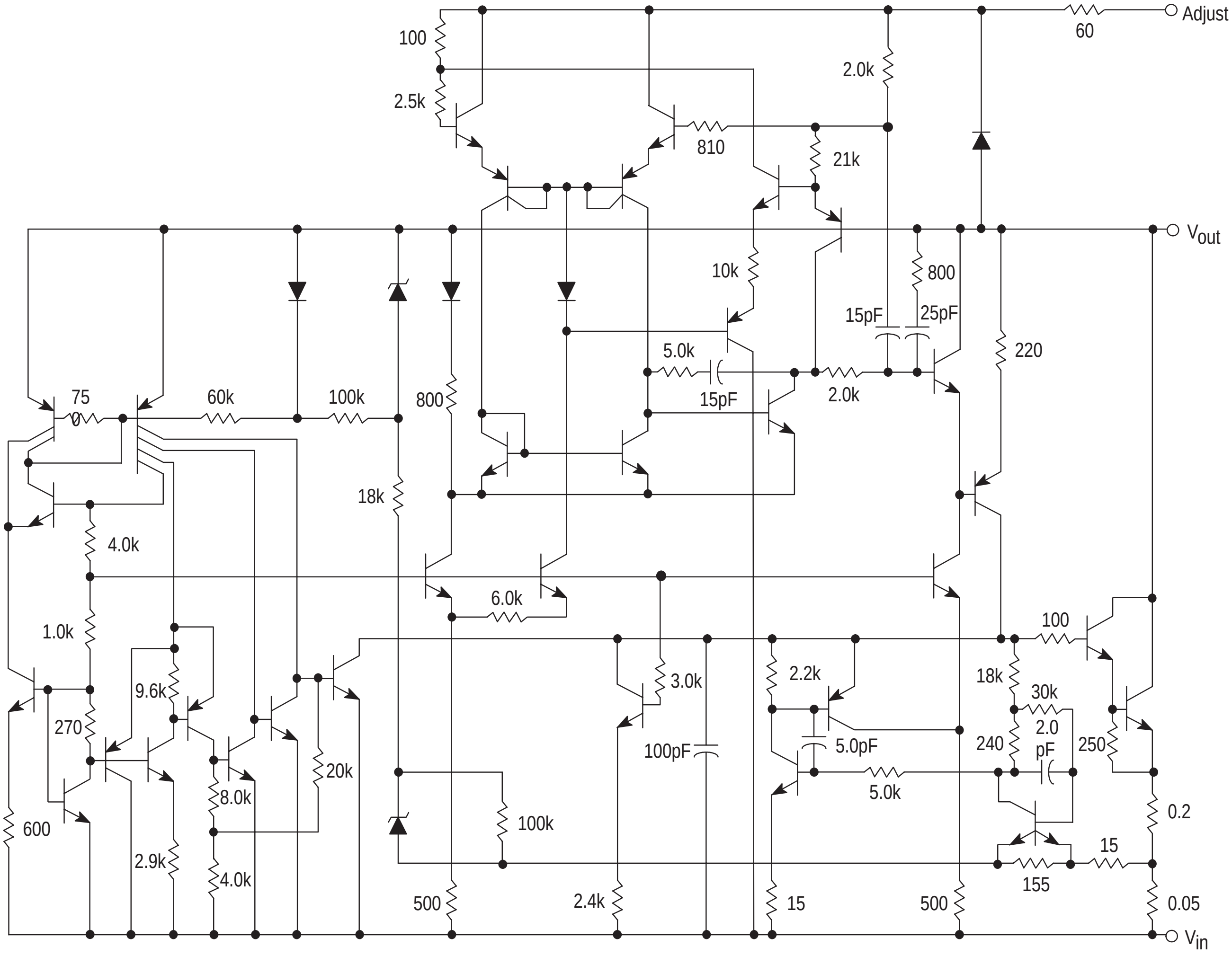
Rating	Symbol	Value	Unit
Input–Output Voltage Differential	$V_I–V_O$	40	Vdc
Power Dissipation			
Case 221A			
T_A = +25°C	P_D	Internally Limited	W
Thermal Resistance, Junction–to–Ambient	θ_{JA}	65	°C/W
Thermal Resistance, Junction–to–Case	θ_{JC}	5.0	°C/W
Case 936 (D^2PAK)			
T_A = +25°C	P_D	Internally Limited	W
Thermal Resistance, Junction–to–Ambient	θ_{JA}	70	°C/W
Thermal Resistance, Junction–to–Case	θ_{JC}	5.0	°C/W
Operating Junction Temperature Range	T_J	–40 to +125	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

ELECTRICAL CHARACTERISTICS ($|V_I–V_O|$ = 5.0 V; I_O = 0.5 A for T package; $T_J = T_{low}$ to T_{high} [Note 1]; I_{max} and P_{max} [Note 2].)

Characteristics	Figure	Symbol	Min	Typ	Max	Unit
Line Regulation (Note 3), T_A = +25°C, 3.0 V ≤ $\lvert V_I–V_O \rvert$ ≤ 40 V	1	Reg_{line}	–	0.01	0.04	%/V
Load Regulation (Note 3), T_A = +25°C, 10 mA ≤ I_O ≤ I_{max}	2	Reg_{load}				
$\lvert V_O \rvert$ ≤ 5.0 V			–	15	50	mV
$\lvert V_O \rvert$ ≥ 5.0 V			–	0.3	1.0	% V_O
Thermal Regulation, T_A = +25°C (Note 6), 10 ms Pulse		Reg_{therm}	–	0.003	0.04	% V_O/W
Adjustment Pin Current	3	I_{Adj}	–	65	100	µA
Adjustment Pin Current Change, 2.5 V ≤ $\lvert V_I–V_O \rvert$ ≤ 40 V, 10 mA ≤ I_L ≤ I_{max}, P_D ≤ P_{max}, T_A = +25°C	1, 2	ΔI_{Adj}	–	2.0	5.0	µA
Reference Voltage, T_A = +25°C, 3.0 V ≤ $\lvert V_I–V_O \rvert$ ≤ 40 V,	3	V_{ref}	–1.213	–1.250	–1.287	V
10 mA ≤ I_O ≤ I_{max}, P_D ≤ P_{max}, $T_J = T_{low}$ to T_{high}			–1.20	–1.25	–1.30	
Line Regulation (Note 3), 3.0 V ≤ $\lvert V_I–V_O \rvert$ ≤ 40 V	1	Reg_{line}	–	0.02	0.07	%/V
Load Regulation (Note 3), 10 mA ≤ I_O ≤ I_{max}	2	Reg_{load}				
$\lvert V_O \rvert$ ≤ 5.0 V			–	20	70	mV
$\lvert V_O \rvert$ ≥ 5.0 V			–	0.3	1.5	% V_O
Temperature Stability (T_{low} ≤ T_J ≤ T_{high})	3	T_S	–	0.6	–	% V_O
Minimum Load Current to Maintain Regulation	3	I_{Lmin}				mA
($\lvert V_I–V_O \rvert$ ≤ 10 V)			–	1.5	6.0	
($\lvert V_I–V_O \rvert$ ≤ 40 V)			–	2.5	10	
Maximum Output Current	3	I_{max}				A
$\lvert V_I–V_O \rvert$ ≤ 15 V, P_D ≤ P_{max}, T Package			–	1.5	2.2	
$\lvert V_I–V_O \rvert$ ≤ 40 V, P_D ≤ P_{max}, T_J = +25°C, T Package			–	0.15	0.4	
RMS Noise, % of V_O, T_A = +25°C, 10 Hz ≤ f ≤ 10 kHz		N	–	0.003	–	% V_O
Ripple Rejection, V_O = –10 V, f = 120 Hz (Note 4)	4	RR				dB
Without C_{Adj}			–	60	–	
C_{Adj} = 10 µF			66	77	–	
Long–Term Stability, $T_J = T_{high}$ (Note 5), T_A = +25°C for Endpoint Measurements	3	S	–	0.3	1.0	%/1.0 k Hrs.
Thermal Resistance Junction–to–Case, T Package		$R_{\theta JC}$	–	4.0	–	°C/W

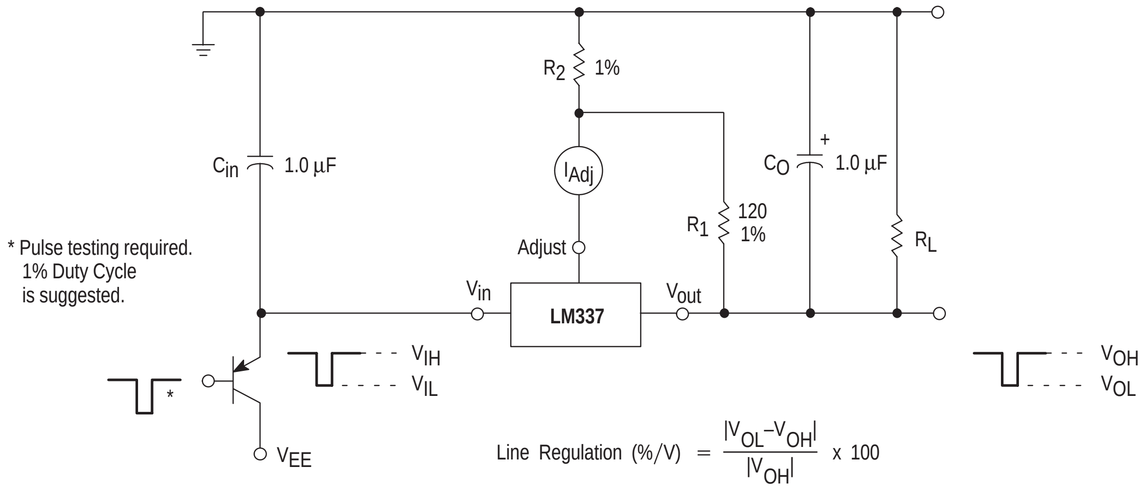
NOTES:
1. T_{low} to T_{high} = 0° to +125°C, for LM337T, D2T. T_{low} to T_{high} = –40° to +125°C, for LM337BT, BD2T.
2. I_{max} = 1.5 A, P_{max} = 20 W
3. Load and line regulation are specified at constant junction temperature. Change in V_O because of heating effects is covered under the Thermal Regulation specification. Pulse testing with a low duty cycle is used.
4. C_{Adj}, when used, is connected between the adjustment pin and ground.
5. Since Long Term Stability cannot be measured on each device before shipment, this specification is an engineering estimate of average stability from lot to lot.
6. Power dissipation within an IC voltage regulator produces a temperature gradient on the die, affecting individual IC components on the die. These effects can be minimized by proper integrated circuit design and layout techniques. Thermal Regulation is the effect of these temperature gradients on the output voltage and is expressed in percentage of output change per watt of power change in a specified time.

Representative Schematic Diagram



This device contains 39 active transistors.

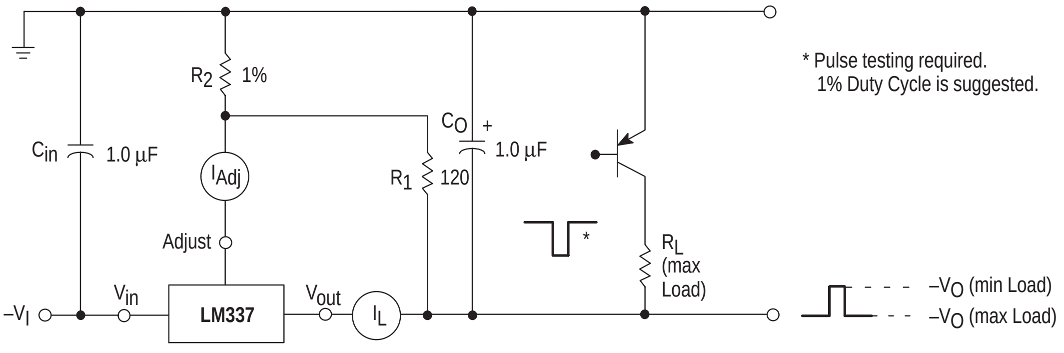
Figure 1. Line Regulation and ΔI_{Adj}/Line Test Circuit



* Pulse testing required.
1% Duty Cycle
is suggested.

$$\text{Line Regulation } (\%/V) = \frac{|V_{OL} - V_{OH}|}{|V_{OH}|} \times 100$$

Figure 2. Load Regulation and ΔI_{Adj}/Load Test Circuit

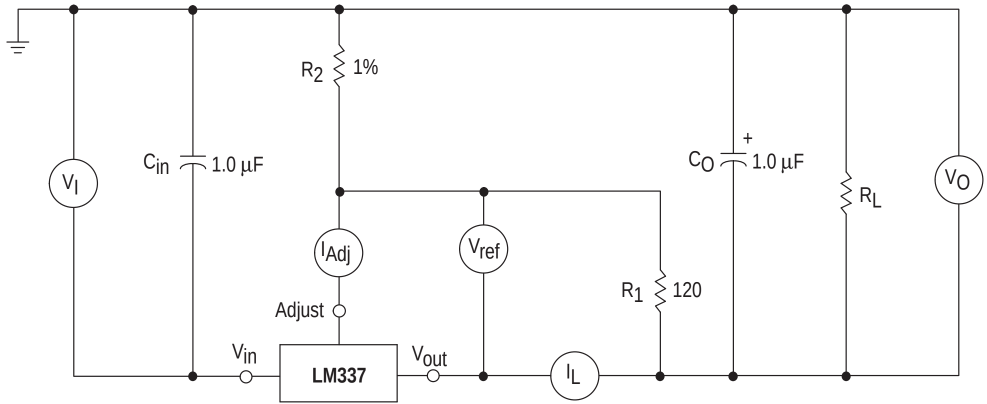


* Pulse testing required.
1% Duty Cycle is suggested.

Load Regulation (mV) = V_O (min Load) – V_O (max Load)

$$\text{Load Regulation } (\%\ V_O) = \frac{V_O \text{ (min Load)} - V_O \text{ (max Load)}}{V_O \text{ (min Load)}} \times 100$$

Figure 3. Standard Test Circuit

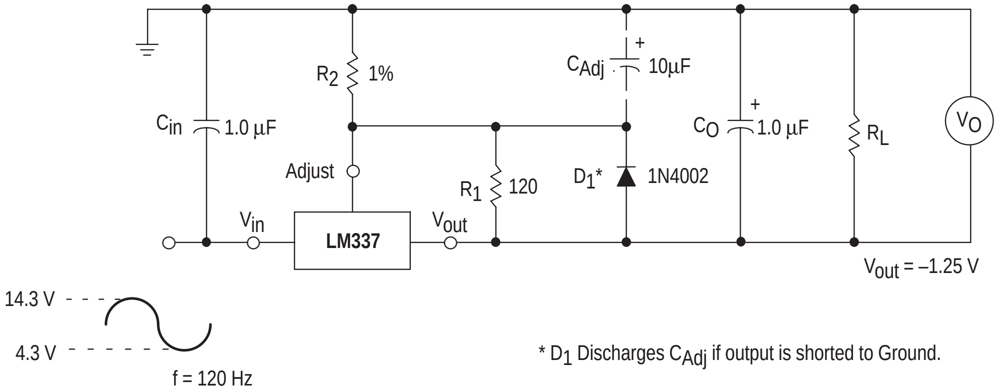


To Calculate R_2: $R_2 = \left(\frac{V_O}{V_{ref}} - 1\right) R_1$

This assumes I_{Adj} is negligible.

* Pulse testing required.
1% Duty Cycle is suggested.

Figure 4. Ripple Rejection Test Circuit



* D_1 Discharges C_{Adj} if output is shorted to Ground.

Figure 5. Load Regulation

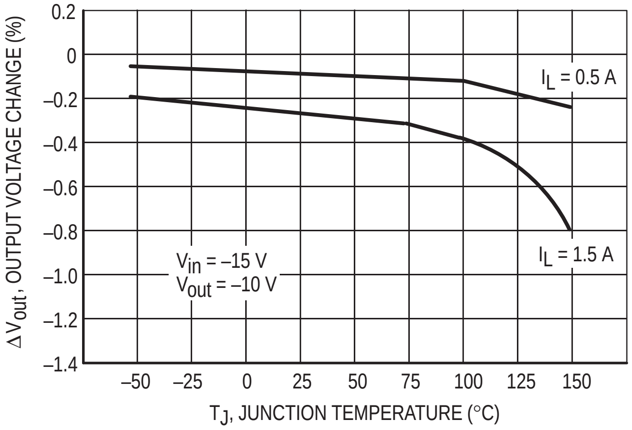


Figure 6. Current Limit

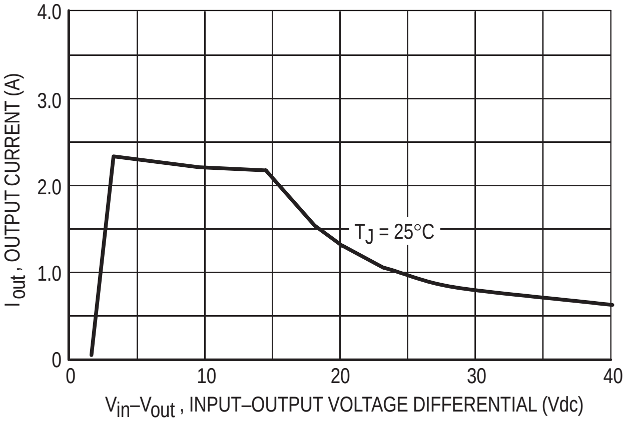


Figure 7. Adjustment Pin Current

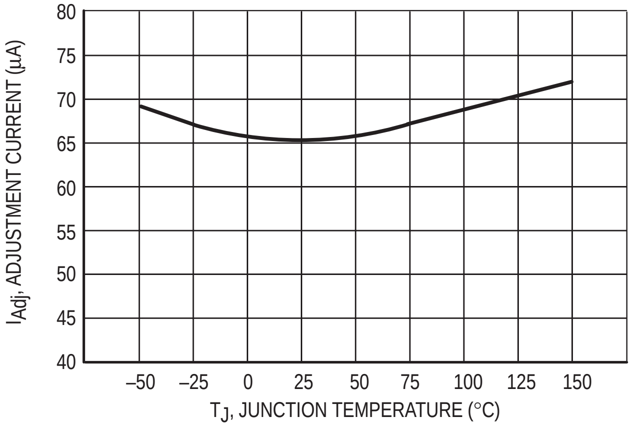


Figure 8. Dropout Voltage

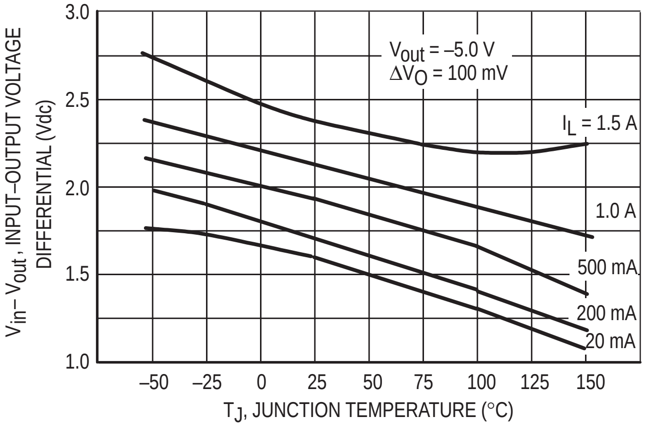


Figure 9. Temperature Stability

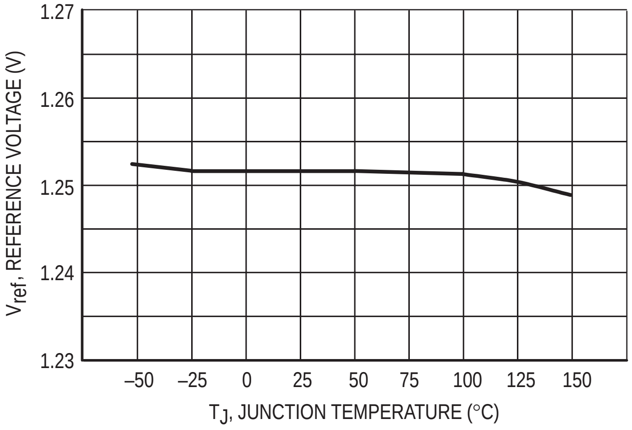


Figure 10. Minimum Operating Current

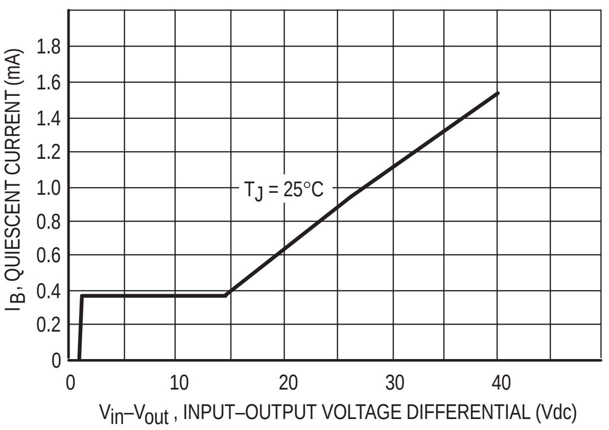


Figure 11. Ripple Rejection versus Output Voltage

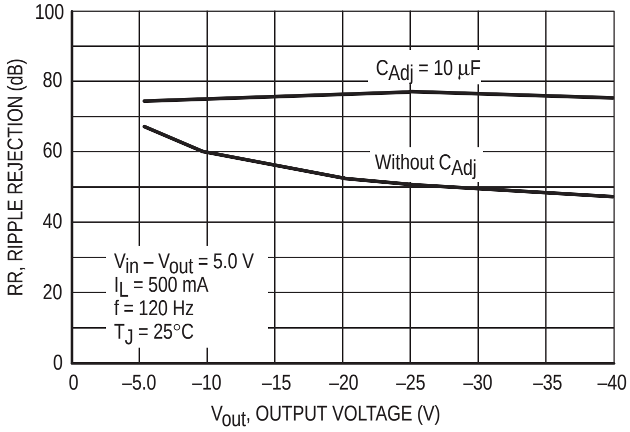


Figure 12. Ripple Rejection versus Output Current

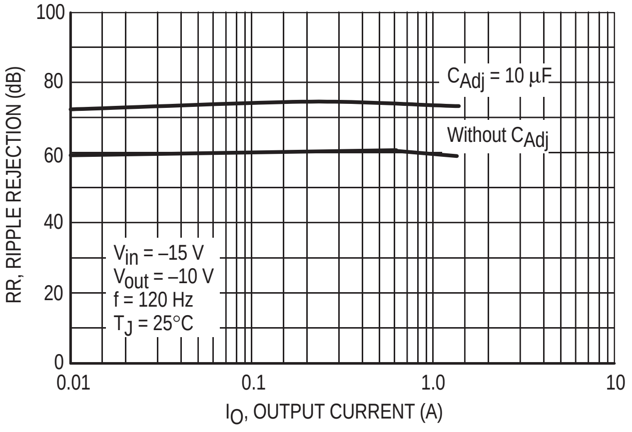


Figure 13. Ripple Rejection versus Frequency

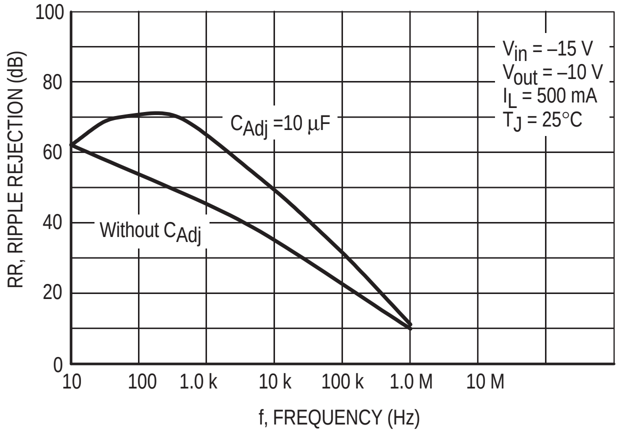


Figure 14. Output Impedance

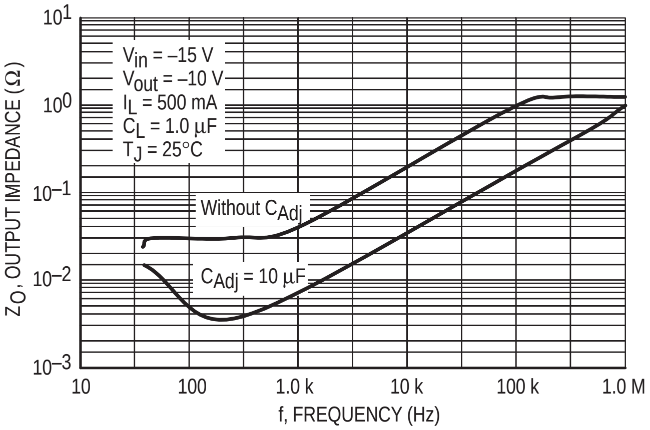


Figure 15. Line Transient Response

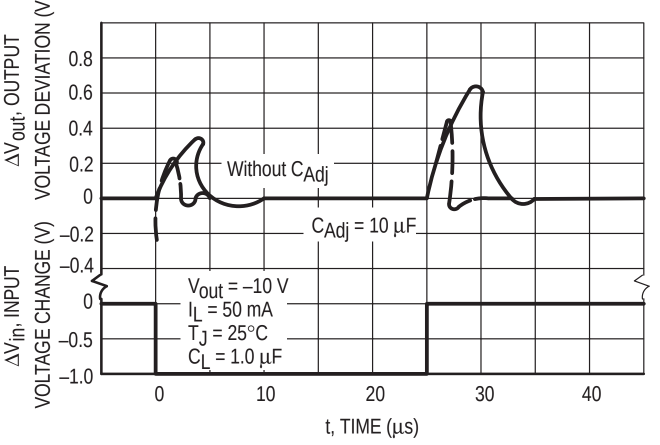
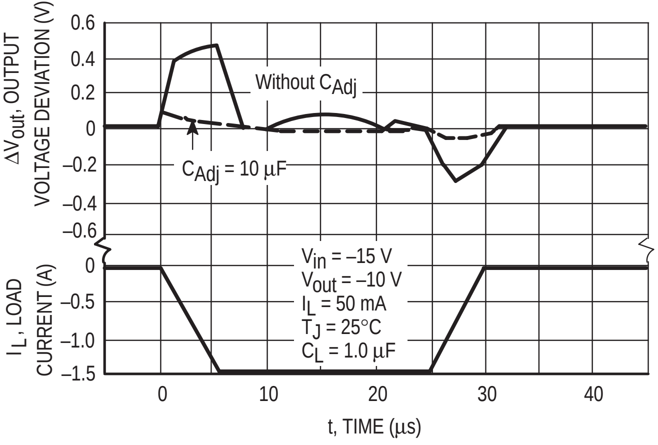


Figure 16. Load Transient Reponse



APPLICATIONS INFORMATION

Basic Circuit Operation

The LM337 is a 3–terminal floating regulator. In operation, the LM337 develops and maintains a nominal –1.25 V reference (V_{ref}) between its output and adjustment terminals. This reference voltage is converted to a programming current (I_{PROG}) by R_1 (see Figure 17), and this constant current flows through R_2 from ground.

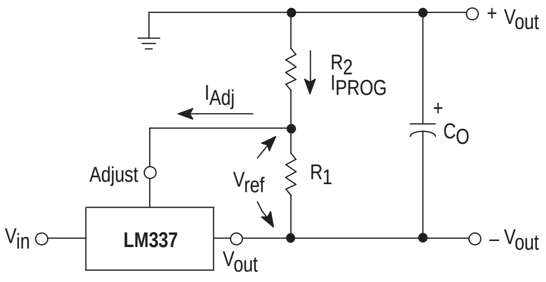
The regulated output voltage is given by:

$$V_{out} = V_{ref}\left(1 + \frac{R_2}{R_1}\right) + I_{Adj}\, R_2$$

Since the current into the adjustment terminal (I_{Adj}) represents an error term in the equation, the LM337 was designed to control I_{Adj} to less than 100 µA and keep it constant. To do this, all quiescent operating current is returned to the output terminal. This imposes the requirement for a minimum load current. If the load current is less than this minimum, the output voltage will rise.

Since the LM337 is a floating regulator, it is only the voltage differential across the circuit which is important to performance, and operation at high voltages with respect to ground is possible.

Figure 17. Basic Circuit Configuration



V_{ref} = –1.25 V Typical

Load Regulation

The LM337 is capable of providing extremely good load regulation, but a few precautions are needed to obtain maximum performance. For best performance, the programming resistor (R_1) should be connected as close to the regulator as possible to minimize line drops which effectively appear in series with the reference, thereby degrading regulation. The ground end of R_2 can be returned near the load ground to provide remote ground sensing and improve load regulation.

External Capacitors

A 1.0 µF tantalum input bypass capacitor (C_{in}) is recommended to reduce the sensitivity to input line impedance.

The adjustment terminal may be bypassed to ground to improve ripple rejection. This capacitor (C_{Adj}) prevents ripple from being amplified as the output voltage is increased. A 10 µF capacitor should improve ripple rejection about 15 dB at 120 Hz in a 10 V application.

An output capacitance (C_O) in the form of a 1.0 µF tantalum or 10 µF aluminum electrolytic capacitor is required for stability.

Protection Diodes

When external capacitors are used with any IC regulator it is sometimes necessary to add protection diodes to prevent the capacitors from discharging through low current points into the regulator.

Figure 18 shows the LM337 with the recommended protection diodes for output voltages in excess of –25 V or high capacitance values (C_O > 25 µF, C_{Adj} > 10 µF). Diode D_1 prevents C_O from discharging thru the IC during an input short circuit. Diode D_2 protects against capacitor C_{Adj} discharging through the IC during an output short circuit. The combination of diodes D_1 and D_2 prevents C_{Adj} from the discharging through the IC during an input short circuit.

Figure 18. Voltage Regulator with Protection Diodes

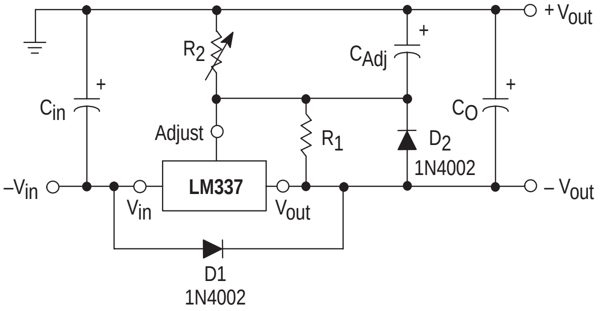
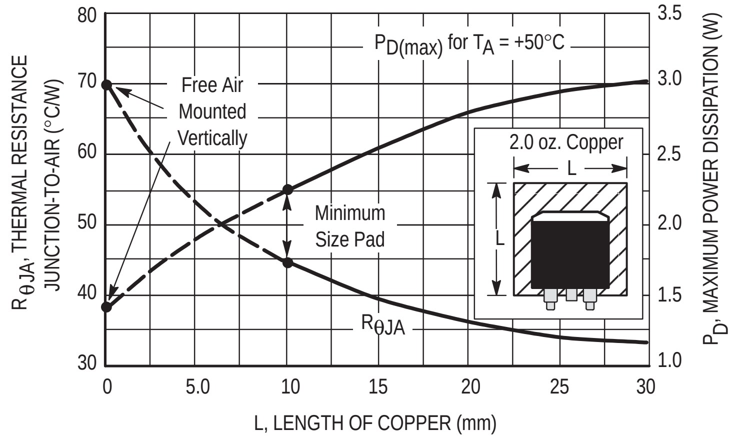


Figure 19. D²PAK Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length



MOTOROLA

LM337M

Three-Terminal Adjustable Output Negative Voltage Regulator

MEDIUM CURRENT THREE–TERMINAL ADJUSTABLE NEGATIVE VOLTAGE REGULATOR

SEMICONDUCTOR TECHNICAL DATA

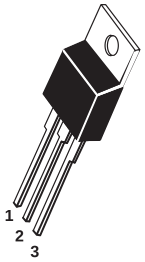
The LM337M is an adjustable three–terminal negative voltage regulator capable of supplying in excess of 500 mA over an output voltage range of –1.2 V to –37 V. This voltage regulator is exceptionally easy to use and requires only two external resistors to set the output voltage. Further, it employs internal current limiting, thermal shutdown and safe area compensation, making it essentially blow–out proof.

The LM337M serves a wide variety of applications including local, on–card regulation. This device can also be used to make a programmable output regulator or by connecting a fixed resistor between the adjustment and output. The LM337M can be used as a precision current regulator.

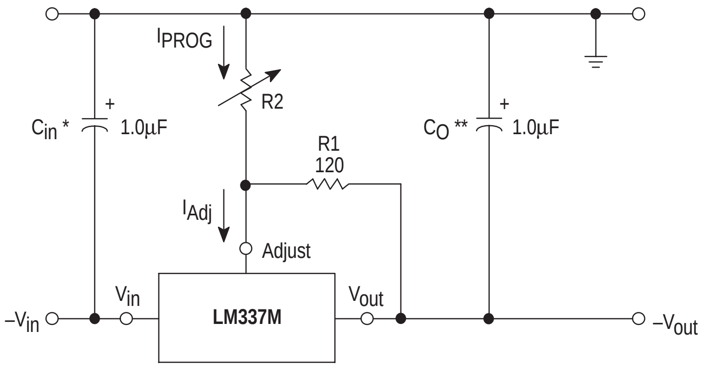
- Output Current in Excess of 500 mA
- Output Adjustable Between –1.2 V and –37 V
- Internal Thermal Overload Protection
- Internal Short Circuit Current Limiting
- Output Transistor Safe–Area Compensation
- Floating Operation for High Voltage Applications
- Standard 3–Lead Transistor Packages
- Eliminates Stocking Many Fixed Voltages

T SUFFIX
PLASTIC PACKAGE
CASE 221A

Pin 1. Adjust
2. V_{in}
3. V_{out}



Standard Application



*C_{in} is required if regulator is located more than 4″ from power supply filter. A 1.0 µF solid tantalum or 10 µF aluminum electrolytic is recommended.
**C_O is necessary for stability. A 1.0 µF solid tantalum or 10 µF aluminum electrolytic is recommeded.

$$V_{out} = -1.25\ V\left(1 + \frac{R2}{R1}\right)$$

ORDERING INFORMATION

Device	Operating Temperature Range	Package
LM337MT	T_J = 0° to +125°C	Plastic Power

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input–Output Voltage Differential	$V_I–V_O$	40	Vdc
Power Dissipation	P_D	Internally Limited	W
Operating Junction Temperature Range	T_J	0 to +125	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

ELECTRICAL CHARACTERISTICS ($|V_I – V_O| = 5.0$ V, $I_O = 0.1$; $T_J = T_{low}$ to T_{high} [Note 1], P_{max} per Note 2, unless otherwise noted.)

Characteristics	Figure	Symbol	Min	Typ	Max	Unit
Line Regulation (Note 3) $T_A = 25°C$, $3.0\ V \le |V_I–V_O| \le 40\ V$	1	Reg_{line}	–	0.01	0.04	%/V
Load Regulation (Note 3) $T_A = 25°C$, $10\ mA \le I_O \le 0.5\ A$	2	Reg_{load}				
$|V_O| \le 5.0V$			–	15	15	mV
$|V_O| \ge 5.0V$			–	0.3	1.0	%/V_O
Thermal Regulation 10 ms Pulse, $T_A = 25°C$	–	Reg_{therm}	–	0.03	0.04	% V_O/W
Adjustment Pin Current	3	I_{Adj}	–	65	100	µA
Adjustment Pin Current Change $2.5\ V \le |V_I–V_O| \le 40\ V$, $10\ mA \le I_L \le 0.5\ A$, $P_D \le P_{max}$, $T_A = 25°C$	1, 2	ΔI_{Adj}	–	2.0	5.0	µA
Reference Voltage $3.0\ V \le |V_I–V_O| \le 40\ V$, $10\ mA \le I_O \le 0.5\ A$,	3	V_{ref}				V
$P_D \le P_{max}$, $T_A = 25°C$			–1.213	–1.250	–1.287	
T_{low} to T_{high}			–1.20	–1.25	–1.30	
Line Regulation (Note 3) $3.0\ V \le |V_I–V_O| \le 40\ V$	1	Reg_{line}	–	0.02	0.07	%/V
Load Regulation (Note 3) $10\ mA \le I_O \le 0.5\ A$	2	Reg_{load}				mV
$|V_O| \le 5.0\ V$			–	20	70	%/V_O
$|V_O| \ge 5.0\ V$			–	0.3	1.5	
Temperature Stability ($T_{low} \le T_J \le T_{high}$)	3	T_S	–	0.6	–	%/V_O
Minimum Load Current to Maintain Regulation	3	I_{Lmin}				mA
($|V_I–V_O| \le 10\ V$)			–	1.5	6.0	
($|V_I–V_O| \le 40\ V$)			–	2.5	10	
Maximum Output Current	3	I_{max}				A
$|V_I–V_O| \le 15\ V$, $P_D \le P_{max}$			0.5	0.9	–	
$|V_I–V_O| \le 40\ V$, $P_D \le P_{max}$, $T_J = 25°C$			0.1	0.25	–	
RMS Noise, % of V_O $T_A = 25°C$, $10\ Hz \le f \le 10\ kHz$	–	N	–	0.003	–	%/V_O
Ripple Rejection, $V_O = –10$ V, f = 120 Hz (Note 4)	4	RR				dB
Without C_{Adj}			–	60	–	
$C_{Adj} = 10\ \mu F$			66	77	–	
Long Term Stability, $T_J = T_{high}$ (Note 5) $T_A = 25°C$ for Endpoint Measurements	3	S	–	0.3	1.0	%/1.0 k Hrs
Thermal Resistance, Junction–to–Case	–	$R_{\Theta JC}$	–	7.0	–	°C/W

NOTES: 1. T_{low} to T_{high} = 0° to +125°C
2. P_{max} = 7.5 W
3 Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.
4. C_{Adj}, when used, is connected between the adjustment pin and ground.
5. Since Long Term Stability cannot be measured on each device before shipment, this specification is an engineering estimate of average stability from lot to lot.

Schematic Diagram

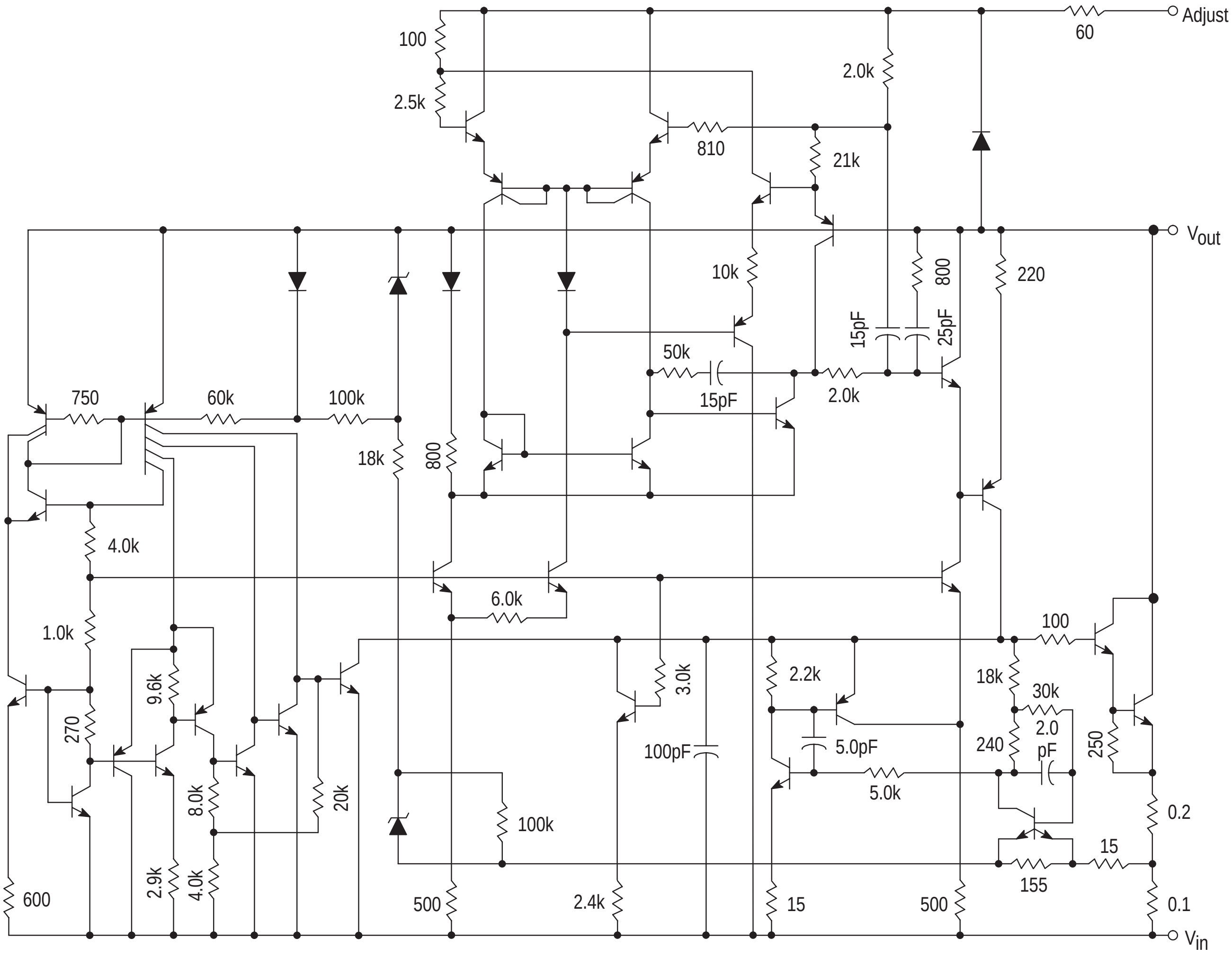
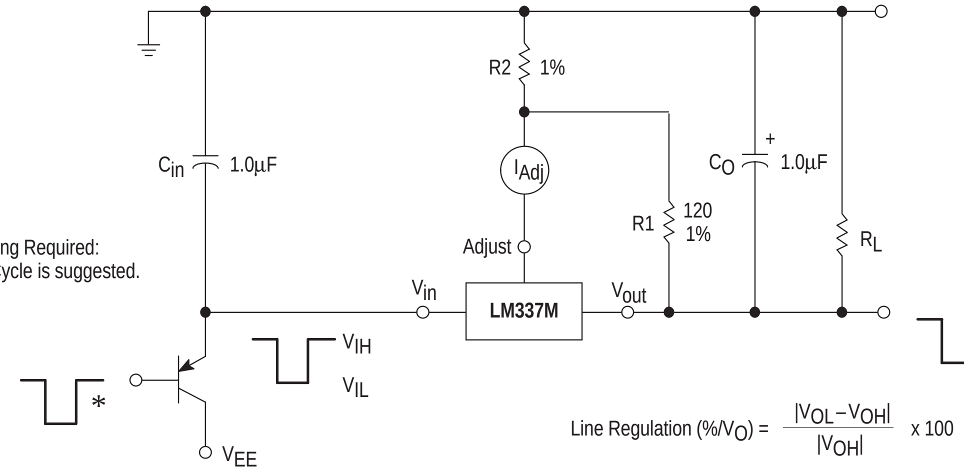


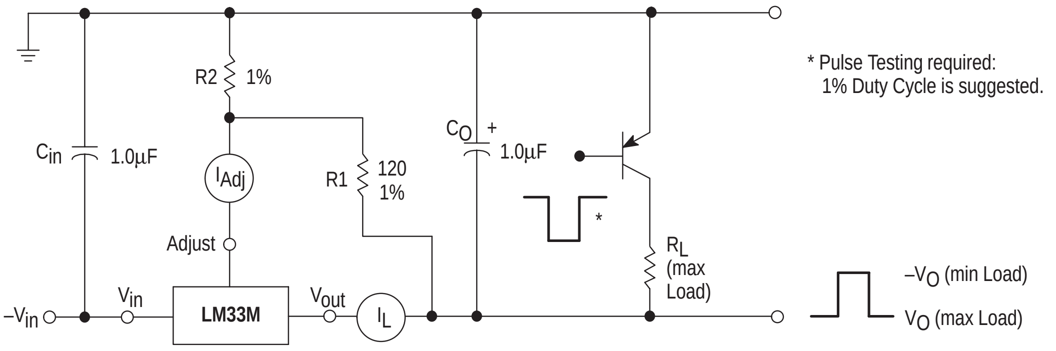
Figure 1. Line Regulation and ΔI_{Adj}/Line Test Circuit



* Pulse Testing Required:
1% Duty Cycle is suggested.

$$\text{Line Regulation } (\%/V_O) = \frac{|V_{OL} - V_{OH}|}{|V_{OH}|} \times 100$$

Figure 2. Load Regulation and ΔI_{Adj}/Load Test Circuit

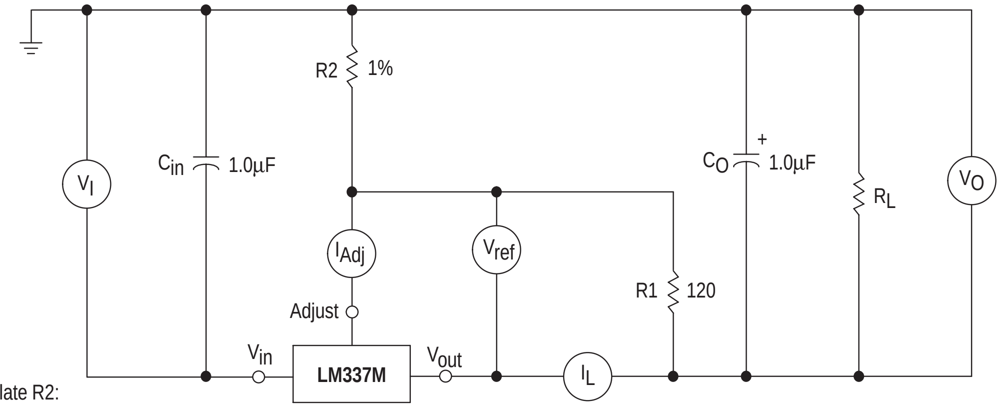


* Pulse Testing required:
1% Duty Cycle is suggested.

Load Regulation (mV) = V_O (min Load) – V_O (max Load)

$$\text{Load Regulation (\%/}V_O\text{)} = \frac{V_O \text{ (min Load)} - V_O \text{(max Load)}}{V_O \text{ (min Load)}} \times 100$$

Figure 3. Standard Test Circuit



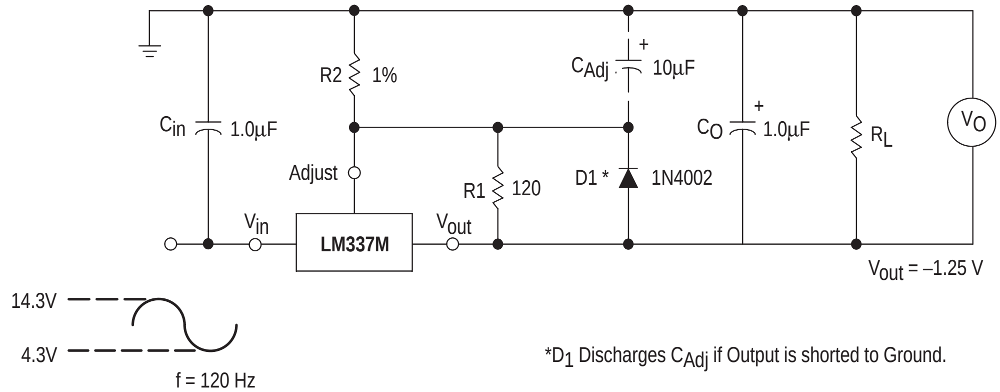
To Calculate R2:

$$R2 = \left(\frac{V_O}{V_{ref}} - 1\right) R_1$$

This assumes I_{Adj} is negligible.

Pulse Testing Required: 1% Duty Cycle is suggested.

Figure 4. Ripple Rejection Test Circuit



*D_1 Discharges C_{Adj} if Output is shorted to Ground.

Figure 5. Load Regulation

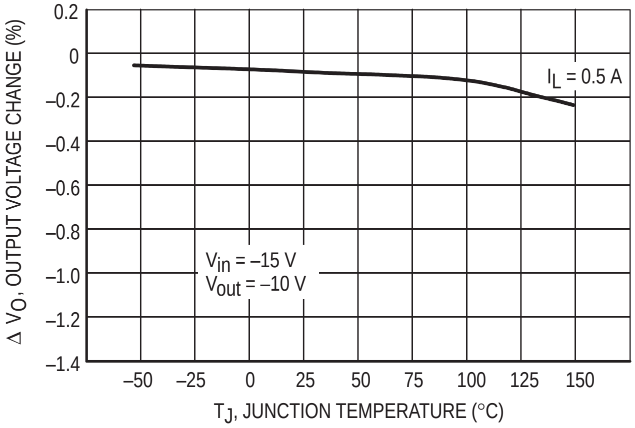


Figure 6. Current Limit

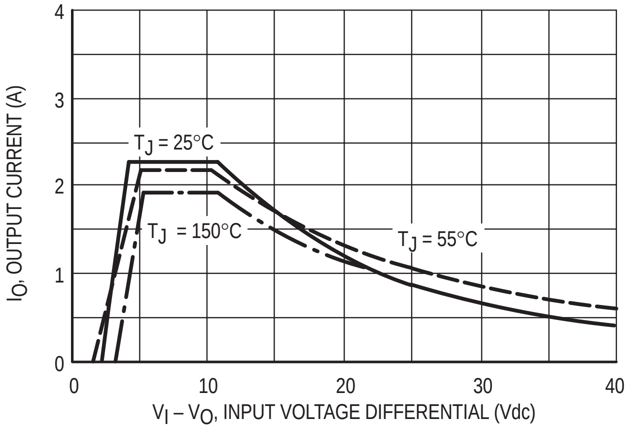


Figure 7. Adjustment Pin Current

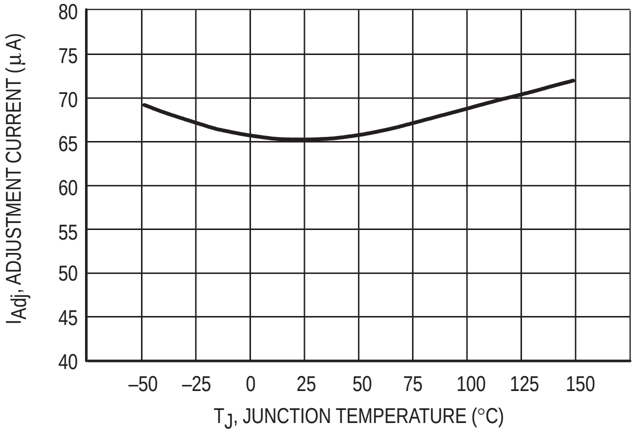


Figure 8. Dropout Voltage

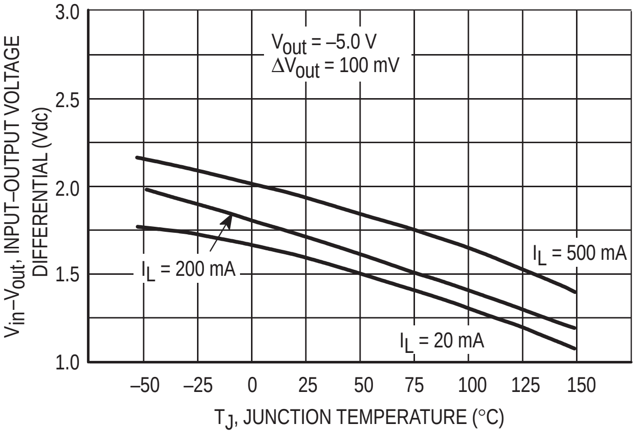


Figure 9. Temperature Stability

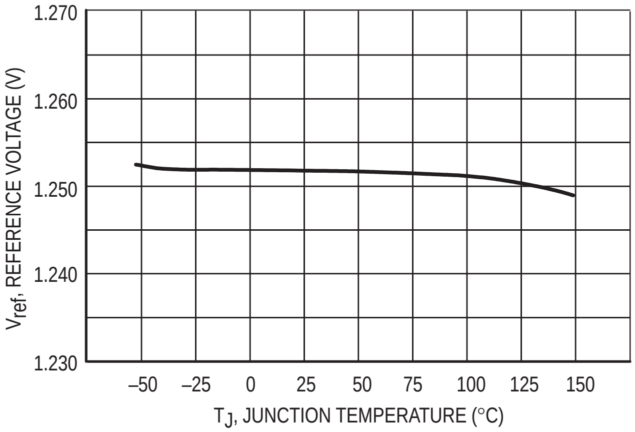


Figure 10. Minimum Operating Current

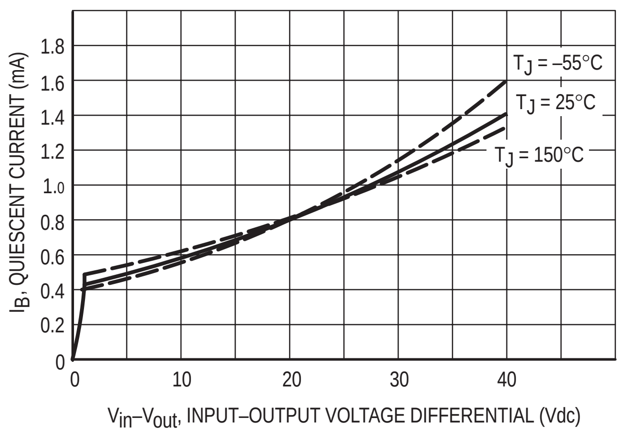


Figure 11. Ripple Rejection versus Output Voltage

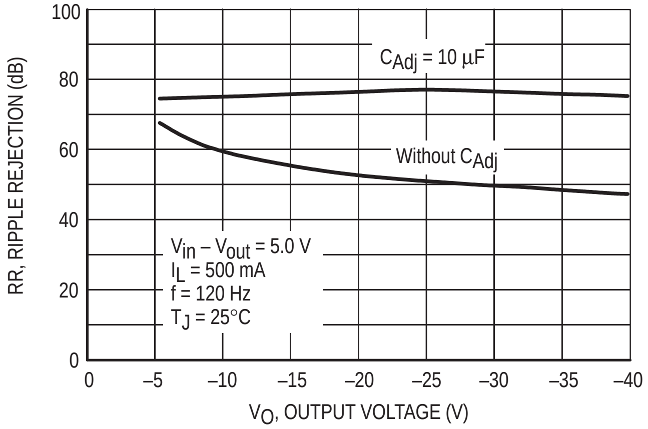


Figure 12. Ripple Rejection versus Output Current

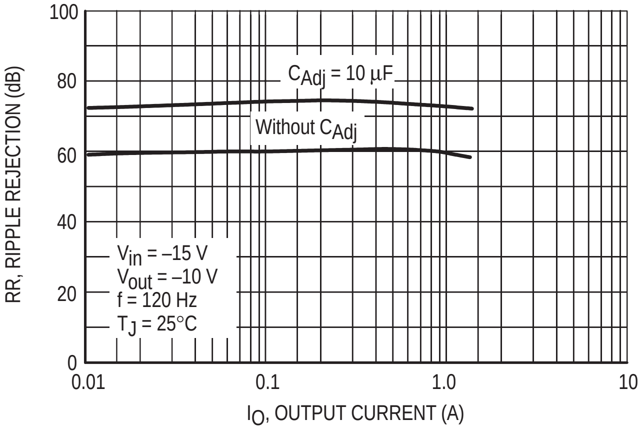


Figure 13. Ripple Rejection versus Frequency

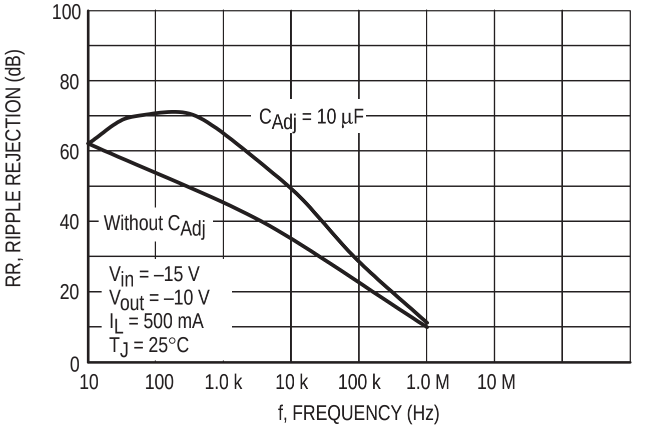


Figure 14. Output Impedance

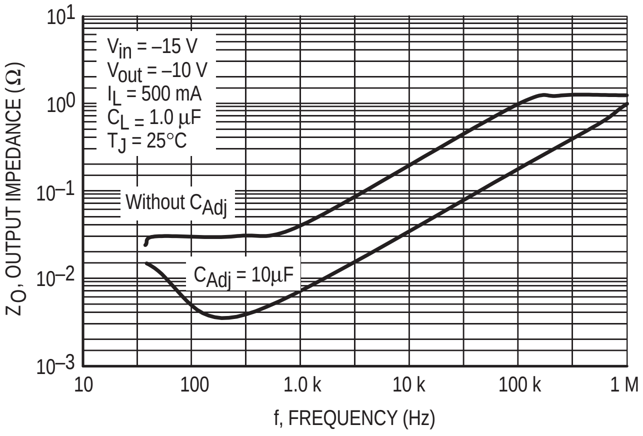


Figure 15. Line Transient Response

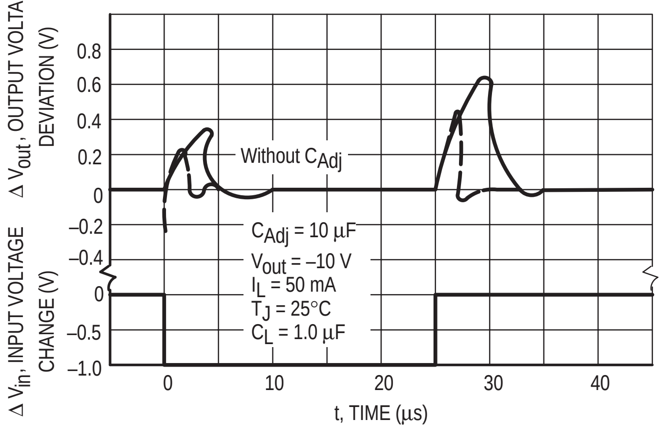
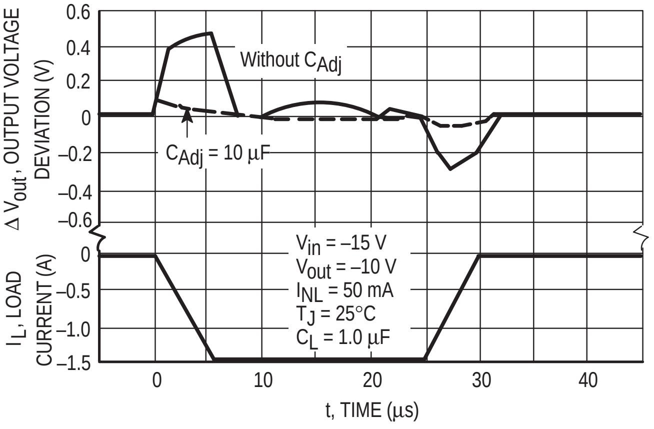


Figure 16. Load Transient Reponse



APPLICATIONS INFORMATION

Basic Circuit Operation

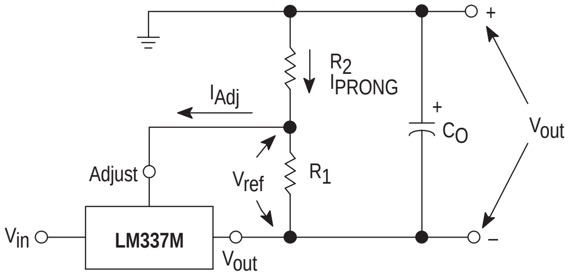
The LM337M is a three–terminal floating regulator. In operation, the LM337M develops and maintains a nominal –1.25 V reference (V_{ref}) between its output and adjustment terminals. This reference voltage is converted to a programming current (I_{PROG}) by R_1 (see Figure 17), and this constant current flows through R_2 to ground. The regulated output voltage is given by:

$$V_{out} = V_{ref} \left(1 + \frac{R_2}{R_1}\right) + I_{Adj} R_2$$

Since the current into the adjustment terminal (I_{Adj}) represents an error term in the equation, the LM337M was designed to control I_{Adj} to less than 100 µA and keep it constant. To do this, all quiescent operating current is returned to the output terminal. This imposes the requirement for a minimum load current. If the load current is less than this minimum, the output voltage will rise.

Since the LM337M is a floating regulator, it is only the voltage differential across the circuit which is important to performance, and operation at high voltages with respect to ground is possible.

Figure 17. Basic Circuit Configuration



V_{ref} = –1.25 V Typically

Load Regulation

The LM337M is capable of providing extremely good load regulation, but a few precautions are needed to obtain maximum performance. For best performance, the programming resistor (R_1) should be connected as close to the regulator as possible to minimize line drops which effectively appear in series with the reference, thereby degrading regulation. The ground end of R_2 can be returned near the load ground to provide remote ground sensing and improve load regulation.

External Capacitors

A 1.0 µF tantalum input bypass capacitor (C_{in}) is recommended to reduce the sensitivity to input line impedance.

The adjustment terminal may be bypassed to ground to improve ripple rejection. This capacitor (C_{Adj}) prevents ripple from being amplified as the output voltage is increased. A 10 µF capacitor should improve ripple rejection about 15 dB at 120 Hz in a 10 V application.

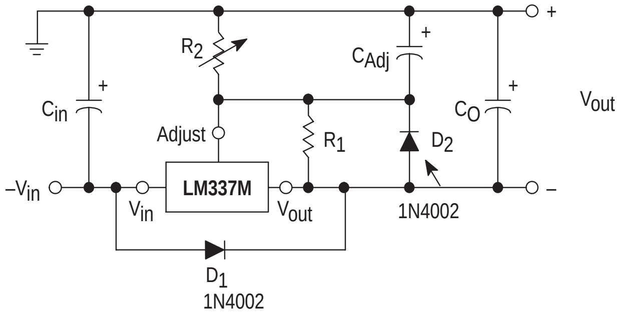
An output capacitance (C_O) in the form of a 1.0 µF tantalum or 10 µF aluminum electrolytic capacitor is required for stability.

Protection Diodes

When external capacitors are used with any IC regulator it is sometimes necessary to add protection diodes to prevent the capacitors from discharging through low current points into the regulator.

Figure 18 shows the LM337M with the recommended protection diodes for output voltages in excess of –25 V or high capacitance values (C_O > 25 µF, C_{Adj} > 10 µF). Diode D_1 prevents C_O from discharging thru the IC during an input short circuit. Diode D_2 protects against capacitor C_{Adj} discharging through the IC during an output short circuit. The combination of diodes D_1 and D_2 prevents C_{Adj} from discharging through the IC during an input short circuit.

Figure 18. Voltage Regulator with Protection Diodes



LM340, A Series

Three-Terminal Positive Fixed Voltage Regulators

This family of fixed voltage regulators are monolithic integrated circuits capable of driving loads in excess of 1.0 A. These three–terminal regulators employ internal current limiting, thermal shutdown, and safe–area compensation. Devices are available with improved specifications, including a 2% output voltage tolerance, on A–suffix 5.0, 12 and 15 V device types.

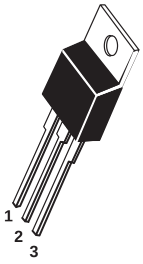
Although designed primarily as a fixed voltage regulator, these devices can be used with external components to obtain adjustable voltages and currents. This series of devices can be used with a series–pass transistor to boost output current capability at the nominal output voltage.

- Output Current in Excess of 1.0 A
- No External Components Required
- Output Voltage Offered in 2% and 4% Tolerance*
- Internal Thermal Overload Protection
- Internal Short Circuit Current Limiting
- Output Transistor Safe–Area Compensation

THREE–TERMINAL POSITIVE FIXED VOLTAGE REGULATORS

**SEMICONDUCTOR
TECHNICAL DATA**

T SUFFIX
PLASTIC PACKAGE
CASE 221A



Pin 1. Input
2. Ground
3. Output

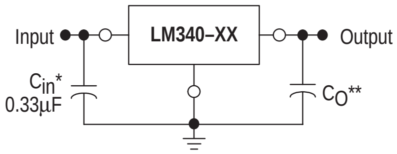
Heatsink surface is connected to Pin 2.

ORDERING INFORMATION

Device	Output Voltage and Tolerance	Operating Temperature Range	Package
LM340T–5.0	5.0 V ± 4%	T_J = 0° to +125°C	Plastic Power
LM340AT–5.0	5.0 V ± 2%		
LM340T–6.0	6.0 V ± 4%		
LM340T–8.0	8.0 V ± 4%		
LM340T–12	12 V ± 4%		
LM340AT–12	12 V ± 2%		
LM340T–15	15 V ± 4%		
LM340AT–15	15 V ± 2%		
LM340T–18	18 V ± 4%		
LM340T–24	24 V ± 4%		

* 2% regulators are available in 5, 12 and 15 V devices.

Simplified Application



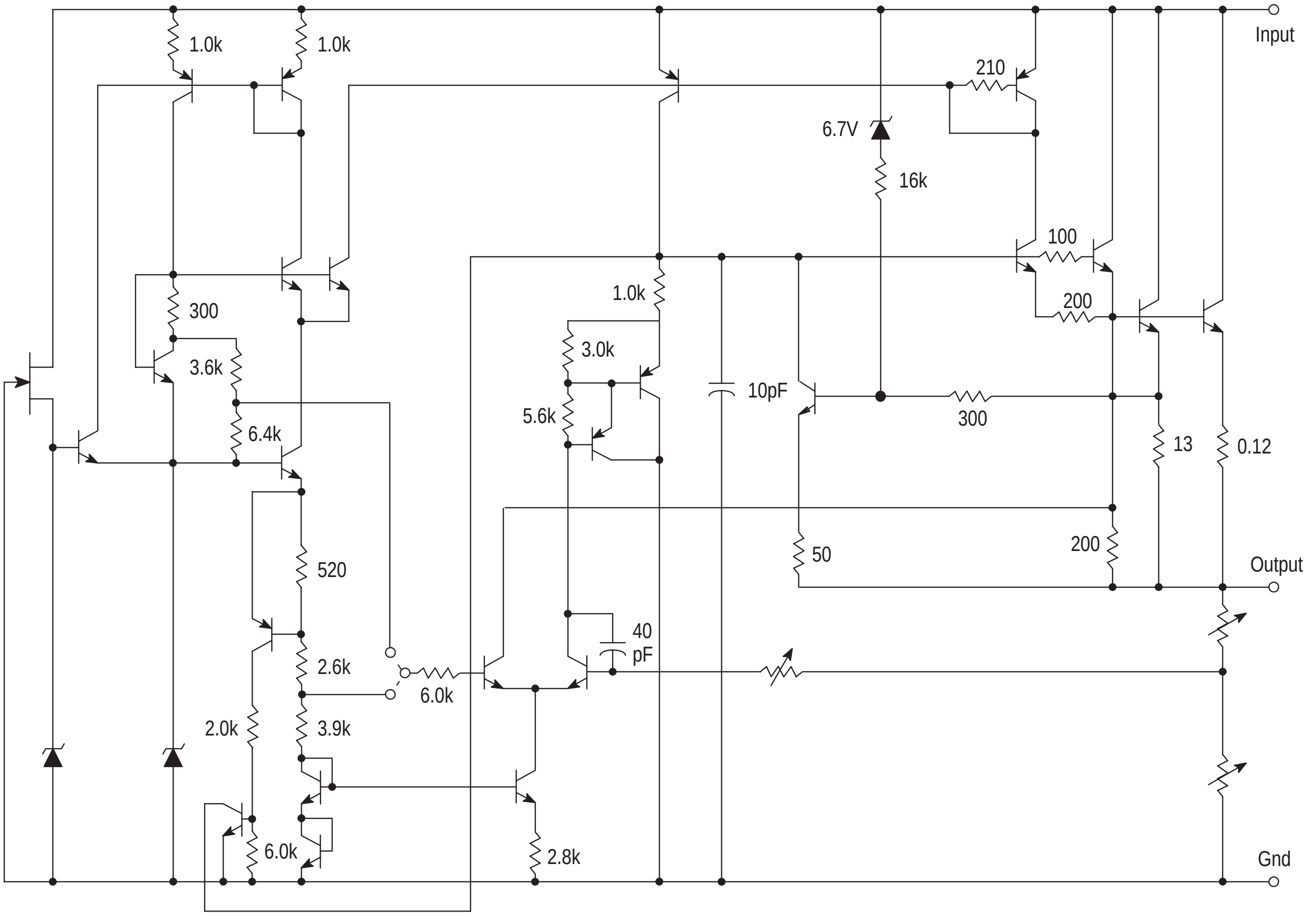
A common ground is required between the input and the output voltages. The input voltage must remain typically 1.7 V above the output voltage even during the low point on the input ripple voltage.

XX these two digits of the type number indicate voltage.
* C_{in} is required if regulator is located an appreciable distance from power supply filter.
** C_O is not needed for stability; however, it does improve transient response. If needed, use a 0.1 µF ceramic disc.

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Input Voltage (5.0 V – 18 V) (24 V)	V_{in}	35 40	Vdc
Power Dissipation and Thermal Characteristics			
Plastic Package			
T_A = +25°C	P_D	Internally Limited	W
Derate above T_A = +25°C	$1/\theta_{JA}$	15.4	mW/°C
Thermal Resistance, Junction–to–Air	θ_{JA}	65	°C/W
T_C= +25°C	P_D	Internally Limited	W
Derate above T_C = +75°C (See Figure 1)	$1/\theta_{JA}$	200	mW/°C
Thermal Resistance, Junction–to–Case	θ_{JC}	5.0	°C/W
Storage Temperature Range	T_{stg}	–65 to +150	°C
Operating Junction Temperature Range	T_J	0 to +150	°C

Representative Schematic Diagram



LM340–5.0

ELECTRICAL CHARACTERISTICS (V_{in} = 10 V, I_O = 500 mA, $T_J = T_{low}$ to T_{high} [Note 1], unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C) I_O = 5.0 mA to 1.0 A	V_O	4.8	5.0	5.2	Vdc
Line Regulation (Note 2)	Reg_{line}				mV
8.0 Vdc to 20 Vdc		–	–	50	
7.0 Vdc to 25 Vdc (T_J = +25°C)		–	–	50	
8.0 Vdc to 12 Vdc, I_O = 1.0 A		–	–	25	
7.3 Vdc to 20 Vdc, I_O = 1.0 A (T_J = +25°C)		–	–	50	
Load Regulation (Note 2)	Reg_{load}				mV
5.0 mA ≤ I_O ≤ 1.0 A		–	–	50	
5.0 mA ≤ I_O ≤ 1.5 A (T_J = +25°C)		–	–	50	
250 mA ≤ I_O ≤ 750 mA (T_J = +25°C)		–	–	25	
Output Voltage 7.0 ≤ V_{in} ≤ 20 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P_D ≤ 15 W	V_O	4.75	–	5.25	Vdc
Quiescent Current	I_B				mA
I_O = 1.0 A		–	–	8.5	
T_J = +25°C		–	4.0	8.0	
Quiescent Current Change	ΔI_B				mA
7.0 ≤ V_{in} ≤ 25 Vdc, I_O = 500 mA		–	–	1.0	
5.0 mA ≤ I_O ≤ 1.0 A, V_{in} = 10 V		–	–	0.5	
7.5 ≤ V_{in} ≤ 20 Vdc, I_O = 1.0 A		–	–	1.0	
Ripple Rejection I_O = 1.0 A (T_J = +25°C)	RR	62	80	–	dB
Dropout Voltage	$V_I - V_O$	–	1.7	–	Vdc
Output Resistance (f = 1.0 kHz)	r_O	–	2.0	–	mΩ
Short Circuit Current Limit (T_J = +25°C)	I_{SC}	–	2.0	–	A
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	–	40	–	µV
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA	TCV_O	–	±0.6	–	mV/°C
Peak Output Current (T_J = +25°C)	I_O	–	2.4	–	A
Input Voltage to Maintain Line Regulation (T_J = +25°C) I_O = 1.0 A		7.3	–	–	Vdc

NOTES: 1. T_{low} to T_{high} = 0° to +125°C
2. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

DEFINITIONS

Line Regulation – The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

Load Regulation – The change in output voltage for a change in load current at constant chip temperature.

Maximum Power Dissipation – The maximum total device dissipation for which the regulator will operate within specifications.

Quiescent Current – That part of the input current that is not delivered to the load.

Output Noise Voltage – The rms AC voltage at the output, with constant load and no input ripple, measured over a specified frequency range.

LM340A–5.0

ELECTRICAL CHARACTERISTICS (V_{in} = 10 V, I_O = 1.0 A, T_J = T_{low} to T_{high} [Note 1], unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C) I_O = 5.0 mA to 1.0 A	V_O	4.9	5.0	5.1	Vdc
Line Regulation	Reg_{line}				mV
7.5 Vdc to 20 Vdc, I_O = 500 mA		–	–	10	
7.3 Vdc to 25 Vdc (T_J = +25°C)		–	3.0	10	
8.0 Vdc to 12 Vdc		–	–	12	
8.0 Vdc to 12 Vdc (T_J = +25°C)		–	–	4.0	
Load Regulation	Reg_{load}				mV
5.0 mA ≤ I_O ≤ 1.0 A		–	–	25	
5.0 mA ≤ I_O ≤ 1.5 A (T_J = +25°C)		–	–	25	
250 mA ≤ I_O ≤ 750 mA (T_J = +25°C)		–	–	15	
Output Voltage 7.5 ≤ V_{in} ≤ 20 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P_D ≤ 15 W	V_O	4.8	–	5.2	Vdc
Quiescent Current	I_B	–	–	6.5	mA
T_J = +25°C		–	3.5	6.0	
Quiescent Current Change	ΔI_B				mA
5.0 mA ≤ I_O ≤ 1.0 A, V_{in} = 10 V		–	–	0.5	
8.0 ≤ V_{in} ≤ 25 Vdc, I_O = 500 mA		–	–	0.8	
7.5 ≤ V_{in} ≤ 20 Vdc, I_O = 1.0 A (T_J = +25°C)		–	–	0.8	
Ripple Rejection 8.0 ≤ V_{in} ≤ 18 Vdc, f = 120 Hz	RR				dB
I_O = 500 mA		68	–	–	
I_O = 1.0 A (T_J = +25°C)		68	80	–	
Dropout Voltage	$V_I – V_O$	–	1.7	–	Vdc
Output Resistance (f = 1.0 kHz)	r_O	–	2.0	–	mΩ
Short Circuit Current Limit (T_J = +25°C)	I_{SC}	–	2.0	–	A
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	–	40	–	µV
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA	TCV_O	–	±0.6	–	mV/°C
Peak Output Current (T_J = +25°C)	I_O	–	2.4	–	A
Input Voltage to Maintain Line Regulation (T_J = +25°C) I_O = 1.0 A		7.3	–	–	Vdc

NOTE: 1. T_{low} to T_{high} = 0° to +125°C

LM340–6.0
ELECTRICAL CHARACTERISTICS (V_{in} = 11 V, I_O = 500 mA, $T_J = T_{low}$ to T_{high} [Note 1], unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C) I_O = 5.0 mA to 1.0 A	V_O	5.75	6.0	6.25	Vdc
Line Regulation	Reg_{line}				mV
9.0 Vdc to 21 Vdc		–	–	60	
8.0 Vdc to 25 Vdc (T_J = +25°C)		–	–	60	
9.0 Vdc to 13 Vdc, I_O = 1.0 A		–	–	30	
8.3 Vdc to 21 Vdc, I_O = 1.0 A (T_J = +25°C)		–	–	60	
Load Regulation	Reg_{load}				mV
5.0 mA ≤ I_O ≤ 1.0 A		–	–	60	
5.0 mA ≤ I_O ≤ 1.5 A (T_J = +25°C)		–	–	60	
250 mA ≤ I_O ≤ 750 mA (T_J = +25°C)		–	–	30	
Output Voltage 8.0 ≤ V_{in} ≤ 21 Vdc, 6.0 mA ≤ I_O ≤ 1.0 A, P_D ≤ 15 W	V_O	5.7	–	6.3	Vdc
Quiescent Current	I_B				mA
I_O = 1.0 A		–	–	8.5	
T_J = +25°C		–	4.0	8.0	
Quiescent Current Change	ΔI_B				mA
8.0 ≤ V_{in} ≤ 25 Vdc, I_O = 500 mA		–	–	1.0	
5.0 mA ≤ I_O ≤ 1.0 A, V_{in} = 11 V		–	–	0.5	
8.6 ≤ V_{in} ≤ 21 Vdc, I_O = 1.0 A		–	–	1.0	
Ripple Rejection I_O = 1.0 A (T_J = +25°C)	RR	59	78	–	dB
Dropout Voltage	$V_I – V_O$	–	1.7	–	Vdc
Output Resistance (f = 1.0 kHz)	r_O	–	2.0	–	mΩ
Short Circuit Current Limit (T_J = +25°C)	I_{SC}	–	1.9	–	A
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	–	45	–	µV
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA	TCV_O	–	±0.7	–	mV/°C
Peak Output Current (T_J = +25°C)	I_O	–	2.4	–	A
Input Voltage to Maintain Line Regulation (T_J = +25°C) I_O = 1.0 A		8.3	–	–	Vdc

NOTE: 1. T_{low} to T_{high} = 0° to +125°C

LM340–8.0

ELECTRICAL CHARACTERISTICS (V_{in} = 14 V, I_O = 500 mA, T_J = T_{low} to T_{high} [Note 1], unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C) I_O = 5.0 mA to 1.0 A	V_O	7.7	8.0	8.3	Vdc
Line Regulation	Reg_{line}				mV
11 Vdc to 23 Vdc		–	–	80	
10.5 Vdc to 25 Vdc (T_J = +25°C)		–	–	80	
11 Vdc to 17 Vdc, I_O = 1.0 A		–	–	40	
10.5 Vdc to 23 Vdc, I_O = 1.0 A (T_J = +25°C)		–	–	80	
Load Regulation	Reg_{load}				mV
5.0 mA ≤ I_O ≤ 1.0 A		–	–	80	
5.0 mA ≤ I_O ≤ 1.5 A (T_J = +25°C)		–	–	80	
250 mA ≤ I_O ≤ 750 mA (T_J = +25°C)		–	–	40	
Output Voltage 10.5 ≤ V_{in} ≤ 23 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P_D ≤ 15 W	V_O	7.6	–	8.4	Vdc
Quiescent Current	I_B				mA
I_O = 1.0 A		–	–	8.5	
T_J = +25°C		–	4.0	8.0	
Quiescent Current Change	ΔI_B				mA
10.5 ≤ V_{in} ≤ 25 Vdc, I_O = 500 mA		–	–	1.0	
5.0 mA ≤ I_O ≤ 1.0 A, V_{in} = 14 V		–	–	0.5	
10.6 ≤ V_{in} ≤ 23 Vdc, I_O = 1.0 A		–	–	1.0	
Ripple Rejection I_O = 1.0 A (T_J = +25°C)	RR	56	76	–	dB
Dropout Voltage	$V_I – V_O$	–	1.7	–	Vdc
Output Resistance (f = 1.0 kHz)	r_O	–	2.0	–	mΩ
Short Circuit Current Limit (T_J = +25°C)	I_{SC}	–	1.5	–	A
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	–	52	–	µV
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA	TCV_O	–	±1.0	–	mV/°C
Peak Output Current (T_J = +25°C)	I_O	–	2.4	–	A
Input Voltage to Maintain Line Regulation (T_J = +25°C) I_O = 1.0 A		10.5	–	–	Vdc

NOTE: 1. T_{low} to T_{high} = 0° to +125°C

LM340–12

ELECTRICAL CHARACTERISTICS (V_{in} = 19 V, I_O = 500 mA, T_J = T_{low} to T_{high} [Note 1], unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C) I_O = 5.0 mA to 1.0 A	V_O	11.5	12	12.5	Vdc
Line Regulation (Note 2)	Reg_{line}				mV
15 Vdc to 27 Vdc		–	–	120	
14.6 Vdc to 30 Vdc (T_J = +25°C)		–	–	120	
16 Vdc to 22 Vdc, I_O = 1.0 A		–	–	60	
14.6 Vdc to 27 Vdc, I_O = 1.0 A (T_J = +25°C)		–	–	120	
Load Regulation (Note 2)	Reg_{load}				mV
5.0 mA ≤ I_O ≤ 1.0 A		–	–	120	
5.0 mA ≤ I_O ≤ 1.5 A (T_J = +25°C)		–	–	120	
250 mA ≤ I_O ≤ 750 mA (T_J = +25°C)		–	–	60	
Output Voltage 14.5 ≤ V_{in} ≤ 27 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P_D ≤ 15 W	V_O	11.4	–	12.6	Vdc
Quiescent Current	I_B				mA
I_O = 1.0 A		–	–	8.5	
T_J = +25°C		–	4.0	8.0	
Quiescent Current Change	ΔI_B				mA
14.5 ≤ V_{in} ≤ 30 Vdc, I_O = 500 mA		–	–	1.0	
5.0 mA ≤ I_O ≤ 1.0 A, V_{in} = 19 V		–	–	0.5	
14.8 ≤ V_{in} ≤ 27 Vdc, I_O = 1.0 A		–	–	1.0	
Ripple Rejection I_O = 1.0 A (T_J = +25°C)	RR	55	72	–	dB
Dropout Voltage	$V_I – V_O$	–	1.7	–	Vdc
Output Resistance (f = 1.0 kHz)	r_O	–	2.0	–	mΩ
Short Circuit Current Limit (T_J = +25°C)	I_{SC}	–	1.1	–	A
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	–	75	–	µV
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA	TCV_O	–	±1.5	–	mV/°C
Peak Output Current (T_J = +25°C)	I_O	–	2.4	–	A
Input Voltage to Maintain Line Regulation (T_J = +25°C) I_O = 1.0 A		14.6	–	–	Vdc

NOTES: 1. T_{low} to T_{high} = 0° to +125°C
2. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

LM340A–12

ELECTRICAL CHARACTERISTICS (V_{in} = 19 V, I_O = 1.0 mA, T_J = T_{low} to T_{high} [Note 1], unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C) I_O = 5.0 mA to 1.0 A	V_O	11.75	12	12.25	Vdc
Line Regulation	Reg_{line}				mV
14.8 Vdc to 27 Vdc, I_O = 500 mA		–	–	18	
14.5 Vdc to 30 Vdc (T_J = +25°C)		–	4.0	18	
16 Vdc to 22 Vdc		–	–	30	
16 Vdc to 22 Vdc (T_J = +25°C)		–	–	9.0	
Load Regulation	Reg_{load}				mV
5.0 mA ≤ I_O ≤ 1.0 A		–	–	60	
5.0 mA ≤ I_O ≤ 1.5 A (T_J = +25°C)		–	–	32	
250 mA ≤ I_O ≤ 750 mA (T_J = +25°C)		–	–	19	
Output Voltage 14.8 ≤ V_{in} ≤ 27 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P_D ≤ 15 W	V_O	11.5	–	12.5	Vdc
Quiescent Current	I_B	–	–	6.5	mA
T_J = +25°C		–	3.5	6.0	
Quiescent Current Change	ΔI_B				mA
5.0 mA ≤ I_O ≤ 1.0 A, V_{in} = 19 V		–	–	0.5	
15 ≤ V_{in} ≤ 30 Vdc, I_O = 500 mA		–	–	0.8	
14.8 ≤ V_{in} ≤ 27 Vdc, I_O = 1.0 A(T_J = +25°C)		–	–	0.8	
Ripple Rejection 15 ≤ V_{in} ≤ 25 Vdc, f = 120 Hz	RR				dB
I_O = 500 mA		61	–	–	
I_O = 1.0 A (T_J = +25°C)		61	72	–	
Dropout Voltage	$V_I – V_O$	–	1.7	–	Vdc
Output Resistance (f = 1.0 kHz)	r_O	–	2.0	–	mΩ
Short Circuit Current Limit (T_J = +25°C)	I_{SC}	–	1.1	–	A
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	–	75	–	µV
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA	TCV_O	–	±1.5	–	mV/°C
Peak Output Current (T_J = +25°C)	I_O	–	2.4	–	A
Input Voltage to Maintain Line Regulation (T_J = +25°C)		14.5	–	–	Vdc

NOTE: 1. T_{low} to T_{high} = 0° to +125°C

LM340–15

ELECTRICAL CHARACTERISTICS (V_{in} = 23 V, I_O = 500 mA, T_J = T_{low} to T_{high} [Note 1], unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C) I_O = 5.0 mA to 1.0 A	V_O	14.4	15	15.6	Vdc
Line Regulation (Note 2)	Reg_{line}				mV
18.5 Vdc to 30 Vdc		–	–	150	
17.5 Vdc to 30 Vdc (T_J = +25°C)		–	–	150	
20 Vdc to 26 Vdc, I_O = 1.0 A		–	–	75	
17.7 Vdc to 30 Vdc, I_O = 1.0 A (T_J = +25°C)		–	–	150	
Load Regulation (Note 2)	Reg_{load}				mV
5.0 mA ≤ I_O ≤ 1.0 A		–	–	150	
5.0 mA ≤ I_O ≤ 1.5 A (T_J = +25°C)		–	–	150	
250 mA ≤ I_O ≤ 750 mA (T_J = +25°C)		–	–	75	
Output Voltage 17.5 ≤ V_{in} ≤ 30 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P_D ≤ 15 W	V_O	14.25	–	15.75	Vdc
Quiescent Current	I_B				mA
I_O = 1.0 A		–	–	8.5	
T_J = +25°C		–	4.0	8.0	
Quiescent Current Change	ΔI_B				mA
17.5 ≤ V_{in} ≤ 30 Vdc, I_O = 500 mA		–	–	1.0	
5.0 mA ≤ I_O ≤ 1.0 A, V_{in} = 23 V		–	–	0.5	
17.9 ≤ V_{in} ≤ 30 Vdc, I_O = 1.0 A		–	–	1.0	
Ripple Rejection I_O = 1.0 mA (T_J = +25°C)	RR	54	70	–	dB
Dropout Voltage	$V_I – V_O$	–	1.7	–	Vdc
Output Resistance (f = 1.0 kHz)	r_O	–	2.0	–	mΩ
Short Circuit Current Limit (T_J = +25°C)	I_{SC}	–	800	–	A
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	–	90	–	µV
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA	TCV_O	–	±1.8	–	mV/°C
Peak Output Current (T_J = +25°C)	I_O	–	2.4	–	A
Input Voltage to Maintain Line Regulation (T_J = +25°C) I_O = 1.0 A		17.7	–	–	Vdc

NOTES: 1. T_{low} to T_{high} = 0° to +125°C
2. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

LM340A–15

ELECTRICAL CHARACTERISTICS (V_{in} = 23 V, I_O = 1.0 mA, $T_J = T_{low}$ to T_{high} [Note 1], unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C) I_O = 5.0 mA to 1.0 A	V_O	14.7	15	15.3	Vdc
Line Regulation	Reg_{line}				mV
17.9 Vdc to 30 Vdc, I_O = 500 mA		–	–	22	
17.5 Vdc to 30 Vdc (T_J = +25°C)		–	4.0	22	
20 Vdc to 26 Vdc, I_O = 1.0 A		–	–	30	
20 Vdc to 26 Vdc, I_O = 1.0 A (T_J = +25°C)		–	–	10	
Load Regulation	Reg_{load}				mV
5.0 mA ≤ I_O ≤ 1.0 A		–	–	75	
5.0 mA ≤ I_O ≤ 1.5 A (T_J = +25°C)		–	12	35	
250 mA ≤ I_O ≤ 750 mA (T_J = +25°C)		–	–	21	
Output Voltage 17.9 ≤ V_{in} ≤ 30 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P_D ≤ 15 W	V_O	14.4	–	15.6	Vdc
Quiescent Current	I_B	–	–	6.5	mA
T_J = +25°C		–	3.5	6.0	
Quiescent Current Change	ΔI_B				mA
5.0 mA ≤ I_O ≤ 1.0 A, V_{in} = 23 V		–	–	0.5	
17.9 ≤ V_{in} ≤ 30 Vdc, I_O = 500 mA		–	–	0.8	
17.9 ≤ V_{in} ≤ 30 Vdc, I_O = 1.0 A (T_J = +25°C)		–	–	0.8	
Ripple Rejection 18.5 ≤ V_{in} ≤ 28.5 Vdc, f = 120 Hz	RR				dB
I_O = 500 mA		60	–	–	
I_O = 1.0 A (T_J = +25°C)		60	70	–	
Dropout Voltage	$V_I - V_O$	–	1.7	–	Vdc
Output Resistance (f = 1.0 kHz)	r_O	–	2.0	–	mΩ
Short Circuit Current Limit (T_J = +25°C)	I_{SC}	–	800	–	A
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	–	90	–	µV
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA	TCV_O	–	±1.8	–	mV/°C
Peak Output Current (T_J = +25°C)	I_O	–	2.4	–	A
Input Voltage to Maintain Line Regulation (T_J = +25°C)		17.5	–	–	Vdc

NOTE: 1. T_{low} to T_{high} = 0° to +125°C

LM340–18

ELECTRICAL CHARACTERISTICS (V_{in} = 27 V, I_O = 500 mA, T_J = T_{low} to T_{high} [Note 1], unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C) I_O = 5.0 mA to 1.0 A	V_O	17.3	18	18.7	Vdc
Line Regulation	Reg_{line}				mV
21.5 Vdc to 33 Vdc		–	–	180	
21 Vdc to 33 Vdc (T_J = +25°C)		–	–	180	
24 Vdc to 30 Vdc, I_O = 1.0 A		–	–	90	
21 Vdc to 33 Vdc, I_O = 1.0 A (T_J = +25°C)		–	–	180	
Load Regulation	Reg_{load}				mV
5.0 mA ≤ I_O ≤ 1.0 A		–	–	180	
5.0 mA ≤ I_O ≤ 1.5 A (T_J = +25°C)		–	–	180	
250 mA ≤ I_O ≤ 750 mA (T_J = +25°C)		–	–	90	
Output Voltage 21 ≤ V_{in} ≤ 33 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P_D ≤ 15 W	V_O	17.1	–	18.9	Vdc
Quiescent Current	I_B				mA
I_O = 1.0 A		–	–	8.5	
T_J = +25°C		–	4.0	8.0	
Quiescent Current Change	ΔI_B				mA
21 ≤ V_{in} ≤ 33 Vdc, I_O = 500 mA		–	–	1.0	
5.0 mA ≤ I_O ≤ 1.0 A, V_{in} = 27 V		–	–	0.5	
21 ≤ V_{in} ≤ 33 Vdc, I_O = 1.0 A		–	–	1.0	
Ripple Rejection I_O = 1.0 mA (T_J = +25°C)	RR	53	69	–	dB
Dropout Voltage	$V_I - V_O$	–	1.7	–	Vdc
Output Resistance (f = 1.0 kHz)	r_O	–	2.0	–	mΩ
Short Circuit Current Limit (T_J = +25°C)	I_{SC}	–	500	–	A
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	–	110	–	µV
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA	TCV_O	–	±2.3	–	mV/°C
Peak Output Current (T_J = +25°C)	I_O	–	2.4	–	A
Input Voltage to Maintain Line Regulation (T_J = +25°C) I_O = 1.0 A		21	–	–	Vdc

NOTE: 1. T_{low} to T_{high} = 0° to +125°C

LM340–24

ELECTRICAL CHARACTERISTICS (V_{in} = 33 V, I_O = 500 mA, T_J = T_{low} to T_{high} [Note 1], unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C) I_O = 5.0 mA to 1.0 A	V_O	23	24	25	Vdc
Line Regulation	Reg_{line}				mV
28 Vdc to 38 Vdc		–	–	240	
27 Vdc to 38 Vdc (T_J = +25°C)		–	–	240	
30 Vdc to 36 Vdc, I_O = 1.0 A		–	–	120	
27.1 Vdc to 38 Vdc, I_O = 1.0 A (T_J = +25°C)		–	–	240	
Load Regulation	Reg_{load}				mV
5.0 mA ≤ I_O ≤ 1.0 A		–	–	240	
5.0 mA ≤ I_O ≤ 1.5 A (T_J = +25°C)		–	–	240	
250 mA ≤ I_O ≤ 750 mA (T_J = +25°C)		–	–	120	
Output Voltage 27 ≤ V_{in} ≤ 38 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P_D ≤ 15 W	V_O	22.8	–	25.2	Vdc
Quiescent Current	I_B				mA
I_O = 1.0 A		–	–	8.5	
T_J = +25°C		–	4.0	8.0	
Quiescent Current Change	ΔI_B				mA
27 ≤ V_{in} ≤ 38 Vdc, I_O = 500 mA		–	–	1.0	
5.0 mA ≤ I_O ≤ 1.0 A, V_{in} = 33 V		–	–	0.5	
27.3 ≤ V_{in} ≤ 38 Vdc, I_O = 1.0 A		–	–	1.0	
Ripple Rejection I_O = 1.0 mA (T_J = +25°C)	RR	50	66	–	dB
Dropout Voltage	$V_I - V_O$	–	1.7	–	Vdc
Output Resistance (f = 1.0 kHz)	r_O	–	2.0	–	mΩ
Short Circuit Current Limit (T_J = +25°C)	I_{SC}	–	200	–	A
Output Noise Voltage (T_A = +25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	–	170	–	µV
Average Temperature Coefficient of Output Voltage I_O = 5.0 m_A	TCV_O	–	±3.0	–	mV/°C
Peak Output Current (T_J = +25°C)	I_O	–	2.4	–	A
Input Voltage to Maintain Line Regulation (T_J = +25°C) I_O = 1.0 A		27.1	–	–	Vdc

NOTE: 1. T_{low} to T_{high} = 0° to +125°C

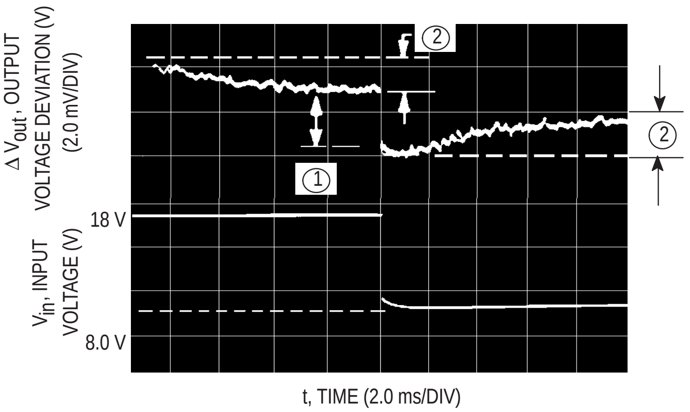
VOLTAGE REGULATOR PERFORMANCE

The performance of a voltage regulator is specified by its immunity to changes in load, input voltage, power dissipation, and temperature. Line and load regulation are tested with a pulse of short duration (< 100 μs) and are strictly a function of electrical gain. However, pulse widths of longer duration (> 1.0 ms) are sufficient to affect temperature gradients across the die. These temperature gradients can cause a change in the output voltage, in addition to changes caused by line and load regulation. Longer pulse widths and thermal gradients make it desirable to specify thermal regulation.

Thermal regulation is defined as the change in output voltage caused by a change in dissipated power for a specified time, and is expressed as a percentage output voltage change per watt. The change in dissipated power can be caused by a change in either input voltage or the load current. Thermal regulation is a function of IC layout and die attach techniques, and usually occurs within 10 ms of a change in power dissipation. After 10 ms, additional changes in the output voltage are due to the temperature coefficient of the device.

Figure 1 shows the line and thermal regulation response of a typical LM340AT–5.0 to a 10 W input pulse. The variation of the output voltage due to line regulation is labeled À and the thermal regulation component is labeled Á. Figure 2 shows the load and thermal regulation response of a typical LM340AT–5.0 to a 15 W load pulse. The output voltage variation due to load regulation is labeled À and the thermal regulation component is labeled Á.

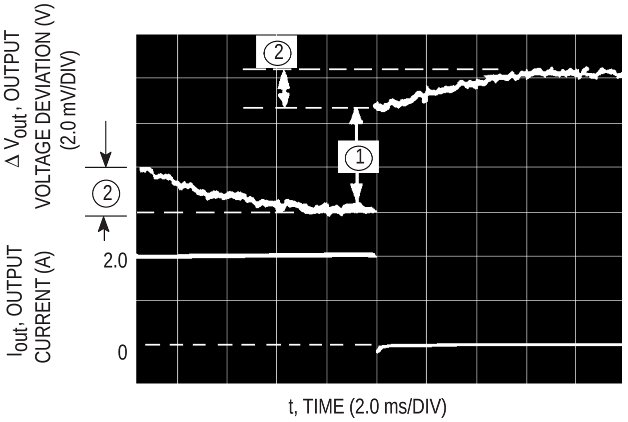
Figure 1. Line and Thermal Regulation



LM340AT–5.0
V_{out} = 5.0 V
V_{in} = 8.0 V → 18 V → 8.0 V
I_{out} = 1.0 A

① = Reg_{line} = 2.4 mV
② = Reg_{therm} = 0.0030% V_O/W

Figure 2. Load and Thermal Regulation



LM340AT–5.0
V_{out} = 5.0 V
V_{in} = 15 V
I_{out} = 0 A → 1.5 A → 0 A

① = Reg_{line} = 4.4 mV
② = Reg_{therm} = 0.0020% V_O/W

Figure 3. Temperature Stability

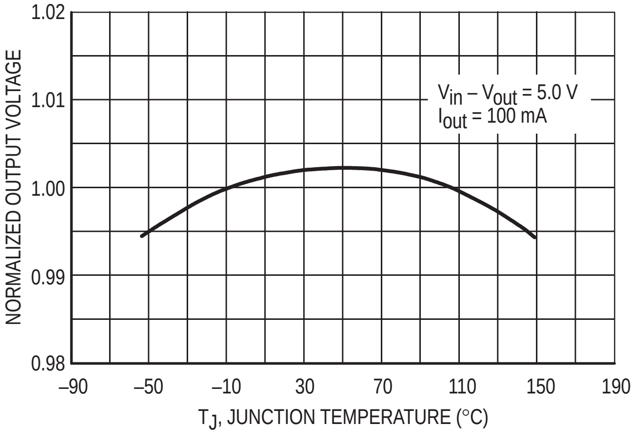


Figure 4. Output Impedance

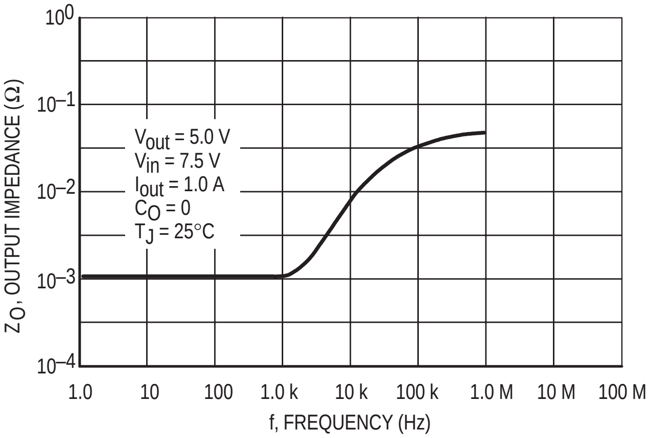


Figure 5. Ripple Rejection versus Frequency

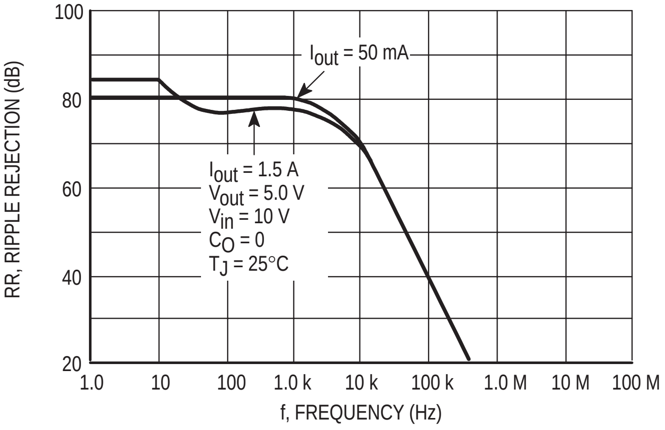


Figure 6. Ripple Rejection versus Output Current

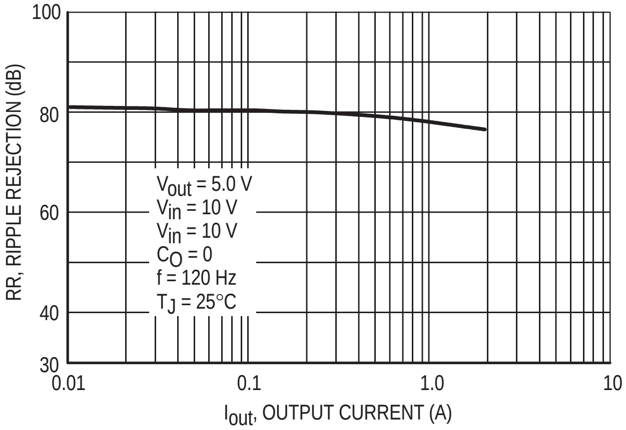


Figure 7. Quiescent Current versus Input Voltage

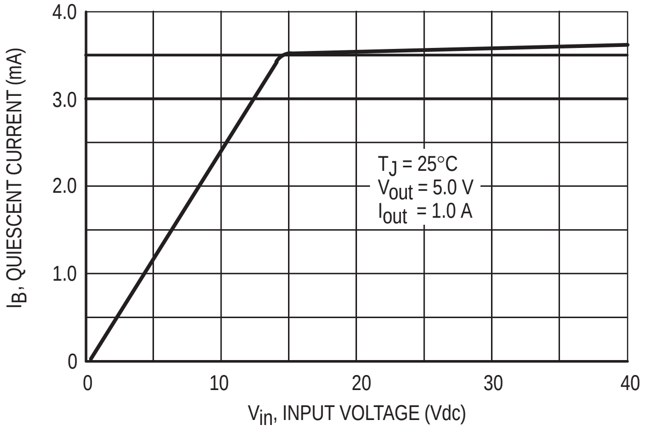


Figure 8. Quiescent Current versus Output Current

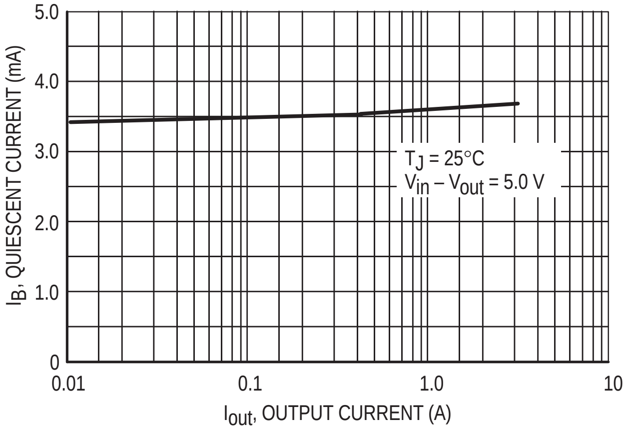


Figure 9. Dropout Voltage

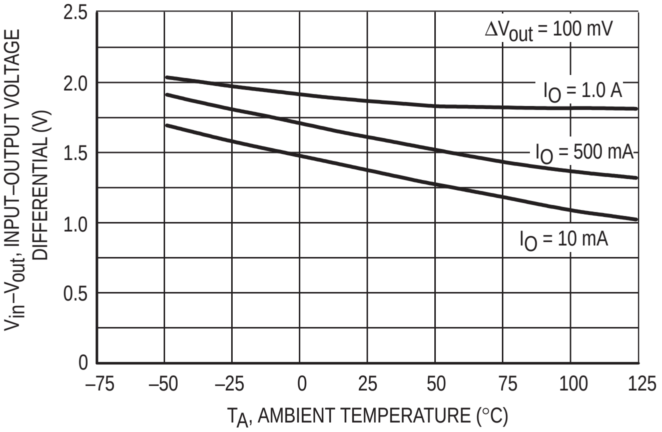


Figure 10. Peak Output Current

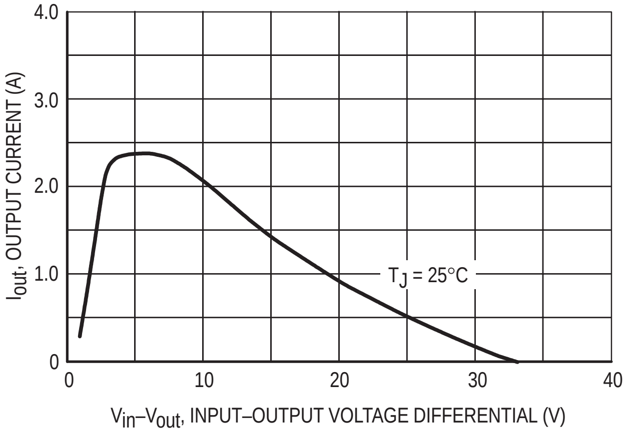


Figure 11. Line Transient Response

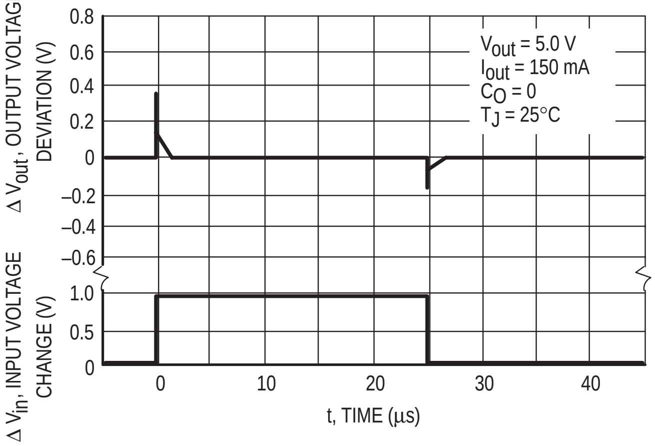


Figure 12. Load Transient Response

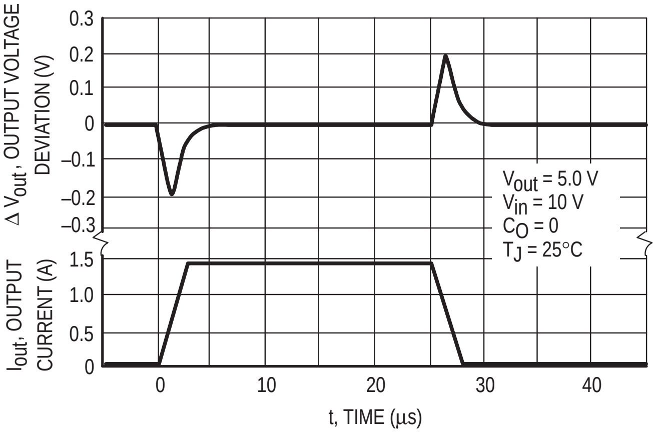
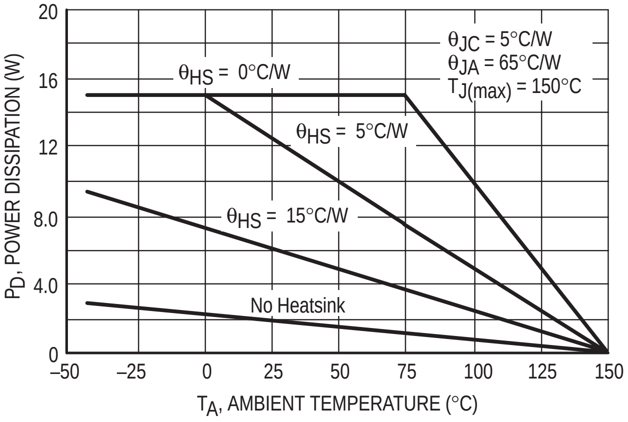


Figure 13. Worst Case Power Dissipation versus Ambient Temperature (Case 221A)



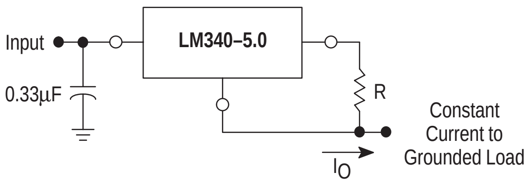
APPLICATIONS INFORMATION

Design Considerations

The LM340, A series of fixed voltage regulators are designed with Thermal Overload Protection that shuts down the circuit when subjected to an excessive power overload condition, Internal Short Circuit Protection that limits the maximum current the circuit will pass, and Output Transistor Safe–Area Compensation that reduces the output short circuit current as the voltage across the pass transistor is increased.

In many low current applications, compensation capacitors are not required. However, it is recommended that the regulator input be bypassed with a capacitor if the regulator is connected to the power supply filter with long wire lengths, or if the output load capacitance is large. An input bypass capacitor should be selected to provide good high–frequency characteristics to insure stable operation under all load conditions. A 0.33 µF or larger tantalum, mylar, or other capacitor having low internal impedance at high frequencies should be chosen. The bypass capacitor should be mounted with the shortest possible leads directly across the regulators input terminals. Normally good construction techniques should be used to minimize ground loops and lead resistance drops since the regulator has no external sense lead.

Figure 14. Current Regulator



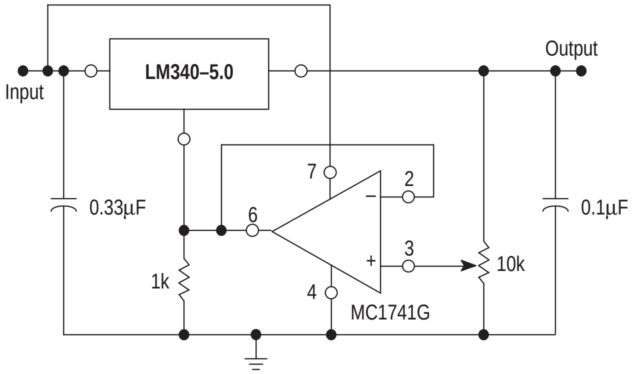
These regulators can also be used as a current source when connected as above. In order to minimize dissipation the LM340–5.0 is chosen in this application. Resistor R determines the current as follows:

$$I_O = \frac{5.0\ V}{R} + I_Q$$

$I_Q \cong$ 1.5 mA over line and load changes

For example, a 1 A current source would require R to be a 5 Ω, 10 W resistor and the output voltage compliance would be the input voltage less 7.0 V.

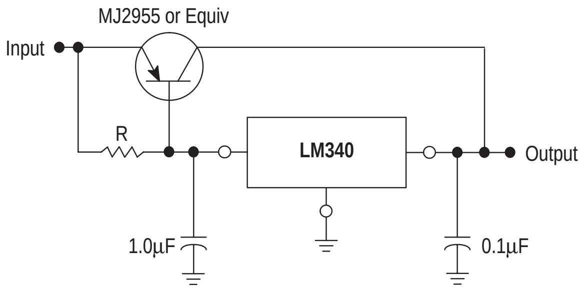
Figure 15. Adjustable Output Regulator



V_{out}, 7.0 V to 20 V
$V_{in} - V_O \geq 2.0$ V

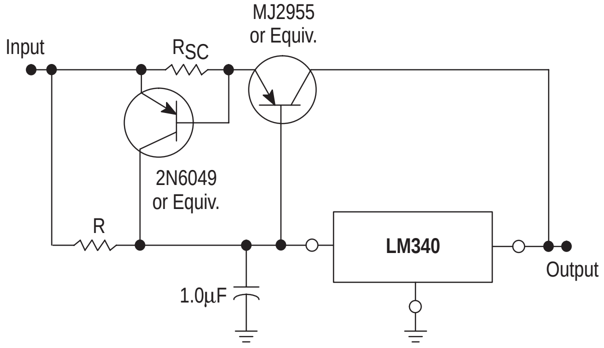
The addition of an operational amplifier allows adjustment to higher or intermediate values while retaining regulation characteristics. The minimum voltage obtainable with this arrangement is 2.0 V greater than the regulator voltage.

Figure 16. Current Boost Regulator



The LM340, A series can be current boosted with a PNP transistor. The MJ2955 provides current to 5.0 A. Resistor R in conjuction with the V_{BE} of the PNP determines when the pass transistor begins conducting; this circuit is not short circuit proof. Input–output differential voltage minimum is increased by V_{BE} of the pass transistor.

Figure 17. Short Circuit Protection



The circuit of Figure 17 can be modified to provide supply protection against short circuits by adding a short circuit sense resistor, R_{SC}, and an additional PNP transistor. The current sensing PNP must be able to handle the short circuit current of the three–terminal regulator. Therefore, 4.0 A plastic power transistor is specified.

MOTOROLA

LM350

Three-Terminal Adjustable Output Positive Voltage Regulator

THREE–TERMINAL ADJUSTABLE POSITIVE VOLTAGE REGULATOR

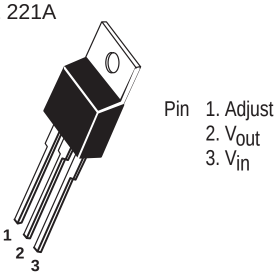
SEMICONDUCTOR TECHNICAL DATA

The LM350 is an adjustable three–terminal positive voltage regulator capable of supplying in excess of 3.0 A over an output voltage range of 1.2 V to 33 V. This voltage regulator is exceptionally easy to use and requires only two external resistors to set the output voltage. Further, it employs internal current limiting, thermal shutdown and safe area compensation, making it essentially blow–out proof.

The LM350 serves a wide variety of applications including local, on card regulation. This device also makes an especially simple adjustable switching regulator, a programmable output regulator, or by connecting a fixed resistor between the adjustment and output, the LM350 can be used as a precision current regulator.

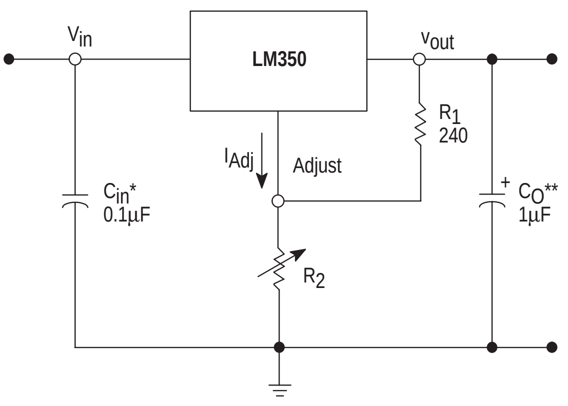
- Guaranteed 3.0 A Output Current
- Output Adjustable between 1.2 V and 33 V
- Load Regulation Typically 0.1%
- Line Regulation Typically 0.005%/V
- Internal Thermal Overload Protection
- Internal Short Circuit Current Limiting Constant with Temperature
- Output Transistor Safe Area Compensation
- Floating Operation for High Voltage Applications
- Standard 3–lead Transistor Package
- Eliminates Stocking Many Fixed Voltages

T SUFFIX
PLASTIC PACKAGE
CASE 221A



Heatsink surface is connected to Pin 2.

Simplified Application



* = C_{in} is required if regulator is located an appreciable distance from power supply filter.
** = C_O is not needed for stability, however, it does improve transient response.

$$V_{out} = 1.25\ V\left(1+\frac{R_2}{R_1}\right)+I_{Adj}\,R_2$$

Since I_{Adj} is controlled to less than 100 µA, the error associated with this term is negligible in most applications.

ORDERING INFORMATION

Device	Operating Temperature Range	Package
LM350T	T_J = 0° to +125°C	Plastic Power
LM350BT#	T_J = –40° to +125°C	Plastic Power

\# Automotive temperature range selections are available with special test conditions and additional tests. Contact your local Motorola sales office for information.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input–Output Voltage Differential	$V_I–V_O$	35	Vdc
Power Dissipation	P_D	Internally Limited	W
Operating Junction Temperature Range	T_J	–40 to +125	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Soldering Lead Temperature (10 seconds)	T_{solder}	300	°C

ELECTRICAL CHARACTERISTICS ($V_I–V_O$ = 5.0 V; I_L = 1.5 A; T_J = T_{low} to T_{high}; P_{max} [Note 1], unless otherwise noted.)

Characteristics	Figure	Symbol	Min	Typ	Max	Unit
Line Regulation (Note 2) T_A = 25°C, 3.0 V ≤ $V_I–V_O$ ≤ 35 V	1	Reg_{line}	–	0.0005	0.03	%/V
Load Regulation (Note 2) T_A = 25°C, 10 mA ≤ I_I ≤ 3.0 A	2	Reg_{load}				
V_O ≤ 5.0 V			–	5.0	25	mV
V_O ≥ 5.0 V			–	0.1	0.5	% V_O
Thermal Regulation, Pulse = 20 ms, (T_A = +25°C)		Reg_{therm}	–	0.002	–	% V_O/W
Adjustment Pin Current	3	I_{Adj}	–	50	100	µA
Adjustment Pin Current Change 3.0 V ≤ $V_I–V_O$ ≤ 35 V 10 mA ≤ I_L ≤ 3.0 A, P_D ≤ P_{max}	1,2	ΔI_{Adj}	–	0.2	5.0	µA
Reference Voltage 3.0 V ≤ $V_I–V_O$ ≤ 35 V 10 mA ≤ I_O ≤ 3.0 A, P_D ≤ P_{max}	3	V_{ref}	1.20	1.25	1.30	V
Line Regulation (Note 2) 3.0 V ≤ $V_I–V_O$ ≤ 35 V	1	Reg_{line}	–	0.02	0.07	%/V
Load Regulation (Note 2) 10 mA ≤ I_L ≤ 3.0 A	2	Reg_{load}				
V_O ≤ 5.0 V			–	20	70	mV
V_O ≥ 5.0 V			–	0.3	1.5	% V_O
Temperature Stability (T_{low} ≤ T_J ≤ T_{high})	3	T_S	–	1.0	–	% V_O
Minimum Load Current to Maintain Regulation ($V_I–V_O$ = 35 V)	3	I_{Lmin}	–	3.5	10	mA
Maximum Output Current	3	I_{max}				A
$V_I–V_O$ ≤ 10 V, P_D ≤ P_{max}			3.0	4.5	–	
$V_I–V_O$ = 30 V, P_D ≤ P_{max}, T_A = 25°C			0.25	1.0	–	
RMS Noise, % of V_O T_A= 25°C, 10 Hz ≤ f ≤ 10 kHz		N	–	0.003	–	% V_O
Ripple Rejection, V_O = 10 V, f = 120 Hz (Note 3)	4	RR				dB
Without C_{Adj}			–	65	–	
C_{Adj} = 10 µF			66	80	–	
Long Term Stability, T_J = T_{high} (Note 4) T_A= 25°C for Endpoint Measurements	3	S	–	0.3	1.0	%/1.0 k Hrs.
Thermal Resistance, Junction–to–Case		$R_{\theta JC}$				°C/W
Peak (Note 5)			–	2.3	–	
Average (Note 6)			–	–	1.5	

NOTES:
1. T_{low} to T_{high} = 0° to +125°C; P_{max} = 25 W for LM350T; T_{low} to T_{high} = –40° to +125°C; P_{max} = 25 W for LM350BT
2. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.
3. C_{Adj}, when used, is connected between the adjustment pin and ground.
4. Since Long–Term Stability cannot be measured on each device before shipment, this specification is an engineering estimate of average stability from lot to lot.
5. Thermal Resistance evaluated measuring the hottest temperature on the die using an infrared scanner. This method of evaluation yields very accurate thermal resistance values which are conservative when compared to the other measurement techniques.
6. The average die temperature is used to derive the value of thermal resistance junction to case (average).

Representative Schematic Diagram

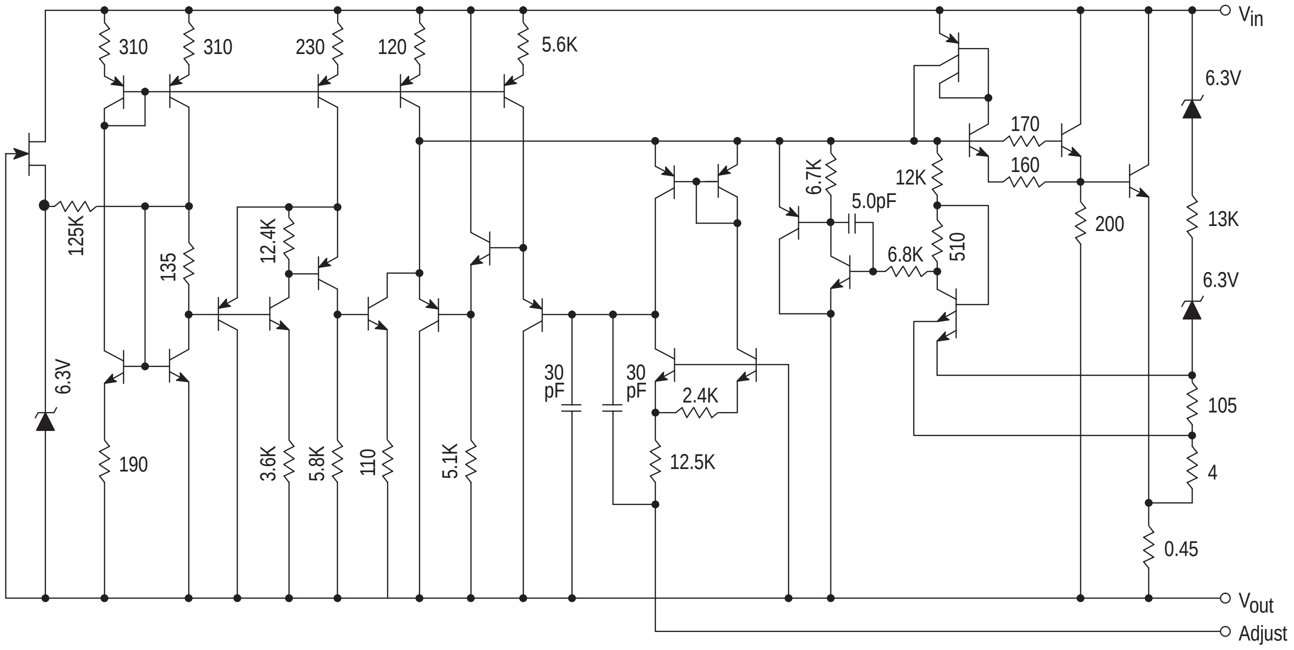
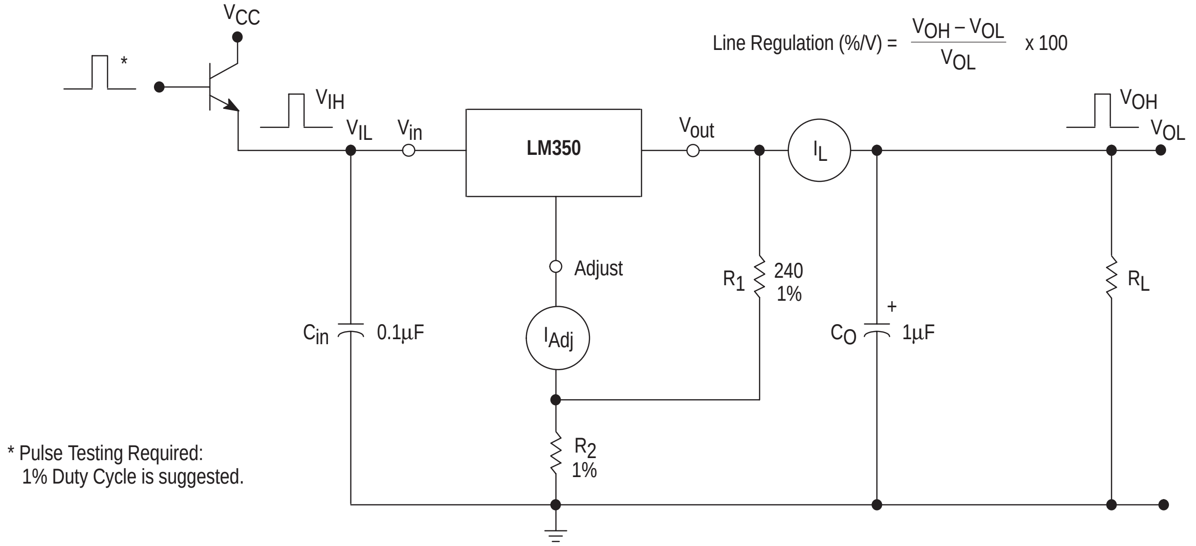


Figure 1. Line Regulation and ΔI_{Adj}/Line Test Circuit



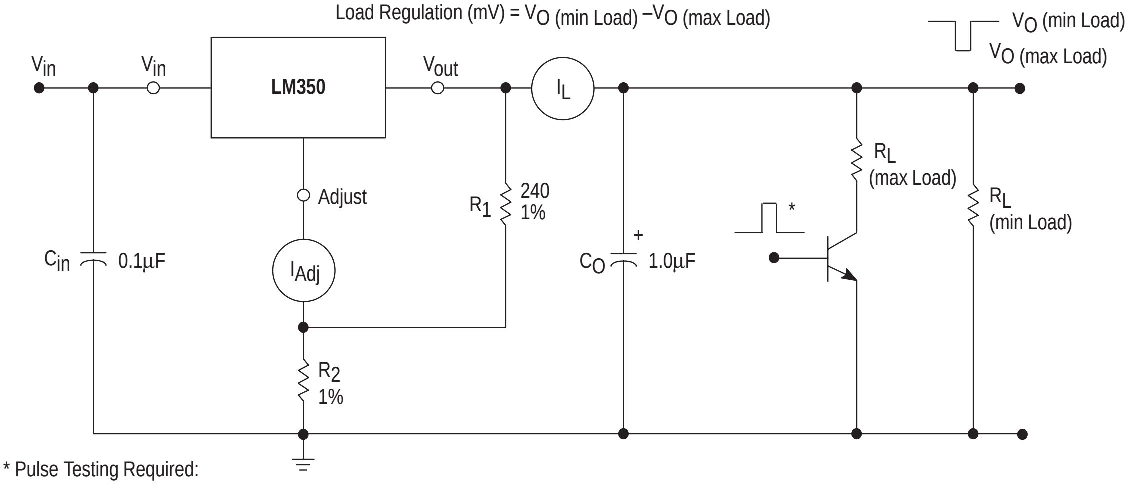
$$\text{Line Regulation (\%/V)} = \frac{V_{OH} - V_{OL}}{V_{OL}} \times 100$$

* Pulse Testing Required:
1% Duty Cycle is suggested.

Figure 2. Load Regulation and ΔI_{Adj}/Load Test Circuit

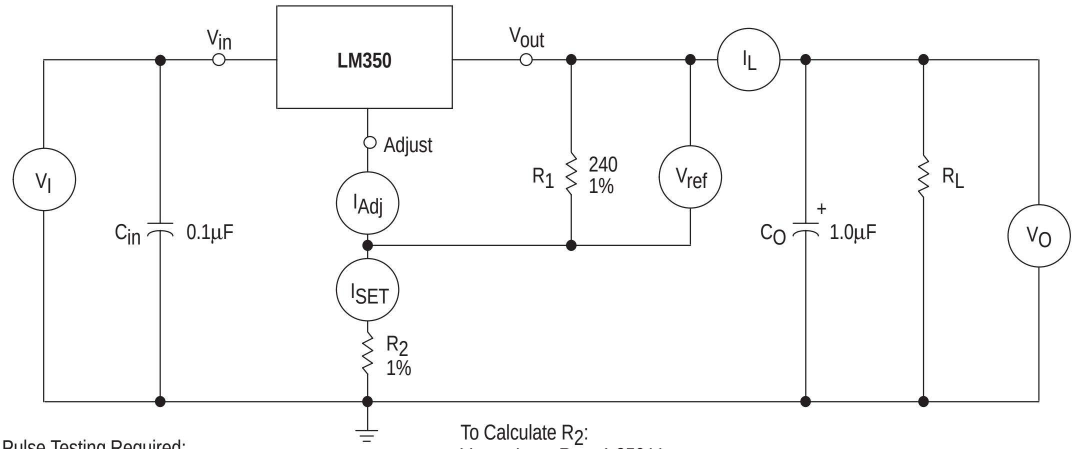
$$\text{Load Regulation } (\%\ V_O) = \frac{V_O\text{ (min Load)} - V_O\text{ (max Load)}}{V_O\text{ (min Load)}} \times 100$$

$$\text{Load Regulation (mV)} = V_O\text{ (min Load)} - V_O\text{ (max Load)}$$



* Pulse Testing Required:
1% Duty Cycle is suggested.

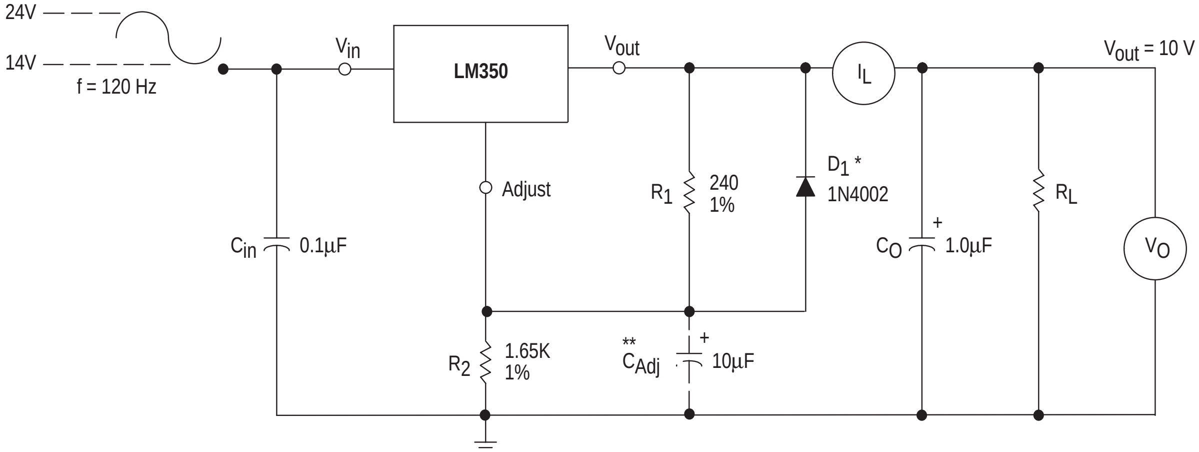
Figure 3. Standard Test Circuit



Pulse Testing Required:
1% Duty Cycle is suggested.

To Calculate R_2:
$V_{out} = I_{SET} R_2 + 1.250$ V
Assume $I_{SET} = 5.25$ mA

Figure 4. Ripple Rejection Test Circuit



* D_1 Discharges C_{Adj} if Output is Shorted to Ground.
**C_{Adj} provides an AC ground to the adjust pin.

Figure 5. Load Regulation

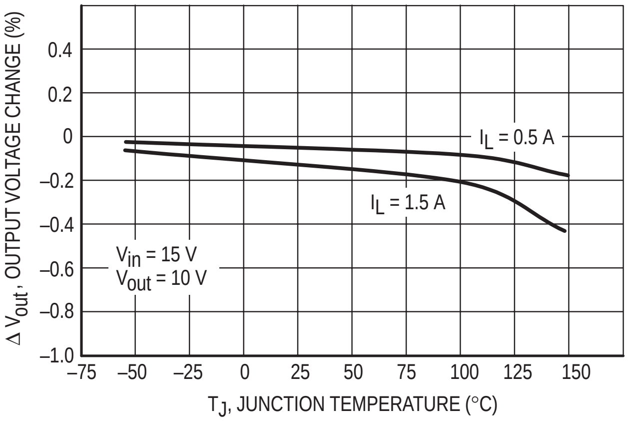


Figure 6. Current Limit

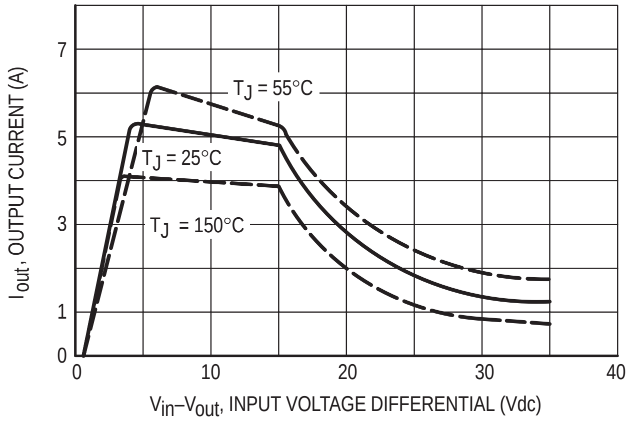


Figure 7. Adjustment Pin Current

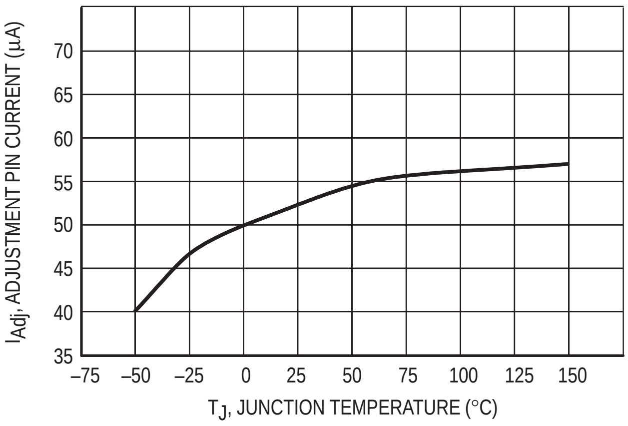


Figure 8. Dropout Voltage

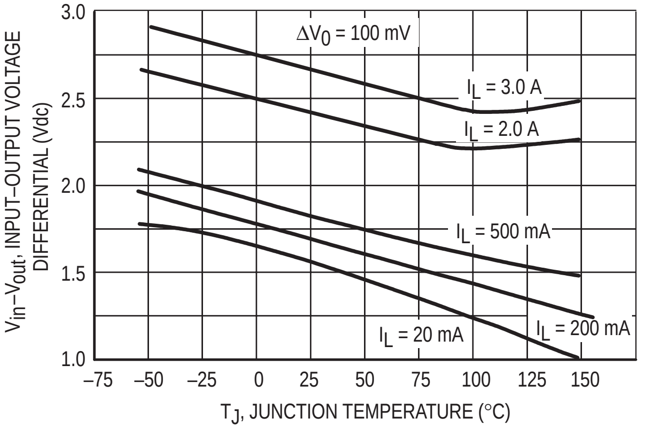


Figure 9. Temperature Stability

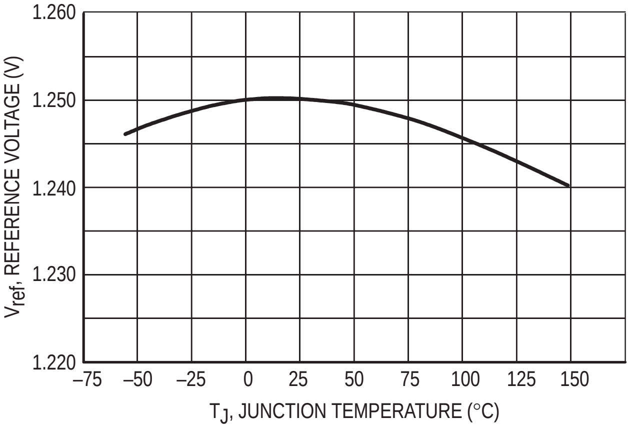


Figure 10. Minimum Operating Current

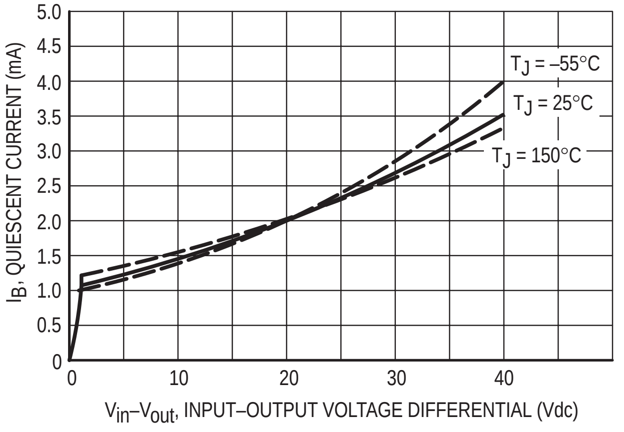


Figure 11. Ripple Rejection versus Output Voltage

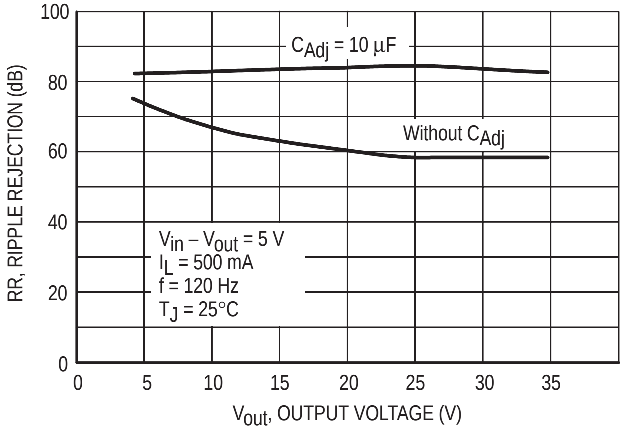


Figure 12. Ripple Rejection versus Output Current

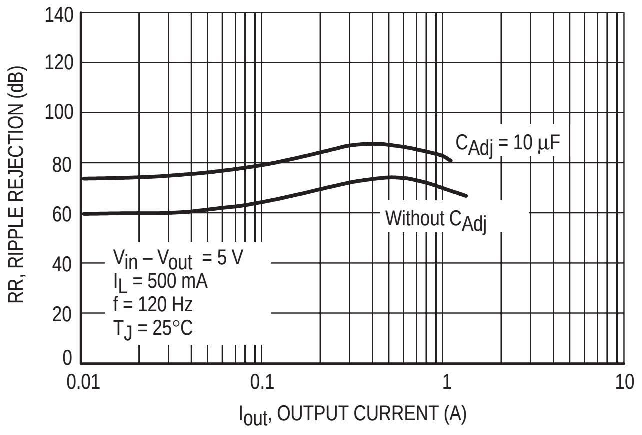


Figure 13. Ripple Rejection versus Frequency

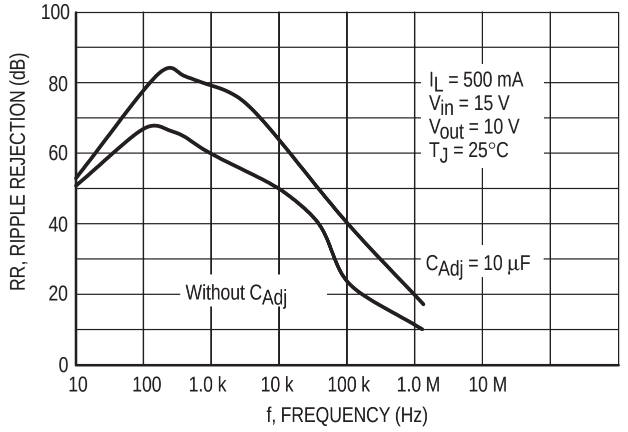


Figure 14. Output Impedance

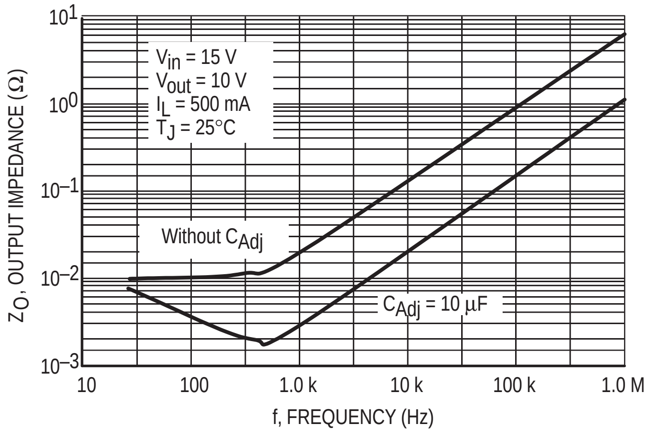


Figure 15. Line Transient Response

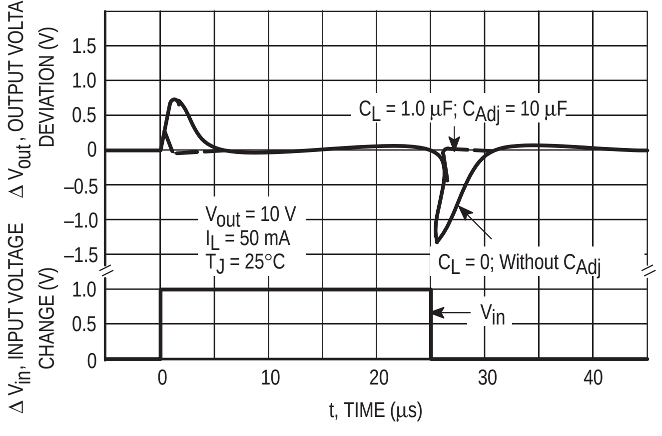
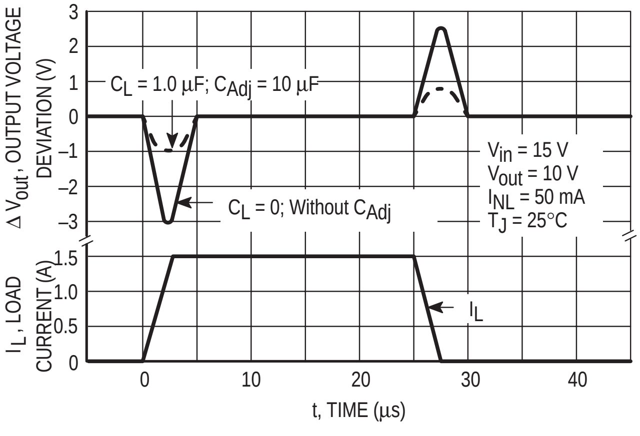


Figure 16. Load Transient Response



APPLICATIONS INFORMATION

Basic Circuit Operation

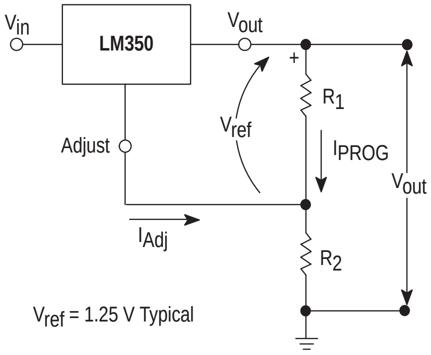
The LM350 is a three–terminal floating regulator. In operation, the LM350 develops and maintains a nominal 1.25 V reference (V_{ref}) between its output and adjustment terminals. This reference voltage is converted to a programming current (I_{PROG}) by R_1 (see Figure 17), and this constant current flows through R_2 to ground. The regulated output voltage is given by:

$$V_{out} = V_{ref}\,(1 + \frac{R_2}{R_1}) + I_{Adj}\,R_2$$

Since the current from the terminal (I_{Adj}) represents an error term in the equation, the LM350 was designed to control I_{Adj} to less than 100 µA and keep it constant. To do this, all quiescent operating current is returned to the output terminal. This imposes the requirement for a minimum load current. If the load current is less than this minimum, the output voltage will rise.

Since the LM350 is a floating regulator, it is only the voltage differential across the circuit which is important to performance, and operation at high voltages with respect to ground is possible.

Figure 17. Basic Circuit Configuration



Load Regulation

The LM350 is capable of providing extremely good load regulation, but a few precautions are needed to obtain maximum performance. For best performance, the programming resistor (R_1) should be connected as close to the regulator as possible to minimize line drops which effectively appear in series with the reference, thereby degrading regulation. The ground end of R_2 can be returned near the load ground to provide remote ground sensing and improve load regulation.

External Capacitors

A 0.1 µF disc or 1 µF tantalum input bypass capacitor (C_{in}) is recommended to reduce the sensitivity to input line impedance.

The adjustment terminal may be bypassed to ground to improve ripple rejection. This capacitor (C_{Adj}) prevents ripple from being amplified as the output voltage is increased. A 10 µF capacitor should improve ripple rejection about 15 dB at 120 Hz in a 10 V application.

Although the LM350 is stable with no output capacitance, like any feedback circuit, certain values of external capacitance can cause excessive ringing. An output capacitance (C_O) in the form of a 1 µF tantalum or 25 µF aluminum electrolytic capacitor on the output swamps this effect and insures stability.

Protection Diodes

When external capacitors are used with any IC regulator, it is sometimes necessary to add protection diodes to prevent the capacitors from discharging through low current points into the regulator.

Figure 18 shows the LM350 with the recommended protection diodes for output voltages in excess of 25 V or high capacitance values (C_O > 25 µF, C_{Adj} > 10 µF). Diode D_1 prevents C_O from discharging thru the IC during an input short circuit. Diode D_2 protects against capacitor C_{Adj} discharging through the IC during an output short circuit. The combination of diodes D_1 and D_2 prevents C_{Adj} from discharging through the IC during an input short circuit.

Figure 18. Voltage Regulator with Protection Diodes

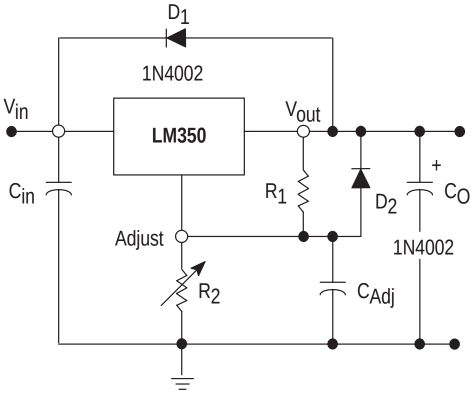
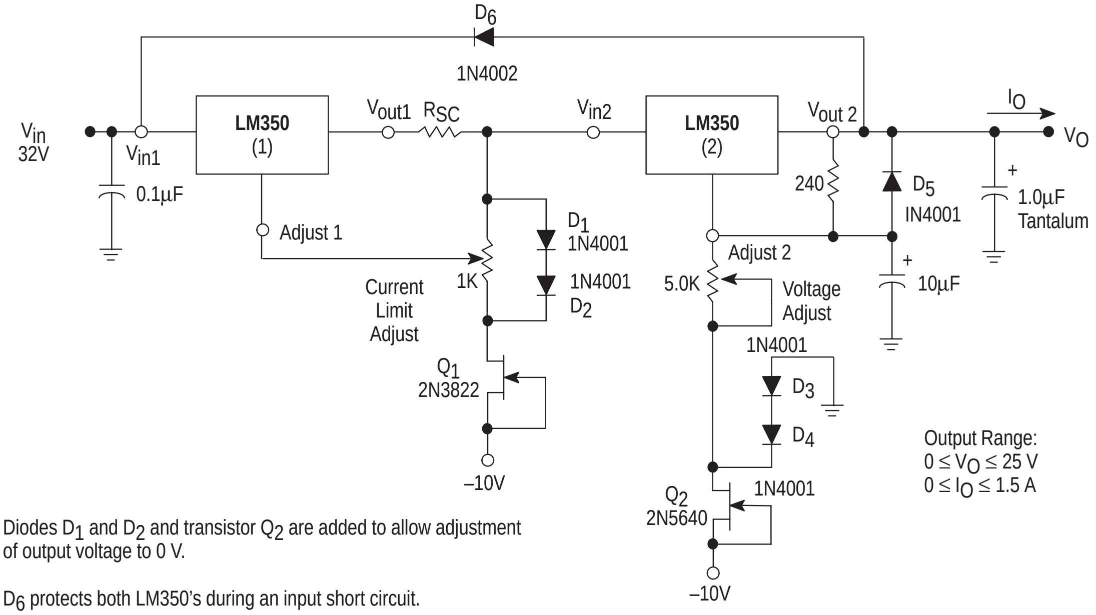


Figure 19. “Laboratory” Power Supply with Adjustable Current Limit and Output Voltage

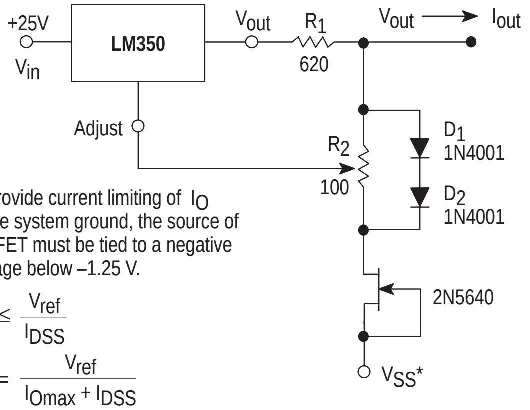


Output Range:
$0 \le V_O \le 25$ V
$0 \le I_O \le 1.5$ A

Diodes D_1 and D_2 and transistor Q_2 are added to allow adjustment of output voltage to 0 V.

D_6 protects both LM350’s during an input short circuit.

Figure 20. Adjustable Current Limiter



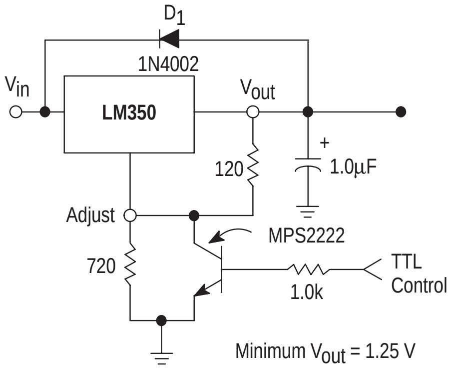
* To provide current limiting of I_O to the system ground, the source of the FET must be tied to a negative voltage below –1.25 V.

$$R_2 \le \frac{V_{ref}}{I_{DSS}}$$

$$R_1 = \frac{V_{ref}}{I_{Omax} + I_{DSS}}$$

$V_O < V_{(BR)DSS} + 1.25\ V + V_{SS}$
$I_{Lmin} - I_{DSS} < I_O < 3.0\ A$
As shown $O < I_O < 1.0\ A$

Figure 21. 5.0 V Electronic Shutdown Regulator



Minimum $V_{out} = 1.25$ V

D_1 protects the device during an input short circuit.

Figure 22. Slow Turn–On Regulator

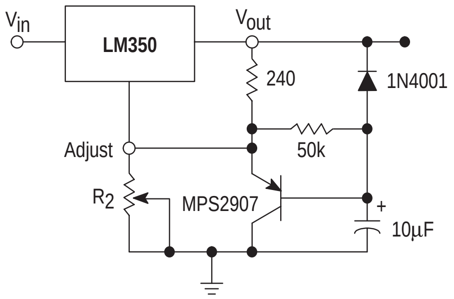
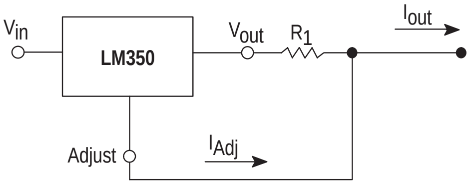


Figure 23. Current Regulator



$$I_{out} = \left(\frac{V_{ref}}{R_1}\right) + I_{Adj}$$

$$\cong \frac{1.25\ V}{R_1}$$

$10\ mA \le I_{out} \le 3.0\ A$

MOTOROLA

LM2575

Advance Information

Easy Switcher™ 1.0 A Step-Down Voltage Regulator

The LM2575 series of regulators are monolithic integrated circuits ideally suited for easy and convenient design of a step–down switching regulator (buck converter). All circuits of this series are capable of driving a 1.0 A load with excellent line and load regulation. These devices are available in fixed output voltages of 3.3 V, 5.0 V, 12 V, 15 V, and an adjustable output version.

These regulators were designed to minimize the number of external components to simplify the power supply design. Standard series of inductors optimised for use with the LM2575 are offered by several different inductor manufacturers.

Since the LM2575 converter is a switch–mode power supply, its efficiency is significantly higher in comparison with popular three–terminal linear regulators, especially with higher input voltages. In many cases, the power dissipated by the LM2575 regulator is so low, that no heatsink is required or its size could be reduced dramatically.

The LM2575 features include a guaranteed ±4% tolerance on output voltage within specified input voltages and output load conditions, and ±10% on the oscillator frequency (±2% over 0°C to 125°C). External shutdown is included, featuring 80 µA typical standby current. The output switch includes cycle–by–cycle current limiting, as well as thermal shutdown for full protection under fault conditions.

Features

- 3.3 V, 5.0 V, 12 V, 15 V, and Adjustable Output Versions
- Adjustable Version Output Voltage Range of 1.23 V to 37 V ±4% Maximum Over Line and Load Conditions
- Guaranteed 1.0 A Output Current
- Wide Input Voltage Range: 4.75 V to 40 V
- Requires Only 4 External Components
- 52 kHz Fixed Frequency Internal Oscillator
- TTL Shutdown Capability, Low Power Standby Mode
- High Efficiency
- Uses Readily Available Standard Inductors
- Thermal Shutdown and Current Limit Protection

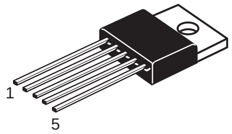
Applications

- Simple and High–Efficiency Step–Down (Buck) Regulators
- Efficient Pre–Regulator for Linear Regulators
- On–Card Switching Regulators
- Positive to Negative Converters (Buck–Boost)
- Negative Step–Up Converters
- Power Supply for Battery Chargers

EASY SWITCHER™ 1.0 A STEP–DOWN VOLTAGE REGULATOR

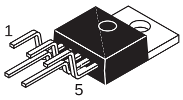
SEMICONDUCTOR TECHNICAL DATA

T SUFFIX
PLASTIC PACKAGE
CASE 314D



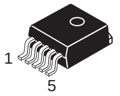
Pin 1. V_{in}
2. Output
3. Ground
4. Feedback
5. ON/OFF

TV SUFFIX
PLASTIC PACKAGE
CASE 314B



Heatsink surface connected to Pin 3.

D2T SUFFIX
PLASTIC PACKAGE
CASE 936A
(D^2PAK)



Heatsink surface (shown as terminal 6 in case outline drawing) is connected to Pin 3.

DEVICE TYPE/NOMINAL OUTPUT VOLTAGE

LM2575–3.3	3.3 V
LM2575–5	5.0 V
LM2575–12	12 V
LM2575–15	15 V
LM2575–Adj	1.23 V to 37 V

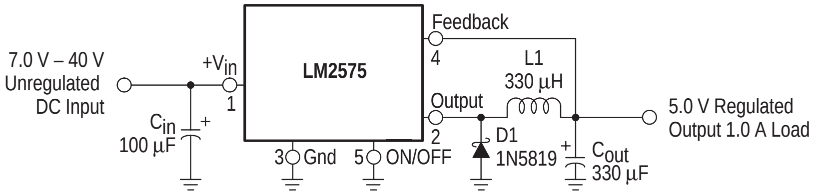
ORDERING INFORMATION

Device	Operating Temperature Range	Package
LM2575T–**	T_J = –40° to +125°C	Straight Lead
LM2575TV–**		Vertical Mount
LM2575D2T–**		Surface Mount

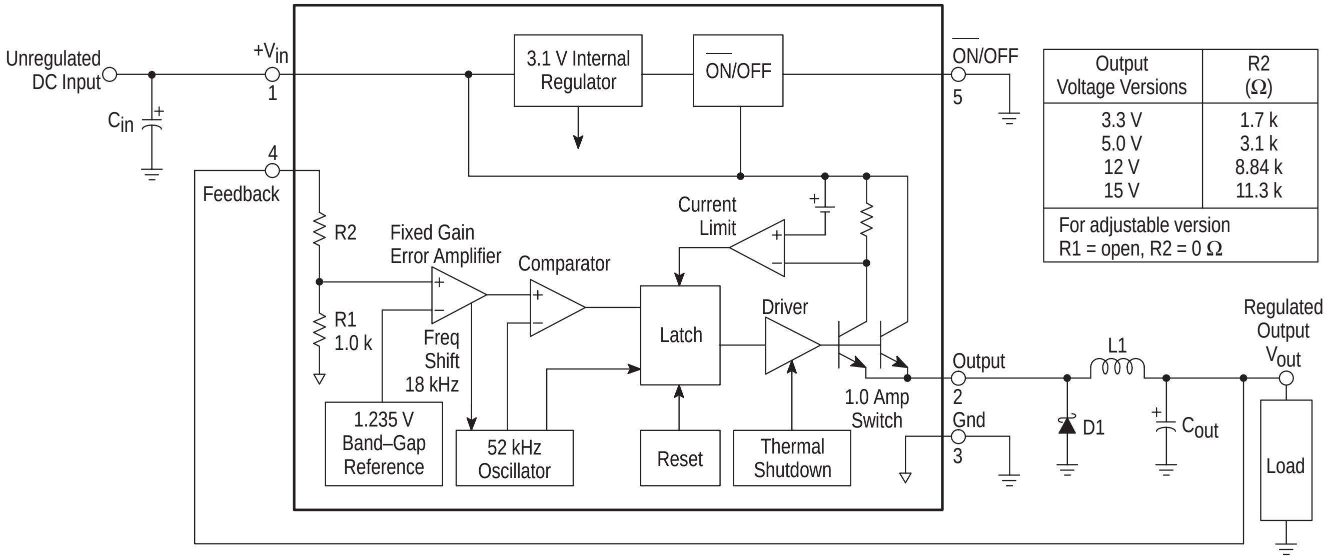
** = Voltage Option, ie. 3.3, 5.0, 12, 15 V and Adjustable Output.

Figure 1. Block Diagram and Typical Application

Typical Application (Fixed Output Voltage Versions)



Representative Block Diagram and Typical Application



Output Voltage Versions	R2 (Ω)
3.3 V	1.7 k
5.0 V	3.1 k
12 V	8.84 k
15 V	11.3 k

For adjustable version
R1 = open, R2 = 0 Ω

This device contains 162 active transistors.

ABSOLUTE MAXIMUM RATINGS (Absolute Maximum Ratings indicate limits beyond which damage to the device may occur.)

Rating	Symbol	Value	Unit
Maximum Supply Voltage	V_{in}	45	V
$\overline{\text{ON}}$/OFF Pin Input Voltage	–	–0.3 V ≤ V ≤ +V_{in}	V
Output Voltage to Ground (Steady–State)	–	–1.0	V
Power Dissipation Case 314B and 314D (TO–220, 5–Lead) Thermal Resistance, Junction–to–Ambient Thermal Resistance, Junction–to–Case Case 936A (D^2PAK) Thermal Resistance, Junction–to–Ambient (Figure 34) Thermal Resistance, Junction–to–Case	 P_D $R_{\theta JA}$ $R_{\theta JC}$ P_D $R_{\theta JA}$ $R_{\theta JC}$	 Internally Limited 65 5.0 Internally Limited 70 5.0	 W °C/W °C/W W °C/W °C/W
Storage Temperature Range	T_{stg}	–65 to +150	°C
Minimum ESD Rating (Human Body Model: C = 100 pF, R = 1.5 kΩ)	–	3.0	kV
Lead Temperature (Soldering, 10 s)	–	260	°C
Maximum Junction Temperature	T_J	150	°C

NOTE: ESD data available upon request.

OPERATING RATINGS (Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics.)

Rating	Symbol	Value	Unit
Operating Junction Temperature Range	T_J	–40 to +125	°C
Supply Voltage	V_{in}	40	V

SYSTEM PARAMETERS ([Note 1] Test Circuit Figure 14)

ELECTRICAL CHARACTERISTICS (Unless otherwise specified, V_{in} = 12 V for the 3.3 V, 5.0 V, and Adjustable version, V_{in} = 25 V for the 12 V version, and V_{in} = 30 V for the 15 V version. I_{Load} = 200 mA. For typical values T_J = 25°C, for min/max values T_J is the operating junction temperature range that applies [Note 2], unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
LM2575–3.3 ([Note 1] Test Circuit Figure 14)					
Output Voltage (V_{in} = 12 V, I_{Load} = 0.2 A, T_J = 25°C)	V_{out}	3.234	3.3	3.366	V
Output Voltage (4.75 V ≤ V_{in} ≤ 40 V, 0.2 A ≤ I_{Load} ≤ 1.0 A)	V_{out}				V
T_J = 25°C		3.168	3.3	3.432	
T_J = –40 to +125°C		3.135	–	3.465	
Efficiency (V_{in} = 12 V, I_{Load} = 1.0 A)	η	–	75	–	%
LM2575–5 ([Note 1] Test Circuit Figure 14)					
Output Voltage (V_{in} = 12 V, I_{Load} = 0.2 A, T_J = 25°C)	V_{out}	4.9	5.0	5.1	V
Output Voltage (8.0 V ≤ V_{in} ≤ 40 V, 0.2 A ≤ I_{Load} ≤ 1.0 A)	V_{out}				V
T_J = 25°C		4.8	5.0	5.2	
T_J = –40 to +125°C		4.75	–	5.25	
Efficiency (V_{in} = 12 V, I_{Load} = 1.0 A)	η	–	77	–	%
LM2575–12 ([Note 1] Test Circuit Figure 14)					
Output Voltage (V_{in} = 25 V, I_{Load} = 0.2 A, T_J = 25°C)	V_{out}	11.76	12	12.24	V
Output Voltage (15 V ≤ V_{in} ≤ 40 V, 0.2 A ≤ I_{Load} ≤ 1.0 A)	V_{out}				V
T_J = 25°C		11.52	12	12.48	
T_J = –40 to +125°C		11.4	–	12.6	
Efficiency (V_{in} = 15V, I_{Load} = 1.0 A)	η	–	88	–	%
LM2575–15 ([Note 1] Test Circuit Figure 14)					
Output Voltage (V_{in} = 30 V, I_{Load} = 0.2 A, T_J = 25°C)	V_{out}	14.7	15	15.3	V
Output Voltage (18 V ≤ V_{in} ≤ 40 V, 0.2 A ≤ I_{Load} ≤ 1.0 A)	V_{out}				V
T_J = 25°C		14.4	15	15.6	
T_J = –40 to +125°C		14.25	–	15.75	
Efficiency (V_{in} = 18 V, I_{Load} = 1.0 A)	η	–	88	–	%
LM2575 ADJUSTABLE VERSION ([Note 1] Test Circuit Figure 14)					
Feedback Voltage (V_{in} = 12 V, I_{Load} = 0.2 A, V_{out} = 5.0 V, T_J = 25°C)	V_{FB}	1.217	1.23	1.243	V
Feedback Voltage (8.0 V ≤ V_{in} ≤ 40 V, 0.2 A ≤ I_{Load} ≤ 1.0 A, V_{out} = 5.0 V)	V_{FB}				V
T_J = 25°C		1.193	1.23	1.267	
T_J = –40 to +125°C		1.18	–	1.28	
Efficiency (V_{in} = 12 V, I_{Load} = 1.0 A, V_{out} = 5.0 V)	η	–	77	–	%

NOTES: 1. External components such as the catch diode, inductor, input and output capacitors can affect switching regulator system performance. When the LM2575 is used as shown in the Figure 14 test circuit, system performance will be as shown in system parameters section.

2. Tested junction temperature range for the LM2575: T_{low} = –40°C T_{high} = +125°C

DEVICE PARAMETERS

ELECTRICAL CHARACTERISTICS (Unless otherwise specified, V_{in} = 12 V for the 3.3 V, 5.0 V, and Adjustable version, V_{in} = 25 V for the 12 V version, and V_{in} = 30 V for the 15 V version. I_{Load} = 200 mA. For typical values T_J = 25°C, for min/max values T_J is the operating junction temperature range that applies [Note 2], unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
ALL OUTPUT VOLTAGE VERSIONS					
Feedback Bias Current (V_{out} = 5.0 V [Adjustable Version Only])	I_b				nA
T_J = 25°C		–	25	100	
T_J = –40 to +125°C		–	–	200	
Oscillator Frequency [Note 3]	f_{osc}				kHz
T_J = 25°C		–	52	–	
T_J = 0 to +125°C		47	–	58	
T_J = –40 to +125°C		42	–	63	
Saturation Voltage (I_{out} = 1.0 A [Note 4])	V_{sat}				V
T_J = 25°C		–	1.0	1.2	
T_J = –40 to +125°C		–	–	1.3	
Max Duty Cycle (“on”) [Note 5]	DC	94	98	–	%
Current Limit (Peak Current [Notes 4 and 3])	I_{CL}				A
T_J = 25°C		1.7	2.3	3.0	
T_J = –40 to +125°C		1.4	–	3.2	
Output Leakage Current [Notes 6 and 7], T_J = 25°C	I_L				mA
Output = 0 V		–	0.8	2.0	
Output = –1.0 V		–	6.0	20	
Quiescent Current [Note 6]	I_Q				mA
T_J = 25°C		–	5.0	9.0	
T_J = –40 to +125°C		–	–	11	
Standby Quiescent Current ($\overline{\text{ON}}$/OFF Pin = 5.0 V (“off”))	I_{stby}				µA
T_J = 25°C		–	80	200	
T_J = –40 to +125°C		–	–	400	
$\overline{\text{ON}}$/OFF Pin Logic Input Level (Test Circuit Figure 14)					V
V_{out} = 0 V	V_{IH}				
T_J = 25°C		2.2	1.4	–	
T_J = –40 to +125°C		2.4	–	–	
V_{out} = Nominal Output Voltage	V_{IL}				
T_J = 25°C		–	1.2	1.0	
T_J = –40 to +125°C		–	–	0.8	
$\overline{\text{ON}}$/OFF Pin Input Current (Test Circuit Figure 14)					µA
$\overline{\text{ON}}$/OFF Pin = 5.0 V (“off”), T_J = 25°C	I_{IH}	–	15	30	
$\overline{\text{ON}}$/OFF Pin = 0 V (“on”), T_J = 25°C	I_{IL}	–	0	5.0	

NOTES:
3. The oscillator frequency reduces to approximately 18 kHz in the event of an output short or an overload which causes the regulated output voltage to drop approximately 40% from the nominal output voltage. This self protection feature lowers the average dissipation of the IC by lowering the minimum duty cycle from 5% down to approximately 2%.
4. Output (Pin 2) sourcing current. No diode, inductor or capacitor connected to output pin.
5. Feedback (Pin 4) removed from output and connected to 0 V.
6. Feedback (Pin 4) removed from output and connected to +12 V for the Adjustable, 3.3 V, and 5.0 V versions, and +25 V for the 12 V and 15 V versions, to force the output transistor “off”.
7. V_{in} = 40 V.

TYPICAL PERFORMANCE CHARACTERISTICS (Circuit of Figure 14)

Figure 2. Normalized Output Voltage

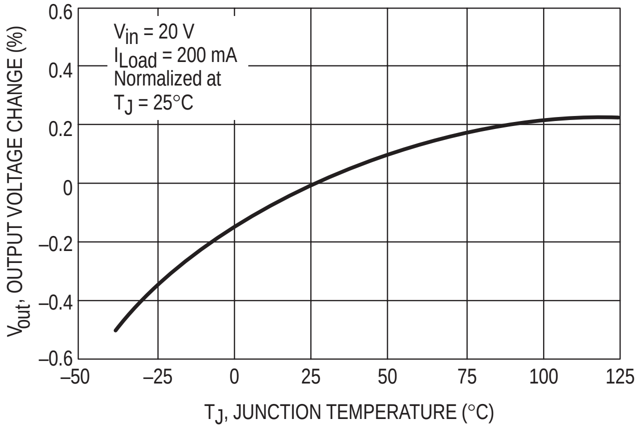


Figure 3. Line Regulation

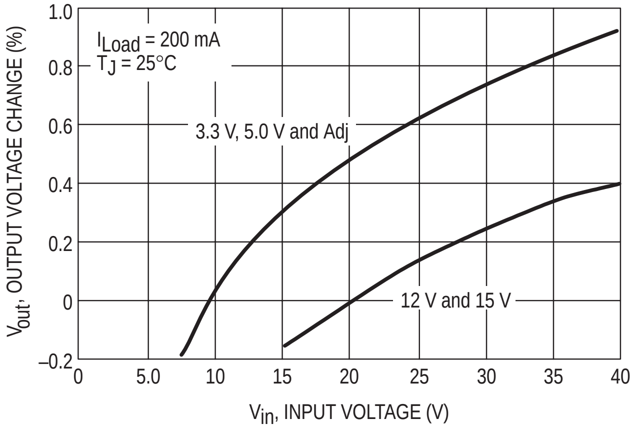


Figure 4. Switch Saturation Voltage

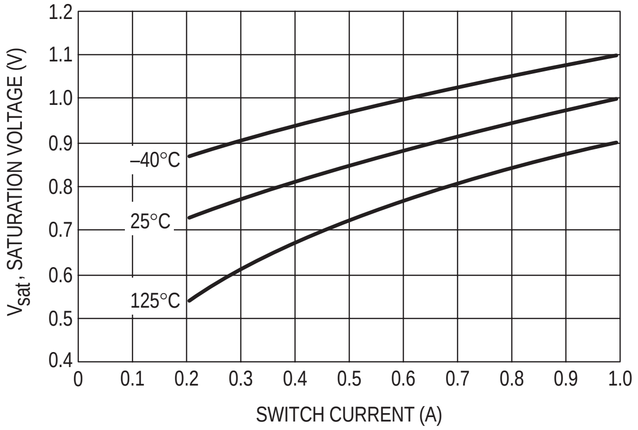


Figure 5. Current Limit

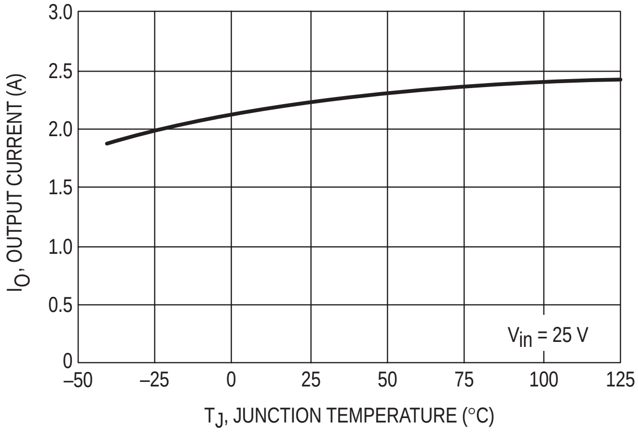


Figure 6. Dropout Voltage

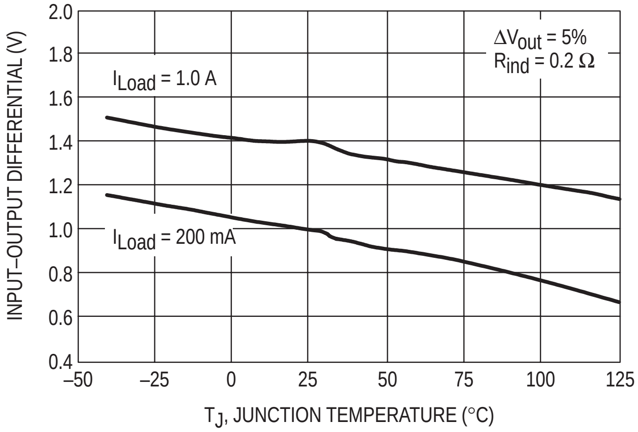


Figure 7. Quiescent Current

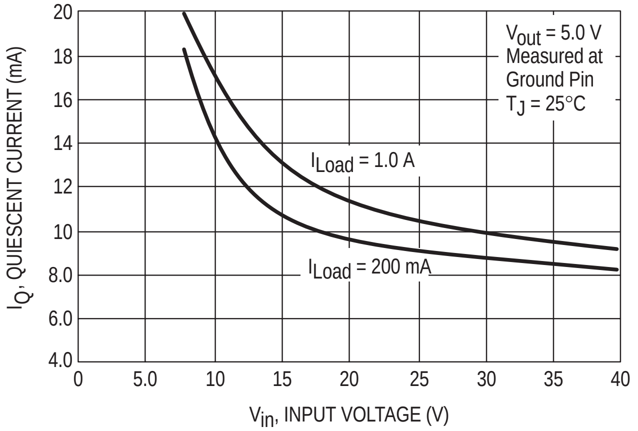


Figure 8. Standby Quiescent Current

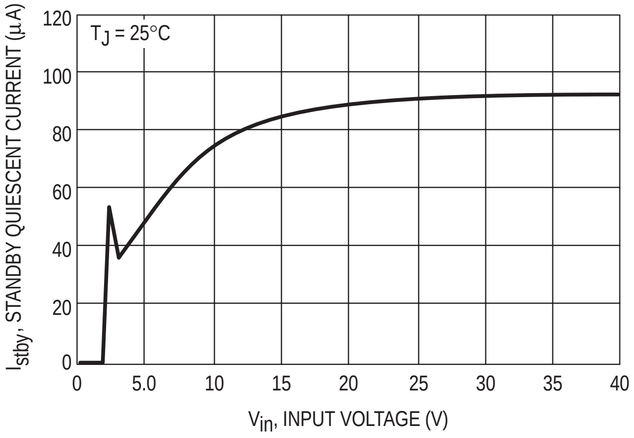


Figure 9. Standby Quiescent Current

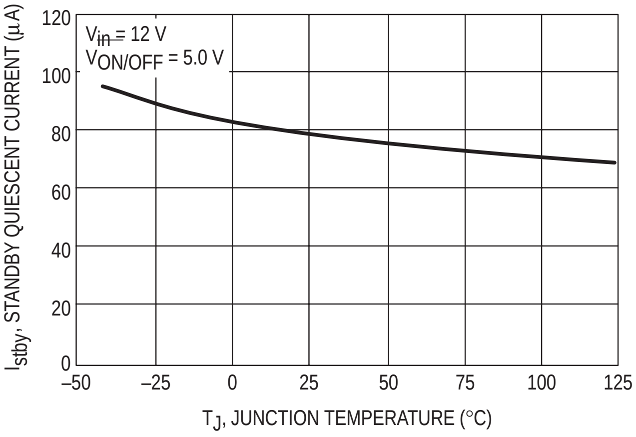


Figure 10. Oscillator Frequency

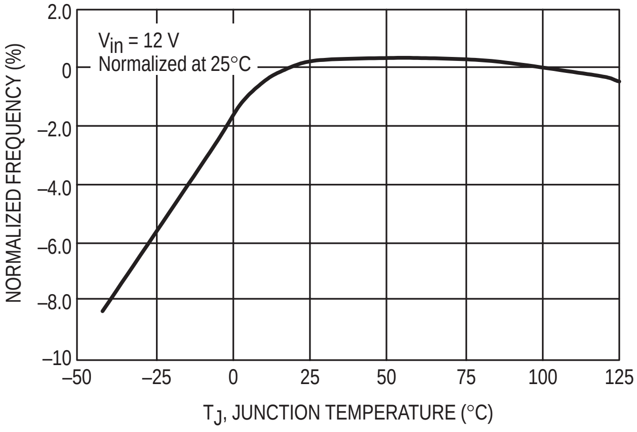


Figure 11. Feedback Pin Current

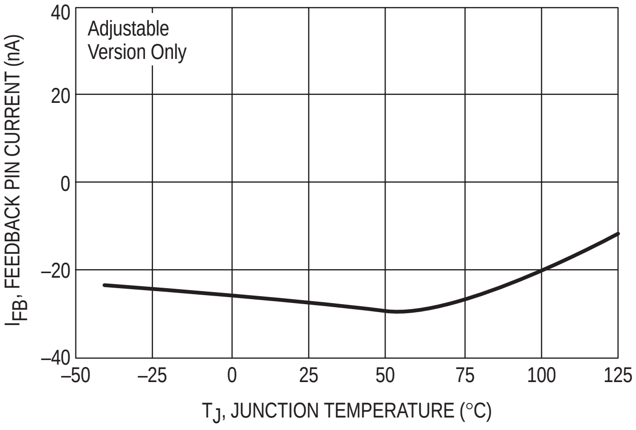


Figure 12. Switching Waveforms

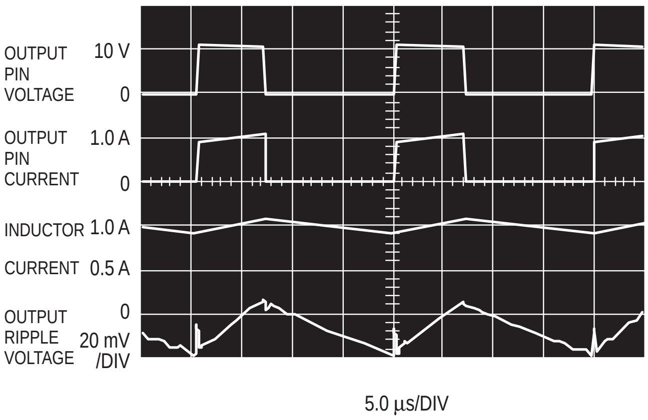


Figure 13. Load Transient Response

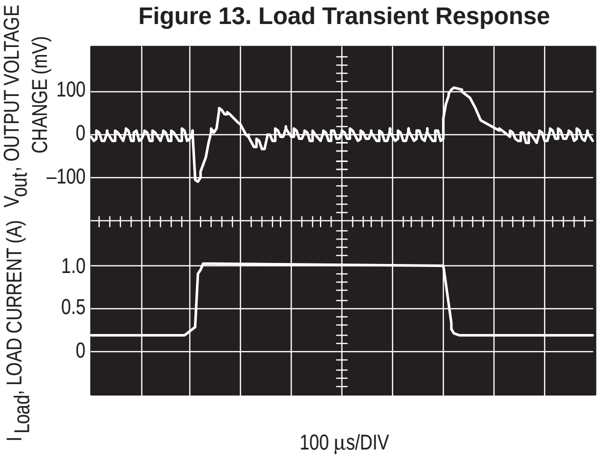
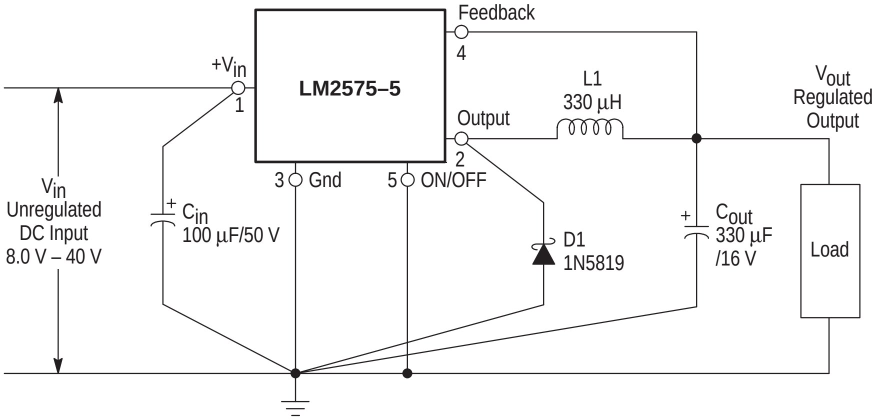


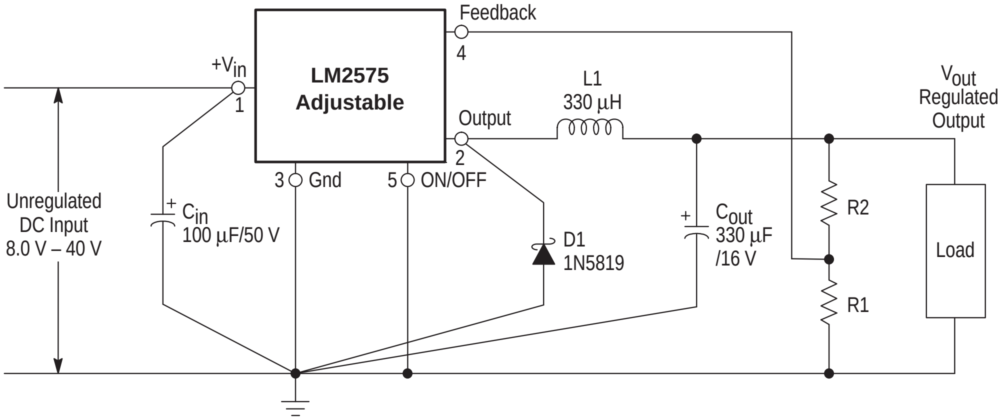
Figure 14. Typical Test Circuit

5.0 Output Voltage Versions



C_{in}	100 µF, 50 V, Aluminium Electrolytic
C_{out}	330 µF, 16 V, Aluminium Electrolytic
D1	Schottky, 1N5819
L1	330 µF, PE–52627 (for 5.0 V in, 3.3 V out, use 100 µH, PE–92108)

Adjustable Output Voltage Versions



$$V_{out} = V_{ref}\left(1 + \frac{R2}{R1}\right)$$

$$R2 = R1\left(\frac{V_{out}}{V_{ref}} - 1\right)$$

Where V_{ref} = 1.23 V, R1 between 1.0 kΩ and 5.0 kΩ

PCB LAYOUT GUIDELINES

As in any switching regulator, the layout of the printed circuit board is very important. Rapidly switching currents associated with wiring inductance, stray capacitance and parasitic inductance of the printed circuit board traces can generate voltage transients which can generate electromagnetic interferences (EMI) and affect the desired operation. As indicated in the Figure 14, to minimize inductance and ground loops, the length of the leads indicated by heavy lines should be kept as short as possible. For best results, single–point grounding (as indicated) or ground plane construction should be used.

On the other hand, the PCB area connected to the Pin 2 (emitter of the internal switch) of the LM2575 should be kept to a minimum in order to minimize coupling to sensitive circuitry.

Another sensitive part of the circuit is the feedback. It is important to keep the sensitive feedback wiring short. To assure this, physically locate the programming resistors near to the regulator, when using the adjustable version of the LM2575 regulator.

PIN FUNCTION DESCRIPTION

Pin	Symbol	Description (Refer to Figure 1)
1	V_{in}	This pin is the positive input supply for the LM2575 step–down switching regulator. In order to minimize voltage transients and to supply the switching currents needed by the regulator, a suitable input bypass capacitor must be present (C_{in} in Figure 1).
2	Output	This is the emitter of the internal switch. The saturation voltage V_{sat} of this output switch is typically 1.0 V. It should be kept in mind that the PCB area connected to this pin should be kept to a minimum in order to minimize coupling to sensitive circuitry.
3	Gnd	Circuit ground pin. See the information about the printed circuit board layout.
4	Feedback	This pin senses regulated output voltage to complete the feedback loop. The signal is divided by the internal resistor divider network R2, R1 and applied to the non–inverting input of the internal error amplifier. In the Adjustable version of the LM2575 switching regulator this pin is the direct input of the error amplifier and the resistor network R2, R1 is connected externally to allow programming of the output voltage.
5	$\overline{\text{ON}}$/OFF	It allows the switching regulator circuit to be shut down using logic level signals, thus dropping the total input supply current to approximately 80 µA. The input threshold voltage is typically 1.4 V. Applying a voltage above this value (up to $+V_{in}$) shuts the regulator off. If the voltage applied to this pin is lower than 1.4 V or if this pin is connected to ground, the regulator will be in the “on” condition.

DESIGN PROCEDURE

Buck Converter Basics

The LM2575 is a “Buck” or Step–Down Converter which is the most elementary forward–mode converter. Its basic schematic can be seen in Figure 15.

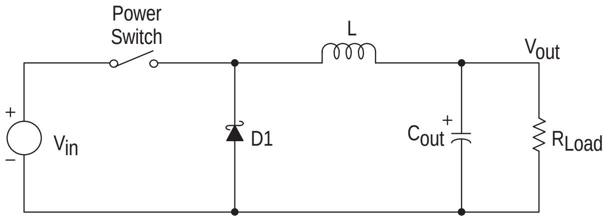
The operation of this regulator topology has two distinct time periods. The first one occurs when the series switch is on, the input voltage is connected to the input of the inductor.

The output of the inductor is the output voltage, and the rectifier (or catch diode) is reverse biased. During this period, since there is a constant voltage source connected across the inductor, the inductor current begins to linearly ramp upwards, as described by the following equation:

$$I_{L(on)} = \frac{\left(V_{in} - V_{out}\right) t_{on}}{L}$$

During this “on” period, energy is stored within the core material in the form of magnetic flux. If the inductor is properly designed, there is sufficient energy stored to carry the requirements of the load during the “off” period.

Figure 15. Basic Buck Converter



The next period is the “off” period of the power switch. When the power switch turns off, the voltage across the inductor reverses its polarity and is clamped at one diode voltage drop below ground by catch dioded. Current now flows through the catch diode thus maintaining the load current loop. This removes the stored energy from the inductor. The inductor current during this time is:

$$I_{L(off)} = \frac{\left(V_{out} - V_D\right) t_{off}}{L}$$

This period ends when the power switch is once again turned on. Regulation of the converter is accomplished by varying the duty cycle of the power switch. It is possible to describe the duty cycle as follows:

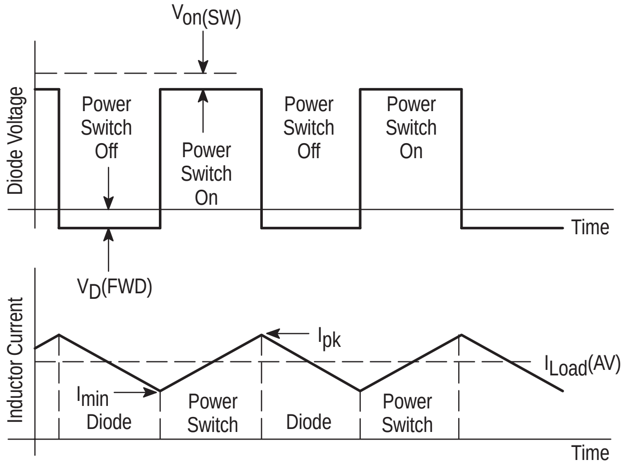
$d = \frac{t_{on}}{T}$, where T is the period of switching.

For the buck converter with ideal components, the duty cycle can also be described as:

$$d = \frac{V_{out}}{V_{in}}$$

Figure 16 shows the buck converter idealized waveforms of the catch diode voltage and the inductor current.

Figure 16. Buck Converter Idealized Waveforms



Procedure (Fixed Output Voltage Version) In order to simplify the switching regulator design, a step–by–step design procedure and example is provided.

Procedure	Example
Given Parameters: V_{out} = Regulated Output Voltage (3.3 V, 5.0 V, 12 V or 15 V) $V_{in(max)}$ = Maximum DC Input Voltage $I_{Load(max)}$ = Maximum Load Current	**Given Parameters:** V_{out} = 5.0 V $V_{in(max)}$ = 20 V $I_{Load(max)}$ = 0.8 A
1. Controller IC Selection According to the required input voltage, output voltage and current, select the appropriate type of the controller IC output voltage version.	**1. Controller IC Selection** According to the required input voltage, output voltage, current polarity and current value, use the LM2575–5 controller IC
2. Input Capacitor Selection (C_{in}) To prevent large voltage transients from appearing at the input and for stable operation of the converter, an aluminium or tantalum electrolytic bypass capacitor is needed between the input pin $+V_{in}$ and ground pin Gnd. This capacitor should be located close to the IC using short leads. This capacitor should have a low ESR (Equivalent Series Resistance) value.	**2. Input Capacitor Selection (C_{in})** A 47 µF, 25 V aluminium electrolytic capacitor located near to the input and ground pins provides sufficient bypassing.
3. Catch Diode Selection (D1) **A.** Since the diode maximum peak current exceeds the regulator maximum load current the catch diode current rating must be at least 1.2 times greater than the maximum load current. For a robust design the diode should have a current rating equal to the maximum current limit of the LM2575 to be able to withstand a continuous output short **B.** The reverse voltage rating of the diode should be at least 1.25 times the maximum input voltage.	**3. Catch Diode Selection (D1)** **A.** For this example the current rating of the diode is 1.0 A. **B.** Use a 30 V 1N5818 Schottky diode, or any of the suggested fast recovery diodes shown in the Table 4.
4. Inductor Selection (L1) **A.** According to the required working conditions, select the correct inductor value using the selection guide from Figures 17 to 21. **B.** From the appropriate inductor selection guide, identify the inductance region intersected by the Maximum Input Voltage line and the Maximum Load Current line. Each region is identified by an inductance value and an inductor code. **C.** Select an appropriate inductor from the several different manufacturers part numbers listed in Table 1 or Table 2. When using Table 2 for selecting the right inductor the designer must realize that the inductor current rating must be higher than the maximum peak current flowing through the inductor. This maximum peak current can be calculated as follows: $I_{p(max)} = I_{Load(max)} + \frac{\left(V_{in}-V_{out}\right) t_{on}}{2L}$ where t_{on} is the “on” time of the power switch and $t_{on} = \frac{V_{out}}{V_{in}} \times \frac{1}{f_{osc}}$ For additional information about the inductor, see the inductor section in the “External Components” section of this data sheet.	**4. Inductor Selection (L1)** **A.** Use the inductor selection guide shown in Figures 17 to 21. **B.** From the selection guide, the inductance area intersected by the 20 V line and 0.8 A line is L330. **C.** Inductor value required is 330 µH. From the Table 1 or Table 2, choose an inductor from any of the listed manufacturers.

Procedure (Fixed Output Voltage Version) (continued) In order to simplify the switching regulator design, a step–by–step design procedure and example is provided.

Procedure	Example
5. Output Capacitor Selection (C_{out}) **A.** Since the LM2575 is a forward–mode switching regulator with voltage mode control, its open loop 2–pole–2–zero frequency characteristic has the dominant pole–pair determined by the output capacitor and inductor values. For stable operation and an acceptable ripple voltage, (approximately 1% of the output voltage) a value between 100 µF and 470 µF is recommended. **B.** Due to the fact that the higher voltage electrolytic capacitors generally have lower ESR (Equivalent Series Resistance) numbers, the output capacitor's voltage rating should be at least 1.5 times greater than the output voltage. For a 5.0 V regulator, a rating at least 8V is appropriate, and a 10 V or 16 V rating is recommended.	**5. Output Capacitor Selection (C_{out})** **A.** C_{out} = 100 µF to 470 µF standard aluminium electrolytic. **B.** Capacitor voltage rating = 16 V.

Procedure (Adjustable Output Version: LM2575–Adj)

Procedure	Example
Given Parameters: V_{out} = Regulated Output Voltage $V_{in(max)}$ = Maximum DC Input Voltage $I_{Load(max)}$ = Maximum Load Current	**Given Parameters:** V_{out} = 8.0 V $V_{in(max)}$ = 12 V $I_{Load(max)}$ = 1.0 A
1. Programming Output Voltage To select the right programming resistor R1 and R2 value (see Figure 14) use the following formula: $V_{out} = V_{ref}\left(1 + \frac{R2}{R1}\right)$ where V_{ref} = 1.23 V Resistor R1 can be between 1.0 k and 5.0 kΩ. (For best temperature coefficient and stability with time, use 1% metal film resistors). $R2 = R1\left(\frac{V_{out}}{V_{ref}} - 1\right)$	**1. Programming Output Voltage** (selecting R1 and R2) Select R1 and R2: $V_{out} = 1.23\left(1 + \frac{R2}{R1}\right)$ Select R1 = 1.8 kΩ $R2 = R1\left(\frac{V_{out}}{V_{ref}} - 1\right) = 1.8\ k\left(\frac{8.0\ V}{1.23\ V} - 1\right)$ R2 = 9.91 kΩ, choose a 9.88 k metal film resistor.
2. Input Capacitor Selection (C_{in}) To prevent large voltage transients from appearing at the input and for stable operation of the converter, an aluminium or tantalum electrolytic bypass capacitor is needed between the input pin $+V_{in}$ and ground pin Gnd This capacitor should be located close to the IC using short leads. This capacitor should have a low ESR (Equivalent Series Resistance) value**.** For additional information see input capacitor section in the "External Components" section of this data sheet.	**2. Input Capacitor Selection (C_{in})** A 100 µF aluminium electrolytic capacitor located near the input and ground pin provides sufficient bypassing.
3. Catch Diode Selection (D1) **A.** Since the diode maximum peak current exceeds the regulator maximum load current the catch diode current rating must be at least 1.2 times greater than the maximum load current. For a robust design, the diode should have a current rating equal to the maximum current limit of the LM2575 to be able to withstand a continuous output short. **B.** The reverse voltage rating of the diode should be at least 1.25 times the maximum input voltage.	**3. Catch Diode Selection (D1)** **A.** For this example, a 3.0 A current rating is adequate. **B.** Use a 20 V 1N5820 or MBR320 Schottky diode or any suggested fast recovery diode in the Table 4.

Procedure (Adjustable Output Version: LM2575–Adj) (continued)

Procedure	Example
4. Inductor Selection (L1)	**4. Inductor Selection (L1)**
A. Use the following formula to calculate the inductor Volt x microsecond [V x µs] constant: $E \times T = \left(V_{in} - V_{out}\right) \frac{V_{out}}{V_{on}} \times \frac{10^6}{F[Hz]}\ [V \times \mu s]$	**A.** Calculate E x T [V x µs] constant: $E \times T = (12 - 8.0) \times \frac{8.0}{12} \times \frac{1000}{52} = 51\ [V \times \mu s]$
B. Match the calculated E x T value with the corresponding number on the vertical axis of the Inductor Value Selection Guide shown in Figure 21. This E x T constant is a measure of the energy handling capability of an inductor and is dependent upon the type of core, the core area, the number of turns, and the duty cycle.	**B.** E x T = 51 [V x µs]
C. Next step is to identify the inductance region intersected by the E x T value and the maximum load current value on the horizontal axis shown in Figure 21.	**C.** $I_{Load(max)}$ = 1.0 A Inductance Region = L220
D. From the inductor code, identify the inductor value. Then select an appropriate inductor from the Table 1 or Table 2. The inductor chosen must be rated for a switching frequency of 52 kHz and for a current rating of 1.15 x I_{load}. The inductor current rating can also be determined by calculating the inductor peak current: $I_{p(max)} = I_{Load(max)} + \frac{\left(V_{in} - V_{out}\right) t_{on}}{2L}$ where t_{on} is the “on” time of the power switch and $t_{on} = \frac{V_{out}}{V_{in}} \times \frac{1}{f_{osc}}$ For additional information about the inductor, see the inductor section in the “External Components” section of this data sheet.	**D.** Proper inductor value = 220 µH Choose the inductor from the Table 1 or Table 2.
5. Output Capacitor Selection (C_{out})	**5. Output Capacitor Selection (C_{out})**
A. Since the LM2575 is a forward–mode switching regulator with voltage mode control, its open loop 2–pole–2–zero frequency characteristic has the dominant pole–pair determined by the output capacitor and inductor values. For stable operation, the capacitor must satisfy the following requirement: $C_{out} \geq 7.785 \frac{V_{in(max)}}{V_{out} \times L\ [\mu H]}\ [\mu F]$	**A.** $C_{out} \geq 7.785 \frac{12}{8.220} = 53\ \mu F$ To achieve an acceptable ripple voltage, select C_{out} = 100 µF electrolytic capacitor.
B. Capacitor values between 10 µF and 2000 µF will satisfy the loop requirements for stable operation. To achieve an acceptable output ripple voltage and transient response, the output capacitor may need to be several times larger than the above formula yields.	
C. Due to the fact that the higher voltage electrolytic capacitors generally have lower ESR (Equivalent Series Resistance) numbers, the output capacitor’s voltage rating should be at least 1.5 times greater than the output voltage. For a 5.0 V regulator, a rating of at least 8V is appropriate, and a 10 V or 16 V rating is recommended.	

INDUCTOR VALUE SELECTION GUIDE

Figure 17. LM2575–3.3

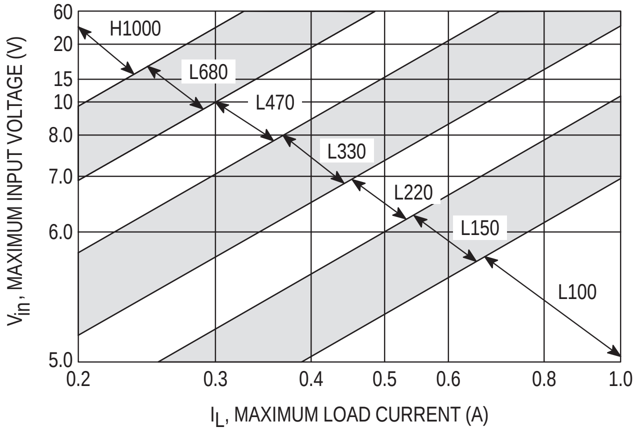


Figure 18. LM2575–5.0

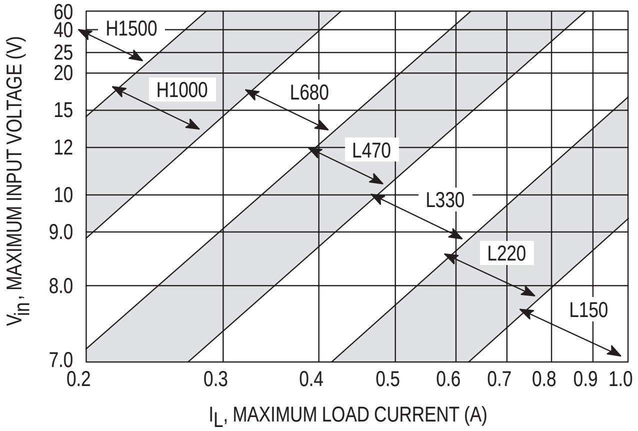


Figure 19. LM2575–12

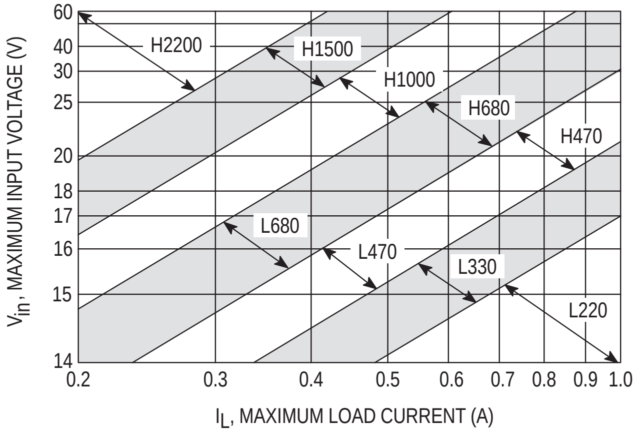


Figure 20. LM2575–15

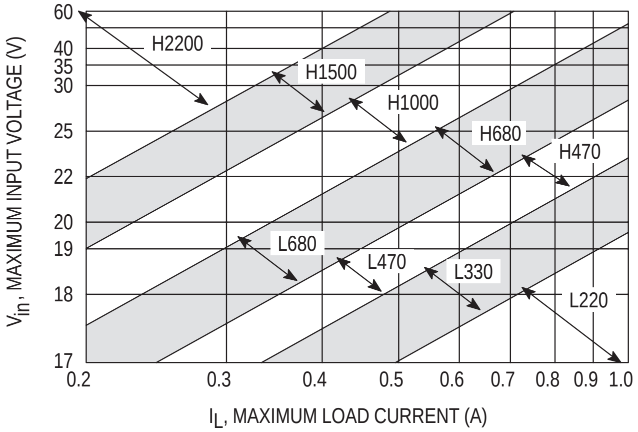
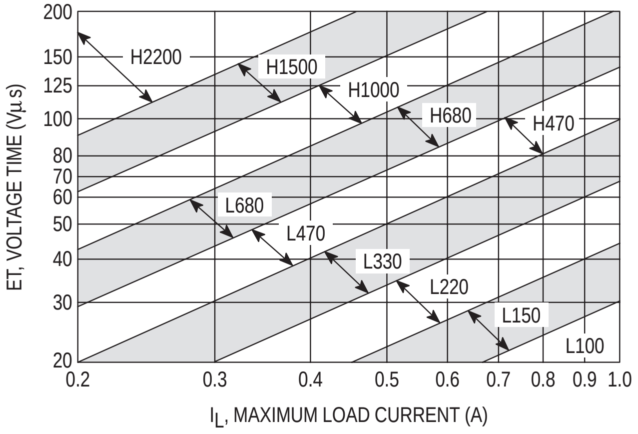


Figure 21. LM2575–Adj



NOTE: This Inductor Value Selection Guide is applicable for continuous mode only.

Table 1. Inductor Selection Guide

Inductor Code	Inductor Value	Pulse Eng	Renco	AIE	Tech 39
L100	100 µH	PE–92108	RL2444	415–0930	77 308 BV
L150	150 µH	PE–53113	RL1954	415–0953	77 358 BV
L220	220 µH	PE–52626	RL1953	415–0922	77 408 BV
L330	330 µH	PE–52627	RL1952	415–0926	77 458 BV
L470	470 µH	PE–53114	RL1951	415–0927	–
L680	680 µH	PE–52629	RL1950	415–0928	77 508 BV
H150	150 µH	PE–53115	RL2445	415–0936	77 368 BV
H220	220 µH	PE–53116	RL2446	430–0636	77 410 BV
H330	330 µH	PE–53117	RL2447	430–0635	77 460 BV
H470	470 µH	PE–53118	RL1961	430–0634	–
H680	680 µH	PE–53119	RL1960	415–0935	77 510 BV
H1000	1000 µH	PE–53120	RL1959	415–0934	77 558 BV
H1500	1500 µH	PE–53121	RL1958	415–0933	–
H2200	2200 µH	PE–53122	RL2448	415–0945	77 610 BV

Table 2. Inductor Selection Guide

Inductance	Current	Schott		Renco		Pulse Engineering		Coilcraft
(µH)	(A)	THT	SMT	THT	SMT	THT	SMT	SMT
68	0.32	67143940	67144310	RL–1284–68–43	RL1500–68	PE–53804	PE–53804–S	DO1608–68
	0.58	67143990	67144360	RL–5470–6	RL1500–68	PE–53812	PE–53812–S	DO3308–683
	0.99	67144070	67144450	RL–5471–5	RL1500–68	PE–53821	PE–53821–S	DO3316–683
	1.78	67144140	67144520	RL–5471–5	–	PE–53830	PE–53830–S	DO5022P–683
100	0.48	67143980	67144350	RL–5470–5	RL1500–100	PE–53811	PE–53811–S	DO3308–104
	0.82	67144060	67144440	RL–5471–4	RL1500–100	PE–53820	PE–53820–S	DO3316–104
	1.47	67144130	67144510	RL–5471–4	–	PE–53829	PE–53829–S	DO5022P–104
150	0.39	–	67144340	RL–5470–4	RL1500–150	PE–53810	PE–53810–S	DO3308–154
	0.66	67144050	67144430	RL–5471–3	RL1500–150	PE–53819	PE–53819–S	DO3316–154
	1.20	67144120	67144500	RL–5471–3	–	PE–53828	PE–53828–S	DO5022P–154
220	0.32	67143960	67144330	RL–5470–3	RL1500–220	PE–53809	PE–53809–S	DO3308–224
	0.55	67144040	67144420	RL–5471–2	RL1500–220	PE–53818	PE–53818–S	DO3316–224
	1.00	67144110	67144490	RL–5471–2	–	PE–53827	PE–53827–S	DO5022P–224
330	0.42	67144030	67144410	RL–5471–1	RL1500–330	PE–53817	PE–53817–S	DO3316–334
	0.80	67144100	67144480	RL–5471–1	–	PE–53826	PE–53826–S	DO5022P–334

NOTE: Table 1 and Table 2 of this Indicator Selection Guide shows some examples of different manufacturer products suitable for design with the LM2575.

Table 3. Example of Several Inductor Manufacturers Phone/Fax Numbers

Pulse Engineering Inc.	Phone Fax	+ 1–619–674–8100 + 1–619–674–8262
Pulse Engineering Inc. Europe	Phone Fax	+ 353 93 24 107 + 353 93 24 459
Renco Electronics Inc.	Phone Fax	+ 1–516–645–5828 + 1–516–586–5562
AIE Magnetics	Phone Fax	+ 1–813–347–2181
Coilcraft Inc.	Phone Fax	+ 1–708–322–2645 + 1–708–639–1469
Coilcraft Inc., Europe	Phone Fax	+ 44 1236 730 595 + 44 1236 730 627
Tech 39	Phone Fax	+ 33 8425 2626 + 33 8425 2610
Schott Corp.	Phone Fax	+ 1–612–475–1173 + 1–612–475–1786

Table 4. Diode Selection Guide gives an overview about both surface–mount and through–hole diodes for an effective design. Device listed in bold are available from Motorola.

	Schottky				Ultra–Fast Recovery			
	1.0 A		3.0 A		1.0 A		3.0 A	
V_R	SMT	THT	SMT	THT	SMT	THT	SMT	THT
20 V	SK12	**1N5817** SR102	SK32 **MBRD320**	**1N5820** **MBR320** SR302				
30 V	**MBRS130LT3** SK13	**1N5818** SR103 11DQ03	SK33 **MBRD330**	**1N5821** **MBR330** SR303 31DQ03	**MURS120T3**	**MUR120** 11DF1 HER102	**MURS320T3**	
40 V	**MBRS140T3** SK14 10BQ040 10MQ040	**1N5819** SR104 11DQ04	**MBRS340T3** **MBRD340** 30WQ04 SK34	**1N5822** **MBR340** SR304 31DQ04	10BF10		**MURD320**	**MUR320** 30WF10 **MUR420**
50 V	**MBRS150** 10BQ050	**MBR150** SR105 11DQ05	**MBRD350** SK35 30WQ05	**MBR350** SR305 11DQ05			31DF1 HER302	

EXTERNAL COMPONENTS

Input Capacitor (C_{in})

The Input Capacitor Should Have a Low ESR

For stable operation of the switch mode converter a low ESR (Equivalent Series Resistance) aluminium or solid tantalum bypass capacitor is needed between the input pin and the ground pin to prevent large voltage transients from appearing at the input. It must be located near the regulator and use short leads. With most electrolytic capacitors, the capacitance value decreases and the ESR increases with lower temperatures. For reliable operation in temperatures below –25°C larger values of the input capacitor may be needed. Also paralleling a ceramic or solid tantalum capacitor will increase the regulator stability at cold temperatures.

RMS Current Rating of C_{in}

The important parameter of the input capacitor is the RMS current rating. Capacitors that are physically large and have large surface area will typically have higher RMS current ratings. For a given capacitor value, a higher voltage electrolytic capacitor will be physically larger than a lower voltage capacitor, and thus be able to dissipate more heat to the surrounding air, and therefore will have a higher RMS current rating. The consequence of operating an electrolytic capacitor above the RMS current rating is a shortened operating life. In order to assure maximum capacitor operating lifetime, the capacitor's RMS ripple current rating should be:

$$I_{rms} > 1.2 \times d \times I_{Load}$$

where d is the duty cycle, for a buck regulator

$$d = \frac{t_{on}}{T} = \frac{V_{out}}{V_{in}}$$

and $d = \frac{t_{on}}{T} = \frac{|V_{out}|}{|V_{out}| + V_{in}}$ for a buck–boost regulator.

Output Capacitor (C_{out})

For low output ripple voltage and good stability, low ESR output capacitors are recommended. An output capacitor has two main functions: it filters the output and provides regulator loop stability. The ESR of the output capacitor and the peak–to–peak value of the inductor ripple current are the main factors contributing to the output ripple voltage value.Standard aluminium electrolytics could be adequate for some applications but for quality design low ESR types are recommended.

An aluminium electrolytic capacitor's ESR value is related to many factors such as the capacitance value, the voltage rating, the physical size and the type of construction. In most cases, the higher voltage electrolytic capacitors have lower ESR value. Often capacitors with much higher voltage ratings may be needed to provide low ESR values that are required for low output ripple voltage.

The Output Capacitor Requires an ESR Value That Has an Upper and Lower Limit

As mentioned above, a low ESR value is needed for low output ripple voltage, typically 1% to 2% of the output voltage. But if the selected capacitor's ESR is extremely low (below 0.05 Ω), there is a possibility of an unstable feedback loop, resulting in oscillation at the output. This situation can occur when a tantalum capacitor, that can have a very low ESR, is used as the only output capacitor.

At Low Temperatures, Put in Parallel Aluminium Electrolytic Capacitors with Tantalum Capacitors

Electrolytic capacitors are not recommended for temperatures below –25°C. The ESR rises dramatically at cold temperatures and typically rises 3 times at –25°C and as much as 10 times at –40°C. Solid tantalum capacitors have much better ESR spec at cold temperatures and are recommended for temperatures below –25°C. They can be also used in parallel with aluminium electrolytics. The value of the tantalum capacitor should be about 10% or 20% of the total capacitance. The output capacitor should have at least 50% higher RMS ripple current rating at 52 kHz than the peak–to–peak inductor ripple current.

Catch Diode

Locate the Catch Diode Close to the LM2575

The LM2575 is a step–down buck converter; it requires a fast diode to provide a return path for the inductor current when the switch turns off. This diode must be located close to the LM2575 using short leads and short printed circuit traces to avoid EMI problems.

Use a Schottky or a Soft Switching Ultra–Fast Recovery Diode

Since the rectifier diodes are very significant source of losses within switching power supplies, choosing the rectifier that best fits into the converter design is an important process. Schottky diodes provide the best performance because of their fast switching speed and low forward voltage drop.

They provide the best efficiency especially in low output voltage applications (5.0 V and lower). Another choice could be Fast–Recovery, or Ultra–Fast Recovery diodes. It has to be noted, that some types of these diodes with an abrupt turnoff characteristic may cause instability or EMI troubles.

A fast–recovery diode with soft recovery characteristics can better fulfill a quality, low noise design requirements. Table 4 provides a list of suitable diodes for the LM2575 regulator. Standard 50/60 Hz rectifier diodes such as the 1N4001 series or 1N5400 series are **NOT** suitable.

Inductor

The magnetic components are the cornerstone of all switching power supply designs. The style of the core and the winding technique used in the magnetic component's design has a great influence on the reliability of the overall power supply.

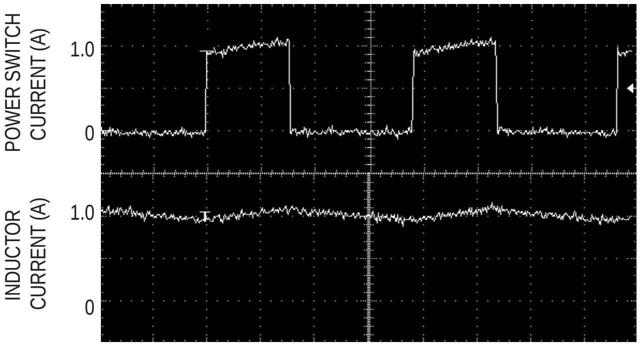
Using an improper or poorly designed inductor can cause high voltage spikes generated by the rate of transitions in current within the switching power supply, and the possibility of core saturation can arise during an abnormal operational mode. Voltage spikes can cause the semiconductors to enter avalanche breakdown and the part can instantly fail if enough energy is applied. It can also cause significant RFI (Radio Frequency Interference) and EMI (Electro–Magnetic Interference) problems.

Continuous and Discontinuous Mode of Operation

The LM2575 step–down converter can operate in both the continuous and the discontinuous modes of operation. The regulator works in the continuous mode when loads are relatively heavy, the current flows through the inductor continuously and never falls to zero. Under light load conditions, the circuit will be forced to the discontinuous mode when inductor current falls to zero for certain period of time (see Figure 22 and Figure 23). Each mode has distinctively different operating characteristics, which can affect the regulator performance and requirements. In many cases the preferred mode of operation is the continuous mode. It offers greater output power, lower peak currents in the switch, inductor and diode, and can have a lower output ripple voltage. On the other hand it does require larger inductor values to keep the inductor current flowing continuously, especially at low output load currents and/or high input voltages.

To simplify the inductor selection process, an inductor selection guide for the LM2575 regulator was added to this data sheet (Figures 17 through 21). This guide assumes that the regulator is operating in the continuous mode, and selects an inductor that will allow a peak–to–peak inductor ripple current to be a certain percentage of the maximum design load current. This percentage is allowed to change as different design load currents are selected. For light loads (less than approximately 200 mA) it may be desirable to operate the regulator in the discontinuous mode, because the inductor value and size can be kept relatively low. Consequently, the percentage of inductor peak–to–peak current increases. This discontinuous mode of operation is perfectly acceptable for this type of switching converter. Any buck regulator will be forced to enter discontinuous mode if the load current is light enough.

Figure 22. Continuous Mode Switching Current Waveforms



HORTIZONTAL TIME BASE: 5.0 µs/DIV

Selecting the Right Inductor Style

Some important considerations when selecting a core type are core material, cost, the output power of the power supply, the physical volume the inductor must fit within, and the amount of EMI (Electro–Magnetic Interference) shielding that the core must provide. The inductor selection guide covers different styles of inductors, such as pot core, E–core, toroid and bobbin core, as well as different core materials such as ferrites and powdered iron from different manufacturers.

For high quality design regulators the toroid core seems to be the best choice. Since the magnetic flux is completely contained within the core, it generates less EMI, reducing noise problems in sensitive circuits. The least expensive is the bobbin core type, which consists of wire wound on a ferrite rod core. This type of inductor generates more EMI due to the fact that its core is open, and the magnetic flux is not completely contained within the core.

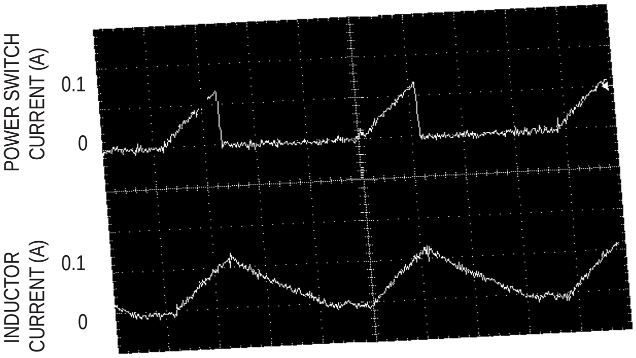
When multiple switching regulators are located on the same printed circuit board, open core magnetics can cause interference between two or more of the regulator circuits, especially at high currents due to mutual coupling. A toroid, pot core or E–core (closed magnetic structure) should be used in such applications.

Do Not Operate an Inductor Beyond its Maximum Rated Current

Exceeding an inductor's maximum current rating may cause the inductor to overheat because of the copper wire losses, or the core may saturate. Core saturation occurs when the flux density is too high and consequently the cross sectional area of the core can no longer support additional lines of magnetic flux.

This causes the permeability of the core to drop, the inductance value decreases rapidly and the inductor begins to look mainly resistive. It has only the dc resistance of the winding. This can cause the switch current to rise very rapidly and force the LM2575 internal switch into cycle–by–cycle current limit, thus reducing the dc output load current. This can also result in overheating of the inductor and/or the LM2575. Different inductor types have different saturation characteristics, and this should be kept in mind when selecting an inductor.

Figure 23. Discontinuous Mode Switching Current Waveforms



HORTIZONTAL TIME BASE: 5.0 µs/DIV

GENERAL RECOMMENDATIONS

Output Voltage Ripple and Transients

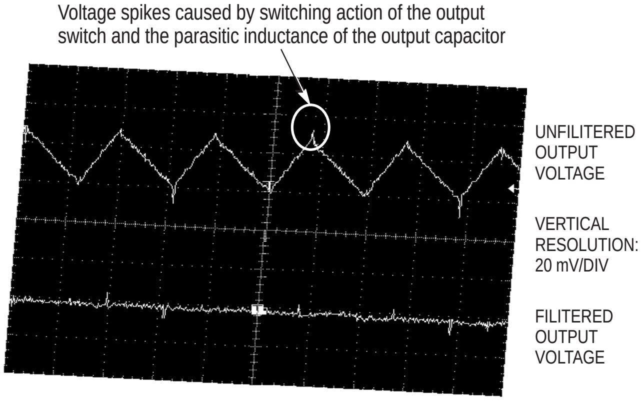
Source of the Output Ripple

Since the LM2575 is a switch mode power supply regulator, its output voltage, if left unfiltered, will contain a sawtooth ripple voltage at the switching frequency. The output ripple voltage value ranges from 0.5% to 3% of the output voltage. It is caused mainly by the inductor sawtooth ripple current multiplied by the ESR of the output capacitor.

Short Voltage Spikes and How to Reduce Them

The regulator output voltage may also contain short voltage spikes at the peaks of the sawtooth waveform (see Figure 24). These voltage spikes are present because of the fast switching action of the output switch, and the parasitic inductance of the output filter capacitor. There are some other important factors such as wiring inductance, stray capacitance, as well as the scope probe used to evaluate these transients, all these contribute to the amplitude of these spikes. To minimise these voltage spikes, low inductance capacitors should be used, and their lead lengths must be kept short. The importance of quality printed circuit board layout design should also be highlighted.

Figure 24. Output Ripple Voltage Waveforms



HORTIZONTAL TIME BASE: 10 µs/DIV

Minimizing the Output Ripple

In order to minimise the output ripple voltage it is possible to enlarge the inductance value of the inductor L1 and/or to use a larger value output capacitor. There is also another way to smooth the output by means of an additional LC filter (20 µH, 100 µF), that can be added to the output (see Figure 33) to further reduce the amount of output ripple and transients. With such a filter it is possible to reduce the output ripple voltage transients 10 times or more. Figure 24 shows the difference between filtered and unfiltered output waveforms of the regulator shown in Figure 33.

The upper waveform is from the normal unfiltered output of the converter, while the lower waveform shows the output ripple voltage filtered by an additional LC filter.

Heatsinking and Thermal Considerations

The Through–Hole Package TO–220

The LM2575 is available in two packages, a 5–pin TO–220(T, TV) and a 5–pin surface mount D^{2}PAK(D2T). There are many applications that require no heatsink to keep the LM2575 junction temperature within the allowed operating range. The TO–220 package can be used without a heatsink for ambient temperatures up to approximately 50°C (depending on the output voltage and load current). Higher ambient temperatures require some heatsinking, either to the printed circuit (PC) board or an external heatsink.

The Surface Mount Package D^{2}PAK and its Heatsinking

The other type of package, the surface mount D^{2}PAK, is designed to be soldered to the copper on the PC board. The copper and the board are the heatsink for this package and the other heat producing components, such as the catch diode and inductor. The PC board copper area that the package is soldered to should be at least 0.4 in^2 (or 100 mm^2) and ideally should have 2 or more square inches (1300 mm^2) of 0.0028 inch copper. Additional increasing of copper area beyond approximately 3.0 in^2 (2000 mm^2) will not improve heat dissipation significantly. If further thermal improvements are needed, double sided or multilayer PC boards with large copper areas should be considered.

Thermal Analysis and Design

The following procedure must be performed to determine whether or not a heatsink will be required. First determine:

1. $P_{D(max)}$ maximum regulator power dissipation in the application.
2. $T_{A(max)}$ maximum ambient temperature in the application.
3. $T_{J(max)}$ maximum allowed junction temperature (125°C for the LM2575). For a conservative design, the maximum junction temperature should not exceed 110°C to assure safe operation. For every additional 10°C temperature rise that the junction must withstand, the estimated operating lifetime of the component is halved.
4. $R_{\theta JC}$ package thermal resistance junction–case.
5. $R_{\theta JA}$ package thermal resistance junction–ambient.

(Refer to Absolute Maximum Ratings in this data sheet or $R_{\theta JC}$ and $R_{\theta JA}$ values).

The following formula is to calculate the total power dissipated by the LM2575:

$$P_D = (V_{in} \times I_Q) + d \times I_{Load} \times V_{sat}$$

where d is the duty cycle and for buck converter

$$d = \frac{t_{on}}{T} = \frac{V_O}{V_{in}},$$

I_Q (quiescent current) and V_{sat} can be found in the LM2575 data sheet,

V_{in} is minimum input voltage applied,

V_O is the regulator output voltage,

I_{Load} is the load current.

The dynamic switching losses during turn–on and turn–off can be neglected if proper type catch diode is used.

Packages Not on a Heatsink (Free–Standing)

For a free–standing application when no heatsink is used, the junction temperature can be determined by the following expression:

$$T_J = (R_{\theta JA})(P_D) + T_A$$

where $(R_{\theta JA})(P_D)$ represents the junction temperature rise caused by the dissipated power and T_A is the maximum ambient temperature.

Packages on a Heatsink

If the actual operating junction temperature is greater than the selected safe operating junction temperature determined in step 3, than a heatsink is required. The junction temperature will be calculated as follows:

$$T_J = P_D\,(R_{\theta JA} + R_{\theta CS} + R_{\theta SA}) + T_A$$

where $R_{\theta JC}$ is the thermal resistance junction–case,
$R_{\theta CS}$ is the thermal resistance case–heatsink,
$R_{\theta SA}$ is the thermal resistance heatsink–ambient.

If the actual operating temperature is greater than the selected safe operating junction temperature, then a larger heatsink is required.

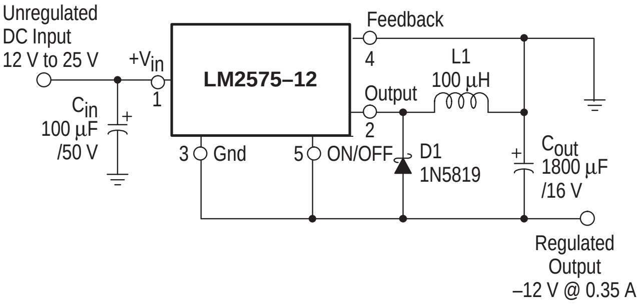
Some Aspects That can Influence Thermal Design

It should be noted that the package thermal resistance and the junction temperature rise numbers are all approximate, and there are many factors that will affect these numbers, such as PC board size, shape, thickness, physical position, location, board temperature, as well as whether the surrounding air is moving or still.

Other factors are trace width, total printed circuit copper area, copper thickness, single– or double–sided, multilayer board, the amount of solder on the board or even colour of the traces.

The size, quantity and spacing of other components on the board can also influence its effectiveness to dissipate the heat.

Figure 25. Inverting Buck–Boost Regulator Using the LM2575–12 Develops –12 V @ 0.35 A



ADDITIONAL APPLICATIONS

Inverting Regulator

An inverting buck–boost regulator using the LM2575–12 is shown in Figure 25. This circuit converts a positive input voltage to a negative output voltage with a common ground by bootstrapping the regulators ground to the negative output voltage. By grounding the feedback pin, the regulator senses the inverted output voltage and regulates it.

In this example the LM2575–12 is used to generate a –12 V output. The maximum input voltage in this case cannot exceed +28 V because the maximum voltage appearing across the regulator is the absolute sum of the input and output voltages and this must be limited to a maximum of 40 V.

This circuit configuration is able to deliver approximately 0.35 A to the output when the input voltage is 12 V or higher. At lighter loads the minimum input voltage required drops to approximately 4.7 V, because the buck–boost regulator topology can produce an output voltage that, in its absolute value, is either greater or less than the input voltage.

Since the switch currents in this buck–boost configuration are higher than in the standard buck converter topology, the available output current is lower.

This type of buck–boost inverting regulator can also require a larger amount of startup input current, even for light loads. This may overload an input power source with a current limit less than 1.5 A.

Such an amount of input startup current is needed for at least 2.0 ms or more. The actual time depends on the output voltage and size of the output capacitor.

Because of the relatively high startup currents required by this inverting regulator topology, the use of a delayed startup or an undervoltage lockout circuit is recommended.

Using a delayed startup arrangement, the input capacitor can charge up to a higher voltage before the switch–mode regulator begins to operate.

The high input current needed for startup is now partially supplied by the input capacitor C_{in}.

Design Recommendations:

The inverting regulator operates in a different manner than the buck converter and so a different design procedure has to be used to select the inductor L1 or the output capacitor C_{out}.

The output capacitor values must be larger than is normally required for buck converter designs. Low input voltages or high output currents require a large value output capacitor (in the range of thousands of µF).

The recommended range of inductor values for the inverting converter design is between 68 µH and 220 µH. To select an inductor with an appropriate current rating, the inductor peak current has to be calculated.

The following formula is used to obtain the peak inductor current:

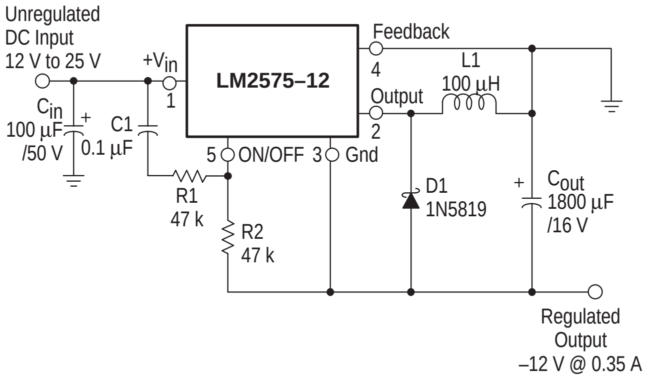
$$I_{peak} \approx \frac{I_{Load}\,(V_{in} + |V_O|)}{V_{in}} + \frac{V_{in} \times t_{on}}{2L_1}$$

where $t_{on} = \frac{|V_O|}{V_{in} + |V_O|} \times \frac{1}{f_{osc}}$, and $f_{osc} = 52$ kHz.

Under normal continuous inductor current operating conditions, the worst case occurs when V_{in} is minimal.

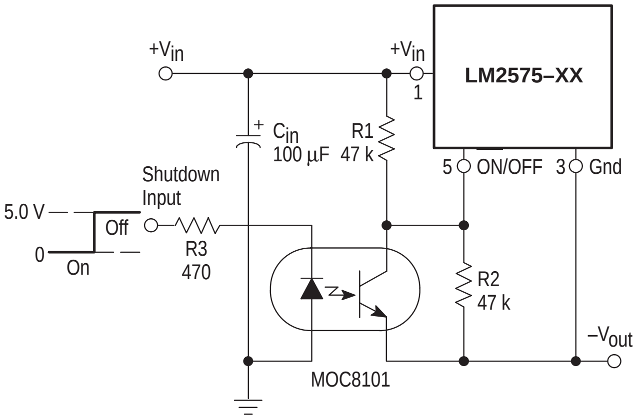
Note that the voltage appearing across the regulator is the absolute sum of the input and output voltage, and must not exceed 40 V.

Figure 26. Inverting Buck–Boost Regulator with Delayed Startup



It has been already mentioned above, that in some situations, the delayed startup or the undervoltage lockout features could be very useful. A delayed startup circuit applied to a buck–boost converter is shown in Figure 26. Figure 31 in the "Undervoltage Lockout" section describes an undervoltage lockout feature for the same converter topology.

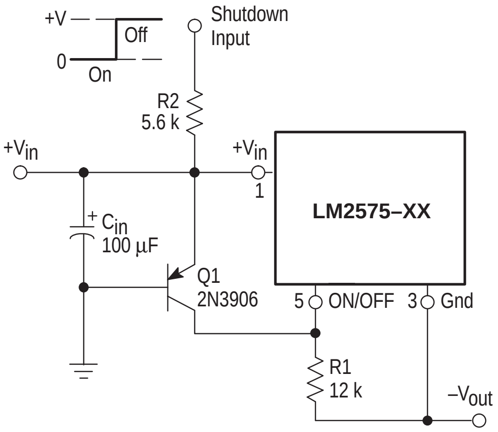
Figure 27. Inverting Buck–Boost Regulator Shut Down Circuit Using an Optocoupler



NOTE: This picture does not show the complete circuit.

With the inverting configuration, the use of the $\overline{\text{ON}}$/OFF pin requires some level shifting techniques. This is caused by the fact, that the ground pin of the converter IC is no longer at ground. Now, the $\overline{\text{ON}}$/OFF pin threshold voltage (1.4 V approximately) has to be related to the negative output voltage level. There are many different possible shut down methods, two of them are shown in Figures 27 and 28.

Figure 28. Inverting Buck–Boost Regulator Shut Down Circuit Using a PNP Transistor



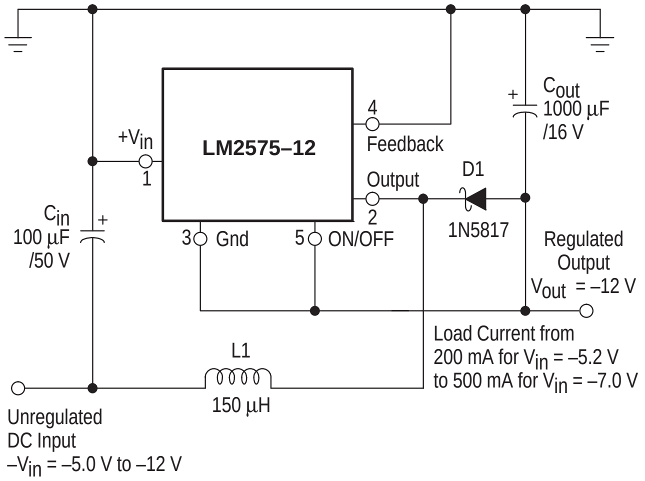
NOTE: This picture does not show the complete circuit.

Negative Boost Regulator

This example is a variation of the buck–boost topology and is called a negative boost regulator. This regulator experiences relatively high switch current, especially at low input voltages. The internal switch current limiting results in lower output load current capability.

The circuit in Figure 29 shows the negative boost configuration. The input voltage in this application ranges from –5.0 V to –12 V and provides a regulated –12 V output. If the input voltage is greater than –12 V, the output will rise above –12 V accordingly, but will not damage the regulator.

Figure 29. Negative Boost Regulator



Design Recommendations:

The same design rules as for the previous inverting buck–boost converter can be applied. The output capacitor C_{out} must be chosen larger than would be required for a standard buck converter. Low input voltages or high output currents require a large value output capacitor (in the range of thousands of µF). The recommended range of inductor values for the negative boost regulator is the same as for inverting converter design.

Another important point is that these negative boost converters cannot provide current limiting load protection in the event of a short in the output so some other means, such as a fuse, may be necessary to provide the load protection.

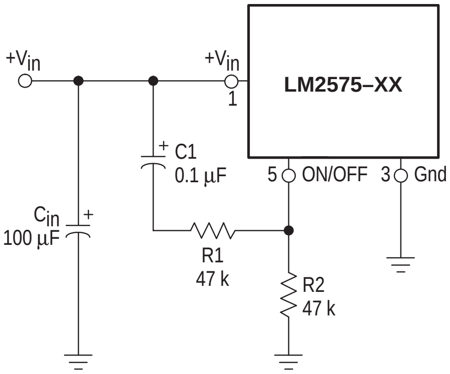
Delayed Startup

There are some applications, like the inverting regulator already mentioned above, which require a higher amount of startup current. In such cases, if the input power source is limited, this delayed startup feature becomes very useful.

To provide a time delay between the time the input voltage is applied and the time when the output voltage comes up, the circuit in Figure 30 can be used. As the input voltage is applied, the capacitor C1 charges up, and the voltage across the resistor R2 falls down. When the voltage on the ON/OFF pin falls below the threshold value 1.4 V, the regulator starts up. Resistor R1 is included to limit the maximum voltage applied to the ON/OFF pin, reduces the power supply noise sensitivity, and also limits the capacitor C1 discharge current, but its use is not mandatory.

When a high 50 Hz or 60 Hz (100 Hz or 120 Hz respectively) ripple voltage exists, a long delay time can cause some problems by coupling the ripple into the ON/OFF pin, the regulator could be switched periodically on and off with the line (or double) frequency.

Figure 30. Delayed Startup Circuitry



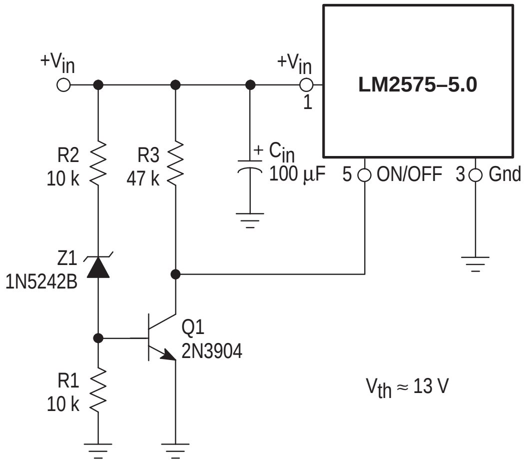
NOTE: This picture does not show the complete circuit.

Undervoltage Lockout

Some applications require the regulator to remain off until the input voltage reaches a certain threshold level. Figure 31 shows an undervoltage lockout circuit applied to a buck regulator. A version of this circuit for buck–boost converter is shown in Figure 32. Resistor R3 pulls the $\overline{\text{ON}}$/OFF pin high and keeps the regulator off until the input voltage reaches a predetermined threshold level, which is determined by the following expression:

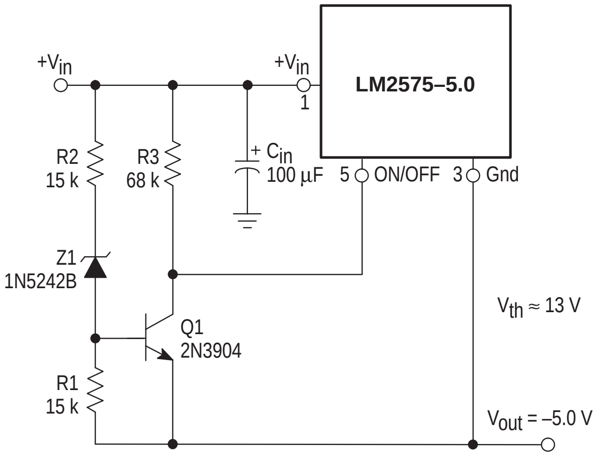
$$V_{th} \approx V_{Z1} + \left(1 + \frac{R2}{R1}\right) V_{BE}\ (Q1)$$

Figure 31. Undervoltage Lockout Circuit for Buck Converter



NOTE: This picture does not show the complete circuit.

Figure 32. Undervoltage Lockout Circuit for Buck–Boost Converter



NOTE: This picture does not show the complete circuit.

Adjustable Output, Low–Ripple Power Supply

A 1.0 A output current capability power supply that features an adjustable output voltage is shown in Figure 33.

This regulator delivers 1.0 A into 1.2 V to 35 V output. The input voltage ranges from roughly 8.0 V to 40 V. In order to achieve a 10 or more times reduction of output ripple, an additional L–C filter is included in this circuit.

Figure 33. Adjustable Power Supply with Low Ripple Voltage

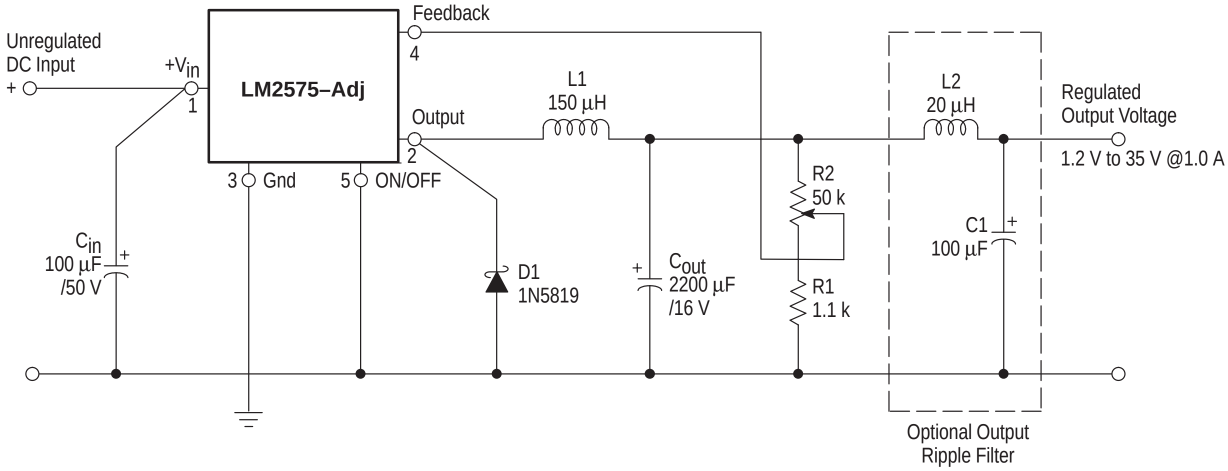
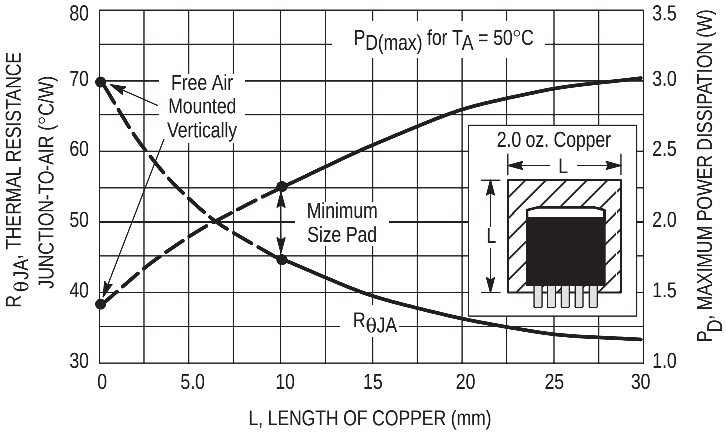
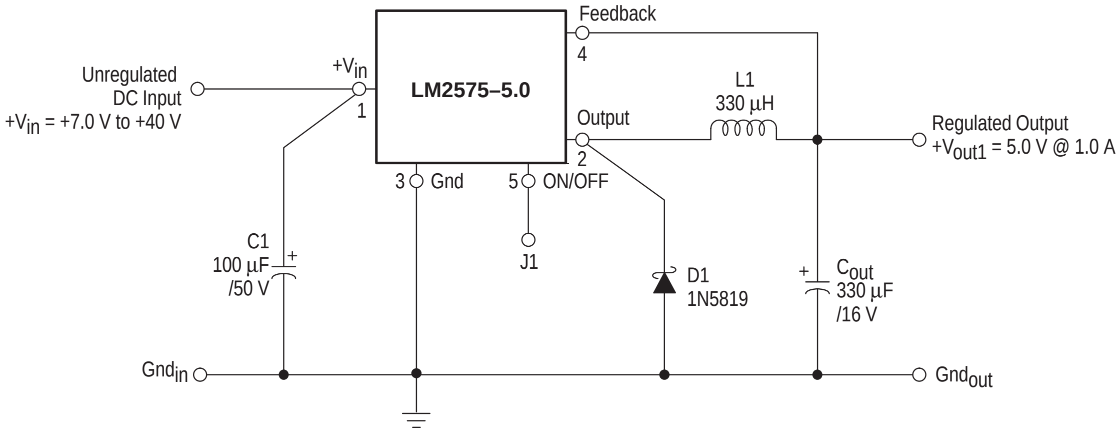


Figure 34. D^2PAK Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length



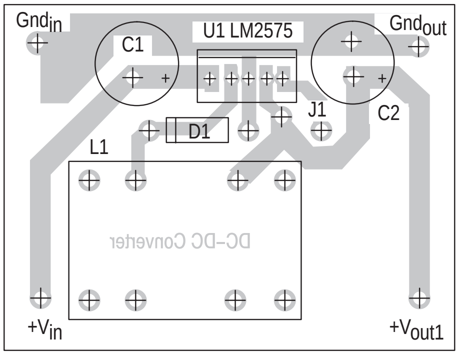
THE LM2575–5.0 STEP–DOWN VOLTAGE REGULATOR WITH 5.0 V @ 1.0 A OUTPUT POWER CAPABILITY. TYPICAL APPLICATION WITH THROUGH–HOLE PC BOARD LAYOUT

Figure 35. Schematic Diagram of the LM2575–5.0 Step–Down Converter



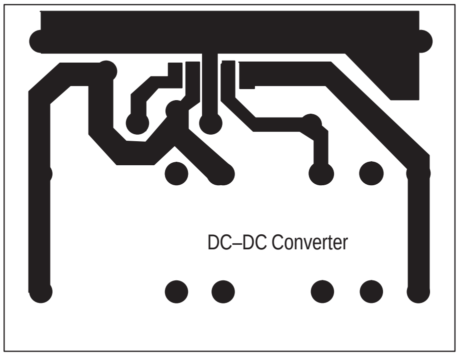
C1 – 100 µF, 50 V, Aluminium Electrolytic
C2 – 330 µF, 16 V, Aluminium Electrolytic
D1 – 1.0 A, 40 V, Schottky Rectifier, 1N5819
L1 – 330 µH, Tech 39: 77 458 BV, Toroid Core, Through–Hole, Pin 3 = Start, Pin 7 = Finish

Figure 36. Printed Circuit Board Component Side



NOTE: Not to scale.

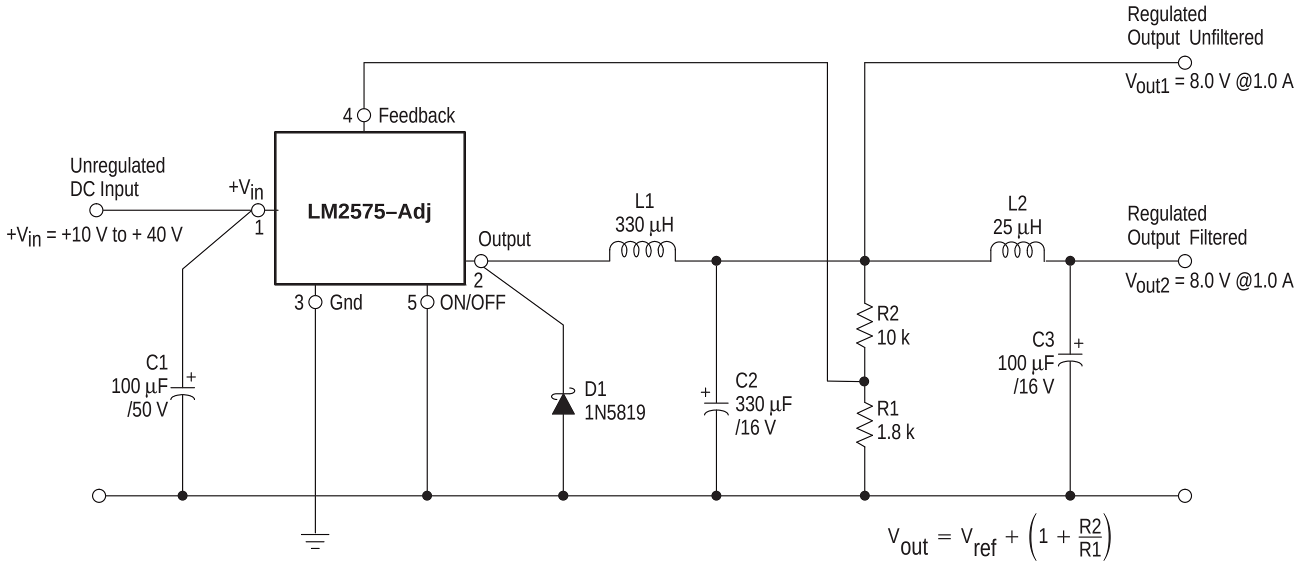
Figure 37. Printed Circuit Board Copper Side



NOTE: Not to scale.

THE LM2575–ADJ STEP–DOWN VOLTAGE REGULATOR WITH 8.0 V @ 1.0 A OUTPUT POWER CAPABILITY. TYPICAL APPLICATION WITH THROUGH–HOLE PC BOARD LAYOUT

Figure 38. Schematic Diagram of the 8.0 V @ 1.0 V Step–Down Converter Using the LM2575–Adj
(An additional LC filter is included to achieve low output ripple voltage)

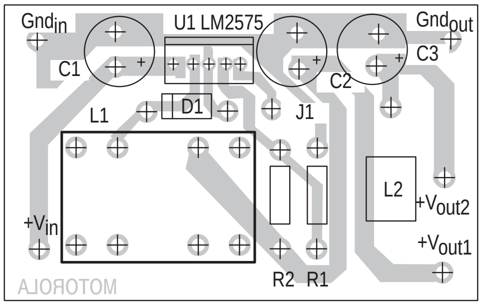


$$V_{out} = V_{ref} + \left(1 + \frac{R2}{R1}\right)$$

V_{ref} = 1.23 V
R1 is between 1.0 k and 5.0 k

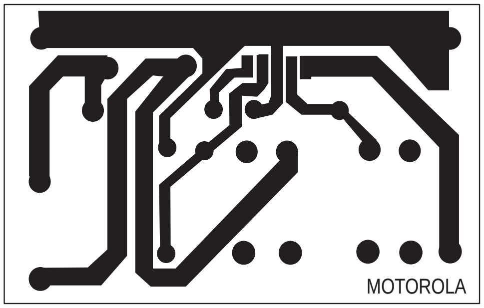
C1 – 100 µF, 50 V, Aluminium Electrolytic
C2 – 330 µF, 16 V, Aluminium Electrolytic
C3 – 100 µF, 16 V, Aluminium Electrolytic
D1 – 1.0 A, 40 V, Schottky Rectifier, 1N5819
L1 – 330 µH, Tech 39: 77 458 BV, Toroid Core, Through–Hole, Pin 3 = Start, Pin 7 = Finish
L2 – 25 µH, TDK: SFT52501, Toroid Core, Through–Hole
R1 – 1.8 k
R2 – 10 k

Figure 39. PC Board Component Side



NOTE: Not to scale.

Figure 40. PC Board Copper Side



NOTE: Not to scale.

References

- National Semiconductor LM2575 Data Sheet and Application Note
- National Semiconductor LM2595 Data Sheet and Application Note
- Marty Brown “Pratical Switching Power Supply Design”, Academic Press, Inc., San Diego 1990
- Ray Ridley “High Frequency Magnetics Design”, Ridley Engineering, Inc. 1995

MOTOROLA

LM2931 Series

Low Dropout Voltage Regulators

LOW DROPOUT VOLTAGE REGULATORS

The LM2931 series consists of positive fixed and adjustable output voltage regulators that are specifically designed to maintain proper regulation with an extremely low input–to–output voltage differential. These devices are capable of supplying output currents in excess of 100 mA and feature a low bias current of 0.4 mA at 10 mA output.

Designed primarily to survive in the harsh automotive environment, these devices will protect all external load circuitry from input fault conditions caused by reverse battery connection, two battery jump starts, and excessive line transients during load dump. This series also includes internal current limiting, thermal shutdown, and additionally, is able to withstand temporary power–up with mirror–image insertion.

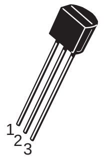
Due to the low dropout voltage and bias current specifications, the LM2931 series is ideally suited for battery powered industrial and consumer equipment where an extension of useful battery life is desirable. The ‘C’ suffix adjustable output regulators feature an output inhibit pin which is extremely useful in microprocessor–based systems.

- Input–to–Output Voltage Differential of < 0.6 V @ 100 mA
- Output Current in Excess of 100 mA
- Low Bias Current
- 60 V Load Dump Protection
- –50 V Reverse Transient Protection
- Internal Current Limiting with Thermal Shutdown
- Temporary Mirror–Image Protection
- Ideally Suited for Battery Powered Equipment
- Economical 5–Lead TO–220 Package with Two Optional Leadforms
- Available in Surface Mount SOP–8, D^{2}PAK and DPAK Packages

(See Following Page for Ordering Information.)

FIXED OUTPUT VOLTAGE

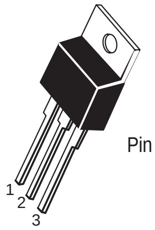
Z SUFFIX
PLASTIC PACKAGE
CASE 29



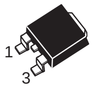
Pin 1. Output
2. Ground
3. Input

T SUFFIX
PLASTIC PACKAGE
CASE 221A

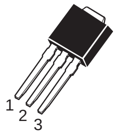
Heatsink surface
connected to Pin 2.



Pin 1. Input
2. Ground
3. Output

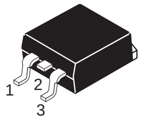


DT SUFFIX
PLASTIC PACKAGE
CASE 369A
(DPAK)



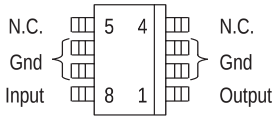
DT–1 SUFFIX
PLASTIC PACKAGE
CASE 369
(DPAK)

D2T SUFFIX
PLASTIC PACKAGE
CASE 936
(D^{2}PAK)

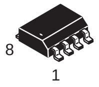


Heatsink surface (shown as terminal 4 in
case outline drawing) is connected to Pin 2.

FIXED

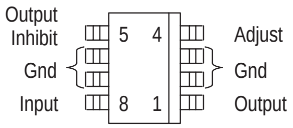


(Top View)



D SUFFIX
PLASTIC PACKAGE
CASE 751
(SOP–8)

ADJUSTABLE

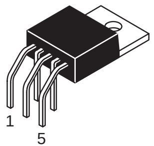


(Top View)

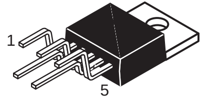
ADJUSTABLE OUTPUT VOLTAGE

Pin 1. Adjust
2. Output Inhibit
3. Ground
4. Input
5. Output

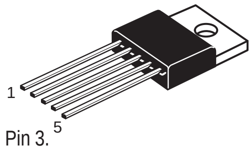
TH SUFFIX
PLASTIC PACKAGE
CASE 314A



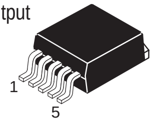
TV SUFFIX
PLASTIC PACKAGE
CASE 314B



T SUFFIX
PLASTC PACKAGE
CASE 314D



Heatsink surface connected to Pin 3.



D2T SUFFIX
PLASTIC PACKAGE
CASE 936A
(D^{2}PAK)

Heatsink surface (shown as
terminal 6 in case outline
drawing) is connected to Pin 3.

ORDERING INFORMATION

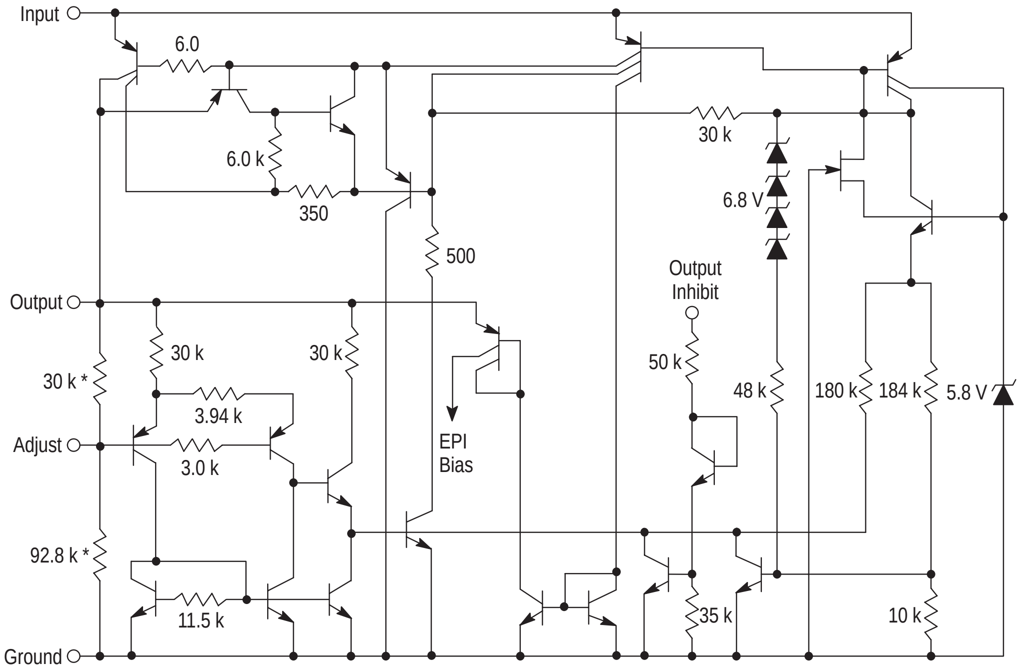
Device	Output		Case	Package
	Voltage	Tolerance		
LM2931AD–5.0	5.0 V	± 3.8%	751	SOP–8 Surface Mount
LM2931ADT–5.0			369A	Surface Mount DPAK
LM2931ADT–1–5.0			369	DPAK
LM2931AD2T–5.0			936	Surface Mount D^{2}PAK
LM2931AT–5.0			221A	TO–220 Type
LM2931AZ–5.0			29	TO–92 Type
LM2931D–5.0		± 5.0%	751	SOP–8 Surface Mount
LM2931D2T–5.0			936	Surface Mount D^{2}PAK
LM2931DT–5.0			369A	Surface Mount DPAK
LM2931DT–1–5.0			369	DPAK
LM2931T–5.0			221A	TO–220 Type
LM2931Z–5.0			29	TO–92 Type
LM2931CD	Adjustable		751	SOP–8 Surface Mount
LM2931CD2T			936A	Surface Mount D^{2}PAK
LM2931CT			314D	5–Pin TO–220 Type
LM2931CTH			314A	5–Pin Horizontal Leadform
LM2931CTV			314B	5–Pin Vertical Leadform

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage Continuous	V_I	40	Vdc
Transient Input Voltage ($\tau \leq 100$ ms)	$V_I(\tau)$	60	Vpk
Transient Reverse Polarity Input Voltage 1.0% Duty Cycle, $\tau \leq 100$ ms	$-V_I(\tau)$	–50	Vpk
Power Dissipation			
Case 29 (TO–92 Type)			
$T_A = 25°C$	P_D	Internally Limited	W
Thermal Resistance, Junction–to–Ambient	$R_{\theta JA}$	178	°C/W
Thermal Resistance, Junction–to–Case	$R_{\theta JC}$	83	°C/W
Case 221A, 314A, 314B and 314D (TO–220 Type)			
$T_A = 25°C$	P_D	Internally Limited	W
Thermal Resistance, Junction–to–Ambient	$R_{\theta JA}$	65	°C/W
Thermal Resistance, Junction–to–Case	$R_{\theta JC}$	5.0	°C/W
Case 369 and 369A (DPAK) [Note 1]			
$T_A = 25°C$	P_D	Internally Limited	W
Thermal Resistance, Junction–to–Ambient	$R_{\theta JA}$	92	°C/W
Thermal Resistance, Junction–to–Case	$R_{\theta JC}$	6.0	°C/W
Case 751 (SOP–8) [Note 2]			
$T_A = 25°C$	P_D	Internally Limited	W
Thermal Resistance, Junction–to–Ambient	$R_{\theta JA}$	160	°C/W
Thermal Resistance, Junction–to–Case	$R_{\theta JC}$	25	°C/W
Case 936 and 936A (D^{2}PAK) [Note 3]			
$T_A = 25°C$	P_D	Internally Limited	W
Thermal Resistance, Junction–to–Ambient	$R_{\theta JA}$	70	°C/W
Thermal Resistance, Junction–to–Case	$R_{\theta JC}$	5.0	°C/W
Tested Operating Junction Temperature Range	T_J	–40 to +125	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

NOTES: 1. DPAK Junction–to–Ambient Thermal Resistance is for vertical mounting. Refer to Figure 23 for board mounted Thermal Resistance.
2. SOP–8 Junction–to–Ambient Thermal Resistance is for minimum recommended pad size. Refer to Figure 23 for Thermal Resistance variation versus pad size.
3. D^{2}PAK Junction–to–Ambient Thermal Resistance is for vertical mounting. Refer to Figure 25 for board mounted Thermal Resistance.

Representative Schematic Diagram



*Deleted on Adjustable Regulators

This device contains 26 active transistors.

ELECTRICAL CHARACTERISTICS (V_{in} = 14 V, I_O = 10 mA, C_O = 100 µF, $C_{O(ESR)}$ = 0.3 Ω, T_J = 25°C [Note 4].)

Characteristic	Symbol	LM2931–5.0			LM2931A–5.0			Unit
		Min	Typ	Max	Min	Typ	Max	
FIXED OUTPUT								
Output Voltage V_{in} = 14 V, I_O = 10 mA, T_J = 25°C V_{in} = 6.0 V to 26 V, $I_O \le$ 100 mA, T_J = –40° to +125°C	V_O	 4.75 4.50	 5.0 –	 5.25 5.50	 4.81 4.75	 5.0 –	 5.19 5.25	V
Line Regulation V_{in} = 9.0 V to 16 V V_{in} = 6.0 V to 26 V	Reg_{line}	 – –	 2.0 4.0	 10 30	 – –	 2.0 4.0	 10 30	mV
Load Regulation (I_O = 5.0 mA to 100 mA)	Reg_{load}	–	14	50	–	14	50	mV
Output Impedance I_O = 10 mA, ΔI_O = 1.0 mA, f = 100 Hz to 10 kHz	Z_O	 –	 200	 –	 –	 200	 –	mΩ
Bias Current V_{in} = 14 V, I_O = 100 mA, T_J = 25°C V_{in} = 6.0 V to 26 V, I_O = 10 mA, T_J = –40° to +125°C	I_B	 – –	 5.8 0.4	 30 1.0	 – –	 5.8 0.4	 30 1.0	mA
Output Noise Voltage (f = 10 Hz to 100 kHz)	V_n	–	700	–	–	700	–	µVrms
Long Term Stability	S	–	20	–	–	20	–	mV/kHR
Ripple Rejection (f = 120 Hz)	RR	60	90	–	60	90	–	dB
Dropout Voltage I_O = 10 mA I_O = 100 mA	$V_I–V_O$	 – –	 0.015 0.16	 0.2 0.6	 – –	 0.015 0.16	 0.2 0.6	V
Over–Voltage Shutdown Threshold	$V_{th(OV)}$	26	29.5	40	26	29.5	40	V
Output Voltage with Reverse Polarity Input (V_{in} = –15 V)	$–V_O$	–0.3	0	–	–0.3	0	–	V

NOTE: 4. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.

ELECTRICAL CHARACTERISTICS (V_{in} = 14 V, V_O = 3.0 V, I_O = 10 mA, R_1 = 27 k, C_O = 100 µF, $C_{O(ESR)}$ = 0.3 Ω, T_J = 25°C [Note 4].)

Characteristic	Symbol	LM2931C			Unit
		Min	Typ	Max	
ADJUSTABLE OUTPUT					
Reference Voltage (Note 5, Figure 18)	V_{ref}				V
I_O = 10 mA, T_J = 25°C		1.14	1.20	1.26	
I_O ≤ 100 mA, T_J = –40 to +125°C		1.08	–	1.32	
Output Voltage Range	$V_{O\ range}$	3.0 to 24	2.7 to 29.5	–	V
Line Regulation (V_{in} = V_O + 0.6 V to 26 V)	Reg_{line}	–	0.2	1.5	mV/V
Load Regulation (I_O = 5.0 mA to 100 mA)	Reg_{load}	–	0.3	1.0	%/V
Output Impedance	Z_O				mΩ/V
I_O = 10 mA, ΔI_O = 1.0 mA, f = 10 Hz to 10 kHz		–	40	–	
Bias Current	I_B				mA
I_O = 100 mA		–	6.0	–	
I_O = 10 mA		–	0.4	1.0	
Output Inhibited ($V_{th(OI)}$ = 2.5 V)		–	0.2	1.0	
Adjustment Pin Current	I_{Adj}	–	0.2	–	µA
Output Noise Voltage (f = 10 Hz to 100 kHz)	V_n	–	140	–	µVrms/V
Long–Term Stability	S	–	0.4	–	%/kHR
Ripple Rejection (f = 120 Hz)	RR	0.10	0.003	–	%/V
Dropout Voltage	V_I–V_O				V
I_O = 10 mA		–	0.015	0.2	
I_O = 100 mA		–	0.16	0.6	
Over–Voltage Shutdown Threshold	$V_{th(OV)}$	26	29.5	40	V
Output Voltage with Reverse Polarity Input (V_{in} = –15 V)	$-V_O$	–0.3	0	–	V
Output Inhibit Threshold Voltages	$V_{th(OI)}$				V
Output “On”: T_J = 25°C		–	2.15	1.90	
T_J = –40° to +125°C		–	–	1.20	
Output “Off”: T_J = 25°C		2.50	2.26	–	
T_J = –40° to +125°C		3.25	–	–	
Output Inhibit Threshold Current ($V_{th(OI)}$ = 2.5 V)	$I_{th(OI)}$	–	30	50	µA

NOTES: 4. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
5. The reference voltage on the adjustable device is measured from the output to the adjust pin across R_1.

Figure 1. Dropout Voltage versus Output Current

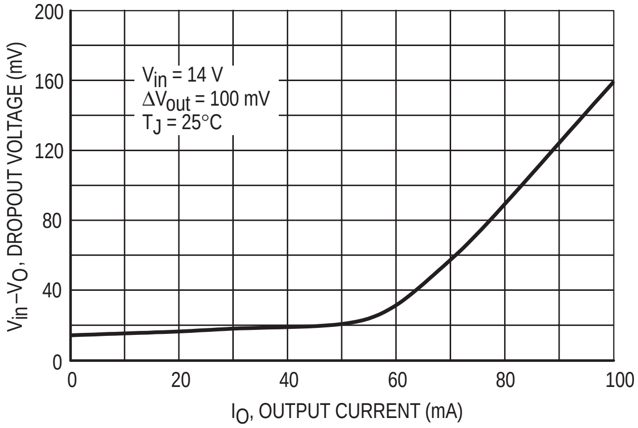


Figure 2. Dropout Voltage versus Junction Temperature

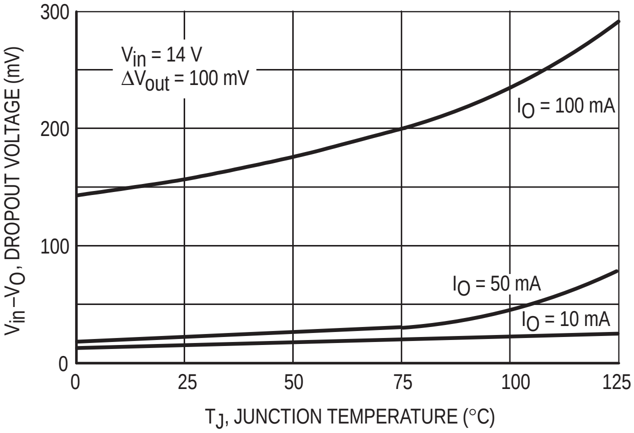


Figure 3. Peak Output Current versus Input Voltage

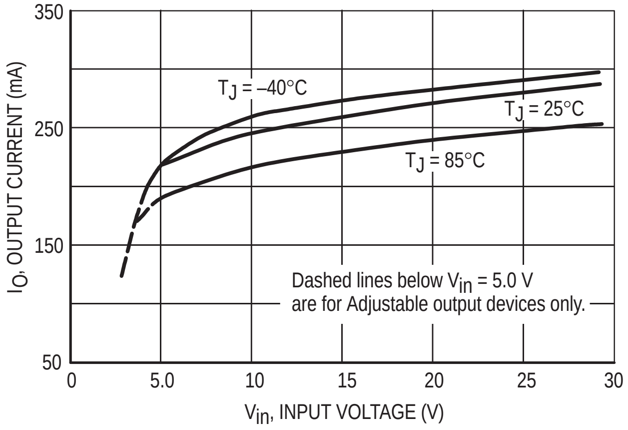


Figure 4. Output Voltage versus Input Voltage

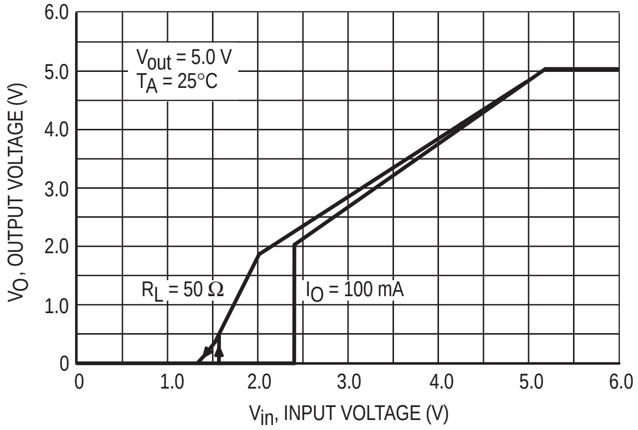


Figure 5. Output Voltage versus Input Voltage

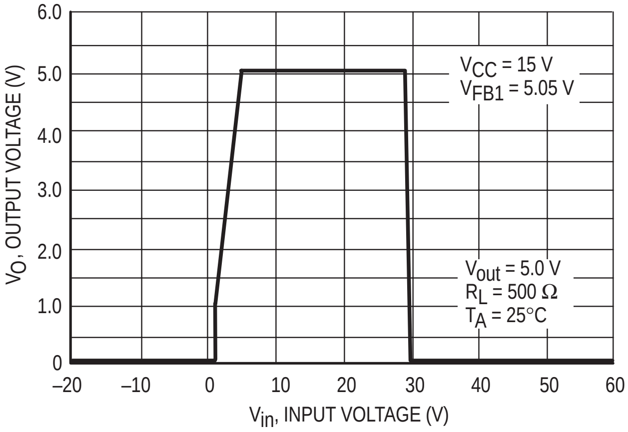


Figure 6. Load Dump Characteristics

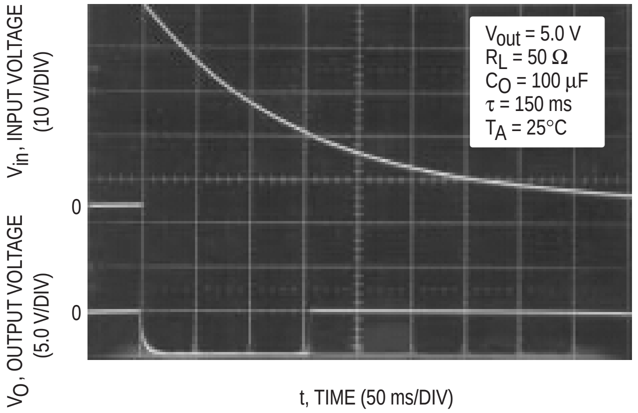


Figure 7. Bias Current versus Input Voltage

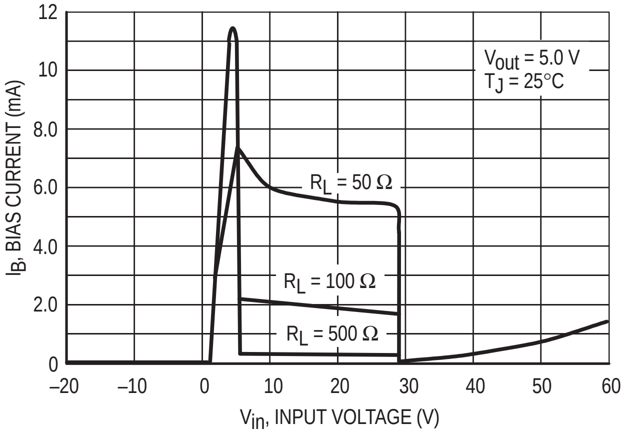


Figure 8. Bias Current versus Output Current

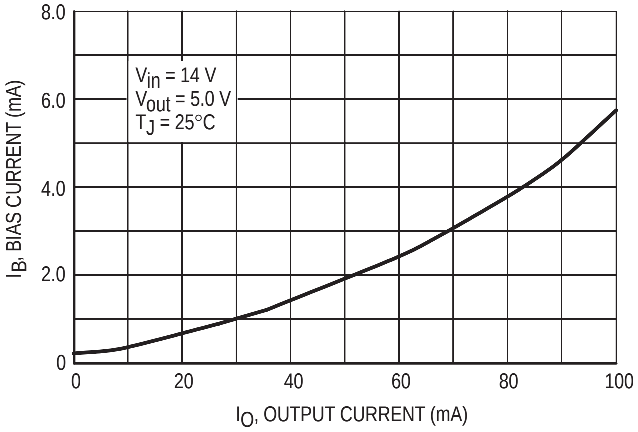


Figure 9. Bias Current versus Junction Temperature

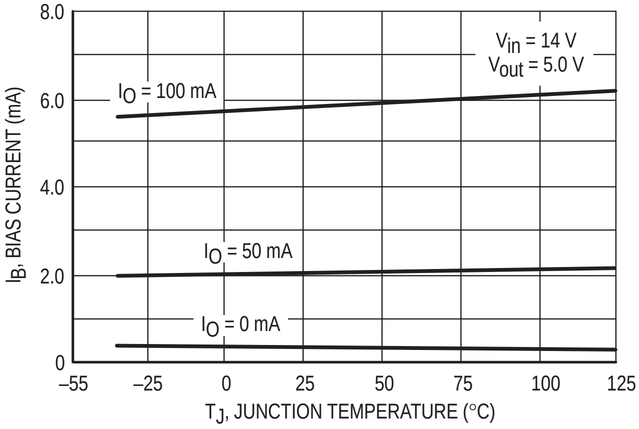


Figure 10. Output Impedance versus Frequency

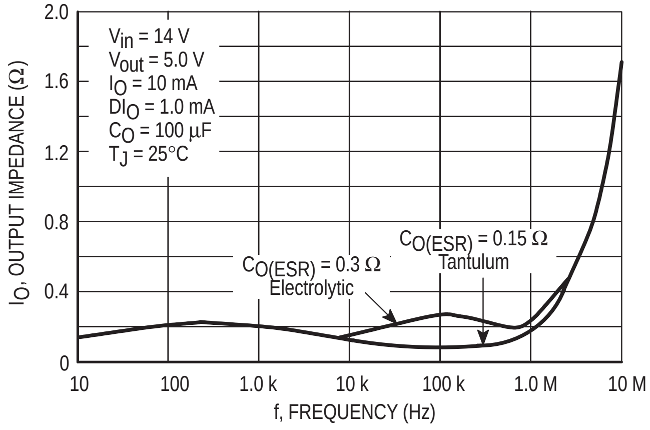


Figure 11. Ripple Rejection versus Frequency

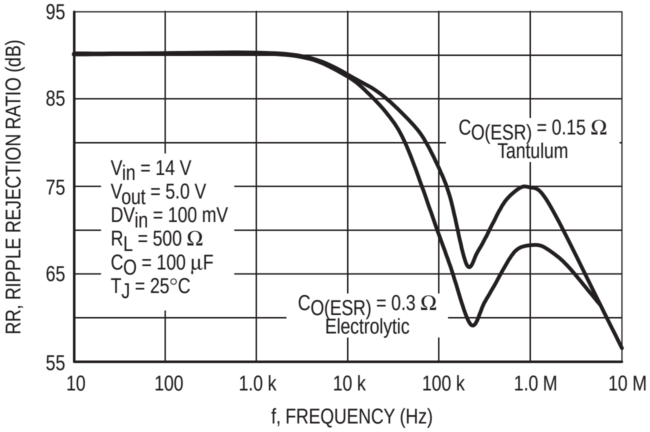


Figure 12. Ripple Rejection versus Output Current

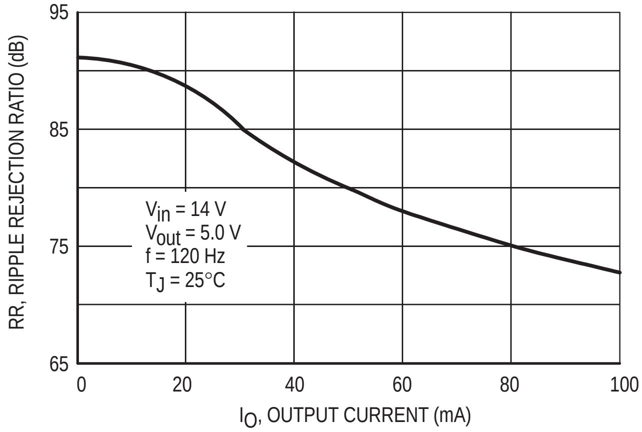


Figure 13. Line Regulation

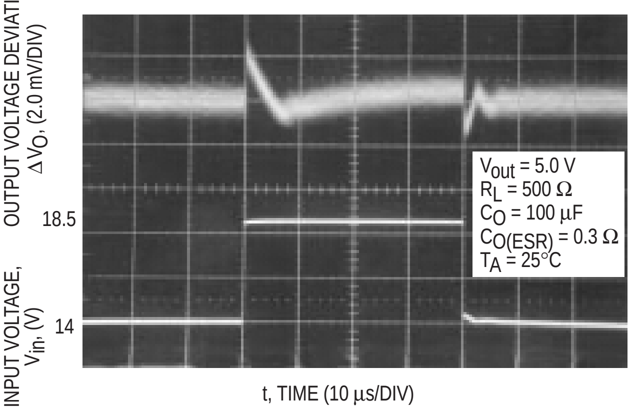


Figure 14. Load Regulation

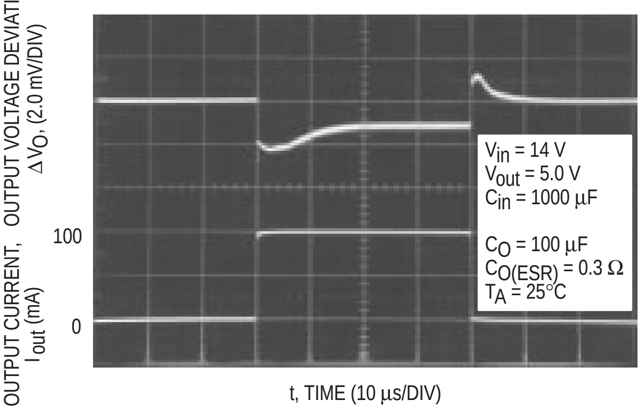


Figure 15. Reference Voltage versus Output Voltage

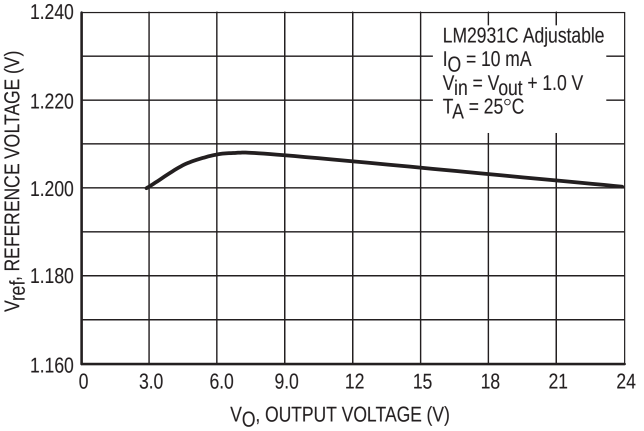
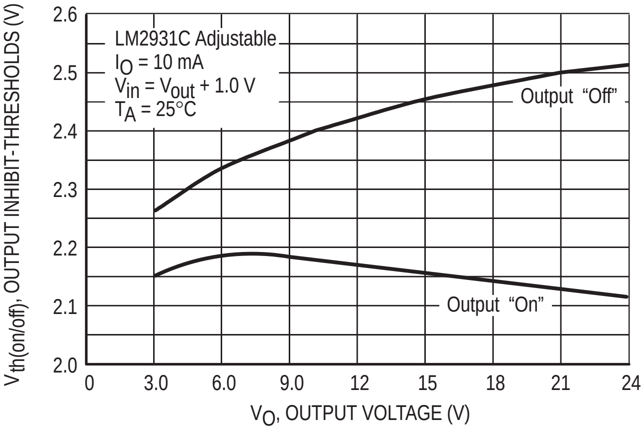


Figure 16. Output Inhibit–Thresholds versus Output Voltage



APPLICATIONS INFORMATION

The LM2931 series regulators are designed with many protection features making them essentially blow–out proof. These features include internal current limiting, thermal shutdown, overvoltage and reverse polarity input protection, and the capability to withstand temporary power–up with mirror–image insertion. Typical application circuits for the fixed and adjustable output device are shown in Figures 17 and 18.

The input bypass capacitor C_{in} is recommended if the regulator is located an appreciable distance (≥ 4″) from the supply input filter. This will reduce the circuit's sensitivity to the input line impedance at high frequencies.

This regulator series is not internally compensated and thus requires an external output capacitor for stability. The capacitance value required is dependent upon the load current, output voltage for the adjustable regulator, and the type of capacitor selected. The least stable condition is encountered at maximum load current and minimum output voltage. Figure 22 shows that for operation in the "Stable" region, under the conditions specified, the magnitude of the output capacitor impedance $|Z_O|$ must not exceed 0.4 Ω. This limit must be observed over the entire operating temperature range of the regulator circuit.

With economical electrolytic capacitors, cold temperature operation can pose a serious stability problem. As the electrolyte freezes, around –30°C, the capacitance will decrease and the equivalent series resistance (ESR) will increase drastically, causing the circuit to oscillate. Quality electrolytic capacitors with extended temperature ranges of –40° to +85°C and –55° to +105°C are readily available. Solid tantalum capacitors may be a better choice if small size is a requirement, however, the maximum $|Z_O|$ limit over temperature must be observed.

Note that in the stable region, the output noise voltage is linearly proportional to $|Z_O|$. In effect, C_O dictates the high frequency roll–off point of the circuit. Operation in the area titled "Marginally Stable" will cause the output of the regulator to exhibit random bursts of oscillation that decay in an under–damped fashion. Continuous oscillation occurs when operating in the area titled "Unstable". It is suggested that oven testing of the entire circuit be performed with maximum load, minimum input voltage, and minimum ambient temperature.

Figure 17. Fixed Output Regulator

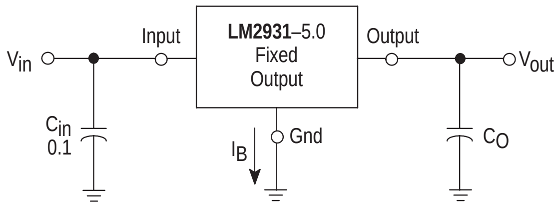
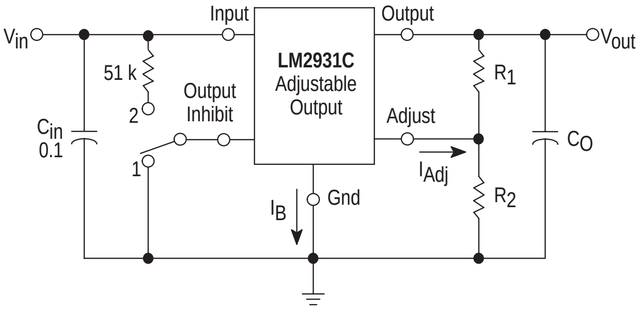


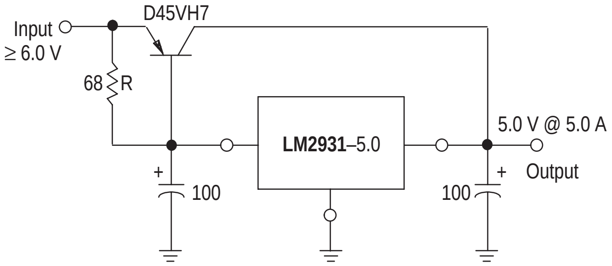
Figure 18. Adjustable Output Regulator



Switch Position 1 = Output “On”, 2 = Output “Off”

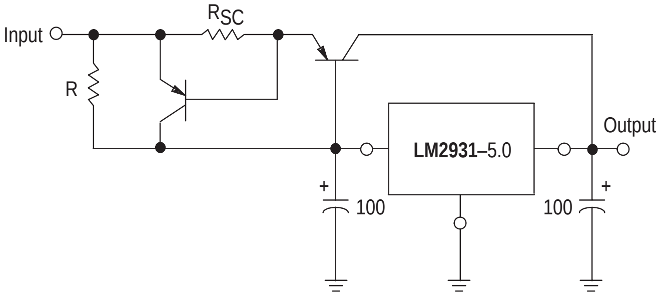
$$V_{out} = V_{ref}\left(1 + \frac{R_2}{R_1}\right) + I_{Adj}\,R_2 \qquad 22.5\ k \geq \frac{R_1\,R_2}{R_1 + R_2}$$

Figure 19. (5.0 A) Low Differential Voltage Regulator



The LM2931 series can be current boosted with a PNP transistor. The D45VH7, on a heatsink, will provide an output current of 5.0 A with an input to output voltage differential of approximately 1.0 V. Resistor R in conjunction with the V_{BE} of the PNP determines when the pass transistor begins conducting. This circuit is not short circuit proof.

Figure 20. Current Boost Regulator with Short Circuit Projection



The circuit of Figure 19 can be modified to provide supply protection against short circuits by adding the current sense resistor R_{SC} and an additional PNP transistor. The current sensing PNP must be capable of handling the short circuit current of the LM2931. Safe operating area of both transistors must be considered under worst case conditions.

Figure 21. Constant Intensity Lamp Flasher

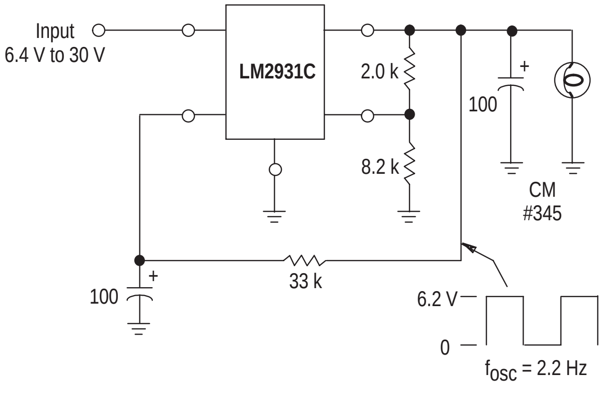


Figure 22. Output Noise Voltage versus Output Capacitor Impedance

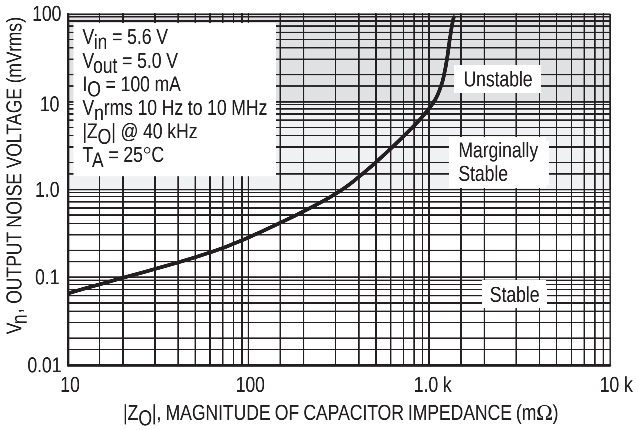


Figure 23. SOP–8 Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length

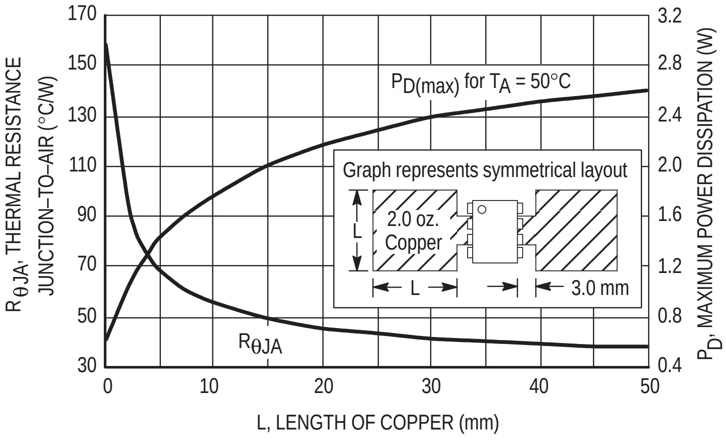


Figure 24. DPAK Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length

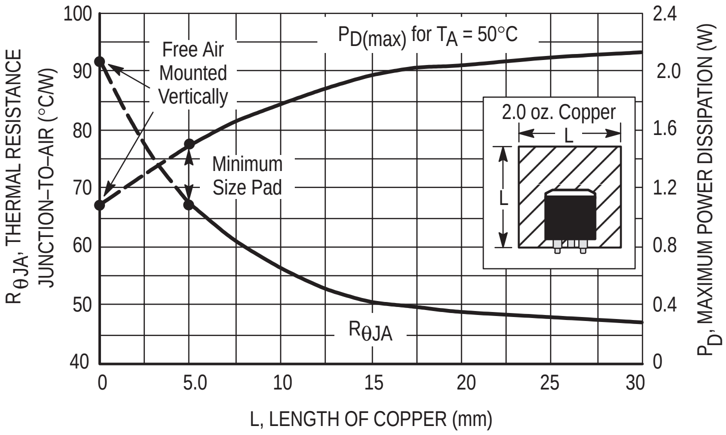
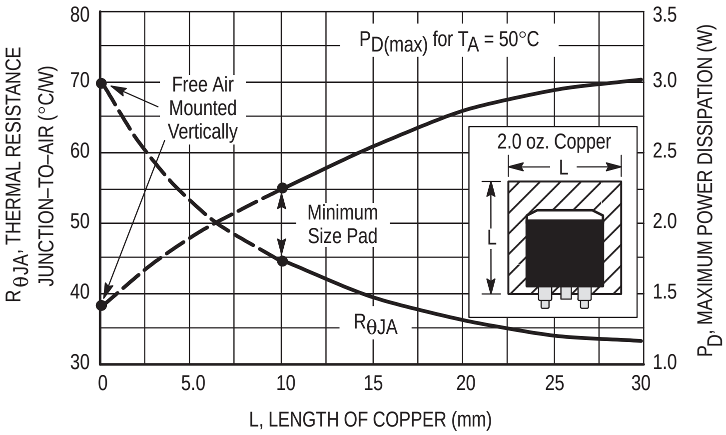


Figure 25. 3–Pin and 5–Pin D²PAK Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length



DEFINITIONS

Dropout Voltage – The input/output voltage differential at which the regulator output no longer maintains regulation against further reductions in input voltage. Measured when the output decreases 100 mV from nominal value at 14 V input, dropout voltage is affected by junction temperature and load current.

Line Regulation – The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

Load Regulation – The change in output voltage for a change in load current at constant chip temperature.

Maximum Power Dissipation – The maximum total device dissipation for which the regulator will operate within specifications.

Bias Current – That part of the input current that is not delivered to the load.

Output Noise Voltage – The rms AC voltage at the output, with constant load and no input ripple, measured over a specified frequency range.

Long–Term Stabliity – Output voltage stability under accelerated life test conditions with the maximum rated voltage listed in the devices electrical characteristics and maximum power dissipation.

MOTOROLA

LM2935

Low Dropout Dual Voltage Regulator

The LM2935 is a dual positive 5.0 V low dropout voltage regulator, designed for standby power systems. The main output is capable of supplying 750 mA for microprocessor power, and can be turned “on” and “off” by the switch/reset input. The other output is dedicated for standby operation of volatile memory, and is capable of supplying up to 10 mA loads. The total device features a low quiescent current of 3.0 mA or less when supplying 10 mA from the standby output.

This part was designed for harsh automotive environments and is therefore immune to many input supply voltage problems such as reverse battery (–12 V), double battery (+24 V), and load dump transients (+60 V).

- Two Regulated 5.0 V Outputs
- Main Output Current in Excess of 750 mA
- On/Off Control of Main Output
- Standby Output Current in Excess of 10 mA
- Low Input/Output Differential of Less than 0.6 V at 500 mA
- Short Circuit Current Limiting
- Internal Thermal Shutdown
- Low Voltage Indicator Output
- Designed for Automotive Environment Including
  - Reverse Battery Protection
  - Double Battery Protection
  - Load Dump Protection
  - Reverse Transient Protection
- Economical 5–Lead TO–220 Package with Two Optional Leadforms
- Also Available in Surface Mount D^{2}PAK Package

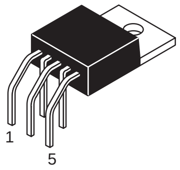
ORDERING INFORMATION

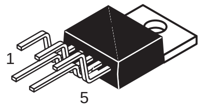
Device	Operating Temperature Range	Package
LM2935D2T	T_J = –40° to +125°C	Surface Mount
LM2935T		Plastic Power
LM2935TH		Horizontal Mount
LM2935TV		Vertical Mount

LOW DROPOUT DUAL VOLTAGE REGULATOR

SEMICONDUCTOR TECHNICAL DATA

TH SUFFIX
PLASTIC PACKAGE
CASE 314A

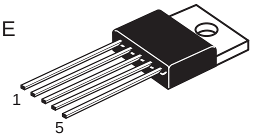




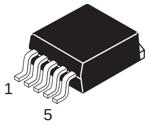
TV SUFFIX
PLASTIC PACKAGE
CASE 314B

Heatsink surface connected to Pin 3.

T SUFFIX
PLASTIC PACKAGE
CASE 314D



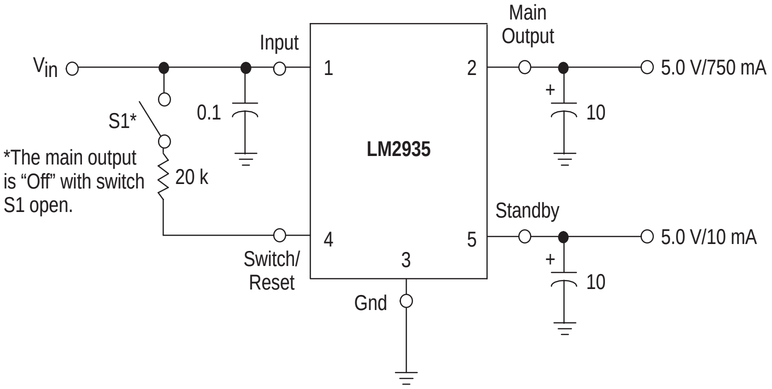
Pin 1. Input Voltage/V_{CC}
2. Main Output
3. Ground
4. Switch/Reset
5. Standby/Output



D2T SUFFIX
PLASTIC PACKAGE
CASE 936A
(D^{2}PAK)

Heatsink surface (shown as terminal 6 in case outline drawing) is connected to Pin 3.

Typical Application Circuit



An input bypass capacitor is recommended if the regulator is located more than 4″ from the supply input filter. The LM2935 is not internally compensated and thus requires an external output capacitor for stability. A minimum capacitance of 10 µF is recommended. The actual capacitance value is dependent upon load current, temperature, and the capacitor’s equivalent series resistance (ESR). The least stable condition is encountered at maximum load current and minimum ambient temperature.

This device contains 29 active transistors.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage Continuous	V_I	60	Vdc
Transient Reverse Polarity Input Voltage 1.0% Duty Cycle, $\tau \leq 100$ ms	$-V_I(\tau)$	–50	Vpk
Switch/Reset Input Current	I_{in}	5.0	mA
Power Dissipation			
Case 314A, 314B and 314D (TO–220 Type)			
$T_A = 25°C$	P_D	Internally Limited	W
Thermal Resistance, Junction–to–Ambient	$R_{\theta JA}$	65	°C/W
Thermal Resistance, Junction–to–Case	$R_{\theta JC}$	5.0	°C/W
Case 936A (D^2PAK)			
$T_A = 25°C$	P_D	Internally Limited	W
Thermal Resistance, Junction–to–Ambient	$R_{\theta JA}$	Per Figure 1	°C/W
Thermal Resistance, Junction–to–Case	$R_{\theta JC}$	5.0	°C/W
Operating Junction Temperature Range	T_J	–40 to +150	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{in} = 14 V, I_O = 500 mA, I_{stby} = 0 mA, C_O = 10 µF, C_{stby} = 10 µF, T_J = 25°C [Note 1].)

Characteristic	Symbol	Min	Typ	Max	Unit
MAIN OUTPUT					
Output Voltage (V_{in} = 6.0 V to 26 V, I_O = 5.0 mA to 500 mA, T_J = –40 to +125°C)	V_O	4.75	5.0	5.25	V
Line Regulation	Reg_{line}				mV
V_{in} = 9.0 V to 16 V, I_O = 5.0 mA		–	4.0	25	
V_{in} = 6.0 V to 26 V, I_O = 5.0 mA		–	10	50	
Load Regulation (I_O = 5.0 mA to 500 mA)	Reg_{load}	–	10	50	mV
Output Impedance I_O = 500 mAdc and 10 mArms, f = 100 Hz to 10 kHz	Z_O	–	200	–	mΩ
Output Noise Voltage (f = 10 Hz to 100 kHz)	V_n	–	100	–	µVrms
Long Term Stability	S	–	20	–	mV/kHR

ELECTRICAL CHARACTERISTICS (V_{in} = 14 V, I_O = 500 mA, I_{stby} = 0 mA, C_O = 10 µF, C_{stby} = 10 µF, T_J = 25°C [Note 1].)

Characteristic	Symbol	Min	Typ	Max	Unit
MAIN OUTPUT (continued)					
Ripple Rejection (f = 120 Hz)	RR	–	66	–	dB
Dropout Voltage	$V_I–V_O$				V
I_O = 500 mA		–	0.45	0.6	
I_O = 750 mA		–	0.82	–	
Short Circuit Current Limit	I_{SC}	0.75	1.2	–	A
Over–Voltage Shutdown Threshold	$V_{th(OV)}$	26	31	–	V
SWITCH/RESET					
Output Sink Current (V_{OL} = 1.2 V)	I_{Sink}	–	5.0	–	mA
Output Voltage ($R_{on/off}$ = 20 kΩ)					V
Low State, V_{in} = 4.0 V	V_{OL}	–	0.9	1.2	
High State, V_{in} = 14 V	V_{OH}	4.5	5.0	6.0	
Output Pull–Up Resistor, “On”/“Off” (Note 2)	$R_{on/off}$	–	20	30	kΩ
Output Voltage with Reverse Polarity Input (V_{in} = –15 V, R_L = 10 Ω)	$–V_O$	–0.6	0	–	V

ELECTRICAL CHARACTERISTICS (V_{in} = 14 V, I_O = 0 mA, I_{stby} = 10 mA, C_O = 10 µF, C_{stby} = 10 µF, T_J = 25°C [Note 1].)

Characteristic	Symbol	Min	Typ	Max	Unit
STANDBY OUTPUT					
Output Voltage (V_{in} = 6.0 V to 26 V, I_{stby} = 1.0 mA to 10 mA, T_J = –40 to +125°C)	$V_{O(stby)}$	4.75	5.0	5.25	V
Tracking Voltage	$V_O–V_{O(stby)}$	–200	0	200	mV
Line Regulation (V_{in} = 6.0 V to 26 V)	Reg_{line}	–	4.0	50	mV
Load Regulation (I_{stby} = 1.0 mA to 10 mA)	Reg_{load}	–	10	50	mV
Output Impedance $I_{(stby)}$ = 10 mAdc and 1.0 mArms, f = 100 Hz to 10 kHz	$Z_{O(stby)}$	–	1.0	–	Ω
Output Noise Voltage (f = 10 Hz to 100 kHz)	V_n	–	300	–	µVrms
Long Term Stability	S	–	20	–	mV/kHR
Ripple Rejection (f = 120 Hz)	RR	–	66	–	dB
Dropout Voltage (I_{stby} = 10 mA)	$V_I–V_{O(stby)}$	–	0.55	0.7	V
Short Circuit Current Limit	I_{SC}	25	70	–	mA
Output Voltage with Reverse Polarity Input V_{in} = –15 V, R_L = 510 Ω	$–V_O$	–0.3	0	–	V
Output Voltage with Maximum Positive Input V_{in} = 60 V, R_L = 510 Ω	$V_{O(max)}$	–	5.0	6.0	V
TOTAL DEVICE					
Bias Current	I_B				mA
I_O = 10 mA, I_{stby} = 0 mA		–	3.0	–	
I_O = 500 mA, I_{stby} = 0 mA		–	40	100	
I_O = 750 mA, I_{stby} = 0 mA		–	90	–	
Main Output “Off”, I_{stby} = 10 mA		–	2.0	3.0	

NOTES: 1. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
2. The maximum switch/reset current must not exceed 5.0 mA.

TYPICAL CIRCUIT WAVEFORMS

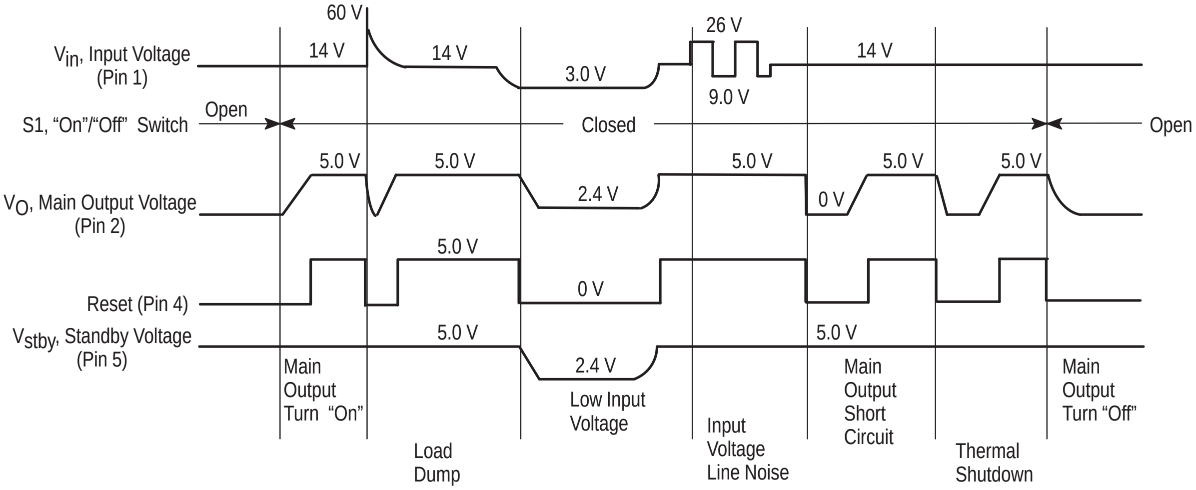
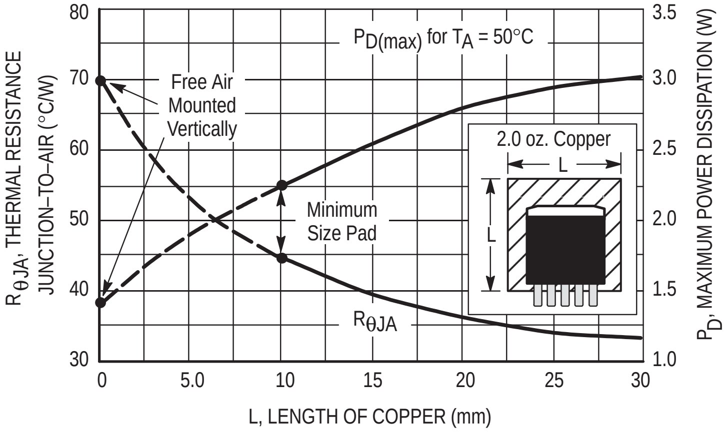


Figure 1. D2PAK Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length



MOTOROLA

LP2950
LP2951

Micropower Voltage Regulators

The LP2950 and LP2951 are micropower voltage regulators that are specifically designed to maintain proper regulation with an extremely low input–to–output voltage differential. These devices feature a very low quiescent bias current of 75 µA and are capable of supplying output currents in excess of 100 mA. Internal current and thermal limiting protection is provided.

The LP2951 has three additional features. The first is the $\overline{\text{Error}}$ Output that can be used to signal external circuitry of an out of regulation condition, or as a microprocessor power–on reset. The second feature allows the output voltage to be preset to 5.0 V, 3.3 V or 3.0 V output (depending on the version) or programmed from 1.25 V to 29 V. It consists of a pinned out resistor divider along with direct access to the Error Amplifier feedback input. The third feature is a Shutdown input that allows a logic level signal to turn–off or turn–on the regulator output.

Due to the low input–to–output voltage differential and bias current specifications, these devices are ideally suited for battery powered computer, consumer, and industrial equipment where an extension of useful battery life is desirable. The LP2950 is available in the three pin case 29 and DPAK packages, and the LP2951 is available in the eight pin dual–in–line, SO–8 and Micro–8 surface mount packages. The ‘A’ suffix devices feature an initial output voltage tolerance ±0.5%.

LP2950 and LP2951 Features:

- Low Quiescent Bias Current of 75 µA
- Low Input–to–Output Voltage Differential of 50 mV at 100 µA and 380 mV at 100 mA
- 5.0 V, 3.3 V or 3.0 V ±0.5% Allows Use as a Regulator or Reference
- Extremely Tight Line and Load Regulation
- Requires Only a 1.0 µF Output Capacitor for Stability
- Internal Current and Thermal Limiting

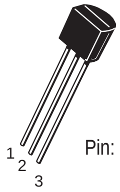
LP2951 Additional Features:

- $\overline{\text{Error}}$ Output Signals an Out of Regulation Condition
- Output Programmable from 1.25 V to 29 V
- Logic Level Shutdown Input

(See Following Page for Ordering Information.)

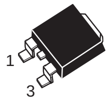
MICROPOWER LOW DROPOUT VOLTAGE REGULATORS

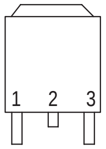
Z SUFFIX
PLASTIC PACKAGE
CASE 29
(TO–226AA/TO–92)



Pin: 1. Output
2. Ground
3. Input

DT SUFFIX
PLASTIC PACKAGE
CASE 369A
(DPAK)



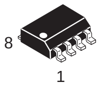


(Top View)

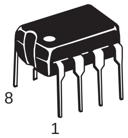
Pin: 1. Input
2. Ground
3. Output

Heatsink surface (shown as terminal 4 in case outline drawing) is connected to Pin 2.

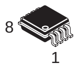
D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

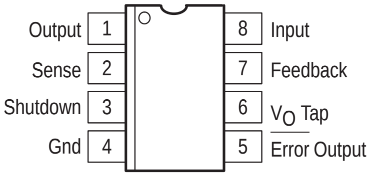


N SUFFIX
PLASTIC PACKAGE
CASE 626



DM SUFFIX
PLASTIC PACKAGE
CASE 846A
(Micro–8)





(Top View)

ORDERING INFORMATION

Device	Type	Operating Temperature Range	Package
LP2950CZ–** LP2950ACZ–**	Fixed Voltage (3.0, 3.3 or 5.0 V)	T_J = –40° to +125°C	TO–92/TO–226AA
LP2950CDT–** LP2950ACDT–**			DPAK
LP2951CD LP2951ACD	Adjustable or 5.0 V Fixed		SO–8
LP2951CD–** LP2951ACD–**	Adjustable or Fixed (3.0, 3.3 V)		
LP2951CN LP2951ACN	Adjustable or 5.0 V Fixed		Plastic
LP2951CN–** LP2951ACN–**	Adjustable or Fixed (3.0, 3.3 V)		
LP2951CDM LP2951ACDM	Adjustable or 5.0 V Fixed		Micro–8
LP2951CDM–** LP2951ACDM–**	Adjustable or Fixed (3.0, 3.3 V)		

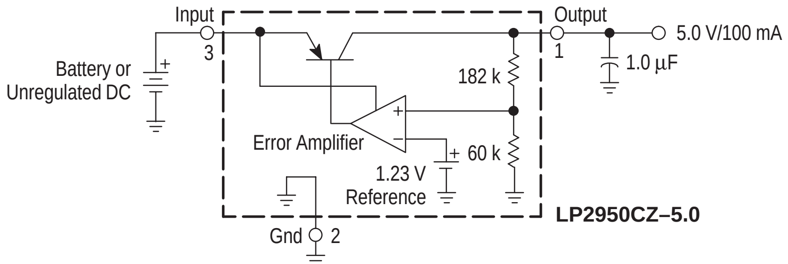
** = Voltage option of 3.0, 3.3 or 5.0 V.

DEVICE TYPE/NOMINAL OUTPUT VOLTAGE

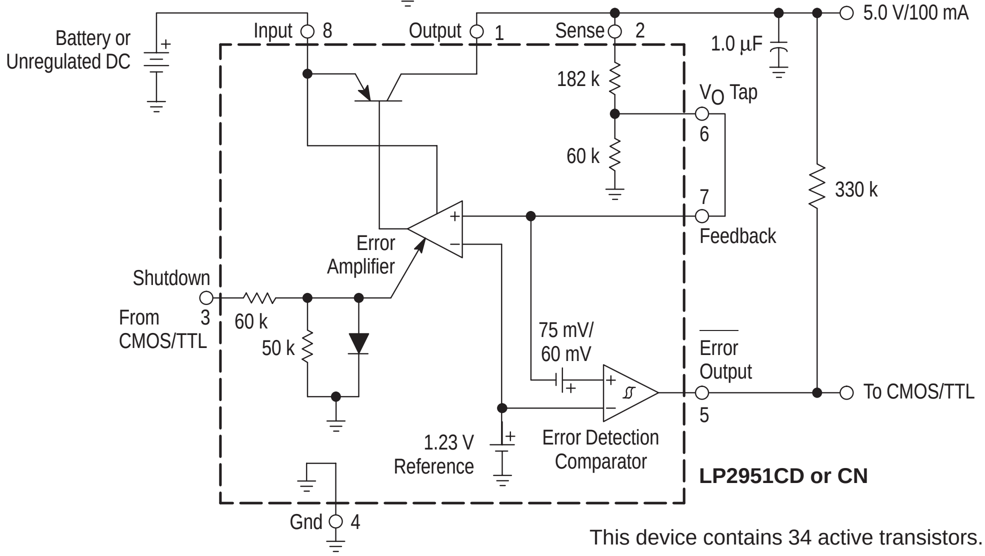
Device No. (±1%)	Device No. (±0.5%)	Nominal Voltage
LP2950CX–5.0	LP2950ACX–5.0	5.0
LP2950CX–3.3	LP2950ACX–3.3	3.3
LP2950CX–3.0	LP2950ACX–3.0	3.0
LP2951CX	LP2951ACX	Adjustable or 5.0
LP2950CX–3.3	LP2951ACX–3.3	Adjustable or 3.3
LP2951CX–3.0	LP2951ACX–3.0	Adjustable or 3.0

X = Package suffix.

Representative Block Diagrams



LP2950CZ–5.0



LP2951CD or CN

This device contains 34 active transistors.

MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted.)

Rating	Symbol	Value	Unit
Input Voltage	V_{CC}	30	Vdc
Power Dissipation and Thermal Characteristics			
Maximum Power Dissipation	P_D	Internally Limited	W
Case 751(SO–8) D Suffix			
Thermal Resistance, Junction–to–Ambient	$R_{\theta JA}$	180	°C/W
Thermal Resistance, Junction–to–Case	$R_{\theta JC}$	45	°C/W
Case 369A (DPAK) DT Suffix [Note 1]			
Thermal Resistance, Junction–to–Ambient	$R_{\theta JA}$	92	°C/W
Thermal Resistance, Junction–to–Case	$R_{\theta JC}$	6.0	°C/W
Case 29 (TO–226AA/TO–92) Z Suffix			
Thermal Resistance, Junction–to–Ambient	$R_{\theta JA}$	160	°C/W
Thermal Resistance, Junction–to–Case	$R_{\theta JC}$	83	°C/W
Case 626 N Suffix			
Thermal Resistance, Junction–to–Ambient	$R_{\theta JA}$	105	°C/W
Case 846A (Micro–8) DM Suffix			
Thermal Resistance, Junction–to–Ambient	$R_{\theta JA}$	240	°C/W
Feedback Input Voltage	V_{fb}	–1.5 to +30	Vdc
Shutdown Input Voltage	V_{sd}	–0.3 to +30	Vdc
Error Comparator Output Voltage	V_{err}	–0.3 to +30	Vdc
Operating Junction Temperature	T_J	–40 to +125	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

NOTE: 1. The Junction–to–Ambient Thermal Resistance is determined by PC board copper area per Figure 26.
2. ESD data available upon request.

ELECTRICAL CHARACTERISTICS (V_{in} = V_O + 1.0 V, I_O = 100 µA, C_O = 1.0 µF, T_J = 25°C [Note 1], unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage, 5.0 V Versions	V_O				V
V_{in} = 6.0 V, I_O = 100 µA, T_J = 25°C					
LP2950C–5.0/LP2951C		4.950	5.000	5.050	
LP2950AC–5.0/LP2951AC		4.975	5.000	5.025	
T_J = –40 to +125°C					
LP2950C–5.0/LP2951C		4.900	–	5.100	
LP2950AC–5.0/LP2951AC		4.940	–	5.060	
V_{in} = 6.0 to 30 V, I_O = 100 µA to 100 mA, T_J = –40 to +125°C					
LP2950C–5.0/LP2951C		4.880	–	5.120	
LP2950AC–5.0/LP2951AC		4.925	–	5.075	
Output Voltage, 3.3 V Versions	V_O				V
V_{in} = 4.3 V, I_O = 100 µA, T_J = 25°C					
LP2950C–3.3/LP2951C–3.3		3.267	3.300	3.333	
LP2950AC–3.3/LP2951AC–3.3		3.284	3.300	3.317	
T_J = –40 to +125°C					
LP2950C–3.3/LP2951C–3.3		3.234	–	3.366	
LP2950AC–3.3/LP2951AC–3.3		3.260	–	3.340	
V_{in} = 4.3 to 30 V, I_O = 100 µA to 100 mA, T_J = –40 to +125°C					
LP2950C–3.3/LP2951C–3.3		3.221	–	3.379	
LP2950AC–3.3/LP2951AC–3.3		3.254	–	3.346	
Output Voltage, 3.0 V Versions	V_O				V
V_{in} = 4.0 V, I_O = 100 µA, T_J = 25°C					
LP2950C–3.0/LP2951C–3.0		2.970	3.000	3.030	
LP2950AC–3.0/LP2951AC–3.0		2.985	3.000	3.015	
T_J = –40 to +125°C					
LP2950C–3.0/LP2951C–3.0		2.940	–	3.060	
LP2950AC–3.0/LP2951AC–3.0		2.964	–	3.036	
V_{in} = 4.0 to 30 V, I_O = 100 µA to 100 mA, T_J = –40 to +125°C					
LP2950C–3.0/LP2951C–3.0		2.928	–	3.072	
LP2950AC–3.0/LP2951AC–3.0		2.958	–	3.042	

ELECTRICAL CHARACTERISTICS (continued) (V_{in} = V_O + 1.0 V, I_O = 100 µA, C_O = 1.0 µF, T_J = 25°C [Note 1], unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Line Regulation (V_{in} = $V_{O(nom)}$ +1.0 V to 30 V) [Note 2]	Reg_{line}				%
LP2950C–XX/LP2951C/LP2951C–XX		–	0.08	0.20	
LP2950AC–XX/LP2951AC/LP2951AC–XX		–	0.04	0.10	
Load Regulation (I_O = 100 µA to 100 mA)	Reg_{load}				%
LP2950C–XX/LP2951C/LP2951C–XX		–	0.13	0.20	
LP2950AC–XX/LP2951AC/LP2951AC–XX		–	0.05	0.10	
Dropout Voltage	V_I – V_O				mV
I_O = 100 µA		–	30	80	
I_O = 100 mA		–	350	450	
Supply Bias Current	I_{CC}				
I_O = 100 µA		–	93	120	µA
I_O = 100 mA		–	4.0	12	mA
Dropout Supply Bias Current (V_{in} = $V_{O(nom)}$ – 0.5 V, I_O = 100 µA) [Note 2]	$I_{CCdropout}$	–	110	170	µA
Current Limit (V_O Shorted to Ground)	I_{Limit}	–	220	300	mA
Thermal Regulation	$Reg_{thermal}$	–	0.05	0.20	%/W
Output Noise Voltage (10 Hz to 100 kHz) [Note 3]	V_n				µVrms
C_L = 1.0 µF		–	126	–	
C_L = 100 µF		–	56	–	
LP2951A/LP2951AC ONLY					
Reference Voltage (T_J = 25°C)	V_{ref}				V
LP2951C/LP2951C–XX		1.210	1.235	1.260	
LP2951AC/LP2951AC–XX		1.220	1.235	1.250	
Reference Voltage (T_J = –40 to +125°C)	V_{ref}				V
LP2951C/LP2951C–XX		1.200	–	1.270	
LP2951AC/LP2951AC–XX		1.200	–	1.260	
Reference Voltage (T_J = –40 to +125°C)	V_{ref}				V
I_O = 100 µA to 100 mA, V_{in} = 23 to 30 V					
LP2951C/LP2951C–XX		1.185	–	1.285	
LP2951AC/LP2951AC–XX		1.190	–	1.270	
Feedback Pin Bias Current	I_{FB}	–	15	40	nA
ERROR COMPARATOR					
Output Leakage Current (V_{OH} = 30 V)	I_{lkg}	–	0.01	1.0	µA
Output Low Voltage (V_{in} = 4.5 V, I_{OL} = 400 µA)	V_{OL}	–	150	250	mV
Upper Threshold Voltage (V_{in} = 6.0 V)	V_{thu}	40	45	–	mV
Lower Threshold Voltage (V_{in} = 6.0 V)	V_{thl}	–	60	95	mV
Hysteresis (V_{in} = 6.0 V)	V_{hy}	–	15	–	mV
SHUTDOWN INPUT					
Input Logic Voltage	V_{shtdn}				V
Logic “0” (Regulator “On”)		0	–	0.7	
Logic “1” (Regulator “Off”)		2.0	–	30	
Shutdown Pin Input Current	I_{shtdn}				µA
V_{shtdn} = 2.4 V		–	35	50	
V_{shtdn} = 30 V		–	450	600	
Regulator Output Current in Shutdown Mode (V_{in} = 30 V, V_{shtdn} = 2.0 V, V_O = 0, Pin 6 Connected to Pin 7)	I_{off}	–	3.0	10	µA

NOTES: 1. Low duty pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
2. $V_{O(nom)}$ is the part number voltage option.
3. Noise tests on the LP2951 are made with a 0.01 µF capacitor connected across Pins 7 and 1.

DEFINITIONS

Dropout Voltage – The input/output voltage differential at which the regulator output no longer maintains regulation against further reductions in input voltage. Measured when the output drops 100 mV below its nominal value (which is measured at 1.0 V differential), dropout voltage is affected by junction temperature, load current and minimum input supply requirements.

Line Regulation – The change in output voltage for a change in input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that average chip temperature is not significantly affected.

Load Regulation – The change in output voltage for a change in load current at constant chip temperature.

Maximum Power Dissipation – The maximum total device dissipation for which the regulator will operate within specifications.

Bias Current – Current which is used to operate the regulator chip and is not delivered to the load.

Output Noise Voltage – The rms ac voltage at the output, with constant load and no input ripple, measured over a specified frequency range.

Leakage Current – Current drawn through a bipolar transistor collector–base junction, under a specified collector voltage, when the transistor is "off".

Upper Threshold Voltage – Voltage applied to the comparator input terminal, below the reference voltage which is applied to the other comparator input terminal, which causes the comparator output to change state from a logic "0" to "1".

Lower Threshold Voltage – Voltage applied to the comparator input terminal, below the reference voltage which is applied to the other comparator input terminal, which causes the comparator output to change state from a logic "1" to "0".

Hysteresis – The difference between Lower Threshold voltage and Upper Threshold voltage.

Figure 1. Quiescent Current

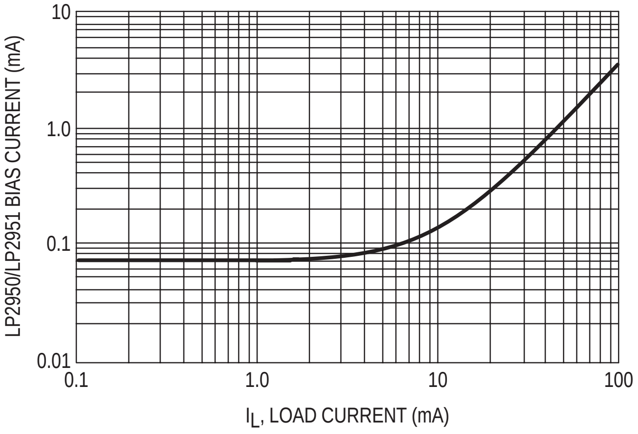


Figure 2. Dropout Characteristics

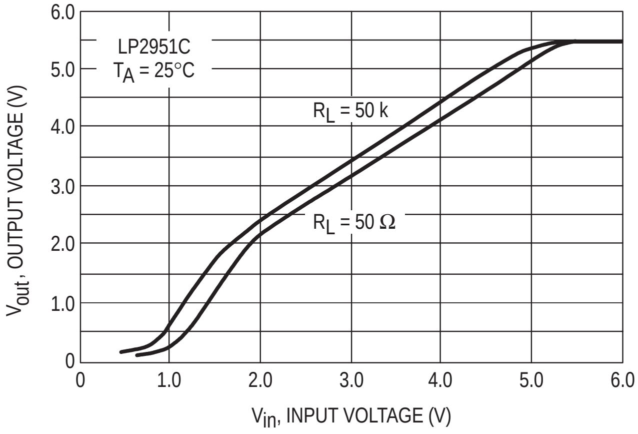


Figure 3. Input Current

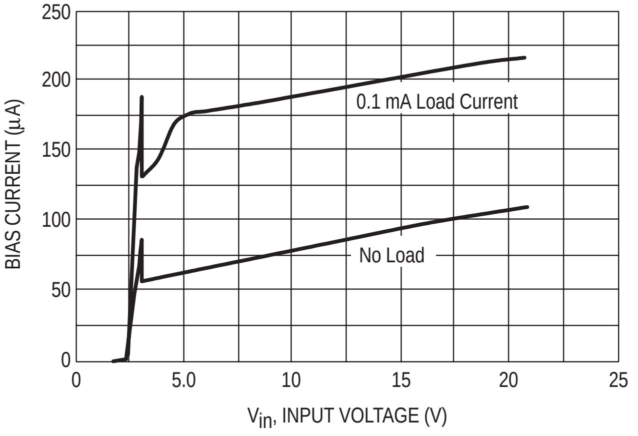


Figure 4. Output Voltage versus Temperature

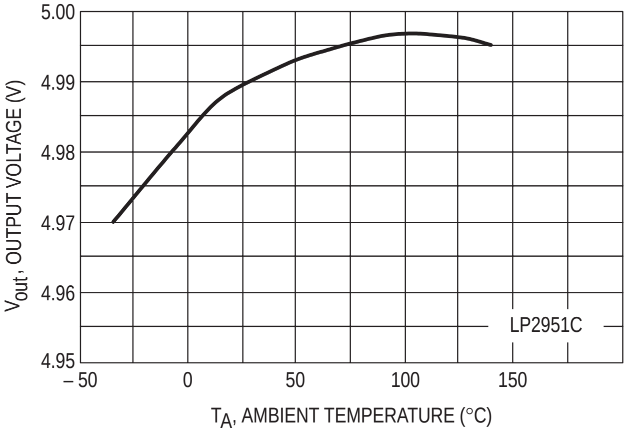


Figure 5. Dropout Voltage versus Output Current

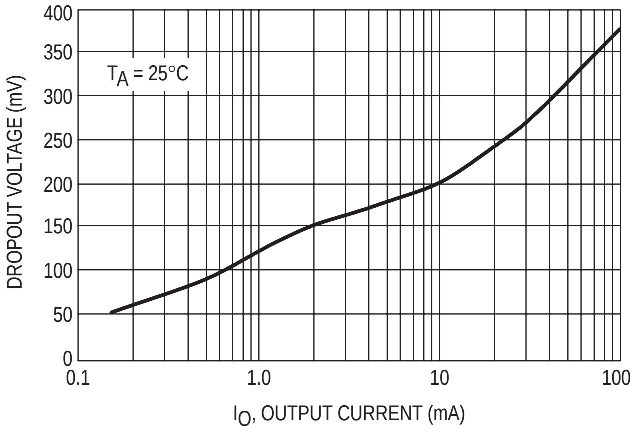


Figure 6. Dropout Voltage versus Temperature

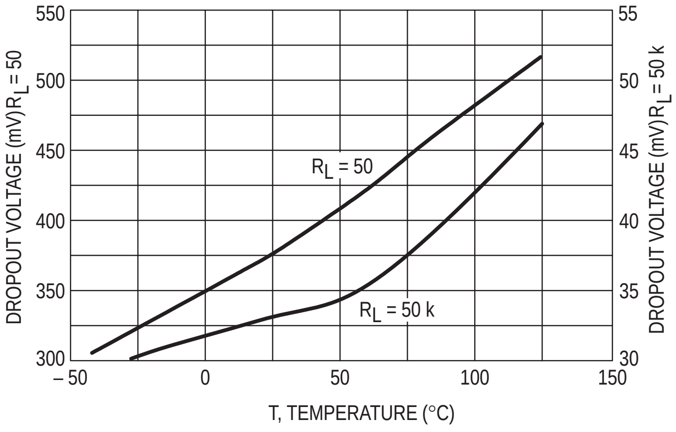


Figure 7. Error Comparator Output

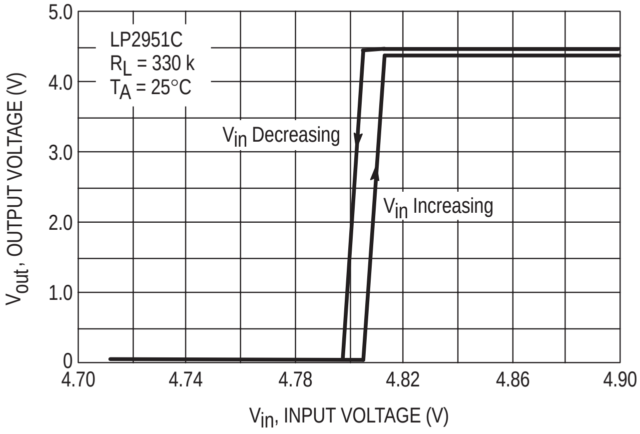


Figure 8. Line Transient Response

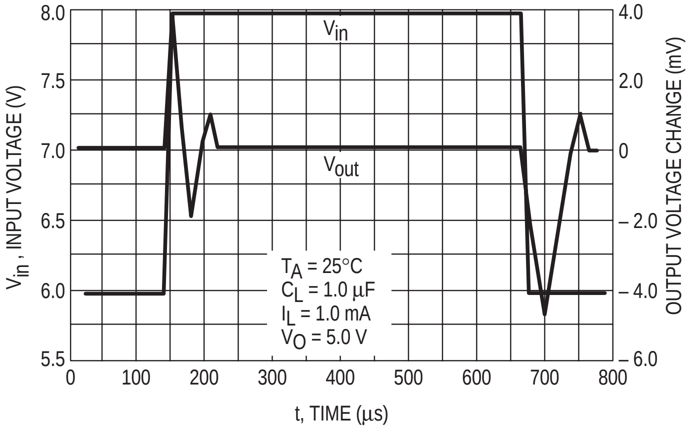


Figure 9. LP2951 Enable Transient

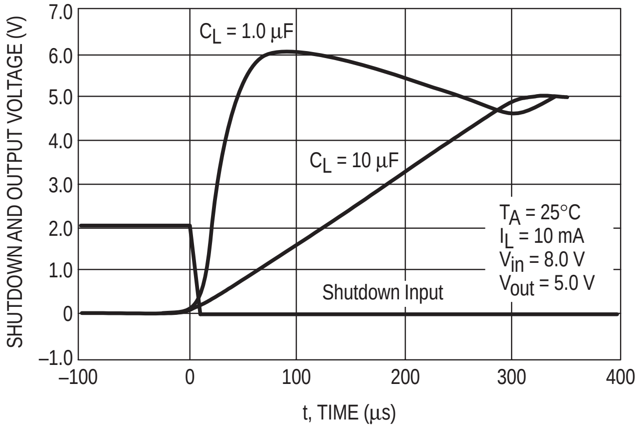


Figure 10. Load Transient Response

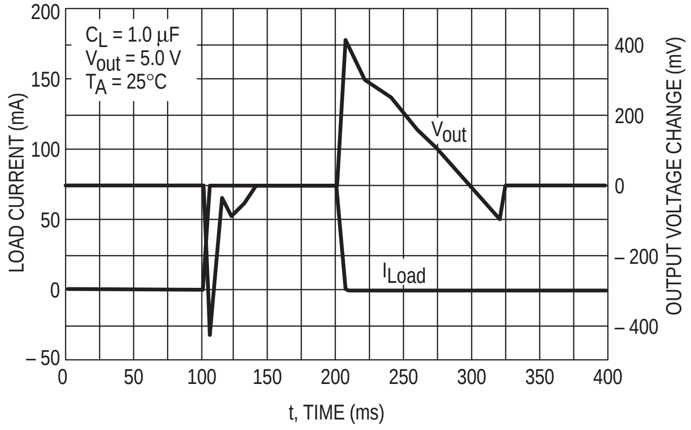


Figure 11. Ripple Rejection

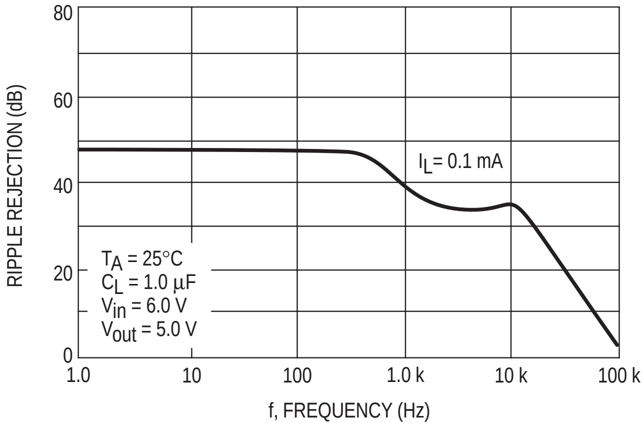


Figure 12. Output Noise

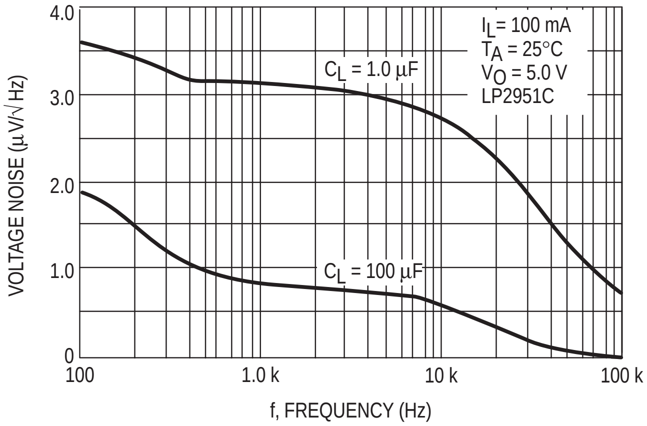


Figure 13. Shutdown Threshold Voltage versus Temperature

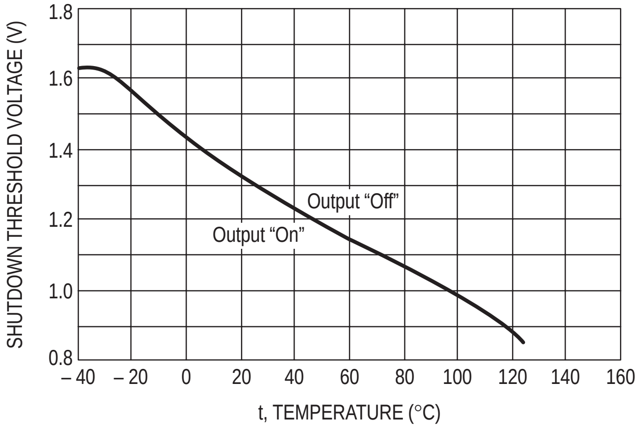
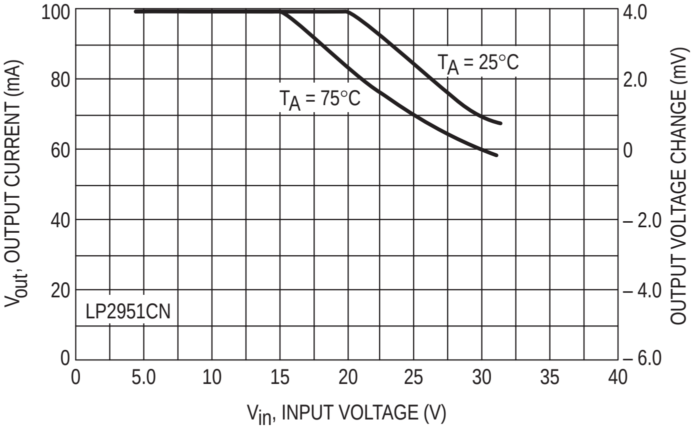


Figure 14. Maximum Rated Output Current



APPLICATIONS INFORMATION

Introduction

The LP2950/LP2951 regulators are designed with internal current limiting and thermal shutdown making them user–friendly. Typical application circuits for the LP2950 and LP2951 are shown in Figures 17 through 25.

These regulators are not internally compensated and thus require a 1.0 µF (or greater) capacitance between the LP2950/LP2951 output terminal and ground for stability. Most types of aluminum, tantalum or multilayer ceramic will perform adequately. Solid tantalums or appropriate multilayer ceramic capacitors are recommended for operation below 25°C.

At lower values of output current, less output capacitance is required for output stability. The capacitor can be reduced to 0.33 µF for currents less than 10 mA, or 0.1 µF for currents below 1.0 mA. Using the 8–pin versions at voltages less than 5.0 V operates the error amplifier at lower values of gain, so that more output capacitance is needed for stability. For the worst case operating condition of a 100 mA load at 1.23 V output (Output Pin 1 connected to the feedback Pin 7) a minimum capacitance of 3.3 µF is recommended.

The LP2950 will remain stable and in regulation when operated with no output load. When setting the output voltage of the LP2951 with external resistors, the resistance values should be chosen to draw a minimum of 1.0 µA.

A bypass capacitor is recommended across the LP2950/LP2951 input to ground if more than 4 inches of wire connects the input to either a battery or power supply filter capacitor.

Input capacitance at the LP2951 Feedback Pin 7 can create a pole, causing instability if high value external resistors are used to set the output voltage. Adding a 100 pF capacitor between the Output Pin 1 and the Feedback Pin 7 and increasing the output filter capacitor to at least 3.3 µF will stabilize the feedback loop.

Error Detection Comparator

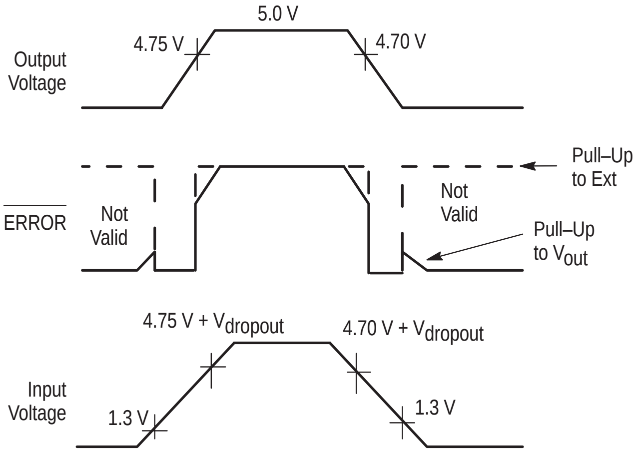
The comparator switches to a positive logic low whenever the LP2951 output voltage falls more than approximately 5.0% out of regulation. This value is the comparator's designed–in offset voltage of 60 mV divided by the 1.235 V internal reference. As shown in the representative block diagram. This trip level remains 5.0% below normal regardless of the value of regulated output voltage. For example, the error flag trip level is 4.75 V for a normal 5.0 V regulated output, or 9.50 V for a 10 V output voltage.

Figure 1 is a timing diagram which shows the ERROR signal and the regulated output voltage as the input voltage to the LP2951 is ramped up and down. The ERROR signal becomes valid (low) at about 1.3 V input. It goes high when the input reaches about 5.0 V (V_{out} exceeds about 4.75 V). Since the LP2951's dropout voltage is dependent upon the load current (refer to the curve in the Typical Performance Characteristics), the input voltage trip point will vary with load current. The output voltage trip point does not vary with load.

The error comparator output is an open collector which requires an external pull–up resistor. This resistor may be returned to the output or some other voltage within the system. The resistance value should be chosen to be consistent with the 400 µA sink capability of the error comparator. A value between 100 k and 1.0 MΩ is suggested. No pull–up resistance is required if this output is unused.

When operated in the shutdown mode, the error comparator output will go high if it has been pulled up to an external supply. To avoid this invalid response, the error comparator output should be pulled up to V_{out} (see Figure 15).

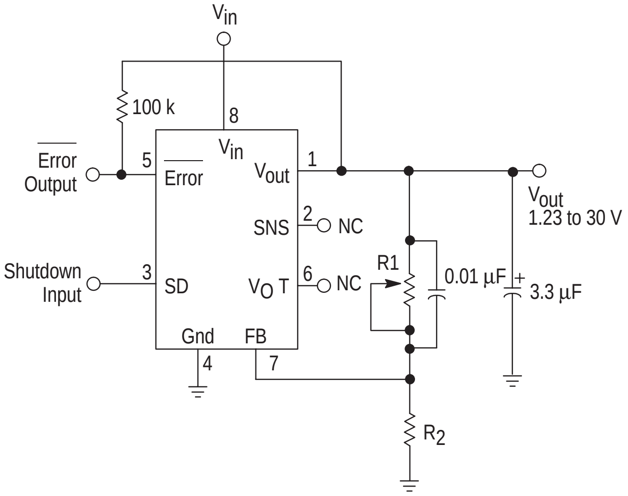
Figure 15. ERROR Output Timing



Programming the Output Voltage (LP2951)

The LP2951CX may be pin–strapped for 5.0 V using its internal voltage divider by tying Pin 1 (output) to Pin 2 (sense) and Pin 7 (feedback) to Pin 6 (5.0 V tap). Alternatively, it may be programmed for any output voltage between its 1.235 reference voltage and its 30 V maximum rating. An external pair of resistors is required, as shown in Figure 16.

Figure 16. Adjustable Regulator



The complete equation for the output voltage is:

$$V_{out} = V_{ref}\ (1 + R1/R2) + I_{FB}\ R1$$

where V_{ref} is the nominal 1.235 V reference voltage and I_{FB} is the feedback pin bias current, nominally −20 nA. The minimum recommended load current of 1.0 µA forces an upper limit of 1.2 MΩ on the value of R2, if the regulator must work with no load. I_{FB} will produce a 2% typical error in V_{out} which may be eliminated at room temperature by adjusting R1. For better accuracy, choosing R2 = 100 k reduces this error to 0.17% while increasing the resistor program current to 12 µA. Since the LP2951 typically draws 75 µA at no load with Pin 2 open circuited, the extra 12 µA of current drawn is often a worthwhile tradeoff for eliminating the need to set output voltage in test.

Output Noise

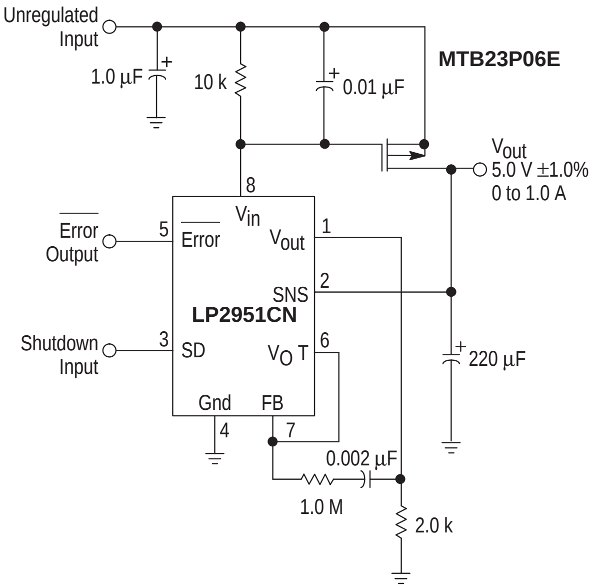
In many applications it is desirable to reduce the noise present at the output. Reducing the regulator bandwidth by increasing the size of the output capacitor is the only method for reducing noise on the 3 lead LP2950. However, increasing the capacitor from 1.0 µF to 220 µF only decreases the noise from 430 µV to 160 µVrms for a 100 kHz bandwidth at the 5.0 V output.

Noise can be reduced fourfold by a bypass capacitor across R1, since it reduces the high frequency gain from 4 to unity. Pick

$$C_{Bypass} \approx \frac{1}{2\pi R1 \times 200\ Hz}$$

or about 0.01 µF. When doing this, the output capacitor must be increased to 3.3 µF to maintain stability. These changes reduce the output noise from 430 µV to 126 µVrms for a 100 kHz bandwidth at 5.0 V output. With bypass capacitor added, noise no longer scales with output voltage so that improvements are more dramatic at higher output voltages.

Figure 17. 1.0 A Regulator with 1.2 V Dropout



TYPICAL APPLICATIONS

Figure 18. Lithium Ion Battery Cell Charger

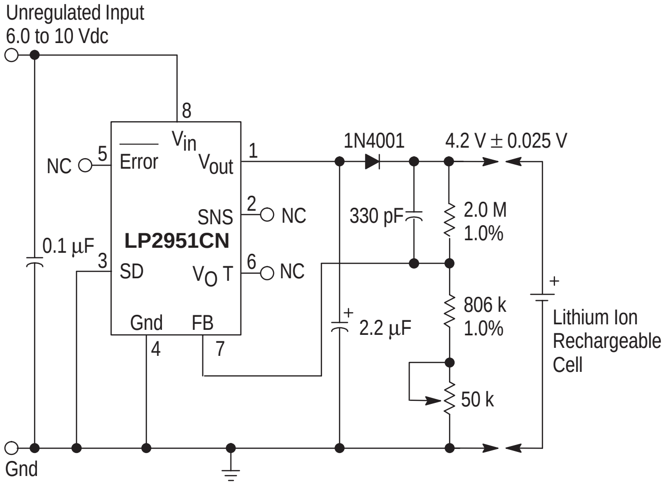


Figure 19. Low Drift Current Sink

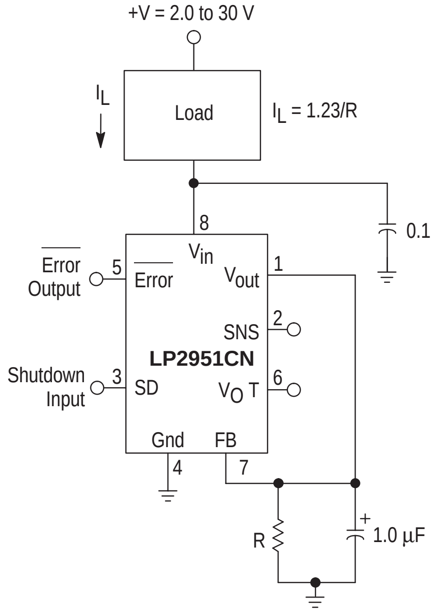
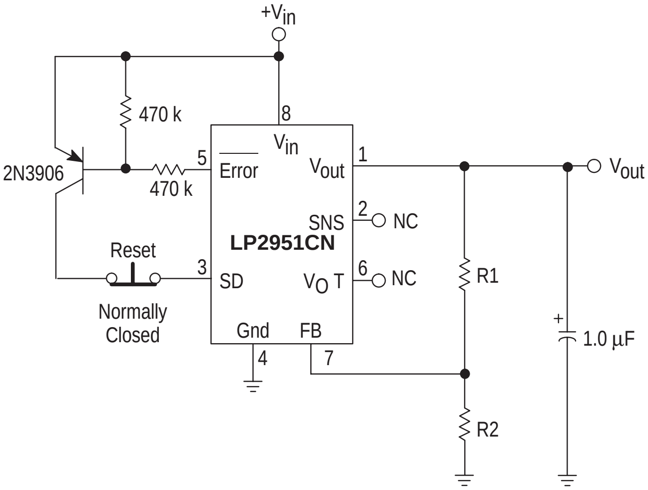


Figure 20. Latch Off When Error Flag Occurs



Error flag occurs when V_{in} is too low to maintain V_{out}, or if V_{out} is reduced by excessive load current.

Figure 21. 5.0 V Regulator with 2.5 V Sleep Function

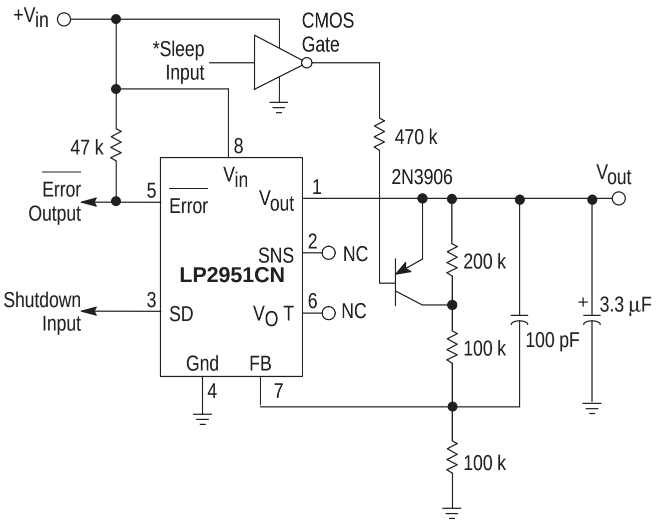
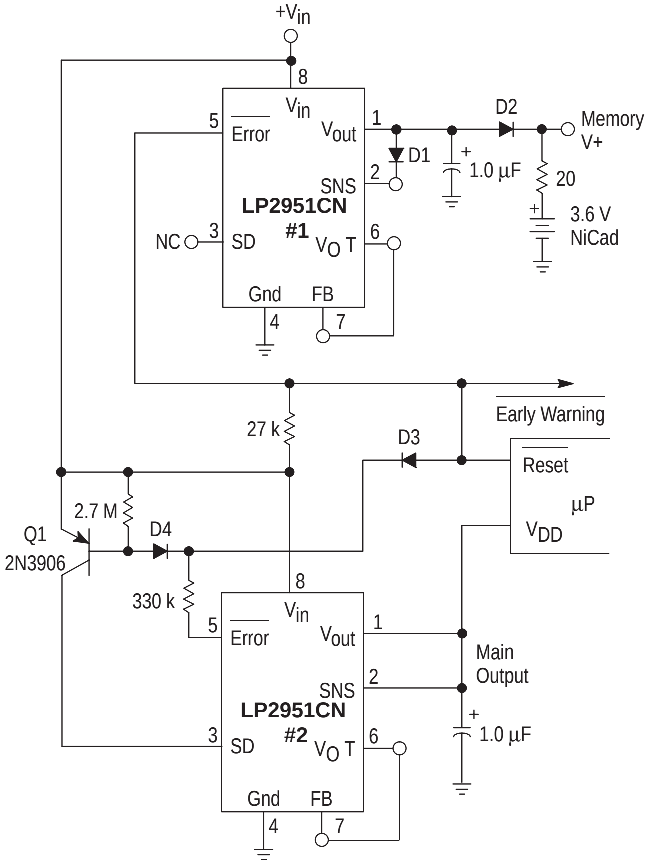


Figure 22. Regulator with Early Warning and Auxiliary Output



All diodes are 1N4148.

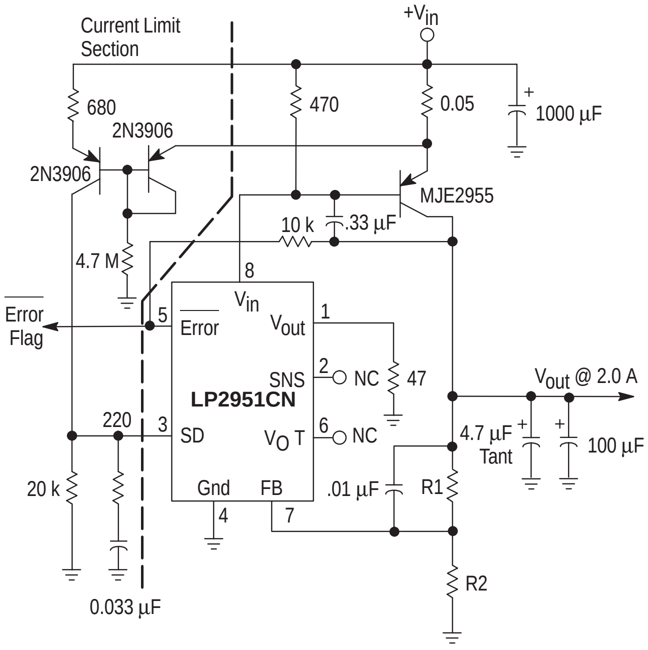
Early Warning flag on low input voltage.

Main output latches off at lower input voltages.

Battery backup on auxiliary output.

Operation: Regulator #1's V_{out} is programmed one diode drop above 5.0 V. Its error flag becomes active when $V_{in} \leq 5.7$ V. When V_{in} drops below 5.3 V, the error flag of regulator #2 becomes active and via Q1 latches the main output "off". When V_{in} again exceeds 5.7 V, regulator #1 is back in regulation and the early warning signal rises, unlatching regulator #2 via D3.

Figure 23. 2.0 A Low Dropout Regulator



$V_{out} = 1.25V\ (1.0 + R1/R2)$

For 5.0 V output, use internal resistors. Wire Pin 6 to 7, and wire Pin 2 to $+V_{out}$ Bus.

Figure 24. Open Circuit Detector for 4.0 to 20 mA Current Loop

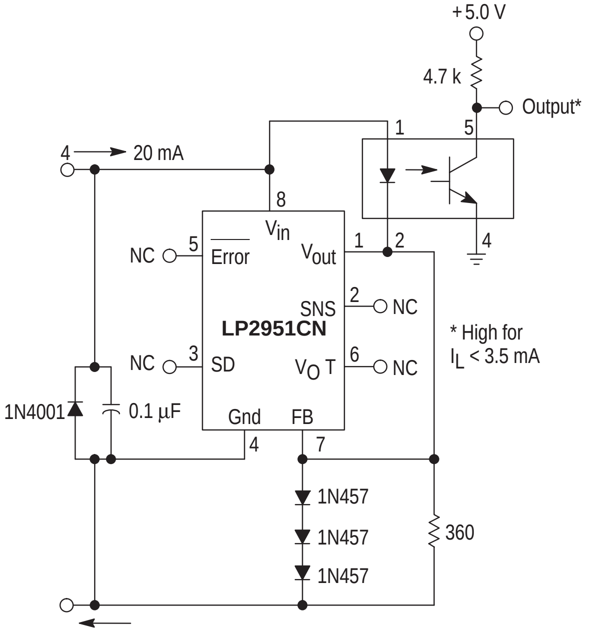


Figure 25. Low Battery Disconnect

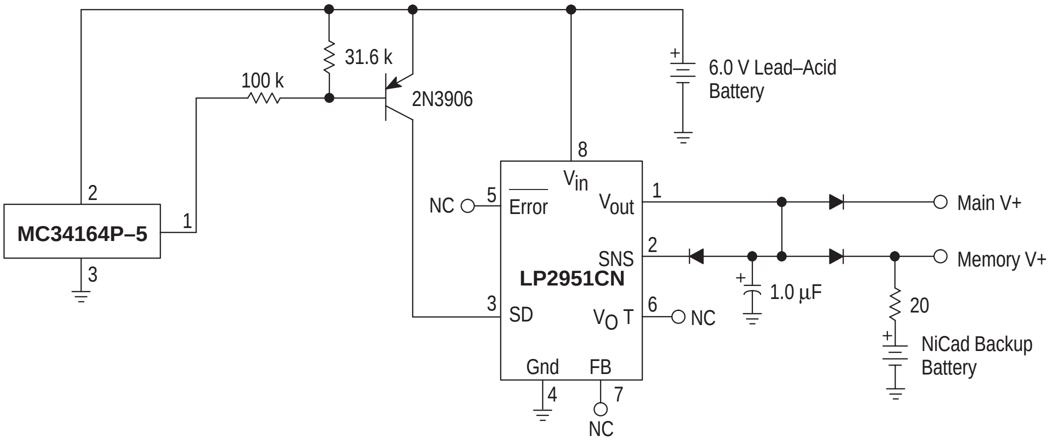
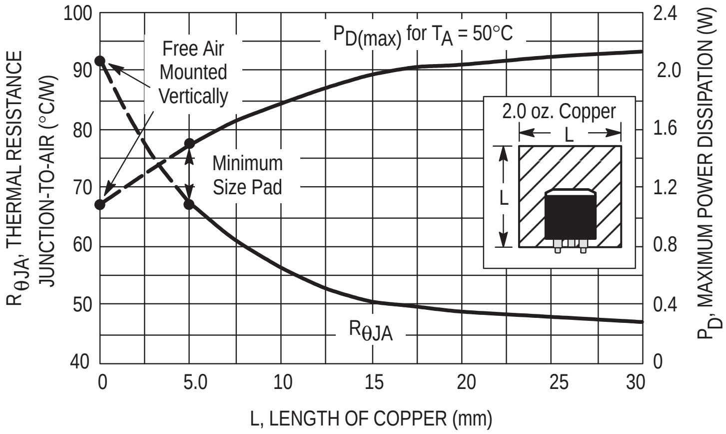


Figure 26. DPAK Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length



MC1723C

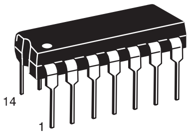
Voltage Regulator

The MC1723C is a positive or negative voltage regulator designed to deliver load current to 150 mAdc. Output current capability can be increased to several amperes through use of one or more external pass transistors. MC1723C is specified for operation over the commercial temperature range (0° to +70°C).

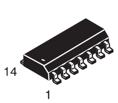
- Output Voltage Adjustable from 2.0 Vdc to 37 Vdc
- Output Current to 150 mAdc Without External Pass Transistors
- 0.01% Line and 0.03% Load Regulation
- Adjustable Short Circuit Protection

VOLTAGE REGULATOR

SEMICONDUCTOR
TECHNICAL DATA



P SUFFIX
PLASTIC PACKAGE
CASE 646



D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO–14)

ORDERING INFORMATION

Device	Alternate	Operating Temperature Range	Package
MC1723CD	–	T_A = 0° to +70°C	SO–14
MC1723CP	LM723CN µA723PC		Plastic DIP

Figure 1. Representative Schematic Diagram

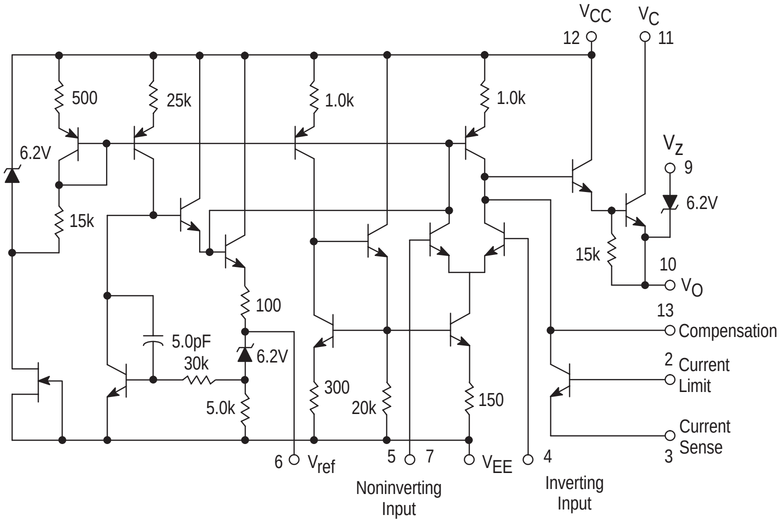
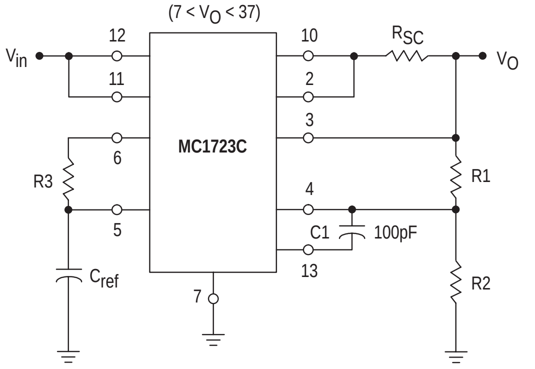


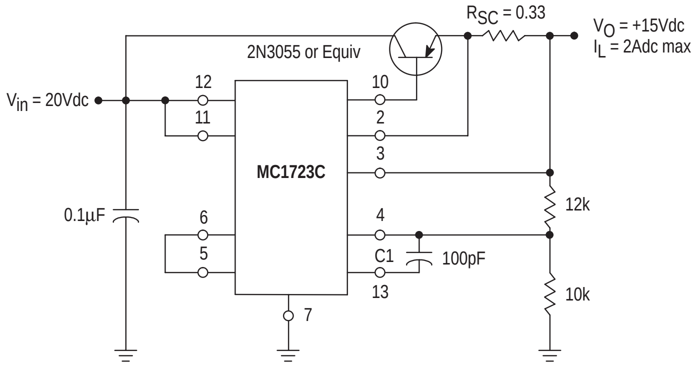
Figure 2. Typical Circuit Connection



$V_O \cong 7\left(\frac{R1 + R2}{R2}\right)$ $I_{SC} = \frac{V_{sense}}{R_{SC}} = \frac{0.66}{R_{SC}}$ at $T_J = +25°C$

For best results 10 k < R2 < 100 k
For minimum drift R3 = R1 | | R2

Figure 3. Typical NPN Current Boost Connection



MAXIMUM RATINGS (T_A = +25°C, unless otherwise noted.)

Rating	Symbol	Value	Unit
Pulse Voltage from V_{CC} to V_{EE} (50 ms)	$V_{I(p)}$	50	V_{pk}
Continuous Voltage from V_{CC} to V_{EE}	V_I	40	Vdc
Input–Output Voltage Differential	$V_I–V_O$	40	Vdc
Maximum Output Current	I_L	150	mAdc
Current from V_{ref}	I_{ref}	15	mAdc
Current from V_z	I_z	25	mA
Voltage Between Noninverting Input and V_{EE}	V_{ie}	8.0	Vdc
Differential Input Voltage	V_{id}	±5.0	Vdc
Power Dissipation and Thermal Characteristics T_A = +25°C Derate above T_A = +25°C Thermal Resistance, Junction–to–Air	 P_D $1/\theta_{JA}$ θ_{JA}	 1.25 10 100	 W mW/°C °C/W
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +175	°C
Operating Ambient Temperature Range	T_A	0 to +70	°C

ELECTRICAL CHARACTERISTICS (T_A = +25°C, V_{in} 12 Vdc, V_O = 5.0 Vdc, I_L = 1.0 mAdc, R_{SC} = 0, C1 = 100 pF, C_{ref} = 0 and divider impedance as seen by the error amplifier ≤ 10 kΩ connected as shown in Figure 2, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Input Voltage Range	V_I	9.5	–	40	Vdc
Output Voltage Range	V_O	2.0	–	37	Vdc
Input–Output Voltage Differential	$V_I–V_O$	3.0	–	38	Vdc
Reference Voltage	V_{ref}	6.80	7.15	7.50	Vdc
Standby Current Drain (I_L = 0, V_{in} = 30 V)	I_{IB}	–	2.3	4.0	mAdc
Output Noise Voltage (f = 100 Hz to 10 kHz) C_{ref} = 0 C_{ref} = 5.0 µF	V_n	 – –	 20 2.5	 – –	µV(RMS)
Average Temperature Coefficient of Output Voltage (T_{low} < T_A < T_{high})	TCV_O	–	0.003	0.015	%/°C
Line Regulation (T_A = 25°C) { 12 V < V_{in} < 15 V 12 V < V_{in} < 40 V (T_{low} < T_A < T_{high}) 12 V < V_{in} < 15 V	Reg_{line}	 – – –	 0.01 0.1 –	 0.1 0.5 0.3	% V_O
Load Regulation (1.0 mA < I_L < 50 mA) T_A = 25°C T_{low} < T_A < T_{high}	Reg_{load}	 – –	 0.03 –	 0.2 0.6	% V_O
Ripple Rejection (f = 50 Hz to 10 kHz) C_{ref} = 0 C_{ref} = 5.0 µF	RR	 – –	 74 86	 – –	dB
Short Circuit Current Limit (R_{SC} = 10 Ω, V_O = 0)	I_{SC}	–	65	–	mAdc
Long Term Stability	^V_O/^t	–	0.1	–	%/1000 Hr.

NOTE: T_{low} to T_{high} = 0° to +70°C

Figure 4. Maximum Load Current as a Function of Input–Output Voltage Differential

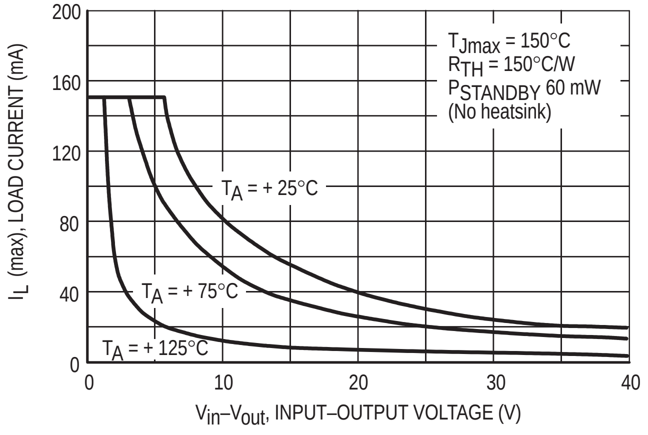


Figure 5. Load Regulation Characteristics Without Current Limiting

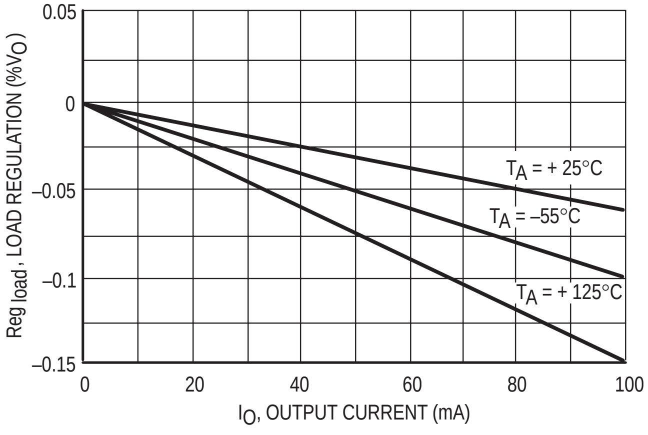


Figure 6. Load Regulation Characteristics With Current Limiting

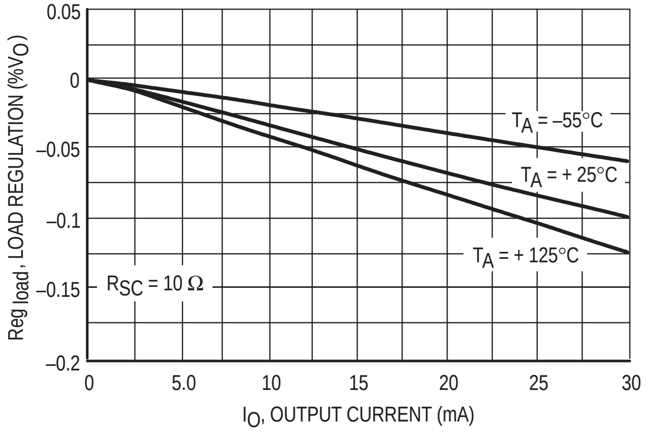


Figure 7. Load Regulation Characteristics With Current Limiting

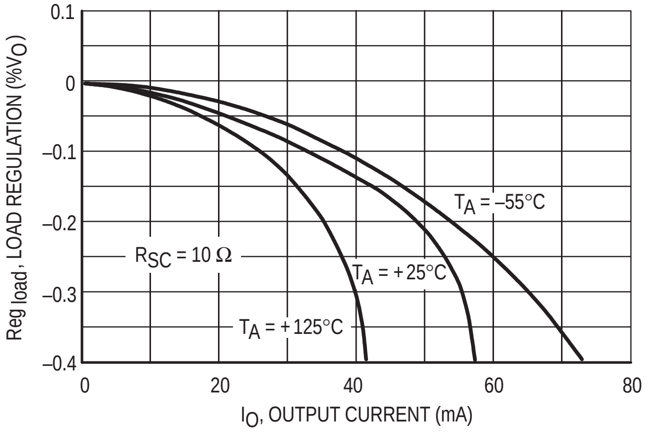


Figure 8. Current Limiting Characteristics

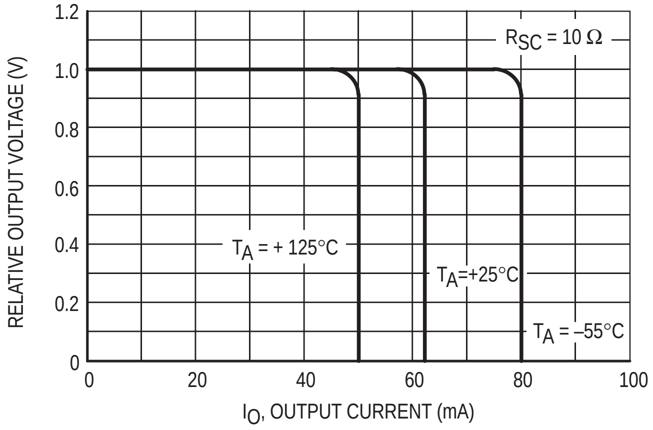


Figure 9. Current Limiting Characteristics as a Function of Junction Temperature

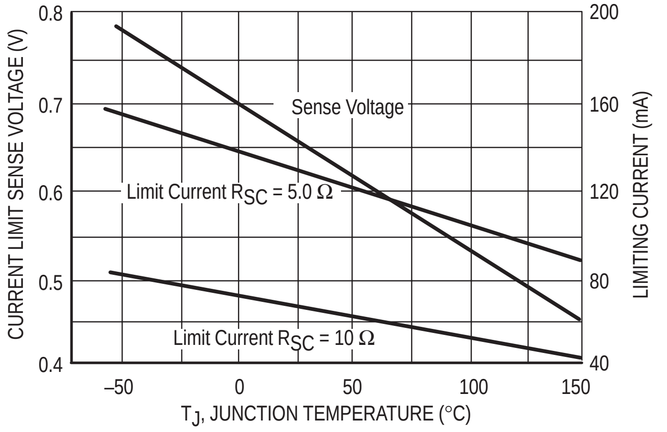


Figure 10. Line Regulation as a Function of Input–Output Voltage Differential

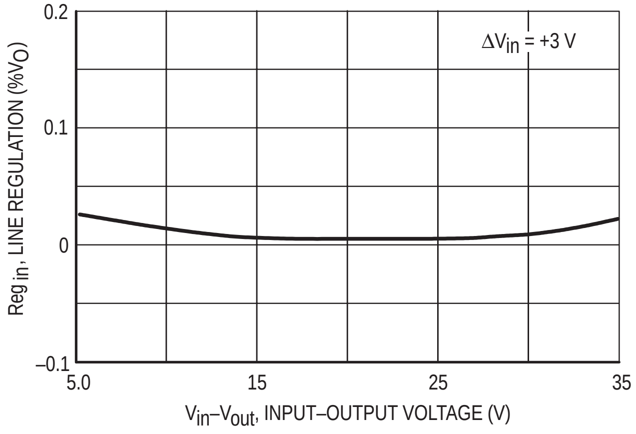


Figure 11. Load Regulation as a Function of Input–Output Voltage Differential

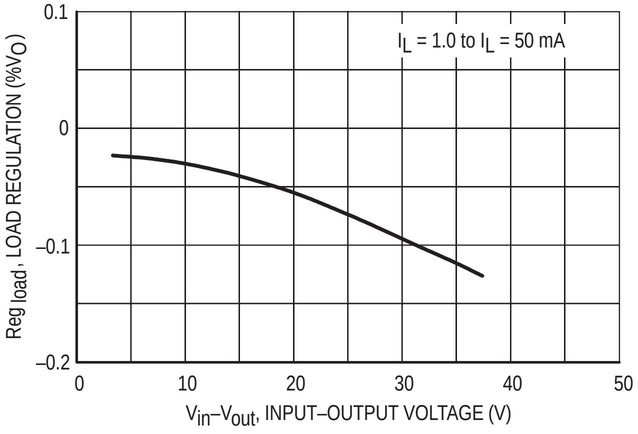


Figure 12. Standby Current Drain as a Function of Input Voltage

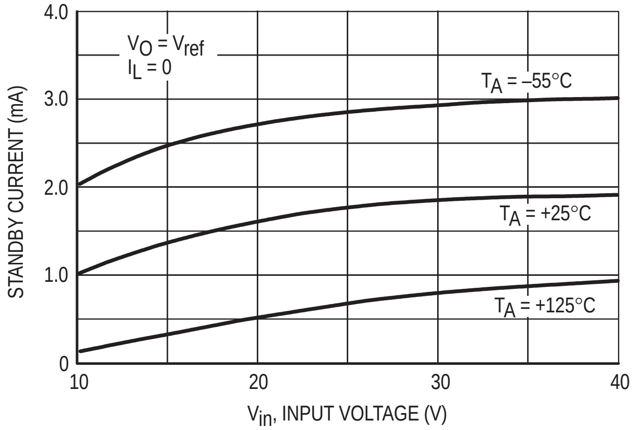


Figure 13. Line Transient Response

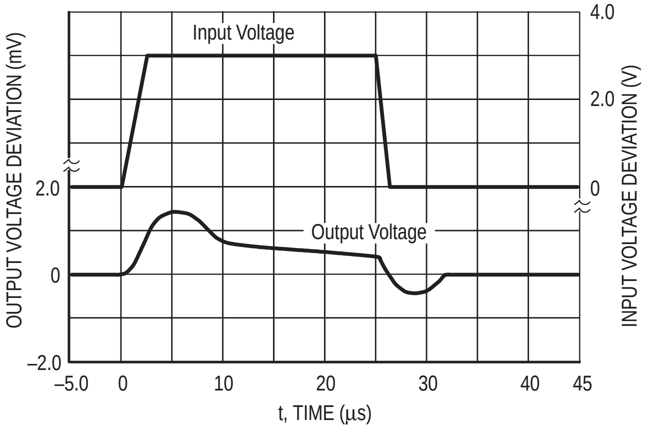


Figure 14. Load Transient Response

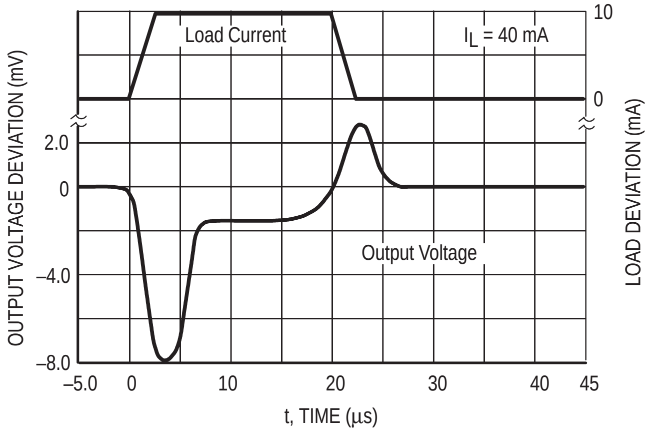


Figure 15. Output Impedance as Function of Frequency

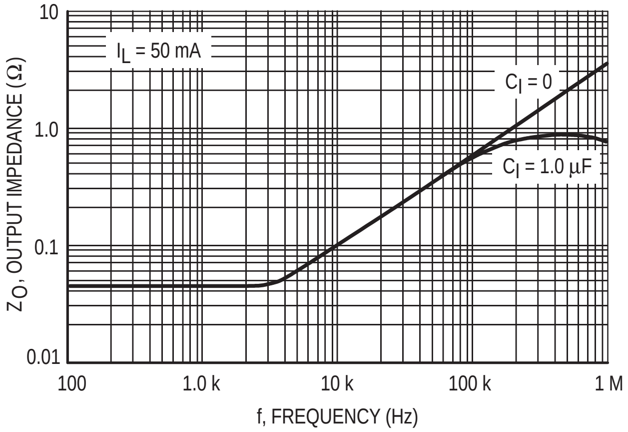
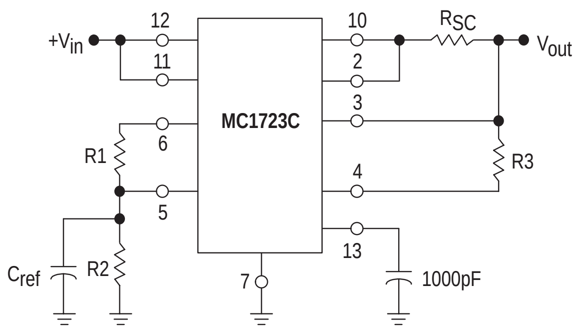


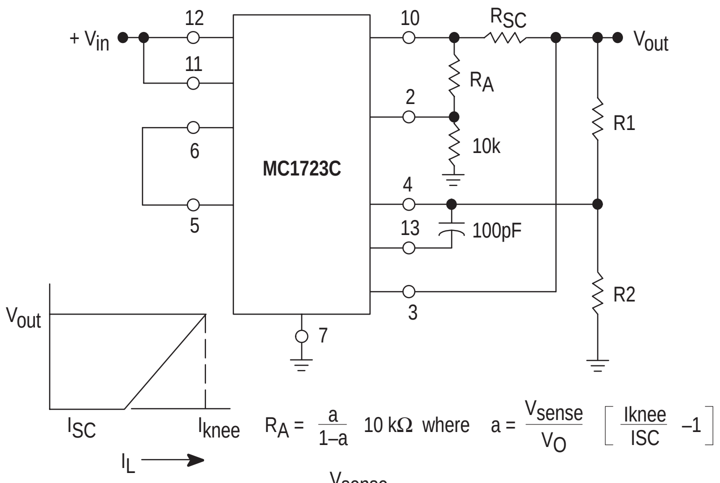
Figure 16. Typical Connection for $2 < V_O < 7$



$V_O \cong 7\left[\frac{R2}{R1 + R2}\right]$ $\quad I_{SC} = \frac{V_{sense}}{R_{SC}} \cong \frac{0.66}{RSC}$ at $T_J = +25°C$

For best results 10 k < R1 +R2 < 100 k
For minimum drift R3 = R1 R2

Figure 17. Foldback Connection



$R_A = \frac{a}{1-a}$ 10 kΩ where $a = \frac{V_{sense}}{V_O}\left[\frac{Iknee}{ISC} - 1\right]$

$R_{SC} = \frac{V_{sense}}{(1-a)\,I_{SC}}$

Figure 18. +5.0 V, 1.0 A Switching Regulator

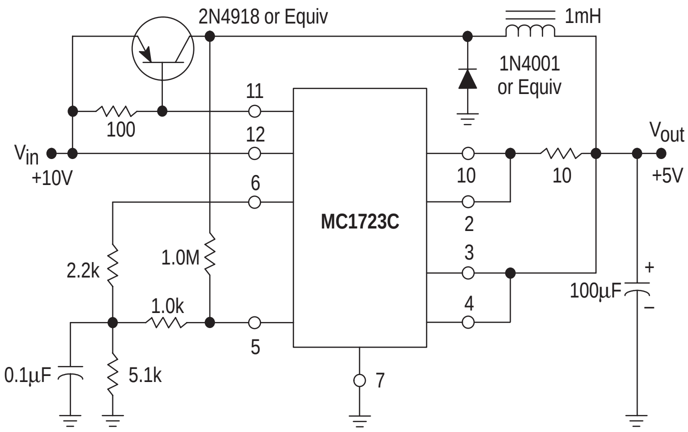


Figure 19. +5.0 V, 1.0 A High Efficiency Regulator

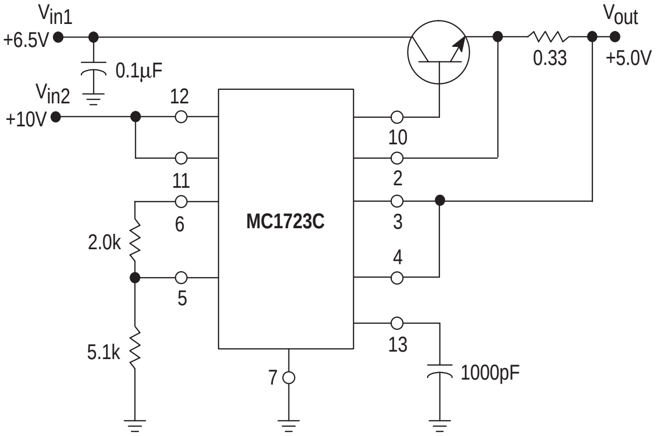


Figure 20. +15 V, 1.0 A Regulator with Remote Sense

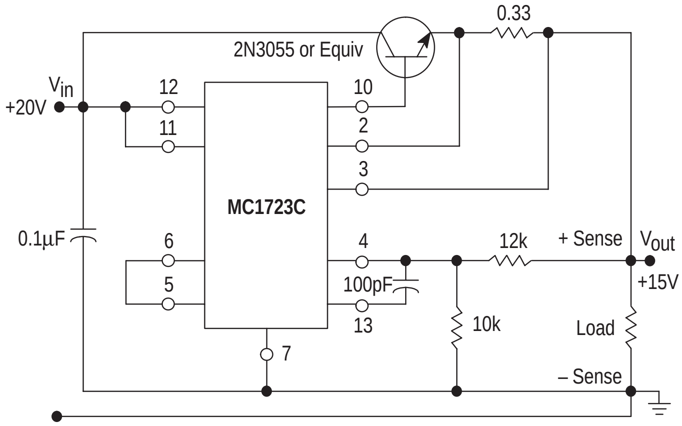


Figure 21. –15 V Negative Regulator

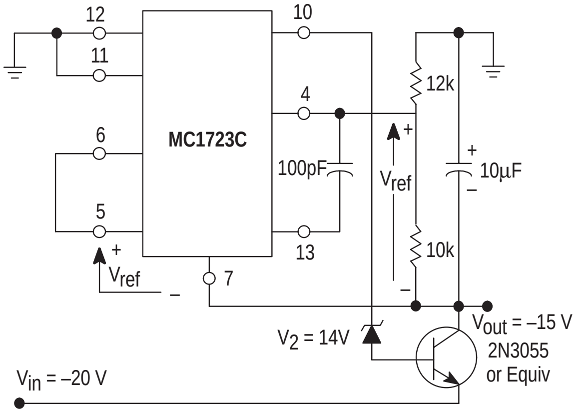
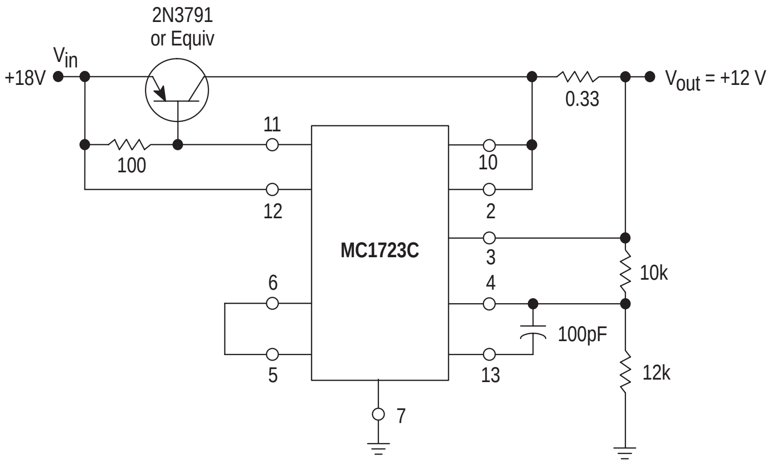


Figure 22. +12V, 1.0 A Regulator
(Using PNP Current Boost)



MC3423

Overvoltage Crowbar Sensing Circuit

This overvoltage protection circuit (OVP) protects sensitive electronic circuitry from overvoltage transients or regulator failures when used in conjunction with an external "crowbar" SCR. The device senses the overvoltage condition and quickly "crowbars" or short circuits the supply, forcing the supply into current limiting or opening the fuse or circuit breaker.

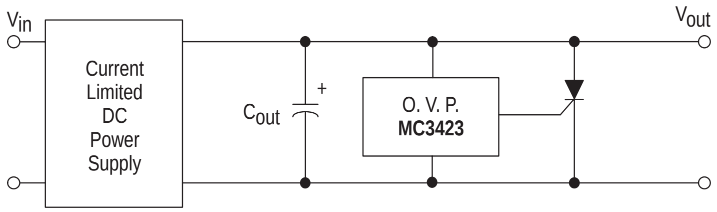
The protection voltage threshold is adjustable and the MC3423 can be programmed for minimum duration of overvoltage condition before tripping, thus supplying noise immunity.

The MC3423 is essentially a "two terminal" system, therefore it can be used with either positive or negative supplies.

MAXIMUM RATINGS

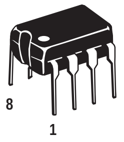
Rating	Symbol	Value	Unit
Differential Power Supply Voltage	$V_{CC}–V_{EE}$	40	Vdc
Sense Voltage (1)	V_{Sense1}	6.5	Vdc
Sense Voltage (2)	V_{Sense2}	6.5	Vdc
Remote Activation Input Voltage	V_{act}	7.0	Vdc
Output Current	I_O	300	mA
Operating Ambient Temperature Range	T_A	0 to +70	°C
Operating Junction Temperature	T_J	125	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

Simplified Application

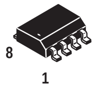


OVERVOLTAGE SENSING CIRCUIT

SEMICONDUCTOR TECHNICAL DATA

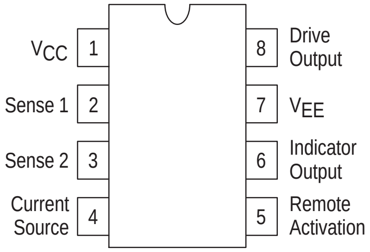


P1 SUFFIX
PLASTIC PACKAGE
CASE 626



D SUFFIX
PLASTIC PACKAGE
CASE 751
(SOP–8)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC3423D	T_A = 0° to +70°C	SO–8
MC3423P1		Plastic DIP

ELECTRICAL CHARACTERISTICS ($5.0\ V \le V_{CC} - V_{EE} \le 36\ V$, $T_{low} < T_A$, T_{high}, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Supply Voltage Range	V_{CC}–V_{EE}	4.5	–	40	Vdc
Output Voltage (I_O = 100 mA)	V_O	V_{CC}–2.2	V_{CC}–1.8	–	Vdc
Indicator Output Voltage ($I_{O(Ind)}$ = 1.6 mA)	V_{OL}(Ind)	–	0.1	0.4	Vdc
Sense Trip Voltage (T_A = 25°C)	V_{Sense1}, V_{Sense2}	2.45	2.6	2.75	Vdc
Temperature Coefficient of V_{Sense1} (Figure 2)	TCV_{S1}	–	0.06	–	%/°C
Remote Activation Input Current (V_{IH} = 2.0 V, $V_{CC} - V_{EE}$ = 5.0 V) (V_{IL} = 0.8 V, $V_{CC} - V_{EE}$ = 5.0 V)	 I_{IH} I_{IL}	 – –	 5.0 –120	 40 –180	µA
Source Current	I_{Source}	0.1	0.2	0.3	mA
Output Current Risetime (T_A = 25°C)	t_r	–	400	–	mA/µs
Propagation Delay Time (T_A = 25°C)	t_{pd}	–	0.5	–	µs
Supply Current	I_D	–	6.0	10	mA

NOTES: T_{low} to T_{high} = 0° to +70°C

Figure 1. Representative Block Diagram

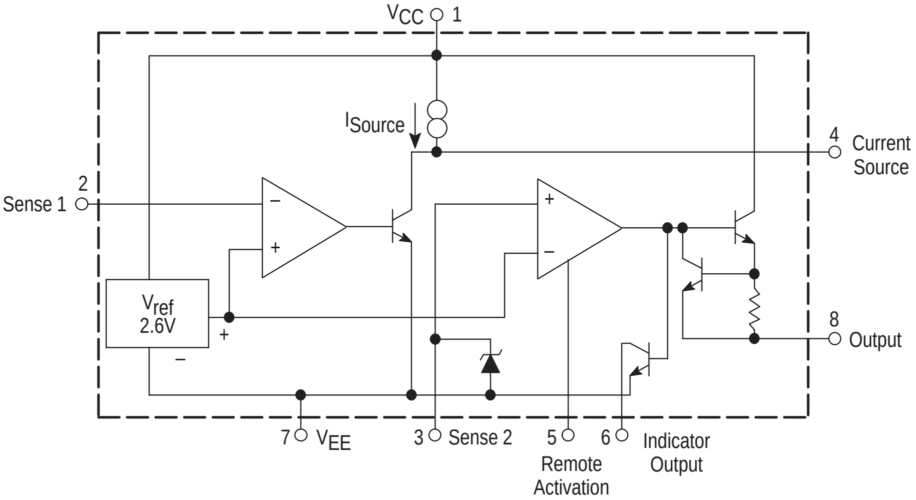
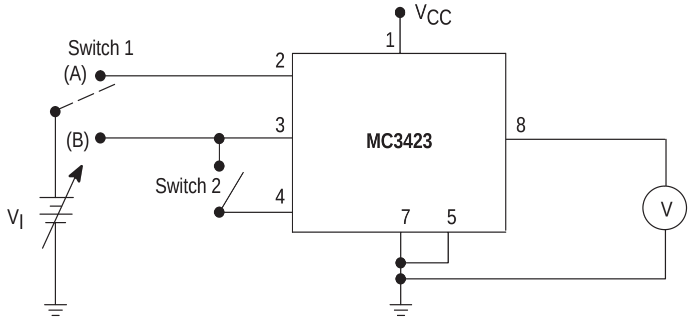


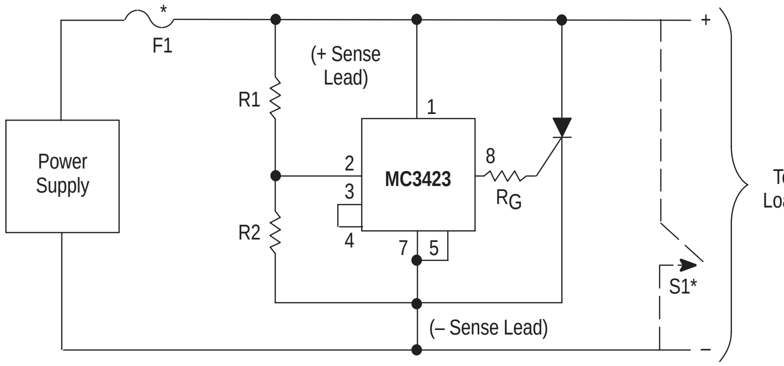
Figure 2. Sense Voltage Test Circuit



	Switch 1	Switch 2
$V_{Sense\ 1}$	Position A	Closed
$V_{Sense\ 2}$	Position B	Open

Ramp V_I until output goes high; this is the V_{Sense} threshold.

Figure 3. Basic Circuit Configuration



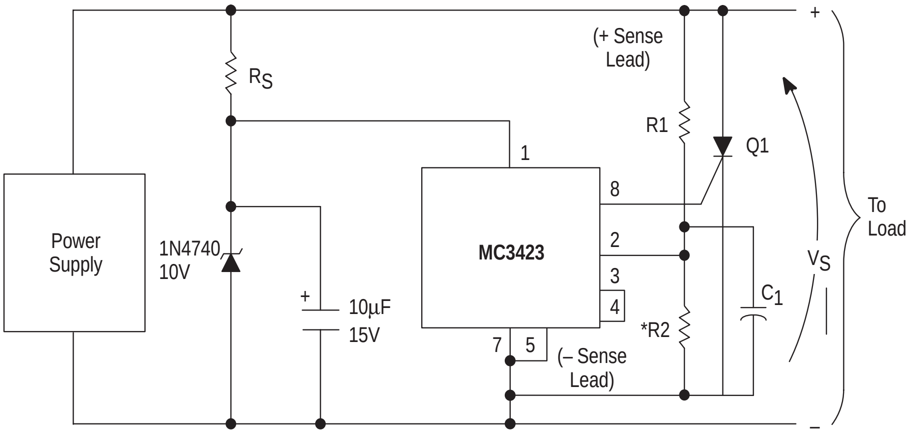
$$V_{trip} = V_{ref}\left(1 + \frac{R1}{R2}\right) \approx 2.6\ V\left(1 + \frac{R1}{R2}\right)$$

R2 ≤ 10 kΩ for minimum drift

For minimum value of R_G, see Figure 9.

*See text for explanation.

Figure 4. Circuit Configuration for Supply Voltage Above 36 V



$$C_1 > \frac{R_S}{R_1R_2}(R_1 + R_2)\ 10\mu F$$

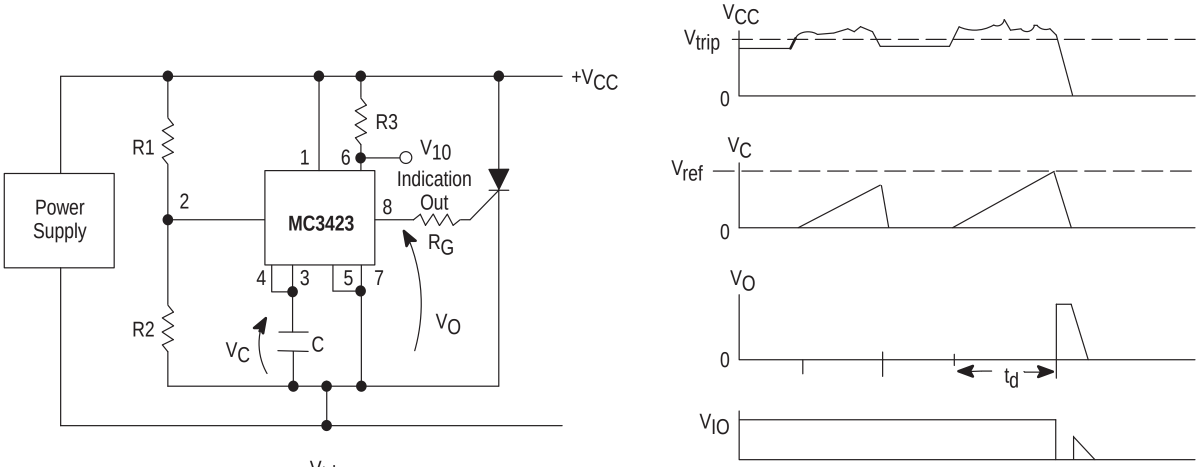
$$R_S = \left(\frac{V_S - 10}{25}\right) k\Omega$$

$$V_{trip} = V_{ref}\left(1 + \frac{R1}{R2}\right) \approx 2.6\ V\left(1 + \frac{R1}{R2}\right)$$

*R2 ≤ 10 kΩ

Q1: $V_S \le 50$ V; 2N6504 or equivalent
$V_S \le 100$ V; 2N6505 or equivalent
$V_S \le 200$ V; 2N6506 or equivalent
$V_S \le 400$ V; 2N6507 or equivalent
$V_S \le 600$ V; 2N6508 or equivalent
$V_S \le 800$ V; 2N6509 or equivalent

Figure 5. Basic Configuration for Programmable Duration of Overvoltage Condition Before Trip



$$R3 \ge \frac{V_{trip}}{10\ mA}$$

$$t_d = \frac{V_{ref}}{I_{source}} \times C \approx [12 \times 10^3]\ C$$

(See Figure 10)

APPLICATION INFORMATION

Basic Circuit Configuration

The basic circuit configuration of the MC3423 OVP is shown in Figure 3 for supply voltages from 4.5 V to 36 V, and in Figure 4 for trip voltages above 36 V. The threshold or trip voltage at which the MC3423 will trigger and supply gate drive to the crowbar SCR, Q1, is determined by the selection of R1 and R2. Their values can be determined by the equation given in Figures 3 and 4, or by the graph shown in Figure 8. The minimum value of the gate current limiting resistor, R_G, is given in Figure 9. Using this value of R_G, the SCR, Q1, will receive the greatest gate current possible without damaging the MC3423. If lower output currents are required, R_G can be increased in value. The switch, S1, shown in Figure 3 may be used to reset the crowbar. Otherwise, the power supply, across which the SCR is connected, must be shut down to reset the crowbar. If a non current–limited supply is used, a fuse or circuit breaker, F1, should be used to protect the SCR and/or the load.

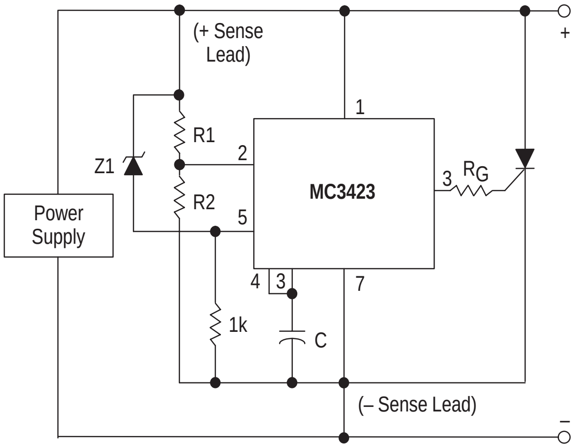
The circuit configurations shown in Figures 3 and 4 will have a typical propogation delay of 1.0 µs. If faster operation is desired, Pin 3 may be connected to Pin 2 with Pin 4 left floating. This will result in decreasing the propogation delay to approximately 0.5 µs at the expense of a slightly increased TC for the trip voltage value.

Configuration for Programmable Minimum Duration of Overvoltage Condition Before Tripping

In many instances, the MC3423 OVP will be used in a noise environment. To prevent false tripping of the OVP circuit by noise which would not normally harm the load, MC3423 has a programmable delay feature. To implement this feature, the circuit configuration of Figure 5 is used. In this configuration, a capacitor is connected from Pin 3 to V_{EE}. The value of this capacitor determines the minimum duration of the overvoltage condition which is necessary to trip the OVP. The value of C can be found from Figure 10. The circuit operates in the following manner: When V_{CC} rises above the trip point set by R1 and R2, an internal current source (Pin 4) begins charging the capacitor, C, connected to Pin 3. If the overvoltage condition disappears before this occurs, the capacitor is discharged at a rate ≅ 10 times faster than the charging rate, resetting the timing feature until the next overvoltage condition occurs.

Occasionally, it is desired that immediate crowbarring of the supply occur when a high overvoltage condition occurs, while retaining the false tripping immunity of Figure 5. In this case, the circuit of Figure 6 can be used. The circuit will operate as previously described for small overvoltages, but will immediately trip if the power supply voltage exceeds V_{Z1} + 1.4 V.

Figure 6. Configuration for Programmable Duration of Overvoltage Condition Before Trip/With Immediate Trip at High Overvoltages



Additional Features

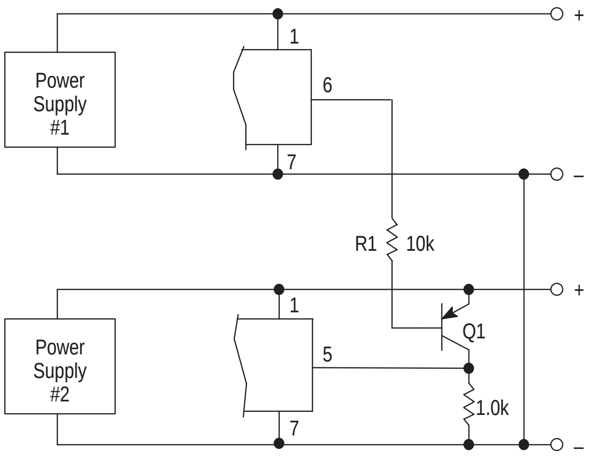
1. Activation Indication Output

An additional output for use as an indicator of OVP activation is provided by the MC3423. This output is an open collector transistor which saturates when the OVP is activated. In addition, it can be used to clock an edge triggered flip–flop whose output inhibits or shuts down the power supply when the OVP trips. This reduces or eliminates the heatsinking requirements for the crowbar SCR.

2. Remote Activation Input

Another feature of the MC3423 is its remote activation input, Pin 5. If the voltage on this CMOS/TTL compatible input is held below 0.8 V, the MC3423 operates normally. However, if it is raised to a voltage above 2.0 V, the OVP output is activated independent of whether or not an overvoltage condition is present. It should be noted that Pin 5 has an internal pull–up current source. This feature can be used to accomplish an orderly and sequenced shutdown of system power supplies during a system fault condition. In addition, the activation indication output of one MC3423 can be used to activate another MC3423 if a single transistor inverter is used to interface the former's indication output to the latter's remote activation input, as shown in Figure 7. In this circuit, the indication output (Pin 6) of the MC3423 on power supply 1 is used to activate the MC3423 associated with power supply 2. Q1 is any small PNP with adequate voltage rating.

Figure 7. Circuit Configuration for Activating One MC3423 from Another



Note that both supplies have their negative output leads tied together (i.e., both are positive supplies). If their positive leads are common (two negative supplies) the emitter of Q1 would be moved to the positive lead of supply 1 and R1 would therefore have to be resized to deliver the appropriate drive to Q1.

Crowbar SCR Considerations

Referring to Figure 11, it can be seen that the crowbar SCR, when activated, is subject to a large current surge from the output capacitance, C_{out}. This capacitance consists of the power supply output caps, the load's decoupling caps, and in the case of Figure 11A, the supply's input filter caps. This surge current is illustrated in Figure 12, and can cause SCR failure or degradation by any one of three mechanisms: di/dt, absolute peak surge, or I^2t. The interrelationship of these failure methods and the breadth of the applications make specification of the SCR by the semiconductor manufacturer difficult and expensive. Therefore, the designer must empirically determine the SCR and circuit elements which result in reliable and effective OVP operation. However, an understanding of the factors which influence the SCR's di/dt and surge capabilities simplifies this task.

di/dt

As the gate region of the SCR is driven on, its area of conduction takes a finite amount of time to grow, starting as a very small region and gradually spreading. Since the anode current flows through this turned–on gate region, very high current densities can occur in the gate region if high anode currents appear quickly (di/dt). This can result in immediate destruction of the SCR or gradual degradation of its forward blocking voltage capabilities – depending on the severity of the occasion.

Figure 8. R1 versus Trip Voltage

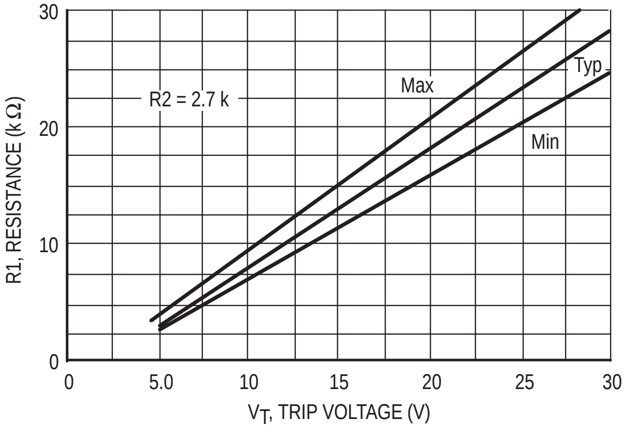


Figure 9. Minimum R_G versus Supply Voltage

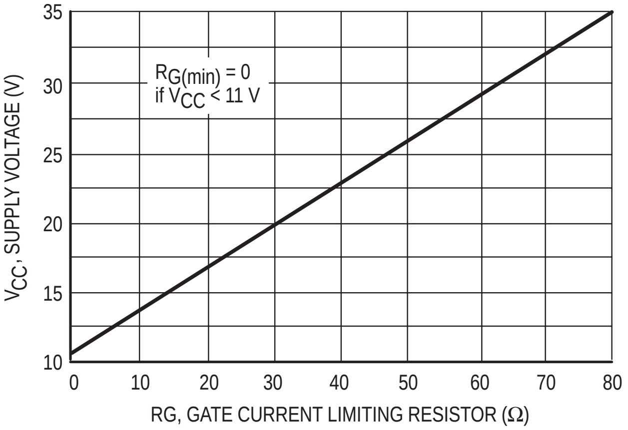


Figure 10. Capacitance versus Minimum Overvoltage Duration

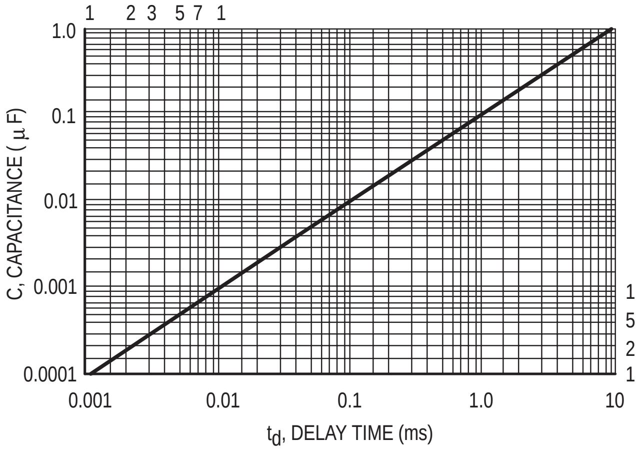
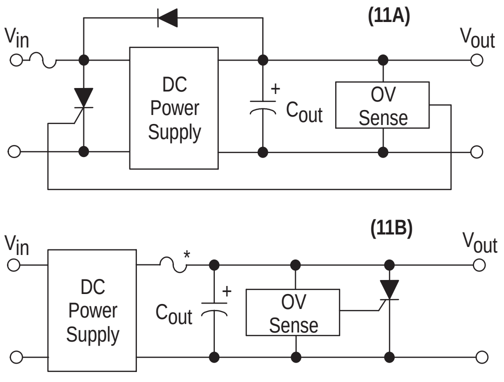


Figure 11. Typical Crowbar OVP Circuit Configurations



*Needed if supply not current limited

Figure 12. Crowbar SCR Surge Current Waveform

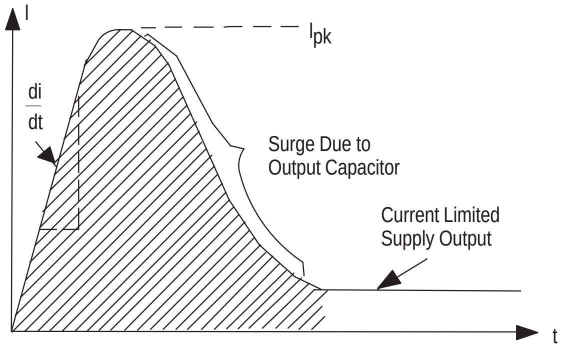
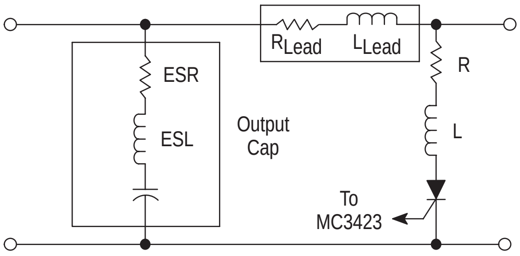


Figure 13. Circuit Elements Affecting SCR Surge and di/dt



R & L EMPIRICALLY DETERMINED!

The usual design compromise then is to use a garden variety fuse (3AG or 3AB style) which cannot be relied on to blow before the thyristor does, and trust that if the SCR does fail, it will fail short circuit. In the majority of the designs, this will be the case, though this is difficult to guarantee. Of course, a sufficiently high surge will cause an open. These comments also apply to the fuse in Figure 11B.

The value of di/dt that an SCR can safely handle is influenced by its construction and the characteristics of the gate drive signal. A center–gate–fire SCR has more di/dt capability than a corner–gate–fire type, and heavily overdriving (3 to 5 times I_{GT}) the SCR gate with a fast < 1.0 µs rise time signal will maximize its di/dt capability. A typical maximum number in phase control SCRs of less than 50 A(RMS) rating might be 200 A/µs, assuming a gate current of five times I_{GT} and < 1.0 µs rise time. If having done this, a di/dt problem is seen to still exist, the designer can also decrease the di/dt of the current waveform by adding inductance in series with the SCR, as shown in Figure 13. Of course, this reduces the circuit's ability to rapidly reduce the DC bus voltage and a tradeoff must be made between speedy voltage reduction and di/dt.

Surge Current

If the peak current and/or the duration of the surge is excessive, immediate destruction due to device overheating will result. The surge capability of the SCR is directly proportional to its die area. If the surge current cannot be reduced (by adding series resistance – see Figure 13) to a safe level which is consistent with the systems requirements for speedy bus voltage reduction, the designer must use a higher current SCR. This may result in the average current capability of the SCR exceeding the steady state current requirements imposed by the DC power supply.

A WORD ABOUT FUSING

Before leaving the subject of the crowbar SCR, a few words about fuse protection are in order. Referring back to Figure 11A, it will be seen that a fuse is necessary if the power supply to be protected is not output current limited. This fuse is not meant to prevent SCR failure but rather to prevent a fire!

In order to protect the SCR, the fuse would have to possess an I^2t rating less than that of the SCR and yet have a high enough continuous current rating to survive normal supply output currents. In addition, it must be capable of successfully clearing the high short circuit currents from the supply. Such a fuse as this is quite expensive, and may not even be available.

CROWBAR SCR SELECTION GUIDE

As an aid in selecting an SCR for crowbar use, the following selection guide is presented.

Device	I_{RMS}	I_{FSM}	Package
2N6400 Series	16 A	160 A	TO–220 Plastic
2N6504 Series	25 A	160 A	TO–220 Plastic
2N1842 Series	16 A	125 A	Metal Stud
2N2573 Series	25 A	260 A	Metal TO–3 Type
2N681 Series	25 A	200 A	Metal Stud
MCR3935–1 Series	35 A	350 A	Metal Stud
MCR81–5 Series	80 A	1000 A	Metal Stud

MOTOROLA

MC3425

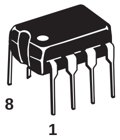
Power Supply Supervisory/ Over and Undervoltage Protection Circuit

The MC3425 is a power supply supervisory circuit containing all the necessary functions required to monitor over and undervoltage fault conditions. These integrated circuits contain dedicated over and undervoltage sensing channels with independently programmable time delays. The overvoltage channel has a high current Drive Output for use in conjunction with an external SCR Crowbar for shutdown. The undervoltage channel input comparator has hysteresis which is externally programmable, and an open–collector output for fault indication.

- Dedicated Over and Undervoltage Sensing
- Programmable Hysteresis of Undervoltage Comparator
- Internal 2.5 V Reference
- 300 mA Overvoltage Drive Output
- 30 mA Undervoltage Indicator Output
- Programmable Time Delays
- 4.5 V to 40 V Operation

POWER SUPPLY SUPERVISORY/ OVER AND UNDERVOLTAGE PROTECTION CIRCUIT

SEMICONDUCTOR TECHNICAL DATA



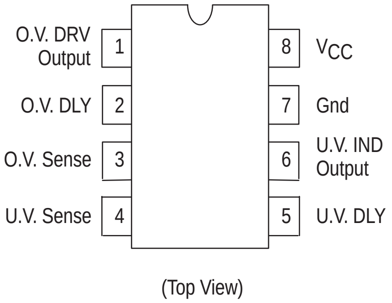
P1 SUFFIX
PLASTIC PACKAGE
CASE 626

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	40	Vdc
Comparator Input Voltage Range (Note 1)	V_{IR}	–0.3 to +40	Vdc
Drive Output Short Circuit Current	$I_{OS(DRV)}$	Internally Limited	mA
Indicator Output Voltage	V_{IND}	0 to 40	Vdc
Indicator Output Sink Current	I_{IND}	30	mA
Power Dissipation and Thermal Characteristics Maximum Power Dissipation @ T_A = 70°C Thermal Resistance, Junction–to–Air	 P_D $R_{\theta JA}$	 1000 80	 mW °C/W
Operating Junction Temperature	T_J	+150	°C
Operating Ambient Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	–55 to +150	°C

NOTE: 1. The input signal voltage should not be allowed to go negative by more than 300 mV or positive by more than 40 V, independent of V_{CC}, without device destruction.

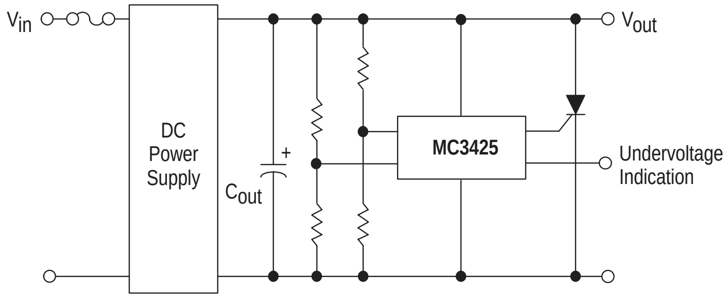
PIN CONNECTIONS



(Top View)

Simplified Application

Overvoltage Crowbar Protection, Undervoltage Indication



ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC3425P1	T_A = 0° to +70°C	Plastic DIP

ELECTRICAL CHARACTERISTICS (4.5 V ≤ V_{CC} ≤ 40 V; T_A = T_{low} to T_{high} [Note 2], unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
REFERENCE SECTION					
Sense Trip Voltage (Referenced Voltage)	V_{Sense}				Vdc
V_{CC} = 15 V					
T_A= 25°C		2.4	2.5	2.6	
T_{low} to T_{high} (Note 2)		2.33	2.5	2.63	
Line Regulation of V_{Sense} 4.5 V ≤ V_{CC} ≤ 40 V; T_J = 25°C	Reg_{line}	–	7.0	15	mV
Power Supply Voltage Operating Range	V_{CC}	4.5	–	40	Vdc
Power Supply Current					
V_{CC} = 40 V; T_A = 25°C; No Output Loads					
O.V. Sense (Pin 3) = 0 V; U.V. Sense (Pin 4) = V_{CC}	$I_{CC(off)}$	–	8.5	10	mA
O.V. Sense (Pin 3) = V_{CC}; U.V. Sense (Pin 4) = 0 V	$I_{CC(on)}$	–	16.5	19	mA
INPUT SECTION					
Input Bias Current, O.V. and U.V. Sense	I_{IB}	–	1.0	2.0	µA
Hysteresis Activation Voltage, U.V. Sense	$V_{H(act)}$				V
V_{CC} = 15 V; T_A = 25°C;					
I_H = 10%		–	0.6	–	
I_H = 90%		–	0.8	–	
Hysteresis Current, U.V. Sense V_{CC} = 15 V; T_A = 25°C; U.V. Sense (Pin 4) = 2.5 V	I_H	9.0	12.5	16	µA
Delay Pin Voltage (I_{DLY} = 0 mA)					V
Low State	$V_{OL(DLY)}$	–	0.2	0.5	
High State	$V_{OH(DLY)}$	V_{CC}–0.5	V_{CC}–0.15	–	
Delay Pin Source Current V_{CC} = 15 V; V_{DLY} = 0 V	$I_{DLY(source)}$	140	200	260	µA
Delay Pin Sink Current V_{CC} = 15 V; V_{DLY} = 2.5V	$I_{DLY(sink)}$	1.8	3.0	–	mA
OUTPUT SECTION					
Drive Output Peak Current (T_A = 25°C)	$I_{DRV(peak)}$	200	300	–	mA
Drive Output Voltage I_{DRV} = 100 mA; T_A = 25° C	$V_{OH(DRV)}$	V_{CC}–2.5	V_{CC}–2.0	–	V
Drive Output Leakage Current V_{DRV} = 0 V	$I_{DRV(leak)}$	–	15	200	nA
Drive Output Current Slew Rate (T_A = 25°C)	di/dt	–	2.0	–	A/µs
Drive Output V_{CC} Transient Rejection V_{CC} = 0 V to 15 V at dV/dt = 200 V µs; O.V. Sense (Pin 3) = 0 V; T_A = 25°C	$I_{DRV(trans)}$	–	1.0	–	mA (Peak)
Indicator Output Saturation Voltage I_{IND} = 30 mA; T_A = 25°C	$V_{IND(sat)}$	–	560	800	mV
Indicator Output Leakage Current $V_{OH(IND)}$ = 40 V	$I_{IND(leak)}$	–	25	200	nA
Output Comparator Threshold Voltage (Note 3)	$V_{th(OC)}$	2.33	2.5	2.63	V
Propagation Delay Time					
(V_{CC} = 15 V; T_A = 25°C)					
Input to Drive Output or Indicator Output 100 mV Overdrive, C_{DLY} = 0 µF	$t_{PLH(IN/OUT)}$	–	1.7	–	µs
Input to Delay 2.5 V Overdrive (0 V to 5.0 V Step)	$t_{PLH(IN//DLY)}$	–	700	–	ns

NOTES: 2. T_{low} to T_{high} = 0° to +70°C
3. The $V_{th(OC)}$ limits are approximately the V_{Sense} limits over the applicable temperature range.

Figure 1. Hysteresis Current versus Hysteresis Activation Voltage

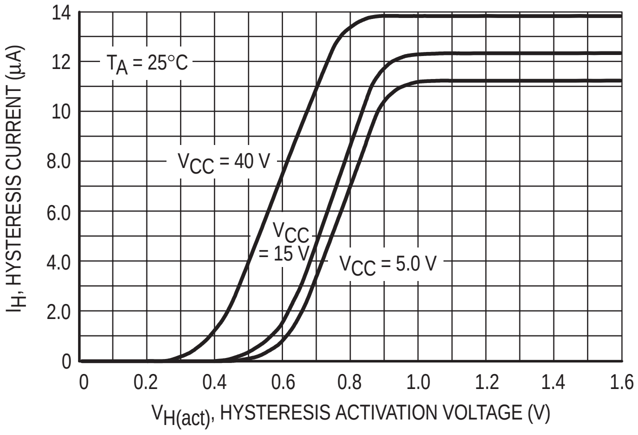


Figure 2. Hysteresis Activation Voltage versus Temperature

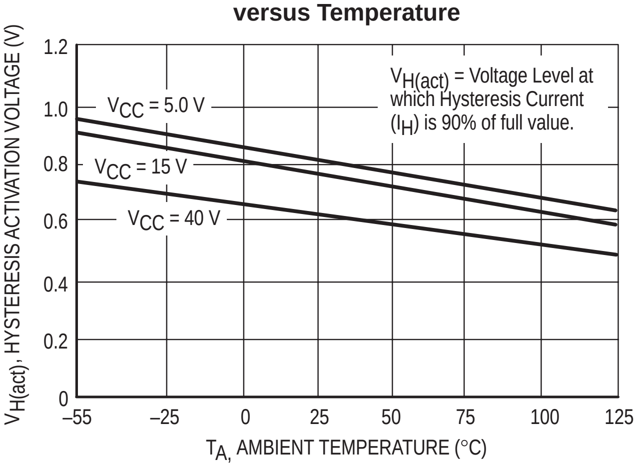


Figure 3. Hysteresis Current versus Temperature

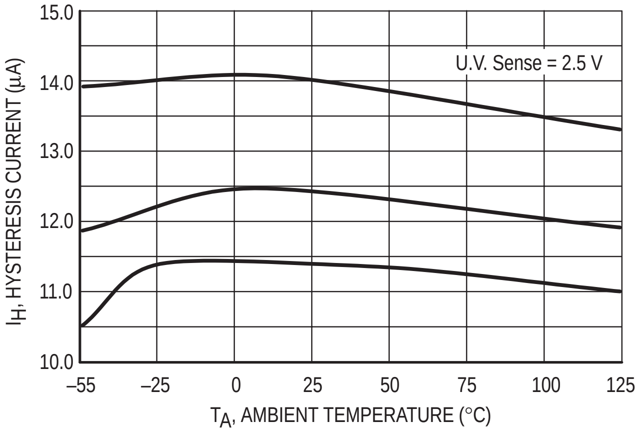


Figure 4. Sense Trip Voltage Change versus Temperature

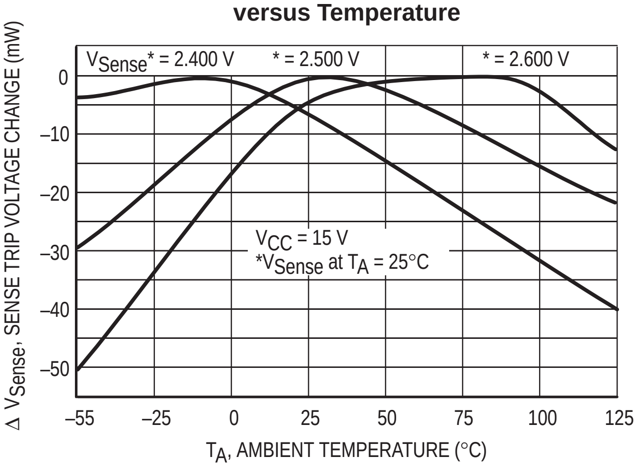


Figure 5. Output Delay Time versus Delay Capacitance

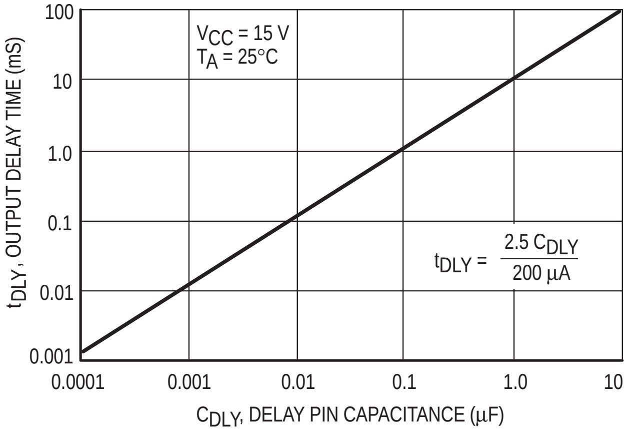


Figure 6. Delay Pin Source Current versus Temperature

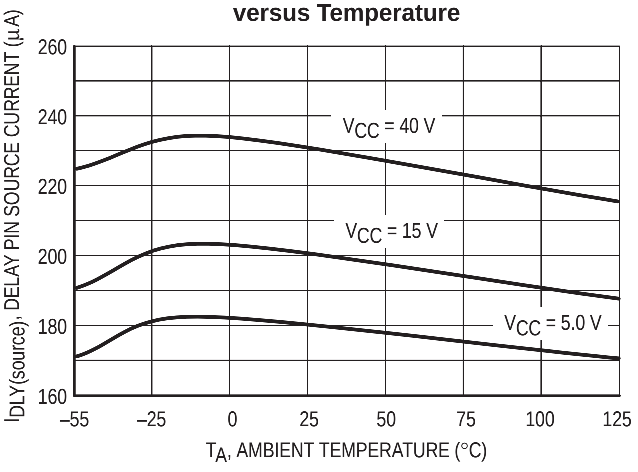


Figure 7. Drive Output Saturation Voltage versus Output Peak Current

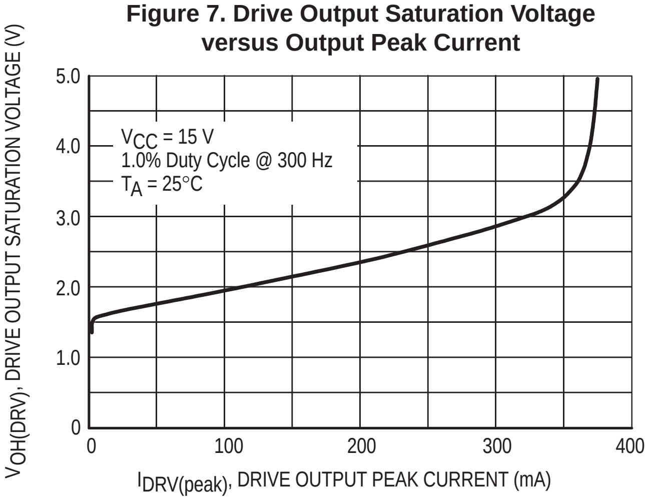


Figure 8. Indicator Output Saturation Voltage versus Output Sink Current

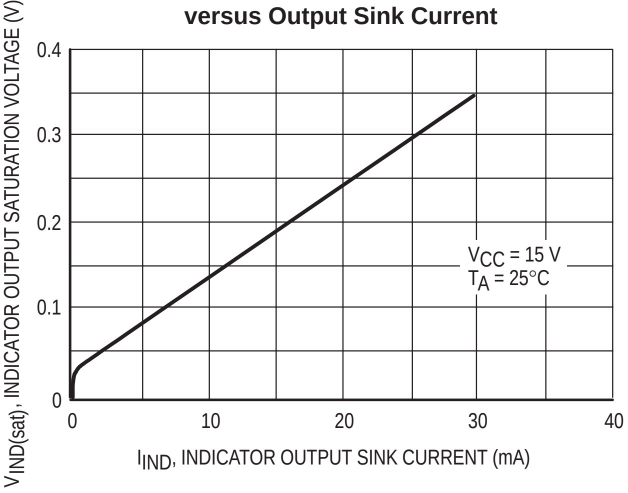


Figure 9. Drive Output Saturation Voltage versus Temperature

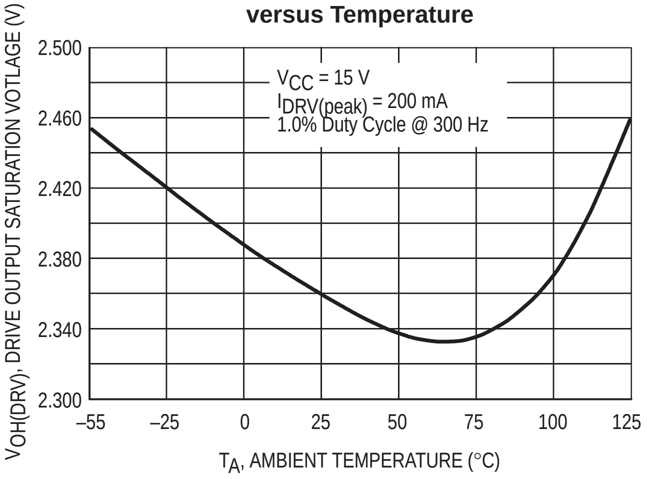
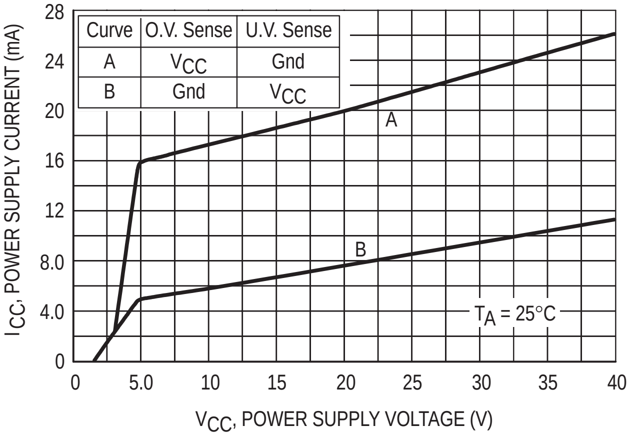
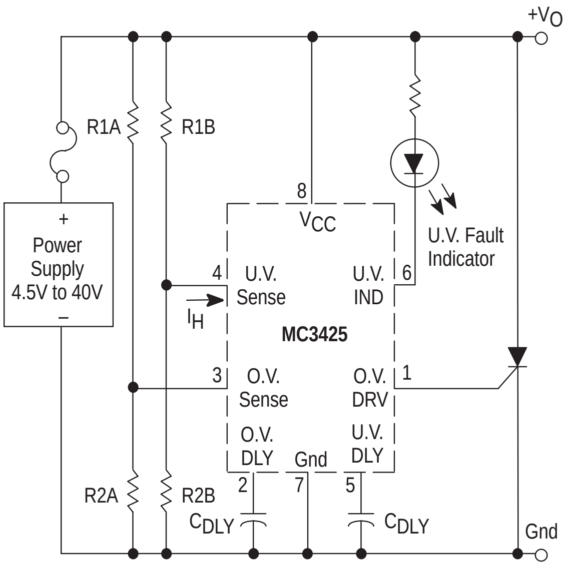


Figure 10. Power Supply Current versus Voltage



APPLICATIONS INFORMATION

Figure 11. Overvoltage Protection and Undervoltage Fault Indication with Programmable Delay



$$\text{U.V. Hysteresis} = I_H\left(\frac{R1B\ R2B}{R1B + R2B}\right),\ V_{O(trip)} - 2.5\ V\left(1 + \frac{R1A}{R2A}\right)$$

$$t_{DLY} = 12500\ C_{DLY}$$

Figure 12. Overvoltage Protection of 5.0 V Supply with Line Loss Detector

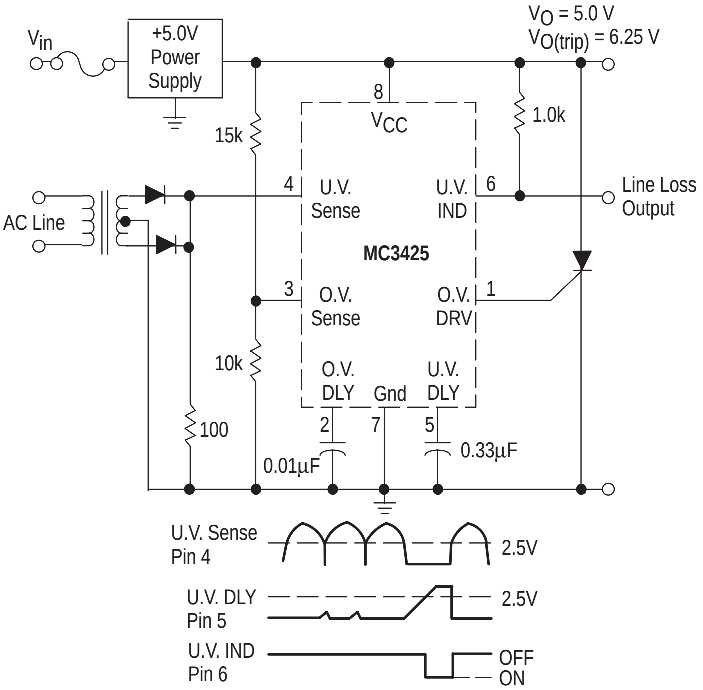


Figure 13. Overvoltage Audio Alarm Circuit

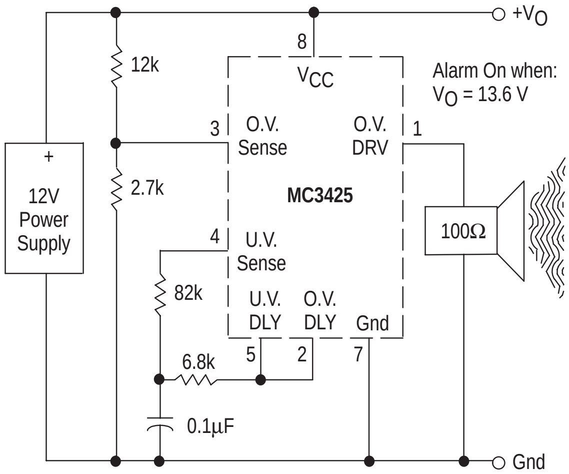
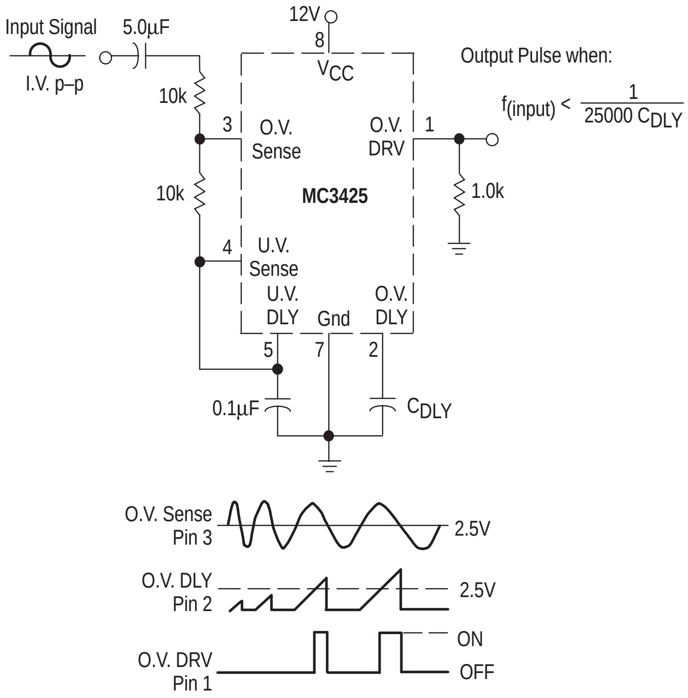


Figure 14. Programmable Frequency Switch



CIRCUIT DESCRIPTION

The MC3425 is a power supply supervisory circuit containing all the necessary functions required to monitor over and undervoltage fault conditions. The block diagram is shown below in Figure 15. The Overvoltage (O.V.) and Undervoltage (U.V.) Input Comparators are both referenced to an internal 2.5 V regulator. The U.V. Input Comparator has a feedback activated 12.5 µA current sink (I_H) which is used for programming the input hysteresis voltage (V_H). The source resistance feeding this input (R_H) determines the amount of hysteresis voltage by $V_H = I_H R_H = 12.5 \times 10^{-6} R_H$.

Separate Delay pins (O.V. DLY, U.V. DLY.) are provided for each channel to independently delay the Drive and Indicator outputs, thus providing greater input noise immunity. The two Delay pins are essentially the outputs of the respective input comparators, and provide a constant current source, $I_{DLY(source)}$, of typically 200 µA when the noninverting input voltage is greater than the inverting input level. A capacitor connected from these Delay pins to ground, will establish a predictable delay time (t_{DLY}) for the Drive and Indicator outputs. The Delay pins are internally connected to the noninverting inputs of the O.V. and U.V. Output Comparators, which are referenced to the internal 2.5 V regulator. Therefore, delay time (t_{DLY}) is based on the constant current source, $I_{DLY(source)}$, charging the external delay capacitor (C_{DLY}) to 2.5 V.

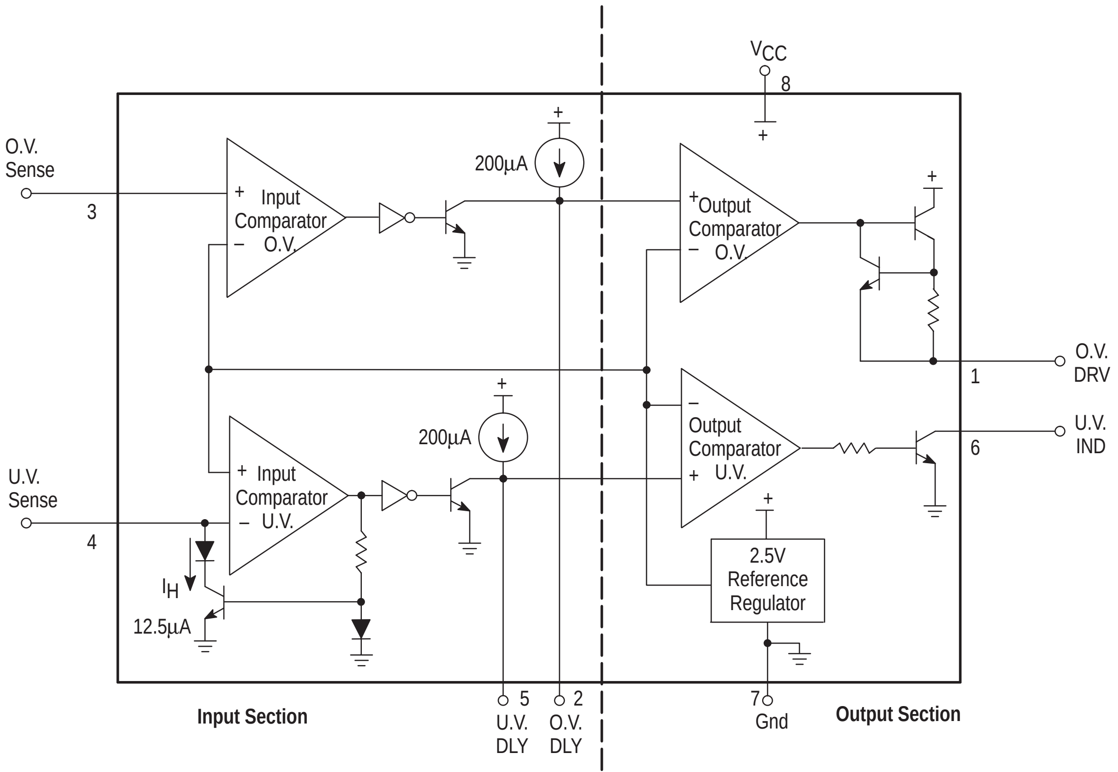
$$t_{DLY} = \frac{V_{ref}\, C_{DLY}}{I_{DLY(source)}} = \frac{2.5\, C_{DLY}}{200\ \mu A} = 12500\, C_{DLY}$$

Figure 5 provides C_{DLY} values for a wide range of time delays. The Delay pins are pulled low when the respective input comparator's noninverting input is less than the inverting input. The sink current, $I_{DLY(sink)}$, capability of the Delay pins is ≥ 1.8 mA and is much greater than the typical 200 µA source current, thus enabling a relatively fast delay capacitor discharge time.

The Overvoltage Drive Output is a current–limited emitter–follower capable of sourcing 300 mA at a turn–on slew rate at 2.0 A/µs, ideal for driving "Crowbar" SCR's. The Undervoltage Indicator Output is an open–collector, NPN transistor, capable of sinking 30 mA to provide sufficient drive for LED's, small relays or shut–down circuitry. These current capabilities apply to both channels operating simultaneously, providing device power dissipation limits are not exceeded.

The MC3425 has an internal 2.5 V bandgap reference regulator with an accuracy of ± 4.0% for the basic device.

Figure 15. Representative Block Diagram



Note: All voltages and currents are nominal.

CROWBAR SCR CONSIDERATIONS

Referring to Figure 16, it can be seen that the crowbar SCR, when activated, is subject to a large current surge from the output capacitance, C_{out}. This capacitance consists of the power supply output capacitors, the load's decoupling capacitors, and in the case of Figure 16A, the supply's input filter capacitors. This surge current is illustrated in Figure 17, and can cause SCR failure or degradation by any one of three mechanisms: di/dt, absolute peak surge, or I^2t. The interrelationship of these failure methods and the breadth of the applications make specification of the SCR by the semiconductor manufacturer difficult and expensive. Therefore, the designer must empirically determine the SCR and circuit elements which result in reliable and effective OVP operation. However, an understanding of the factors which influence the SCR's di/dt and surge capabilities simplifies this task.

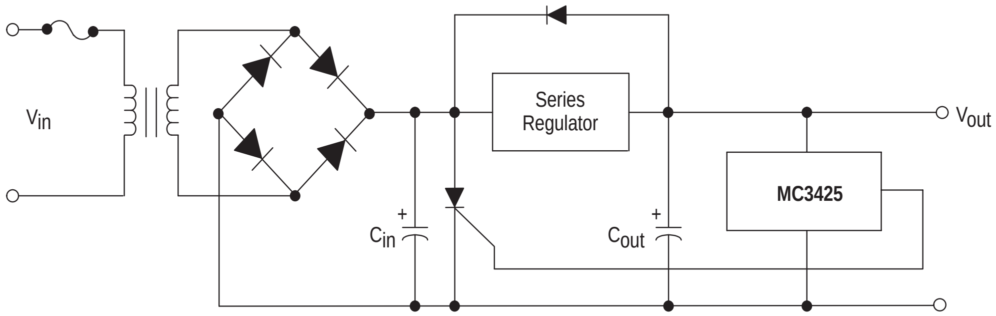
1. di/dt

As the gate region of the SCR is driven on, its area of conduction takes a finite amount of time to grow, starting as a very small region and gradually spreading. Since the anode current flows through this turned–on gate region, very high current densities can occur in the gate region if high anode currents appear quickly (di/dt). This can result in immediate destruction of the SCR or gradual degradation of its forward blocking voltage capabilities – depending on the severity of the occasion.

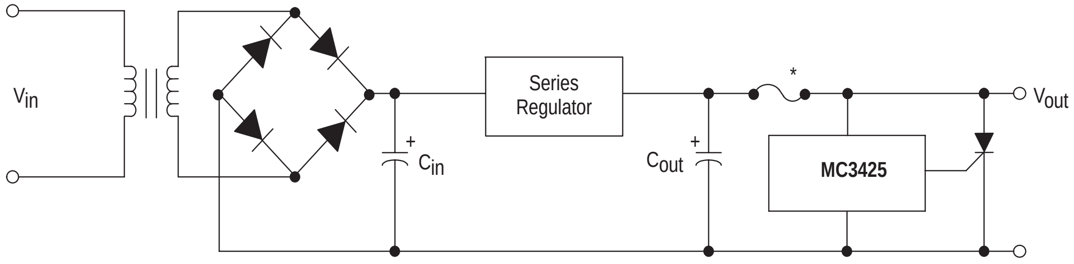
The value of di/dt that an SCR can safely handle is influenced by its construction and the characteristics of the gate drive signal. A center–gate–fire SCR has more di/dt capability than a corner–gate–fire type, and heavily overdriving (3 to 5 times I_{GT}) the SCR gate with a fast < 1.0 µs rise time signal will maximize its di/dt capability. A typical maximum number in phase control SCRs of less than 50 A(RMS) rating might be 200 A/µs, assuming a gate current of five times I_{GT} and < 1.0 µs rise time. If having done this, a di/dt problem is seen to still exist, the designer can also decrease the di/dt of the current waveform by adding inductance in series with the SCR, as shown in Figure 18. Of course, this reduces the circuit's ability to rapidly reduce the dc bus voltage and a tradeoff must be made between speedy voltage reduction and di/dt.

Figure 16. Typical Crowbar Circuit Configurations

(A) SCR Across Input of Regulator

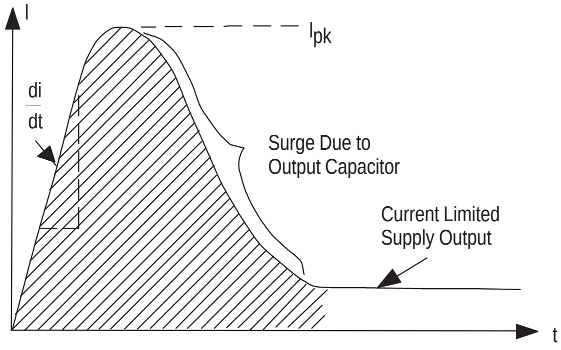


(B) SCR Across Output of Regulator



*Needed if supply is not current limited.

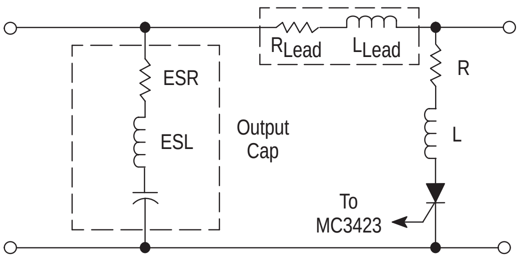
Figure 17. Crowbar SCR Surge Current Waveform



2. Surge Current

If the peak current and/or the duration of the surge is excessive, immediate destruction due to device overheating will result. The surge capability of the SCR is directly proportional to its die area. If the surge current cannot be reduced (by adding series resistance – see Figure 18) to a safe level which is consistent with the system's requirements for speedy bus voltage reduction, the designer must use a higher current SCR. This may result in the average current capability of the SCR exceeding the steady state current requirements imposed by the DC power supply.

Figure 18. Circuit Elements Affecting SCR Surge & di/dt



R & L EMPIRICALLY DETERMINED!

UNDERVOLTAGE SENSING

An undervoltage sense circuit with hysteresis may be designed, as shown in Figure 11, using the following equations:

$$R1 = \frac{V_{CCU} - V_{CC1}}{12.5\ \mu A}$$

$$R2 = \frac{2.5\ R1}{V_{CC1} - 2.5}$$

where: V_{CCU} is the designed upper trip point (output indicator goes off)
V_{CC1} is the lower trip point (output indicator goes on)

A WORD ABOUT FUSING

Before leaving the subject of the crowbar SCR, a few words about fuse protection are in order. Referring back to Figure 16A, it will be seen that a fuse is necessary if the power supply to be protected is not output current limited. This fuse is not meant to prevent SCR failure but rather to prevent a fire!

In order to protect the SCR, the fuse would have to possess an I^2t rating less than that of the SCR and yet have a high enough continuous current rating to survive normal supply output currents. In addition, it must be capable of successfully clearing the high short circuit currents from the supply. Such a fuse as this is quite expensive, and may not even be available.

The usual design compromise then is to use a garden variety fuse (3AG or 3AB style) which cannot be relied on to blow before the thyristor does, and trust that if the SCR does fail, it will fail short circuit. In the majority of the designs, this will be the case, though this is difficult to guarantee. Of course, a sufficiently high surge will cause an open. These comments also apply to the fuse in Figure 16B.

CROWBAR SCR SELECTION GUIDE

As an aid in selecting an SCR for crowbar use, the following selection guide is presented.

Device	I_{RMS}	I_{TSM}
MCR310 Series	10 A	100 A
MCR16 Series	16 A	150 A
MCR25 Series	25 A	300 A
2N6501 Series	25 A	300 A
MCR69 Series	25 A	750 A
MCR264 Series	40 A	400 A
MCR265 Series	55 A	550 A

MOTOROLA

MC7800 Series

Three-Terminal Positive Voltage Regulators

These voltage regulators are monolithic integrated circuits designed as fixed–voltage regulators for a wide variety of applications including local, on–card regulation. These regulators employ internal current limiting, thermal shutdown, and safe–area compensation. With adequate heatsinking they can deliver output currents in excess of 1.0 A. Although designed primarily as a fixed voltage regulator, these devices can be used with external components to obtain adjustable voltages and currents.

- Output Current in Excess of 1.0 A
- No External Components Required
- Internal Thermal Overload Protection
- Internal Short Circuit Current Limiting
- Output Transistor Safe–Area Compensation
- Output Voltage Offered in 2% and 4% Tolerance
- Available in Surface Mount D^{2}PAK and Standard 3–Lead Transistor Packages

DEVICE TYPE/NOMINAL OUTPUT VOLTAGE

MC7805	5.0 V	MC7812	12 V
MC7806	6.0 V	MC7815	15 V
MC7808	8.0 V	MC7818	18 V
MC7809	9.0 V	MC7824	24 V

ORDERING INFORMATION

Device	Output Voltage Tolerance	Operating Temperature Range	Package
MC78XXACT	2%	T_J = 0° to +125°C	Insertion Mount
MC78XXACD2T			Surface Mount
MC78XXCT	4%		Insertion Mount
MC78XXCD2T			Surface Mount
MC78XXBT		T_J = – 40° to +125°C	Insertion Mount
MC78XXBD2T			Surface Mount

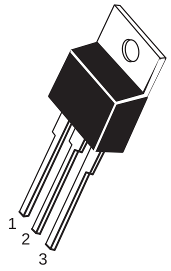
XX indicates nominal voltage.

THREE–TERMINAL POSITIVE FIXED VOLTAGE REGULATORS

SEMICONDUCTOR TECHNICAL DATA

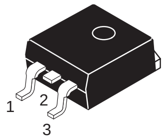
T SUFFIX
PLASTIC PACKAGE
CASE 221A

Heatsink surface connected to Pin 2.



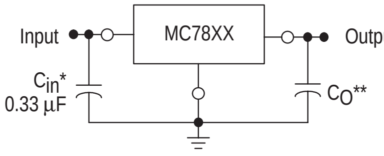
Pin 1. Input
2. Ground
3. Output

D2T SUFFIX
PLASTIC PACKAGE
CASE 936
(D^{2}PAK)



Heatsink surface (shown as terminal 4 in case outline drawing) is connected to Pin 2.

STANDARD APPLICATION



A common ground is required between the input and the output voltages. The input voltage must remain typically 2.0 V above the output voltage even during the low point on the input ripple voltage.

XX, These two digits of the type number indicate nominal voltage.

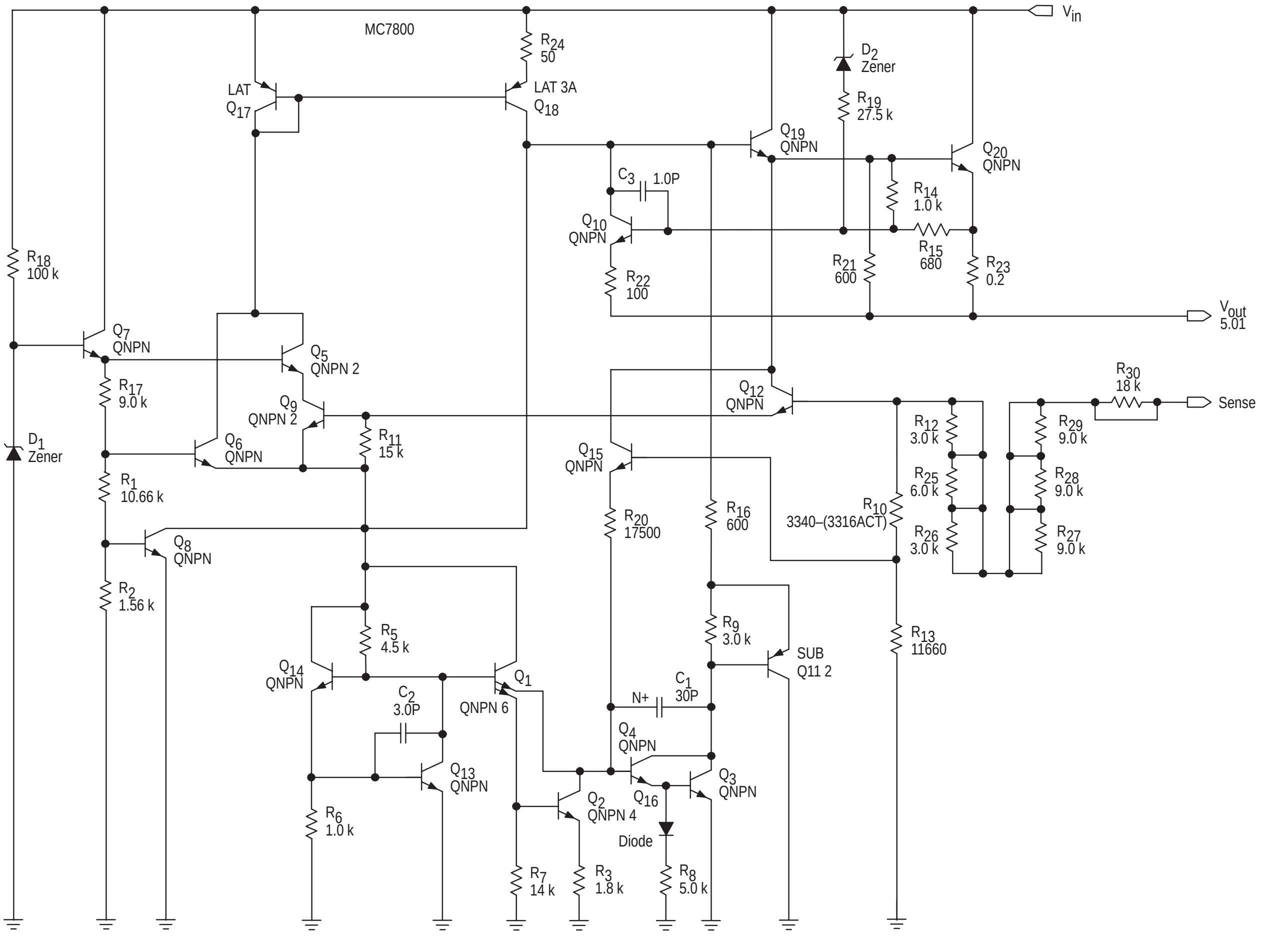
* C_{in} is required if regulator is located an appreciable distance from power supply filter.

** C_O is not needed for stability; however, it does improve transient response. Values of less than 0.1 µF could cause instability.

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Input Voltage (5.0 – 18 V) (24 V)	V_I	35 40	Vdc
Power Dissipation			
Case 221A			
T_A = 25°C	P_D	Internally Limited	W
Thermal Resistance, Junction–to–Ambient	$R_{\theta JA}$	65	°C/W
Thermal Resistance, Junction–to–Case	$R_{\theta JC}$	5.0	°C/W
Case 936 (D^2PAK)			
T_A = 25°C	P_D	Internally Limited	W
Thermal Resistance, Junction–to–Ambient	$R_{\theta JA}$	See Figure 13	°C/W
Thermal Resistance, Junction–to–Case	$R_{\theta JA}$	5.0	°C/W
Storage Junction Temperature Range	T_{stg}	–65 to +150	°C
Operating Junction Temperature	T_J	+150	°C

Representative Schematic Diagram



This device contains 22 active transistors.

ELECTRICAL CHARACTERISTICS (V_{in} = 10 V, I_O = 500 mA, T_J = T_{low} to T_{high} [Note 1], unless otherwise noted.)

Characteristic	Symbol	MC7805B			MC7805C			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = 25°C)	V_O	4.8	5.0	5.2	4.8	5.0	5.2	Vdc
Output Voltage (5.0 mA ≤ I_O ≤ 1.0 A, P_D ≤15 W)	V_O							Vdc
7.0 Vdc ≤ V_{in} ≤ 20 Vdc		–	–	–	4.75	5.0	5.25	
8.0 Vdc ≤ V_{in} ≤ 20 Vdc		4.75	5.0	5.25	–	–	–	
Line Regulation, T_J = 25°C (Note 2)	Reg_{line}							mV
7.0 Vdc ≤ V_{in} ≤ 25 Vdc		–	5.0	100	–	5.0	100	
8.0 Vdc ≤ V_{in} ≤ 12 Vdc		–	1.3	50	–	1.3	50	
Load Regulation, T_J = 25°C (Note 2)	Reg_{load}							mV
5.0 mA ≤ I_O ≤ 1.5 A		–	1.3	100	–	1.3	100	
250 mA ≤ I_O ≤ 750 mA		–	0.15	50	–	0.15	50	
Quiescent Current (T_J = 25°C)	I_B	–	3.2	8.0	–	3.2	8.0	mA
Quiescent Current Change	ΔI_B							mA
7.0 Vdc ≤ V_{in} ≤ 25 Vdc		–	–	–	–	–	1.3	
8.0 Vdc ≤ V_{in} ≤ 25 Vdc		–	–	1.3	–	–	–	
5.0 mA ≤ I_O ≤ 1.0 A		–	–	0.5	–	–	0.5	
Ripple Rejection	RR							dB
8.0 Vdc ≤ V_{in} ≤ 18 Vdc, f = 120 Hz		–	68	–	–	68	–	
Dropout Voltage (I_O = 1.0 A, T_J = 25°C)	$V_I - V_O$	–	2.0	–	–	2.0	–	Vdc
Output Noise Voltage (T_A = 25°C)	V_n							$\mu V/V_O$
10 Hz ≤ f ≤ 100 kHz		–	10	–	–	10	–	
Output Resistance f = 1.0 kHz	r_O	–	0.9	–	–	0.9	–	mΩ
Short Circuit Current Limit (T_A = 25°C)	I_{SC}							A
V_{in} = 35 Vdc		–	0.2	–	–	0.2	–	
Peak Output Current (T_J = 25°C)	I_{max}	–	2.2	–	–	2.2	–	A
Average Temperature Coefficient of Output Voltage	TCV_O	–	–0.3	–	–	–0.3	–	mV/°C

ELECTRICAL CHARACTERISTICS (V_{in} = 10 V, I_O = 1.0 A, T_J = T_{low} to T_{high} [Note 1], unless otherwise noted.)

Characteristic	Symbol	MC7805AC			Unit
		Min	Typ	Max	
Output Voltage (T_J = 25°C)	V_O	4.9	5.0	5.1	Vdc
Output Voltage	V_O				Vdc
(5.0 mA ≤ I_O ≤ 1.0 A, P_D ≤15 W)		4.8	5.0	5.2	
7.5 Vdc ≤ V_{in} ≤ 20 Vdc					
Line Regulation (Note 2)	Reg_{line}				mV
7.5 Vdc ≤ V_{in} ≤ 25 Vdc, I_O = 500 mA		–	5.0	50	
8.0 Vdc ≤ V_{in} ≤ 12 Vdc		–	1.3	50	
8.0 Vdc ≤ V_{in} ≤ 12 Vdc, T_J = 25°C		–	1.3	25	
7.3 Vdc ≤ V_{in} ≤ 20 Vdc, T_J = 25°C		–	4.5	50	
Load Regulation (Note 2)	Reg_{load}				mV
5.0 mA ≤ I_O ≤ 1.5 A, T_J = 25°C		–	1.3	100	
5.0 mA ≤ I_O ≤ 1.0 A		–	0.8	100	
250 mA ≤ I_O ≤ 750 mA		–	0.15	50	
Quiescent Current	I_B	–	–	6.0	mA
(T_J = 25°C)		–	3.2	6.0	
Quiescent Current Change	ΔI_B				mA
8.0 Vdc ≤ V_{in} ≤ 25 Vdc, I_O = 500 mA		–	–	0.8	
7.5 Vdc ≤ V_{in} ≤ 20 Vdc, T_J = 25°C		–	–	0.8	
5.0 mA ≤ I_O ≤ 1.0 A		–	–	0.5	

NOTES: 1. T_{low} = 0°C for MC78XXAC, C T_{high} = +125°C for MC78XXAC, C, B
= –40°C for MC78XXB

2. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

ELECTRICAL CHARACTERISTICS (continued) (V_{in} = 10 V, I_O = 1.0 A, T_J = T_{low} to T_{high} [Note 1], unless otherwise noted.)

Characteristic	Symbol	MC7805AC			Unit
		Min	Typ	Max	
Ripple Rejection 8.0 Vdc ≤ V_{in} ≤ 18 Vdc, f = 120 Hz, I_O = 500 mA	RR	–	68	–	dB
Dropout Voltage (I_O = 1.0 A, T_J = 25°C)	$V_I – V_O$	–	2.0	–	Vdc
Output Noise Voltage (T_A = 25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	–	10	–	µV/V_O
Output Resistance (f = 1.0 kHz)	r_O	–	0.9	–	mΩ
Short Circuit Current Limit (T_A = 25°C) V_{in} = 35 Vdc	I_{SC}	–	0.2	–	A
Peak Output Current (T_J = 25°C)	I_{max}	–	2.2	–	A
Average Temperature Coefficient of Output Voltage	TCV_O	–	–0.3	–	mV/°C

ELECTRICAL CHARACTERISTICS (V_{in} = 11 V, I_O = 500 mA, T_J = T_{low} to T_{high} [Note 1], unless otherwise noted.)

Characteristic	Symbol	MC7806B			MC7806C			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = 25°C)	V_O	5.75	6.0	6.25	5.75	6.0	6.25	Vdc
Output Voltage (5.0 mA ≤ I_O ≤ 1.0 A, P_D ≤15 W) 8.0 Vdc ≤ V_{in} ≤ 21 Vdc 9.0 Vdc ≤ V_{in} ≤ 21 Vdc	V_O	– 5.7	– 6.0	– 6.3	5.7 –	6.0 –	6.3 –	Vdc
Line Regulation, T_J = 25°C (Note 2) 8.0 Vdc ≤ V_{in} ≤ 25 Vdc 9.0 Vdc ≤ V_{in} ≤ 13 Vdc	Reg_{line}	– –	5.5 1.4	120 60	– –	5.5 1.4	120 60	mV
Load Regulation, T_J = 25°C (Note 2) 5.0 mA ≤ I_O ≤ 1.5 A 250 mA ≤ I_O ≤ 750 mA	Reg_{load}	– –	1.3 0.2	120 60	– –	1.3 0.2	120 60	mV
Quiescent Current (T_J = 25°C)	I_B	–	3.3	8.0	–	3.3	8.0	mA
Quiescent Current Change 8.0 Vdc ≤ V_{in} ≤ 25 Vdc 9.0 Vdc ≤ V_{in} ≤ 25 Vdc 5.0 mA ≤ I_O ≤ 1.0 A	ΔI_B	– – –	– – –	– 1.3 0.5	– – –	– – –	1.3 – 0.5	mA
Ripple Rejection 9.0 Vdc ≤ V_{in} ≤ 19 Vdc, f = 120 Hz	RR	–	65	–	–	65	–	dB
Dropout Voltage (I_O = 1.0 A, T_J = 25°C)	$V_I – V_O$	–	2.0	–	–	2.0	–	Vdc
Output Noise Voltage (T_A = 25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	–	10	–	–	10	–	µV/V_O
Output Resistance f = 1.0 kHz	r_O	–	0.9	–	–	0.9	–	mΩ
Short Circuit Current Limit (T_A = 25°C) V_{in} = 35 Vdc	I_{SC}	–	0.2	–	–	0.2	–	A
Peak Output Current (T_J = 25°C)	I_{max}	–	2.2	–	–	2.2	–	A
Average Temperature Coefficient of Output Voltage	TCV_O	–	–0.3	–	–	–0.3	–	mV/°C

NOTES: 1. T_{low} = 0°C for MC78XXAC, C T_{high} = +125°C for MC78XXAC, C, B
= –40°C for MC78XXB

2. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

ELECTRICAL CHARACTERISTICS (V_{in} = 11 V, I_O = 1.0 A, T_J = T_{low} to T_{high} [Note 1], unless otherwise noted.)

Characteristic	Symbol	MC7806AC			Unit
		Min	Typ	Max	
Output Voltage (T_J = 25°C)	V_O	5.88	6.0	6.12	Vdc
Output Voltage	V_O				Vdc
(5.0 mA ≤ I_O ≤ 1.0 A, P_D ≤15 W) 8.6 Vdc ≤ V_{in} ≤ 21 Vdc		5.76	6.0	6.24	
Line Regulation (Note 2)	Reg_{line}				mV
8.6 Vdc ≤ V_{in} ≤ 25 Vdc, I_O = 500 mA		–	5.0	60	
9.0 Vdc ≤ V_{in} ≤ 13 Vdc		–	1.4	60	
9.0 Vdc ≤ V_{in} ≤ 13 Vdc, T_J = 25°C		–	1.4	30	
8.3 Vdc ≤ V_{in} ≤ 21 Vdc, T_J = 25°C		–	4.5	60	
Load Regulation (Note 2)	Reg_{load}				mV
5.0 mA ≤ I_O ≤ 1.5 A, T_J = 25°C		–	1.3	100	
5.0 mA ≤ I_O ≤ 1.0 A		–	0.9	100	
250 mA ≤ I_O ≤ 750 mA		–	0.2	50	
Quiescent Current	I_B	–	–	6.0	mA
T_J = 25°C		–	3.3	6.0	
Quiescent Current Change	ΔI_B				mA
9.0 Vdc ≤ V_{in} ≤ 25 Vdc, I_O = 500 mA		–	–	0.8	
8.6 Vdc ≤ V_{in} ≤ 21 Vdc, T_J = 25°C		–	–	0.8	
5.0 mA ≤ I_O ≤ 1.0 A		–	–	0.5	
Ripple Rejection	RR				dB
9.0 Vdc ≤ V_{in} ≤ 19 Vdc, f = 120 Hz, I_O = 500 mA		–	65	–	
Dropout Voltage (I_O = 1.0 A, T_J = 25°C)	$V_I - V_O$	–	2.0	–	Vdc
Output Noise Voltage (T_A = 25°C)	V_n				µV/V_O
10 Hz ≤ f ≤ 100 kHz		–	10	–	
Output Resistance (f = 1.0 kHz)	r_O	–	0.9	–	mΩ
Short Circuit Current Limit (T_A = 25°C)	I_{SC}				A
V_{in} = 35 Vdc		–	0.2	–	
Peak Output Current (T_J = 25°C)	I_{max}	–	2.2	–	A
Average Temperature Coefficient of Output Voltage	TCV_O	–	–0.3	–	mV/°C

ELECTRICAL CHARACTERISTICS (V_{in} = 14 V, I_O = 500 mA, T_J = T_{low} to T_{high} [Note 1], unless otherwise noted.)

Characteristic	Symbol	MC7808B			MC7808C			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = 25°C)	V_O	7.7	8.0	8.3	7.7	8.0	8.3	Vdc
Output Voltage	V_O							Vdc
(5.0 mA ≤ I_O ≤ 1.0 A, P_D ≤15 W)								
10.5 Vdc ≤ V_{in} ≤ 23 Vdc		–	–	–	7.6	8.0	8.4	
11.5 Vdc ≤ V_{in} ≤ 23 Vdc		7.6	8.0	8.4	–	–	–	
Line Regulation, T_J = 25°C, (Note 2)	Reg_{line}							mV
10.5 Vdc ≤ V_{in} ≤ 25 Vdc		–	6.0	160	–	6.0	160	
11 Vdc ≤ V_{in} ≤ 17 Vdc		–	1.7	80	–	1.7	80	
Load Regulation, T_J = 25°C (Note 2)	Reg_{load}							mV
5.0 mA ≤ I_O ≤ 1.5 A		–	1.4	160	–	1.4	160	
250 mA ≤ I_O ≤ 750 mA		–	.22	80	–	.22	80	
Quiescent Current (T_J = 25°C)	I_B	–	3.3	8.0	–	3.3	8.0	mA

NOTES: 1. T_{low} = 0°C for MC78XXAC, C T_{high} = +125°C for MC78XXAC, C, B
= –40°C for MC78XXB

2. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

ELECTRICAL CHARACTERISTICS (continued) (V_{in} = 14 V, I_O = 500 mA, T_J = T_{low} to T_{high} [Note 1], unless otherwise noted.)

Characteristic	Symbol	MC7808B			MC7808C			Unit
		Min	Typ	Max	Min	Typ	Max	
Quiescent Current Change	ΔI_B							mA
10.5 Vdc ≤ V_{in} ≤ 25 Vdc		–	–	–	–	–	1.0	
11.5 Vdc ≤ V_{in} ≤ 25 Vdc		–	–	1.0	–	–	–	
5.0 mA ≤ I_O ≤ 1.0 A		–	–	0.5	–	–	0.5	
Ripple Rejection 11.5 Vdc ≤ V_{in} ≤ 18 Vdc, f = 120 Hz	RR	–	62	–	–	62	–	dB
Dropout Voltage (I_O = 1.0 A, T_J = 25°C)	$V_I - V_O$	–	2.0	–	–	2.0	–	Vdc
Output Noise Voltage (T_A = 25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	–	10	–	–	10	–	µV/V_O
Output Resistance f = 1.0 kHz	r_O	–	0.9	–	–	0.9	–	mΩ
Short Circuit Current Limit (T_A = 25°C) V_{in} = 35 Vdc	I_{SC}	–	0.2	–	–	0.2	–	A
Peak Output Current (T_J = 25°C)	I_{max}	–	2.2	–	–	2.2	–	A
Average Temperature Coefficient of Output Voltage	TCV_O	–	–0.4	–	–	–0.4	–	mV/°C

ELECTRICAL CHARACTERISTICS (V_{in} = 14 V, I_O = 1.0 A, T_J = T_{low} to T_{high} [Note 1], unless otherwise noted.)

Characteristic	Symbol	MC7808AC			Unit
		Min	Typ	Max	
Output Voltage (T_J = 25°C)	V_O	7.84	8.0	8.16	Vdc
Output Voltage (5.0 mA ≤ I_O ≤ 1.0 A, P_D ≤15 W) 10.6 Vdc ≤ V_{in} ≤ 23 Vdc	V_O	7.7	8.0	8.3	Vdc
Line Regulation (Note 2)	Reg_{line}				mV
10.6 Vdc ≤ V_{in} ≤ 25 Vdc, I_O = 500 mA		–	6.0	80	
11 Vdc ≤ V_{in} ≤ 17 Vdc		–	1.7	80	
11 Vdc ≤ V_{in} ≤ 17 Vdc, T_J = 25°C		–	1.7	40	
10.4 Vdc ≤ V_{in} ≤ 23 Vdc, T_J = 25°C		–	5.0	80	
Load Regulation (Note 2)	Reg_{load}				mV
5.0 mA ≤ I_O ≤ 1.5 A, T_J = 25°C		–	1.4	100	
5.0 mA ≤ I_O ≤ 1.0 A		–	1.0	100	
250 mA ≤ I_O ≤ 750 mA		–	.22	50	
Quiescent Current	I_B	–	–	6.0	mA
T_J = 25°C		–	3.3	6.0	
Quiescent Current Change	ΔI_B				mA
11 Vdc ≤ V_{in} ≤ 25 Vdc, I_O = 500 mA		–	–	0.8	
10.6 Vdc ≤ V_{in} ≤ 20 Vdc, T_J = 25°C		–	–	0.8	
5.0 mA ≤ I_O ≤ 1.0 A		–	–	0.5	
Ripple Rejection 11.5 Vdc ≤ V_{in} ≤ 21.5 Vdc, f = 120 Hz, I_O = 500 mA	RR	–	62	–	dB
Dropout Voltage (I_O = 1.0 A, T_J = 25°C)	$V_I - V_O$	–	2.0	–	Vdc
Output Noise Voltage (T_A = 25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	–	10	–	µV/V_O
Output Resistance f = 1.0 kHz	r_O	–	0.9	–	mΩ
Short Circuit Current Limit (T_A = 25°C) V_{in} = 35 Vdc	I_{SC}	–	0.2	–	A
Peak Output Current (T_J = 25°C)	I_{max}	–	2.2	–	A
Average Temperature Coefficient of Output Voltage	TCV_O	–	–0.4	–	mV/°C

NOTES: 1. T_{low} = 0°C for MC78XXAC, C T_{high} = +125°C for MC78XXAC, C, B
= –40°C for MC78XXB

2. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

ELECTRICAL CHARACTERISTICS (V_{in} = 15 V, I_O = 500 mA, T_J = T_{low} to T_{high} [Note 1], unless otherwise noted.)

Characteristic	Symbol	MC7809CT			Unit
		Min	Typ	Max	
Output Voltage (T_J = 25°C)	V_O	8.65	9.0	9.35	Vdc
Output Voltage (5.0 mA ≤ I_O ≤ 1.0 A, P_D ≤15 W) 11.5 Vdc ≤ V_{in} ≤ 24 Vdc	V_O	8.55	9.0	9.45	Vdc
Line Regulation, T_J = 25°C (Note 2) 11.5 Vdc ≤ V_{in} ≤ 26 Vdc 11.5 Vdc ≤ V_{in} ≤ 17 Vdc	Reg_{line}	– –	6.2 1.8	50 25	mV
Load Regulation, T_J = 25°C (Note 2) 5.0 mA ≤ I_O ≤ 1.5 A 250 mA ≤ I_O ≤ 750 mA	Reg_{load}	– –	1.5 0.3	50 25	mV
Quiescent Current (T_J = 25°C)	I_B	–	3.4	8.0	mA
Quiescent Current Change 11.5 Vdc ≤ V_{in} ≤ 26 Vdc 5.0 mA ≤ I_O ≤ 1.0 A	ΔI_B	– –	– –	1.0 0.5	mA
Ripple Rejection 11.5 Vdc ≤ V_{in} ≤ 21.5 Vdc, f = 120 Hz	RR	–	61	–	dB
Dropout Voltage (I_O = 1.0 A, T_J = 25°C)	$V_I - V_O$	–	2.0	–	Vdc
Output Noise Voltage (T_A = 25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	–	10	–	$\mu V/V_O$
Output Resistance f = 1.0 kHz	r_O	–	1.0	–	mΩ
Short Circuit Current Limit (T_A = 25°C) V_{in} = 35 Vdc	I_{SC}	–	0.2	–	A
Peak Output Current (T_J = 25°C)	I_{max}	–	2.2	–	A
Average Temperature Coefficient of Output Voltage	TCV_O	–	–0.5	–	mV/°C

ELECTRICAL CHARACTERISTICS (V_{in} = 19 V, I_O = 500 mA, T_J = T_{low} to T_{high} [Note 1], unless otherwise noted.)

Characteristic	Symbol	MC7812B			MC7812C			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = 25°C)	V_O	11.5	12	12.5	11.5	12	12.5	Vdc
Output Voltage (5.0 mA ≤ I_O ≤ 1.0 A, P_D ≤15 W) 14.5 Vdc ≤ V_{in} ≤ 27 Vdc 15.5 Vdc ≤ V_{in} ≤ 27 Vdc	V_O	– 11.4	– 12	– 12.6	11.4 –	12 –	12.6 –	Vdc
Line Regulation, T_J = 25°C (Note 2) 14.5 Vdc ≤ V_{in} ≤ 30 Vdc 16 Vdc ≤ V_{in} ≤ 22 Vdc	Reg_{line}	– –	7.5 2.2	240 120	– –	7.5 2.2	240 120	mV
Load Regulation, T_J = 25°C (Note 2) 5.0 mA ≤ I_O ≤ 1.5 A 250 mA ≤ I_O ≤ 750 mA	Reg_{load}	– –	1.6 1.0	240 120	– –	1.6 1.0	240 120	mV
Quiescent Current (T_J = 25°C)	I_B	–	3.4	8.0	–	3.4	8.0	mA
Quiescent Current Change 14.5 Vdc ≤ V_{in} ≤ 30 Vdc 15 Vdc ≤ V_{in} ≤ 30 Vdc 5.0 mA ≤ I_O ≤ 1.0 A	ΔI_B	– – –	– – –	– 1.0 0.5	– – –	– – –	1.0 – 0.5	mA
Ripple Rejection 15 Vdc ≤ V_{in} ≤ 25 Vdc, f = 120 Hz	RR	–	60	–	–	60	–	dB
Dropout Voltage (I_O = 1.0 A, T_J = 25°C)	$V_I - V_O$	–	2.0	–	–	2.0	–	Vdc

NOTES: 1. T_{low} = 0°C for MC78XXAC, C T_{high} = +125°C for MC78XXAC, C, B
= –40°C for MC78XXB
2. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

ELECTRICAL CHARACTERISTICS (continued) (V_{in} = 19 V, I_O = 500 mA, T_J = T_{low} to T_{high} [Note 1], unless otherwise noted.)

Characteristic	Symbol	MC7812B			MC7812C			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Noise Voltage (T_A = 25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	–	10	–	–	10	–	µV/V_O
Output Resistance f = 1.0 kHz	r_O	–	1.1	–	–	1.1	–	mΩ
Short Circuit Current Limit (T_A = 25°C) V_{in} = 35 Vdc	I_{SC}	–	0.2	–	–	0.2	–	A
Peak Output Current (T_J = 25°C)	I_{max}	–	2.2	–	–	2.2	–	A
Average Temperature Coefficient of Output Voltage	TCV_O	–	–0.8	–	–	–0.8	–	mV/°C

ELECTRICAL CHARACTERISTICS (V_{in} = 19 V, I_O = 10 A, T_J = T_{low} to T_{high} [Note 1], unless otherwise noted.)

Characteristic	Symbol	MC7812AC			Unit
		Min	Typ	Max	
Output Voltage (T_J = 25°C)	V_O	11.75	12	12.25	Vdc
Output Voltage (5.0 mA ≤ I_O ≤ 1.0 A, P_D ≤15 W) 14.8 Vdc ≤ V_{in} ≤ 27 Vdc	V_O	11.5	12	12.5	Vdc
Line Regulation (Note 2)	Reg_{line}				mV
14.8 Vdc ≤ V_{in} ≤ 30 Vdc, I_O = 500 mA		–	7.5	120	
16 Vdc ≤ V_{in} ≤ 22 Vdc		–	2.2	120	
16 Vdc ≤ V_{in} ≤ 22 Vdc, T_J = 25°C		–	2.2	60	
14.5 Vdc ≤ V_{in} ≤ 27 Vdc, T_J = 25°C		–	6.0	120	
Load Regulation (Note 2)	Reg_{load}				mV
5.0 mA ≤ I_O ≤ 1.5 A, T_J = 25°C		–	1.6	100	
5.0 mA ≤ I_O ≤ 1.0 A		–	1.2	100	
250 mA ≤ I_O ≤ 750 mA		–	1.0	50	
Quiescent Current	I_B	–	–	6.0	mA
T_J = 25°C		–	3.4	6.0	
Quiescent Current Change	ΔI_B				mA
15 Vdc ≤ V_{in} ≤ 30 Vdc, I_O = 500 mA		–	–	0.8	
14.8 Vdc ≤ V_{in} ≤ 27 Vdc, T_J = 25°C		–	–	0.8	
5.0 mA ≤ I_O ≤ 1.0 A		–	–	0.5	
Ripple Rejection 15 Vdc ≤ V_{in} ≤ 25 Vdc, f = 120 Hz, I_O = 500 mA	RR	–	60	–	dB
Dropout Voltage (I_O = 1.0 A, T_J = 25°C)	$V_I – V_O$	–	2.0	–	Vdc
Output Noise Voltage (T_A = 25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	–	10	–	µV/V_O
Output Resistance (f = 1.0 kHz)	r_O	–	1.1	–	mΩ
Short Circuit Current Limit (T_A = 25°C) V_{in} = 35 Vdc	I_{SC}	–	0.2	–	A
Peak Output Current (T_J = 25°C)	I_{max}	–	2.2	–	A
Average Temperature Coefficient of Output Voltage	TCV_O	–	–0.8	–	mV/°C

NOTES: 1. T_{low} = 0°C for MC78XXAC, C T_{high} = +125°C for MC78XXAC, C, B
= –40°C for MC78XXB

2. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

ELECTRICAL CHARACTERISTICS (V_{in} = 23 V, I_O = 500 mA, T_J = T_{low} to T_{high} [Note 1], unless otherwise noted.)

Characteristic	Symbol	MC7815B			MC7815C			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = 25°C)	V_O	14.4	15	15.6	14.4	15	15.6	Vdc
Output Voltage	V_O							Vdc
(5.0 mA ≤ I_O ≤ 1.0 A, P_D ≤15 W)								
17.5 Vdc ≤ V_{in} ≤ 30 Vdc		–	–	–	14.25	15	15.75	
18.5 Vdc ≤ V_{in} ≤ 30 Vdc		14.25	15	15.75	–	–	–	
Line Regulation, T_J = 25°C (Note 2)	Reg_{line}							mV
17.5 Vdc ≤ V_{in} ≤ 30 Vdc		–	8.5	300	–	8.5	300	
20 Vdc ≤ V_{in} ≤ 26 Vdc		–	3.0	150	–	3.0	150	
Load Regulation, T_J = 25°C (Note 2)	Reg_{load}							mV
5.0 mA ≤ I_O ≤ 1.5 A		–	1.8	300	–	1.8	300	
250 mA ≤ I_O ≤ 750 mA		–	1.2	150	–	1.2	150	
Quiescent Current (T_J = 25°C)	I_B	–	3.5	8.0	–	3.5	8.0	mA
Quiescent Current Change	ΔI_B							mA
17.5 Vdc ≤ V_{in} ≤ 30 Vdc		–	–	–	–	–	1.0	
18.5 Vdc ≤ V_{in} ≤ 30 Vdc		–	–	1.0	–	–	–	
5.0 mA ≤ I_O ≤ 1.0 A		–	–	0.5	–	–	0.5	
Ripple Rejection	RR							dB
18.5 Vdc ≤ V_{in} ≤ 28.5 Vdc, f = 120 Hz		–	58	–	–	58	–	
Dropout Voltage (I_O = 1.0 A, T_J = 25°C)	$V_I – V_O$	–	2.0	–	–	2.0	–	Vdc
Output Noise Voltage (T_A = 25°C)	V_n							µV/V_O
10 Hz ≤ f ≤ 100 kHz		–	10	–	–	10	–	
Output Resistance f = 1.0 kHz	r_O	–	1.2	–	–	1.2	–	mΩ
Short Circuit Current Limit (T_A = 25°C)	I_{SC}							A
V_{in} = 35 Vdc		–	0.2	–	–	0.2	–	
Peak Output Current (T_J = 25°C)	I_{max}	–	2.2	–	–	2.2	–	A
Average Temperature Coefficient of Output Voltage	TCV_O	–	–1.0	–	–	–1.0	–	mV/°C

ELECTRICAL CHARACTERISTICS (V_{in} = 23 V, I_O = 1.0 A, T_J = T_{low} to T_{high} [Note 1], unless otherwise noted.)

Characteristic	Symbol	MC7815AC			Unit
		Min	Typ	Max	
Output Voltage (T_J = 25°C)	V_O	14.7	15	15.3	Vdc
Output Voltage	V_O				Vdc
(5.0 mA ≤ I_O ≤ 1.0 A, P_D ≤15 W)		14.4	15	15.6	
17.9 Vdc ≤ V_{in} ≤ 30 Vdc					
Line Regulation (Note 2)	Reg_{line}				mV
17.9 Vdc ≤ V_{in} ≤ 30 Vdc, I_O = 500 mA		–	8.5	150	
20 Vdc ≤ V_{in} ≤ 26 Vdc		–	3.0	150	
20 Vdc ≤ V_{in} ≤ 26 Vdc, T_J = 25°C		–	3.0	75	
17.5 Vdc ≤ V_{in} ≤ 30 Vdc, T_J = 25°C		–	7.0	150	
Load Regulation (Note 2)	Reg_{load}				mV
5.0 mA ≤ I_O ≤ 1.5 A, T_J = 25°C		–	1.8	100	
5.0 mA ≤ I_O ≤ 1.0 A		–	1.5	100	
250 mA ≤ I_O ≤ 750 mA		–	1.2	50	
Quiescent Current	I_B	–	–	6.0	mA
T_J = 25°C		–	3.5	6.0	
Quiescent Current Change	ΔI_B				mA
17.5 Vdc ≤ V_{in} ≤ 30 Vdc, I_O = 500 mA		–	–	0.8	
17.5 Vdc ≤ V_{in} ≤ 30 Vdc, T_J = 25°C		–	–	0.8	
5.0 mA ≤ I_O ≤ 1.0 A		–	–	0.5	

NOTES: 1. T_{low} = 0°C for MC78XXAC, C T_{high} = +125°C for MC78XXAC, C, B
= –40°C for MC78XXB

2. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

ELECTRICAL CHARACTERISTICS (continued) (V_{in} = 23 V, I_O = 1.0 A, T_J = T_{low} to T_{high} [Note 1], unless otherwise noted.)

Characteristic	Symbol	MC7815AC			Unit
		Min	Typ	Max	
Ripple Rejection 18.5 Vdc ≤ V_{in} ≤ 28.5 Vdc, f = 120 Hz, I_O = 500 mA	RR	–	58	–	dB
Dropout Voltage (I_O = 1.0 A, T_J = 25°C)	$V_I - V_O$	–	2.0	–	Vdc
Output Noise Voltage (T_A = 25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	–	10	–	µV/V_O
Output Resistance f = 1.0 kHz	r_O	–	1.2	–	mΩ
Short Circuit Current Limit (T_A = 25°C) V_{in} = 35 Vdc	I_{SC}	–	0.2	–	A
Peak Output Current (T_J = 25°C)	I_{max}	–	2.2	–	A
Average Temperature Coefficient of Output Voltage	TCV_O	–	–1.0	–	mV/°C

ELECTRICAL CHARACTERISTICS (V_{in} = 27 V, I_O = 500 mA, T_J = T_{low} to T_{high} [Note 1], unless otherwise noted.)

Characteristic	Symbol	MC7818B			MC7818C			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = 25°C)	V_O	17.3	18	18.7	17.3	18	18.7	Vdc
Output Voltage (5.0 mA ≤ I_O ≤ 1.0 A, P_D ≤15 W)	V_O							Vdc
21 Vdc ≤ V_{in} ≤ 33 Vdc		–	–	–	17.1	18	18.9	
22 Vdc ≤ V_{in} ≤ 33 Vdc		17.1	18	18.9	–	–	–	
Line Regulation, T_J = 25°C (Note 2)	Reg_{line}							mV
21 Vdc ≤ V_{in} ≤ 33 Vdc		–	9.5	360	–	9.5	360	
24 Vdc ≤ V_{in} ≤ 30 Vdc		–	3.2	180	–	3.2	180	
Load Regulation, T_J = 25°C (Note 2)	Reg_{load}							mV
5.0 mA ≤ I_O ≤ 1.5 A		–	2.0	360	–	2.0	360	
250 mA ≤ I_O ≤ 750 mA		–	1.5	180	–	1.5	180	
Quiescent Current (T_J = 25°C)	I_B	–	3.5	8.0	–	3.5	8.0	mA
Quiescent Current Change	ΔI_B							mA
21 Vdc ≤ V_{in} ≤ 33 Vdc		–	–	–	–	–	1.0	
22 Vdc ≤ V_{in} ≤ 33 Vdc		–	–	1.0	–	–	–	
5.0 mA ≤ I_O ≤ 1.0 A		–	–	0.5	–	–	0.5	
Ripple Rejection 22 Vdc ≤ V_{in} ≤ 33 Vdc, f = 120 Hz	RR	–	57	–	–	57	–	dB
Dropout Voltage (I_O = 1.0 A, T_J = 25°C)	$V_I - V_O$	–	2.0	–	–	2.0	–	Vdc
Output Noise Voltage (T_A = 25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	–	10	–	–	10	–	µV/V_O
Output Resistance f = 1.0 kHz	r_O	–	1.3	–	–	1.3	–	mΩ
Short Circuit Current Limit (T_A = 25°C) V_{in} = 35 Vdc	I_{SC}	–	0.2	–	–	0.2	–	A
Peak Output Current (T_J = 25°C)	I_{max}	–	2.2	–	–	2.2	–	A
Average Temperature Coefficient of Output Voltage	TCV_O	–	–1.5	–	–	–1.5	–	mV/°C

NOTES: 1. T_{low} = 0°C for MC78XXAC, C T_{high} = +125°C for MC78XXAC, C, B
= –40°C for MC78XXB

2. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

ELECTRICAL CHARACTERISTICS (V_{in} = 27 V, I_O = 10 A, T_J = T_{low} to T_{high} [Note 1], unless otherwise noted.)

Characteristic	Symbol	MC7818AC			Unit
		Min	Typ	Max	
Output Voltage (T_J = 25°C)	V_O	17.64	18	18.36	Vdc
Output Voltage	V_O				Vdc
(5.0 mA ≤ I_O ≤ 1.0 A, P_D ≤15 W) 21 Vdc ≤ V_{in} ≤ 33 Vdc		17.3	18	18.7	
Line Regulation (Note 2)	Reg_{line}				mV
21 Vdc ≤ V_{in} ≤ 33 Vdc, I_O = 500 mA		–	9.5	180	
24 Vdc ≤ V_{in} ≤ 30 Vdc		–	3.2	180	
24 Vdc ≤ V_{in} ≤ 30 Vdc, T_J = 25°C		–	3.2	90	
20.6 Vdc ≤ V_{in} ≤ 33 Vdc, T_J = 25°C		–	8.0	180	
Load Regulation (Note 2)	Reg_{load}				mV
5.0 mA ≤ I_O ≤ 1.5 A, T_J = 25°C		–	2.0	100	
5.0 mA ≤ I_O ≤ 1.0 A		–	1.8	100	
250 mA ≤ I_O ≤ 750 mA		–	1.5	50	
Quiescent Current	I_B	–	–	6.0	mA
T_J = 25°C		–	3.5	6.0	
Quiescent Current Change	ΔI_B				mA
21 Vdc ≤ V_{in} ≤ 33 Vdc, I_O = 500 mA		–	–	0.8	
21 Vdc ≤ V_{in} ≤ 33 Vdc, T_J = 25°C		–	–	0.8	
5.0 mA ≤ I_O ≤ 1.0 A		–	–	0.5	
Ripple Rejection	RR				dB
22 Vdc ≤ V_{in} ≤ 32 Vdc, f = 120 Hz, I_O = 500 mA		–	57	–	
Dropout Voltage (I_O = 1.0 A, T_J = 25°C)	$V_I – V_O$	–	2.0	–	Vdc
Output Noise Voltage (T_A = 25°C)	V_n				µV/V_O
10 Hz ≤ f ≤ 100 kHz		–	10	–	
Output Resistance f = 1.0 kHz	r_O	–	1.3	–	mΩ
Short Circuit Current Limit (T_A = 25°C)	I_{SC}				A
V_{in} = 35 Vdc		–	0.2	–	
Peak Output Current (T_J = 25°C)	I_{max}	–	2.2	–	A
Average Temperature Coefficient of Output Voltage	TCV_O	–	–1.5	–	mV/°C

ELECTRICAL CHARACTERISTICS (V_{in} = 33 V, I_O = 500 mA, T_J = T_{low} to T_{high} [Note 1], unless otherwise noted.)

Characteristic	Symbol	MC7824B			MC7824C			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = 25°C)	V_O	23	24	25	23	24	25	Vdc
Output Voltage (5.0 mA ≤ I_O ≤ 1.0 A, P_D ≤15 W)	V_O							Vdc
27 Vdc ≤ V_{in} ≤ 38 Vdc		–	–	–	22.8	24	25.2	
28 Vdc ≤ V_{in} ≤ 38 Vdc		22.8	24	25.2	–	–	–	
Line Regulation, T_J = 25°C (Note 2)	Reg_{line}							mV
27 Vdc ≤ V_{in} ≤ 38 Vdc		–	11.5	480	–	11.5	480	
30 Vdc ≤ V_{in} ≤ 36 Vdc		–	3.8	240	–	3.8	240	
Load Regulation, T_J = 25°C (Note 2)	Reg_{load}							mV
5.0 mA ≤ I_O ≤ 1.5 A		–	2.1	480	–	2.1	480	
250 mA ≤ I_O ≤ 750 mA		–	1.8	240	–	1.8	240	
Quiescent Current (T_J = 25°C)	I_B	–	3.6	8.0	–	3.6	8.0	mA

NOTES: 1. T_{low} = 0°C for MC78XXAC, C T_{high} = +125°C for MC78XXAC, C, B
= –40°C for MC78XXB

2. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

ELECTRICAL CHARACTERISTICS (continued) (V_{in} = 33 V, I_O = 500 mA, T_J = T_{low} to T_{high} [Note 1], unless otherwise noted.)

Characteristic	Symbol	MC7824B			MC7824C			Unit
		Min	Typ	Max	Min	Typ	Max	
Quiescent Current Change	ΔI_B							mA
27 Vdc ≤ V_{in} ≤ 38 Vdc		–	–	–	–	–	1.0	
28 Vdc ≤ V_{in} ≤ 38 Vdc		–	–	1.0	–	–	–	
5.0 mA ≤ I_O ≤ 1.0 A		–	–	0.5	–	–	0.5	
Ripple Rejection 28 Vdc ≤ V_{in} ≤ 38 Vdc, f = 120 Hz	RR	–	54	–	–	54	–	dB
Dropout Voltage (I_O = 1.0 A, T_J = 25°C)	$V_I – V_O$	–	2.0	–	–	2.0	–	Vdc
Output Noise Voltage (T_A = 25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	–	10	–	–	10	–	µV/V_O
Output Resistance f = 1.0 kHz	r_O	–	1.4	–	–	1.4	–	mΩ
Short Circuit Current Limit (T_A = 25°C) V_{in} = 35 Vdc	I_{SC}	–	0.2	–	–	0.2	–	A
Peak Output Current (T_J = 25°C)	I_{max}	–	2.2	–	–	2.2	–	A
Average Temperature Coefficient of Output Voltage	TCV_O	–	–2.0	–	–	–2.0	–	mV/°C

ELECTRICAL CHARACTERISTICS (V_{in} = 33 V, I_O = 1.0 A, T_J = T_{low} to T_{high} [Note 1], unless otherwise noted.)

Characteristic	Symbol	MC7824AC			Unit
		Min	Typ	Max	
Output Voltage (T_J = 25°C)	V_O	23.5	24	24.5	Vdc
Output Voltage (5.0 mA ≤ I_O ≤ 1.0 A, P_D ≤15 W) 27.3 Vdc ≤ V_{in} ≤ 38 Vdc	V_O	23	24	25	Vdc
Line Regulation (Note 2)	Reg_{line}				mV
27 Vdc ≤ V_{in} ≤ 38 Vdc, I_O = 500 mA		–	11.5	240	
30 Vdc ≤ V_{in} ≤ 36 Vdc		–	3.8	240	
30 Vdc ≤ V_{in} ≤ 36 Vdc, T_J = 25°C		–	3.8	120	
26.7 Vdc ≤ V_{in} ≤ 38 Vdc, T_J = 25°C		–	10	240	
Load Regulation (Note 2)	Reg_{load}				mV
5.0 mA ≤ I_O ≤ 1.5 A, T_J = 25°C		–	2.1	100	
5.0 mA ≤ I_O ≤ 1.0 A		–	2.0	100	
250 mA ≤ I_O ≤ 750 mA		–	1.8	50	
Quiescent Current	I_B	–	–	6.0	mA
T_J = 25°C		–	3.6	6.0	
Quiescent Current Change	ΔI_B				mA
27.3 Vdc ≤ V_{in} ≤ 38 Vdc, I_O = 500 mA		–	–	0.8	
27.3 Vdc ≤ V_{in} ≤ 38 Vdc, T_J = 25°C		–	–	0.8	
5.0 mA ≤ I_O ≤ 1.0 A		–	–	0.5	
Ripple Rejection 28 Vdc ≤ V_{in} ≤ 38 Vdc, f = 120 Hz, I_O = 500 mA	RR	–	54	–	dB
Dropout Voltage (I_O = 1.0 A, T_J = 25°C)	$V_I – V_O$	–	2.0	–	Vdc
Output Noise Voltage (T_A = 25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	–	10	–	µV/V_O
Output Resistance (f = 1.0 kHz)	r_O	–	1.4	–	mΩ
Short Circuit Current Limit (T_A = 25°C) V_{in} = 35 Vdc	I_{SC}	–	0.2	–	A
Peak Output Current (T_J = 25°C)	I_{max}	–	2.2	–	A
Average Temperature Coefficient of Output Voltage	TCV_O	–	–2.0	–	mV/°C

NOTES: 1. T_{low} = 0°C for MC78XXAC, C T_{high} = +125°C for MC78XXAC, C, B
= –40°C for MC78XXB

2. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

Figure 1. Peak Output Current as a Function of Input/Output Differential Voltage (MC78XXC, AC, B)

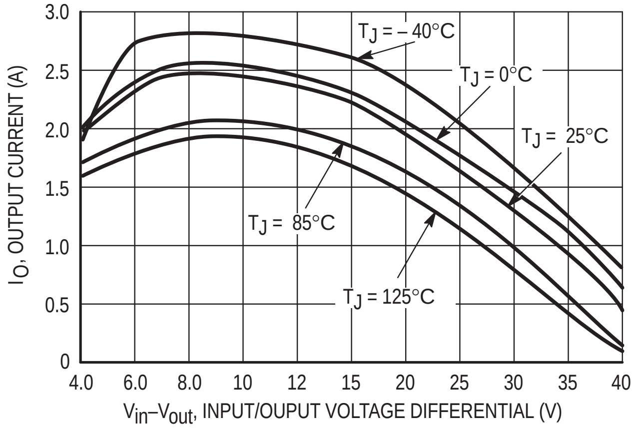


Figure 2. Ripple Rejection as a Function of Output Voltages (MC78XXC, AC)

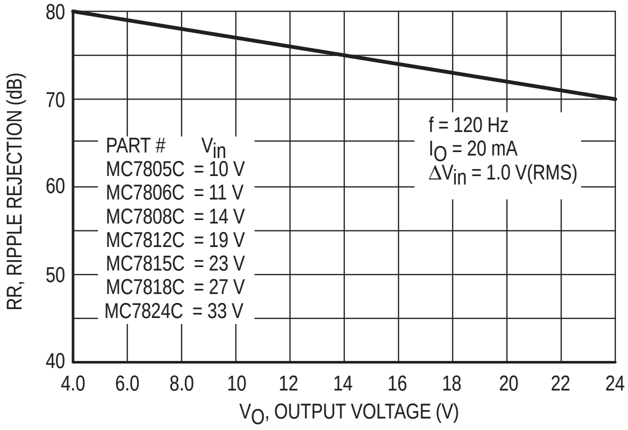


Figure 3. Ripple Rejection as a Function of Frequency (MC78XXC, AC)

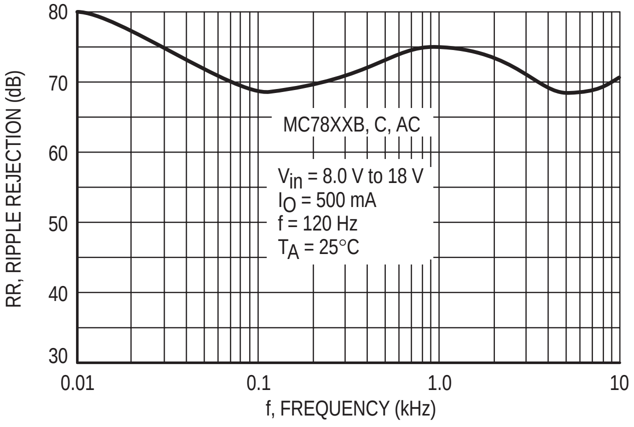


Figure 4. Output Voltage as a Function of Junction Temperature (MC7805C, AC, B)

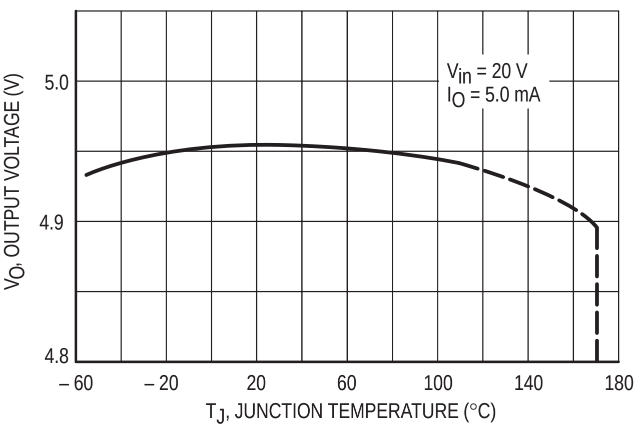


Figure 5. Output Impedance as a Function of Output Voltage (MC78XXC, AC)

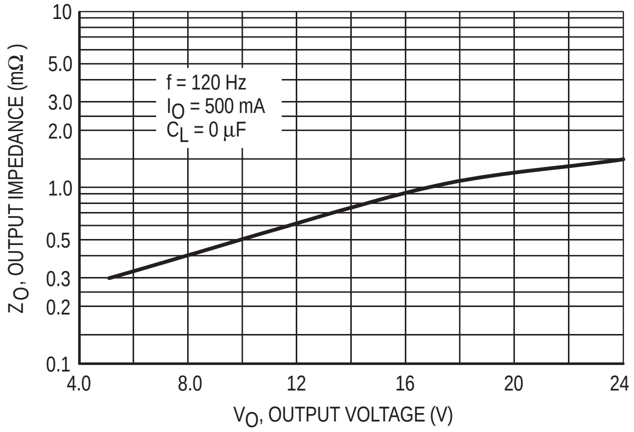
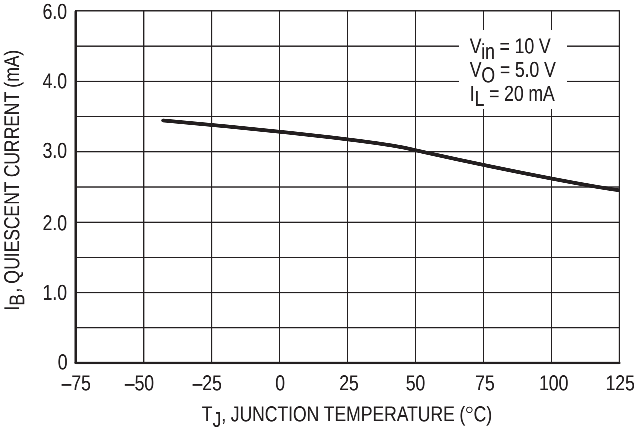


Figure 6. Quiescent Current as a Function of Temperature (MC78XXC, AC, B)



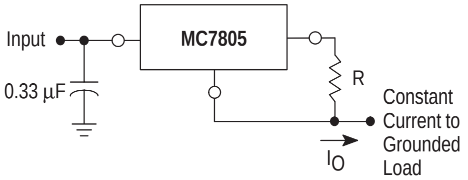
APPLICATIONS INFORMATION

Design Considerations

The MC7800 Series of fixed voltage regulators are designed with Thermal Overload Protection that shuts down the circuit when subjected to an excessive power overload condition, Internal Short Circuit Protection that limits the maximum current the circuit will pass, and Output Transistor Safe–Area Compensation that reduces the output short circuit current as the voltage across the pass transistor is increased.

In many low current applications, compensation capacitors are not required. However, it is recommended that the regulator input be bypassed with a capacitor if the regulator is connected to the power supply filter with long wire lengths, or if the output load capacitance is large. An input bypass capacitor should be selected to provide good high–frequency characteristics to insure stable operation under all load conditions. A 0.33 µF or larger tantalum, mylar, or other capacitor having low internal impedance at high frequencies should be chosen. The bypass capacitor should be mounted with the shortest possible leads directly across the regulators input terminals. Normally good construction techniques should be used to minimize ground loops and lead resistance drops since the regulator has no external sense lead.

Figure 7. Current Regulator



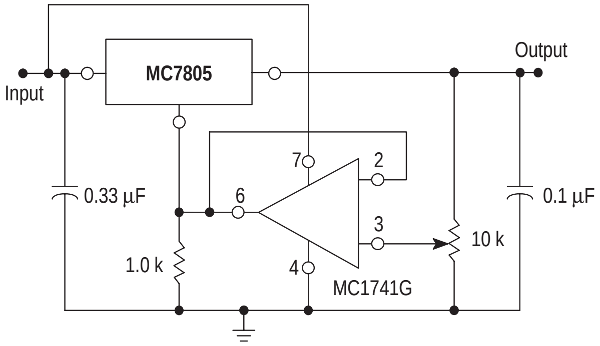
The MC7800 regulators can also be used as a current source when connected as above. In order to minimize dissipation the MC7805C is chosen in this application. Resistor R determines the current as follows:

$$I_O = \frac{5.0\ V}{R} + I_B$$

$I_B \cong$ 3.2 mA over line and load changes.

For example, a 1.0 A current source would require R to be a 5.0 Ω, 10 W resistor and the output voltage compliance would be the input voltage less 7.0 V.

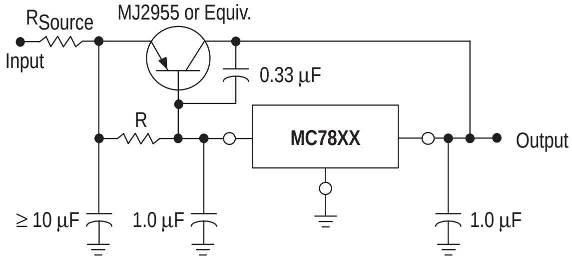
Figure 8. Adjustable Output Regulator



V_O = 7.0 V to 20 V
$V_{IN} = V_O \geq 2.0$ V

The addition of an operational amplifier allows adjustment to higher or intermediate values while retaining regulation characteristics. The minimum voltage obtainable with this arrangement is 2.0 V greater than the regulator voltage.

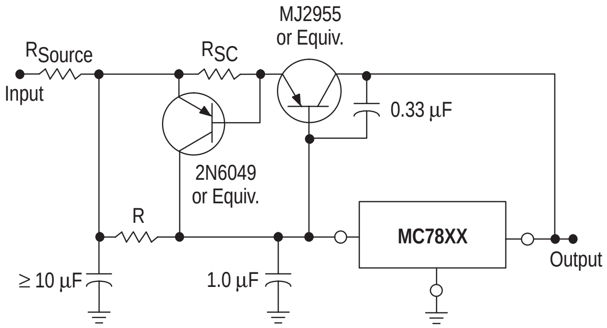
Figure 9. Current Boost Regulator



XX = 2 digits of type number indicating voltage.

The MC7800 series can be current boosted with a PNP transistor. The MJ2955 provides current to 5.0 A. Resistor R in conjunction with the V_{BE} of the PNP determines when the pass transistor begins conducting; this circuit is not short circuit proof. Input/output differential voltage minimum is increased by V_{BE} of the pass transistor.

Figure 10. Short Circuit Protection



XX = 2 digits of type number indicating voltage.

The circuit of Figure 9 can be modified to provide supply protection against short circuits by adding a short circuit sense resistor, R_{SC}, and an additional PNP transistor. The current sensing PNP must be able to handle the short circuit current of the three–terminal regulator. Therefore, a four–ampere plastic power transistor is specified.

Figure 11. Worst Case Power Dissipation versus Ambient Temperature (Case 221A)

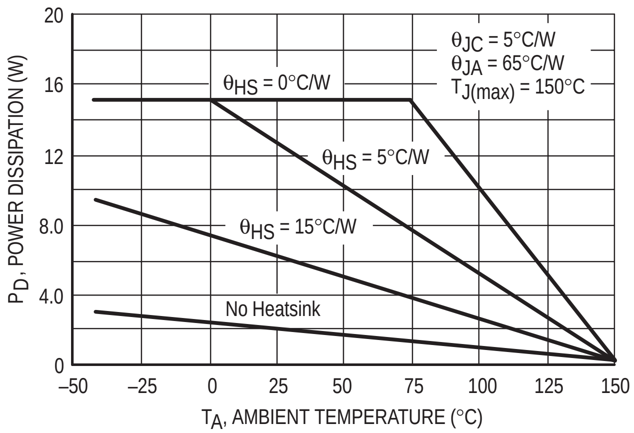


Figure 12. Input Output Differential as a Function of Junction Temperature (MC78XXC, AC, B)

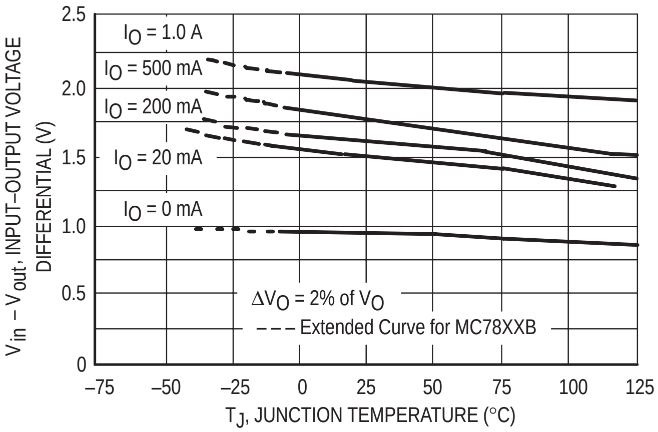
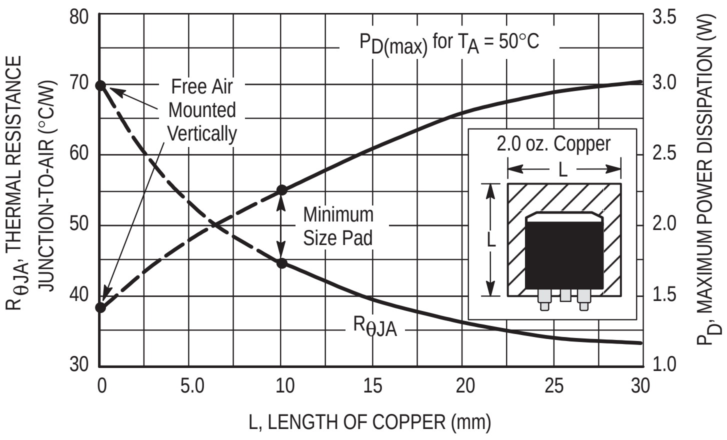


Figure 13. D²PAK Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length



DEFINITIONS

Line Regulation – The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

Load Regulation – The change in output voltage for a change in load current at constant chip temperature.

Maximum Power Dissipation – The maximum total device dissipation for which the regulator will operate within specifications.

Quiescent Current – That part of the input current that is not delivered to the load.

Output Noise Voltage – The rms AC voltage at the output, with constant load and no input ripple, measured over a specified frequency range.

Long Term Stability – Output voltage stability under accelerated life test conditions with the maximum rated voltage listed in the devices' electrical characteristics and maximum power dissipation.

MOTOROLA

MC78L00, A Series

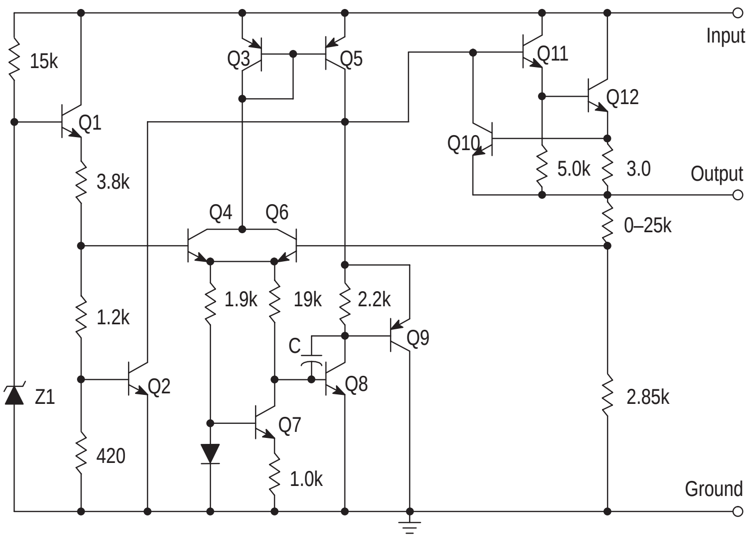
Three-Terminal Low Current Positive Voltage Regulators

The MC78L00, A Series of positive voltage regulators are inexpensive, easy–to–use devices suitable for a multitude of applications that require a regulated supply of up to 100 mA. Like their higher powered MC7800 and MC78M00 Series cousins, these regulators feature internal current limiting and thermal shutdown making them remarkably rugged. No external components are required with the MC78L00 devices in many applications.

These devices offer a substantial performance advantage over the traditional zener diode–resistor combination, as output impedance and quiescent current are substantially reduced.

- Wide Range of Available, Fixed Output Voltages
- Low Cost
- Internal Short Circuit Current Limiting
- Internal Thermal Overload Protection
- No External Components Required
- Complementary Negative Regulators Offered (MC79L00 Series)
- Available in either ±5% (AC) or ±10% (C) Selections

Representative Schematic Diagram

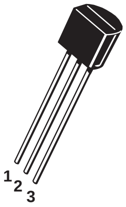


ORDERING INFORMATION

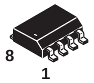
Device	Operating Temperature Range	Package
MC78LXXACD*	T_J = 0° to +125°C	SOP–8
MC78LXXACP		Plastic Power
MC78LXXCP		Plastic Power
MC78LXXABD*	T_J = –40° to +125°C	SOP–8
MC78LXXABP*		Plastic Power

XX indicates nominal voltage
*Available in 5, 8, 9, 12 and 15 V devices.

P SUFFIX
CASE 29



Pin 1. Output
2. GND
3. Input

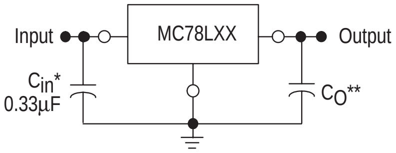


D SUFFIX
PLASTIC PACKAGE
CASE 751
(SOP–8)*

Pin		
	1. V_{out}	5. NC
	2. GND	6. GND
	3. GND	7. GND
	4. NC	8. V_{in}

* SOP–8 is an internally modified SO–8 package. Pins 2, 3, 6, and 7 are electrically common to the die attach flag. This internal lead frame modification decreases package thermal resistance and increases power dissipation capability when appropriately mounted on a printed circuit board. SOP–8 conforms to all external dimensions of the standard SO–8 package.

Standard Application



A common ground is required between the input and the output voltages. The input voltage must remain typically 2.0 V above the output voltage even during the low point on the input ripple voltage.

*C_{in} is required if regulator is located an appreciable distance from power supply filter.

**C_O is not needed for stability; however, it does improve transient response.

DEVICE TYPE/NOMINAL VOLTAGE

10%	5%	Voltage
MC78L05C	MC78L05AC	5.0
MC78L08C	MC78L08AC	8.0
MC78L09C	MC78L09AC	9.0
MC78L12C	MC78L12AC	12
MC78L15C	MC78L15AC	15
MC78L18C	MC78L18AC	18
MC78L24C	MC78L24AC	24

MAXIMUM RATINGS (T_A = +125°C, unless otherwise noted.)

Rating	Symbol	Value	Unit
Input Voltage (2.6 V–8.0 V)	V_I	30	Vdc
(12 V–18 V)		35	
(24 V)		40	
Storage Temperature Range	T_{stg}	–65 to +150	°C
Operating Junction Temperature Range	T_J	0 to +150	°C

ELECTRICAL CHARACTERISTICS (V_I = 10 V, I_O = 40 mA, C_I = 0.33 µF, C_O = 0.1 µF, –40°C < T_J < +125°C (for MC78LXXAB), 0°C < T_J < +125°C (for MC78LXXAC), unless otherwise noted.)

Characteristics	Symbol	MC78L05AC, AB			MC78L05C			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	4.8	5.0	5.2	4.6	5.0	5.4	Vdc
Line Regulation	Reg_{line}							mV
(T_J = +25°C, I_O = 40 mA)								
7.0 Vdc ≤ V_I ≤ 20 Vdc		–	55	150	–	55	200	
8.0 Vdc ≤ V_I ≤ 20 Vdc		–	45	100	–	45	150	
Load Regulation	Reg_{load}							mV
(T_J = +25°C, 1.0 mA ≤ I_O ≤ 100 mA)		–	11	60	–	11	60	
(T_J = +25°C, 1.0 mA ≤ I_O ≤ 40 mA)		–	5.0	30	–	5.0	30	
Output Voltage	V_O							Vdc
(7.0 Vdc ≤ V_I ≤ 20 Vdc, 1.0 mA ≤ I_O ≤ 40 mA)		4.75	–	5.25	4.5	–	5.5	
(V_I = 10 V, 1.0 mA ≤ I_O ≤ 70 mA)		4.75	–	5.25	4.5	–	5.5	
Input Bias Current	I_{IB}							mA
(T_J = +25°C)		–	3.8	6.0	–	3.8	6.0	
(T_J = +125°C)		–	–	5.5	–	–	5.5	
Input Bias Current Change	ΔI_{IB}							mA
(8.0 Vdc ≤ V_I ≤ 20 Vdc)		–	–	1.5	–	–	1.5	
(1.0 mA ≤ I_O ≤ 40 mA)		–	–	0.1	–	–	0.2	
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	–	40	–	–	40	–	µV
Ripple Rejection (I_O = 40 mA, f = 120 Hz, 8.0 Vdc ≤ V_I ≤ 18 V, T_J = +25°C)	RR	41	49	–	40	49	–	dB
Dropout Voltage (T_J = +25°C)	$V_I - V_O$	–	1.7	–	–	1.7	–	Vdc

ELECTRICAL CHARACTERISTICS (V_I = 14 V, I_O = 40 mA, C_I = 0.33 µF, C_O = 0.1 µF, –40°C < T_J < +125°C (for MC78LXXAB), 0°C < T_J < +125°C (for MC78LXXAC), unless otherwise noted.)

Characteristics	Symbol	MC78L08AC, AB			MC78L08C			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	7.7	8.0	8.3	7.36	8.0	8.64	Vdc
Line Regulation	Reg_{line}							mV
(T_J = +25°C, I_O = 40 mA)								
10.5 Vdc ≤ V_I ≤ 23 Vdc		–	20	175	–	20	200	
11 Vdc ≤ V_I ≤ 23 Vdc		–	12	125	–	12	150	
Load Regulation	Reg_{load}							mV
(T_J = +25°C, 1.0 mA ≤ I_O ≤ 100 mA)		–	15	80	–	15	80	
(T_J = +25°C, 1.0 mA ≤ I_O ≤ 40 mA)		–	8.0	40	–	6.0	40	
Output Voltage	V_O							Vdc
(10.5 Vdc ≤ V_I ≤ 23 Vdc, 1.0 mA ≤ I_O ≤ 40 mA)		7.6	–	8.4	7.2	–	8.8	
(V_I = 14 V, 1.0 mA ≤ I_O ≤ 70 mA)		7.6	–	8.4	7.2	–	8.8	
Input Bias Current	I_{IB}							mA
(T_J = +25°C)		–	3.0	6.0	–	3.0	6.0	
(T_J = +125°C)		–	–	5.5	–	–	5.5	
Input Bias Current Change	ΔI_{IB}							mA
(11 Vdc ≤ V_I ≤ 23 Vdc)		–	–	1.5	–	–	1.5	
(1.0 mA ≤ I_O ≤ 40 mA)		–	–	0.1	–	–	0.2	
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	–	60	–	–	52	–	µV
Ripple Rejection (I_O = 40 mA, f = 120 Hz, 12 V ≤ V_I ≤ 23 V, T_J = +25°C)	RR	37	57	–	36	55	–	dB
Dropout Voltage (T_J = +25°C)	$V_I - V_O$	–	1.7	–	–	1.7	–	Vdc

ELECTRICAL CHARACTERISTICS (V_I = 15 V, I_O = 40 mA, C_I = 0.33 µF, C_O = 0.1 µF, –40°C < T_J < +125°C (for MC78LXXAB), 0°C < T_J < +125°C (for MC78LXXAC), unless otherwise noted.)

Characteristics	Symbol	MC78L09AC, AB			MC78L09C			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	8.6	9.0	9.4	8.3	9.0	9.7	Vdc
Line Regulation	Reg_{line}							mV
(T_J = +25°C, I_O = 40 mA)								
11.5 Vdc ≤ V_I ≤ 24 Vdc		–	20	175	–	20	200	
12 Vdc ≤ V_I ≤ 24 Vdc		–	12	125	–	12	150	
Load Regulation	Reg_{load}							mV
(T_J = +25°C, 1.0 mA ≤ I_O ≤ 100 mA)		–	15	90	–	15	90	
(T_J = +25°C, 1.0 mA ≤ I_O ≤ 40 mA)		–	8.0	40	–	6.0	40	
Output Voltage	V_O							Vdc
(11.5 Vdc ≤ V_I ≤ 24 Vdc, 1.0 mA ≤ I_O ≤ 40 mA)		8.5	–	9.5	8.1	–	9.9	
(V_I = 15 V, 1.0 mA ≤ I_O ≤ 70 mA)		8.5	–	9.5	8.1	–	9.9	
Input Bias Current	I_{IB}							mA
(T_J = +25°C)		–	3.0	6.0	–	3.0	6.0	
(T_J = +125°C)		–	–	5.5	–	–	5.5	
Input Bias Current Change	ΔI_{IB}							mA
(11 Vdc ≤ V_I ≤ 23 Vdc)		–	–	1.5	–	–	1.5	
(1.0 mA ≤ I_O ≤ 40 mA)		–	–	0.1	–	–	0.2	
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	–	60	–	–	52	–	µV
Ripple Rejection (I_O = 40 mA, f = 120 Hz, 13 V ≤ V_I ≤ 24 V, T_J = +25°C)	RR	37	57	–	36	55	–	dB
Dropout Voltage (T_J = +25°C)	$V_I – V_O$	–	1.7	–	–	1.7	–	Vdc

ELECTRICAL CHARACTERISTICS (V_I = 19 V, I_O = 40 mA, C_I = 0.33 µF, C_O = 0.1 µF, –40°C < T_J < +125°C (for MC78LXXAB), 0°C < T_J < +125°C (for MC78LXXAC), unless otherwise noted.)

Characteristics	Symbol	MC78L12AC, AB			MC78L12C			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	11.5	12	12.5	11.1	12	12.9	Vdc
Line Regulation	Reg_{line}							mV
(T_J = +25°C, I_O = 40 mA)								
14.5 Vdc ≤ V_I ≤ 27 Vdc		–	120	250	–	120	250	
16 Vdc ≤ V_I ≤ 27 Vdc		–	100	200	–	100	200	
Load Regulation	Reg_{load}							mV
(T_J = +25°C, 1.0 mA ≤ I_O ≤ 100 mA)		–	20	100	–	20	100	
(T_J = +25°C, 1.0 mA ≤ I_O ≤ 40 mA)		–	10	50	–	10	50	
Output Voltage	V_O							Vdc
(14.5 Vdc ≤ V_I ≤ 27 Vdc, 1.0 mA ≤ I_O ≤ 40 mA)		11.4	–	12.6	10.8	–	13.2	
(V_I = 19 V, 1.0 mA ≤ I_O ≤ 70 mA)		11.4	–	12.6	10.8	–	13.2	
Input Bias Current	I_{IB}							mA
(T_J = +25°C)		–	4.2	6.5	–	4.2	6.5	
(T_J = +125°C)		–	–	6.0	–	–	6.0	
Input Bias Current Change	ΔI_{IB}							mA
(16 Vdc ≤ V_I ≤ 27 Vdc)		–	–	1.5	–	–	1.5	
(1.0 mA ≤ I_O ≤ 40 mA)		–	–	0.1	–	–	0.2	
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	–	80	–	–	80	–	µV
Ripple Rejection (I_O = 40 mA, f = 120 Hz, 15 V ≤ V_I ≤ 25 V, T_J = +25°C)	RR	37	42	–	36	42	–	dB
Dropout Voltage (T_J = +25°C)	$V_I – V_O$	–	1.7	–	–	1.7	–	Vdc

ELECTRICAL CHARACTERISTICS (V_I = 23 V, I_O = 40 mA, C_I = 0.33 μF, C_O = 0.1 μF, –40°C < T_J < +125°C (for MC78LXXAB), 0°C < T_J < +125°C (for MC78LXXAC), unless otherwise noted.)

Characteristics	Symbol	MC78L15AC, AB			MC78L15C			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	14.4	15	15.6	13.8	15	16.2	Vdc
Line Regulation	Reg_{line}							mV
(T_J = +25°C, I_O = 40 mA)								
17.5 Vdc ≤ V_I ≤ 30 Vdc		–	130	300	–	130	300	
20 Vdc ≤ V_I ≤ 30 Vdc		–	110	250	–	110	250	
Load Regulation	Reg_{load}							mV
(T_J = +25°C, 1.0 mA ≤ I_O ≤ 100 mA)		–	25	150	–	25	150	
(T_J = +25°C, 1.0 mA ≤ I_O ≤ 40 mA)		–	12	75	–	12	75	
Output Voltage	V_O							Vdc
(17.5 Vdc ≤ V_I ≤ 30 Vdc, 1.0 mA ≤ I_O ≤ 40 mA)		14.25	–	15.75	13.5	–	16.5	
(V_I = 23 V, 1.0 mA ≤ I_O ≤ 70 mA)		14.25	–	15.75	13.5	–	16.5	
Input Bias Current	I_{IB}							mA
(T_J = +25°C)		–	4.4	6.5	–	4.4	6.5	
(T_J = +125°C)		–	–	6.0	–	–	6.0	
Input Bias Current Change	ΔI_{IB}							mA
(20 Vdc ≤ V_I ≤ 30 Vdc)		–	–	1.5	–	–	1.5	
(1.0 mA ≤ I_O ≤ 40 mA)		–	–	0.1	–	–	0.2	
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	–	90	–	–	90	–	μV
Ripple Rejection (I_O = 40 mA, f = 120 Hz, 18.5 V ≤ V_I ≤ 28.5 V, T_J = +25°C)	RR	34	39	–	33	39	–	dB
Dropout Voltage (T_J = +25°C)	$V_I - V_O$	–	1.7	–	–	1.7	–	Vdc

ELECTRICAL CHARACTERISTICS (V_I = 27 V, I_O = 40 mA, C_I = 0.33 μF, C_O = 0.1 μF, 0°C < T_J < +125°C, unless otherwise noted.)

Characteristics	Symbol	MC78L18AC			MC78L18C			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	17.3	18	18.7	16.6	18	19.4	Vdc
Line Regulation	Reg_{line}							mV
(T_J = +25°C, I_O = 40 mA)								
21.4 Vdc ≤ V_I ≤ 33 Vdc					–	32	325	
20.7 Vdc ≤ V_I ≤ 33 Vdc		–	45	325				
22 Vdc ≤ V_I ≤ 33 Vdc					–	27	275	
21 Vdc ≤ V_I ≤ 33 Vdc		–	35	275				
Load Regulation	Reg_{load}							mV
(T_J = +25°C, 1.0 mA ≤ I_O ≤ 100 mA)		–	30	170	–	30	170	
(T_J = +25°C, 1.0 mA ≤ I_O ≤ 40 mA)		–	15	85	–	15	85	
Output Voltage	V_O							Vdc
(21.4 Vdc ≤ V_I ≤ 33 Vdc, 1.0 mA ≤ I_O ≤ 40 mA)					16.2	–	19.8	
(20.7 Vdc ≤ V_I ≤ 33 Vdc, 1.0 mA ≤ I_O ≤ 40 mA)		17.1	–	18.9				
(V_I = 27 V, 1.0 mA ≤ I_O ≤ 70 mA)					16.2	–	19.8	
(V_I = 27 V, 1.0 mA ≤ I_O ≤ 70 mA)		17.1	–	18.9				
Input Bias Current	I_{IB}							mA
(T_J = +25°C)		–	3.1	6.5	–	3.1	6.5	
(T_J = +125°C)		–	–	6.0	–	–	6.0	
Input Bias Current Change	ΔI_{IB}							mA
(22 Vdc ≤ V_I ≤ 33 Vdc)					–	–	1.5	
(21 Vdc ≤ V_I ≤ 33 Vdc)		–	–	1.5				
(1.0 mA ≤ I_O ≤ 40 mA)		–	–	0.1	–	–	0.2	
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	–	150	–	–	150	–	μV
Ripple Rejection (I_O = 40 mA, f = 120 Hz, 23 V ≤ V_I ≤ 33 V, T_J = +25°C)	RR	33	48	–	32	46	–	dB
Dropout Voltage (T_J = +25°C)	$V_I - V_O$	–	1.7	–	–	1.7	–	Vdc

ELECTRICAL CHARACTERISTICS (V_I = 33 V, I_O = 40 mA, C_I = 0.33 µF, C_O = 0.1 µF, 0°C < T_J < +125°C, unless otherwise noted.)

Characteristics	Symbol	MC78L24AC			MC78L24C			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	23	24	25	22.1	24	25.9	Vdc
Line Regulation	Reg_{line}							mV
(T_J = +25°C, I_O = 40 mA)								
27.5 Vdc ≤ V_I ≤ 38 Vdc		–	–	–	–	35	350	
28 Vdc ≤ V_I ≤ 80 Vdc		–	50	300	–	30	300	
27 Vdc ≤ V_I ≤ 38 Vdc		–	60	350	–	–	–	
Load Regulation	Reg_{load}							mV
(T_J = +25°C, 1.0 mA ≤ I_O ≤ 100 mA)		–	40	200	–	40	200	
(T_J = +25°C, 1.0 mA ≤ I_O ≤ 40 mA)		–	20	100	–	20	100	
Output Voltage	V_O							Vdc
(28 Vdc ≤ V_I ≤ 38 Vdc, 1.0 mA ≤ I_O ≤ 40 mA)					21.6	–	26.4	
(27 Vdc ≤ V_I ≤ 38 Vdc, 1.0 mA ≤ I_O ≤ 40 mA)		22.8	–	25.2				
(28 Vdc ≤ V_I = 33 Vdc, 1.0 mA ≤ I_O ≤ 70 mA)					21.6	–	26.4	
(27 Vdc ≤ V_I ≤ 33 Vdc, 1.0 mA ≤ I_O ≤ 70 mA)		22.8	–	25.2				
Input Bias Current	I_{IB}							mA
(T_J = +25°C)		–	3.1	6.5	–	3.1	6.5	
(T_J = +125°C)		–	–	6.0	–	–	6.0	
Input Bias Current Change	ΔI_{IB}							mA
(28 Vdc ≤ V_I ≤ 38 Vdc)		–	–	1.5	–	–	1.5	
(1.0 mA ≤ I_O ≤ 40 mA)		–	–	0.1	–	–	0.2	
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	–	200	–	–	200	–	µV
Ripple Rejection (I_O = 40 mA, f = 120 Hz, 29 V ≤ V_I ≤ 35 V, T_J = +25°C)	RR	31	45	–	30	43	–	dB
Dropout Voltage (T_J = +25°C)	$V_I – V_O$	–	1.7	–	–	1.7	–	Vdc

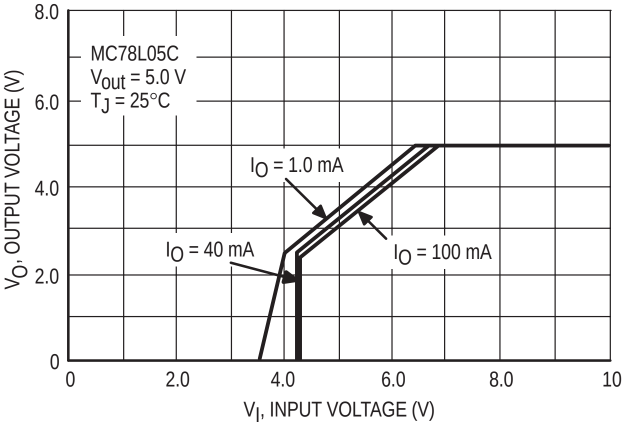


Figure 1. Dropout Characteristics

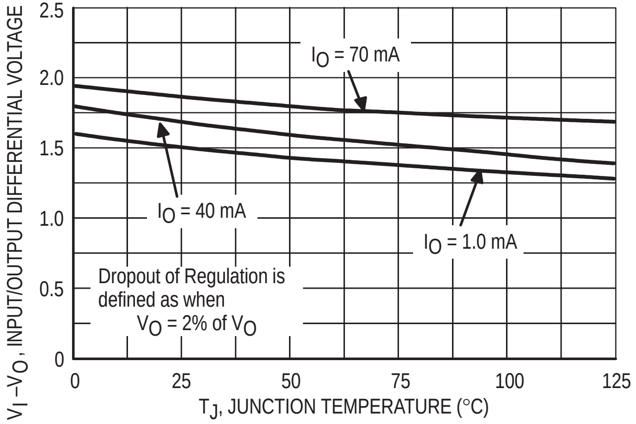


Figure 2. Dropout Voltage versus Junction Temperature

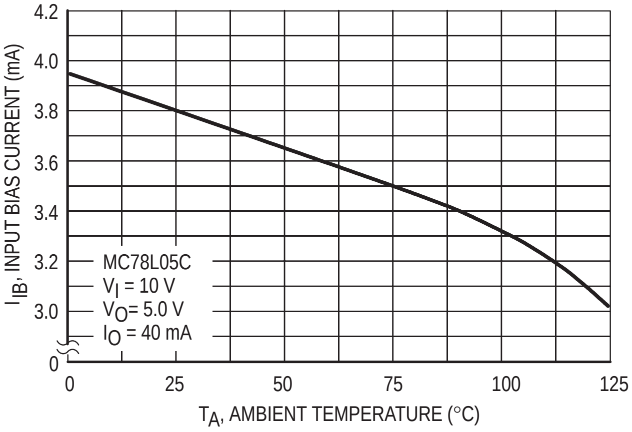


Figure 3. Input Bias Current versus Ambient Temperature

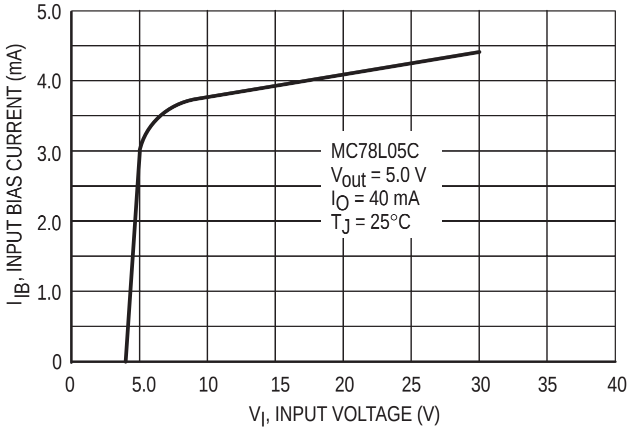


Figure 4. Input Bias Current versus Input Voltage

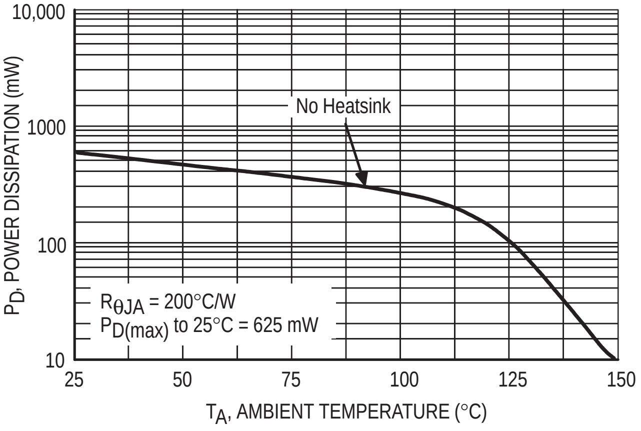


Figure 5. Maximum Average Power Dissipation versus Ambient Temperature – TO–92 Type Package

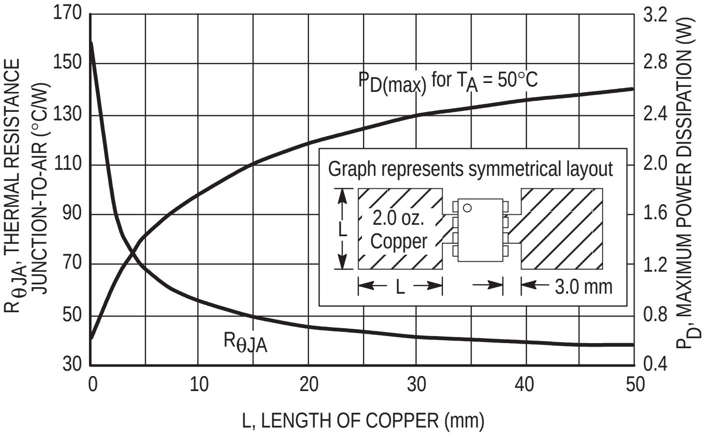


Figure 6. SOP–8 Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length

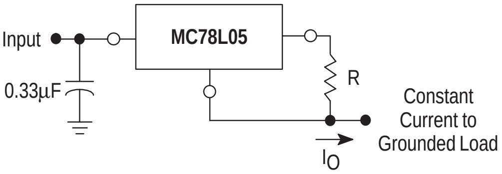
APPLICATIONS INFORMATION

Design Considerations

The MC78L00 Series of fixed voltage regulators are designed with Thermal Overload Protection that shuts down the circuit when subjected to an excessive power overload condition. Internal Short Circuit Protection limits the maximum current the circuit will pass.

In many low current applications, compensation capacitors are not required. However, it is recommended that the regulator input be bypassed with a capacitor if the regulator is connected to the power supply filter with long wire lengths, or if the output load capacitance is large. The input bypass capacitor should be selected to provide good high–frequency characteristics to insure stable operation under all load conditions. A 0.33 µF or larger tantalum, mylar, or other capacitor having low internal impedance at high frequencies should be chosen.The bypass capacitor should be mounted with the shortest possible leads directly across the regulators input terminals. Good construction techniques should be used to minimize ground loops and lead resistance drops since the regulator has no external sense lead. Bypassing the output is also recommended.

Figure 7. Current Regulator



The MC78L00 regulators can also be used as a current source when connected as above. In order to minimize dissipation the MC78L05C is chosen in this application. Resistor R determines the current as follows:

$$I_O = \frac{5.0\ V}{R} + I_B$$

I_{IB} = 3.8 mA over line and load changes

For example, a 100 mA current source would require R to be a 50 Ω, 1/2 W resistor and the output voltage compliance would be the input voltage less 7 V.

Figure 8. ± 15 V Tracking Voltage Regulator

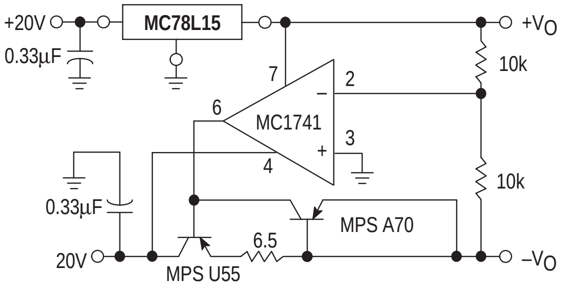
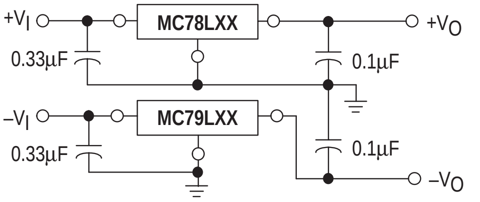


Figure 9. Positive and Negative Regulator



MOTOROLA

MC78M00 Series

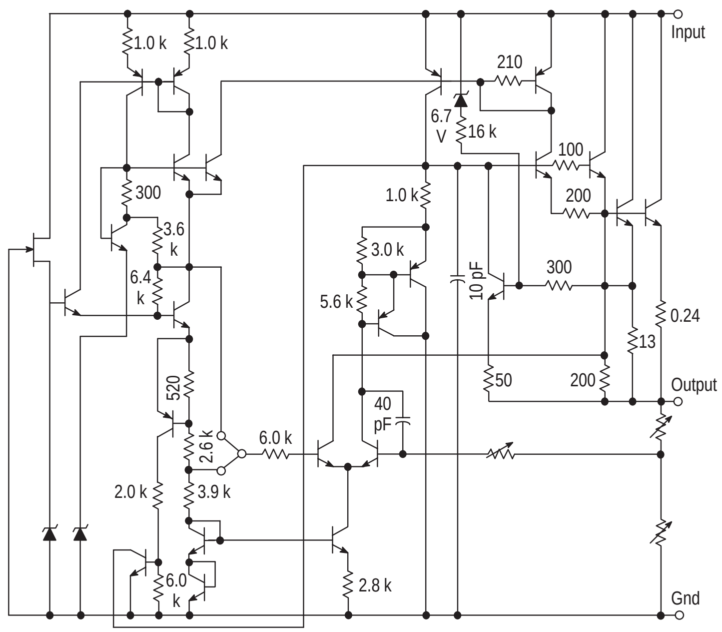
Three-Terminal Medium Current Positive Voltage Regulators

The MC78M00 Series positive voltage regulators are identical to the popular MC7800 Series devices, except that they are specified for only half the output current. Like the MC7800 devices, the MC78M00 three–terminal regulators are intended for local, on–card voltage regulation.

Internal current limiting, thermal shutdown circuitry and safe–area compensation for the internal pass transistor combine to make these devices remarkably rugged under most operating conditions. Maximum output current, with adequate heatsinking is 500 mA.

- No External Components Required
- Internal Thermal Overload Protection
- Internal Short Circuit Current Limiting
- Output Transistor Safe–Area Compensation

Representative Schematic Diagram



This device contains 28 active transistors.

DEVICE TYPE/NOMINAL OUTPUT VOLTAGE

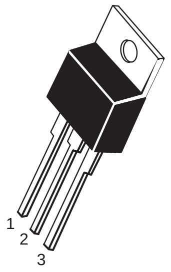
MC78M05B,C	5.0 V	MC78M09B,C	9.0 V	MC78M18B,C	18 V
MC78M06B,C	6.0 V	MC78M12B,C	12 V	MC78M20B,C	20 V
MC78M08B,C	8.0 V	MC78M15B,C	15 V	MC78M24B,C	24 V

THREE–TERMINAL MEDIUM CURRENT POSITIVE FIXED VOLTAGE REGULATORS

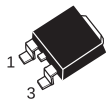
SEMICONDUCTOR TECHNICAL DATA

T SUFFIX
PLASTIC PACKAGE
CASE 221A
(TO–220)

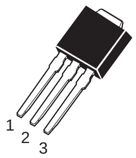
Heatsink surface connected to Pin 2.



Pin 1. Input
2. Ground
3. Output



DT SUFFIX
PLASTIC PACKAGE
CASE 369A
(DPAK)



DT–1 SUFFIX
PLASTIC PACKAGE
CASE 369
(DPAK)

Heatsink surface (shown as terminal 4 in case outline drawing) is connected to Pin 2.

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC78MXXCDT* MC78MXXCDT–1*	T_J = 0° to +125°C	DPAK
MC78MXXCT		TO–220
MC78MXXBT#	T_J = – 40° to +125°C	
MC78MXXBDT#		DPAK

XX Indicates nominal voltage.

* Available in 5, 8, 12 and 15 V devices.

\# Automotive temperature range selections are available with special test conditions and additional tests. Contact your local Motorola sales office for information.

MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted.)

Rating	Symbol	Value	Unit
Input Voltage (5.0 V–18 V)	V_I	35	Vdc
(20 V–24V)		40	
Power Dissipation (Package Limitation)			
Plastic Package, T Suffix			
T_A = 25°C	P_D	Internally Limited	
Thermal Resistance, Junction–to–Air	θ_{JA}	70	°C/W
Thermal Resistance, Junction–to–Case	θ_{JC}	5.0	°C/W
Plastic Package, DT Suffix			
T_A = 25°C	P_D	Internally Limited	
Thermal Resistance, Junction–to–Air	θ_{JA}	92	°C/W
Thermal Resistance, Junction–to–Case	θ_{JC}	5.0	°C/W
Operating Junction Temperature Range	T_J	+150	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

MC78M05B,C ELECTRICAL CHARACTERISTICS (V_I = 10 V, I_O = 350 mA, 0°C < T_J < +125°C, $P_D \leq$ 5.0 W, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = 25°C)	V_O	4.8	5.0	5.2	Vdc
Line Regulation (T_J = 25°C, 7.0 Vdc $\leq V_I \leq$ 25 Vdc, I_O = 200 mA)	Reg_{line}	–	3.0	50	mV
Load Regulation	Reg_{load}				mV
(T_J = 25°C, 5.0 mA $\leq I_O \leq$ 500 mA)		–	20	100	
(T_J = 25°C, 5.0 mA $\leq I_O \leq$ 200 mA)		–	10	50	
Output Voltage (7.0 Vdc $\leq V_I \leq$ 25 Vdc, 5.0 mA $\leq I_O \leq$ 200 mA) (7.0 Vdc $\leq V_I \leq$ 20 Vdc, 5.0 mA $\leq I_O \leq$ 350 mA)	V_O	4.75	–	5.25	Vdc
Input Bias Current (T_J = 25°C)	I_{IB}	–	3.2	6.0	mA
Quiescent Current Change	ΔI_{IB}				mA
(8.0 Vdc $\leq V_I \leq$ 25 Vdc, I_O = 200 mA)		–	–	0.8	
(5.0 mA $\leq I_O \leq$ 350 mA)		–	–	0.5	
Output Noise Voltage (T_A = 25°C, 10 Hz $\leq f \leq$ 100 kHz)	V_n	–	40	–	µV
Ripple Rejection	RR				dB
(I_O = 100 mA, f = 120 Hz, 8.0 V $\leq V_I \leq$ 18 V)		62	–	–	
(I_O = 300 mA, f = 120 Hz, 8.0 $\leq V_I \leq$ 18 V, T_J = 25°C)		62	80	–	
Dropout Voltage (T_J = 25°C)	$V_I–V_O$	–	2.0	–	Vdc
Short Circuit Current Limit (T_J = 25°C, V_I = 35 V)	I_{OS}	–	50	–	mA
Average Temperature Coefficient of Output Voltage (I_O = 5.0 mA)	$\Delta V_O/\Delta T$	–	±0.2	–	mV/°C
Peak Output Current (T_J = 25°C)	I_O	–	700	–	mA

MC78M06B,C ELECTRICAL CHARACTERISTICS (V_I = 11 V, I_O = 350 mA, 0°C < T_J < +125°C, P_D ≤ 5.0 W, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = 25°C)	V_O	5.75	6.0	6.25	Vdc
Line Regulation (T_J = 25°C, 8.0 Vdc ≤ V_I ≤ 25 Vdc, I_O = 200 mA)	Reg_{line}	–	5.0	50	mV
Load Regulation (T_J = 25°C, 5.0 mA ≤ I_O ≤ 500 mA) (T_J = 25°C, 5.0 mA ≤ I_O ≤ 200 mA)	Reg_{load}	 – –	 20 10	 120 60	mV
Output Voltage (8.0 Vdc ≤ V_I ≤ 25 Vdc, 5.0 mA ≤ I_O ≤ 200 mA) (8.0 Vdc ≤ V_I ≤ 21 Vdc, 5.0 mA ≤ I_O ≤ 350 mA)	V_O	5.7	–	6.3	Vdc
Input Bias Current (T_J = 25°C)	I_{IB}	–	3.2	6.0	mA
Quiescent Current Change (9.0 Vdc ≤ V_I ≤ 25 Vdc, I_O = 200 mA) (5.0 mA ≤ I_O ≤ 350 mA)	ΔI_{IB}	 – –	 – –	 0.8 0.5	mA
Output Noise Voltage (T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	–	45	–	µV
Ripple Rejection (I_O = 100 mA, f = 120 Hz, 9.0 V ≤ V_I ≤ 19 V) (I_O = 300 mA, f = 120 Hz, 9.0 V ≤ V_I ≤ 19 V, T_J = 25°C)	RR	 59 59	 – 80	 – –	dB
Dropout Voltage (T_J = 25°C)	$V_I – V_O$	–	2.0	–	Vdc
Short Circuit Current Limit (T_J = 25°C, V_I = 35 V)	I_{OS}	–	50	–	mA
Average Temperature Coefficient of Output Voltage (I_O = 5.0 mA)	$\Delta V_O/\Delta T$	–	±0.2	–	mV/°C
Peak Output Current (T_J = 25°C)	I_O	–	700	–	mA

MC78M08B,C ELECTRICAL CHARACTERISTICS (V_I = 14 V, I_O = 350 mA, 0°C < T_J < +125°C, P_D ≤ 5.0 W, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = 25°C)	V_O	7.7	8.0	8.3	Vdc
Line Regulation (T_J = 25°C, 10.5 Vdc ≤ V_I ≤ 25 Vdc, I_O = 200 mA)	Reg_{line}	–	6.0	50	mV
Load Regulation (T_J = 25°C, 5.0 mA ≤ I_O ≤ 500 mA) (T_J = 25°C, 5.0 mA ≤ I_O ≤ 200 mA)	Reg_{load}	 – –	 25 10	 160 80	mV
Output Voltage (10.5 Vdc ≤ V_I ≤ 25 Vdc, 5.0 mA ≤ I_O ≤ 200 mA) (10.5 Vdc ≤ V_I ≤ 23 Vdc, 5.0 mA ≤ I_O ≤ 350 mA)	V_O	7.6	–	8.4	Vdc
Input Bias Current (T_J = 25°C)	I_{IB}	–	3.2	6.0	mA
Quiescent Current Change (10.5 Vdc ≤ V_I ≤ 25 Vdc, I_O = 200 mA) (5.0 mA ≤ I_O ≤ 350 mA)	ΔI_{IB}	 – –	 – –	 0.8 0.5	mA
Output Noise Voltage (T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	–	52	–	µV
Ripple Rejection (I_O = 100 mA, f = 120 Hz, 11.5 V ≤V_I ≤ 21.5 V) (I_O = 300 mA, f = 120 Hz, 11.5 V ≤V_I ≤ 21.5 V, T_J = 25°C)	RR	 56 56	 – 80	 – –	dB
Dropout Voltage (T_J = 25°C)	$V_I–V_O$	–	2.0	–	Vdc
Short Circuit Current Limit (T_J = 25°C, V_I = 35 V)	I_{OS}	–	50	–	mA
Average Temperature Coefficient of Output Voltage (I_O = 5.0 mA)	$\Delta V_O/\Delta T$	–	±0.2	–	mV/°C
Peak Output Current (T_J = 25°C)	I_O	–	700	–	mA

MC78M09B,C ELECTRICAL CHARACTERISTICS (V_I = 15 V, I_O = 350 mA, 0°C < T_J < +125°C, $P_D \le 5.0$ W, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = 25°C)	V_O	8.64	9.0	9.45	Vdc
Line Regulation (T_J = 25°C, 11.5 Vdc ≤ V_I ≤ 25 Vdc, I_O = 200 mA)	Reg_{line}	–	6.0	50	mV
Load Regulation (T_J = 25°C, 5.0 mA ≤ I_O ≤ 500 mA) (T_J = 25°C, 5.0 mA ≤ I_O ≤ 200 mA)	Reg_{load}	 – –	 25 10	 180 90	mV
Output Voltage (11.5 Vdc ≤ V_I ≤ 25 Vdc, 5.0 mA ≤ I_O ≤ 200 mA) (11.5 Vdc ≤ V_I ≤ 23 Vdc, 5.0 mA ≤ I_O ≤ 350 mA)	V_O	8.55	–	9.45	Vdc
Input Bias Current (T_J = 25°C)	I_{IB}	–	3.2	6.0	mA
Quiescent Current Change (11.5 Vdc ≤ V_I ≤ 25 Vdc, I_O = 200 mA) (5.0 mA ≤ I_O ≤ 350 mA)	ΔI_{IB}	 – –	 – –	 0.8 0.5	mA
Output Noise Voltage (T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	–	52	–	µV
Ripple Rejection (I_O = 100 mA, f = 120 Hz, 12.5 V ≤V_I ≤ 22.5 V) (I_O = 300 mA, f = 120 Hz, 12.5 V ≤V_I ≤ 22.5 V, T_J = 25°C)	RR	 56 56	 – 80	 – –	dB
Dropout Voltage (T_J = 25°C)	$V_I–V_O$	–	2.0	–	Vdc
Short Circuit Current Limit (T_J = 25°C, V_I = 35 V)	I_{OS}	–	50	–	mA
Average Temperature Coefficient of Output Voltage (I_O = 5.0 mA)	$\Delta V_O/\Delta T$	–	±0.2	–	mV/°C
Peak Output Current (T_J = 25°C)	I_O	–	700	–	mA

MC78M12B,C ELECTRICAL CHARACTERISTICS (V_I = 19 V, I_O = 350 mA, 0°C < T_J < +125°C, $P_D \le 5.0$ W, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = 25°C)	V_O	11.5	12	12.5	Vdc
Line Regulation (T_J = 25°C, 14.5 Vdc ≤ V_I ≤ 30 Vdc, I_O = 200 mA)	Reg_{line}	–	8.0	50	mV
Load Regulation (T_J = 25°C, 5.0 mA ≤ I_O ≤ 500 mA) (T_J = 25°C, 5.0 mA ≤ I_O ≤ 200 mA)	Reg_{load}	 – –	 25 10	 240 120	mV
Output Voltage (14.5 Vdc ≤ V_I ≤ 27 Vdc, 5.0 mA ≤ I_O ≤ 350 mA)	V_O	11.4	–	12.6	Vdc
Input Bias Current (T_J = 25°C)	I_{IB}	–	3.2	6.0	mA
Quiescent Current Change (14.5 Vdc ≤ V_I ≤ 30 Vdc, I_O = 200 mA) (5.0 mA ≤ I_O ≤ 350 mA)	ΔI_{IB}	 – –	 – –	 0.8 0.5	mA
Output Noise Voltage (T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	–	75	–	µV
Ripple Rejection (I_O = 100 mA, f = 120 Hz, 15 V ≤V_I ≤ 25 V) (I_O = 300 mA, f = 120 Hz, 15 V ≤V_I ≤ 25 V, T_J = 25°C)	RR	 55 55	 – 80	 – –	dB
Dropout Voltage (T_J = 25°C)	$V_I–V_O$	–	2.0	–	Vdc
Short Circuit Current Limit (T_J = 25°C, V_I = 35 V)	I_{OS}	–	50	–	mA
Average Temperature Coefficient of Output Voltage (I_O = 5.0 mA)	$\Delta V_O/\Delta T$	–	±0.3	–	mV/°C
Peak Output Current (T_J = 25°C)	I_O	–	700	–	mA

MC78M15B,C ELECTRICAL CHARACTERISTICS (V_I = 23 V, I_O = 350 mA, 0°C < T_J < +125°C, $P_D \le 5.0$ W, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = 25°C)	V_O	14.4	15	15.6	Vdc
Input Regulation (T_J = 25°C, 17.5 Vdc ≤ V_I ≤ 30 Vdc, I_O = 200 mA)	Reg_{line}	–	10	50	mV
Load Regulation	Reg_{load}				mV
(T_J = 25°C, 5.0 mA ≤ I_O ≤ 500 mA)		–	25	300	
(T_J = 25°C, 5.0 mA ≤ I_O ≤ 200 mA)		–	10	150	
Output Voltage (17.5 Vdc ≤ V_I ≤ 30 Vdc, 5.0 mA ≤ I_O ≤ 350 mA)	V_O	14.25	–	15.75	Vdc
Input Bias Current (T_J = 25°C)	I_{IB}	–	3.2	6.0	mA
Quiescent Current Change	ΔI_{IB}				mA
(17.5 Vdc ≤ V_I ≤ 30 Vdc, I_O = 200 mA)		–	–	0.8	
(5.0 mA ≤ I_O ≤ 350 mA)		–	–	0.5	
Output Noise Voltage (T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	–	90	–	µV
Ripple Rejection	RR				dB
(I_O = 100 mA, f = 120 Hz, 18.5 V ≤ V_I ≤ 28.5 V)		54	–	–	
(I_O = 300 mA, f = 120 Hz, 18.5 V ≤ V_I ≤ 28.5 V, T_J = 25°C)		54	70	–	
Dropout Voltage (T_J = 25°C)	$V_I–V_O$	–	2.0	–	Vdc
Short Circuit Current Limit (T_J = 25°C, V_I = 35 V)	I_{OS}	–	50	–	mA
Average Temperature Coefficient of Output Voltage (I_O = 5.0 mA)	$\Delta V_O/\Delta T$	–	±0.3	–	mV/°C
Peak Output Current (T_J = 25°C)	I_O	–	700	–	mA

MC78M18B,C ELECTRICAL CHARACTERISTICS (V_I = 27 V, I_O = 350 mA, 0°C < T_J < +125°C, $P_D \le 5.0$ W, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = 25°C)	V_O	17.3	18	18.7	Vdc
Line Regulation (T_J = 25°C, 21 Vdc ≤ V_I ≤ 33 Vdc, I_O = 200 mA)	Reg_{line}	–	10	50	mV
Load Regulation	Reg_{load}				mV
(T_J = 25°C, 5.0 mA ≤ I_O ≤ 500 mA)		–	30	360	
(T_J = 25°C, 5.0 mA ≤ I_O ≤ 200 mA)		–	10	180	
Output Voltage (21 Vdc ≤ V_I ≤ 33 Vdc, 5.0 mA ≤ I_O ≤ 350 mA)	V_O	17.1	–	18.9	Vdc
Input Bias Current (T_J = 25°C)	I_{IB}	–	3.2	6.5	mA
Quiescent Current Change	ΔI_{IB}				mA
(21 Vdc ≤ V_I ≤ 33 Vdc, I_O = 200 mA)		–	–	0.8	
(5.0 mA ≤ I_O ≤ 350 mA)		–	–	0.5	
Output Noise Voltage (T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	–	100	–	µV
Ripple Rejection	RR				dB
(I_O = 100 mA, f = 120 Hz, 22 V ≤ V_I ≤ 32 V)		53	–	–	
(I_O = 300 mA, f = 120 Hz, 22 V ≤ V_I ≤ 32 V, T_J = 25°C)		53	70	–	
Dropout Voltage (T_J = 25°C)	$V_I–V_O$	–	2.0	–	Vdc
Short Circuit Current Limit (T_J = 25°C, V_I = 35 V)	I_{OS}	–	50	–	mA
Average Temperature Coefficient of Output Voltage (I_O = 5.0 mA)	$\Delta V_O/\Delta T$	–	±0.3	–	mV/°C
Peak Output Current (T_J = 25°C)	I_O	–	700	–	mA

MC78M20B,C ELECTRICAL CHARACTERISTICS (V_I = 29 V, I_O = 350 mA, 0°C < T_J < +125°C, $P_D \le$ 5.0 W, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = 25°C)	V_O	19.2	20	20.8	Vdc
Line Regulation (T_J = 25°C, 23 Vdc $\le V_I \le$ 35 Vdc, I_O = 200 mA)	Reg_{line}	–	10	50	mV
Load Regulation	Reg_{load}				mV
(T_J = 25°C, 5.0 mA $\le I_O \le$ 500 mA)		–	30	400	
(T_J = 25°C, 5.0 mA $\le I_O \le$ 200 mA)		–	10	200	
Output Voltage (23 Vdc $\le V_I \le$ 35 Vdc, 5.0 mA $\le I_O \le$ 350 mA)	V_O	19	–	21	Vdc
Input Bias Current (T_J = 25°C)	I_{IB}	–	3.2	6.5	mA
Quiescent Current Change	ΔI_{IB}				mA
(23 Vdc $\le V_I \le$ 35 Vdc, I_O = 200 mA)		–	–	0.8	
(5.0 mA $\le I_O \le$ 350 mA)		–	–	0.5	
Output Noise Voltage (T_A = 25°C, 10 Hz $\le$ f $\le$ 100 kHz)	V_n	–	110	–	µV
Ripple Rejection	RR				dB
(I_O = 100 mA, f = 120 Hz, 24 V $\le V_I \le$ 34 V)		52	–	–	
(I_O = 300 mA, f = 120 Hz, 24 V $\le V_I \le$ 34 V, T_J = 25°C)		52	70	–	
Dropout Voltage (T_J = 25°C)	$V_I–V_O$	–	2.0	–	Vdc
Short Circuit Current Limit (T_J = 25°C, V_I = 35 V)	I_{OS}	–	50	–	mA
Average Temperature Coefficient of Output Voltage (I_O = 5.0 mA)	$\Delta V_O/\Delta T$	–	±0.5	–	mV/°C
Peak Output Current (T_J = 25°C)	I_O	–	700	–	mA

MC78M24B,C ELECTRICAL CHARACTERISTICS (V_I = 33 V, I_O = 350 mA, 0°C < T_J < +125°C, $P_D \le$ 5.0 W, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = 25°C)	V_O	23	24	25	Vdc
Line Regulation (T_J = 25°C, 27 Vdc $\le V_I \le$ 38 Vdc, I_O = 200 mA)	Reg_{line}	–	10	50	mV
Load Regulation	Reg_{load}				mV
(T_J = 25°C, 5.0 mA $\le I_O \le$ 500 mA)		–	30	480	
(T_J = 25°C, 5.0 mA $\le I_O \le$ 200 mA)		–	10	240	
Output Voltage (27 Vdc $\le V_I \le$ 38 Vdc, 5.0 mA $\le I_O \le$ 350 mA)	V_O	22.8	–	25.2	Vdc
Input Bias Current (T_J = 25°C)	I_{IB}	–	3.2	7.0	mA
Quiescent Current Change	ΔI_{IB}				mA
(27 Vdc $\le V_I \le$ 38 Vdc, I_O = 200 mA)		–	–	0.8	
(5.0 mA $\le I_O \le$ 350 mA)		–	–	0.5	
Output Noise Voltage (T_A = 25°C, 10 Hz $\le$ f $\le$ 100 kHz)	V_n	–	170	–	µV
Ripple Rejection	RR				dB
(I_O = 100 mA, f = 120 Hz, 28 V $\le V_I \le$ 38 V)		50	–	–	
(I_O = 300 mA, f = 120 Hz, 28 V $\le V_I \le$ 38 V, T_J = 25°C)		50	70	–	
Dropout Voltage (T_J = 25°C)	$V_I–V_O$	–	2.0	–	Vdc
Short Circuit Current Limit (T_J = 25°C)	I_{OS}	–	50	–	mA
Average Temperature Coefficient of Output Voltage (I_O = 5.0 mA)	$\Delta V_O/\Delta T$	–	±0.5	–	mV/°C
Peak Output Current (T_J = 25°C)	I_O	–	700	–	mA

DEFINITIONS

Line Regulation – The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

Load Regulation – The change in output voltage for a change in load current at constant chip temperature.

Maximum Power Dissipation – The maximum total device dissipation for which the regulator will operate within specifications.

Input Bias Current – That part of the input current that is not delivered to the load.

Output Noise Voltage – The rms AC voltage at the output, with constant load and no input ripple, measured over a specified frequency range.

Long Term Stability – Output voltage stability under accelerated life test conditions with the maximum rated voltage listed in the devices' electrical characteristics and maximum power dissipation.

Figure 1. DPAK Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length

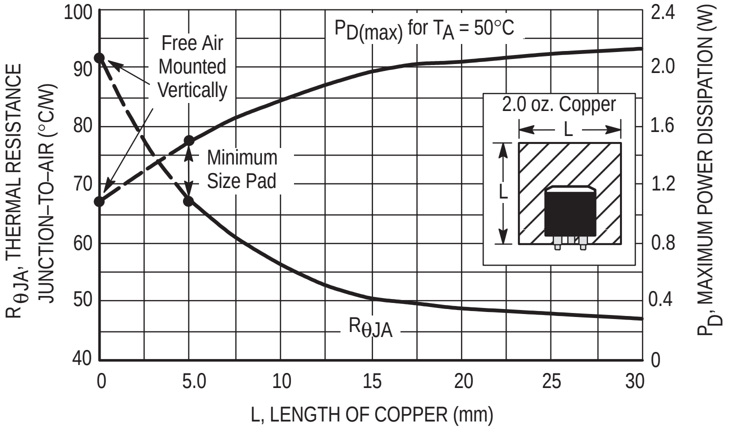


Figure 2. Worst Case Power Dissipation versus Ambient Temperature (TO–220)

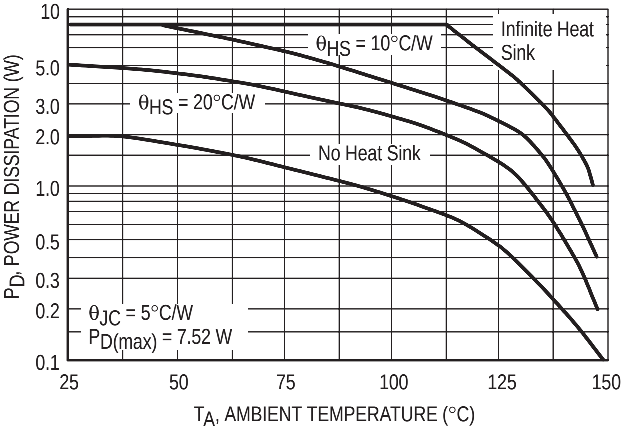


Figure 3. Peak Output Current versus Dropout Voltage

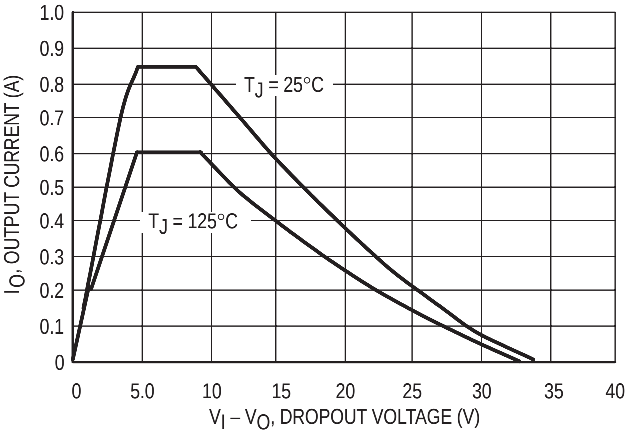


Figure 4. Dropout Voltage versus Junction Temperature

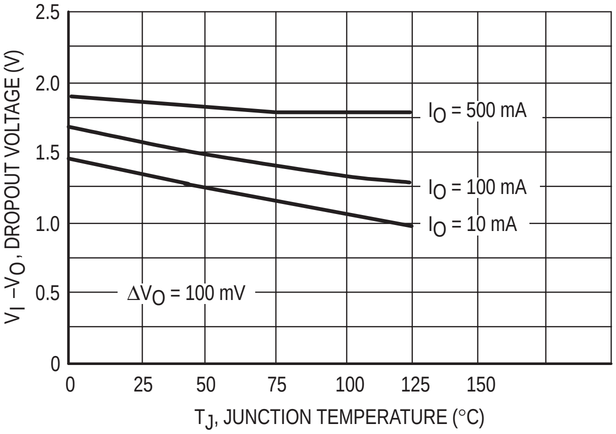


Figure 5. Ripple Rejection versus Frequency

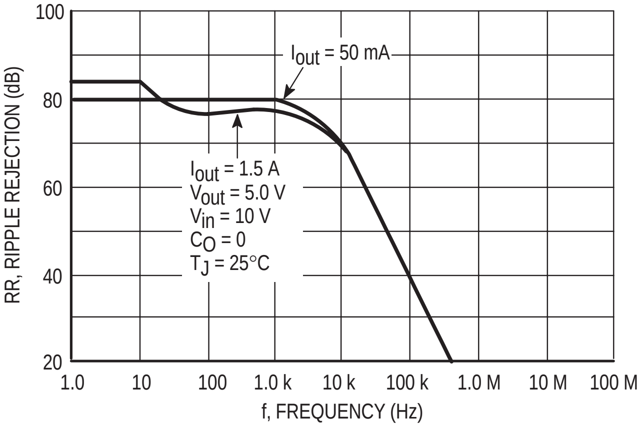


Figure 6. Ripple Rejection versus Output Current

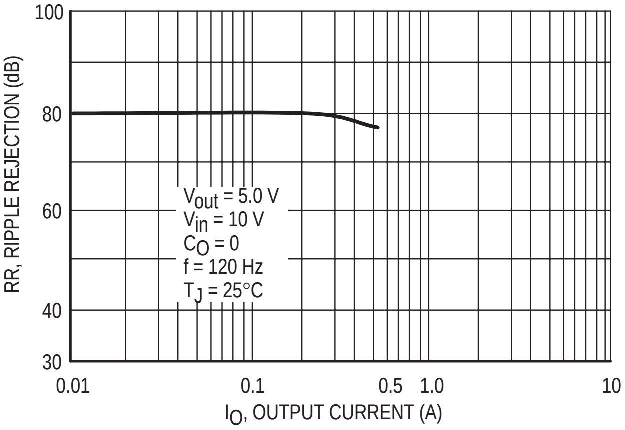


Figure 7. Bias Current versus Input Voltage

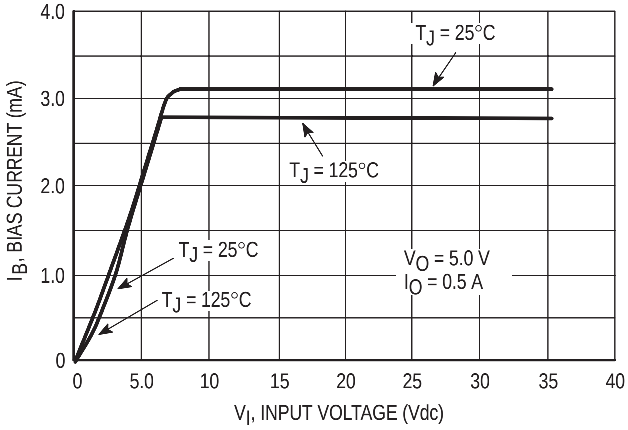
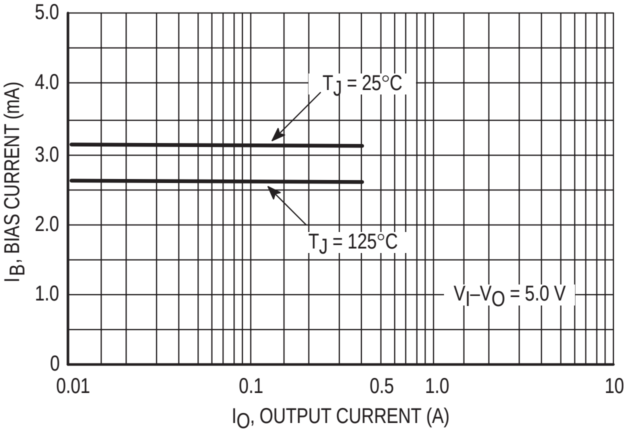


Figure 8. Bias Current versus Output Current



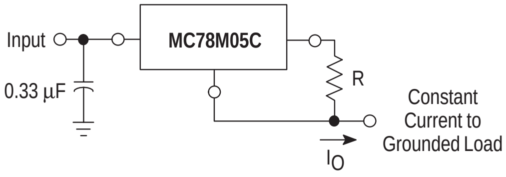
APPLICATIONS INFORMATION

Design Considerations

The MC78M00 Series of fixed voltage regulators are designed with Thermal Overload Protection that shuts down the circuit when subjected to an excessive power overload condition, Internal Short Circuit Protection that limits the maximum current the circuit will pass, and Output Transistor Safe–Area Compensation that reduces the output short circuit current as the voltage across the pass transistor is increased.

In many low current applications, compensation capacitors are not required. However, it is recommended that the regulator input be bypassed with a capacitor if the regulator is connected to the power supply filter with long wire lengths, or if the output load capacitance is large. An input bypass capacitor should be selected to provide good high frequency characteristics to insure stable operation under all load conditions. A 0.33 μF or larger tantalum, mylar, or other capacitor having low internal impedance at high frequencies should be chosen. The bypass capacitor should be mounted with the shortest possible leads directly across the regulator's input terminals. Normally good construction techniques should be used to minimize ground loops and lead resistance drops since the regulator has no external sense lead.

Figure 9. Current Regulator



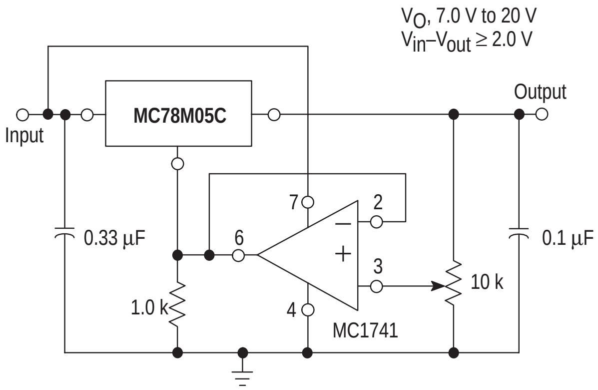
The MC78M00 regulators can also be used as a current source when connected as above. In order to minimize dissipation the MC78M05C is chosen in this application. Resistor R determines the current as follows:

$$I_O = \frac{5.0\ V}{R} + I_{IB}$$

I_{IB} = 1.5 mA over line and load changes.

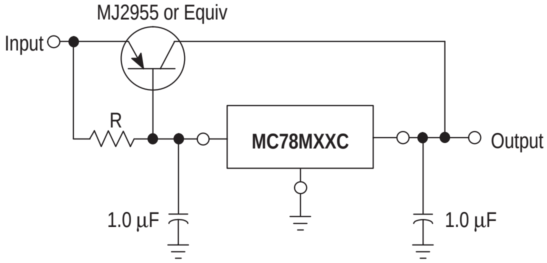
For example, a 500 mA current source would require R to be a 5.0 Ω, 10 W resistor and the output voltage compliance would be the input voltage less 7 V.

Figure 10. Adjustable Output Regulator



The addition of an operational amplifier allows adjustment to higher or intermediate values while retaining regulation characteristics. The minimum voltage obtainable with this arrangement is 2.0 V greater than the regulator voltage.

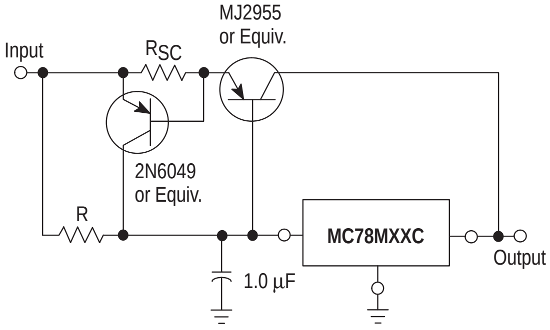
Figure 11. Current Boost Regulator



XX = 2 digits of type number indicating voltage.

The MC78M00 series can be current boosted with a PNP transistor. The MJ2955 provides current to 5.0 A. Resistor R in conjunction with the V_{BE} of the PNP determines when the pass transistor begins conducting; this circuit is not short circuit proof. Input–output differential voltage minimum is increased by V_{BE} of the pass transistor.

Figure 12. Current Boost with Short Circuit Protection



XX = 2 digits of type number indicating voltage.

The circuit of Figure 10 can be modified to provide supply protection against short circuits by adding a short circuit sense resistor, R_{SC}, and an additional PNP transistor. The current sensing PNP must be able to handle the short circuit current of the three–terminal regulator .Therefore, a 4 A plastic power transistor is specified.

MOTOROLA

MC78T00
Series

Three-Ampere Positive Voltage Regulators

This family of fixed voltage regulators are monolithic integrated circuits capable of driving loads in excess of 3.0 A. These three–terminal regulators employ internal current limiting, thermal shutdown, and safe–area compensation. Devices are available with improved specifications, including a 2% output voltage tolerance, on AC–suffix 5.0, 12 and 15 V device types.

Although designed primarily as a fixed voltage regulator, these devices can be used with external components to obtain adjustable voltages and currents. This series of devices can be used with a series–pass transistor to supply up to 15 A at the nominal output voltage.

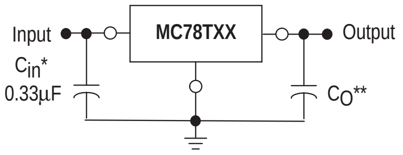
- Output Current in Excess of 3.0 A
- Power Dissipation: 25 W
- No External Components Required
- Output Voltage Offered in 2% and 4% Tolerance*
- Thermal Regulation is Specified
- Internal Thermal Overload Protection
- Internal Short Circuit Current Limiting
- Output Transistor Safe–Area Compensation

MAXIMUM RATINGS (T_A = +25°C, unless otherwise noted.)

Rating	Symbol	Value	Unit
Input Voltage (5.0 V – 12 V) (15 V)	V_I	35 40	Vdc
Power Dissipation and Thermal Characteristics Plastic Package (Note 1) T_A = +25°C Thermal Resistance, Junction–to–Air T_C = +25°C Thermal Resistance, Junction–to–Case	 P_D $R_{\theta JA}$ P_D $R_{\theta JC}$	 Internally Limited 65 Internally Limited 2.5	 °C/W °C/W
Storage Junction Temperature	T_{stg}	+150	°C
Operating Junction Temperature Range (MC78T00C, AC)	T_J	0 to +125	°C

NOTES: 1. Although power dissipation is internally limited, specifications apply only for $P_O \le P_{max}$, P_{max} = 25 W.

Simplified Application



A common ground is required between the input and the output voltages. The input voltage must remain typically 2.2 V above the output voltage even during the low point on the input ripple voltage.

XX these two digits of the type number indicate voltage.

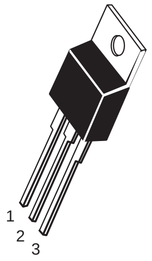
* C_{in} is required if regulator is located an appreciable distance from power supply filter. (See Applications Information for details.)

** C_O is not needed for stability; however, it does improve transient response.

THREE–AMPERE POSITIVE FIXED VOLTAGE REGULATORS

**SEMICONDUCTOR
TECHNICAL DATA**

T SUFFIX
PLASTIC PACKAGE
CASE 221A



Pin 1. Input
2. Ground
3. Output

Heatsink surface is connected to Pin 2.

DEVICE TYPE/NOMINAL OUTPUT VOLTAGE

MC78T05	5.0 V	MC78T12	12 V
MC78T08	8.0 V	MC78T15	15 V

ORDERING INFORMATION

Device	V_O Tol.	Operating Temperature Range	Package
MC78TXXCT MC78TXXACT	4% 2%*	T_J = 0° to +125°C	Plastic Power
MC78TXXBT# MC78TXXABT#	4% 2%*	T_J = –40° to +125°C	Plastic Power

XX Indicates nominal voltage.

* 2% regulators available in 5, 12 and 15 V devices.

\# Automotive temperature range selections are available with special test conditions and additional tests. Contact your local Motorola sales office for information.

ELECTRICAL CHARACTERISTICS (V_{in} = 10 V, I_O = 3.0 A, 0°C ≤ T_J ≤ 125°C, P_O ≤ P_{max} [Note 1], unless otherwise noted.)

Characteristics	Symbol	MC78T05AC			MC78T05C			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage	V_O							Vdc
(5.0 mA ≤ I_O ≤ 3.0 A, T_J = +25°C)		4.9	5.0	5.1	4.8	5.0	5.2	
(5.0 mA ≤ I_O ≤ 3.0 A; 5.0 mA ≤ I_O ≤ 2.0 A, 7.3 Vdc ≤ V_{in} ≤ 20 Vdc)		4.8	5.0	5.2	4.75	5.0	5.25	
Line Regulation (Note 2) (7.2 Vdc ≤ V_{in} ≤ 35 Vdc, I_O = 5.0 mA, T_J = +25°C; 7.2 Vdc ≤ V_{in} ≤ 35 Vdc, I_O = 1.0 A, T_J = +25°C; 8.0 Vdc ≤ V_{in} ≤ 12 Vdc, I_O = 3.0 A, T_J = +25°C; 7.5 Vdc ≤ V_{in} ≤ 20 Vdc, I_O = 1.0 A)	Reg_{line}	–	3.0	25	–	3.0	25	mV
Load Regulation (Note 2)	Reg_{load}							mV
(5.0 mA ≤ I_O ≤ 3.0 A, T_J = +25°C)		–	10	30	–	10	30	
(5.0 mA ≤ I_O ≤ 3.0 A)		–	15	80	–	15	80	
Thermal Regulation (Pulse = 10 ms, P = 20 W, T_A = +25°C)	Reg_{therm}	–	0.001	0.01	–	0.002	0.03	%V_O/W
Quiescent Current	I_B							mA
(5.0 mA ≤ I_O ≤ 3.0 A, T_J = +25°C)		–	3.5	5.0	–	3.5	5.0	
(5.0 mA ≤ I_O ≤ 3.0 A)		–	4.0	6.0	–	4.0	6.0	
Quiescent Current Change (7.2 Vdc ≤ V_{in} ≤ 35 Vdc, I_O = 5.0 mA, T_J = +25°C; 5.0 mA ≤ I_O ≤ 3.0 A, T_J = +25°C; 7.5 Vdc ≤ V_{in} ≤ 20 Vdc, I_O = 1.0 A)	ΔI_B	–	0.3	1.0	–	0.3	1.0	mA
Ripple Rejection (8.0 Vdc ≤ V_{in} ≤ 18 Vdc, f = 120 Hz, I_O = 2.0 A, T_J = 25°C)	RR	62	75	–	62	75	–	dB
Dropout Voltage (I_O = 3.0 A, T_J = +25°C)	$V_{in}–V_O$	–	2.2	2.5	–	2.2	2.5	Vdc
Output Noise Voltage (10 Hz ≤ f ≤ 100 kHz, T_J = +25°C)	V_n	–	10	–	–	10	–	µV/V_O
Output Resistance (f = 1.0 kHz)	R_O	–	2.0	–	–	20	–	mΩ
Short Circuit Current Limit (V_{in} = 35 Vdc, T_J = +25°C)	I_{SC}	–	1.5	–	–	1.5	–	A
Peak Output Current (T_J = +25°C)	I_{max}	–	5.0	–	–	5.0	–	A
Average Temperature Coefficient of Output Voltage (I_O = 5.0 mA)	TCV_O	–	0.2	–	–	0.2	–	mV/°C

NOTES: 1. Although power dissipation is internally limited, specifications apply only for P_O ≤ P_{max}, P_{max} = 25 W.
2. Line and load regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

ELECTRICAL CHARACTERISTICS (V_{in} = 13 V, I_O = 3.0 A, 0°C ≤ T_J ≤ 125°C, P_O ≤ P_{max} [Note 1], unless otherwise noted.)

Characteristics	Symbol	MC78T08C			Unit
		Min	Typ	Max	
Output Voltage	V_O				Vdc
(5.0 mA ≤ I_O ≤ 3.0 A, T_J = +25°C)		7.7	8.0	8.3	
(5.0 mA ≤ I_O ≤ 3.0 A; 5.0 mA ≤ I_O ≤ 2.0 A, 10.4 Vdc ≤ V_{in} ≤ 23 Vdc)		7.6	8.0	8.4	
Line Regulation (Note 2) (10.3 Vdc ≤ V_{in} ≤ 35 Vdc, I_O = 5.0 mA, T_J = +25°C 10.3 Vdc ≤ V_{in} ≤ 35 Vdc, I_O = 1.0 A, T_J = +25°C 11 Vdc ≤ V_{in} ≤ 17 Vdc, I_O = 3.0 A, T_J = +25°C 10.7 Vdc ≤ V_{in} ≤ 23 Vdc, I_O = 1.0 A)	Reg_{line}	–	4.0	35	mV
Load Regulation (Note 2)	Reg_{load}				mV
(5.0 mA ≤ I_O ≤ 3.0 A, T_J = +25°C)		–	10	30	
(5.0 mA ≤ I_O ≤ 3.0 A)		–	15	80	
Thermal Regulation (Pulse = 10 ms, P = 20 W, T_A = +25°C)	Reg_{therm}	–	0.002	0.03	%V_O/W
Quiescent Current	I_B				mA
(5.0 mA ≤ I_O ≤ 3.0 A, T_J = +25°C)		–	3.5	5.0	
(5.0 mA ≤ I_O ≤ 3.0 A)		–	4.0	6.0	
Quiescent Current Change (10.3 Vdc ≤ V_{in} ≤ 35 Vdc, I_O = 5.0 mA, T_J = +25°C; 5.0 mA ≤ I_O ≤ 3.0 A, T_J = +25°C; 10.7 Vdc ≤ V_{in} ≤ 23 Vdc, I_O = 1.0 A)	ΔI_B	–	0.3	1.0	mA
Ripple Rejection (11 Vdc ≤ V_{in} ≤ 21 Vdc, f = 120 Hz, I_O = 2.0 A, T_J = 25°C)	RR	60	71	–	dB
Dropout Voltage (I_O = 3.0 A, T_J = +25°C)	$V_{in}–V_O$	–	2.2	2.5	Vdc
Output Noise Voltage (10 Hz ≤ f ≤ 100 kHz, T_J = +25°C)	V_n	–	10	–	µV/V_O
Output Resistance (f = 1.0 kHz)	R_O	–	2.0	–	mΩ
Short Circuit Current Limit (V_{in} = 35 Vdc, T_J = +25°C)	I_{SC}	–	1.5	–	A
Peak Output Current (T_J = +25°C)	I_{max}	–	5.0	–	A
Average Temperature Coefficient of Output Voltage (I_O = 5.0 mA)	TCV_O	–	0.3	–	mV/°C

NOTES: 1. Although power dissipation is internally limited, specifications apply only for P_O ≤ P_{max}, P_{max} = 25 W.
2. Line and load regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

ELECTRICAL CHARACTERISTICS (V_{in} = 17 V, I_O = 3.0 A, 0°C ≤ T_J ≤ 125°C, $P_O \le P_{max}$ [Note 1], unless otherwise noted.)

Characteristics	Symbol	MC78T12AC			MC78T12C			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (5.0 mA ≤ I_O ≤ 3.0 A, T_J = +25°C) (5.0 mA ≤ I_O ≤ 3.0 A, 5.0 mA ≤ I_O ≤ 2.0 A, 14.5 Vdc ≤ V_{in} ≤ 27 Vdc)	V_O	 11.75 11.5	 12 12	 12.25 12.5	 11.5 11.4	 12 12	 12.5 12.6	Vdc
Line Regulation (Note 2) (14.5 Vdc ≤ V_{in} ≤ 35 Vdc, I_O = 5.0 mA, T_J = +25°C; 14.5 Vdc ≤ V_{in} ≤ 35 Vdc, I_O = 1.0 A, T_J = +25°C; 16 Vdc ≤ V_{in} ≤ 22 Vdc, I_O = 3.0 A, T_J = +25°C; 14.9 Vdc ≤ V_{in} ≤ 27 Vdc, I_O = 1.0 A)	Reg_{line}	–	6.0	45	–	6.0	45	mV
Load Regulation (Note 2) (5.0 mA ≤ I_O ≤ 3.0 A, T_J = +25°C) (5.0 mA ≤ I_O ≤ 3.0 A)	Reg_{load}	 – –	 10 15	 30 80	 – –	 10 15	 30 80	mV
Thermal Regulation (Pulse = 10 ms, P = 20 W, T_A = +25°C)	Reg_{therm}	–	0.001	0.01	–	0.002	0.03	%V_O/W
Quiescent Current (5.0 mA ≤ I_O ≤ 3.0 A, T_J = +25°C) (5.0 mA ≤ I_O ≤ 3.0 A)	I_B	 – –	 3.5 4.0	 5.0 6.0	 – –	 3.5 4.0	 5.0 6.0	mA
Quiescent Current Change (14.5 Vdc ≤ V_{in} ≤ 35 Vdc, I_O = 5.0 mA, T_J = +25°C; 5.0 mA ≤ I_O ≤ 3.0 A, T_J = +25°C; 14.9 Vdc ≤ V_{in} ≤ 27 Vdc, I_O = 1.0 A)	ΔI_B	–	0.3	1.0	–	0.3	1.0	mA
Ripple Rejection (15 Vdc ≤ V_{in} ≤ 25 Vdc, f = 120 Hz, I_O = 2.0 A, T_J = 25°C)	RR	57	67	–	57	67	–	dB
Dropout Voltage (I_O = 3.0 A, T_J = +25°C)	$V_{in} - V_O$	–	2.2	2.5	–	2.2	2.5	Vdc
Output Noise Voltage (10 Hz ≤ f ≤ 100 kHz, T_J = +25°C)	V_n	–	10	–	–	10	–	µV/V_O
Output Resistance (f = 1.0 kHz)	R_O	–	2.0	–	–	20	–	mΩ
Short Circuit Current Limit (V_{in} = 35 Vdc, T_J = +25°C)	I_{SC}	–	1.5	–	–	1.5	–	A
Peak Output Current (T_J = +25°C)	I_{max}	–	5.0	–	–	5.0	–	A
Average Temperature Coefficient of Output Voltage (I_O = 5.0 mA)	TCV_O	–	0.5	–	–	0.5	–	mV/°C

NOTES: 1. Although power dissipation is internally limited, specifications apply only for $P_O \le P_{max}$, P_{max} = 25 W.
2. Line and load regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

ELECTRICAL CHARACTERISTICS (V_{in} = 20 V, I_O = 3.0 A, 0°C ≤ T_J ≤ 125°C, $P_O \le P_{max}$ [Note 1], unless otherwise noted.)

Characteristics	Symbol	MC78T15AC			MC78T15C			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage	V_O							Vdc
(5.0 mA ≤ I_O ≤ 3.0 A, T_J = +25°C)		14.7	15	15.3	14.4	15	15.6	
(5.0 mA ≤ I_O ≤ 3.0 A; 5.0 mA ≤ I_O ≤ 2.0 A, 17.5 Vdc ≤ V_{in} ≤ 30 Vdc)		14.4	15	15.6	14.25	15	15.75	
Line Regulation (Note 2) (17.6 Vdc ≤ V_{in} ≤ 40 Vdc, I_O = 5.0 mA, T_J = +25°C; 17.6 Vdc ≤ V_{in} ≤ 40 Vdc, I_O = 1.0 A, T_J = +25°C; 20 Vdc ≤ V_{in} ≤ 26 Vdc, I_O = 3.0 A, T_J = +25°C; 18 Vdc ≤ V_{in} ≤ 30 Vdc, I_O = 1.0 A)	Reg_{line}	–	7.5	55	–	7.5	55	mV
Load Regulation (Note 2)	Reg_{load}							mV
(5.0 mA ≤ I_O ≤ 3.0 A, T_J = +25°C)		–	10	30	–	10	30	
(5.0 mA ≤ I_O ≤ 3.0 A)		–	15	80	–	15	80	
Thermal Regulation (Pulse = 10 ms, P = 20 W, T_A = +25°C)	Reg_{therm}	–	0.001	0.01	–	0.002	0.03	$\%V_O/W$
Quiescent Current	I_B							mA
(5.0 mA ≤ I_O ≤ 3.0 A, T_J = +25°C)		–	3.5	5.0	–	3.5	5.0	
(5.0 mA ≤ I_O ≤ 3.0 A)		–	4.0	6.0	–	4.0	6.0	
Quiescent Current Change (17.6 Vdc ≤ V_{in} ≤ 40 Vdc, I_O = 5.0 mA, T_J = +25°C; 5.0 mA ≤ I_O ≤ 3.0 A, T_J = +25°C; 18 Vdc ≤ V_{in} ≤ 30 Vdc, I_O = 1.0 A)	ΔI_B	–	0.3	1.0	–	0.3	1.0	mA
Ripple Rejection (18.5 Vdc ≤ V_{in} ≤ 28.5 Vdc, f = 120 Hz, I_O = 2.0 A, T_J = 25°C)	RR	55	65	–	55	65	–	dB
Dropout Voltage (I_O = 3.0 A, T_J = +25°C)	$V_{in}–V_O$	–	2.2	2.5	–	2.2	2.5	Vdc
Output Noise Voltage (10 Hz ≤ f ≤ 100 kHz, T_J = +25°C)	V_n	–	10	–	–	10	–	$\mu V/V_O$
Output Resistance (f = 1.0 kHz)	R_O	–	2.0	–	–	20	–	mΩ
Short Circuit Current Limit (V_{in} = 40 Vdc, T_J = +25°C)	I_{SC}	–	1.0	–	–	1.0	–	A
Peak Output Current (T_J = +25°C)	I_{max}	–	5.0	–	–	5.0	–	A
Average Temperature Coefficient of Output Voltage (I_O = 5.0 mA)	TCV_O	–	0.6	–	–	0.6	–	mV/°C

NOTES: 1. Although power dissipation is internally limited, specifications apply only for $P_O \le P_{max}$, P_{max} = 25 W.
2. Line and load regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

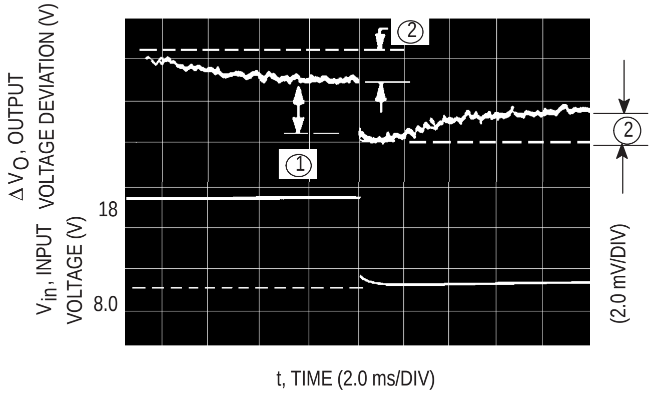
VOLTAGE REGULATOR PERFORMANCE

The performance of a voltage regulator is specified by its immunity to changes in load, input voltage, power dissipation, and temperature. Line and load regulation are tested with a pulse of short duration (< 100µs) and are strictly a function of electrical gain. However, pulse widths of longer duration (> 1.0 ms) are sufficient to affect temperature gradients across the die. These temperature gradients can cause a change in the output voltage, in addition to changes caused by line and load regulation. Longer pulse widths and thermal gradients make it desirable to specify thermal regulation.

Thermal regulation is defined as the change in output voltage caused by a change in dissipated power for a specified time, and is expressed as a percentage output voltage change per watt. The change in dissipated power can be caused by a change in either the input voltage or the load current. Thermal regulation is a function of IC layout and die attach techniques, and usually occurs within 10 ms of a change in power dissipation. After 10 ms, additional changes in the output voltage are due to the temperature coefficient of the device.

Figure 1 shows the line and thermal regulation response of a typical MC78T05AC to a 20 W input pulse. The variation of the output voltage due to line regulation is labeled ① and the thermal regulation component is labeled ②. Figure 2 shows the load and thermal regulation response of a typical MC78T05AC to a 20 W load pulse. The output voltage variation due to load regulation is labeled ① and the thermal regulation component is labeled ②.

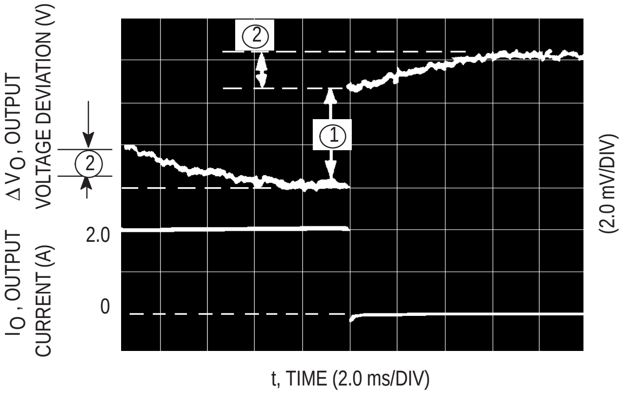
Figure 1. MC78T05AC Line and Thermal Regulation



V_{out} = 5.0 V
V_{in} = 8.0 V → 18 V → 8.0 V
I_{out} = 2.0 A

① = Reg_{line} = 2.4 mV
② = Reg_{therm} = 0.0015%V_O/W

Figure 2. MC78T05AC Load and Thermal Regulation



V_{out} = 5.0 V
V_{in} = 15
I_{out} = 0 A → 2.0 A → 0 A

① = Reg_{line} = 4.4 mV
② = Reg_{therm} = 0.0015%V_O/W

Representative Schematic Diagram

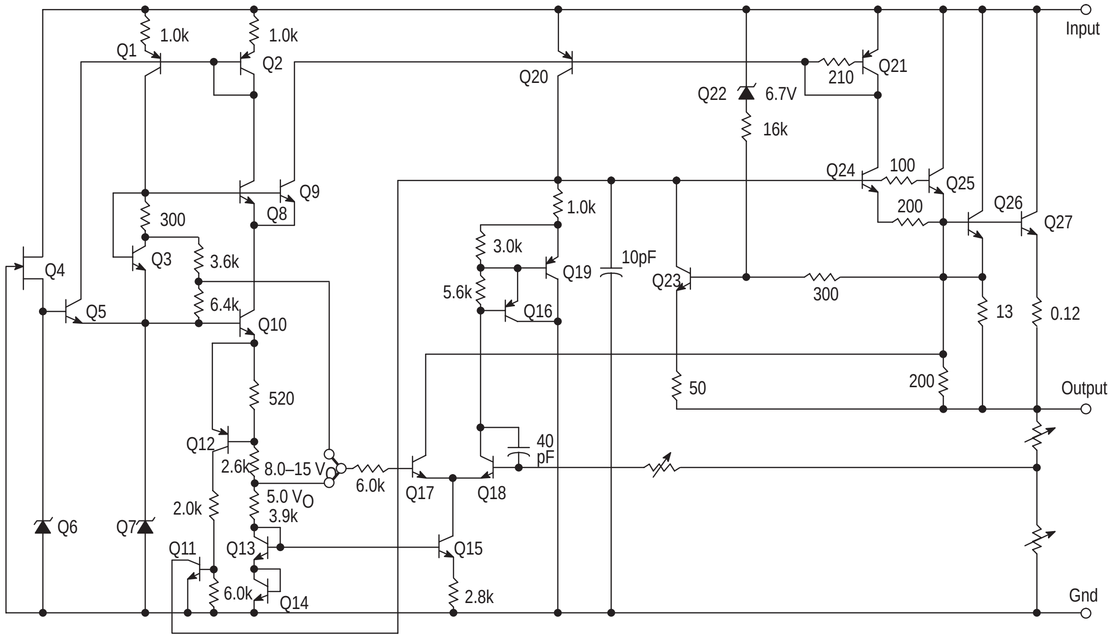


Figure 3. Temperature Stability

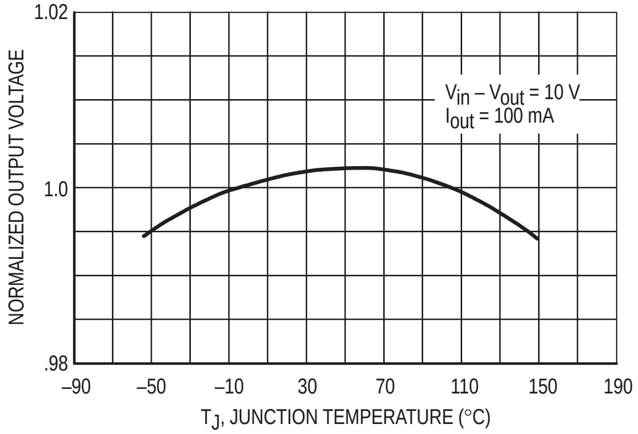


Figure 4. Output Impedance

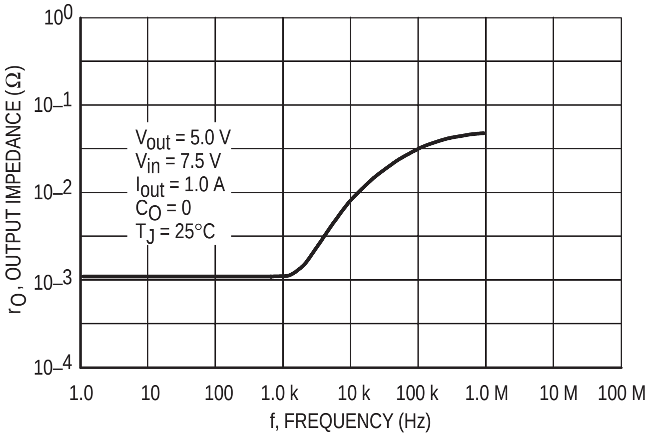


Figure 5. Ripple Rejection versus Frequency

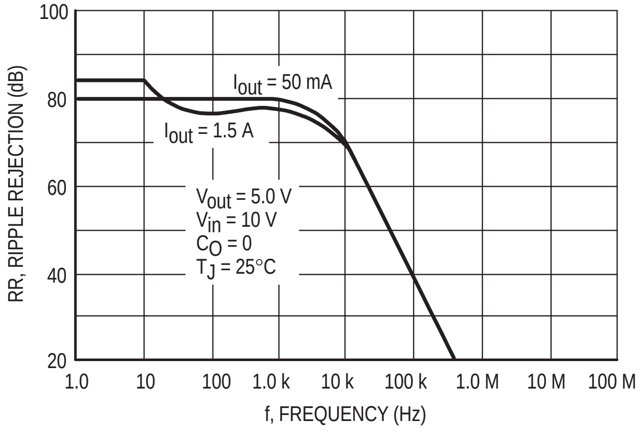


Figure 6. Ripple Rejection versus Output Current

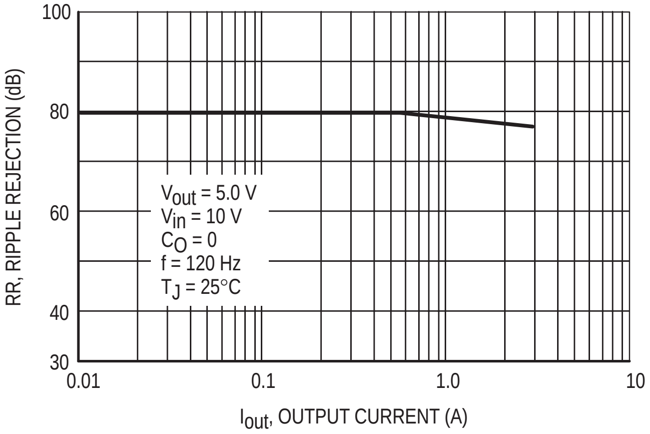


Figure 7. Quiescent Current versus Input Voltage

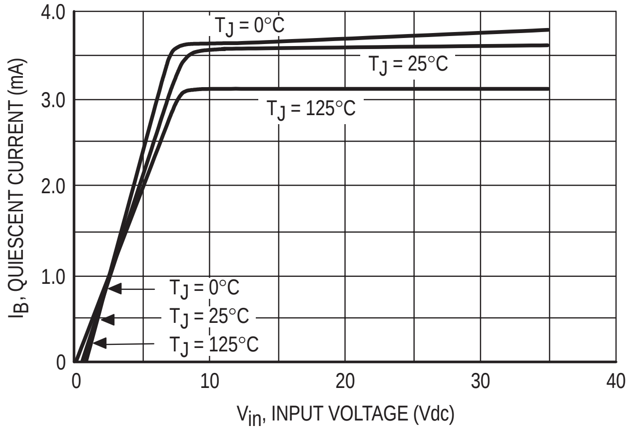


Figure 8. Quiescent Current versus Output Current

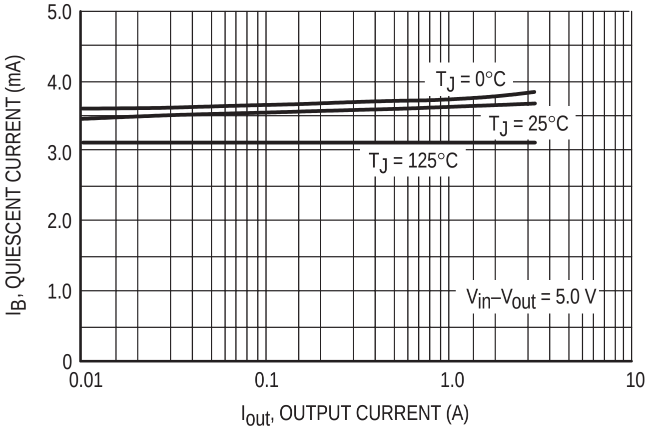


Figure 9. Dropout Voltage

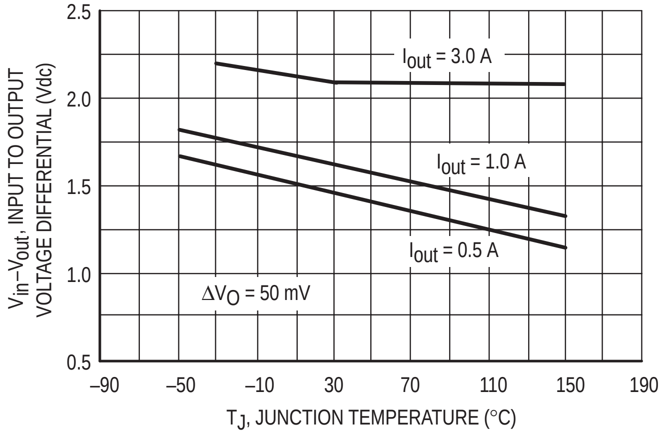


Figure 10. Peak Output Current

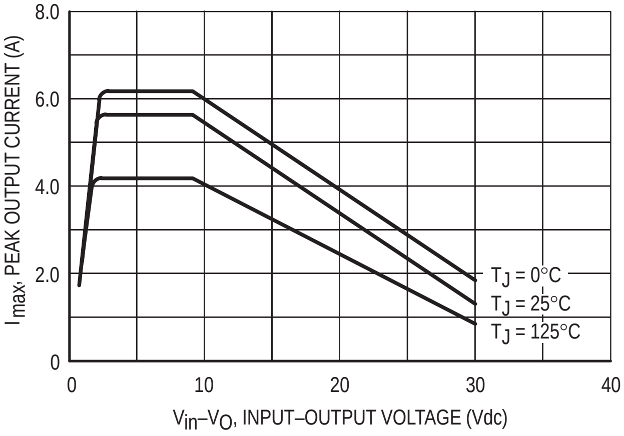


Figure 11. Line Transient Response

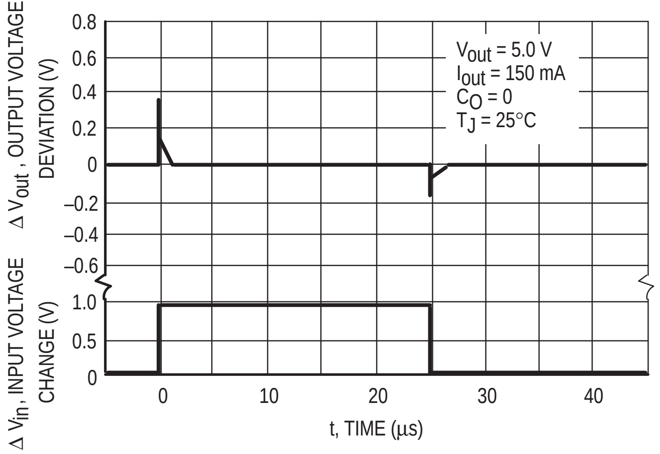


Figure 12. Load Transient Response

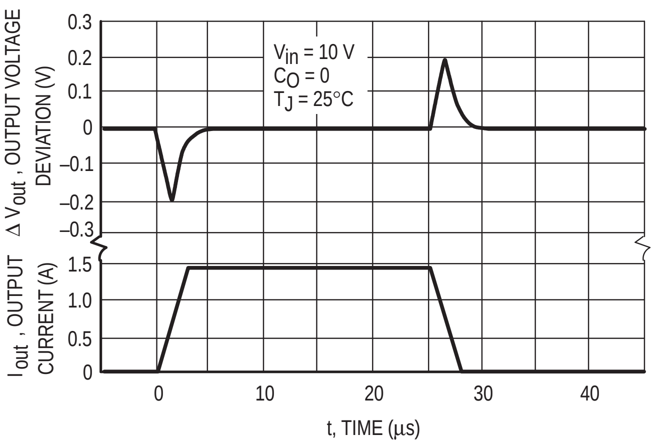
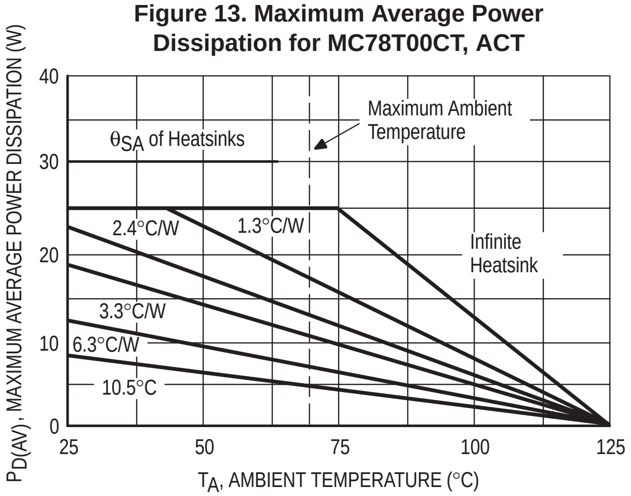


Figure 13. Maximum Average Power Dissipation for MC78T00CT, ACT



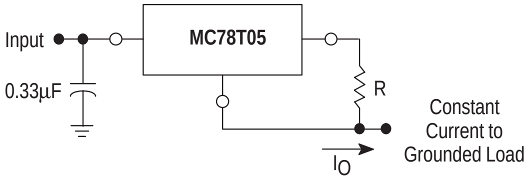
APPLICATIONS INFORMATION

Design Considerations

The MC78T00 Series of fixed voltage regulators are designed with Thermal Overload Protection that shuts down the circuit when subjected to an excessive power overload condition, Internal Short Circuit Protection that limits the maximum current the circuit will pass, and Output Transistor Safe–Area Compensation that reduces the output short circuit current as the voltage across the pass transistor is increased.

In many low current applications, compensation capacitors are not required. However, it is recommended that the regulator input be bypassed with a capacitor if the regulator is connected to the power supply filter with long wire lengths, or if the output load capacitance is large. An input bypass capacitor should be selected to provide good high frequency characteristics to insure stable operation under all load conditions. A 0.33 µF or larger tantalum, mylar, or other capacitor having low internal impedance at high frequencies should be chosen. The bypass capacitor should be mounted with the shortest possible leads directly across the regulator's input terminals. Normally good construction techniques should be used to minimize ground loops and lead resistance drops since the regulator has no external sense lead.

Figure 14. Current Regulator



The MC78T05 regulator can also be used as a current source when connected as above. In order to minimize dissipation the MC78T05 is chosen in this application. Resistor R determines the current as follows:

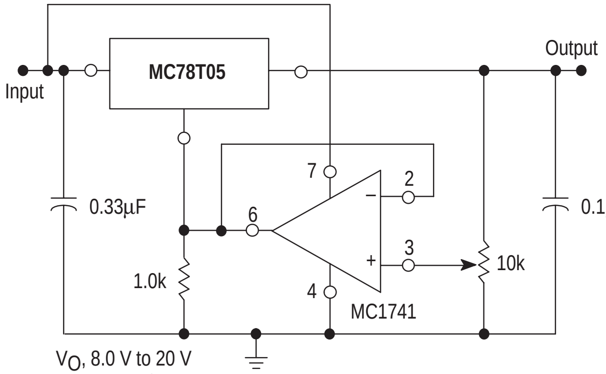
$$I_O = \frac{5.0\ V}{R} + I_B$$

$\Delta I_B \cong$ 0.7 mA over line, load and Temperature changes

$I_B \cong$ 3.5 mA

For example, a 2.0 A current source would require R to be a 2.5 Ω, 10 W resistor and the output voltage compliance would be the input voltage less 7.0 V.

Figure 15. Adjustable Output Regulator

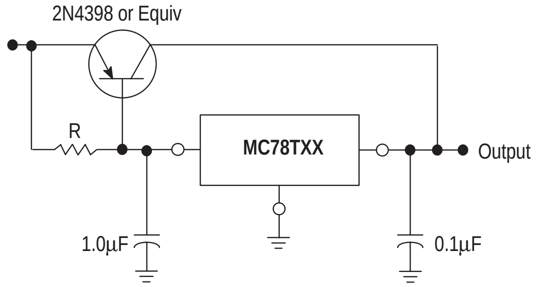


V_O, 8.0 V to 20 V

$V_{in} - V_O \geq 2.5$ V

The addition of an operational amplifier allows adjustment to higher or intermediate values while retaining regulation characteristics. The minimum voltage obtainable with this arrangement is 3.0 V greater than the regulator voltage.

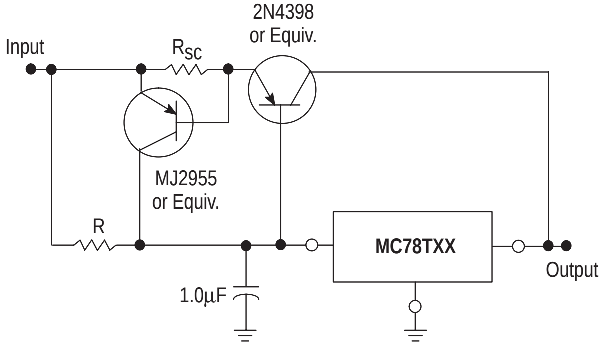
Figure 16. Current Boost Regulator



XX = 2 digits of type number indicating voltage.

The MC78T00 series can be current boosted with a PNP transistor. The 2N4398 provides current to 15 A. Resistor R in conjuction with the V_{BE} of the PNP determines when the pass transistor begins conducting; this circuit is not short circuit proof. Input–output differential voltage minimum is increased by the V_{BE} of the pass transistor.

Figure 17. Current Boost With Short Circuit Protection



XX = 2 digits of type number indicating voltage.

The circuit of Figure 17 can be modified to provide supply protection against short circuits by adding a short circuit sense resistor, R_{SC}, and an additional PNP transistor. The current sensing PNP must be able to handle the short circuit current of the three–terminal regulator. Therefore, an eight–ampere power transistor is specified.

MOTOROLA

MC78BC00 Series

Product Preview

Micropower Voltage Regulator

The MC78BC00 voltage regulators are specifically designed to be used with an external power transistor to deliver high current with high voltage accuracy and low quiescent current.

The MC78BC00 series are devices suitable for constructing regulators with ultra–low dropout voltage and output current in the range of several tens of mA to hundreds of mA. These devices have a chip enable function, which minimizes the standby mode current drain. Each of these devices contains a voltage reference unit, an error amplifier, a driver transistor and resistors. These devices are available in the SOT–23, 5 pin surface mount packages.

These devices are ideally suited for battery powered equipment, and power sources for hand–held audio instruments, communication equipment and domestic appliances.

MC78BC00 Series Features:

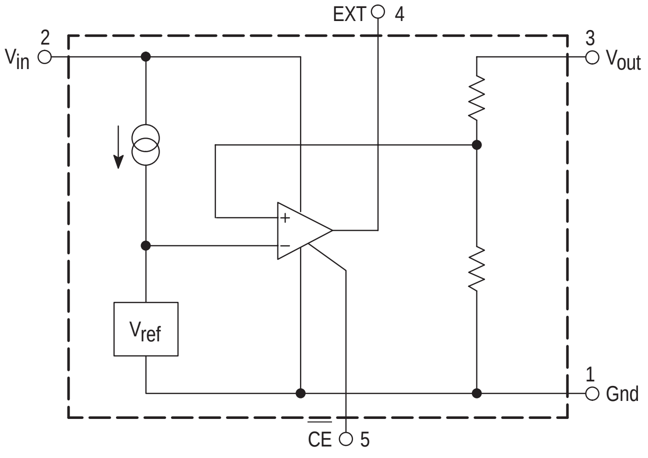
- Ultra–Low Supply Current (50 µA)
- Standby Mode (0.2 µA)
- Ultra–Low Dropout Voltage (0.1 V with External Transistor and I_O = 100 mA)
- Excellent Line Regulation (Typically 0.1%/V)
- High Accuracy Output Voltage (±2.5%)

ORDERING INFORMATION

Device	Output Voltage	Operating Temperature Range	Package
MC78BC30NTR	3.0	T_A = –30° to +80°C	SOT–23
MC78BC33NTR	3.3		
MC78BC40NTR	4.0		
MC78BC50NTR	5.0		

Other voltages from 2.0 to 6.0 V, in 0.1 V increments, are available upon request. Consult your local Motorola sales office for information.

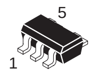
Representative Block Diagram



This device contains 13 active transistors.

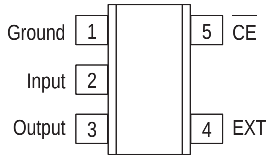
VOLTAGE REGULATOR WITH EXTERNAL POWER TRANSISTOR

SEMICONDUCTOR TECHNICAL DATA



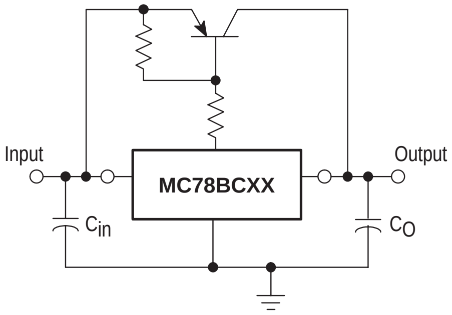
N SUFFIX
PLASTIC PACKAGE
CASE 1212
(SOT–23)

PIN CONNECTIONS



(Top View)

Standard Application



MOTOROLA

MC78FC00 Series

Product Preview

Micropower Voltage Regulator

The MC78FC00 series voltage regulators are specifically designed for use as a power source for video instruments, handheld communication equipment, and battery powered equipment.

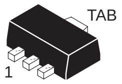
The MC78FC00 series voltage regulator ICs feature a high accuracy output voltage and ultra–low quiescent current. Each device contains a voltage reference unit, an error amplifier, a driver transistor, and resistors for setting output voltage, and a current limit circuit. These devices are available in SOT–89 surface mount packages, and allow construction of an efficient, constant voltage power supply circuit.

MC78FC00 Series Features:

- Ultra–Low Quiescent Current of 1.1 µA Typical
- Ultra–Low Dropout Voltage (0.5 V Typical)
- Large Output Current (120 mA Typical)
- Excellent Line Regulation (0.1%)
- Wide Operating Voltage Range (2.0 V to 10 V)
- High Accuracy Output Voltage (±2.5%)
- Wide Output Voltage Range (2.0 V to 6.0 V)
- Surface Mount Package (SOT–89)

MICROPOWER ULTRA–LOW QUIESCENT CURRENT VOLTAGE REGULATORS

SEMICONDUCTOR TECHNICAL DATA



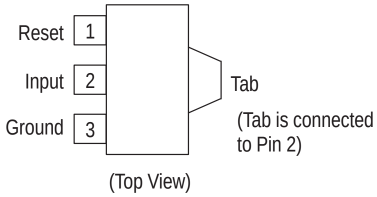
H SUFFIX
PLASTIC PACKAGE
CASE 1213
(SOT–89)

ORDERING INFORMATION

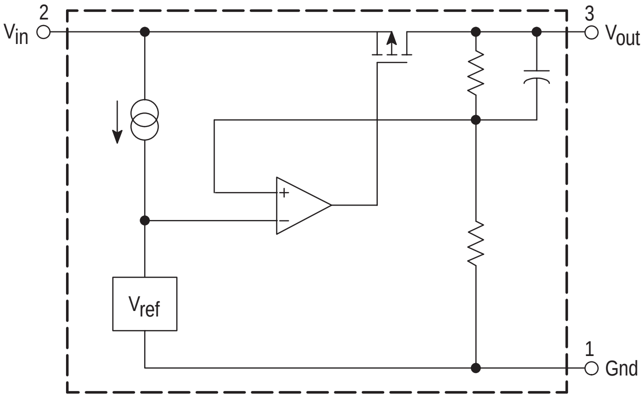
Device	Output Voltage	Operating Temperature Range	Package
MC78FC30HT1	3.0	T_A = –30° to +80°C	SOT–89
MC78FC33HT1	3.3		
MC78FC40HT1	4.0		
MC78FC50HT1	5.0		

Other voltages from 2.0 to 6.0 V, in 0.1 V increments, are available upon request. Consult your local Motorola sales office for information.

PIN CONNECTIONS

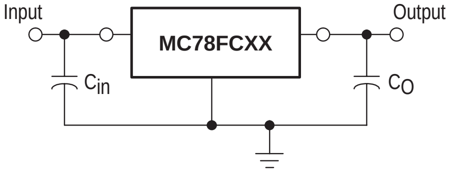


Representative Block Diagram



This device contains 11 active transistors.

Standard Application



MOTOROLA

Product Preview

Micropower Voltage Regulator

The MC78LC00 series voltage regulators are specifically designed for use as a power source for video instruments, handheld communication equipment, and battery powered equipment.

The MC78LC00 series features an ultra–low quiescent of 1.1 µA and a high accuracy output voltage. Each device contains a voltage reference, an error amplifier, a driver transistor and resistors for setting the output voltage. These devices are available in either SOT–89, 3 pin, or SOT–23, 5 pin, surface mount packages.

MC78LC00 Series Features:

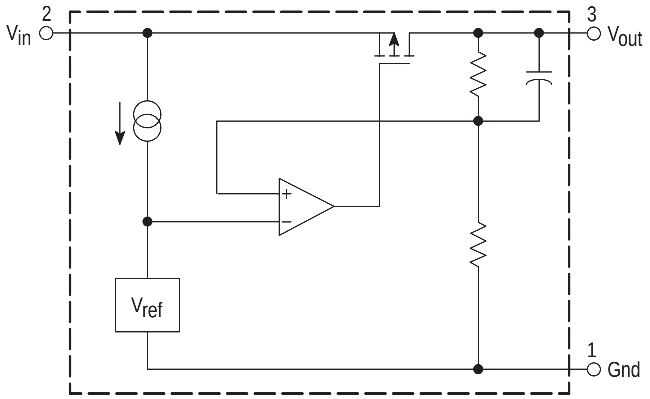
- Low Quiescent Current of 1.1 µA Typical
- Low Dropout Voltage (30 mV Typical)
- Excellent Line Regulation (0.1%)
- High Accuracy Output Voltage (±2.5%)
- Wide Output Voltage Range (2.0 V to 6.0 V)
- Output Current for Low Power (80 mA Typical)
- Two Surface Mount Packages (SOT–89, 3 Pin, or SOT–23, 5 Pin)

ORDERING INFORMATION

Device	Output Voltage	Operating Temperature Range	Package
MC78LC30HT1	3.0	T_A = –30° to +80°C	SOT–89
MC78LC33HT1	3.3		
MC78LC40HT1	4.0		
MC78LC50HT1	5.0		
MC78LC30NTR	3.0		SOT–23
MC78LC33NTR	3.3		
MC78LC40NTR	4.0		
MC78LC50NTR	5.0		

Other voltages from 2.0 to 6.0 V, in 0.1 V increments, are available upon request. Consult your local Motorola sales office for information.

Representative Block Diagram

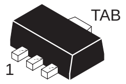


This device contains 8 active transistors.

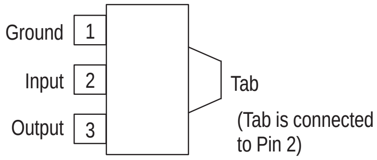
MC78LC00 Series

MICROPOWER ULTRA–LOW QUIESCENT CURRENT VOLTAGE REGULATORS

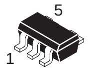
SEMICONDUCTOR TECHNICAL DATA



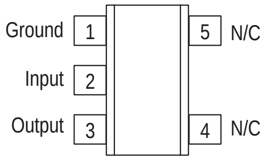
H SUFFIX
PLASTIC PACKAGE
CASE 1213
(SOT–89)



(Top View)

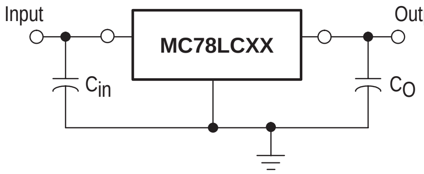


N SUFFIX
PLASTIC PACKAGE
CASE 1212
(SOT–23)



(Top View)

Standard Application



MOTOROLA

MC7900 Series

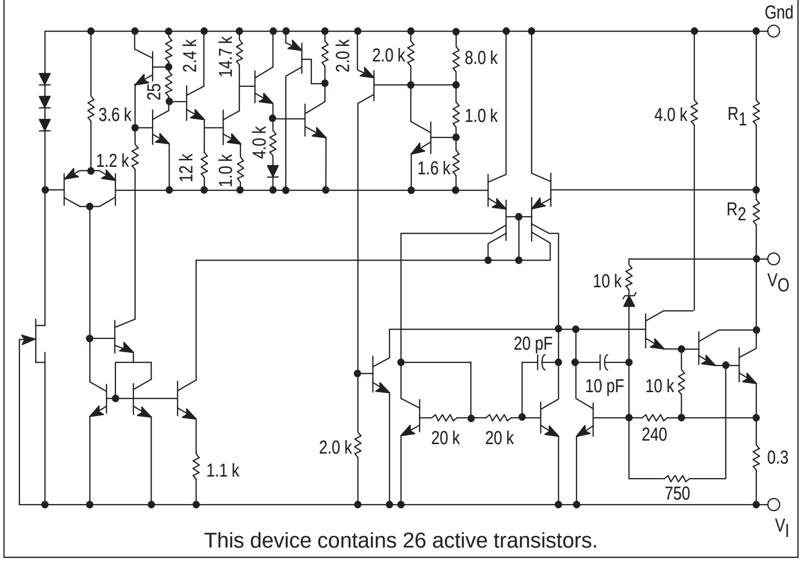
Three-Terminal Negative Voltage Regulators

The MC7900 series of fixed output negative voltage regulators are intended as complements to the popular MC7800 series devices. These negative regulators are available in the same seven–voltage options as the MC7800 devices. In addition, one extra voltage option commonly employed in MECL systems is also available in the negative MC7900 series.

Available in fixed output voltage options from –5.0 V to –24 V, these regulators employ current limiting, thermal shutdown, and safe–area compensation – making them remarkably rugged under most operating conditions. With adequate heatsinking they can deliver output currents in excess of 1.0 A.

- No External Components Required
- Internal Thermal Overload Protection
- Internal Short Circuit Current Limiting
- Output Transistor Safe–Area Compensation
- Available in 2% Voltage Tolerance (See Ordering Information)

Representative Schematic Diagram



This device contains 26 active transistors.

ORDERING INFORMATION

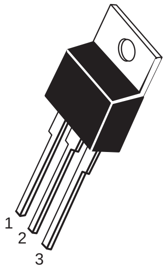
Device	Output Voltage Tolerance	Operating Temperature Range	Package
MC79XXACD2T	2%	T_J = 0° to +125°C	Surface Mount
MC79XXCD2T	4%		
MC79XXACT	2%		Insertion Mount
MC79XXCT	4%		
MC79XXBD2T	4%	T_J = –40° to +125°C	Surface Mount
MC79XXBT			Insertion Mount

XX indicates nominal voltage.

THREE–TERMINAL NEGATIVE FIXED VOLTAGE REGULATORS

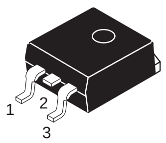
T SUFFIX
PLASTIC PACKAGE
CASE 221A

Heatsink surface
connected to Pin 2.



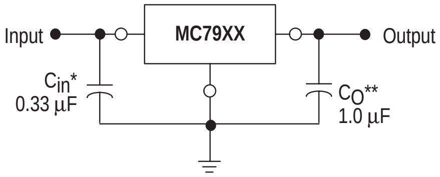
Pin 1. Ground
2. Input
3. Output

D2T SUFFIX
PLASTIC PACKAGE
CASE 936
(D^2PAK)



Heatsink surface (shown as terminal 4 in case outline drawing) is connected to Pin 2.

STANDARD APPLICATION



A common ground is required between the input and the output voltages. The input voltage must remain typically 2.0 V above more negative even during the high point of the input ripple voltage.

XX, These two digits of the type number indicate nominal voltage.
* C_{in} is required if regulator is located an appreciable distance from power supply filter.
** C_O improve stability and transient response.

DEVICE TYPE/NOMINAL OUTPUT VOLTAGE

MC7905	5.0 V	MC7912	12 V
MC7905.2	5.2 V	MC7915	15 V
MC7906	6.0 V	MC7918	28 V
MC7908	8.0 V	MC7924	24 V

MAXIMUM RATINGS (T_A = +25°C, unless otherwise noted.)

Rating	Symbol	Value	Unit
Input Voltage (–5.0 V ≥ V_O ≥ –18 V) (24 V)	V_I	–35 –40	Vdc
Power Dissipation			
Case 221A			
T_A = +25°C	P_D	Internally Limited	W
Thermal Resistance, Junction–to–Ambient	θ_{JA}	65	°C/W
Thermal Resistance, Junction–to–Case	θ_{JC}	5.0	°C/W
Case 936 (D^2PAK)			
T_A = +25°C	P_D	Internally Limited	W
Thermal Resistance, Junction–to–Ambient	θ_{JA}	70	°C/W
Thermal Resistance, Junction–to–Case	θ_{JC}	5.0	°C/W
Storage Junction Temperature Range	T_{stg}	–65 to +150	°C
Junction Temperature	T_J	+150	°C

THERMAL CHARACTERISTICS

Characteristics	Symbol	Max	Unit
Thermal Resistance, Junction–to–Ambient	$R_{\theta JA}$	65	°C/W
Thermal Resistance, Junction–to–Case	$R_{\theta JC}$	5.0	°C/W

MC7905C
ELECTRICAL CHARACTERISTICS (V_I = –10 V, I_O = 500 mA, 0°C < T_J < +125°C, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	–4.8	–5.0	–5.2	Vdc
Line Regulation (Note 1)	Reg_{line}				mV
(T_J = +25°C, I_O = 100 mA)					
–7.0 Vdc ≥ V_I ≥ –25 Vdc		–	7.0	50	
–8.0 Vdc ≥ V_I ≥ –12 Vdc		–	2.0	25	
(T_J = +25°C, I_O = 500 mA)					
–7.0 Vdc ≥ V_I ≥ –25 Vdc		–	35	100	
–8.0 Vdc ≥ V_I ≥ –12 Vdc		–	8.0	50	
Load Regulation, T_J = +25°C (Note 1)	Reg_{load}				mV
5.0 mA ≤ I_O ≤ 1.5 A		–	11	100	
250 mA ≤ I_O ≤ 750 mA		–	4.0	50	
Output Voltage –7.0 Vdc ≥ V_I ≥ –20 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P ≤ 15 W	V_O	–4.75	–	–5.25	Vdc
Input Bias Current (T_J = +25°C)	I_{IB}	–	4.3	8.0	mA
Input Bias Current Change	ΔI_{IB}				mA
–7.0 Vdc ≥ V_I ≥ –25 Vdc		–	–	1.3	
5.0 mA ≤ I_O ≤ 1.5 A		–	–	0.5	
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	–	40	–	µV
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	–	70	–	dB
Dropout Voltage I_O = 1.0 A, T_J = +25°C	$V_I–V_O$	–	2.0	–	Vdc
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA, 0°C ≤ T_J ≤ +125°C	$\Delta V_O/\Delta T$	–	–1.0	–	mV/°C

NOTE: 1. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

MC7905AC

ELECTRICAL CHARACTERISTICS (V_I = –10 V, I_O = 500 mA, 0°C < T_J < +125°C, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	–4.9	–5.0	–5.1	Vdc
Line Regulation (Note 1)	Reg_{line}				mV
–8.0 Vdc ≥ V_I ≥ –12 Vdc; I_O = 1.0 A, T_J = +25°C		–	2.0	25	
–8.0 Vdc ≥ V_I ≥ –12 Vdc; I_O = 1.0 A		–	7.0	50	
–7.5 Vdc ≥ V_I ≥ –25 Vdc; I_O = 500 mA		–	7.0	50	
–7.0 Vdc ≥ V_I ≥ –20 Vdc; I_O = 1.0 A, T_J = +25°C		–	6.0	50	
Load Regulation (Note 1)	Reg_{load}				mV
5.0 mA ≤ I_O ≤ 1.5 A, T_J = +25°C		–	11	100	
250 mA ≤ I_O ≤ 750 mA		–	4.0	50	
5.0 mA ≤ I_O ≤ 1.0 A		–	9.0	100	
Output Voltage –7.5 Vdc ≥ V_I ≥ –20 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P ≤ 15 W	V_O	–4.80	–	–5.20	Vdc
Input Bias Current	I_{IB}	–	4.4	8.0	mA
Input Bias Current Change	ΔI_{IB}				mA
–7.5 Vdc ≥ V_I ≥ –25 Vdc		–	–	1.3	
5.0 mA ≤ I_O ≤ 1.0 A		–	–	0.5	
5.0 mA ≤ I_O ≤ 1.5 A, T_J = +25°C		–	–	0.5	
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	–	40	–	µV
Ripple Rejection (I_O = mA, f = 120 Hz)	RR	–	70	–	dB
Dropout Voltage I_O = 1.0 A. T_J = +25°C	V_I–V_O	–	2.0	–	Vdc
Average Temperature Coefficient of Output Voltage I_O = 5.0 A, 0°C ≤ T_J ≤ +125°C	$\Delta V_O/\Delta T$	–	–1.0	–	mV/°C

MC7905.2C

ELECTRICAL CHARACTERISTICS (V_I = –10 V, I_O = 500 mA, 0°C < T_J < +125°C, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	–5.0	–5.2	–5.4	Vdc
Line Regulation (Note 1)	Reg_{line}				mV
(T_J = +25°C, I_O = 100 mA)					
–7.2 Vdc ≥ V_I ≥ –25 Vdc		–	8.0	52	
–8.0 Vdc ≥ V_I ≥ –12 Vdc		–	2.2	27	
(T_J = +25°C, I_O = 500 mA)					
–7.2 Vdc ≥ V_I ≥ –25 Vdc		–	37	105	
–8.0 Vdc ≥ V_I ≥ –12 Vdc		–	8.5	52	
Load Regulation, T_J = +25°C (Note 1)	Reg_{load}				mV
5.0 mA ≤ I_O ≤ 1.5 A		–	12	105	
250 mA ≤ I_O ≤ 750 mA		–	4.5	52	
Output Voltage –7.2 Vdc ≥ V_I ≥ –20 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P ≤ 15 W	V_O	–4.95	–	–5.45	Vdc
Input Bias Current (T_J = +25°C)	I_{IB}	–	4.3	8.0	mA
Input Bias Current Change	ΔI_{IB}				mA
–7.2 Vdc ≥ V_I ≥ –25 Vdc		–	–	1.3	
5.0 mA ≤ I_O ≤ 1.5 A		–	–	0.5	
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	–	42	–	µV
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	–	68	–	dB
Dropout Voltage I_O = 1.0 A, T_J = +25°C	V_I–V_O	–	2.0	–	Vdc
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA, 0°C ≤ T_J ≤ +125°C	$\Delta V_O/\Delta T$	–	–1.0	–	mV/°C

NOTE: 1. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

MC7906C
ELECTRICAL CHARACTERISTICS (V_I = –11 V, I_O = 500 mA, 0°C < T_J < +125°C, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	–5.75	–6.0	–6.25	Vdc
Line Regulation (Note 1)	Reg_{line}				mV
(T_J = +25°C, I_O = 100 mA)					
–8.0 Vdc ≥ V_I ≥ –25 Vdc		–	9.0	60	
–9.0 Vdc ≥ V_I ≥ –13 Vdc		–	3.0	30	
(T_J = +25°C, I_O = 500 mA)					
–8.0 Vdc ≥ V_I ≥ –25 Vdc		–	43	120	
–9.0 Vdc ≥ V_I ≥ –13 Vdc		–	10	60	
Load Regulation, T_J = +25°C (Note 1)	Reg_{load}				mV
5.0 mA ≤ I_O ≤ 1.5 A		–	13	120	
250 mA ≤ I_O ≤ 750 mA		–	5.0	60	
Output Voltage	V_O				Vdc
–8.0 Vdc ≥ V_I ≥ –21 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P ≤ 15 W		–5.7	–	–6.3	
Input Bias Current (T_J = +25°C)	I_{IB}	–	4.3	8.0	mA
Input Bias Current Change	ΔI_{IB}				mA
–8.0 Vdc ≥ V_I ≥ –25 Vdc		–	–	1.3	
5.0 mA ≤ I_O ≤ 1.5 A		–	–	0.5	
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	–	45	–	µV
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	–	65	–	dB
Dropout Voltage	$V_I–V_O$				Vdc
I_O = 1.0 A, T_J = +25°C		–	2.0	–	
Average Temperature Coefficient of Output Voltage	$\Delta V_O/\Delta T$				mV/°C
I_O = 5.0 A, 0°C ≤ T_J ≤ +125°C		–	–1.0	–	

MC7908C
ELECTRICAL CHARACTERISTICS (V_I = –14 V, I_O = 500 mA, 0°C < T_J < +125°C, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	–7.7	–8.0	–8.3	Vdc
Line Regulation (Note 1)	Reg_{line}				mV
(T_J = +25°C, I_O = 100 mA)					
–10.5 Vdc ≥ V_I ≥ –25 Vdc		–	12	80	
–11 Vdc ≥ V_I ≥ –17 Vdc		–	5.0	40	
(T_J = +25°C, I_O = 500 mA)					
–10.5 Vdc ≥ V_I ≥ –25 Vdc		–	50	160	
–11 Vdc ≥ V_I ≥ –17 Vdc		–	22	80	
Load Regulation, T_J = +25°C (Note 1)	Reg_{load}				mV
5.0 mA ≤ I_O ≤ 1.5 A		–	26	160	
250 mA ≤ I_O ≤ 750 mA		–	9.0	80	
Output Voltage	V_O				Vdc
–10.5 Vdc ≥ V_I ≥ –23 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P ≤ 15 W		–7.6	–	–8.4	
Input Bias Current (T_J = +25°C)	I_{IB}	–	4.3	8.0	mA
Input Bias Current Change	ΔI_{IB}				mA
–10.5 Vdc ≥ V_I ≥ –25 Vdc		–	–	1.0	
5.0 mA ≤ I_O ≤ 1.5 A		–	–	0.5	
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	–	52	–	µV
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	–	62	–	dB
Dropout Voltage	$V_I–V_O$				Vdc
I_O = 1.0 A, T_J = +25°C		–	2.0	–	
Average Temperature Coefficient of Output Voltage	$\Delta V_O/\Delta T$				mV/°C
I_O = 5.0 mA, 0°C ≤ T_J ≤ +125°C		–	–1.0	–	

NOTE: 1. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

MC7912C

ELECTRICAL CHARACTERISTICS (V_I = –19 V, I_O = 500 mA, 0°C < T_J < +125°C, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	–11.5	–12	–12.5	Vdc
Line Regulation (Note 1)	Reg_{line}				mV
(T_J = +25°C, I_O = 100 mA)					
–14.5 Vdc ≥ V_I ≥ –30 Vdc		–	13	120	
–16 Vdc ≥ V_I ≥ –22 Vdc		–	6.0	60	
(T_J = +25°C, I_O = 500 mA)					
–14.5 Vdc ≥ V_I ≥ –30 Vdc		–	55	240	
–16 Vdc ≥ V_I ≥ –22 Vdc		–	24	120	
Load Regulation, T_J = +25°C (Note 1)	Reg_{load}				mV
5.0 mA ≤ I_O ≤ 1.5 A		–	46	240	
250 mA ≤ I_O ≤ 750 mA		–	17	120	
Output Voltage	V_O				Vdc
–14.5 Vdc ≥ V_I ≥ –27 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P ≤ 15 W		–11.4	–	–12.6	
Input Bias Current (T_J = +25°C)	I_{IB}	–	4.4	8.0	mA
Input Bias Current Change	ΔI_{IB}				mA
–14.5 Vdc ≥ V_I ≥ –30 Vdc		–	–	1.0	
5.0 mA ≤ I_O ≤ 1.5 A		–	–	0.5	
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	–	75	–	µV
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	–	61	–	dB
Dropout Voltage	$V_I–V_O$				Vdc
I_O = 1.0 A, T_J = +25°C		–	2.0	–	
Average Temperature Coefficient of Output Voltage	$\Delta V_O/\Delta T$				mV/°C
I_O = 5.0 mA, 0°C ≤ T_J ≤ +125°C		–	–1.0	–	

MC7912AC

ELECTRICAL CHARACTERISTICS (V_I = –19 V, I_O = 500 mA, 0°C < T_J < +125°C, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	–11.75	–12	–12.25	Vdc
Line Regulation (Note 1)	Reg_{line}				mV
–16 Vdc ≥ V_I ≥ –22 Vdc; I_O = 1.0 A, T_J = +25°C		–	6.0	60	
–16 Vdc ≥ V_I ≥ –22 Vdc; I_O = 1.0 A		–	24	120	
–14.8 Vdc ≥ V_I ≥ –30 Vdc; I_O = 500 mA		–	24	120	
–14.5 Vdc ≥ V_I ≥ –27 Vdc; I_O = 1.0 A, T_J = +25°C		–	13	120	
Load Regulation (Note 1)	Reg_{load}				mV
5.0 mA ≤ I_O ≤ 1.5 A, T_J = +25°C		–	46	150	
250 mA ≤ I_O ≤ 750 mA		–	17	75	
5.0 mA ≤ I_O ≤ 1.0 A		–	35	150	
Output Voltage	V_O				Vdc
–14.8 Vdc ≥ V_I ≥ –27 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P ≤ 15 W		–11.5	–	–12.5	
Input Bias Current	I_{IB}	–	4.4	8.0	mA
Input Bias Current Change	ΔI_{IB}				mA
–15 Vdc ≥ V_I ≥ –30 Vdc		–	–	0.8	
5.0 mA ≤ I_O ≤ 1.0 A		–	–	0.5	
5.0 mA ≤ I_O ≤ 1.5 A, T_J = +25°C		–	–	0.5	
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	–	75	–	µV
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	–	61	–	dB
Dropout Voltage	$V_I–V_O$				Vdc
I_O = 1.0 A, T_J = +25°C		–	2.0	–	
Average Temperature Coefficient of Output Voltage	$\Delta V_O/\Delta T$				mV/°C
I_O = 5.0 A, 0°C ≤ T_J ≤ +125°C		–	–1.0	–	

NOTE: 1. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

MC7915C

ELECTRICAL CHARACTERISTICS (V_I = –23 V, I_O = 500 mA, 0°C < T_J < +125°C, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	–14.4	–15	–15.6	Vdc
Line Regulation (Note 1)	Reg_{line}				mV
(T_J = +25°C, I_O = 100 mA)					
–17.5 Vdc ≥ V_I ≥ –30 Vdc		–	14	150	
–20 Vdc ≥ V_I ≥ –26 Vdc		–	6.0	75	
(T_J = +25°C, I_O = 500 mA)					
–17.5 Vdc ≥ V_I ≥ –30 Vdc		–	57	300	
–20 Vdc ≥ V_I ≥ –26 Vdc		–	27	150	
Load Regulation, T_J = +25°C (Note 1)	Reg_{load}				mV
5.0 mA ≤ I_O ≤ 1.5 A		–	68	300	
250 mA ≤ I_O ≤ 750 mA		–	25	150	
Output Voltage	V_O				Vdc
–17.5 Vdc ≥ V_I ≥ –30 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P ≤ 15 W		–14.25	–	–15.75	
Input Bias Current (T_J = +25°C)	I_{IB}	–	4.4	8.0	mA
Input Bias Current Change	ΔI_{IB}				mA
–17.5 Vdc ≥ V_I ≥ –30 Vdc		–	–	1.0	
5.0 mA ≤ I_O ≤ 1.5 A		–	–	0.5	
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	–	90	–	µV
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	–	60	–	dB
Dropout Voltage	$V_I–V_O$				Vdc
I_O = 1.0 A, T_J = +25°C		–	2.0	–	
Average Temperature Coefficient of Output Voltage	$\Delta V_O/\Delta T$				mV/°C
I_O = 5.0 A, 0°C ≤ T_J ≤ +125°C		–	–1.0	–	

MC7915AC

ELECTRICAL CHARACTERISTICS (V_I = –23 V, I_O = 500 mA, 0°C < T_J < +125°C, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	–14.7	–15	–15.3	Vdc
Line Regulation (Note 1)	Reg_{line}				mV
–20 Vdc ≥ V_I ≥ –26 Vdc, I_O = 1.0 A, T_J = +25°C		–	27	75	
–20 Vdc ≥ V_I ≥ –26 Vdc, I_O = 1.0 A,		–	57	150	
–17.9 Vdc ≥ V_I ≥ –30 Vdc, I_O = 500 mA		–	57	150	
–17.5 Vdc ≥ V_I ≥ –30 Vdc, I_O = 1.0 A, T_J = +25°C		–	57	150	
Load Regulation (Note 1)	Reg_{load}				mV
5.0 mA ≤ I_O ≤ 1.5 A, T_J = +25°C		–	68	150	
250 mA ≤ I_O ≤ 750 mA		–	25	75	
5.0 mA ≤ I_O ≤ 1.0 A		–	40	150	
Output Voltage	V_O				Vdc
–17.9 Vdc ≥ V_I ≥ –30 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P ≤ 15 W		–14.4	–	–15.6	
Input Bias Current	I_{IB}	–	4.4	8.0	mA
Input Bias Current Change	ΔI_{IB}				mA
–17.5 Vdc ≥ V_I ≥ –30 Vdc		–	–	0.8	
5.0 mA ≤ I_O ≤ 1.0 A		–	–	0.5	
5.0 mA ≤ I_O ≤ 1.5 A, T_J = +25°C		–	–	0.5	
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	–	90	–	µV
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	–	60	–	dB
Dropout Voltage	$V_I–V_O$				Vdc
I_O = 1.0 A, T_J = +25°C		–	2.0	–	
Average Temperature Coefficient of Output Voltage	$\Delta V_O/\Delta T$				mV/°C
I_O = 5.0 mA, 0°C ≤ T_J ≤ +125°C		–	–1.0	–	

NOTE: 1. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

MC7918C

ELECTRICAL CHARACTERISTICS (V_I = –27 V, I_O = 500 mA, 0°C < T_J < +125°C, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	–17.3	–18	–18.7	Vdc
Line Regulation (Note 1)	Reg_{line}				mV
(T_J = +25°C, I_O = 100 mA)					
–21 Vdc ≥ V_I ≥ –33 Vdc		–	25	180	
–24 Vdc ≥ V_I ≥ –30 Vdc		–	10	90	
(T_J = +25°C, I_O = 500 mA)					
–21 Vdc ≥ V_I ≥ –33 Vdc		–	90	360	
–24 Vdc ≥ V_I ≥ –30 Vdc		–	50	180	
Load Regulation, T_J = +25°C (Note 1)	Reg_{load}				mV
5.0 mA ≤ I_O ≤ 1.5 A		–	110	360	
250 mA ≤ I_O ≤ 750 mA		–	55	180	
Output Voltage	V_O				Vdc
–21 Vdc ≥ V_I ≥ –33 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P ≤ 15 W		–17.1	–	–18.9	
Input Bias Current (T_J = +25°C)	I_{IB}	–	4.5	8.0	mA
Input Bias Current Change	ΔI_{IB}				mA
–21 Vdc ≥ V_I ≥ –33 Vdc		–	–	1.0	
5.0 mA ≤ I_O ≤ 1.5 A		–	–	0.5	
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	–	110	–	µV
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	–	59	–	dB
Dropout Voltage	V_I–V_O				Vdc
I_O = 1.0 A, T_J = +25°C		–	2.0	–	
Average Temperature Coefficient of Output Voltage	$\Delta V_O/\Delta T$				mV/°C
I_O = 5.0 mA, 0°C ≤ T_J ≤ +125°C		–	–1.0	–	

MC7924C

ELECTRICAL CHARACTERISTICS (V_I = –33 V, I_O = 500 mA, 0°C < T_J < +125°C, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	–23	–24	–25	Vdc
Line Regulation (Note 1)	Reg_{line}				mV
(T_J = +25°C, I_O = 100 mA)					
–27 Vdc ≥ V_I ≥ –38 Vdc		–	31	240	
–30 Vdc ≥ V_I ≥ –36 Vdc		–	14	120	
(T_J = +25°C, I_O = 500 mA)					
–27 Vdc ≥ V_I ≥ –38 Vdc		–	118	470	
–30 Vdc ≥ V_I ≥ –36 Vdc		–	70	240	
Load Regulation, T_J = +25°C (Note 1)	Reg_{load}				mV
5.0 mA ≤ I_O ≤ 1.5 A		–	150	480	
250 mA ≤ I_O ≤ 750 mA		–	85	240	
Output Voltage	V_O				Vdc
–27 Vdc ≥ V_I ≥ –38 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P ≤ 15 W		–22.8	–	–25.2	
Input Bias Current (T_J = +25°C)	I_{IB}	–	4.6	8.0	mA
Input Bias Current Change	ΔI_{IB}				mA
–27 Vdc ≥ V_I ≥ –38 Vdc		–	–	1.0	
5.0 mA ≤ I_O ≤ 1.5 A		–	–	0.5	
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	–	170	–	µV
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	–	56	–	dB
Dropout Voltage	V_I–V_O				Vdc
I_O = 1.0 A, T_J = +25°C		–	2.0	–	
Average Temperature Coefficient of Output Voltage	$\Delta V_O/\Delta T$				mV/°C
I_O = 5.0 mA, 0°C ≤ T_J ≤ +125°C		–	–1.0	–	

NOTE: 1. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

Figure 1. Worst Case Power Dissipation as a Function of Ambient Temperature

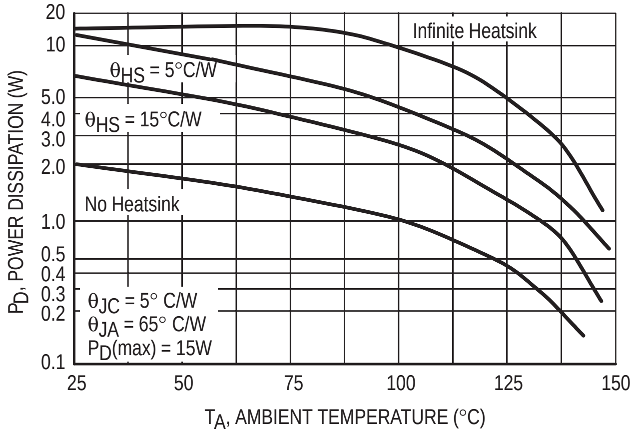


Figure 2. Peak Output Current as a Function of Input–Output Differential Voltage

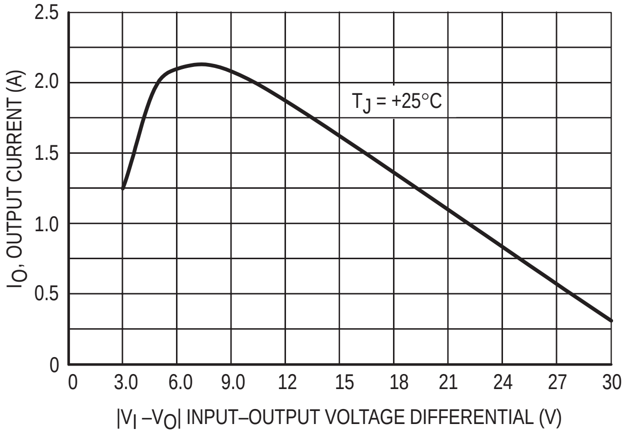


Figure 3. Ripple Rejection as a Function of Frequency

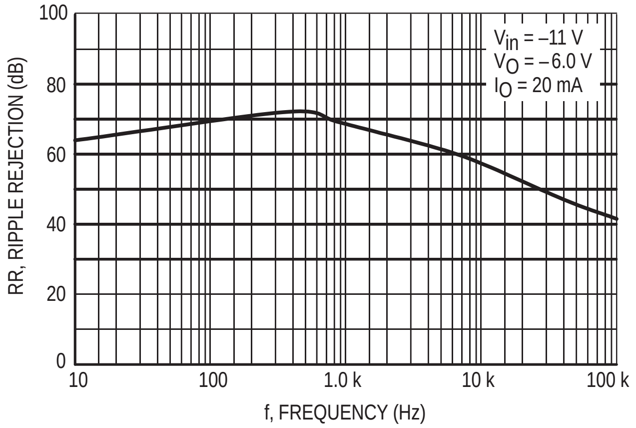


Figure 4. Ripple Rejection as a Function of Output Voltage

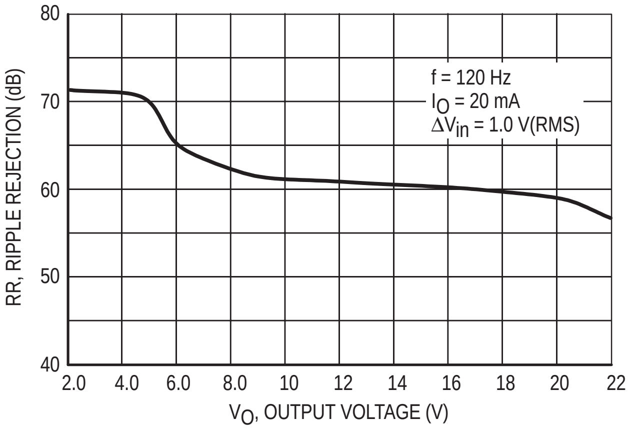


Figure 5. Output Voltage as a Function of Junction Temperature

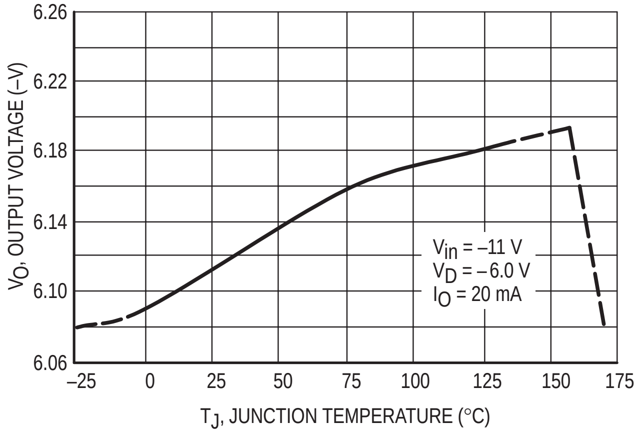
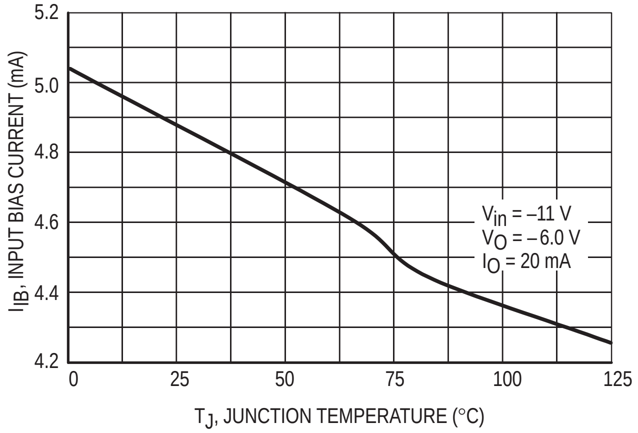


Figure 6. Quiescent Current as a Function of Temperature



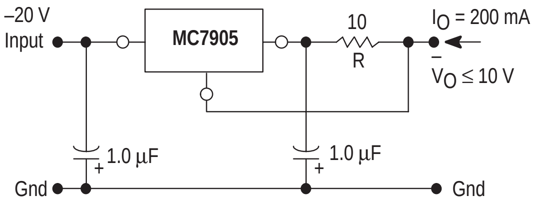
APPLICATIONS INFORMATION

Design Considerations

The MC7900 Series of fixed voltage regulators are designed with Thermal overload Protection that shuts down the circuit when subjected to an excessive power overload condition. Internal Short Circuit Protection that limits the maximum current the circuit will pass, and Output Transistor Safe–Area Compensation that reduces the output short circuit current as the voltage across the pass transistor is increased.

In many low current applications, compensation capacitors are not required. However, it is recommended that the regulator input be bypassed with a capacitor if the regulator is connected to the power supply filter with long wire lengths, or if the output load capacitance is large. An input bypass capacitor should be selected to provide good high–frequency characteristics to insure stable operation under all load conditions. A 0.33 µF or larger tantalum, mylar, or other capacitor having low internal impedance at high frequencies should be chosen. The capacitor chosen should have an equivalent series resistance of less than 0.7 Ω. The bypass capacitor should be mounted with the shortest possible leads directly across the regulators input terminals. Normally good construction techniques should be used to minimize ground loops and lead resistance drops since the regulator has no external sense lead. Bypassing the output is also recommended.

Figure 7. Current Regulator



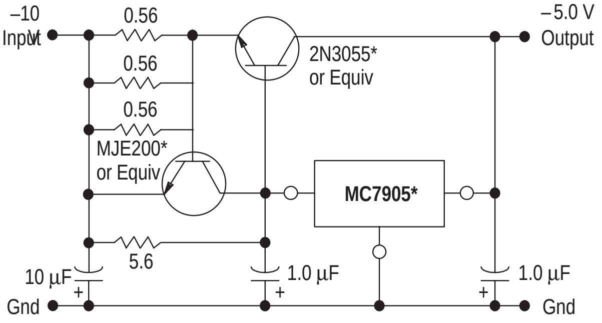
The MC7905, –5.0 V regulator can be used as a constant current source when connected as above. The output current is the sum of resistor R current and quiescent bias current as follows.

$$I_O = \frac{5.0\ V}{R} + I_B$$

The quiescent current for this regulator is typically 4.3 mA. The 5.0 V regulator was chosen to minimize dissipation and to allow the output voltage to operate to within 6.0 V below the input voltage.

Figure 8. Current Boost Regulator

(–5.0 V @ 4.0 A, with 5.0 A Current Limiting)

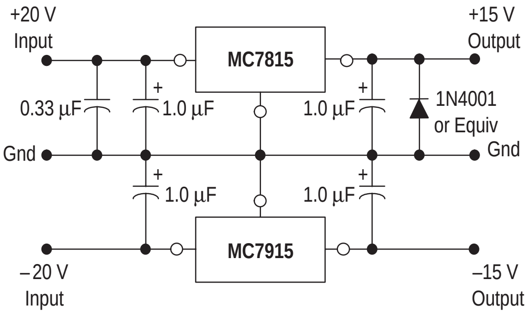


*Mounted on heatsink.

When a boost transistor is used, short circuit currents are equal to the sum of the series pass and regulator limits, which are measured at 3.2 A and 1.8 A respectively in this case. Series pass limiting is approximately equal to 0.6 V/R_{SC}. Operation beyond this point to the peak current capability of the MC7905C is possible if the regulator is mounted on a heatsink; otherwise thermal shutdown will occur when the additional load current is picked up by the regulator.

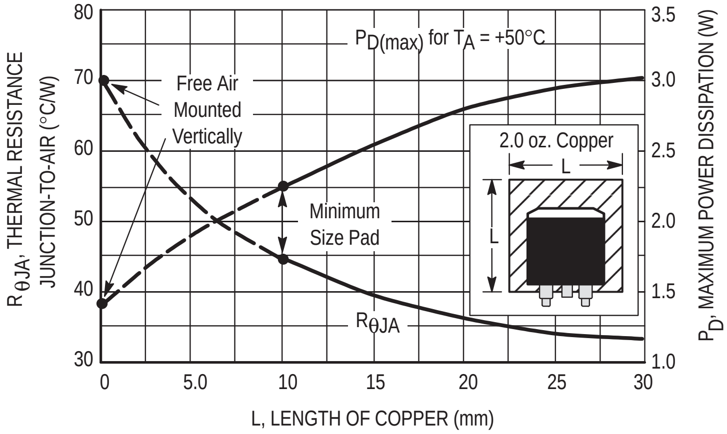
Figure 9. Operational Amplifier Supply

(±15 @ 1.0 A)



The MC7815 and MC7915 positive and negative regulators may be connected as shown to obtain a dual power supply for operational amplifiers. A clamp diode should be used at the output of the MC7815 to prevent potential latch–up problems whenever the output of the positive regulator (MC7815) is drawn below ground with an output current greater than 200 mA.

Figure 10. D^2PAK Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length



DEFINITIONS

Line Regulation – The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

Load Regulation – The change in output voltage for a change in load current at constant chip temperature.

Maximum Power Dissipation – The maximum total device dissipation for which the regulator will operate within specifications.

Input Bias Current – That part of the input current that is not delivered to the load.

Output Noise Voltage – The rms AC voltage at the output, with constant load and no input ripple, measured over a specified frequency range.

Long Term Stability – Output voltage stability under accelerated life test conditions with the maximum rated voltage listed in the devices' electrical characteristics and maximum power dissipation.

MOTOROLA

MC79L00, A Series

Three-Terminal Low Current Negative Voltage Regulators

The MC79L00, A Series negative voltage regulators are inexpensive, easy–to–use devices suitable for numerous applications requiring up to100 mA. Like the higher powered MC7900 Series negative regulators, this series features thermal shutdown and current limiting, making them remarkably rugged. In most applications, no external components are required for operation.

The MC79L00 devices are useful for on–card regulation or any other application where a regulated negative voltage at a modest current level is needed. These regulators offer substantial advantage over the common resistor/zener diode approach.

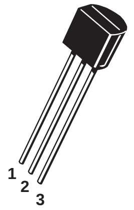
- No External Components Required
- Internal Short Circuit Current Limiting
- Internal Thermal Overload Protection
- Low Cost
- Complementary Positive Regulators Offered (MC78L00 Series)
- Available in Either ±5% (AC) or ±10% (C) Selections

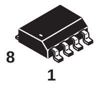
THREE–TERMINAL LOW CURRENT NEGATIVE FIXED VOLTAGE REGULATORS

SEMICONDUCTOR
TECHNICAL DATA

P SUFFIX
PLASTIC PACKAGE
CASE 29

Pin 1. Ground
2. Input
3. Output





D SUFFIX
PLASTIC PACKAGE
CASE 751
(SOP–8)*

Pin		
1. V_{out}	5. GND
2. V_{in}	6. V_{in}
3. V_{in}	7. V_{in}
4. NC	8. NC

* SOP–8 is an internally modified SO–8 package. Pins 2, 3, 6, and 7 are electrically common to the die attach flag. This internal lead frame modification decreases package thermal resistance and increases power dissipation capability when appropriately mounted on a printed circuit board. SOP–8 conforms to all external dimensions of the standard SO–8 package.

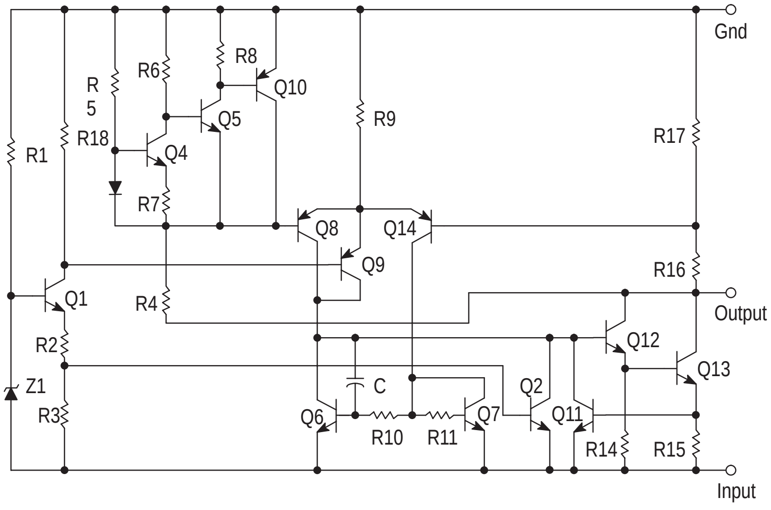
Device No. ±10%	Device No. 5%	Nominal Voltage
MC79L05C	MC79L05AC	–5.0
MC79L12C	MC79L12AC	–12
MC79L15C	MC79L15AC	–15
MC79L18C	MC79L18AC	–18
MC79L24C	MC79L24AC	–24

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC79LXXACD*	T_J = 0° to +125°C	SOP–8
MC79LXXACP		Plastic Power
MC79LXXCP		Plastic Power
MC79LXXABD*	T_J = –40° to +125°C	SOP–8
MC79LXXABP*		Plastic Power

XX indicates nominal voltage

Representative Schematic Diagram



* Automotive temperature range selections are available with special test conditions and additional tests in 5, 12 and 15 V devices. Contact your local Motorola sales office for information.

MAXIMUM RATINGS (T_A = +25°C, unless otherwise noted.)

Rating	Symbol	Value	Unit
Input Voltage (–5 V) (–12, –15, –18 V) (–24 V)	V_I	–30 –35 –40	Vdc
Storage Temperature Range	T_{stg}	–65 to +150	°C
Junction Temperature	T_J	+150	°C

ELECTRICAL CHARACTERISTICS (V_I = –10 V, I_O = 40 mA, C_I = 0.33 µF, C_O = 0.1 µF, –40°C < T_J +125°C (for MC79LXXAB), 0°C < T_J < +125°C (for MC79LXXAC)).

Characteristics	Symbol	MC79L05C, AB			MC79L05AC, AB			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	–4.6	–5.0	–5.4	–4.8	–5.0	–5.2	Vdc
Input Regulation (T_J = +25°C)	Reg_{line}							mV
–7.0 Vdc ≥ V_I ≥ –20 Vdc		–	–	200	–	–	150	
–8.0 Vdc ≥ V_I ≥ –20 Vdc		–	–	150	–	–	100	
Load Regulation	Reg_{load}							mV
T_J = +25°C, 1.0 mA ≤ I_O ≤ 100 mA		–	–	60	–	–	60	
1.0 mA ≤ I_O ≤ 40 mA		–	–	30	–	–	30	
Output Voltage	V_O							Vdc
–7.0 Vdc ≥ V_I ≥ –20 Vdc, 1.0 mA ≤ I_O ≤ 40 mA		–4.5	–	–5.5	–4.75	–	–5.25	
V_I = –10 Vdc, 1.0 mA ≤ I_O ≤ 70 mA		–4.5	–	–5.5	–4.75	–	–5.25	
Input Bias Current	I_{IB}							mA
(T_J = +25°C)		–	–	6.0	–	–	6.0	
(T_J = +125°C)		–	–	5.5	–	–	5.5	
Input Bias Current Change	I_{IB}							mA
–8.0 Vdc ≥ V_I ≥ –20 Vdc		–	–	1.5	–	–	1.5	
1.0 mA ≤ I_O ≤ 40 mA		–	–	0.2	–	–	0.1	
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	–	40	–	–	40	–	µV
Ripple Rejection (–8.0 ≥ V_I ≥ –18 Vdc, f = 120 Hz, T_J = +25°C)	RR	40	49	–	41	49	–	dB
Dropout Voltage (I_O = 40 mA, T_J = +25°C)	$\lvert V_I – V_O \rvert$	–	1.7	–	–	1.7	–	Vdc

ELECTRICAL CHARACTERISTICS (V_I = –19 V, I_O = 40 mA, C_I = 0.33 µF, C_O = 0.1 µF, –40°C < T_J +125°C (for MC79LXXAC), 0°C < T_J < +125°C (for MC79LXXAB)).

Characteristics	Symbol	MC79L12C, AB			MC79L12AC, AB			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	–11.1	–12	–12.9	–11.5	–12	–12.5	Vdc
Input Regulation (T_J = +25°C)	Reg_{line}							mV
–14.5 Vdc ≥ V_I ≥ –27 Vdc		–	–	250	–	–	250	
–16 Vdc ≥ V_I ≥ –27 Vdc		–	–	200	–	–	200	
Load Regulation	Reg_{load}							mV
T_J = +25°C, 1.0 mA ≤ I_O ≤ 100 mA		–	–	100	–	–	100	
1.0 mA ≤ I_O ≤ 40 mA		–	–	50	–	–	50	
Output Voltage	V_O							Vdc
–14.5 Vdc ≥ V_I ≥ –27 Vdc, 1.0 mA ≤ I_O ≤ 40 mA		–10.8	–	–13.2	–11.4	–	–12.6	
V_I = –19 Vdc, 1.0 mA ≤ I_O ≤ 70 mA		–10.8	–	–13.2	–11.4	–	–12.6	
Input Bias Current	I_{IB}							mA
(T_J = +25°C)		–	–	6.5	–	–	6.5	
(T_J = +125°C)		–	–	6.0	–	–	6.0	
Input Bias Current Change	I_{IB}							mA
–16 Vdc ≥ V_I ≥ –27 Vdc		–	–	1.5	–	–	1.5	
1.0 mA ≤ I_O ≤ 40 mA		–	–	0.2	–	–	0.2	
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	–	80	–	–	80	–	µV
Ripple Rejection (–15 ≤ V_I ≤ –25 Vdc, f = 120 Hz, T_J = +25°C)	RR	36	42	–	37	42	–	dB
Dropout Voltage (I_O = 40 mA, T_J = +25°C)	$\lvert V_I – V_O \rvert$	–	1.7	–	–	1.7	–	Vdc

ELECTRICAL CHARACTERISTICS (V_I = –23 V, I_O = 40 mA, C_I = 0.33 µF, C_O = 0.1 µF, –40°C < T_J +125°C (for MC79LXXAB), 0°C < T_J < +125°C (for MC79LXXAC)).

Characteristics	Symbol	MC79L15C			MC79L15AC, AB			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	–13.8	–15	–16.2	–14.4	–15	–15.6	Vdc
Input Regulation (T_J = +25°C) –17.5 Vdc ≥ V_I ≥ –30 Vdc –20 Vdc ≥ V_I ≥ –30 Vdc	Reg_{line}	 – –	 – –	 300 250	 – –	 – –	 300 250	mV
Load Regulation T_J = +25°C, 1.0 mA ≤ I_O ≤ 100 mA 1.0 mA ≤ I_O ≤ 40 mA	Reg_{load}	 – –	 – –	 150 75	 – –	 – –	 150 75	mV
Output Voltage –17.5 Vdc ≥ V_I ≥ –Vdc, 1.0 mA ≤ I_O ≤ 40 mA V_I = –23 Vdc, 1.0 mA ≤ I_O ≤ 70 mA	V_O	 –13.5 –13.5	 – –	 –16.5 –16.5	 –14.25 –14.25	 – –	 –15.75 –15.75	Vdc
Input Bias Current (T_J = +25°C) (T_J = +125°C)	I_{IB}	 – –	 – –	 6.5 6.0	 – –	 – –	 6.5 6.0	mA
Input Bias Current Change –20 Vdc ≥ V_I ≥ –30 Vdc 1.0 mA ≤ I_O ≤ 40 mA	ΔI_{IB}	 – –	 – –	 1.5 0.2	 – –	 – –	 1.5 0.1	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_N	–	90	–	–	90	–	µV
Ripple Rejection (–18.5 ≤ V_I ≤ –28.5 Vdc, f = 120 Hz)	RR	33	39	–	34	39	–	dB
Dropout Voltage I_O = 40 mA, T_J = +25°C	$\lvert V_I – V_O \rvert$	–	1.7	–	–	1.7	–	Vdc

ELECTRICAL CHARACTERISTICS (V_I = –27 V, I_O = 40 mA, C_I = 0.33 µF, C_O = 0.1 µF, 0°C < T_J > +125°C, unless otherwise noted).

Characteristics	Symbol	MC79L18C			MC79L18AC			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	–16.6	–18	–19.4	–17.3	–18	–18.7	Vdc
Input Regulation (T_J = +25°C) –20.7 Vdc ≥ V_I ≥ –33 Vdc –21.4 Vdc ≥ V_I ≥ –33 Vdc –22 Vdc ≥ V_I ≥ –33 Vdc –21 Vdc ≥ V_I ≥ –33 Vdc	Reg_{line}	 – – – –	 – – – –	 – 325 275 –	 – – – –	 – – – –	 325 – – 275	mV
Load Regulation T_J = +25°C, 1.0 mA ≤ I_O ≤ 100 mA 1.0 mA ≤ I_O ≤ 40 mA	Reg_{load}	 – –	 – –	 170 85	 – –	 – –	 170 85	mV
Output Voltage –20.7 Vdc ≥ V_I ≥ –33 Vdc, 1.0 mA ≤ I_O ≤ 40 mA –21.4 Vdc ≥ V_I ≥ –33 Vdc, 1.0 mA ≤ I_O ≤ 40 mA V_I = –27 Vdc, 1.0 mA ≤ I_O ≤ 70 mA	V_O	 – –16.2 –16.2	 – – –	 – –19.8 –19.8	 –17.1 – –17.1	 – – –	 –18.9 – –18.9	Vdc
Input Bias Current (T_J = +25°C) (T_J = +125°C)	I_{IB}	 – –	 – –	 6.5 6.0	 – –	 – –	 6.5 6.0	mA
Input Bias Current Change –21 Vdc ≥ V_I ≥ –33 Vdc –27 Vdc ≥ V_I ≥ –33 Vdc 1.0 mA ≤ I_O ≤ 40 mA	I_{IB}	 – – –	 – – –	 – 1.5 0.2	 – – –	 – – –	 1.5 – 0.1	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	–	150	–	–	150	–	µV
Ripple Rejection (–23 ≤ V_I ≤ –33 Vdc, f = 120 Hz, T_J = +25°C)	RR	32	46	–	33	48	–	dB
Dropout Voltage I_O = 40 mA, T_J = +25°C	$\lvert V_I – V_O \rvert$	–	1.7	–	–	1.7	–	Vdc

ELECTRICAL CHARACTERISTICS (V_I = –33 V, I_O = 40 mA, C_I = 0.33 µF, C_O = 0.1 µF, 0°C < T_J < +125°C, unless otherwise noted).

Characteristics	Symbol	MC79L24C			MC79L24AC			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	–22.1	–24	–25.9	–23	–24	–25	Vdc
Input Regulation	Reg_{line}							mV
(T_J = +25°C)								
–27 Vdc ≥ V_I ≥ –38 Vdc		–	–	–	–	–	350	
–27.5 Vdc ≥ V_I ≥ –38 Vdc		–	–	350	–	–	–	
–28 Vdc ≥ V_I ≥ –38 Vdc		–	–	300	–	–	300	
Load Regulation	Reg_{load}							mV
T_J = +25°C, 1.0 mA ≤ I_O ≤ 100 mA		–	–	200	–	–	200	
1.0 mA ≤ I_O ≤ 40 mA		–	–	100	–	–	100	
Output Voltage	V_O							Vdc
–27 Vdc ≥ V_I ≥ –38 V, 1.0 mA ≤ I_O ≤ 40 mA		–	–	–	–22.8	–	–25.2	
–28 Vdc ≥ V_I ≥ –38 Vdc, 1.0 mA ≤ I_O ≤ 40 mA		–21.4	–	–26.4	–	–	–	
V_I = –33 Vdc, 1.0 mA ≤ I_O ≤ 70 mA		–21.4	–	–26.4	–22.8	–	–25.2	
Input Bias Current	I_{IB}							mA
(T_J = +25°C)		–	–	6.5	–	–	6.5	
(T_J = +125°C)		–	–	6.0	–	–	6.0	
Input Bias Current Change	ΔI_{IB}							mA
–28 Vdc ≥ V_I ≥ –38 Vdc		–	–	1.5	–	–	1.5	
1.0 mA ≤ I_O ≤ 40 mA		–	–	0.2	–	–	0.1	
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	–	200	–	–	200	–	µV
Ripple Rejection (–29 ≤ V_I ≤ –35 Vdc, f = 120 Hz, T_J = +25°C)	RR	30	43	–	31	47	–	dB
Dropout Voltage I_O = 40 mA, T_J = +25°C	$\lvert V_I–V_O \rvert$	–	1.7	–	–	1.7	–	Vdc

APPLICATIONS INFORMATION

Design Considerations

The MC79L00, A Series of fixed voltage regulators are designed with Thermal Overload Protections that shuts down the circuit when subjected to an excessive power overload condition, Internal Short Circuit Protection that limits the maximum current the circuit will pass.

In many low current applications, compensation capacitors are not required. However, it is recommended that the regulator input be bypassed with a capacitor if the regulator is connected to the power supply filter with long wire length, or if the output load capacitance is large. An input bypass capacitor should be selected to provide good high–frequency characteristics to insure stable operation under all load conditions. A 0.33 µF or larger tantalum, mylar, or other capacitor having low internal impedance at high frequencies should be chosen. The bypass capacitor should be mounted with the shortest possible leads directly across the regulator's input terminals. Normally good construction techniques should be used to minimize ground loops and lead resistance drops since the regulator has no external sense lead. Bypassing the output is also recommended.

Figure 1. Positive and Negative Regulator

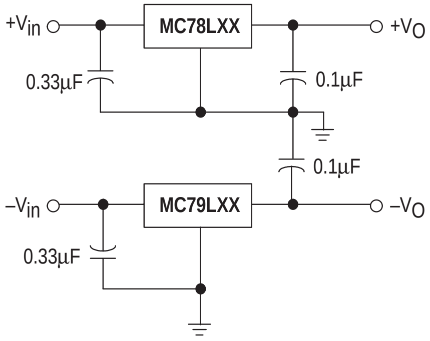
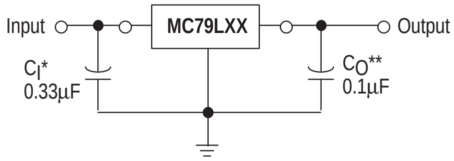


Figure 2. Standard Application



A common ground is required between the input and the output voltages. The input voltage must remain typically 2.0 V above the output voltage even during the low point on the ripple voltage.

* C_I is required if regulator is located an appreciable distance from the power supply filter

** C_O improves stability and transient response.

TYPICAL CHARACTERISTICS

(T_A = +25°C, unless otherwise noted.)

Figure 3. Dropout Characteristics

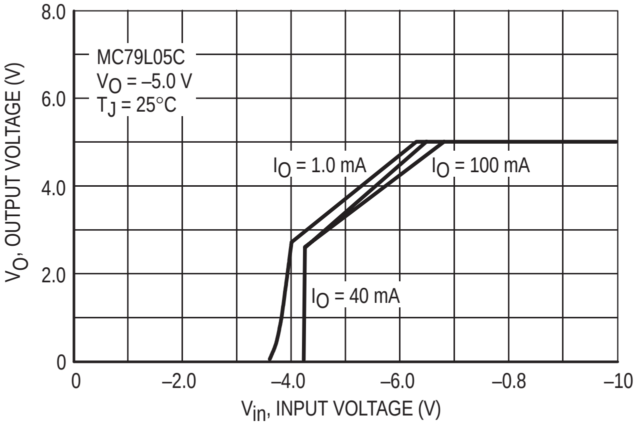


Figure 4. Dropout Voltage versus Junction Temperature

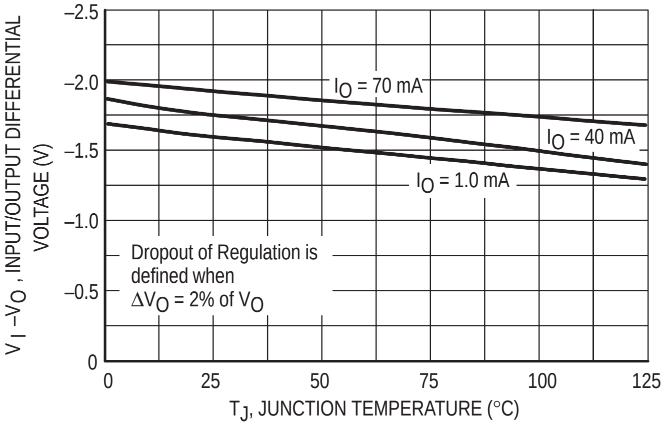


Figure 5. Input Bias Current versus Ambient Temperature

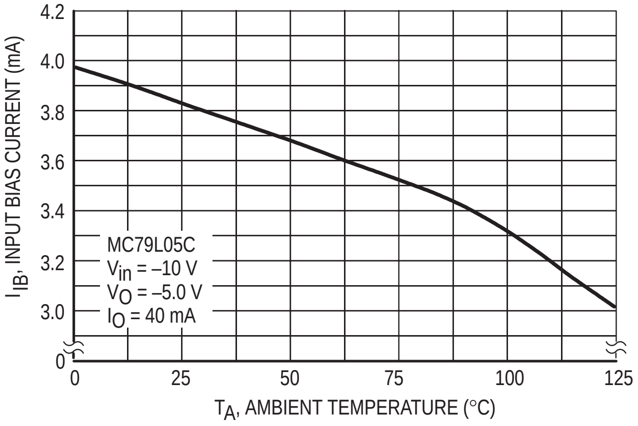


Figure 6. Input Bias Current versus Input Voltage

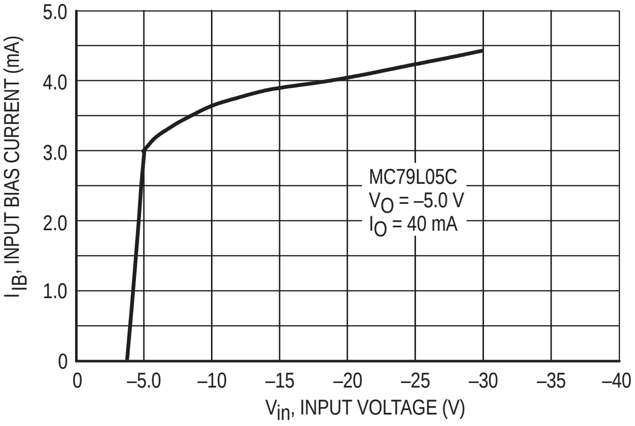


Figure 7. Maximum Average Power Dissipation versus Ambient Temperature (TO–92)

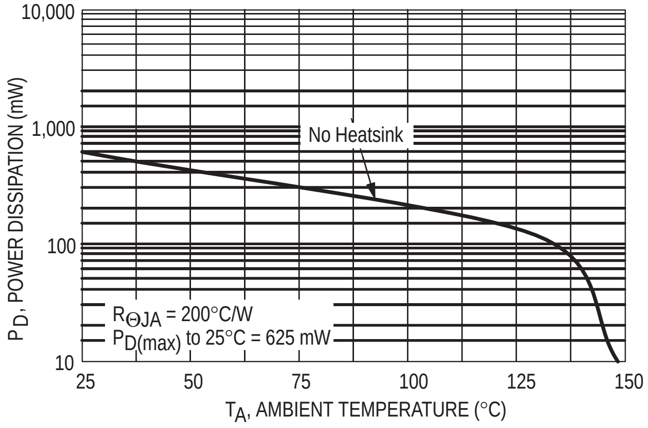
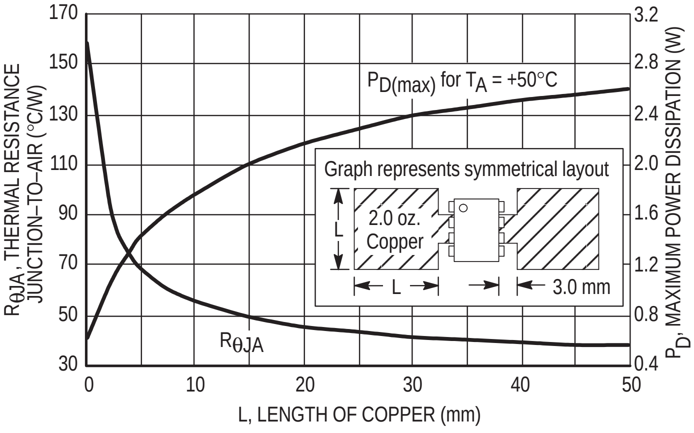


Figure 8. SOP–8 Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length



MOTOROLA

MC79M00 Series

Three-Terminal Negative Voltage Regulators

The MC79M00 series of fixed output negative voltage regulators are intended as complements to the popular MC78M00 series devices.

Available in fixed output voltage options of –5.0, –8.0, –12 and –15 V, these regulators employ current limiting, thermal shutdown, and safe–area compensation – making them remarkably rugged under most operating conditions. With adequate heatsinking they can deliver output currents in excess of 0.5 A.

- No External Components Required
- Internal Thermal Overload Protection
- Internal Short Circuit Current Limiting
- Output Transistor Safe–Area Compensation
- Also Available in Surface Mount DPAK (DT) Package

DEVICE TYPE/NOMINAL OUTPUT VOLTAGE

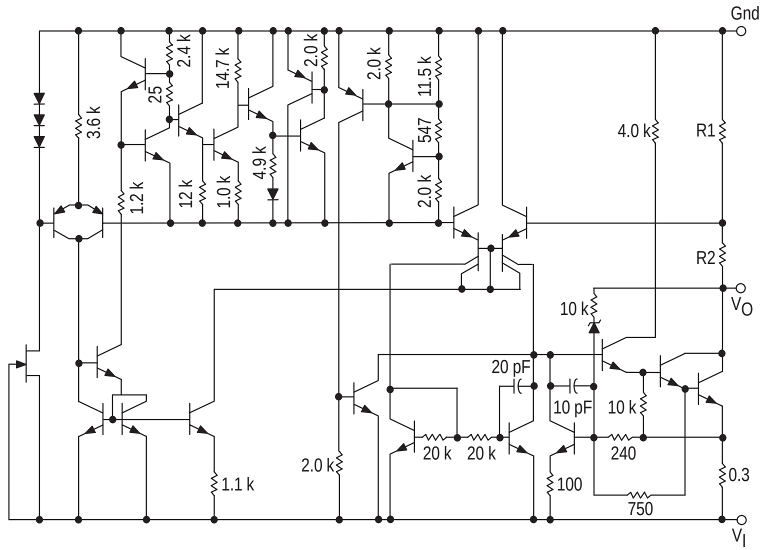
MC79M05 MC79M08	–5.0 V –8.0 V	MC79M12 MC79M15	–12 V –15 V

ORDERING INFORMATION

Device	Output Voltage Tolerance	Operating Temperature Range	Package
MC79MXXBDT, BDT–1	4.0%	T_J = –40° to +125°C	DPAK
MC79MXXBT			Plastic Power
MC79MXXCDT, CDT–1		T_J = 0° to +125°C	DPAK
MC79MXXCT			Plastic Power

XX indicates nominal voltage.

Representative Schematic Diagram

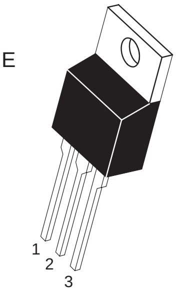


This device contains 31 active transistors.

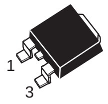
THREE–TERMINAL NEGATIVE FIXED VOLTAGE REGULATORS

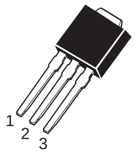
T SUFFIX
PLASTIC PACKAGE
CASE 221A

Heatsink surface
connected to Pin 2.



Pin 1. Ground
2. Input
3. Output



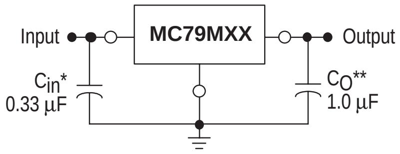


DT SUFFIX
PLASTIC PACKAGE
CASE 369A
(DPAK)

DT–1 SUFFIX
PLASTIC PACKAGE
CASE 369
(DPAK)

Heatsink surface (shown as terminal 4 in case outline drawing) is connected to Pin 2.

STANDARD APPLICATION



A common ground is required between the input and the output voltages. The input voltage must remain typically 1.1 V more negative even during the high point of the input ripple voltage.

XX, These two digits of the type number indicate nominal voltage.
* C_{in} is required if regulator is located an appreciable distance from power supply filter.
** C_O improve stability and transient response.

MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted.)

Rating	Symbol	Value	Unit
Input Voltage	V_I	–35	Vdc
Power Dissipation Case 221A T_A = 25°C Thermal Resistance, Junction–to–Ambient Thermal Resistance, Junction–to–Case Case 369 and 369A (DPAK) T_A = 25°C Thermal Resistance, Junction–to–Ambient Thermal Resistance, Junction–to–Case	 P_D θ_{JA} θ_{JC} P_D θ_{JA} θ_{JC}	 Internally Limited 65 5.0 Internally Limited 92 6.0	 W °C/W °C/W W °C/W °C/W
Storage Junction Temperature	T_{stg}	–65 to +150	°C
Junction Temperature	T_J	150	°C

NOTE: ESD data available upon request.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction–to–Ambient	$R_{\theta JA}$	65	°C/W
Thermal Resistance, Junction–to–Case	$R_{\theta JC}$	5.0	°C/W

MC79M05B, C
ELECTRICAL CHARACTERISTICS (V_I = –10 V, I_O = 350 mA, T_{low} to T_{high} [Note 2], unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = 25°C)	V_O	–4.8	–5.0	–5.2	Vdc
Line Regulation, T_J = 25°C (Note 1) –7.0 Vdc ≥ V_I ≥ –25 Vdc –8.0 Vdc ≥ V_I ≥ –18 Vdc	Reg_{line}	 – –	 7.0 2.0	 50 30	mV
Load Regulation, T_J = 25°C (Note 1) 5.0 mA ≤ I_O ≤ 500 mA	Reg_{load}	 –	 30	 100	mV
Output Voltage –7.0 Vdc ≥ V_I ≥ –25 Vdc, 5.0 mA ≤ I_O ≤ 350 mA	V_O	 –4.75	 –	 –5.25	Vdc
Input Bias Current (T_J = 25°C)	I_{IB}	–	4.3	8.0	mA
Input Bias Current Change –8.0 Vdc ≥ V_I ≥ –25 Vdc, I_O = 350 mA 5.0 mA ≤ I_O ≤ 350 mA, V_I = –10 V	ΔI_{IB}	 – –	 – –	 0.4 0.4	mA
Output Noise Voltage, T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz	V_n	–	40	–	µV
Ripple Rejection (f = 120 Hz)	RR	54	66	–	dB
Dropout Voltage I_O = 500 mA, T_J = 25°C	$V_I – V_O$	 –	 1.1	 –	Vdc
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA, 0°C ≤ T_J ≤ 125°C	$\Delta V_O/\Delta T$	 –	 0.2	 –	mV/°C

NOTES: 1. Load and line regulation are specified at constant temperature. Change in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.
2. B = T_{low} to T_{high}, –40°C < T_J < 125°C
C = T_{low} to T_{high}, 0°C < T_J < 125°C

MC79M08B, C

ELECTRICAL CHARACTERISTICS (V_I = –10 V, I_O = 350 mA, T_{low} to T_{high} [Note 2], unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = 25°C)	V_O	–7.7	–8.0	–8.3	Vdc
Line Regulation, T_J = 25°C (Note 1)	Reg_{line}				mV
–7.0 Vdc ≥ V_I ≥ –25 Vdc		–	5.0	80	
–8.0 Vdc ≥ V_I ≥ –18 Vdc		–	3.0	50	
Load Regulation, T_J = 25°C (Note 1) 5.0 mA ≤ I_O ≤ 500 mA	Reg_{load}	–	30	100	mV
Output Voltage –7.0 Vdc ≥ V_I ≥ –25 Vdc, 5.0 mA ≤ I_O ≤ 350 mA	V_O	–7.6	–8.0	–8.4	Vdc
Input Bias Current (T_J = 25°C)	I_{IB}	–	–	8.0	mA
Input Bias Current Change	ΔI_{IB}				mA
–8.0 Vdc ≥ V_I ≥ –25 Vdc, I_O = 350 mA		–	–	0.4	
5.0 mA ≤ I_O ≤ 350 mA, V_I = –10 V		–	–	0.4	
Output Noise Voltage, T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz	V_n	–	60	–	µV
Ripple Rejection (f = 120 Hz)	RR	54	63	–	dB
Dropout Voltage I_O = 500 mA, T_J = 25°C	$V_I–V_O$	–	1.1	–	Vdc
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA, 0°C ≤ T_J ≤ 125°C	$\Delta V_O/\Delta T$	–	0.4	–	mV/°C

MC79M12B, C

ELECTRICAL CHARACTERISTICS (V_I = –19 V, I_O = 350 mA, T_{low} to T_{high} [Note 2], unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = 25°C)	V_O	–11.5	–12	–12.5	Vdc
Line Regulation, T_J = 25°C (Note 1)	Reg_{line}				mV
–14.5 Vdc ≥ V_I ≥ –30 Vdc		–	5.0	80	
–15 Vdc ≥ V_I ≥ –25 Vdc		–	3.0	50	
Load Regulation, T_J = 25°C (Note 1) 5.0 mA ≤ I_O ≤ 500 mA	Reg_{load}	–	30	240	mV
Output Voltage –14.5 Vdc ≥ V_I ≥ –30 Vdc, 5.0 mA ≤ I_O ≤ 350 mA	V_O	–11.4	–	–12.6	Vdc
Input Bias Current (T_J = 25°C)	I_{IB}	–	4.4	8.0	mA
Input Bias Current Change	ΔI_{IB}				mA
–14.5 Vdc ≥ V_I ≥ –30 Vdc, I_O = 350 mA		–	–	0.4	
5.0 mA ≤ I_O ≤ 350 mA, V_I = –19 V		–	–	0.4	
Output Noise Voltage, T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz	V_n	–	75	–	µV
Ripple Rejection (f = 120 Hz)	RR	54	60	–	dB
Dropout Voltage I_O = 500 mA, T_J = 25°C	$V_I–V_O$	–	1.1	–	Vdc
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA, 0°C ≤ T_J ≤ 125°C	$\Delta V_O/\Delta T$	–	–0.8	–	mV/°C

NOTES: 1. Load and line regulation are specified at constant temperature. Change in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

2. B = T_{low} to T_{high}, –40°C < T_J < 125°C
C = T_{low} to T_{high}, 0°C < T_J < 125°C

MC79M15B, C

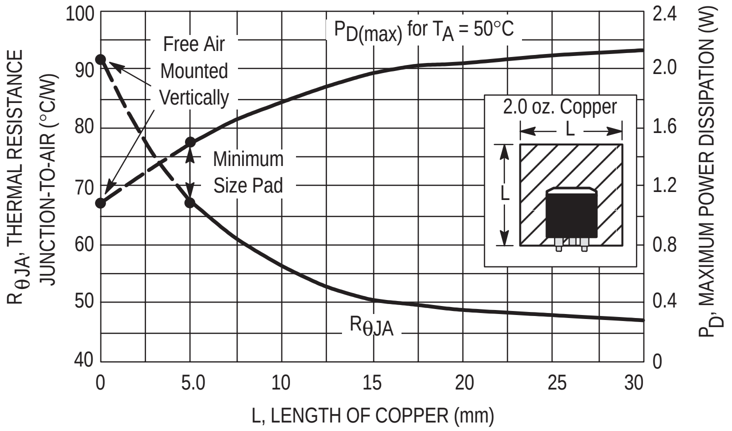
ELECTRICAL CHARACTERISTICS (V_I = –23 V, I_O = 350 mA, T_{low} to T_{high} [Note 2], unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = 25°C)	V_O	–14.4	–15	–15.6	Vdc
Line Regulation, T_J = 25°C (Note 1)	Reg_{line}				mV
–17.5 Vdc ≥ V_I ≥ –30 Vdc		–	5.0	80	
–18 Vdc ≥ V_I ≥ –28 Vdc		–	3.0	50	
Load Regulation, T_J = 25°C (Note 1)	Reg_{load}				mV
5.0 mA ≤ I_O ≤ 500 mA		–	30	240	
Output Voltage	V_O				Vdc
–17.5 Vdc ≥ V_I ≥ –30 Vdc, 5.0 mA ≤ I_O ≤ 350 mA		–14.25	–	–15.75	
Input Bias Current (T_J = 25°C)	I_{IB}	–	4.4	8.0	mA
Input Bias Current Change	ΔI_{IB}				mA
–17.5 Vdc ≥ V_I ≥ –30 Vdc, I_O = 350 mA		–	–	0.4	
5.0 mA ≤ I_O ≤ 350 mA, V_I = –23 V		–	–	0.4	
Output Noise Voltage, T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz	V_n	–	90	–	µV
Ripple Rejection (f = 120 Hz)	RR	54	60	–	dB
Dropout Voltage	V_I–V_O				Vdc
I_O = 500 mA, T_J = 25°C		–	1.1	–	
Average Temperature Coefficient of Output Voltage	$\Delta V_O/\Delta T$				mV/°C
I_O = 5.0 mA, 0°C ≤ T_J ≤ 125°C		–	–1.0	–	

NOTES: 1. Load and line regulation are specified at constant temperature. Change in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

2. B = T_{low} to T_{high}, –40°C < T_J < 125°C
C = T_{low} to T_{high}, 0°C < T_J < 125°C

Figure 1. DPAK Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length



MOTOROLA

MC33128

Power Management Controller

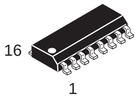
POWER MANAGEMENT CONTROLLER

SEMICONDUCTOR TECHNICAL DATA

The MC33128 is a power management controller specifically designed for use in battery powered cellular telephone and pager applications. This device contains all of the active functions required to interface the user to the system electronics via a microprocessor. This integrated circuit consists of a low dropout voltage regulator with power–up reset for MPU power, two low dropout voltage regulators for independant powering of analog and digital circuitry, and a negative charge pump voltage regulator for full depletion of gallium arsenide MESFETs.

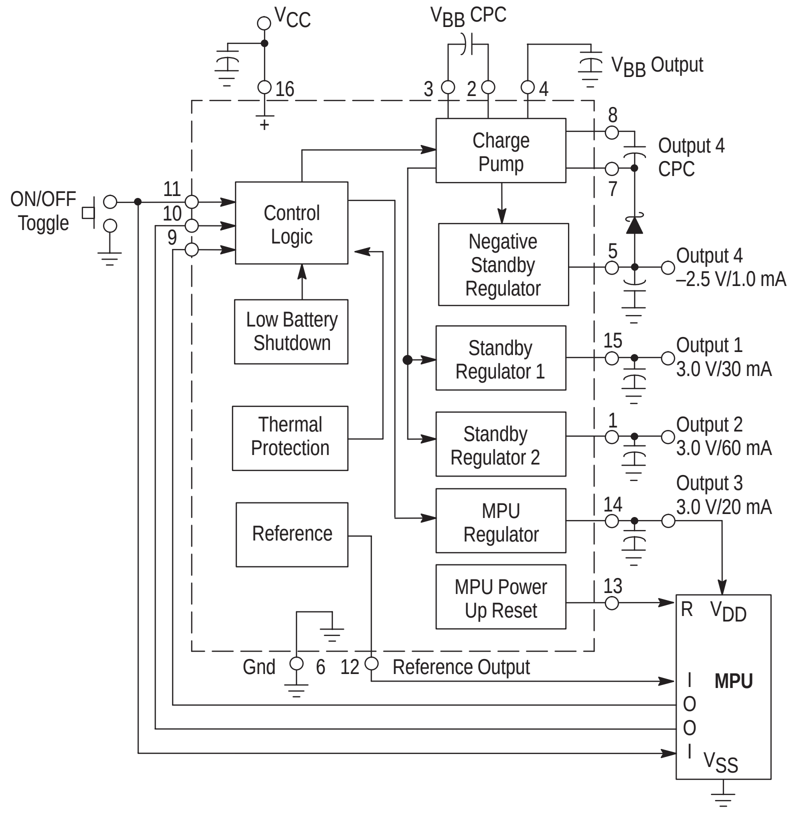
Also included are protective system shutdown features consisting of a battery latch that is activated upon battery insertion, low battery voltage shutdown, and a thermal over temperature detector. This device is available in a 16–pin narrow body surface mount plastic package.

- Three Positive Regulated Outputs Featuring Low Dropout Voltage
- Negative Regulated Output for Full Depletion of GaAs MESFETs
- MPU Power Up Reset
- Battery Latch
- Low Battery Shutdown
- Pinned–Out Reference for MPU A/D Converter
- Low Start–Up and Operating Current
- Thermal Protection

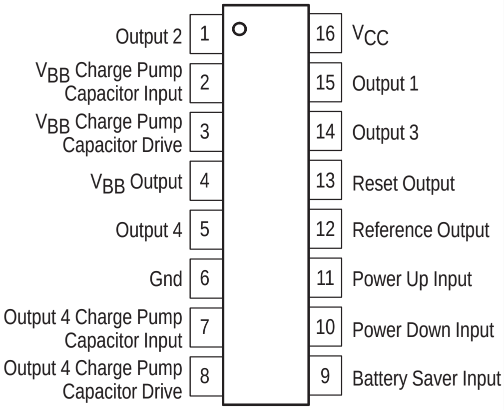


D SUFFIX
PLASTIC PACKAGE
CASE 751B
(SO–16)

Simplified Block Diagram



PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC33128D	T_A = – 30° to +60°C	SO–16

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Input Voltage (Pin 16)	V_{CC}	+7.0	V
Input Voltage Range Power Up, Power Down, and Battery Saver Inputs (Pins 11, 10, 9)	V_{in}	–1.0 to V_{CC} + 1.0	V
Charge Pump Capacitor Drive Outputs, Source or Sink Current (Pins 3, 8)	$I_{O(max)}$	30	mA
Schottky Diode Forward Current (Pins 16 to 2, 2 to 4, and 7 to 6)	$I_{F(max)}$	30	mA
Output Source Current (Note 1) Regulator Output 1 (Pin 15) Regulator Output 2 (Pin 1) Regulator Output 3 (Pin 14) Regulator Output 4 (Pin 5) Reference (Pin 12)	I_{Source}	 150 250 50 10 40	mA
Reset Sink Current (Pin 13)	I_{Sink}	5.0	mA
Power Dissipation and Thermal Characteristic D Suffix, Plastic Package Case 751B Maximum Power Dissipation @ T_A = 50°C Thermal Resistance, Junction–to–Air	 P_D $R_{\varnothing JA}$	 560 180	 mW °C/W
Operating Junction Temperature	T_J	+150	°C
Operating Ambient Temperature (Note 1)	T_A	–30 to +60	°C
Storage Temperature	T_{stg}	–60 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 4.5 V, C_{in} = 33 µF with ESR ≤ 1.6 Ω, C_O = 4.7 µF with ESR ≤ 4.5 Ω, I_{O1} = 30 mA, I_{O2} = 60 mA, I_{O3} = 20 mA, I_{O4} = 1.0 mA, I_{Oref} = 10 mA [Note 2], T_A = 25°C.)

Characteristic	Symbol	Min	Typ	Max	Unit
POWER UP INPUT (Pin 11)					
Low State Input Threshold Voltage	$V_{th(toggle)}$	V_{CC} – 1.5	V_{CC} – 1.2	V_{CC} – 0.8	V
Input Current ($V_{in} = V_{O3}$)	$I_{in(toggle)}$	–	–	120	µA
Internal Pull Up Resistance	$R_{PU(ON/OFF)}$	10	20	30	kΩ
POWER DOWN INPUT (Pin 10)					
High State Input Threshold Voltage (Places IC in Standby Mode)	$V_{th(PDI)}$	1.3	1.5	1.8	V
Input Current ($V_{in} = V_{O3}$)	$I_{in(PDI)}$	–	–	120	µA
BATTERY SAVER INPUT (Pin 9)					
High State Input Threshold Voltage (V_{BB}, V_{O1}, V_{O2}, V_{O4} Activated)	$V_{th(BSI)}$	1.2	1.4	1.7	V
Input Current ($V_{in} = V_{O3}$)	$I_{in(BSI)}$	–	–	120	µA
V_{BB} GENERATOR					
Oscillator Frequency	f_{OSC}	85	95	105	kHz
Oscillator Duty Cycle	DC	35	50	65	%
Charge Pump Capacitor Drive Output Voltage Swing (Pin 3) High State (I_{Source} = 3.0 mA) Low State (I_{Sink} = 3.0 mA)	 V_{OH} V_{OL}	 – –	 V_{CC} – 0.9 0.15	 – –	V
Schottky Diode (Pins 2, 4) Forward Voltage Drop (I_F = 3.0 mA) Reverse Leakage Current (V_{BB} = 7.0 V)	 V_F I_L	 – –	 0.5 0.01	 – –	 V µA
Output Voltage (Pin 4) V_{CC} = 4.5 V V_{CC} = 2.9 V	$V_{O(VBB)}$	 – –	 7.9 4.4	 – –	V

NOTES: 1. Maximum package power dissipation limits must be observed.
2. All outputs are fully loaded as stated in the Electrical Characteristics Table above, except for the one under test.

ELECTRICAL CHARACTERISTICS (V_{CC} = 4.5 V, C_{in} = 33 µF with ESR ≤ 1.6 Ω, C_O = 4.7 µF with ESR ≤ 4.5 Ω, I_{O1} = 30 mA, I_{O2} = 60 mA, I_{O3} = 20 mA, I_{O4} = 1.0 mA, I_{Oref} = 10 mA [Note 2], T_A = 25°C.)

Characteristic	Symbol	Min	Typ	Max	Unit
REGULATOR OUTPUT 1 (Pin 15)					
Output Voltage (V_{CC} = 3.15 V to 4.5 V, I_{O1} = 30 mA)	Reg_{line1}	2.9	3.0	3.1	V
Load Regulation (I_{O1} = 0 mA to 35 mA)	Reg_{load1}	–	5.0	30	mV
Dropout Voltage (V_{CC} = 2.9 V, I_{O1} = 30 mA)	$V_{in} – V_{O1}$	–	–	0.1	V
Power Supply Rejection Ratio f = 120 Hz f = 100 kHz	PSRR 1	 – –	 70 40	 – –	dB
Turn ON Delay Time (Battery Saver Input to 90% V_{O1} Output)	t_{DLY1}	–	0.2	2.0	ms
REGULATOR OUTPUT 2 (Pin 1)					
Output Voltage (V_{CC} = 3.15 V to 4.5 V, I_{O2} = 60 mA)	Reg	2.9	3.0	3.1	V
Load Regulation (I_{O2} = 0 mA to 60 mA)	Reg_{load2}	–	5.0	40	mV
Dropout Voltage (V_{CC} = 2.9 V, I_{O2} = 60 mA)	$V_{in} – V_{O2}$	–	–	0.11	V
Power Supply Rejection Ratio f = 120 Hz f = 100 kHz	PSRR 2	 – –	 70 40	 – –	dB
Turn ON Delay Time (Battery Saver Input to 90% V_{O2} Output)	t_{DLY2}	–	0.2	2.0	ms
REGULATOR OUTPUT 3 (Pin 14)					
Output Voltage (V_{CC} = 3.15 V to 4.5 V, I_{O3} = 20 mA)	Reg_{line3}	2.9	3.0	3.1	V
Load Regulation (I_{O3} = 0 mA to 20 mA)	Reg_{load3}	–	5.0	25	mV
Dropout Voltage (V_{CC} = 2.9 V, I_{O3} = 20 mA)	$V_{in} – V_{O3}$	–	–	0.1	V
Power Supply Rejection Ratio f = 120 Hz f = 100 kHz	PSRR 3	 – –	 70 40	 – –	dB
Turn ON Delay Time (ON/OFF Toggle Input to 90% V_{O3} Output)	t_{DLY3}	–	0.5	3.0	ms
REGULATOR OUTPUT 4 (Pin 5)					
Output Voltage (V_{CC} = 3.15 V to 4.5 V, I_{O4} = 1.0 mA)	Reg_{line4}	–2.35	–2.5	–2.65	V
Load Regulation (I_{O4} = 0 mA to 1.0 mA)	Reg_{load4}	–	5.0	20	mV
Power Supply Rejection Ratio f = 120 Hz f = 100 kHz	PSRR 4	 – –	 70 40	 – –	dB
Schottky Diode Forward Voltage Drop (Pins 7, 6, I_F = 1.0 mA)	V_F	–	0.5	–	V
Charge Pump Capacitor Drive Output Voltage Swing (Pin 8) High State (I_{Source} = 1.0 mA) Low State (I_{Sink} = 1.0 mA)	 V_{OH} V_{OL}	 – –	 V_{BB} – 0.25 0.15	 – –	V
Turn ON Delay Time (Battery Saver Input to 90% V_{O4} Output)	t_{DLY4}	–	4.0	10	ms
REFERENCE OUTPUT (Pin 12)					
Output Voltage (I_O = 0 mA to 10 mA)	Reg_{load}	1.46	1.5	1.54	V
MPU POWER UP RESET COMPARATOR (Pin 13)					
Threshold Voltage Low State Output (V_{O3} Decreasing) Hysteresis (V_{O3} Increasing)	 $V_{th(low)}$ V_H	 2.5 40	 2.6 60	 2.7 100	 V mV
Output Sink Saturation (I_{Sink} = 100 µA, V_{O3} = 2.5 V to 1.0 V)	$V_{CE(sat)}$	–	130	300	mV
Internal Pull–up Resistance	R_{PU}	10	26	40	kΩ
High State Output Voltage (V_{O3} = 2.8 V)	V_{OH}	0.95 V_{O3}	V_{O3}	–	V

NOTE: 2. All outputs are fully loaded as stated in the Electrical Characteristics Table above, except for the one under test.

ELECTRICAL CHARACTERISTICS (V_{CC} = 4.5 V, C_{in} = 33 µF with ESR ≤ 1.6 Ω, C_O = 4.7 µF with ESR ≤ 4.5 Ω, I_{O1} = 30 mA, I_{O2} = 60 mA, I_{O3} = 20 mA, I_{O4} = 1.0 mA, I_{Oref} = 10 mA [Note 2], T_A = 25°C.)

Characteristic	Symbol	Min	Typ	Max	Unit
LOW BATTERY SHUTDOWN COMPARATOR (Pin 16)					
Shutdown Threshold Voltage (V_{CC} Decreasing, Pin 10 = Gnd)	$V_{th(LBSC)}$	2.25	2.4	2.55	V
TOTAL DEVICE (Pin 16)					
Power Supply Current (No Load On All Outputs)	I_{CC}				
Operating					
Battery Saver Input High (Pin 9 = 2.0 V)		–	2.6	4.0	mA
Battery Saver Input Low (Pin 9 ≤ 0.8 V)		–	270	330	µA
Standby (After Power Down Input Strobe)		–	8.0	12	µA

NOTE: 2. All outputs are fully loaded as stated in the Electrical Characteristics Table above, except for the one under test.

Figure 1. Dropout Voltage versus Source Current

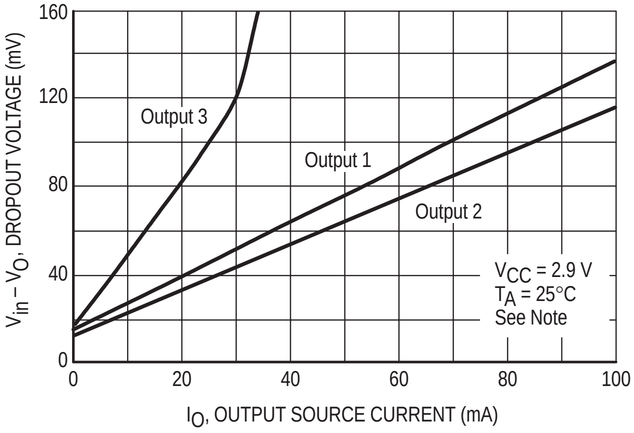


Figure 2. Output 4 Voltage versus Source Current

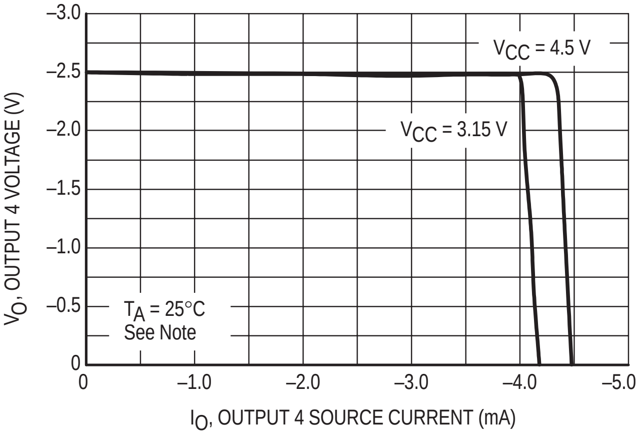


Figure 3. Reference Output Voltage Change versus Source Current

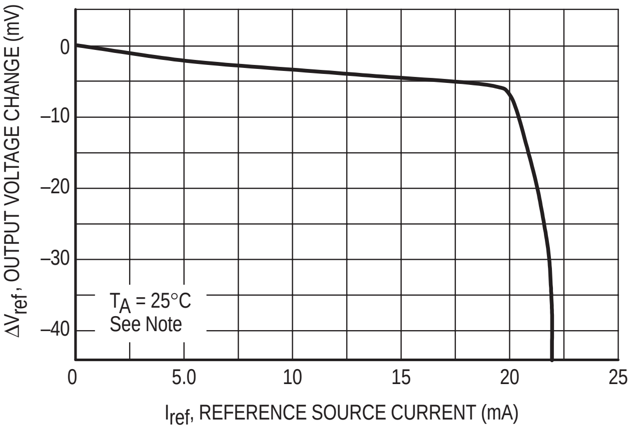
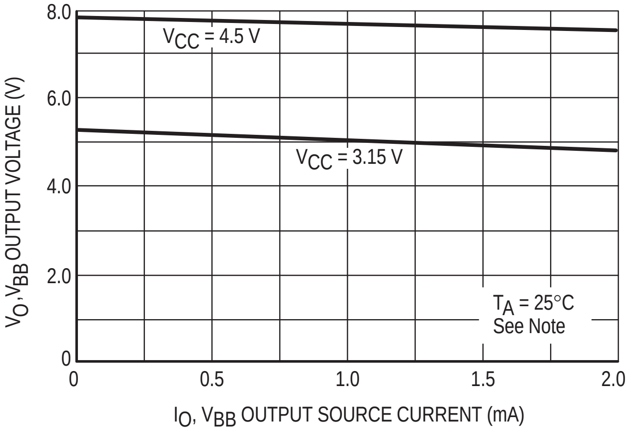


Figure 4. V_{BB} Output Voltage Change versus Source Current



NOTE: All outputs are fully loaded as stated in the Electrical Characteristics Table above, except for the one under test.

OPERATING DESCRIPTION

The MC33128 is a complete power management controller that is designed to interface the user to the system electronics via a microprocessor.

Outputs

Three low dropout voltage regulators are provided at outputs 1, 2 and 3. Outputs 1 and 2 were contemplated for independent powering of the systems analog and digital circuitry. This significantly reduces the possibility of digitally generated noise and spurious signals from coupling into the RF and analog circuits. The low dropout characteristic of Outputs 1 and 2 is achieved by applying a boosted battery voltage, V_{BB}, to their respective driver transistors. This allows the output pass transistors to be driven into saturation when the battery voltage approaches 3.0 V. The V_{BB} Output appears at Pin 4 and can be used to provide gate bias for enhancing external N channel MOSFET switches. Excessive loading of the V_{BB} output will result in an increase in dropout voltage.

Output 4 is derived from a voltage inverting charge pump circuit and is intended to provide the negative gate bias required for full depletion of RF gallium arsenide MESFETs. In personal communication system applications such as cellular telephone, negative gate bias is usually required by the antenna switch and power amplifier circuit blocks with a typical combined current of less than 1.0 mA. Output 4 can supply in excess of 2.0 mA, but there will be an increase in dropout voltage of Outputs 1, 2 and 3.

Outputs 1, 2, 4, V_{BB} Generator and Thermal Protection are all enabled and disabled in unison by the Battery Saver Input, Pin 9. The microprocessor can be programmed to significantly extend the system battery operating time by periodically enabling the receiver circuitry.

Output 3 provides power to the microprocessor, flash EPROM and the system display. These blocks are enabled by the Power Up Input, Pin 11, and disabled by the Power Down Input, Pin 10. By having separate power up and power down inputs, the microprocessor can store any pending information before turning the system and then itself OFF. This allows a controlled or graceful shutdown. Note that the power down request is initiated by pressing the toggle switch while the system is “ON”. This action generates a microprocessor non–maskable interrupt that initiates the graceful shutdown.

Battery Voltage Detection

Reverse biasing and eventual failure of the lowest capacity cell in the battery pack can occur if the system is accidentally left on for an extended time period. To prevent this condition the following circuit blocks were incorporated.

A means for low battery detection is accomplished by using the Reference Output, Pin 12, in conjunction with the microprocessor’s analog to digital converter input. A microprocessor output (LBO) can be designated to flash a display enunciator when a low battery condition exists. The Reference Output is 1.5 V ±2.7% and is capable of sourcing in excess of 10 mA.

The Power Up Reset Output, Pin 13, is designed to hold the microprocessor reset input low until the voltage at Output 3 rises above 2.66 V. This feature prevents the microprocessor from hanging or writing invalid information into its memory during power up. Notice that the output of the MPU Power Up Reset comparator also drives the base of transistor Q_{PD}. If Output 3 should fall below 2.6 V, due to an overload or a low battery condition, the comparator will drive Q_{PD} “ON”, causing its collector to pull high on the Power Down Input, immediately forcing the system into standby mode. Externally pulling down on Pin 13, base of Q_{PD}, will also force the system into standby mode.

A redundant Low Battery Shutdown circuit is included. This circuit directly monitors the battery voltage and also forces the system into standby mode when the battery voltage falls below 2.4 V. To test the functionality of this circuit, the high state signal generated by transistor Q_{PD} must be clamped low, to prevent resetting the ON/OFF Latch. An external short or a pull–down, capable of sinking 2.0 mA at less than 0.8 V, must be connected to Pin 10.

A Battery Latch circuit is designed into the IC to prevent the system from turning on when the batteries are inserted into the finished product. This feature is useful for the end customer as well as the equipment manufacturer. Upon initial application of battery voltage, the lower comparator (0.7 V threshold) forces the Battery Latch into a reset state with its “Q” output low. This in turn triggers a reset of the ON/OFF Latch via the OR gate and also locks out the set signal present at the upper input of the AND gate. As the voltage at Pin 11 rises above (V_{CC} – 1.5 V), the set signal disappears, leaving the state of the ON/OFF Latch unchanged (reset). When the voltage at Pin 11 rises above (V_{CC} –1.0 V), the upper comparator forces the Battery Latch into a set state causing its “Q” output to go high. This allows the AND gate and the ON/OFF Latch to receive a set signal from Pin 11. The initial Battery Latch lockout time is controlled by the internal 20 kΩ resistor and the external 0.1 μF capacitor.

Figure 5. MC33128 Block Diagram

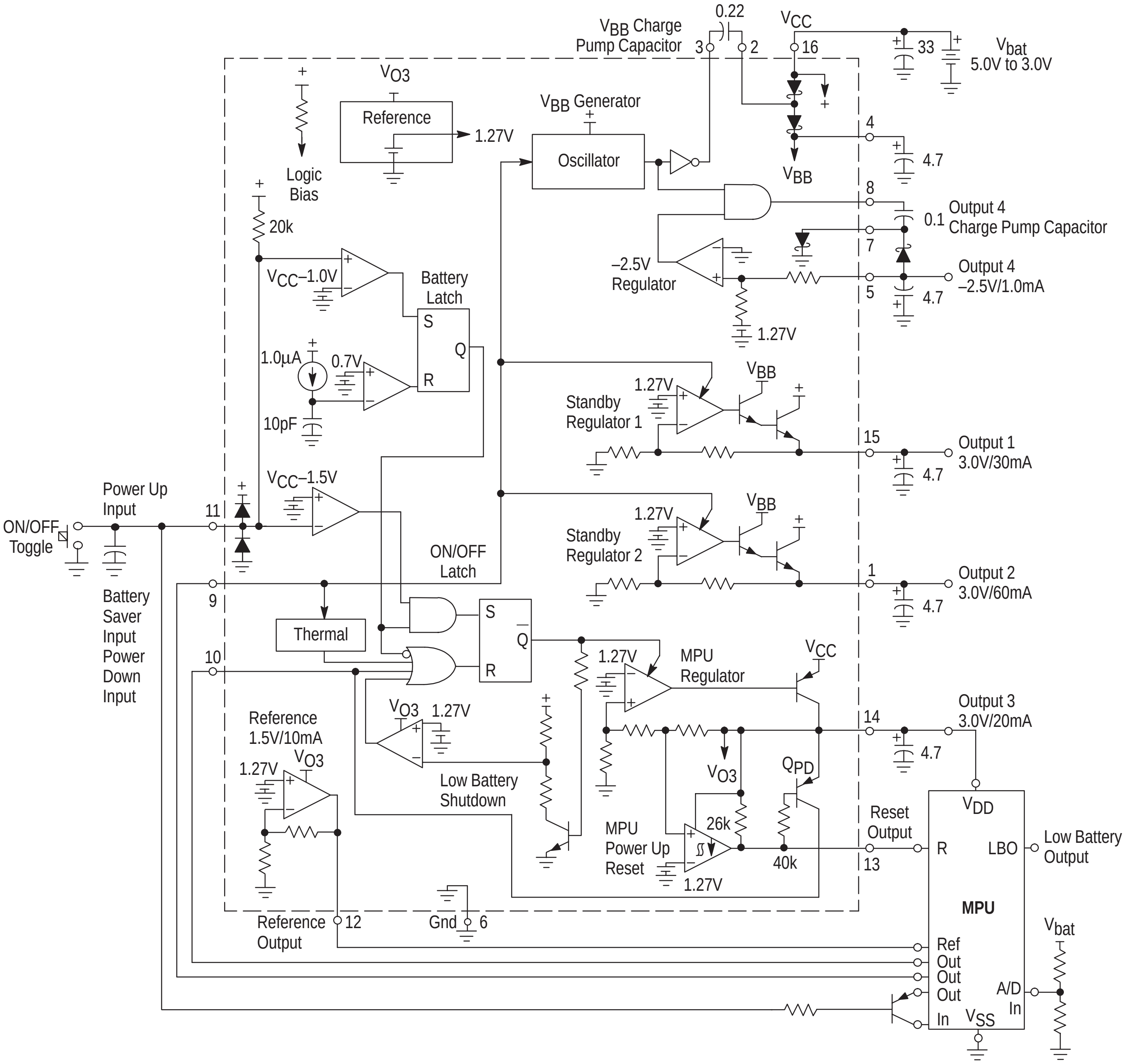
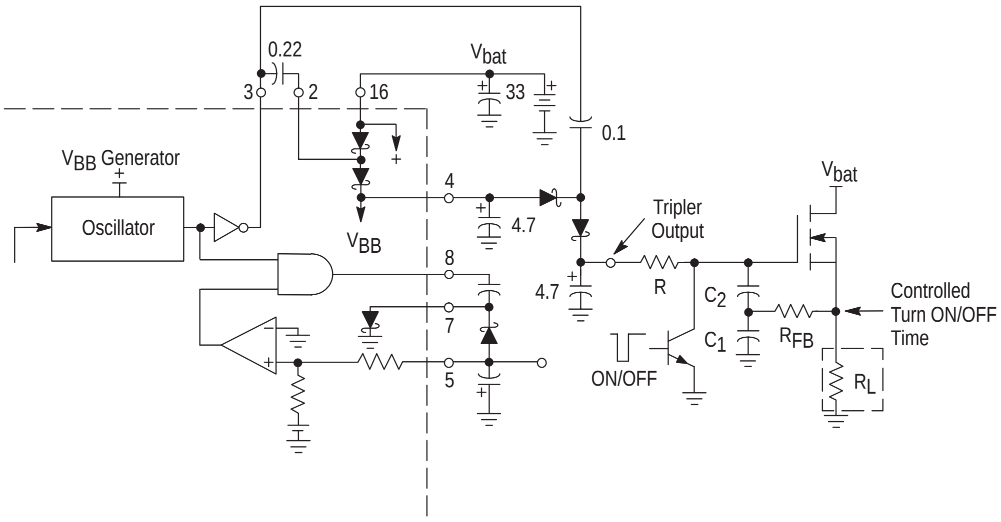


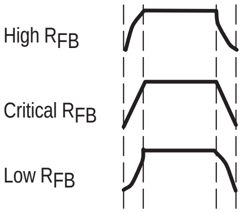
Figure 6. Voltage Tripler and Switch Driver



Tripler Output Voltage

Load Current (mA)	V_{CC} = 3.15 V	V_{CC} = 4.5 V
0	7.96	12.01
0.5	7.48	11.54
1.0	7.24	11.29
1.5	6.99	11.04
2.0	6.62	10.69

Load Turn ON/OFF Time



External Switch

A low threshold N–channel MOSFET can be used to switch the transmitting power amplifier (R_L) ON and OFF. To ensure that all of the available battery voltage appears across the load, the MOSFET must be fully enhanced over the system's required operating voltage range. With the addition of two Schottky diodes and two capacitors, the V_{BB} Generator can be made to function as a voltage tripler. The table in Figure 6 shows the output voltage characteristics of the tripler circuit.

In order to minimize adjacent channel splatter, the RF power amplifier must be turned ON and OFF in a controlled (soft) manner. The applied voltage rise and fall time, as well as the rate of change in rise and fall time, must be tailored to the amplifiers characteristics. The circuit consisting of resistors R, R_{FB}, and capacitors C_1 and C_2 is a simple solution allowing the system designer a means to control the ON and OFF time as well as the waveshape. Feedback resistor R_{FB} controls the waveshape. Capacitors C_1 and C_2 are usually of equal value.

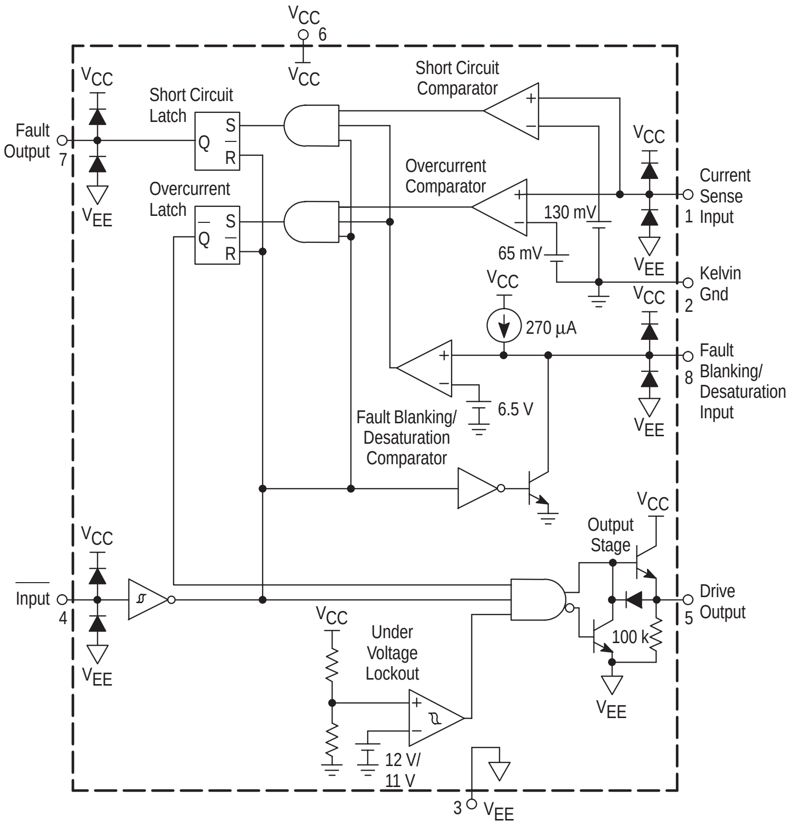
MOTOROLA

Single IGBT Gate Driver

The MC33153 is specifcally designed as an IGBT driver for high power applications that include ac induction motor control, brushless dc motor control and uninterruptable power supplies. Although designed for driving discrete and module IGBTs, this device offers a cost effective solution for driving power MOSFETs and Bipolar Transistors. Device protection features include the choice of desaturation or overcurrent sensing and undervoltage detection. These devices are available in dual–in–line and surface mount packages and include the following features:

- High Current Output Stage: 1.0 A Source/2.0 A Sink
- Protection Circuits for Both Conventional and Sense IGBT's
- Programmable Fault Blanking Time
- Protection against Overcurrent and Short Circuit
- Undervoltage Lockout Optimzed for IGBT's
- Negative Gate Drive Capability
- Cost Effectively Drives Power MOSFETs and Bipolar Transistors

Representative Block Diagram

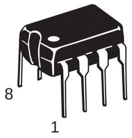


This device contains 133 active transistors.

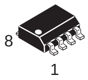
MC33153

SINGLE IGBT GATE DRIVER

SEMICONDUCTOR TECHNICAL DATA

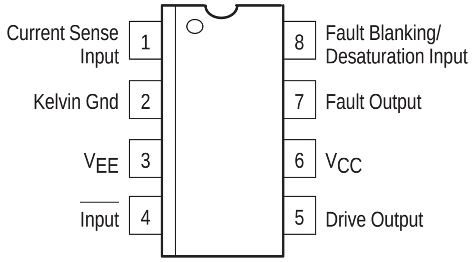


P SUFFIX
PLASTIC PACKAGE
CASE 626



D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC33153D	T_A = –40° to +105°C	SO–8
MC33153P		DIP–8

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage			V
V_{CC} to V_{EE}	$V_{CC} – V_{EE}$	23	
Kelvin Ground to V_{EE} (Note 1)	$KGnd – V_{EE}$	23	
Logic Input	V_{in}	V_{EE} –0.3 to V_{CC}	V
Current Sense Input	V_S	–0.3 to V_{CC}	V
Blanking/Desaturation Input	V_{BD}	–0.3 to V_{CC}	V
Gate Drive Output	I_O		A
Source Current		1.0	
Sink Current		2.0	
Diode Clamp Current		1.0	
Fault Output	I_{FO}		mA
Source Current		25	
Sink Curent		10	
Power Dissipation and Thermal Characteristics			
D Suffix SO–8 Package, Case 751			
Maximum Power Dissipation @ $T_A = 50°C$	P_D	0.56	W
Thermal Resistance, Junction–to–Air	$R_{\theta JA}$	180	°C/W
P Suffix DIP–8 Package, Case 626			
Maximum Power Dissipation @ $T_A = 50°C$	P_D	1.0	W
Thermal Resistance, Junction–to–Air	$R_{\theta JA}$	100	°C/W
Operating Junction Temperature	T_J	+150	°C
Operating Ambient Temperature	T_A	–40 to +105	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V, V_{EE} = 0 V, Kelvin Gnd connected to V_{EE}. For typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies (Note 2), unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
LOGIC INPUT					
Input Threshold Voltage					V
High State (Logic 1)	V_{IH}	–	2.70	3.2	
Low State (Logic 0)	V_{IL}	1.2	2.30	–	
Input Current					µA
High State (V_{IH} = 3.0 V)	I_{IH}	–	130	500	
Low State (V_{IL} = 1.2 V)	I_{IL}	–	50	100	
DRIVE OUTPUT					
Output Voltage					V
Low State (I_{Sink} = 1.0 A)	V_{OL}	–	2.0	2.5	
High State (I_{Source} = 500 mA)	V_{OH}	12	13.9	–	
Output Pull–Down Resistor	R_{PD}	–	100	200	kΩ
FAULT OUTPUT					
Output voltage					V
Low State (I_{Sink} = 5.0 mA)	V_{FL}	–	0.2	1.0	
High State (I_{Source} = 20 mA)	V_{FH}	12	13.3	–	
SWITCHING CHARACTERISTICS					
Propagation Delay (50% Input to 50% Output C_L = 1.0 nF)					ns
Logic Input to Drive Output Rise	$t_{PLH(in/out)}$	–	80	300	
Logic Input to Drive Output Fall	$t_{PHL\ (in/out)}$	–	120	300	
Drive Output Rise Time (10% to 90%) C_L = 1.0 nF	t_r	–	17	55	ns
Drive Output Fall Time (90% to 10%) C_L = 1.0 nF	t_f	–	17	55	ns
Propagation Delay					µs
Current Sense Input to Drive Output	$t_{P(OC)}$	–	0.3	1.0	
Fault Blanking/Desaturation Input to Drive Output	$t_{P(FLT)}$	–	0.3	1.0	

NOTE: 1. Kelvin Ground must always be between V_{EE} and V_{CC}.
2. Low duty cycle pulse techniques are used during test to maintain the junction temperature as close to ambient as possible.
T_{low} = –40°C for MC33153 T_{high} = +105°C for MC33153

ELECTRICAL CHARACTERISTICS (continued) (V_{CC} = 15 V, V_{EE} = 0 V, Kelvin Gnd connected to V_{EE}. For typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies (Note 2), unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
UVLO					
Startup Voltage	$V_{CC\ start}$	11.3	12	12.6	V
Disable Voltage	$V_{CC\ dis}$	10.4	11	11.7	V
COMPARATORS					
Overcurrent Threshold Voltage (V_{Pin8} > 7.0 V)	V_{SOC}	50	65	80	mV
Short Circuit Threshold Voltage (V_{Pin8} > 7.0 V)	V_{SSC}	100	130	160	mV
Fault Blanking/Desaturation Threshold (V_{Pin1} > 100 mV)	$V_{th(FLT)}$	6.0	6.5	7.0	V
Current Sense Input Current (V_{SI} = 0 V)	I_{SI}	–	–1.4	–10	µA
FAULT BLANKING/DESATURATION INPUT					
Current Source (V_{Pin8} = 0 V, V_{Pin4} = 0 V)	I_{chg}	–200	–270	–300	µA
Discharge Current (V_{Pin8} = 15 V, V_{Pin4} = 5.0 V)	I_{dschg}	1.0	2.5	–	mA
TOTAL DEVICE					
Power Supply Current	I_{CC}				mA
Standby ($V_{Pin\ 4}$ = V_{CC}, Output Open)		–	7.2	14	
Operating (C_L = 1.0 nF, f = 20 kHz)		–	7.9	20	

NOTE: 1. Kelvin Ground must always be between V_{EE} and V_{CC}.
2. Low duty cycle pulse techniques are used during test to maintain the junction temperature as close to ambient as possible.
T_{low} = –40°C for MC33153 T_{high} = +105°C for MC33153

Figure 1. Input Current versus Input Voltage

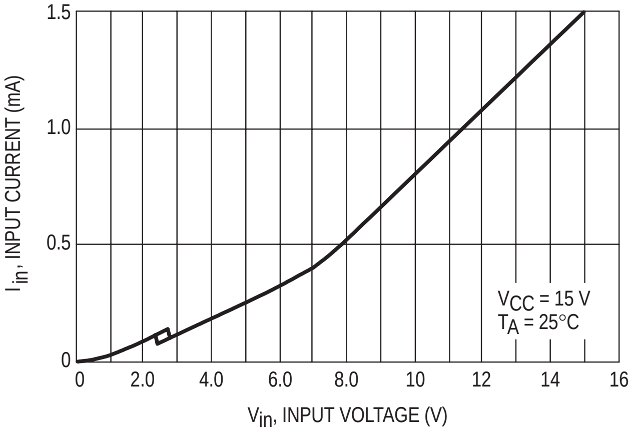


Figure 2. Output Voltage versus Input Voltage

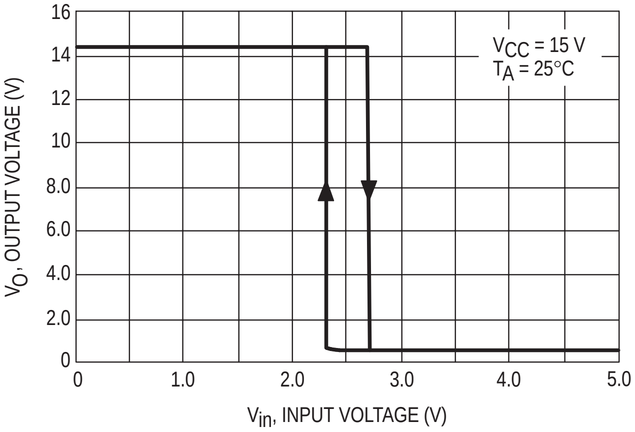


Figure 3. Input Threshold Voltage versus Temperature

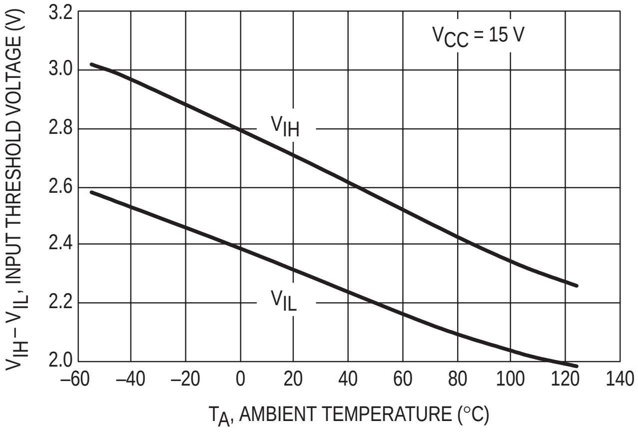


Figure 4. Input Threshold Voltage versus Supply Voltage

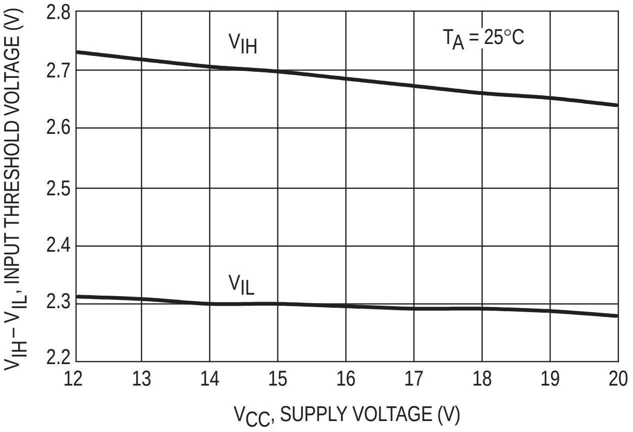


Figure 5. Drive Output Low State Voltage versus Temperature

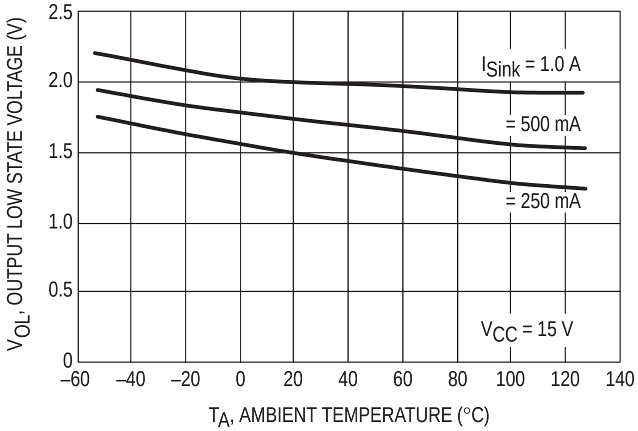


Figure 6. Drive Output Low State Voltage versus Sink Current

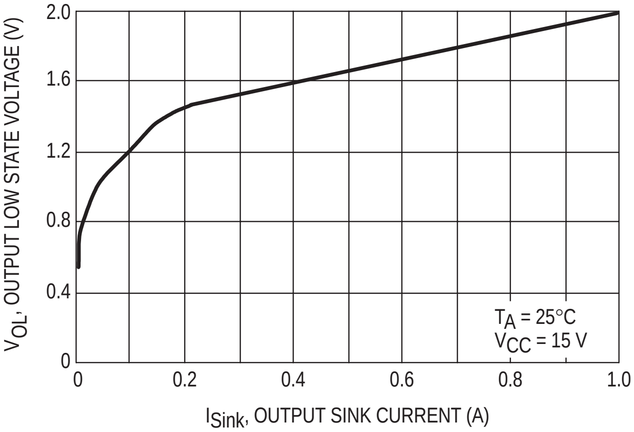


Figure 7. Drive Output High State Voltage versus Temperature

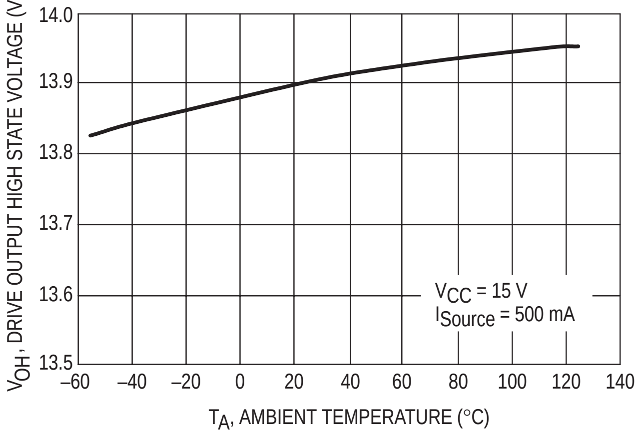


Figure 8. Drive Output High State Voltage versus Source Current

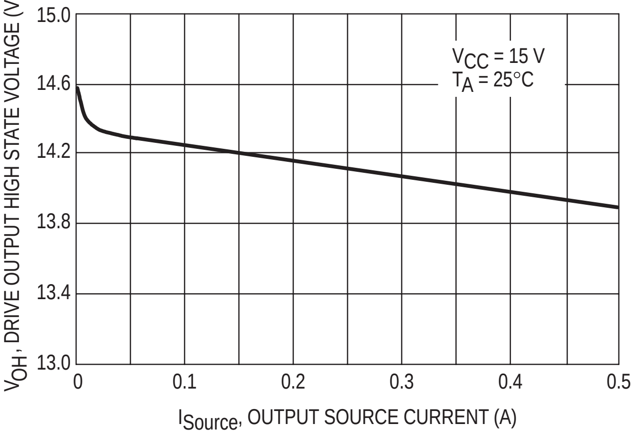


Figure 9. Drive Output Voltage versus Current Sense Input Voltage

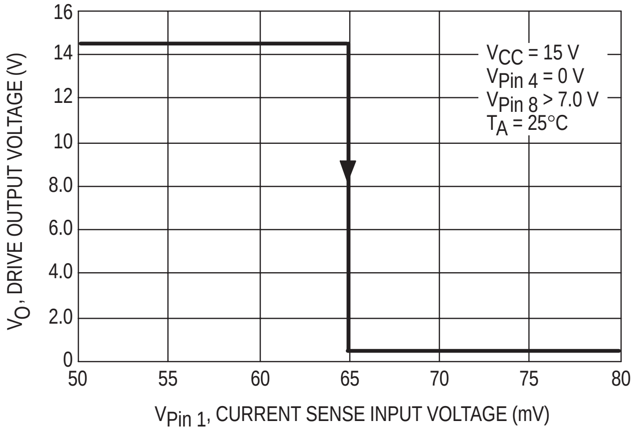


Figure 10. Fault Output Voltage versus Current Sense Input Voltage

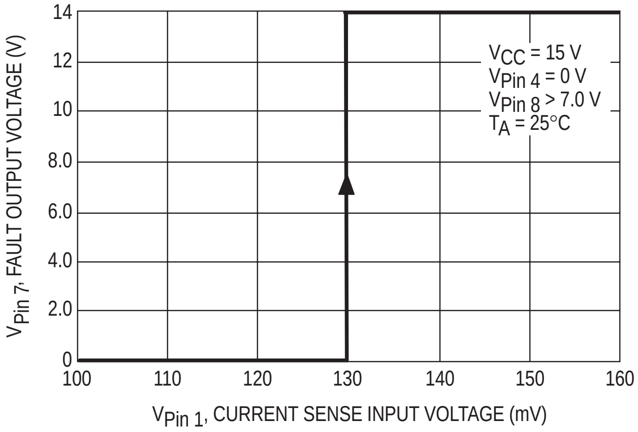


Figure 11. Overcurrent Protection Threshold Voltage versus Temperature

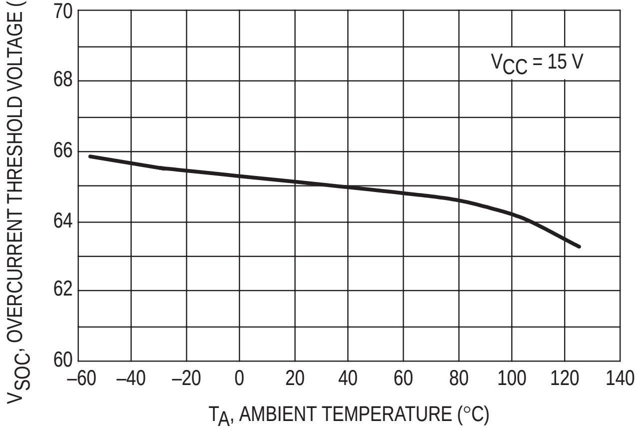


Figure 12. Overcurrent Protection Threshold Voltage versus Supply Voltage

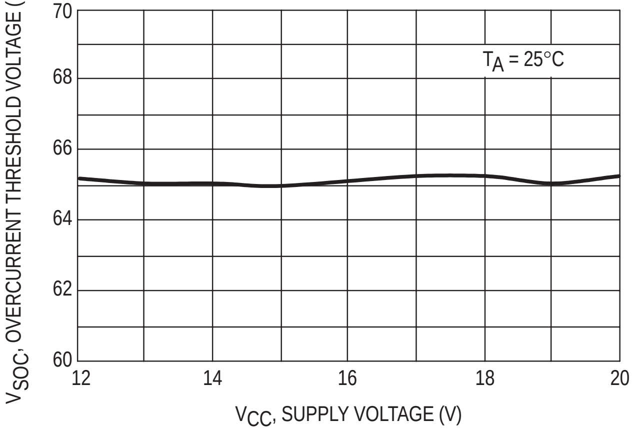


Figure 13. Short Circuit Comparator Threshold Voltage versus Temperature

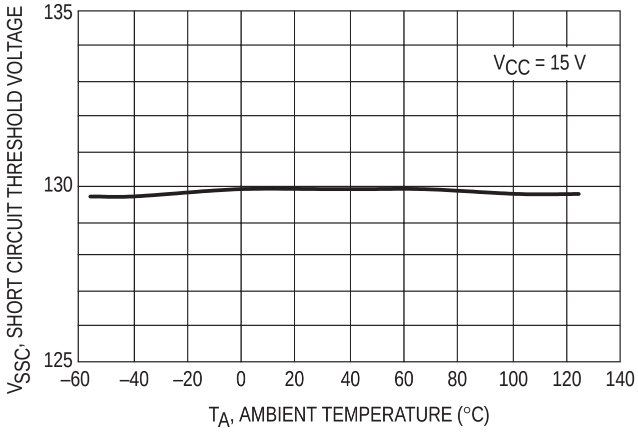


Figure 14. Short Circuit Comparator Threshold Voltage versus Supply Voltage

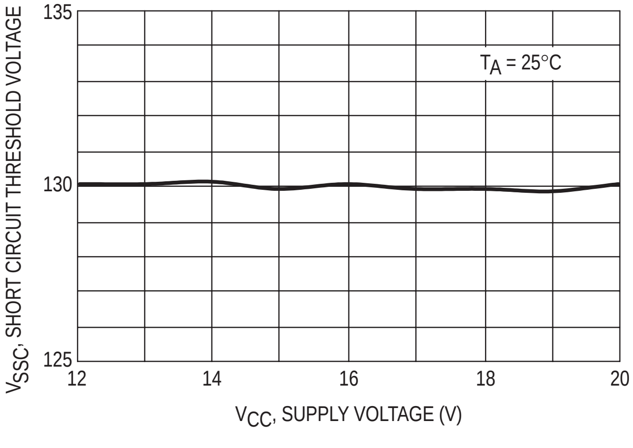


Figure 15. Current Sense Input Current versus Voltage

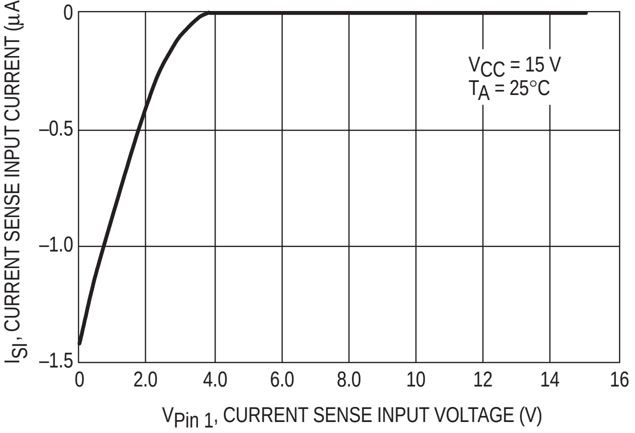


Figure 16. Drive Output Voltage versus Fault Blanking/Desaturation Input Voltage

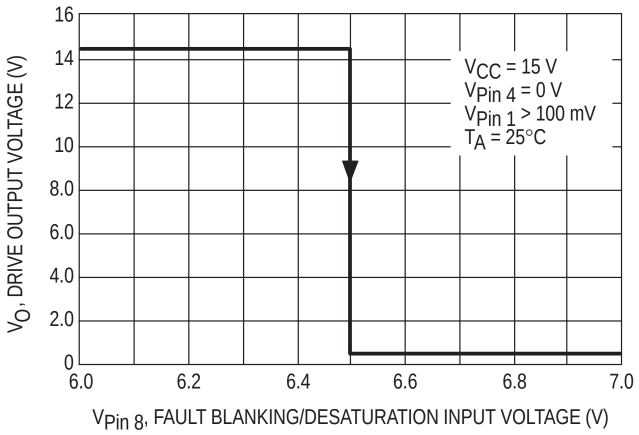


Figure 17. Fault Blanking/Desaturation Comparator Threshold Voltage versus Temperature

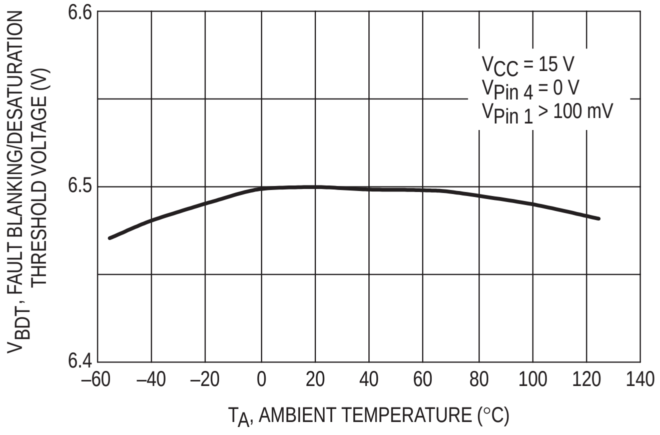


Figure 18. Fault Blanking/Desaturation Comparator Threshold Voltage versus Supply Voltage

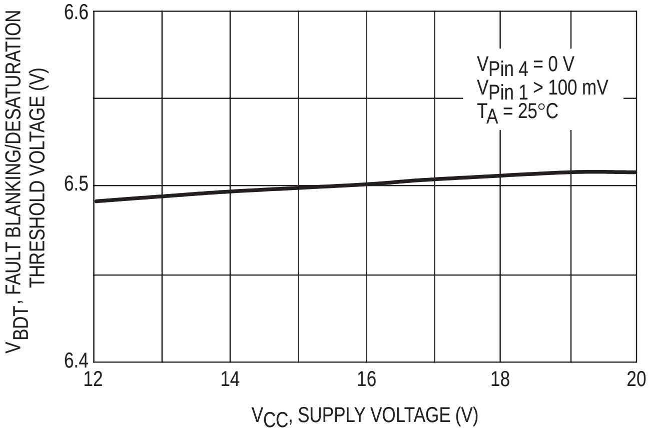


Figure 19. Fault Blanking/Desaturation Current Source versus Temperature

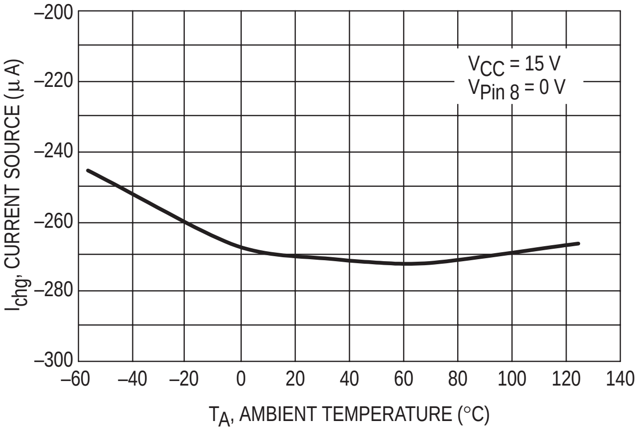


Figure 20. Fault Blanking/Desaturation Current Source versus Supply Voltage

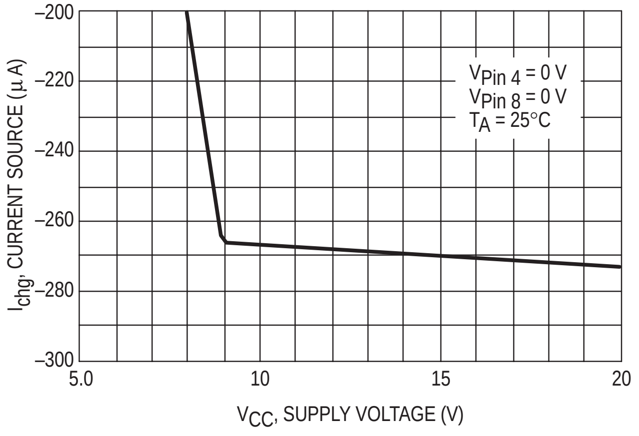


Figure 21. Fault Blanking/Desaturation Current Source versus Input Voltage

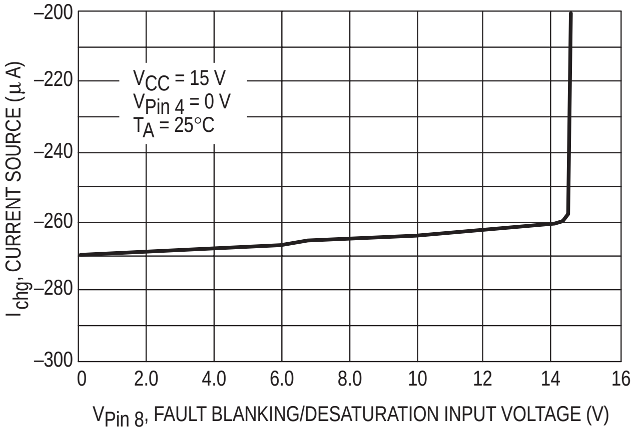


Figure 22. Fault Blanking/Desaturation Discharge Current versus Input Voltage

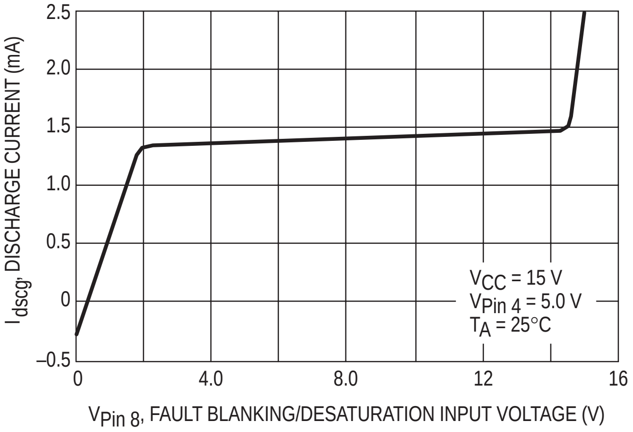


Figure 23. Fault Output Low State Voltage versus Sink Current

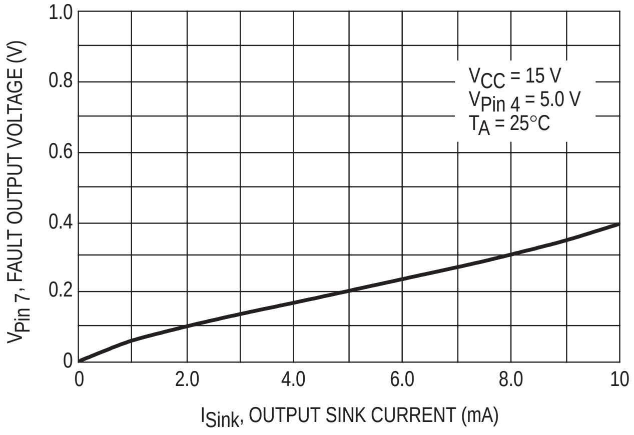


Figure 24. Fault Output High State Voltage versus Source Current

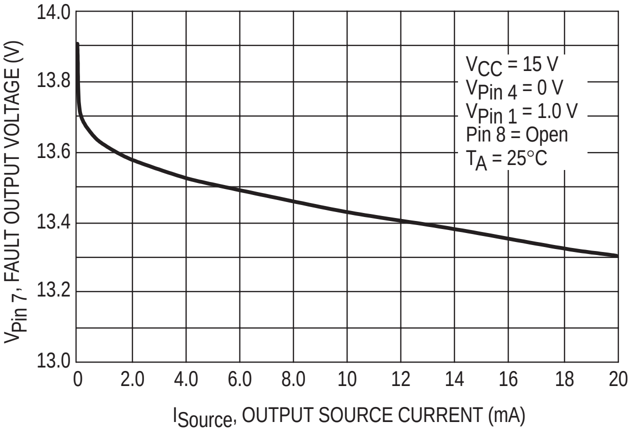


Figure 25. Drive Output Voltage versus Supply Voltage

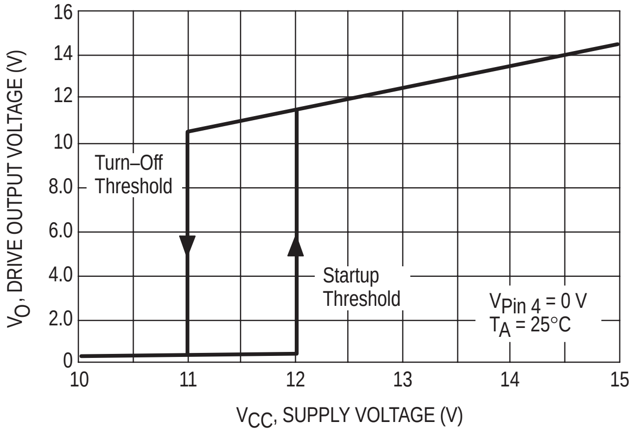


Figure 26. UVLO Thresholds versus Temperature

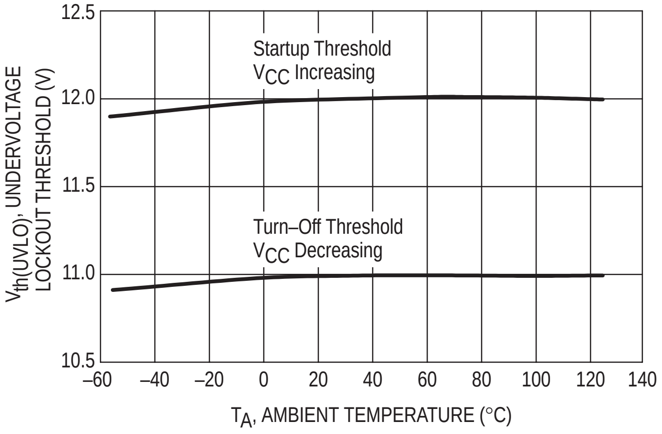


Figure 27. Supply Current versus Supply Voltage

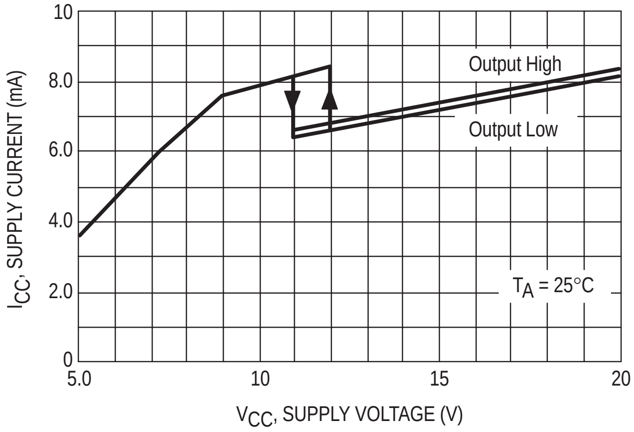


Figure 28. Supply Current versus Temperature

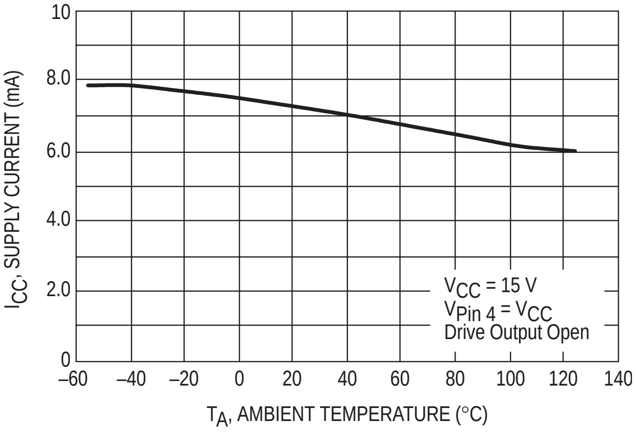
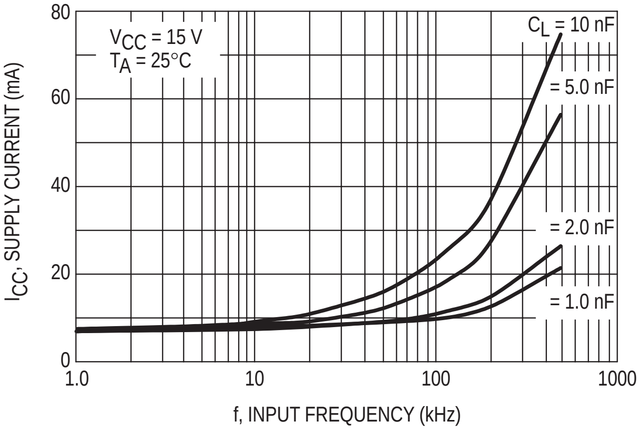


Figure 29. Supply Current versus Input Frequency



OPERATING DESCRIPTION

GATE DRIVE

Controlling Switching Times

The most important design aspect of an IGBT gate drive is optimization of the switching characteristics. The switching characteristics are especially important in motor control applications in which PWM transistors are used in a bridge configuration. In these applications, the gate drive circuit components should be selected to optimize turn–on, turn–off and off–state impedance. A single resistor may be used to control both turn–on and turn–off as shown in Figure 30. However, the resistor value selected must be a compromise in turn–on abruptness and turn–off losses. Using a single resistor is normally suitable only for very low frequency PWM. An optimized gate drive output stage is shown in Figure 31. This circuit allows turn–on and turn–off to be optimized separately. The turn–on resistor, R_{on}, provides control over the IGBT turn–on speed. In motor control circuits, the resistor sets the turn–on di/dt that controls how fast the free–wheel diode is cleared. The interaction of the IGBT and free–wheeling diode determines the turn–on dv/dt. Excessive turn–on dv/dt is a common problem in half–bridge circuits. The turn–off resistor, R_{off}, controls the turn–off speed and ensures that the IGBT remains off under commutation stresses. Turn–off is critical to obtain low switching losses. While IGBTs exhibit a fixed minimum loss due to minority carrier recombination, a slow gate drive will dominate the turn–off losses. This is particularly true for fast IGBTs. It is also possible to turn–off an IGBT too fast. Excessive turn–off speed will result in large overshoot voltages. Normally, the turn–off resistor is a small fraction of the turn–on resistor.

The MC33153 contains a bipolar totem pole output stage that is capable of sourcing 1.0 amp and sinking 2.0 amps peak. This output also contains a pull down resistor to ensure that the IGBT is off whenever there is insufficient V_{CC} to the MC33153.

In a PWM inverter, IGBTs are used in a half–bridge configuration. Thus, at least one device is always off. While the IGBT is in the off–state, it will be subjected to changes in voltage caused by the other devices. This is particularly a problem when the opposite transistor turns on.

When the lower device is turned on, clearing the upper diode, the turn–on dv/dt of the lower device appears across the collector emitter of the upper device. To eliminate shoot–through currents, it is necessary to provide a low sink impedance to the device that is in the off–state. In most applications the turn–off resistor can be made small enough to hold off the device that is under commutation without causing excessively fast turn–off speeds.

Figure 30. Using a Single Gate Resistor

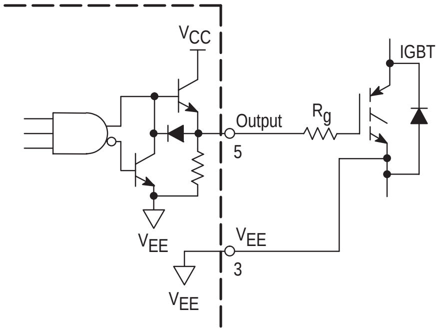
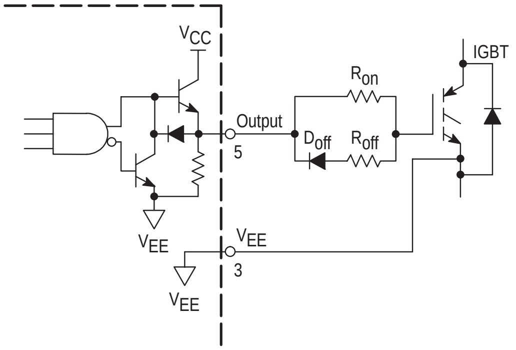


Figure 31. Using Separate Resistors for Turn–On and Turn–Off



A negative bias voltage can be used to drive the IGBT into the off–state. This is a practice carried over from bipolar Darlington drives and is generally not required for IGBTs. However, a negative bias will reduce the possibility of shoot–through. The MC33153 has separate pins for V_{EE} and Kelvin Ground. This permits operation using a +15/–5.0 V supply.

INTERFACING WITH OPTOISOLATORS

Isolated Input

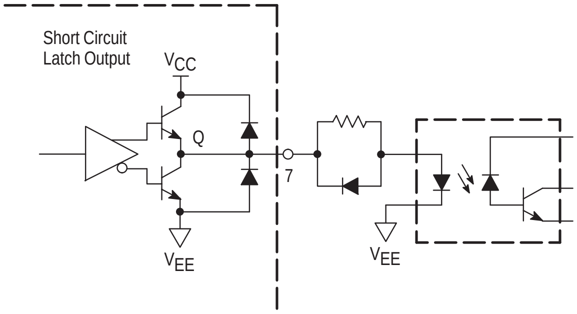
The MC33153 may be used with an optically isolated input. The optoisolator can be used to provide level shifting, and if desired, isolation from ac line voltages. An optoisolator with a very high dv/dt capability should be used, such as the Hewlett Packard HCPL4053. The IGBT gate turn–on resistor should be set large enough to ensure that the opto's dv/dt capability is not exceeded. Like most optoisolators, the HCPL4053 has an active low open–collector output. Thus, when the LED is on, the output will be low. The MC33153 has an inverting input pin to interface directly with an optoisolator using a pull up resistor. The input may also be interfaced directly to 5.0 V CMOS logic or a microcontroller.

Optoisolator Output Fault

The MC33153 has an active high fault output. The fault output may be easily interfaced to an optoisolator. While it is important that all faults are properly reported, it is equally important that no false signals are propagated. Again, a high dv/dt optoisolator should be used.

The LED drive provides a resistor programmable current of 10 to 20 mA when on, and provides a low impedance path when off. An active high output, resistor, and small signal diode provide an excellent LED driver. This circuit is shown in Figure 32.

Figure 32. Output Fault Optoisolator



UNDERVOLTAGE LOCKOUT

It is desirable to protect an IGBT from insufficient gate voltage. IGBTs require 15 V on the gate to achieve the rated on–voltage. At gate voltages below 13 V, the on–voltage increases dramatically, especially at higher currents. At very low gate voltages, below 10 V, the IGBT may operate in the linear region and quickly overheat. Many PWM motor drives use a bootstrap supply for the upper gate drive. The UVLO provides protection for the IGBT in case the bootstrap capacitor discharges.

The MC33153 will typically start up at about 12 V. The UVLO circuit has about 1.0 V of hysteresis and will disable the output if the supply voltage falls below about 11V.

PROTECTION CIRCUITRY

Desaturation Protection

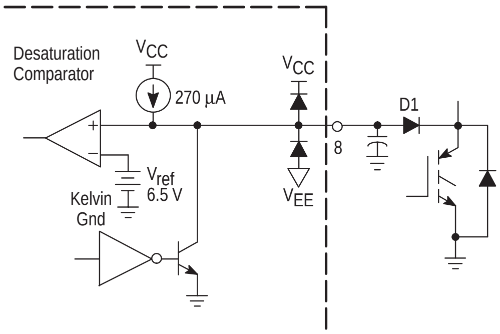
Bipolar Power circuits have commonly used what is known as “Desaturation Detection”. This involves monitoring the collector voltage and turning off the device if this voltage rises above a certain limit. A bipolar transistor will only conduct a certain amount of current for a given base drive. When the base is overdriven, the device is in saturation. When the collector current rises above the knee, the device pulls out of saturation. The maximum current the device will conduct in the linear region is a function of the base current and the dc current gain (h_{FE}) of the transistor.

The output characteristics of an IGBT are similar to a Bipolar device. However, the output current is a function of gate voltage instead of current. The maximum current depends on the gate voltage and the device type. IGBTs tend to have a very high transconductance and a much higher current density under a short circuit than a bipolar device. Motor control IGBTs are designed for a lower current density under shorted conditions and a longer short circuit survival time.

The best method for detecting desaturation is the use of a high voltage clamp diode and a comparator. The MC33153 has a Fault Blanking/Desaturation Comparator which senses the collector voltage and provides an output indicating when the device is not fully saturated. Diode D1 is an external high voltage diode with a rated voltage comparable to the power device. When the IGBT is “on” and saturated, D1 will pull down the voltage on the Fault Blanking/Desaturation Input. When the IGBT pulls out of saturation or is “off”, the current source will pull up the input and trip the comparator. The comparator threshold is 6.5 V, allowing a maximum on–voltage of about 5.8 V.

A fault exists when the gate input is high and V_{CE} is greater than the maximum allowable $V_{CE(sat)}$. The output of the Desaturation Comparator is ANDed with the gate input signal and fed into the Short Circuit and Overcurrent Latches. The Overcurrent Latch will turn–off the IGBT for the remainder of the cycle when a fault is detected. When input goes high, both latches are reset. The reference voltage is tied to the Kelvin Ground instead of the V_{EE} to make the threshold independent of negative gate bias. Note that for proper operation of the Desaturation Comparator and the Fault Output, the Current Sense Input must be biased above the Overcurrent and Short Circuit Comparator thresholds. This can be accomplished by connecting Pin 1 to V_{CC}.

Figure 33. Desaturation Detection



The MC33153 also features a programmable fault blanking time. During turn–on, the IGBT must clear the opposing free–wheeling diode. The collector voltage will remain high until the diode is cleared. Once the diode has been cleared, the voltage will come down quickly to the $V_{CE(sat)}$ of the device. Following turn–on, there is normally considerable ringing on the collector due to the C_{OSS} capacitance of the IGBTs and the parasitic wiring inductance. The fault signal from the Desaturation Comparator must be blanked sufficiently to allow the diode to be cleared and the ringing to settle out.

The blanking function uses an NPN transistor to clamp the comparator input when the gate input is low. When the input is switched high, the clamp transistor will turn “off”, allowing the internal current source to charge the blanking capacitor. The time required for the blanking capacitor to charge up from the on–voltage of the internal NPN transistor to the trip voltage of the comparator is the blanking time.

If a short circuit occurs after the IGBT is turned on and saturated, the delay time will be the time required for the current source to charge up the blanking capacitor from the $V_{CE(sat)}$ level of the IGBT to the trip voltage of the comparator. Fault blanking can be disabled by leaving Pin 8 unconnected.

Sense IGBT Protection

Another approach to protecting the IGBTs is to sense the emitter current using a current shunt or Sense IGBTs. This method has the advantage of being able to use high gain IGBTs which do not have any inherent short circuit capability. Current sense IGBTs work as well as current sense MOSFETs in most circumstances. However, the basic problem of working with very low sense voltages still exists. Sense IGBTs sense current through the channel and are therefore linear with respect to the collector current. Because IGBTs have a very low incremental on–resistance, sense IGBTs behave much like low–on resistance current sense MOSFETs. The output voltage of a properly terminated sense IGBT is very low, normally less than 100 mV.

The sense IGBT approach requires fault blanking to prevent false tripping during turn–on. The sense IGBT also requires that the sense signal is ignored while the gate is low. This is because the mirror output normally produces large transient voltages during both turn–on and turn–off due to the collector to mirror capacitance. With non–sensing types of IGBTs, a low resistance current shunt (5.0 to 50 mΩ) can be used to sense the emitter current. When the output is an actual short circuit, the inductance will be very low. Since the blanking circuit provides a fixed minimum on–time, the peak current under a short circuit can be very high. A short circuit discern function is implemented by the second comparator which has a higher trip voltage. The short circuit signal is latched and appears at the Fault Output. When a short circuit is detected, the IGBT should be turned–off for several milliseconds allowing it to cool down before it is turned back on. The sense circuit is very similar to the desaturation circuit. It is possible to build a combination circuit that provides protection for both Short Circuit capable IGBTs and Sense IGBTs.

APPLICATION INFORMATION

Figure 34 shows a basic IGBT driver application. When driven from an optoisolator, an input pull up resistor is required. This resistor value should be set to bias the output transistor at the desired current. A decoupling capacitor should be placed close to the IC to minimize switching noise.

A bootstrap diode may be used for a floating supply. If the protection features are not required, then both the Fault Blanking/Desaturation and Current Sense Inputs should both be connected to the Kelvin Ground (Pin 2). When used with a single supply, the Kelvin Ground and V_{EE} pins should be connected together. Separate gate resistors are recommended to optimize the turn–on and turn–off drive.

Figure 34. Basic Application

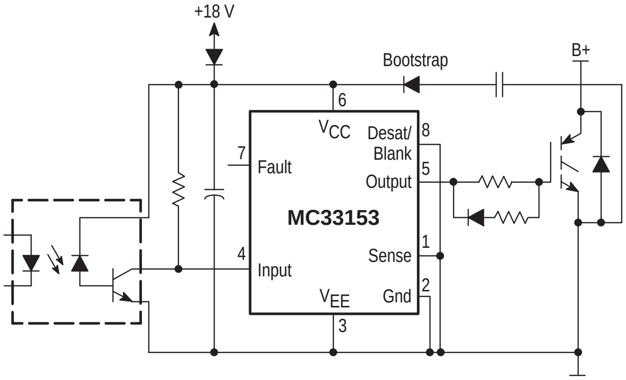
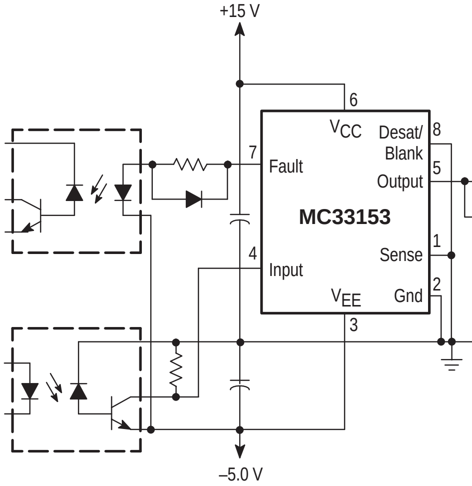


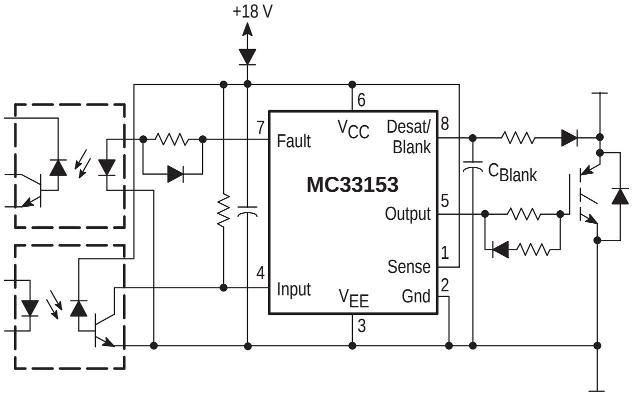
Figure 35. Dual Supply Application



When used in a dual supply application as in Figure 35, the Kelvin Ground should be connected to the emitter of the IGBT. If the protection features are not used, then both the Fault Blanking/Desaturation and the Current Sense Inputs should be connected to Ground. The input optoisolator should always be referenced to V_{EE}.

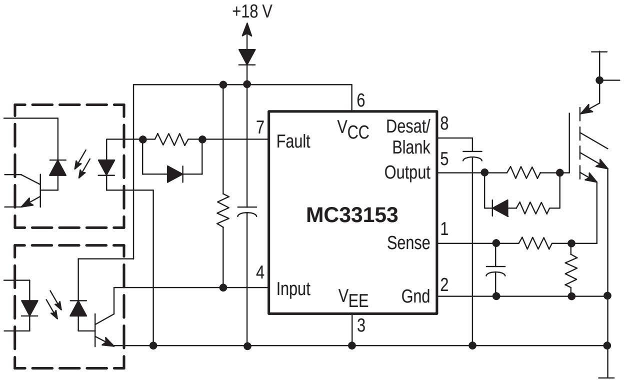
If desaturation protection is desired, a high voltage diode is connected to the Fault Blanking/Desaturation pin. The blanking capacitor should be connected from the Desaturation pin to the V_{EE} pin. If a dual supply is used, the blanking capacitor should be connected to the Kelvin Ground. The Current Sense Input should be tied high because the two comparator outputs are ANDed together. Although the reverse voltage on collector of the IGBT is clamped to the emitter by the free–wheeling diode, there is normally considerable inductance within the package itself. A small resistor in series with the diode can be used to protect the IC from reverse voltage transients.

Figure 36. Desaturation Application



When using sense IGBTs or a sense resistor, the sense voltage is applied to the Current Sense Input. The sense trip voltages are referenced to the Kelvin Ground pin. The sense voltage is very small, typically about 65 mV, and sensitive to noise. Therefore, the sense and ground return conductors should be routed as a differential pair. An RC filter is useful in filtering any high frequency noise. A blanking capacitor is connected from the blanking pin to V_{EE}. The stray capacitance on the blanking pin provides a very small level of blanking if left open. The blanking pin should not be grounded when using current sensing, that would disable the sense. The blanking pin should never be tied high, that would short out the clamp transistor.

Figure 37. Sense IGBT Application



MOTOROLA

MC33154

Product Preview

Single IGBT Gate Driver

The MC33154 is specifically designed as an IGBT driver for high power applications including ac induction motor control, brushless dc motor control and uninterruptible power supplies.

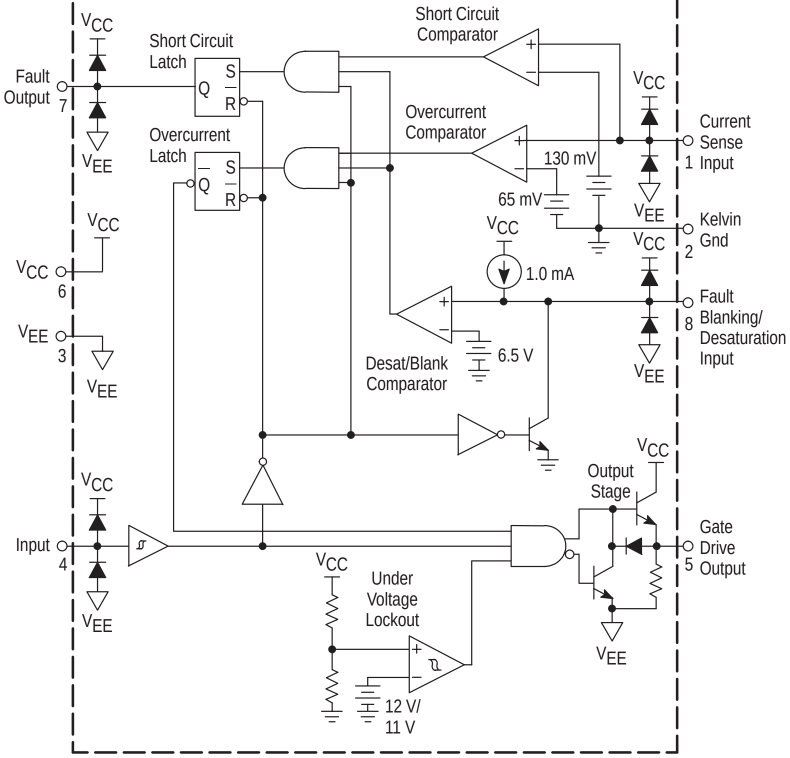
The MC33154 is similar to the MC33153, except that the output drive is in–phase with the logic input, the output source current drive is four times higher and the supply voltage rating is higher.

Although designed for driving discrete and module IGBTs, this device offers a cost effective solution for driving power MOSFETs and Bipolar Transistors.

These devices are available in dual–in–line and surface mount packages and include the following features:

- High Current Output Stage: 4.0 A Source/2.0 A Sink
- Protection Circuits for Both Conventional and Sense IGBTs
- Programmable Fault Blanking Time
- Protection against Overcurrent and Short Circuit
- Undervoltage Lockout Optimzed for IGBTs
- Negative Gate Drive Capability
- Cost Effectively Drives Power MOSFETs and Bipolar Transistors

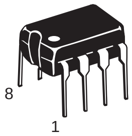
Representative Block Diagram



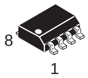
This device contains 133 active transistors.

SINGLE IGBT GATE DRIVER

SEMICONDUCTOR TECHNICAL DATA

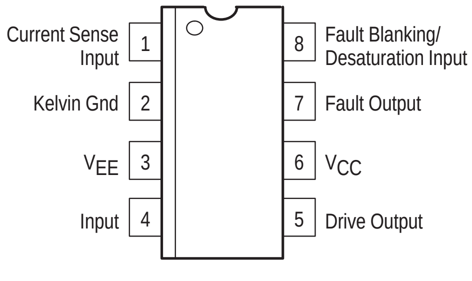


P SUFFIX
PLASTIC PACKAGE
CASE 626



D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC33154D	T_A = –40° to +85°C	SO–8
MC33154P		DIP–8

MC33169

Advance Information

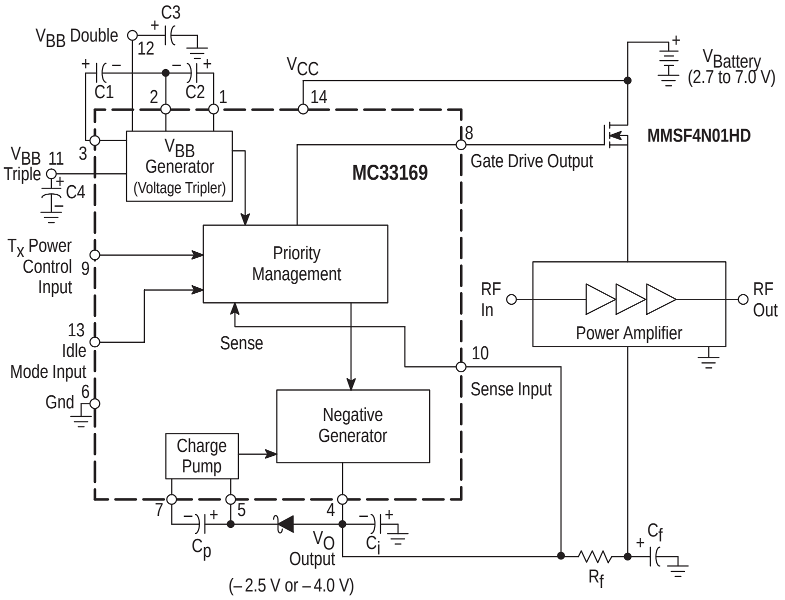
GaAs Power Amplifier Support IC

The MC33169 is a support IC for GaAs Power Amplifier Enhanced FETs used in hand portable telephones such as GSM, PCN and DECT. This device provides negative voltages for full depletion of Enhanced MESFETs as well as a priority management system of drain switching, ensuring that the negative voltage is always present before turning “on” the Power Amplifier. Additional features include an idle mode input and a direct drive of the N–Channel drain switch transistor.

This product is available in two versions, –2.5 and –4.0 V. The –4.0 V version is intended for supplying RF modules for GSM and DCS1800 applications, whereas the –2.5 V version is dedicated for DECT and PHS systems.

- Negative Regulated Output for Full Depletion of GaAs MESFETs
- Drain Switch Priority Management Circuit
- CMOS Compatible Inputs
- Idle Mode Input (Standby Mode) for Very Low Current Consumption
- Output Signal Directly Drives N–Channel FET
- Low Startup and Operating Current

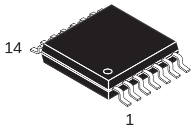
Simplified Block Diagram



This device contains 148 active transistors.

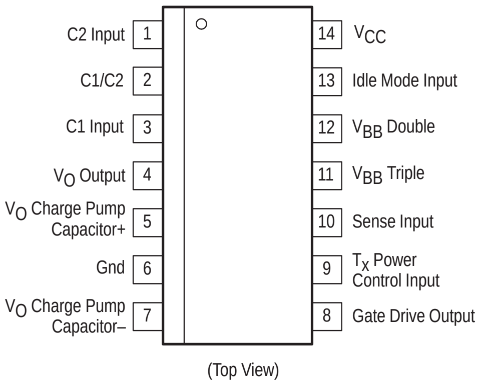
GaAs POWER AMPLIFIER SUPPORT IC

SEMICONDUCTOR TECHNICAL DATA



DTB SUFFIX
PLASTIC PACKAGE
CASE 948G
(TSSOP–14)

PIN CONNECTIONS



ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC33169DTB–4.0	T_A = –40° to +85°C	TSSOP–14
MC33169DTB–2.5		

MAXIMUM RATINGS

Rating	Pin	Symbol	Value	Unit
Power Supply Voltage	14	V_{CC}	9.5	V
T_X Power Control Input	9	VT_X	V_{CC}	V
Idle Mode Input	13	V_i	V_{CC}	V
Sense Input	10	V_{Sense}	–5.0 to 0	V
Negative Generator Output Source Current	4	I_{SS}	20	mA
Charge Pump Capacitor Current	–	I_{max}	60	mA
Diode Forward Current	–	I_{Fmax}	60	mA
Gate Drive Output Current	8	I_{GO}	5.0	mA
Power Dissipation and Thermal Characteristics	–			
Maximum Power Dissipation @ T_A = 50°C		P_D	417	mW
Thermal Resistance, Junction–to–Air		$R_{\theta JA}$	240	°C/W
Operating Junction Temperature		T_J	+150	°C
Operating Ambient Temperature	–	T_A	–40 to +85	°C
Storage Temperature Range	–	T_{stg}	–60 to +150	°C

NOTE: ESD data available upon request.

MC33169–4.0

ELECTRICAL CHARACTERISTICS (V_{CC} = 4.8 V. For typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies, unless otherwise noted.)

Characteristic	Pin	Symbol	Min	Typ	Max	Unit
V_{BB} GENERATOR (VOLTAGE TRIPLER)						
Oscillator Frequency	–	f_{osc}	90	100	110	kHz
Oscillator Duty Cycle	–	DC	35	50	65	%
Output Voltage (V_{CC} = 3.0 V, I_O = 3.0 mA)						V
Double Voltage	12	V_{BBD}	4.6	5.0	–	
Triple Voltage	11	V_{BBT}	6.1	7.0	–	
Triple Voltage (V_{CC} = 7.2 V, I_O = 3.0 mA)	11	V_{BBT}	–	11.2	–	
NEGATIVE GENERATOR OUTPUT						
Output Voltage (I_O = 3.0 mA)	4	V_O	–3.75	–4.0	–4.25	V
Output Voltage Ripple with Filter (R_f = 33 Ω, C_f = 4.7 µF) (I_O = 0 to 5.0 mA)	4	V_r	–	2.0	–	mVpp
PRIORITY MANAGEMENT SECTION						
Idle Mode Input	13					
Input Voltage High State (Logic 1)		V_{IH}	2.0	–	2.7	V
Input Voltage Low State (Logic 0)		V_{IL}	0	–	0.5	V
Input Current High State (Logic 1)		I_{IH}	10	–	80	µA
Input Current Low State (Logic 0), i.e. Standby Mode		I_{IL}	–	–	1.0	µA
T_X Power Control Input	9					
Input Voltage Range		VT_X	0	–	3.1	V
Input Voltage “Off” State (Zero RF Output Level)		$VT_{X(off)}$	–	0.7	–	V
Input Voltage “On” State (Maximum RF Output Level)		$VT_{X(on)}$	–	2.7	–	V
Input Resistance		R_{in}	–	90	–	kΩ
Bandwidth (–3.0 dB)		B	–	1.0	–	MHz
Gate Drive Output	8					
Voltage (VT_X = 0 V)		V_{GO}	–	–	0.5	V
(VT_X = 3.0 V)			V_{CC}+2.7	–	–	
Peak Current (Source and Sink) (VT_X = 3.0 V)		I_{GO}	–	3.0	–	mA
Undervoltage Lockout Voltage on Sense Input (Magnitude)	10	V_{sense}	–3.0	–3.2	–	V

MC33169–4.0

ELECTRICAL CHARACTERISTICS (continued) (V_{CC} = 4.8 V. For typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies, unless otherwise noted.)

Characteristic	Pin	Symbol	Min	Typ	Max	Unit
TOTAL DEVICE POWER CONSUMPTION						
I_{CC} Operating (VT_X = 3.0 V, I_O = 3.0 mA)	–	I_{CC}	–	10	15	mA
I_{CC} Operating	–	I_{CC}				mA
(VT_X = 0 V, I_O = 3.0 mA)			–	12	15	
(VT_X = 0 V, I_O = 0 mA)			–	4.0	5.0	
Standby Mode (Idle Mode Input = 0 V)	–	I_{CC}	–	–	1.0	µA

MC33169–4.0

ELECTRICAL CHARACTERISTICS (V_{CC} = 2.7 V. For typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies, unless otherwise noted.)

Characteristic	Pin	Symbol	Min	Typ	Max	Unit
V_{BB} GENERATOR (VOLTAGE TRIPLER)						
Oscillator Frequency	–	f_{osc}	90	100	110	kHz
Oscillator Duty Cycle	–	DC	35	50	65	%
Output Voltage (V_{CC} = 3.0 V, I_O = 3.0 mA)						V
Double Voltage	12	V_{BBD}	4.6	5.0	–	
Triple Voltage	11	V_{BBT}	6.1	7.0	–	
Triple Voltage (V_{CC} = 7.2 V, I_O = 3.0 mA)	11	V_{BBT}	–	11.2	–	
NEGATIVE GENERATOR OUTPUT						
Output Voltage (I_O = 1.0 mA)	4	V_O	–3.75	–4.0	–4.25	V
Output Voltage Ripple with Filter (R_f = 33 Ω, C_f = 4.7 µF) (I_O = 0 to 5.0 mA)	4	V_r	–	2.0	–	mVpp
PRIORITY MANAGEMENT SECTION						
Idle Mode Input	13					
Input Voltage High State (Logic 1)		V_{IH}	2.0	–	2.7	V
Input Voltage Low State (Logic 0)		V_{IL}	0	–	0.5	V
Input Current High State (Logic 1)		I_{IH}	10	–	80	µA
Input Current Low State (Logic 0), i.e. Standby Mode		I_{IL}	–	–	1.0	µA
T_X Power Control Input	9					
Input Voltage Range		VT_X	0	–	3.0	V
Input Voltage “Off” State (Zero RF Output Level)		$VT_{X(off)}$	–	0.7	–	V
Input Voltage “On” State (Maximum RF Output Level)		$VT_{X(on)}$	–	2.7	–	V
Input Resistance		R_{in}	–	90	–	kΩ
Bandwidth (–3.0 dB)		B	–	1.0	–	MHz
Gate Drive Output	8					
Voltage (VT_X = 0 V)		V_{GO}	–	–	0.5	V
(VT_X = 3.0 V)			V_{CC}+2.7	–	–	
Peak Current (Source and Sink) (VT_X = 3.0 V)		I_{GO}	–	3.0	–	mA
Undervoltage Lockout Voltage on Sense Input (Magnitude)	10	V_{sense}	–3.0	–3.2	–	V
TOTAL DEVICE POWER CONSUMPTION						
I_{CC} Operating (VT_X = 3.0 V)	14	I_{CC}				mA
(I_O = 3.0 mA)			–	–	15	
(I_O = 1.0 mA)			–	–	9.0	
I_{CC} Operating (VT_X = 0 V)	14	I_{CC}				mA
(I_O = 3.0 mA)			–	–	13	
(I_O = 1.0 mA)			–	–	9.0	
(I_O = 0 mA)			–	4.5	6.0	
Standby Mode (Idle Mode Input = 0 V)	14	I_{CC}	–	–	1.0	µA

MC33169–2.5

ELECTRICAL CHARACTERISTICS (V_{CC} = 4.8 V. For typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies, unless otherwise noted.)

Characteristic	Pin	Symbol	Min	Typ	Max	Unit
V_{BB} GENERATOR (VOLTAGE TRIPLER)						
Oscillator Frequency	–	f_{osc}	90	100	110	kHz
Oscillator Duty Cycle	–	DC	35	50	65	%
Output Voltage (V_{CC} = 3.0 V, I_O = 3.0 mA)						V
Double Voltage	12	V_{BBD}	4.6	5.0	–	
Triple Voltage	11	V_{BBT}	6.1	7.0	–	
Triple Voltage (V_{CC} = 7.2 V, I_O = 3.0 mA)	11	V_{BBT}	–	11.2	–	
NEGATIVE GENERATOR OUTPUT						
Output Voltage	4	V_O				V
(I_O = 3.0 mA)			–2.35	–2.5	–2.65	
(I_O = 5.0 mA, V_{CC} = 6.0 V)			–	–2.5	–	
Output Voltage Ripple with Filter (R_f = 33 Ω, C_f = 4.7 μF)	4	V_r				mVpp
(I_O = 0 to 5.0 mA)			–	2.0	8.0	
PRIORITY MANAGEMENT SECTION						
Idle Mode Input	13					
Input Voltage High State (Logic 1)		V_{IH}	2.0	–	2.7	V
Input Voltage Low State (Logic 0)		V_{IL}	0	–	0.5	V
Input Current High State (Logic 1)		I_{IH}	10	–	80	μA
Input Current Low State (Logic 0), i.e. Standby Mode		I_{IL}	–	–	1.0	μA
T_X Power Control Input	9					
Input Voltage Range		VT_X	0	–	3.0	V
Input Voltage “Off” State (Zero RF Output Level)		$VT_{X(off)}$	–	0.7	–	V
Input Voltage “On” State (Maximum RF Output Level)		$VT_{X(on)}$	–	2.7	–	V
Input Resistance		R_{in}	–	90	–	kΩ
Bandwidth (–3.0 dB)		B	–	1.0	–	MHz
Gate Drive Output	8					
Voltage (VT_X = 0 V)		V_{GO}	–	–	0.5	V
(VT_X = 3.0 V)			V_{CC}+2.7	–	–	
Peak Current (VT_X = 3.0 V)		I_{GO}	–	3.0	–	mA
Undervoltage Lockout Voltage on Sense Input (Magnitude)	10	V_{sense}	–2.0	–2.3	–	V
TOTAL DEVICE POWER CONSUMPTION						
I_{CC} Operating (VT_X = 3.0 V, I_O = 3.0 mA)	14	I_{CC}	–	14	17	mA
I_{CC} Operating	14	I_{CC}				mA
(VT_X = 0 V, I_O = 3.0 mA)			–	13.5	16	
(VT_X = 0 V, I_O = 0 mA)			–	4.5	6.0	
Standby Mode (Idle Mode Input = 0 V)	14	I_{CC}	–	–	1.0	μA

PRIORITY MANAGEMENT TRUTH TABLE

Control Inputs		Outputs	
Idle Mode	T_X Power Control	V_O	Gate Drive
0	0	Off	0.5 V max
1	0	–2.5 or –4.0 V	0.5 V max
0	1	Off	0.5 V max
1	1	–2.5 or –4.0 V	V_{CC} + 2.7 V min

PIN FUNCTION DESCRIPTION

Pin	Name	Description
1	C2 Input	This is the positive pin for the charge pump capacitor in the voltage doubler.
2	C1/C2	This is the negative pin for the charge pump capacitors.
3	C1 Input	This is the positive pin for the charge pump capacitor in the voltage tripler.
4	V_O Output	It delivers a regulated negative voltage of –4.0 V or –2.5 V depending on the product version. It can source an output current in excess of 5.0 mA.
5	V_O Charge Pump Capacitor +	This is the positive pin for the capacitor in the inverting charge pump.
6	Gnd	This pin is Ground for both signal and power circuitry.
7	V_O Charge Pump Capacitor –	This is the negative pin for the capacitor in the inverting charge pump.
8	Gate Drive Output	This is the output of the gate amplifier which directly drives the gate of an N–Channel MOSFET. It can sink and source peak currents up to 3.0 mA.
9	T_x Power Control Input	The input signal applied on this pin controls the N–Channel switching MOSFET in follower mode and therefore, linearly controls the RF output voltage.
10	Sense Input Pin	It senses the negative voltage directly on the Power Amplifier. It is also the input pin of an internal Undervoltage Lockout circuit which blocks the switching of the N–Channel MOSFET if the sensed voltage is more positive than –3.0 V (–4.0 V version) or –2.0 V (–2.5 V version).
11	V_{BB} Triple	This is the positive pin of the output filter capacitor in the voltage tripler. The triple voltage at that pin is used internally to supply the inverting charge pump and the gate amplifier.
12	V_{BB} Double	This is the positive pin of the output filter capacitor in the voltage doubler.
13	Idle Mode Input	This pin is used to set the circuit in Low Power Consumption Standby mode. It is CMOS compatible, i.e. a voltage lower than 0.5 V applied on this pin makes the device go into Standby mode in which the current consumption is lower than 1.0 µA. The MC33169 is then awakened by a voltage higher than 2.0 V applied on that pin.
14	V_{CC}	This is the supply input pin for the MC33169, V_{CC} voltage ranges from 2.7 V to 7.2 V.

Figure 1. MC33169 Representative Block Diagram

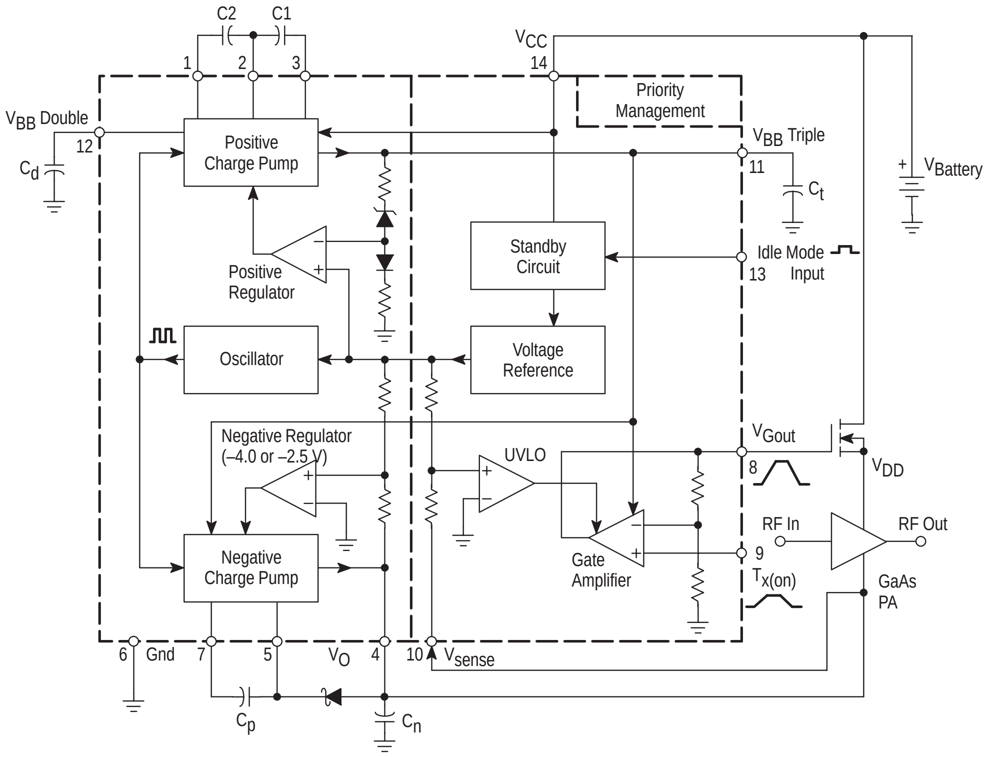


Figure 2. Operating Current versus Temperature

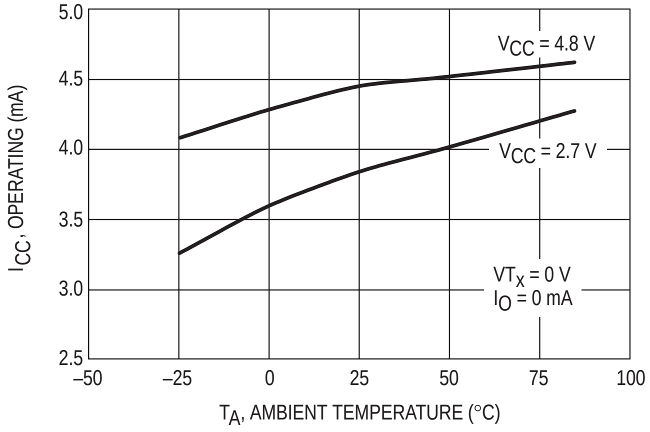


Figure 3. Operating Current versus Temperature

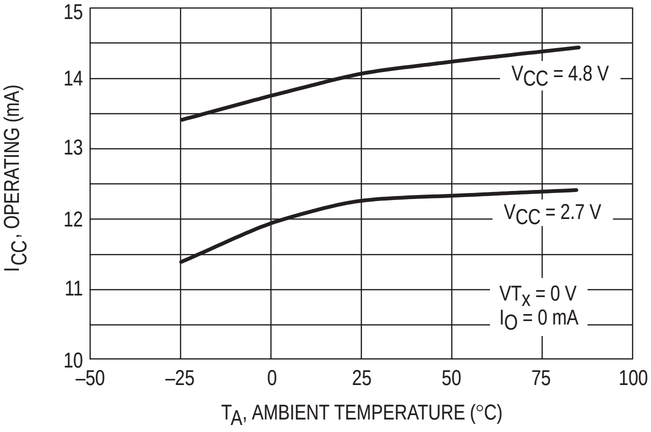


Figure 4. Operating Current versus Temperature

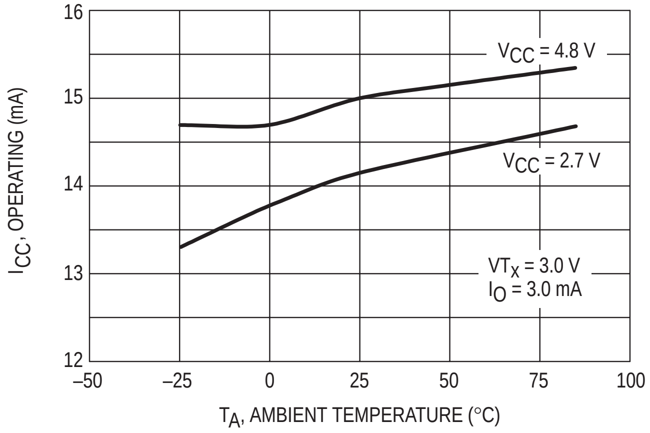


Figure 5. Operating Current versus Temperature

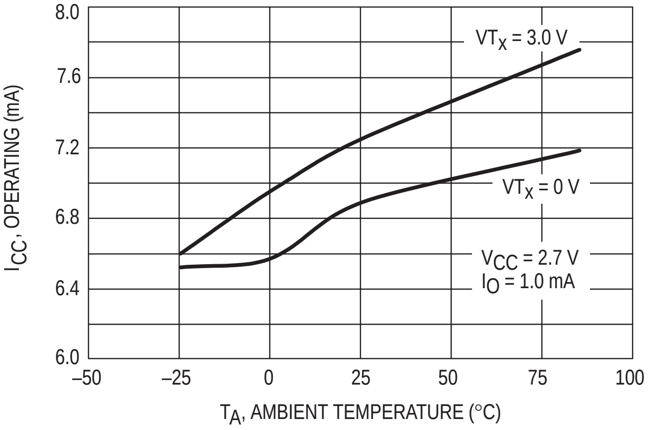


Figure 6. Output Voltage versus Temperature

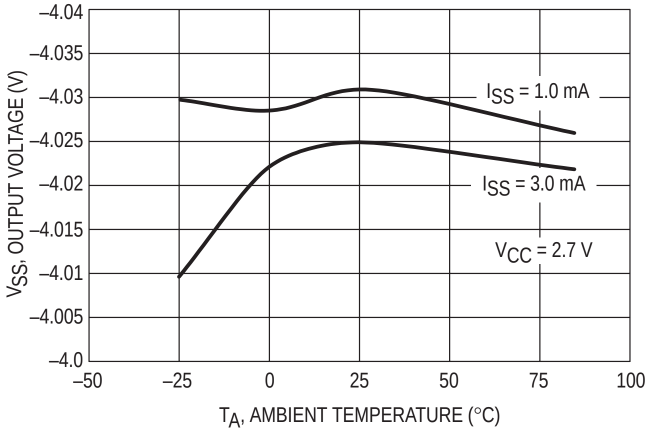


Figure 7. Output Voltage versus Temperature

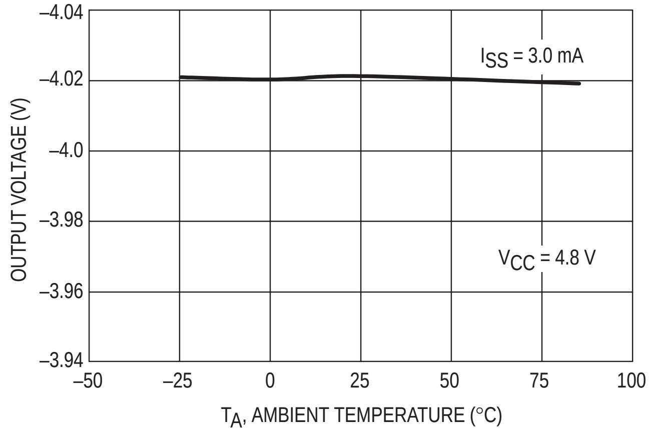


Figure 8. Output Voltage versus Load Current

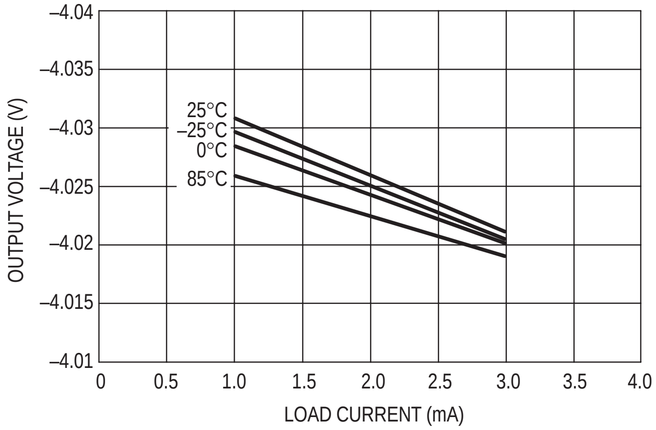
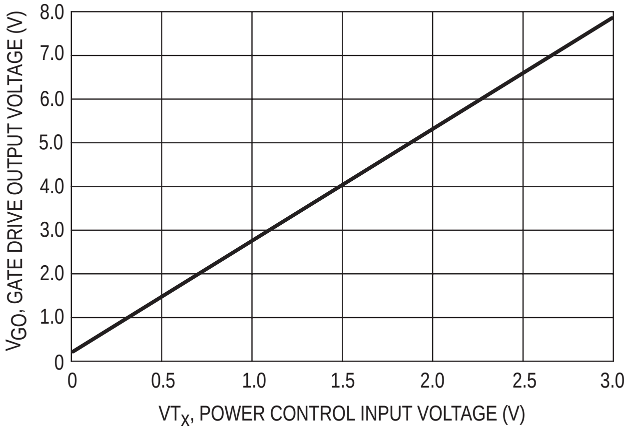


Figure 9. VT_X Control Voltage versus Gate Drive Output Voltage



OPERATING DESCRIPTION

The MC33169 is a power amplifier support IC that is designed to properly switch “on” or “off” a MESFET Power Amplifier either manually or by microprocessor. Controlling the power drain of the RF Amplifier extends operating battery life in many portable systems.

Outputs

The IC is designed to provide a –4.0 V or –2.5 V bias to the gate of the RF Ampllifier MESFET devices prior to application of a positive battery voltage to the drain. The negative output voltage can provide up to 5.0 mA of current. The positive voltage control requires an external N–Channel logic level MOSFET, connected as a source follower. The Gate Drive Output, Pin 8, can source or sink 3.0 mA to the external MOSFET. The low drive current slows the MOSFET switching speed, thereby minimizing voltage glitches on the V_{CC} line which could cause disturbances to other circuitry.

Inputs

A Sense Input, Pin 10, protects the Power Amplifier load by monitoring the level of the negative output voltage. If the negative voltage magnitude falls below a preset level, 3.2 V typical for the –4.0 V version or 2.3 V for the –2.5 V version, an undervoltage lockout circuit disables the external MOSFET gate drive.

The T_X Power Control Input controls the N–Channel external switching MOSFET in source follower mode, which allows linear control of the RF Output voltage level.

The Idle mode input is CMOS compatible, allowing the RF Amplifier to be placed in a standby mode, drawing less than 1.0 µA from the power source.

Figure 10. Class 4 GSM with a Two–Stage Integrated Power Amplifier (I.P.A.)

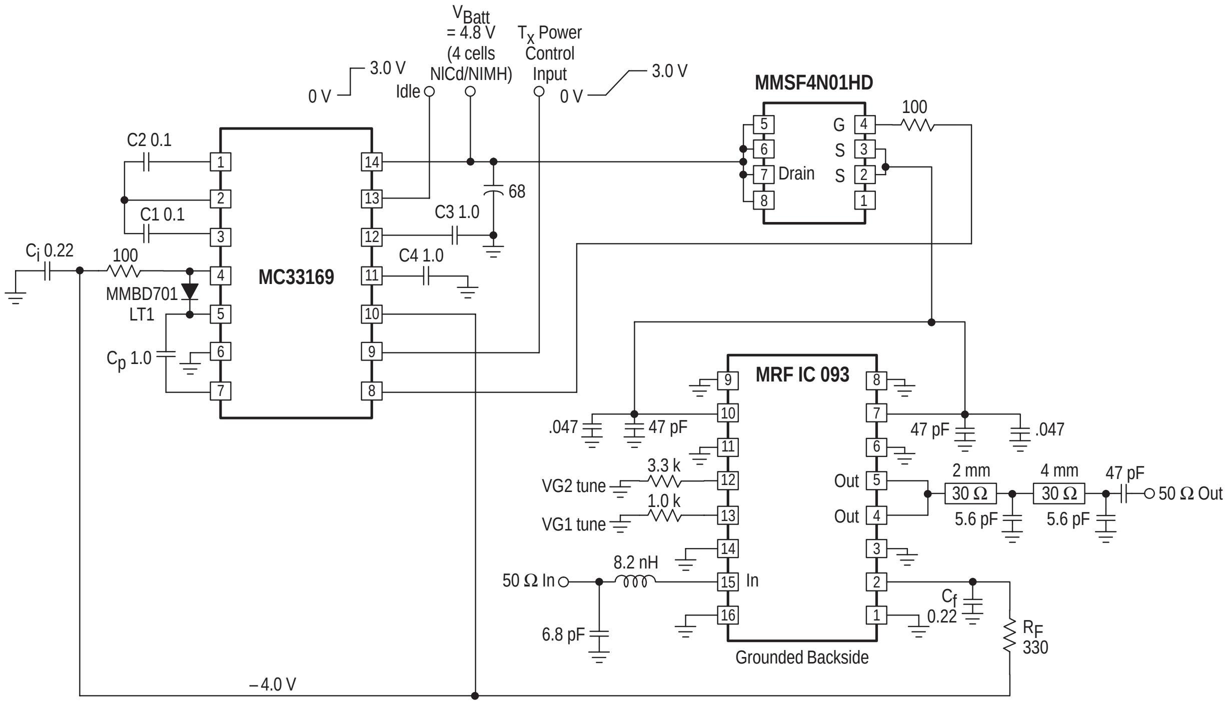
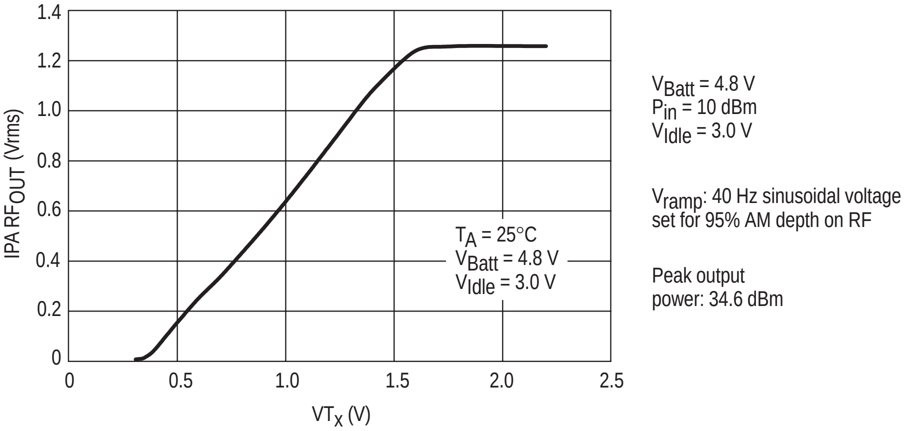


Figure 11. Transfer Characteristic for Gate Drive Output



CURVES RELATED TO APPLICATION GSM CLASS 4

Figure 12. RF Output Voltage (40 Hz/95% AM) and VT_X Driving Voltage

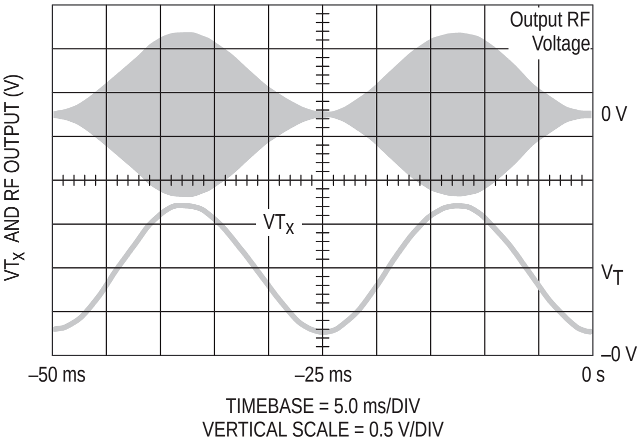


Figure 13. Idle, PA Drain, RF Output and V_O Voltages During a Burst Period

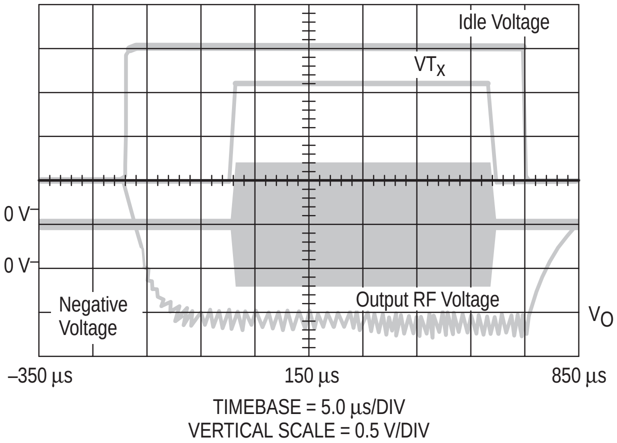


Figure 14. RF Output Voltage, PA Drain Voltage and VT_X Driving Voltage, During Fall Time

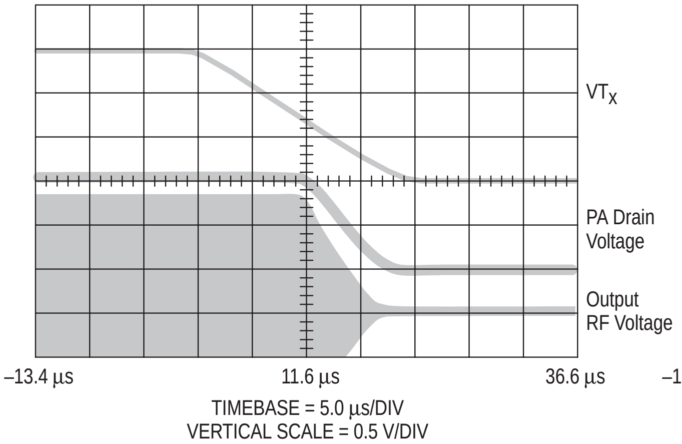


Figure 15. RF Output Voltage, PA Drain Voltage and VT_X Driving Voltage, During Rise Time

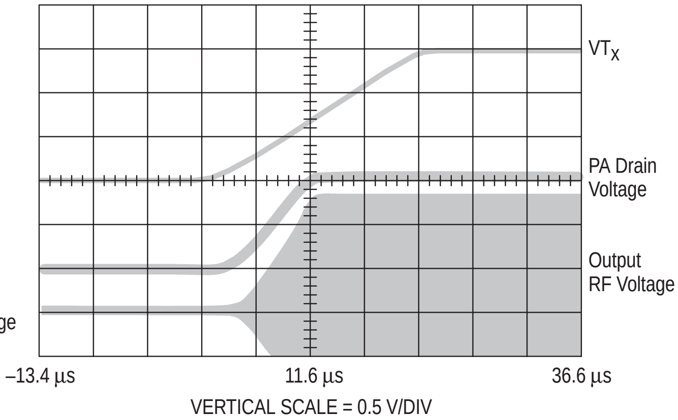


Figure 16. AMPS version with MRFIC0913, Integrated Power Amplifier (I.P.A.)

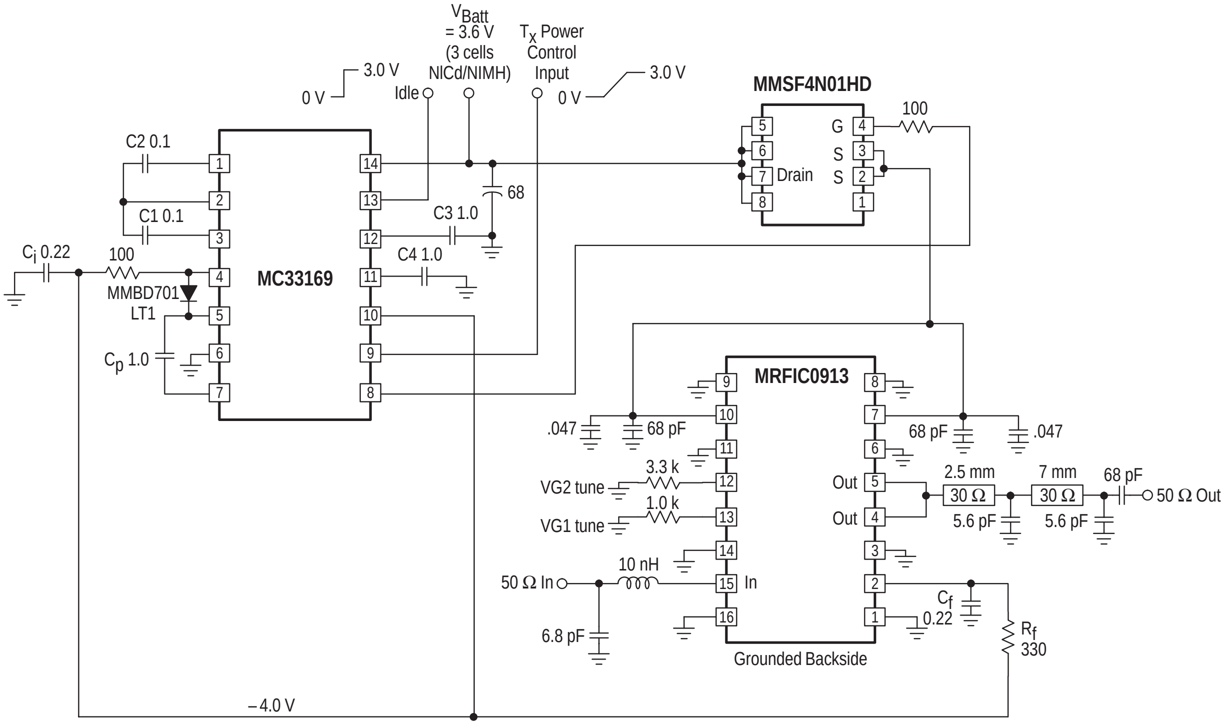
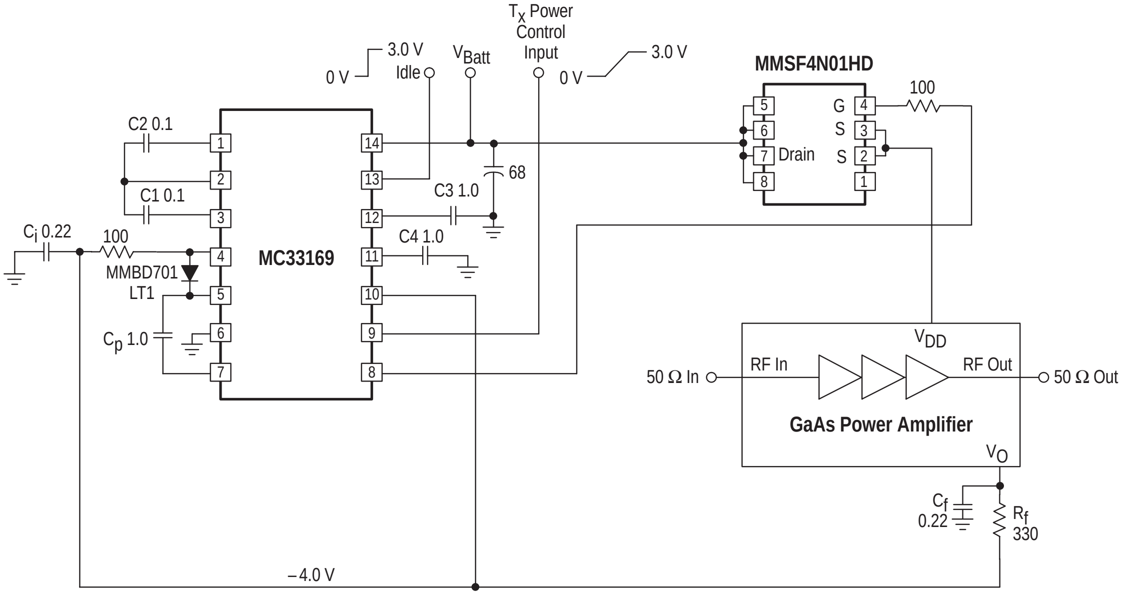


Figure 17. MC33169 with GaAs RF Power Amplifier



MOTOROLA

MC33264

Advance Information

Micropower Voltage Regulators with On/Off Control

LOW DROPOUT MICROPOWER VOLTAGE REGULATORS WITH ON/OFF CONTROL

SEMICONDUCTOR TECHNICAL DATA

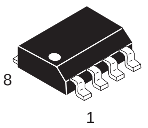
The MC33264 series are micropower low dropout voltage regulators available in SO–8 and Micro–8 surface mount packages and a wide range of output voltages. These devices feature a very low quiescent current (100 µA in the ON mode; 0.1 µA in the OFF mode), and are capable of supplying output currents up to 100 mA. Internal current and thermal limiting protection is provided.

Additionally, the MC33264 has either active HIGH or active LOW control (Pins 2 and 3) that allows a logic level signal to turn–off or turn–on the regulator output.

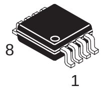
Due to the low input–to–output voltage differential and bias current specifications, these devices are ideally suited for battery powered computer, consumer, and industrial equipment where an extension of useful battery life is desirable.

MC33264 Features:

- Low Quiescent Current (0.3 µA in OFF Mode; 95 µA in ON Mode)
- Low Input–to–Output Voltage Differential of 47 mV at 10 mA, and 131 mV at 50 mA
- Multiple Output Voltages Available
- Extremely Tight Line and Load Regulation
- Stable with Output Capacitance of Only
  0.33 µF for 5.0 V, 6.0 V and 4.75 V Output Voltages
  0.22 µF for 2.8 V, 3.0 V and 3.3 V Output Voltages
- Internal Current and Thermal Limiting
- Logic Level ON/OFF Control
- Functionally Equivalent to TK115XXMC and LP2980

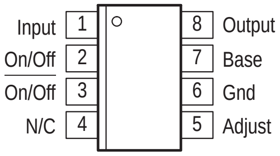


D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)



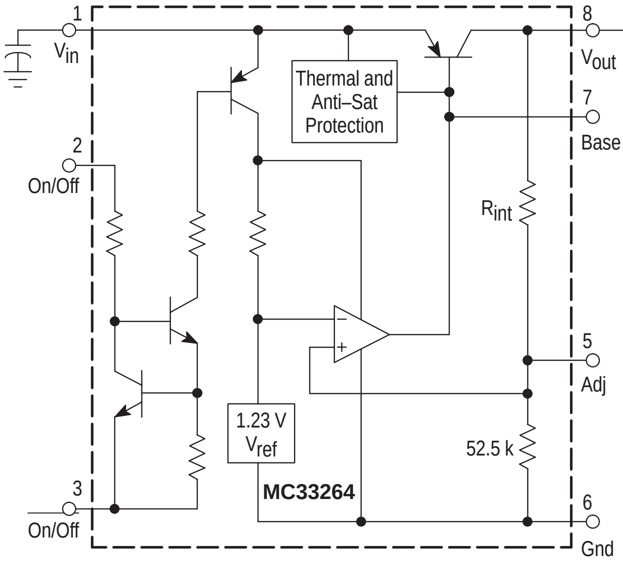
DM SUFFIX
PLASTIC PACKAGE
CASE 846A
(Micro–8)

PIN CONNECTIONS



(Top View)

Representative Block Diagram



This device contains 37 active transistors.

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC33264D–2.8	T_A = – 40° to +85°C	SO–8
MC33264D–3.0		
MC33264D–3.3		
MC33264D–3.8		
MC33264D–4.0		
MC33264D–4.75		
MC33264D–5.0		
MC33264DM–2.8		Micro–8
MC33264DM–3.0		
MC33264DM–3.3		
MC33264DM–3.8		
MC33264DM–4.0		
MC33264DM–4.75		
MC33264DM–5.0		

MAXIMUM RATINGS (T_C = 25°C, unless otherwise noted.)

Rating	Symbol	Value	Unit
Input Voltage	V_{CC}	13	Vdc
Power Dissipation and Thermal Characteristics			
Maximum Power Dissipation	P_D	Internally Limited	W
Case 751 (SO–8) D Suffix			
Thermal Resistance, Junction–to–Ambient	$R_{\theta JA}$	180	°C/W
Thermal Resistance, Junction–to–Case	$R_{\theta JC}$	45	°C/W
Case 846A (Micro–8) DM Suffix			
Thermal Resistance, Junction–to–Ambient	$R_{\theta JA}$	240	°C/W
Output Current	I_O	100	mA
Maximum Adjustable Output Voltage	V_O	1.15 x V_{nom}	Vdc
Operating Junction Temperature	T_J	125	°C
Operating Ambient Temperature	T_A	–40 to +85	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

NOTE: ESD data available upon request.

ELECTRICAL CHARACTERISTICS (V_{in} = 6.0 V, I_O = 10 mA, C_O = 1.0 µF, T_J = 25°C (Note 1), unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (I_O = 0 mA)	V_O				V
2.8 Suffix (V_{CC} = 3.8 V)		2.74	2.8	2.86	
3.0 Suffix (V_{CC} = 4.0 V)		2.96	3.0	3.04	
3.3 Suffix (V_{CC} = 4.3 V)		3.23	3.3	3.37	
3.8 Suffix (V_{CC} = 4.8 V)		3.72	3.8	3.88	
4.0 Suffix (V_{CC} = 5.0 V)		3.92	4.0	4.08	
4.75 Suffix (V_{CC} = 5.75 V)		4.66	4.75	4.85	
5.0 Suffix (V_{CC} = 6.0 V)		4.9	5.0	5.1	
V_{in} = (V_O + 1.0) V to 12 V, I_O < 60 mA,T_A= –40° to +85°C					
2.8 Suffix		2.7	–	2.9	
3.0 Suffix		2.9	–	3.1	
3.3 Suffix		3.18	–	3.42	
3.8 Suffix		3.67	–	3.93	
4.0 Suffix		3.86	–	4.14	
4.75 Suffix		4.58	–	4.92	
5.0 Suffix		4.83	–	5.17	
Line Regulation (V_{in} = [V_O + 1.0] V to 12 V, I_O = 60 mA) All Suffixes	Reg_{line}	–	2.0	10	mV
Load Regulation (V_{in} = [V_O + 1.0], I_O = 0 mA to 60 mA) All Suffixes	Reg_{load}	–	16	25	mV
Dropout Voltage	$V_I – V_O$				mV
I_O = 10 mA		–	47	90	
I_O = 50 mA		–	131	200	
I_O = 60 mA		–	147	230	
Quiescent Current	I_Q				µA
ON Mode (V_{in} = [V_O + 1.0] V, I_O = 0 mA)		–	95	150	
OFF Mode		–	0.3	2.0	
ON Mode (V_{in} = [V_O – 0.5] V, I_O = 0 mA) [Note2]		–	540	900	
Ripple Rejection (V_{in} peak–to–peak = [V_O + 1.5] to [V_O + 5.5] V at f = 1.0 kHz)	–	55	65	–	dB
Output Voltage Temperature Coefficient	TC	–	±120	–	ppm/°C
Current Limit (V_{in} = [V_O + 1.0], V_O Shorted)	I_{Limit}	100	150	–	mA
Output Noise Voltage (10 Hz to 100 kHz) (Note 3)	V_n				µVrms
C_L = 1.0 µF		–	110	–	
C_L = 100 µF		–	46	–	

NOTES:
1. Low duty pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
2. Quiescent current is measured where the PNP pass transistor is in saturation. V_{CE} = –0.5 V guarantees this condition.
3. Noise tests on the MC33264 are made with a 0.01 µF capacitor connected across Pins 8 and 5.

ELECTRICAL CHARACTERISTICS (continued) (V_{in} = 6.0 V, I_O = 10 mA, C_O = 1.0 µF, T_J = 25°C (Note 1), unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
ON/OFF INPUTS					
On/Off Input (Pin 3 Tied to Ground)	$V_{On/Off}$				V
Logic “1” (Regulator ON)		2.4	–	V_{in}	
Logic “0” (Regulator OFF)		0	–	0.5	
On/Off Input (Pin 2 Tied to V_{in})					
Logic “0” (Regulator ON)		0	–	V_{in} – 2.4	
Logic “1” (Regulator OFF)		V_{in} – 0.2	–	V_{in}	
On/Off Pin Input Current (Pin 3 Tied to Ground)	$I_{On/Off}$				µA
$V_{On/Off}$ = 2.4 V		–	1.9	–	
On/Off Pin Input Current (Pin 2 Tied to V_{in})					
$V_{On/Off}$ = V_{in} – 2.4 V		–	12	–	

NOTES: 1. Low duty pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
2. Quiescent current is measured where the PNP pass transistor is in saturation. V_{CE} = –0.5 V guarantees this condition.
3. Noise tests on the MC33264 are made with a 0.01 µF capacitor connected across Pins 8 and 5.

DEFINITIONS

Dropout Voltage – The input/output voltage differential at which the regulator output no longer maintains regulation against further reductions in input voltage. Measured when the output drops 100 mV below its nominal value (which is measured at 1.0 V differential), dropout voltage is affected by junction temperature, load current and minimum input supply requirements.

Line Regulation – The change in output voltage for a change in input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that average chip temperature is not significantly affected.

Load Regulation – The change in output voltage for a change in load current at constant chip temperature.

Maximum Power Dissipation – The maximum total device dissipation for which the regulator will operate within specifications.

Quiescent Current – Current which is used to operate the regulator chip and is not delivered to the load.

Output Noise Voltage – The rms ac voltage at the output, with constant load and no input ripple, measured over a specified frequency range.

Figure 1. Quiescent Current versus Load Current

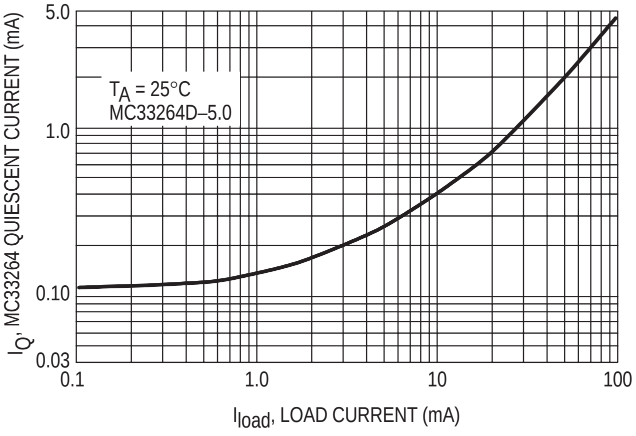


Figure 2. Dropout Voltage versus Input Voltage

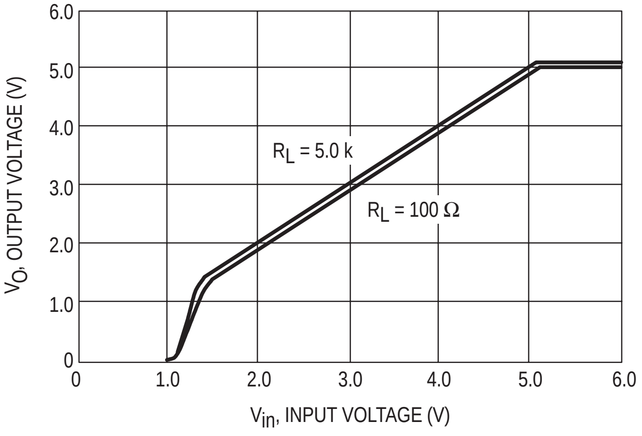


Figure 3. Input Current versus Input Voltage

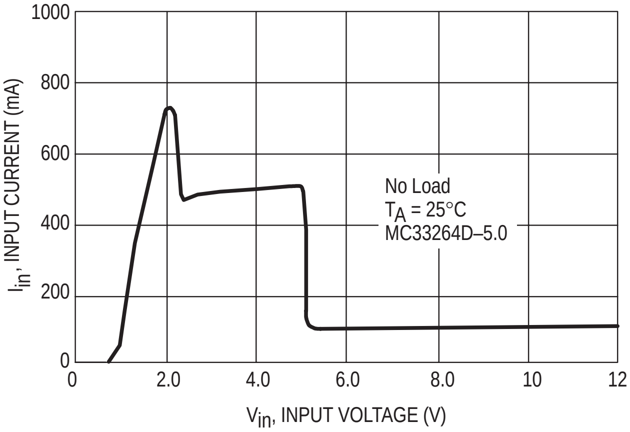


Figure 4. Output Voltage versus Temperature

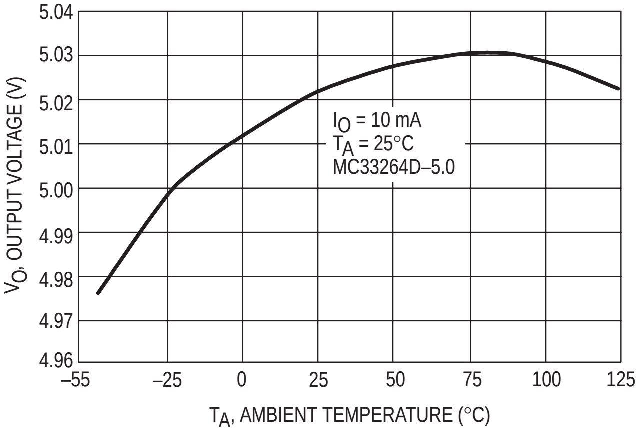


Figure 5. Dropout Voltage versus Output Current

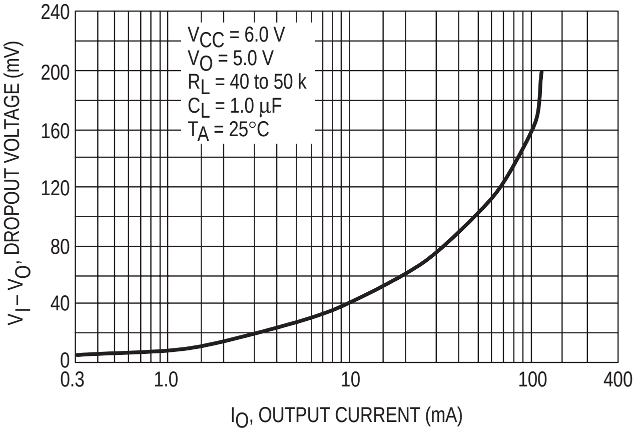
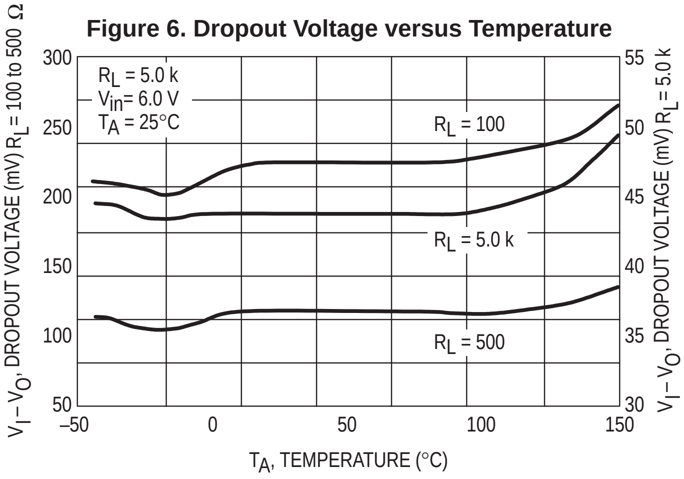


Figure 6. Dropout Voltage versus Temperature



APPLICATION INFORMATION

Introduction

The MC33264 regulators are designed with internal current limiting and thermal shutdown making them user–friendly. These regulators require only 0.33 µF (or greater) capacitance between the output terminal and ground for stability for 2.8 V, 3.0 V, and 3.3 V output voltage options. Output voltage options of 5.0 V, 6.0 V and 4.75 V require only 0.22 µF for stability. The output capacitor must be mounted as close to the MC33264 as possible. If the output capacitor must be mounted further than two centimeters away from the MC33264, then a larger value of output capacitor may be required for stability. A value of 0.68 µF or larger is recommended. Most types of aluminum, tantalum or multilayer ceramic will perform adequately. Solid tantalums or appropriate multilayer ceramic capacitors are recommended for operation below 25°C.

A bypass capacitor is recommended across the MC33264 input to ground if more than 4.0 inches of wire connects the input to either a battery or power supply filter capacitor.

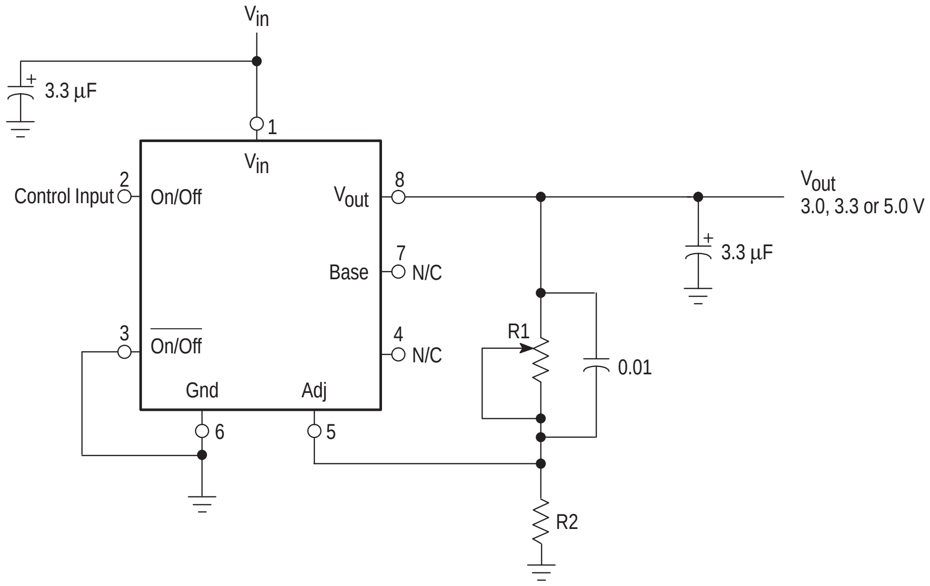
On/Off Control

On/Off control of the regulator may be accomplished in either of two ways. Pin 3 may be tied to circuit ground and a positive logic control applied to Pin 2. The regulator will be turned on by a positive (>2.4 V) level, typically 5.0 V with respect to ground, sourcing a typical current of 6.0 µA. The regulator will turn off if the control input is a logic “0” (<0.5 V). Alternatively, Pin 2 may be tied to the regulator input voltage and a negative logic control applied to Pin 3. The regulator will be turned on when the control voltage is less than V_{in} – 2.4 V, sinking a typical current of 18 µA when V_{in} = 6.0 V. The regulator is off when the control input is open or greater than V_{in} – 0.2 V.

Programming The Output Voltage

The MC33264 output voltage is automatically set using its internal voltage divider. Alternatively, it may be programmed within a typical ±15% range of its preset output voltage. An external pair of resistors is required, as shown in Figure 7.

Figure 7. Regulator Output Voltage Trim



The complete equation for the output voltage is:

$$V_{out} = V_{ref}\left(1 + \frac{R1}{R2}\right) + I_{FB}\ R1$$

where V_{ref} is the nominal 1.235 V reference voltage and I_{FB} is the feedback pin bias current, nominally –20 nA. The minimum recommended load current of 1.0 µA forces an upper limit of 1.2 MΩ on the value of R2, if the regulator must work with no load. I_{FB} will produce a 2% typical error in V_{out} which may be eliminated at room temperature by adjusting R1. For better accuracy, choosing R2 = 100 K reduces this error to 0.17% while increasing the resistor program current to 12 µA.

Output Noise

In many applications it is desirable to reduce the noise present at the output. Reducing the regulator bandwidth by increasing the size of the output capacitor is the only method for reducing noise.

Noise can be reduced fourfold by a bypass capacitor across R1, since it reduces the high frequency gain from 4 to unity for the MC33264D–5.0. Pick

$$C_{BYPASS} = \frac{1}{2\pi\ R1\ x\ 200\ Hz}$$

or about 0.01 µF. When doing this, the output capacitor must be increased to 3.3 µF to maintain stability. These changes reduce the output noise from 430 µV to 100 Vrms for a 100 kHz bandwidth for the 5.0 V output device. With the bypass capacitor added, noise no longer scales with output voltage so that improvements are more dramatic at higher output voltages.

TYPICAL APPLICATIONS

Figure 8. Lithium Ion Battery Cell Charger

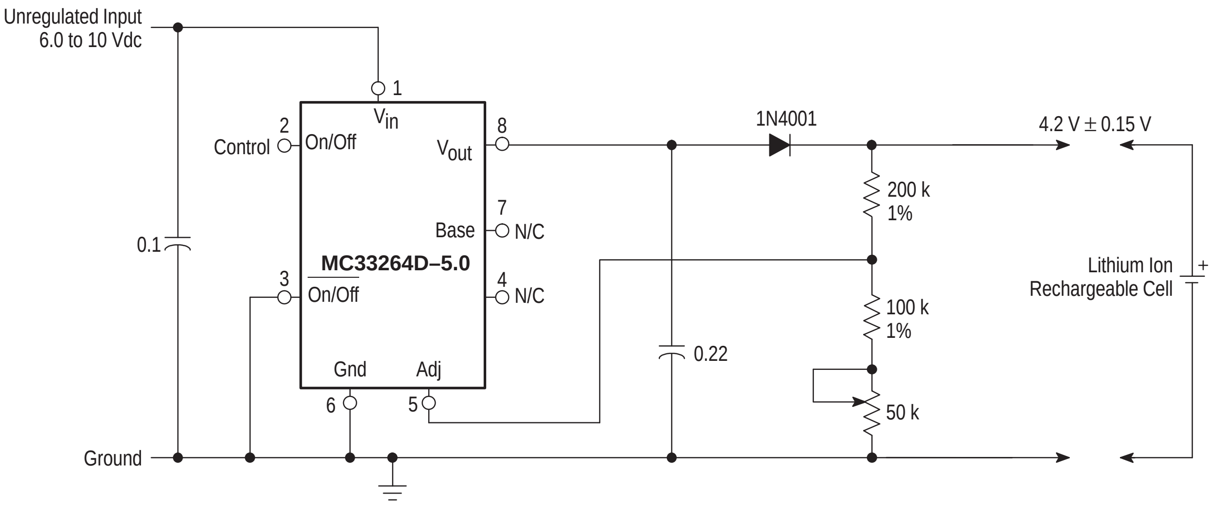


Figure 9. Low Drift Current Source

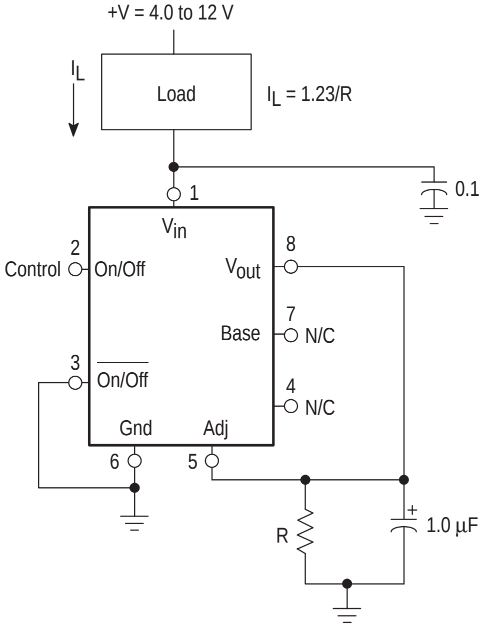


Figure 10. 2.0 Ampere Low Dropout Regulator

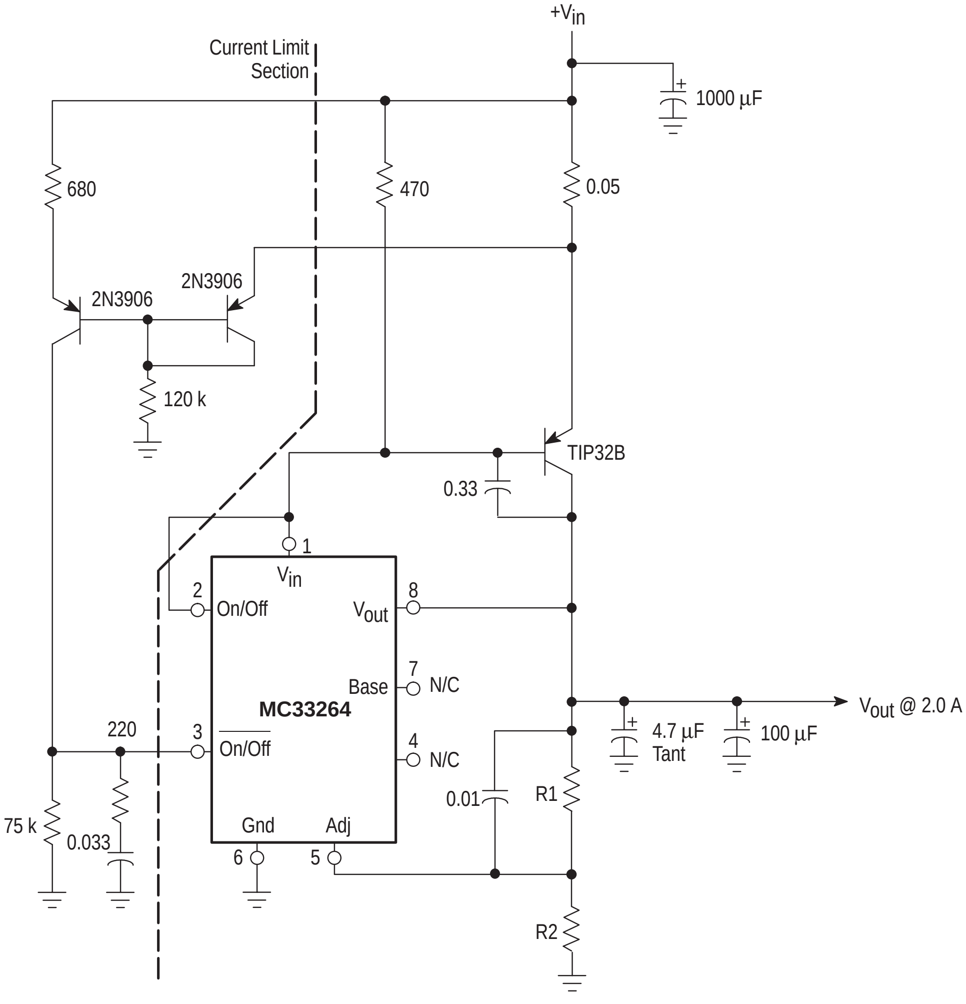


Figure 11. Low Battery Disconnect

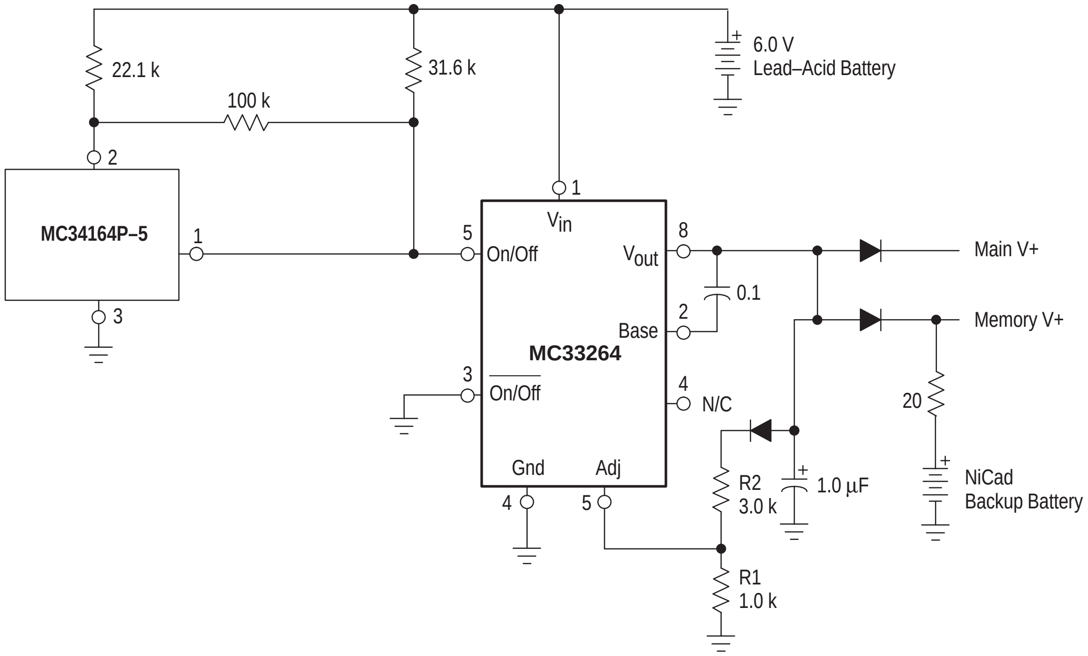
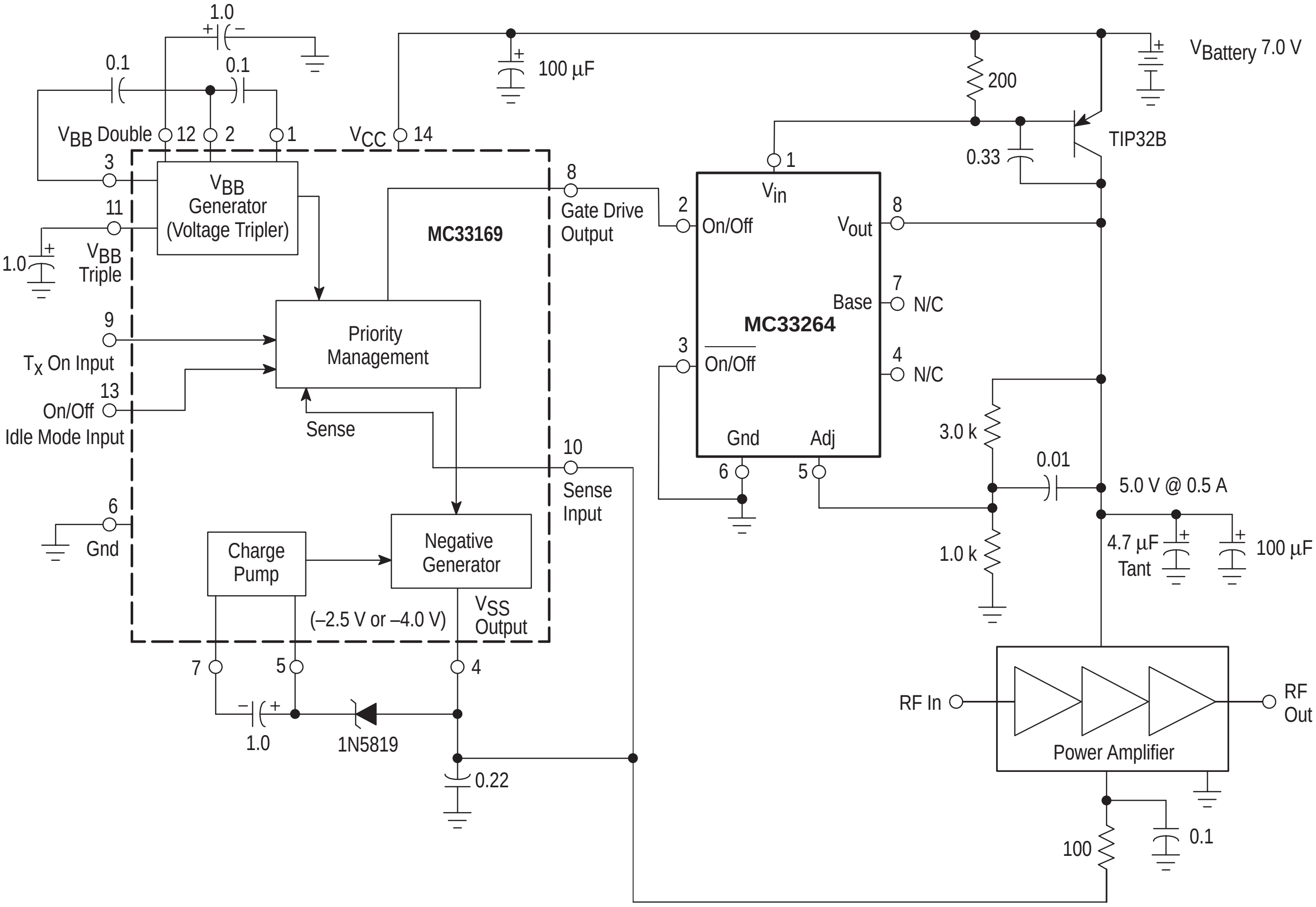


Figure 12. RF Amplifier Supply



MOTOROLA

MC33267

Low Dropout Regulator

The MC33267 is a positive fixed 5.0 V regulator that is specifically designed to maintain proper voltage regulation with an extremely low input–to–output voltage differential. This device is capable of supplying output currents in excess of 500 mA and contains internal current limiting and thermal shutdown protection. Also featured is an on–chip power–up reset circuit that is ideally suited for use in microprocessor based systems. Whenever the regulator output voltage is below nominal, the reset output is held low. A programmable time delay is initiated after the regulator has reached its nominal level and upon timeout, the reset output is released.

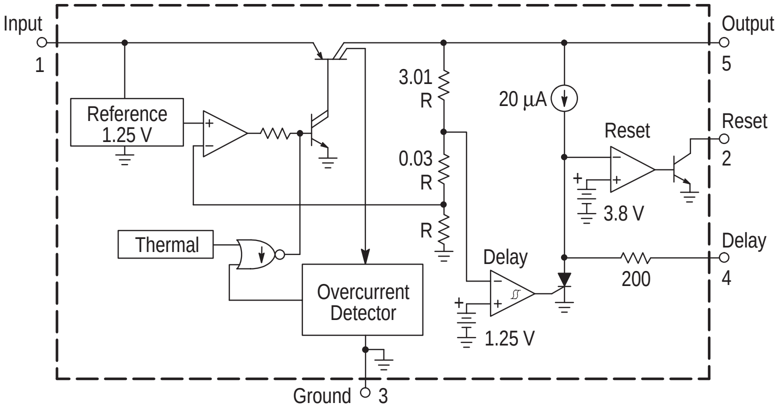
Due to the low dropout voltage specifications, the MC33267 is ideally suited for use in battery powered industrial and consumer equipment where an extension of useful battery life is desirable. This device is contained in an economical five lead TO–220 type package.

- Low Input–to–Output Voltage Differential
- Output Current in Excess of 500 mA
- On–Chip Power–Up Reset Circuit with Programmable Delay
- Internal Current Limiting with Thermal Shutdown
- Economical Five Lead TO–220 Type Packages

ORDERING INFORMATION

Device	Tested Operating Temperature Range	Package
MC33267T	T_J = –40 ° to +125°C	Plastic Power
MC33267TV		Plastic Power
MC33267D2T	T_J = –40 ° to +105°C	Surface Mount

Representative Block Diagram

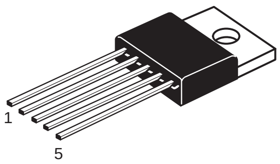


This device contains 37 active transistors.

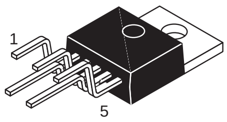
LOW DROPOUT REGULATOR with POWER–UP RESET

SEMICONDUCTOR TECHNICAL DATA

Pin 1. V_{CC} Input
2. Reset
3. Ground
4. Delay
5. Output

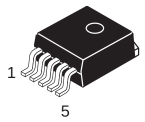


T SUFFIX
PLASTIC PACKAGE
CASE 314D



TV SUFFIX
PLASTIC PACKAGE
CASE 314B

Heatsink surface connected to Pin 3.



D2T SUFFIX
PLASTIC PACKAGE
CASE 936A
(D^2PAK)

Heatsink surface (shown as terminal 6 in case outline drawing) is connected to Pin 3.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage Range	V_{in}	– 20 to + 40	Vdc
Delay Voltage Range	V_{DLYR}	– 0.3 to V_O	V
Delay Sink Current	$I_{DLY(sink)}$	25	mA
Reset Voltage Range	V_{RR}	– 0.3 to +15	V
Reset Sink Current	$I_{R(sink)}$	50	mA
Power Dissipation			
Case 314B and 314D (TO–220 Type)			
T_A = 25°C	P_D	Internally Limited	W
Thermal Resistance, Junction–to–Ambient	$R_{\theta JA}$	62.5	°C/W
Thermal Resistance, Junction–to–Case	$R_{\theta JC}$	4.0	°C/W
Case 936A (D^2PAK) [Note 1]			
T_A = 90°C	P_D	Internally Limited	W
Thermal Resistance, Junction–to–Ambient	$R_{\theta JA}$	70	°C/W
Thermal Resistance, Junction–to–Case	$R_{\theta JC}$	5.0	°C/W
Operating Junction Temperature Range	T_J	–40 to +150	°C
Storage Temperature Range	T_{stg}	–55 to +150	°C

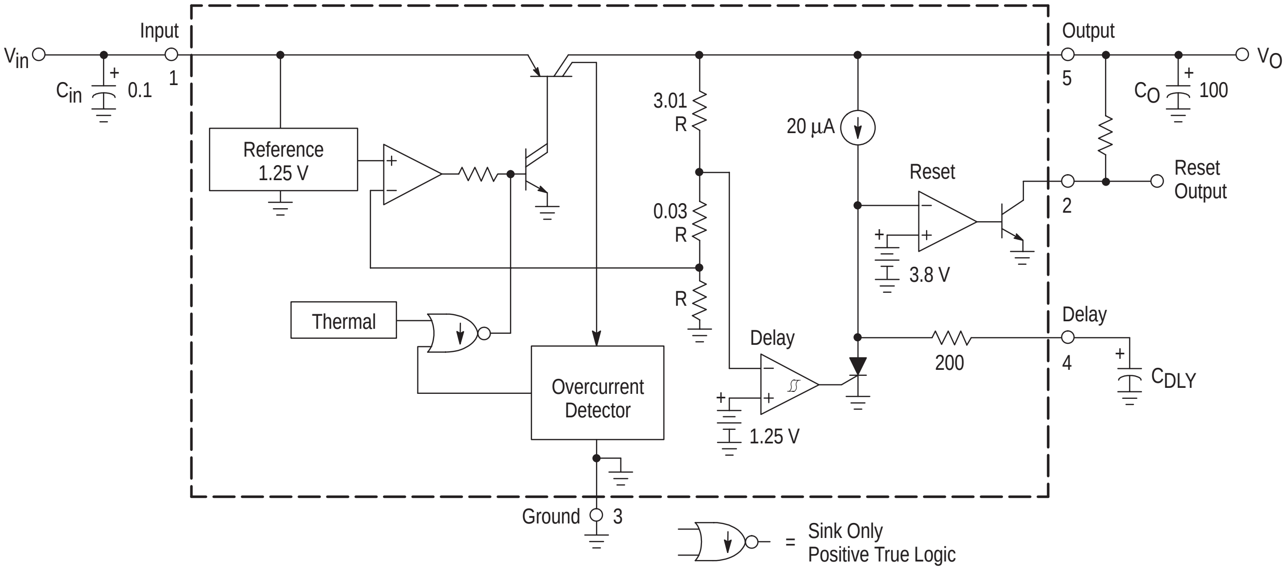
NOTE: 1. D^2PAK Junction–to–Ambient Thermal Resistance is for vertical mounting. Refer to Figure 7 for board mounted thermal resistance.

ELECTRICAL CHARACTERISTICS (V_{in} = 14.4 V, I_O = 5.0 mA, C_O = 100 µF, $C_{O(ESR)} \leq 0.3\ \Omega$, T_J = 25°C (Note 2), unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (I_O = 5.0 mA to 500 mA, V_{in} = 6.0 V to 28 V)	V_O				V
T_J = 25°C		4.95	5.05	5.15	
T_J = – 40° to +125°C		4.9	–	5.2	
Line Regulation (V_{in} = 6.0 V to 26 V)	Reg_{line}	–	3.0	50	mV
Load Regulation (I_O = 5.0 mA to 500 mA)	Reg_{load}	–	1.0	50	mV
Bias Current	I_B				mA
I_O = 0 mA		–	12	20	
I_O = 150 mA		–	22	40	
I_O = 500 mA		–	100	200	
I_O = 500 mA, V_{in} = 6.2 V		–	120	300	
Ripple Rejection (f = 120 Hz, V_{in} = 7.0 V to 17 V, I_O = 350 mA, C_O = 100 µF)	RR	60	80	–	dB
Dropout Voltage (I_O = 500 mA)	$V_{in} – V_O$	–	0.58	0.8	V
Delay Comparator Threshold (V_O Decreasing)	$V_{th(DLY)}$	4.8	V_O – 0.15	V_O – 0.08	V
Delay Pin Source Current	$I_{DLY(source)}$	12	20	28	µA
Reset Comparator Threshold	$V_{th(R)}$	3.6	3.8	4.0	V
Reset Sink Saturation (I_{sink} = 10 mA)	$V_{CE(sat)}$	–	0.2	0.8	V
Reset Off–State Leakage (V_{CE} = 5.0 V)	$I_{R(leak)}$	–	0.3	10	µA

NOTE: 2. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.

Figure 1. Typical Application Circuit



APPLICATION CIRCUIT INFORMATION

The MC33267 is a low dropout, positive fixed 5.0 V, 500 mA regulator. Protection features include output current limiting and thermal shutdown. System protection consists of an on–chip power–up microprocessor reset circuit.

A typical applications circuit is shown in Figure 1. The input bypass capacitor (C_{in}) is recommended if the regulator is located an appreciable distance (≥ 4″) from the supply input filter. This will reduce the circuit's sensitivity to the input line impedance at high frequencies.

These regulators are not internally compensated and thus require an external output capacitor (C_O) for stability. The recommended capacitance is 100 µF with an equivalent series resistance (ESR) of less than 0.3 Ω. A minimum capacitance of 33 µF with a maximum ESR of 3.0 Ω can be used in applications where space is a premium, however, these limits must be observed over the entire operating temperature range of the regulator circuit.

With economical electrolytic capacitors, cold temperature operation can pose a serious stability problem. As the electrolyte freezes, around – 30°C, the capacitance will decrease and the ESR will increase drastically, causing the circuit to oscillate. Quality electrolytic capacitors with extended temperature ranges of – 40°C to + 85°C and – 55°C to +105°C are readily available. It is suggested that oven testing of the entire circuit be performed with maximum load, minimum input voltage, and minimum ambient temperature.

Figure 2 shows the reset circuit timing relationship. Note that whenever the regulator's output is less than 4.9 V, the delay capacitor (C_{DLY}) is immediately discharged, and the reset output is held in a low state. As the regulator's output voltage increases beyond 4.97 V, the delay comparator will allow the 20 µA current source to charge C_{DLY}. The reset output will go to a high state when C_{DLY} crosses the 3.8 V threshold of the reset comparator. The reset delay time is controlled by the value selected for C_{DLY}. The required system reset time is governed by the microprocessor and usually a reset signal which lasts several machine cycles is sufficient.

Figure 2. Timing Waveforms

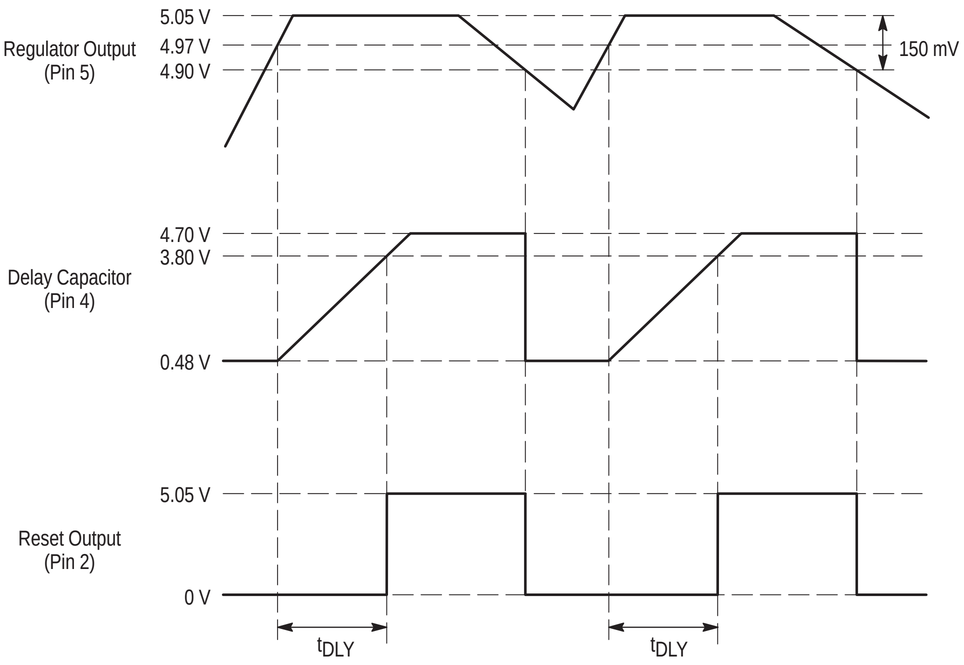


Figure 3. Reset Output versus Input Voltage

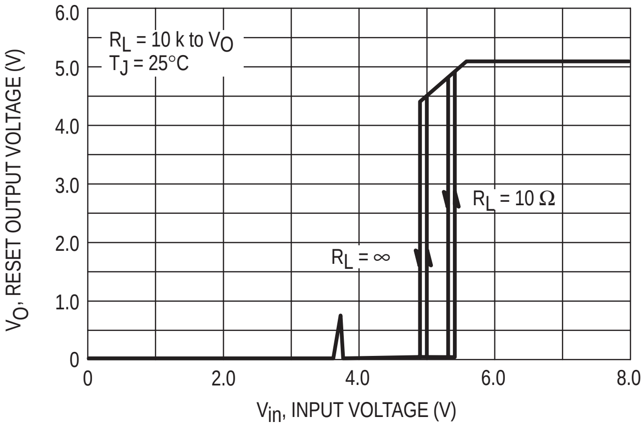


Figure 4. Output Voltage versus Input Voltage

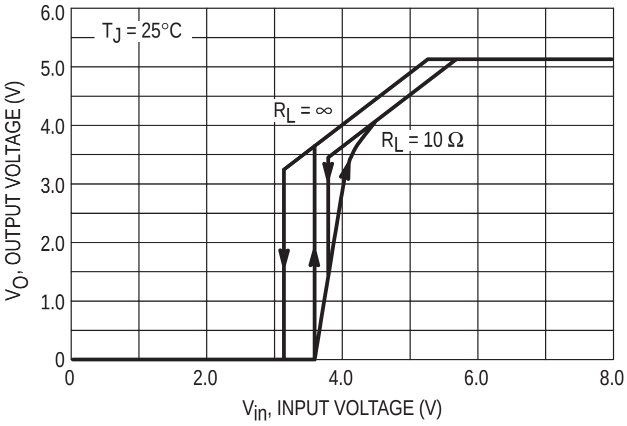


Figure 5. Reset Output versus Input Voltage

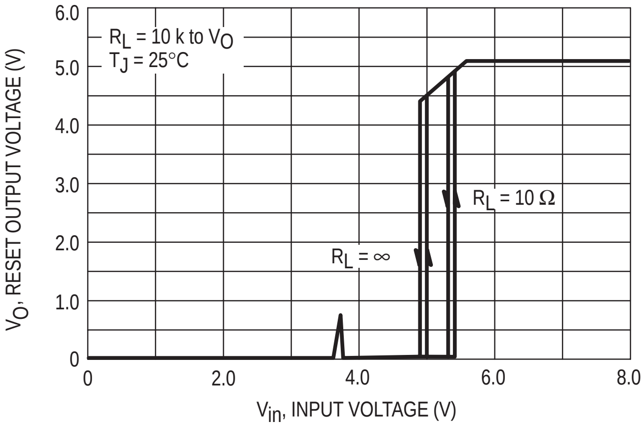


Figure 6. Output Voltage versus Input Voltage

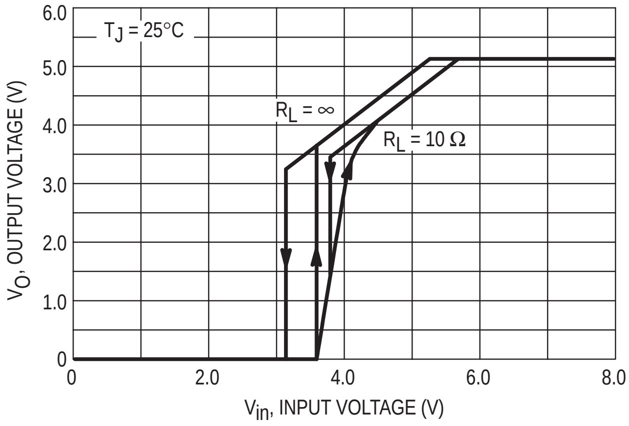
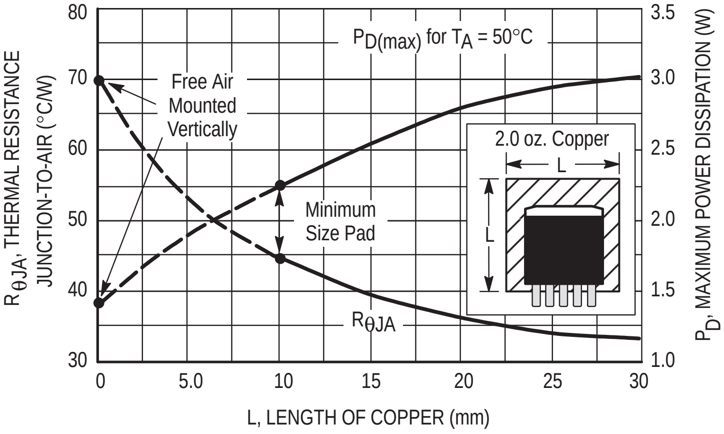


Figure 7. D²PAK Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length



MOTOROLA

MC33269

Advance Information

Low Dropout Positive Fixed and Adjustable Voltage Regulators

The MC33269 series are low dropout, medium current, fixed and adjustable, positive voltage regulators specifically designed for use in low input voltage applications. These devices offer the circuit designer an economical solution for precision voltage regulation, while keeping power losses to a minimum.

The regulator consists of a 1.0 V dropout composite PNP–NPN pass transistor, current limiting, and thermal shutdown.

- 3.3 V, 5.0 V, 12 V and Adjustable Versions
- Space Saving DPAK and SOP–8 Power Package
- 1.0 V Dropout
- Output Current in Excess of 800 mA
- Thermal Protection
- Short Circuit Protection
- Output Trimmed to 1.0% Tolerance
- No Minimum Load Requirement for Fixed Voltage Output Devices

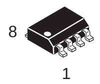
ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC33269D	$T_J = -40°$ to $+125°C$	SOP–8
MC33269DT		DPAK
MC33269T		Insertion Mount
MC33269D–3.3		SOP–8
MC33269DT–3.3		DPAK
MC33269T–3.3		Insertion Mount
MC33269D–5.0		SOP–8
MC33269DT–5.0		DPAK
MC33269T–5.0		Insertion Mount
MC33269D–12		SOP–8
MC33269DT–12		DPAK
MC33269T–12		Insertion Mount

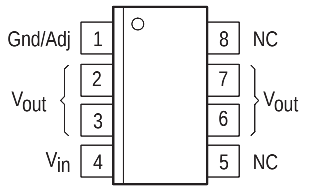
DEVICE TYPE/NOMINAL OUTPUT VOLTAGE

MC33269D	Adj	MC33269D–5.0	5.0 V
MC33269DT	Adj	MC33269DT–5.0	5.0 V
MC33269T	Adj	MC33269T–5.0	5.0 V
MC33269D–3.3	3.3 V	MC33269D–12	12 V
MC33269DT–3.3	3.3 V	MC33269DT–12	12 V
MC33269T–3.3	3.3 V	MC33269T–12	12 V

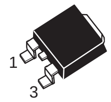
800 mA
LOW DROPOUT
THREE–TERMINAL
VOLTAGE REGULATORS



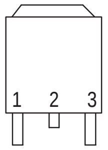
D SUFFIX
PLASTIC PACKAGE
CASE 751
(SOP–8)



(Top View)



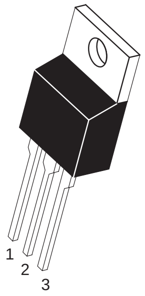
DT SUFFIX
PLASTIC PACKAGE
CASE 369A
(DPAK)



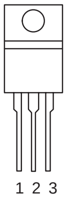
1. Gnd/Adj
2. V_{out}
3. V_{in}

(Top View)

Heatsink surface (shown as terminal 4 in case outline drawing) is connected to Pin 2.



T SUFFIX
PLASTIC PACKAGE
CASE 221A



Pin: 1. Gnd/Adj
2. V_{out}
3. V_{in}

(Top View)

Heatsink surface (shown as terminal 4 in case outline drawing) is connected to Pin 2.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Input Voltage	V_{in}	20	V
Power Dissipation			
Case 369A (DPAK)			
T_A = 25°C	P_D	Internally Limited	W
Thermal Resistance, Junction–to–Ambient	θ_{JA}	92	°C/W
Thermal Resistance, Junction–to–Case	θ_{JC}	6.0	°C/W
Case 751 (SOP–8)			
T_A = 25°C	P_D	Internally Limited	W
Thermal Resistance, Junction–to–Ambient	θ_{JA}	160	°C/W
Thermal Resistance, Junction–to–Case	θ_{JC}	25	°C/W
Case 221A			
T_A = 25°C	P_D	Internally Limited	W
Thermal Resistance, Junction–to–Ambient	θ_{JA}	65	°C/W
Thermal Resistance, Junction–to–Case	θ_{JC}	5.0	°C/W
Operating Junction Temperature Range	T_J	–40 to +150	°C
Storage Temperature	T_{stg}	–55 to +150	°C

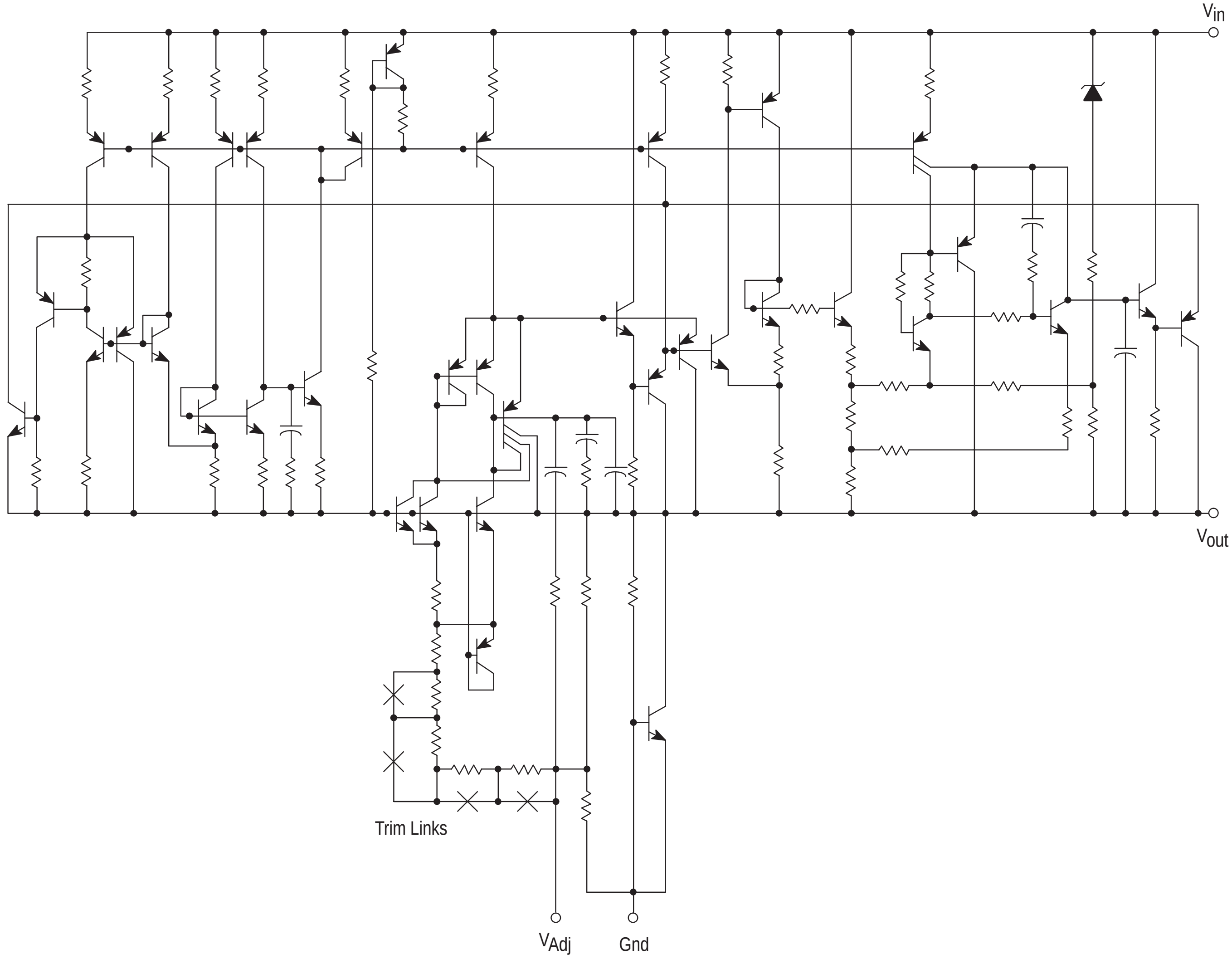
NOTE: ESD data available upon request.

ELECTRICAL CHARACTERISTICS (C_O = 10 µF, T_A = 25°C, for min/max values T_J = –40°C to +125°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (I_{out} = 10 mA, T_J = 25°C)	V_O				V
3.3 Suffix (V_{CC} = 5.3 V)		3.27	3.3	3.33	
5.0 Suffix (V_{CC} = 7.0 V)		4.95	5.0	5.05	
12 Suffix (V_{CC} = 14 V)		11.88	12	12.12	
Output Voltage (Line, Load and Temperature) (Note 1) (1.25 V ≤ V_{in} – V_{out} ≤ 15 V, I_{out} = 500 mA) (1.35 V ≤ V_{in} – V_{out} ≤ 10 V, I_{out} = 800 mA)	V_O				V
3.3 Suffix		3.23	3.3	3.37	
5.0 Suffix		4.9	5.0	5.1	
12 Suffix		11.76	12	12.24	
Reference Voltage (I_{out} = 10 mA, V_{in} – V_{out} = 2.0 V, T_J = 25°C) Adjustable	V_{ref}	1.235	1.25	1.265	V
Reference Voltage (Line, Load and Temperature) (Note 1) (1.25 V ≤ V_{in} – V_{out} ≤ 15 V, I_{out} = 500 mA) (1.35 V ≤ V_{in} – V_{out} ≤ 10 V, I_{out} = 800 mA) Adjustable	V_{ref}	1.225	1.25	1.275	V
Line Regulation (I_{out} = 10 mA, V_{in} = [V_{out} + 1.5 V] to V_{in} = 20 V, T_J = 25°C)	Reg_{line}	–	–	0.3	%
Load Regulation (V_{in} = V_{out} + 3.0 V, I_{out} = 10 mA to 800 mA, T_J = 25°C)	Reg_{load}	–	–	0.5	%
Dropout Voltage	V_{in} – V_{out}				V
(I_{out} = 500 mA)		–	1.0	1.25	
(I_{out} = 800 mA)		–	1.1	1.35	
Ripple Rejection (10 Vpp, 120 Hz Sinewave; I_{out} = 500 mA)	RR	55	–	–	dB
Current Limit (V_{in} – V_{out} = 10 V)	I_{Limit}	800	–	–	mA
Quiescent Current (Fixed Output)	I_Q	–	5.5	8.0	mA
Minimum Required Load Current	I_{Load}				mA
Fixed Output		–	–	0	
Adjustable		8.0	–	–	
Adjustment Pin Current	I_{Adj}	–	–	120	µA

NOTE 1: The MC33269–12, V_{in} – V_{out} is limited to 8.0 V maximum, because of the 20 V maximum rating applied to V_{in}.

Internal Schematic



This device contains 38 active transistors.

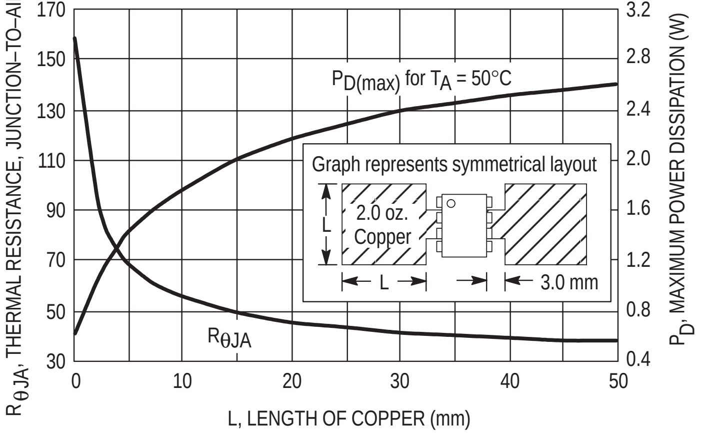


Figure 1. SOP–8 Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length

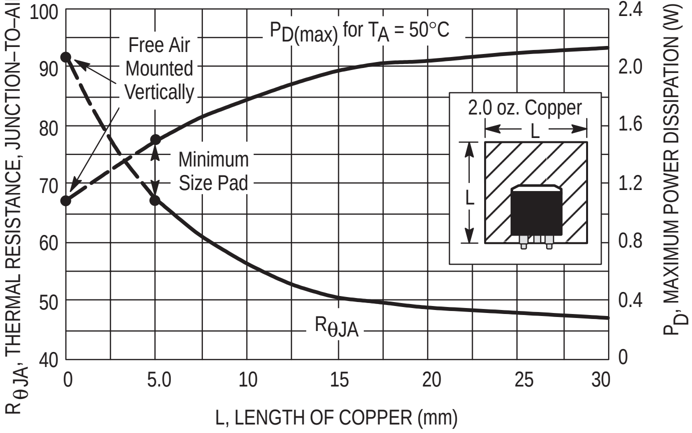


Figure 2. DPAK Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length

Figure 3. Dropout Voltage versus Output Load Current

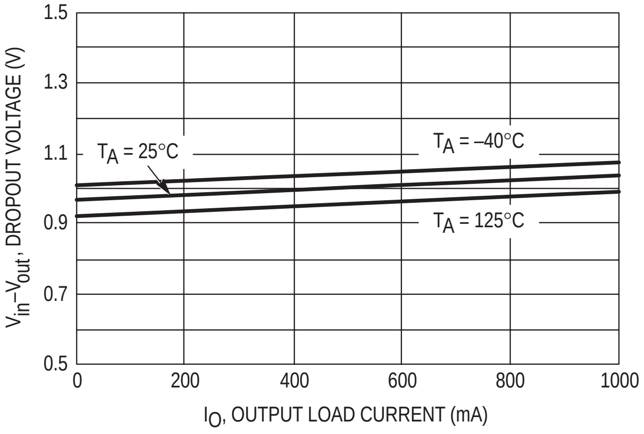


Figure 4. Transient Load Regulation

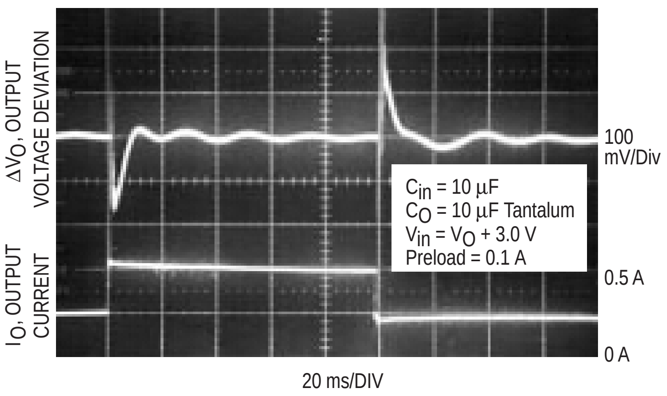


Figure 5. Dropout Voltage versus Temperature

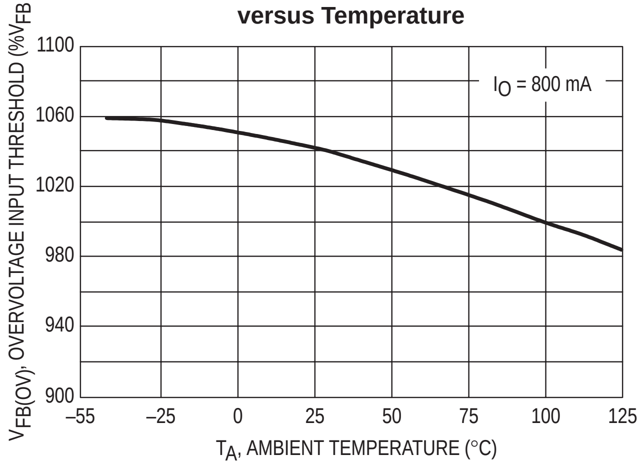


Figure 6. MC33269–XX Output DC Current versus Input–Output Differential Voltage

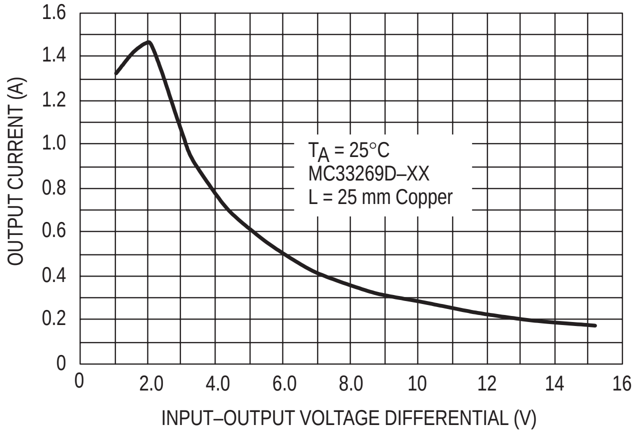


Figure 7. MC33269 Ripple Rejection versus Frequency

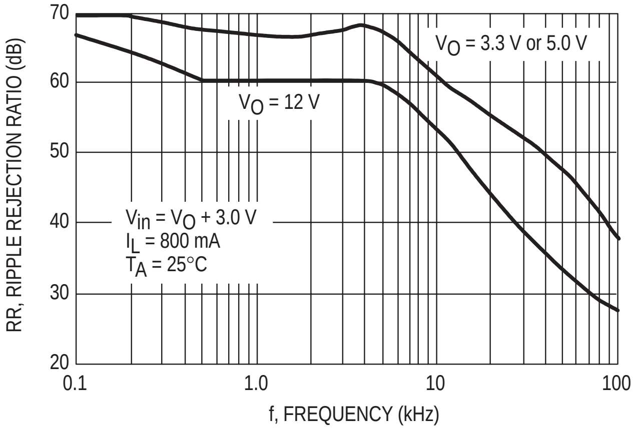
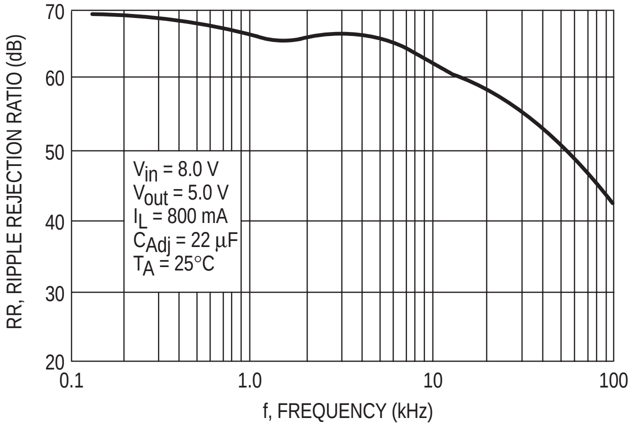


Figure 8. MC33269–ADJ Ripple Rejection versus Frequency



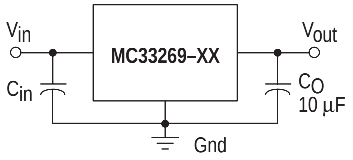
APPLICATIONS INFORMATION

Figures 9 through 13 are typical application circuits. The output current capability of the regulator is in excess of 800 mA, with a typical dropout voltage of less than 1.0 V. Internal protective features include current and thermal limiting.

The MC33269 is not internally compensated and thus requires an external output capacitor for stability. The capacitor should be at least 10 μF with an equivalent series resistance (ESR) of less than 10 Ω over the anticipated operating temperature range. With economical electrolytic capacitors, cold temperature operation can pose a problem. As temperature decreases, the capacitance also decreases and the ESR increases, which could cause the circuit to oscillate. Solid tantalum capacitors may be a better choice if small size is a requirement. Also capacitance and ESR of a solid tantalum capacitor is more stable over temperature. An input bypass capacitor is recommended to improve transient response or if the regulator is connected to the supply input filter with long wire lengths. This will reduce the circuit's sensitivity to the input line impedance at high frequencies. A 0.33 μF or larger tantalum, mylar, ceramic, or other capacitor having low internal impedance at high frequencies should be chosen. The bypass capacitor should be mounted with shortest possible lead or track length directly across the regulator's input terminals. **Applications should be tested over all operating conditions to insure stability.**

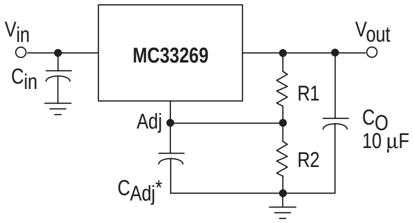
Internal thermal limiting circuitry is provided to protect the integrated circuit in the event that the maximum junction temperature is exceeded. When activated, typically at 170°C, the output is disabled. There is no hysteresis built into the thermal limiting circuit. As a result, if the device is overheating, the output will appear to be oscillating. This feature is provided to prevent catastrophic failures from accidental device overheating. **It is not intended to be used as a substitute for proper heatsinking.**

Figure 9. Typical Fixed Output Application



An input capacitor is not necessary for stability, however it will improve the overall performance.

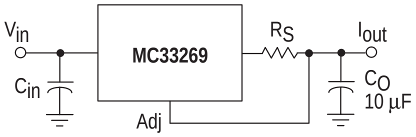
Figure 10. Typical Adjustable Output Application



$$V_{out} = 1.25 \left(1 + \frac{R2}{R1}\right) + I_{Adj}\, R2$$

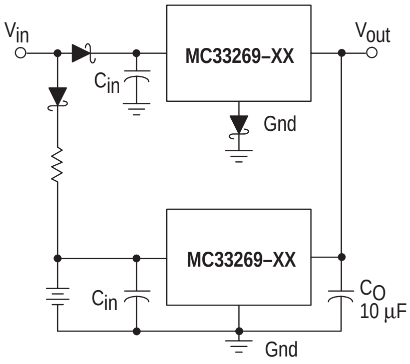
*C_{Adj} is optional, however it will improve the ripple rejection. The MC34269 develops a 1.25 V reference voltage between the output and the adjust terminal. Resistor R1, operates with constant current to flow through it and resistor R2. This current should be set such that the Adjust Pin current causes negligible drop across resistor R2. The total current with minimum load should be greater than 8.0 mA.

Figure 11. Current Regulator



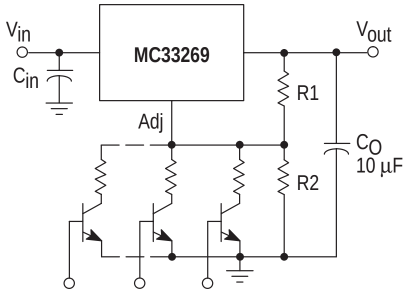
$$I_{out} = \frac{1.25}{R_S}$$

Figure 12. Battery Backed–Up Power Supply



The Schottky diode in series with the ground leg of the upper regulator shifts its output voltage higher by the forward voltage drop of the diode. This will cause the lower device to remain off until the input voltage is removed.

Figure 13. Digitally Controlled Voltage Regulator



R_2 sets the maximum output voltage. Each transistor reduces the output voltage when turned on.

MOTOROLA

MC33340

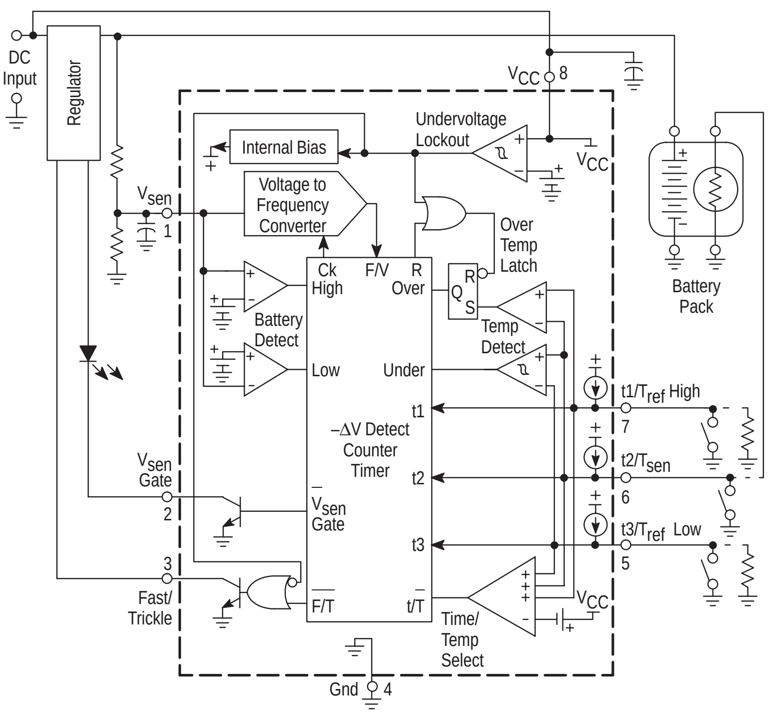
Product Preview

Battery Fast Charge Controller

The MC33340 is a monolithic control IC that is specifically designed as a fast charge controller for Nickel Cadmium (NiCd) and Nickel Metal Hydride (NiMH) batteries. This device features negative slope voltage detection as the primary means for fast charge termination. Accurate detection is ensured by an output that momentarily interrupts the charge current for precise voltage sampling. An additional secondary backup termination method can be selected that consists of either a programmable time or temperature limit. Protective features include battery over and undervoltage detection, latched over temperature detection, and power supply input undervoltage lockout with hysteresis. Provisions for entering a rapid test mode are available to enhance end product testing. This device is available in an economical 8–lead surface mount package.

- Negative Slope Voltage Detection
- Accurate Zero Current Battery Voltage Sensing
- Programmable 1 to 4 Hour Fast Charge Time Limit
- Programmable Over/Under Temperature Detection
- Battery Over and Undervoltage Fast Charge Protection
- Rapid System Test Mode
- Power Supply Input Undervoltage Lockout with Hysteresis
- Operating Voltage Range of 3.0 V to 18 V

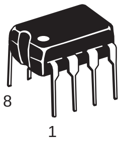
Simplified Block Diagram



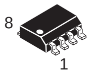
This device contains 2,512 active transistors.

BATTERY FAST CHARGE CONTROLLER

SEMICONDUCTOR TECHNICAL DATA

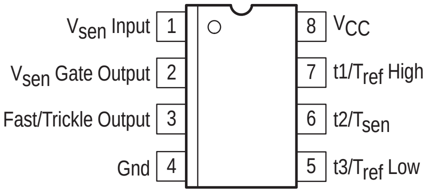


P SUFFIX
PLASTIC PACKAGE
CASE 626



D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC33340D	T_A = –25° to +85°C	SO–8
MC33340P		Plastic DIP

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage (Pin 8)	V_{CC}	18	V
Input Voltage Range			V
Time/Temperature Select (Pins 5, 6, 7)	$V_{IR(t/T)}$	–1.0 to V_{CC}	
Battery Sense, Note 1 (Pin 1)	$V_{IR(sen)}$	–1.0 to V_{CC} + 0.6 or –1.0 to 10	
V_{sen} Gate Output (Pin 2)			
Voltage	$V_{O(gate)}$	20	V
Current	$I_{O(gate)}$	50	mA
Fast/Trickle Output (Pin 3)			
Voltage	$V_{O(F/T)}$	20	V
Current	$I_{O(F/T)}$	50	mA
Thermal Resistance, Junction–to–Air	$R_{\theta JA}$		°C/W
P Suffix, DIP Plastic Package, Case 626		100	
D Suffix, SO–8 Plastic Package, Case 751		178	
Operating Junction Temperature	T_J	+150	°C
Operating Ambient Temperature (Note 2)	T_A	–25 to +85	°C
Storage Temperature	T_{stg}	–55 to +150	°C

NOTE: ESD data available upon request.

ELECTRICAL CHARACTERISTICS (V_{CC} = 6.0 V, T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies (Note 2), unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
BATTERY SENSE INPUT (Pin 1)					
Overvoltage Threshold	$V_{th(OV)}$				V
T_A = 25°C		–	2.0	–	
T_A = T_{low} to T_{high}		–	1.94 to 2.06	–	
Undervoltage Threshold	$V_{th(UV)}$				V
T_A = 25°C		–	1.0	–	
T_A = T_{low} to T_{high}		–	1.97 to 1.03	–	
Input Bias Current	I_{IB}	–	10	–	nA
Input Resistance	R_{in}	–	10	–	MΩ
TIME/TEMPERATURE INPUTS (Pins 5, 6, 7)					
Programming Inputs (V_{in} = 1.5 V)					
Input Current	I_{in}	–	–30	–	μA
Input Current Matching	ΔI_{in}	–	0.5	–	%
Input Offset Voltage, Over and Under Temperature Comparators	V_{IO}	–	5.0	–	mV
Under Temperature Comparator Hysteresis (Pin 5)	$V_{H(T)}$	–	44	–	mV
Temperature Select Threshold	$V_{th(t/T)}$	–	V_{CC} – 0.7	–	mV
INTERNAL TIMING					
Internal Clock Oscillator Frequency	f_{OSC}				kHz
T_A = 25°C					
V_{CC} = 6.0 V		–	840	–	
V_{CC} = 3.0 V to 18 V		–	693 to 987	–	
T_A = T_{low} to T_{high}					
V_{CC} = 6.0 V		–	680 to 1000	–	
V_{CC} = 3.0 V to 18 V		–	670 to 1010	–	
V_{sen} Gate Output (Pin 2)	t_{gate}				
Gate Time		–	30	–	ms
Gate Repetition Rate		–	1.25	–	s
Trickle Mode Holdoff Time from –ΔV Detection	t_{hold}	–	160	–	s

NOTES: 1. Whichever voltage is lower.
2. Tested ambient temperature range for the MC33340: T_{low} = – 25°C T_{high} = + 85°C
Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.

ELECTRICAL CHARACTERISTICS (continued) (V_{CC} = 6.0 V, T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies (Note 2), unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
V_{sen} GATE OUTPUT (Pin 2)					
Off–State Leakage Current (V_O = 20 V)	I_{off}	–	0.1	–	µA
Low State Saturation Voltage (I_{sink} = 10 mA)	V_{OL}	–	1.2	–	V
FAST/TRICKLE OUTPUT (Pin 3)					
Off–State Leakage Current (V_O = 20 V)	I_{off}	–	0.1	–	µA
Low State Saturation Voltage (I_{sink} = 10 mA)	V_{OL}	–	1.0	–	V
UNDERVOLTAGE LOCKOUT (Pin 8)					
Startup Threshold (V_{CC} Increasing)	$V_{th(on)}$	–	3.0	–	V
Hysteresis (V_{CC} Decreasing)	V_H	–	100	–	mV
TOTAL DEVICE (Pin 8)					
Power Supply Current (Pins 5, 6, 7 Open)	I_{CC}				mA
Startup (V_{CC} = 2.9 V)		–	0.65	–	
Operating (V_{CC} = 6.0 V)		–	0.61	–	

NOTES: 1. Whichever voltage is lower.
2. Tested ambient temperature range for the MC33340: T_{low} = –25°C T_{high} = +85°C
Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.

Figure 1. Battery Sense Input Thresholds versus Temperature

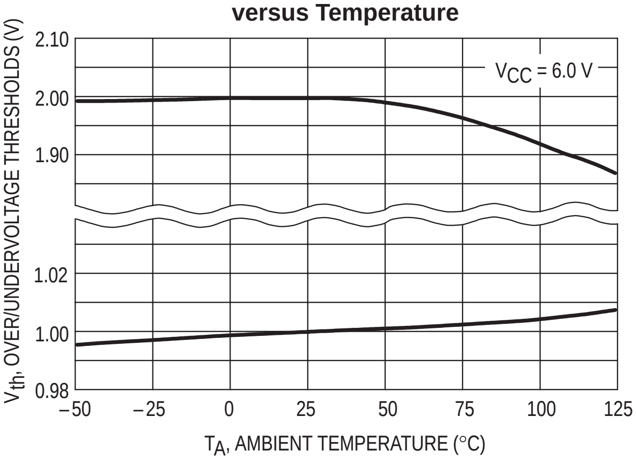


Figure 2. Oscillator Frequency versus Temperature

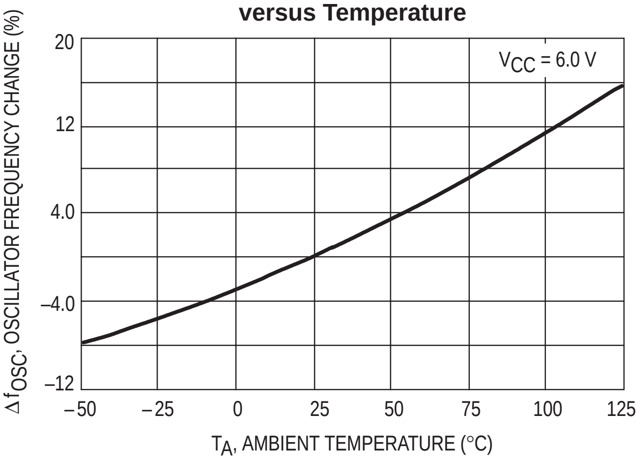


Figure 3. Temperature Select Threshold Voltage versus Temperature

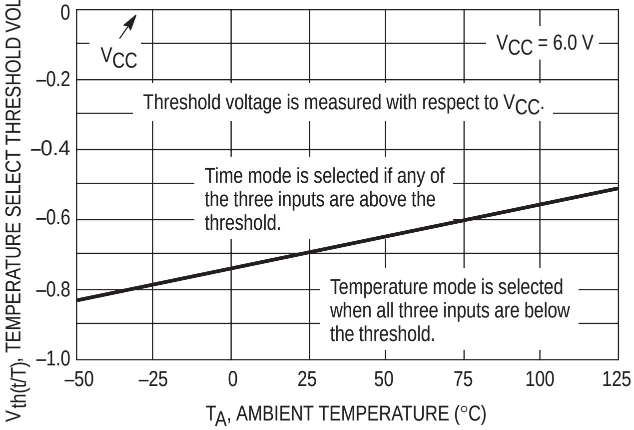


Figure 4. Saturation Voltage versus Sink Current V_{sen} Gate and Fast/Trickle Outputs

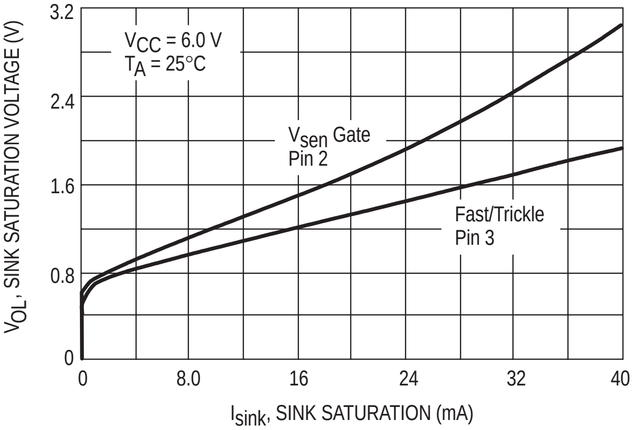


Figure 5. Undervoltage Lockout Thresholds versus Temperature

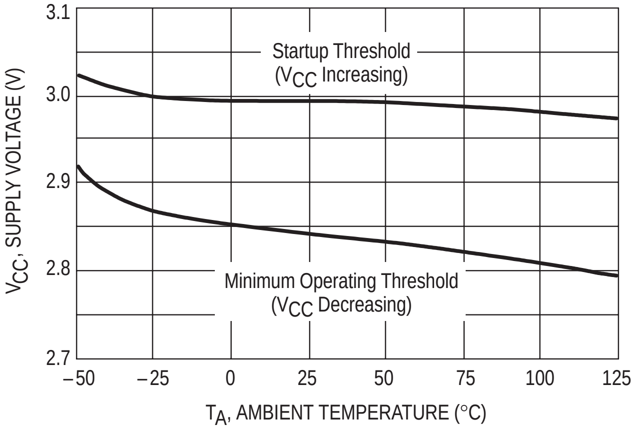
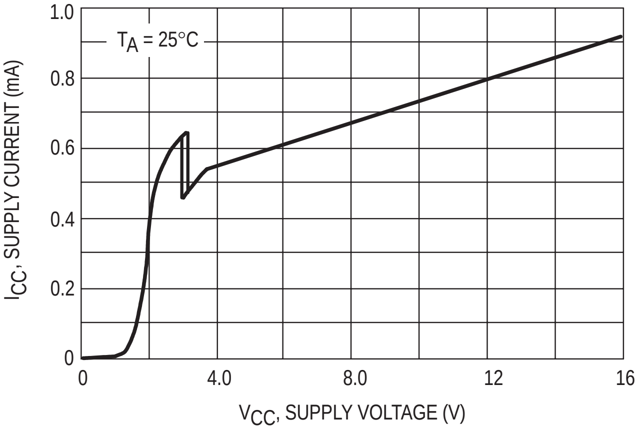


Figure 6. Supply Current versus Supply Voltage



INTRODUCTION

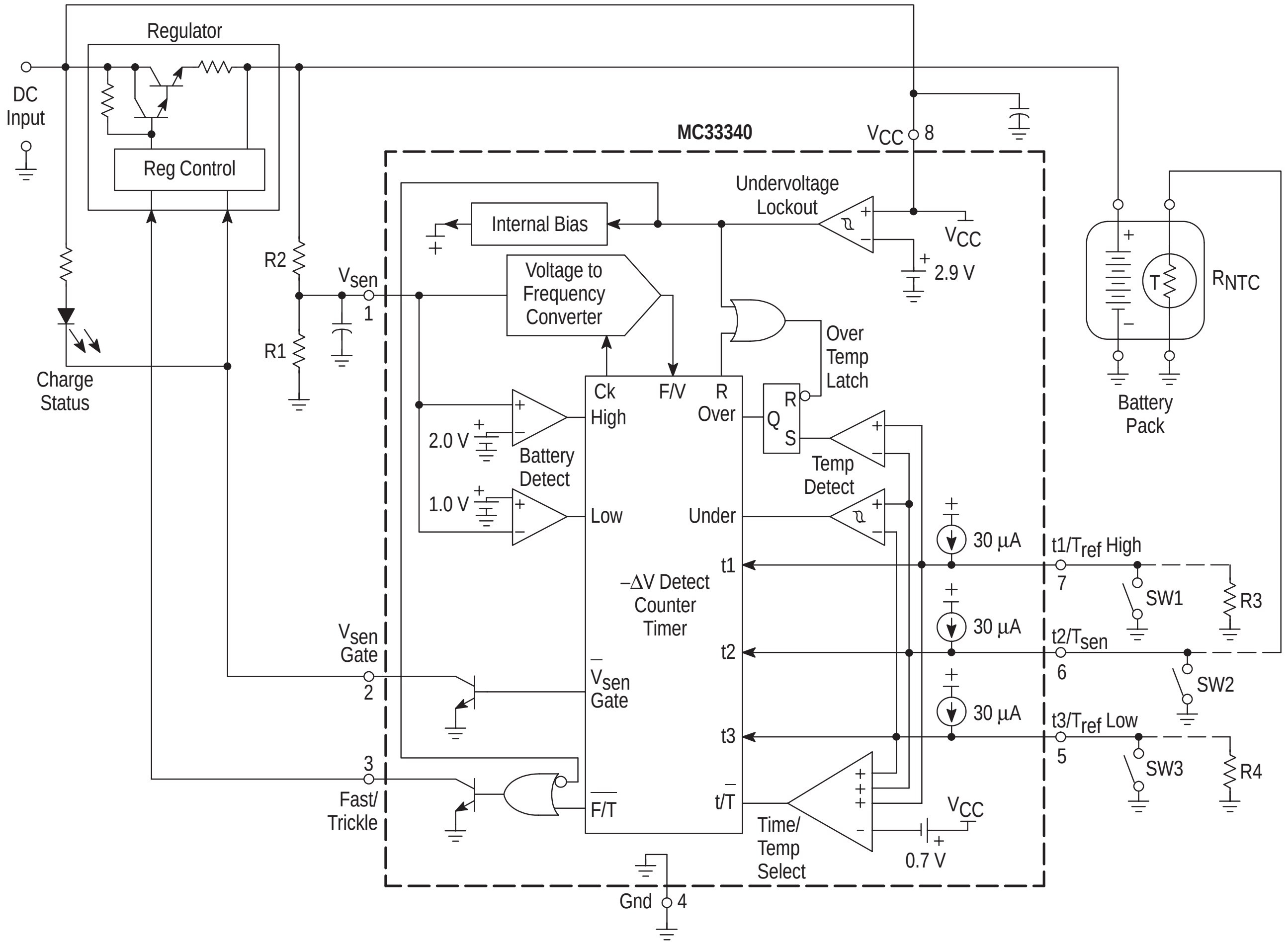
Nickel Cadmium and Nickel Metal Hydride batteries require precise charge termination control to maximize cell capacity and operating time while preventing overcharging. Overcharging can result in a reduction of battery life as well as physical harm to the end user. Since most portable applications require the batteries to be charged rapidly, a primary and usually a secondary or redundant charge sensing technique is employed into the charging system. It is also desirable to disable rapid charging if the battery voltage or temperature is either too high or too low. In order to address these issues, an economical and flexible fast charge controller was developed.

The MC33340 contains many of the building blocks and protection features that are employed in modern high performance battery charger controllers that are specifically designed for Nickel Cadmium and Nickel Metal Hydride batteries. The device is designed to interface with either primary or secondary side regulators for easy implementation of a complete charging system. A representative block diagram in a typical charging application is shown in Figure 7.

The battery voltage is monitored by the V_{sen} input that internally connects to a voltage to frequency converter and counter for detection of a negative slope in battery voltage. A timer with three programming inputs is available to provide backup charge termination. Alternatively, these inputs can be used to monitor the battery pack temperature and to set the over and under temperature limits also for backup charge termination.

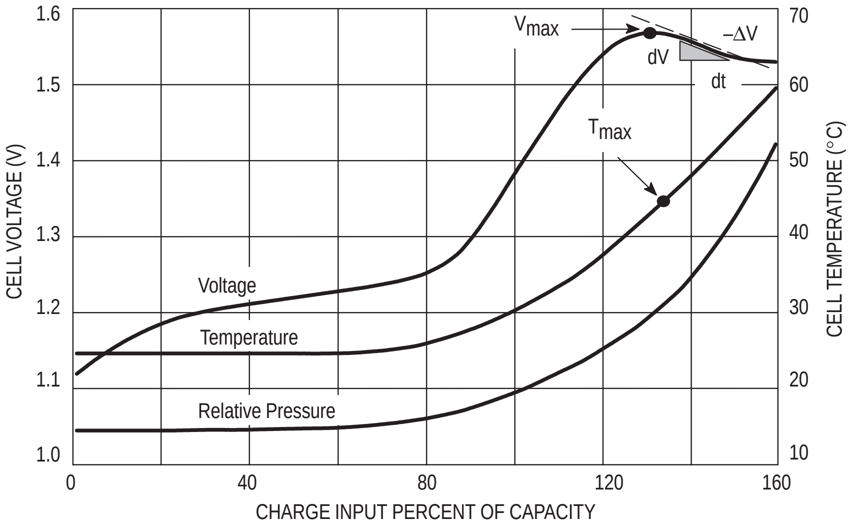
Two active low open collector outputs are provided to interface this controller with the external charging circuit. The first output furnishes a gating pulse that momentarily interrupts the charge current. This allows an accurate method of sampling the battery voltage by eliminating voltage drops that are associated with high charge currents and wiring resistances. Also, any noise voltages generated by the charging circuitry are eliminated. The second output is designed to switch the charging source between fast and trickle modes based upon the results of voltage, time, or temperature. These outputs normally connect directly to a linear or switching regulator control circuit in non–isolated primary or secondary side applications. Both outputs can be used to drive optoisolators in primary side applications that require galvanic isolation. Figure 8 shows the typical charge characteristics for NiCd and NiMh batteries.

Figure 7. Typical Battery Charging Application



$$R2 = R1\left(\frac{V_{Batt}}{V_{sen}} - 1\right)$$

Figure 8. Typical Charge Characteristics for NiCd and NiMh Batteries



OPERATING DESCRIPTION

The MC33340 starts up in the fast charge mode when power is applied to V_{CC}. A change to the trickle mode can occur as a result of three possible conditions. The first is if the V_{sen} input voltage is above 2.0 V or below 1.0 V. Above 2.0 V indicates that the battery pack is open or disconnected, while below 1.0 V indicates the possibility of a shorted or defective cell. The second condition is if a negative slope in battery voltage is detected after a minimum of 160 seconds of fast charging. This indicates that the battery pack is fully charged. The third condition is either due to the battery pack being out of a programmed temperature range, or that the preset timer period has been exceeded.

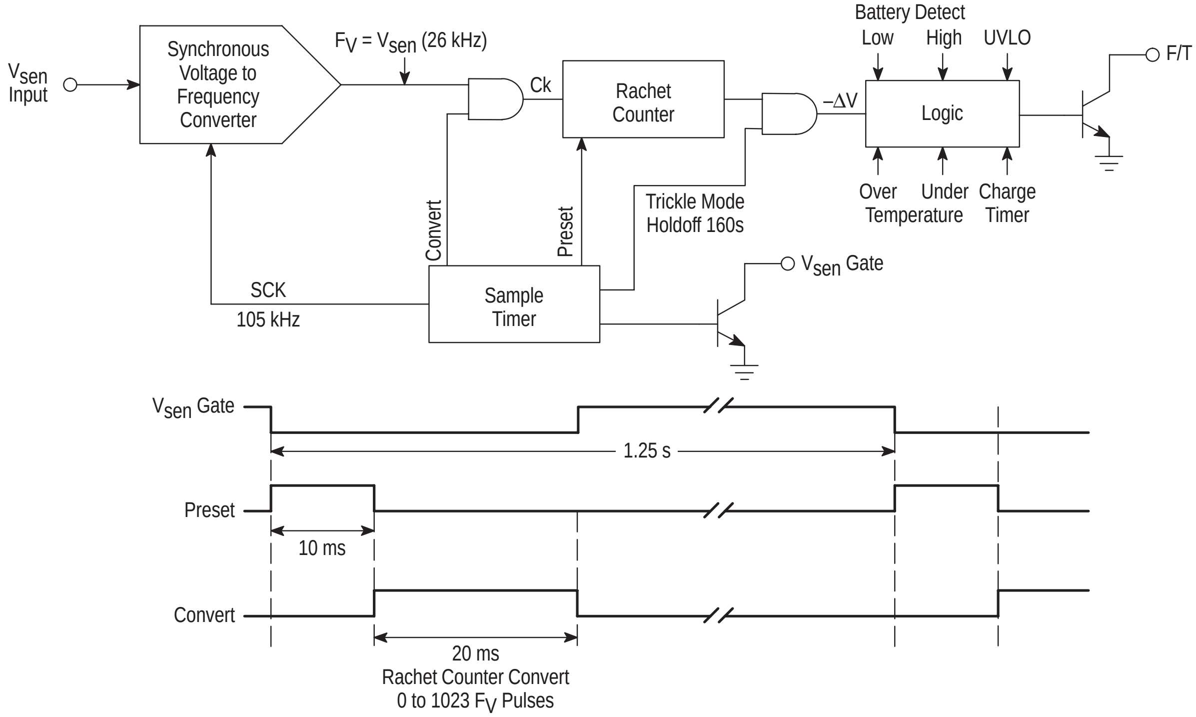
There are three conditions that will cause the controller to return from trickle to fast charge mode. The first is if the V_{sen} input voltage moved to within the 1.0 to 2.0 V range from initially being either too high or too low. The second is if the battery pack temperature moved to within the programmed temperature range, but only from initially being too cold. Third is by cycling V_{CC} off and then back on causing the internal logic to reset. A concise description of the major circuit blocks is given below.

Negative Slope Voltage Detection

A representative block diagram of the negative slope voltage detector is shown in Figure 9. It includes a Synchronous Voltage to Frequency Converter, a Sample Timer, and a Ratchet Counter. The V_{sen} pin is the input for the Voltage to Frequency Converter (VFC), and it connects to the rechargeable battery pack terminals through a resistive voltage divider. The input has an impedance of approximately 3.0 MΩ and a maximum voltage range of –1.0 V to V_{CC} + 0.6 V or 0 V to 10 V, whichever is lower. The 10 V upper limit is set by an internal zener clamp that provides protection in the event of an electrostatic discharge. The VFC is a charge–balanced synchronous type which generates output pulses at a rate of $F_V = V_{sen}$ (26 kHz).

The Sample Timer circuit provides a 105 kHz system clock signal (SCK) to the VFC. This signal synchronizes the F_V output to the other Sample Timer outputs used within the detector. At 1.25 second intervals the V_{sen} Gate output goes low for a 30 ms period. This output is used to momentarily interrupt the external charging power source so that a precise voltage measurement can be taken. As the V_{sen} Gate goes low, the internal Preset control line is driven high for 10 ms. During this time, the battery voltage at the V_{sen} input is allowed to stabilize and the previous F_V count is preloaded. At the Preset high–to–low transition, the Convert line goes high for 20 ms. This gates the F_V pulses into the ratchet counter for a comparison to the preloaded count. Since the Convert time is derived from the same clock that controls the VFC, the number of F_V pulses is independent of the clock frequency. If the new sample has more counts than were preloaded, it becomes the new peak count and the cycle is repeated 1.25 seconds later. If the new sample has two fewer counts, a less than peak voltage event has occurred, and a register is initialized. If two successive less than peak voltage events occur, the –ΔV ‘AND’ gate output goes high and the Fast/Trickle output is latched in a low state, signifying that the battery pack has reached full charge status. Negative slope voltage detection can only occur after 160 seconds have elapsed in the fast charge mode. The trickle mode holdoff time is implemented to ignore any initial drop in voltage that may occur when charging batteries that have been stored for an extended time period. The negative slope voltage detector has a maximum resolution of 2.0 V divided by 1023, or 1.955 mV per count with an uncertainty of ±1.0 count. In order to obtain maximum sensing accuracy, the R2/R1 voltage divider must be adjusted so that the V_{sen} input voltage is slightly less than 2.0 V when the battery pack is fully charged. Voltage variations due to temperature and cell manufacturing must be considered.

Figure 9. Negative Slope Voltage Detector



Fast Charge Timer

A programmable backup charge timer is available for fast charge termination. The timer is activated by the Time/Temp Select comparator, and is programmed from the t1/T_{ref} High, t2/T_{sen}, and t3/T_{ref} Low inputs. If one or more of these inputs is allowed to go above V_{CC} – 0.7 V or is left open, the comparator output will switch high, indicating that the timer feature is desired. The three inputs allow one of seven possible fast charge time limits to be selected. The programmable time limits, rounded to the nearest whole minute, are shown in Figure 10.

Over/Under Temperature Detection

A backup over/under temperature detector is available and can be used in place of the timer for fast charge termination. The timer is disabled by the Time/Temp Select comparator when each of the three programming inputs are held below V_{CC} – 0.7 V.

Temperature sensing is accomplished by placing a negative temperature coefficient (NTC) thermistor in thermal contact with the battery pack. The thermistor connects to the t2/T_{sen} input which has a 30 μA current source pull–up for developing a temperature dependent voltage. The temperature limits are set by a resistor that connects from the t1/T_{ref} High and the t3/T_{ref} Low inputs to ground. Since all three inputs contain matched 30 μA current source pull–ups, the required programming resistor values are identical to that of the thermistor at the desired over and under trip temperature. The temperature window detector is composed of two comparators with a common input that connects to the t2/T_{sen} input.

The lower comparator senses the presence of an under temperature condition. When the lower temperature limit is exceeded, the charger is switched to the trickle mode. The comparator has 44 mV of hysteresis to prevent erratic switching between the fast and trickle modes as the lower temperature limit is crossed. The amount of temperature rise to overcome the hysteresis is determined by the thermistor's rate of resistance change or sensitivity at the under temperature trip point. The required resistance change is:

$$\Delta R(T_{Low} \rightarrow T_{High}) = \frac{V_{H(T)}}{I_{in}} = \frac{44\ \text{mV}}{30\ \mu\text{A}} = 1.46\ \text{k}$$

The resistance change approximates a thermal hysteresis of 2°C with a 10 kΩ thermistor operating at 0°C. The under temperature fast charge inhibit feature can be disabled by biasing the t3/T_{ref} Low input to a voltage that is greater than that present at t2/T_{sen}, and less than V_{CC} – 0.7 V. Under extremely cold conditions, it is possible that the thermistor resistance can become too high, allowing the t2/T_{sen} input to go above V_{CC} – 0.7 V, and activate the timer. This condition can be prevented by placing a resistor in parallel with the thermistor. Note that the time/temperature threshold of V_{CC} – 0.7 V is a typical value at room temperature. Refer to the Electrical Characteristics table and to Figure 3 for additional information.

The upper comparator senses the presence of an over temperature condition. When the upper temperature limit is exceeded, the comparator output sets the Over Temperature Latch and the charger is switched to trickle mode. Once the latch is set, the charger cannot be returned to fast charge, even after the temperature falls below the limit. This feature prevents the battery pack from being continuously temperature cycled and overcharged. The latch can be reset by removing and reconnecting the battery pack or by cycling the power supply voltage.

If the charger does not require either the time or temperature backup features, they can both be easily disabled. This is accomplished by biasing the t3/T_{ref} Low input to a voltage greater than t2/T_{sen}, and by grounding the t1/T_{ref} High input. Under these conditions, the Time/Temp Select comparator output is low, indicating that the temperature mode is selected, and that the t2/T_{sen} input is biased within the limits of an artificial temperature window.

Operating Logic

The order of events in the charging process is controlled by the logic circuitry. Each event is dependent upon the input conditions and the chosen method of charge termination. A table summary containing all of the possible operating modes is shown in Figure 11.

Figure 10. Fast Charge Backup Termination Time/Temperature Limit

Backup Termination Mode	Programming Inputs			Time Limit Fast Charge (Minutes)
	t3/T_{ref} Low (Pin 5)	t2/T_{sen} (Pin 6)	t1/T_{ref} High (Pin 7)	
Time	Open	Open	Open	256
Time	Open	Open	Gnd	224
Time	Open	Gnd	Open	192
Time	Open	Gnd	Gnd	160
Time	Gnd	Open	Open	128
Time	Gnd	Open	Gnd	96
Time	Gnd	Gnd	Open	64
Temperature	0 V to V_{CC} – 0.7 V	0 V to V_{CC} – 0.7 V	0 V to V_{CC} – 0.7 V	Timer Disabled

Figure 11. Controller Operating Mode Table

Input Condition	Controller Operation
V_{sen} Input Voltage: >1.0 V and <2.0 V	The divided down battery pack voltage is within the fast charge voltage range. The charger switches from trickle to fast charge mode as V_{sen} enters this voltage range, and the reset signal that was applied to the timer and the over temperature latch is now released.
>1.0 V and <2.0 V with two consecutive –ΔV events detected after 160 s	The battery pack has reached full charge and the charger switches from fast to a latched trickle mode. A reset signal must be applied and then released for the charger to switch back to the fast mode. The reset signal is applied when either V_{sen} <1.0 V or >2.0 V, or V_{CC} <2.8 V. A signal is released when both V_{sen} >1.0 V and <2.0 V, and V_{CC} >3.0 V.
<1.0 V or >2.0 V	The divided down battery pack voltage is outside of the fast charge voltage range. The charger switches from fast to trickle mode, and a reset signal is applied to the timer and over temperature latch.
Timer Backup: Within time limit	The timer has not exceeded the programmed limit. The charger will be in fast charge mode if V_{sen} and V_{CC} are within their respective operating limits.
Beyond time limit	The timer has exceeded the programmed limit. The charger switches from fast to a latched trickle mode.
Temperature Backup: Within limits	The battery pack temperature is within the programmed limits. The charger will be in fast charge mode if V_{sen} and V_{CC} are within their respective operating limits.
Below lower limit	The battery pack temperature is below the programmed lower limit. The charger will stay in trickle mode until the lower temperature limit is exceeded. When exceeded, the charger will switch from trickle to fast charge mode.
Above upper limit	The battery pack temperature has exceeded the programmed upper limit. The charger switches from fast to a latched trickle mode. A reset signal must be applied and then released for the charger to switch back to the fast charge mode. A reset signal is applied when either V_{sen} <1.0 V or >2.0 V, or V_{CC} <2.8 V, and is released when both V_{sen} >1.0 V and <2.0 V, and V_{CC} >3.0 V.
Power Supply Voltage: V_{CC} >3.0 V and <18 V	This is the nominal power supply operating voltage range. The charger will be in fast charge mode if V_{sen}, and temperature backup or timer backup are within their respective operating limits.
V_{CC} >0.6 V and <2.8 V	The undervoltage lockout comparator will be activated and the charger will be in trickle mode. A reset signal is applied to the timer and over temperature latch.

Testing

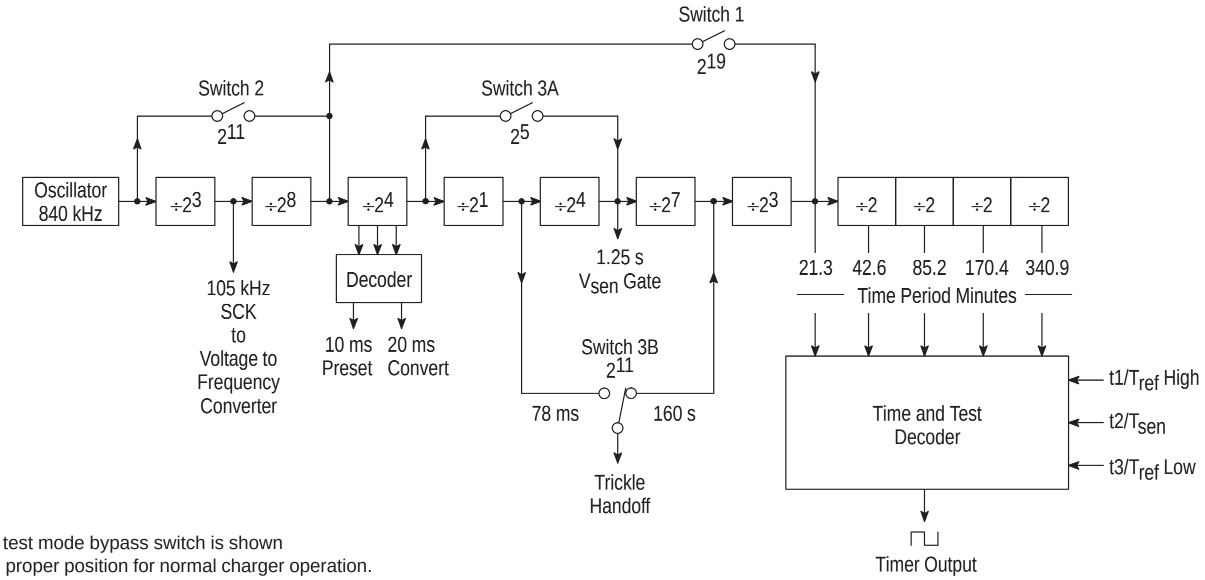
Under normal operating conditions, it would take 256 minutes to verify the operation of the 34 stage ripple counter used in the timer. In order to significantly reduce the test time, three digital switches were added to the circuitry and are used to bypass selected divider stages. Entering each of the test modes without requiring additional package pins or affecting normal device operation proved to be challenging. Refer to the timer functional block diagram in Figure 12.

Switch 1 bypasses 19 divider stages to provide a 524,288 times speedup of the clock. This switch is enabled when the V_{sen} input falls below 1.0 V. Verification of the programmed fast charge time limit is accomplished by measuring the propagation delay from when the V_{sen} input falls below 1.0 V, to when the F/T output changes from a high–to–low state. The 64, 96, 128, 160, 192, 224 and 256 minute timeouts will now correspond to 7.3, 11, 14.6, 18.3, 22, 25.6 and 29.3 ms delays. It is possible to enter this test mode during operation if the equivalent battery pack voltage was to fall below 1.0 V. This will not present a problem since the device would normally switch from fast to trickle mode under these conditions, and the relatively short variable time delay would be transparent to the user.

Switch 2 bypasses 11 divider stages to provide a 2048 times speedup of the clock. This switch is necessary for testing the 19 stages that were bypassed when switch 1 was enabled. Switch 2 is enabled when the V_{sen} input falls below 1.0 V and the $t1/T_{ref}$ Low input is biased at –100 mV. Verification of the 19 stages is accomplished by measuring a nominal propagation delay of 308 ms from when the V_{sen} input falls below 1.0 V, to when the F/T output changes from a high–to–low state.

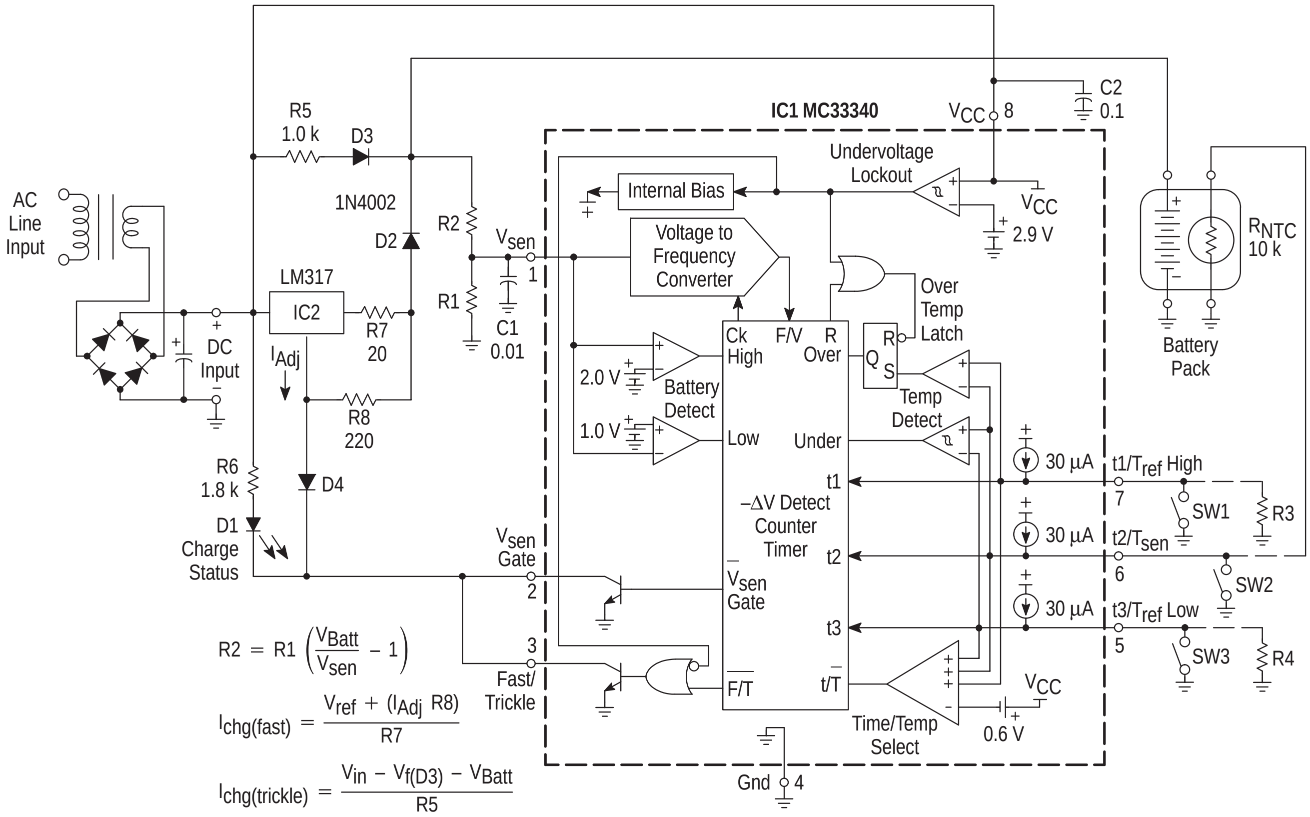
Switch 3 is a dual switch consisting of sections “A” and “B”. Section “A” bypasses 5 divider stages to provide a 32 times speedup of the V_{sen} gate signal that is used in sampling the battery voltage. This speedup allows faster test verification of two successive –ΔV events. Section “B” bypasses 11 divider stages to provide a 2048 speedup of the trickle mode holdoff timer. Switches 3A and 3B are both activated when the $t1/T_{ref}$ Low input is biased at –100 mV with respect to Pin 4. Activation results in a reduction of the V_{sen} gate sample rate from 1.25 s to 39 ms, and a trickle mode holdoff time of 160 s to 68 ms.

Figure 12. Timer Functional Block Diagram



Each test mode bypass switch is shown
in the proper position for normal charger operation.

Figure 13. Line Isolated Linear Regulator Charger



$$R2 = R1\left(\frac{V_{Batt}}{V_{sen}} - 1\right)$$

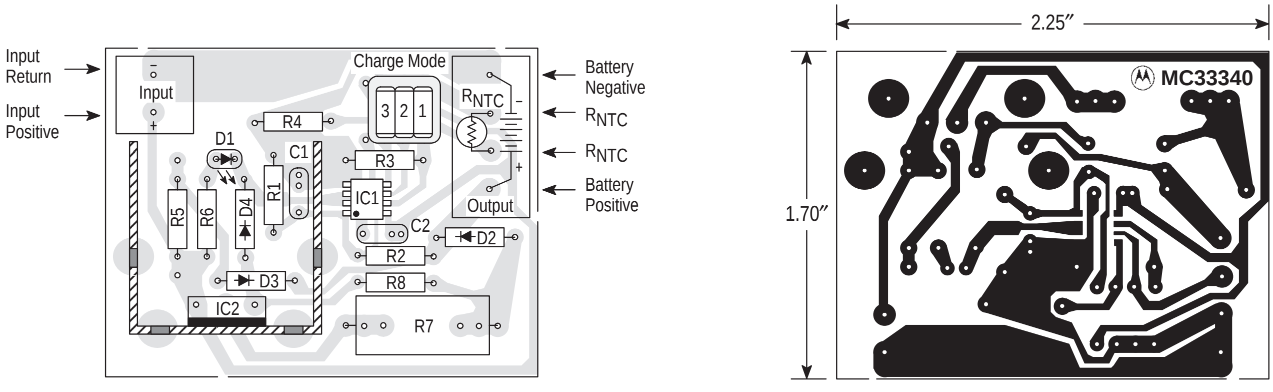
$$I_{chg(fast)} = \frac{V_{ref} + (I_{Adj}\ R8)}{R7}$$

$$I_{chg(trickle)} = \frac{V_{in} - V_{f(D3)} - V_{Batt}}{R5}$$

This application combines the MC33340 with an adjustable three terminal regulator to form an isolated secondary side battery charger. Regulator IC2 operates as a constant current source with R7 setting the fast charge level. The trickle charge level is set by R5. The R2/R1 divider should be adjusted so that the V_{sen} input is less than 2.0 V when the batteries are fully charged. The printed circuit board shown below will accept the several TO–220 style heatsinks for IC2 and are all manufactured by AAVID Engineering Inc.

AAVID #	θ_{SA} °C/W
592502B03400	24.0
593002B03400	14.0
590302B03600	9.2

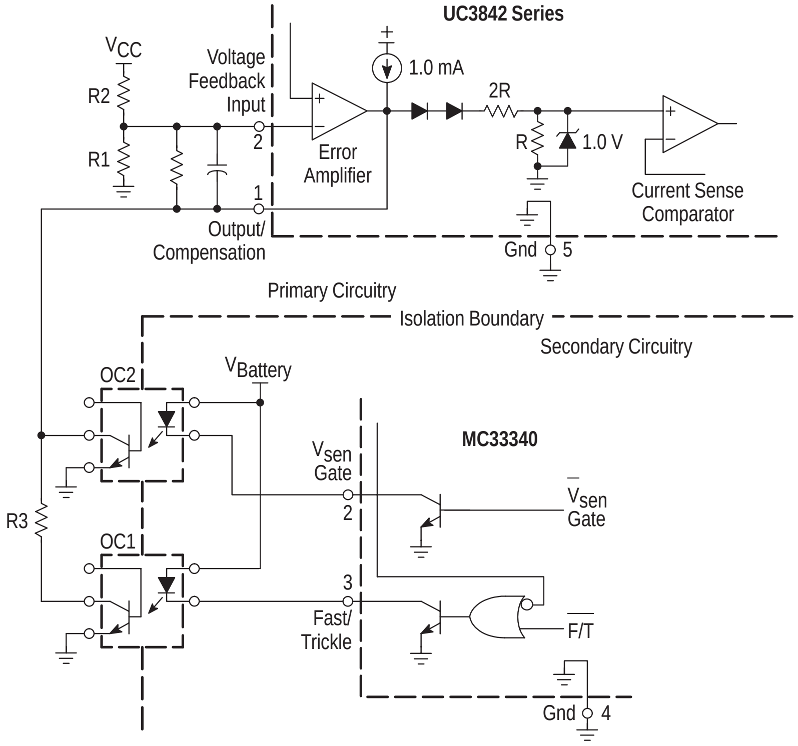
Figure 14. Printed Circuit Board and Component Layout (Circuit of Figure 13)



(Top View)

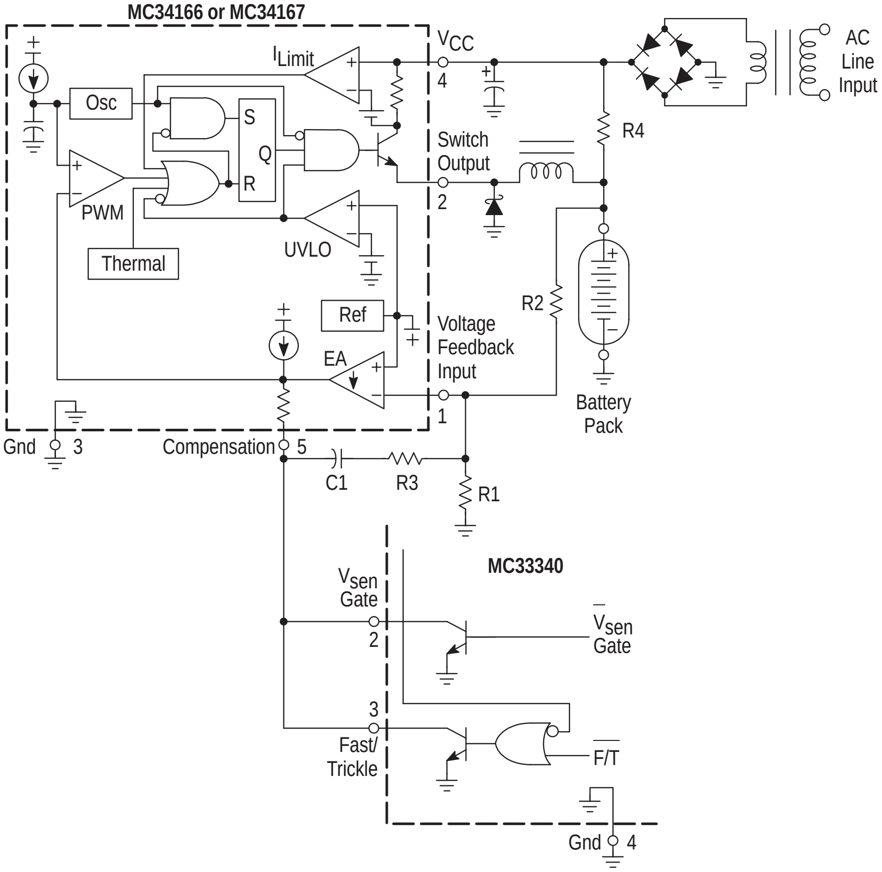
(Bottom View)

Figure 15. Line Isolated Switch Mode Charger



The MC33340 can be combined with any of the devices in the UC3842 family of current mode controllers to form a switch mode battery charger. In this example, optocouplers OC1 and OC2 are used to provide isolated control signals to the UC3842. During battery voltage sensing, OC2 momentarily grounds the Output/Compensation pin, effectively turning off the charger. When fast charge termination is reached, OC1 turns on, and grounds the lower side of R3. This reduces the peak switch current threshold of the Current Sense Comparator to a programmed trickle current level. For additional converter design information, refer to the UC3842 and UC3844 device family data sheets.

Figure 16. Switch Mode Fast Charger



The MC33340 can be used to control the MC34166 or MC34167 power switching regulators to produce an economical and efficient fast charger. These devices are capable of operating continuously in current limit with an input voltage range of 7.5 to 40 V. The typical charging current for the MC34166 and MC34167 is 4.3 A and 6.5 A respectively. Resistors R2 and R1 are used to set the battery pack fast charge float voltage. If precise float voltage control is not required, components R1, R2, R3 and C1 can be deleted, and Pin 1 must be grounded. The trickle current level is set by resistor R4. It is recommended that a redundant charge termination method be employed for end user protection. This is especially true for fast charger systems. For additional converter design information, refer to the MC34166 and MC34167 data sheets.

MOTOROLA

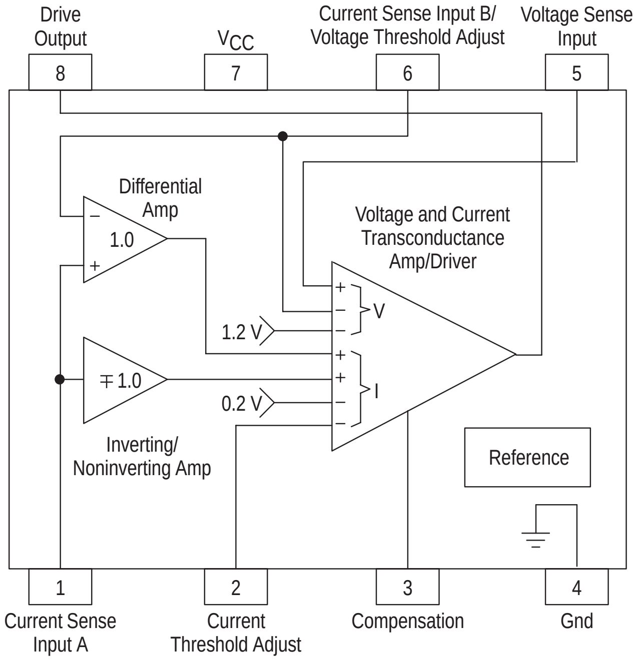
Product Preview

Power Supply Battery Charger Regulation Control Circuit

The MC33341 is a monolithic regulation control circuit that is specifically designed to close the voltage and current feedback loops in power supply and battery charger applications. This device features the unique ability to perform source high–side, load high–side, source low–side and load low–side current sensing, each with either an internally fixed or externally adjustable threshold. The various current sensing modes are accomplished by a means of selectively using the internal differential amplifier, inverting amplifier, or a direct input path. Positive voltage sensing is performed by an internal voltage amplifier. The voltage amplifier threshold is internally fixed and can be externally adjusted in all low–side current sensing applications. An active high drive output is provided to directly interface with economical optoisolators for isolated output power systems. This device is available in 8–lead dual–in–line and surface mount packages.

- Differential Amplifier for High–Side Source and Load Current Sensing
- Inverting Amplifier for Source Return Low–Side Current Sensing
- Non–Inverting Input Path for Load Low–Side Current Sensing
- Fixed or Adjustable Current Threshold in All Current Sensing Modes
- Positive Voltage Sensing in All Current Sensing Modes
- Fixed Voltage Threshold in All Current Sensing Modes
- Adjustable Voltage Threshold in All Low–Side Current Sensing Modes
- Output Driver Directly Interfaces with Economical Optoisolators
- Operating Voltage Range of 2.3 V to 18 V

Representative Block Diagram

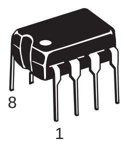


This device contains 114 active transistors.

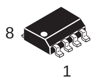
MC33341

POWER SUPPLY BATTERY CHARGER REGULATION CONTROL CIRCUIT

SEMICONDUCTOR TECHNICAL DATA

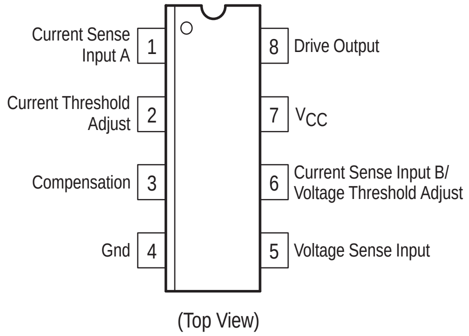


P SUFFIX
PLASTIC PACKAGE
CASE 626



D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

PIN CONNECTIONS



ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC33341D	T_A = –40° to +85°C	SO–8
MC33341P		Plastic DIP

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage (Pin 7)	V_{CC}	18	V
Voltage Range Current Sense Input A (Pin 1) Current Threshold Adjust (Pin 2) Compensation (Pin 3) Voltage Sense Input (Pin 5) Current Sense Input B/Voltage Threshold Adjust (Pin 6) Drive Output (Pin 8)	V_{IR}	–1.0 to V_{CC}	V
Drive Output Source Current (Pin 8)	I_{Source}	50	mA
Thermal Resistance, Junction–to–Air P Suffix, DIP Plastic Package, Case 626 D Suffix, SO–8 Plastic Package, Case 751	$R_{\theta JA}$	 100 178	°C/W
Operating Junction Temperature (Note 1)	T_J	–25 to +150	°C
Storage Temperature	T_{stg}	–55 to +150	°C

NOTE: ESD data available upon request.

ELECTRICAL CHARACTERISTICS (V_{CC} = 6.0 V, T_A = 25°C, for min/max values T_A is the operating junction temperature range that applies (Note 1), unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
CURRENT SENSING (Pins 1, 2, 6)					
Source High–Side and Load High–Side Sensing Pin 1 to Pin 6 (Pin 1 >1.6 V)	$V_{th(I\ HS)}$				mV
Internally Fixed Threshold Voltage (Pin 2 = V_{CC})					
T_A = 25°C		–	200	–	
T_A = T_{low} to T_{high}		–	196 to 204	–	
Externally Adjusted Threshold Voltage (Pin 2 = 0 V)		–	10	–	
Externally Adjusted Threshold Voltage (Pin 2 = 200 mV)		–	180	–	
Load Low–Side Sensing Pin 1 to Pin 4 (Pin 1 = 0 V to 0.8 V)	$V_{th(I\ LS+)}$				mV
Internally Fixed Threshold Voltage (Pin 2 = V_{CC})					
T_A = 25°C		–	200	–	
T_A = T_{low} to T_{high}		–	196 to 204	–	
Externally Adjusted Threshold Voltage (Pin 2 = 0 V)		–	10	–	
Externally Adjusted Threshold Voltage (Pin 2 = 200 mV)		–	180	–	
Source Return Low–Side Sensing Pin 1 to Pin 4 (Pin 1 = 0 V to –0.2 V)	$V_{th(I\ LS–)}$				mV
Internally Fixed Threshold Voltage (Pin 2 = V_{CC})					
T_A = 25°C		–	–200	–	
T_A = T_{low} to T_{high}		–	–196 to –204	–	
Externally Adjusted Threshold Voltage (Pin 2 = 0 V)		–	–10	–	
Externally Adjusted Threshold Voltage (Pin 2 = 200 mV)		–	–180	–	
Current Sense Input A (Pin 1)					
Input Bias Current, High–Side Source and Load Sensing (Pin 2 = 0 V to $V_{Pin\ 6}$ V)	$I_{IB(A\ HS)}$	–	40	–	µA
Input Bias Current, Low–Side Load Sensing (Pin 2 = 0 V to 0.8 V)	$I_{IB(A\ LS+)}$	–	10	–	nA
Input Resistance, Low–Side Source Return Sensing (Pin 2 = –0.6 V to 0 V)	$R_{in(A\ LS–)}$	–	10	–	kΩ
Current Sense Input B/Voltage Threshold Adjust (Pin 6)	$I_{IB(B)}$				
Input Bias Current					
High–Side Source and Load Current Sensing (Pin 6 > 2.0 V)		–	20	–	µA
Voltage Threshold Adjust (Pin 6 < 1.2 V)		–	100	–	nA
Current Sense Threshold Adjust (Pin 2) Input Bias Current	$I_{IB(I\ th)}$	–	10	–	nA
Transconductance, Current Sensing Inputs to Drive Output (I_O – 0.7 mA)	$g_{m(I)}$	–	6.0	–	mhos

NOTE: 1. Tested ambient temperature range for the MC33341: T_{low} = –25°C, T_{high} = +85°C.

ELECTRICAL CHARACTERISTICS (continued) (V_{CC} = 6.0 V, T_A = 25°C, for min/max values T_A is the operating junction temperature range that applies (Note 1), unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
DIFFERENTIAL AMPLIFIER DISABLE LOGIC (Pins 1, 6)					
Logic Threshold Voltage Pin 1 (Pin 6 = 0 V)					V
Enabled, High–Side Source and Load Current Sensing	$V_{th(I\ HS)}$	–	1.2	–	
Disabled, Low–Side Load and Source Return Current Sensing	$V_{th(I\ LS)}$	–	1.2	–	
VOLTAGE SENSING (Pins 5, 6)					
Positive Sensing Pin 5 to Pin 4					
Internally Fixed Threshold Voltage	$V_{th(V)}$				
T_A = 25°C		–	1.200	–	V
T_A = T_{low} to T_{high}		–	1.176 to 1.224	–	mV
Externally Adjusted Threshold Voltage (Pin 6 = 0 V)		–	40	–	V
Externally Adjusted Threshold Voltage (Pin 6 = 1.2 V)		–	1.175	–	
Voltage Sense, Input Bias Current (Pin 5)	$I_{IB(V)}$	–	10	–	nA
Transconductance, Voltage Sensing Inputs to Drive Output (I_O = 0.7 mA)	$g_{m(V)}$	–	7.0	–	mhos
DRIVE OUTPUT (Pin 8)					
High State Source Voltage (I_{Source} = 8.0 mA)	V_{OH}	–	V_{CC} – 0.8	–	V
TOTAL DEVICE (Pin 7)					
Operating Voltage Range	V_{CC}	–	2.3 to 18	–	V
Power Supply Current (V_{CC} = 6.0 V)	I_{CC}	–	300	–	μA

NOTE: 1. Tested ambient temperature range for the MC33341: T_{low} = –25°C, T_{high} = +85°C.

PIN FUNCTION DESCRIPTION

Pin	Name	Description
1	Current Sense Input A	This multi–mode current sensing input can be used for either source high–side, load high–side, source–return low–side, or load low–side sensing. It is common to a Differential Amplifier, Inverting Amplifier, and a Noninverting input path. Each of these sensing paths indirectly connect to the current sense input of the Transconductance Amplifier. This input is connected to the high potential side of a current sense resistor when used in source high–side, load high–side, or load low–side current sensing modes. In source return low–side current sensing mode, this pin connects to the low potential side of a current sense resistor.
2	Current Threshold Adjust	The current sense threshold can be externally adjusted over a range of 0 V to 200 mV with respect to Pin 4, or internally fixed at 200 mV by connecting Pin 2 to V_{CC}.
3	Compensation	This pin is connected to a high impedance node within the transconductance amplifier and is made available for loop compensation. It can also be used as an input to directly control the Drive Output. An active low at this pin will force the Drive Output into a high state.
4	Ground	This pin is the regulation control IC ground. The control threshold voltages are with respect to this pin.
5	Voltage Sense Input	This is the voltage sensing input of the Transconductance Amplifier. It is normally connected to the power supply/battery charger output through a resistor divider. The input threshold is controlled by Pin 6.
6	Current Sense Input B/ Voltage Threshold Adjust	This is a dual function input that is used for either high–side current sensing, or as a voltage threshold adjustment for Pin 5. This input is connected to the low potential side of a current sense resistor when used in source high–side or load high–side current sensing modes. In all low–side current sensing modes, Pin 6 is available as a voltage threshold adjustment for Pin 5. The threshold can be externally adjusted over a range of 0 V to 1.2 V with respect to Pin 4, or internally fixed at 1.2 V by connecting Pin 6 to V_{CC}.
7	V_{CC}	This is the positive supply voltage for the regulation control IC. The typical operating voltage range is 2.3 V to 18 V with respect to Pin 4.
8	Drive Output	This is a source–only output that normally connects to a linear or switching regulator control circuit. This output is capable of 15 mA, allowing it to directly drive an optoisolator in primary side control applications where galvanic isolation is required.

Figure 1. Voltage Sensing Threshold Change versus Temperature

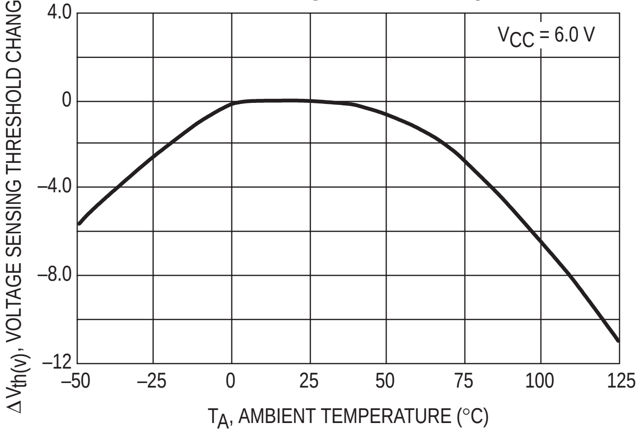


Figure 2. Current Sensing Threshold Change versus Temperature

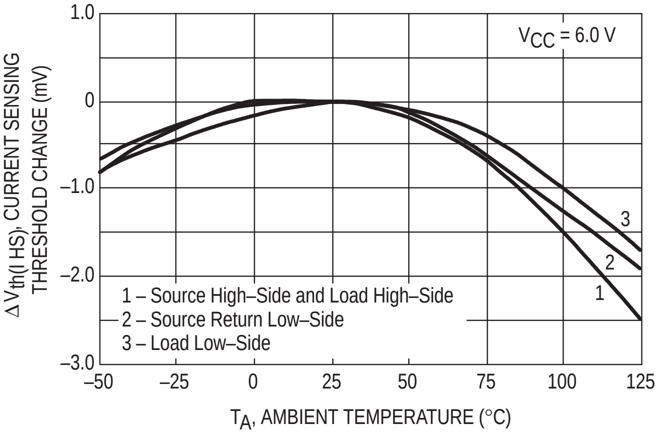


Figure 3. Closed–Loop Voltage Sensing Input versus Voltage Threshold Adjust

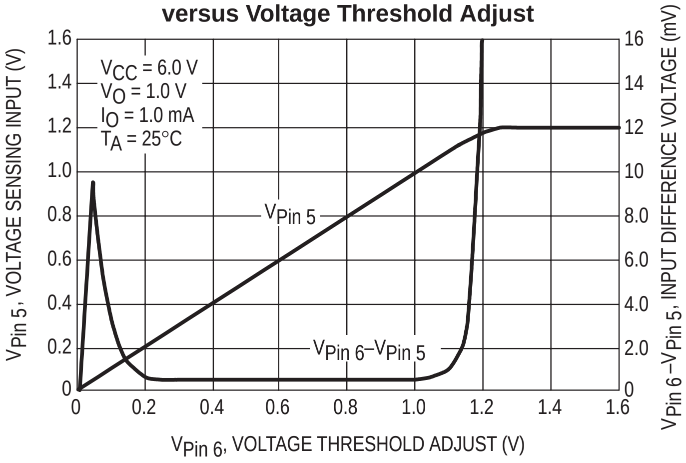


Figure 4. Closed–Loop Current Sense Input B versus Current Threshold Adjust

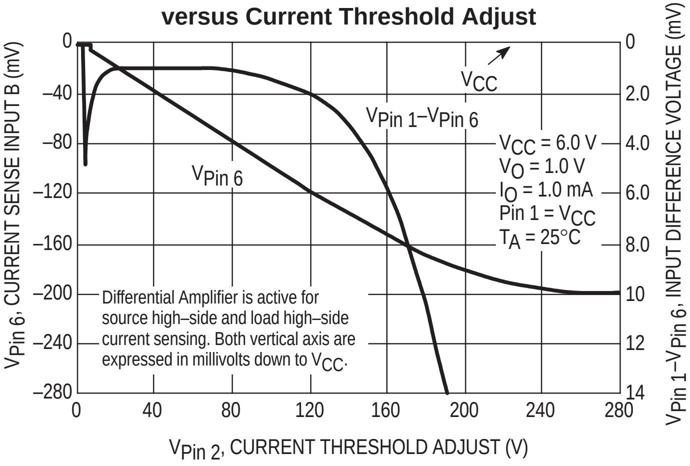


Figure 5. Closed–Loop Current Sensing Input A versus Current Threshold Adjust

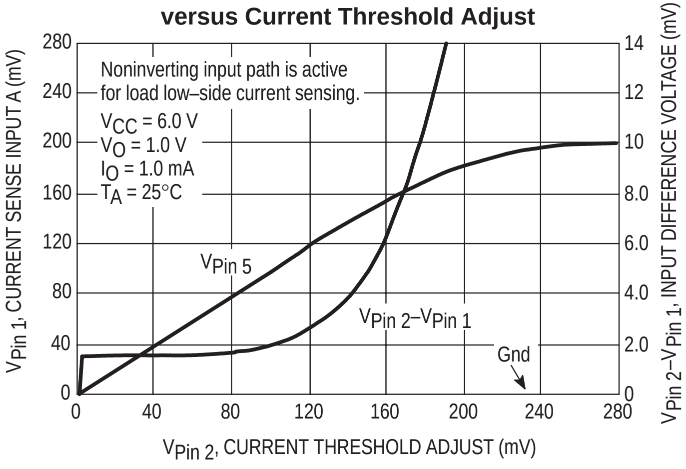


Figure 6. Closed–Loop Current Sensing Input A versus Current Threshold Adjust

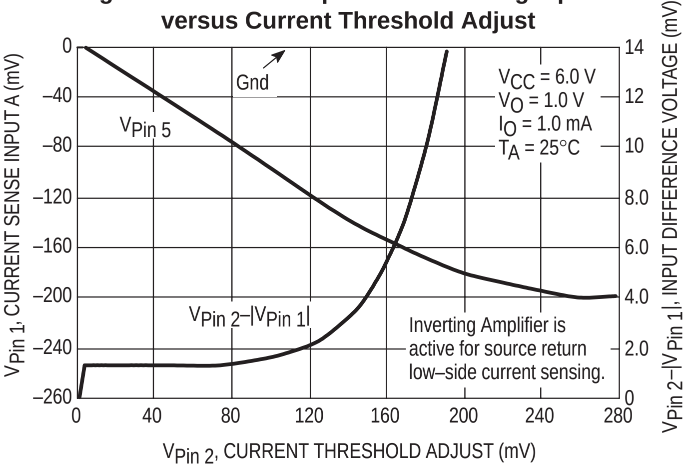


Figure 7. Bode Plot Voltage Sensing Inputs to Drive Output

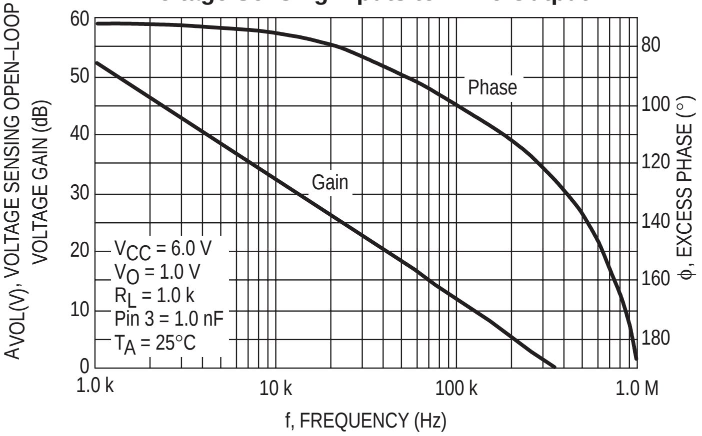


Figure 8. Bode Plot Current Sensing Inputs to Drive Output

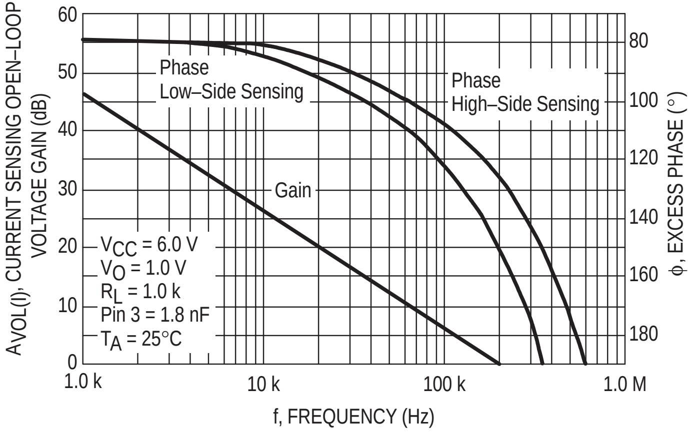


Figure 9. Transconductance Voltage Sensing Inputs to Drive Output

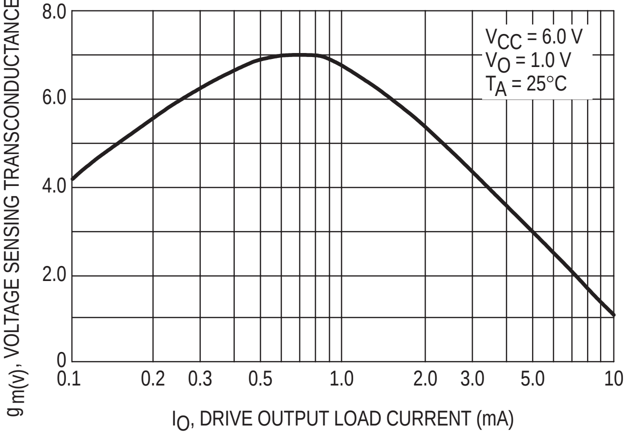


Figure 10. Transconductance Current Sensing Inputs to Drive Output

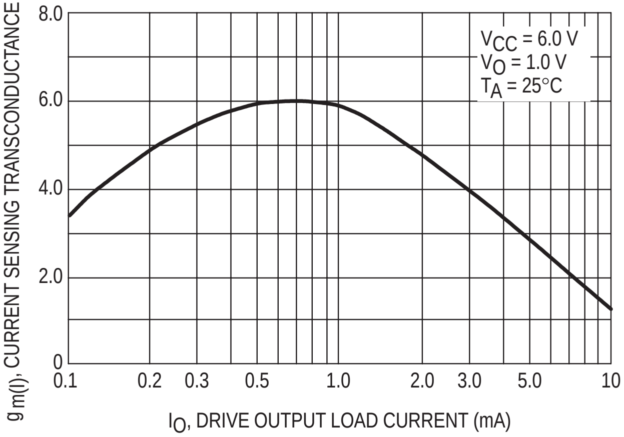


Figure 11. Drive Output High State Source Saturation versus Load Current

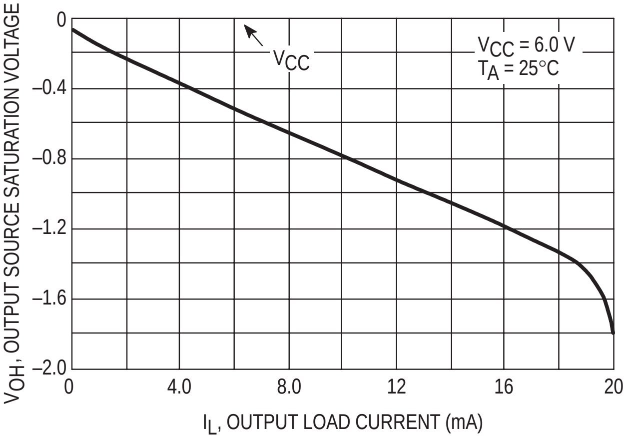
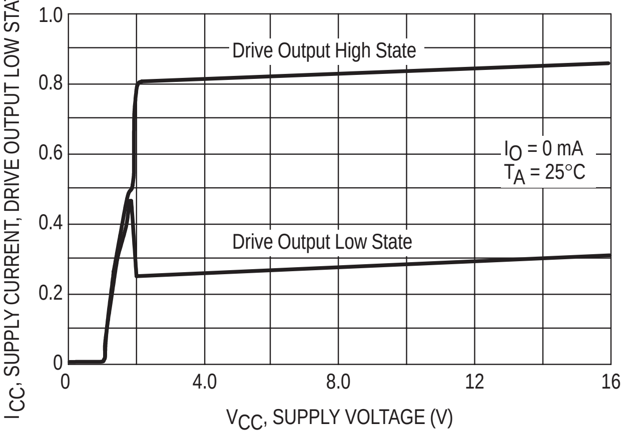


Figure 12. Supply Current versus Supply Voltage



INTRODUCTION

Power supplies and battery chargers require precise control of output voltage and current in order to prevent catastrophic damage to the system load. Many present day power sources contain a wide assortment of building blocks and glue devices to perform the required sensing for proper regulation. Typical feedback loop circuits may consist of a voltage and current amplifier, level shifting circuitry, summing circuitry and a reference. The MC33341 contains all of these basic functions in a manner that is easily adaptable to many of the various power source–load configurations.

OPERATING DESCRIPTION

The MC33341 is an analog regulation control circuit that is specifically designed to simultaneously close the voltage and current feedback loops in power supply and battery charger applications. This device can control the feedback loop in either constant–voltage or constant–current mode with automatic crossover. A concise description of the integrated circuit blocks is given below. Refer to the block diagram in Figure 13.

Transconductance Amplifier

A quad input transconductance amplifier is used to control the feedback loop. This amplifier has separate voltage and current channels, each with a sense and a threshold input. Within a given channel, if the sense input level exceeds that of the threshold input, the amplifier output is driven high. The channel with the largest difference between the sense and threshold inputs will set the output source current of the amplifier and thus dominate control of the feedback loop. The amplifier output appears at Pin 8 and is a source–only type that is capable of 15 mA.

A high impedance node within the transconductance amplifier is made available at Pin 3 for loop compensation. This pin can sink and source up to 10 µA of current. System stability is achieved by connecting a capacitor from Pin 3 to ground. The Compensation Pin signal is out of phase with respect to the Drive Output. By actively clamping Pin 3 low, the Drive Output is forced into a high state. This, in effect, will shutdown the power supply or battery charger, by forcing the output voltage and current regulation threshold down towards zero.

Voltage Sensing

The voltage that appears across the load is monitored by the noninverting V_{sen} input of the transconductance amplifier. This voltage is resistively scaled down and connected to Pin 5. The threshold at which voltage regulation occurs is set by the level present at the inverting V_{th} input of the transconductance amplifier. This level is controlled by Pin 6. In source high–side and load high–side current sensing modes, Pin 6 must be connected to the low potential side of current sense resistor R_S. Under these conditions, the voltage regulation threshold is internally fixed at 1.2 V. In source return low–side and load low–side current sensing modes, Pin 6 is available, and can be used to lower the regulation threshold of Pin 5. This threshold can be externally adjusted over a range of 0 V to 1.2 V with respect to the IC ground at Pin 4.

Current Sensing

Current sensing is accomplished by monitoring the voltage that appears across sense resistor R_S, level shifting it with respect to Pin 4 if required, and applying it to the noninverting I_{sen} input of the transconductance amplifier. In order to allow for maximum circuit flexibility, there are three methods of current sensing, each with different internal paths.

In source high–side (Figures 13 and 14) and load high–side (Figures 17 and 18) current sensing, the Differential Amplifier is active with a gain of 1.0. Pin 1 connects to the high potential side of current sense resistor R_S while Pin 6 connects to the low side. Logic circuitry is provided to disable the Differential Amplifier output whenever low–side current sensing is required. This circuit clamps the Differential Amplifier output high which disconnects it from the I_{sen} input of the Transconductance Amplifier. This happens if Pin 1 is less than 1.2 V or if Pin 1 is less than Pin 6.

With source return low–side current sensing (Figures 15 and 16), the Inverting Amplifier is active with a gain of –1.0. Pin 1 connects to the low potential side of current sense resistor R_S while Pin 4 connects to the high side. Note that a negative voltage appears across R_S with respect to Pin 4.

In load low–side current sensing (Figures 19 and 20) a Noninverting input path is active with a gain of 1.0. Pin 1 connects to the high potential side of current sense resistor R_S while Pin 4 connects to the low side. The Noninverting input path lies from Pin 1, through the Inverting Amplifier input and feedback resistors R, to the cathode of the output diode. With load low–side current sensing, Pin 1 will be more positive than Pin 4, forcing the Inverting Amplifier output low. This causes the diode to be reverse biased, thus preventing the output stage of the amplifier from loading the input signal that is flowing through the feedback resistors.

The regulation threshold in all of the current sensing modes is internally fixed at 200 mV with Pin 2 connected to V_{CC}. Pin 2 can be used to externally adjust the threshold over a range of 0 to 200 mV with respect to the IC ground at Pin 4.

Reference

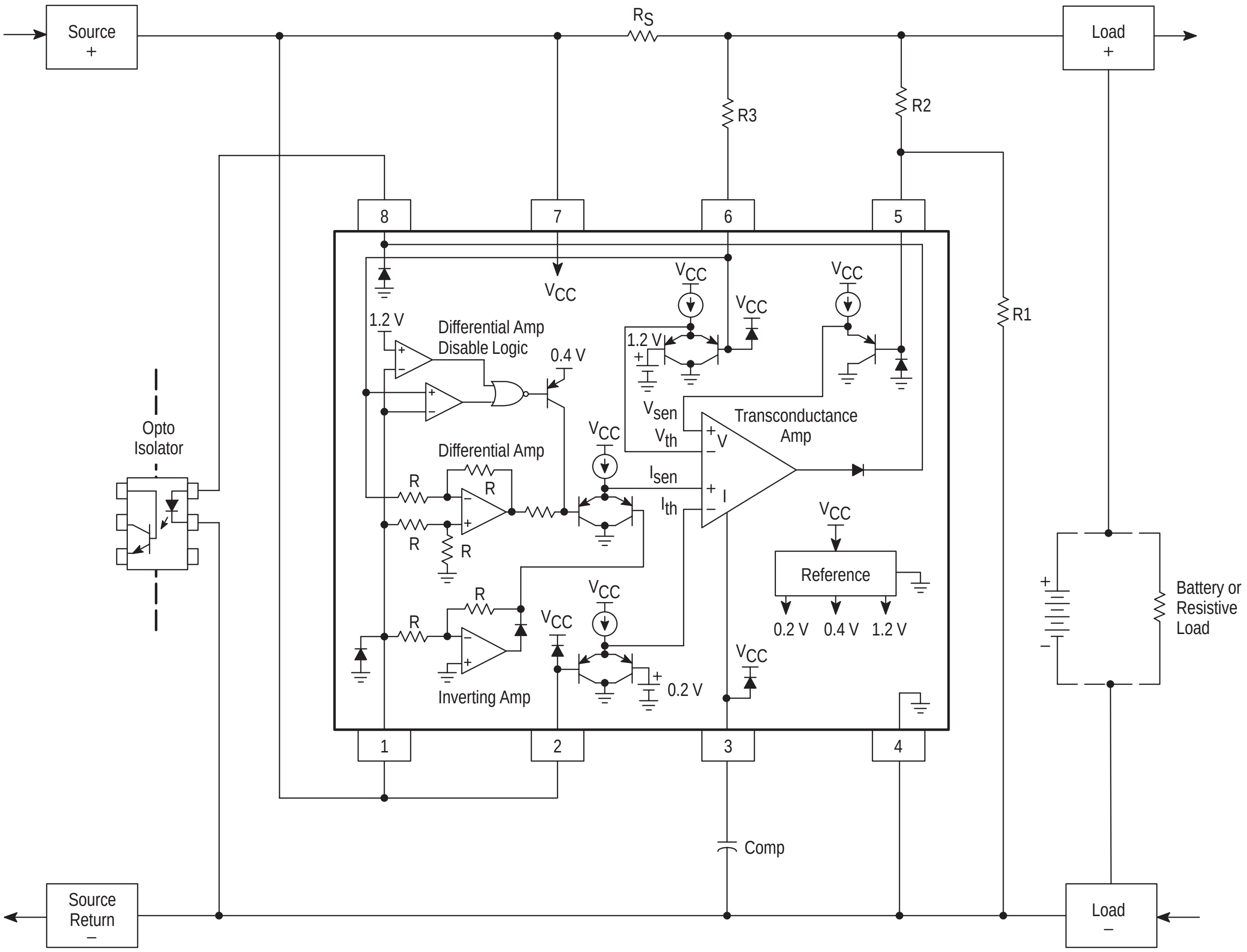
An internal band gap reference is used to set the 1.2 V voltage threshold and 200 mV current threshold. The reference is initially trimmed to a ±1.0% tolerance at T_A = 25°C and is guaranteed to be within ±2.0% over an ambient operating temperature range of –25° to 85°C.

Applications

Each of the application circuits illustrate the flexibility of this device. The circuits shown in Figures 13 through 20 contain an optoisolator connected from the Drive Output at Pin 8 to ground. This configuration is shown for ease of understanding and would normally be used to provide an isolated control signal to a primary side switching regulator controller. In non–isolated, primary or secondary side applications, a load resistor can be placed from Pin 8 to ground. This resistor will convert the Drive Output current to a voltage for direct control of a regulator.

In applications where excessively high peak currents are possible from the source or load, the load induced voltage drop across R_S could exceed 1.6 V. Depending upon the current sensing configuration used, this will result in forward biasing of either the internal V_{CC} clamp diode, Pin 6, or the device substrate, Pin 1. Under these conditions, input series resistor R3 is required. The peak input current should be limited to 20 mA. Excessively large values for R3 will degrade the current sensing accuracy. Figure 21 shows a method of bounding the voltage drop across R_S without sacrificing current sensing accuracy.

Figure 13. Source High–Side Current Sensing with Internally Fixed Voltage and Current Thresholds



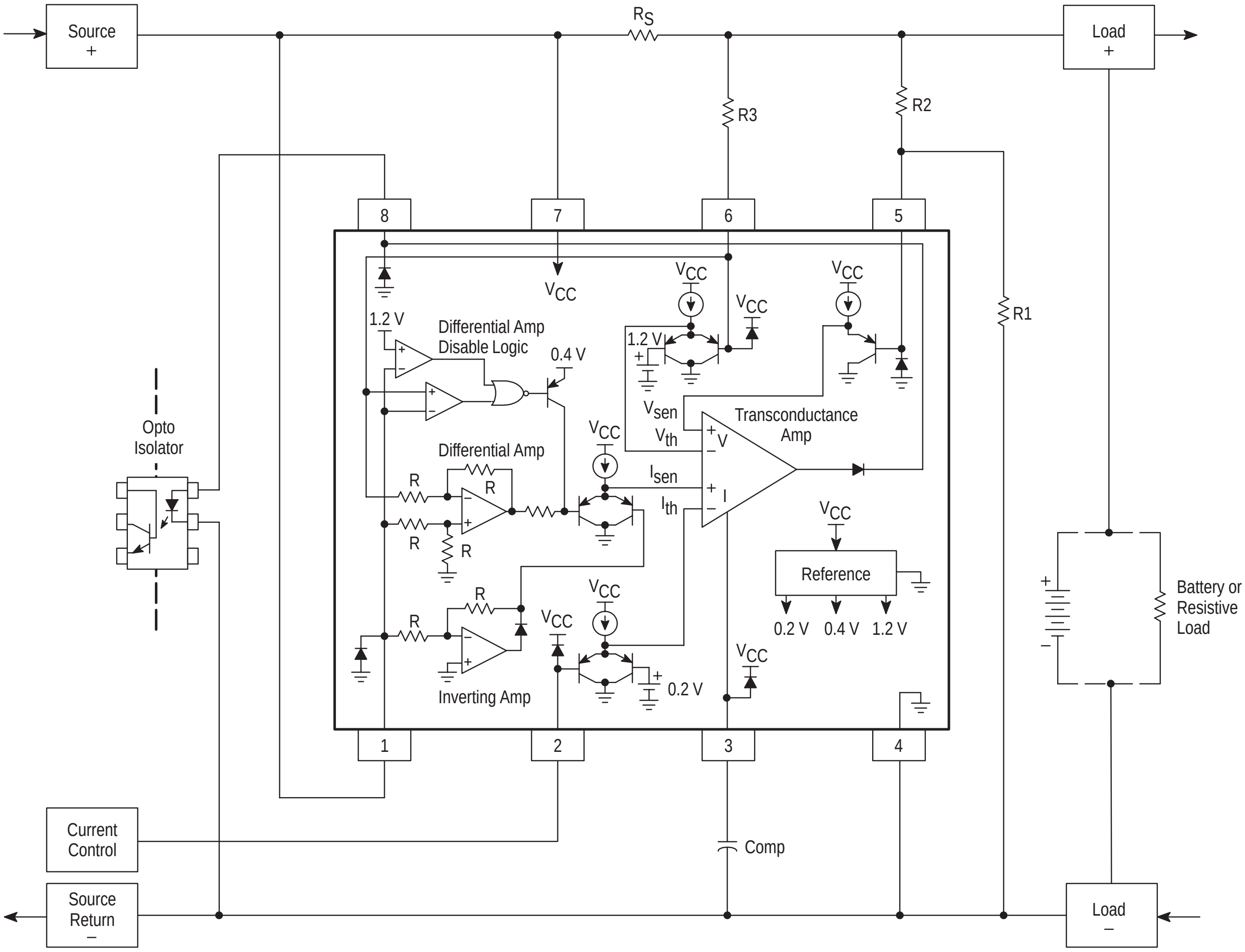
The above figure shows the MC33341 configured for source high–side current sensing allowing a common ground path between Load – and Source Return –. The Differential Amplifier inputs, Pins 1 and 6, are used to sense the load induced voltage drop that appears across resistor R_S. The internal voltage and current regulation thresholds are selected by the respective external connections of Pins 2 and 6. Resistor R3 is required in applications where a high peak level of reverse current is possible if the source inputs are shorted. The resistor value should be chosen to limit the input current of the internal V_{CC} clamp diode to less than 20 mA. Excessively large values for R3 will degrade the current sensing accuracy.

$$V_{reg} = V_{th(V)}\left(\frac{R2}{R1} + 1\right) = 1.2\left(\frac{R2}{R1} + 1\right)$$

$$I_{reg} = \frac{V_{th(I\ HS)}}{R_S} = \frac{0.2}{R_S}$$

$$R3 = \frac{\left(I_{pk}\,R_S\right) - 0.6}{0.02}$$

Figure 14. Source High–Side Current Sensing with Externally Adjustable Current and Internally Fixed Voltage Thresholds



The above figure shows the MC33341 configured for source high–side current sensing with an externally adjustable current threshold. Operation of this circuit is similar to that of Figure 13. The current regulation threshold can be adjusted over a range of 0 V to 200 mV with respect to Pin 4.

$$V_{reg} = V_{th(V)}\left(\frac{R2}{R1} + 1\right)$$

$$I_{reg} = \frac{V_{th(Pin\ 2)}}{R_S}$$

$$R3 = \frac{\left(I_{pk}\,R_S\right) - 0.6}{0.02}$$

$$= 1.2\left(\frac{R2}{R1} + 1\right)$$

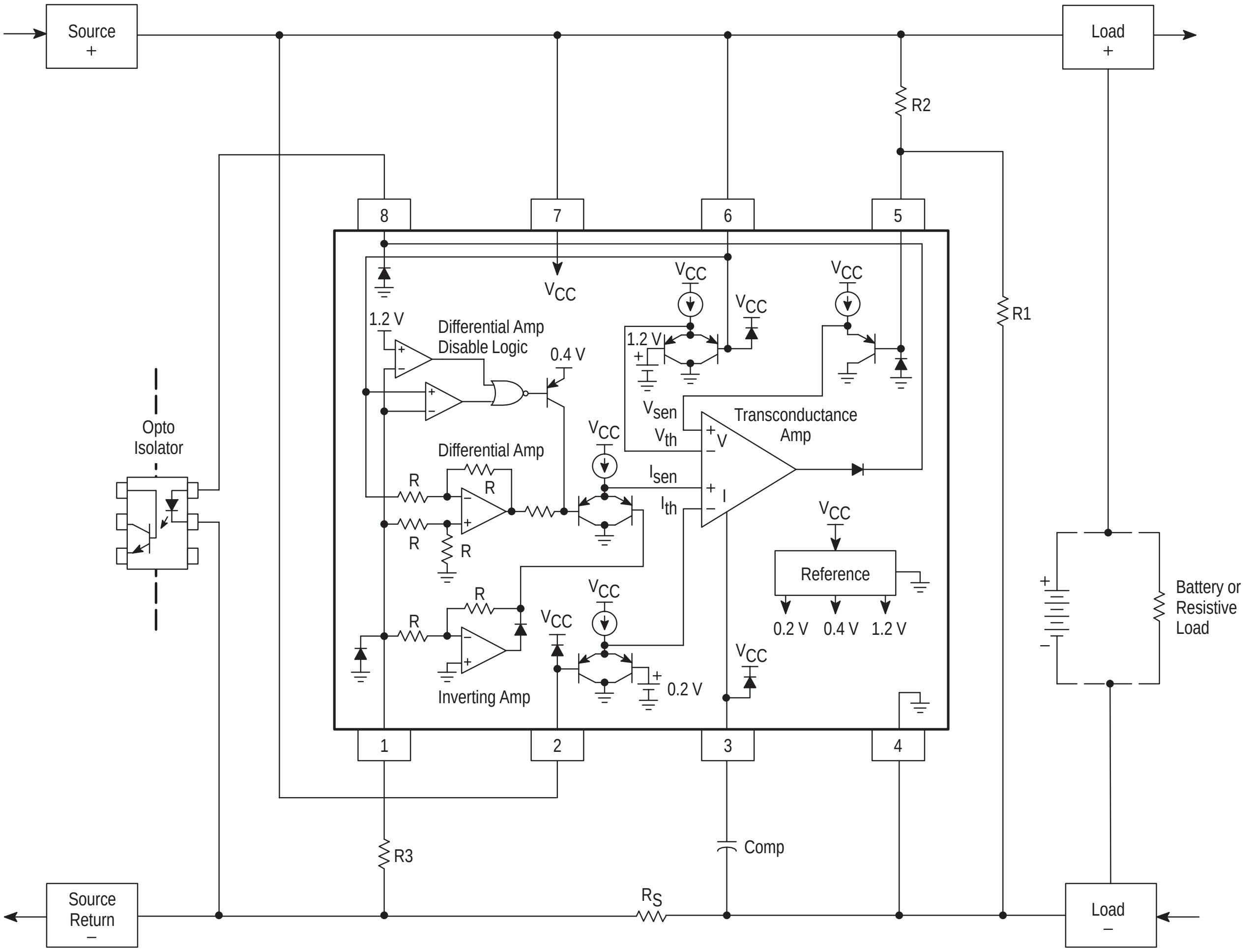


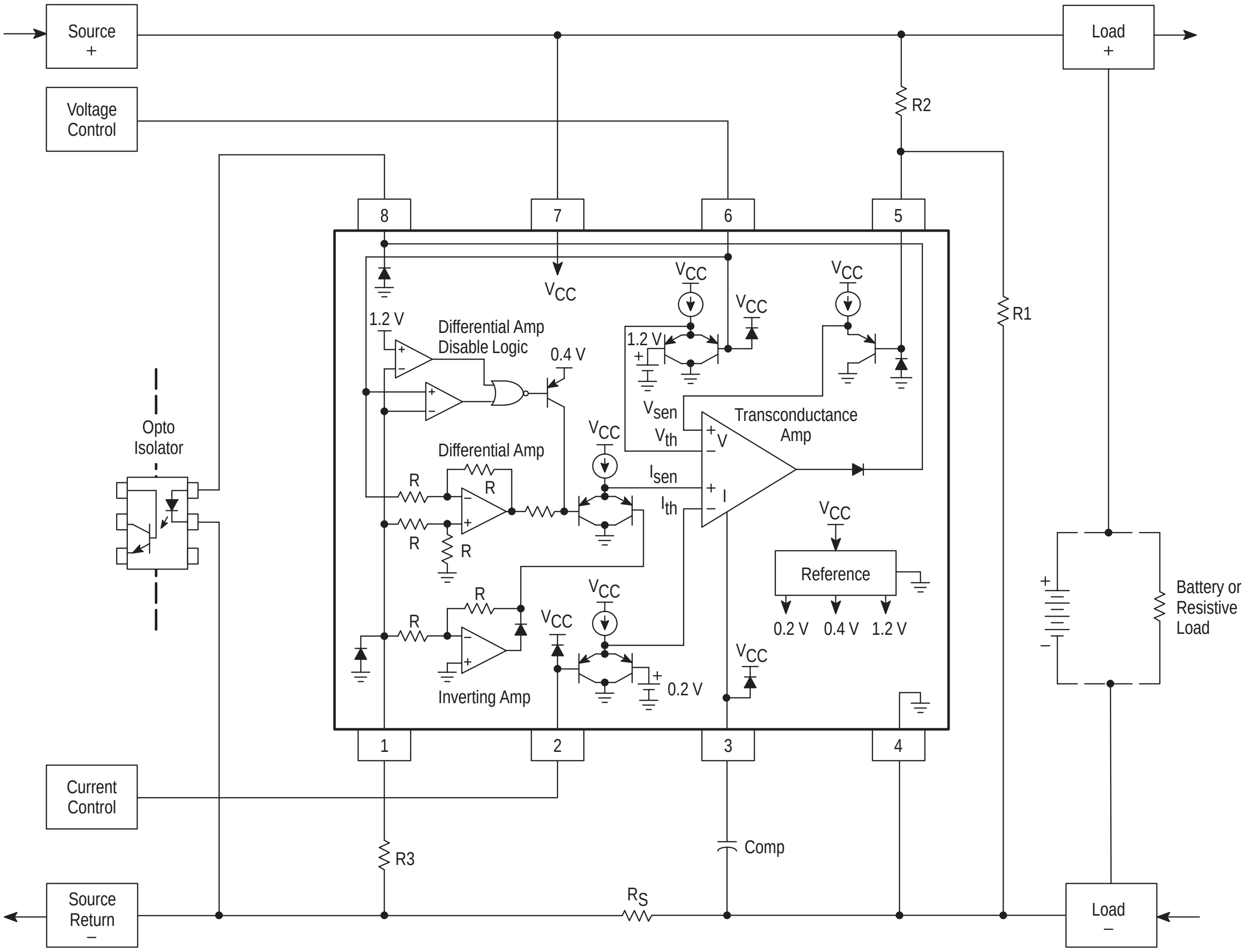
Figure 15. Source Return Low–Side Current Sensing with Internally Fixed Current and Voltage Thresholds

The above figure shows the MC33341 configured for source return low–side current sensing allowing a common power path between Source + and Load +. This configuration is especially suited for negative output applications where a common ground path, Source + to Load +, is desired. The Inverting Amplifier inputs, Pins 1 and 4, are used to sense the load induced voltage drop that appears across resistor R_S. The internal voltage and current regulation thresholds are selected by the respective external connections of Pins 2 and 6. Resistor R3 is required in applications where high peak levels of inrush current are possible. The resistor value should be chosen to limit the negative substrate current to less than 20 mA. Excessively large values for R3 will degrade the current sensing accuracy.

$$V_{reg} = V_{th(V)}\left(\frac{R2}{R1} + 1\right) \qquad I_{reg} = \frac{V_{th(I\ LS-)}}{R_S} \qquad R3 = \frac{\left(I_{pk}\ R_S\right) - 0.6}{0.02}$$

$$= 1.2\left(\frac{R2}{R1} + 1\right) \qquad = \frac{-0.2}{R_S}$$

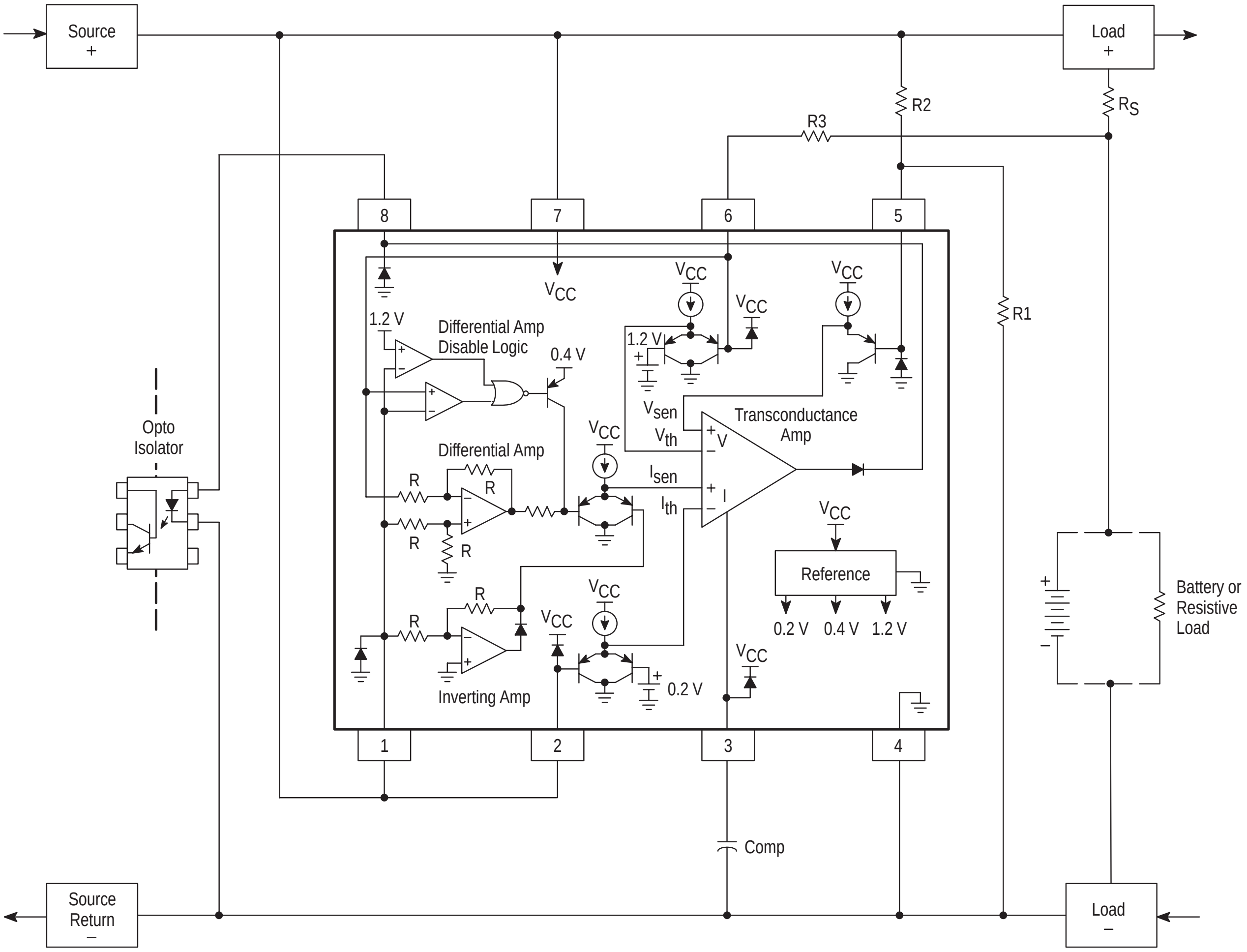
Figure 16. Source Return Low–Side Current Sensing with Externally Adjustable Current and Voltage Thresholds



The above figure shows the MC33341 configured for source return low–side current sensing with externally adjustable voltage and current thresholds. Operation of this circuit is similar to that of Figure 15. The respective voltage and current regulation threshold can be adjusted over a range of 0 to 1.6 V and 0 V to 200 mV with respect to Pin 4.

$$V_{reg} = V_{th(Pin\ 6)}\left(\frac{R2}{R1} + 1\right) \qquad I_{reg} = -\frac{V_{th(Pin\ 2)}}{R_S} \qquad R3 = \frac{\left(I_{pk}\,R_S\right) - 0.6}{0.02}$$

Figure 17. Load High–Side Current Sensing with Internally Fixed Current and Voltage Thresholds



The above figure shows the MC33341 configured for load high–side current sensing allowing common paths for both power and ground, between the source and load. The Differential Amplifier inputs, Pins 1 and 6, are used to sense the load induced voltage drop that appears across resistor R_S. The internal voltage and current regulation thresholds are selected by the respective external connections of Pins 2 and 6. Resistor R3 is required in applications where high peak levels of load current are possible from the battery or load bypass capacitor. The resistor value should be chosen to limit the input current of the internal V_{CC} clamp diode to less than 20 mA. Excessively large values for R3 ill degrade the current sensing accuracy.

$$V_{reg} = V_{th(V)}\left(\frac{R2}{R1} + 1\right)$$

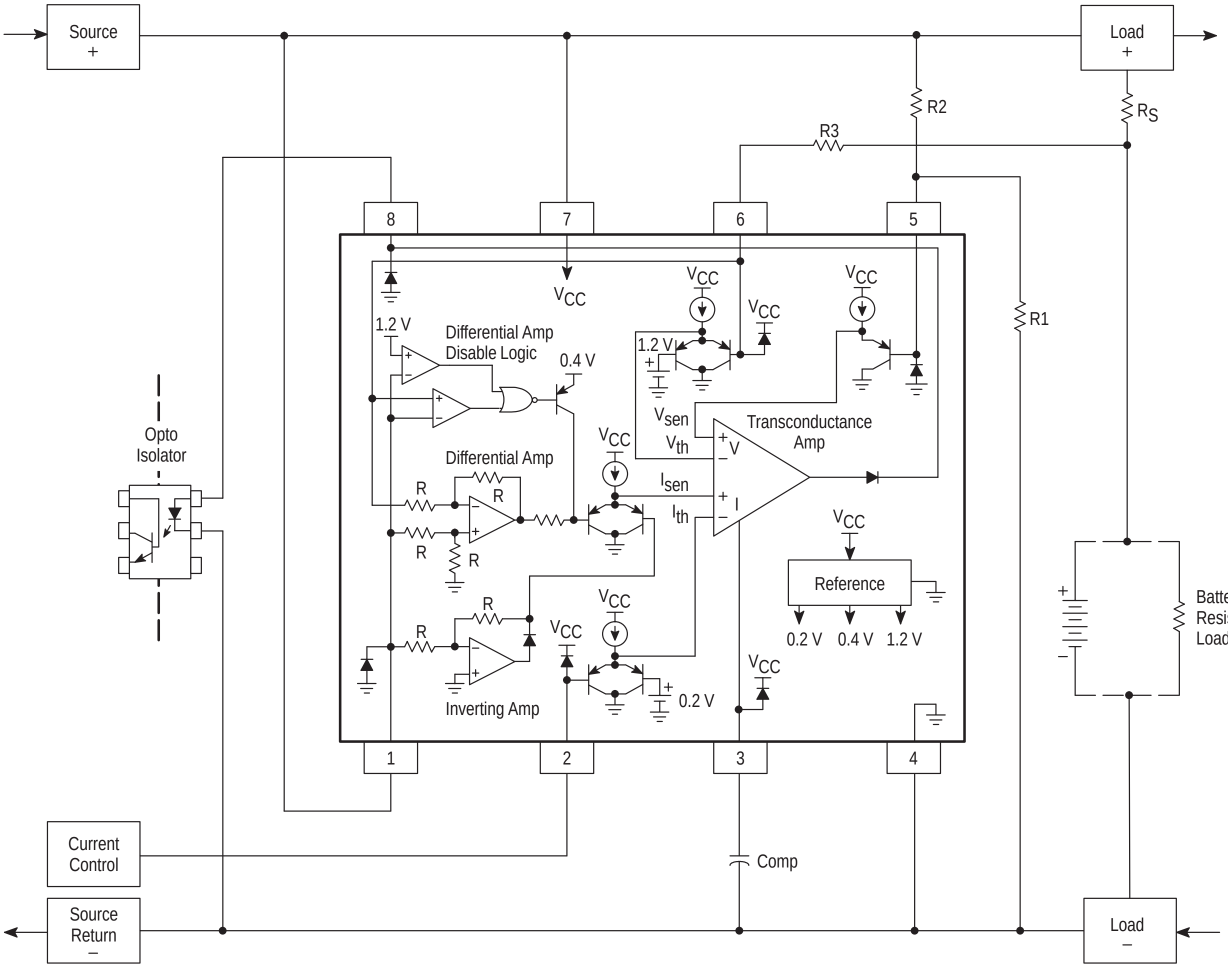
$$= 1.2\left(\frac{R2}{R1} + 1\right)$$

$$I_{reg} = \frac{V_{th(I\ HS)}}{R_S}$$

$$= \frac{0.2}{R_S}$$

$$R3 = \frac{\left(I_{pk}\ R_S\right) - 0.6}{0.02}$$

Figure 18. Load High–Side Current Sensing with Externally Adjustable Current and Internally Fixed Voltage Thresholds



The above figure shows the MC33341 configured for load high–side current sensing with an externally adjustable current threshold. Operation of this circuit is similar to that of Figure 17. The current regulation threshold can be adjusted over a range of 0 V to 200 mV with respect to Pin 4.

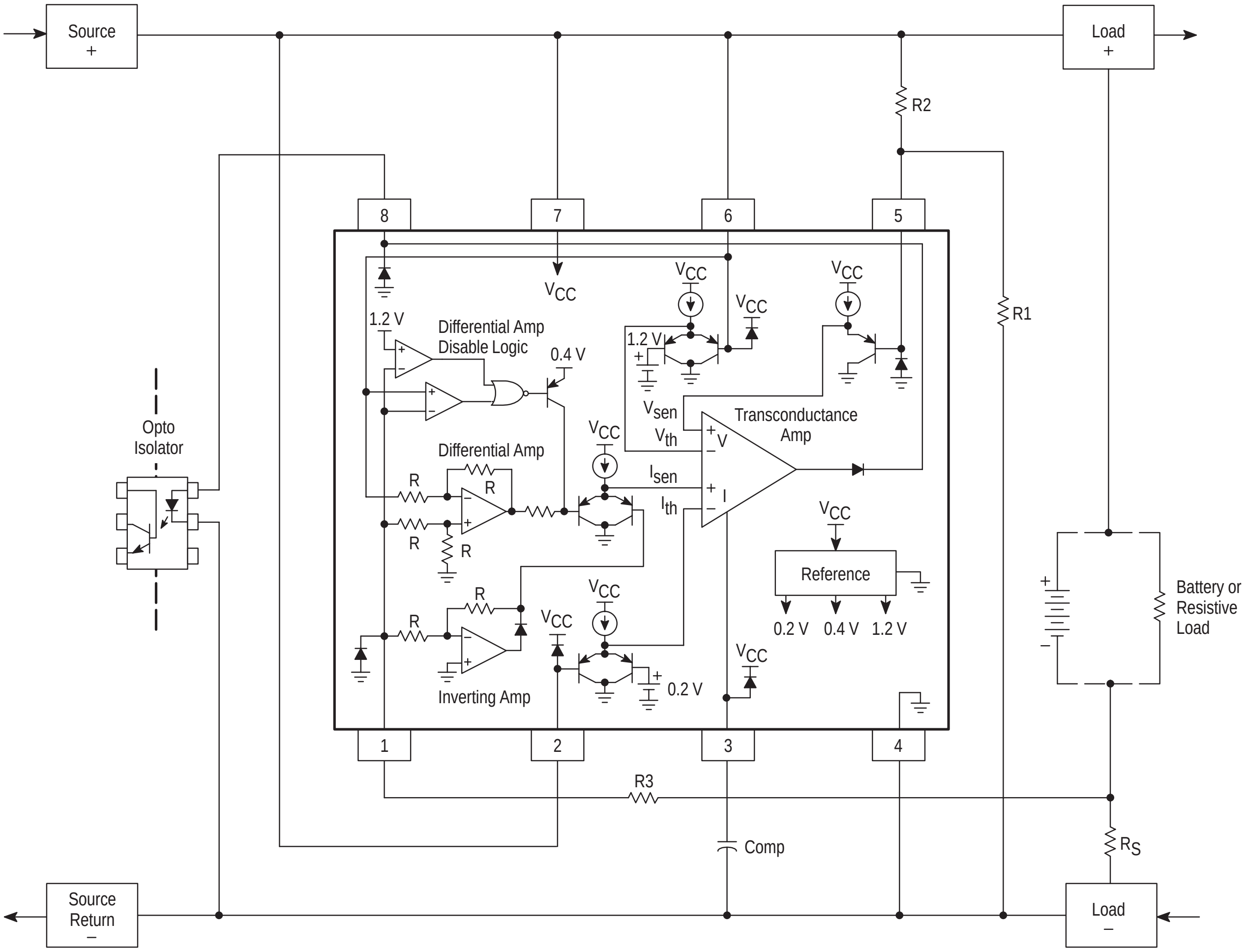
$$V_{reg} = V_{th(V)}\left(\frac{R2}{R1} + 1\right)$$

$$= 1.2\left(\frac{R2}{R1} + 1\right)$$

$$I_{reg} = \frac{V_{th(Pin\ 2)}}{R_S}$$

$$R3 = \frac{\left(I_{pk}\,R_S\right) - 0.6}{0.02}$$

Figure 19. Load Low–Side Current Sensing with Internally Fixed Current and Voltage Thresholds



The above figure shows the MC33341 configured for load low–side current sensing allowing common paths for both power and ground, between the source and load. The Noninverting input paths, Pins 1 and 4, are used to sense the load induced voltage drop that appears across resistor R_S. The internal voltage and current regulation thresholds are selected by the respective external connections of Pins 2 and 6. Resistor R3 is required in applications where high peak levels of load current are possible from the battery or load bypass capacitor. The resistor value should be chosen to limit the negative substratecurrent to less than 20 mA. Excessively large values for R3 will degrade the current sensing accuracy.

$$V_{reg} = V_{th(V)}\left(\frac{R2}{R1} + 1\right)$$

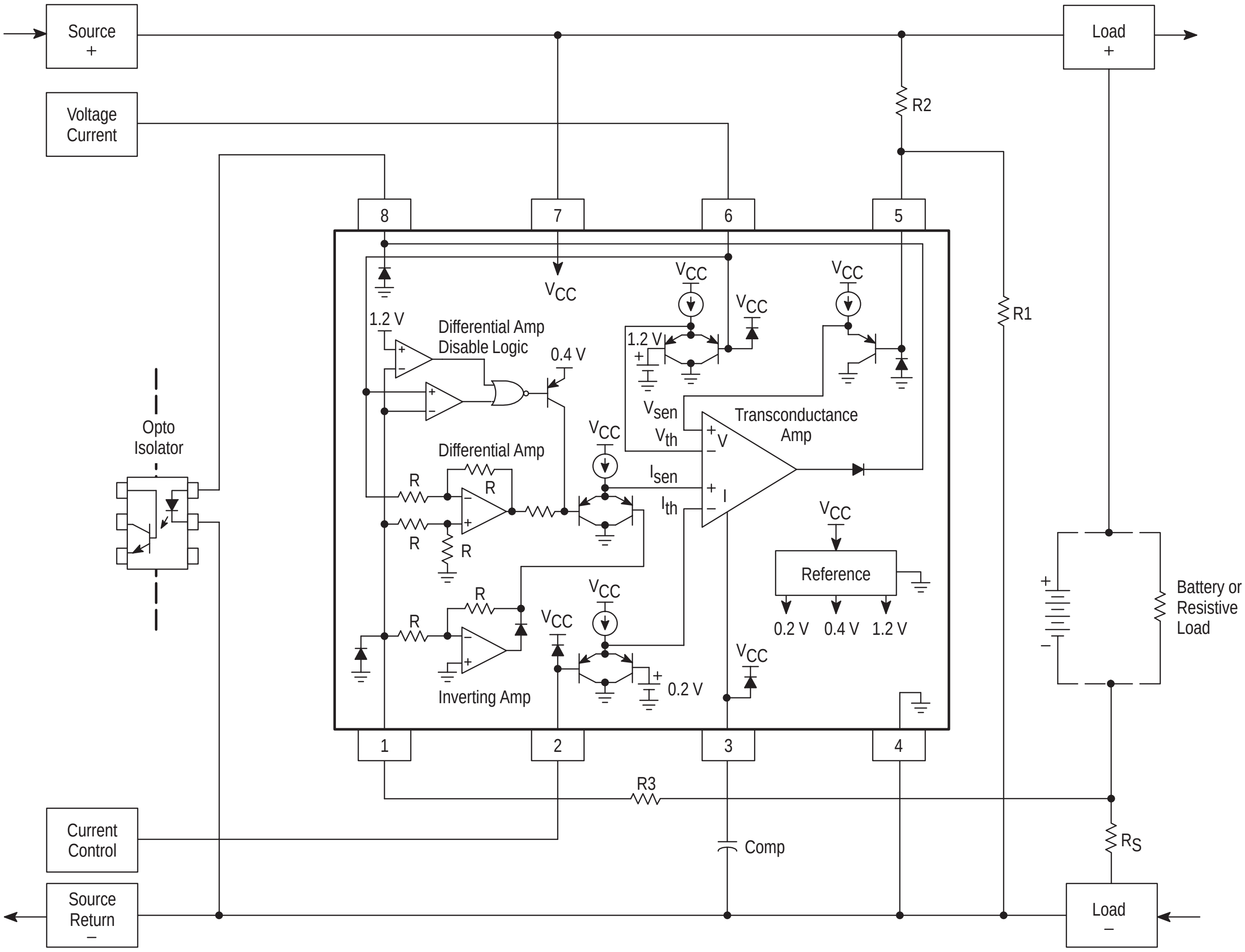
$$= 1.2\left(\frac{R2}{R1} + 1\right)$$

$$I_{reg} = \frac{V_{th(I\,LS+)}}{R_S}$$

$$= \frac{0.2}{R_S}$$

$$R3 = \frac{\left(I_{pk}\,R_S\right) - 0.6}{0.02}$$

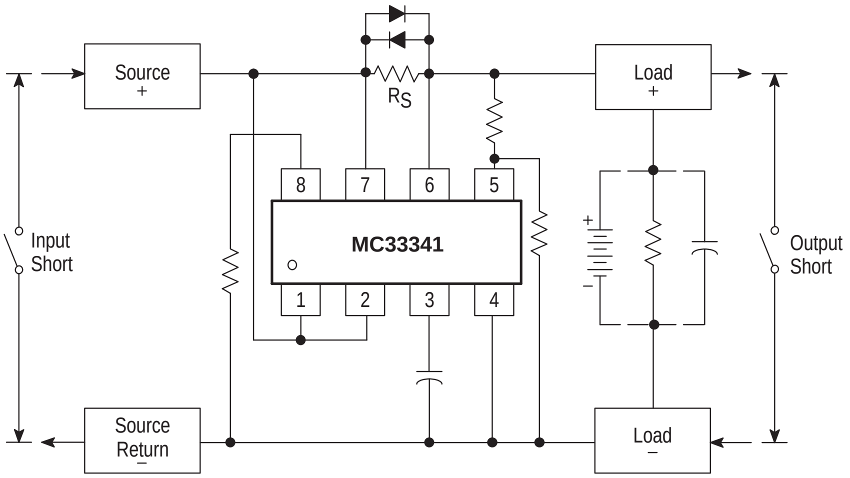
Figure 20. Load Low–Side Current Sensing with Externally Adjustable Current and Voltage Thresholds



The above figure shows the MC33341 configured for load low–side current sensing with an externally adjustable voltage and current threshold. Operation of this circuit is similar to that of Figure 19. The respective voltage and current regulation threshold can be adjusted over a range of 0 to 1.2 V and 0 V to 200 mV, with respect to Pin 4.

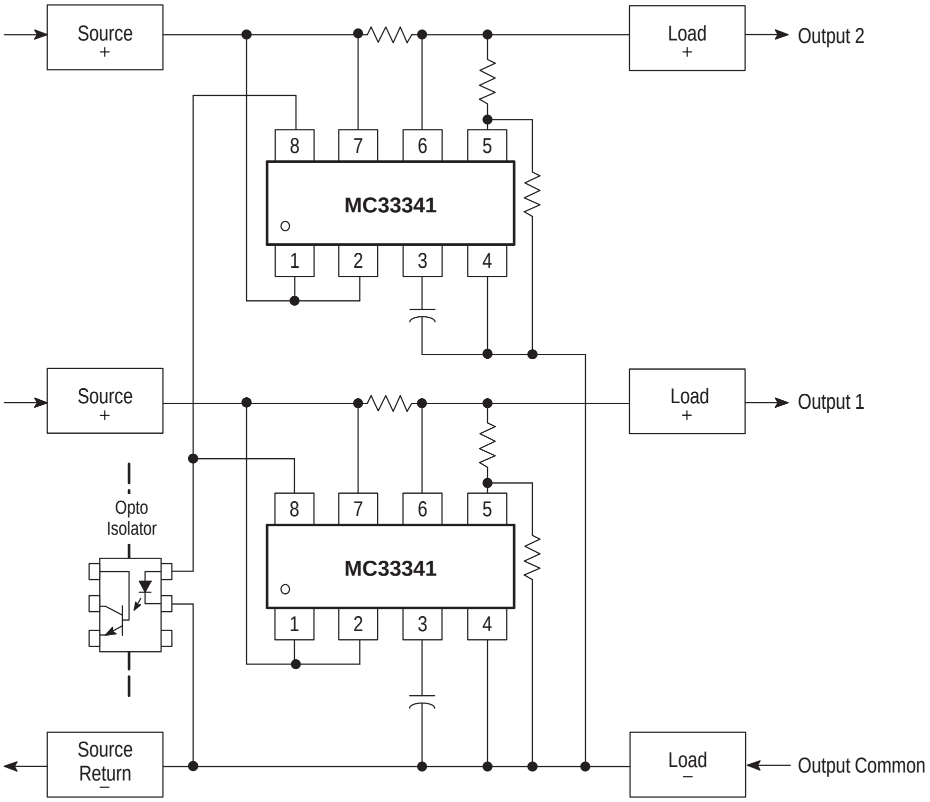
$$V_{reg} = V_{th(Pin\ 6)}\left(\frac{R2}{R1} + 1\right) \qquad I_{reg} = \frac{V_{th(Pin\ 2)}}{R_S} \qquad R3 = \frac{\left(I_{pk}\,R_S\right) - 0.6}{0.02}$$

Figure 21. Current Sense Resistor Bounding



NOTE: An excessive load induced voltage across R_S can occur if either the source input or load output is shorted. This voltage can easily be bounded with the addition of the diodes shown without degrading the current sensing accuracy. This bounding technique can be used in any of the MC33341 applications where high peak currents are anticipated.

Figure 22. Multiple Output Current and Voltage Regulation



NOTE: Multiple outputs can be controlled by summing the error signal into a common optoisolator. The converter output with the largest voltage or current error will dominate control of the feedback loop.

MOTOROLA

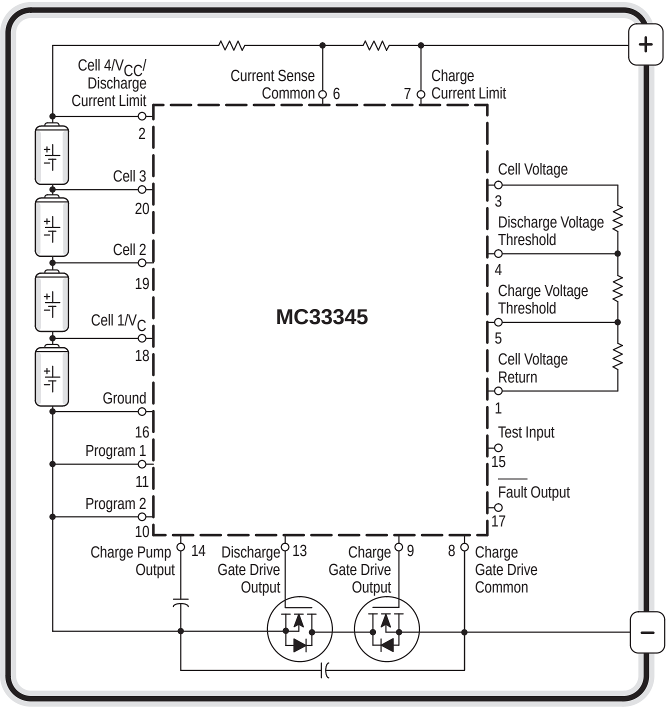
Product Preview

Lithium Battery Protection Circuit for One to Four Cell Battery Packs

The MC33345 is a monolithic lithium battery protection circuit that is designed to enhance the useful operating life of one to four cell rechargeable battery packs. Cell protection features consist of independently programmable charge and discharge limits for both voltage and current with a delayed current shutdown, cell voltage balancing with on–chip balancing resistors, and a virtually zero current sleepmode state when the cells are discharged. Additional features include an on–chip charge pump for reduced MOSFET losses while charging or discharging a low cell voltage battery pack, and the programmability for a one to four cell battery pack. This protection circuit requires a minimum number of external components and is targeted for inclusion within the battery pack. The MC33345 is available in standard and low profile 20 lead surface mount packages.

- Independently Programmable Charge and Discharge Limits for Both Voltage and Current
- Charge and Discharge Current Limit Detection with Delayed Shutdown
- Cell Voltage Balancing
- On–Chip Balancing Resistors
- Virtually Zero Current Sleepmode State when Cells are Discharged
- Charge Pump for Reduced Losses with a Low Cell Voltage Battery Pack
- Programmable for One, Two, Three or Four Cell Applications
- Minimum External Components for Inclusion within the Battery Pack
- Available in Low Profile Surface Mount Packages

Typical Four Cell Smart Battery Pack

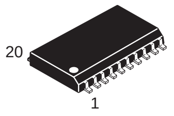


This device contains 1808 active transistors.

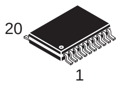
MC33345

**LITHIUM BATTERY
PROTECTION CIRCUIT
FOR
ONE TO FOUR CELL
SMART BATTERY PACKS**

**SEMICONDUCTOR
TECHNICAL DATA**

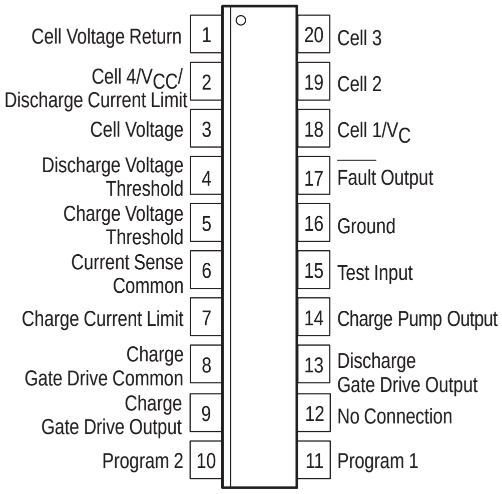


DW SUFFIX
PLASTIC PACKAGE
CASE 751D
(SO–20L)



DTB SUFFIX
PLASTIC PACKAGE
CASE 948E
(TSSOP–20)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC33345DW	T_A = –25° to +85°C	SO–20L
MC33345DTB		TSSOP–20

MAXIMUM RATINGS

Ratings	Symbol	Value	Unit
Input Voltage (Measured with Respect to Ground, Pin 16)	V_{IR}		V
Cell Voltage Divider (Pins 1, 3, 4 and 5)		18	
Cell 1/V_C (Pin 18)		7.5	
Cell 2 (Pin 19)		10	
Cell 3 (Pin 20)		18	
Cell 4/V_{CC}/Discharge Current Limit (Pin 2)		20	
Current Sense Common (Pin 6)		30	
Charge Current Limit (Pin 7)		30	
Charge Gate Drive Common (Pin 8)		±20	
Charge Gate Drive Output (Pin 9)		18 to –20	
Program 1 (Pin 11)		7.5	
Program 2 (Pin 10)		7.5	
Discharge Gate Drive Output (Pin 13)		18	
Charge Pump Output (Pin 14)		12	
Test (Pin 15)		7.5	
$\overline{\text{Fault}}$ Output (Pin 17)		20	
Cell Voltage Divider Current	I_{div}		mA
Source Current (Pin 4 to 6)		0.5	
Sink Current (Pin 5 to 16)		0.5	
$\overline{\text{Fault}}$ Output Sink Current (Pin 17)	I_{flt}	10	mA
Thermal Resistance, Junction to Air	$R_{\theta JA}$		°C/W
DTB Suffix, TSSOP–20 Plastic Package, Case 948E		135	
DW Suffix, SO–20 Plastic Package, Case 751D		105	
Operating Junction Temperature (Notes 1, 2 and 3)	T_J	–40 to +150	°C
Storage Temperature	T_{stg}	–55 to +150	°C

NOTE: ESD data available upon request.

ELECTRICAL CHARACTERISTICS (V_{CC} (Pin 2) = 8.0 V, V_C (Pin 18) = 4.0 V, T_A = 25°C, for min/max values T_A is the operating junction temperature range that applies (Notes 2 and 3), unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
VOLTAGE SENSING					
Charge or Discharge Voltage Inputs (Pin 4 or 5 to Pin 1)					
Threshold Voltage	V_{th}	–	1.23	–	V
Input Bias Current	I_{IB}	–	20	–	nA
Input Hysteresis Source Current (Pin 5)	I_H	–	2.0	–	µA
Cell Charge or Discharge Programmable Input Voltage Range (Pin 4 or 5)	$V_{IR(pgm)}$	–	V_{th} to 7.5	–	V
Cell Selector Series Resistance					Ω
Cell Positive to Top of Divider (Pin 2, 20, 19, or 18 to Pin 3)	R_{S+}	–	100	–	
Cell Negative to Bottom of Divider (Pin 20, 19, 18 or 16 to Pin 1)	R_{S-}	–	100	–	
Cell Voltage Sampling Rate	$t_{(smpl)}$	–	1.0	–	s
Test Input Threshold Voltage (Pin 15)	V_{th}	–	$V_{Cell\ 1}$/2.0	–	V
CELL VOLTAGE BALANCING					
Internal Balancing Resistance (Pins 2, 20, 19 and 18)	R_{bal}	–	140	–	Ω
CURRENT SENSING					
Charge Current Limit (Pin 7 to Pin 6)					
Threshold Voltage	$V_{th(chg)}$	–	18	–	mV
Input Bias Current	$I_{IB(chg)}$	–	200	–	nA
Delay	$I_{dly(chg)}$	–	1.0	–	s

NOTES: 1. Maximum package power dissipation limits must be observed.
2. Low duty cycle pulse techniques are used during test to maintain the junction temperature as close to ambient as possible.
3. Tested ambient temperature range for the MC33345:
T_{low} = –25°C T_{high} = +85°C

ELECTRICAL CHARACTERISTICS (continued) (V_{CC} (Pin 2) = 8.0 V, V_C (Pin 18) = 4.0 V, T_A = 25°C, for min/max values T_A is the operating junction temperature range that applies (Notes 2 and 3), unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
CURRENT SENSING					
Discharge Current Limit (Pin 2 to Pin 6)					
Threshold Voltage	$V_{th(dschg)}$	–	50	–	mV
Input Bias Current	$I_{IB(dschg)}$	–	200	–	nA
Delay	$I_{dly(dschg)}$	–	3.0	–	ms
CHARGE PUMP					
Output Voltage (Pin 14, $R_L \geq 10^{10}$ Ω)	V_O	–	10.2	–	V
TOTAL DEVICE					
Average Cell Current	I_{CC}				
Operating (V_{CC} = 8.0 V)		–	15	–	µA
Sleepmode (V_{CC} = 5.0 V)		–	5.0	–	nA
Minimum Operating Cell Voltage for Logic and Gate Drivers	V_{CC}				V
Programmed for One Cell Operation					
Cell 1 Voltage		–	2.2	–	
Programmed for Two, Three, or Four Cell Operation					
Cell 1 Voltage		–	1.5	–	
Cell 2, Cell 3, or Cell 4 Voltage, Sum Voltage of Cells		–	0.7	–	

NOTES: 1. Maximum package power dissipation limits must be observed.
2. Low duty cycle pulse techniques are used during test to maintain the junction temperature as close to ambient as possible.
3. Tested ambient temperature range for the MC33345:
T_{low} = –25°C T_{high} = +85°C

PIN FUNCTION DESCRIPTION

Pin	Symbol	Description
1	Cell Voltage Return	The bottom side of a three resistor divider string connects to this pin. The Cell Selector internally switches this point to the negative terminal of the cell that is to be monitored.
2	Cell 4/V_{CC}/ Discharge Current Limit	This is a multifunction pin that connects to a high impedance node of the Cell Selector where it is used to monitor the positive terminal of Cell 4 and to provide positive supply voltage for the protection IC. This pin is also used to monitor the voltage drop across the discharge current limit resistor and it provides a discharge path for the internal balancing of Cell 4.
3	Cell Voltage	The top side of a three resistor divider string connects to this pin. The Cell Selector internally switches this point to the positive terminal of the cell that is to be monitored.
4	Discharge Voltage Threshold	The upper tap of a three resistor divider string connects to this pin. The Cell Voltage Detector compares the divided down cell voltage to an internal reference. If the comparator detects that the cell voltage has fallen below the programmed level, discharge switch Q2 is disabled, and the protection circuit enters into a low current sleepmode state. This prevents further discharging of the battery pack.
5	Charge Voltage Threshold	The lower tap of a three resistor divider string connects to this pin. The Cell Voltage Detector compares the divided down cell voltage to an internal reference. If the comparator detects that the cell voltage has risen above the programmed level, charge switch Q1 is disabled, preventing further charging of the battery pack. A 2.0 µA current source pull–up is internally applied to this pin creating input hysteresis.
6	Current Sense Common	This pin is a common point that is used to monitor the voltage drop across the charge and discharge current limit resistors.
7	Charge Current Limit	This pin is used to monitor the voltage drop across the charge current limit resistor.
8	Charge Gate Drive Common	This pin provides a gate turn–off path for charge switch Q1. The charge switch source and the battery pack negative terminal connect to this point.
9	Charge Gate Drive Output	This output connects to the gate of charge switch Q1 allowing it to enable or disable battery pack charging.
10	Program 2	This pin is used in conjunction with Pin 11 to program the number of cells.
11	Program 1	This pin is used in conjunction with Pin 10 to program the number of cells.
12	No Connection	This pin is not internally connected.
13	Discharge Gate Drive Output	This output connects to the gate of discharge switch Q2 allowing it to enable or disable battery pack discharging.
14	Charge Pump Output	This is the charge pump output. A reservoir capacitor is connected from this pin to ground.
15	Test Input	This input is used to facilitate circuit testing and is normally not connected. It has an internal 2.0 k pull–up resistor.
16	Ground	This is the protection IC ground and all voltage ratings are with respect to this pin.
17	Fault Output	This is on open drain output that is active low when a charging fault limit has been exceeded. The limits sensed are both charge voltage and current.
18	Cell 1/V_C	This is a multifunction pin that connects to a high impedance node of the Cell Selector where it is used to monitor the positive terminal of Cell 1 and the negative terminal of Cell 2. This pin also provides logic biasing and a discharge path for the internal balancing of Cell 1.
19	Cell 2	This pin connects to a high impedance node of the Cell Selector where it is used to monitor the positive terminal of Cell 2 and the negative terminal of Cell 3. This pin also provides a discharge path for the internal balancing of Cell 2.
20	Cell 3	This pin connects to a high impedance node of the Cell Selector where it is used to monitor the positive terminal of Cell 3 and the negative terminal of Cell 4. This pin also provides a discharge path for the internal balancing of Cell 3.

INTRODUCTION

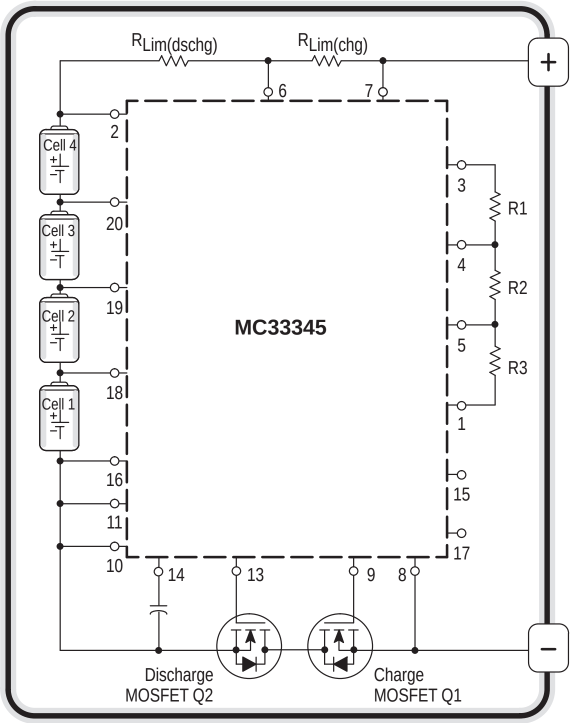
The insatiable demand for smaller lightweight portable electronic equipment has dramatically increased the requirements of battery performance. Batteries are expected to have higher energy densities, superior cycle life, be safe in operation and environmentally friendly. To address these high expectations, battery manufacturers have invested heavily in developing rechargeable lithium–based cells. Today's most attractive chemistries include lithium–polymer, lithium–ion, and lithium–metal. Each of these chemistries require electronic protection in order to constrain cell operation to within the manufacturers limits.

Rechargeable lithium–based cells require precise charge and discharge termination limits for both voltage and current in order to maximize cell capacity, cycle life, and to protect the end user from a catastrophic event. The termination limits are not as well defined as with older non–lithium chemistries. These limits are dependent upon a manufacturer's particular lithium chemistry, construction technique, and intended application. Battery pack assemblers may also choose to enhance cell capacity at the expense of cycle life. In order to address these requirements the MC33345 was developed. This device features programmable voltage and current limits, cell voltage balancing, low operating current, a virtually zero current sleepmode state, and requires few external components to implement a complete one to four cell smart battery pack.

OPERATING DESCRIPTION

The MC33345 is specifically designed to be placed in the battery pack where it is continuously powered from either one, two, three, or four lithium cells. In order to maintain cell operation within specified limits, the protection circuit senses both cell voltage and current, and correspondingly controls the state of two N–channel MOSFET switches. These switches, Q1 and Q2, are placed in series with the negative terminal of Cell 1 and the negative terminal of the battery pack.

Figure 1. Simplified Four Cell Smart Battery Pack



This configuration allows the protection circuit to interrupt the appropriate charge or discharge path FET in the event that a programmed voltage or current limit for any cell has been exceeded.

A functional description of the protection circuit blocks follows. Refer to the detailed block diagram shown in Figure 6.

Voltage Sensing

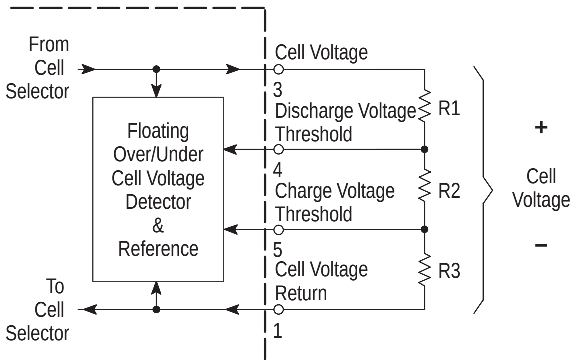
Individual cell voltage sensing is accomplished by the use of the Cell Selector in conjunction with the Floating Over/Under Voltage Detector and Reference block. The Cell Selector applies the voltage of each cell across an external resistor divider string that connects from Pins 3 to 1. The voltage at each of the tap points is sequentially polled and compared to an internal reference. If a limit has been exceeded, the result is stored in the Over/Under Data Latch and Control Logic block. The Cell Selector is gated on for an 8.0 ms period at a one second repetition rate. This low duty cycle sampling technique reduces the average load current that the divider presents across each cell, thus extending the useful battery pack capacity. The cells are sensed in the following sequence:

Figure 2. Cell Sensing Sequence

Polling Sequence	Time (ms)	Cell Sensed	Tested Limit
1	1.0	Cell 4	Overvoltage
2	1.0	Cell 3	Overvoltage
3	1.0	Cell 2	Overvoltage
4	1.0	Cell 1	Overvoltage
5	1.0	Cell 4	Undervoltage
6	1.0	Cell 3	Undervoltage
7	1.0	Cell 2	Undervoltage
8	1.0	Cell 1	Undervoltage

By incorporating this polling technique with a single floating comparator and voltage divider, a significant reduction of circuitry and trim elements is achieved. This results in a smaller die size, lower cost, and reduced operating current.

Figure 3. Cell Voltage Limit Programming



The cell charge and discharge voltage limits are controlled by the values selected for the resistor divider string and the 1.23 V input threshold of Pins 4 and 5. As the battery pack reaches full charge, the Cell Voltage Detector will sense an overvoltage fault condition on the first cell that exceeds the programmed overvoltage limit. The fault information is stored in a data latch and charge MOSFET Q1 is turned off, disconnecting the battery pack from the charging source. An internal 2.0 μA current source pull–up is then applied to Pin 5 creating an input hysteresis voltage. As a result of an overvoltage fault, the battery pack is available for discharging only.

The overvoltage fault is reset by applying a load to the battery pack. As the voltage across each cell falls below the input hysteresis level, charge MOSFET Q1 will turn on. The battery pack will now be available for charging or discharging. The over voltage limit and hysteresis voltage are given by:

$$V_{OV} = V_{th\,(Pin\,5)}\left(\frac{R1 + R2 + R3}{R3}\right)$$

$$V_{H} = I_{H\,(Pin\,5)}(R1 + R2)$$

As the load eventually depletes the battery pack charge, the Cell Voltage Detector will sense an undervoltage fault condition on the first cell that falls below the programmed undervoltage limit. After an undervoltage cell is detected, discharge MOSFET Q2 is turned off, disconnecting the battery pack from the load. The protection circuit will now enter a low current sleepmode state drawing just 5.0 nA typically, thus preventing any further cell discharging. As a result of the undervoltage fault, the battery pack is available for charging only. The undervoltage limit is given by:

$$V_{UV} = V_{th\,(Pin\,4)}\left(\frac{R1 + R2 + R3}{R2 + R3}\right)$$

The undervoltage fault is reset by applying charge current to the battery pack. When the voltage on Pin 16 exceeds Pin 8 by 0.6 V, discharge MOSFET Q2 will turned on. The battery pack will now be available for charging or discharging.

Since the thresholds of Pins 4 and 5 are equal, the above equations can be rewritten to directly solve for specific resistor values as shown in the example below.

Let the desired limits be:

V_{OV} = 4.2 V, V_H = 0.4 V, and V_{UV} = 2.5 V

With nominal values for:

V_{th} = 1.23 V, and I_H = 2.0 μA

$$R3 = \frac{\left(\frac{V_H}{I_H}\right)}{\left(\frac{V_{OV}}{V_{th}} - 1\right)} = \frac{\left(\frac{0.4}{2.0 \times 10^{-6}}\right)}{\left(\frac{4.2}{1.23} - 1\right)} = 82{,}828\ \Omega$$

$$R2 = R3\left(\frac{V_{OV}}{V_{UV}} - 1\right) = 82{,}828\ \left(\frac{4.2}{2.5} - 1\right) = 56{,}323\ \Omega$$

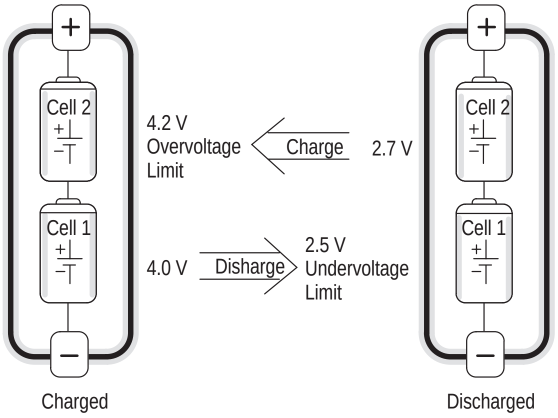
$$R1 = \left(\frac{V_H}{I_H}\right) - R2 = \left(\frac{0.4}{2.0 \times 10^{-6}}\right) - 56{,}323 = 143{,}677\ \Omega$$

Note that the Cell Selector has a typical total series resistance of 200 Ω. This will have a minimal effect on the programmed limits if the total divider resistance is in excess of 100 kΩ.

Cell Voltage Balancing

With series connected cells, successive charge and discharge cycles can result in a significant difference in cell voltage with a corresponding degradation of battery pack capacity. Figure 4 illustrates the operation of an unbalanced two cell pack. As the cells become unbalanced, the full battery pack capacity is not realized. This is due to the requirement that charging must terminate when Cell 2 reaches the overvoltage limit, and discharging must terminate when Cell 1 reaches the undervoltage limit. By employing a method of keeping the cell voltages equal, both cells can be charged and discharged to their specified limits, thus attaining the maximum possible capacity .

Figure 4. Unbalanced Battery Pack Operation



The MC33345 contains a Cell Voltage Balancing Logic circuit that controls four N–channel MOSFETs. The circuit samples the voltage of each cell during the polling period. If all of the cells are below the programmed overvoltage fault limit, no cell balancing takes place. If one or more cells reach the overvoltage fault limit, a specific latch is set for each cell. At the end of the polling period, charge MOSFET Q1 is turned off and the latches are interrogated. If all of the latches were set, no cell balancing takes place. If one, two, or three latches were set, the required cell balancing MOSFETs are then activated. The overvoltage cells are discharged to the programmed level of $V_{OV} – V_H$. As each cell attains this level, the discharge MOSFETs successively turn off. Upon completion of cell balancing, charge MOSFET Q1 is turned on. Cell voltage balancing is active during charge and discharge, but disabled during the low current sleepmode state.

Cell Programming and Test

The protection circuit can be programmed for operation with either one, two, three, or four cell battery packs. Programming inputs 1 and 2 are used to set up the internal logic for the number of cells to be monitored. If less than four cells are required, the input for each empty cell position must be connected to V_{CC}. This process starts with Cell 4 decending down to Cell 2 if required. Refer to the Cell Programming table shown below and the specific application figure.

Figure 5. Cell Sensing Sequence

Number of Cells	Program 1 (Pin 11)	Program 2 (Pin 10)	Application Figure
1	Ground	Cell 1/V_C	16
2	Cell 1/V_C	Ground	15
3	Cell 1/V_C	Cell 1/V_C	14
4	Ground	Ground	13

A test option is provided to speed up device and battery pack testing. By connecting Pin 15 to ground, the internal logic is held in a reset state and both MOSFET switches are turned on. Upon release, the Control Logic becomes active and the cells are polled within 8.0 ms.

Current Sensing

Charge and discharge current limit protection can be selectively added to the battery pack with the addition of a sense resistor. The resistors are placed in series with the positive terminal of the battery pack and the cells. Refer to Figure 1.

As the battery pack charges, Pins 6 and 7 sense the voltage drop across $R_{Lim(chg)}$. A charge current limit fault is detected if the voltage at Pin 7 exceeds Pin 6 by 18 mV for the entire delay period of 1.0 second. The fault information is stored in a data latch and charge MOSFET Q1 is turned off, disconnecting the battery pack from the charging source. As a result of the charge current fault, the battery pack is available for discharging only. The charge current limit is given by:

$$I_{Lim(chg)} = \frac{V_{th(chg)}}{R_{Lim(chg)}} = \frac{18\ \text{mV}}{R_{Lim(chg)}}$$

The charge current fault is reset by either disconnecting the battery pack from the charger, or by connecting a load to the battery pack. When the voltage on Pin 16 no longer exceeds Pin 8 by approximately 2.0 V, the Sense Enable circuit will turn on charge MOSFET Q1. Charge current sensing can be disabled by connecting Pin 7 to Pin 6.

The discharge current limiting operates in a similar manner. As the battery pack discharges, Pins 2 and 6 sense the voltage drop across $R_{Lim(dschg)}$. A discharge current limit fault is detected if the voltage at Pin 2 is less than Pin 6 by 50 mV for more than 3.0 ms. The fault information is stored in a data latch and discharge MOSFET Q2 is turned off, disconnecting the battery pack from the load. As a result of the discharge current fault, the battery pack is available for charging only. The discharge current limit is given by:

$$I_{Lim(dschg)} = \frac{V_{th(dschg)}}{R_{Lim(dschg)}} = \frac{50\ \text{mV}}{R_{Lim(dschg)}}$$

The discharge current fault is reset by either disconnecting the load from the battery pack, or by connecting the battery pack to the charger. When the voltage on Pin 8 no longer exceeds Pin 16 by approximately 2.0 V, the Sense Enable circuit will turn on discharge MOSFET Q2. Discharge current sensing can be disabled by connecting Pin 2 to Pin 6.

The charge and discharge current protection circuits contain a built in response delay of 1.0 s and 3.0 ms respectively. This helps to prevent fault activation when the battery pack is subjected to pulsed currents during charging or discharging.

Charge Pump and MOSFET Switches

The MC33345 contains an on chip Charge Pump to ensure that the MOSFET switches are fully enhanced for reduced power losses. An external reservoir capacitor normally connects from the Charge Pump output to ground, Pins 14 and 16. The capacitor value is not critical and is usually within the range of 10 nF to 100 nF. The Charge Pump output is regulated at 10.2 V allowing the use of economical logic level MOSFETs in one and two cell applications. The main requirement in selecting a particular type of MOSFET switch is to consider the desired on–resistance at the lowest anticipated operating voltage of the battery pack. A table of small outline surface mount devices is given in Figure 6. When using extremely low threshold MOSFETs, it may be desirable to disable the Charge Pump so that the maximum gate to source voltage is not exceeded. This is accomplished by connecting Pin 14 to Pin 19 with two, three, or four cell battery packs.

Battery Pack Application

Upon assembly of the battery pack, it is imperative that Cell 1 be connected first so that V_C is properly biased. The remaining cells can then be connected in any order. This assembly method prevents forward biasing the protection IC substrate which can result in overheating and non–functionality.

Each of the application figures show a capacitor labeled C_{ESD}. This capacitor provides a path around the MOSFET switches in the event of an electrostatic discharge.

Figure 6. Small Outline Surface Mount MOSFET Switches

Device Type	On–Resistance (Ω) versus Gate to Source Voltage (V)						
	2.5 V	3.0 V	4.0 V	5.0 V	6.0 V	7.5 V	9.0 V
MMFT3055VL	–	–	–	0.120 Ω	0.115 Ω	0.108 Ω	0.100 Ω
MMDF3N03HD	–	0.525 Ω	0.080 Ω	0.065 Ω	0.063 Ω	0.062 Ω	0.060 Ω
MMDF4N01HD	0.047 Ω	0.042 Ω	0.037 Ω	0.035 Ω	0.034 Ω	0.033 Ω	See Note
MMSF5N02HD	–	0.065 Ω	0.023 Ω	0.021 Ω	0.020 Ω	0.018 Ω	0.018 Ω
MMDF6N02HD	0.043 Ω	0.035 Ω	0.029 Ω	0.028 Ω	0.026 Ω	0.025 Ω	0.023 Ω

NOTE: Exceeds maximum V_{GS} voltage rating.

PROTECTION CIRCUIT OPERATING MODE TABLE

Input Conditions Cell Status	Circuit Operation Battery Pack Status	Outputs			
		MOSFET Switches		Function	
		Charge Q1	Discharge Q2	Charge Pump	Cell Balancing (See Note)
CELL CHARGING/DISCHARGING					
Storage or Nominal Operation: No current or voltage faults	Both Charge MOSFET Q1 and Discharge MOSFET Q2 are on. The battery pack is available for charging or discharging.	On	On	Active	Active
CELL CHARGING FAULT/RESET					
Charge Current Limit Fault: $V_{Pin\ 7} \geq (V_{Pin\ 6} + 18\ mV)$ for 1.0 s	Charge MOSFET Q1 is latched off and the cells are disconnected from the charging source. Q1 will remain in the off state as long as $V_{Pin\ 16}$ exceeds $V_{Pin\ 11}$ by ≈ 2.0 V. The battery pack is available for discharging.	On to Off	On	Active	Active
Charge Current Limit Reset: $V_{Pin\ 16} - V_{Pin\ 8} < 2.0\ V$	The Sense Enable circuit will reset and turn on charge MOSFET Q1 when $V_{Pin\ 16}$ no longer exceeds $V_{Pin\ 11}$ by ≈ 2.0 V. This can be accomplished by either disconnecting the charger from the battery pack, or by connecting a load to the battery pack.	Off to On	On	Active	Active
Charge Voltage Limit Fault: $V_{Pin\ 5} \geq 1.23\ V$ for 1.0 s	Charge MOSFET Q1 is latched off and the cells are disconnected from the charging source. An internal current source pull–up of 2.0 µA is applied to Pin 8 creating an input hysteresis voltage of V_H with divider resistors R1 and R2. The battery pack is available for discharging.	On to Off	On	Active	Active
Charge Voltage Limit Reset: $V_{Pin\ 5} < 1.23\ V$ for 1.0 s	Charge MOSFET Q1 will turn on when the voltage across each cell falls sufficiently to overcome the input hysteresis voltage. This can be accomplished by applying a load to the battery pack.	Off to On	On	Active	Active
CELL DISCHARGING FAULT/RESET					
Discharge Current Limit Fault: $V_{Pin\ 6} \leq (V_{Pin\ 2} - 50\ mV)$ for 3.0 ms	Discharge MOSFET Q2 is latched off and the cells are disconnected from the load. Q2 will remain in the off state as long as $V_{Pin\ 11}$ exceeds $V_{Pin\ 16}$ by ≈ 2.0 V. The battery pack is available for charging.	On	On to Off	Active	Active
Discharge Current Limit Reset: $V_{Pin\ 8} - V_{Pin\ 16} < 2.0\ V$	The Sense Enable circuit will reset and turn on discharge MOSFET Q2 when $V_{Pin\ 11}$ no longer exceeds $V_{Pin\ 16}$ by ≈ 2.0 V. This can be accomplished by either disconnecting the load from the battery pack, or by connecting the battery pack to the charger.	On	Off to On	Active	Active
Discharge Voltage Limit Fault: $V_{Pin\ 4} \leq 1.23\ V$ for 1.0 s	Discharge MOSFET Q2 is latched off, the cells are disconnected from the load, and the protection circuit enters a low current sleepmode state. The battery pack is available for charging.	On	On to Off	Disabled	Disabled
Discharge Voltage Limit Reset: $V_{Pin\ 16} > (V_{Pin\ 8} + 0.6\ V)$	The Sense Enable circuit will reset and turn on discharge MOSFET Q2 when $V_{Pin\ 16}$ exceeds $V_{Pin\ 8}$ by 0.6 V. This can be accomplished by connecting the battery pack to the charger.	On	Off to On	Active	Active
FAULTY CELL					
Simultaneous Charge and Discharge Voltage Limit Faults: $V_{Pin\ 5} \geq 1.23\ V$ for 1.0 s and $V_{Pin\ 4} \leq 1.23\ V$ for 1.0 s	This condition can happen if there is a defective cell in the battery pack. The protection circuit will remain in the sleepmode state until the battery pack is connected to a charger. If Cell 2, 3, or 4 is faulty and a charger is connected, the protection circuit will cycle in and out of sleepmode. If Cell 1 is faulty (<1.5 V), the protection circuit logic will not function and the battery pack cannot be charged.	Cycles Cell 1 Good Disabled Cell 1 Faulty	Cycles Cell 1 Good Disabled Cell 1 Faulty	Cycles Cell 1 Good Disabled Cell 1 Faulty	Cycles Cell 1 Good Disabled Cell 1 Faulty

NOTE: Cell balancing is not active when programmed for one cell operation.

Figure 7. Four Cell Smart Battery Pack

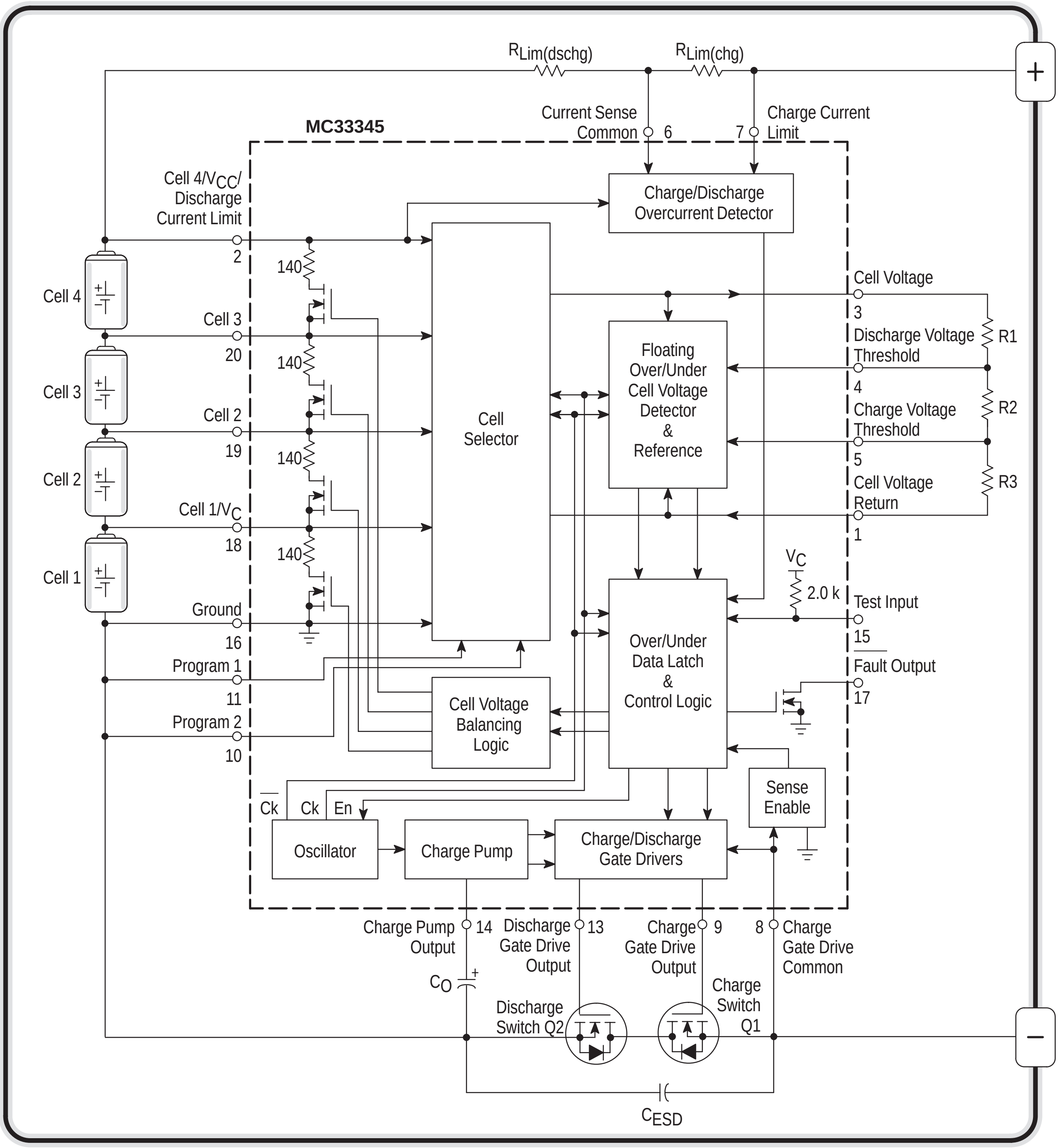


Figure 8. Three Cell Smart Battery Pack

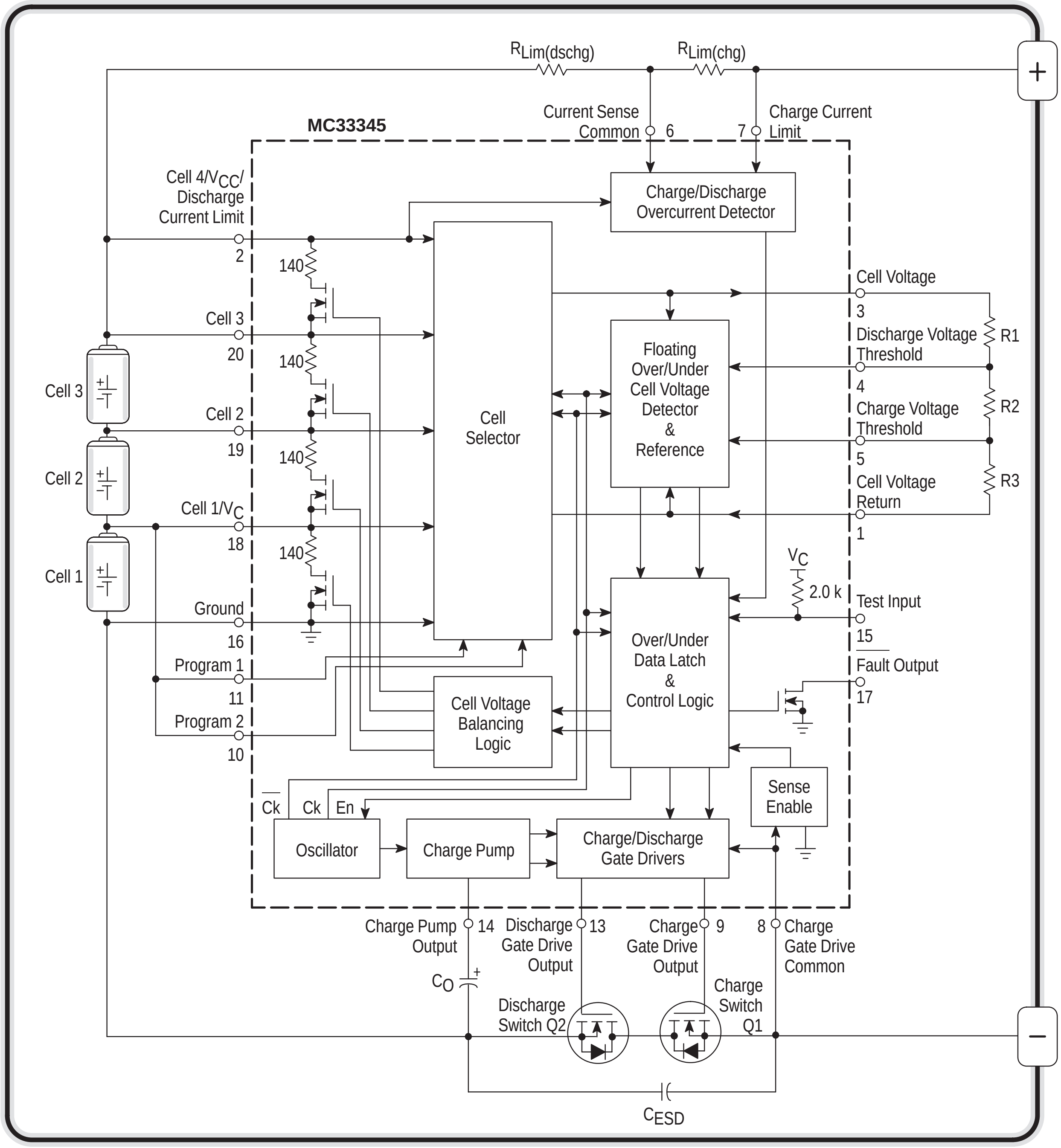


Figure 9. Two Cell Smart Battery Pack

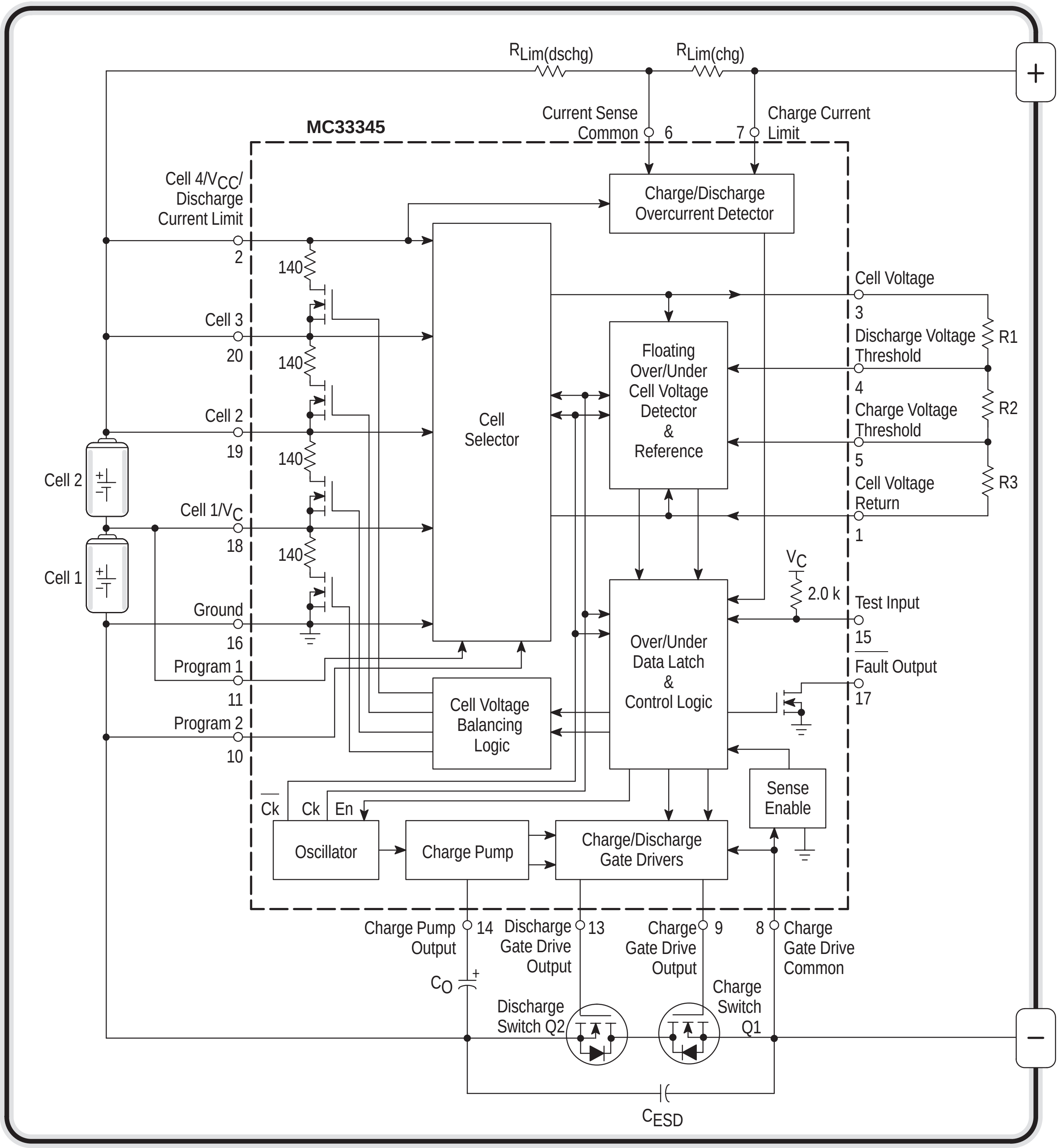
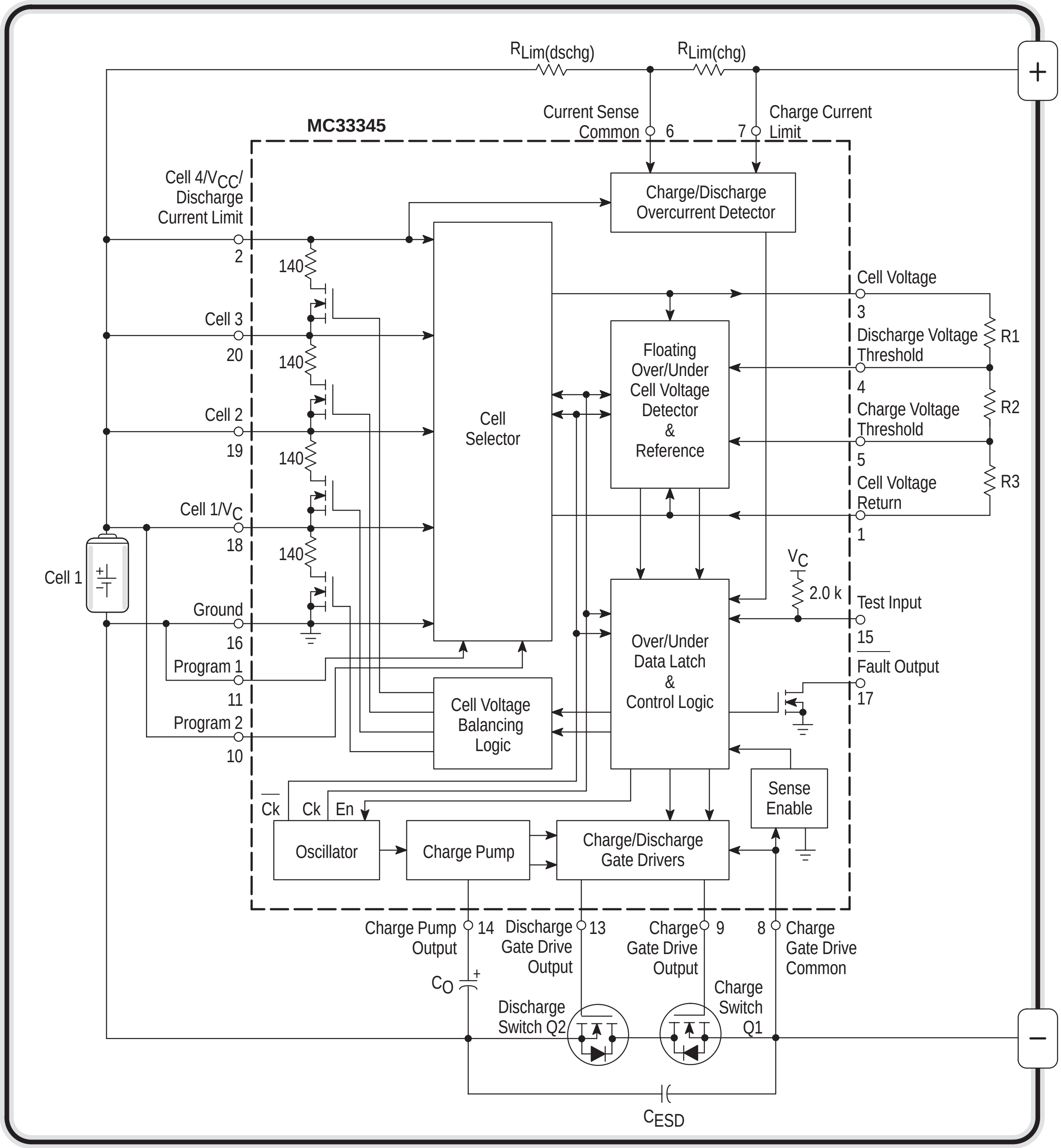


Figure 10. One Cell Smart Battery Pack



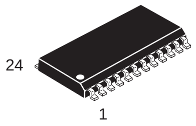
MC33346

Product Preview

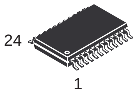
Lithium Battery Protection Circuit for Three or Four Cell Battery Packs

LITHIUM BATTERY PROTECTION CIRCUIT FOR THREE OR FOUR CELL SMART BATTERY PACKS

The MC33346 is a monolithic lithium battery protection circuit that is designed to enhance the useful operating life of three or four cell rechargeable battery packs. Cell protection features consist of independently programmable charge and discharge limits for both voltage and current with a delayed current shutdown, cell voltage balancing with on–chip balancing resistors, and virtually zero current sleepmode state when the cells are discharged. Additional features consists of a six wire microcontroller interface bus that can selectively provide a pulse output that represents the internal reference voltage, cell voltage, cell current and temperature, as well as control the states of four internal balancing and two external MOSFET switches. A microcontroller time reference output is available for gas gauge implementation. This protection circuit requires a minimum number of external components and is targeted for inclusion within the battery pack. The MC33346 is available in standard and low profile 24 lead surface mount packages.



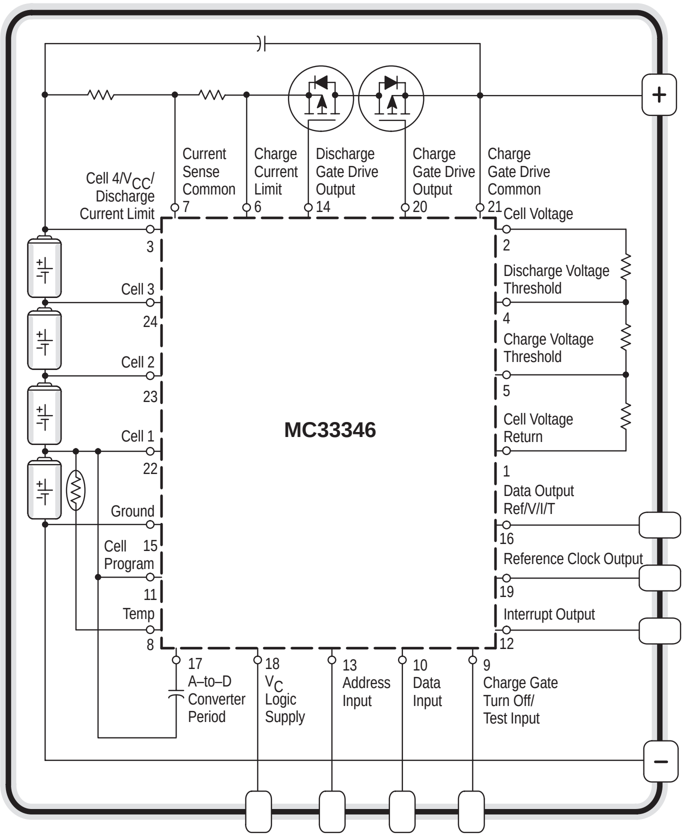
DW SUFFIX
PLASTIC PACKAGE
CASE 751E
(SO–24L)



DTB SUFFIX
PLASTIC PACKAGE
CASE 948H
(TSSOP–24)

- Independently Programmable Charge and Discharge Limits for Both Voltage and Current
- Delayed Current Shutdown
- Cell Voltage Balancing with On–Chip Resistors
- Six Wire Microcontroller Interface Bus
- Data Output for Reference, Voltage, Current, and Temperature
- Microcontroller Time Reference Output for Gas Gauging
- Virtually Zero Current Sleepmode State when Cells are Discharged
- Programmable for Three or Four Cell Applications
- Minimum External Components for Inclusion within the Battery Pack
- Available in Low Profile Surface Mount Packages

Typical Four Cell Smart Battery Pack



This device contains 4760 active transistors.

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC33346DW	T_A = –40° to +85°C	SO–24L
MC33346DTB		TSSOP–24

MOTOROLA

MC33347

Product Preview

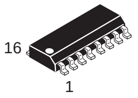
Lithium Battery Protection Circuit for One or Two Cell Battery Packs

The MC33347 is a monolithic lithium battery protection circuit that is designed to enhance the useful operating life of one or two cell rechargeable battery packs. Cell protection features consist of independently programmable charge and discharge limits for both voltage and current with a delayed current shutdown, continuous cell voltage balancing with the choice of on–chip or external balancing resistors, and a virtually zero current sleepmode state when the cells are discharged. Additional features include an on–chip charge pump for reduced MOSFET losses while charging or discharging a low cell voltage battery pack, and the programmability for one or two cell battery pack. This protection circuit requires a minimum number of external components and is targeted for inclusion within the battery pack. This MC33347 is avaialble in standard and low profile 16 lead surface mount packages.

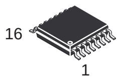
- Independently Programmable Charge and Discharge Limits for Both Voltage and Current
- Charge and Discharge Current Limit Detection with Delayed Shutdown
- Continuous Cell Voltage Balancing
- On–Chip or External Balancing Resistors
- Virtually Zero Current Sleepmode State when Cells are Discharged
- Charge Pump for Reduced Losses with a Low Cell Voltage Battery Pack
- Programmable for One or Two Cell Applications
- Minimum External Components for Inclusion within the Battery Pack
- Available in Low Profile Surface Mount Packages

LITHIUM BATTERY PROTECTION CIRCUIT FOR ONE OR TWO CELL SMART BATTERY PACKS

SEMICONDUCTOR TECHNICAL DATA

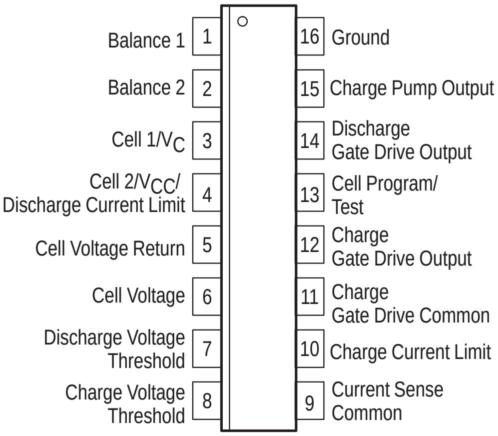


D SUFFIX
PLASTIC PACKAGE
CASE 751B
(SO–16)



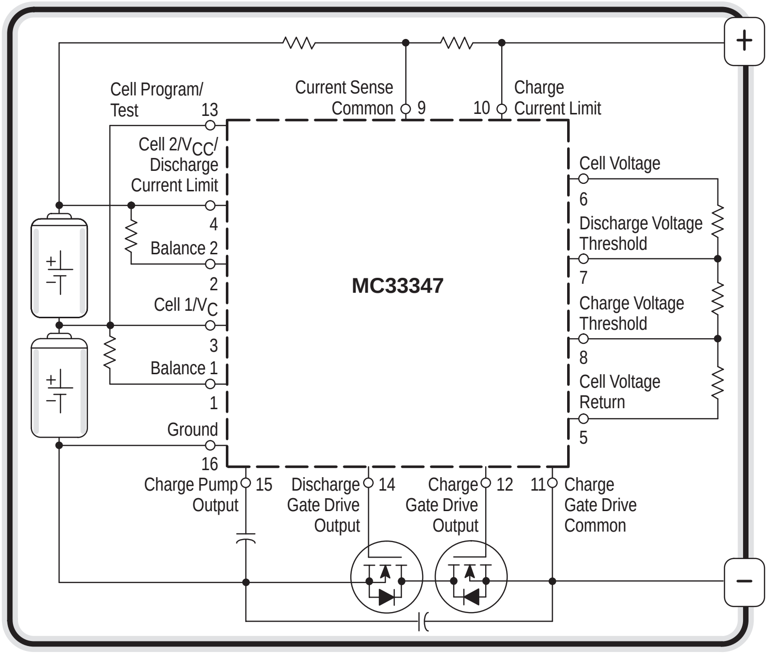
DTB SUFFIX
PLASTIC PACKAGE
CASE 948F
(TSSOP–16)

PIN CONNECTIONS



(Top View)

Typical Two Cell Smart Battery Pack



This device contains 1543 active transistors.

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC33347D	T_A = –25° to +85°C	SO–16
MC33347DTB		TSSOP–16

MAXIMUM RATINGS

Ratings	Symbol	Value	Unit
Input Voltage (Measured with Respect to Ground, Pin 16)	V_{IR}		V
Balance 1, 2 (Pin 1, 2)		15	
Cell 1/V_C (Pin 3)		7.5	
Cell 2/V_{CC}/Discharge Current Limit (Pin 4)		18	
Cell Voltage Divider (Pins 5, 6, 7 and 8)		18	
Current Sense Common (Pin 9)		30	
Charge Current Limit (Pin 10)		30	
Charge Gate Drive Common (Pin 11)		±20	
Charge Gate Drive Output (Pin 12)		18 to –20	
Cell Program/Test (Pin 13)		7.5	
Discharge Gate Drive Output (Pin 14)		18	
Charge Pump Output (Pin 15)		18	
External Cell Balancing Current (Pin 1, 2, Note 1)	I_{bal}	1.0	A
Cell Voltage Divider Current	I_{div}		mA
Source Current (Pin 4 to 6)		0.5	
Sink Current (Pin 5 to 16)		0.5	
Thermal Resistance, Junction–to–Air	$R_{\theta JA}$		°C/W
DTB Suffix, TSSOP–16 Plastic Package, Case 948F		176	
D Suffix, SO–16 Plastic Package, Case 751B		145	
Operating Junction Temperature (Notes 1, 2 and 3)	T_J	–40 to +150	°C
Storage Temperature	T_{stg}	–55 to +150	°C

NOTE: ESD data available upon request.

ELECTRICAL CHARACTERISTICS (V_{CC} (Pin 4) = 8.0 V, V_C (Pin 3) = 4.0 V, T_A = 25°C, for min/max values T_A is the operating junction temperature range that applies (Notes 2 and 3), unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
VOLTAGE SENSING					
Charge or Discharge Voltage Inputs (Pin 7 or 8 to Pin 5)					
Threshold Voltage	V_{th}	–	1.230	–	V
Input Bias Current	I_{IB}	–	20	–	nA
Input Hysteresis Source Current (Pin 8)	I_H	–	2.0	–	µA
Cell Charge or Discharge Programmable Input Voltage Range (Pin 7 or 8)	$V_{IR(pgm)}$	–	V_{th} to 7.5	–	V
Cell Selector Series Resistance					Ω
Cell Positive to Top of Divider (Pin 3 or 4 to Pin 6)	R_{S+}	–	100	–	
Cell Negative to Bottom of Divider (Pin 3 or 16 to Pin 5)	R_{S-}	–	100	–	
Cell Voltage Sampling Rate	$t_{(smpl)}$	–	1.0	–	s
Cell Program/ Test Input Threshold Voltage (Pin 13)	V_{th}	–	$V_{Cell\ 1}/2.0$	–	V
CELL VOLTAGE BALANCING					
Cell Voltage Balancing Accuracy (Note 4)	ΔV	–	1.0	–	%
Internal Balancing Resistance (Pin 3, 4)	R_{bal}	–	80	–	Ω
Balancing MOSFET On Resistance (Pin 1, 2)	$R_{DS(on)}$	–	1.0	–	Ω

NOTES: 1. Maximum package power dissipation limits must be observed.
2. Low duty cycle pulse techniques are used during test to maintain the junction temperature as close to ambient as possible.
3. Tested ambient temperature range for the MC33347:
T_{low} = –25°C T_{high} = +85°C
4. Cell voltage balancing accuracy is defined as: $\left|\frac{\Delta V}{V_{avg}}\right| \times 100 = \left|\frac{V_{Cell\ 1} - V_{Cell\ 2}}{\left(\frac{V_{Cell\ 1} + V_{Cell\ 2}}{2}\right)}\right| \times 100$

ELECTRICAL CHARACTERISTICS (continued) (V_{CC} (Pin 4) = 8.0 V, V_C (Pin 3) = 4.0 V, T_A = 25°C, for min/max values T_A is the operating junction temperature range that applies (Notes 2 and 3), unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
CURRENT SENSING					
Charge Current Limit (Pin 10 to Pin 9)					
Threshold Voltage	$V_{th(chg)}$	–	18	–	mV
Input Bias Current	$I_{IB(chg)}$	–	200	–	nA
Delay	$I_{dly(chg)}$	–	3.0	–	ms
Discharge Current Limit (Pin 4 to Pin 9)					
Threshold Voltage	$V_{th(dschg)}$	–	50	–	mV
Input Bias Current	$I_{IB(dschg)}$	–	200	–	nA
Delay	$I_{dly(dschg)}$	–	3.0	–	ms
CHARGE PUMP					
Output Voltage (Pin 15, $R_L \geq 10^{10}$ Ω)	V_O	–	10.2	–	V
TOTAL DEVICE					
Average Cell Current	I_{CC}				
Operating (V_{CC} = 8.0 V)		–	12.5	–	µA
Sleepmode (V_{CC} = 5.0 V)		–	15	–	nA
Minimum Operating Cell Voltage for Logic and Gate Drivers	V_{CC}				V
Programmed for Two Cell Operation					
Cell 1 Voltage		–	1.5	–	
Cell 2 Voltage		–	0	–	
Programmed for One Cell Operation					
Cell 1 Voltage		–	1.5	–	

NOTES: 1. Maximum package power dissipation limits must be observed.
2. Low duty cycle pulse techniques are used during test to maintain the junction temperature as close to ambient as possible.
3. Tested ambient temperature range for the MC33347:
T_{low} = –25°C T_{high} = +85°C
4. Cell voltage balancing accuracy is defined as:

$$\left|\frac{\Delta V}{V_{avg}}\right| \times 100 = \left|\frac{V_{Cell\ 1} - V_{Cell\ 2}}{\left(\frac{V_{Cell\ 1} + V_{Cell\ 2}}{2}\right)}\right| \times 100$$

PIN FUNCTION DESCRIPTION

Pin	Symbol	Description
1	Balance 1	This is the drain connection to an internal MOSFET. An external resistor is placed from this pin to the positive terminal of Cell 1 for increased cell balancing capability. This allows most of the additional power to be dissipated off–chip.
2	Balance 2	This is the drain connection to an internal MOSFET. An external resistor is placed from this pin to the positive terminal of Cell 2 for increased cell balancing capability. This allows most of the additional power to be dissipated off–chip.
3	Cell 1/V_C	This is a multifunction pin that connects to a high impedance node of the Cell Selector where it is used to monitor the positive terminal of Cell 1 and the negative terminal of Cell 2. This pin also provides logic biasing and a discharge path for the internal balancing of Cell 1.
4	Cell 2/V_{CC}/ Discharge Current Limit	This is a multifunction pin that connects to a high impedance node of the Cell Selector where it is used to monitor the positive terminal of Cell 2 and to provide positive supply voltage for the protection IC. This pin is also used to monitor the voltage drop across the discharge current limit resistor and it provides a discharge path for the internal balancing of Cell 2.
5	Cell Voltage Return	The bottom side of a three resistor divider string connects to this pin. The Cell Selector internally switches this point to the negative terminal of the cell that is to be monitored.
6	Cell Voltage	The top side of a three resistor divider string connects to this pin. The Cell Selector internally switches this point to the positive terminal of the cell that is to be monitored.
7	Discharge Voltage Threshold	The upper tap of a three resistor divider string connects to this pin. The Cell Voltage Detector compares the divided down cell voltage to an internal reference. If the comparator detects that the cell voltage has fallen below the programmed level for three consecutive samples, discharge switch Q2 is disabled, and the protection circuit enters into a low current sleepmode state. This prevents further discharging of the battery pack.
8	Charge Voltage Threshold	The lower tap of a three resistor divider string connects to this pin. The Cell Voltage Detector compares the divided down cell voltage to an internal reference. If the comparator detects that the cell voltage has risen above the programmed level, charge switch Q1 is disabled, preventing further charging of the battery pack. A 2.0 µA current source pull–up is internally applied to this pin creating input hysteresis.
9	Current Sense Common	This pin is a common point that is used to monitor the voltage drop across the charge and discharge current limit resistors.
10	Charge Current Limit	This pin is used to monitor the voltage drop across the charge current limit resistor.
11	Charge Gate Drive Common	This pin provides a gate turn–off path for charge switch Q1. The charge switch source and the battery pack negative terminal connect to this point.
12	Charge Gate Drive Output	This output connects to the gate of charge switch Q1 allowing it to enable or disable battery pack charging.
13	Cell Program/Test	This is a multifunction input that is used to program the number of cells and to facilitate circuit testing. This input is connected to Pin 3 for two cell operation, and to Pin 16 for one cell operation.
14	Discharge Gate Drive Output	This output connects to the gate of discharge switch Q2 allowing it to enable or disable battery pack discharging.
15	Charge Pump Output	This is the charge pump output. A reservoir capacitor is connected from this pin to ground.
16	Ground	This is the protection IC ground and all voltage ratings are with respect to this pin.

INTRODUCTION

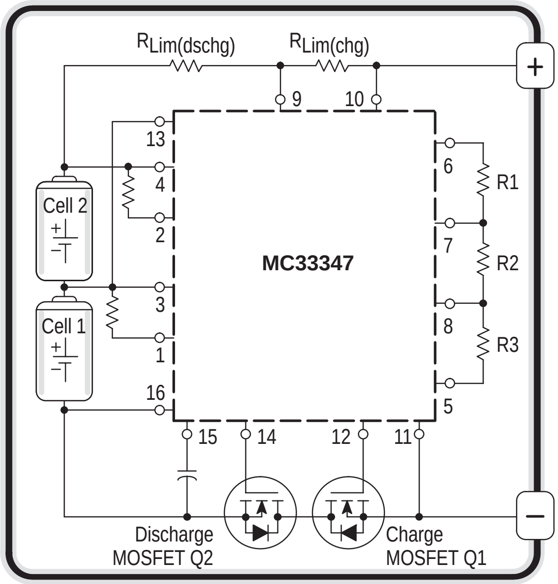
The insatiable demand for smaller lightweight portable electronic equipment has dramatically increased the requirements of battery performance. Batteries are expected to have higher energy densities, superior cycle life, be safe in operation and environmentally friendly. To address these high expectations, battery manufacturers have invested heavily in developing rechargeable lithium–based cells. Today's most attractive chemistries include lithium–polymer, lithium–ion, and lithium–metal. Each of these chemistries require electronic protection in order to constrain cell operation to within the manufacturers limits.

Rechargeable lithium–based cells require precise charge and discharge termination limits for both voltage and current in order to maximize cell capacity, cycle life, and to protect the end user from a catastrophic event. The termination limits are not as well defined as with older non–lithium chemistries. These limits are dependent upon a manufacturer's particular lithium chemistry, construction technique, and intended application. Battery pack assemblers may also choose to enhance cell capacity at the expense of cycle life. In order to address these requirements the MC33347 was developed. This device features programmable voltage and current limits, cell voltage balancing, low operating current, a virtually zero current sleepmode state, and requires few external components to implement a complete one or two cell smart battery pack.

OPERATING DESCRIPTION

The MC33347 is specifically designed to be placed in the battery pack where it is continuously powered from either one or two lithium cells. In order to maintain cell operation within specified limits, the protection circuit senses both cell voltage and current, and correspondingly controls the state of two N–channel MOSFET switches. These switches, Q1 and Q2, are placed in series with the negative terminal of Cell 1 and the negative terminal of the battery pack. This configuration allows the protection circuit to interrupt the appropriate charge or discharge path FET in the event that a programmed voltage or current limit for either cell has been exceeded.

Figure 1. Simplified Two Cell Smart Battery Pack



A functional description of the protection circuit blocks follows. Refer to the detailed block diagram shown in Figures 7 and 8.

Voltage Sensing

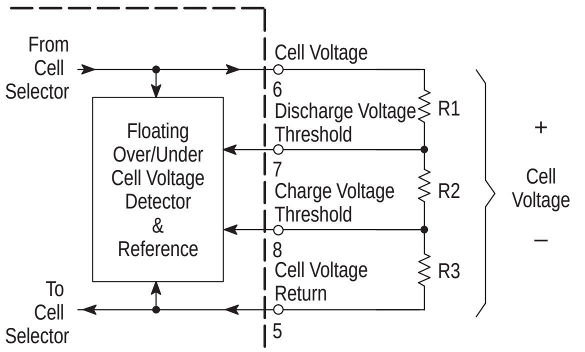
Individual cell voltage sensing is accomplished by the use of the Cell Selector in conjunction with the Floating Over/Under Voltage Detector and Reference block. The Cell Selector applies the voltage of each cell across an external resistor divider string that connects from Pins 6 to 5. The voltage at each of the tap points is sequentially polled and compared to an internal reference. If a limit has been exceeded, the result is stored in the Over/Under Data Latch and Control Logic block. The Cell Selector is gated on for a 1.0 ms period at a one second repetition rate. This low duty cycle sampling technique reduces the average load current that the divider presents across each cell, thus extending the useful battery pack capacity. The cells are sensed in the following sequence:

Figure 2. Cell Sensing Sequence

Polling Sequence	Time (ms)	Cell Sensed	Tested Limit
1	0.25	Cell 2	Overvoltage
2	0.25	Cell 1	Overvoltage
3	0.25	Cell 2	Undervoltage
4	0.25	Cell 1	Undervoltage

By incorporating this polling technique with a single floating comparator and voltage divider, a significant reduction of circuitry and trim elements is achieved. This results in a smaller die size, lower cost, and reduced operating current.

Figure 3. Cell Voltage Limit Programming



The cell charge and discharge voltage limits are controlled by the values selected for the resistor divider string and the 1.23 V input threshold of Pins 7 and 8. As the battery pack reaches full charge, the Cell Voltage Detector will sense an overvoltage fault condition on the first cell that exceeds the programmed overvoltage limit. The fault information is stored in a data latch and charge MOSFET Q1 is turned off, disconnecting the battery pack from the charging source. An internal 2.0 μA current source pull–up is then applied to Pin 8 creating an input hysteresis voltage. As a result of an overvoltage fault, the battery pack is available for discharging only.

The overvoltage fault is reset by applying a load to the battery pack. As the voltage across each cell falls below the input hysteresis level, charge MOSFET Q1 will turn on. The battery pack will now be available for charging or discharging. The over voltage limit and hysteresis voltage are given by:

$$V_{OV} = V_{th\ (Pin\ 8)}\left(\frac{R1 + R2 + R3}{R3}\right)$$

$$V_H = I_{H\ (Pin\ 8)}(R1 + R2)$$

As the load eventually depletes the battery pack charge, the Cell Voltage Detector will sense an undervoltage fault condition on the first cell that falls below the programmed undervoltage limit. After three consecutive faults are detected, discharge MOSFET Q2 is turned off, disconnecting the battery pack from the load. The protection circuit will now enter a low current sleepmode state drawing just 15 nA, thus preventing any further cell discharging. As a result of the undervoltage fault, the battery pack is available for charging only. The undervoltage limit is given by:

$$V_{UV} = V_{th\ (Pin\ 7)}\left(\frac{R1 + R2 + R3}{R2 + R3}\right)$$

The undervoltage logic is designed to automatically reset if less than three consecutive faults appear. This helps to prevent a premature disconnection of the load during high current pulses when the battery pack charge is close to being depleted.

The undervoltage fault is reset by applying charge current to the battery pack. When the voltage on Pin 16 exceeds Pin 11 by 0.6 V, discharge MOSFET Q2 will turned on. The battery pack will now be available for charging or discharging.

Since the thresholds of Pin 7 and 8 are equal, the above equations can be rewritten to directly solve for specific resistor values as shown in the example below.

Let the desired limits be:

V_{OV} = 4.2 V, V_H = 0.4 V, and V_{UV} = 2.5 V

With nominal values for:

V_{th} = 1.23 V, and I_H = 2.0 µA

$$R3 = \frac{\left(\frac{V_H}{I_H}\right)}{\left(\frac{V_{OV}}{V_{th}} - 1\right)} = \frac{\left(\frac{0.4}{2.0 \times 10^{-6}}\right)}{\left(\frac{4.2}{1.23} - 1\right)} = 82{,}828\ \Omega$$

$$R2 = R3\left(\frac{V_{OV}}{V_{UV}} - 1\right) = 82{,}828\left(\frac{4.2}{2.5} - 1\right) = 56{,}323\ \Omega$$

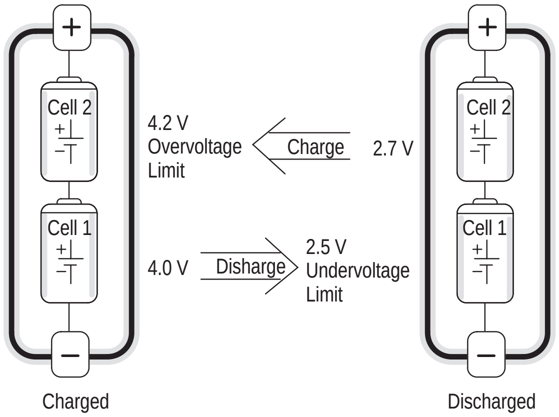
$$R1 = \left(\frac{V_H}{I_H}\right) - R2 = \left(\frac{0.4}{2.0 \times 10^{-6}}\right) - 56{,}323 = 143{,}677\ \Omega$$

Note that the Cell Selector has a maximum total series resistance of 200 Ω. This will have a minimal effect on the programmed limits if the total divider resistance is in excess of 100 kΩ.

Cell Voltage Balancing

With series connected cells, successive charge and discharge cycles can result in a significant difference in cell voltage with a corresponding degradation of battery pack capacity. Figure 4 illustrates the operation of an unbalanced pack. As the cells become unbalanced, the full battery pack capacity is not realized. This is due to the requirement that charging must terminate when Cell 2 reaches the overvoltage limit, and discharging must terminate when Cell 1 reaches the undervoltage limit. By employing a method of keeping the cell voltages equal, both cells can be charged and discharged to their specified limits, thus attaining the maximum possible capacity.

Figure 4. Unbalanced Battery Pack Operation



The MC33347 contains a Cell Voltage Balancing Amplifier that controls four N–channel MOSFETs. The amplifier samples the cell voltages during the polling period. If the detected cell voltage difference exceeds 1.0 %, the MOSFET that connects across the higher voltage cell is turned on. The excess charge will eventually be bled off through the internal 80 Ω resistor with a typical balancing current that ranges from 40 mA to 80 mA. If higher balancing currents are desired, Pins 1 and 2 provide a means for paralleling a lower value external resistor for in excess of 500 mA. The use of an external resistor allows a reduction of on–chip power dissipation. Cell voltage balancing is active during charge and discharge, but disabled during the low current sleepmode state.

Cell Programming and Test

The protection circuit can be programmed for operation with either one or two cell battery packs. The Cell Programming/Test input, Pin 13, is used to control the Cell Selector and to enable or disable the Cell Voltage Balancing Amplifier. For one cell operation, Pin 13 is connected to Pin 16, and Pin 4 is connected to Pin 3 and the positive terminal of Cell 1, refer to Figure 8. For two cell operation, Pin 13, is connected to Pin 3 and the positive terminal of Cell 1, and Pin 4 is connected to the positive terminal of Cell 2, refer to Figure 7.

A test option is provided to speed up device and battery pack testing. By biasing Pin 13 above Pin 3 by 2.0 V, the internal logic is held in a reset state and both MOSFET switches are turned on. Upon release, the logic becomes active and the cells are polled within 2.0 ms.

Current Sensing

Charge and discharge current limit protection can be selectively added to the battery pack with the addition of a sense resistor. The resistors are placed in series with the positive terminal of the battery pack and the cells. Refer to Figure 1.

As the battery pack charges, Pins 9 and 10 sense the voltage drop across $R_{Lim(chg)}$. A charge current limit fault is detected if the voltage at Pin 10 exceeds Pin 9 by 18 mV. The fault information is stored in a data latch and charge MOSFET Q1 is turned off, disconnecting the battery pack from the charging source. As a result of the charge current fault, the battery pack is available for discharging only. The charge current limit is given by:

$$I_{Lim(chg)} = \frac{V_{th(chg)}}{R_{Lim(chg)}} = \frac{18\ mV}{R_{Lim(chg)}}$$

The charge current fault is reset by either disconnecting the battery pack from the charger, or by connecting a load to the battery pack. When the voltage on Pin 16 no longer exceeds Pin 11 by approximately 2.0 V, the Sense Enable circuit will turn on charge MOSFET Q1. Charge current sensing can be disabled by connecting Pin 10 to Pin 9.

The discharge current limiting operates in a similar manner. As the battery pack discharges, Pins 4 and 9 sense the voltage drop across $R_{Lim(dschg)}$. A discharge current limit fault is detected if the voltage at Pin 4 is less than Pin 9 by 50 mV. The fault information is stored in a data latch and discharge MOSFET Q2 is turned off, disconnecting the battery pack from the load. As a result of the discharge current fault, the battery pack is available for charging only. The discharge current limit is given by:

$$I_{Lim(dschg)} = \frac{V_{th(dschg)}}{R_{Lim(dschg)}} = \frac{50\ mV}{R_{Lim(dschg)}}$$

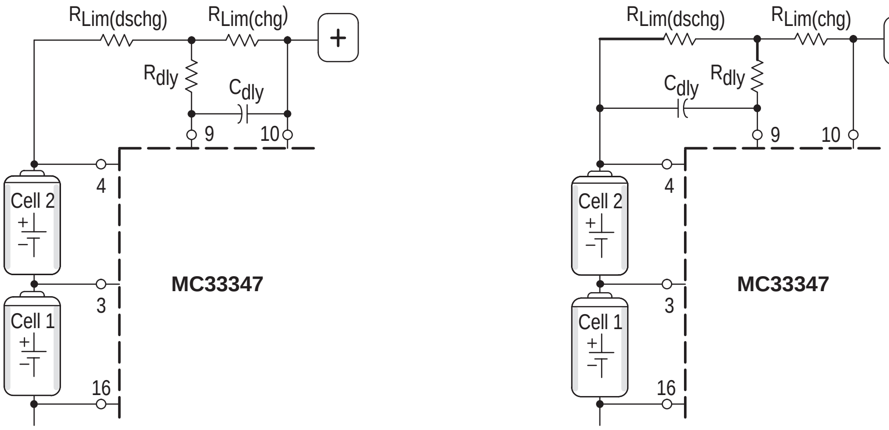
The discharge current fault is reset by either disconnecting the load from the battery pack, or by connecting the battery pack to the charger. When the voltage on Pin 11 no longer exceeds Pin 16 by approximately 2.0 V, the Sense Enable circuit will turn on discharge MOSFET Q2. Discharge current sensing can be disabled by connecting Pin 4 to Pin 9.

The charge and discharge current protection circuits contain a built in response delay of 3.0 ms. This helps to prevent fault activation when the battery pack is subjected to pulsed currents during charging or discharging. An additional current sense delay can selectively be added as shown in Figure 5.

Charge Pump and MOSFET Switches

The MC33347 contains an on chip Charge Pump to ensure that the MOSFET switches are fully enhanced for reduced power losses. An external reservoir capacitor normally connects from the Charge Pump output to ground, Pins 15 and 16. The capacitor value is not critical and is usually within the range of 10 nF to 100 nF. The Charge Pump output is regulated at 10.2 V allowing the use of economical logic level MOSFETs in one and two cell applications. The main requirement in selecting a particular type of MOSFET switch is to consider the desired on–resistance at the lowest anticipated operating voltage of the battery pack. A table of small outline surface mount devices is given in Figure 6. When using extremely low threshold MOSFETs, it may be desirable to disable the Charge Pump so that the maximum gate to source voltage is not exceeded. This is accomplished by connecting Pin 15 to Pin 4. Application Figures 7 and 8 show a capacitor labeled C_{ESD}. This capacitor provides a path around the MOSFET switches in the event of an electrostatic discharge.

Figure 5. Additional Current Limit Delay



Charge Delay

Discharge Delay

Figure 6. Small Outline Surface Mount MOSFET Switches

Device Type	On–Resistance (Ω) versus Gate to Source Voltage (V)						
	2.5 V	**3.0 V**	**4.0 V**	**5.0 V**	**6.0 V**	**7.5 V**	**9.0 V**
MMFT3055VL	–	–	–	0.120 Ω	0.115 Ω	0.108 Ω	0.100 Ω
MMDF3N03HD	–	0.525 Ω	0.080 Ω	0.065 Ω	0.063 Ω	0.062 Ω	0.060 Ω
MMDF4N01HD	0.047 Ω	0.042 Ω	0.037 Ω	0.035 Ω	0.034 Ω	0.033 Ω	See Note
MMSF5N02HD	–	0.065 Ω	0.023 Ω	0.021 Ω	0.020 Ω	0.018 Ω	0.018 Ω
MMDF6N02HD	0.043 Ω	0.035 Ω	0.029 Ω	0.028 Ω	0.026 Ω	0.025 Ω	0.023 Ω

NOTE: Exceeds maximum V_{GS} voltage rating.

PROTECTION CIRCUIT OPERATING MODE TABLE

Input Conditions Cell Status	Circuit Operation Battery Pack Status	Outputs			
		MOSFET Switches		Function	
		Charge Q1	Discharge Q2	Charge Pump	Cell Balancing (See Note)
CELL CHARGING/DISCHARGING					
Storage or Nominal Operation: No current or voltage faults	Both Charge MOSFET Q1 and Discharge MOSFET Q2 are on. The battery pack is available for charging or discharging.	On	On	Active	Active
CELL CHARGING FAULT/RESET					
Charge Current Limit Fault: $V_{Pin\ 10} \geq (V_{Pin\ 9} + 18\ mV)$ for 3.0 ms	Charge MOSFET Q1 is latched off and the cells are disconnected from the charging source. Q1 will remain in the off state as long as $V_{Pin\ 16}$ exceeds $V_{Pin\ 11}$ by ≈ 2.0 V. The battery pack is available for discharging.	On to Off	On	Active	Active
Charge Current Limit Reset: $V_{Pin\ 16} - V_{Pin\ 11} < 2.0\ V$	The Sense Enable circuit will reset and turn on charge MOSFET Q1 when $V_{Pin\ 16}$ no longer exceeds $V_{Pin\ 11}$ by ≈ 2.0 V. This can be accomplished by either disconnecting the charger from the battery pack, or by connecting a load to the battery pack.	Off to On	On	Active	Active
Charge Voltage Limit Fault: $V_{Pin\ 8} \geq 1.23\ V$ for 1.0 s	Charge MOSFET Q1 is latched off and the cells are disconnected from the charging source. An internal current source pull–up of 2.0 μA is applied to Pin 8 creating an input hysteresis voltage of V_H with divider resistors R1 and R2. The battery pack is available for discharging.	On to Off	On	Active	Active
Charge Voltage Limit Reset: $V_{Pin\ 8} < 1.23\ V$ for 1.0 s	Charge MOSFET Q1 will turn on when the voltage across each cell falls sufficiently to overcome the input hysteresis voltage. This can be accomplished by applying a load to the battery pack.	Off to On	On	Active	Active
CELL DISCHARGING FAULT/RESET					
Discharge Current Limit Fault: $V_{Pin\ 4} \leq (V_{Pin\ 9} - 50\ mV)$ for 3.0 ms	Discharge MOSFET Q2 is latched off and the cells are disconnected from the load. Q2 will remain in the off state as long as $V_{Pin\ 11}$ exceeds $V_{Pin\ 16}$ by ≈ 2.0 V. The battery pack is available for charging.	On	On to Off	Active	Active
Discharge Current Limit Reset: $V_{Pin\ 11} - V_{Pin\ 16} < 2.0\ V$	The Sense Enable circuit will reset and turn on discharge MOSFET Q2 when $V_{Pin\ 11}$ no longer exceeds $V_{Pin\ 16}$ by ≈ 2.0 V. This can be accomplished by either disconnecting the load from the battery pack, or by connecting the battery pack to the charger.	On	Off to On	Active	Active
Discharge Voltage Limit Fault: $V_{Pin\ 7} \leq 1.23\ V$ for three consecutive 1.0 s samples	Discharge MOSFET Q2 is latched off, the cells are disconnected from the load, and the protection circuit enters a low current sleepmode state. The battery pack is available for charging.	On	On to Off	Disabled	Disabled
Discharge Voltage Limit Reset: $V_{Pin\ 16} > (V_{Pin\ 11} + 0.6\ V)$	The Sense Enable circuit will reset and turn on discharge MOSFET Q2 when $V_{Pin\ 16}$ exceeds $V_{Pin\ 11}$ by 0.6 V. This can be accomplished by connecting the battery pack to the charger.	On	Off to On	Active	Active
FAULTY CELL					
Simultaneous Charge and Discharge Voltage Limit Faults: $V_{Pin\ 8} \geq 1.23\ V$ for 1.0 s and $V_{Pin\ 7} \leq 1.23\ V$ for three consecutive 1.0 s samples	This condition can happen if there is a defective cell in the battery pack. The protection circuit will remain in the sleepmode state until the battery pack is connected to a charger. If Cell 2 is faulty and a charger is connected, the protection circuit will cycle in and out of sleepmode. If Cell 1 is faulty (<1.5 V), the protection circuit logic will not function and the battery pack cannot be charged.	Cycles Cell 1 Good Disabled Cell 1 Faulty	Cycles Cell 1 Good Disabled Cell 1 Faulty	Cycles Cell 1 Good Disabled Cell 1 Faulty	Cycles Cell 1 Good Disabled Cell 1 Faulty

NOTE: Cell balancing is not active when programmed for one cell operation.

Figure 7. Two Cell Smart Battery Pack

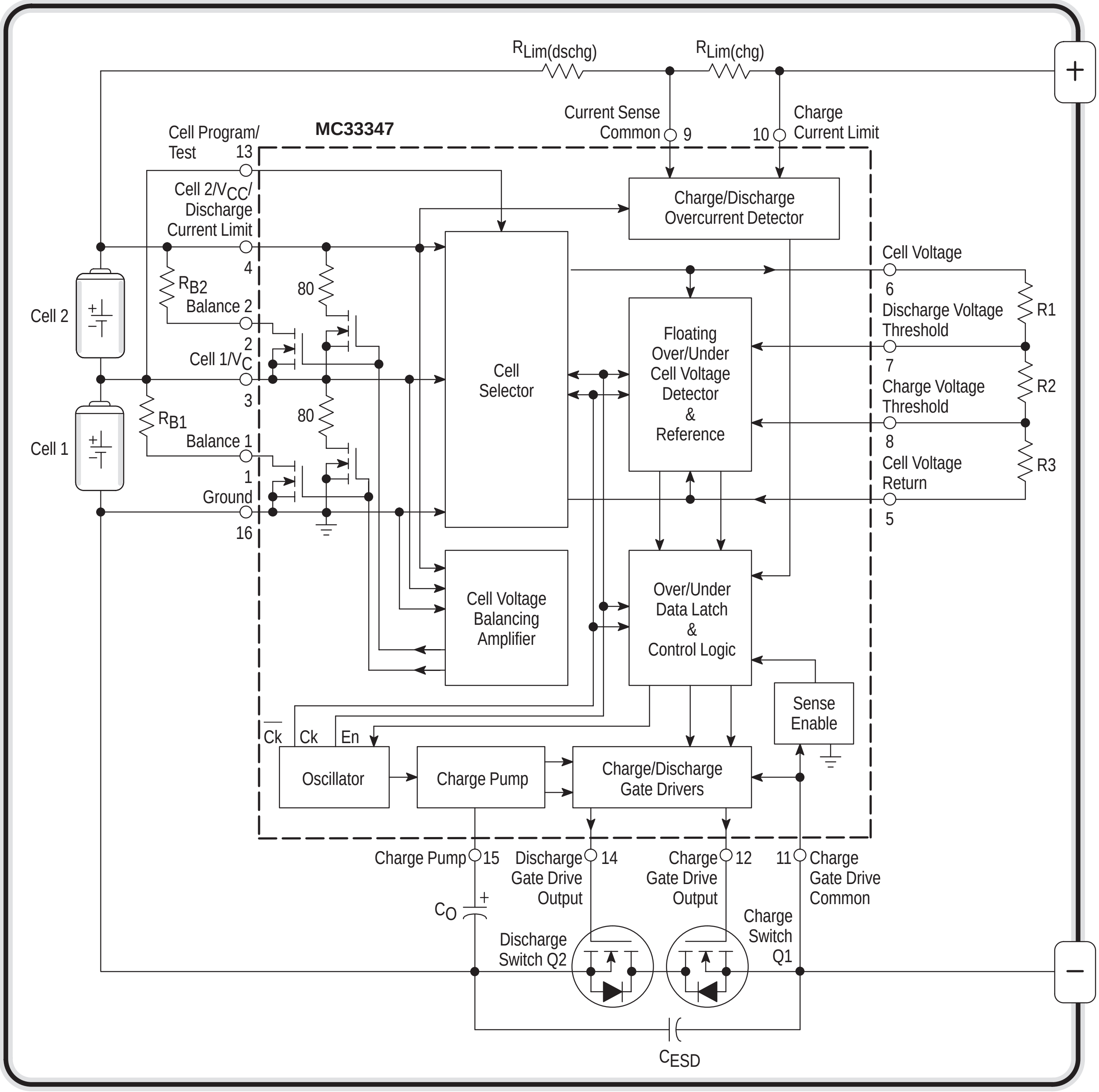
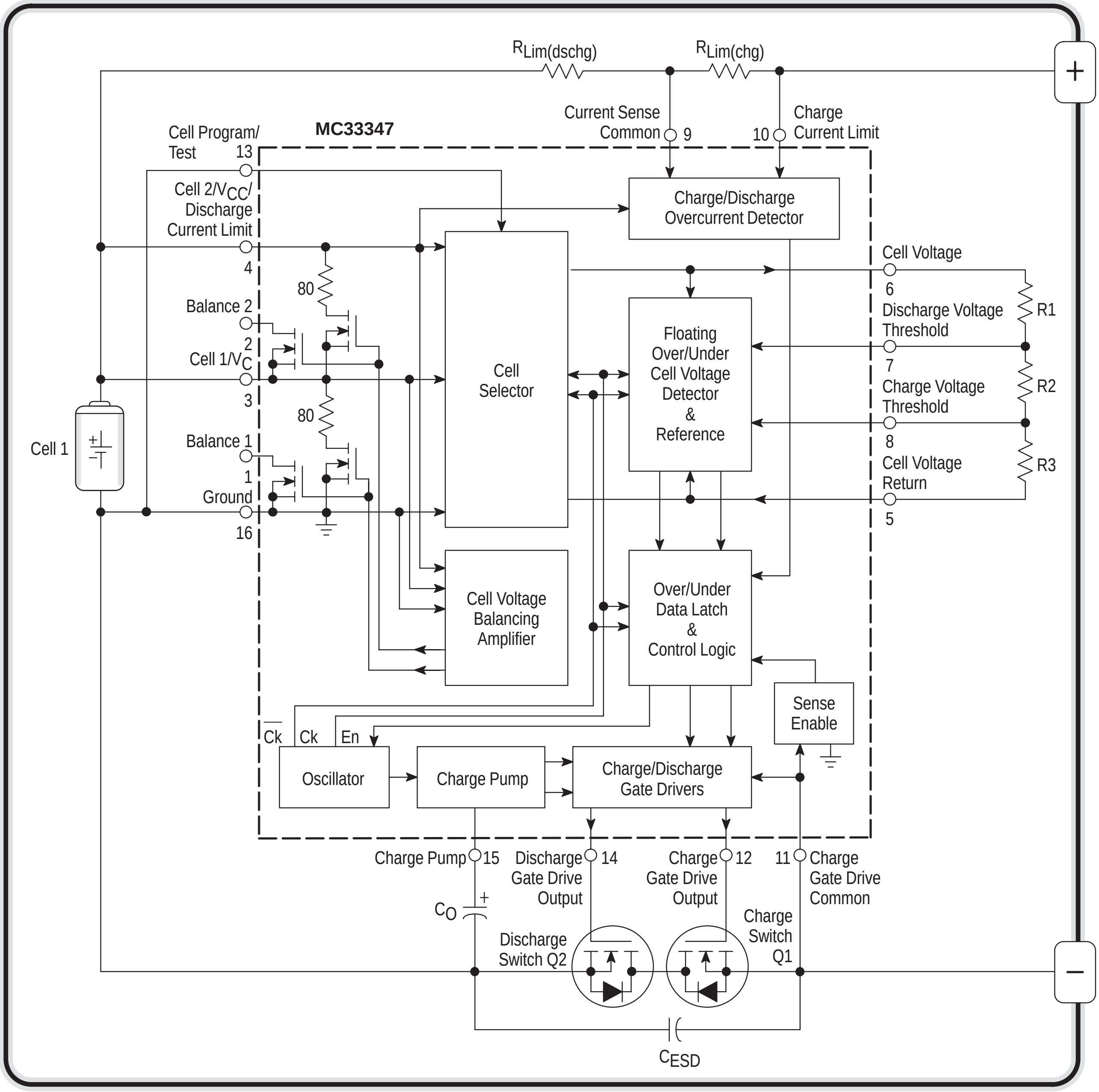


Figure 8. One Cell Smart Battery Pack



MOTOROLA

MC33348

Product Preview

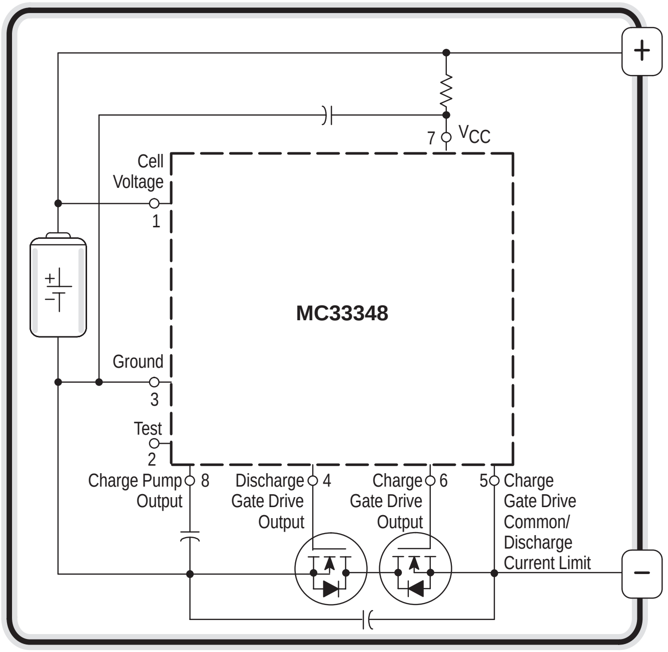
Lithium Battery Protection Circuit for One Cell Battery Packs

The MC33348 is a monolithic lithium battery protection circuit that is designed to enhance the useful operating life of one cell rechargeable battery pack. Cell protection features consist of internally trimmed charge and discharge voltage limits, discharge current limit detection with a delayed shutdown, and a virtually zero current sleepmode state when the cell is discharged. An additional feature includes an on–chip charge pump for reduced MOSFET losses while charging or discharging a low cell voltage battery pack. This protection circuit requires a minimum number of external components and is targeted for inclusion within the battery pack. This MC33348 is available in standard and micro 8 lead surface mount packages.

- Internally Trimmed Charge and Discharge Voltage Limits
- Discharge Current Limit Detection with Delayed Shutdown
- Virtually Zero Current Sleepmode State when Cells are Discharged
- Charge Pump for Reduced Losses with a Low Cell Voltage Battery Pack
- Dedicated for One Cell Applications
- Minimum Components for Inclusion within the Battery Pack
- Available in Low Profile Surface Mount Packages

Ordering Information shown on following page.

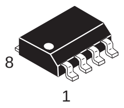
Typical One Cell Smart Battery Pack



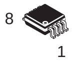
This device contains 1170 active transistors.

LITHIUM BATTERY PROTECTION CIRCUIT FOR ONE CELL SMART BATTERY PACKS

SEMICONDUCTOR TECHNICAL DATA

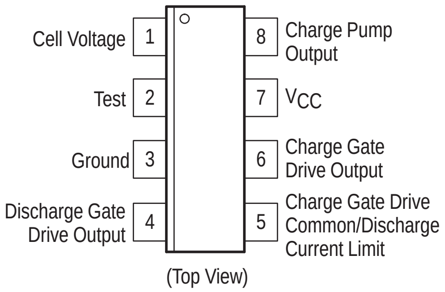


D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)



DM SUFFIX
PLASTIC PACKAGE
CASE 846A
(Micro–8)

PIN CONNECTIONS



ORDERING INFORMATION

Device	Charge Overvoltage Threshold (V)	Charge Overvoltage Hysteresis (mV)	Discharge Undervoltage Threshold (V)	Discharge Current Limit Threshold (mV)	Operating Temperature Range	Package
MC33348D–1	4.20	300	2.25	400	T_A = –25° to +85°C	SO–8
MC33348D–2				200		
MC33348D–3	4.25		2.28	400		
MC33348D–4				200		
MC33348D–5	4.35		2.30	400		
MC33348D–6				200		
MC33348DM–1	4.20		2.25	400		Micro–8
MC33348DM–2				200		
MC33348DM–3	4.25		2.28	400		
MC33348DM–4				200		
MC33348DM–5	4.35		2.30	400		
MC33348DM–6				200		

NOTE: Additional threshold limit options can be made available. Consult your local Motorola sales office for information.

MAXIMUM RATINGS

Ratings	Symbol	Value	Unit
Input Voltage (Measured with Respect to Ground, Pin 3) Cell Voltage (Pin 1) Test (Pin 2) Discharge Gate Drive Output (Pin 4) Charge Gate Drive Common/Discharge Current Limit (Pin 5) Charge Gate Drive Output (Pin 6) V_{CC} (Pin 7) Charge Pump Output (Pin 8)	V_{IR}	 7.5 7.5 18 ±20 18 to –20 7.5 18	V
Thermal Resistance, Junction–to–Air DM Suffix, Micro–8 Plastic Package, Case 846A D Suffix, SO–8 Plastic Package, Case 751	$R_{\theta JA}$	 240 178	°C/W
Operating Junction Temperature (Note 1)	T_J	–40 to +150	°C
Storage Temperature	T_{stg}	–55 to +150	°C

NOTE: 1. Tested ambient temperature range for the MC33348:
T_{low} = –25°C T_{high} = +85°C
2. ESD data available upon request.

ELECTRICAL CHARACTERISTICS (V_{CC} = 4.0 V, T_A = 25°C, for min/max values T_A is the operating junction temperature range that applies (Note 1), unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
VOLTAGE SENSING					
Cell Charging Cutoff (Pin 1 to Pin 3)					
Overvoltage Threshold, V_{Cell} Increasing	$V_{th(OV)}$				V
–1 Suffix		–	4.20	–	
–2 Suffix		–	4.20	–	
–3 Suffix		–	4.25	–	
–4 Suffix		–	4.25	–	
–5 Suffix		–	4.35	–	
–6 Suffix		–	4.35	–	
Overvoltage Hysteresis V_{Cell} Decreasing	V_H				mV
–1 Suffix		–	300	–	
–2 Suffix		–	300	–	
–3 Suffix		–	300	–	
–4 Suffix		–	300	–	
–5 Suffix		–	300	–	
–6 Suffix		–	300	–	
Cell Discharging Cutoff (Pin 1 to Pin 3, T_A = 25°C)					
Undervoltage Threshold, V_{Cell} Decreasing	$V_{th(UV)}$				V
–1 Suffix		–	2.25	–	
–2 Suffix		–	2.25	–	
–3 Suffix		–	2.28	–	
–4 Suffix		–	2.28	–	
–5 Suffix		–	2.30	–	
–6 Suffix		–	2.30	–	
Input Bias Current During Cell Voltage Sample (Pin 1)	I_{IIB}	–	28	–	µA
Cell Voltage Sampling Rate	$t_{(smpl)}$	–	1.0	–	s
CURRENT SENSING					
Discharge Current Limit (Pin 5 to Pin 3)					
Threshold Voltage	$V_{th(dschg)}$				mV
–1 Suffix		–	400	–	
–2 Suffix		–	200	–	
–3 Suffix		–	400	–	
–4 Suffix		–	200	–	
–5 Suffix		–	400	–	
–6 Suffix		–	200	–	
Delay	$I_{dly(dschg)}$	–	3.0	–	ms
CHARGE PUMP					
Output Voltage (Pin 8, $R_L \geq 10^{10}$ Ω)	V_O	–	10.2	–	V
TOTAL DEVICE					
Average Cell Current	I_{CC}				
Operating (V_{CC} = 4.0 V)		–	20	–	µA
Sleepmode (V_{CC} = 2.0 V)		–	1.4	–	nA
Minimum Operating Cell Voltage for Logic and Gate Drivers	V_{CC}	–	1.5	–	V

NOTE: 1. Tested ambient temperature range for the MC33348:
T_{low} = –25°C T_{high} = +85°C

Figure 1. Charge and Discharge Threshold Voltage Change versus Temperature

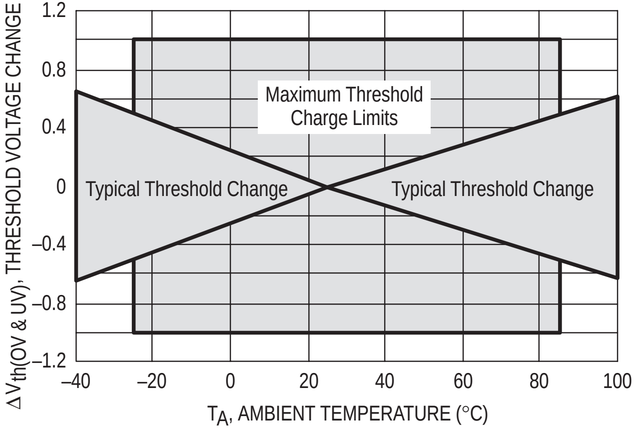


Figure 2. Discharge Current Limit Threshold Voltage Change versus Temperature

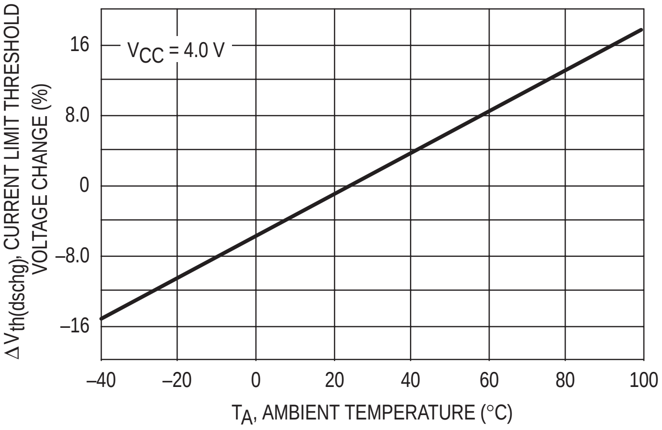


Figure 3. Gate Drive Output Voltage versus Load Current

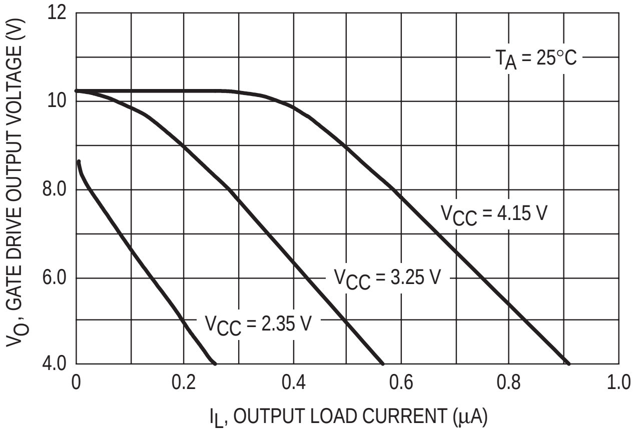


Figure 4. Gate Drive Output Voltage versus Supply Voltage

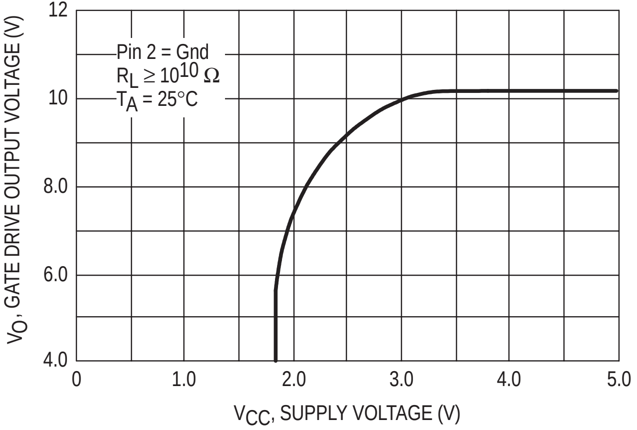


Figure 5. Charge Pump Output Voltage versus Temperature

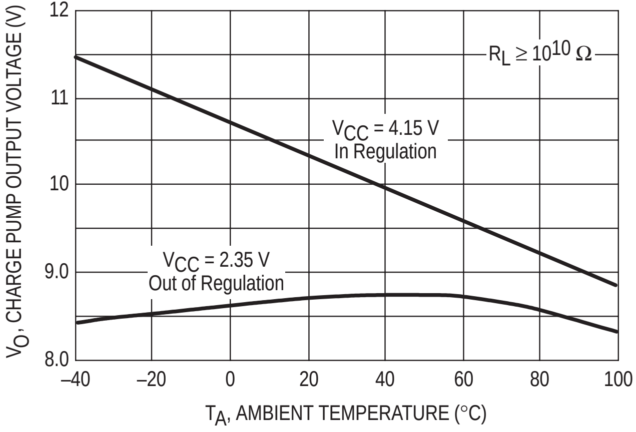
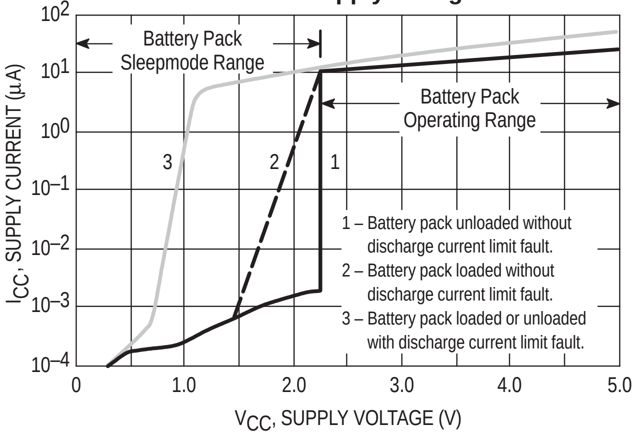


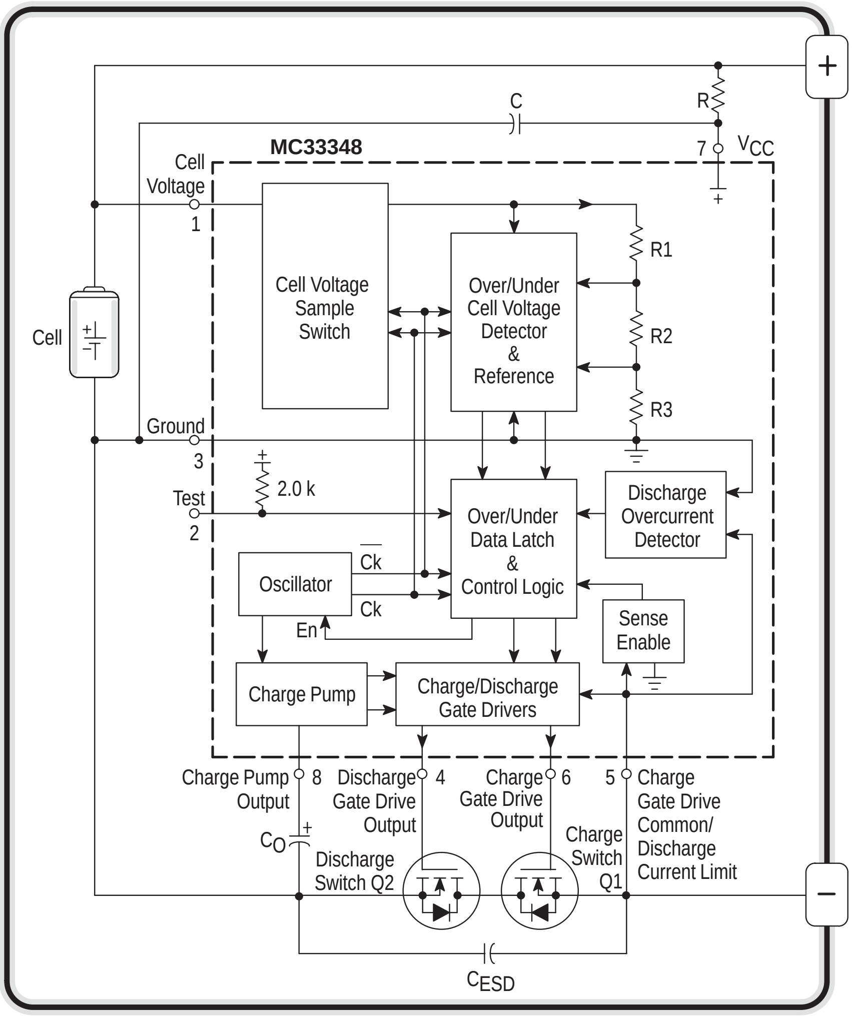
Figure 6. Supply Current versus Supply Voltage



PROTECTION CIRCUIT OPERATING MODE TABLE

Input Conditions Cell Status	Circuit Operation Battery Pack Status	Outputs		
		MOSFET Switches		Function
		Charge Q1	Discharge Q2	Charge Pump
CELL CHARGING/DISCHARGING				
Storage or Nominal Operation: No current or voltage faults	Both Charge MOSFET Q1 and Discharge MOSFET Q2 are on. The battery pack is available for charging or discharging.	On	On	Active
CELL CHARGING FAULT/RESET				
Charge Voltage Limit Fault: $V_{Pin\ 1} \geq V_{th(OV)}$ for 1.0 s	Charge MOSFET Q1 is latched off and the cell is disconnected from the charging source. An internal current source pull–up is applied to divider resistors R1 and R2 creating a hysteresis voltage of V_H. The battery pack is available for discharging. Discharge current limit protection is disabled.	On to Off	On	Active
Charge Voltage Limit Reset: $V_{Pin\ 1} < (V_{th(OV)} - V_H)$ for 1.0 s	Charge MOSFET Q1 will turn on when the voltage across the cell falls sufficiently to overcome hysteresis voltage V_H. This can be accomplished by applying a load to the battery pack. Discharge current limit protection is enabled.	Off to On	On	Active
CELL DISCHARGING FAULT/RESET				
Discharge Current Limit Fault: $V_{Pin\ 5} \geq (V_{Pin\ 1} + 400\ mV)$ for 3.0 ms and $V_{Pin\ 1} < (V_{th(OV)} - V_H)$ for 1.0 ms	Discharge MOSFET Q2 is latched off and the cell is disconnected from the load. Q2 will remain in the off state as long as $V_{Pin\ 5}$ exceeds $V_{Pin\ 3}$ by ≈ 2.0 V. The battery pack is available for charging.	On	On to Off	Active
Discharge Current Limit Reset: $V_{Pin\ 5} - V_{Pin\ 3} < 2.0\ V$	The Sense Enable circuit will reset and turn on discharge MOSFET Q2 when $V_{Pin\ 3}$ no longer exceeds $V_{Pin\ 5}$ by ≈ 2.0 V. This can be accomplished by either disconnecting the load from the battery pack, or by connecting the battery pack to the charger.	On	Off to On	Active
Discharge Voltage Limit Fault: $V_{Pin\ 1} \leq V_{th(UV)}$ for three consecutive 1.0 s samples	Discharge MOSFET Q2 is latched off, the cells are disconnected from the load, and the protection circuit enters a low current sleepmode state. The battery pack is available for charging.	On	On to Off	Disabled
Discharge Voltage Limit Reset: $V_{Pin\ 3} > (V_{Pin\ 5} + 0.6\ V)$	The Sense Enable circuit will reset and turn on discharge MOSFET Q2 when $V_{Pin\ 3}$ exceeds $V_{Pin\ 5}$ by 0.6 V. This can be accomplished by connecting the battery pack to the charger.	On	Off to On	Active
FAULTY CELL				
Discharge Voltage Limit Fault: $V_{Pin\ 1} \leq 1.5\ V$	This condition can happen if the cell is a defective (<1.5 V). The protection circuit logic will not function and the battery pack cannot be charged.	Disabled	Disabled	Disabled

Figure 7. One Cell Smart Battery Pack



PIN FUNCTION DESCRIPTION

Pin	Symbol	Description
1	Cell Voltage	This input is connected to the positive terminal of the cell for voltage monitoring. Internally, the Cell Voltage Sample Switch applies this voltage to a resistor divider where it is compared by the Cell Voltage Detector to an internal reference.
2	Test	This pin is normally not connected and is used in testing the protection IC. An active low at this input resets the internal logic and turns on both MOSFET switches. Upon release, the logic becomes active and the cell voltage is sampled within 1.0 ms.
3	Ground	This is the protection IC ground and all voltage ratings are with respect to this pin.
4	Discharge Gate Drive Output	This output connects to the gate of discharge switch Q2 allowing it to enable or disable battery pack discharging.
5	Charge Gate Drive Common/Discharge Current Limit	This is a multifunction pin that is used to monitor cell discharge current and to provide a gate turn–off path for charge switch Q1. A discharge current limit fault is set when the battery pack load causes the combined voltage drop of charge switch Q1 and discharge switch Q2 to exceed the discharge current limit threshold voltage, $V_{th(dschg)}$, with respect to Pin 3.
6	Charge Gate Drive Output	This output connects to the gate of charge switch Q1 allowing it to enable or disable battery pack charging.
7	V_{CC}	This pin is the positive supply voltage for the protection IC.
8	Charge Pump Output	This is the charge pump output. A reservoir capacitor is connected from this pin to ground.

INTRODUCTION

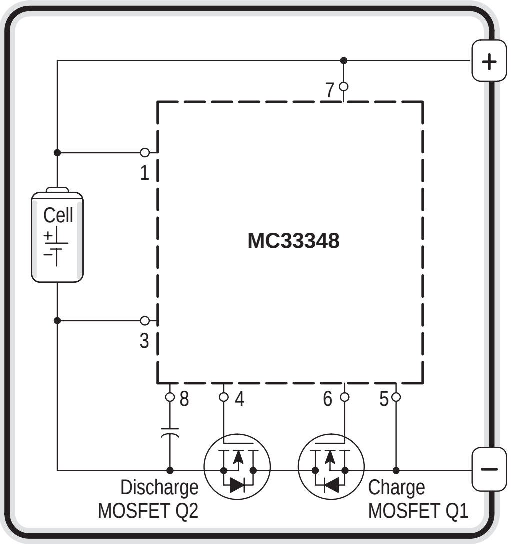
The insatiable demand for smaller lightweight portable electronic equipment has dramatically increased the requirements of battery performance. Batteries are expected to have higher energy densities, superior cycle life, be safe in operation and environmentally friendly. To address these high expectations, battery manufacturers have invested heavily in developing rechargeable lithium–based cells. Today's most attractive chemistries include lithium–polymer, lithium–ion, and lithium–metal. Each of these chemistries require electronic protection in order to constrain cell operation to within the manufacturers limits.

Rechargeable lithium–based cells require precise charge and discharge termination limits for both voltage and current in order to maximize cell capacity, cycle life, and to protect the end user from a catastrophic event. The termination limits are not as well defined as with older non–lithium chemistries. These limits are dependent upon a manufacturer's particular lithium chemistry, construction technique, and intended application. Battery pack assemblers may also choose to enhance cell capacity at the expense of cycle life. In order to address these requirements, six versions of the MC33348 protection circuit were developed. These devices feature charge overvoltage protection, discharge current limit protection with delayed shutdown, low operating current, a virtually zero current sleepmode state, and requires few external components to implement a complete one cell smart battery pack.

Operating Description

The MC33348 is specifically designed to be placed in the battery pack where it is continuously powered from a single lithium cell. In order to maintain cell operation within specified limits, the protection circuit senses both cell voltage and discharge current, and correspondingly controls the state of two N–channel MOSFET switches. These switches, Q1 and Q2, are placed in series with the negative terminal of the Cell and the negative terminal of the battery pack. This configuration allows the protection circuit to interrupt the appropriate charge or discharge path FET in the event that either a voltage threshold or the discharge current limit for the cell has been exceeded.

Figure 8. Simplified One Cell Smart Battery Pack



A functional description of the protection circuit blocks follows. Refer to the detailed block diagram shown in Figure 7.

Voltage Sensing

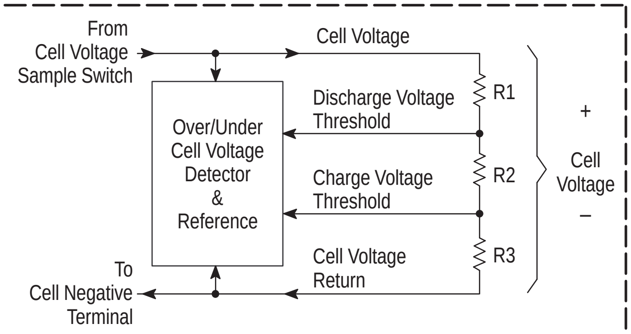
Voltage sensing is accomplished by the use of the Cell Voltage Sample Switch in conjunction with the Over/Under Voltage Detector and Reference block. The Sample Switch applies the cell voltage to the top resistor of an internal divider string. The voltage at each of the tap points is sequentially polled and compared to an internal reference. If a limit has been exceeded, the result is stored in the Over/Under Data Latch and Control Logic block. The Cell Voltage Sample Switch is gated on for a 1.0 ms period at a one second repetition rate. This low duty cycle sampling technique reduces the average load current that the divider presents across the cell, thus extending the useful battery pack capacity. The cell voltage limits are tested in the following sequence:

Figure 9. Cell Sensing Sequence

Polling Sequence	Time (ms)	Tested Limit
1	0.5	Overvoltage
2	0.5	Undervoltage

By incorporating this polling technique with a single comparator and voltage divider, a significant reduction of circuitry and trim elements is achieved. This results in a smaller die size, lower cost, and reduced operating current.

Figure 10. Cell Voltage Limit Sampling



The cell charge and discharge voltage limits are controlled by the values selected for the internal resistor divider string and the comparator input threshold. As the battery pack reaches full charge, the Cell Voltage Detector will sense an overvoltage fault condition when the cell exceeds the designed overvoltage limit. The fault information is stored in a data latch and charge MOSFET Q1 is turned off, disconnecting the battery pack from the charging source. An internal current source pull–up is then applied to lower tap of the divider, creating a hysteresis voltage. As a result of an overvoltage fault, the battery pack is available for discharging only.

The overvoltage fault is reset by applying a load to the battery pack. As the voltage across the cell falls below the hysteresis level, charge MOSFET Q1 will turn on. The battery pack will now be available for charging or discharging.

As the load eventually depletes the battery pack charge, the Cell Voltage Detector will sense an undervoltage fault condition when the cell falls below the designed undervoltage limit. After three consecutive faults are detected, discharge MOSFET Q2 is turned off, disconnecting the battery pack from the load. The protection circuit will now enter a low current sleepmode state drawing less than 10 nA, thus preventing any further cell discharging. As a result of the undervoltage fault, the battery pack is available for charging only. The typical cutoff thresholds and hysteresis voltage are shown in Figure 11.

Figure 11. Cutoff and Hysteresis Limits

Device Suffix	Charging Cutoff (V)	Hysteresis (mV)	Disharging Cutoff (V)
–1, –2	4.20	300	2.25
–3, –4	4.25	300	2.28
–5, –6	4.35	300	2.30

The undervoltage logic is designed to automatically reset if less than three consecutive faults appear. This helps to prevent a premature disconnection of the load during high current pulses when the battery pack charge is close to being depleted.

The undervoltage fault is reset by applying charge current to the battery pack. When the voltage on Pin 3 exceeds Pin 5 by 0.6 V, discharge MOSFET Q2 will turned on. The battery pack will now be available for charging or discharging.

Current Sensing

Discharge current limit protection is internally provided by the MC33348. As the battery pack discharges, Pins 8 and 5 sense the voltage drop across MOSFETs Q1 and Q2. A discharge current limit fault is detected if the voltage at Pin 5 is greater than Pin 3 by 400 mV for –1, –3 and –5 suffix devices, or 200 mV for –2, –4 and –6 suffix devices. The fault information is stored in a data latch and discharge MOSFET Q2 is turned off, disconnecting the battery pack from the load. As a result of the discharge current fault, the battery pack is available for charging only. The discharge current limit is given by:

$$I_{Lim(dschg)} = \frac{V_{th(dschg)}}{R_{Lim(dschg)}} = \frac{V_{th(dschg)}}{R_{DS(on)Q1} + R_{DS(on)Q2}}$$

The discharge current fault is reset by either disconnecting the load from the battery pack, or by connecting the battery pack to the charger. When the voltage on Pin 5 no longer exceeds Pin 3 by approximately 2.0 V, the Sense Enable circuit will turn on discharge MOSFET Q2.

Figure 12. Additional Current Limit Delay

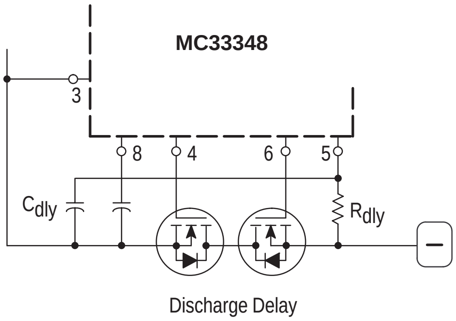
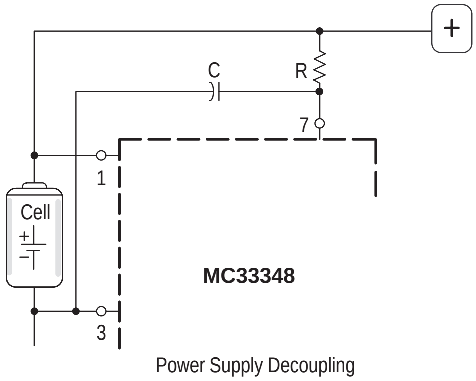


Figure 13. V_{CC} Decoupling



As previously stated in the voltage sensing operating description, charge MOSFET Q1 is held off during an overvoltage fault condition. When this condition is present, the discharge current limit protection function is internally disabled. This is required, since the voltage across Q1, in the off state, would exceed the current sense threshold. This would cause Q2 to turn off as well, preventing both charging and discharging of the cell. Discharge current limit protection is enabled whenever an overvoltage fault is not present.

The discharge current protection circuit contain a built in response delay of 3.0 ms. This helps to prevent fault activation when the battery pack is subjected to pulsed currents during discharging. An additional current sense delay can be added as shown in Figure 12. If the battery pack is subjected to extremely high discharge current pulses or is shorted, the V_{CC} pin must be decoupled from the cell. This is required so that the protection circuit will have sufficient operating voltage during the load transient, to ensure turn off of discharge MOSFET Q2. Figure 13 shows the placement of decoupling components.

Charge Pump and MOSFET Switches

The MC33348 contains an on chip Charge Pump to ensure that the MOSFET switches are fully enhanced for reduced power losses. An external reservoir capacitor normally connects from the Charge Pump output to ground, Pins 8 and 3. The capacitor value is not critical and is usually within the range of 10 nF to 100 nF. The Charge Pump output is regulated at 10.2 V allowing the use of economical logic level MOSFETs. The main requirement in selecting a particular type of MOSFET switch is to consider the desired on–resistance at the lowest anticipated operating voltage of the battery pack. A table of small outline surface mount devices is given in Figure 14. When using extremely low threshold MOSFETs, it may be desirable to disable the Charge Pump so that the maximum gate to source voltage is not exceeded. This is accomplished by connecting Pin 8 to Pin 7. Application Figure 7 show a capacitor labeled C_{ESD}. This capacitor provides a path around the MOSFET switches in the event of an electrostatic discharge.

Testing

A test pin is provided in order to speed up device and battery pack testing. By grounding Pin 2, the internal logic is held in a reset state and both MOSFET switches are turned on. Upon release, the logic becomes active and the cell voltage is polled within 1.0 ms.

Figure 14. Small Outline Surface Mount MOSFET Switches

Device Type	On–Resistance (Ω) versus Gate to Source Voltage (V)						
	2.5 V	3.0 V	4.0 V	5.0 V	6.0 V	7.5 V	9.0 V
MMFT3055VL	–	–	–	0.120 Ω	0.115 Ω	0.108 Ω	0.100 Ω
MMDF3N03HD	–	0.525 Ω	0.080 Ω	0.065 Ω	0.063 Ω	0.062 Ω	0.060 Ω
MMDF4N01HD	0.047 Ω	0.042 Ω	0.037 Ω	0.035 Ω	0.034 Ω	0.033 Ω	See Note
MMSF5N02HD	–	0.065 Ω	0.023 Ω	0.021 Ω	0.020 Ω	0.018 Ω	0.018 Ω
MMDF6N02HD	0.043 Ω	0.035 Ω	0.029 Ω	0.028 Ω	0.026 Ω	0.025 Ω	0.023 Ω

NOTE: Exceeds maximum V_{GS} voltage rating.

MC33362

Advance Information

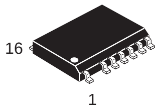
High Voltage Switching Regulator

HIGH VOLTAGE OFF–LINE SWITCHING REGULATOR

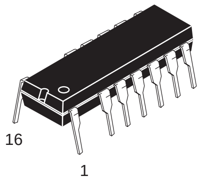
SEMICONDUCTOR TECHNICAL DATA

The MC33362 is a monolithic high voltage switching regulator that is specifically designed to operate from a rectified 120 VAC line source. This integrated circuit features an on–chip 500 V/2.0 A SenseFET power switch, 250 V active off–line startup FET, duty cycle controlled oscillator, current limiting comparator with a programmable threshold and leading edge blanking, latching pulse width modulator for double pulse suppression, high gain error amplifier, and a trimmed internal bandgap reference. Protective features include cycle–by–cycle current limiting, input undervoltage lockout with hysteresis, output overvoltage protection, and thermal shutdown. This device is available in a 16–lead dual–in–line and wide body surface mount packages.

- On–Chip 500 V, 2.0 A SenseFET Power Switch
- Rectified 120 VAC Line Source Operation
- On–Chip 250 V Active Off–Line Startup FET
- Latching PWM for Double Pulse Suppression
- Cycle–By–Cycle Current Limiting
- Input Undervoltage Lockout with Hysteresis
- Output Overvoltage Protection Comparator
- Trimmed Internal Bandgap Reference
- Internal Thermal Shutdown

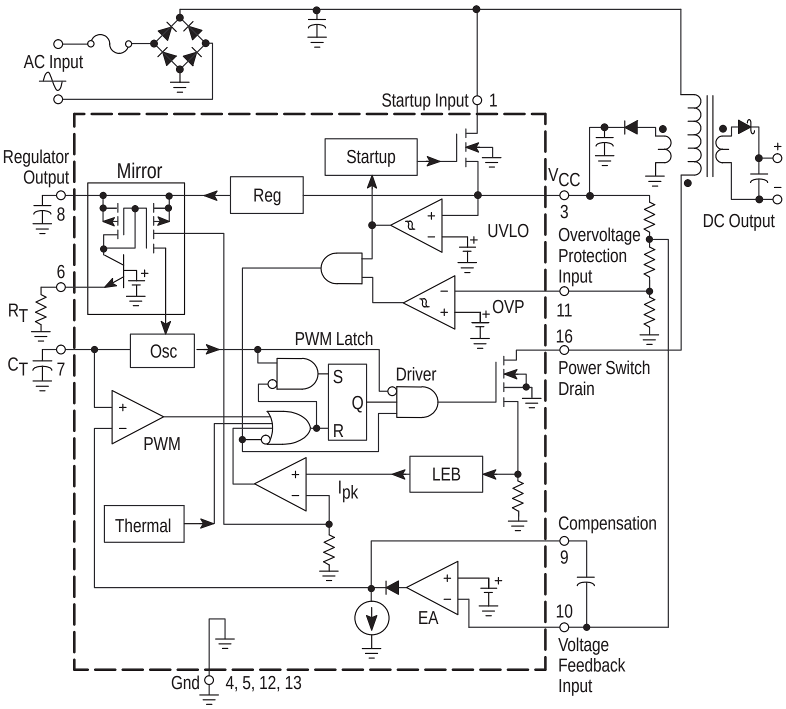


DW SUFFIX
PLASTIC PACKAGE
CASE 751N
(SOP–16L)



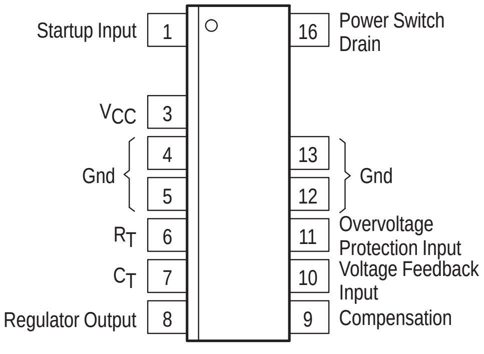
P SUFFIX
PLASTIC PACKAGE
CASE 648E
(DIP–16)

Simplified Application



This device contains 221 active transistors.

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC33362DW	T_J = –25° to +125°C	SOP–16L
MC33362P		DIP–16

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Switch (Pin 16)			
Drain Voltage	V_{DS}	500	V
Drain Current	I_{DS}	2.0	A
Startup Input Voltage (Pin 1, Note 1)	V_{in}		V
Pin 3 = Gnd		250	
Pin 3 ≤ 1000 µF to ground		400	
Power Supply Voltage (Pin 3)	V_{CC}	40	V
Input Voltage Range Voltage Feedback Input (Pin 10) Compensation (Pin 9) Overvoltage Protection Input (Pin 11) R_T (Pin 6) C_T (Pin 7)	V_{IR}	–1.0 to V_{reg}	V
Thermal Characteristics			°C/W
P Suffix, Dual–In–Line Case 648E			
Thermal Resistance, Junction–to–Air	$R_{\theta JA}$	80	
Thermal Resistance, Junction–to–Case (Pins 4, 5, 12, 13)	$R_{\theta JC}$	15	
DW Suffix, Surface Mount Case 751N			
Thermal Resistance, Junction–to–Air	$R_{\theta JA}$	95	
Thermal Resistance, Junction–to–Case (Pins 4, 5, 12, 13)	$R_{\theta JC}$	15	
Refer to Figures 15 and 16 for additional thermal information.			
Operating Junction Temperature	T_J	– 25 to +150	°C
Storage Temperature	T_{stg}	– 55 to +150	°C

NOTE: ESD data available upon request.

ELECTRICAL CHARACTERISTICS (V_{CC} = 20 V, R_T = 10 k, C_T = 390 pF, $C_{Pin\ 8}$ = 1.0 µF, for typical values T_J = 25°C, for min/max values T_J is the operating junction temperature range that applies (Note 2), unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
REGULATOR (Pin 8)					
Output Voltage (I_O = 0 mA, T_J = 25°C)	V_{reg}	5.5	6.5	7.5	V
Line Regulation (V_{CC} = 20 V to 40 V)	Reg_{line}	–	30	500	mV
Load Regulation (I_O = 0 mA to 10 mA)	Reg_{load}	–	44	200	mV
Total Output Variation over Line, Load, and Temperature	V_{reg}	5.3	–	8.0	V
OSCILLATOR (Pin 7)					
Frequency	f_{OSC}				kHz
C_T = 390 pF					
T_J = 25°C (V_{CC} = 20 V)		260	285	310	
T_J = T_{low} to T_{high} (V_{CC} = 20 V to 40 V)		255	–	315	
C_T = 2.0 nF					
T_J = 25°C (V_{CC} = 20 V)		60	67.5	75	
T_J = T_{low} to T_{high} (V_{CC} = 20 V to 40 V)		59	–	76	
Frequency Change with Voltage (V_{CC} = 20 V to 40 V)	$\Delta f_{OSC}/\Delta V$	–	0.1	2.0	kHz
ERROR AMPLIFIER (Pins 9, 10)					
Voltage Feedback Input Threshold	V_{FB}	2.52	2.6	2.68	V
Line Regulation (V_{CC} = 20 V to 40 V, T_J = 25°C)	Reg_{line}	–	0.6	5.0	mV
Input Bias Current (V_{FB} = 2.6 V)	I_{IB}	–	20	500	nA
Open Loop Voltage Gain (T_J= 25°C)	A_{VOL}	–	82	–	dB
Gain Bandwidth Product (f = 100 kHz, T_J= 25°C)	GBW	–	1.0	–	MHz

NOTES: 1. Maximum power dissipation limits must be observed.
2. Tested junction temperature range for the MC33362:
T_{low} = –25°C T_{high} = +125°C

ELECTRICAL CHARACTERISTICS (continued) (V_{CC} = 20 V, R_T = 10 k, C_T = 390 pF, $C_{Pin\ 8}$ = 1.0 µF, for typical values T_J = 25°C, for min/max values T_J is the operating junction temperature range that applies (Note 2), unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
ERROR AMPLIFIER (Pins 9, 10)					
Output Voltage Swing High State (I_{Source} = 100 µA, V_{FB} < 2.0 V) Low State (I_{Sink} = 100 µA, V_{FB} > 3.0 V)	 V_{OH} V_{OL}	 4.0 –	 5.3 0.2	 – 0.35	V
OVERVOLTAGE DETECTION (Pin 11)					
Input Threshold Voltage	V_{th}	2.47	2.6	2.73	V
Input Bias Current (V_{in} = 2.6 V)	I_{IB}	–	100	500	nA
PWM COMPARATOR (Pins 7, 9)					
Duty Cycle Maximum (V_{FB} = 0 V) Minimum (V_{FB} = 2.7 V)	 $DC_{(max)}$ $DC_{(min)}$	 48 –	 50 0	 52 0	%
POWER SWITCH (Pin 16)					
Drain–Source On–State Resistance (I_D = 200 mA) T_J = 25°C T_J = T_{low} to T_{high}	$R_{DS(on)}$	 – –	 4.4 –	 6.0 12	Ω
Drain–Source Off–State Leakage Current (V_{DS} = 500 V)	$I_{D(off)}$	–	0.2	50	µA
Rise Time	t_r	–	50	–	ns
Fall Time	t_f	–	50	–	ns
OVERCURRENT COMPARATOR (Pin 16)					
Current Limit Threshold (R_T = 10 k)	I_{lim}	0.7	0.9	1.1	A
STARTUP CONTROL (Pin 1)					
Peak Startup Current (V_{in} = 200 V) V_{CC} = 0 V V_{CC} = ($V_{th(on)}$ – 0.2 V)	I_{start}	 – –	 55 26	 – –	mA
Off–State Leakage Current (V_{in} = 50 V, V_{CC} = 20 V)	$I_{D(off)}$	–	40	200	µA
UNDERVOLTAGE LOCKOUT (Pin 3)					
Startup Threshold (V_{CC} Increasing)	$V_{th(on)}$	11	14.5	18	V
Minimum Operating Voltage After Turn–On	$V_{CC(min)}$	7.5	9.5	11.5	V
TOTAL DEVICE (Pin 3)					
Power Supply Current Startup (V_{CC} = 10 V, Pin 1 Open) Operating	I_{CC}	 – –	 0.3 3.6	 0.5 5.0	mA

Figure 1. Oscillator Frequency versus Timing Resistor

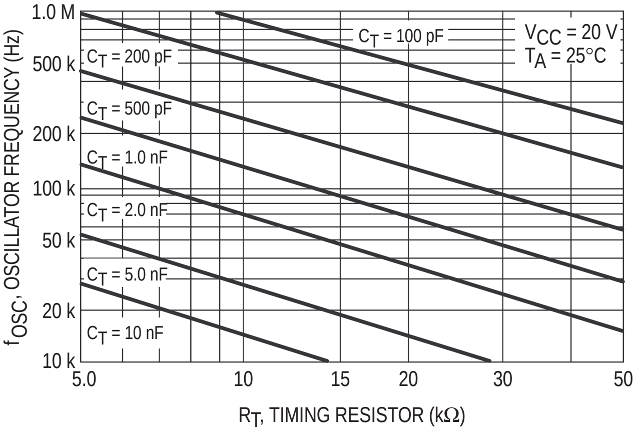


Figure 2. Power Switch Peak Drain Current versus Timing Resistor

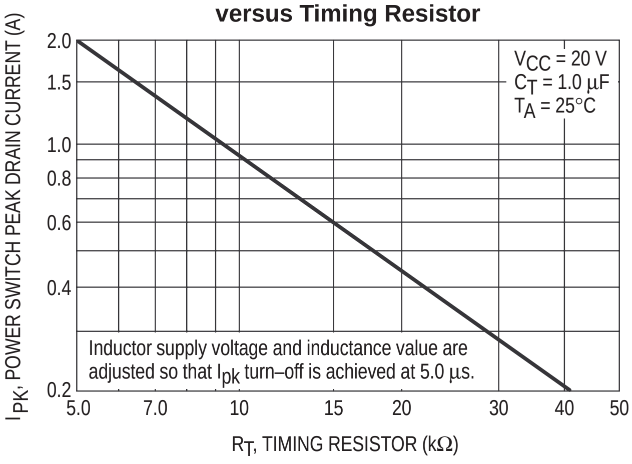


Figure 3. Oscillator Charge/Discharge Current versus Timing Resistor

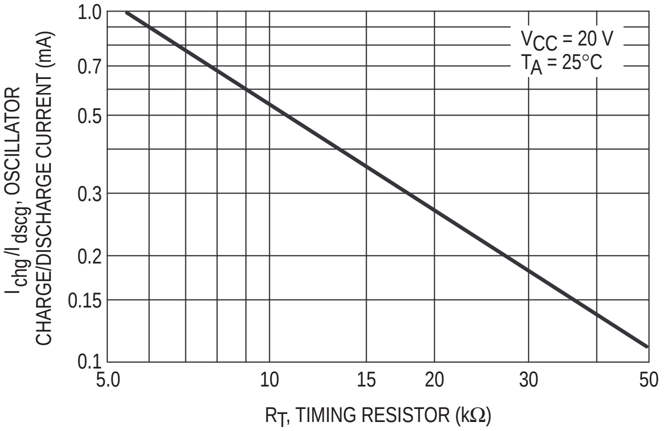


Figure 4. Maximum Output Duty Cycle versus Timing Resistor Ratio

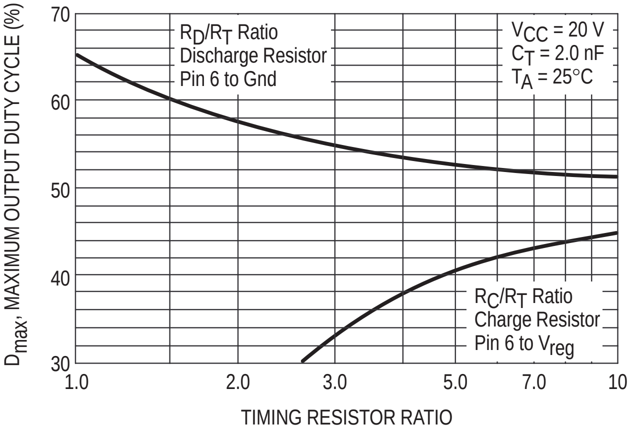


Figure 5. Error Amp Open Loop Gain and Phase versus Frequency

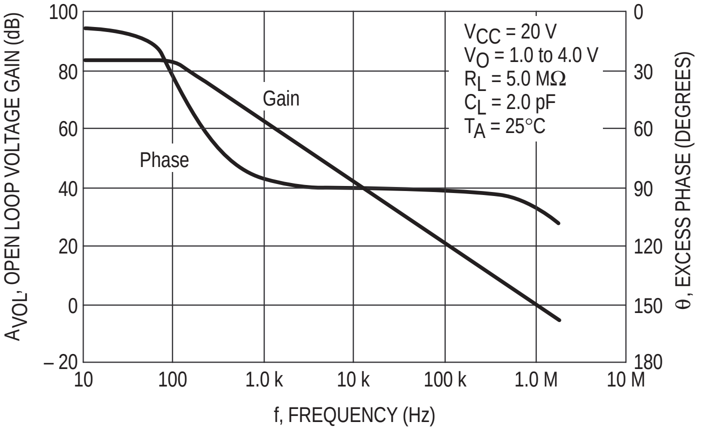


Figure 6. Error Amp Output Saturation Voltage versus Load Current

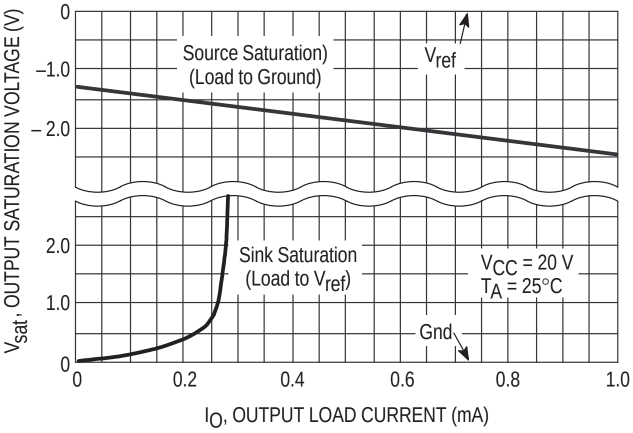


Figure 7. Error Amplifier Small Signal Transient Response

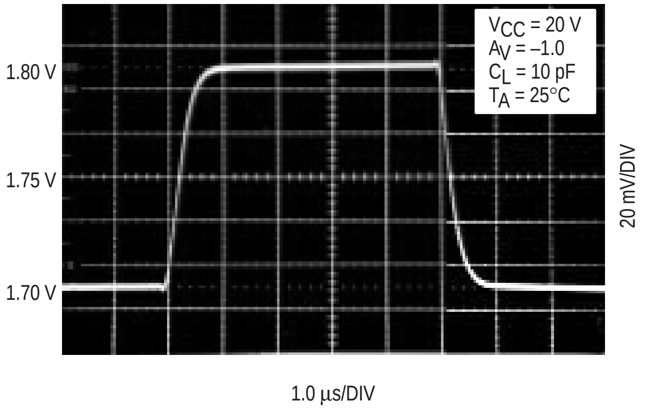


Figure 8. Error Amplifier Large Signal Transient Response

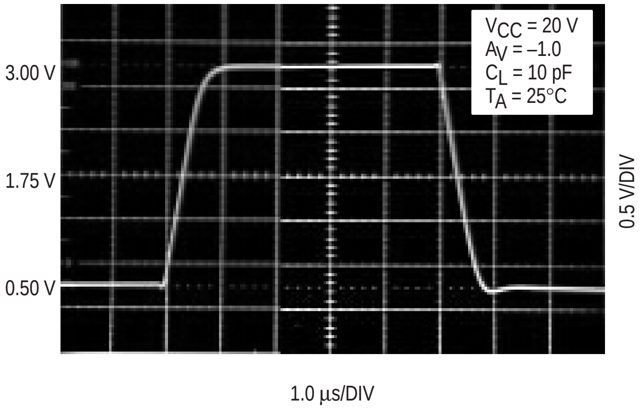


Figure 9. Regulator Output Voltage Change versus Source Current

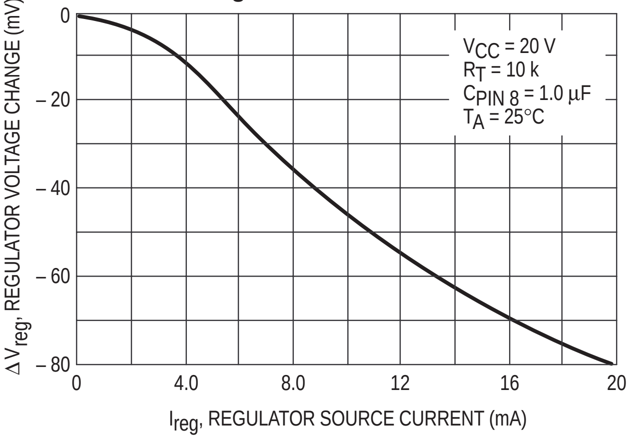


Figure 10. Peak Startup Current versus Power Supply Voltage

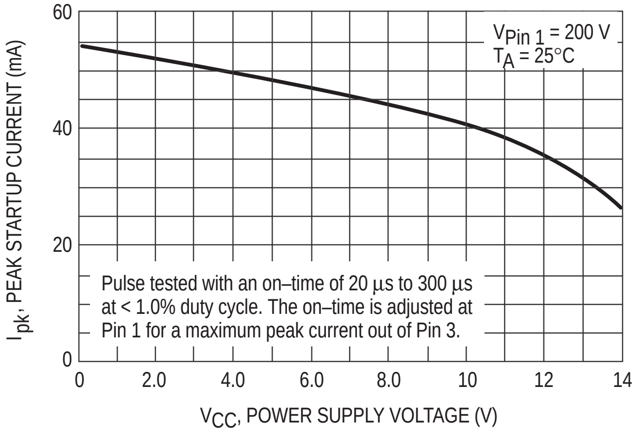


Figure 11. Power Switch Drain–Source On–Resistance versus Temperature

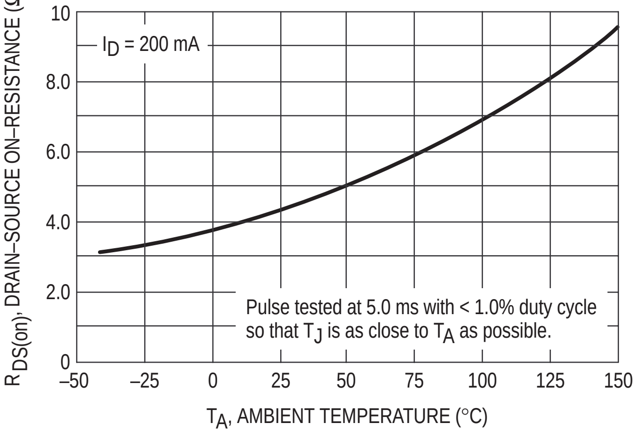


Figure 12. Power Switch Drain–Source Capacitance versus Voltage

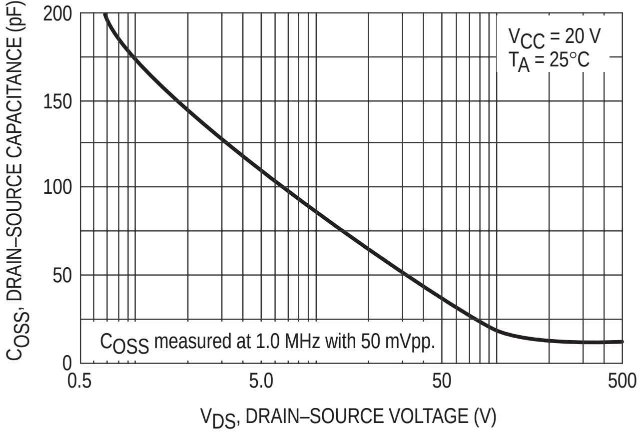


Figure 13. Supply Current versus Supply Voltage

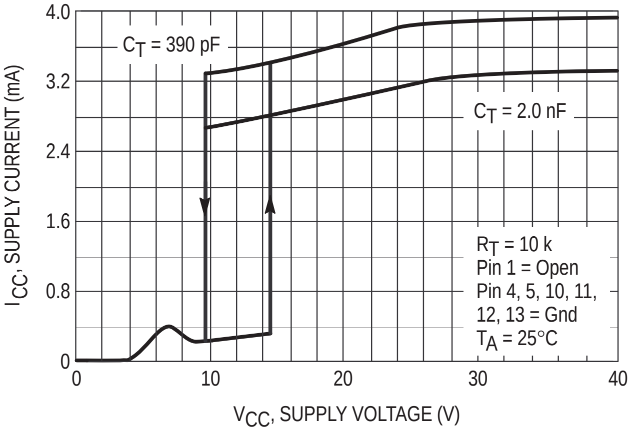


Figure 14. DW and P Suffix Transient Thermal Resistance

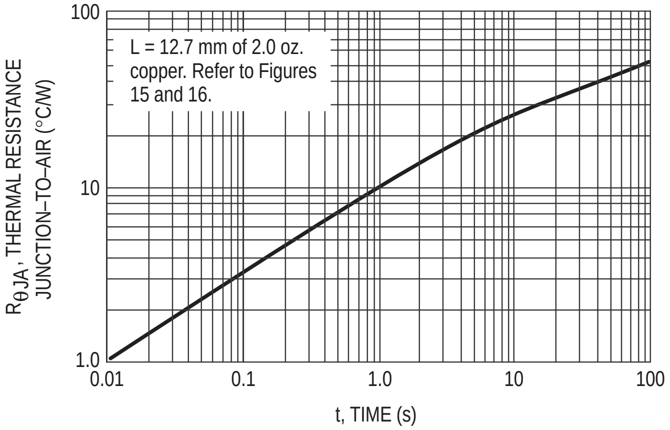


Figure 15. DW Suffix (SOP–16L) Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length

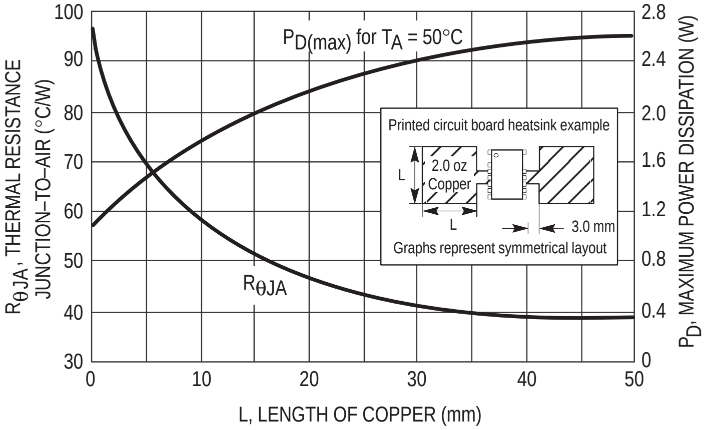
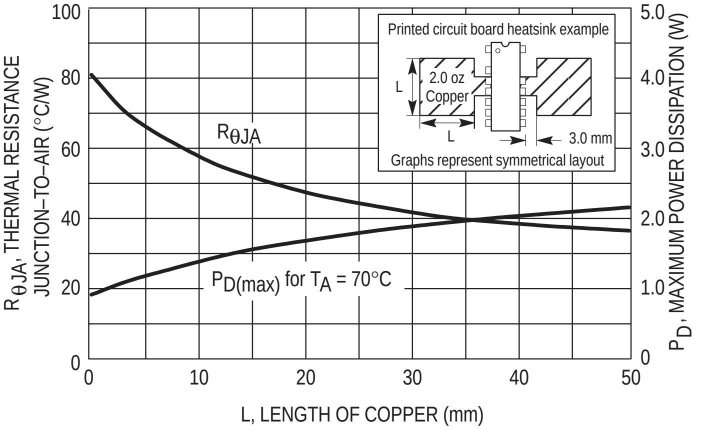


Figure 16. P Suffix (DIP–16) Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length



PIN FUNCTION DESCRIPTION

Pin	Function	Description
1	Startup Input	This pin connects directly to the rectified ac line voltage source. Internally Pin 1 is tied to the drain of a high voltage startup MOSFET. During startup, the MOSFET supplies internal bias, and charges an external capacitor that connects from the V_{CC} pin to ground.
2	–	This pin has been omitted for increased spacing between the rectified AC line voltage on Pin 1 and the V_{CC} potential on Pin 3.
3	V_{CC}	This is the positive supply voltage input. During startup, power is supplied to this input from Pin 1. When V_{CC} reaches the UVLO upper threshold, the startup MOSFET turns off and power is supplied from an auxiliary transformer winding.
4, 5, 12, 13	Ground	These pins are the control circuit grounds. They are part of the IC lead frame and provide a thermal path from the die to the printed circuit board.
6	R_T	Resistor R_T connects from this pin to ground. The value selected will program the Current Limit Comparator threshold and affect the Oscillator frequency.
7	C_T	Capacitor C_T connects from this pin to ground. The value selected, in conjunction with resistor R_T, programs the Oscillator frequency.
8	Regulator Output	This 6.5 V output is available for biasing external circuitry. It requires an external bypass capacitor of at least 1.0 µF for stability.
9	Compensation	This pin is the Error Amplifier output and is made available for loop compensation. It can be used as an input to directly control the PWM Comparator.
10	Voltage Feedback Input	This is the inverting input of the Error Amplifier. It has a 2.6 V threshold and normally connects through a resistor divider to the converter output, or to a voltage that represents the converter output.
11	Overvoltage Protection Input	This input provides runaway output voltage protection due to an external component or connection failure in the control loop feedback signal path. It has a 2.6 V threshold and normally connects through a resistor divider to the converter output, or to a voltage that represents the converter output.
14, 15	–	These pins have been omitted for increased spacing between the high voltages present on the Power Switch Drain, and the ground potential on Pins 12 and 13.
16	Power Switch Drain	This pin is designed to directly drive the converter transformer and is capable of switching a maximum of 500 V and 2.0 A.

Figure 17. Representative Block Diagram

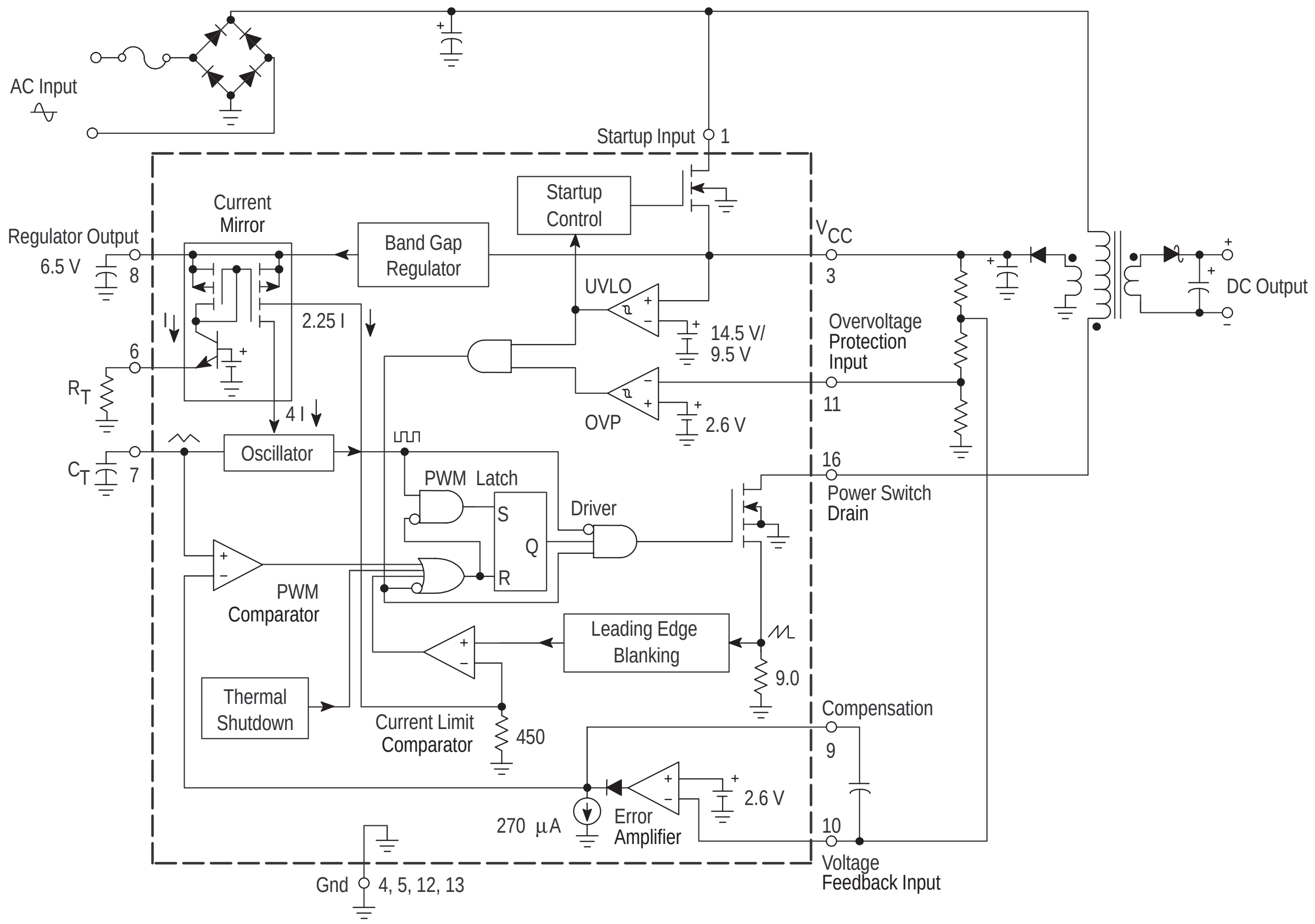
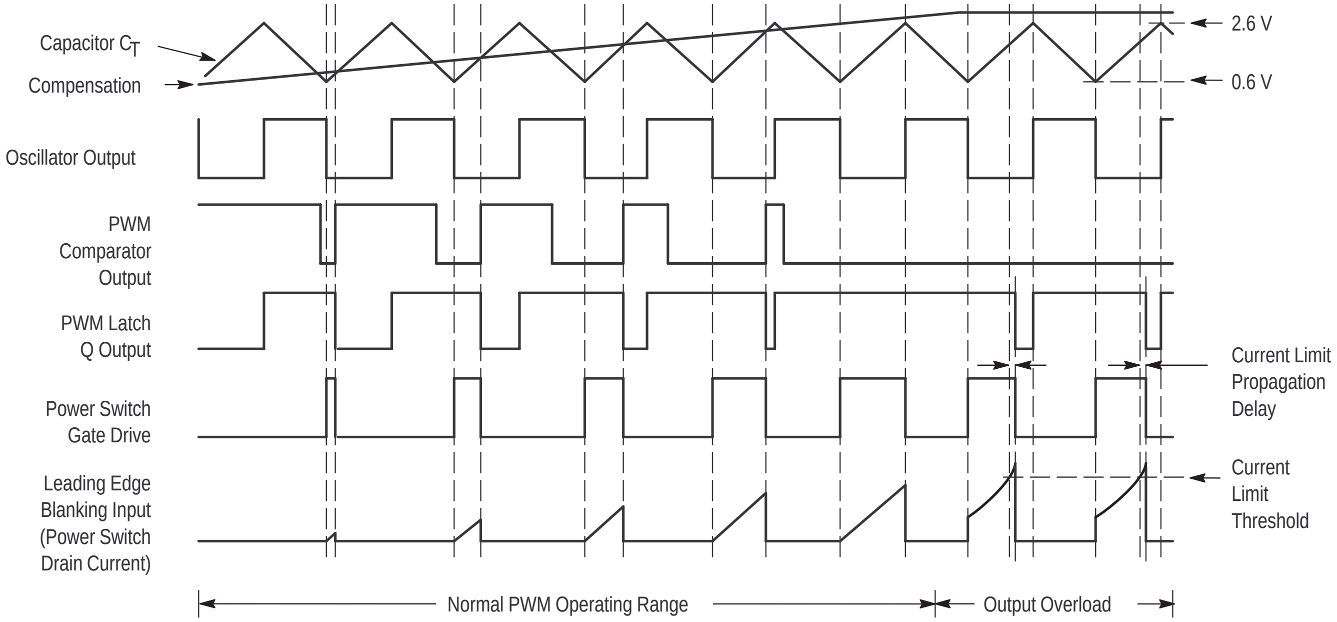


Figure 18. Timing Diagram



OPERATING DESCRIPTION

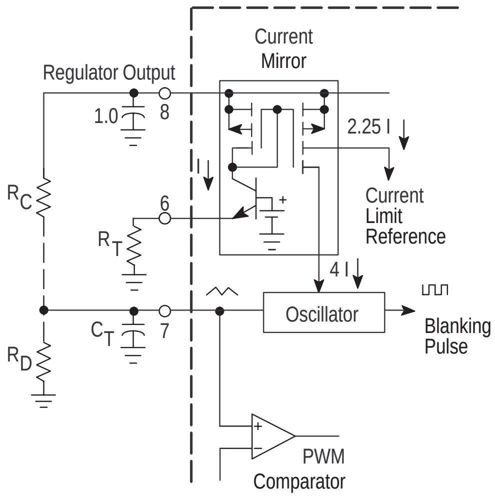
Introduction

The MC33362 represents a new higher level of integration by providing all the active high voltage power, control, and protection circuitry required for implementation of a flyback or forward converter on a single monolithic chip. This device is designed for direct operation from a rectified 120 VAC line source and requires a minimum number of external components to implement a complete converter. A description of each of the functional blocks is given below, and the representative block and timing diagrams are shown in Figures 17 and 18.

Oscillator and Current Mirror

The oscillator frequency is controlled by the values selected for the timing components R_T and C_T. Resistor R_T programs the oscillator charge/discharge current via the Current Mirror 4 I output, Figure 3. Capacitor C_T is charged and discharged by an equal magnitude internal current source and sink. This generates a symmetrical 50 percent duty cycle waveform at Pin 7, with a peak and valley threshold of 2.6 V and 0.6 V respectively. During the discharge of C_T, the oscillator generates an internal blanking pulse that holds the inverting input of the AND gate Driver high. This causes the Power Switch gate drive to be held in a low state, thus producing a well controlled amount of output deadtime. The amount of deadtime is relatively constant with respect to the oscillator frequency when operating below 1.0 MHz. The maximum Power Switch duty cycle at Pin 16 can be modified from the internal 50% limit by providing an additional charge or discharge current path to C_T, Figure 19. In order to increase the maximum duty cycle, a discharge current resistor R_D is connected from Pin 7 to ground. To decrease the maximum duty cycle, a charge current resistor R_C is connected from Pin 7 to the Regulator Output. Figure 4 shows an obtainable range of maximum output duty cycle versus the ratio of either R_C or R_D with respect to R_T.

Figure 19. Maximum Duty Cycle Modification



The formula for the charge/discharge current along with the oscillator frequency are given below. The frequency formula is a first order approximation and is accurate for C_T values greater than 500 pF. For smaller values of C_T, refer to Figure 1. Note that resistor R_T also programs the Current Limit Comparator threshold.

$$I_{chg/dscg} = \frac{5.4}{R_T} \qquad f \approx \frac{I_{chg/dscg}}{4C_T}$$

PWM Comparator and Latch

The pulse width modulator consists of a comparator with the oscillator ramp voltage applied to the non–inverting input, while the error amplifier output is applied into the inverting input. The Oscillator applies a set pulse to the PWM Latch while C_T is discharging, and upon reaching the valley voltage, Power Switch conduction is initiated. When C_T charges to a voltage that exceeds the error amplifier output, the PWM Latch is reset, thus terminating Power Switch conduction for the duration of the oscillator ramp–up period. This PWM Comparator/Latch combination prevents multiple output pulses during a given oscillator clock cycle. The timing diagram shown in Figure 18 illustrates the Power Switch duty cycle behavior versus the Compensation voltage.

Current Limit Comparator and Power Switch

The MC33362 uses cycle–by–cycle current limiting as a means of protecting the output switch transistor from overstress. Each on–cycle is treated as a separate situation. Current limiting is implemented by monitoring the output switch current buildup during conduction, and upon sensing an overcurrent condition, immediately turning off the switch for the duration of the oscillator ramp–up period.

The Power Switch is constructed as a SenseFET allowing a virtually lossless method of monitoring the drain current. It consists of a total of 3770 cells, of which 50 are connected to a 9.0 Ω ground–referenced sense resistor. The Current Sense Comparator detects if the voltage across the sense resistor exceeds the reference level that is present at the inverting input. If exceeded, the comparator quickly resets the PWM Latch, thus protecting the Power Switch. The current limit reference level is generated by the 2.25 I output of the Current Mirror. This current causes a reference voltage to appear across the 450 Ω resistor. This voltage level, as well as the Oscillator charge/discharge current are both set by resistor R_T. Therefore when selecting the values for R_T and C_T, R_T must be chosen first to set the Power Switch peak drain current, while C_T is chosen second to set the desired Oscillator frequency. A graph of the Power Switch peak drain current versus R_T is shown in Figure 2 with the related formula below.

$$I_{pk} = 12.3\left(\frac{R_T}{1000}\right)^{-1.115}$$

The Power Switch is designed to directly drive the converter transformer and is capable of switching a maximum of 500 V and 2.0 A. Proper device voltage snubbing and heatsinking are required for reliable operation.

A Leading Edge Blanking circuit was placed in the current sensing signal path. This circuit prevents a premature reset of the PWM Latch. The premature reset is generated each time the Power Switch is driven into conduction. It appears as a narrow voltage spike across the current sense resistor, and is due to the MOSFET gate to source capacitance, transformer interwinding capacitance, and output rectifier recovery time. The Leading Edge Blanking circuit has a dynamic behavior in that it masks the current signal until the Power Switch turn–on transition is completed. The current limit propagation delay time is typically 233 ns. This time is measured from when an overcurrent appears at the Power Switch drain, to the beginning of turn–off.

Error Amplifier

An fully compensated Error Amplifier with access to the inverting input and output is provided for primary side voltage sensing, Figure 17. It features a typical dc voltage gain of 82 dB, and a unity gain bandwidth of 1.0 MHz with 78 degrees of phase margin, Figure 5. The noninverting input is internally biased at 2.6 V ±3.1% and is not pinned out. The Error Amplifier output is pinned out for external loop compensation and as a means for directly driving the PWM Comparator. The output was designed with a limited sink current capability of 270 µA, allowing it to be easily overridden with a pull–up resistor. This is desirable in applications that require secondary side voltage sensing, Figure 20. In this application, the Voltage Feedback Input is connected to the Regulator Output. This disables the Error Amplifier by placing its output into the sink state, allowing the optocoupler transistor to directly control the PWM Comparator.

Overvoltage Protection

An Overvoltage Protection Comparator is included to eliminate the possibility of runaway output voltage. This condition can occur if the control loop feedback signal path is broken due to an external component or connection failure. The comparator is normally used to monitor the primary side V_{CC} voltage. When the 2.6 V threshold is exceeded, it will immediately turn off the Power Switch, and protect the load from a severe overvoltage condition. This input can also be driven from external circuitry to inhibit converter operation.

Undervoltage Lockout

An Undervoltage Lockout comparator has been incorporated to guarantee that the integrated circuit has sufficient voltage to be fully functional before the output stage is enabled. The UVLO comparator monitors the V_{CC} voltage at Pin 3 and when it exceeds 14.5 V, the reset signal is removed from the PWM Latch allowing operation of the Power Switch. To prevent erratic switching as the threshold is crossed, 5.0 V of hysteresis is provided.

Startup Control

An internal Startup Control circuit with a high voltage enhancement mode MOSFET is included within the MC33362. This circuitry allows for increased converter efficiency by eliminating the external startup resistor, and its associated power dissipation, commonly used in most off–line converters that utilize a UC3842 type of controller. Rectified ac line voltage is applied to the Startup Input, Pin 1. This causes the MOSFET to enhance and supply internal bias as well as charge current to the V_{CC} bypass capacitor that connects from Pin 3 to ground. When V_{CC} reaches the UVLO upper threshold of 14.5 V, the IC commences operation and the startup MOSFET is turned off. Operating bias is now derived from the auxiliary transformer winding, and all of the device power is efficiently converted down from the rectified ac line.

The startup MOSFET will provide an initial peak current of 55 mA, Figure 10, which decreases rapidly as V_{CC} and the die temperature rise. The steady state current will self limit in the range of 12 mA with V_{CC} shorted to ground. The startup MOSFET is rated at a maximum of 250 V with V_{CC} shorted to ground, and 400 V when charging a V_{CC} capacitor of 1000 µF or less.

Regulator

A low current 6.5 V regulated output is available for biasing the Error Amplifier and any additional control system circuitry. It is capable of up to 10 mA and has short–circuit protection. This output requires an external bypass capacitor of at least 1.0 µF for stability.

Thermal Shutdown and Package

Internal thermal circuitry is provided to protect the Power Switch in the event that the maximum junction temperature is exceeded. When activated, typically at 155°C, the Latch is forced into a ‘reset’ state, disabling the Power Switch. The Latch is allowed to ‘set’ when the Power Switch temperature falls below 145°C. This feature is provided to prevent catastrophic failures from accidental device overheating. It is not intended to be used as a substitute for proper heatsinking.

The MC33362 is contained in a heatsinkable plastic dual–in–line package in which the die is mounted on a special heat tab copper alloy lead frame. This tab consists of the four center ground pins that are specifically designed to improve thermal conduction from the die to the circuit board. Figures 15 and 16 show a simple and effective method of utilizing the printed circuit board medium as a heat dissipater by soldering these pins to an adequate area of copper foil. This permits the use of standard layout and mounting practices while having the ability to halve the junction to air thermal resistance. The examples are for a symmetrical layout on a single–sided board with two ounce per square foot of copper. Figure 22 shows a practical example of a printed circuit board layout that utilizes the copper foil as a heat dissipater. Note that a jumper was added to the layout from Pins 8 to 10 in order to enhance the copper area near the device for improved thermal conductivity. The application circuit requires two ounce copper foil in order to obtain 20 watts of continuous output power at room temperature.

Figure 20. 20 W Off–Line Converter

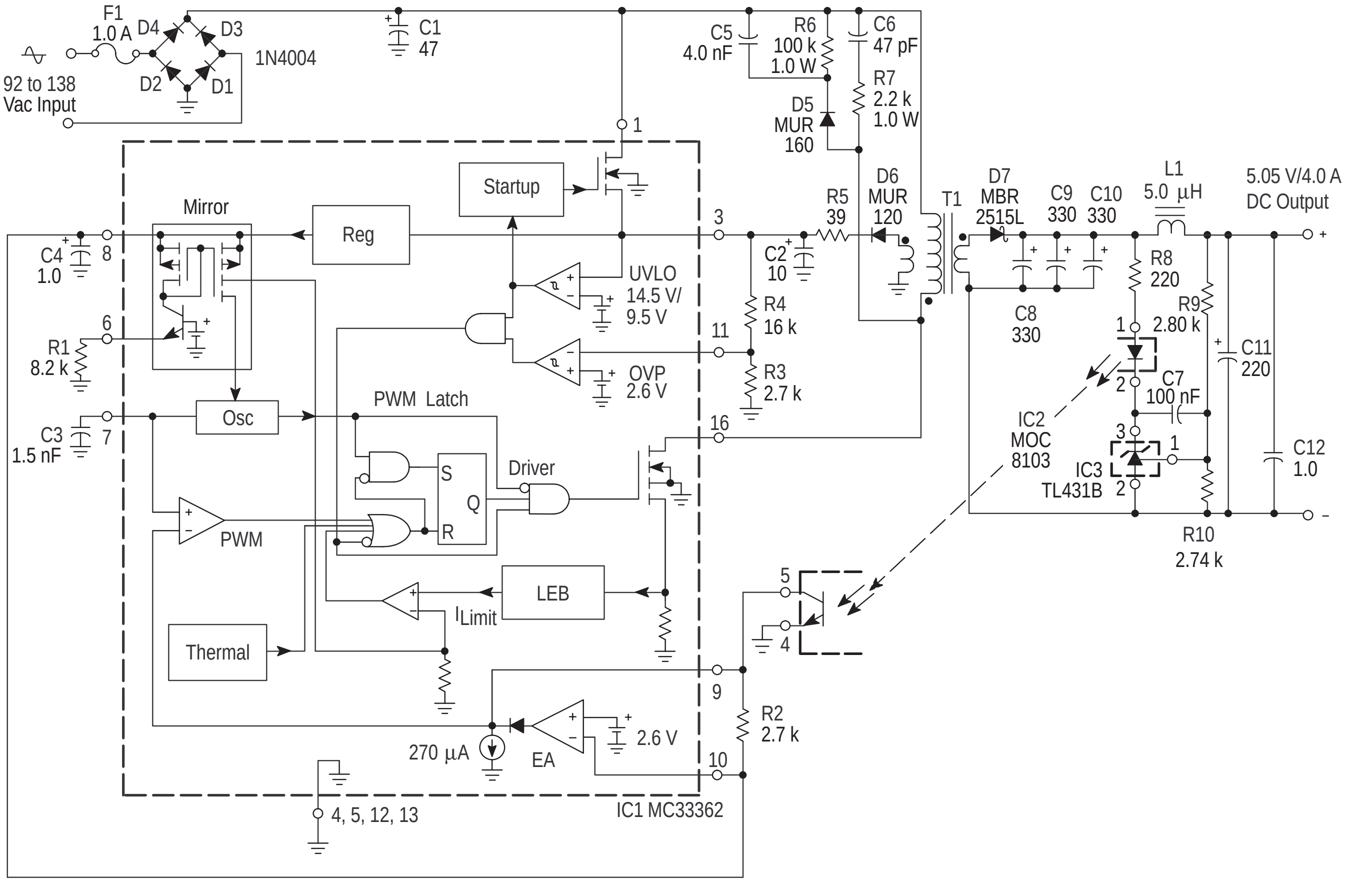


Figure 21. Converter Test Data

Test	Conditions	Results
Line Regulation	V_{in} = 92 Vac to 138 Vac, I_O 4.0 A	Δ = 1.0 mV
Load Regulation	V_{in} = 115 Vac, I_O = 1.0 A to 4.0 A	Δ = 9.0 mV
Output Ripple	V_{in} = 115 Vac, I_O = 4.0 A	Triangular = 10 mVpp Spike = 60 mVpp
Efficiency	V_{in} = 115 Vac, I_O = 4.0 A	78.4%

This data was taken with the components listed below mounted on the printed circuit board shown in Figure 22.

For high efficiency and small circuit board size, the Sanyo Os–Con capacitors are recommended for C8, C9, C10 and C11.

C8, C9, C10 = Sanyo Os–Con #6SA330M, 330 μF 6.3 V.

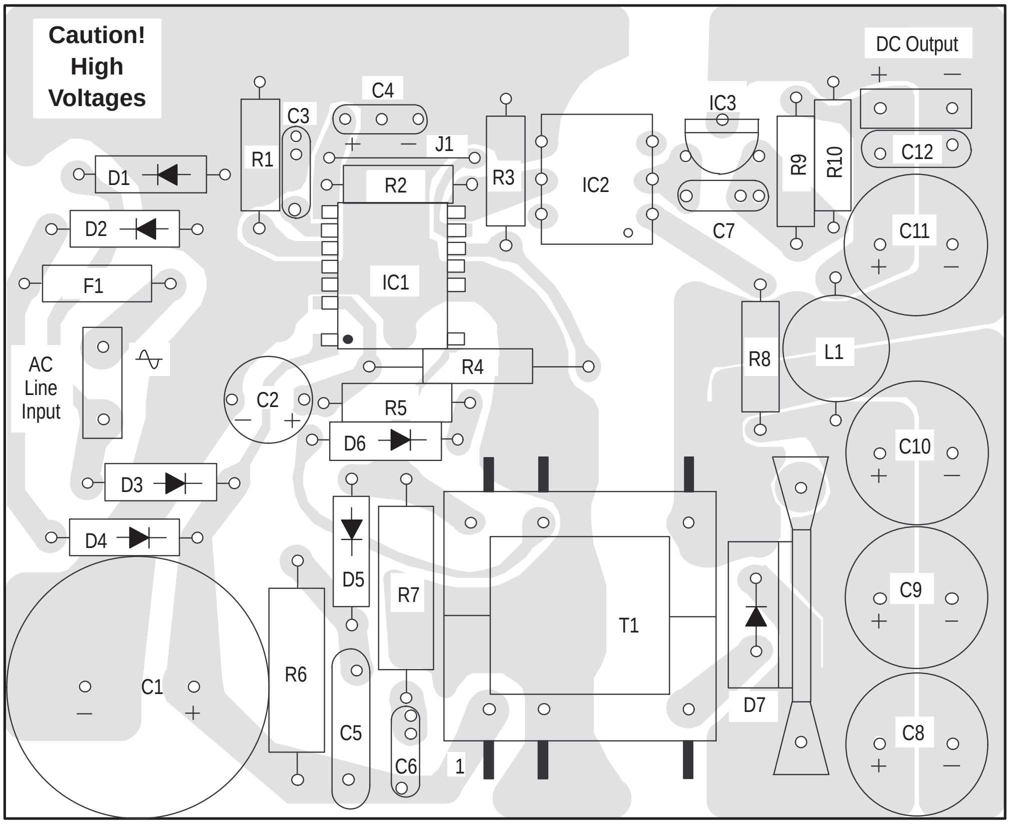
C11 = Sanyo Os–Con #10SA220M, 220 μF 10 V.

D7 = MBR2515L mounted on Aavid #592502B03400 heatsink.

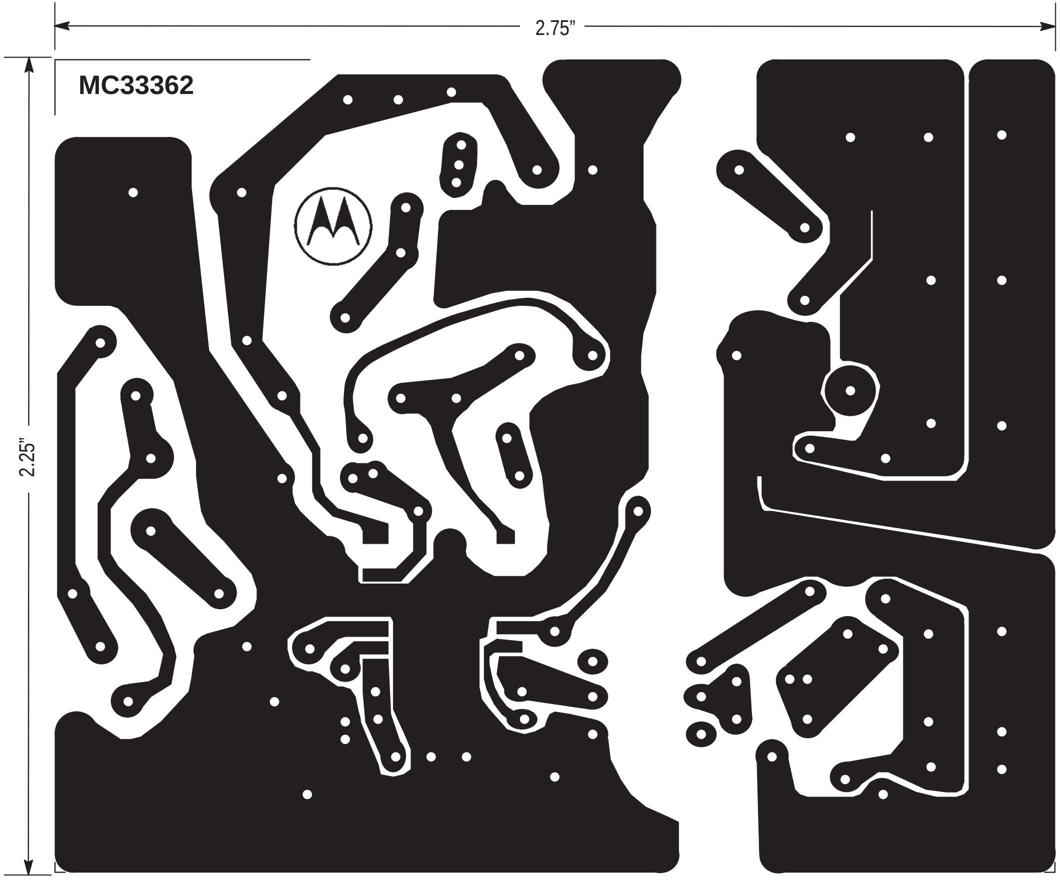
L1 = Coilcraft S5088–A, 5.0 μH, 0.11 Ω.

T1 = Coilcraft S5069–A
Primary: 58 turns of # 26 AWG, Pin 1 = start, Pin 8 = finish.
Two layers 0.002″ Mylar tape.
Secondary: 4 turns of # 18 AWG, 2 strands bifiliar wound, Pin 5 = start, Pin 4 = finish.
Two layers 0.002″ Mylar tape.
Auxiliary: 10 turns of # 26 AWG wound in center of bobbin, Pin 2 = start, Pin 7 = finish.
Two layers 0.002″ Mylar tape.
Gap: 0.014″ total for a primary inductance (L_P) of 330 μH.
Core and Bobbin: Coilcraft PT1950, E187, 3F3 material.

Figure 22. Printed Circuit Board and Component Layout
(Circuit of Figure 20)



(Top View)



(Bottom View)

MOTOROLA

MC33363

Advance Information

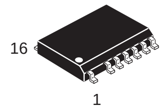
High Voltage Switching Regulator

The MC33363 is a monolithic high voltage switching regulator that is specifically designed to operate from a rectified 240 Vac line source. This integrated circuit features an on–chip 700 V/1.0 A SenseFET power switch, 450 V active off–line startup FET, duty cycle controlled oscillator, current limiting comparator with a programmable threshold and leading edge blanking, latching pulse width modulator for double pulse suppression, high gain error amplifier, and a trimmed internal bandgap reference. Protective features include cycle–by–cycle current limiting, input undervoltage lockout with hysteresis, output overvoltage protection, and thermal shutdown. This device is available in a 16–lead dual–in–line and wide body surface mount packages.

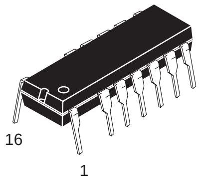
- On–Chip 700 V, 1.0 A SenseFET Power Switch
- Rectified 240 Vac Line Source Operation
- On–Chip 450 V Active Off–Line Startup FET
- Latching PWM for Double Pulse Suppression
- Cycle–By–Cycle Current Limiting
- Input Undervoltage Lockout with Hysteresis
- Output Overvoltage Protection Comparator
- Trimmed Internal Bandgap Reference
- Internal Thermal Shutdown

HIGH VOLTAGE
OFF–LINE
SWITCHING REGULATOR

SEMICONDUCTOR
TECHNICAL DATA

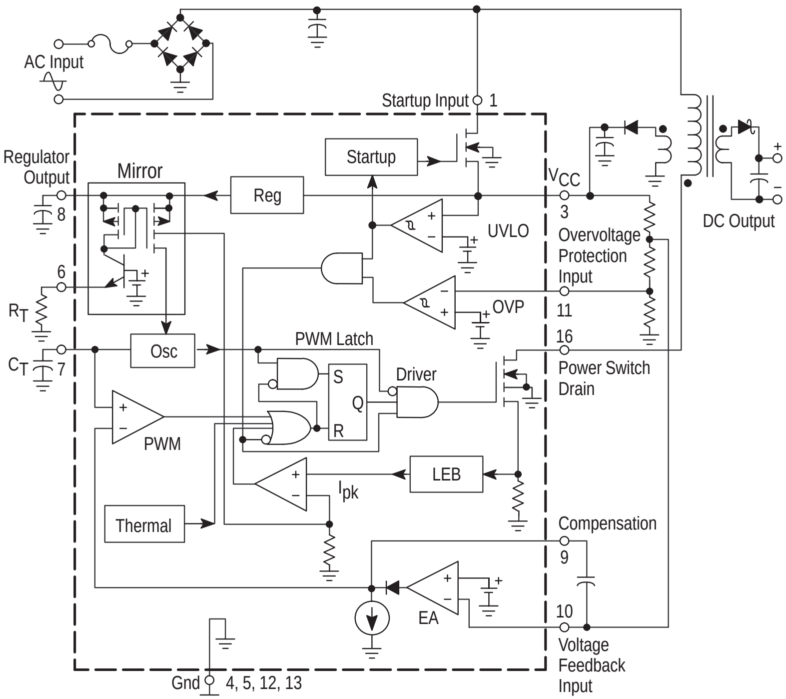


DW SUFFIX
PLASTIC PACKAGE
CASE 751N
(SOP–16L)



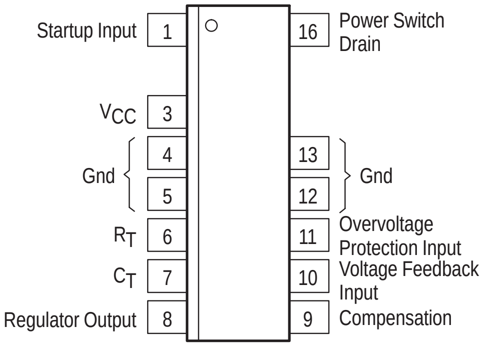
P SUFFIX
PLASTIC PACKAGE
CASE 648E
(DIP–16)

Simplified Application



This device contains 221 active transistors.

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC33363DW	T_J = –25° to +125°C	SOP–16L
MC33363P		DIP–16

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Switch (Pin 16)			
Drain Voltage	V_{DS}	700	V
Drain Current	I_{DS}	1.0	A
Startup Input Voltage (Pin 1, Note 1)	V_{in}		V
Pin 3 = Gnd		400	
Pin 3 ≤ 1000 µF to ground		500	
Power Supply Voltage (Pin 3)	V_{CC}	40	V
Input Voltage Range Voltage Feedback Input (Pin 10) Compensation (Pin 9) Overvoltage Protection Input (Pin 11) R_T (Pin 6) C_T (Pin 7)	V_{IR}	–1.0 to V_{reg}	V
Thermal Characteristics			°C/W
P Suffix, Dual–In–Line Case 648E			
Thermal Resistance, Junction–to–Air	$R_{\theta JA}$	80	
Thermal Resistance, Junction–to–Case (Pins 4, 5, 12, 13)	$R_{\theta JC}$	15	
DW Suffix, Surface Mount Case 751N			
Thermal Resistance, Junction–to–Air	$R_{\theta JA}$	95	
Thermal Resistance, Junction–to–Case (Pins 4, 5, 12, 13)	$R_{\theta JC}$	15	
Refer to Figures 15 and 16 for additional thermal information.			
Operating Junction Temperature	T_J	– 25 to +150	°C
Storage Temperature	T_{stg}	– 55 to +150	°C

NOTE: ESD data available upon request.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 20 V, R_T = 10 k, C_T = 390 pF, $C_{Pin\ 8}$ = 1.0 µF, for typical values T_J = 25°C, for min/max values T_J is the operating junction temperature range that applies (Note 2), unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
REGULATOR (Pin 8)					
Output Voltage (I_O = 0 mA, T_J = 25°C)	V_{reg}	5.5	6.5	7.5	V
Line Regulation (V_{CC} = 20 V to 40 V)	Reg_{line}	–	30	500	mV
Load Regulation (I_O = 0 mA to 10 mA)	Reg_{load}	–	44	200	mV
Total Output Variation over Line, Load, and Temperature	V_{reg}	5.3	–	8.0	V
OSCILLATOR (Pin 7)					
Frequency	f_{OSC}				kHz
C_T = 390 pF					
T_J = 25°C (V_{CC} = 20 V)		260	285	310	
T_J = T_{low} to T_{high} (V_{CC} = 20 V to 40 V)		255	–	315	
C_T = 2.0 nF					
T_J = 25°C (V_{CC} = 20 V)		60	67.5	75	
T_J = T_{low} to T_{high} (V_{CC} = 20 V to 40 V)		59	–	76	
Frequency Change with Voltage (V_{CC} = 20 V to 40 V)	$\Delta f_{OSC}/\Delta V$	–	0.1	2.0	kHz
ERROR AMPLIFIER (Pins 9, 10)					
Voltage Feedback Input Threshold	V_{FB}	2.52	2.6	2.68	V
Line Regulation (V_{CC} = 20 V to 40 V, T_J = 25°C)	Reg_{line}	–	0.6	5.0	mV
Input Bias Current (V_{FB} = 2.6 V)	I_{IB}	–	20	500	nA
Open Loop Voltage Gain (T_J = 25°C)	A_{VOL}	–	82	–	dB
Gain Bandwidth Product (f = 100 kHz, T_J = 25°C)	GBW	–	1.0	–	MHz

NOTES: 1. Maximum power dissipation limits must be observed.
2. Tested junction temperature range for the MC33363:
T_{low} = –25°C T_{high} = +125°C

ELECTRICAL CHARACTERISTICS (continued) (V_{CC} = 20 V, R_T = 10 k, C_T = 390 pF, $C_{Pin\ 8}$ = 1.0 µF, for typical values T_J = 25°C, for min/max values T_J is the operating junction temperature range that applies (Note 2), unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
ERROR AMPLIFIER (Pins 9, 10)					
Output Voltage Swing High State (I_{Source} = 100 µA, V_{FB} < 2.0 V) Low State (I_{Sink} = 100 µA, V_{FB} > 3.0 V)	 V_{OH} V_{OL}	 4.0 –	 5.3 0.2	 – 0.35	V
OVERVOLTAGE DETECTION (Pin 11)					
Input Threshold Voltage	V_{th}	2.47	2.6	2.73	V
Input Bias Current (V_{in} = 2.6 V)	I_{IB}	–	100	500	nA
PWM COMPARATOR (Pins 7, 9)					
Duty Cycle Maximum (V_{FB} = 0 V) Minimum (V_{FB} = 2.7 V)	 $DC_{(max)}$ $DC_{(min)}$	 48 –	 50 0	 52 0	%
POWER SWITCH (Pin 16)					
Drain–Source On–State Resistance (I_D = 200 mA) T_J = 25°C T_J = T_{low} to T_{high}	$R_{DS(on)}$	 – –	 14 –	 17 32	Ω
Drain–Source Off–State Leakage Current (V_{DS} = 700 V)	$I_{D(off)}$	–	0.2	50	µA
Rise Time	t_r	–	50	–	ns
Fall Time	t_f	–	50	–	ns
OVERCURRENT COMPARATOR (Pin 16)					
Current Limit Threshold (R_T = 10 k)	I_{lim}	0.5	0.72	0.9	A
STARTUP CONTROL (Pin 1)					
Peak Startup Current (V_{in} = 400 V) V_{CC} = 0 V V_{CC} = ($V_{th(on)}$ – 0.2 V)	I_{start}	 – –	 20 6.0	 – –	mA
Off–State Leakage Current (V_{in} = 50 V, V_{CC} = 20 V)	$I_{D(off)}$	–	40	200	µA
UNDERVOLTAGE LOCKOUT (Pin 3)					
Startup Threshold (V_{CC} Increasing)	$V_{th(on)}$	11	15.2	18	V
Minimum Operating Voltage After Turn–On	$V_{CC(min)}$	7.5	9.5	11.5	V
TOTAL DEVICE (Pin 3)					
Power Supply Current Startup (V_{CC} = 10 V, Pin 1 Open) Operating	I_{CC}	 – –	 0.25 3.2	 0.5 5.0	mA

Figure 1. Oscillator Frequency versus Timing Resistor

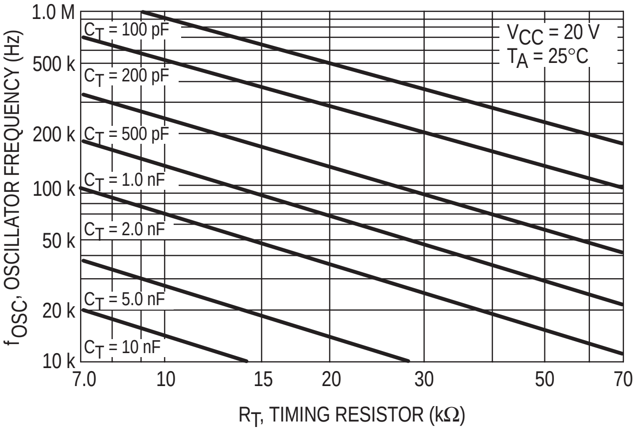
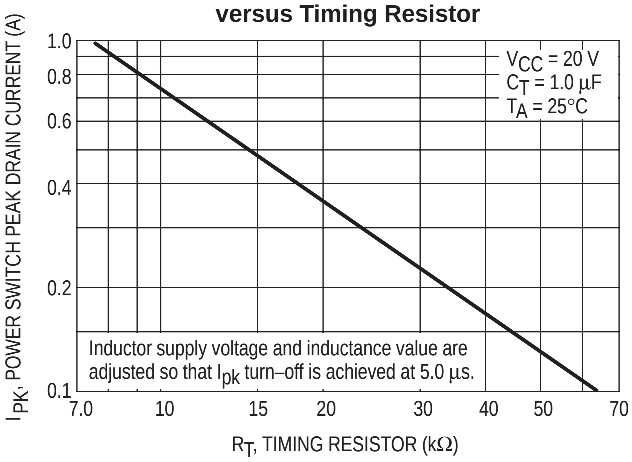


Figure 2. Power Switch Peak Drain Current versus Timing Resistor



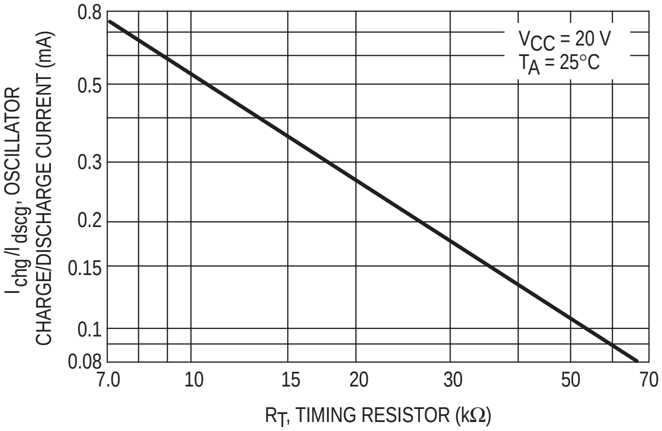


Figure 3. Oscillator Charge/Discharge Current versus Timing Resistor

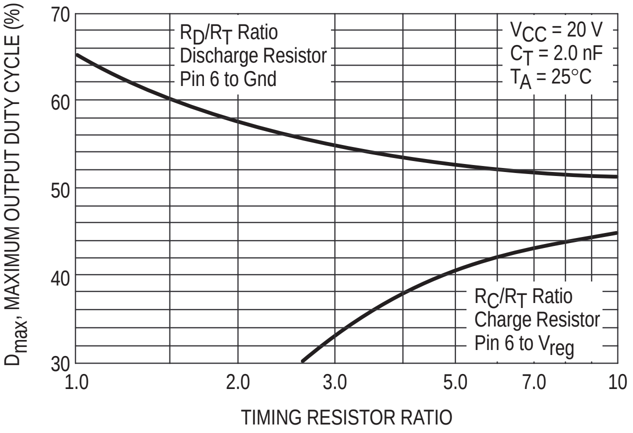


Figure 4. Maximum Output Duty Cycle versus Timing Resistor Ratio

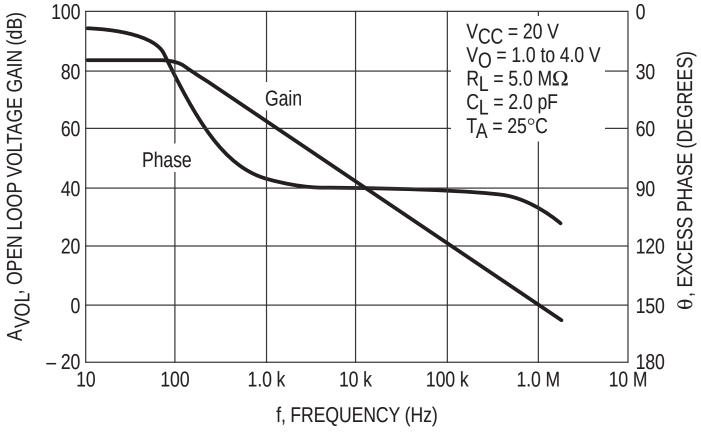


Figure 5. Error Amp Open Loop Gain and Phase versus Frequency

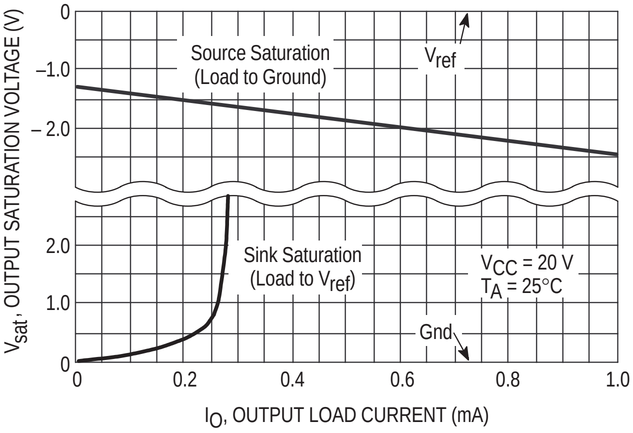


Figure 6. Error Amp Output Saturation Voltage versus Load Current

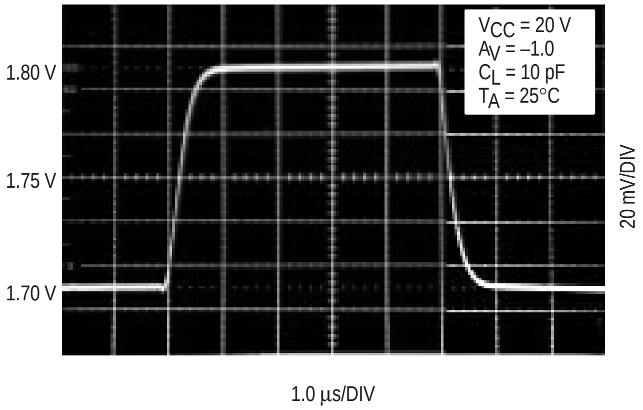


Figure 7. Error Amplifier Small Signal Transient Response

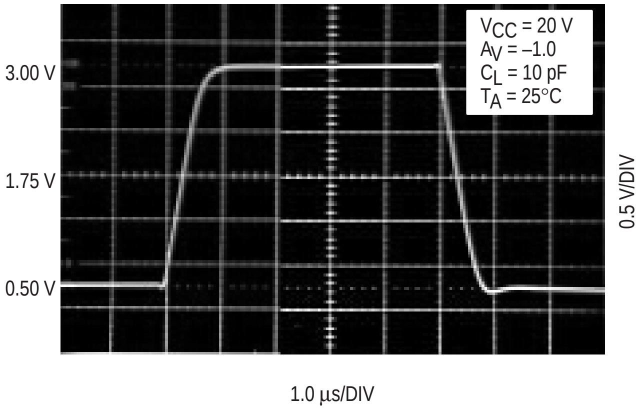


Figure 8. Error Amplifier Large Signal Transient Response

Figure 9. Regulator Output Voltage Change versus Source Current

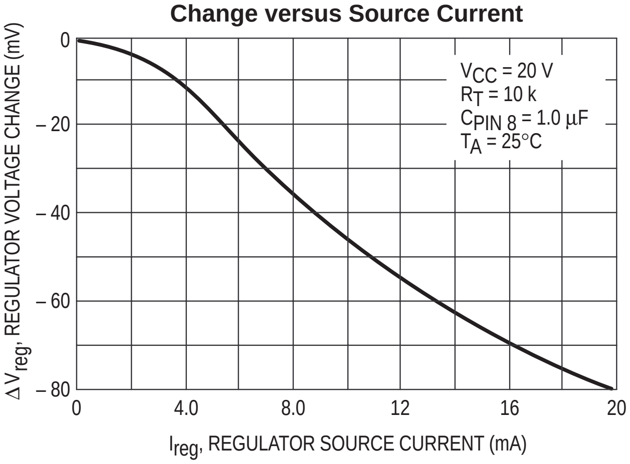
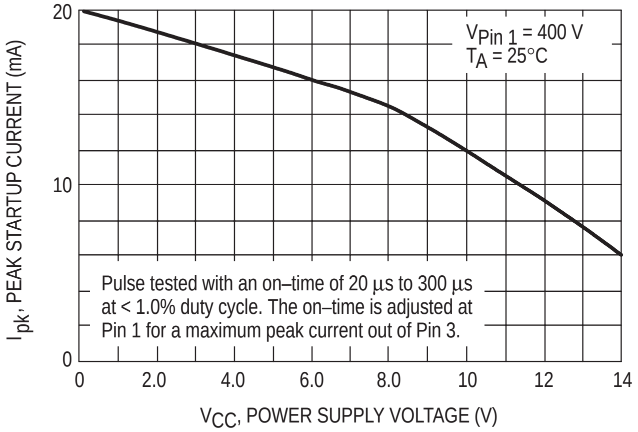
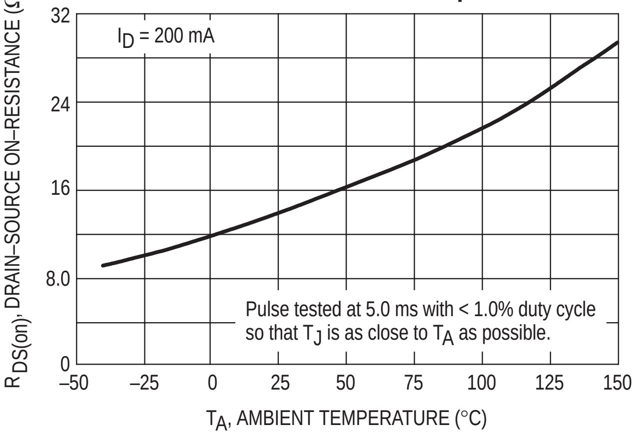


Figure 10. Peak Startup Current versus Power Supply Voltage



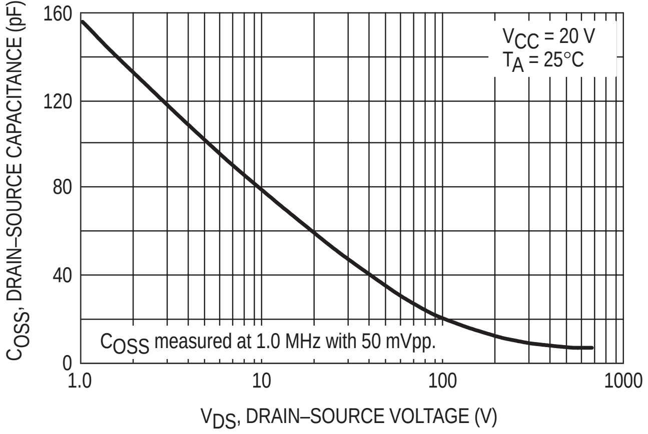
Pulse tested with an on–time of 20 µs to 300 µs at < 1.0% duty cycle. The on–time is adjusted at Pin 1 for a maximum peak current out of Pin 3.

Figure 11. Power Switch Drain–Source On–Resistance versus Temperature



Pulse tested at 5.0 ms with < 1.0% duty cycle so that T_J is as close to T_A as possible.

Figure 12. Power Switch Drain–Source Capacitance versus Voltage



C_{OSS} measured at 1.0 MHz with 50 mVpp.

Figure 13. Supply Current versus Supply Voltage

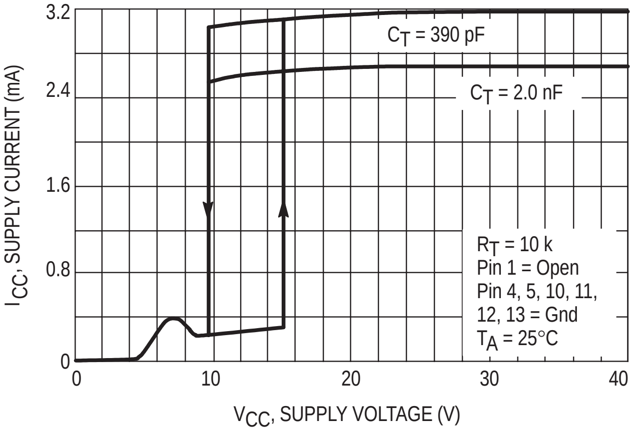
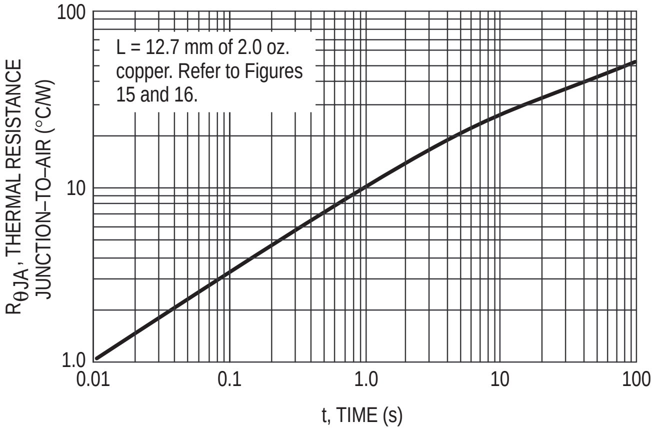


Figure 14. DW and P Suffix Transient Thermal Resistance



L = 12.7 mm of 2.0 oz. copper. Refer to Figures 15 and 16.

Figure 15. DW Suffix (SOP–16L) Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length

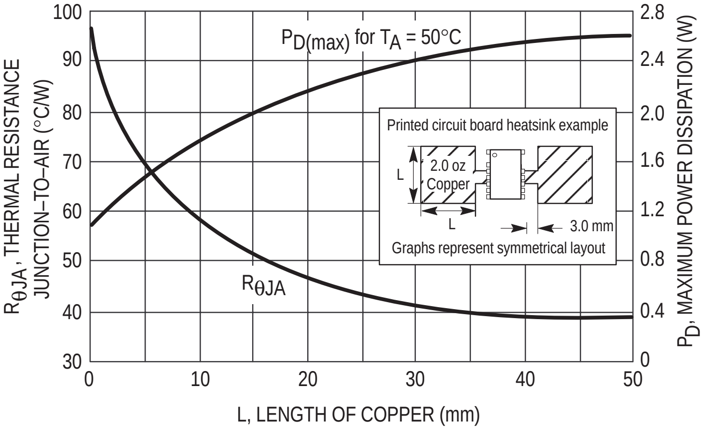
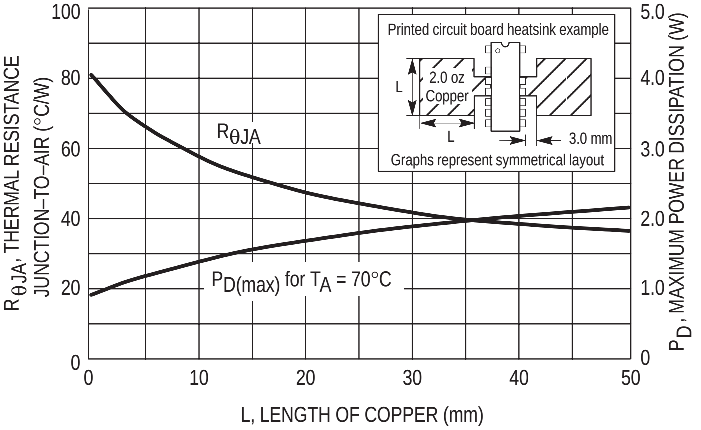


Figure 16. P Suffix (DIP–16) Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length



PIN FUNCTION DESCRIPTION

Pin	Function	Description
1	Startup Input	This pin connects directly to the rectified ac line voltage source. Internally Pin 1 is tied to the drain of a high voltage startup MOSFET. During startup, the MOSFET supplies internal bias, and charges an external capacitor that connects from the V_{CC} pin to ground.
2	–	This pin has been omitted for increased spacing between the rectified ac line voltage on Pin 1 and the V_{CC} potential on Pin 3.
3	V_{CC}	This is the positive supply voltage input. During startup, power is supplied to this input from Pin 1. When V_{CC} reaches the UVLO upper threshold, the startup MOSFET turns off and power is supplied from an auxiliary transformer winding.
4, 5, 12, 13	Ground	These pins are the control circuit grounds. They are part of the IC lead frame and provide a thermal path from the die to the printed circuit board.
6	R_T	Resistor R_T connects from this pin to ground. The value selected will program the Current Limit Comparator threshold and affect the Oscillator frequency.
7	C_T	Capacitor C_T connects from this pin to ground. The value selected, in conjunction with resistor R_T, programs the Oscillator frequency.
8	Regulator Output	This 6.5 V output is available for biasing external circuitry. It requires an external bypass capacitor of at least 1.0 µF for stability.
9	Compensation	This pin is the Error Amplifier output and is made available for loop compensation. It can be used as an input to directly control the PWM Comparator.
10	Voltage Feedback Input	This is the inverting input of the Error Amplifier. It has a 2.6 V threshold and normally connects through a resistor divider to the converter output, or to a voltage that represents the converter output.
11	Overvoltage Protection Input	This input provides runaway output voltage protection due to an external component or connection failure in the control loop feedback signal path. It has a 2.6 V threshold and normally connects through a resistor divider to the converter output, or to a voltage that represents the converter output.
14, 15	–	These pins have been omitted for increased spacing between the high voltages present on the Power Switch Drain, and the ground potential on Pins 12 and 13.
16	Power Switch Drain	This pin is designed to directly drive the converter transformer and is capable of switching a maximum of 700 V and 1.0 A.

Figure 17. Representative Block Diagram

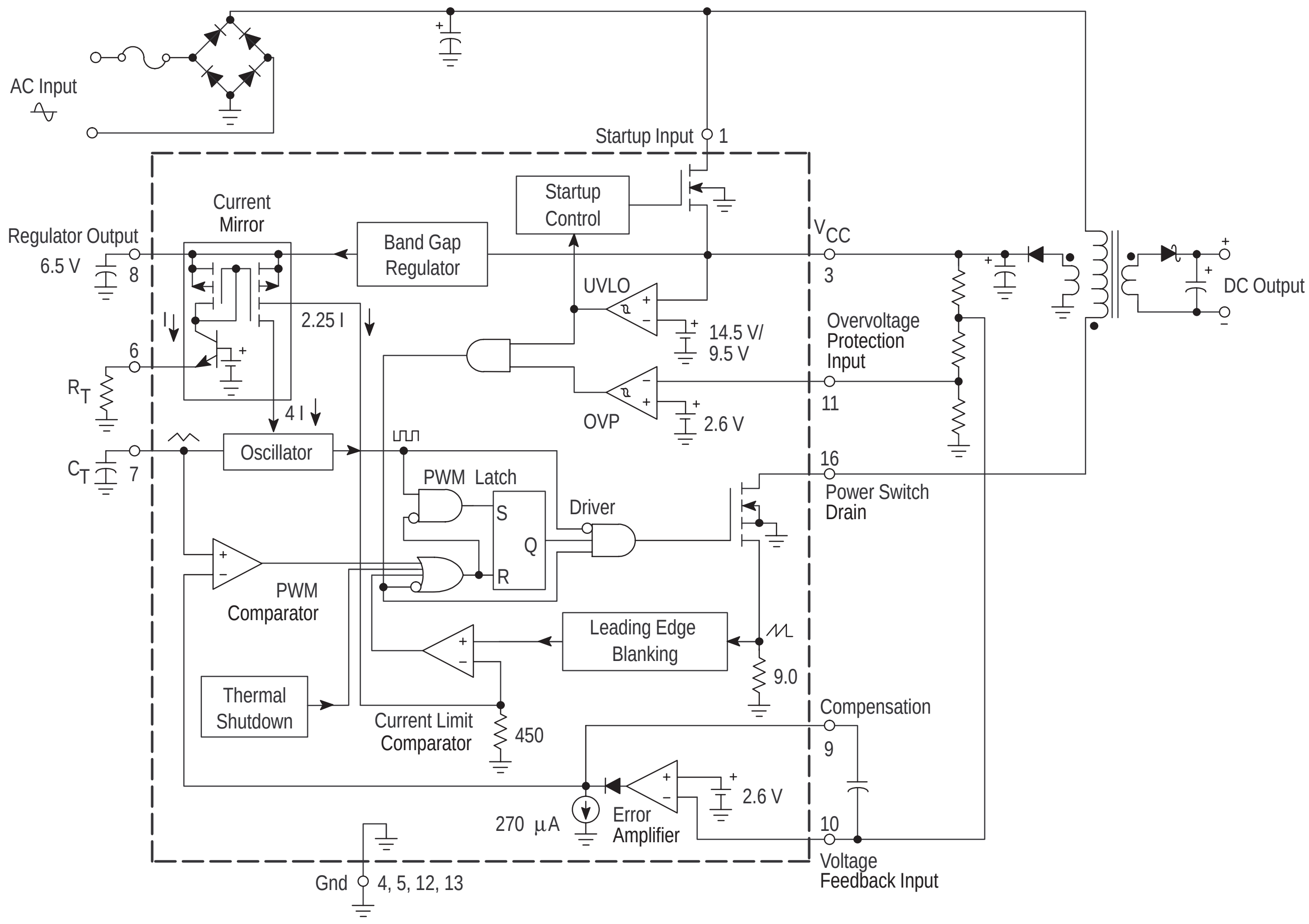
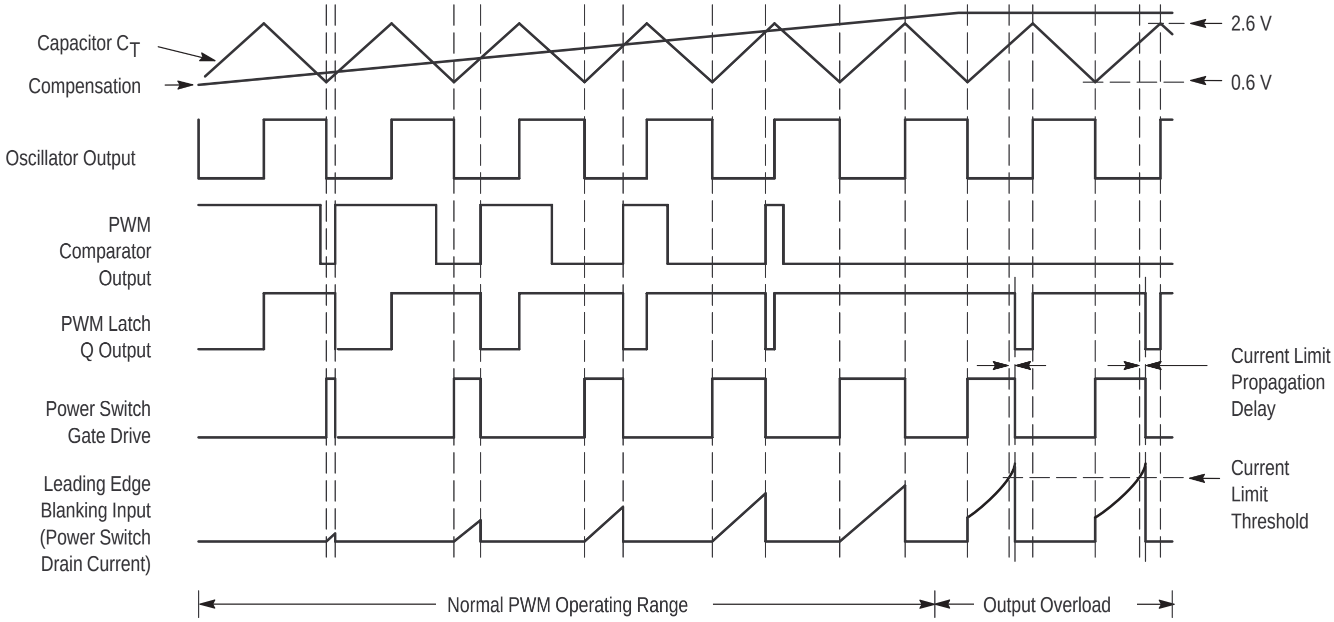


Figure 18. Timing Diagram



OPERATING DESCRIPTION

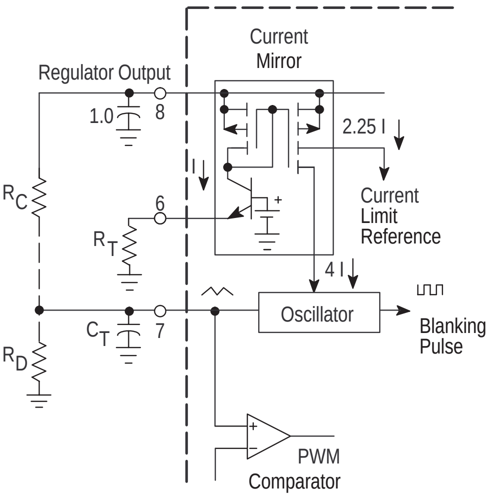
Introduction

The MC33363 represents a new higher level of integration by providing all the active high voltage power, control, and protection circuitry required for implementation of a flyback or forward converter on a single monolithic chip. This device is designed for direct operation from a rectified 240 Vac line source and requires a minimum number of external components to implement a complete converter. A description of each of the functional blocks is given below, and the representative block and timing diagrams are shown in Figures 17 and 18.

Oscillator and Current Mirror

The oscillator frequency is controlled by the values selected for the timing components R_T and C_T. Resistor R_T programs the oscillator charge/discharge current via the Current Mirror 4 I output, Figure 3. Capacitor C_T is charged and discharged by an equal magnitude internal current source and sink. This generates a symmetrical 50 percent duty cycle waveform at Pin 7, with a peak and valley threshold of 2.6 V and 0.6 V respectively. During the discharge of C_T, the oscillator generates an internal blanking pulse that holds the inverting input of the AND gate Driver high. This causes the Power Switch gate drive to be held in a low state, thus producing a well controlled amount of output deadtime. The amount of deadtime is relatively constant with respect to the oscillator frequency when operating below 1.0 MHz. The maximum Power Switch duty cycle at Pin 16 can be modified from the internal 50% limit by providing an additional charge or discharge current path to C_T, Figure 19. In order to increase the maximum duty cycle, a discharge current resistor R_D is connected from Pin 7 to ground. To decrease the maximum duty cycle, a charge current resistor R_C is connected from Pin 7 to the Regulator Output. Figure 4 shows an obtainable range of maximum output duty cycle versus the ratio of either R_C or R_D with respect to R_T.

Figure 19. Maximum Duty Cycle Modification



The formula for the charge/discharge current along with the oscillator frequency are given below. The frequency formula is a first order approximation and is accurate for C_T values greater than 500 pF. For smaller values of C_T, refer to Figure 1. Note that resistor R_T also programs the Current Limit Comparator threshold.

$$I_{chg/dscg} = \frac{5.4}{R_T} \qquad f \approx \frac{I_{chg/dscg}}{4C_T}$$

PWM Comparator and Latch

The pulse width modulator consists of a comparator with the oscillator ramp voltage applied to the non–inverting input, while the error amplifier output is applied into the inverting input. The Oscillator applies a set pulse to the PWM Latch while C_T is discharging, and upon reaching the valley voltage, Power Switch conduction is initiated. When C_T charges to a voltage that exceeds the error amplifier output, the PWM Latch is reset, thus terminating Power Switch conduction for the duration of the oscillator ramp–up period. This PWM Comparator/Latch combination prevents multiple output pulses during a given oscillator clock cycle. The timing diagram shown in Figure 18 illustrates the Power Switch duty cycle behavior versus the Compensation voltage.

Current Limit Comparator and Power Switch

The MC33363 uses cycle–by–cycle current limiting as a means of protecting the output switch transistor from overstress. Each on–cycle is treated as a separate situation. Current limiting is implemented by monitoring the output switch current buildup during conduction, and upon sensing an overcurrent condition, immediately turning off the switch for the duration of the oscillator ramp–up period.

The Power Switch is constructed as a SenseFET allowing a virtually lossless method of monitoring the drain current. It consists of a total of 1780 cells, of which 46 are connected to a 9.0 Ω ground–referenced sense resistor. The Current Sense Comparator detects if the voltage across the sense resistor exceeds the reference level that is present at the inverting input. If exceeded, the comparator quickly resets the PWM Latch, thus protecting the Power Switch. The current limit reference level is generated by the 2.25 I output of the Current Mirror. This current causes a reference voltage to appear across the 450 Ω resistor. This voltage level, as well as the Oscillator charge/discharge current are both set by resistor R_T. Therefore when selecting the values for R_T and C_T, R_T must be chosen first to set the Power Switch peak drain current, while C_T is chosen second to set the desired Oscillator frequency. A graph of the Power Switch peak drain current versus R_T is shown in Figure 2 with the related formula below.

$$I_{pk} = 8.8\left(\frac{R_T}{1000}\right)^{-1.077}$$

The Power Switch is designed to directly drive the converter transformer and is capable of switching a maximum of 700 V and 1.0 A. Proper device voltage snubbing and heatsinking are required for reliable operation.

A Leading Edge Blanking circuit was placed in the current sensing signal path. This circuit prevents a premature reset of the PWM Latch. The premature reset is generated each time the Power Switch is driven into conduction. It appears as a narrow voltage spike across the current sense resistor, and is due to the MOSFET gate to source capacitance, transformer interwinding capacitance, and output rectifier recovery time. The Leading Edge Blanking circuit has a dynamic behavior in that it masks the current signal until the Power Switch turn–on transition is completed. The current limit propagation delay time is typically 233 ns. This time is measured from when an overcurrent appears at the Power Switch drain, to the beginning of turn–off.

Error Amplifier

An fully compensated Error Amplifier with access to the inverting input and output is provided for primary side voltage sensing, Figure 17. It features a typical dc voltage gain of 82 dB, and a unity gain bandwidth of 1.0 MHz with 78 degrees of phase margin, Figure 5. The noninverting input is internally biased at 2.6 V ±3.1% and is not pinned out. The Error Amplifier output is pinned out for external loop compensation and as a means for directly driving the PWM Comparator. The output was designed with a limited sink current capability of 270 µA, allowing it to be easily overridden with a pull–up resistor. This is desirable in applications that require secondary side voltage sensing, Figure 20. In this application, the Voltage Feedback Input is connected to the Regulator Output. This disables the Error Amplifier by placing its output into the sink state, allowing the optocoupler transistor to directly control the PWM Comparator.

Overvoltage Protection

An Overvoltage Protection Comparator is included to eliminate the possibility of runaway output voltage. This condition can occur if the control loop feedback signal path is broken due to an external component or connection failure. The comparator is normally used to monitor the primary side V_{CC} voltage. When the 2.6 V threshold is exceeded, it will immediately turn off the Power Switch, and protect the load from a severe overvoltage condition. This input can also be driven from external circuitry to inhibit converter operation.

Undervoltage Lockout

An Undervoltage Lockout comparator has been incorporated to guarantee that the integrated circuit has sufficient voltage to be fully functional before the output stage is enabled. The UVLO comparator monitors the V_{CC} voltage at Pin 3 and when it exceeds 14.5 V, the reset signal is removed from the PWM Latch allowing operation of the Power Switch. To prevent erratic switching as the threshold is crossed, 5.0 V of hysteresis is provided.

Startup Control

An internal Startup Control circuit with a high voltage enhancement mode MOSFET is included within the MC33363. This circuitry allows for increased converter efficiency by eliminating the external startup resistor, and its associated power dissipation, commonly used in most off–line converters that utilize a UC3842 type of controller. Rectified ac line voltage is applied to the Startup Input, Pin 1. This causes the MOSFET to enhance and supply internal bias as well as charge current to the V_{CC} bypass capacitor that connects from Pin 3 to ground. When V_{CC} reaches the UVLO upper threshold of 15.2 V, the IC commences operation and the startup MOSFET is turned off. Operating bias is now derived from the auxiliary transformer winding, and all of the device power is efficiently converted down from the rectified ac line.

The startup MOSFET will provide an initial peak current of 20 mA, Figure 10, which decreases rapidly as V_{CC} and the die temperature rise. The steady state current will self limit in the range of 8.0 mA with V_{CC} shorted to ground. The startup MOSFET is rated at a maximum of 400 V with V_{CC} shorted to ground, and 500 V when charging a V_{CC} capacitor of 1000 µF or less.

Regulator

A low current 6.5 V regulated output is available for biasing the Error Amplifier and any additional control system circuitry. It is capable of up to 10 mA and has short–circuit protection. This output requires an external bypass capacitor of at least 1.0 µF for stability.

Thermal Shutdown and Package

Internal thermal circuitry is provided to protect the Power Switch in the event that the maximum junction temperature is exceeded. When activated, typically at 155°C, the Latch is forced into a ‘reset’ state, disabling the Power Switch. The Latch is allowed to ‘set’ when the Power Switch temperature falls below 145°C. This feature is provided to prevent catastrophic failures from accidental device overheating. It is not intended to be used as a substitute for proper heatsinking.

The MC33363 is contained in a heatsinkable plastic dual–in–line package in which the die is mounted on a special heat tab copper alloy lead frame. This tab consists of the four center ground pins that are specifically designed to improve thermal conduction from the die to the circuit board. Figures 15 and 16 show a simple and effective method of utilizing the printed circuit board medium as a heat dissipater by soldering these pins to an adequate area of copper foil. This permits the use of standard layout and mounting practices while having the ability to halve the junction to air thermal resistance. The examples are for a symmetrical layout on a single–sided board with two ounce per square foot of copper. Figure 22 shows a practical example of a printed circuit board layout that utilizes the copper foil as a heat dissipater. Note that a jumper was added to the layout from Pins 8 to 10 in order to enhance the copper area near the device for improved thermal conductivity. The application circuit requires two ounce copper foil in order to obtain 8.0 watts of continuous output power at room temperature.

Figure 20. 8.0 W Off–Line Converter

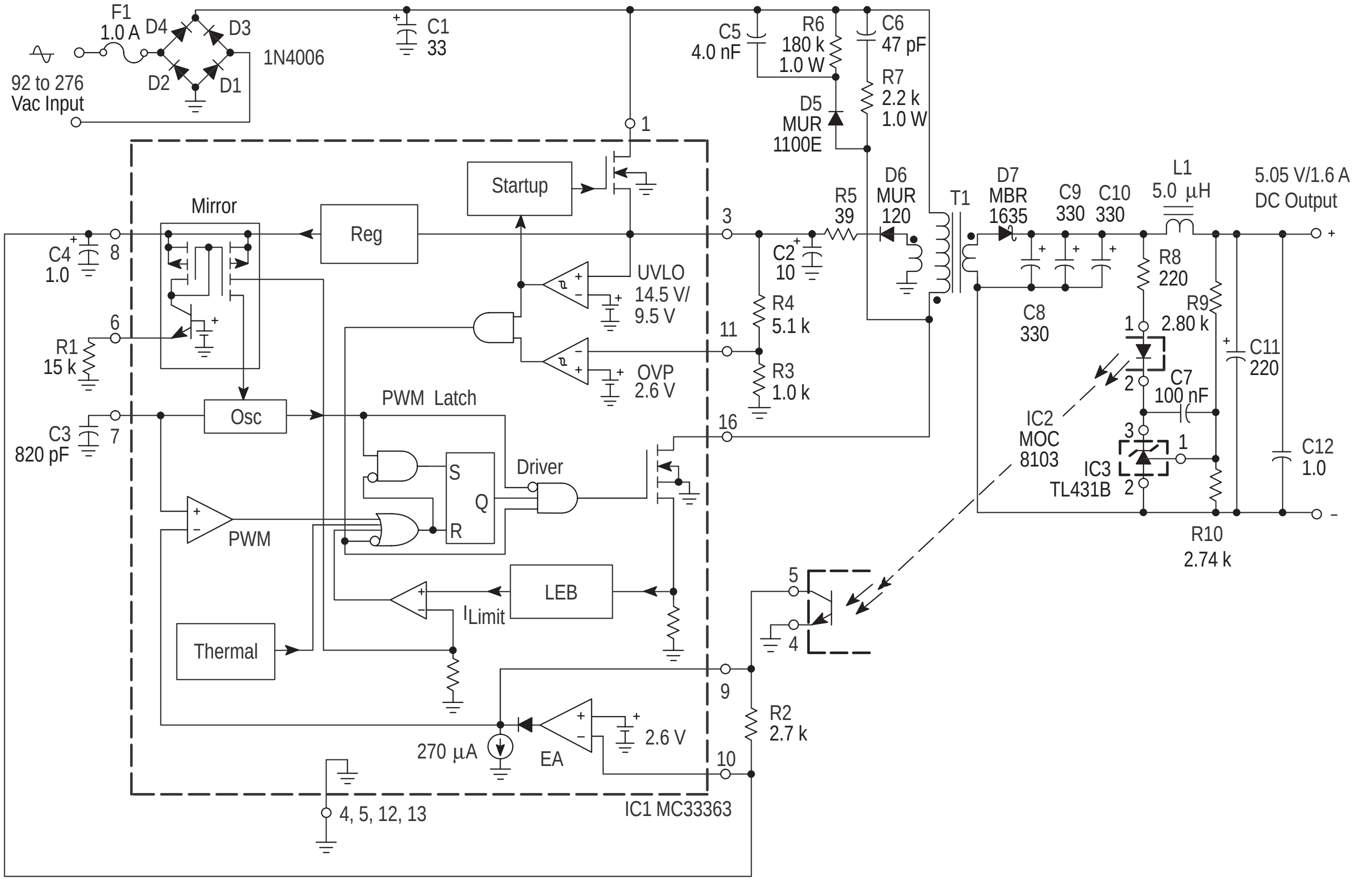


Figure 21. Converter Test Data

Test	Conditions	Results
Line Regulation	V_{in} = 92 Vac to 276 Vac, I_O 1.6 A	Δ = 1.0 mV
Load Regulation	V_{in} = 115 Vac, I_O = 0.4 A to 1.6 A	Δ = 4.0 mV
	V_{in} = 230 Vac, I_O = 0.4 A to 1.6 A	Δ = 4.0 mV
Output Ripple	V_{in} = 115 Vac, I_O = 1.6 A	Triangular = 2.0 mVpp, Spike = 12 mVpp
	V_{in} = 230 Vac, I_O = 1.6 A	Triangular = 2.0 mVpp, Spike = 12 mVpp
Efficiency	V_{in} = 115 Vac, I_O = 1.6 A	78.6%*
	V_{in} = 230 Vac, I_O = 1.6 A	75.6%

This data was taken with the components listed below mounted on the printed circuit board shown in Figure 22.

* With MBR2535CTL, 79.8% efficiency. PCB layout modification is required to use this rectifier.

For high efficiency and small circuit board size, the Sanyo Os–Con capacitors are recommended for C8, C9, C10 and C11.

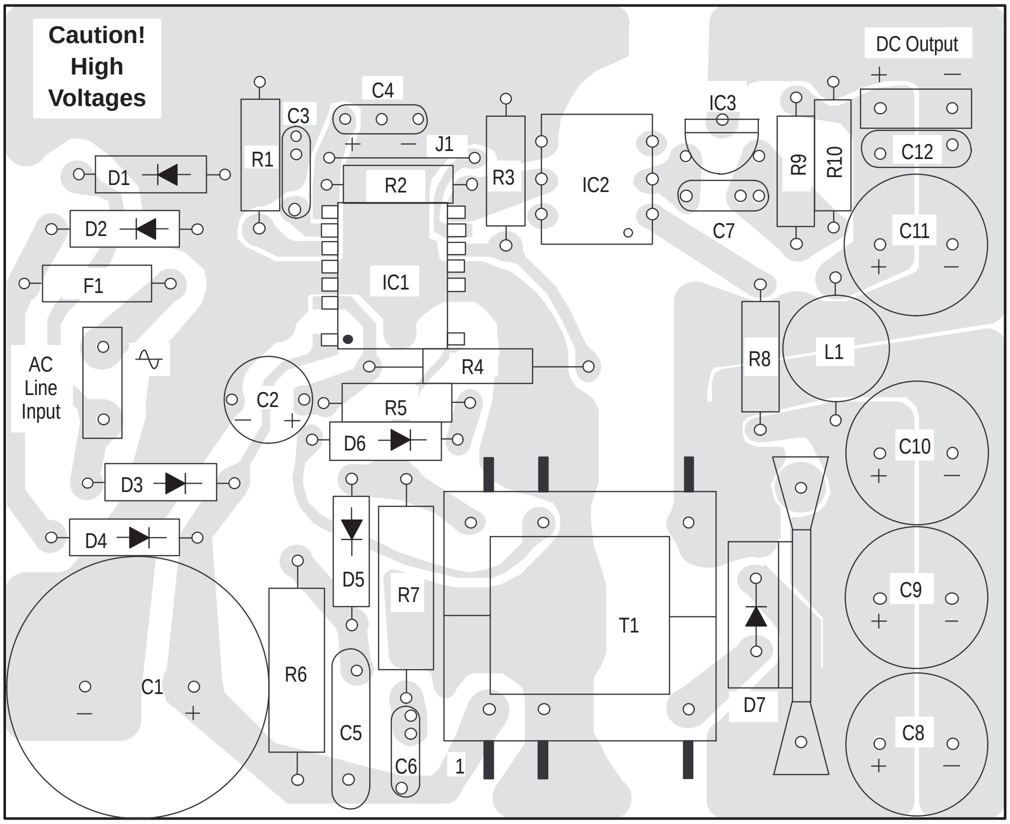
C8, C9, C10 = Sanyo Os–Con #6SA330M, 330 µF 6.3 V.

C11 = Sanyo Os–Con #10SA220M, 220 µF 10 V.

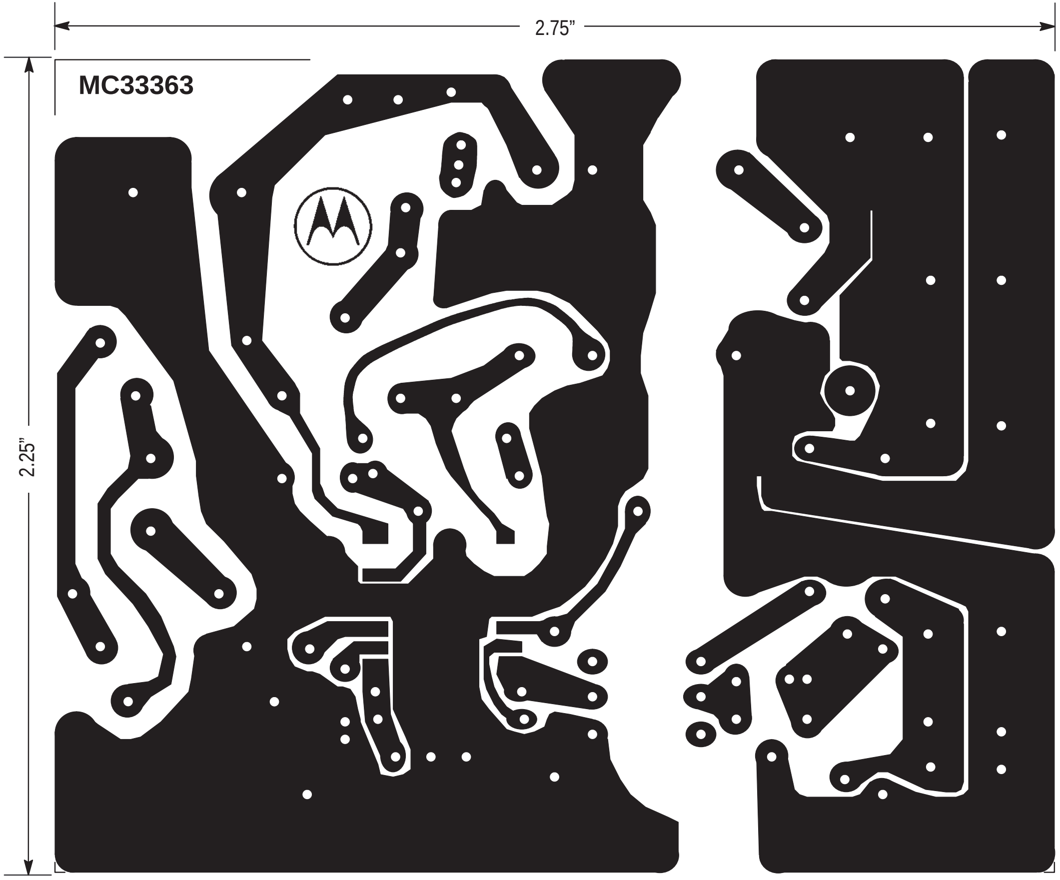
L1 = Coilcraft S5088–A, 5.0 µH, 0.11 Ω.

T1 = Coilcraft S5502–A
Primary: 77 turns of # 28 AWG, Pin 1 = start, Pin 8 = finish.
Two layers 0.002″ Mylar tape.
Secondary: 5 turns of # 22 AWG, 2 strands bifiliar wound, Pin 5 = start, Pin 4 = finish.
Two layers 0.002″ Mylar tape.
Auxiliary: 13 turns of # 28 AWG wound in center of bobbin, Pin 2 = start, Pin 7 = finish.
Two layers 0.002″ Mylar tape.
Gap: 0.006″ total for a primary inductance (L_P) of 1.0 mH.
Core and Bobbin: Coilcraft PT1950, E187, 3F3 material.

Figure 22. Printed Circuit Board and Component Layout
(Circuit of Figure 20)



(Top View)



(Bottom View)

MOTOROLA

MC33363A

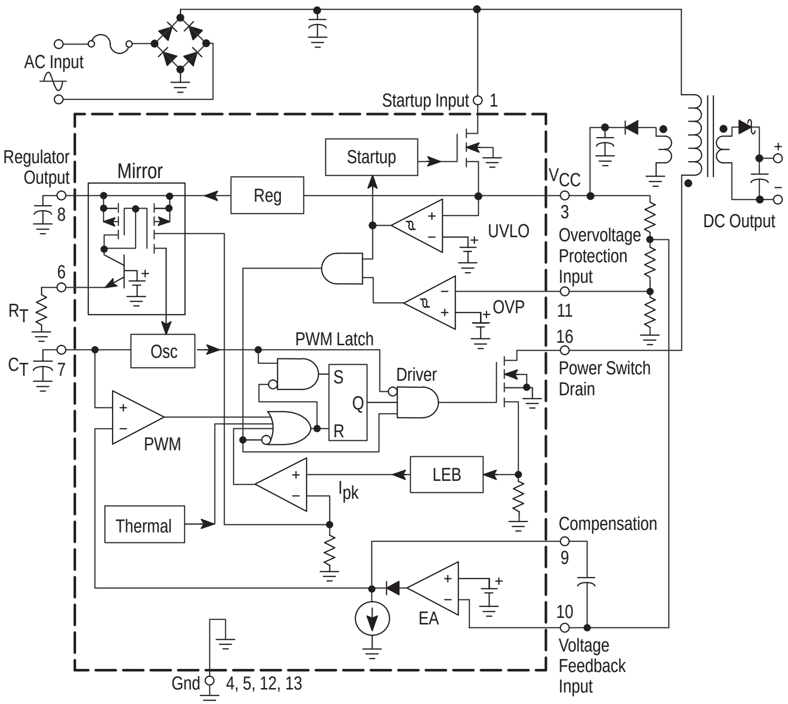
Product Preview

High Voltage Switching Regulator

The MC33363A is a monolithic high voltage switching regulator that is specifically designed to operate from a rectified 240 Vac line source. This integrated circuit features an on–chip 700 V/1.5 A SenseFET power switch, 450 V active off–line startup FET, duty cycle controlled oscillator, current limiting comparator with a programmable threshold and leading edge blanking, latching pulse width modulator for double pulse suppression, high gain error amplifier, and a trimmed internal bandgap reference. Protective features include cycle–by–cycle current limiting, input undervoltage lockout with hysteresis, output overvoltage protection, and thermal shutdown. This device is available in a 16–lead dual–in–line and wide body surface mount packages.

- Enhanced Power Capability Over MC33363
- On–Chip 700 V, 1.5 A SenseFET Power Switch
- Rectified 240 Vac Line Source Operation
- On–Chip 450 V Active Off–Line Startup FET
- Latching PWM for Double Pulse Suppression
- Cycle–By–Cycle Current Limiting
- Input Undervoltage Lockout with Hysteresis
- Output Overvoltage Protection Comparator
- Trimmed Internal Bandgap Reference
- Internal Thermal Shutdown

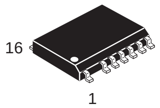
Simplified Application



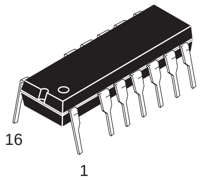
This device contains 221 active transistors.

HIGH VOLTAGE OFF–LINE SWITCHING REGULATOR

SEMICONDUCTOR TECHNICAL DATA

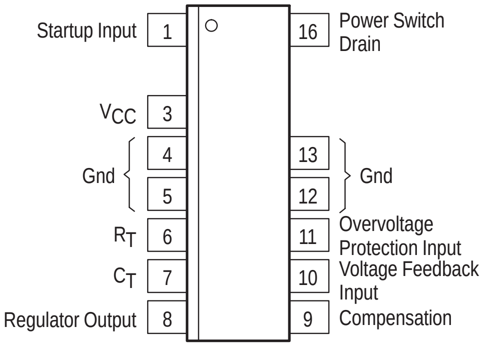


DW SUFFIX
PLASTIC PACKAGE
CASE 751N
(SOP–16L)



P SUFFIX
PLASTIC PACKAGE
CASE 648E
(DIP–16)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC33363ADW	T_J = –25° to +125°C	SOP–16L
MC33363AP		DIP–16

MC33364

Product Preview

Critical Conduction SMPS Controller

The MC33364 series are variable frequency SMPS controllers that operate in the critical conduction mode. They are optimized for low power, high density power supplies requiring minimum board area, reduced component count, and low power dissipation. Each narrow body SOIC package provides a small footprint. Integration of the high voltage startup saves approximately 0.7 W of power compared to resistor bootstrapped circuits.

Each MC33364 features an on–board reference, UVLO function, a watchdog timer to initiate output switching, a zero current detector to ensure critical conduction operation, a current sensing comparator, leading edge blanking, and a CMOS driver. Protection features include the ability to shut down switching, and cycle–by–cycle current limiting.

The MC33364D1 is available in a surface mount SO–8 package. It has an internal 144 kHz frequency clamp. For loads which have a low power operating condition, the frequency clamp limits the maximum operating frequency, preventing excessive switching losses and EMI radiation.

The MC33364D2 is available in the SO–8 package without an internal frequency clamp.

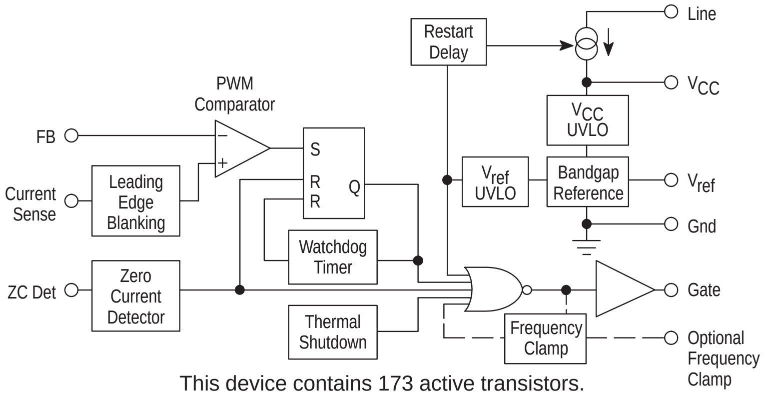
The MC33364D is available in the SO–16 package. It has an internal 144 kHz frequency clamp which is pinned out, so that the designer can adjust the clamp frequency by connecting appropriate values of resistance and capacitance.

- Lossless Off–Line Startup
- Leading Edge Blanking for Noise Immunity
- Watchdog Timer to Initiate Switching
- Minimum Number of Support Components
- Shutdown Capability
- Over Temperature Protection
- Optional Frequency Clamp

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC33364D1	T_J = –25° to +125°C	SO–8
MC33364D2		SO–8
MC33364D		SO–16

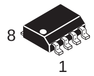
Representative Block Diagram



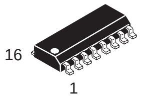
This device contains 173 active transistors.

CRITICAL CONDUCTION SMPS CONTROLLER

SEMICONDUCTOR TECHNICAL DATA



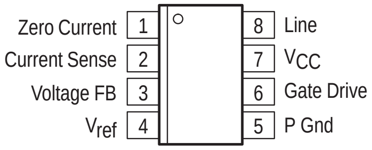
D1, D2 SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)



D SUFFIX
PLASTIC PACKAGE
CASE 751B
(SO–16)

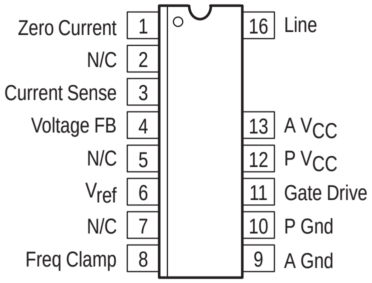
PIN CONNECTIONS

MC33364D1
MC33364D2



(Top View)

MC33364D



(Top View)

MOTOROLA

MC33368

Advance Information

High Voltage GreenLine™ Power Factor Controller

The MC33368 is an active power factor controller that functions as a boost preconverter in off–line power supply applications. MC33368 is optimized for low power, high density power supplies requiring a minimum board area, reduced component count and low power dissipation. The narrow body SOIC package provides a small footprint. Integration of the high voltage startup saves approximately 0.7 W of power compared to resistor bootstrapped circuits.

The MC33368 features a watchdog timer to initiate output switching, a one quadrant multiplier to force the line current to follow the instantaneous line voltage a zero current detector to ensure critical conduction operation, a transconductance error amplifier, a current sensing comparator, a 5.0 V reference, an undervoltage lockout (UVLO) circuit which monitors the V_{CC} supply voltage and a CMOS driver for driving MOSFETs. The MC33368 also includes a programmable output switching frequency clamp. Protection features include an output overvoltage comparator to minimize overshoot, a restart delay timer and cycle–by–cycle current limiting.

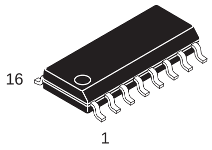
- Lossless Off–Line Startup
- Output Overvoltage Comparator
- Leading Edge Blanking (LEB) for Noise Immunity
- Watchdog Timer to Initiate Switching
- Restart Delay Timer

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC33368D	T_J = –25° to +125°C	SO–16

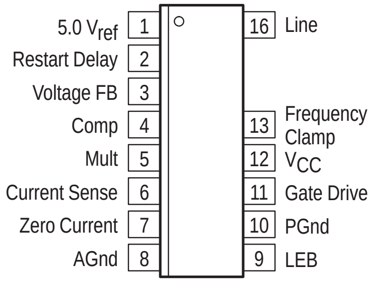
HIGH VOLTAGE GREENLINE™ POWER FACTOR CONTROLLER

SEMICONDUCTOR TECHNICAL DATA



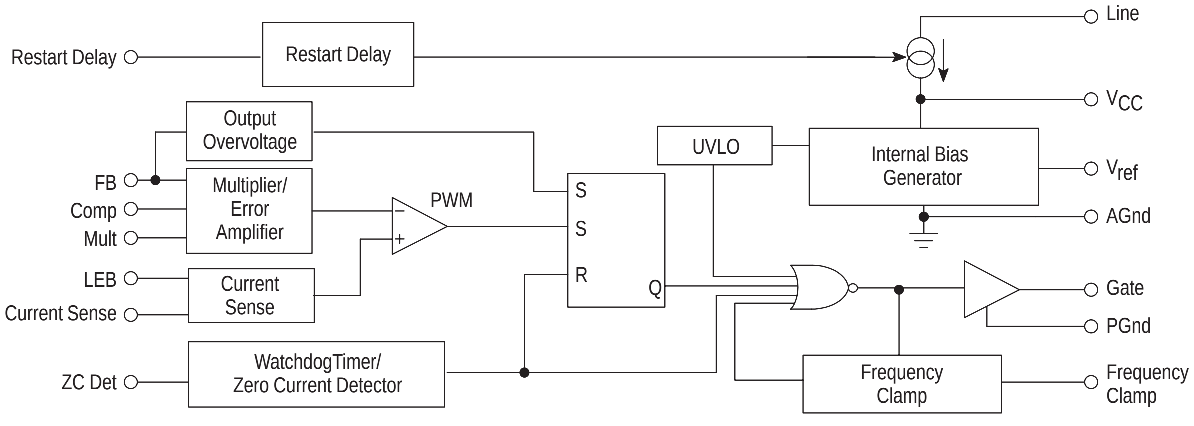
D SUFFIX
PLASTIC PACKAGE
CASE 751K
(SO–16)

PIN CONNECTIONS



(Top View)

Representative Block Diagram



This device contains 240 active transistors.

MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage (Transient)	V_{CC}	20	V
Power Supply Voltage (Operating)	V_{CC}	16	V
Line Voltage	V_{Line}	500	V
Current Sense, Multiplier, Compensation, Voltage Feedback, Restart Delay and Zero Current Input Voltage	V_{in1}	–1.0 to +10	V
LEB Input, Frequency Clamp Input	V_{in2}	–1.0 to +20	V
Zero Current Detect Input	I_{in}	±5.0	mA
Restart Diode Current	I_{in}	5.0	mA
Power Dissipation and Thermal Characteristics D Suffix, Plastic Package Case 626 Maximum Power Dissipation @ T_A = 70°C Thermal Resistance, Junction–to–Air	 P_D $R_{\theta JA}$	 450 178	 mW °C/W
Operating Junction Temperature	T_J	150	°C
Operating Ambient Temperature	T_A	–25 to +125	°C
Storage Temperature Range	T_{stg}	–55 to +150	°C

NOTE: ESD data available upon request.

ELECTRICAL CHARACTERISTICS (V_{CC} = 14.5 V, for typical values T_A = 25°C, for min/max values T_J = –25 to +125°C)

Characteristic	Symbol	Min	Typ	Max	Unit
ERROR AMPLIFIER					
Input Bias Current (V_{FB} = 5.0 V)	I_{IB}	–	0	1.0	µA
Input Offset Voltage (V_{Comp} = 3.0 V)	V_{IO}	–	2.0	50	mV
Transconductance (V_{Comp} = 3.0 V)	g_m	30	51	80	µmho
Output Source (V_{FB} = 4.6 V, V_{Comp} = 3.0 V) Output Sink (V_{FB} = 5.4 V, V_{Comp} = 3.0 V)	I_O I_O	9.0 9.0	17.5 17.5	30 30	µA
OVERVOLTAGE COMPARATOR					
Voltage Feedback Input Threshold	$V_{FB(OV)}$	1.07 V_{FB}	1.084 V_{FB}	1.1 V_{FB}	V
Propagation Time to Output	T_P	–	705	–	ns
MULTIPLIER					
Input Bias Current, V_{Mult} (V_{FB} = 0 V)	I_{IB}	–	–0.2	–1.0	µA
Input Threshold, V_{Comp}	$V_{th(M)}$	1.8	2.1	2.4	V
Dynamic Input Voltage Range Multiplier Input Compensation	 V_{Mult} V_{Comp}	 0 to 2.5 $V_{th(M)}$ to ($V_{th(M)}$ + 1.0)	 0 to 3.5 $V_{th(M)}$ to ($V_{th(M)}$ + 2.0)	 – –	V
Multiplier Gain (V_{Mult} = 0.5 V, V_{Comp} = $V_{th(M)}$ + 1.0 V) $\left[K = \frac{V_{CS}\ \text{Threshold}}{V_{Mult}\left(V_{Comp} - V_{th(M)}\right)}\right]$	K	0.25	0.51	0.75	1/V
VOLTAGE REFERENCE					
Voltage Reference (I_O = 0 mA, T_J = 25°C)	V_{ref}	4.95	5.0	5.05	V
Line Regulation (V_{CC} = 10 V to 16 V)	Reg_{line}	–	5.0	100	mV
Load Regulation (I_O = 0 – 5.0 mA)	Reg_{load}	–	5.0	100	mV
Total Output Variation Over Line, Load and Temperature	V_{ref}	4.8	–	5.2	V
Maximum Output Current	I_O	5.0	10	–	mA
Reference Undervoltage Lockout Threshold	V_{th}	–	4.5	–	V

ELECTRICAL CHARACTERISTICS (continued) (V_{CC} = 14.5 V, for typical values T_A = 25°C, for min/max values T_J = –25 to +125°C)

Characteristic	Symbol	Min	Typ	Max	Unit
ZERO CURRENT DETECTOR					
Input Threshold Voltage (V_{in} Increasing)	V_{th}	1.0	1.2	1.4	V
Hysteresis (V_{in} Decreasing)	V_H	100	200	300	mV
Delay to Output	T_{pd}	–	127	–	ns
CURRENT SENSE COMPARATOR					
Input Bias Current (V_{CS} = 0 to 2.0 V)	I_{IB}	–	0.2	1.0	µA
Input Offset Voltage (V_{Mult} = –0.2 V)	V_{IO}	–	4.0	50	mV
Maximum Current Sense Input Threshold (V_{Comp} = 5.0 V, V_{Mult} = 5.0 V)	$V_{th(max)}$	1.3	1.5	1.8	V
Delay to Output (V_{LEB} = 12 V, V_{Comp} = 5.0 V, V_{Mult} = 5.0 V) (V_{CS} = 0 to 5.0 V Step, C_L = 1.0 nF)	$t_{PHL(in/out)}$	50	270	425	ns
FREQUENCY CLAMP					
Frequency Clamp Input Threshold	$V_{th(FC)}$	1.9	2.0	2.1	V
Frequency Clamp Capacitor Reset Current (V_{FC} = 0.5 V)	I_{reset}	0.5	1.7	4.0	mA
Frequency Clamp Disable Voltage	V_{DFC}	–	7.3	8.0	V
DRIVE OUTPUT					
Source Resistance (Drive = 0 V, V_{Gate} = V_{CC} – 1.0 V) Sink Resistance (Drive = V_{CC}, V_{Gate} = 1.0 V)	R_{OH} R_{OL}	4.0 4.0	8.6 7.2	20 20	Ω
Output Voltage Rise Time (25% – 75%) (C_L = 1.0 nF)	t_r	–	55	200	ns
Output Voltage Fall Time (75% – 25%) (C_L = 1.0 nF)	t_f	–	70	200	ns
Output Voltage in Undervoltage (V_{CC} = 7.0 V, I_{Sink} = 1.0 mA)	$V_{O(UV)}$	–	0.01	0.25	V
LEADING EDGE BLANKING					
Input Bias Current	I_{bias}	–	0.1	0.5	µA
Threshold (as Offset from V_{CC}) (V_{LEB} Increasing)	V_{LEB}	1.0	2.25	2.75	V
Hysteresis (V_{LEB} Decreasing)	V_H	100	270	500	mV
UNDERVOLTAGE LOCKOUT					
Startup Threshold (V_{CC} Increasing)	$V_{th(on)}$	11.5	13	14.5	V
Minimum Operating Voltage After Turn–On (V_{CC} Decreasing)	$V_{Shutdown}$	7.0	8.5	10	V
Hysteresis	V_H	–	4.5	–	V
TIMER					
Watchdog Timer	t_{DLY}	180	385	800	µs
Restart Timer Threshold	$V_{th(restart)}$	1.5	2.3	3.0	V
Restart Pin Output Current ($V_{restart}$ = 0 V, V_{ref} = 5.0 V)	$I_{restart}$	3.1	5.2	7.1	mA
TOTAL DEVICE					
Line Startup Current (V_{CC} = 0 V, V_{Line} = 50 V)	I_{SU}	5.0	16	25	mA
Line Operating Current (V_{CC} = $V_{th(on)}$, V_{Line} = 50 V)	I_{OP}	3.0	12.9	20	mA
V_{CC} Dynamic Operating Current (50 kHz, C_L = 1.0 nF) V_{CC} Static Operating Current (I_O = 0)	I_{CC}	– –	5.3 3.0	8.5 –	mA
Line Pin Leakage (V_{Line} = 500 V)	I_{Line}	–	30	80	µA

Figure 1. Current Sense Input Threshold versus Multiplier Input

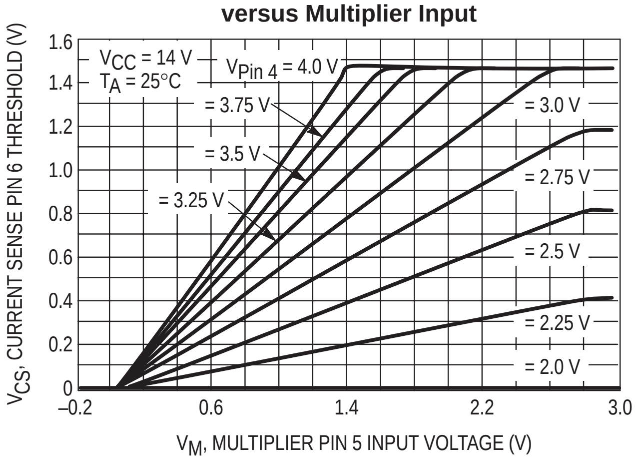


Figure 2. Current Sense Input Threshold versus Multiplier Input, Expanded View

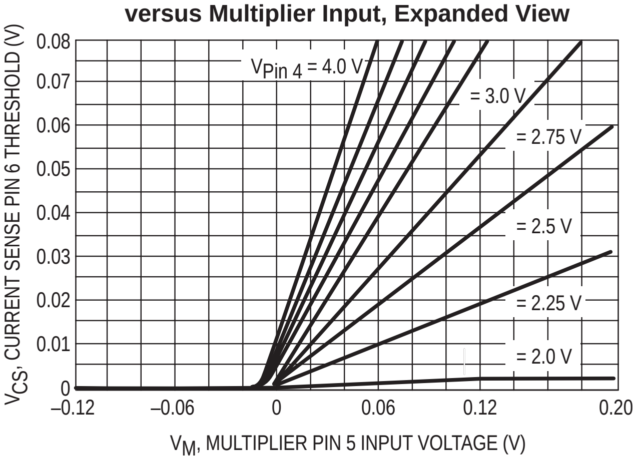


Figure 3. Reference Voltage versus Temperature

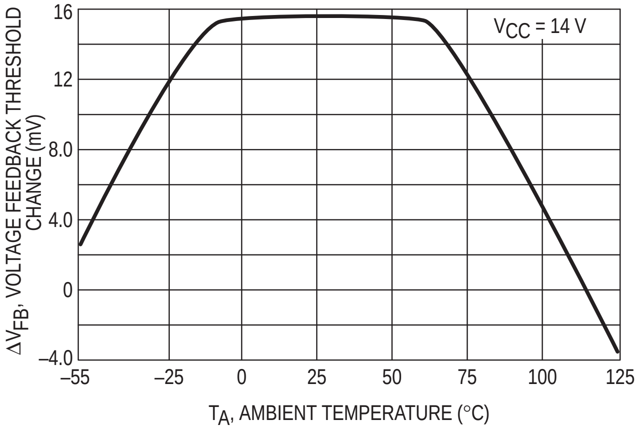


Figure 4. Overvoltage Comparator Input Threshold versus Temperature

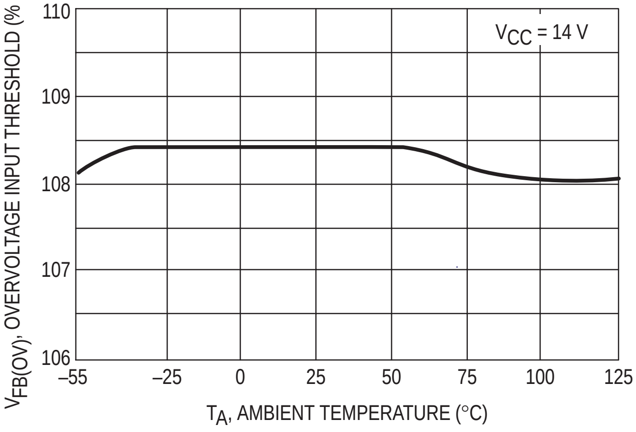


Figure 5. Error Amplifier Transconductance and Phase versus Frequency

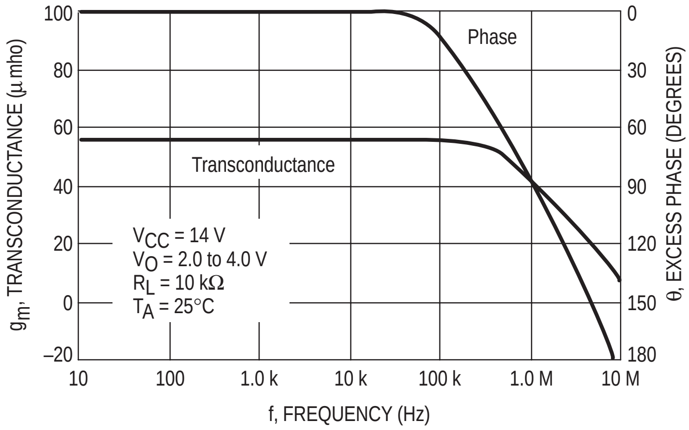


Figure 6. Error Amplifier Transient Response

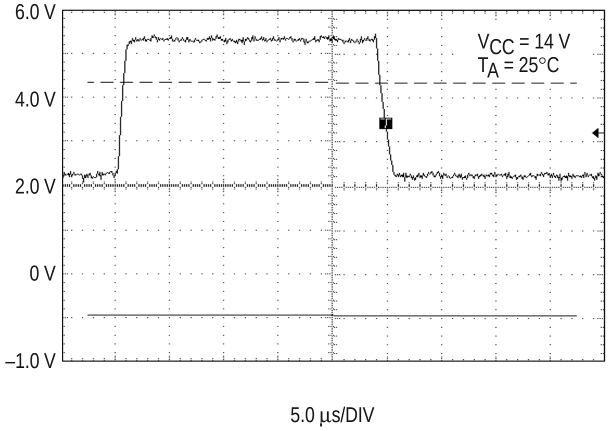


Figure 7. Quickstart Charge Current versus Temperature

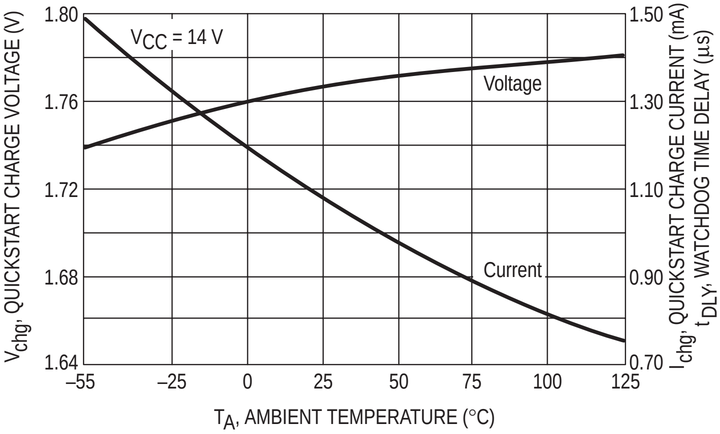


Figure 8. Watchdog Timer Delay versus Temperature

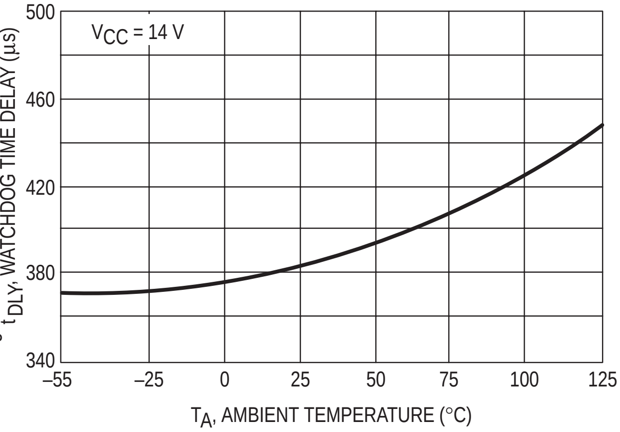


Figure 9. Drive Output Waveform

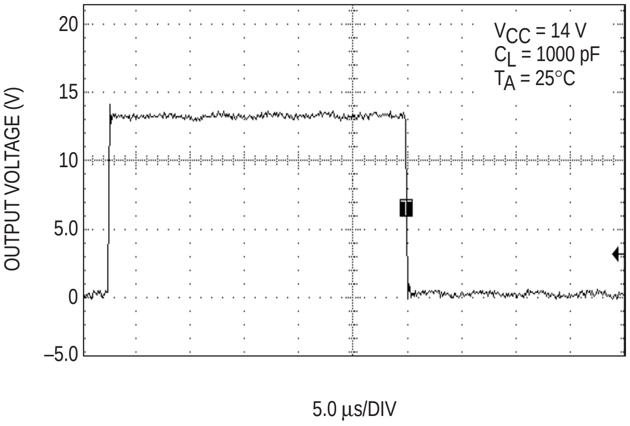


Figure 10. Supply Current versus Supply Voltage

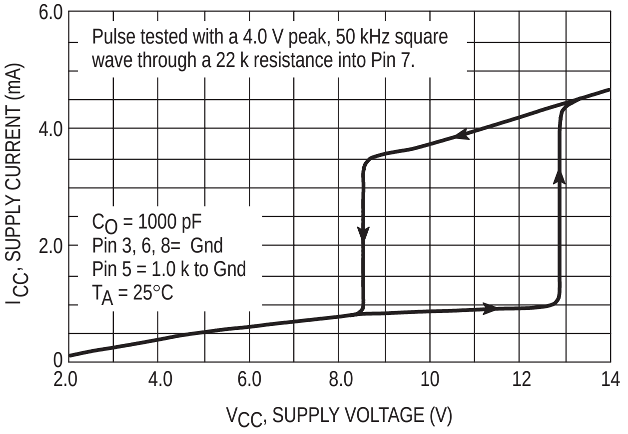


Figure 11. Transient Thermal Resistance

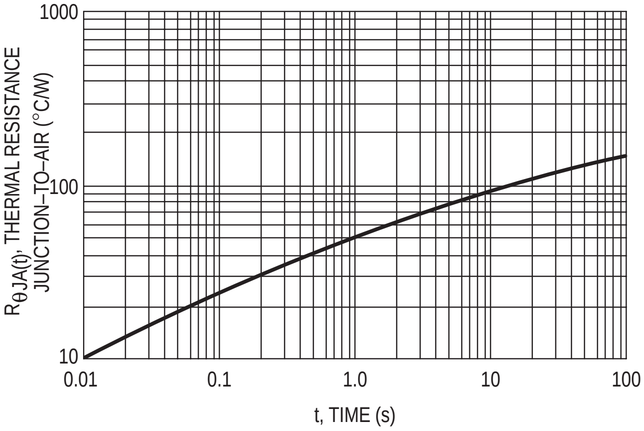
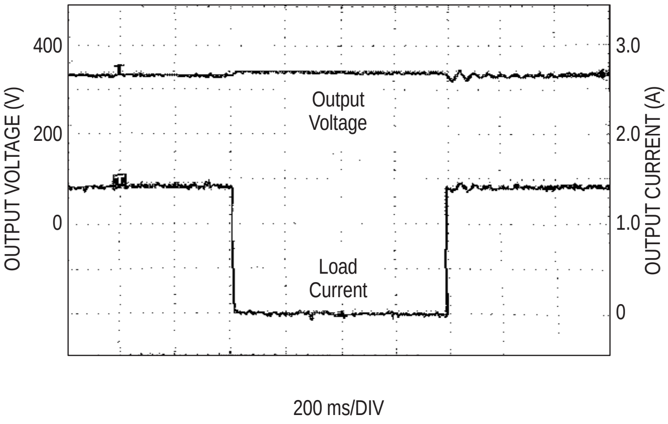


Figure 12. Low Load Detection Response Waveform



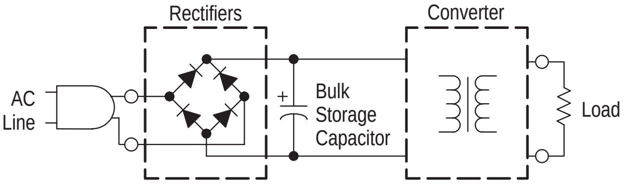
FUNCTIONAL DESCRIPTION

INTRODUCTION

With the goal of exceeding the requirements of legislation on line current harmonic content, there is an ever increasing demand for an economical method of obtaining a unity power factor. This data sheet describes a monolithic control IC that was specifically designed for power factor control with minimal external components. It offers the designer a simple cost effective solution to obtain the benefits of active power factor correction.

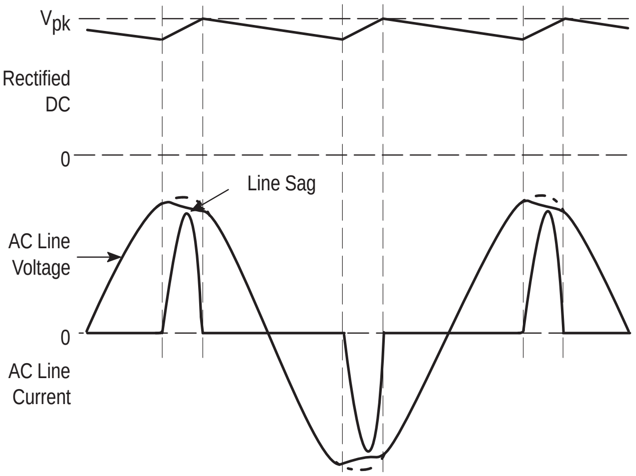
Most electronic ballasts and switching power supplies use a bridge rectifier and a bulk storage capacitor to derive raw dc voltage from the utility ac line, Figure 13.

Figure 13. Uncorrected Power Factor Circuit



This simple rectifying circuit draws power from the line when the instantaneous ac voltage exceeds the capacitor voltage. This occurs near the line voltage peak and results in a high charge current spike, Figure 14. Since power is only taken near the line voltage peaks, the resulting spikes of current are extremely nonsinusoidal with a high content of harmonics. This results in a poor power factor condition where the apparent input power is much higher than the real power. Power factor ratios of 0.5 to 0.7 are common.

Figure 14. Uncorrected Power Factor Input Waveforms



Power factor correction can be achieved with the use of either a passive or active input circuit. Passive circuits usually contain a combination of large capacitors, inductors, and rectifiers that operate at the ac line frequency. Active circuits incorporate some form of a high frequency switching converter for the power processing with the boost converter being the most popular topology. Since active input circuits operate at a frequency much higher than that of the ac line, they are smaller, lighter in weight, and more efficient than a passive circuit that yields similar results. With proper control of the preconverter, almost any complex load can be made to appear resistive to the ac line, thus significantly reducing the harmonic current content.

Operating Description

The MC33368 contains many of the building blocks and protection features that are employed in modern high performance current mode power supply controllers. Referring to the block diagram in Figure 15, note that a multiplier has been added to the current sense loop and that this device does not contain an oscillator. A description of each of the functional blocks is given below.

Error Amplifier

An Error Amplifier with access to the inverting input and output is provided. The amplifier is a transconductance type, meaning that it has high output impedance with controlled voltage–to–current gain ($g_m \approx 50$ μmhos). The noninverting input is internally biased at 5.0 V ±2.0%. The output voltage of the power factor converter is typically divided down and monitored by the inverting input. The maximum input bias current is –1.0 μA which can cause an output voltage error that is equal to the product of the input bias current and the value of the upper divider resistor R2. The Error Amplifier output is internally connected to the Multiplier and is pinned out (Pin 4) for external loop compensation. Typically, the bandwidth is set below 20 Hz so that the amplifier's output voltage is relatively constant over a given ac line cycle. In effect, the error amplifier monitors the average output voltage of the converter over several line cycles resulting in a fixed Drive Output on–time. The amplifier output stage can sink and source 11.5 μA of current and is capable of swinging from 1.7 to 5.0 V, assuring that the Multiplier can be driven over its entire dynamic range.

Note that by using a transconductance type amplifier, the input is allowed to move independently with respect to the output, since the compensation capacitor is connected to ground. This allows dual usage of the Voltage Feedback pin by the Error Amplifier and Overvoltage Comparator.

Overvoltage Comparator

An Overvoltage Comparator is incorporated to eliminate the possibility of runaway output voltage. This condition can occur during initial startup, sudden load removal, or during output arcing and is the result of the low bandwidth that must be used in the Error Amplifier control loop. The Overvoltage Comparator monitors the peak output voltage of the converter, and when exceeded, immediately terminates MOSFET switching. The comparator threshold is internally set to 1.08 V_{ref}. In order to prevent false tripping during normal operation, the value of the output filter capacitor C3 must be large enough to keep the peak–to–peak ripple less than 16% of the average dc output.

Multiplier

A single quadrant, two input multiplier is the critical element that enables this device to control power factor. The ac haversines are monitored at Pin 5 with respect to ground while the Error Amplifier output at Pin 4 is monitored with respect to the Voltage Feedback Input threshold. A graph of the Multiplier transfer curve is shown in Figure 1. Note that both inputs are extremely linear over a wide dynamic range, 0 to 3.2 V for Pin 5 and 2.5 to 4.0 V for Pin 4. The Multiplier output controls the Current Sense Comparator threshold as the ac voltage traverses sinusoidally from zero to peak line. This has the effect of forcing the MOSFET on–time to track the input line voltage, thus making the preconverter load appear to be resistive.

$$\text{Pin 6 Threshold} \approx 0.55 \left(V_{Pin\ 4} - V_{Pin\ 3}\right) V_{Pin\ 5}$$

Zero Current Detector

The MC33368 operates as a critical conduction current mode controller, whereby output switch conduction is initiated by the Zero Current Detector and terminated when the peak inductor current reaches the threshold level established by the Multiplier output. The Zero Current Detector initiates the next on–time by setting the R_S Latch at the instant the inductor current reaches zero. This critical conduction mode of operation has two significant benefits. First, since the MOSFET cannot turn–on until the inductor current reaches zero, the output rectifier's reverse recovery time becomes less critical allowing the use of an inexpensive rectifier. Second, since there are no deadtime gaps between cycles, the ac line current is continuous thus limiting the peak switch to twice the average input current

The Zero Current Detector indirectly senses the inductor current by monitoring when the auxiliary winding voltage falls below 1.2 V. To prevent false tripping, 200 mV of hysteresis is provided. The Zero Current Detector input is internally protected by two clamps. The upper 10 V clamp prevents input overvoltage breakdown while the lower –0.7 V clamp prevents substrate injection. An external resistor must be used in series with the auxiliary winding to limit the current through the clamps to 5.0 mA or less.

Current Sense Comparator and RS Latch

The Current Sense Comparator R_S Latch configuration used ensures that only a single pulse appears at the Drive Output during a given cycle. The inductor current is converted to a voltage by inserting a ground–referenced sense resistor R7 in series with the source of output switch. This voltage is monitored by the Current Sense Input and compared to a level derived from the Multiplier output. The peak inductor current under normal operating conditions is controlled by the threshold voltage of Pin 6 where:

$$I_{pk} = \frac{\text{Pin 6 Threshold}}{R7}$$

Abnormal operating conditions occur when the preconverter is running at extremely low line or if output voltage sensing is lost. Under these conditions, the Current Sense Comparator threshold will be internally clamped to 1.5 V. Therefore, the maximum peak switch current is:

$$I_{pk(max)} = \frac{1.5\ V}{R7}$$

With the component values shown in Figure 15, the Current Sense Comparator threshold, at the peak of the haversine, varies from 110 mV at 90 Vac to 100 mV at 268 Vac. The Current Sense Input to Drive Output propagation delay is typically 200 ns.

Timer

A watchdog timer function was added to the IC to eliminate the need for an external oscillator when used in stand alone applications. The Timer provides a means to automatically start or restart the preconverter if the Drive Output has been off for more than 385 µs after the inductor current reaches zero.

Undervoltage Lockout and Quickstart

The MC33368 has a 5.0 V internal reference brought out to Pin 1 and capable of sourcing 10 mA typically. It also contains an Undervoltage Lockout (UVLO) circuit which suppresses the Gate output at Pin 11 if the V_{CC} supply voltage drops below 8.5 V typical.

A Quickstart circuit has been incorporated to optimize converter startup. During initial startup, compensation capacitor C1 will be discharged, holding the Error Amplifier output below the Multiplier's threshold. This will prevent Drive Output switching and delay bootstraping of capacitor C4 by diode D6. If Pin 4 does not reach the multiplier threshold before C4 discharges below the lower SMPS UVLO threshold, the converter will hiccup and experience a significant startup delay. The Quickstart circuit is designed to precharge C1 to 1.7 V. This level is slightly below the Pin 4 Multiplier threshold, allowing immediate Drive Output switching.

Restart Delay

A restart delay pin is provided to allow hiccup mode fault protection in case of a short circuit condition and to prevent the SMPS from repeatedly trying to restart after the input line voltage has been removed. When power is first applied, there is no startup delay, but subsequent cycling of the V_{CC} voltage will result in delay times that are programmed by an external resistor and capacitor. The Restart Delay, Pin 2, is a high impedance, so that an external capacitor can provide delay times as long as several seconds.

If the SMPS output is short circuited, the transformer winding, which provides the V_{CC} voltage to the control IC and the MC33368, will be unable to sustain V_{CC} to the control circuits. The restart delay capacitor at Pin 2 of the MC33368 prevents the high voltage startup transistor within the IC from maintaining the voltage on C4. After V_{CC} drops below the UVLO threshold in the SMPS, the SMPS switching transistors are held off for the time programmed by the values of the restart capacitor (C9) and resistor (R8). In this manner, the SMPS switching transistors are operated at very low duty cycles, preventing their destruction. If the short circuit fault is removed, the power supply system will turn on by itself in a normal startup mode after the restart delay has timed out.

Output Switching Frequency Clamp

In normal operation, the MC33368 operates the boost inductor in the critical mode. That is, the inductor current ramps to a peak value, ramps down to zero, then immediately begins ramping positive again. The peak current is programmed by the multiplier output within the IC. As the input voltage haversine declines to near zero, the output switch on–time becomes constant, rather than going to zero because of the small integrated dc voltage at Pin 5 caused by C2, R3 and R5. Because of this, the average line current does not exactly follow the line voltage near the zero crossings. The Output Switching Frequency Clamp remedies this situation to improve power factor and minimize EMI generated in this operating region. The values of R10 and C7 program a minimum off–time in the frequency clamp which overrides the zero current detect signal, forcing a minimum off–time. This allows discontinuous conduction operation of the boost inductor in the zero crossing region, and the average line current more nearly follows the voltage. The Output Switching Frequency Clamp function can be disabled by connecting the FC input, Pin 13, to the V_{CC} supply Pin 12.

Output

The IC contains a CMOS output driver that was specifically designed for direct drive of power MOSFETs. The Drive Output is capable of up to ±1500 mA peak current with a typical rise and fall time of 50 ns with a 1.0 nF load. Additional internal circuitry has been added to keep the Drive Output in a sinking mode whenever the Undervoltage Lockout is active. This characteristic eliminates the need for an external gate pull–down resistor. The totem–pole output has been optimized to minimize cross–conduction current during high speed operation.

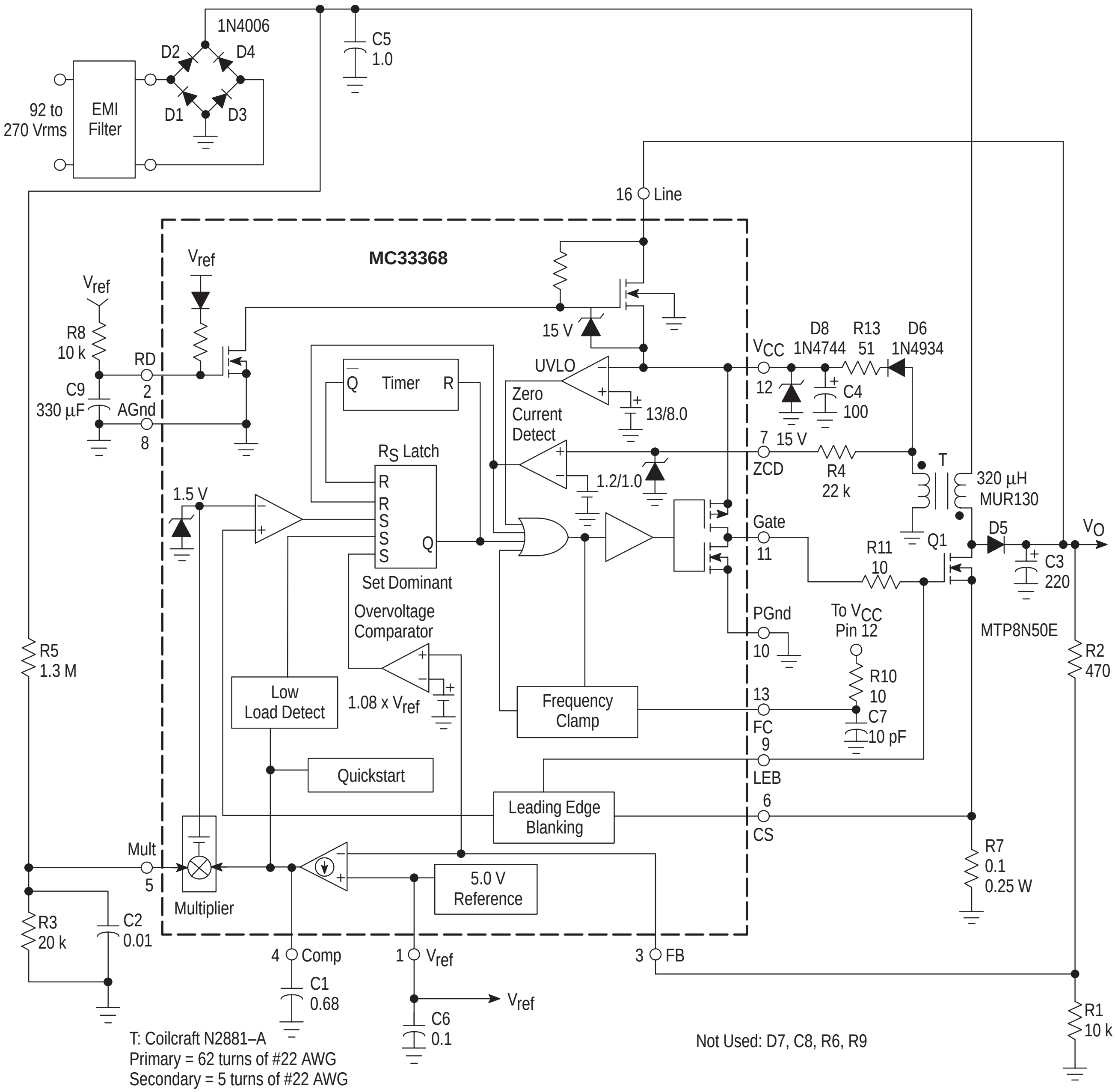
Table 1. Design Equations

Calculation	Formula	Notes
Converter Output Power	$P_O = V_O I_O$	Calculate the maximum required output power.
Peak Indicator Current	$I_{L(pk)} = \frac{2\sqrt{2}\ P_O}{\eta\ Vac_{(LL)}}$	Calculated at the minimum required ac line voltage for output regulation. Let the efficiency η = 0.92 for low line operation.
Inductance	$L_P = \frac{t\left(\frac{V_O}{\sqrt{2}} - Vac_{(LL)}\right)\eta\ Vac_{(LL)}{}^2}{\sqrt{2}\ V_O P_O}$	Let the switching cycle t = 40 µs for universal input (85 to 265 Vac) operation and 20 µs for fixed input (92 to 138 Vac, or 184 to 276 Vac) operation.
Switch On–Time	$t_{(on)} = \frac{2\ P_O L_P}{\eta\ Vac^2}$	In theory, the on–time $t_{(on)}$ is constant. In practice, $t_{(on)}$ tends to increase at the ac line zero crossings due to the charge on capacitor C5. Let Vac = $Vac_{(LL)}$ for initial $t_{(on)}$ and $t_{(off)}$ calculations.
Switch Off–Time	$t_{(off)} = \frac{t_{(on)}}{\frac{V_O}{\sqrt{2}\ Vac\ \lvert \mathrm{Sin}\ \theta \rvert} - 1}$	The off–time $t_{(off)}$ is greatest at the peak of the ac line voltage and approaches zero at the ac line zero crossings. Theta (0) represents the angle of the ac line voltage.
Minimum Switch Off–Time	$t_{(off)_{min}} = \frac{L_P I_{L(pk)}}{V_O}$	The off–time is at a minimum at ac line crossings. This equation is used to calculate $t_{(off)}$ as Theta approaches zero.
Delay Time	$t_d = -\ R10\ C7\ \ln\left(\frac{V_{CC} - 2}{V_{CC}}\right)$	The delay time is used to override the minimum off–time at the ac line zero crossings by programming the Frequency Clamp with C7 and R10.
Switching Frequency	$f = \frac{1}{t_{(on)} + t_{(off)}}$	The minimum switching frequency occurs at the peak of the ac line voltage. As the ac line voltage traverses from peak to zero, $t_{(off)}$ approaches zero producing an increase in switching frequency.
Peak Switch Current	$R7 = \frac{V_{CS}}{I_{L(pk)}}$	Set the current sense threshold V_{CS} to 1.0 V for universal input (85 to 265 Vac) operation and to 0.5 V for fixed input (92 to 138 Vac, or 184 to 276 Vac) operation. Note that V_{CS} must be less than 1.4 V.
Multiplier Input Voltage	$V_M = \frac{Vac\ \sqrt{2}}{\left(\frac{R5}{R3} + 1\right)}$	Set the mulltiplier input voltage V_M to 3.0 V at high line. Empirically adjust V_M for the lowest distortion over the ac line voltage range while guaranteeing startup at minimum line.
Converter Output Voltage	$V_O = V_{ref}\left(\frac{R2}{R1} + 1\right) - I_{IB}\ R1$	The I_{IB} R1 error term can be minimized with a divider current in excess of 100 µA.
Converter Output Peak–to–Peak Ripple Voltage	$\Delta V_{O(pp)} = I_{L(pk)}\sqrt{\left(\frac{1}{2\ \pi\ f_{ac}\ C3}\right)^2 + ESR^2}$	The calculated peak–to–peak ripple must be less than 16% of the average dc output voltage to prevent false tripping of the Overvoltage Comparator. Refer to the Overvoltage Comparator Text. ESR is the equivalent series resistance of C3.
Error Amplifier Bandwidth	$BW = \frac{g_m}{2\ \pi\ C1}$	The bandwidth is typically set to 20 Hz. When operating at high ac line, the value of C1 may need to be increased.

NOTE: The following converter characteristics must be chosen:

V_O = Desired output voltage.
I_O = Desired output current.
Vac = AC RMS operating line voltage.
$Vac_{(LL)}$ = AC RMS minimum required operating line voltage for output regulation.
ΔV_O = Converter output peak–to–peak ripple voltage.

Figure 15. 80 W Power Factor Controller



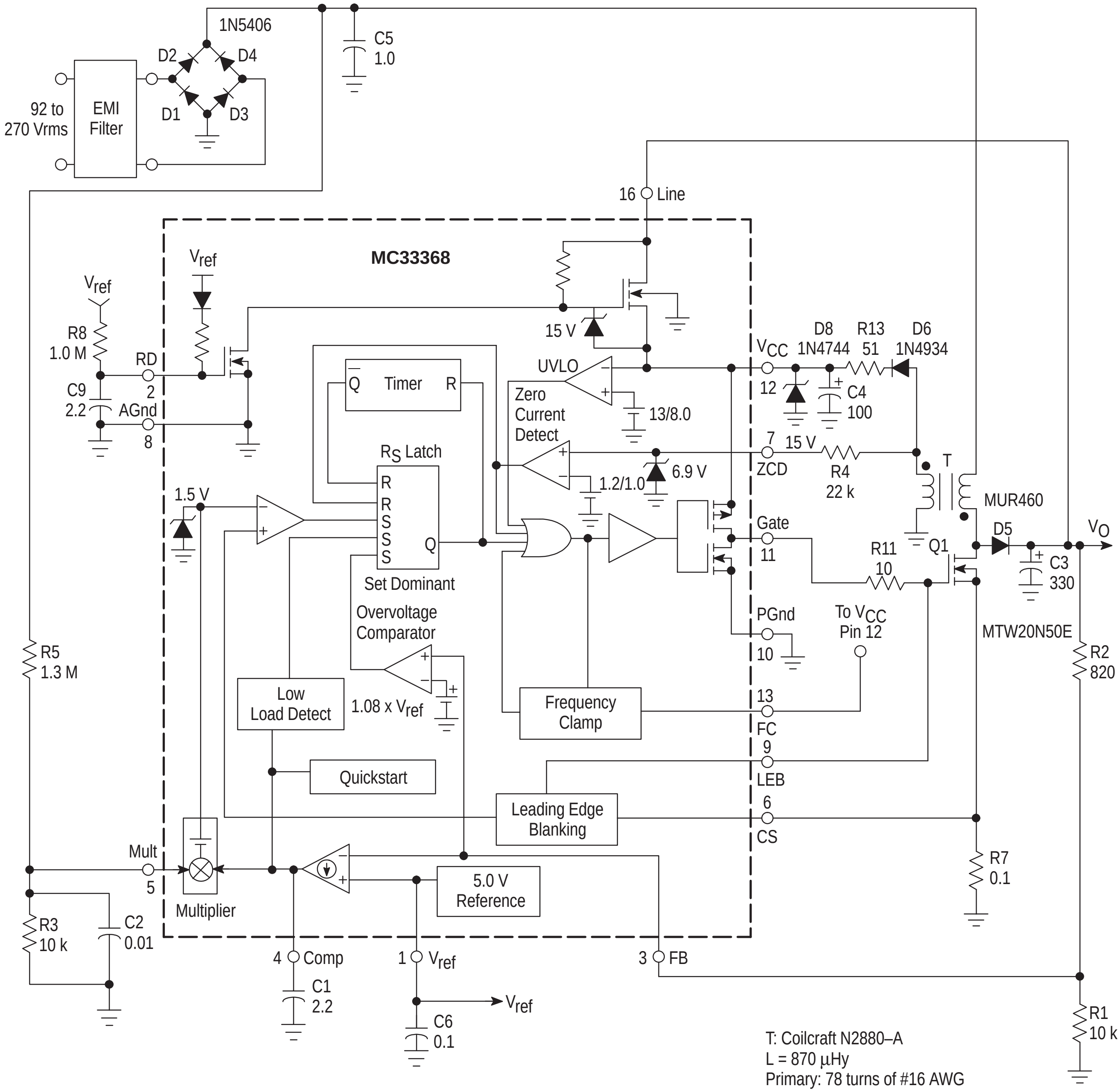
T: Coilcraft N2881–A
Primary = 62 turns of #22 AWG
Secondary = 5 turns of #22 AWG
Core = Coilcraft PT2510, EE25
Gap = 0.072″ total for a primary inductance (Lp) of 320 µH

Power Factor Controller Test Data

AC Line Input									DC Output				
				Current Harmonic Distortion (% I_{fund})									
V_{rms}	Pin	PF	I_{fund}	THD	2	3	5	7	$V_{O(pp)}$	V_O	I_O	P_O	n(%)
90	79.7	0.999	0.89	0.5	0.15	0.09	0.06	0.09	3.0	244.4	0.31	76.01	95.4
100	79.3	0.998	0.79	0.5	0.14	0.09	0.08	0.10	3.0	242.9	0.31	75.54	95.3
110	78.9	0.997	0.72	0.5	0.16	0.13	0.08	0.10	3.0	242.9	0.31	75.30	95.4
120	78.5	0.996	0.66	0.5	0.15	0.12	0.08	0.13	3.0	243.0	0.31	75.57	96.3
130	78.1	0.994	0.60	0.5	0.14	0.12	0.07	0.14	3.0	243.0	0.31	75.57	96.7
138	77.8	0.991	0.57	0.5	0.15	0.14	0.08	0.14	3.0	243.0	0.31	75.57	97.1

Heatsink = AAVID Engineering Inc., 590302B03600, or 593002B03400

Figure 16. 175 W Universal Input Power Factor Controller



Not Used: D7, C7, C8, R6, R9, R10

T: Coilcraft N2880–A
L = 870 µHy
Primary: 78 turns of #16 AWG
Secondary: 6 turns of #18 AWG
Core: Coilcraft PT4215, EE42–15
Gap: 0.104″ total

Power Factor Controller Test Data

AC Line Input									DC Output				
				Current Harmonic Distortion (% I_{fund})									
V_{rms}	Pin	PF	I_{fund}	THD	2	3	5	7	$V_{O(pp)}$	V_O	I_O	P_O	n(%)
90	190.4	0.995	2.11	5.8	0.16	0.32	0.24	0.80	3.6	398.0	0.44	175.9	92.4
120	192.1	0.997	1.60	3.2	0.08	0.17	0.07	0.30	3.6	398.9	0.44	177.1	92.2
138	192.7	0.997	1.40	0.9	0.08	0.24	0.03	0.15	3.6	402.3	0.45	179.0	92.9
180	194.3	0.995	1.08	0.9	0.04	0.18	0.04	0.08	3.6	409.1	0.45	182.9	94.1
240	189.3	0.983	0.80	0.7	0.08	0.21	0.08	0.06	3.6	407.0	0.45	181.1	95.7
268	186.3	0.972	0.71	0.6	0.11	0.32	0.10	0.10	3.6	406.2	0.44	180.4	96.8

Heatsink = AAVID Engineering Inc., 590302B03600

Figure 17. Power Factor Test Setup

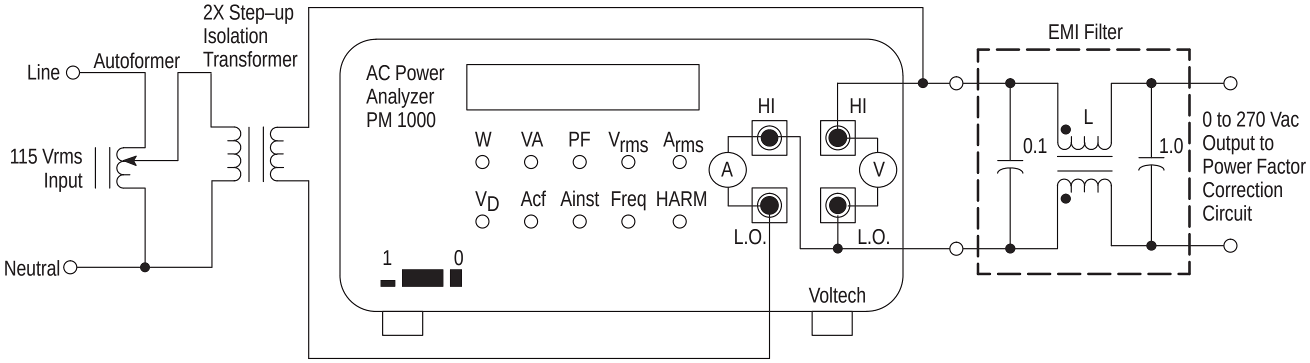


Figure 18. On/Off Control

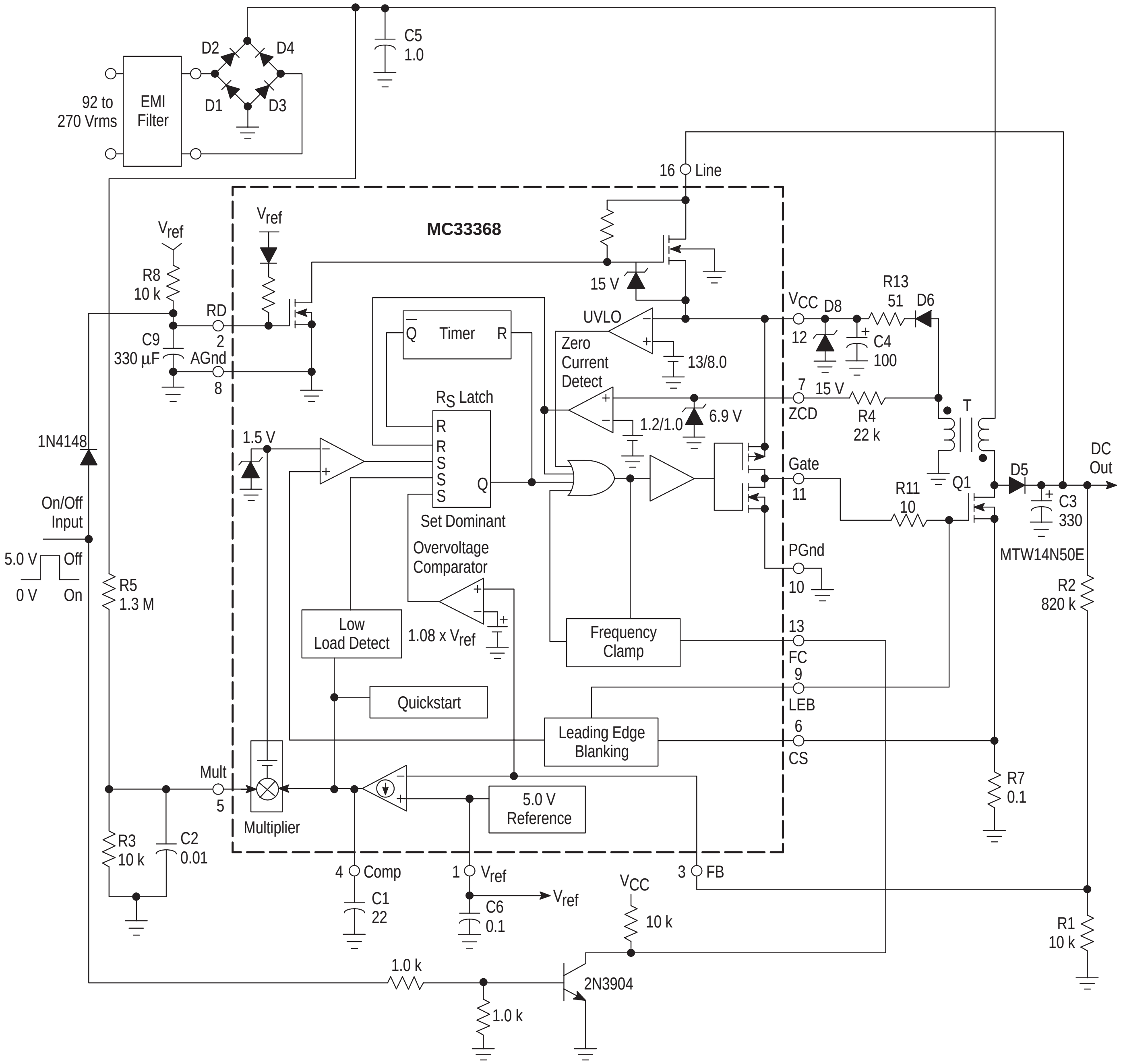
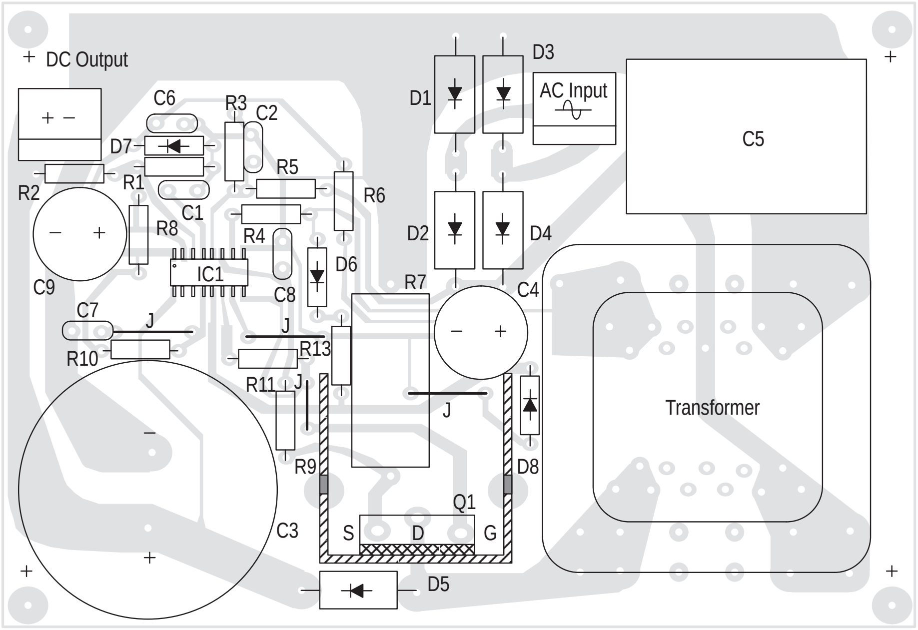
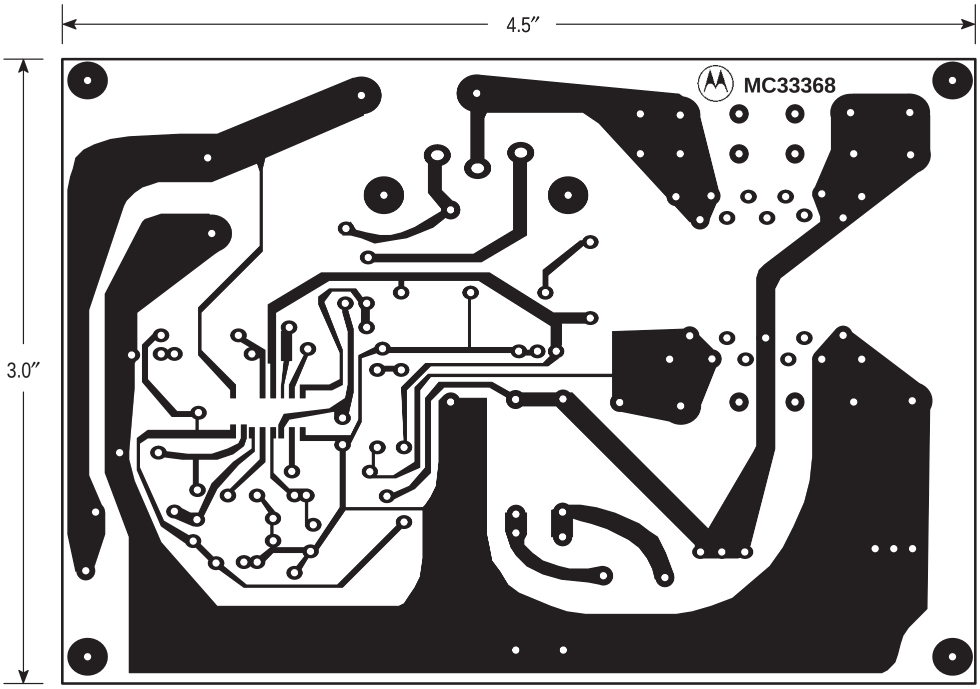


Figure 19. Printed Circuit Board and Component Layout (Circuits of Figures 15 and 16)



J = Jumper

(Top View)



(Bottom View)

MOTOROLA

MC33463

Product Preview

Variable Frequency Micropower DC-to-DC Converter

The MC33463 series are micropower switching voltage regulators, specifically designed for handheld and laptop applications, to provide regulated output voltages using a minimum of external parts. A wide choice of output voltages are available. These devices feature a very low quiescent bias current of 4.0 µA typical.

The MC33463H–XXLT1 series features a highly accurate voltage reference, an oscillator, a variable frequency modulation (VFM) controller, a driver transistor (Lx), an error amplifier and feedback resistive divider.

The MC33463H–XXLT1 is identical to the MC33463H–XXKT1, except that a drive pin (EXT) for an external transistor is provided.

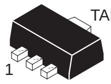
Due to the low bias current specifications, these devices are ideally suited for battery powered computer, consumer, and industrial equipment where an extension of useful battery life is desirable.

MC33463 Series Features:

- Low Quiescent Bias Current of 4.0 µA
- High Output Voltage Accuracy of ±2.5%
- Low Startup Voltage of 0.9 V at 1.0 mA
- Surface Mount Package

VARIABLE FREQUENCY MICROPOWER DC–to–DC CONVERTER

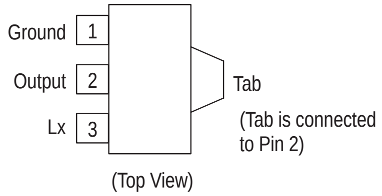
SEMICONDUCTOR TECHNICAL DATA



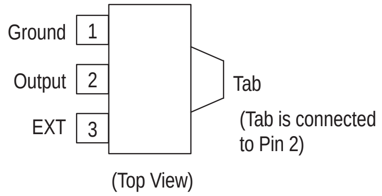
H SUFFIX
PLASTIC PACKAGE
CASE 1213
(SOT–89)

PIN CONNECTIONS

MC33463H–XXKT1



MC33463H–XXLT1



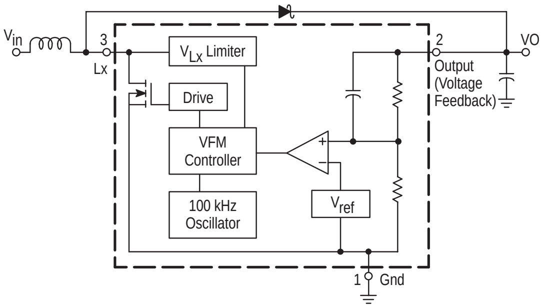
ORDERING INFORMATION

Device	Output Voltage	Type	Operating Temperature Range	Package (Tape/Reel)
MC33463H–30KT1 MC33463H–33KT1 MC33463H–50KT1	3.0 3.3 5.0	Int. Switch	T_A = –30° to +80°C	SOT–89 (Tape)
MC33463H–30LT1 MC33463H–33LT1 MC33463H–50LT1	3.0 3.3 5.0	Ext. Switch Drive		SOT–89 (Tape)

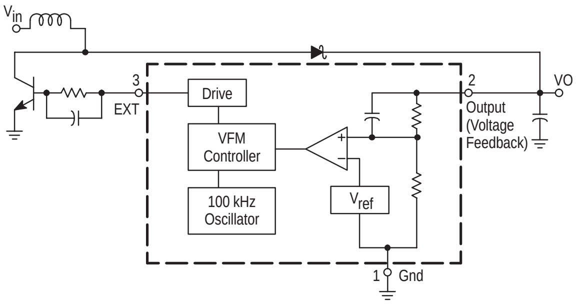
Other voltages from 2.5 V to 7.5 V, in 0.1 V increments are available upon request. Consult your local Motorola sales office for information.

Representative Block Diagram

MC33463H–XXKT1



MC33463H–XXLT1



This device contains 100 active transistors.

MOTOROLA

MC33464

Product Preview

Micropower Undervoltage Sensing Circuits

The MC33464 series are micropower undervoltage sensing circuits that are specifically designed for use with battery powered microprocessor based systems, where extended battery life is required. A choice of several threshold voltages from 0.9 V to 4.5 V are available. These devices feature a very low quiescent bias current of 0.8 µA typical.

The MC33464 series features a highly accurate voltage reference, a comparator with precise thresholds and built–in hysteresis to prevent erratic reset operation, a choice of output configurations between open drain or complementary MOS, and guaranteed operation below 1.0 V with extremely low standby current. These devices are available in either SOT–89 3–pin or SOT–23 5–pin surface mount packages.

Applications include direct monitoring of the MPU/logic power supply used in portable, appliance, automotive and industrial equipment.

MC33464 Features:

- Extremely Low Standby Current of 0.8 µA at V_{in} = 1.5 V
- Wide Input Voltage Range (0.7 V to 10 V)
- Monitors Power Supply Voltages from 1.1 V to 5.0 V
- High Accuracy Detector Threshold (±2.5%)
- Two $\overline{\text{Reset}}$ Output Types (Open Drain or Complementary Drive)
- Two Surface Mount Packages (SOT–89 or SOT–23 5–Pin)

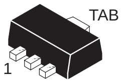
ORDERING INFORMATION

Device	Threshold Voltage	Type	Operating Temperature Range	Package (Qty/Reel)
MC33464H–09AT1	0.9	Open Drain $\overline{\text{Reset}}$	T_A = –30° to +80°C	SOT–89 (1000)
MC33464H–20AT1	2.0			
MC33464H–27AT1	2.7			
MC33464H–30AT1	3.0			
MC33464H–45AT1	4.5			
MC33464H–09CT1	0.9	Compl. MOS $\overline{\text{Reset}}$		
MC33464H–20CT1	2.0			
MC33464H–27CT1	2.7			
MC33464H–30CT1	3.0			
MC33464H–45CT1	4.5			
MC33464N–09ATR	0.9	Open Drain $\overline{\text{Reset}}$		SOT–23 (3000)
MC33464N–20ATR	2.0			
MC33464N–27ATR	2.7			
MC33464N–30ATR	3.0			
MC33464N–45ATR	4.5			
MC33464N–09CTR	0.9	Compl. MOS $\overline{\text{Reset}}$		
MC33464N–20CTR	2.0			
MC33464N–27CTR	2.7			
MC33464N–30CTR	3.0			
MC33464N–45CTR	4.5			

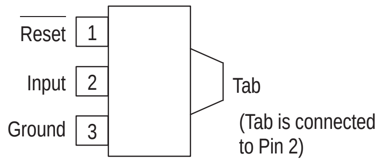
Other voltages from 0.9 to 6.0 V, in 0.1 V increments, are available upon request. Consult your local Motorola sales office for information.

MICROPOWER UNDERVOLTAGE SENSING CIRCUITS

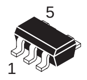
SEMICONDUCTOR TECHNICAL DATA



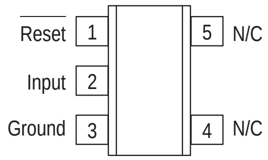
H SUFFIX
PLASTIC PACKAGE
CASE 1213
(SOT–89)



(Top View)



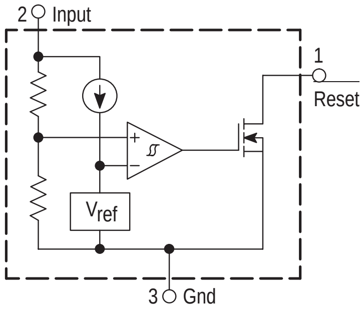
N SUFFIX
PLASTIC PACKAGE
CASE 1212
(SOT–23)



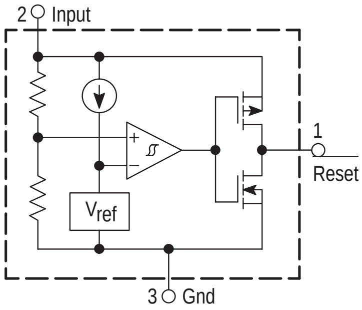
(Top View)

Representative Block Diagrams

MC33464X–YYATZ
Open Drain Configuration



MC33464X–YYCTZ
Complementary Drive Configuration



X Denotes Package Type
YY Denotes Threshold Voltage
TZ Denotes Taping Type

This device contains 25 active transistors.

MOTOROLA

MC33465

Product Preview

Micropower Undervoltage Sensing Circuits with Output Delay

MICROPOWER UNDERVOLTAGE SENSING CIRCUITS WITH OUTPUT DELAY

SEMICONDUCTOR TECHNICAL DATA

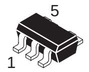
The MC33465 series are micropower undervoltage sensing circuits that are specifically designed for use with battery powered microprocessor based systems, where extended battery life is required. A choice of several threshold voltages from 0.9 V to 4.5 V are available. This device features a very low quiescent bias current of 1.0 µA typical.

The MC33465 series features a highly accurate voltage reference, a comparator with precise thresholds and built–in hysteresis to prevent erratic reset operation, a choice of output configurations between open drain or complementary MOS, a time delayed output, which can be programmed by the system designer, and guaranteed operation below 1.0 V with extremely low standby current. This device is available in a SOT–23 5–pin surface mount packages.

Applications include direct monitoring of the MPU/logic power supply used in portable, appliance, automotive and industrial equipment.

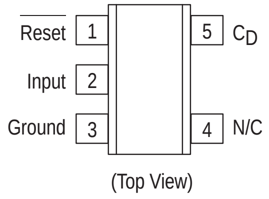
MC33465 Features:

- Extremely Low Standby Current of 1.0 µA at V_{in} = 3.5 V
- Wide Input Voltage Range (0.7 V to 10 V)
- Monitors Power Supply Voltages from 1.1 V to 5.0 V
- High Accuracy Detector Threshold (±2.5%)
- Two Reset Output Types (Open Drain or Complementary Drive)
- Programmable Output Delay by External Capacitor (100 ms typ. with 0.15 µF)
- Surface Mount Package (SOT–23 5–Pin)
- Convenient Tape and Reel (3000 per Reel)



N SUFFIX
PLASTIC PACKAGE
CASE 1212
(SOT–23)

PIN CONNECTIONS



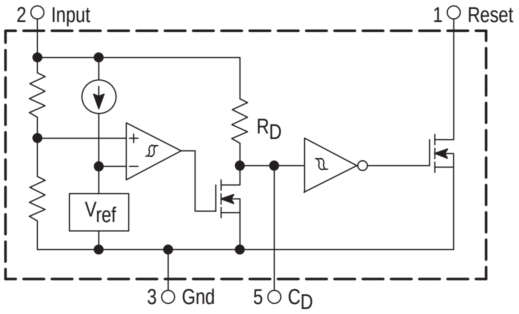
ORDERING INFORMATION

Device	Threshold Voltage	Type	Operating Temperature Range	Package
MC33465N–09ATR	0.9	Open Drain Reset	T_A = –30° to +80°C	SOT–23
MC33465N–20ATR	2.0			
MC33465N–27ATR	2.7			
MC33465N–30ATR	3.0			
MC33465N–45ATR	4.5			
MC33465N–09CTR	0.9	Compl. MOS Reset		
MC33465N–20CTR	2.0			
MC33465N–27CTR	2.7			
MC33465N–30CTR	3.0			
MC33465N–45CTR	4.5			

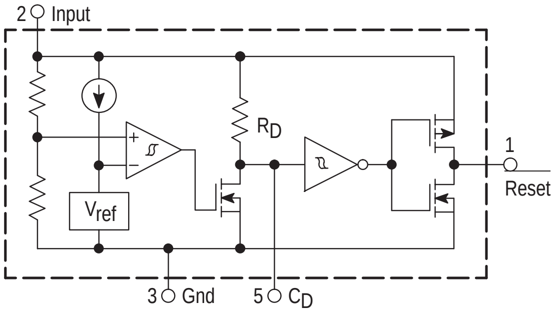
Other voltages from 0.9 to 6.0 V, in 0.1 V increments, are available upon request. Consult your local Motorola sales office for information.

Representative Block Diagrams

MC33465N–YYATZ
Open Drain Configuration



MC33465N–YYCTZ
Complementary Drive Configuration



YY Denotes Threshold Voltage
TZ Denotes Taping Type

This device contains 28 active transistors.

MOTOROLA

MC33466

Product Preview

Fixed Frequency PWM Micropower DC-to-DC Converter

The MC33466 series are micropower switching voltage regulators, specifically designed for handheld and laptop applications, to provide regulated output voltages using a minimum of external parts. A wide choice of output voltages are available. These devices feature a very low quiescent bias current of 15 µA typical.

The MC33466H–XXJT1 series features a highly accurate voltage reference, an oscillator, a pulse width modulation (PWM) controller, a driver transistor (Lx), an error amplifier and feedback resistive divider.

The MC33466H–XXLT1 is identical to the MC33466H–XXJT1, except that a drive pin (EXT) for an external transistor is provided.

Due to the low bias current specifications, these devices are ideally suited for battery powered computer, consumer, and industrial equipment where an extension of useful battery life is desirable.

MC33466 Series Features:

- Low Quiescent Bias Current of 15 µA
- High Output Voltage Accuracy of ±2.5%
- Low Startup Voltage of 0.9 V at 1.0 mA
- Soft–Start = 500 µs
- Surface Mount Package

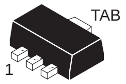
ORDERING INFORMATION

Device	Output Voltage	Type	Operating Temperature Range	Package (Tape/Reel)
MC33466H–30JT1	3.0	Int. Switch	T_A = –30° to +80°C	SOT–89 (Tape)
MC33466H–33JT1	3.3			
MC33466H–50JT1	5.0			
MC33466H–30LT1	3.0	Ext. Switch Drive		SOT–89 (Tape)
MC33466H–33LT1	3.3			
MC33466H–50LT1	5.0			

Other voltages from 2.5 V to 7.5 V, in 0.1 V increments are available upon request. Consult your local Motorola sales office for information.

FIXED FREQUENCY PWM MICROPOWER DC–to–DC CONVERTER

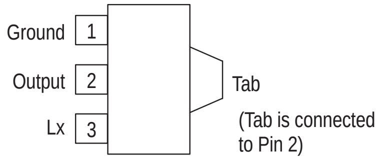
SEMICONDUCTOR TECHNICAL DATA



H SUFFIX
PLASTIC PACKAGE
CASE 1213
(SOT–89)

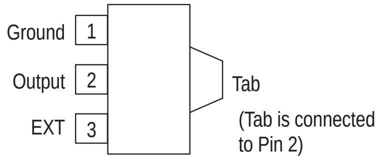
PIN CONNECTIONS

MC33466H–XXJT1



(Top View)

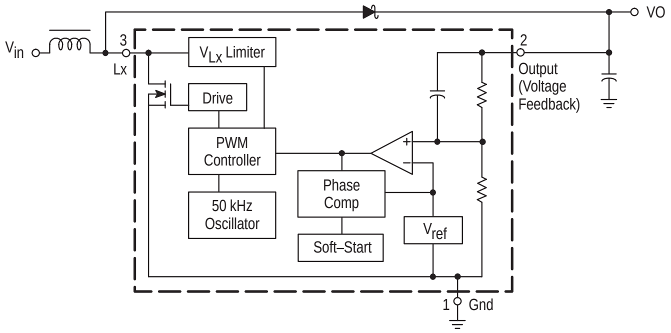
MC33466H–XXLT1



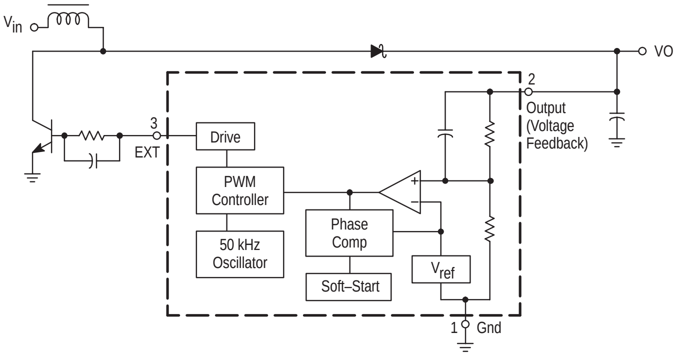
(Top View)

Representative Block Diagram

MC33466H–XXJT1



MC33466H–XXLT1



This device contains 100 active transistors.

MOTOROLA

MC34023
MC33023

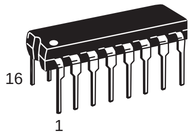
High Speed Single-Ended PWM Controller

The MC34023 series are high speed, fixed frequency, single–ended pulse width modulator controllers optimized for high frequency operation. They are specifically designed for Off–Line and DC–to–DC converter applications offering the designer a cost–effective solution with minimal external components. These integrated circuits feature an oscillator, a temperature compensated reference, a wide bandwidth error amplifier, a high speed current sensing comparator, and a high current totem pole output ideally suited for driving a power MOSFET.

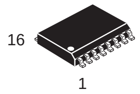
Also included are protective features consisting of input and reference undervoltage lockouts each with hysteresis, cycle–by–cycle current limiting, and a latch for single pulse metering.

The flexibility of this series allows it to be easily configured for either current mode or voltage mode control.

- 50 ns Propagation Delay to Output
- High Current Totem Pole Output
- Wide Bandwidth Error Amplifier
- Fully–Latched Logic with Double Pulse Suppression
- Latching PWM for Cycle–By–Cycle Current Limiting
- Soft–Start Control with Latched Overcurrent Reset
- Input Undervoltage Lockout with Hysteresis
- Low Start–Up Current (500 µA Typ)
- Internally Trimmed Reference with Undervoltage Lockout
- 90% Maximum Duty Cycle (Externally Adjustable)
- Precision Trimmed Oscillator
- Voltage or Current Mode Operation to 1.0 MHz
- Functionally Similar to the UC3823

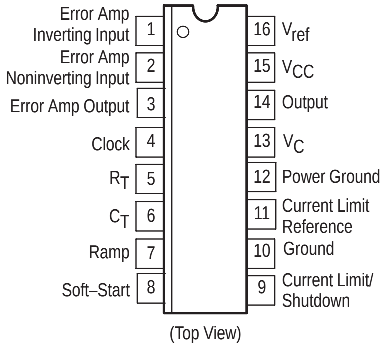


P SUFFIX
PLASTIC PACKAGE
CASE 648

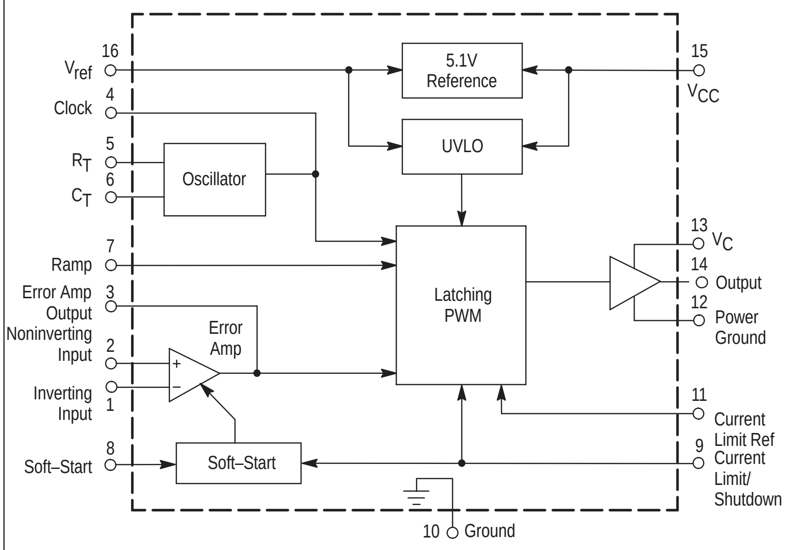


DW SUFFIX
PLASTIC PACKAGE
CASE 751G
(SO–16L)

PIN CONNECTIONS



Simplified Application



This device contains 176 active transistors.

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC33023P	T_A = –40° to +105°C	Plastic DIP
MC33023DW		SO–16L
MC34023P	T_A = 0° to +70°C	Plastic DIP

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	30	V
Output Driver Supply Voltage	V_C	20	V
Output Current, Source or Sink (Note 1) DC Pulsed (0.5 µs)	I_O	 0.5 2.0	A
Current Sense, Soft–Start, Ramp, and Error Amp Inputs	V_{in}	–0.3 to +7.0	V
Error Amp Output and Soft–Start Sink Current	I_O	10	mA
Clock and R_T Output Current	I_{CO}	5.0	mA
Power Dissipation and Thermal Characteristics SO–16L Package (Case 751G) Maximum Power Dissipation @ T_A = +25°C Thermal Resistance, Junction–to–Air DIP Package (Case 648) Maximum Power Dissipation @ T_A = +25°C Thermal Resistance, Junction–to–Air	 P_D $R_{\theta JA}$ P_D $R_{\theta JA}$	 862 145 1.25 100	 mW °C/W W °C/W
Operating Junction Temperature	T_J	+150	°C
Operating Ambient Temperature (Note 2) MC34023 MC33023	T_A	 0 to +70 –40 to +105	°C
Storage Temperature Range	T_{stg}	–55 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V, R_T = 3.65 kΩ, C_T = 1.0 nF, for typical values T_A = +25°C, for min/max values T_A is the operating ambient temperature range that applies [Note 2], unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
REFERENCE SECTION					
Reference Output Voltage (I_O = 1.0 mA, T_J = +25°C)	V_{ref}	5.05	5.1	5.15	V
Line Regulation (V_{CC} = 10 V to 30 V)	Reg_{line}	–	2.0	15	mV
Load Regulation (I_O = 1.0 mA to 10 mA)	Reg_{load}	–	2.0	15	mV
Temperature Stability	T_S	–	0.2	–	mV/°C
Total Output Variation over Line, Load, and Temperature	V_{ref}	4.95	–	5.25	V
Output Noise Voltage (f = 10 Hz to 10 kHz, T_J = +25°C)	V_n	–	50	–	µV
Long Term Stability (T_A = +125°C for 1000 Hours)	S	–	5.0	–	mV
Output Short Circuit Current	I_{SC}	– 30	– 65	–100	mA
OSCILLATOR SECTION					
Frequency T_J = +25°C Line (V_{CC} = 10 V to 30 V) and Temperature (T_A = T_{low} to T_{high})	f_{osc}	 380 370	 400 400	 420 430	kHz
Frequency Change with Voltage (V_{CC} = 10 V to 30 V)	$\Delta f_{osc}/\Delta V$	–	0.2	1.0	%
Frequency Change with Temperature (T_A = T_{low} to T_{high})	$\Delta f_{osc}/\Delta T$	–	2.0	–	%
Sawtooth Peak Voltage	$V_{OSC(P)}$	2.6	2.8	3.0	V
Sawtooth Valley Voltage	$V_{OSC(V)}$	0.7	1.0	1.25	V
Clock Output Voltage High State Low State	 V_{OH} V_{OL}	 3.9 –	 4.5 2.3	 – 2.9	V

NOTES: 1. Maximum package power dissipation limits must be observed.
2. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
T_{low} = 0°C for MC34023 T_{high} = +70°C for MC34023
= –40°C for MC33023 = +105°C for MC33023

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V, R_T = 3.65 kΩ, C_T = 1.0 nF, for typical values T_A = +25°C, for min/max values T_A is the operating ambient temperature range that applies [Note 2], unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
ERROR AMPLIFIER SECTION					
Input Offset Voltage	V_{IO}	–	–	15	mV
Input Bias Current	I_{IB}	–	0.6	3.0	µA
Input Offset Current	I_{IO}	–	0.1	1.0	µA
Open–Loop Voltage Gain (V_O = 1.0 V to 4.0 V)	A_{VOL}	60	95	–	dB
Gain Bandwidth Product (T_J = +25°C)	GBW	4.0	8.3	–	MHz
Common Mode Rejection Ratio (V_{CM} = 1.5 V to 5.5 V)	CMRR	75	95	–	dB
Power Supply Rejection Ratio (V_{CC} = 10 V to 30 V)	PSRR	85	110	–	dB
Output Current, Source (V_O = 4.0 V)	I_{Source}	0.5	3.0	–	mA
Sink (V_O = 1.0 V)	I_{Sink}	1.0	3.6	–	
Output Voltage Swing, High State (I_O = –0.5 mA)	V_{OH}	4.5	4.75	5.0	V
Low State (I_O = 1 mA)	V_{OL}	0	0.4	1.0	
Slew Rate	SR	6.0	12	–	V/µs
PWM COMPARATOR SECTION					
Ramp Input Bias Current	I_{IB}	–	–0.5	–5.0	µA
Duty Cycle, Maximum	$DC_{(max)}$	80	90	–	%
Minimum	$DC_{(min)}$	–	–	0	
Zero Duty Cycle Threshold Voltage Pin 3(4) (Pin 7(9) = 0 V)	V_{th}	1.1	1.25	1.4	V
Propagation Delay (Ramp Input to Output, T_J = +25°C)	$t_{PLH(in/out)}$	–	60	100	ns
SOFT–START SECTION					
Charge Current ($V_{Soft–Start}$ = 0.5 V)	I_{chg}	3.0	9.0	20	µA
Discharge Current ($V_{Soft–Start}$ = 1.5 V)	I_{dischg}	1.0	4.0	–	mA
CURRENT SENSE SECTION					
Input Bias Current (Pin 9(12) = 0 V to 4.0 V)	I_{IB}	–	–	15	µA
Current Limit Comparator Input Offset Voltage (Pin 11(14) = 1.1 V)	V_{IO}	–	–	45	mV
Current Limit Reference Input Common Mode Range (Pin 11(14))	V_{CMR}	1.0	–	1.25	V
Shutdown Comparator Threshold	V_{th}	1.25	1.40	1.55	V
Propagation Delay (Current Limit/Shutdown to Output, T_J = +25°C)	$t_{PLH(in/out)}$	–	50	80	ns
OUTPUT SECTION					
Output Voltage					V
Low State (I_{Sink} = 20 mA)	V_{OL}	–	0.25	0.4	
(I_{Sink} = 200 mA)		–	1.2	2.2	
High State (I_{Source} = 20 mA)	V_{OH}	13	13.5	–	
(I_{Source} = 200 mA)		12	13	–	
Output Voltage with UVLO Activated (V_{CC} = 6.0 V, I_{Sink} = 0.5 mA)	$V_{OL(UVLO)}$	–	0.25	1.0	V
Output Leakage Current (V_C = 20 V)	I_L	–	100	500	µA
Output Voltage Rise Time (C_L = 1.0 nF, T_J = +25°C)	t_r	–	30	60	ns
Output Voltage Fall Time (C_L = 1.0 nF, T_J = +25°C)	t_f	–	30	60	ns
UNDERVOLTAGE LOCKOUT SECTION					
Start–Up Threshold (V_{CC} Increasing)	$V_{th(on)}$	8.8	9.2	9.6	V
UVLO Hysteresis Voltage (V_{CC} Decreasing After Turn–On)	V_H	0.4	0.8	1.2	V
TOTAL DEVICE					
Power Supply Current	I_{CC}				mA
Start–Up (VCC = 8.0 V)		–	0.5	1.2	
Operating		–	20	30	

NOTES: 1. Maximum package power dissipation limits must be observed.
2. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
T_{low} = 0°C for MC34023 T_{high} = +70°C for MC34023
= –40°C for MC33023 = +105°C for MC33023

Figure 1. Timing Resistor versus Oscillator Frequency

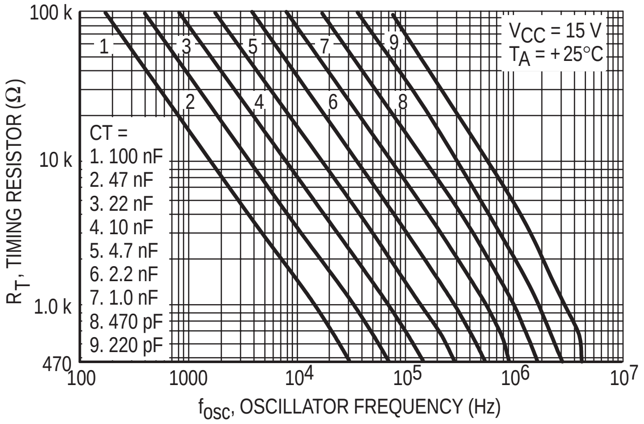


Figure 2. Oscillator Frequency versus Temperature

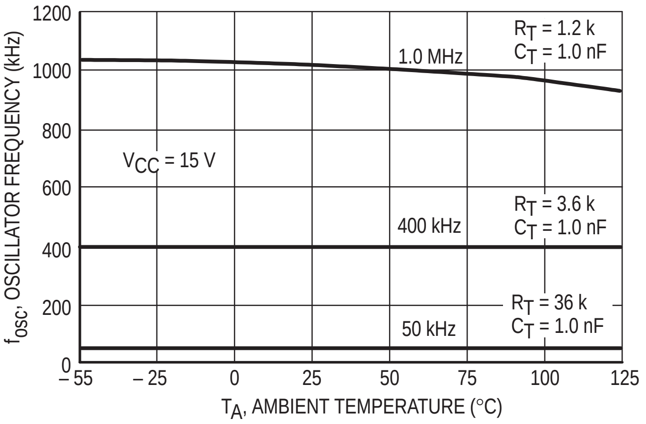


Figure 3. Error Amp Open Loop Gain and Phase versus Frequency

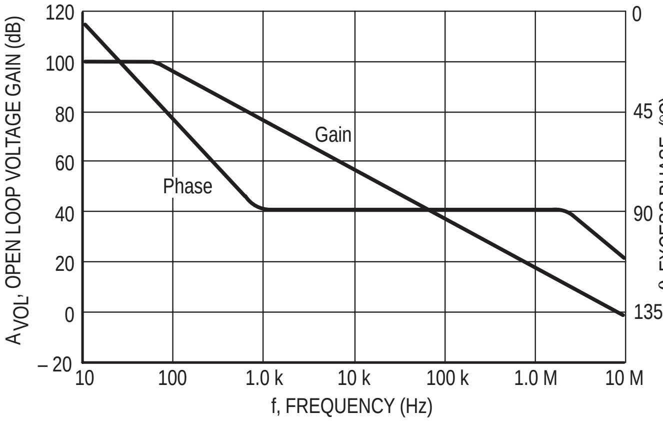


Figure 4. PWM Comparator Zero Duty Cycle Threshold Voltage versus Temperature

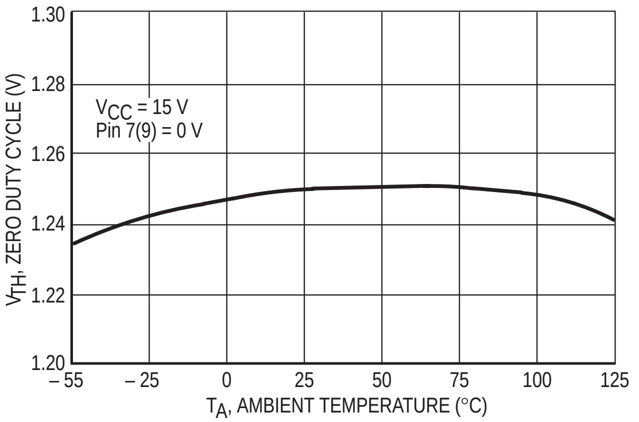


Figure 5. Error Amp Small Signal Transient Response

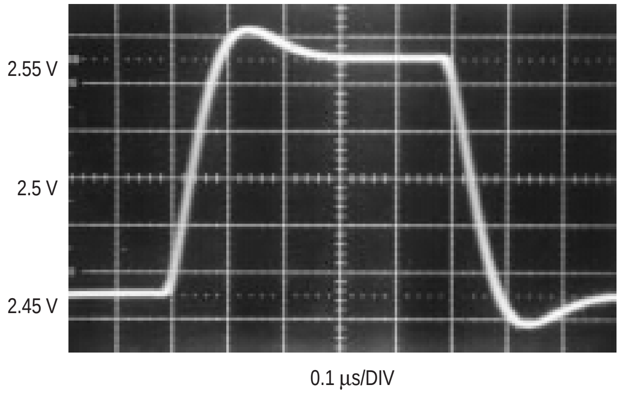


Figure 6. Error Amp Large Signal Transient Response

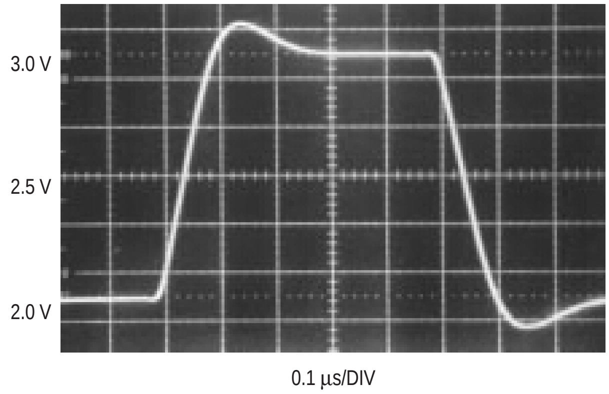


Figure 7. Reference Voltage Change versus Source Current

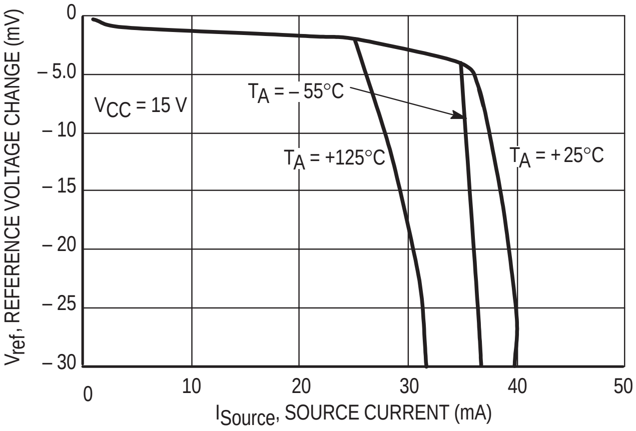


Figure 8. Reference Short Circuit Current versus Temperature

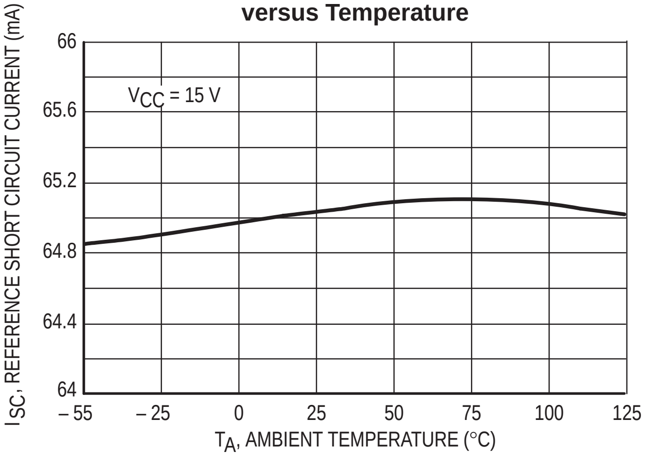
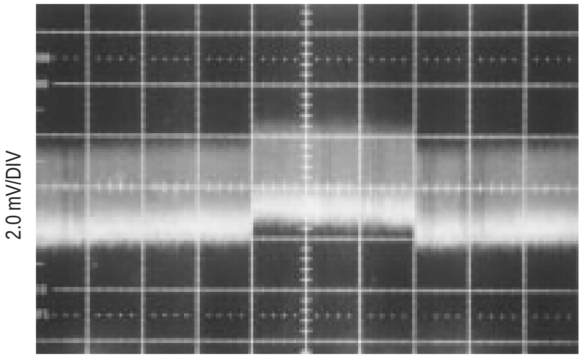
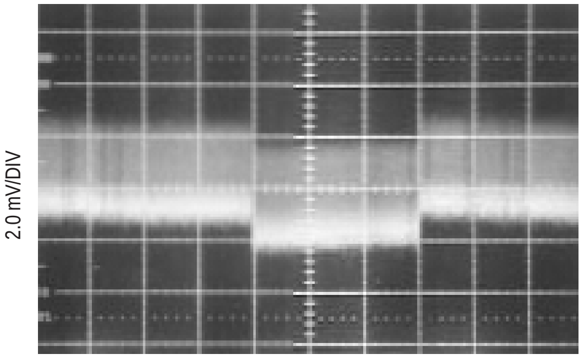


Figure 9. Reference Line Regulation



V_{ref} LINE REGULATION 10 V to 24 V
(2.0 ms/DIV)

Figure 10. Reference Load Regulation



V_{ref} LOAD REGULATION 1.0 mA to 10 mA
(2.0 ms/DIV)

Figure 11. Current Limit Comparator Input Offset Voltage versus Temperature

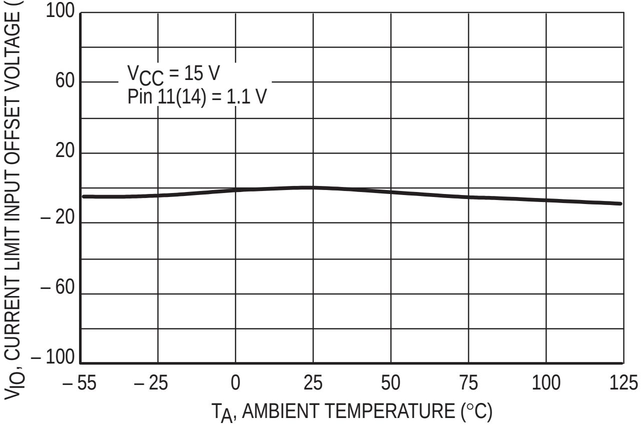


Figure 12. Shutdown Comparator Threshold Voltage versus Temperature

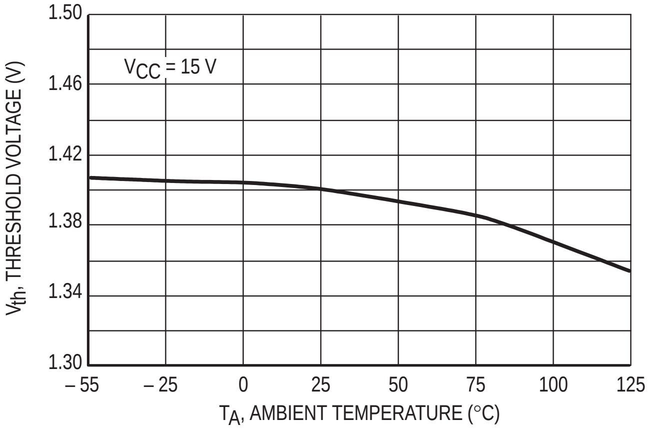


Figure 13. Soft–Start Charge Current versus Temperature

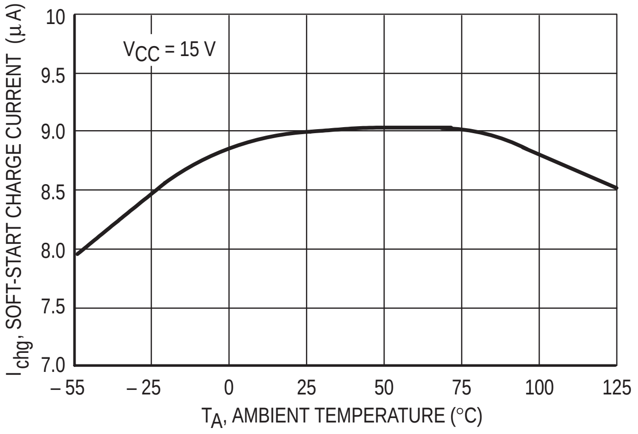


Figure 14. Output Saturation Voltage versus Load Current

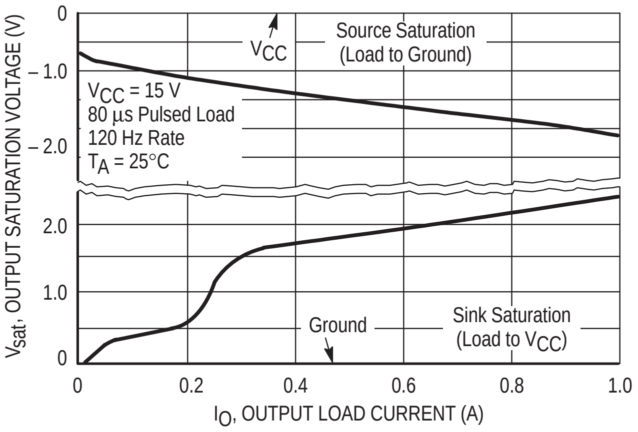
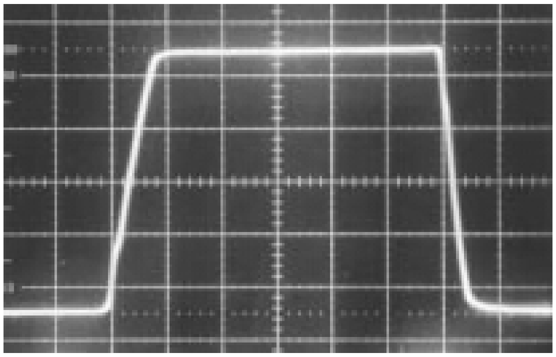
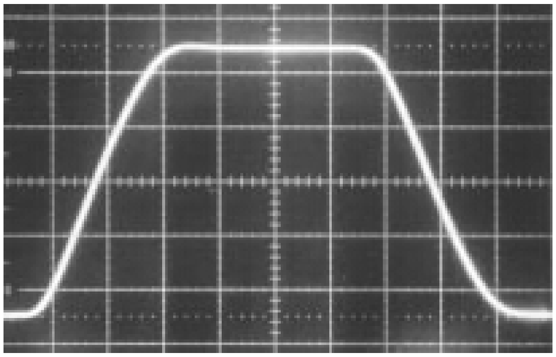


Figure 15. Drive Output Rise and Fall Time



OUTPUT RISE & FALL TIME 1.0 nF LOAD
50 ns/DIV

Figure 16. Drive Output Rise and Fall Time



OUTPUT RISE & FALL TIME 10 nF LOAD
50 ns/DIV

Figure 17. Supply Voltage versus Supply Current

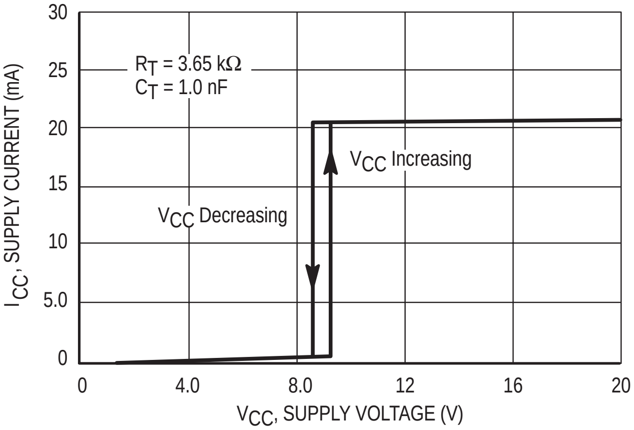


Figure 18. Representative Block Diagram

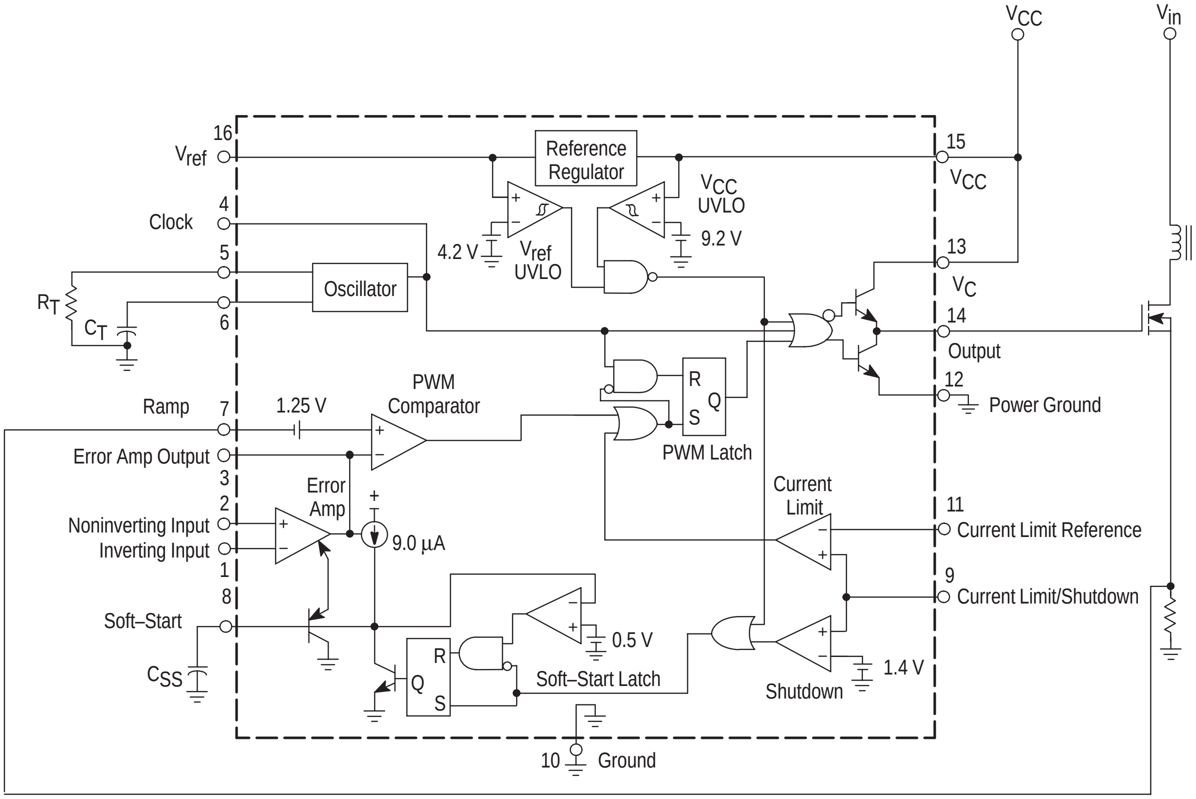
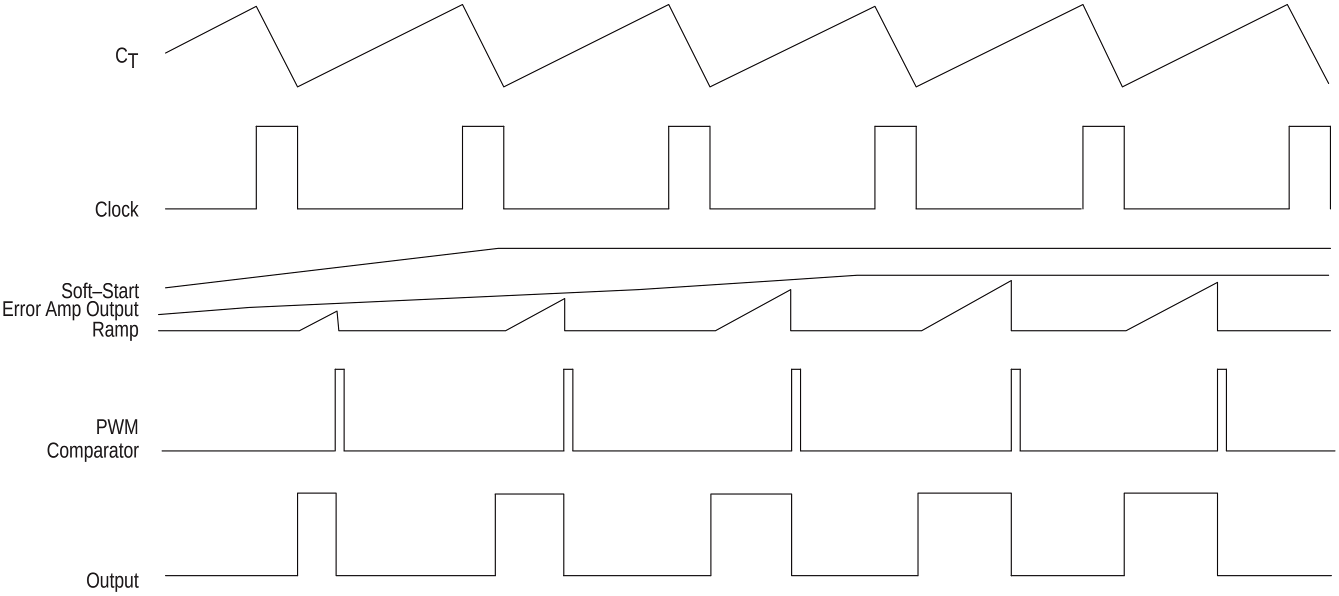


Figure 19. Current Limit Operating Waveforms



OPERATING DESCRIPTION

The MC33023 and MC34023 series are high speed, fixed frequency, single–ended pulse width modulator controllers optimized for high frequency operation. They are specifically designed for Off–Line and DC–to–DC converter applications offering the designer a cost effective solution with minimal external components. A representative block diagram is shown in Figure 18.

Oscillator

The oscillator frequency is programmed by the values selected for the timing components R_T and C_T. The R_T pin is set to a temperature compensated 3.0 V. By selecting the value of R_T, the charge current is set through a current mirror for the timing capacitor C_T. This charge current runs continuously through C_T. The discharge current is ratioed to be 10 times the charge current, which yields the maximum duty cycle of 90%. C_T is charged to 2.8 V and discharged to 1.0 V. During the discharge of C_T, the oscillator generates an internal blanking pulse that resets the PWM Latch and, inhibits the outputs. The threshold voltage on the oscillator comparator is trimmed to guarantee an oscillator accuracy of 5.0% at 25°C.

Additional dead time can be added by externally increasing the charge current to C_T as shown in Figure 23. This changes the charge to discharge ratio of C_T which is set internally to $I_{charge}/10\ I_{charge}$. The new charge to discharge ratio will be:

$$\%\ \text{Deadtime} = \frac{I_{additional} + I_{charge}}{10\ (I_{charge})}$$

A bidirectional clock pin is provided for synchronization or for master/slave operation. As a master, the clock pin provides a positive output pulse during the discharge of C_T. As a slave, the clock pin is an input that resets the PWM latch and blanks the drive output, but does not discharge C_T. Therefore, the oscillator is not synchronized by driving the clock pin alone. Figures 27, 28 and 29 provide suggested synchronization.

Error Amplifier

A fully compensated Error Amplifier is provided. It features a typical DC voltage gain of 95 dB and a gain bandwidth product of 8.3 MHz with 75 degrees of phase margin (Figure 3). Typical application circuits will have the noninverting input tied to the reference. The inverting input will typically be connected to a feedback voltage generated from the output of the switching power supply. Both inputs have a common mode voltage (V_{CM}) input range of 1.5 V to 5.5 V. The Error Amplifier Output is provided for external loop compensation.

Soft–Start Latch

Soft–Start is accomplished in conjunction with an external capacitor. The Soft–Start capacitor is charged by an internal 9.0 µA current source. This capacitor clamps the output of the error amplifier to less than its normal output voltage, thus limiting the duty cycle. The time it takes for a capacitor to reach full charge is given by:

$$t \approx (4.5 \bullet 10^5)\ C_{Soft\text{-}Start}$$

A Soft–Start latch is incorporated to prevent erratic operation of this circuitry. Two conditions can cause the Soft–Start circuit to latch so that the Soft–Start capacitor stays discharged. The first condition is activation of an undervoltage lockout of either V_{CC} or V_{ref}. The second condition is when current sense input exceeds 1.4 V. Since this latch is “set dominant”, it cannot be reset until either of these signals is removed and, the voltage at $C_{Soft–Start}$ is less than 0.5 V.

PWM Comparator and Latch

A PWM circuit typically compares an error voltage with a ramp signal. The outcome of this comparison determines the state of the output. In voltage mode operation the ramp signal is the voltage ramp of the timing capacitor. In current mode operation the ramp signal is the voltage ramp induced in a current sensing element. The ramp input of the PWM comparator is pinned out so that the user can decide which mode of operation best suits the application requirements. The ramp input has a 1.25 V offset such that whenever the voltage at this pin exceeds the error amplifier output voltage minus 1.25 V, the PWM comparator will cause the PWM latch to set, disabling the outputs. Once the PWM latch is set, only a blanking pulse by the oscillator can reset it, thus initiating the next cycle.

Current Limiting and Shutdown

A pin is provided to perform current limiting and shutdown operations. Two comparators are connected to the input of this pin. The reference voltage for the current limit comparator is not set internally. A pin is provided so the user can set the voltage. When the voltage at the current limit input pin exceeds the externally set voltage, the PWM latch is set, disabling the output. In this way cycle–by–cycle current limiting is accomplished. If a current limit resistor is used in series with the power devices, the value of the resistor is found by:

$$R_{Sense} = \frac{I_{Limit\ Reference\ Voltage}}{I_{pk\ (switch)}}$$

If the voltage at this pin exceeds 1.4 V, the second comparator is activated. This comparator sets a latch which, in turn, causes the soft start capacitor to be discharged. In this way a “hiccup” mode of recovery is possible in the case of output short circuits. If a current limit resistor is used in series with the output devices, the peak current at which the controller will enter a “hiccup” mode is given by:

$$I_{shutdown} = \frac{1.4\ V}{R_{Sense}}$$

Undervoltage Lockout

There are two undervoltage lockout circuits within the IC. The first senses V_{CC} and the second V_{ref}. During power–up, V_{CC} must exceed 9.2 V and V_{ref} must exceed 4.2 V before the outputs can be enabled and the Soft–Start latch released. If V_{CC} falls below 8.4 V or V_{ref} falls below 3.6 V, the outputs are disabled and the Soft–Start latch is activated. When the UVLO is active, the part is in a low current standby mode allowing the IC to have an off–line bootstrap start–up circuit. Typical start–up current is 500 µA.

Output

The MC34023 has a high current totem pole output specifically designed for direct drive of power MOSFETs. It is capable of up to ± 2.0 A peak drive current with a typical rise and fall time of 30 ns driving a 1.0 nF load.

Separate pins for V_C and Power Ground are provided. With proper implementation, a significant reduction of switching transient noise imposed on the control circuitry is possible. The separate V_C supply input also allows the designer added flexibility in tailoring the drive voltage independent of V_{CC}.

Reference

A 5.1 V bandgap reference is pinned out and is trimmed to an initial accuracy of ±1.0% at 25°C. This reference has short circuit protection and can source in excess of 10 mA for powering additional control system circuitry.

Design Considerations

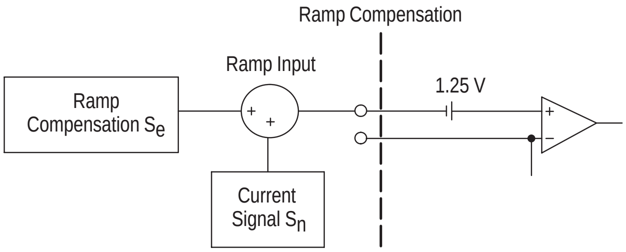
Do not attempt to construct the converter on wire–wrap or plug–in prototype boards. With high frequency, high power, switching power supplies it is imperative to have separate current loops for the signal paths and for the power paths. The printed circuit layout should contain a ground plane with low current signal and high current switch and output grounds returning on separate paths back to the input filter capacitor. Shown in Figure 35 is a printed circuit layout of the application circuit. Note how the power and ground traces are run. All bypass capacitors and snubbers should be connected as close as possible to the specific part in question. The PC board lead lengths must be less than 0.5 inches for effective bypassing for snubbing.

Instabilities

In current mode control, an instability can be encountered at any given duty cycle. The instability is caused by the current feedback loop. It has been shown that the instability is caused by a double pole at half the switching frequency. If an external ramp (S_e) is added to the on–time ramp (S_n) of the current–sense waveform, stability can be achieved.

One must be careful not to add too much ramp compensation. If too much is added the system will start to perform like a voltage mode regulator. All benefits of current mode control will be lost. Figure 25 is an example of one way in which external ramp compensation can be implemented.

Figure 20. Ramp Compensation



A simple equation can be used to calculate the amount of external ramp slope necessary to add that will achieve stability in the current loop. For the following equations, the calculated values for the application circuit in Figure 34 are also shown.

$$S_e = \frac{V_O}{L}\left(\frac{N_S}{N_P}\right)(R_S)A_i$$

where: V_O = DC output voltage
N_P, N_S = number of power transformer primary or secondary turns
A_i = gain of the current sense network (see Figures 23 and 24)
L = output inductor
R_S = current sense resistance

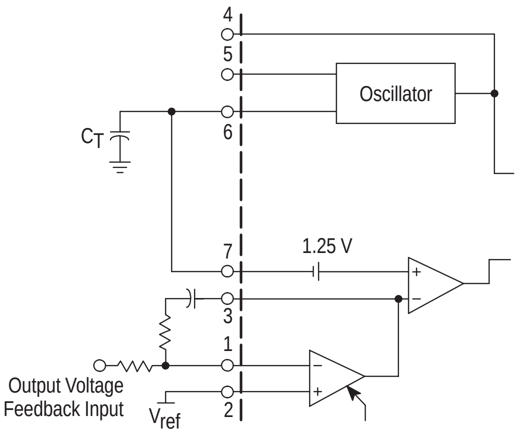
For the application circuit: $S_e = \frac{5}{1.8\ \mu}\left(\frac{2}{8}\right)(0.3)(0.55)$

$= 0.115$ V/ms

PIN FUNCTION DESCRIPTION

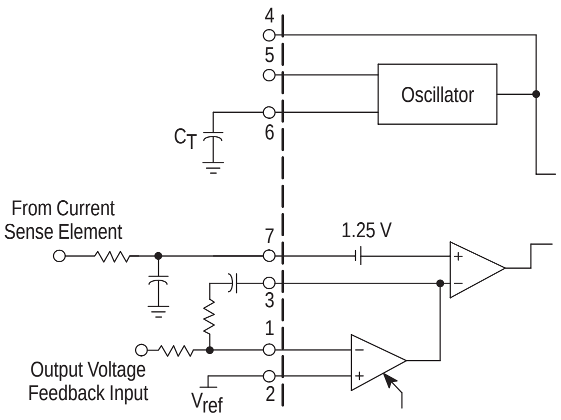
Pin		
DIP/SOIC	Function	Description
1	Error Amp Inverting Input	This pin is usually used for feedback from the output of the power supply.
2	Error Amp Noninverting Input	This pin is used to provide a reference in which an error signal can be produced on the output of the error amp. Usually this is connected to V_{ref}, however an external reference can also be used.
3	Error Amp Output	This pin is provided for compensating the error amp for poles and zeros encountered in the power supply system, mostly the output LC filter.
4	Clock	This is a bidirectional pin used for synchronization.
5	R_T	The value of R_T sets the charge current through timing Capacitor, C_T.
6	C_T	In conjunction with R_T, the timing Capacitor sets the switching frequency.
7	Ramp Input	For voltage mode operation this pin is connected to C_T. For current mode operation this pin is connected through a filter to the current sensing element.
8	Soft–Start	A capacitor at this pin sets the Soft–Start time.
9	Current Limit/ Shutdown	This pin has two functions. First, it provides cycle–by–cycle current limiting. Second, if the current is excessive, this pin will reinitiate a Soft–Start cycle.
10	Ground	This pin is the ground for the control circuitry.
11	Current Limit Reference Input	This pin voltage sets the threshold for cycle–by–cycle current limiting.
12	Power Ground	This is a separate power ground return that is connected back to the power source. It is used to reduce the effects of switching transient noise on the control circuitry.
13	V_C	This is a separate power source connection for the outputs that is connected back to the power source input. With a separate power source connection, it can reduce the effects of switching transient noise on the control circuitry.
14	Output	This is a high current totem pole output.
15	V_{CC}	This pin is the positive supply of the control IC.
16	V_{ref}	This is a 5.1 V reference. It is usually connected to the noninverting input of the error amplifier.

Figure 21. Voltage Mode Operation



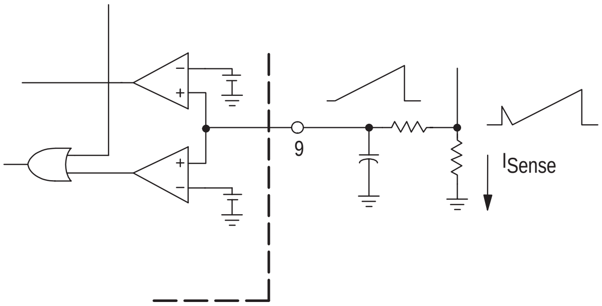
In voltage mode operation, the control range on the output of the Error Amplifier from 0% to 90% duty cycle is from 2.25 V to 4.05 V.

Figure 22. Current Mode Operation



In current mode control, an RC filter should be placed at the ramp input to filter the leading edge spike caused by turn–on of a power MOSFET.

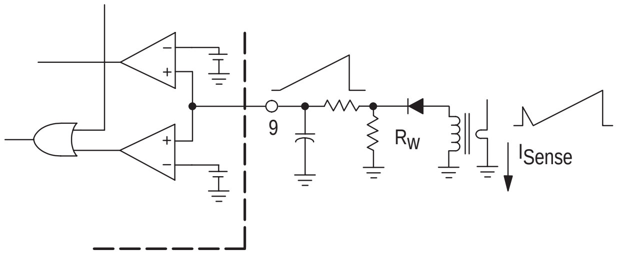
Figure 23. Resistive Current Sensing



The addition of an RC filter will eliminate instability caused by the leading edge spike on the current waveform. This sense signal can also be used at the ramp input pin for current mode control. For ramp compensation it is necessary to know the gain of the current feedback loop. If a transformer is used, the gain can be calculated by:

$$A_i = \frac{R_{Sense}}{\text{turns ratio}}$$

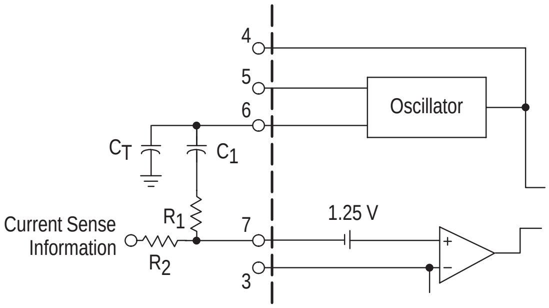
Figure 24. Primary Side Current Sensing



The addition of an RC filter will eliminate instability caused by the leading edge spike on the current waveform. This sense signal can also be used at the ramp input pin for current mode control. For ramp compensation it is necessary to know the gain of the current feedback loop. The gain can be calculated by:

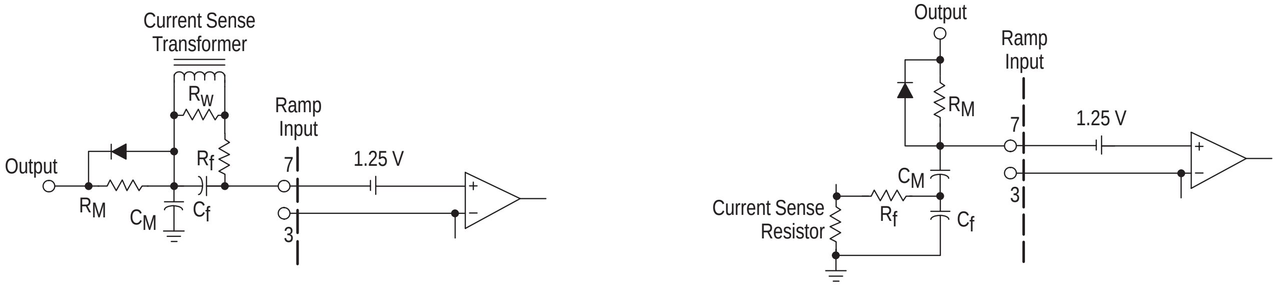
$$A_i = \frac{R_w}{\text{turns ratio}}$$

Figure 25A. Slope Compensation (Noise Sensitive)



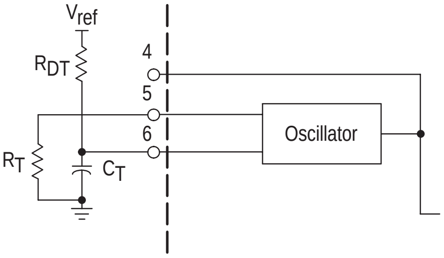
This method of slope compensation is easy to implement, however, it is noise sensitive. Capacitor C_1 provides AC coupling. The oscillator signal is added to the current signal by a voltage divider consisting of resistors R_1 and R_2.

Figure 25B. Slope Compensation (Noise Immune)



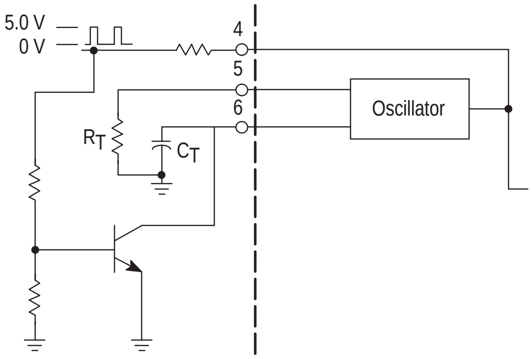
When only one output is used, this method of slope compensation can be used and it is relatively noise immune. Resistor R_M and capacitor C_M provide the added slope necessary. By choosing R_M and C_M with a larger time constant than the switching frequency, you can assume that its charge is linear. First choose C_M, then R_M can be adjusted to achieve the required slope. The diode provides a reset pulse at the ramp input at the end of every cycle. The charge current I_M can be calculated by $I_M = C_M S_e$. Then R_M can be calculated by $R_M = V_{CC}/I_M$.

Figure 26. Dead Time Addition



Additional dead time can be added by the addition of a dead time resistor from V_{ref} to C_T. See text on Oscillator section for more information.

Figure 27. External Clock Synchronization



The sync pulse fed into the clock pin must be at least 3.9 V. R_T and C_T need to be set 10% slower than the sync frequency. This circuit is also used in Voltage Mode operation for master/slave operation. The clock signal would be coming from the master which is set at the desired operating frequency, while the slave is set 10% slower.

Figure 28. Current Mode Master/Slave Operation Over Short Distances

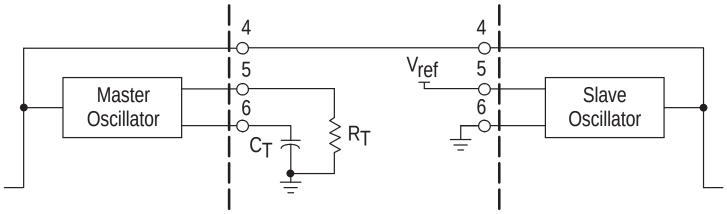


Figure 29. Synchronization Over Long Distances

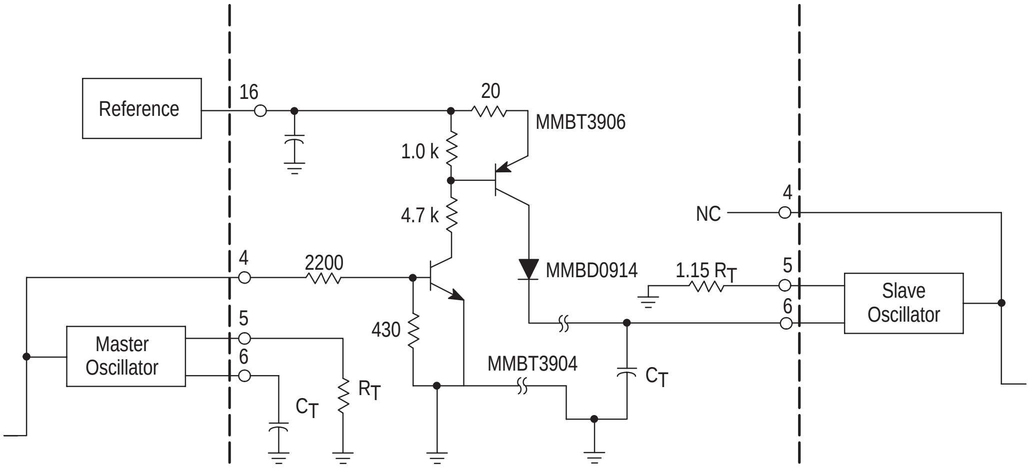
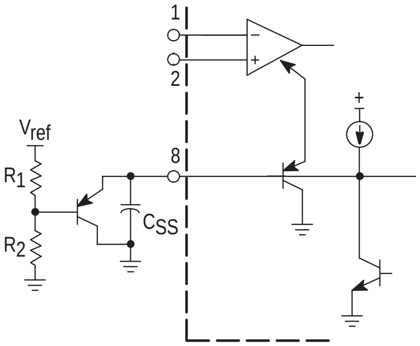


Figure 30. Buffered Maximum Clamp Level

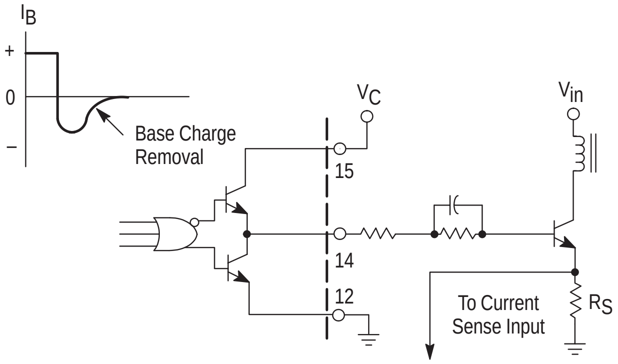


In voltage mode operation, the maximum duty cycle can be clamped. By the addition of a PNP transistor to buffer the clamp voltage, the Soft–Start current is not affected by R_1.

The new equation for Soft–Start is $t \approx \frac{V_{clamp} + 0.6}{9.0\ \mu A}(C_{SS})$

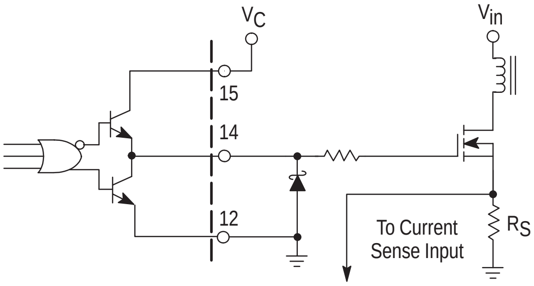
In current mode operation, this circuit will limit the maximum voltage allowed at the ramp input to end a cycle.

Figure 31. Bipolar Transistor Drive



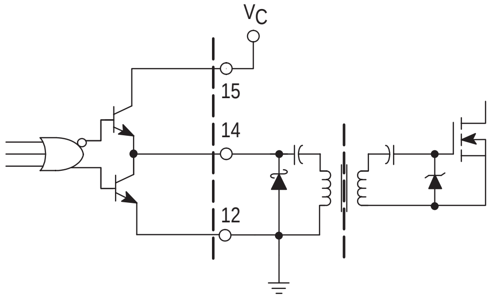
The totem pole output can furnish negative base current for enhanced transistor turn–off, with the addition of the capacitor in series with the base.

Figure 32. MOSFET Parasitic Oscillations



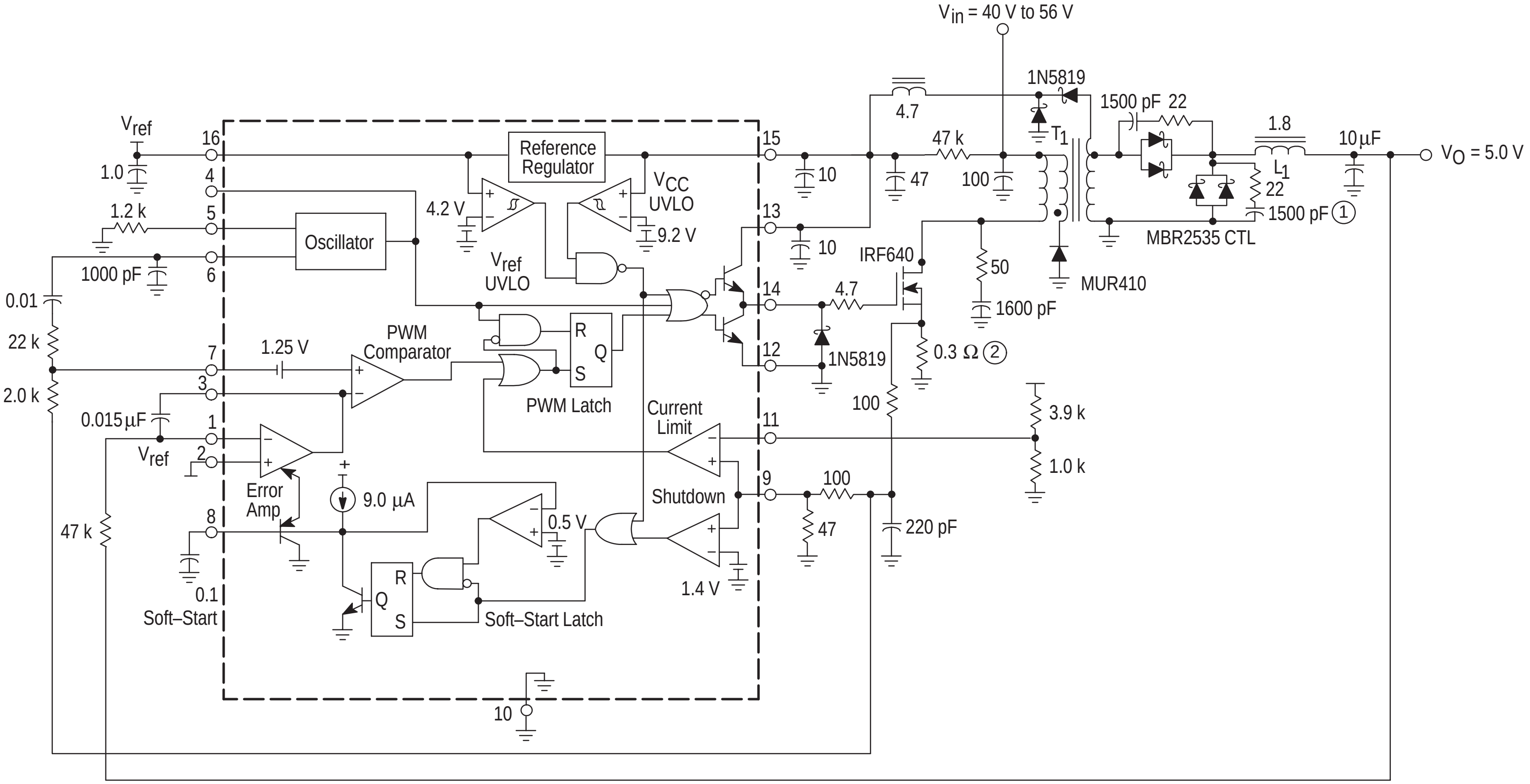
A series gate resistor may be needed to dampen high frequency parasitic oscillation caused by the MOSFET’s input capacitance and any series wiring inductance in the gate–source circuit. The series resistor will also decrease the MOSFET switching speed. A Schottky diode can reduce the driver’s power dissipation due to excessive ringing, by preventing the output pin from being driven below ground. The Schottky diode also prevents substrate injection when the output pin is driven below ground.

Figure 33. Isolated MOSFET Drive



The totem pole output can easily drive pulse transformers. A Schottky diode is recommended when driving inductive loads at high frequencies. The diode can reduce the driver’s power dissipation due to excessive ringing, by preventing the output pin from being driven below ground.

Figure 34. Application Circuit



T_1 – Primary: 8 turns #48 AWG (1300 strands litz wire)
Secondary: 2 turns 0.003’’ (2 layers) copper foil
Bootstrap: 1 turn added to secondary #36 AWG
Core: Philips 3F3, part #4312 020 4124
Bobbin: Philips part #4322 021 3525
Coilcraft P3269–A

L_1 – 2 turns #48 AWG (1300 strands litz wire)
Core: Philips 3F3, part #EP10–3F3
Bobbin: Philips part #EP10PCB1–8
L = 1.8 µH
Coilcraft P3270–A

Heatsinks – Power FET: AAVID Heatsink #533902B02552 with clip
Output Rectifiers: AAVID Heatsink #533402B02552 with clip

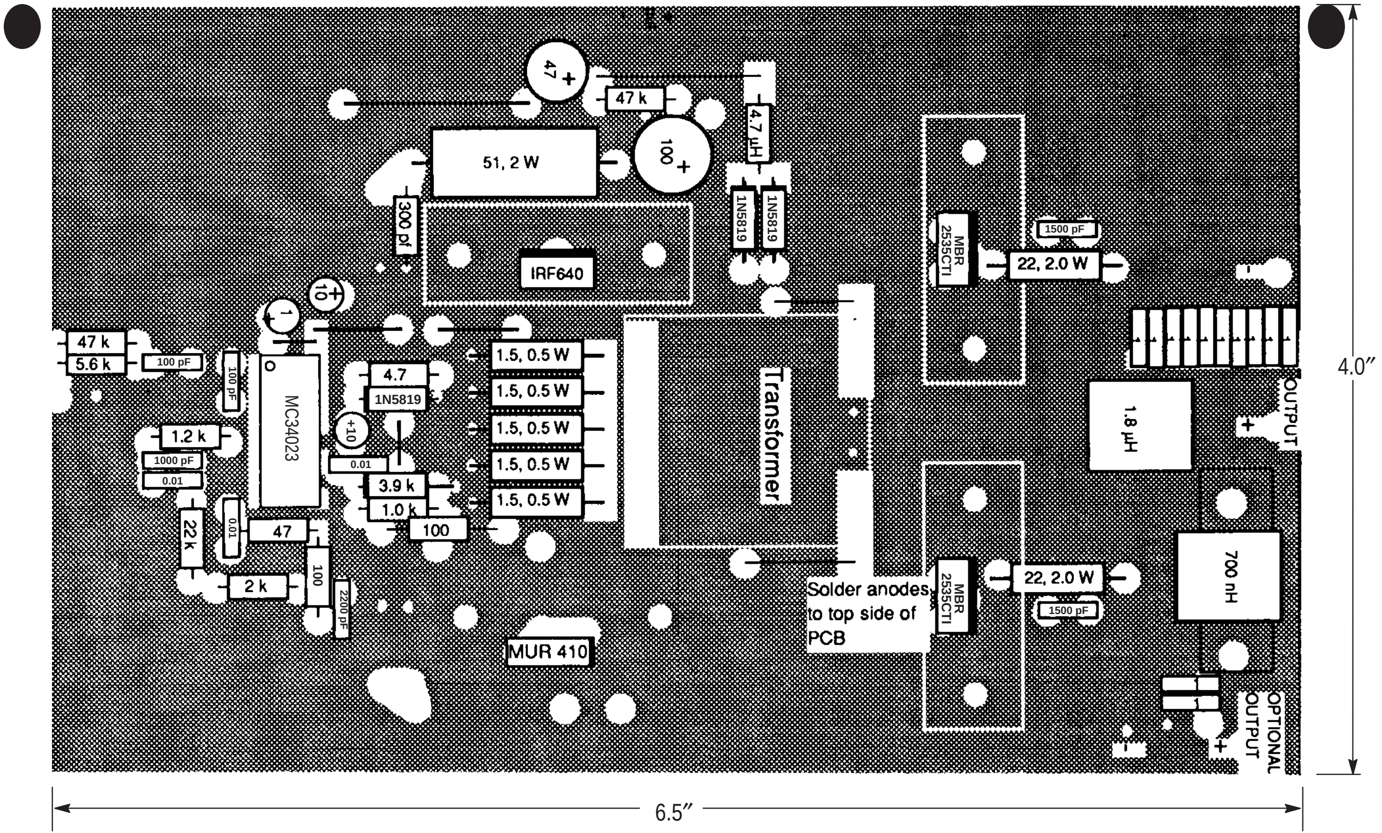
Insulators – All power devices are insulated with Berquist Sil–Pad 150

① – 10(1.0 µF) ceramic capacitors in parallel

② – 5(1.5 Ω) resistors in parallel

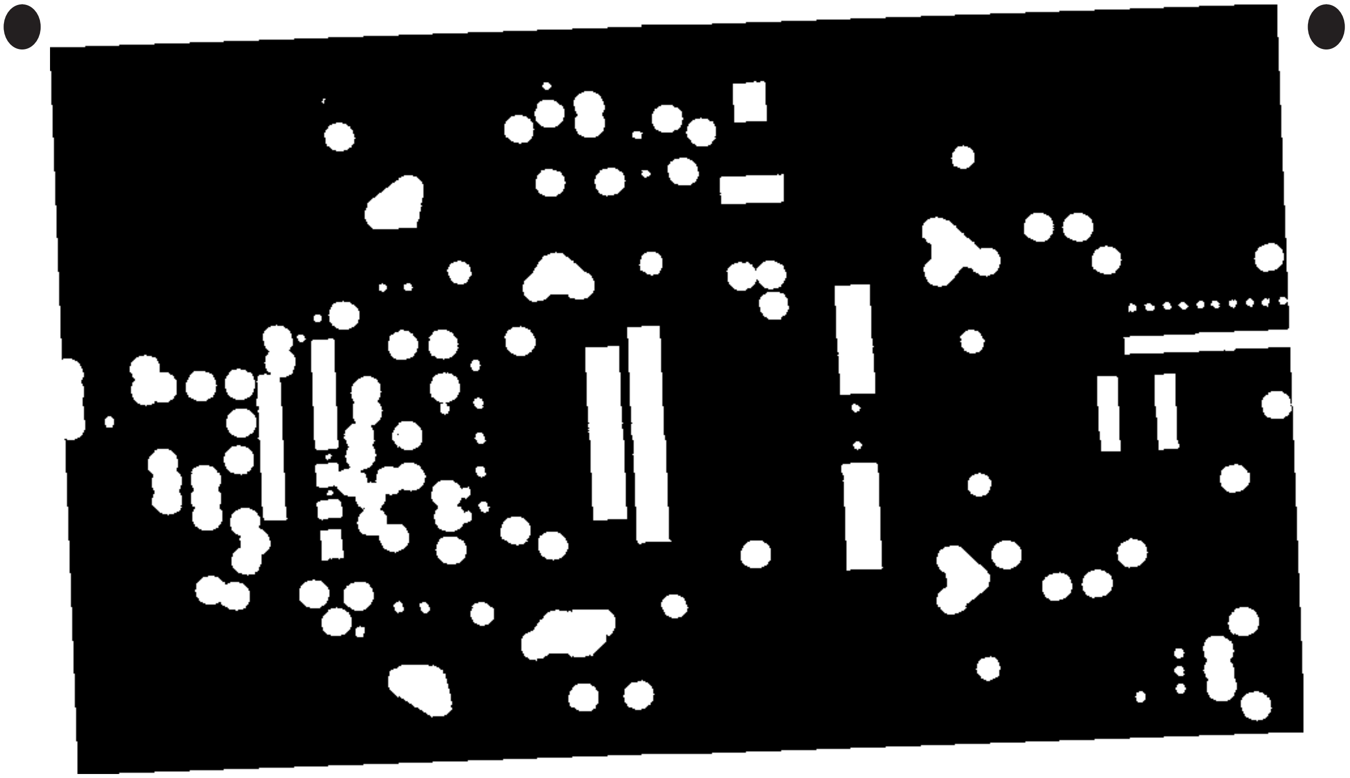
Test	Condition	Result
Line Regulation	V_{in} = 40 V to 56 V, I_O = 7.5A	14 mV = ±0.275%
Load Regulation	V_{in} = 48 V, I_O = 4.0 A to 7.5 A	54 mV = ±1.0%
Output Ripple	V_{in} = 48 V, I_O = 7.5 A	10 mVp–p
Efficiency	V_{in} = 48 V, I_O = 7.5 A	69.8%

Figure 35. PC Board With Components

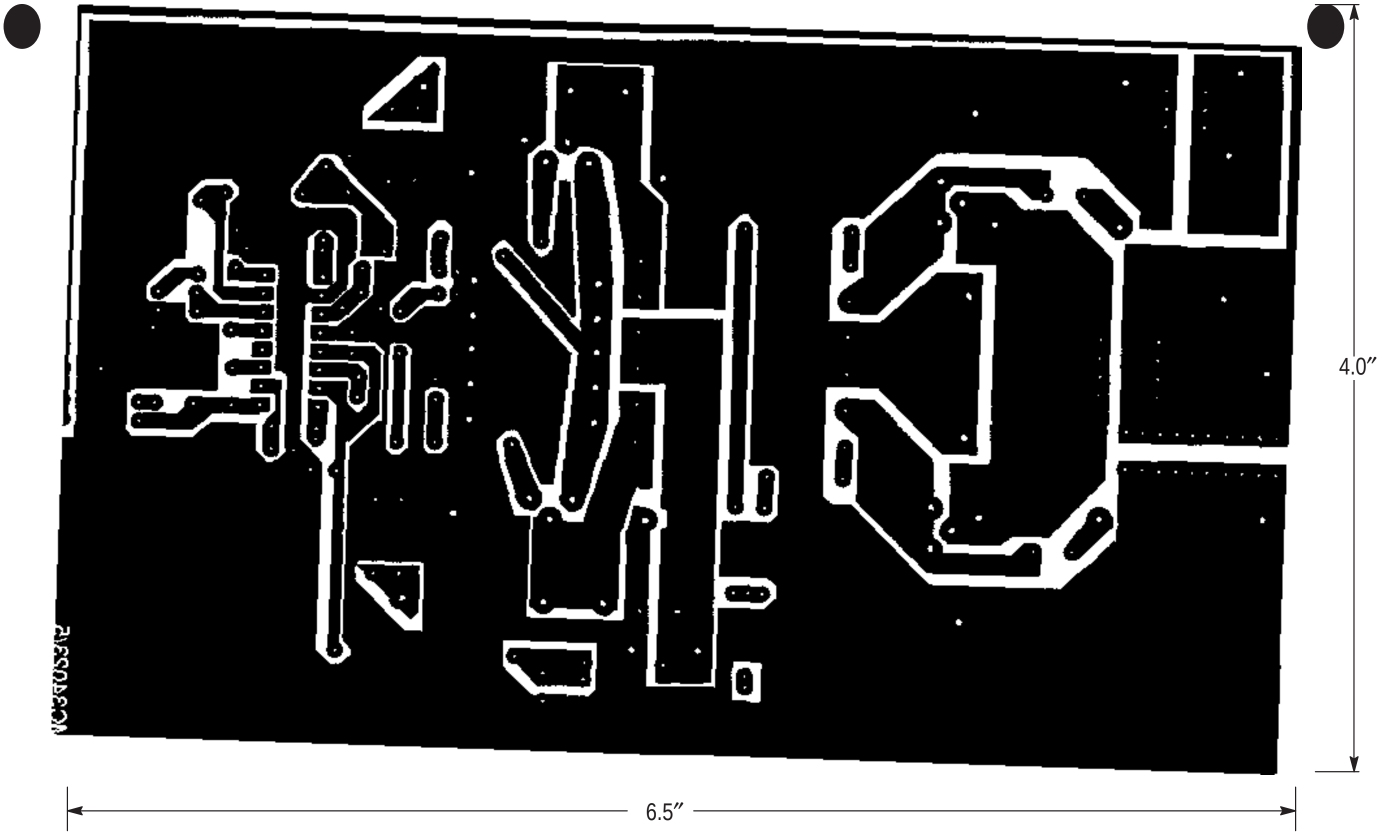


(Top View)

Figure 36. PC Board Without Components



(Top View)



(Bottom View)

MOTOROLA

MC34025
MC33025

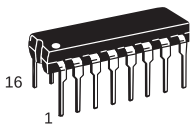
High Speed Double-Ended PWM Controller

The MC34025 series are high speed, fixed frequency, double–ended pulse width modulator controllers optimized for high frequency operation. They are specifically designed for Off–Line and DC–to–DC converter applications offering the designer a cost effective solution with minimal external components. These integrated circuits feature an oscillator, a temperature compensated reference, a wide bandwidth error amplifier, a high speed current sensing comparator, steering flip–flop, and dual high current totem pole outputs ideally suited for driving power MOSFETs.

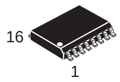
Also included are protective features consisting of input and reference undervoltage lockouts each with hysteresis, cycle–by–cycle current limiting, and a latch for single pulse metering.

The flexibility of this series allows it to be easily configured for either current mode or voltage mode control.

- 50 ns Propagation Delay to Outputs
- Dual High Current Totem Pole Outputs
- Wide Bandwidth Error Amplifier
- Fully–Latched Logic with Double Pulse Suppression
- Latching PWM for Cycle–By–Cycle Current Limiting
- Soft–Start Control with Latched Overcurrent Reset
- Input Undervoltage Lockout with Hysteresis
- Low Start–Up Current (500 µA Typ)
- Internally Trimmed Reference with Undervoltage Lockout
- 90% Maximum Duty Cycle (Externally Adjustable)
- Precision Trimmed Oscillator
- Voltage or Current Mode Operation to 1.0 MHz
- Functionally Similar to the UC3825

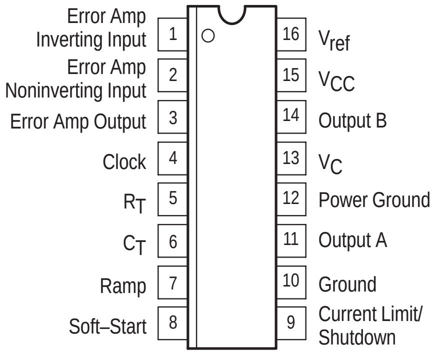


P SUFFIX
PLASTIC PACKAGE
CASE 648



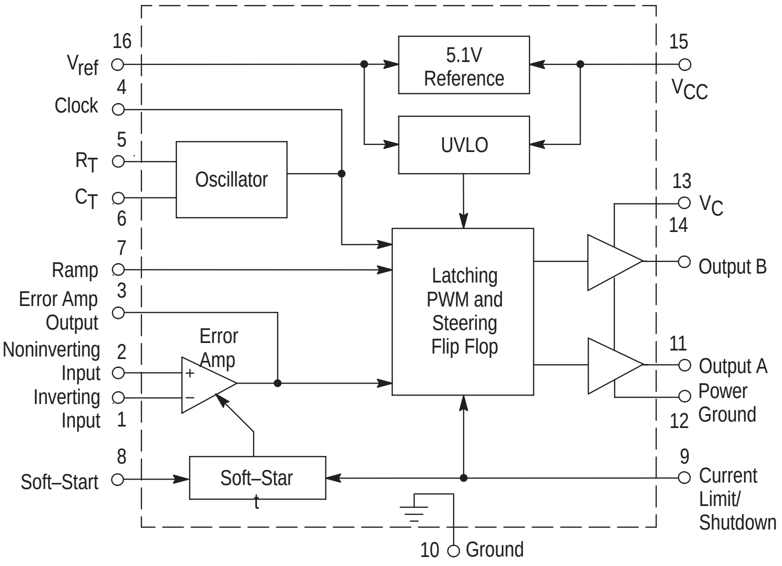
DW SUFFIX
PLASTIC PACKAGE
CASE 751G
(SO–16L)

PIN CONNECTIONS



(Top View)

Simplified Application



This device contains 227 active transistors.

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC33025DW	T_A = –40° to +105°C	SO–16L
MC33025P		Plastic DIP
MC34025DW	T_A = 0° to +70°C	SO–16L
MC34025P		Plastic DIP

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	30	V
Output Driver Supply Voltage	V_C	20	V
Output Current, Source or Sink (Note 1)	I_O		A
DC		0.5	
Pulsed (0.5 µs)		2.0	
Current Sense, Soft–Start, Ramp, and Error Amp Inputs	V_{in}	–0.3 to +7.0	V
Error Amp Output and Soft–Start Sink Current	I_O	10	mA
Clock and R_T Output Current	I_{CO}	5.0	mA
Power Dissipation and Thermal Characteristics			
SO–16 Package (Case 751G)			
Maximum Power Dissipation @ $T_A = +25°C$	P_D	862	mW
Thermal Resistance, Junction–to–Air	$R_{\theta JA}$	145	°C/W
DIP Package (Case 648)			
Maximum Power Dissipation @ $T_A = +25°C$	P_D	1.25	W
Thermal Resistance, Junction–to–Air	$R_{\theta JA}$	100	°C/W
Operating Junction Temperature	T_J	+150	°C
Operating Ambient Temperature (Note 2)	T_A		°C
MC34025		0 to +70	
MC33025		–40 to +105	
Storage Temperature Range	T_{stg}	–55 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V, R_T = 3.65 kΩ, C_T = 1.0 nF, for typical values T_A = +25°C, for min/max values T_A is the operating ambient temperature range that applies [Note 2], unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
REFERENCE SECTION					
Reference Output Voltage (I_O = 1.0 mA, T_J = +25°C)	V_{ref}	5.05	5.1	5.15	V
Line Regulation (V_{CC} = 10 V to 30 V)	Reg_{line}	–	2.0	15	mV
Load Regulation (I_O = 1.0 mA to 10 mA)	Reg_{load}	–	2.0	15	mV
Temperature Stability	T_S	–	0.2	–	mV/°C
Total Output Variation over Line, Load, and Temperature	V_{ref}	4.95	–	5.25	V
Output Noise Voltage (f = 10 Hz to 10 kHz, T_J = +25°C)	V_n	–	50	–	µV
Long Term Stability (T_A = +125°C for 1000 Hours)	S	–	5.0	–	mV
Output Short Circuit Current	I_{SC}	–30	–65	–100	mA
OSCILLATOR SECTION					
Frequency	f_{osc}				kHz
T_J = +25°C		380	400	420	
Line (V_{CC} = 10 V to 30 V) and Temperature ($T_A = T_{low}$ to T_{high})		370	400	430	
Frequency Change with Voltage (V_{CC} = 10 V to 30 V)	$\Delta f_{osc}/\Delta V$	–	0.2	1.0	%
Frequency Change with Temperature ($T_A = T_{low}$ to T_{high})	$\Delta f_{osc}/\Delta T$	–	2.0	–	%
Sawtooth Peak Voltage	V_P	2.6	2.8	3.0	V
Sawtooth Valley Voltage	V_V	0.7	1.0	1.25	V
Clock Output Voltage					V
High State	V_{OH}	3.9	4.5	–	
Low State	V_{OL}	–	2.3	2.9	

NOTES: 1. Maximum package power dissipation limits must be observed.
2. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
T_{low} = 0°C for MC34025 T_{high} = +70°C for MC34025
= – 40°C for MC33025 = +105°C for MC33025

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V, R_T = 3.65 kΩ, C_T = 1.0 nF, for typical values T_A = +25°C, for min/max values T_A is the operating ambient temperature range that applies [Note 2], unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
ERROR AMPLIFIER SECTION					
Input Offset Voltage	V_{IO}	–	–	15	mV
Input Bias Current	I_{IB}	–	0.6	3.0	µA
Input Offset Current	I_{IO}	–	0.1	1.0	µA
Open–Loop Voltage Gain (V_O = 1.0 V to 4.0 V)	A_{VOL}	60	95	–	dB
Gain Bandwidth Product (T_J = +25°C)	GBW	4.0	8.3	–	MHz
Common Mode Rejection Ratio (V_{CM} = 1.5 V to 5.5 V)	CMRR	75	95	–	dB
Power Supply Rejection Ratio (V_{CC} = 10 V to 30 V)	PSRR	85	110	–	dB
Output Current, Source (V_O = 4.0 V) Sink (V_O = 1.0 V)	I_{Source} I_{Sink}	0.5 1.0	3.0 3.6	– –	mA
Output Voltage Swing, High State (I_O = – 0.5 mA) Low State (I_O = 1.0 mA)	V_{OH} V_{OL}	4.5 0	4.75 0.4	5.0 1.0	V
Slew Rate	SR	6.0	12	–	V/µs
PWM COMPARATOR SECTION					
Ramp Input Bias Current	I_{IB}	–	–0.5	–5.0	µA
Duty Cycle, Maximum Minimum	$DC_{(max)}$ $DC_{(min)}$	80 –	90 –	– 0	%
Zero Duty Cycle Threshold Voltage Pin 3(4) (Pin 7(9) = 0 V)	V_{th}	1.1	1.25	1.4	V
Propagation Delay (Ramp Input to Output, T_J = +25°C)	$t_{PLH(in/out)}$	–	60	100	ns
SIFT–START SECTION					
Charge Current ($V_{Soft–Start}$ = 0.5 V)	I_{chg}	3.0	9.0	20	µA
Discharge Current ($V_{Soft–Start}$ = 1.5 V)	I_{dischg}	1.0	4.0	–	mA
CURRENT SENSE SECTION					
Input Bias Current (Pin 9(12) = 0 V to 4.0 V)	I_{IB}	–	–	15	µA
Current Limit Comparator Threshold Shutdown Comparator Threshold	V_{th} V_{th}	0.9 1.25	1.0 1.40	1.10 1.55	V
Propagation Delay (Current Limit/Shutdown to Output, T_J = +25°C)	$t_{PLH(in/out)}$	–	50	80	ns
OUTPUT SECTION					
Output Voltage					V
Low State (I_{Sink} = 20 mA)	V_{OL}	–	0.25	0.4	
(I_{Sink} = 200 mA)		–	1.2	2.2	
High State (I_{Source} = 20 mA)	V_{OH}	13	13.5	–	
(I_{Source} = 200 mA)		12	13	–	
Output Voltage with UVLO Activated (V_{CC} = 6.0 V, I_{Sink} = 0.5 mA)	$V_{OL(UVLO)}$	–	0.25	1.0	V
Output Leakage Current (V_C = 20 V)	I_L	–	100	500	µA
Output Voltage Rise Time (C_L = 1.0 nF, T_J = +25°C)	t_r	–	30	60	ns
Output Voltage Fall Time (C_L = 1.0 nF, T_J = +25°C)	t_f	–	30	60	ns
UNDERVOLTAGE LOCKOUT SECTION					
Start–Up Threshold (V_{CC} Increasing)	$V_{th(on)}$	8.8	9.2	9.6	V
UVLO Hysteresis Voltage (V_{CC} Decreasing After Turn–On)	V_H	0.4	0.8	1.2	V
TOTAL DEVICE					
Power Supply Current	I_{CC}				mA
Start–Up (V_{CC} = 8.0 V)		–	0.5	1.2	
Operating		–	25	35	

NOTES: 1. Maximum package power dissipation limits must be observed.
2. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
T_{low} = 0°C for MC34025 T_{high} = +70°C for MC34025
= – 40°C for MC33025 = +105°C for MC33025

Figure 1. Timing Resistor versus Oscillator Frequency

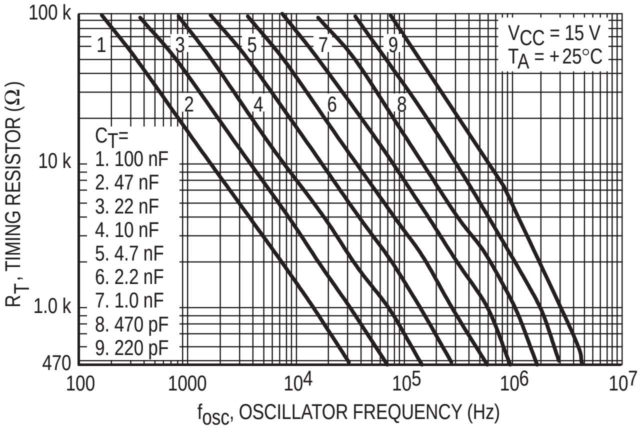


Figure 2. Oscillator Frequency versus Temperature

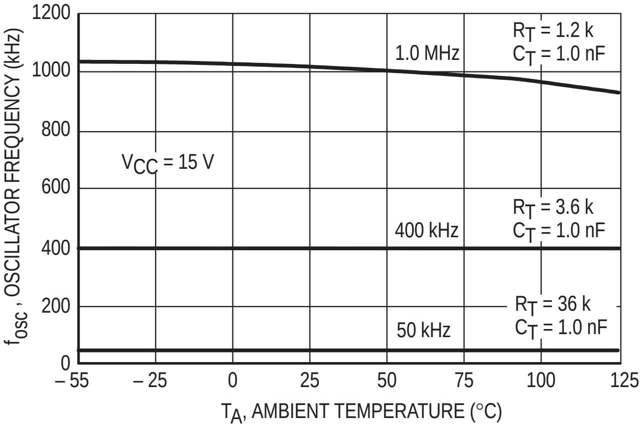


Figure 3. Error Amp Open Loop Gain and Phase versus Frequency

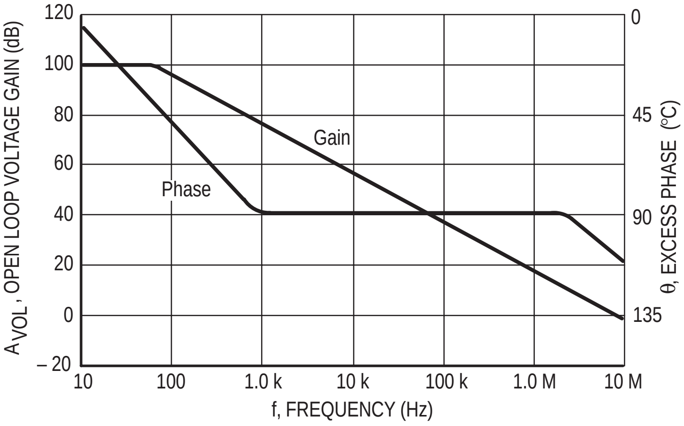


Figure 4. PWM Comparator Zero Duty Cycle Threshold Voltage versus Temperature

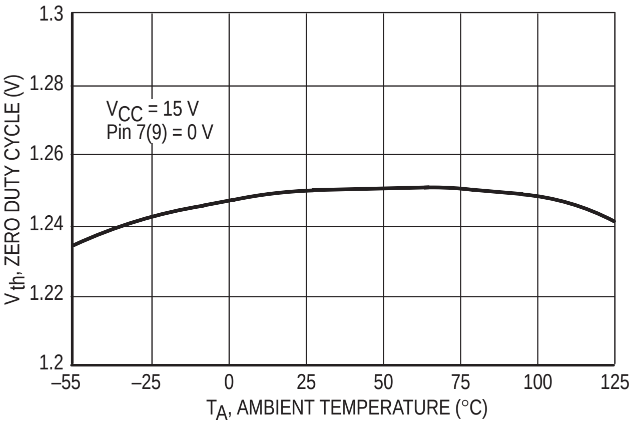


Figure 5. Error Amp Small Signal Transient Response

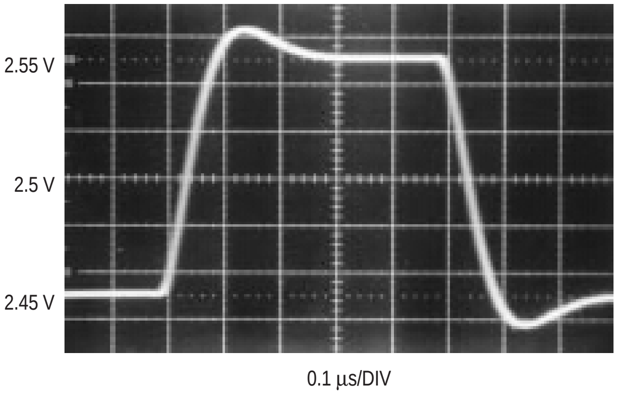


Figure 6. Error Amp Large Signal Transient Response

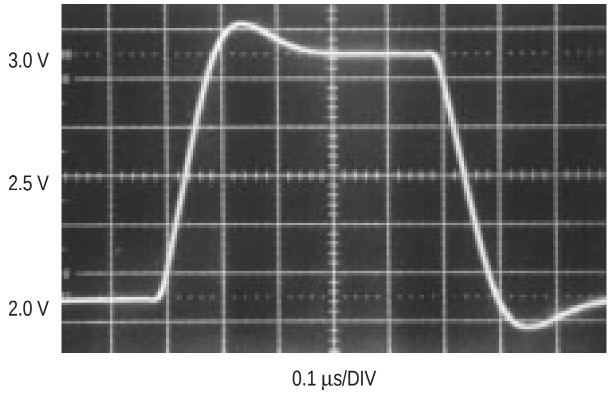


Figure 7. Reference Voltage Change versus Source Current

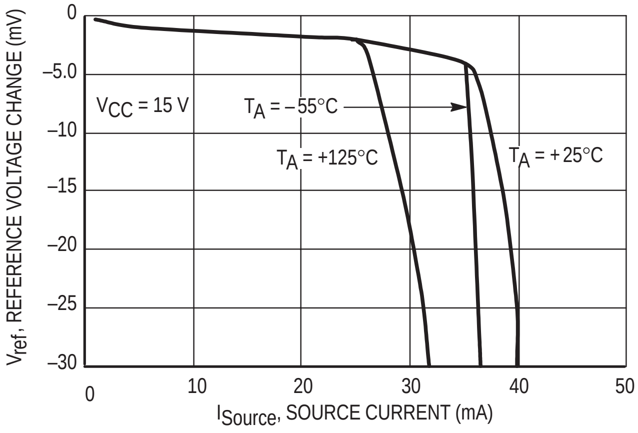


Figure 8. Reference Short Circuit Current versus Temperature

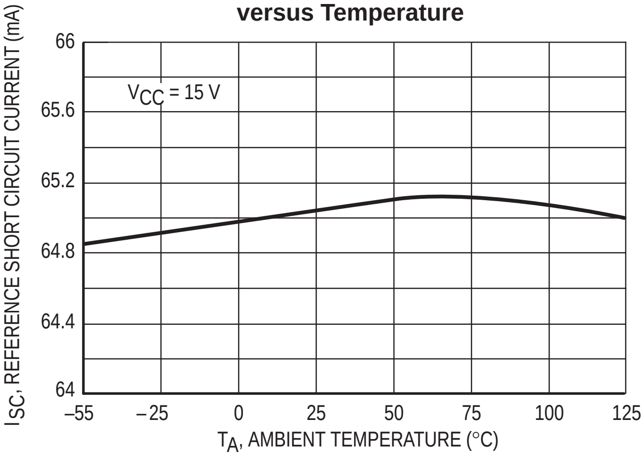
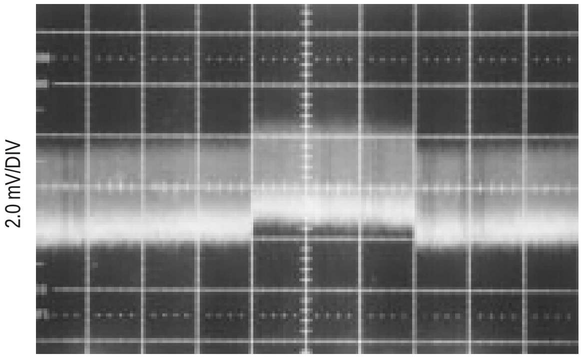
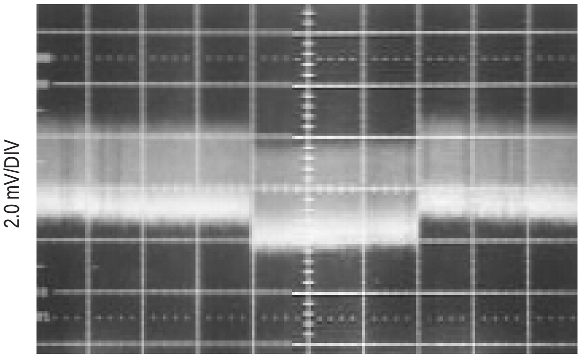


Figure 9. Reference Line Regulation



V_{ref} LINE REGULATION 10 V – 24 V
2.0 ms/DIV

Figure 10. Reference Load Regulation



V_{ref} LINE REGULATION 1.0 mA – 10 mA
2.0 ms/DIV

Figure 11. Current Limit Comparator Threshold Change versus Temperature

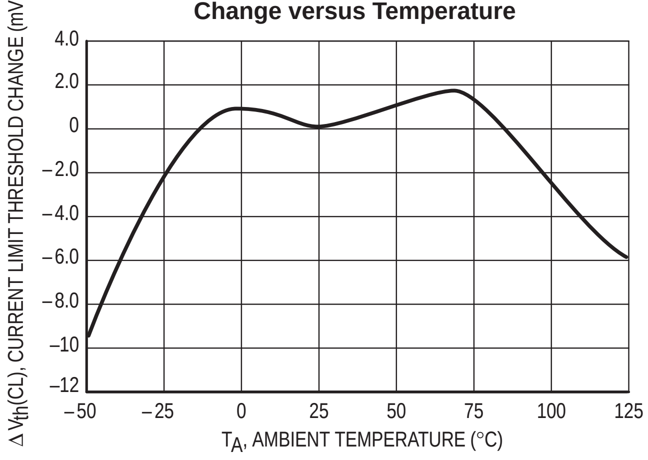


Figure 12. Shutdown Comparator Threshold Voltage versus Temperature

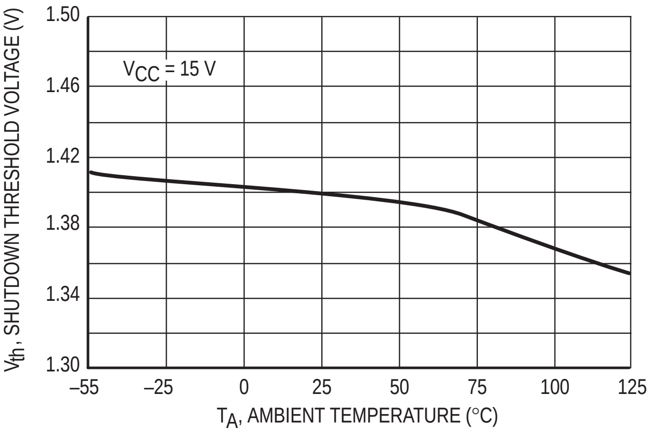


Figure 13. Soft–Start Charge Current versus Temperature

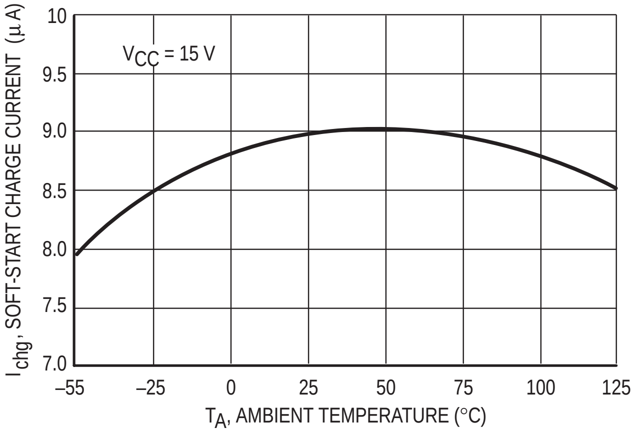


Figure 14. Output Saturation Voltage versus Load Current

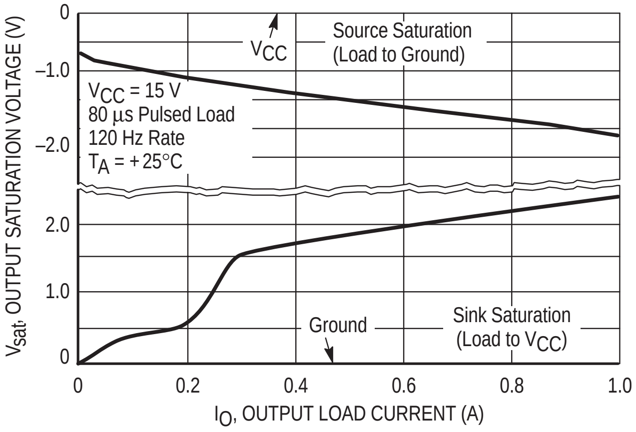
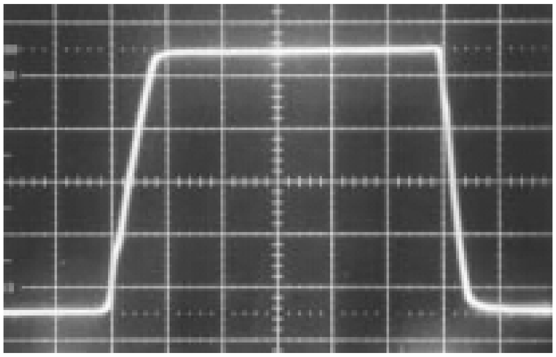
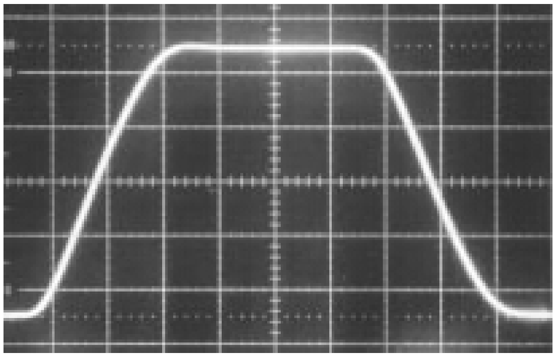


Figure 15. Drive Output Rise and Fall Time



OUTPUT RISE & FALL TIME 1.0 nF LOAD
50 ns/DIV

Figure 16. Drive Output Rise and Fall Time



OUTPUT RISE & FALL TIME 10.0 nF LOAD
50 ns/DIV

Figure 17. Supply Voltage versus Supply Current

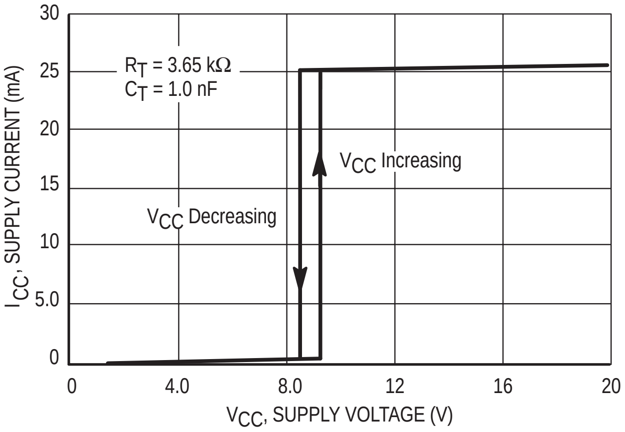


Figure 18. Representative Block Diagram

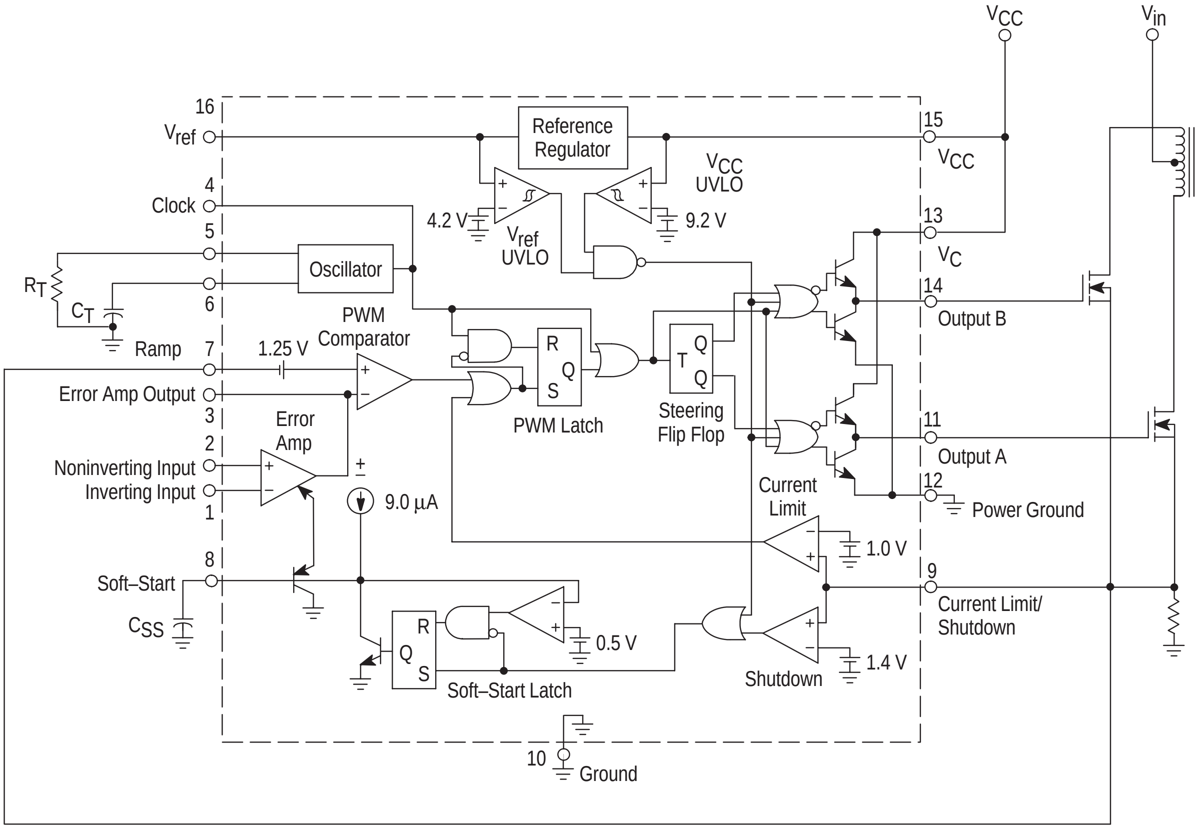
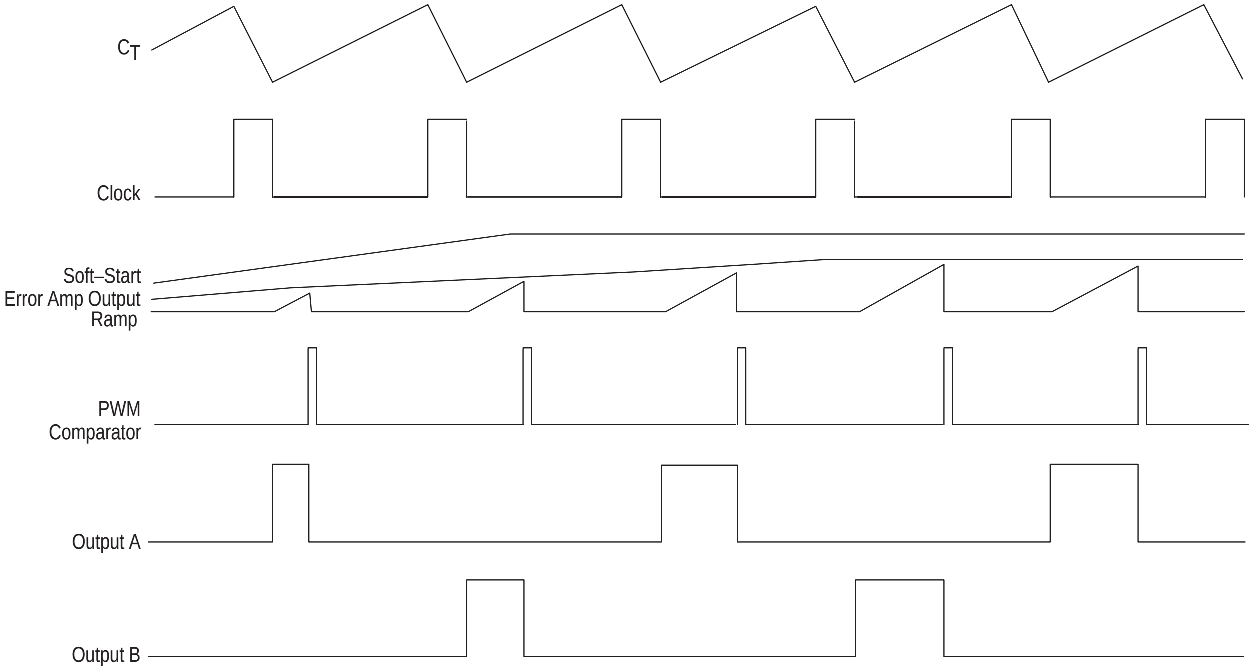


Figure 19. Current Limit Operating Waveforms



OPERATING DESCRIPTION

The MC33025 and MC34025 series are high speed, fixed frequency, double–ended pulse width modulator controllers optimized for high frequency operation. They are specifically designed for Off–Line and DC–to–DC converter applications offering the designer a cost effective solution with minimal external components. A representative block diagram is shown in Figure 18.

Oscillator

The oscillator frequency is programmed by the values selected for the timing components R_T and C_T. The R_T pin is set to a temperature compensated 3.0 V. By selecting the value of R_T, the charge current is set through a current mirror for the timing capacitor C_T. This charge current runs continuously through C_T. The discharge current is ratioed to be 10 times the charge current, which yields the maximum duty cycle of 90%. C_T is charged to 2.8 V and discharged to 1.0 V. During the discharge of C_T, the oscillator generates an internal blanking pulse that resets the PWM Latch, inhibits the outputs, and toggles the steering flip–flop. The threshold voltages on the oscillator comparator is trimmed to guarantee an oscillator accuracy of 5.0% at 25°C.

Additional dead time can be added by externally increasing the charge current to C_T as shown in Figure 23. This changes the charge to discharge ratio of C_T which is set internally to $I_{charge}/10\ I_{charge}$. The new charge to discharge ratio will be:

$$\%\ \text{Deadtime} = \frac{I_{additional} + I_{charge}}{10\ (I_{charge})}$$

A bidirectional clock pin is provided for synchronization or for master/slave operation. As a master, the clock pin provides a positive output pulse during the discharge of C_T. As a slave, the clock pin is an input that resets the PWM latch and blanks the drive output, but does not discharge C_T. Therefore, the oscillator is not synchronized by driving the clock pin alone. Figures 29 and 30 provide suggested synchronization.

Error Amplifier

A fully compensated Error Amplifier is provided. It features a typical DC voltage gain of 95 dB and a gain bandwidth product of 8.3 MHz with 75 degrees of phase margin (Figure 3). Typical application circuits will have the noninverting input tied to the reference. The inverting input will typically be connected to a feedback voltage generated from the output of the switching power supply. Both inputs have a Common Mode Voltage (V_{CM}) input range of 1.5 V to 5.5 V. The Error Amplifier Output is provided for external loop compensation.

Soft–Start Latch

Soft–Start is accomplished in conjunction with an external capacitor. The soft start capacitor is charged by an internal 9.0 µA current source. This capacitor clamps the output of the error amplifier to less than its normal output voltage, thus limiting the duty cycle.

The time it takes for a capacitor to reach full charge is given by:

$$t \approx (4.5 \bullet 10^5)\ C_{Soft\text{-}Start}$$

A Soft–Start latch is incorporated to prevent erratic operation of this circuitry. Two conditions can cause the Soft–Start circuit to latch so that the Soft–Start capacitor stays discharged. The first condition is activation of an undervoltage lockout of either V_{CC} or V_{ref}. The second condition is when current sense input exceeds 1.4 V. Since this latch is "set dominant", it cannot be reset until either of these signals is removed, and the voltage at $C_{Soft–Start}$ is less than 0.5 V.

PWM Comparator and Latch

A PWM circuit typically compares an error voltage with a ramp signal. The outcome of this comparison determines the state of the output. In voltage mode operation the ramp signal is the voltage ramp of the timing capacitor. In current mode operation the ramp signal is the voltage ramp induced in a current sensing element. The ramp input of the PWM comparator is pinned out so that the user can decide which mode of operation best suits the application requirements. The ramp input has a 1.25 V offset such that whenever the voltage at this pin exceeds the Error Amplifier Output voltage minus 1.25 V, the PWM comparator will cause the PWM latch to set, disabling the outputs. Once the PWM latch is set, only a blanking pulse by the oscillator can reset it, thus initiating the next cycle.

A toggle flip flop connected to the output of the PWM latch controls which output is active. The flip flop is pulsed by an OR gate that gets its inputs from the oscillator clock and the output of the PWM latch. A pulse from either one will cause the flip flop to enable the other output.

Current Limiting and Shutdown

A pin is provided to perform current limiting and shutdown operations. Two comparators are connected to the input of this pin. When the voltage at this pin exceeds 1.0 V, one of the comparators is activated. The output of this comparator sets the PWM latch, which disables the output. In this way cycle–by–cycle current limiting is accomplished. If a current limit resistor is used in series with the power devices, the value of the resistor is found by:

$$R_{Sense} = \frac{1.0\ V}{I_{pk\ (switch)}}$$

If the voltage at this pin exceeds 1.4 V, the second comparator is activated. This comparator sets a latch which, in turn, causes the Soft–Start capacitor to be discharged. In this way a "hiccup" mode of recovery is possible in the case of output short circuits. If a current limit resistor is used in series with the output devices, the peak current at which the controller will enter a "hiccup" mode is given by:

$$I_{shutdown} = \frac{1.4\ V}{R_{Sense}}$$

Undervoltage Lockout

There are two undervoltage lockout circuits within the IC. The first senses V_{CC} and the second V_{ref}. During power–up, V_{CC} must exceed 9.2 V and V_{ref} must exceed 4.2 V before the outputs can be enabled and the Soft–Start latch released. If V_{CC} falls below 8.4 V or V_{ref} falls below 3.6 V, the outputs are disabled and the Soft–Start latch is activated. When the UVLO is active, the part is in a low current standby mode allowing the IC to have an off–line bootstrap start–up circuit. Typical start–up current is 500 μA.

Output

The MC34025 has two high current totem pole outputs specifically designed for direct drive of power MOSFETs. They are capable of up to ±2.0 A peak drive current with a typical rise and fall time of 30 ns driving a 1.0 nF load.

Separate pins for V_C and Power Ground are provided. With proper implementation, a significant reduction of switching transient noise imposed on the control circuitry is possible. The separate V_C supply input also allows the designer added flexibility in tailoring the drive voltage independent of V_{CC}.

Reference

A 5.1 V bandgap reference is pinned out and is trimmed to an initial accuracy of ±1.0% at 25°C. This reference has short circuit protection and can source in excess of 10 mA for powering additional control system circuitry.

Design Considerations

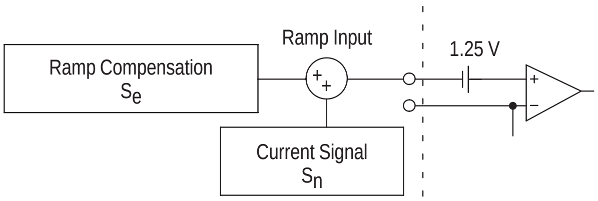
Do not attempt to construct the converter on wire–wrap or plug–in prototype boards. With high frequency, high power, switching power supplies it is imperative to have separate current loops for the signal paths and for the power paths. The printed circuit layout should contain a ground plane with low current signal and high current switch and output grounds returning on separate paths back to the input filter capacitor. All bypass capacitors and snubbers should be connected as close as possible to the specific part in question. The PC board lead lengths must be less than 0.5 inches for effective bypassing or snubbing.

Instabilities

In current mode control, an instability can be encountered at any given duty cycle. The instability is caused by the current feedback loop. It has been shown that the instability is caused by a double pole at half the switching frequency. If an external ramp (S_e) is added to the on–time ramp (S_n) of the current–sense waveform, stability can be achieved (see Figure 20).

One must be careful not to add too much ramp compensation. If too much is added, the system will start to perform like a voltage mode regulator. All benefits of current mode control will be lost. Figures 28A and 28B show examples of two different ways in which external ramp compensation can be implemented.

Figure 20. Ramp Compensation



A simple equation can be used to calculate the amount of external ramp necessary to add that will achieve stability in the current loop. For the following equations, the calculated values for the application circuit in Figure 36 are also shown.

$$S_e = \frac{V_O}{L}\left(\frac{N_S}{N_P}\right)(R_S)A_i$$

where: V_O = DC output voltage
N_P, N_S = number of power transformer primary or secondary turns
A_i = gain of the current sense network (see Figures 25, 26 and 27)
L = output inductor
R_S = current sense resistance

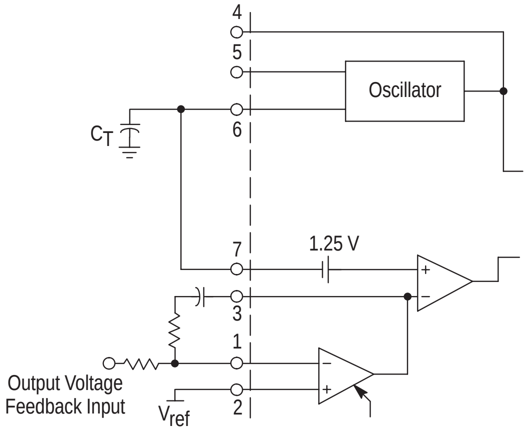
For the application circuit: $S_e = \frac{5}{1.8\ \mu}\left(\frac{4}{16}\right)(0.3)(0.55)$

$= 0.115\ V/\mu s$

PIN FUNCTION DESCRIPTION

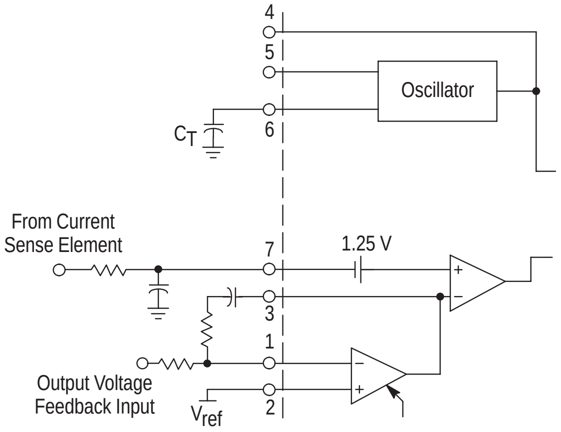
Pin No.		
DIP/SOIC	Function	Description
1	Error Amp Inverting Input	This pin is usually used for feedback from the output of the power supply.
2	Error Amp Noninverting Input	This pin is used to provide a reference in which an error signal can be produced on the output of the error amp. Usually this is connected to V_{ref}, however an external reference can also be used.
3	Error Amp Output	This pin is provided for compensating the error amp for poles and zeros encountered in the power supply system, mostly the output LC filter.
4	Clock	This is a bidirectional pin used for synchronization.
5	R_T	The value of R_T sets the charge current through timing Capacitor, C_T.
6	C_T	In conjunction with R_T, the timing Capacitor sets the switching frequency. Because this part is a push–pull output, each output runs at one–half the frequency set at this pin.
7	Ramp Input	For voltage mode operation this pin is connected to C_T. For current mode operation this pin is connected through a filter to the current sensing element.
8	Soft–Start	A capacitor at this pin sets the Soft–Start time.
9	Current Limit/Shutdown	This pin has two functions. First, it provides cycle–by–cycle current limiting. Second, if the current is excessive, this pin will reinitiate a Soft–Start cycle.
10	Ground	This pin is the ground for the control circuitry.
11	Output A	This is a high current totem pole output.
12	Power Ground	This is a separate power ground return that is connected back to the power source. It is used to reduce the effects of switching transient noise on the control circuitry.
13	V_C	This is a separate power source connection for the outputs that is connected back to the power source input. With a separate power source connection, it can reduce the effects of switching transient noise on the control circuitry.
14	Output B	This is a high current totem pole output.
15	V_{CC}	This pin is the positive supply of the control IC.
16	V_{ref}	This is a 5.1 V reference. It is usually connected to the noninverting input of the error amplifier.

Figure 21. Voltage Mode Operation



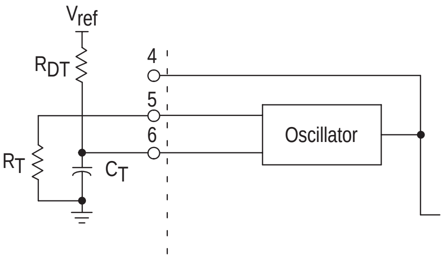
In voltage mode operation, the control range on the output of the Error Amplifier from 0% to 90% duty cycle is from 2.25 V to 4.05 V.

Figure 22. Current Mode Operation



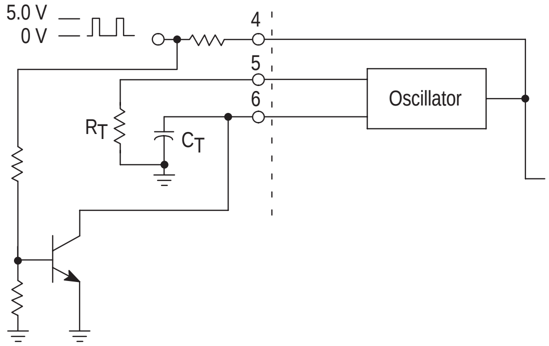
In current mode control, an RC filter should be placed at the ramp input to filter the leading edge spike caused by turn–on of a power MOSFET.

Figure 23. Dead Time Addition



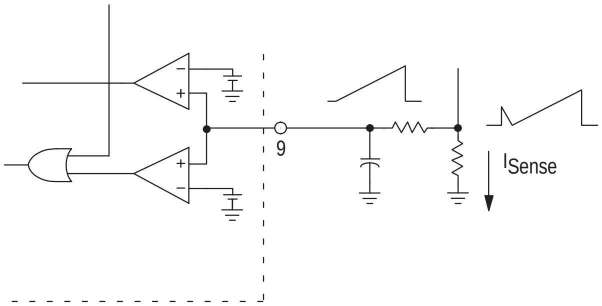
Additional dead time can be added by the addition of a dead time resistor from V_{ref} to C_T. See text on oscillator section for more information.

Figure 24. External Clock Synchronization



The sync pulse fed into the clock pin must be at least 3.9 V. R_T and C_T need to be set 10% slower than the sync frequency. This circuit is also used in voltage mode operation for master/slave operation. The clock signal would be coming from the master which is set at the desired operating frequency, while the slave is set 10% slower.

Figure 25. Resistive Current Sensing



The addition of an RC filter will eliminate instability caused by the leading edge spike on the current waveform. This sense signal can also be used at the ramp input pin for current mode control. For ramp compensation it is necessary to know the gain of the current feedback loop. If a transformer is used, the gain can be calculated by:

$$A_i = \frac{R_{Sense}}{\text{turns ratio}}$$

Figure 26. Primary Side Current Sensing

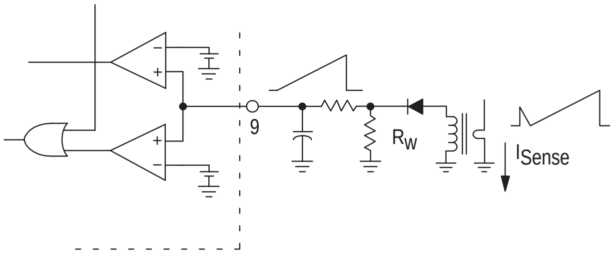
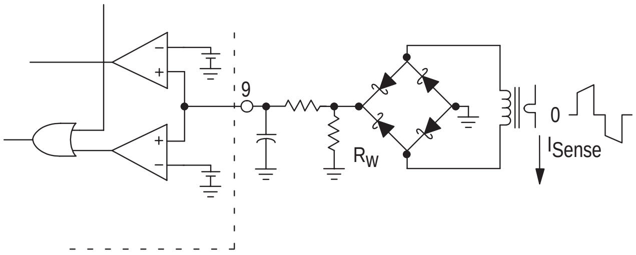


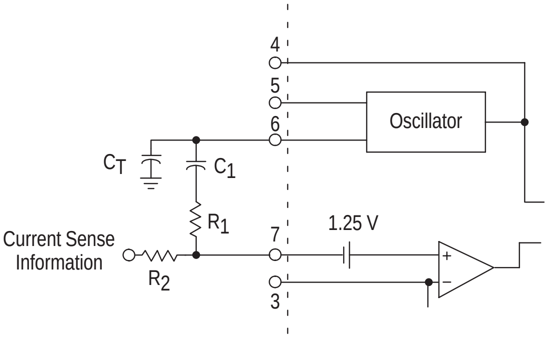
Figure 27. Primary or Secondary Side Current Sensing



The addition of an RC filter will eliminate instability caused by the leading edge spike on the current waveform. This sense signal can also be used at the ramp input pin for current mode control. For ramp compensation it is necessary to know the gain of the current feedback loop. The gain can be calculated by:

$$A_i = \frac{R_w}{\text{turns ratio}}$$

Figure 28A. Slope Compensation (Noise Sensitive)



This method of slope compensation is easy to implement, however, it is noise sensitive. Capacitor C_1 provides AC coupling. The oscillator signal is added to the current signal by a voltage divider consisting of resistors R_1 and R_2.

Figure 28B. Slope Compensation (Noise Immune)

When only one output is used, this method of slope compensation can be used and it is relatively noise immune. Resistor R_M and capacitor C_M provide the added slope necessary. By choosing R_M and C_M with a larger time constant than the switching frequency, you can assume that its charge is linear. First choose C_M, then R_M can be adjusted to achieve the required slope. The diode provides a reset pulse at the ramp input at the end of every cycle. The charge current I_M can be calculated by $I_M = C_M S_e$. Then R_M can be calculated by $R_M = V_{CC}/I_M$.

Figure 29. Current Mode Master/Slave Operation Over Short Distances

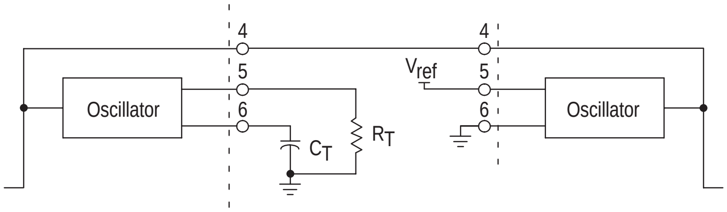


Figure 30. Synchronization Over Long Distances

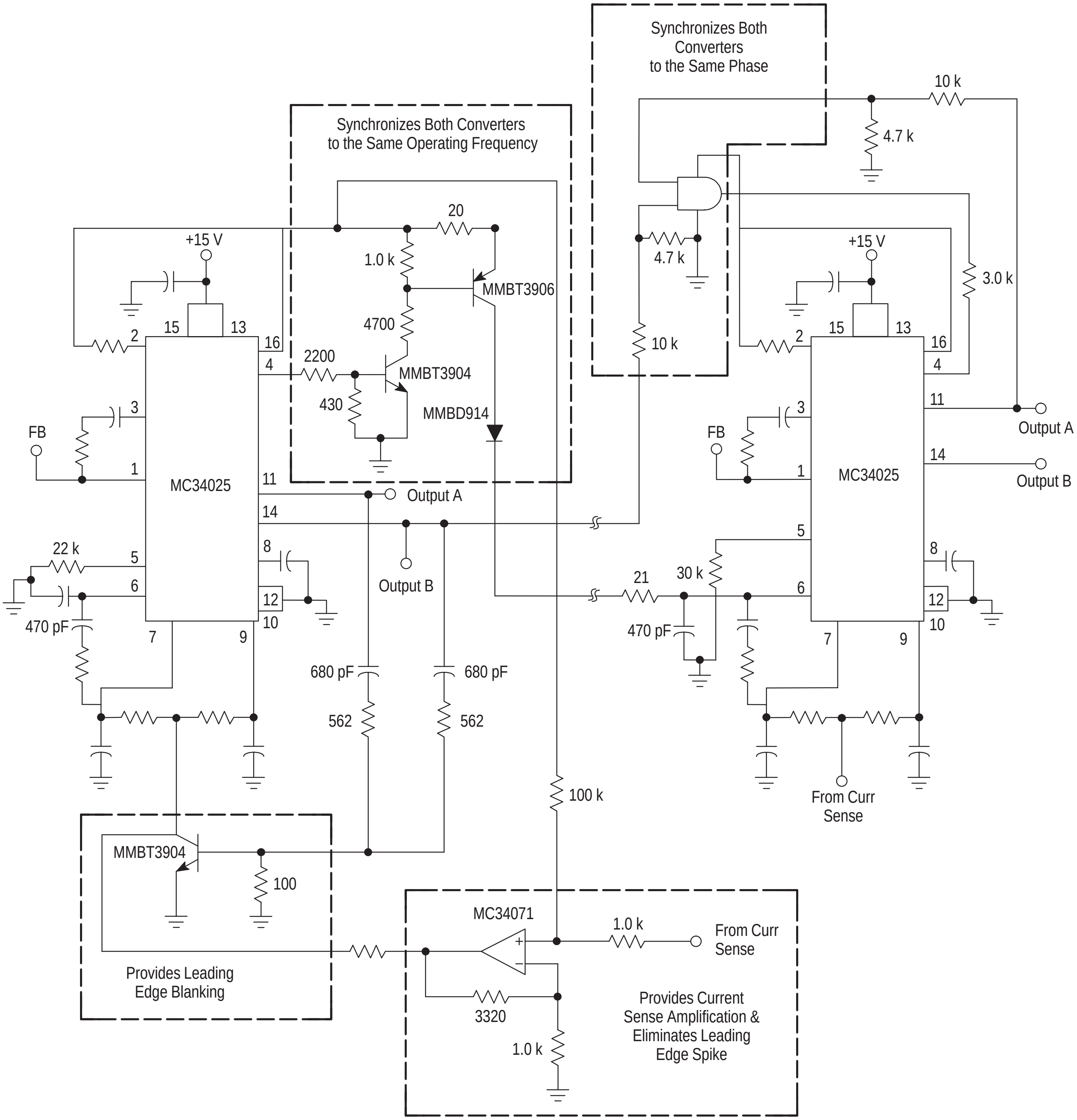
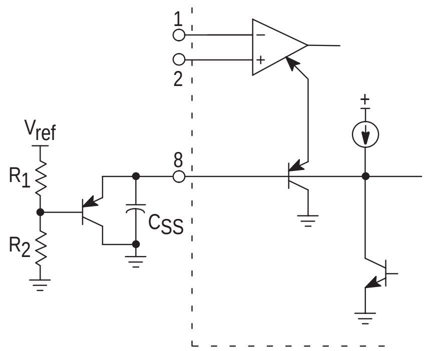


Figure 31. Buffered Maximum Clamp Level

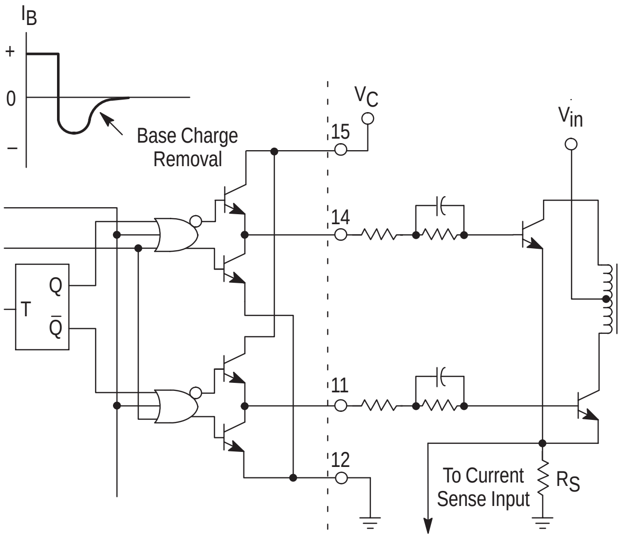


In voltage mode operation, the maximum duty cycle can be clamped. By the addition of a PNP transistor to buffer the clamp voltage, the Soft–Start current is not affected by R_1.

The new equation for Soft–Start is $t \approx \frac{V_{clamp} + 0.6}{9.0\ \mu A} \left(C_{SS}\right)$

In current mode operation, this circuit will limit the maximum voltage allowed at the ramp input to end a cycle.

Figure 32. Bipolar Transistor Drive



The totem pole output can furnish negative base current for enhanced transistor turn–off, with the addition of the capacitor in series with the base.

Figure 33. Isolated MOSFET Drive

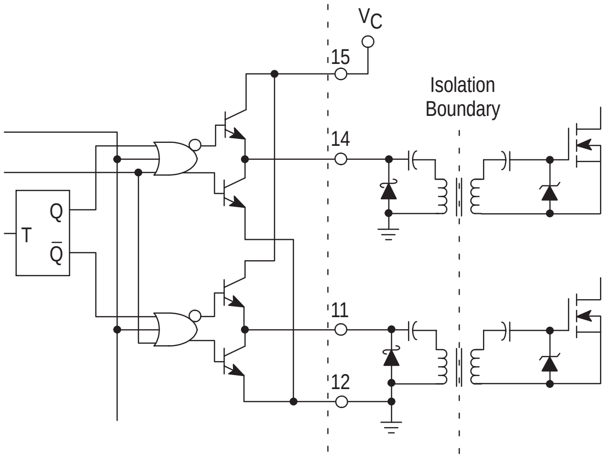
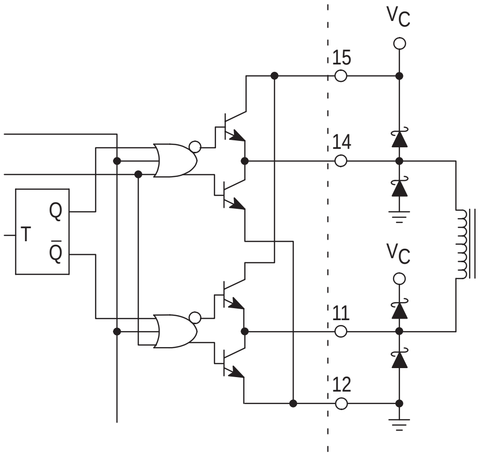
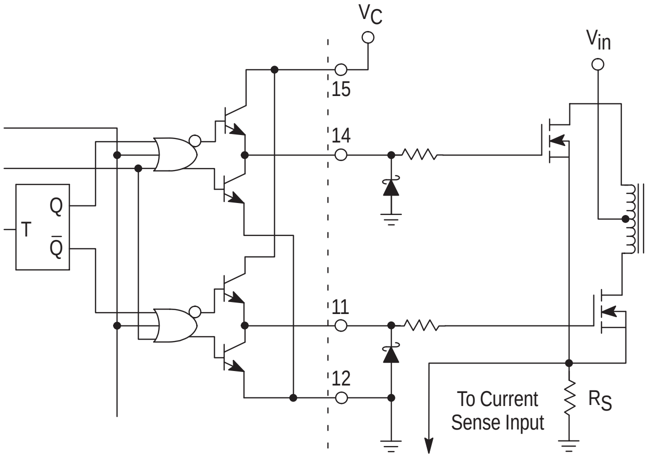


Figure 34. Direct Transformer Drive



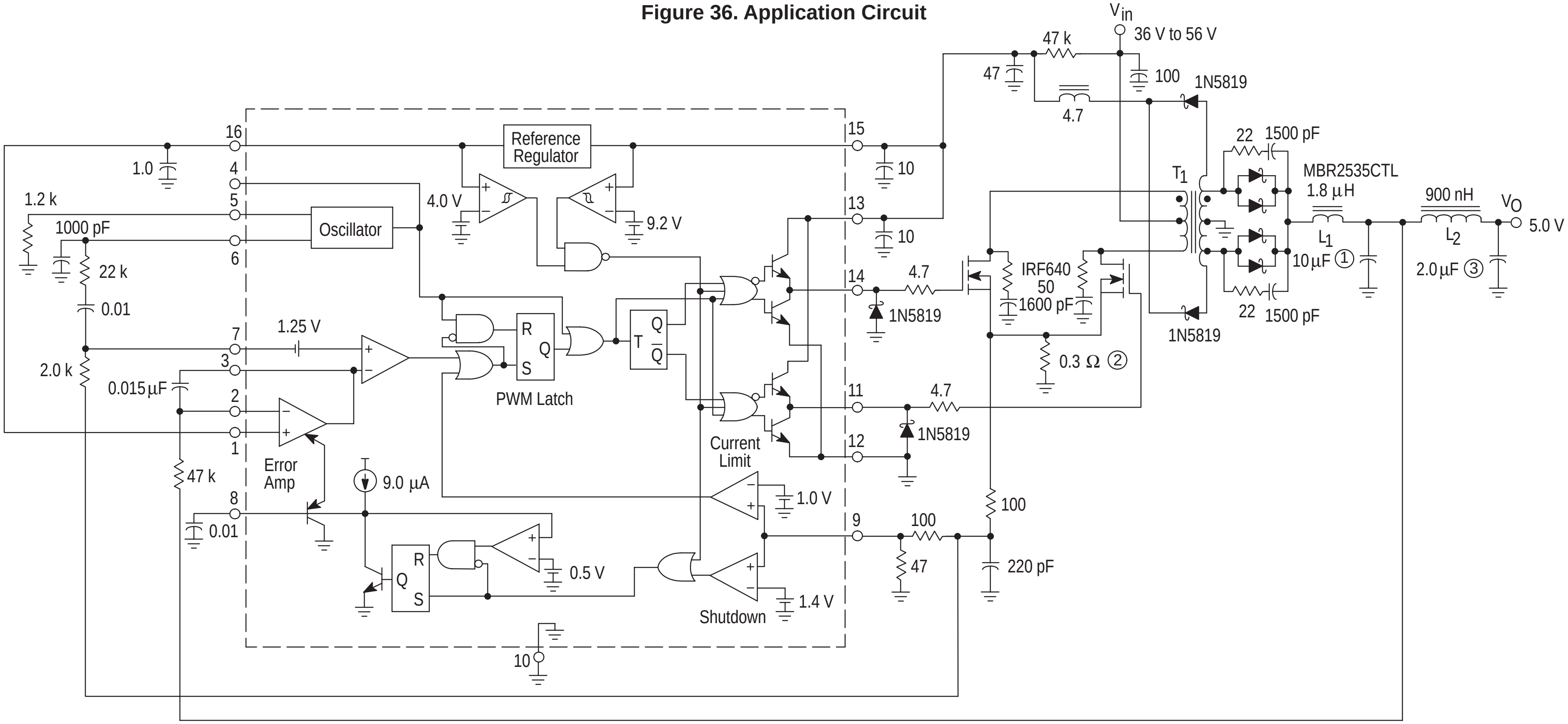
The totem pole output can easily drive pulse transformers. A Schottky diode is recommended when driving inductive loads at high frequencies. The diode can reduce the driver’s power dissipation due to excessive ringing, by preventing the output pin from being driven below ground.

Figure 35. MOSFET Parasitic Oscillations



A series gate resistor may be needed to damp high frequency parasitic oscillation caused by a MOSFET’s input capacitance and any series wiring inductance in the gate–source circuit. The series resistor will also decrease the MOSFET’s switching speed. A Schottky diode can reduce the driver’s power dissipation due to excessive ringing, by preventing the output pin from being driven below ground. The Schottky diode also prevents substrate injection when the output pin is driven below ground.

Figure 36. Application Circuit



T1 – Primary: 16 turns center tapped #48 AWG (1300 strands litz wire)
Secondary: 4 turns center tapped 0.003” (2 layers) copper foil
Bootstrap: 1 turn added to each secondary output #36 AWG
Core: Philips 3F3, part #4312 020 4124
Bobbin: Philips part #4322 021 3525
Coilcraft P3269–A

L1 – 2 turns #48 AWG (1300 strands litz wire)
Core: Philips 3F3, part #EP10–3F3
Bobbin: Philips part #EP10PCB1–8
L = 1.8 µH
Coilcraft P3270–A

L2 – 7 turns #18 AWG, 1/2” diameter air core
Coilcraft P3271–A

Heatsinks – Power FET: AAVID Heatsink #533902B02554 with clip
Output Rectifiers: AAVID Heatsink #533402B02552 with clip

Insulators – All power devices are insulated with Berquist Sil–Pad 1500

① – 10 (1.0 µF) ceramic capacitors in parallel
② – 5 (1.5 Ω) resistors in parallel
③ – 2 (1.0 µF) cearmic capacitors in parallel

Test	Condition	Result
Line Regulation	V_{in} = 40 V to 56 V, I_O = 15 A	14 mV = ±0.275%
Load Regulation	V_{in} = 48 V, I_O = 8.0 V to 15 A	54 mV = ±1.0%
Output Ripple	V_{in} = 48 V, I_O = 15 A	50 mVp–p
Efficiency	V_{in} = 48 V, I_O = 15 A	71.2%

Figure 37. PC Board With Components

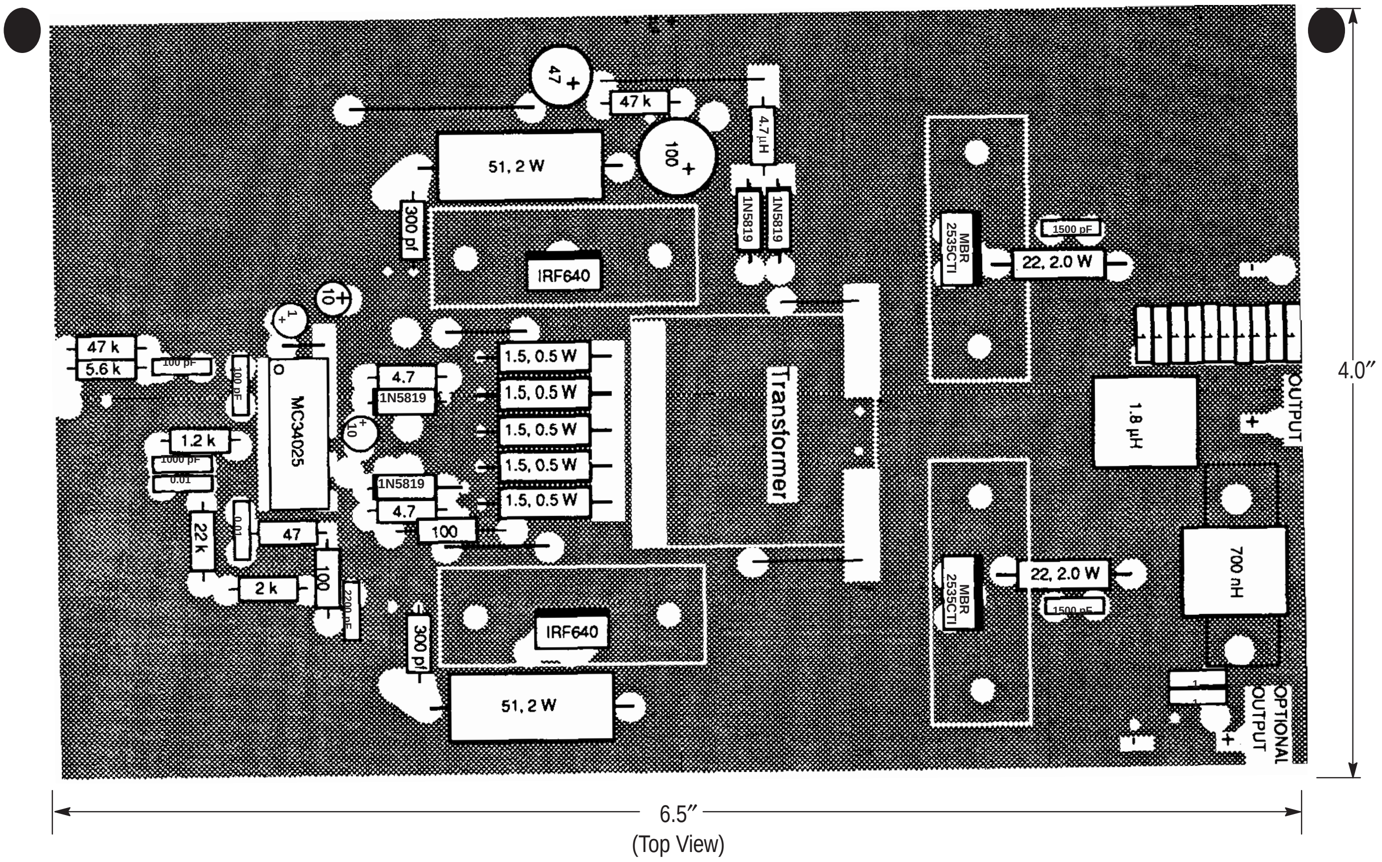
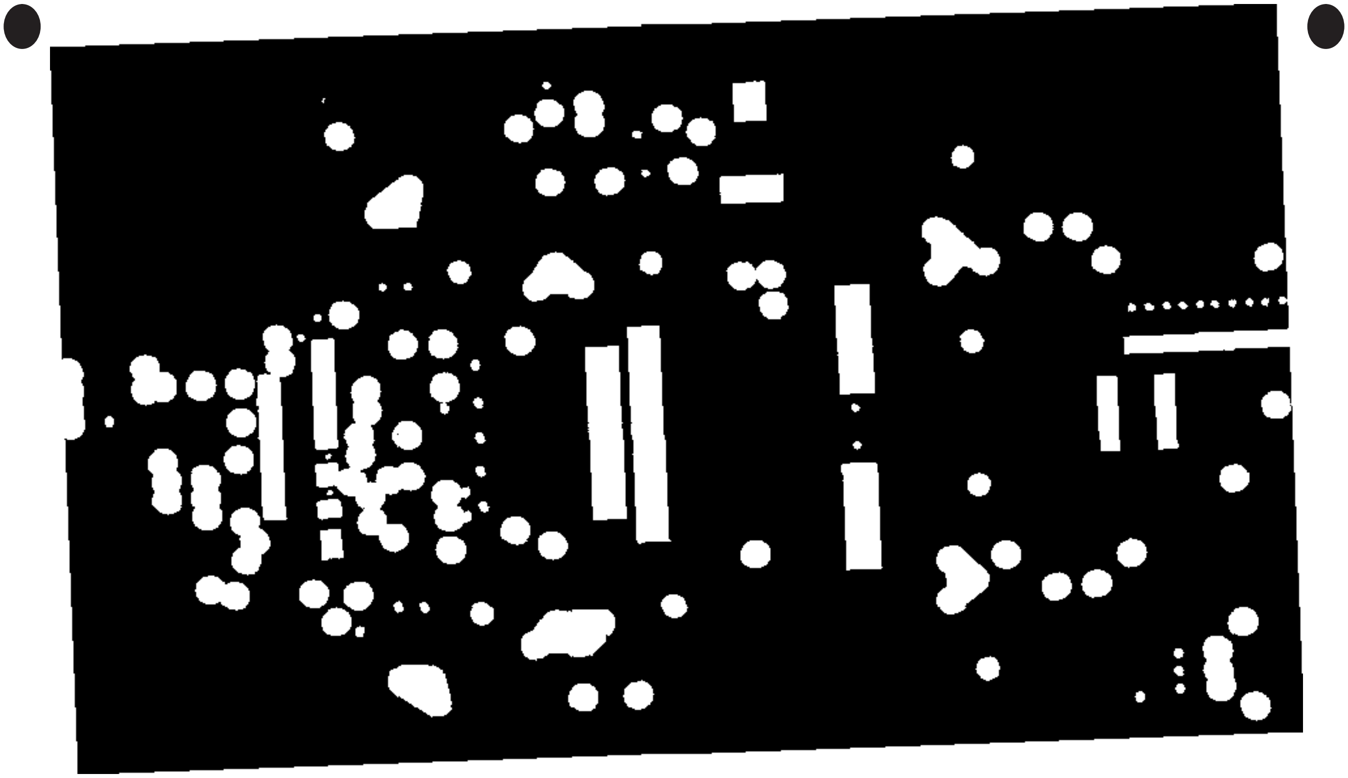
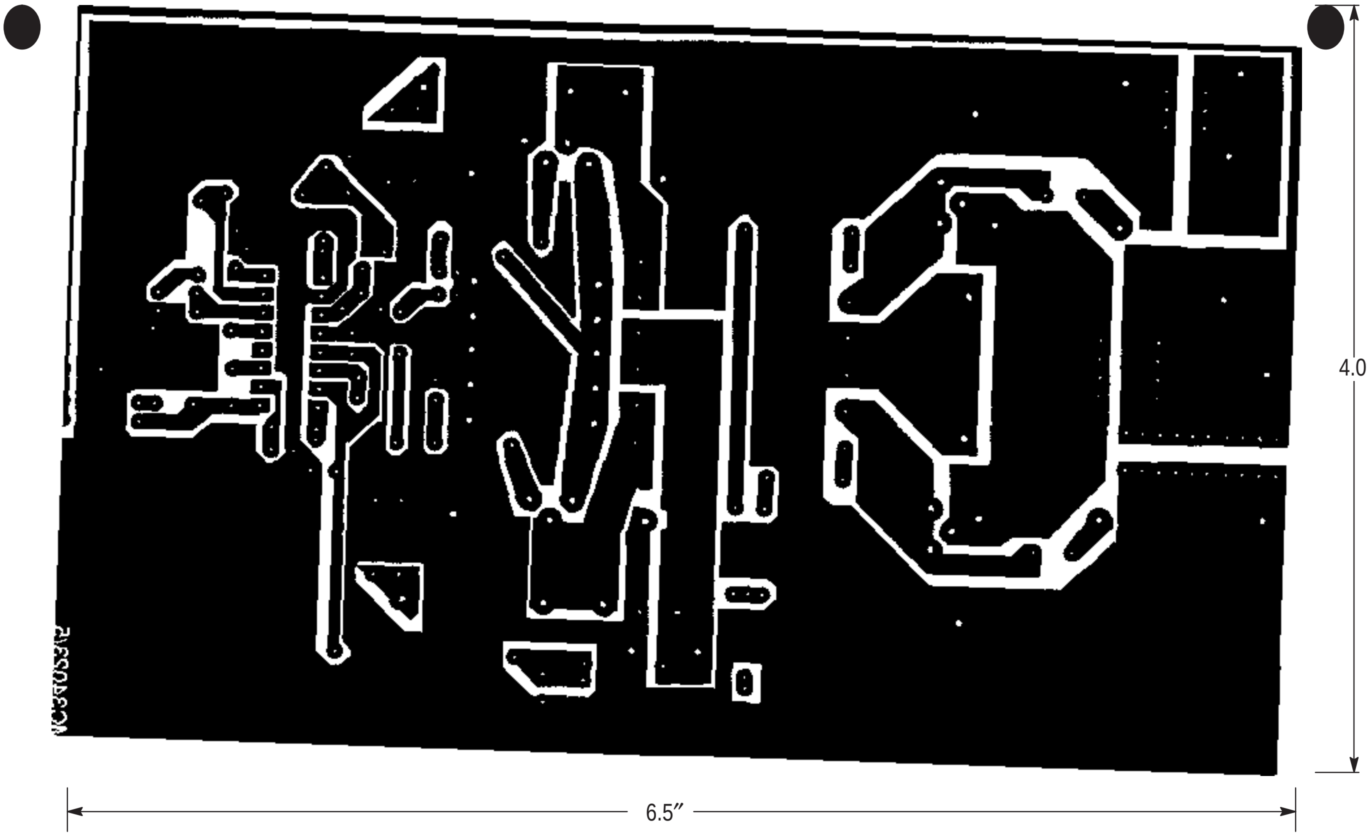


Figure 38. PC Board Without Components



(Top View)



(Bottom View)

MOTOROLA

MC34060A
MC33060A

Precision SWITCHMODE™ Pulse Width Modulator Control Circuit

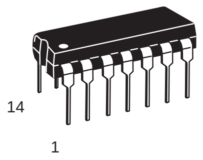
The MC34060A is a low cost fixed frequency, pulse width modulation control circuit designed primarily for single–ended SWITCHMODE power supply control.

The MC34060A is specified over the commercial operating temperature range of 0° to +70°C, and the MC33060A is specified over an automotive temperature range of –40° to +85°C.

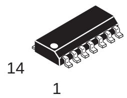
- Complete Pulse Width Modulation Control Circuitry
- On–Chip Oscillator with Master or Slave Operation
- On–Chip Error Amplifiers
- On–Chip 5.0 V Reference, 1.5% Accuracy
- Adjustable Dead–Time Control
- Uncommitted Output Transistor Rated to 200 mA Source or Sink
- Undervoltage Lockout

PRECISION SWITCHMODE PULSE WIDTH MODULATOR CONTROL CIRCUIT

SEMICONDUCTOR TECHNICAL DATA



P SUFFIX
PLASTIC PACKAGE
CASE 646



D SUFFIX
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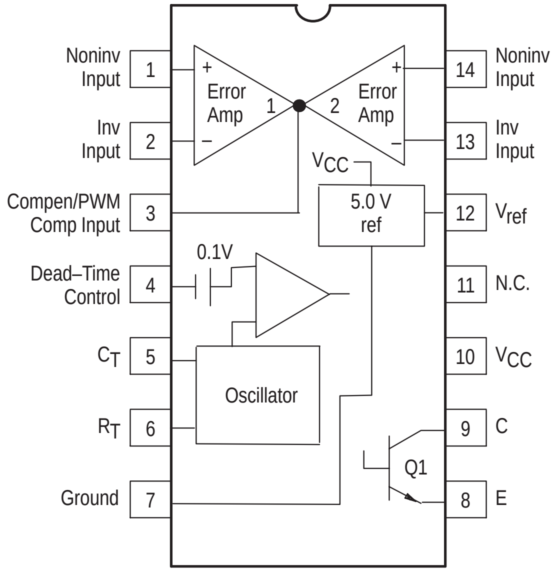
CASE 751A
(SO–14)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC34060AD	T_A = 0° to +70°C	SO–14
MC34060AP		Plastic DIP
MC33060AD	T_A = – 40° to +85°C	SO–14
MC33060AP		Plastic DIP

MAXIMUM RATINGS (Full operating ambient temperature range applies, unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	42	V
Collector Output Voltage	V_C	42	V
Collector Output Current (Note 1)	I_C	500	mA
Amplifier Input Voltage Range	V_{in}	–0.3 to +42	V
Power Dissipation @ $T_A \le 45°C$	P_D	1000	mW
Operating Junction Temperature	T_J	125	°C
Storage Temperature Range	T_{stg}	–55 to +125	°C
Operating Ambient Temperature Range For MC34060A For MC33060A	T_A	 0 to +70 –40 to +85	°C

NOTES: 1. Maximum thermal limits must be observed.

THERMAL CHARACTERISTICS

Characteristics	Symbol	P Suffix Package	D Suffix Package	Unit
Thermal Resistance, Junction–to–Ambient	$R_{\theta JA}$	80	120	°C/W
Derating Ambient Temperature	T_A	45	45	°C

RECOMMENDED OPERATING CONDITIONS

Condition/Value	Symbol	Min	Typ	Max	Unit
Power Supply Voltage	V_{CC}	7.0	15	40	V
Collector Output Voltage	V_C	–	30	40	V
Collector Output Current	I_C	–	–	200	mA
Amplifier Input Voltage	V_{in}	–0.3	–	V_{CC} –2	V
Current Into Feedback Terminal	I_{fb}	–	–	0.3	mA
Reference Output Current	I_{ref}	–	–	10	mA
Timing Resistor	R_T	1.8	47	500	kΩ
Timing Capacitor	C_T	0.00047	0.001	10	µF
Oscillator Frequency	f_{osc}	1.0	25	200	kHz
PWM Input Voltage (Pins 3 and 4)	–	–0.3	–	5.3	V

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V, C_T = 0.01 µF, R_T = 12 kΩ, unless otherwise noted. For typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
REFERENCE SECTION					
Reference Voltage (I_O = 1.0 mA, T_A 25°C) $T_A = T_{low}$ to T_{high} – MC34060A – MC33060A	V_{ref}	4.925 4.9 4.85	5.0 – –	5.075 5.1 5.1	V
Line Regulation (V_{CC} = 7.0 V to 40 V, I_O = 10 mA))	Reg_{line}	–	2.0	25	mV
Load Regulation (I_O = 1.0 mA to 10 mA)	Reg_{load}	–	2.0	15	mV
Short Circuit Output Current (V_{ref} = 0 V)	I_{SC}	15	35	75	mA

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V, C_T = 0.01 µF, R_T = 12 kΩ, unless otherwise noted. For typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
OUTPUT SECTION					
Collector Off–State Current (V_{CC} = 40 V, V_{CE} = 40 V)	$I_{C(off)}$	–	2.0	100	µA
Emitter Off–State Current (V_{CC} = 40 V, V_{CE} = 40 V, V_E = 0 V)	$I_{E(off)}$	–	–	–100	µA
Collector–Emitter Saturation Voltage (Note 2) Common–Emitter (V_E = 0 V, I_C = 200 mA)	$V_{sat(C)}$	–	1.1	1.5	V
Emitter–Follower (V_C = 15 V, I_E = –200 mA)	$V_{sat(E)}$	–	1.5	2.5	
Output Voltage Rise Time (T_A = 25°C)	t_r				ns
Common–Emitter (See Figure 12)		–	100	200	
Emitter–Follower (See Figure 13)		–	100	200	
Output Voltage Fall Time (T_A = 25°C)	t_r				ns
Common–Emitter (See Figure 12		–	40	100	
Emitter–Follower (See Figure 13)		–	40	100	
ERROR AMPLIFIER SECTION					
Input Offset Voltage ($V_{O[Pin\ 3]}$ = 2.5 V)	V_{IO}	–	2.0	10	mV
Input Offset Current ($V_{C[Pin\ 3]}$ = 2.5 V)	I_{IO}	–	5.0	250	nA
Input Bias current ($V_{O[Pin\ 3]}$ = 2.5 V)	I_{IB}	–	–0.1	–2.0	µA
Input Common Mode Voltage Range (V_{CC} = 40 V)	V_{ICR}	0 to V_{CC} –2.0	–	–	V
Inverting Input Voltage Range	$V_{IR(INV)}$	–0.3 to V_{CC}–2.0	–	–	V
Open–Loop Voltage Gain (ΔV_O = 3.0 V, V_O = 0.5 V to 3.5 V, R_L = 2.0 kΩ)	A_{VOL}	70	95	–	dB
Unity–Gain Crossover Frequency (V_O = 0.5 V to 3.5 V, R_L = 2.0 kΩ)	f_c	–	600	–	kHz
Phase Margin at Unity–Gain (V_O = 0.5 V to 3.5 V, R_L = 2.0 kΩ)	ϕ_m	–	65	–	deg.
Common Mode Rejection Ratio (V_{CC} = 40 V, V_{in} = 0 V to 38 V))	CMRR	65	90	–	dB
Power Supply Rejection Ratio (ΔV_{CC} = 33 V, V_O = 2.5 V, R_L = 2.0 kΩ)	PSRR	–	100	–	dB
Output Sink Current ($V_{O[Pin\ 3]}$ = 0.7 V)	I_O–	0.3	0.7	–	mA
Output Source Current ($V_{O[Pin\ 3]}$ = 3.5 V)	I_O+	–2.0	–4.0	–	mA

NOTES: 2. Low duty cycle techniques are used during test to maintain junction temperature as close to ambient temperatures as possible.

T_{low} = –40°C for MC33060A
= 0°C for MC34060A

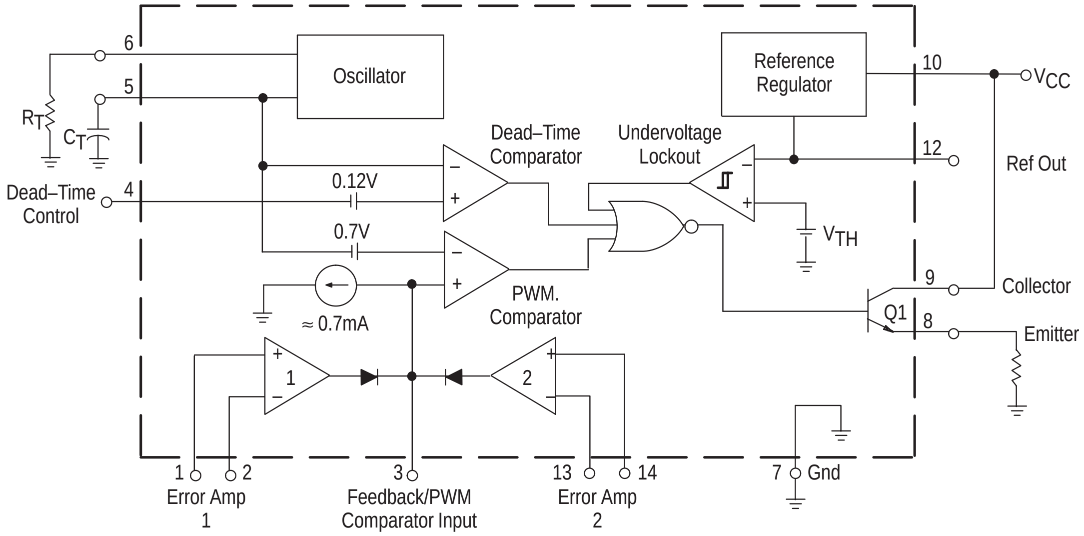
T_{high} = +85°C for MC33060A
= +70°Cfor MC34060A

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V, C_T = 0.01 µF, R_T = 12 kΩ, unless otherwise noted. For typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
PWM COMPARATOR SECTION (Test circuit Figure 11)					
Input Threshold Voltage (Zero Duty Cycle)	V_{TH}	–	3.5	4.5	V
Input Sink Current ($V_{[Pin\ 3]}$ = 0.7 V)	I_I	0.3	0.7	–	mA
DEAD–TIME CONTROL SECTION (Test circuit Figure 11)					
Input Bias Current (Pin 4) (V_{in} = 0 V to 5.25 V)	$I_{IB(DT)}$	–	–1.0	–10	µA
Maximum Output Duty Cycle (V_{in} = 0 V, C_T = 0.01 µF, R_T = 12 kΩ) (V_{in} = 0 V, C_T = 0.001 µF, R_T = 47 kΩ)	DC_{max}	 90 –	 96 92	 100 –	%
Input Threshold Voltage (Pin 4) (Zero Duty Cycle) (Maximum Duty Cycle)	V_{TH}	 – 0	 2.8 –	 3.3 –	V
OSCILLATOR SECTION					
Frequency (C_T = 0.01 µF, R_T = 12 kΩ, T_A = 25°C) T_A = T_{low} to T_{high} – MC34060A – MC33060A (C_T = 0.001 µF, R_T = 47 kΩ)	f_{osc}	 9.7 9.5 9.0 –	 10.5 – – 25	 11.3 11.5 11.5 –	kHz
Standard Deviation of Frequency* (C_T = 0.001 µF, R_T = 47 kΩ)	σf_{osc}	–	1.5	–	%
Frequency Change with Voltage (V_{CC} = 7.0 V to 40 V)	$\Delta f_{osc}(\Delta V)$	–	0.5	2.0	%
Frequency Change with Temperature (ΔT_A = T_{low} to T_{high}) (C_T = 0.01 µF, R_T = 12 kΩ)	$\Delta f_{osc}(\Delta T)$	 – –	 4.0 –	 – –	%
UNDERVOLTAGE LOCKOUT SECTION					
Turn–On Threshold (V_{CC} increasing, I_{ref} = 1.0 mA)	V_{th}	4.0	4.7	5.5	V
Hysteresis	V_H	50	150	300	mV
TOTAL DEVICE					
Standby Supply Current (Pin 6 at V_{ref}, all other inputs and outputs open) (V_{CC} = 15 V) (V_{CC} = 40 V)	I_{CC}	 – –	 5.5 7.0	 10 15	mA
Average Supply Current ($V_{[Pin\ 4]}$ = 2.0 V, C_T = 0.001 µF, R_T = 47 kΩ). See Figure 11.	I_S	–	7.0	–	mA

*Standard deviation is a measure of the statistical distribution about the mean as derived from the formula; $\sigma = \sqrt{\frac{\begin{array}{l}\overset{N}{\Sigma}\,(x_n - x)^2\\ n-1\end{array}}{N-1}}$

Figure 1. Block Diagram



This device contains 46 active transistors.

Description

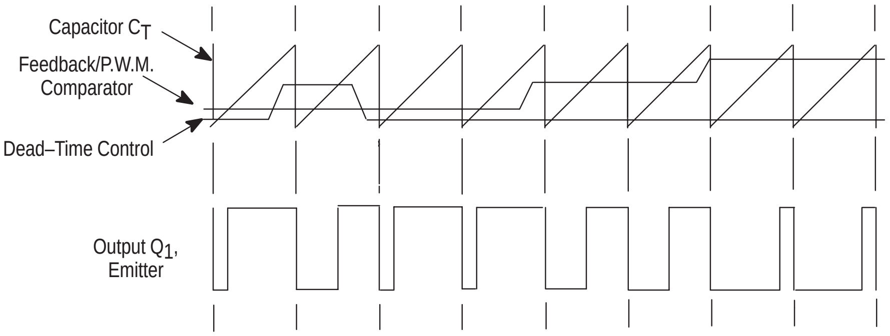
The MC34060A is a fixed–frequency pulse width modulation control circuit, incorporating the primary building blocks required for the control of a switching power supply (see Figure 1). An internal–linear sawtooth oscillator is frequency–programmable by two external components, R_T and C_T. The approximate oscillator frequency is determined by:

$$f_{osc} \cong \frac{1.2}{R_T \bullet C_T}$$

For more information refer to Figure 3.

Output pulse width modulation is accomplished by comparison of the positive sawtooth waveform across capacitor C_T to either of two control signals. The output is enabled only during that portion of time when the sawtooth voltage is greater than the control signals. Therefore, an increase in control–signal amplitude causes a corresponding linear decrease of output pulse width. (Refer to the Timing Diagram shown in Figure 2.)

Figure 2. Timing Diagram



APPLICATIONS INFORMATION

The control signals are external inputs that can be fed into the dead–time control, the error amplifier inputs, or the feed–back input. The dead–time control comparator has an effective 120 mV input offset which limits the minimum output dead time to approximately the first 4% of the sawtooth–cycle time. This would result in a maximum duty cycle of 96%. Additional dead time may be imposed on the output by setting the dead time–control input to a fixed voltage, ranging between 0 V to 3.3 V.

The pulse width modulator comparator provides a means for the error amplifiers to adjust the output pulse width from the maximum percent on–time, established by the dead time control input, down to zero, as the voltage at the feedback pin varies from 0.5 V to 3.5 V. Both error amplifiers have a common mode input range from –0.3 V to (V_{CC} –2.0 V), and may be used to sense power supply output voltage and current. The error–amplifier outputs are active high and are ORed together at the noninverting input of the pulse–width modulator comparator. With this configuration, the amplifier that demands minimum output on time, dominates control of the loop.

The MC34060A has an internal 5.0 V reference capable of sourcing up to 10 mA of load currents for external bias circuits. The reference has an internal accuracy of ±5% with a typical thermal drift of less than 50 mV over an operating temperature range of 0° to +70°C.

Figure 3. Oscillator Frequency versus Timing Resistance

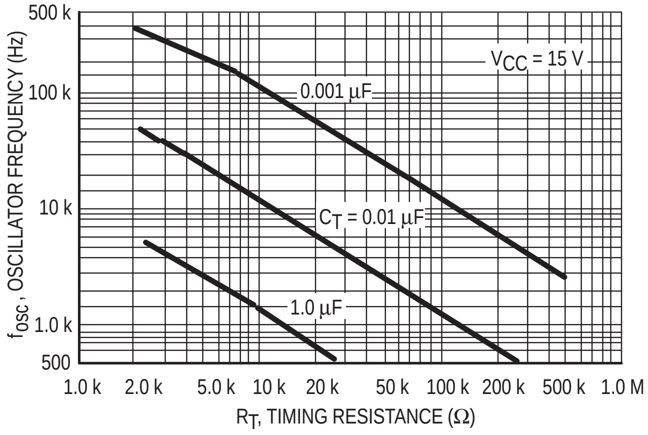


Figure 4. Open Loop Voltage Gain and Phase versus Frequency

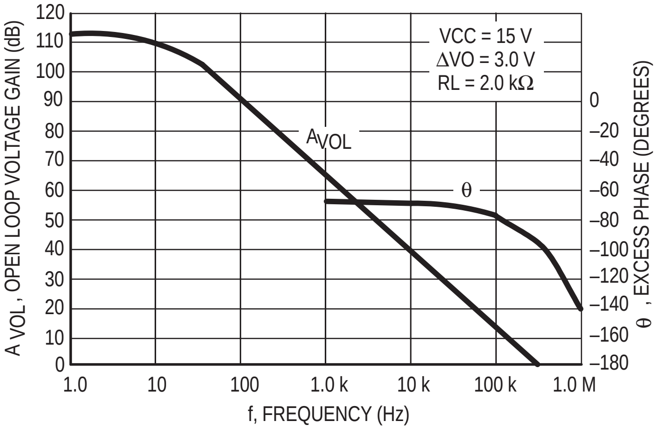


Figure 5. Percent Deadtime versus Oscillator Frequency

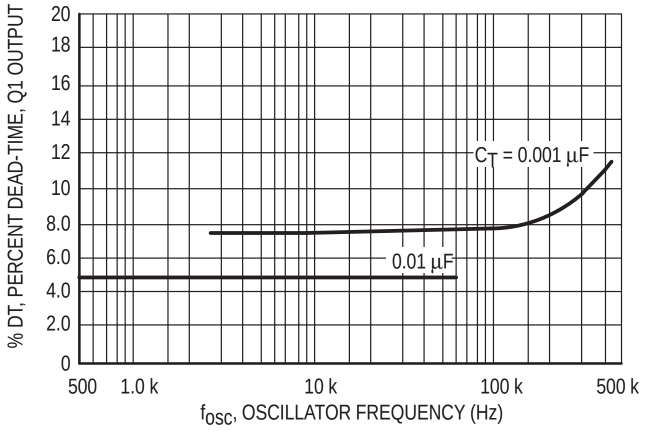


Figure 6. Percent Duty Cycle versus Dead–Time Control Voltage

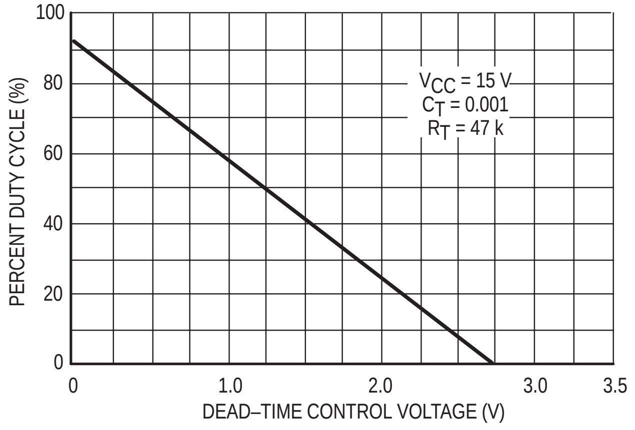


Figure 7. Emitter–Follower Configuration Output Saturation Voltage versus Emitter Current

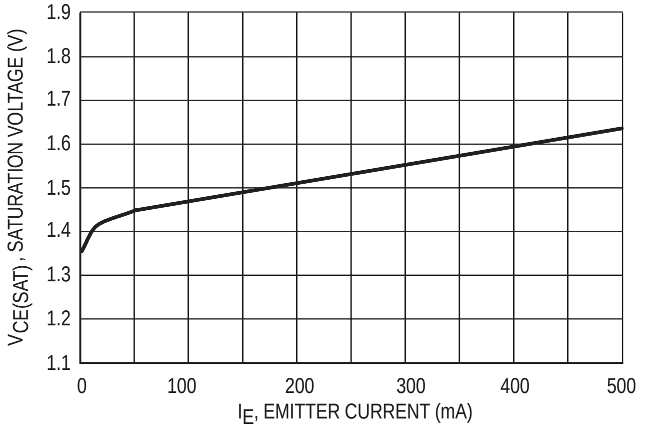


Figure 8. Common–Emitter Configuration Output Saturation Voltage versus Collector Current

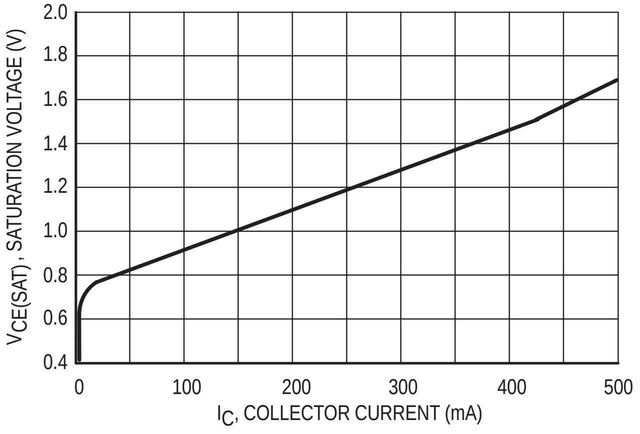


Figure 9. Standby Supply Current versus Supply Voltage

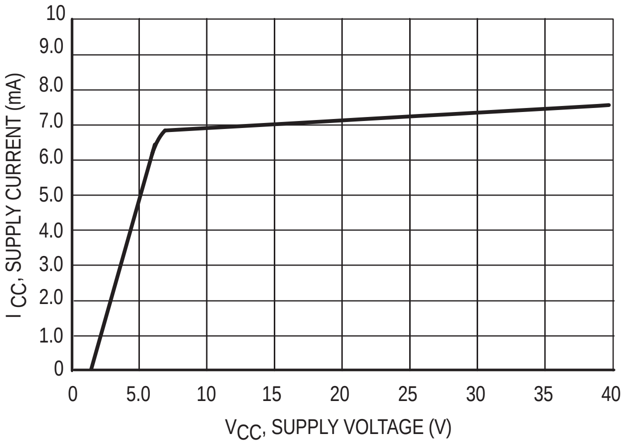


Figure 10. Undervoltage Lockout Thresholds versus Reference Load Current

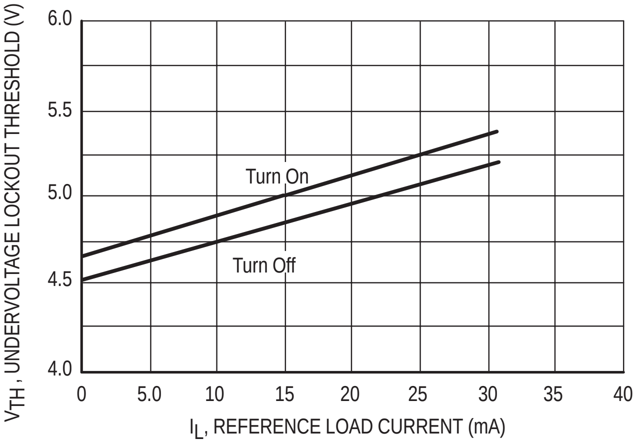


Figure 11. Error Amplifier Characteristics

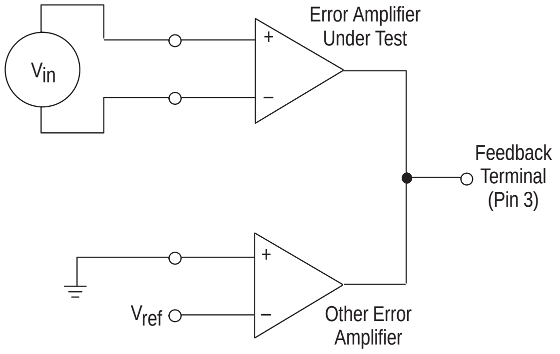


Figure 12. Deadtime and Feedback Control

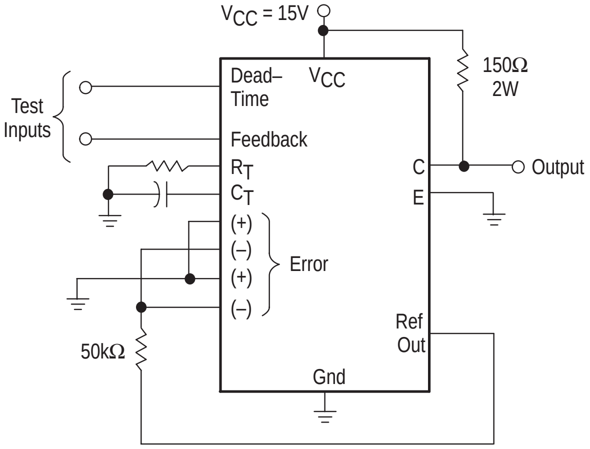


Figure 13. Common–Emitter Configuration and Waveform

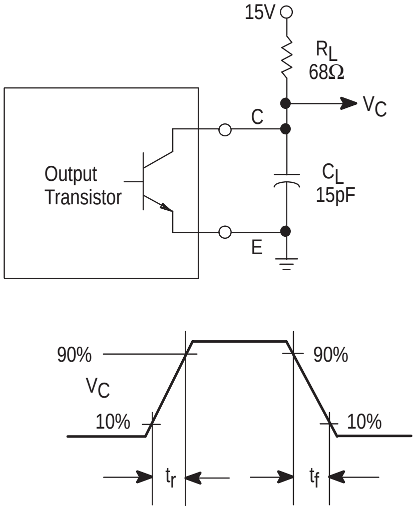


Figure 14. Emitter–Follower Configuration and Waveform

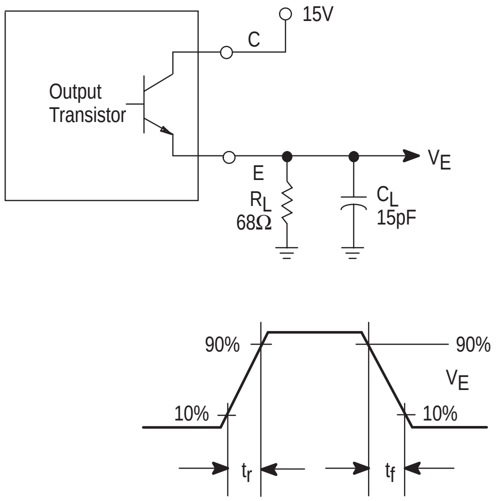


Figure 15. Error Amplifier Sensing Techniques

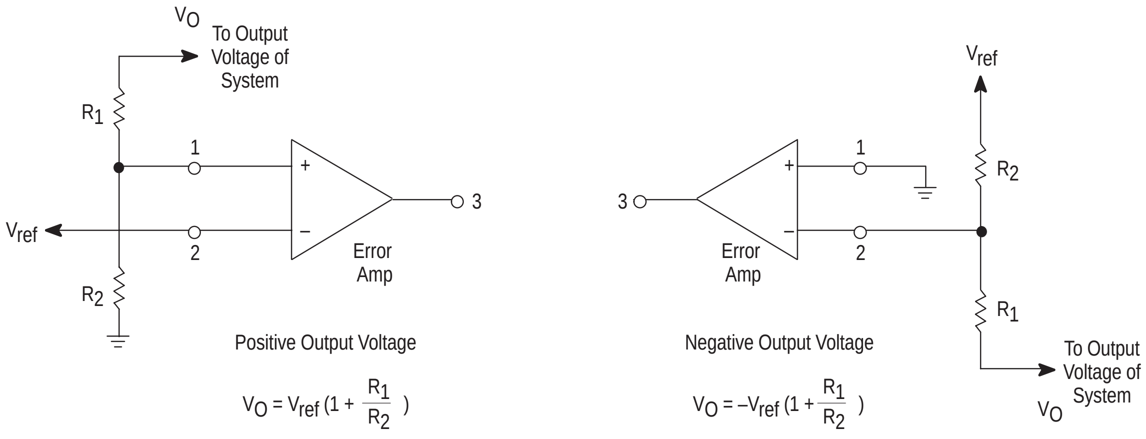


Figure 16. Deadtime Control Circuit

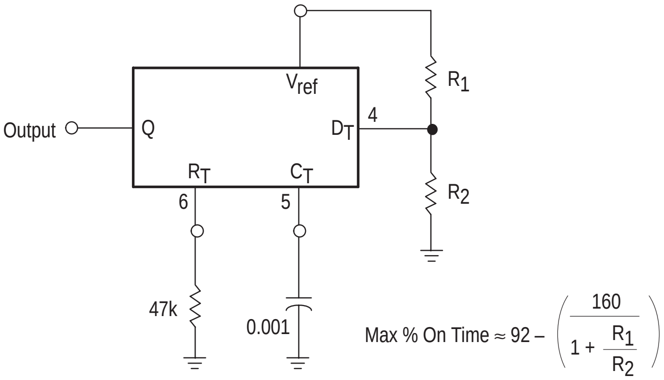


Figure 17. Soft–Start Circuit

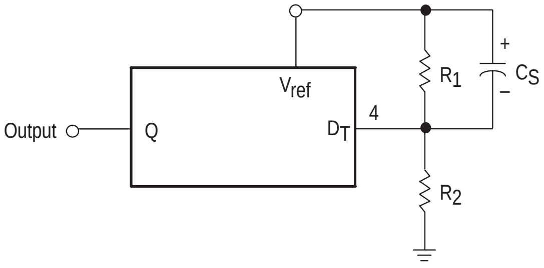


Figure 18. Slaving Two or More Control Circuits

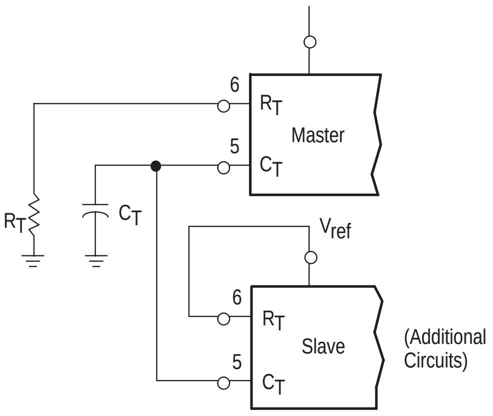
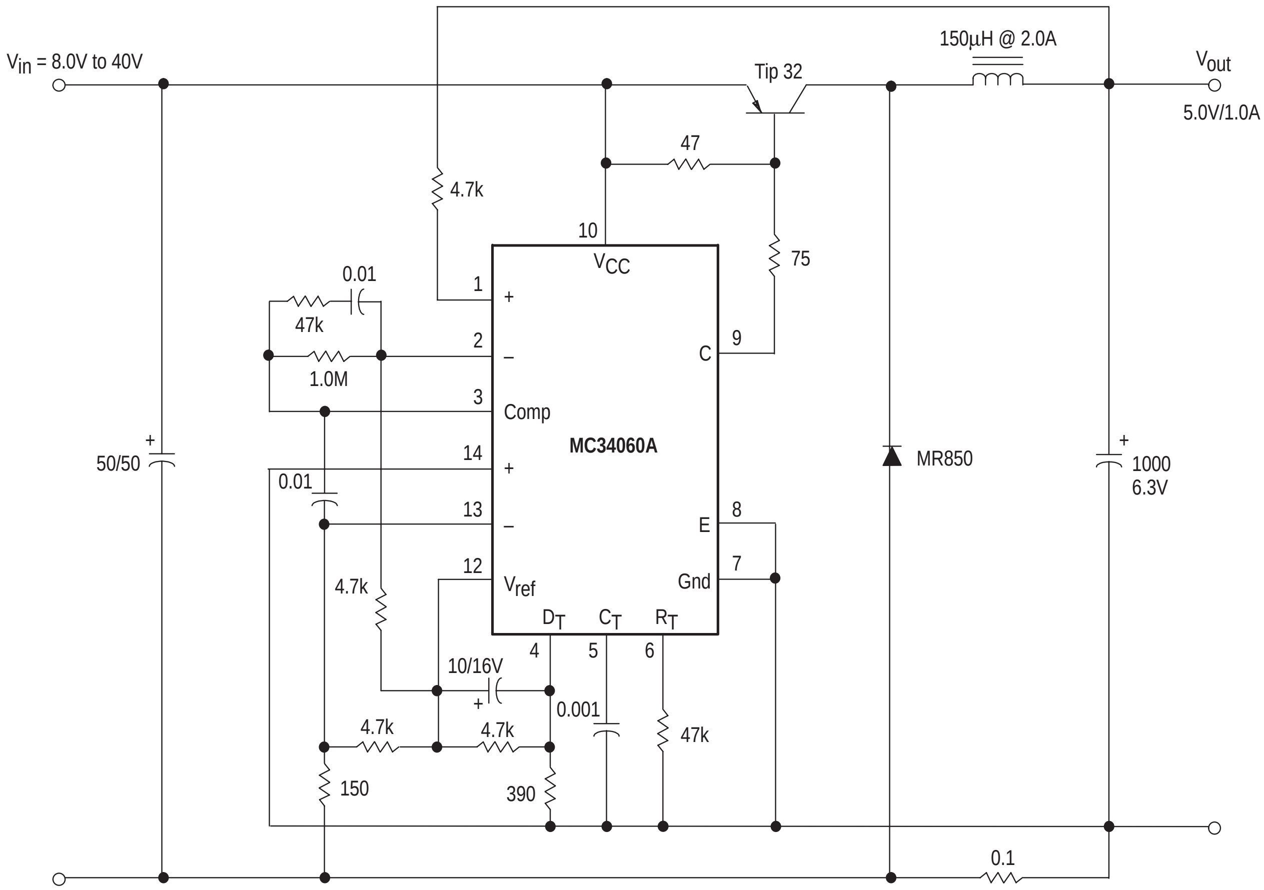
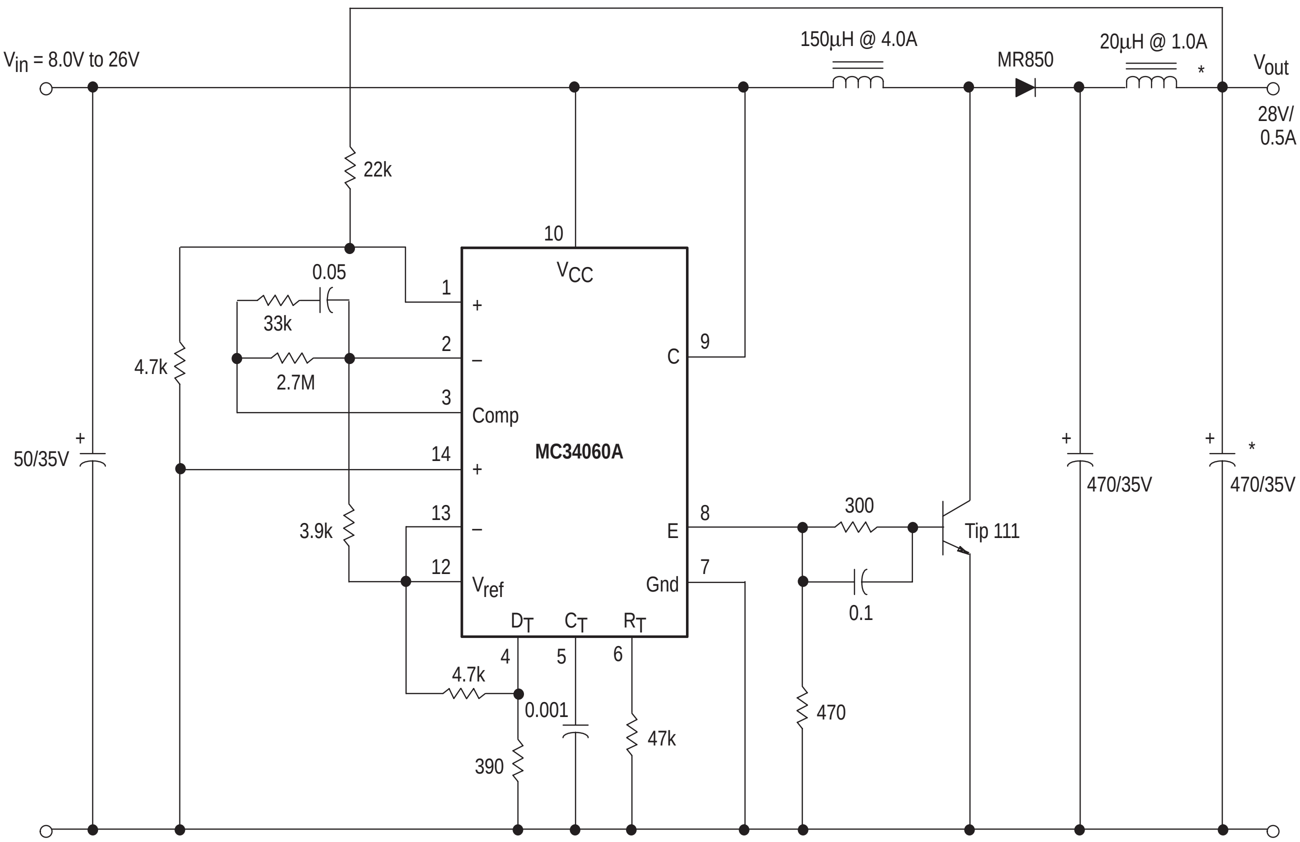


Figure 19. Step–Down Converter with Soft–Start and Output Current Limiting



Test	Conditions	Results
Line Regulation	V_{in} = 8.0 V to 40 V, I_O = 1.0 A	25 mV 0.5%
Load Regulation	V_{in} = 12 V, I_O = 1.0 mA to 1.0 A	3.0 mV 0.06%
Output Ripple	V_{in} = 12 V, I_O = 1.0 A	75 mV p–p P.A.R.D.
Short Circuit Current	V_{in} = 12 V, R_L = 0.1 Ω	1.6 A
Efficiency	V_{in} = 12 V, I_O = 1.0 A	73%

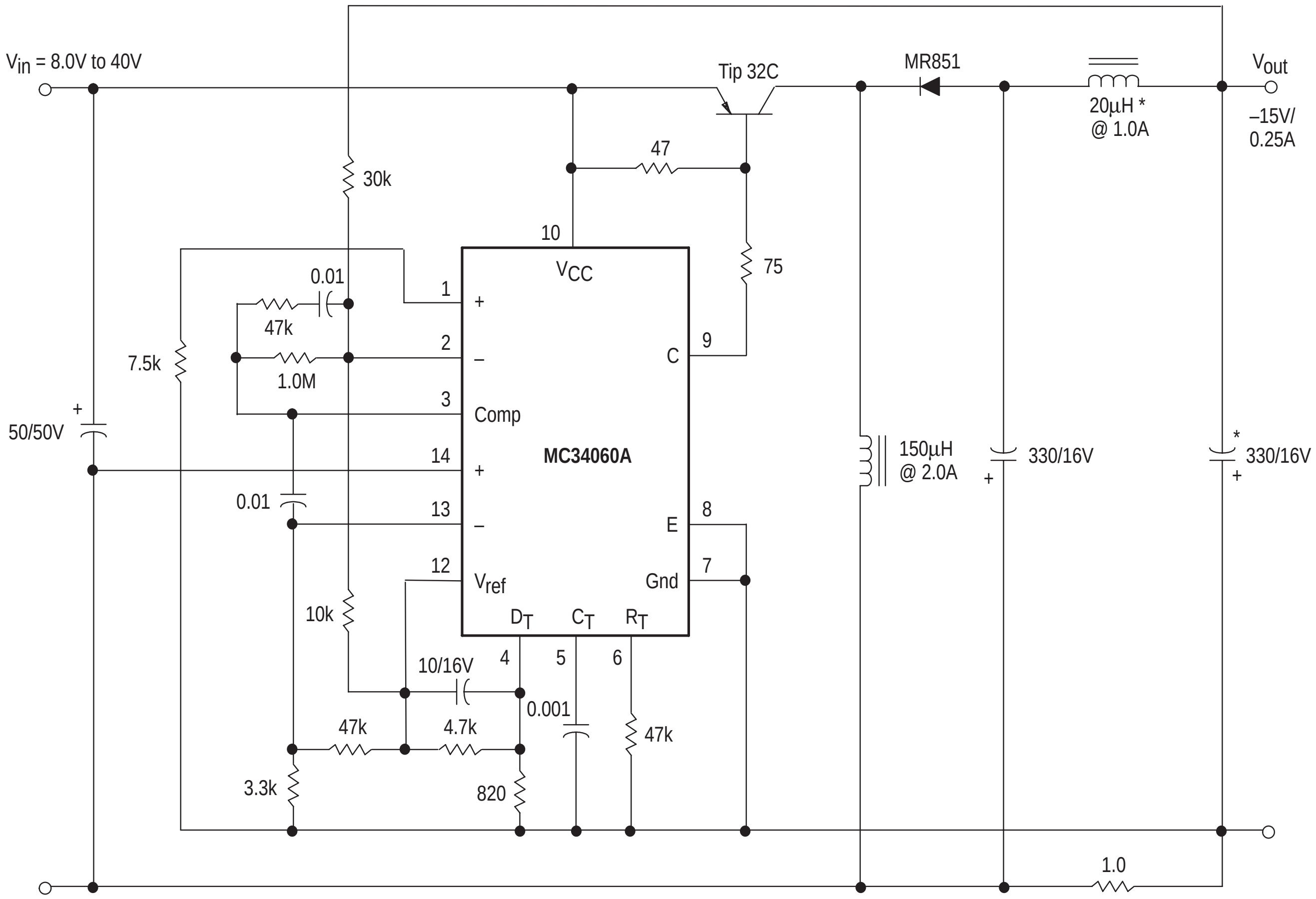
Figure 20. Step–Up Converter



Test	Conditions	Results
Line Regulation	V_{in} = 8.0 V to 26 V, I_O = 0.5 A	40 mV 0.14%
Load Regulation	V_{in} = 12 V, I_O = 1.0 mA to 0.5 A	5.0 mV 0.18%
Output Ripple	V_{in} = 12 V, I_O = 0.5 A	24 mV p–p P.A.R.D.
Efficiency	V_{in} = 12 V, I_O = 0.5 A	75%

* Optional circuit to minimize output ripple

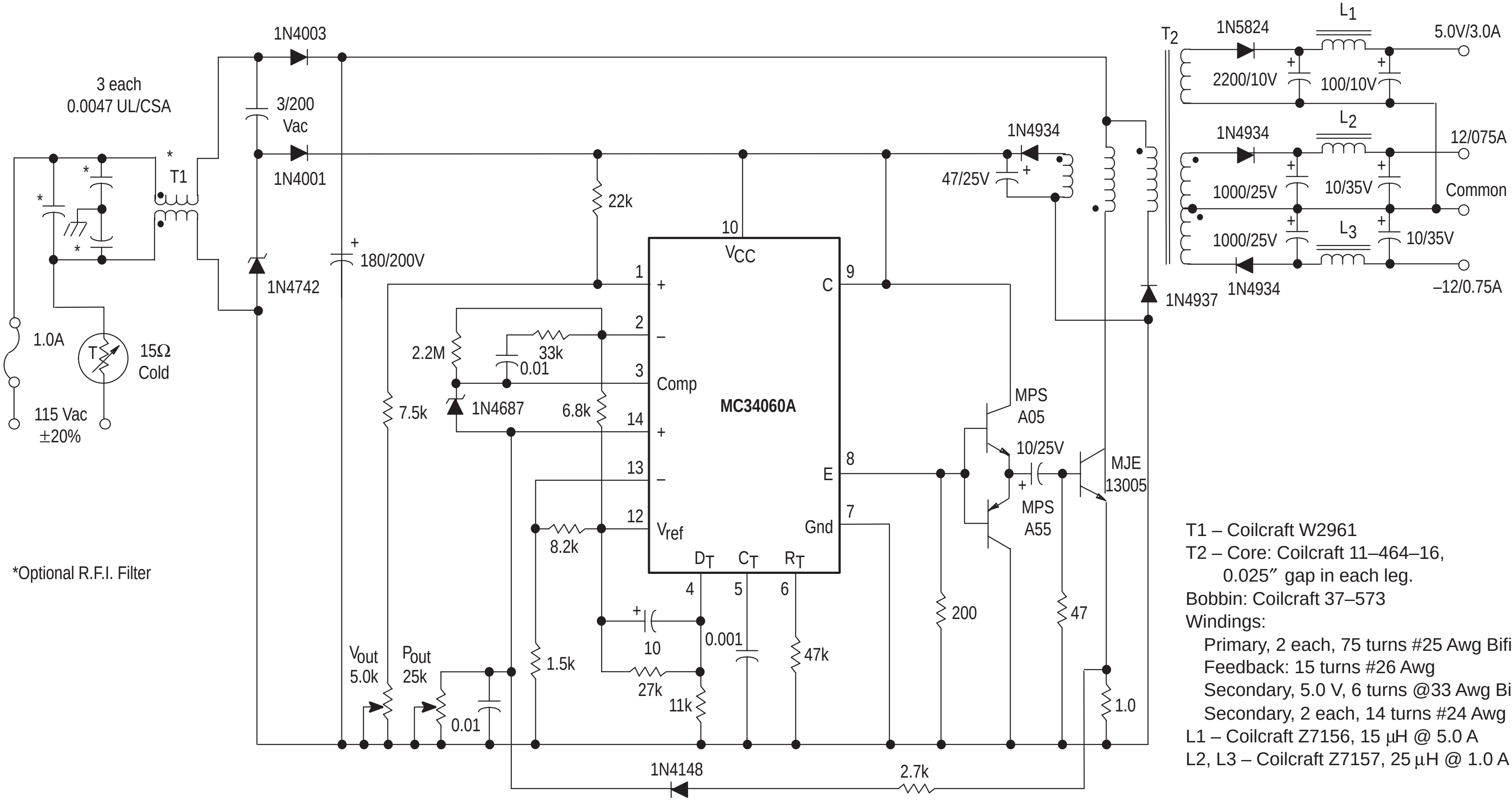
Figure 21. Step–Up/Down Voltage Inverting Converter
with Soft–Start and Current Limiting



Test	Conditions	Results
Line Regulation	V_{in} = 8.0 V to 40 V, I_O = 250 mA	52 mV 0.35%
Load Regulation	V_{in} = 12 V, I_O = 1.0 to 250 mA	47 mV 0.32%
Output Ripple	V_{in} = 12 V, I_O = 250 mA	10 mV p–p P.A.R.D.
Short Circuit Current	V_{in} = 12 V, R_L = 0.1 Ω	330 mA
Efficiency	V_{in} = 12 V, I_O = 250 mA	86%

* Optional circuit to minimize output ripple

Figure 22. 33 W Off–Line Flyback Converter with Soft–Start and Primary Power Limiting



*Optional R.F.I. Filter

T1 – Coilcraft W2961
T2 – Core: Coilcraft 11–464–16,
0.025″ gap in each leg.
Bobbin: Coilcraft 37–573
Windings:
Primary, 2 each, 75 turns #25 Awg Bifilar wound
Feedback: 15 turns #26 Awg
Secondary, 5.0 V, 6 turns @33 Awg Bifilar wound
Secondary, 2 each, 14 turns #24 Awg Bifilar wound
L1 – Coilcraft Z7156, 15 µH @ 5.0 A
L2, L3 – Coilcraft Z7157, 25 µH @ 1.0 A

Test	Conditions	Results
Line Regulation 5.0 V	V_{in} = 95 Vac to 135 Vac, I_O = 3.0 A	20 mV 0.40%
Line Regulation ±12 V	V_{in} = 95 Vac to 135 Vac, I_O = ±0.75 A	52 mV 0.26%
Load Regulation 5.0 V	V_{in} = 115 Vac, I_O = 1.0 A to 4.0 A	476 mV 9.5%
Load Regulation ±12 V	V_{in} = 115 Vac, I_O = ±0.4 A to ±0.9 A	300 mV 2.5%
Output Ripple 5.0 V	V_{in} = 115 Vac, I_O = 3.0 A	45 mV p–p P.A.R.D.
Output Ripple ±12 V	V_{in} = 115 Vac, I_O = ±0.75 A	75 mV p–p P.A.R.D.
Efficiency	V_{in} = 115 Vac, I_O 5.0 V = 3.0 A I_O ±12 V = ±0.75 A	74%

MOTOROLA

MC34063A
MC33063A

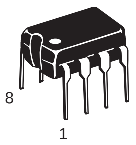
DC-to-DC Converter Control Circuits

DC–to–DC CONVERTER CONTROL CIRCUITS

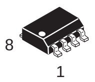
SEMICONDUCTOR TECHNICAL DATA

The MC34063A Series is a monolithic control circuit containing the primary functions required for DC–to–DC converters. These devices consist of an internal temperature compensated reference, comparator, controlled duty cycle oscillator with an active current limit circuit, driver and high current output switch. This series was specifically designed to be incorporated in Step–Down and Step–Up and Voltage–Inverting applications with a minimum number of external components. Refer to Application Notes AN920A/D and AN954/D for additional design information.

- Operation from 3.0 V to 40 V Input
- Low Standby Current
- Current Limiting
- Output Switch Current to 1.5 A
- Output Voltage Adjustable
- Frequency Operation to 100 kHz
- Precision 2% Reference

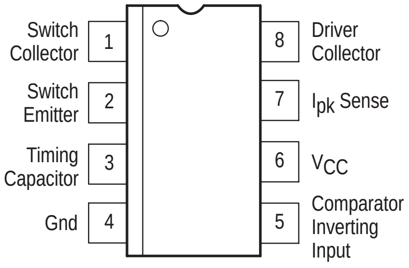


P, P1 SUFFIX
PLASTIC PACKAGE
CASE 626



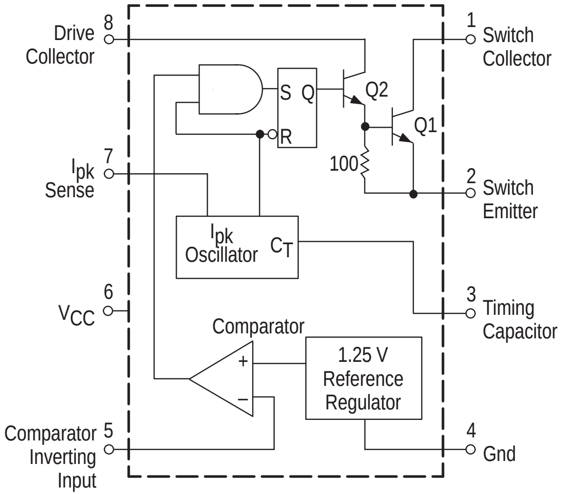
D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

PIN CONNECTIONS



(Top View)

Representative Schematic Diagram



(Bottom View)

This device contains 51 active transistors.

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC33063AD	T_A = – 40° to +85°C	SO–8
MC33063AP1		Plastic DIP
MC33063AVD	T_A = –40° to +125°C	SO–8
MC33063AVP		Plastic DIP
MC34063AD	T_A = 0° to +70°C	SO–8
MC34063AP1		Plastic DIP

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	40	Vdc
Comparator Input Voltage Range	V_{IR}	–0.3 to +40	Vdc
Switch Collector Voltage	$V_{C(switch)}$	40	Vdc
Switch Emitter Voltage ($V_{Pin\ 1}$ = 40 V)	$V_{E(switch)}$	40	Vdc
Switch Collector to Emitter Voltage	$V_{CE(switch)}$	40	Vdc
Driver Collector Voltage	$V_{C(driver)}$	40	Vdc
Driver Collector Current (Note 1)	$I_{C(driver)}$	100	mA
Switch Current	I_{SW}	1.5	A
Power Dissipation and Thermal Characteristics			
Plastic Package, P, P1 Suffix			
T_A = 25°C	P_D	1.25	W
Thermal Resistance	$R_{\theta JA}$	100	°C/W
SOIC Package, D Suffix			
T_A = 25°C	P_D	625	W
Thermal Resistance	$R_{\theta JA}$	160	°C/W
Operating Junction Temperature	T_J	+150	°C
Operating Ambient Temperature Range	T_A		°C
MC34063A		0 to +70	
MC33063AV		–40 to +125	
MC33063A		–40 to +85	
Storage Temperature Range	T_{stg}	–65 to +150	°C

NOTES: 1. Maximum package power dissipation limits must be observed.
2. ESD data available upon request.

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, $T_A = T_{low}$ to T_{high} [Note 3], unless otherwise specified.)

Characteristics	Symbol	Min	Typ	Max	Unit
OSCILLATOR					
Frequency ($V_{Pin\ 5}$ = 0 V, C_T = 1.0 nF, T_A = 25°C)	f_{osc}	24	33	42	kHz
Charge Current (V_{CC} = 5.0 V to 40 V, T_A = 25°C)	I_{chg}	24	35	42	µA
Discharge Current (V_{CC} = 5.0 V to 40 V, T_A = 25°C)	I_{dischg}	140	220	260	µA
Discharge to Charge Current Ratio (Pin 7 to V_{CC}, T_A = 25°C)	I_{dischg}/I_{chg}	5.2	6.5	7.5	–
Current Limit Sense Voltage ($I_{chg} = I_{dischg}$, T_A = 25°C)	$V_{ipk(sense)}$	250	300	350	mV
OUTPUT SWITCH (Note 4)					
Saturation Voltage, Darlington Connection (Note 5) (I_{SW} = 1.0 A, Pins 1, 8 connected)	$V_{CE(sat)}$	–	1.0	1.3	V
Saturation Voltage, Darlington Connection (I_{SW} = 1.0 A, $R_{Pin\ 8}$ = 82 Ω to V_{CC}, Forced $\beta \simeq 20$)	$V_{CE(sat)}$	–	0.45	0.7	V
DC Current Gain (I_{SW} = 1.0 A, V_{CE} = 5.0 V, T_A = 25°C)	h_{FE}	50	75	–	–
Collector Off–State Current (V_{CE} = 40 V)	$I_{C(off)}$	–	0.01	100	µA

NOTES: 3. T_{low} = 0°C for MC34063A, –40°C for MC33063A, AV T_{high} = +70°C for MC34063A, +85°C for MC33063A, +125°C for MC33063AV
4. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient temperature as possible.
5. If the output switch is driven into hard saturation (non–Darlington configuration) at low switch currents (≤ 300 mA) and high driver currents (≥ 30 mA), it may take up to 2.0 µs for it to come out of saturation. This condition will shorten the off time at frequencies ≥ 30 kHz, and is magnified at high temperatures. This condition does not occur with a Darlington configuration, since the output switch cannot saturate. If a non–Darlington configuration is used, the following output drive condition is recommended:

$$\text{Forced } \beta \text{ of output switch} : \frac{I_C \text{ output}}{I_C \text{ driver} - 7.0 \text{ mA}^*} \geq 10$$

*The 100 Ω resistor in the emitter of the driver device requires about 7.0 mA before the output switch conducts.

ELECTRICAL CHARACTERISTICS (continued) (V_{CC} = 5.0 V, T_A = T_{low} to T_{high} [Note 3], unless otherwise specified.)

Characteristics	Symbol	Min	Typ	Max	Unit
COMPARATOR					
Threshold Voltage	V_{th}				V
T_A = 25°C		1.225	1.25	1.275	
T_A = T_{low} to T_{high}		1.21	–	1.29	
Threshold Voltage Line Regulation (V_{CC} = 3.0 V to 40 V)	Reg_{line}				mV
MC33063A, MC34063A		–	1.4	5.0	
MC33363AV		–	1.4	6.0	
Input Bias Current (V_{in} = 0 V)	I_{IB}	–	–20	–400	nA
TOTAL DEVICE					
Supply Current (V_{CC} = 5.0 V to 40 V, C_T = 1.0 nF, Pin 7 = V_{CC}, $V_{Pin\ 5}$ > V_{th}, Pin 2 = Gnd, remaining pins open)	I_{CC}	–	–	4.0	mA

NOTES: 3. T_{low} = 0°C for MC34063A, –40°C for MC33063A, AV T_{high} = +70°C for MC34063A, +85°C for MC33063A, +125°C for MC33063AV

4. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient temperature as possible.

5. If the output switch is driven into hard saturation (non–Darlington configuration) at low switch currents (≤ 300 mA) and high driver currents (≥ 30 mA), it may take up to 2.0 µs for it to come out of saturation. This condition will shorten the off time at frequencies ≥ 30 kHz, and is magnified at high temperatures. This condition does not occur with a Darlington configuration, since the output switch cannot saturate. If a non–Darlington configuration is used, the following output drive condition is recommended:

$$\text{Forced } \beta \text{ of output switch : } \frac{I_C \text{ output}}{I_C \text{ driver} - 7.0 \text{ mA}^*} \geq 10$$

*The 100 Ω resistor in the emitter of the driver device requires about 7.0 mA before the output switch conducts.

Figure 1. Output Switch On–Off Time versus Oscillator Timing Capacitor

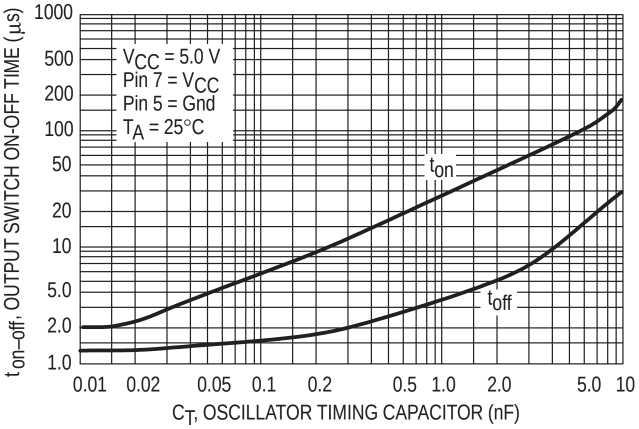


Figure 2. Timing Capacitor Waveform

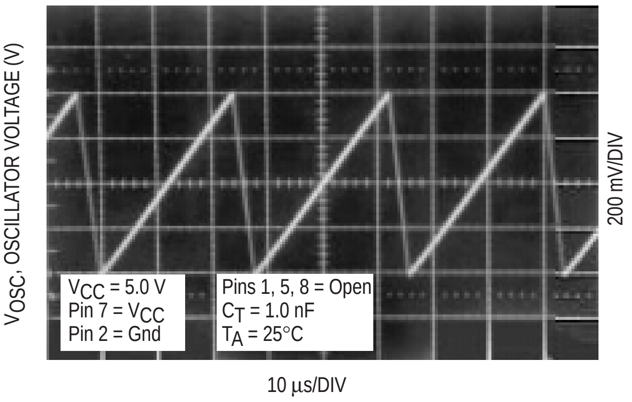


Figure 3. Emitter Follower Configuration Output Saturation Voltage versus Emitter Current

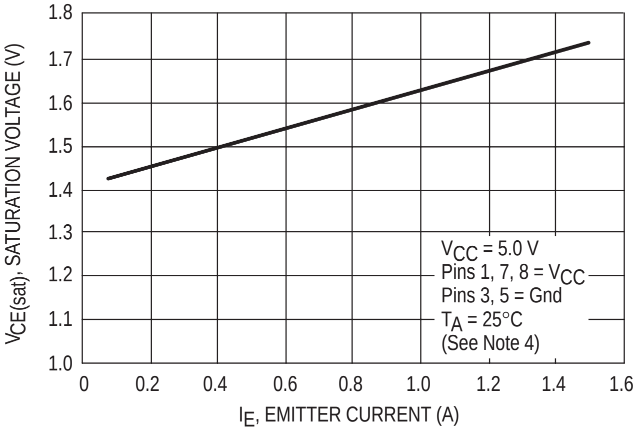


Figure 4. Common Emitter Configuration Output Switch Saturation Voltage versus Collector Current

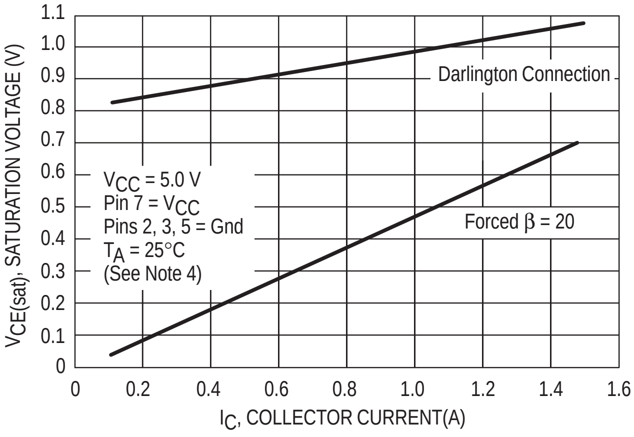


Figure 5. Current Limit Sense Voltage versus Temperature

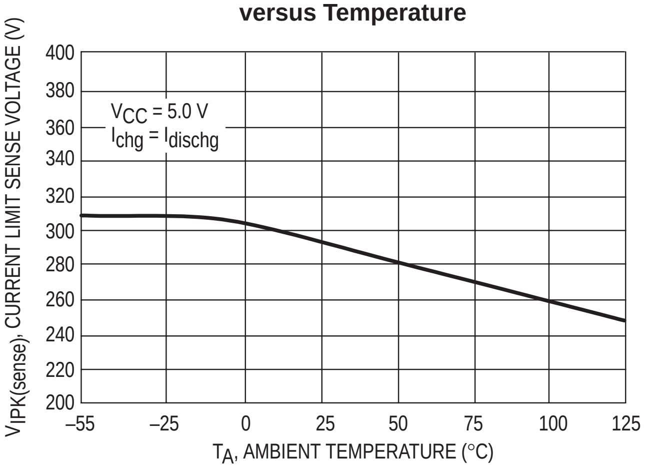
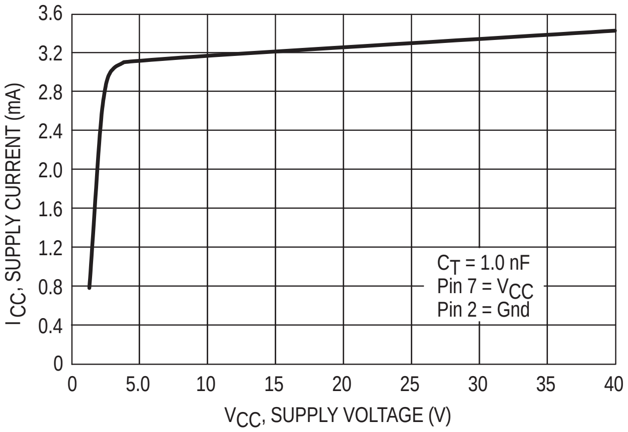
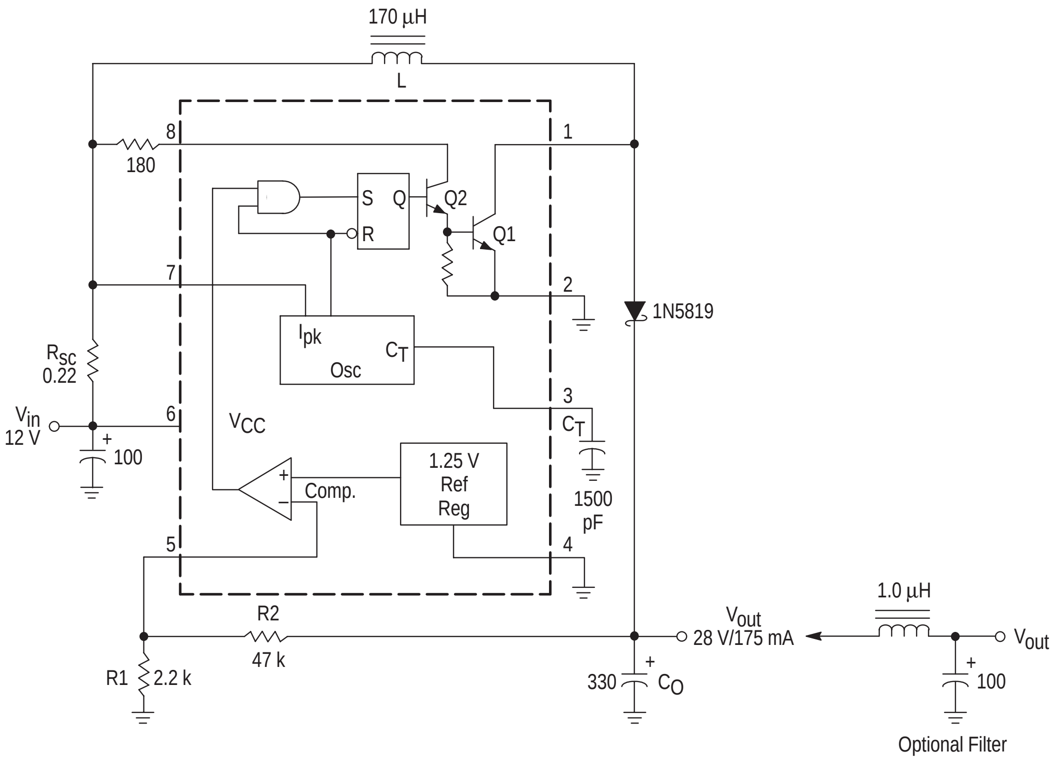


Figure 6. Standby Supply Current versus Supply Voltage



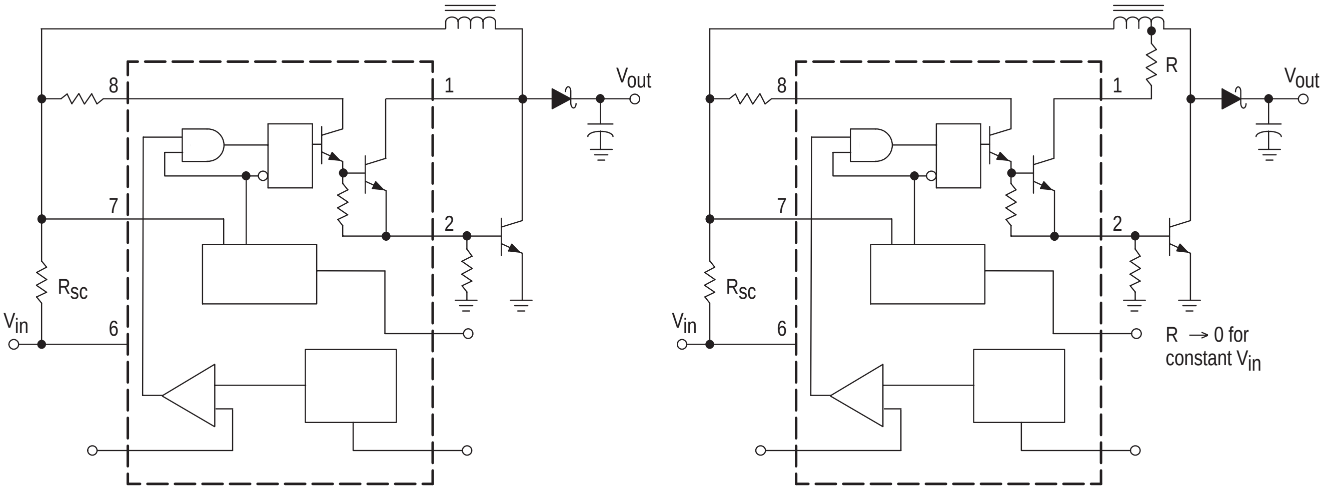
NOTE: 4. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient temperature as possible.

Figure 7. Step–Up Converter



Test	Conditions	Results
Line Regulation	V_{in} = 8.0 V to 16 V, I_O = 175 mA	30 mV = ±0.05%
Load Regulation	V_{in} = 12 V, I_O = 75 mA to 175 mA	10 mV = ±0.017%
Output Ripple	V_{in} = 12 V, I_O = 175 mA	400 mVpp
Efficiency	V_{in} = 12 V, I_O = 175 mA	87.7%
Output Ripple With Optional Filter	V_{in} = 12 V, I_O = 175 mA	40 mVpp

Figure 8. External Current Boost Connections for I_C Peak Greater than 1.5 A



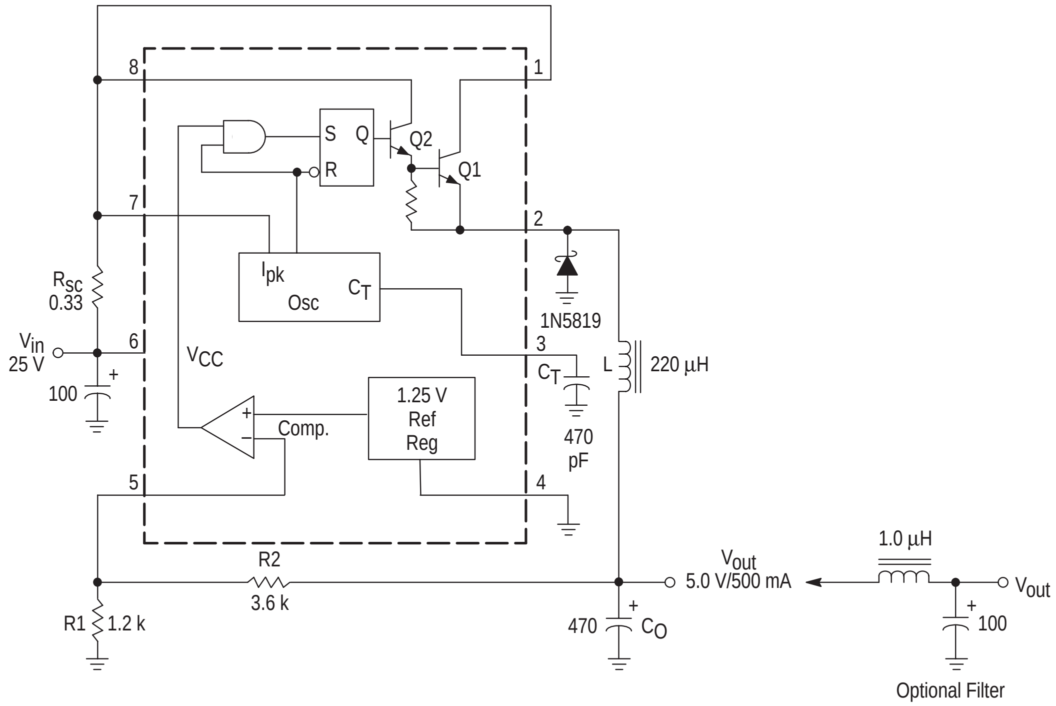
8a. External NPN Switch

8b. External NPN Saturated Switch

(See Note 5)

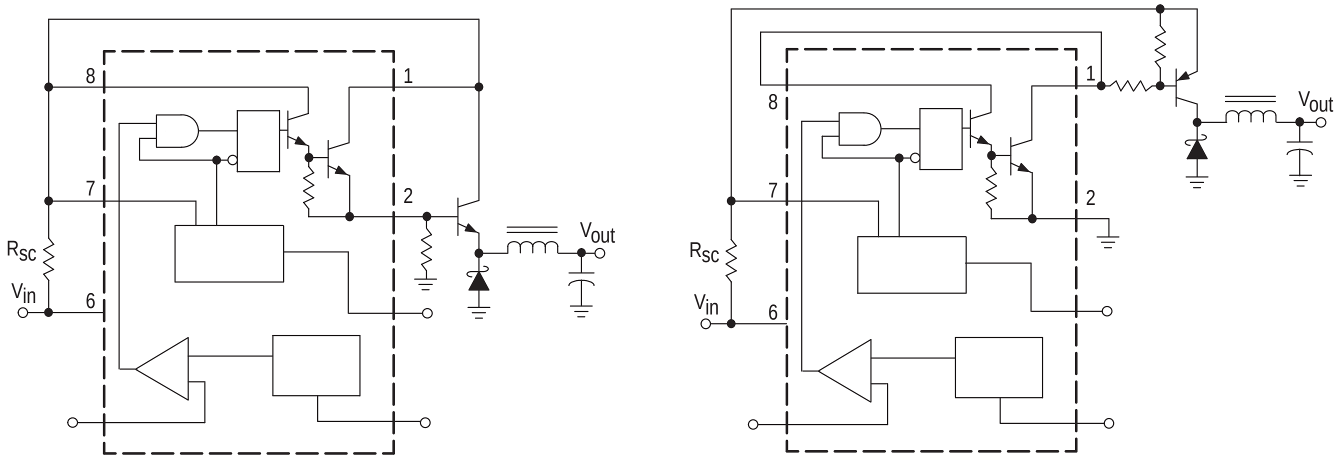
NOTE: 5. If the output switch is driven into hard saturation (non–Darlington configuration) at low switch currents (≤ 300 mA) and high driver currents (≥ 30 mA), it may take up to 2.0 µs to come out of saturation. This condition will shorten the off time at frequencies ≥ 30 kHz, and is magnified at high temperatures. This condition does not occur with a Darlington configuration, since the output switch cannot saturate. If a non–Darlington configuration is used, the following output drive condition is recommended.

Figure 9. Step–Down Converter



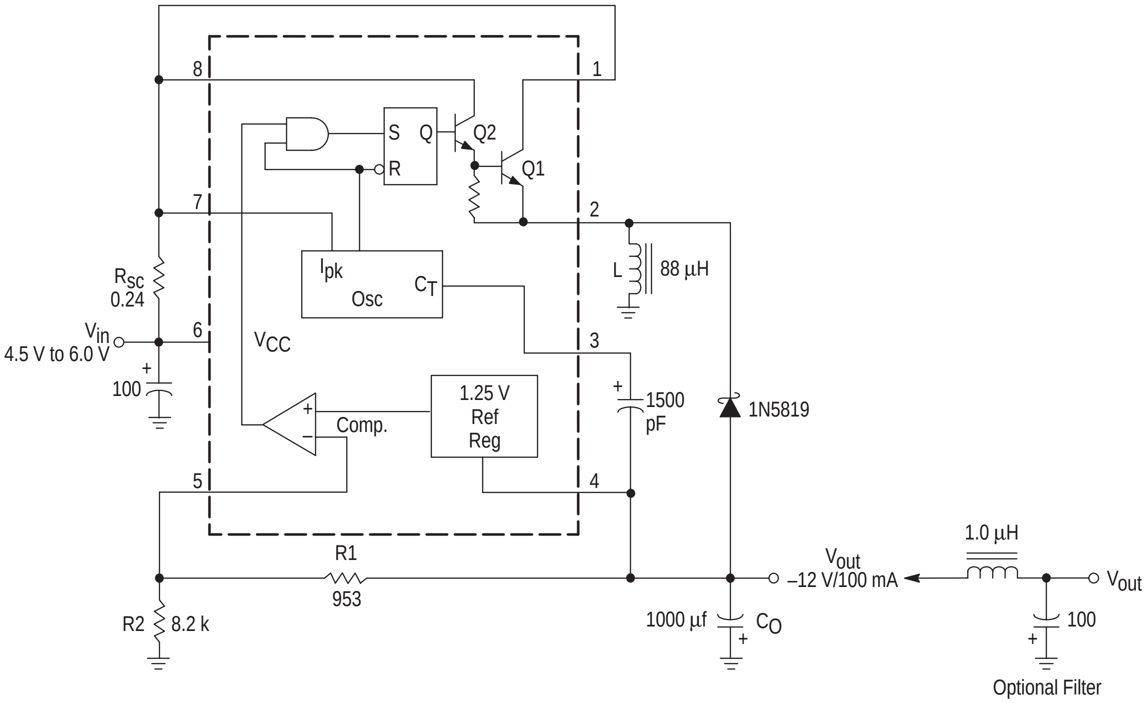
Test	Conditions	Results
Line Regulation	V_{in} = 15 V to 25 V, I_O = 500 mA	12 mV = ±0.12%
Load Regulation	V_{in} = 25 V, I_O = 50 mA to 500 mA	3.0 mV = ±0.03%
Output Ripple	V_{in} = 25 V, I_O = 500 mA	120 mVpp
Short Circuit Current	V_{in} = 25 V, R_L = 0.1 Ω	1.1 A
Efficiency	V_{in} = 25 V, I_O = 500 mA	83.7%
Output Ripple With Optional Filter	V_{in} = 25 V, I_O = 500 mA	40 mVpp

Figure 10. External Current Boost Connections for I_C Peak Greater than 1.5 A


10a. External NPN Switch

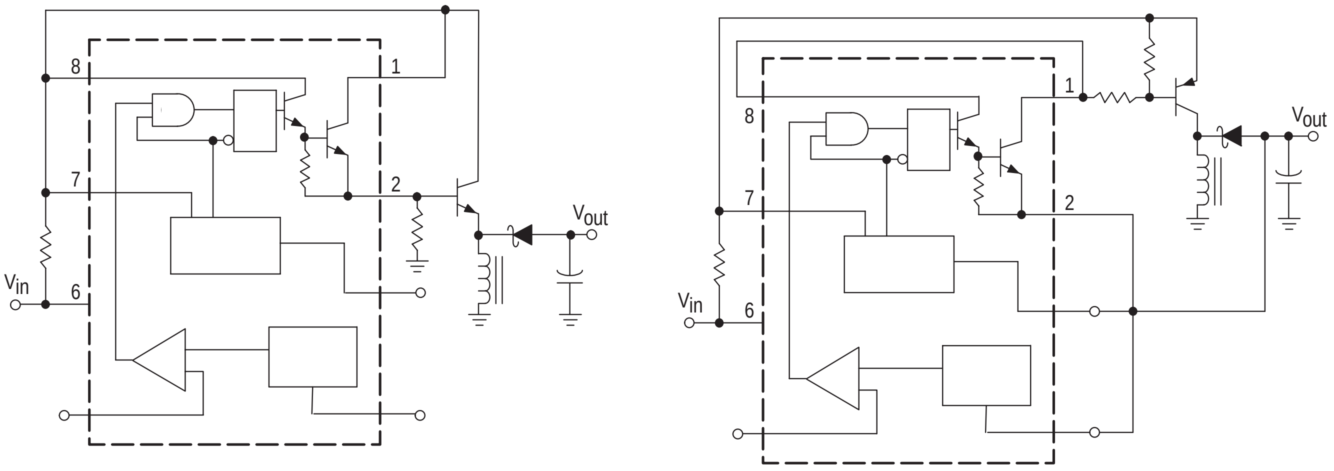
10b. External PNP Saturated Switch

Figure 11. Voltage Inverting Converter



Test	Conditions	Results
Line Regulation	V_{in} = 4.5 V to 6.0 V, I_O = 100 mA	3.0 mV = ±0.012%
Load Regulation	V_{in} = 5.0 V, I_O = 10 mA to 100 mA	0.022 V = ±0.09%
Output Ripple	V_{in} = 5.0 V, I_O = 100 mA	500 mVpp
Short Circuit Current	V_{in} = 5.0 V, R_L = 0.1 Ω	910 mA
Efficiency	V_{in} = 5.0 V, I_O = 100 mA	62.2%
Output Ripple With Optional Filter	V_{in} = 5.0 V, I_O = 100 mA	70 mVpp

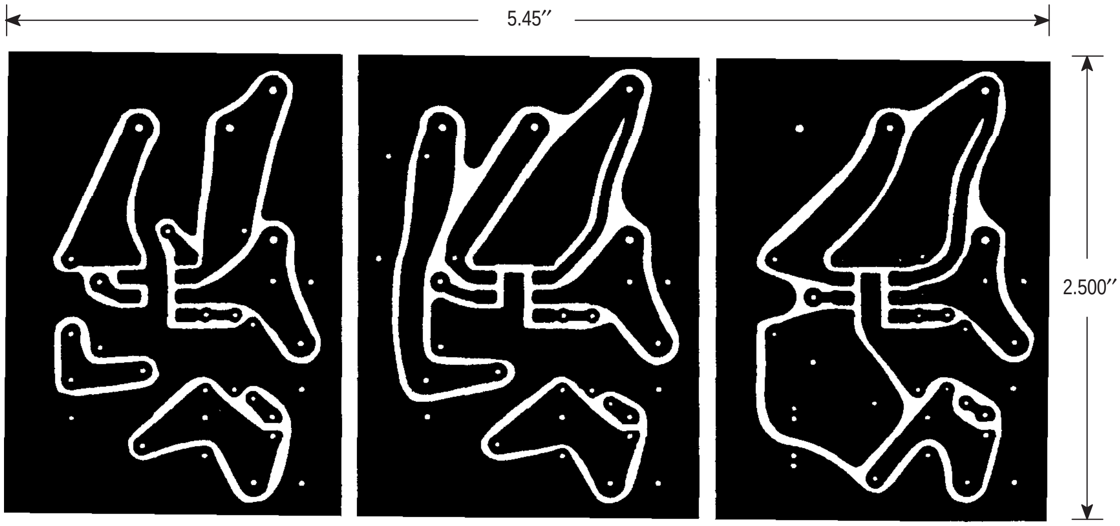
Figure 12. External Current Boost Connections for I_C Peak Greater than 1.5 A


12a. External NPN Switch

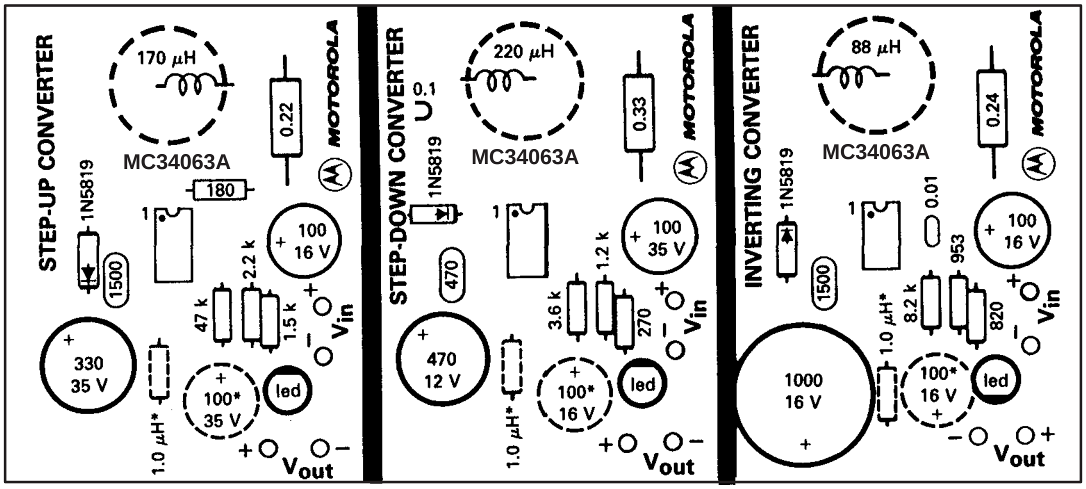
12b. External PNP Saturated Switch

Figure 13. Printed Circuit Board and Component Layout

(Circuits of Figures 7, 9, 11)



(Top view, copper foil as seen through the board from the component side)



(Top View, Component Side)

*Optional Filter.

INDUCTOR DATA

Converter	Inductance (µH)	Turns/Wire
Step–Up	170	38 Turns of #22 AWG
Step–Down	220	48 Turns of #22 AWG
Voltage–Inverting	88	28 Turns of #22 AWG

All inductors are wound on Magnetics Inc. 55117 toroidal core.

Figure 14. Design Formula Table

Calculation	Step–Up	Step–Down	Voltage–Inverting
t_{on}/t_{off}	$\frac{V_{out} + V_F - V_{in(min)}}{V_{in(min)} - V_{sat}}$	$\frac{V_{out} + V_F}{V_{in(min)} - V_{sat} - V_{out}}$	$\frac{\lvert V_{out}\rvert + V_F}{V_{in} - V_{sat}}$
$(t_{on} + t_{off})$	$\frac{1}{f}$	$\frac{1}{f}$	$\frac{1}{f}$
t_{off}	$\frac{t_{on} + t_{off}}{\frac{t_{on}}{t_{off}} + 1}$	$\frac{t_{on} + t_{off}}{\frac{t_{on}}{t_{off}} + 1}$	$\frac{t_{on} + t_{off}}{\frac{t_{on}}{t_{off}} + 1}$
t_{on}	$(t_{on} + t_{off}) - t_{off}$	$(t_{on} + t_{off}) - t_{off}$	$(t_{on} + t_{off}) - t_{off}$
C_T	$4.0 \times 10^{-5}\ t_{on}$	$4.0 \times 10^{-5}\ t_{on}$	$4.0 \times 10^{-5}\ t_{on}$
$I_{pk(switch)}$	$2I_{out(max)}\left(\frac{t_{on}}{t_{off}} + 1\right)$	$2I_{out(max)}$	$2I_{out(max)}\left(\frac{t_{on}}{t_{off}} + 1\right)$
R_{SC}	$0.3/I_{pk(switch)}$	$0.3/I_{pk(switch)}$	$0.3/I_{pk(switch)}$
$L_{(min)}$	$\left(\frac{(V_{in(min)} - V_{sat})}{I_{pk(switch)}}\right) t_{on(max)}$	$\left(\frac{(V_{in(min)} - V_{sat} - V_{out})}{I_{pk(switch)}}\right) t_{on(max)}$	$\left(\frac{(V_{in(min)} - V_{sat})}{I_{pk(switch)}}\right) t_{on(max)}$
C_O	$9\ \frac{I_{out}t_{on}}{V_{ripple(pp)}}$	$\frac{I_{pk(switch)}(t_{on} + t_{off})}{8V_{ripple(pp)}}$	$9\ \frac{I_{out}t_{on}}{V_{ripple(pp)}}$

V_{sat} = Saturation voltage of the output switch.
V_F = Forward voltage drop of the output rectifier.

The following power supply characteristics must be chosen:

V_{in} – Nominal input voltage.
V_{out} – Desired output voltage, $|V_{out}| = 1.25\left(1 + \frac{R2}{R1}\right)$
I_{out} – Desired output current.
f_{min} – Minimum desired output switching frequency at the selected values of V_{in} and I_O.
$V_{ripple(pp)}$ – Desired peak–to–peak output ripple voltage. In practice, the calculated capacitor value will need to be increased due to its equivalent series resistance and board layout. The ripple voltage should be kept to a low value since it will directly affect the line and load regulation.

NOTE: For further information refer to Application Note AN920A/D and AN954/D.

MOTOROLA

MC34064
MC33064

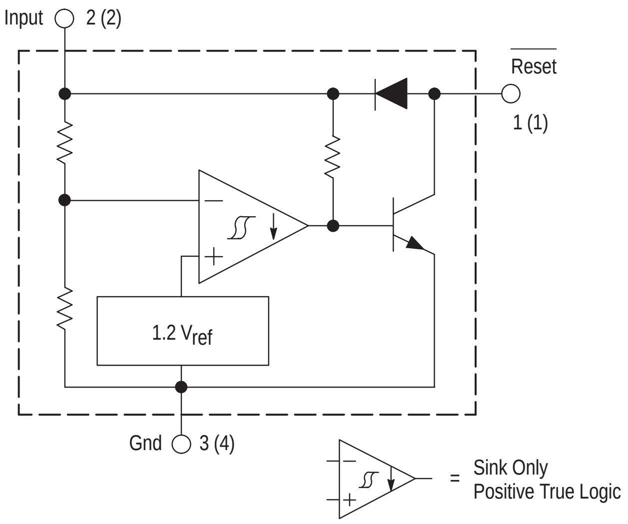
Undervoltage Sensing Circuit

The MC34064 is an undervoltage sensing circuit specifically designed for use as a reset controller in microprocessor-based systems. It offers the designer an economical solution for low voltage detection with a single external resistor. The MC34064 features a trimmed-in-package bandgap reference, and a comparator with precise thresholds and built-in hysteresis to prevent erratic reset operation. The open collector reset output is capable of sinking in excess of 10 mA, and operation is guaranteed down to 1.0 V input with low standby current. These devices are packaged in 3-pin TO-226AA, 8-pin SO–8 and Micro–8 surface mount packages.

Applications include direct monitoring of the 5.0 V MPU/logic power supply used in appliance, automotive, consumer and industrial equipment.

- Trimmed-In-Package Temperature Compensated Reference
- Comparator Threshold of 4.6 V at 25°C
- Precise Comparator Thresholds Guaranteed Over Temperature
- Comparator Hysteresis Prevents Erratic Reset
- Reset Output Capable of Sinking in Excess of 10 mA
- Internal Clamp Diode for Discharging Delay Capacitor
- Guaranteed Reset Operation with 1.0 V Input
- Low Standby Current
- Economical TO–226AA, SO–8 and Micro–8 Surface Mount Packages

Representative Block Diagram



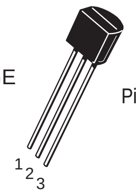
Pin numbers adjacent to terminals are for the 3–pin TO–226AA package.
Pin numbers in parenthesis are for the 8–lead packages.

This device contains 21 active transistors.

UNDERVOLTAGE SENSING CIRCUIT

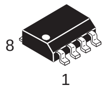
SEMICONDUCTOR TECHNICAL DATA

P SUFFIX
PLASTIC PACKAGE
CASE 29
(TO–226AA)

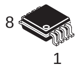


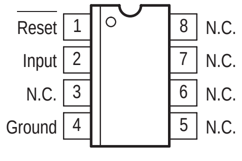
Pin 1. $\overline{\text{Reset}}$
2. Input
3. Ground

D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)



DM SUFFIX
PLASTIC PACKAGE
CASE 846A
(Micro–8)





(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC34064D–5	T_A = 0° to +70°C	SO–8
MC34064DM–5		Micro–8
MC34064P–5		TO–226AA
MC33064D–5	T_A = – 40° to +85°C	SO–8
MC33064DM–5		Micro–8
MC33064P–5		TO–226AA

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Input Supply Voltage	V_{in}	–1.0 to 10	V
$\overline{\text{Reset}}$ Output Voltage	V_O	10	V
$\overline{\text{Reset}}$ Output Sink Current (Note 1)	I_{Sink}	Internally Limited	mA
Clamp Diode Forward Current, Pin 1 to 2 (Note 1)	I_F	100	mA
Power Dissipation and Thermal Characteristics			
P Suffix, Plastic Package			
Maximum Power Dissipation @ T_A = 25°C	P_D	625	mW
Thermal Resistance, Junction–to–Air	$R_{\theta JA}$	200	°C/W
D Suffix, Plastic Package			
Maximum Power Dissipation @ T_A = 25°C	P_D	625	mW
Thermal Resistance, Junction–to–Air	$R_{\theta JA}$	200	°C/W
DM Suffix, Plastic Package			
Maximum Power Dissipation @ T_A = 25°C	P_D	520	mW
Thermal Resistance, Junction–to–Air	$R_{\theta JA}$	240	°C/W
Operating Junction Temperature	T_J	+150	°C
Operating Ambient Temperature	T_A		°C
MC34064		0 to +70	
MC33064		–40 to +85	
Storage Temperature Range	T_{stg}	–65 to +150	°C

NOTE: ESD data available upon request.

ELECTRICAL CHARACTERISTICS (For typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies [Notes 2 and 3] unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
COMPARATOR					
Threshold Voltage					V
High State Output (V_{in} Increasing)	V_{IH}	4.5	4.61	4.7	
Low State Output (V_{in} Decreasing)	V_{IL}	4.5	4.59	4.7	
Hysteresis	V_H	0.01	0.02	0.05	
$\overline{\text{RESET}}$ OUTPUT					
Output Sink Saturation	V_{OL}				V
(V_{in} = 4.0 V, I_{Sink} = 8.0 mA)		–	0.46	1.0	
(V_{in} = 4.0 V, I_{Sink} = 2.0 mA)		–	0.15	0.4	
(V_{in} = 1.0 V, I_{Sink} = 0.1 mA)		–	–	0.1	
Output Sink Current (V_{in}, $\overline{\text{Reset}}$ = 4.0 V)	I_{Sink}	10	27	60	mA
Output Off-State Leakage (V_{in}, $\overline{\text{Reset}}$ = 5.0 V)	I_{OH}	–	0.02	0.5	µA
Clamp Diode Forward Voltage, Pin 1 to 2 (I_F = 10 mA)	V_F	0.6	0.9	1.2	V
TOTAL DEVICE					
Operating Input Voltage Range	V_{in}	1.0 to 6.5	–	–	V
Quiescent Input Current (V_{in} = 5.0 V)	I_{in}	–	390	500	µA

NOTES:
1. Maximum package power dissipation limits must be observed.
2. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
3. T_{low} = 0°C for MC34064 / –40°C for MC33064; T_{high} = +70°C for MC34064 / +85°C for MC33064

Figure 1. $\overline{\text{Reset}}$ Output Voltage versus Input Voltage

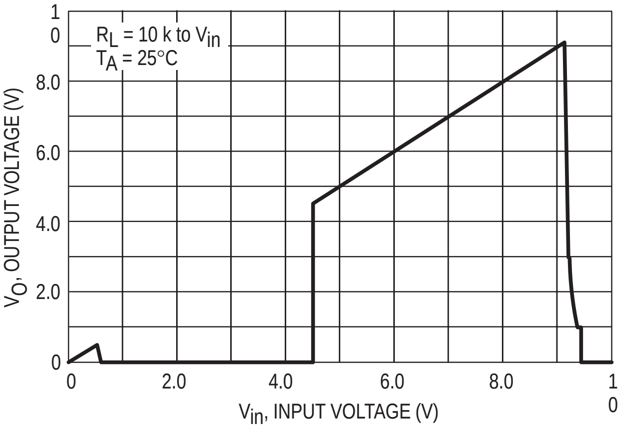


Figure 2. $\overline{\text{Reset}}$ Output Voltage versus Input Voltage

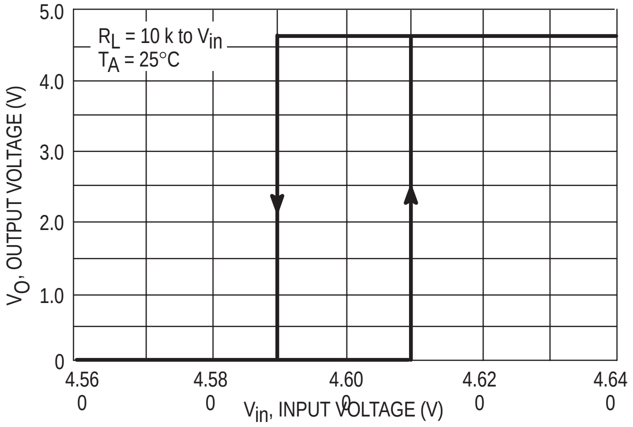


Figure 3. Comparator Threshold Voltage versus Temperature

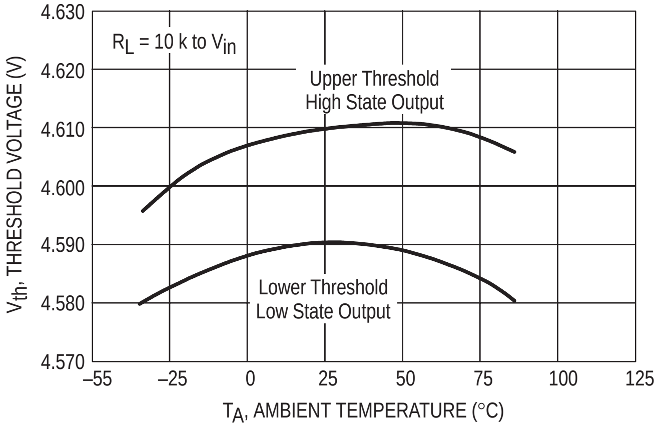


Figure 4. Input Current versus Input Voltage

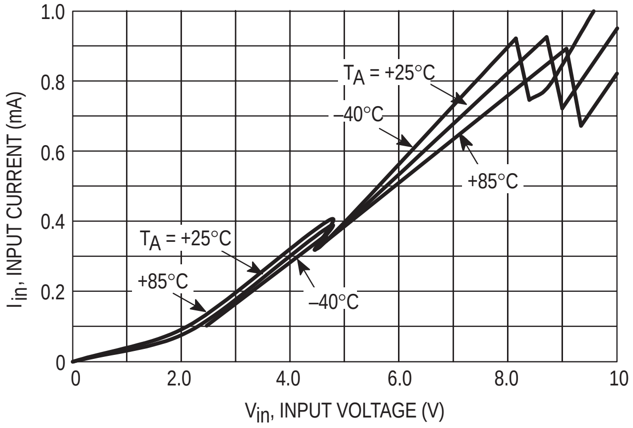


Figure 5. $\overline{\text{Reset}}$ Output Saturation versus Sink Current

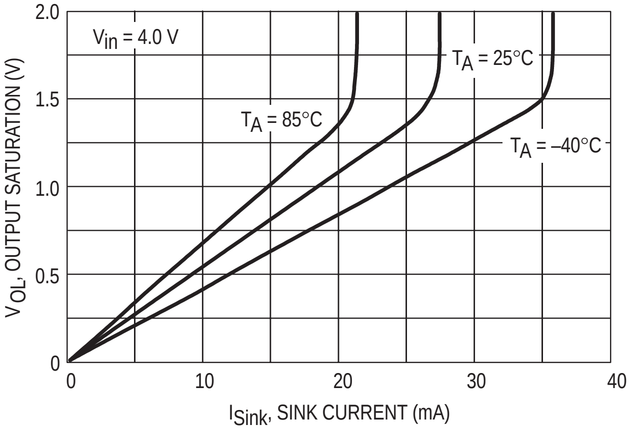


Figure 6. $\overline{\text{Reset}}$ Delay Time

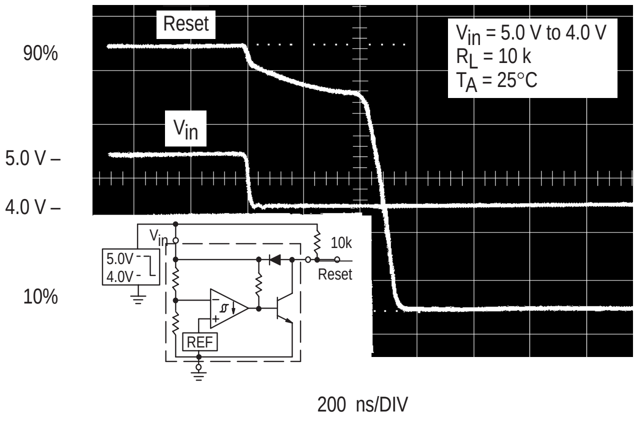


Figure 7. Clamp Diode Forward Current versus Voltage

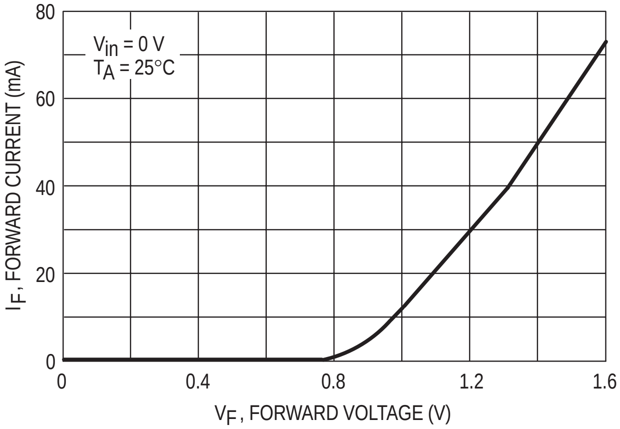
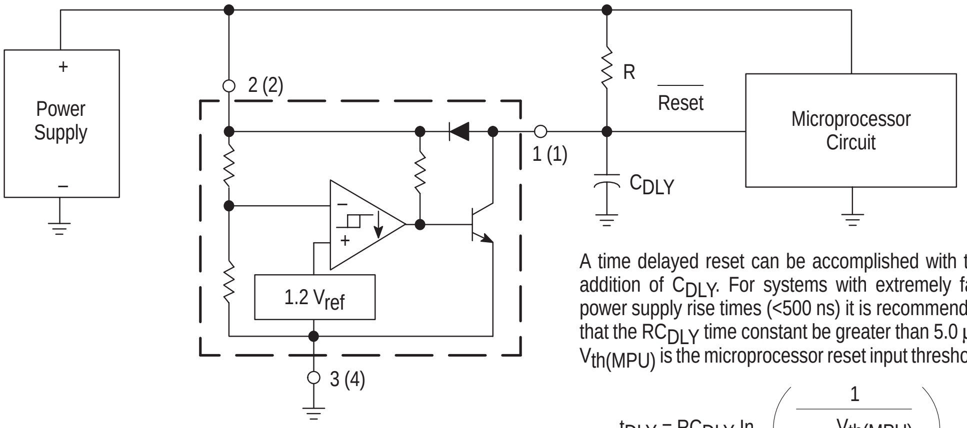


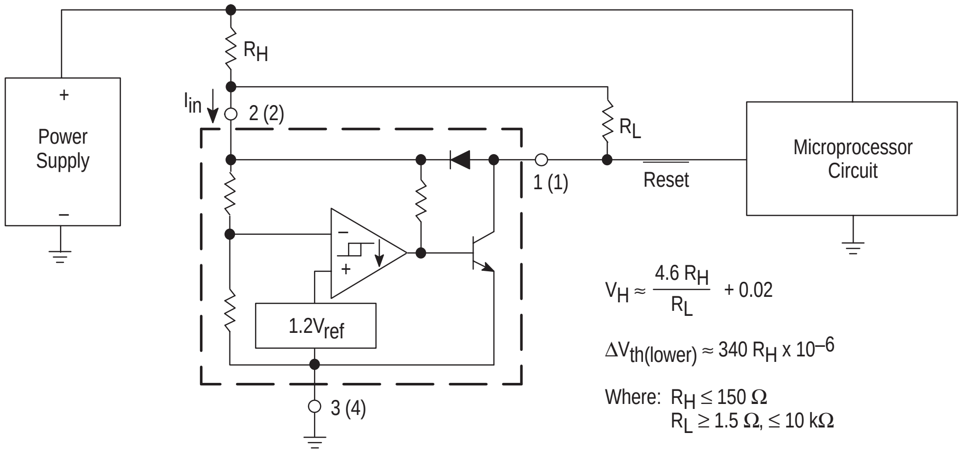
Figure 8. Low Voltage Microprocessor Reset



A time delayed reset can be accomplished with the addition of C_{DLY}. For systems with extremely fast power supply rise times (<500 ns) it is recommended that the RC_{DLY} time constant be greater than 5.0 µs. $V_{th(MPU)}$ is the microprocessor reset input threshold.

$$t_{DLY} = RC_{DLY} \ln \left(\frac{1}{1 - \frac{V_{th(MPU)}}{V_{in}}} \right)$$

Figure 9. Low Voltage Microprocessor Reset with Additional Hysteresis



$$V_H \approx \frac{4.6\,R_H}{R_L} + 0.02$$

$$\Delta V_{th(lower)} \approx 340\,R_H \times 10^{-6}$$

Where: $R_H \leq 150\ \Omega$
$R_L \geq 1.5\ \Omega, \leq 10\ k\Omega$

Test Data			
V_H (mV)	ΔV_{th} (mV)	R_H (Ω)	R_L (kΩ)
20	0	0	0
51	3.4	10	1.5
40	6.8	20	4.7
81	6.8	20	1.5
71	10	30	2.7
112	10	30	1.5
100	16	47	2.7
164	16	47	1.5
190	34	100	2.7
327	34	100	1.5
276	51	150	2.7
480	51	150	1.5

Comparator hysteresis can be increased with the addition of resistor R_H. The hysteresis equation has been simplified and does not account for the change of input current I_{in} as V_{CC} crosses the comparator threshold (Figure 4). An increase of the lower threshold $\Delta V_{th(lower)}$ will be observed due to I_{in} which is typically 340 µA at 4.59 V. The equations are accurate to ±10% with R_H less than 150 Ω and R_L between 1.5 kΩ and 10 kΩ.

Figure 10. Voltage Monitor

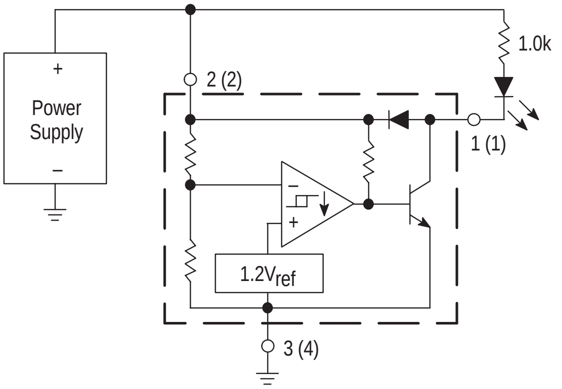


Figure 11. Solar Powered Battery Charger

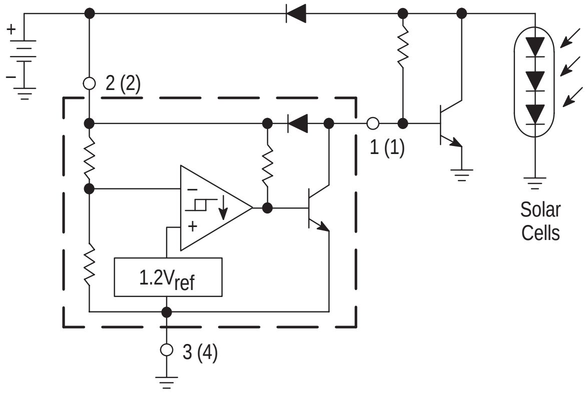
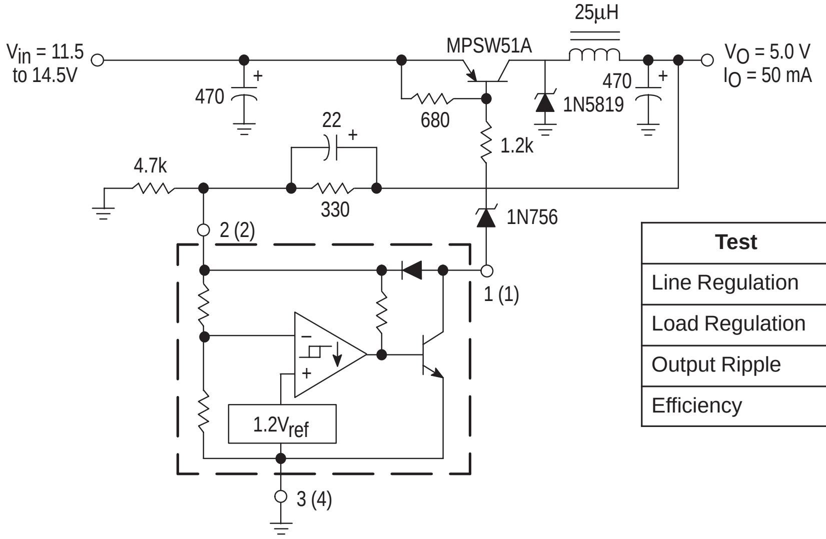
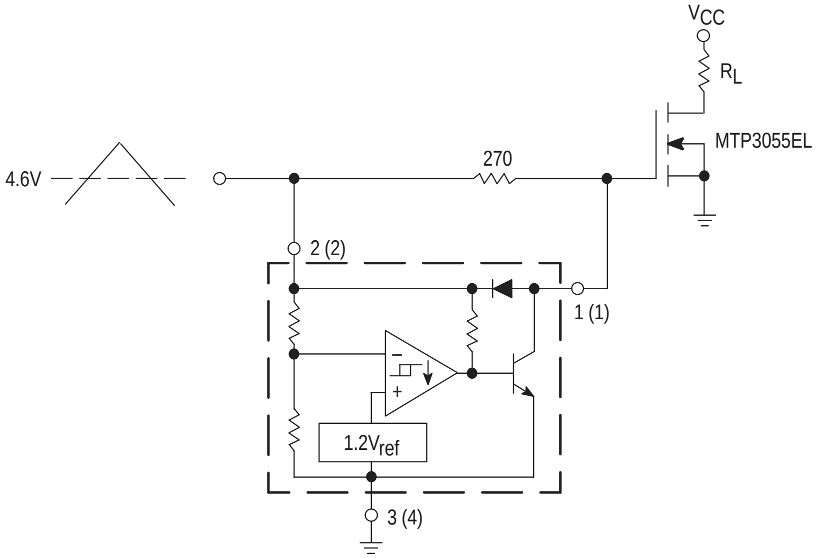


Figure 12. Low Power Switching Regulator



Test	Conditions	Results
Line Regulation	V_{in} = 11.5 V to 14.5 V, I_O = 50 mA	35 mV
Load Regulation	V_{in} = 12.6 V, I_O = 0 mA to 50 mA	12 mV
Output Ripple	V_{in} = 12.6 V, I_O = 50 mA	60 mVpp
Efficiency	V_{in} = 12.6 V, I_O = 50 mA	77%

Figure 13. MOSFET Low Voltage Gate Drive Protection



Overheating of the logic level power MOSFET due to insufficient gate voltage can be prevented with the above circuit. When the input signal is below the 4.6 V threshold of the MC34064, its output grounds the gate of the L^2 MOSFET.

MOTOROLA

MC34065
MC33065

High Performance Dual Channel Current Mode Controller

The MC34065 is a high performance, fixed frequency, dual current mode controllers. It is specifically designed for off–line and dc–to–dc converter applications offering the designer a cost effective solution with minimal external components. This integrated circuit feature a unique oscillator for precise duty cycle limit and frequency control, a temperature compensated reference, two high gain error amplifiers, two current sensing comparators, Drive Output 2 Enable pin, and two high current totem pole outputs ideally suited for driving power MOSFETs.

Also included are protective features consisting of input and reference undervoltage lockouts each with hysteresis, cycle–by–cycle current limiting, and a latch for single pulse metering of each output.

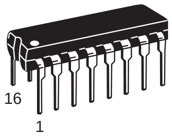
The MC34065 and MC33065 are available in dual–in–line and surface mount packages.

- Unique Oscillator for Precise Duty Cycle Limit and Frequency Control
- Current Mode Operation to 500 kHz
- Automatic Feed Forward Compensation
- Separate Latching PWMs for Cycle–By–Cycle Current Limiting
- Internally Trimmed Reference with Undervoltage Lockout
- Drive Output 2 Enable Pin
- Two High Current Totem Pole Outputs
- Input Undervoltage Lockout with Hysteresis
- Low Startup and Operating Current

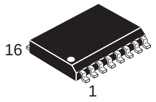
HIGH PERFORMANCE DUAL CHANNEL CURRENT MODE CONTROLLER

SEMICONDUCTOR TECHNICAL DATA

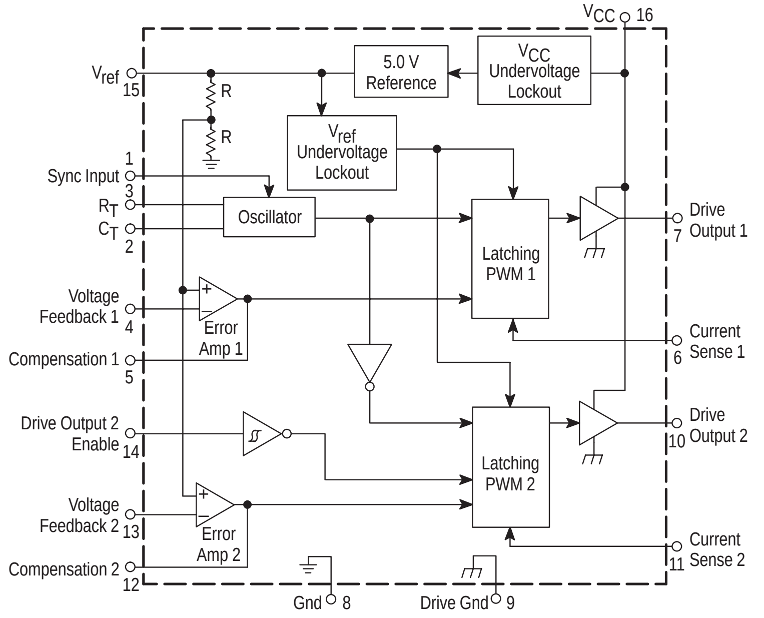
P SUFFIX
PLASTIC PACKAGE
CASE 648



DW SUFFIX
PLASTIC PACKAGE
CASE 751G
(SO–16L)

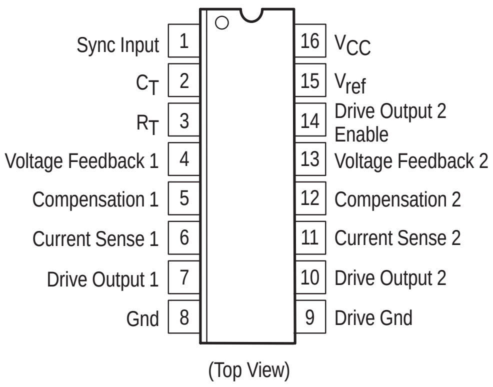


Representative Block Diagram



This device contains 208 active transistors.

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC34065DW	T_A = 0° to +70°C	SO–16L
MC34065P		Plastic DIP
MC33065DW	T_A = –40° to +85°C	SO–16L
MC33065P		Plastic DIP

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Total Power Supply and Zener Current	$(I_{CC} + I_Z)$	50	mA
Output Current, Source or Sink (Note 1)	I_O	1.0	A
Output Energy (Capacitive Load per Cycle)	W	5.0	μJ
Current Sense, Enable, and Voltage Feedback Inputs	V_{in}	–0.3 to +5.5	V
Sync Input High State (Voltage) Low State (Reverse Current)	 V_{IH} I_{IL}	 5.5 –5.0	 V mA
Error Amp Output Sink Current	I_O	10	mA
Power Dissipation and Thermal Characteristics DW Suffix, Plastic Package Case 751G Maximum Power Dissipation @ T_A = 25°C Thermal Resistance, Junction–to–Air P Suffix, Plastic Package Case 648 Maximum Power Dissipation @ T_A = 25°C Thermal Resistance, Junction–to–Air	 P_D $R_{\theta JA}$ P_D $R_{\theta JA}$	 862 145 1.25 100	 mW °C/W W °C/W
Operating Junction Temperature	T_J	+150	°C
Operating Ambient Temperature MC34065 MC33065	T_A	 0 to +70 –40 to +85	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

NOTE: ESD data available upon request.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 15 V [Note 2], R_T = 8.2 kΩ, C_T = 3.3 nF, for typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies [Note 3].)

Characteristics	Symbol	Min	Typ	Max	Unit
REFERENCE SECTION					
Reference Output Voltage (I_O = 1.0 mA, T_J = 25°C)	V_{ref}	4.9	5.0	5.1	V
Line Regulation (V_{CC} = 11 V to 15 V)	Reg_{line}	–	2.0	20	mV
Load Regulation (I_O = 1.0 mA to 10 mA)	Reg_{load}	–	3.0	25	mV
Total Output Variation over Line, Load, and Temperature	V_{ref}	4.85	–	5.15	V
Output Short Circuit Current	I_{SC}	30	100	–	mA
OSCILLATOR AND PWM SECTIONS					
Total Frequency Variation over Line and Temperature V_{CC} = 11 V to 15 V, T_A = T_{low} to T_{high} MC34065 MC33065	f_{osc}	 46.5 45	 49 49	 51.5 53	kHz
Frequency Change with Voltage (V_{CC} = 11 V to 15 V)	$\Delta f_{osc}/\Delta V$	–	0.2	1.0	%
Duty Cycle at each Output Maximum Minimum	 DC_{max} DC_{min}	 46 –	 49.5 –	 52 0	%
Sync Input Current High State (V_{in} = 2.4 V) Low State (V_{in} = 0.8 V)	 I_{IH} I_{IL}	 – –	 170 80	 250 160	μA

NOTES:
1. Maximum package power dissipation limits must be observed.
2. Adjust V_{CC} above the startup threshold before setting to 15 V.
3. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible:
   - T_{low} = 0°C for the MC34065 T_{high} = +70°C for MC34065
   - T_{low} = –40°C for the MC33065 T_{high} = +85°C for MC33065
4. This parameter is measured at the latch trip point with V_{FB} = 0 V
5. Comparator gain is defined as $AV = \dfrac{\Delta V\ \text{Compensation}}{\Delta V\ \text{Current Sense}}$

ELECTRICAL CHARACTERISTICS (continued) (V_{CC} = 15 V [Note 2], R_T = 8.2 kΩ, C_T = 3.3 nF, for typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies [Note 3].)

Characteristics	Symbol	Min	Typ	Max	Unit
ERROR AMPLIFIERS					
Voltage Feedback Input (V_O = 2.5 V)	V_{FB}	2.42	2.5	2.58	V
Input Bias Current (V_{FB} = 5.0 V)	I_{IB}	–	– 0.1	–1.0	µA
Open Loop Voltage Gain (V_O = 2.0 to 4.0 V)	A_{VOL}	65	100	–	dB
Unity Gain Bandwidth (T_J = 25°C)	BW	0.7	1.0	–	MHz
Power Supply Rejection Ratio (V_{CC} = 11 V to 15 V)	PSRR	60	90	–	dB
Output Current					mA
Source (V_O = 3.0 V, V_{FB} = 2.3 V)	I_{source}	–0.45	–1.0	–	
Sink (V_O = 1.2 V, V_{FB} = 2.7 V)	I_{sink}	2.0	12	–	
Output Voltage Swing					V
High State (R_L = 15 k to ground, V_{FB} = 2.3 V)	V_{OH}	5.0	6.2	–	
Low State (R_L = 15 k to V_{ref}, V_{FB} = 2.7 V)	V_{OL}	–	0.8	1.1	
CURRENT SENSE SECTION					
Current Sense Input Voltage Gain (Notes 4 and 5)	A_V	2.75	3.0	3.25	V/V
Maximum Current Sense Input Threshold (Note 4)	V_{th}	430	480	530	mV
Input Bias Current	I_{IB}	–	–2.0	–10	µA
Propagation Delay (Current Sense Input to Output)	$t_{PLN(In/Out)}$	–	150	300	ns
DRIVE OUTPUT 2 ENABLE PIN					
Enable Pin Voltage					V
High State (Output 2 Enabled)	V_{IH}	3.5	–	V_{ref}	
Low State (Output 2 Disabled)	V_{IL}	0	–	1.5	
Low State Input Current (V_{IL} = 0 V)	I_{IB}	100	250	400	µA
DRIVE OUTPUTS					
Output Voltage					V
Low State (I_{sink} = 20 mA)	V_{OL}	–	0.1	0.4	
(I_{sink} = 200 mA)		–	1.6	2.5	
High State (I_{source} = 20 mA)	V_{OH}	13	13.5	–	
(I_{source} = 200 mA)		12	13.4	–	
Output Voltage with UVLO Activated (V_{CC} = 6.0 V, I_{sink} = 1.0 mA)	$V_{OL(UVLO)}$	–	0.1	1.1	V
Output Voltage Rise Time (C_L = 1.0 nF)	t_r	–	28	150	ns
Output Voltage Fall Time (C_L = 1.0 nF)	t_f	–	25	150	ns
UNDERVOLTAGE LOCKOUT SECTION					
Startup Threshold	V_{th}	13	14	15	V
Minimum Operating Voltage After Turn–On	$V_{CC(min)}$	9.0	10	11	V
TOTAL DEVICE					
Power Supply Current	I_{CC}				mA
Startup (V_{CC} = 12 V)		–	0.6	1.0	
Operating (Note 2)		–	20	25	
Power Supply Zener Voltage (I_{CC} = 30 mA)	V_Z	15.5	17	19	V

NOTES: 1. Maximum package power dissipation limits must be observed.
2. Adjust V_{CC} above the startup threshold before setting to 15 V.
3. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible:
T_{low} = 0°C for the MC34065 T_{high} = +70°C for MC34065
T_{low} = –40°C for the MC33065 T_{high} = +85°C for MC33065
4. This parameter is measured at the latch trip point with V_{FB} = 0 V
5. Comparator gain is defined as $AV = \frac{\Delta V\ \text{Compensation}}{\Delta V\ \text{Current Sense}}$

PIN FUNCTION DESCRIPTION

Pin	Function	Description
1	Sync Input	A narrow rectangular waveform applied to this input will synchronize the oscillator. A dc voltage within the range of 2.4 V to 5.5 V will inhibit the oscillator.
2	C_T	Timing capacitor C_T connects from this pin to ground setting the free–running oscillator frequency range.
3	R_T	Resistor R_T connects from this pin to ground precisely setting the charge current for C_T. R_T must be between 4.0 k and 16 k.
4	Voltage Feedback 1	This pin is the inverting input of Error Amplifier 1. It is normally connected to the switching power supply output through a resistor divider.
5	Compensation 1	This pin is the output of Error Amplifier 1 and is made available for loop compensation.
6	Current Sense 1	A voltage proportional to the inductor current is connected to this input. PWM 1 uses this information to terminate conduction of output switch Q1.
7	Drive Output 1	This pin directly drives the gate of a power MOSFET Q1. Peak currents up to 1.0 A are sourced and sunk by this pin.
8	Gnd	This pin is the control circuitry ground return and is connected back to the source ground.
9	Drive Gnd	This pin is a separate power ground return that is connected back to the power source. It is used to reduce the effects of switching transient noise on the control circuitry.
10	Drive Output 2	This pin directly drives the gate of a power MOSFET Q2. Peak currents up to 1.0 A are sourced and sunk by this pin.
11	Current Sense 2	A voltage proportional to inductor current is connected to this input. PWM 2 uses this information to terminate conduction of output switch Q2.
12	Compensation 2	This pin is the output of Error Amplifier 2 and is made available for loop compensation.
13	Voltage Feedback 2	This pin is the inverting input of Error Amplifier 2. It is normally connected to the switching power supply output through a resistor divider.
14	Drive Output 2 Enable	A logic low at this input disables Drive Output 2.
15	V_{ref}	This is the 5.0 V reference output. It can provide bias for any additional system circuitry.
16	V_{CC}	This pin is the positive supply of the control IC. The minimum operating voltage range after startup is 11 V to 15.5 V.

Figure 1. Timing Resistor versus Oscillator Frequency

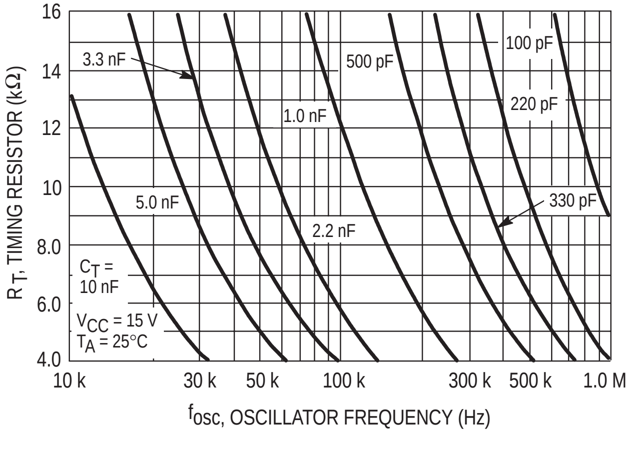


Figure 2. Maximum Output Duty Cycle versus Oscillator Frequency

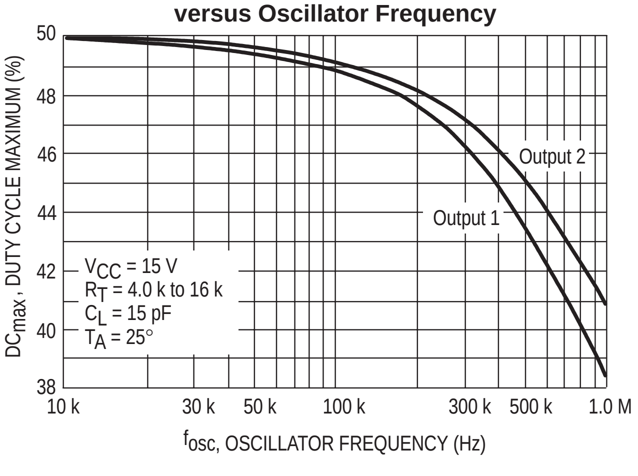


Figure 3. Error Amp Small–Signal Transient Response

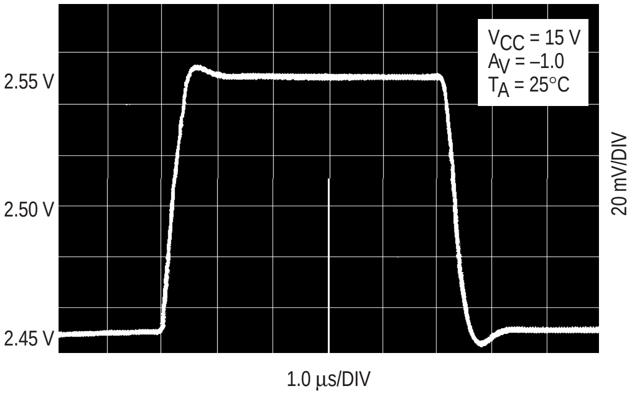


Figure 4. Error Amp Large–Signal Transient Response

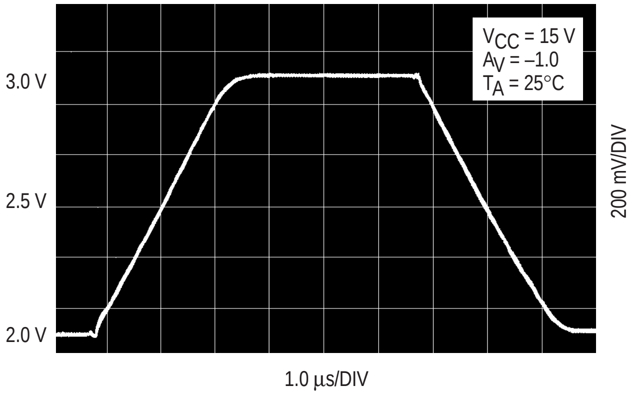


Figure 5. Error Amp Open Loop Gain and Phase versus Frequency

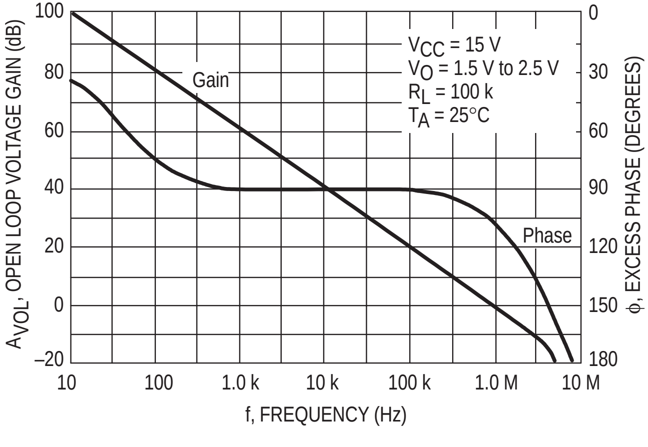


Figure 6. Current Sense Input Threshold versus Error Amp Output Voltage

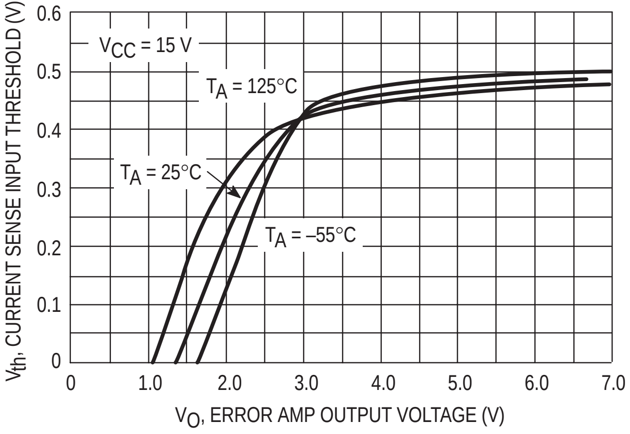


Figure 7. Reference Voltage Change versus Source Current

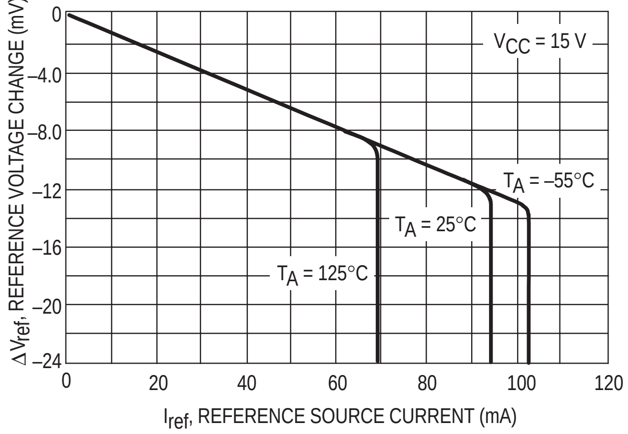


Figure 8. Reference Short Circuit Current versus Temperature

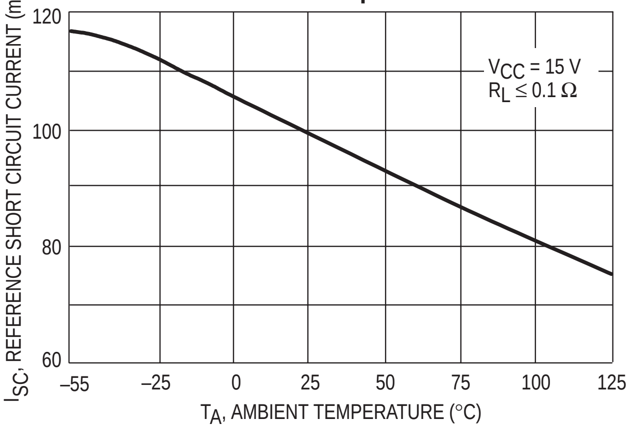


Figure 9. Reference Load Regulation

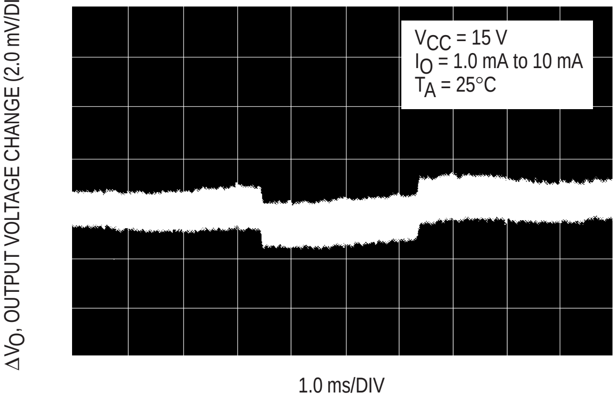


Figure 10. Reference Line Regulation

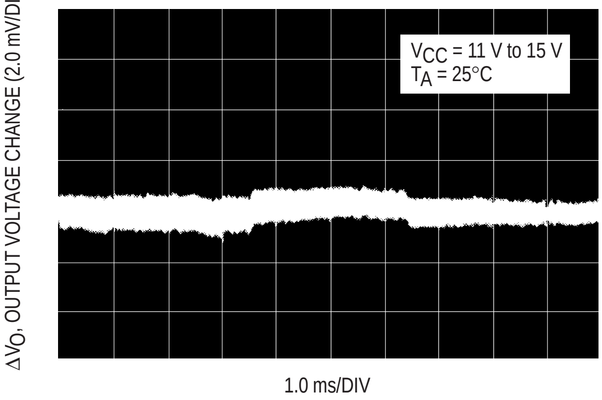


Figure 11. Output Saturation Voltage versus Load Current

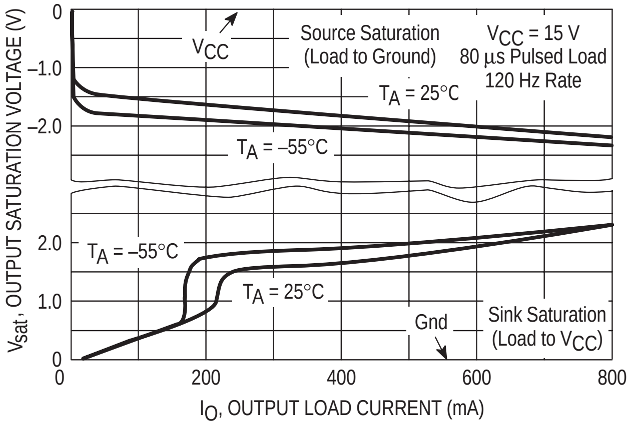


Figure 12. Output Waveform

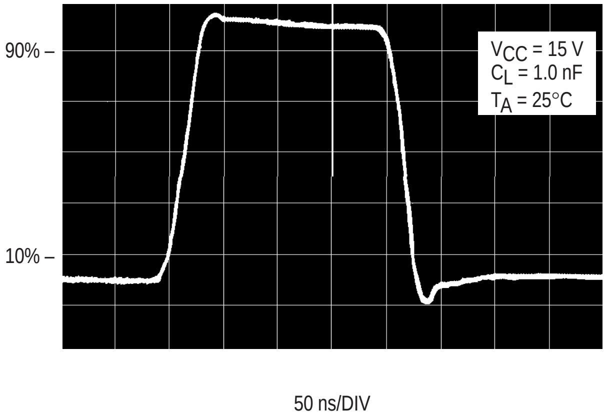


Figure 13. Output Cross Conduction Current

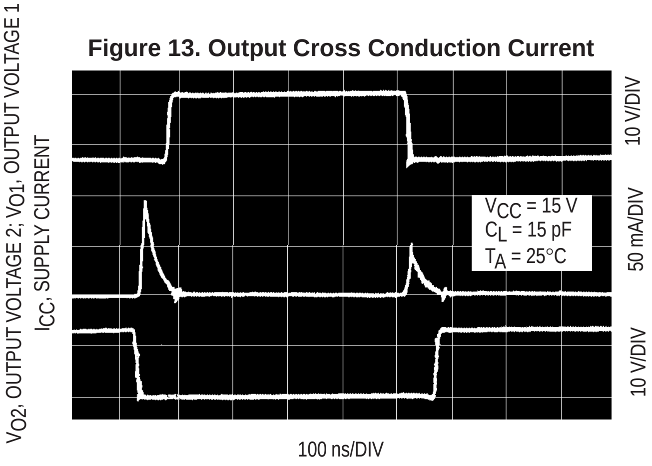
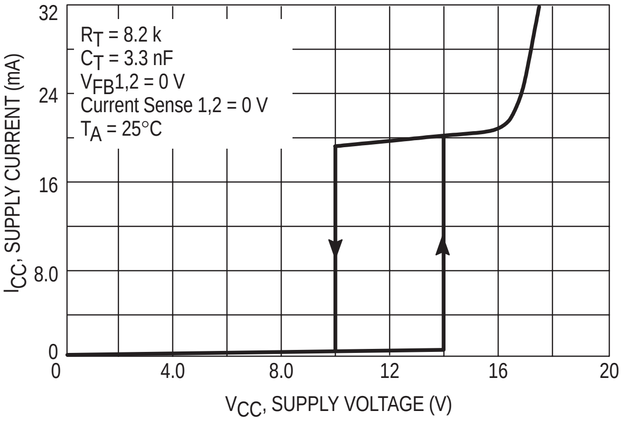


Figure 14. Supply Current versus Supply Voltage



OPERATING DESCRIPTION

The MC34065 series are high performance, fixed frequency, dual channel current mode controllers specifically designed for Off–Line and dc–to–dc converter applications. These devices offer the designer a cost effective solution with minimal external components where independent regulation of two power converters is required. The Representative Block Diagram is shown in Figure 15. Each channel contains a high gain error amplifier, current sensing comparator, pulse width modulator latch, and totem pole output driver. The oscillator, reference regulator, and undervoltage lock–out circuits are common to both channels.

Oscillator

The unique oscillator configuration employed features precise frequency and duty cycle control. The frequency is programmed by the values selected for the timing components R_T and C_T. Capacitor C_T is charged and discharged by an equal magnitude internal current source and sink, generating a symmetrical 50 percent duty cycle waveform at Pin 2. The oscillator peak and valley thresholds are 3.5 V and 1.6 V respectively. The source/sink current magnitude is controlled by resistor R_T. For proper operation over temperature it must be in the range of 4.0 kΩ to 16 kΩ as shown in Figure 1.

As C_T charges and discharges, an internal blanking pulse is generated that alternately drives the center inputs of the upper and lower NOR gates high. This, in conjunction with a precise amount of delay time introduced into each channel, produces well defined non–overlapping output duty cycles. Output 2 is enabled while C_T is charging, and Output 1 is enabled during the discharge. Figure 2 shows the Maximum Output Duty Cycle versus Oscillator Frequency. Note that even at 500 kHz, each output is capable of approximately 44% on–time, making this controller suitable for high frequency power conversion applications.

In many noise sensitive applications it may be desirable to frequency–lock the converter to an external system clock. This can be accomplished by applying a clock signal as shown in Figure 17. For reliable locking, the free–running oscillator frequency should be set about 10% less than the clock frequency. Referring to the timing diagram shown in Figure 16, the rising edge of the clock signal applied to the Sync input, terminates charging of C_T and Drive Output 2 conduction. By tailoring the clock waveform symmetry, accurate duty cycle clamping of either output can be achieved. A circuit method for this, and multi–unit synchronization, is shown in Figure 18.

Error Amplifier

Each channel contains a fully–compensated Error Amplifier with access to the inverting input and output. The amplifier features a typical dc voltage gain of 100 dB, and a unity gain bandwidth of 1.0 MHz with 71° of phase margin (Figure 5). The noninverting input is internally biased at 2.5 V and is not pinned out. The converter output voltage is typically divided down and monitored by the inverting input through a resistor divider. The maximum input bias current is –1.0 µA which will cause an output voltage error that is equal to the product of the input bias current and the equivalent input divider source resistance.

The Error Amp output (Pin 5, 12) is provided for external loop compensation. The output voltage is offset by two diode drops (≈1.4 V) and divided by three before it connects to the inverting input of the Current Sense Comparator. This guarantees that no pulses appear at the Drive Output (Pin 7, 10) when the error amplifier output is at its lowest state (V_{OL}). This occurs when the power supply is operating and the load is removed, or at the beginning of a soft–start interval (Figures 20, 21).

The minimum allowable Error Amp feedback resistance is limited by the amplifier's source current (0.5 mA) and the output voltage (V_{OH}) required to reach the comparator's 0.5 V clamp level with the inverting input at ground. This condition happens during initial system startup or when the sensed output is shorted:

$$R_{f(min)} \approx \frac{3.0\ (0.5\ V)\ +\ 1.4\ V}{0.5\ mA} = 5800\ \Omega$$

Current Sense Comparator and PWM Latch

The MC34065 operates as a current mode controller, whereby output switch conduction is initiated by the oscillator and terminated when the peak inductor current reaches the threshold level established by the Error Amplifier output. Thus the error signal controls the peak inductor current on a cycle–by–cycle basis. The Current Sense Comparator–PWM Latch configuration used ensures that only a single pulse appears at the Drive Output during any given oscillator cycle. The inductor current is converted to a voltage by inserting a ground–referenced sense resistor R_S in series with the source of output switch Q1. This voltage is monitored by the Current Sense Input (Pin 6, 11) and compared to a level derived from the Error Amp output. The peak inductor current under normal operating conditions is controlled by the voltage at Pin 5, 12 where:

$$I_{pk} = \frac{V_{(Pin\ 5,\ 12)} - 1.4\ V}{3\ R_S}$$

Abnormal operating conditions occur when the power supply output is overloaded or if output voltage sensing is lost. Under these conditions, the Current Sense Comparator threshold will be internally clamped to 0.5 V. Therefore the maximum peak switch current is:

$$I_{pk(max)} = \frac{0.5\ V}{R_S}$$

When designing a high power switching regulator it may be desirable to reduce the internal clamp voltage in order to keep the power dissipation of R_S to a reasonable level. A simple method to adjust this voltage is shown in Figure 19. The two external diodes are used to compensate the internal diodes, yielding a constant clamp voltage over temperature. Erratic operation due to noise pickup can result if there is an excessive reduction of the $I_{pk(max)}$ clamp voltage.

A narrow spike on the leading edge of the current waveform can usually be observed and may cause the power supply to exhibit an instability when the output is lightly loaded. This spike is due to the power transformer interwinding capacitance and output rectifier recovery time. The addition of an RC filter on the Current Sense input with a time constant that approximates the spike duration will usually eliminate the instability, refer to Figure 24.

Figure 15. Representative Block Diagram

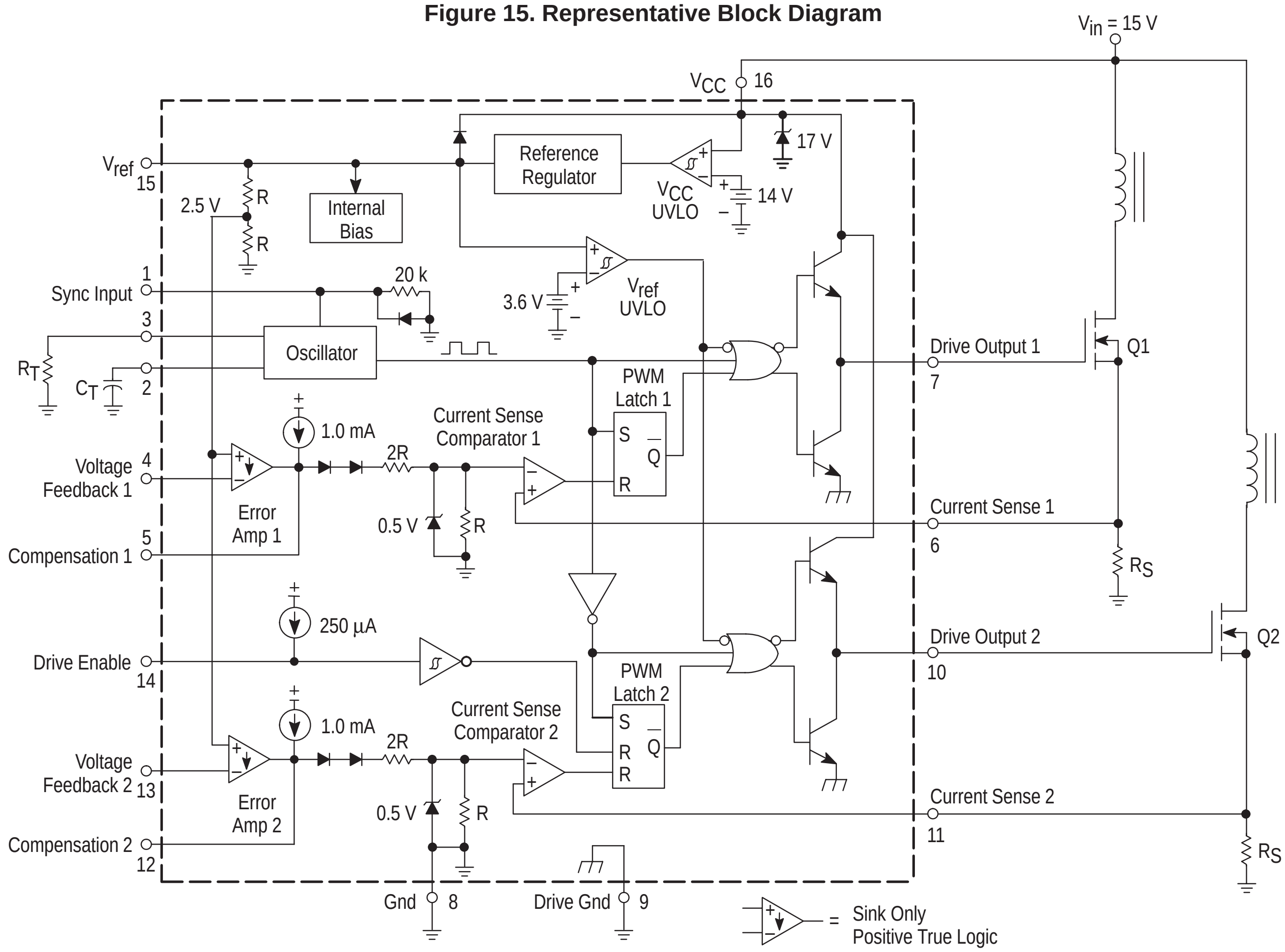
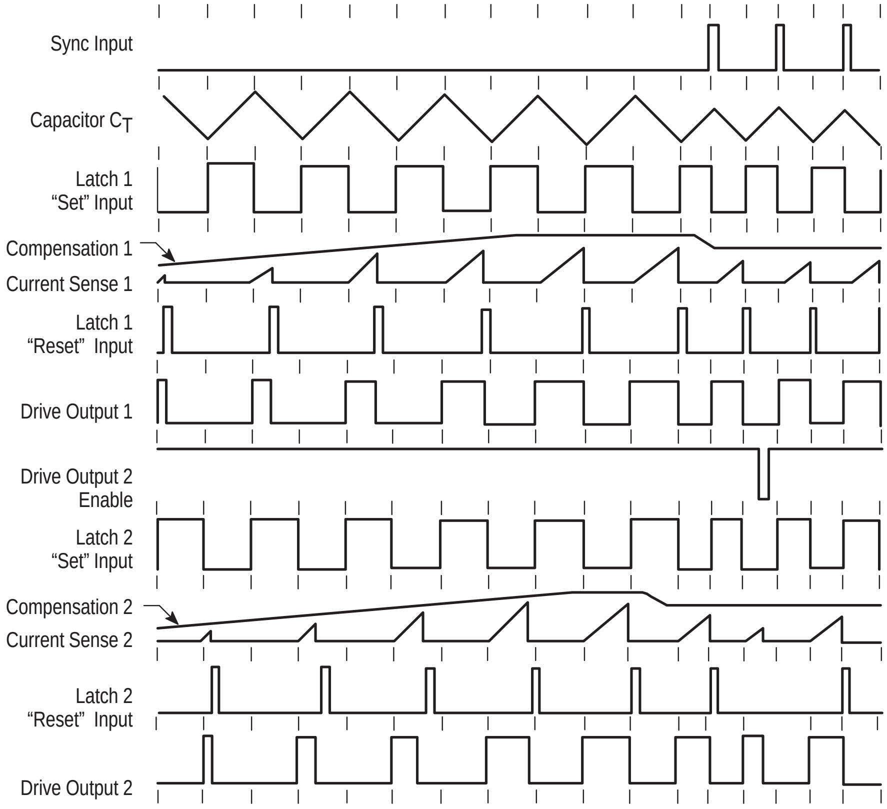


Figure 16. Timing Diagram



Undervoltage Lockout

Two Undervoltage Lockout comparators have been incorporated to guarantee that the IC is fully functional before the output stages are enabled. The positive power supply terminal (V_{CC}) and the reference output (V_{ref}) are each monitored by separate comparators. Each has built–in hysteresis to prevent erratic output behavior as their respective thresholds are crossed. The V_{CC} comparator upper and lower thresholds are 14 V and 10 V respectively. The hysteresis and low startup current makes these devices ideally suited to off–line converter applications where efficient bootstrap startup techniques are required (Figure 28). The V_{ref} comparator disables the Drive Outputs until the internal circuitry is functional. This comparator has upper and lower thresholds of 3.6 V and 3.4 V. A 17 V zener is connected as a shunt regulator from V_{CC} to ground. Its purpose is to protect the IC and power MOSFET gate from excessive voltage that can occur during system startup. The guaranteed minimum operating voltage after turn–on is 11 V.

Drive Outputs and Drive Ground

Each channel contains a single totem–pole output stage that is specifically designed for direct drive of power MOSFETs. The Drive Outputs are capable of up to ±1.0 A peak current with a typical rise and fall time of 28 ns with a 1.0 nF load. Internal circuitry has been added to keep the outputs in a sinking mode whenever an Undervoltage Lockout is active. This characteristic eliminates the need for an external pull–down resistor. Cross–conduction current in the totem–pole output stage has been minimized for high speed operation, as shown in Figure 13. The average added power due to cross–conduction with V_{CC} = 15 V is only 60 mW at 500 kHz.

Although the Drive Outputs were optimized for MOSFETs, they can easily supply the negative base current required by bipolar NPN transistors for enhanced turn–off (Figure 25). The outputs do not contain internal current limiting, therefore an external series resistor may be required to prevent the peak output current from exceeding the 1.0 A maximum rating. The sink saturation (V_{OL}) is less than 0.4 V at 100 mA.

A separate Drive Ground pin is provided and, with proper implementation, will significantly reduce the level of switching transient noise imposed on the control circuitry. This becomes particularly useful when reducing the $I_{pk(max)}$ clamp level. Figure 23 shows the proper ground connections required for current sensing power MOSFET applications.

Drive Output 2 Enable Pin

This input is used to enable Drive Output 2. Drive Output 1 can be used to control circuitry that must run continuously such as volatile memory and the system clock, or a remote controlled receiver, while Drive Output 2 controls the high power circuitry that is occasionally turned off.

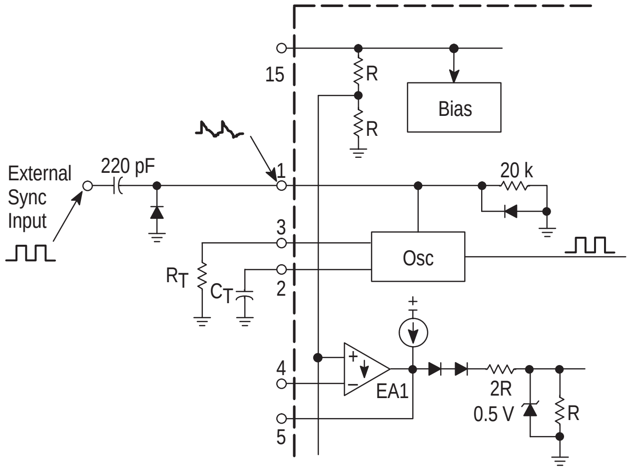
Reference

The 5.0 V bandgap reference is trimmed to ±2.0% tolerance at T_J = 25°C. The reference has short circuit protection and is capable of providing in excess of 30 mA for powering any additional control system circuitry.

Design Considerations

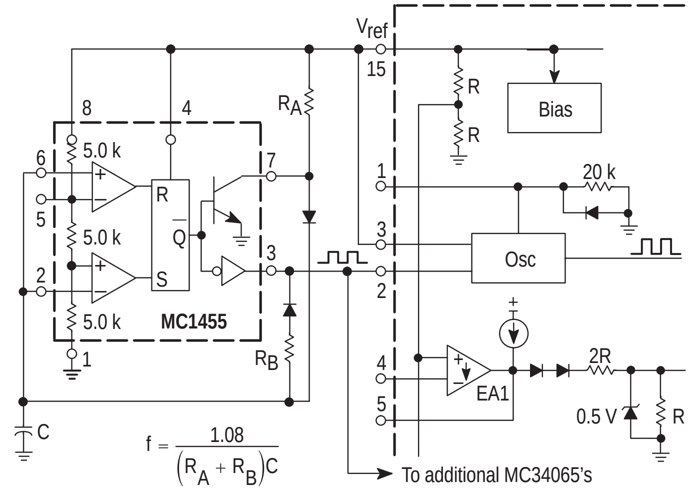
Do not attempt to construct the converter on wire–wrap or plug–in prototype boards. High frequency circuit layout techniques are imperative to prevent pulse–width jitter. This is usually caused by excessive noise pick–up imposed on the Current Sense or Voltage Feedback inputs. Noise immunity can be improved by lowering circuit impedances at these points. The printed circuit layout should contain a ground plane with low current signal and high current switch and output grounds returning on separate paths back to the input filter capacitor. Ceramic bypass capacitors (0.1 µF) connected directly to V_{CC} and V_{ref} may be required depending upon circuit layout. This provides a low impedance path for filtering the high frequency noise. All high current loops should be kept as short as possible using heavy copper runs to minimize radiated EMI. The Error Amp compensation circuitry and the converter output voltage–divider should be located close to the IC and as far as possible from the power switch and other noise generating components.

Figure 17. External Clock Synchronization



The external diode clamp is required if the negative Sync current is greater than –5.0 mA.

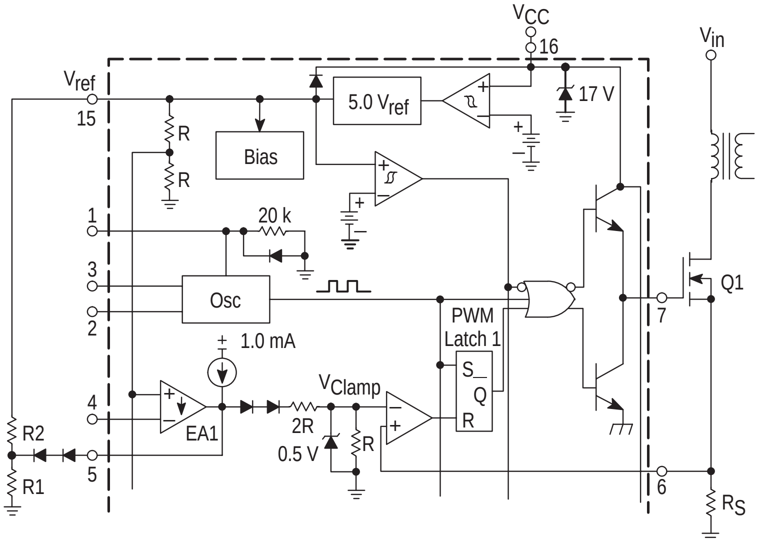
Figure 18. External Duty Cycle Clamp and Multi–Unit Synchronization



$$f = \frac{1.08}{(R_A + R_B)C}$$

$$D_{max}\ \text{Drive Output 1} = \frac{R_B}{R_A + R_B} \qquad D_{max}\ \text{Drive Output 2} = \frac{R_A}{R_A + R_B}$$

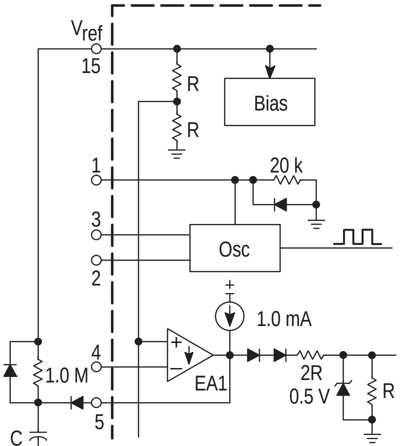
Figure 19. Adjustable Reduction of Clamp Level



$$V_{Clamp} \approx \frac{1.67}{\left(\frac{R2}{R1} + 1\right)} + 0.33 \times 10^{-3}\left(\frac{R1R2}{R1 + R2}\right) \qquad I_{pk(max)} \approx \frac{V_{Clamp}}{R_S}$$

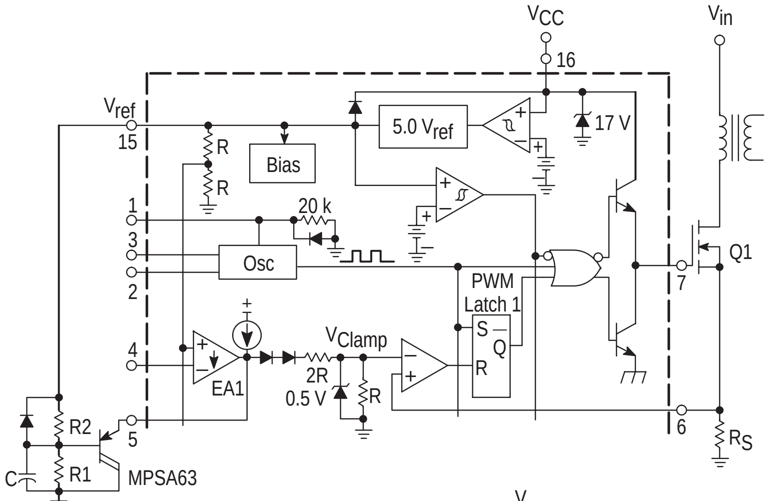
Where: $0 \le V_{Clamp} \le 0.5$ V

Figure 20. Soft–Start Circuit



$t_{Soft–Start} \approx 2100\ C$ in µF

Figure 21. Adjustable Reduction of Clamp Level with Soft–Start



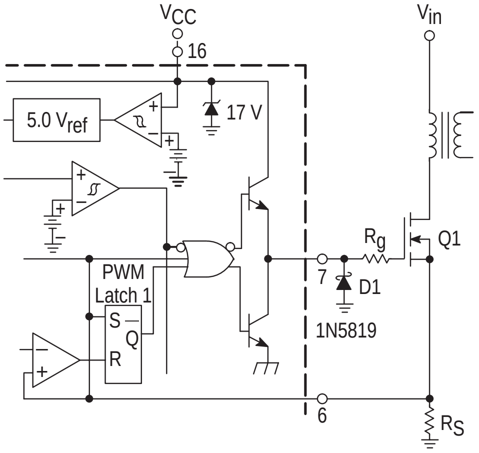
Where: $0 \le V_{Clamp} \le 0.5\ V$

$$I_{pk(max)} \approx \frac{V_{Clamp}}{R_S}$$

$$V_{Clamp} \approx \frac{1.67}{\left(\frac{R2}{R1} + 1\right)}$$

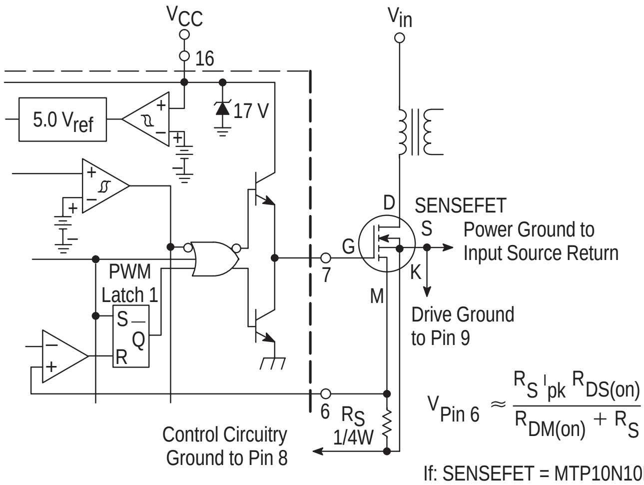
$$t_{Soft\text{–}Start} = \ln\left(\frac{1}{1 - \frac{V_C}{3\ V_{Clamp}}}\right) C\ \frac{R1R2}{R1 + R2}$$

Figure 22. MOSFET Parasitic Oscillations



Series gate resistor R_g may be needed to damp high frequency parasitic oscillations caused by the MOSFET input capacitance and any series wiring inductance in the gate–source circuit. R_g will decrease the MOSFET switching speed. Schottky diode D1 is required if circuit ringing drives the output pin below ground.

Figure 23. Current Sensing Power MOSFET

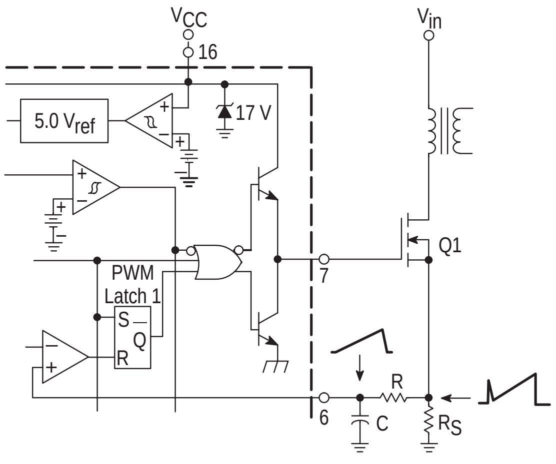


$$V_{Pin\ 6} \approx \frac{R_S\ I_{pk}\ R_{DS(on)}}{R_{DM(on)} + R_S}$$

If: SENSEFET = MTP10N10M
R_S = 200
Then: $V_{Pin\ 6} = 0.075\ I_{pk}$

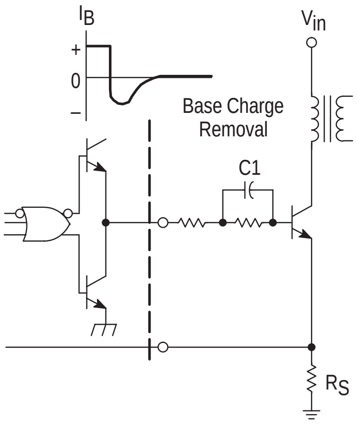
Virtually lossless current sensing can be achieved with the implementation of a SENSEFET power switch. For proper operation during over current conditions, a reduction of the $I_{pk(max)}$ clamp level must be implemented. Refer to Figures 19 and 21.

Figure 24. Current Waveform Spike Suppression



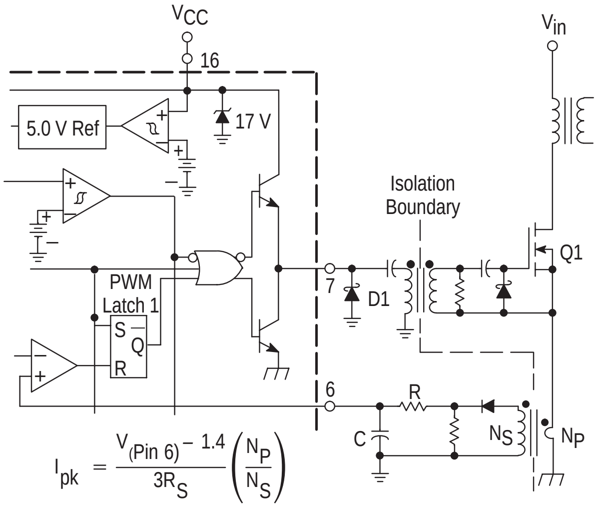
The addition of the RC filter will eliminate instability caused by the leading edge spike on the current waveform.

Figure 25. Bipolar Transistor Drive



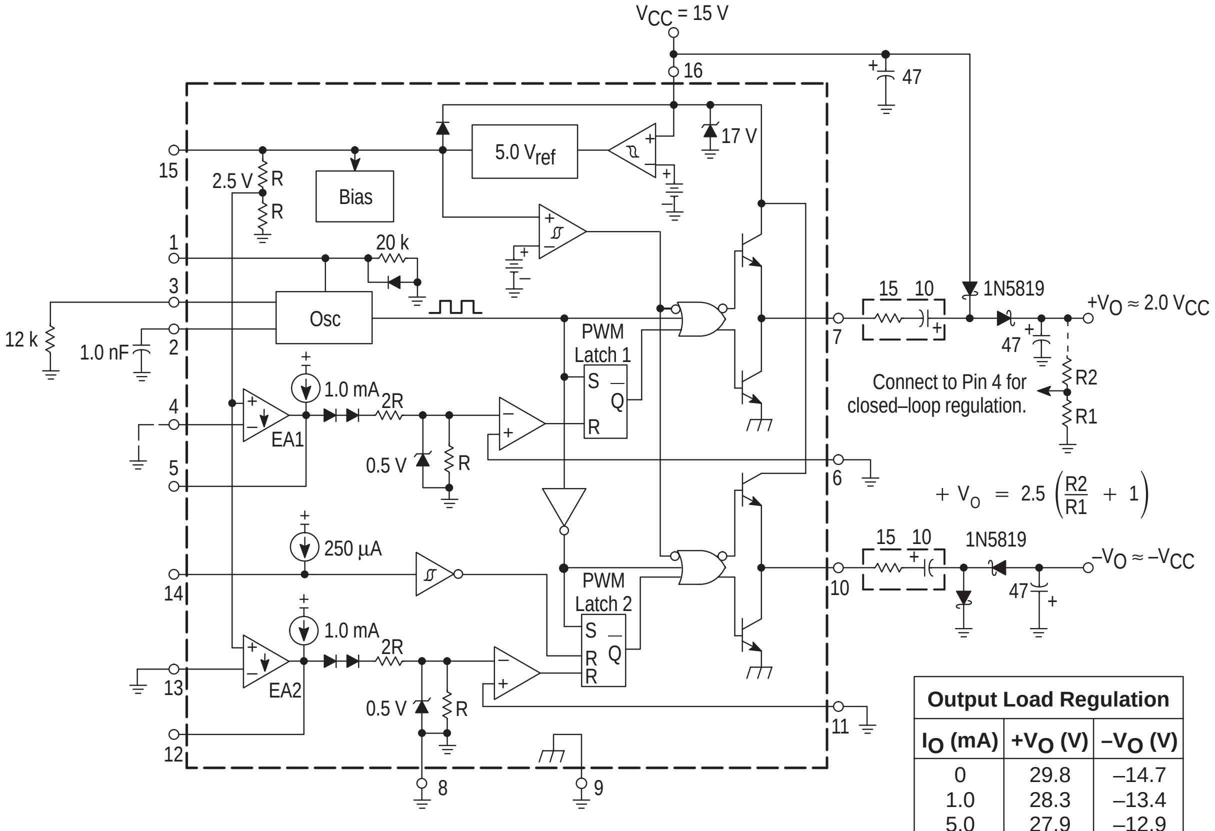
The totem–pole outputs can furnish negative base current for enhanced transistor turn–off, with the addition of capacitor C1.

Figure 26. Isolated MOSFET Drive



$$I_{pk} = \frac{V_{(Pin\ 6)} - 1.4}{3R_S}\left(\frac{N_P}{N_S}\right)$$

Figure 27. Dual Charge Pump Converter



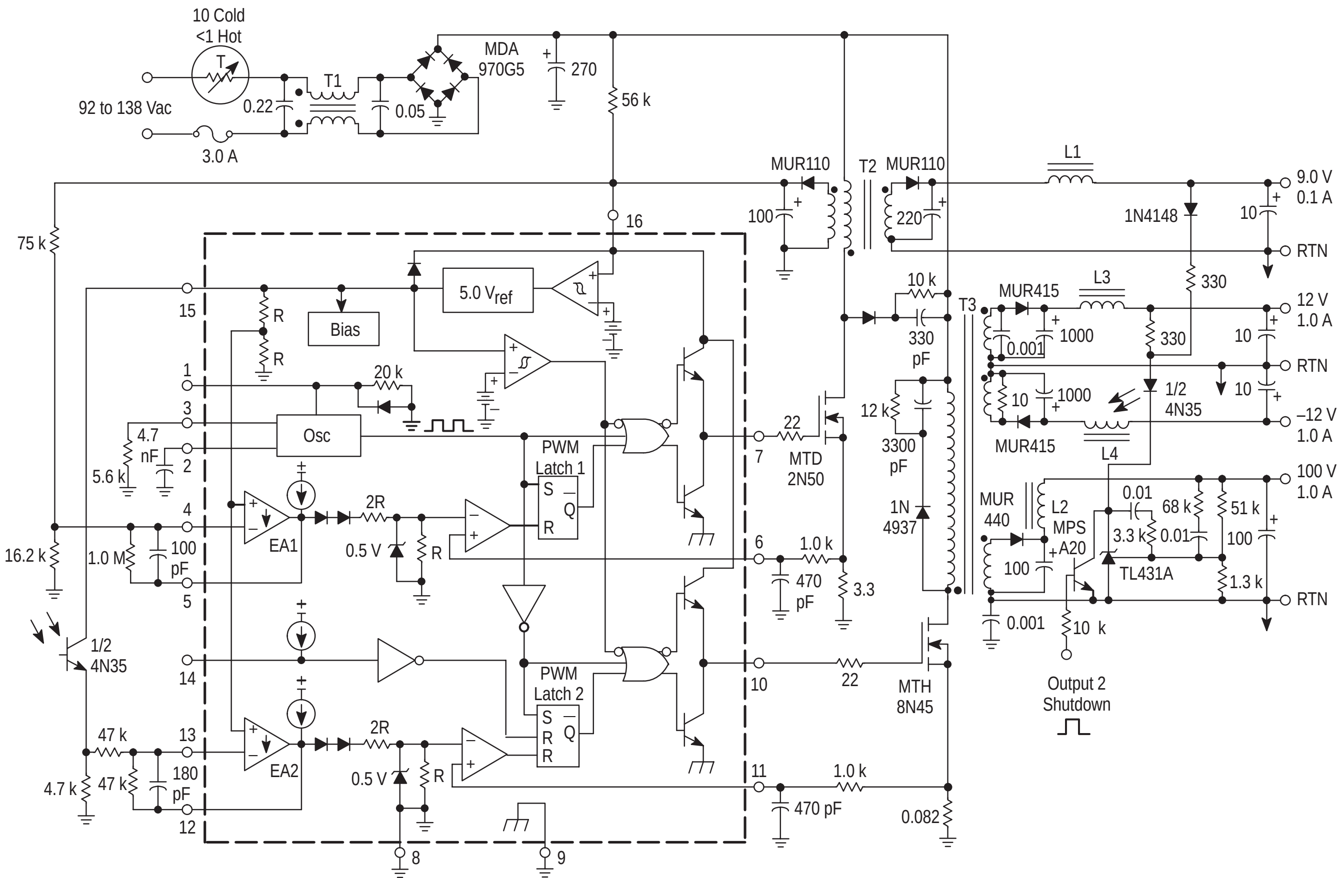
$$+V_O = 2.5\left(\frac{R2}{R1} + 1\right)$$

Output Load Regulation

I_O (mA)	$+V_O$ (V)	$-V_O$ (V)
0	29.8	–14.7
1.0	28.3	–13.4
5.0	27.9	–12.9
10	27.5	–12.5
50	24.4	–9.5

The capacitor’s equivalent series resistance must limit the Drive Output current to 1.0 A. An additional series resistor may be required when using tantalum or other low ESR capacitors. The positive output can provide excellent line and load regulation by connecting the R2/R1 resistor divider as shown.

Figure 28. 125 Watt Off–Line Converter



Test	Conditions	Results
Line Regulation 100 V Output ±12 V Outputs 9.0 V Output	V_{in} = 92 to 138 Vac I_O = 1.0 A I_O = ±1.0 A I_O = 0.1 A	Δ = 40 mV or ±0.02% Δ = 32 mV or ±0.13% Δ = 55 mV or ±0.31%
Load Regulation 100 V Output ±12 V Outputs 9.0 V Output	V_{in} = 115 Vac I_O = 0.25 A to 1.0 A I_O = ±0.25 A to ±1.0 A I_O = 0.08 A to 0.1 A	Δ = 50 mV or ±0.025% Δ = 320 mV or ±1.2% Δ = 234 mV or ±1.3%
Output Ripple 100 V Output ±12 V Outputs 9.0 V Output	V_{in} = 115 Vac I_O = 1.0 A I_O = ±1.0 A I_O = 0.1 A	40 mVpp 100 mVpp 60 mVpp
Short Circuit Current 100 V Output ±12 V Outputs 9.0 V Output	V_{in} = 115 Vac, R_L = 0.1 Ω	4.3 A 17 A Output Hiccups
Efficiency	Vin = 115 Vac, PO = 125 W	86%

T1 – 468 µH per section at 2.5 A,
Coilcraft E3496A.

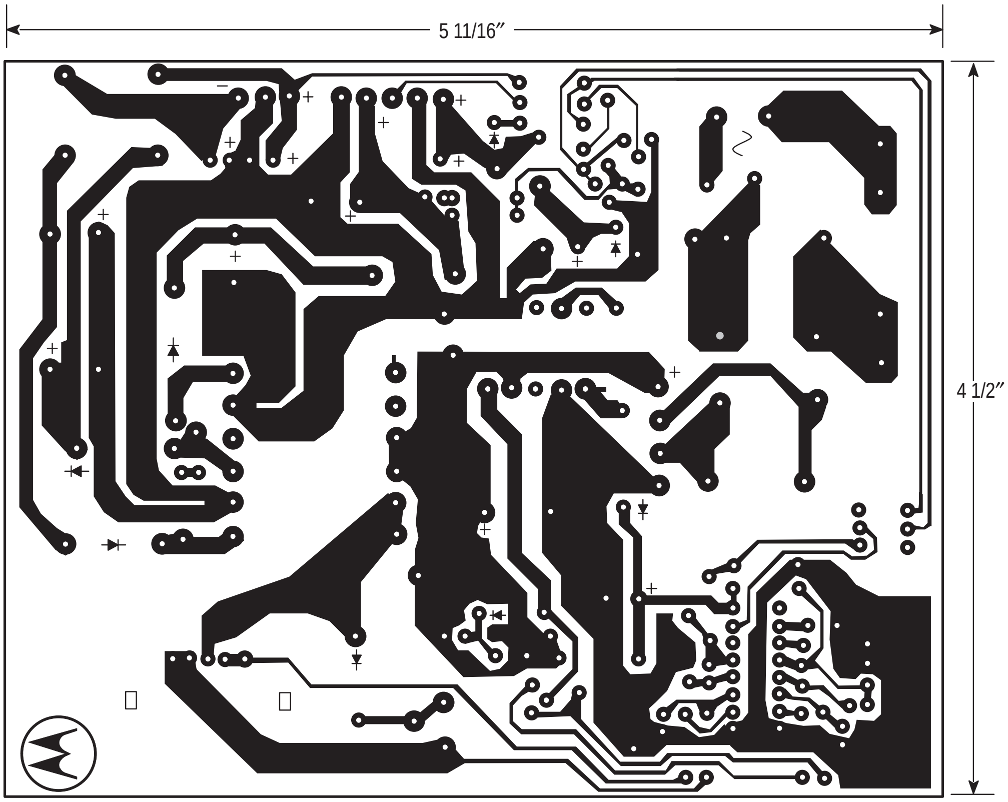
T2 – Primary: 156 Turns, #34 AWG
Primary Feedback: 19 Turns, #34 AWG
Secondary: 17 Turns, #28 AWG
Core: TDK H7C1EE22–Z
Bobbin: BE22–6H
Gap: ≈0.001″ for a primary
inductance of 6.8 mH

T3 – Primary: 56 Turns, #23 AWG
(2 strands) Bifiliar Wound
Secondary: ±12 V, 4 Turns, #23 AWG
(4 strands) Quadfiliar Wound
Secondary 100 V: 32 Turns, #23 AWG
(2 strands) Bifiliar Wound
Core: Ferroxcube EEC 40–3C8
Bobbin: Ferroxcube 40–1112CP
Gap: ≈0.030″ for a primary
inductance of 212 µH

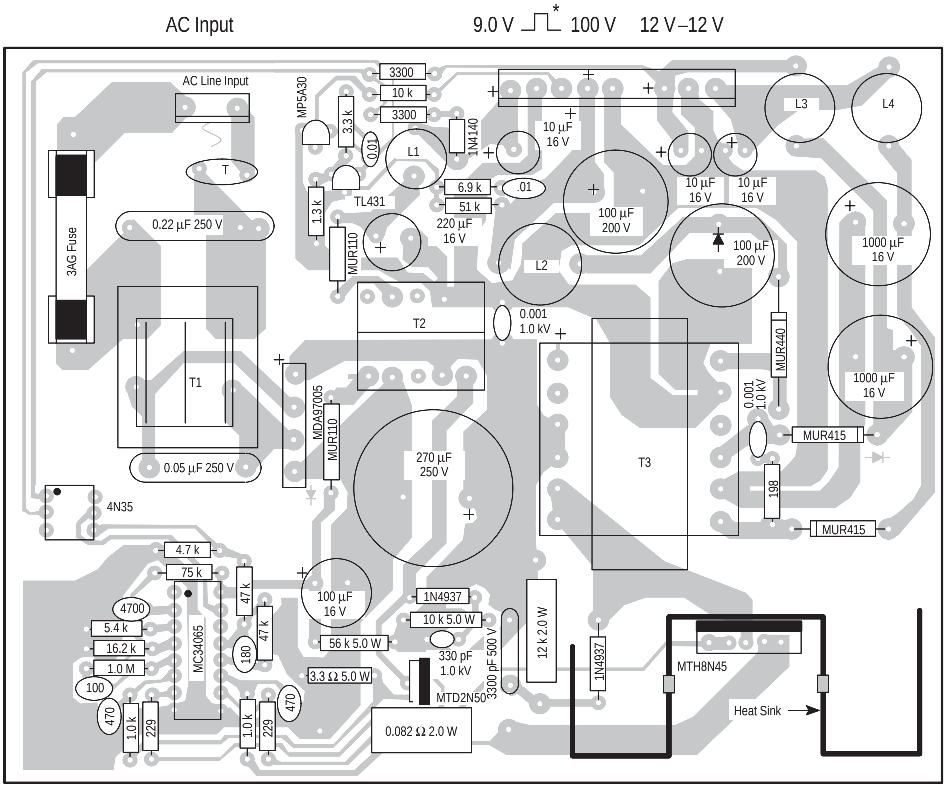
L1, L3, L4 – 25 µH at 1.0 A, Coilcraft Z7157.

L2 – 10 µH at 3.0 A, Coilcraft PCV–0–010–03.

Figure 29. 125 Watt Off–Line Converter



Circuit View



Component View

*100 V and ±12 V Shutdown

MOTOROLA

MC34065-H, L
MC33065-H, L

High Performance Dual Channel Current Mode Controllers

HIGH PERFORMANCE DUAL CHANNEL CURRENT MODE CONTROLLERS

SEMICONDUCTOR TECHNICAL DATA

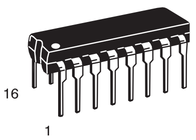
The MC34065–H,L series are high performance, fixed frequency, dual current mode controllers. They are specifically designed for off–line and dc–to–dc converter applications offering the designer a cost effective solution with minimal external components. These integrated circuits feature a unique oscillator for precise duty cycle limit and frequency control, a temperature compensated reference, two high gain error amplifiers, two current sensing comparators, Drive Output 2 Enable pin, and two high current totem pole outputs ideally suited for driving power MOSFETs.

Also included are protective features consisting of input and reference undervoltage lockouts each with hysteresis, cycle–by–cycle current limiting, and a latch for single pulse metering of each output. These devices are available in dual–in–line and surface mount packages.

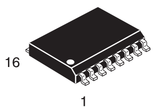
The MC34065–H has UVLO thresholds of 14 V (on) and 10 V (off), ideally suited for off–line converters. The MC34065–L is tailored for lower voltage applications having UVLO thresholds of 8.4 V (on) and 7.8 V (off).

- Unique Oscillator for Precise Duty Cycle Limit and Frequency Control
- Current Mode Operation to 500 kHz
- Automatic Feed Forward Compensation
- Separate Latching PWMs for Cycle–By–Cycle Current Limiting
- Internally Trimmed Reference with Undervoltage Lockout
- Drive Output 2 Enable Pin
- Two High Current Totem Pole Outputs
- Input Undervoltage Lockout with Hysteresis
- Low Startup and Operating Current

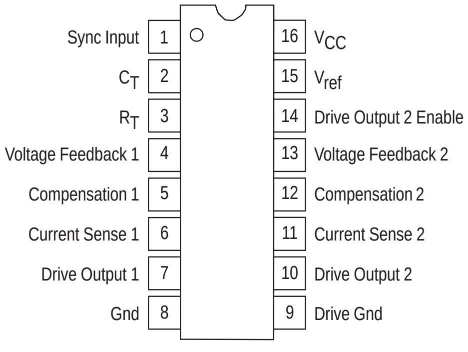
P SUFFIX
PLASTIC PACKAGE
CASE 648



DW SUFFIX
PLASTIC PACKAGE
CASE 751G
(SO–16L)

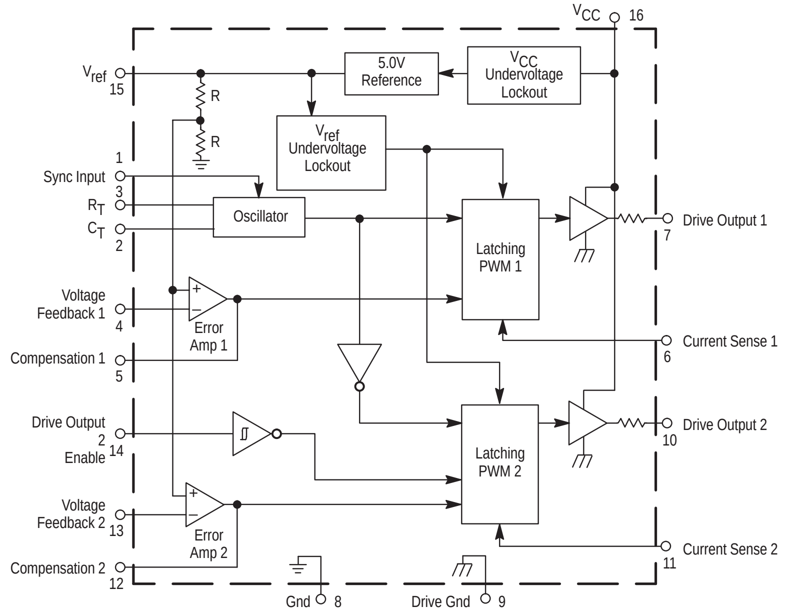


PIN CONNECTIONS



(Top View)

Representative Block Diagram



ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC34065DW–H	T_A = 0° to +70°C	SO–16L
MC34065DW–L		
MC34065P–H		Plastic DIP
MC34065P–L		
MC33065DW–H	T_A = –40° to +85°C	SO–16L
MC33065DW–L		
MC33065P–H		Plastic DIP
MC33065P–L		

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	20	V
Output Current, Source or Sink (Note 1)	I_O	400	mA
Output Energy (Capacitive Load per Cycle)	W	5.0	μJ
Current Sense, Enable, and Voltage Feedback Inputs	V_{in}	– 0.3 to +5.5	V
Sync Input			
High State (Voltage)	V_{IH}	+5.5	V
Low State (Reverse Current)	I_{IL}	– 5.0	mA
Error Amp Output Sink Current	I_O	10	mA
Power Dissipation and Thermal Characteristics			
DW Suffix, Plastic Package Case 751G			
Maximum Power Dissipation @ T_A = 25°C	P_D	862	mW
Thermal Resistance, Junction–to–Air	$R_{\theta JA}$	145	°C/W
P Suffix, Plastic Package Case 648			
Maximum Power Dissipation @ T_A = 25°C	P_D	1.25	mW
Thermal Resistance, Junction–to–Air	$R_{\theta JA}$	100	°C/W
Operating Junction Temperature	T_J	+150	°C
Operating Ambient Temperature (Note 3)	T_A		°C
MC34065		0 to +70	
MC33065		– 40 to +85	
Storage Temperature Range	T_{stg}	– 65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V [Note 2], R_T = 8.2 kΩ, C_T = 3.3 nF, for typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies to [Note 3].)

Characteristics	Symbol	Min	Typ	Max	Unit
REFERENCE SECTION					
Reference Output Voltage (I_O = 1.0 mA, T_J = 25°C)	V_{ref}	4.85	5.0	5.13	V
Line Regulation (V_{CC} = 11 V to 20 V)	Reg_{line}	–	2.0	20	mV
Load Regulation (I_O = 1.0 mA to 10 mA, V_{CC} = 20 V)	Reg_{load}	–	3.0	25	mV
Total Output Variation over Line, Load, and Temperature	V_{ref}	4.8	–	5.15	V
Output Short Circuit Current	I_{SC}	30	100	–	mA
OSCILLATOR AND PWM SECTIONS					
Total Frequency Variation over Line and Temperature	f_{osc}				kHz
V_{CC} = 11 V to 20 V, T_A = T_{low} to T_{high}					
MC34065		46.5	49	51.5	
MC33065		45	49	53	
Frequency Change with Voltage (V_{CC} = 11 V to 20 V)	$\Delta f_{osc}/\Delta V$	–	0.2	1.0	%
Duty Cycle at each Output					%
Maximum	DC_{max}	46	49.5	52	
Minimum	DC_{min}	–	–	0	
Sync Input Current					μA
High State (V_{in} = 2.4 V)	I_{IH}	–	170	250	
Low State (V_{in} = 0.8 V)	I_{IL}	–	80	160	
ERROR AMPLIFIERS					
Voltage Feedback Input (V_O = 2.5 V)	V_{FB}	2.45	2.5	2.55	V
Input Bias Current (V_{FB} = 5.0 V)	I_{IB}	–	– 0.1	– 1.0	μA
Open Loop Voltage Gain (V_O = 2.0 V to 4.0 V)	A_{VOL}	65	100	–	dB
Unity Gain Bandwidth (T_J = 25°C)	BW	0.7	1.0	–	MHz
Power Supply Rejection Ratio (V_{CC} = 11 V to 20 V)	PSRR	60	90	–	dB
Output Current					mA
Source (V_O = 3.0 V, V_{FB} = 2.3 V)	I_{source}	0.45	1.0	–	
Sink (V_O = 1.2 V, V_{FB} = 2.7 V)	I_{sink}	2.0	12	–	
Output Voltage Swing					V
High State (R_L = 15 k to ground, V_{FB} = 2.3 V)	V_{OH}	5.0	6.2	–	
Low State (R_L = 15 k to V_{ref}, V_{FB} = 2.7 V)	V_{OL}	–	0.8	1.1	

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V [Note 2], R_T = 8.2 kΩ, C_T = 3.3 nF, for typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies to [Note 3].)

Characteristics	Symbol	Min	Typ	Max	Unit
CURRENT SENSE SECTION					
Current Sense Input Voltage Gain (Notes 4 and 5)	A_V	2.75	3.0	3.25	V/V
Maximum Current Sense Input Threshold (Note 4)	V_{th}	0.9	1.0	1.1	V
Input Bias Current	I_{IB}	–	– 2.0	– 10	µA
Propagation Delay (Current Sense Input to Output)	$t_{PLN(In/Out)}$	–	150	300	ns
DRIVE OUTPUT 2 ENABLE PIN					
Enable Pin Voltage – High State (Output 2 Enabled) – Low State (Output 2 Disabled)	V_{IH} V_{IL}	3.5 0	– –	V_{ref} 1.5	V
Low State Input Current (V_{IL} = 0 V)	I_{IB}	100	250	400	µA
DRIVE OUTPUTS					
Output Voltage – Low State (I_{sink} = 20 mA) (I_{sink} = 200 mA) – High State (I_{source} = 20 mA) (I_{source} = 200 mA)	V_{OL} V_{OH}	– 1.6 12.8 10	0.3 2.4 13.3 11.2	0.5 3.0 – 12.3	V
Output Voltage with UVLO Activated (V_{CC} = 6.0 V, I_{Sink} = 1.0 mA)	$V_{OL(UVLO)}$	–	0.1	1.1	V
Output Voltage Rise Time (C_L = 1.0 nF)	t_r	–	50	150	ns
Output Voltage Fall Time (C_L = 1.0 nF)	t_f	–	50	150	ns
UNDERVOLTAGE LOCKOUT SECTION					
Startup Threshold (V_{CC} Increasing) –L Suffix –H Suffix	V_{th}	 7.8 13	 8.4 14	 9.0 15	V
Minimum Operating Voltage After Turn–On (V_{CC} Decreasing) –L Suffix –H Suffix	$V_{CC(min)}$	 7.2 9.0	 7.8 10	 8.4 11	V
TOTAL DEVICE					
Power Supply Current Startup –L Suffix (V_{CC} = 6.0 V) –H Suffix (V_{CC} = 12 V) Operating (Note 2)	I_{CC}	 – – –	 0.4 0.6 20	 0.8 1.0 25	mA

NOTES: 1. Maximum package power dissipation limits must be observed.
2. Adjust V_{CC} above the startup threshold before setting to 15 V.
3. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible:
T_{low} = 0°C for the MC34065 T_{high} = +70°C for MC34065
T_{low} = –40°C for the MC33065 T_{high} = +85°C for MC33065
4. This parameter is measured at the latch trip point with V_{FB} = 0 V
5. Comparator gain is defined as $AV = \frac{\Delta V \text{ Compensation}}{\Delta V \text{ Current Sense}}$

Figure 1. Timing Resistor versus Oscillator Frequency

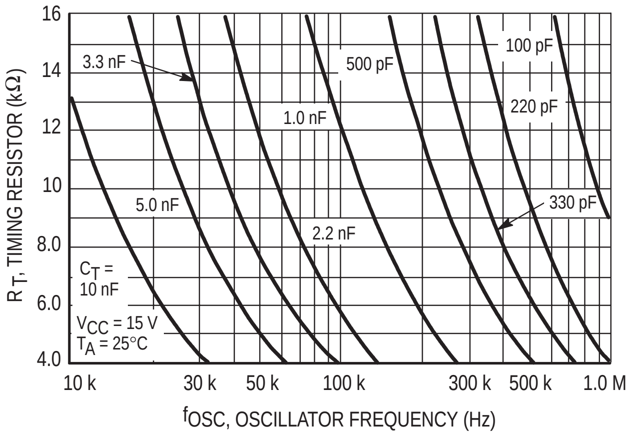


Figure 2. Maximum Output Duty Cycle versus Oscillator Frequency

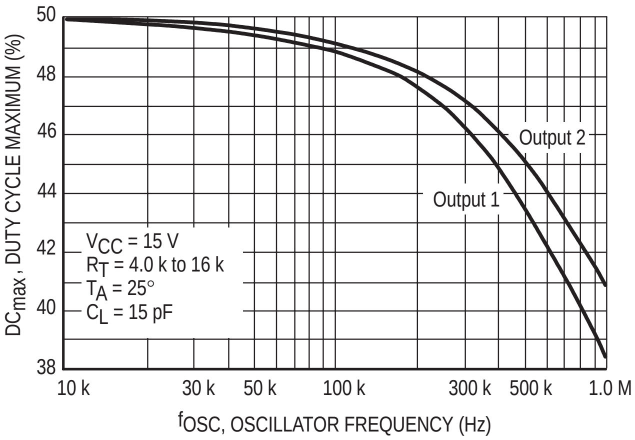


Figure 3. Error Amp Small–Signal Transient Response

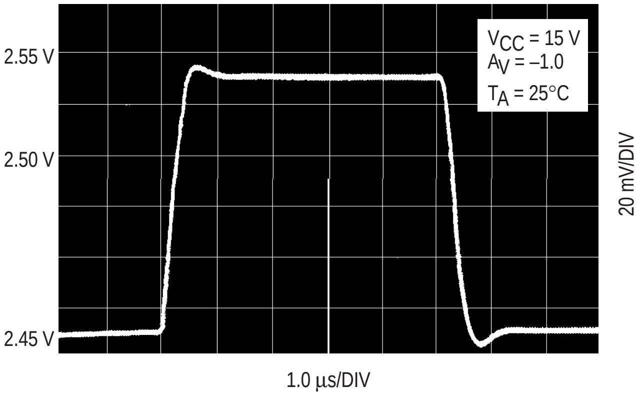


Figure 4. Error Amp Large–Signal Transient Response

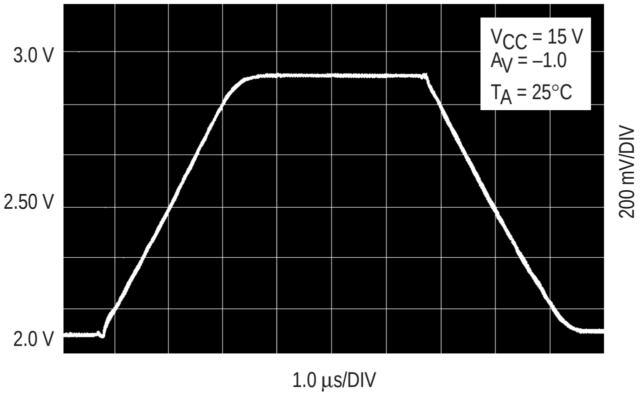


Figure 5. Error Amp Open Loop Gain and Phase versus Frequency

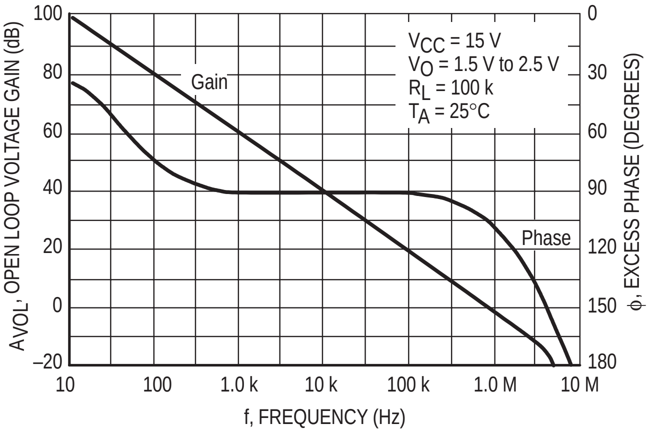


Figure 6. Current Sense Input Threshold versus Error Amp Output Voltage

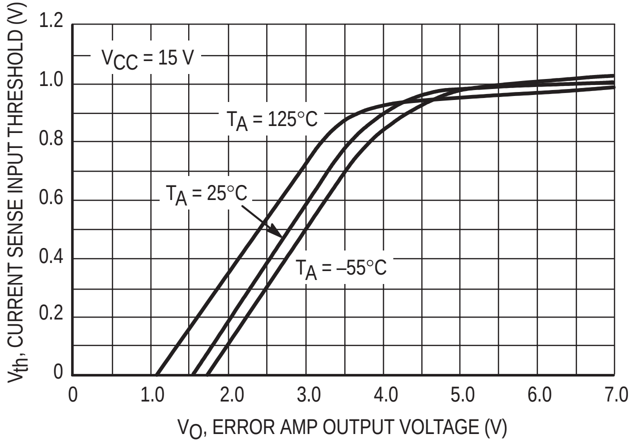


Figure 7. Reference Voltage Change versus Source Current

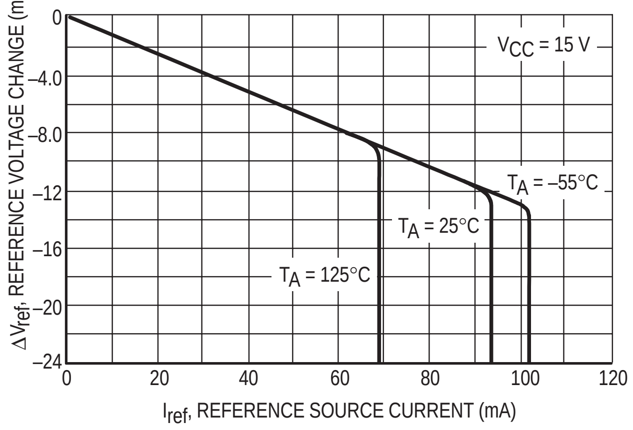


Figure 8. Reference Short Circuit Current versus Temperature

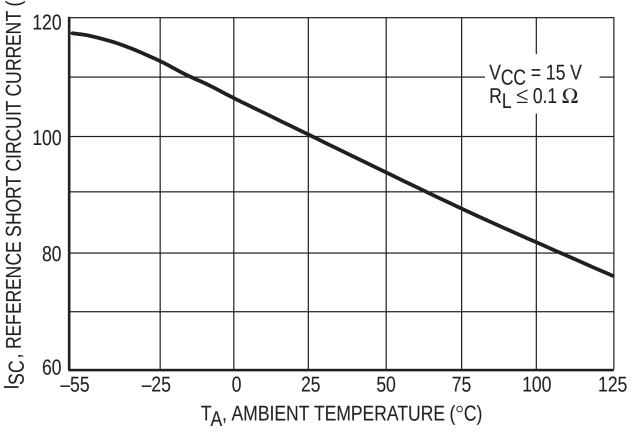


Figure 9. Reference Load Regulation

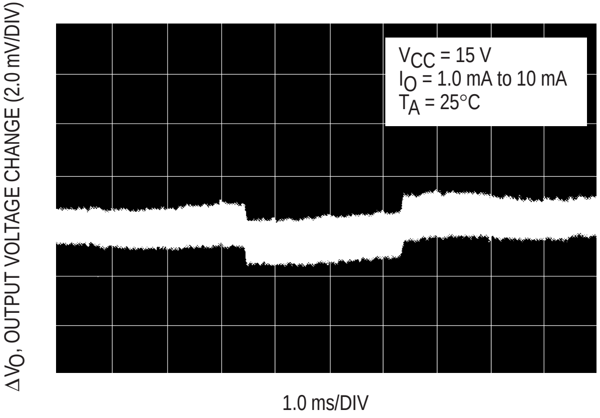


Figure 10. Reference Line Regulation

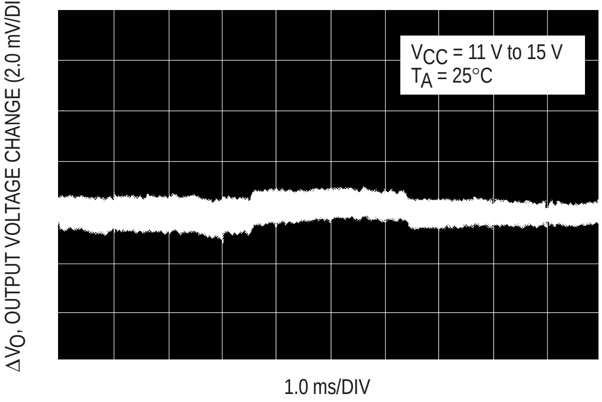


Figure 11. Output Saturation Voltage versus Load Current

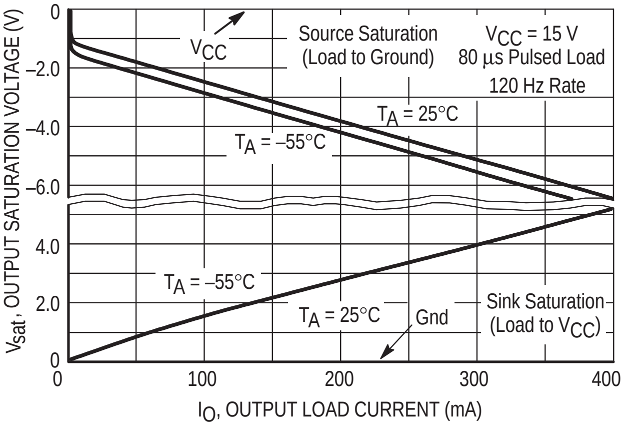


Figure 12. Output Waveform

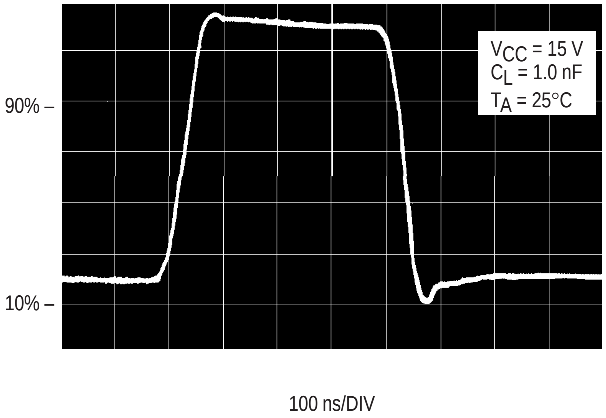


Figure 13. Output Cross Conduction Current

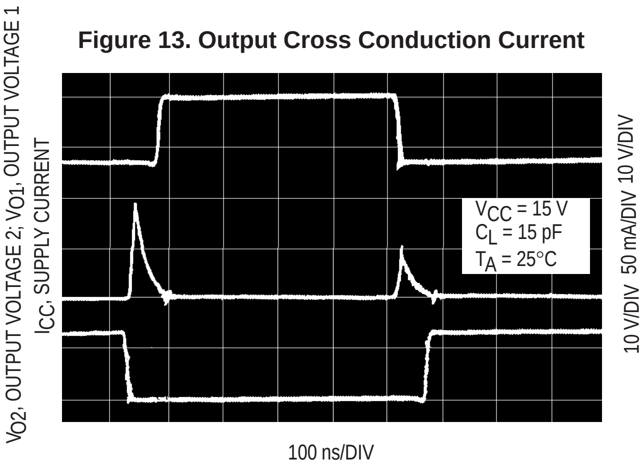
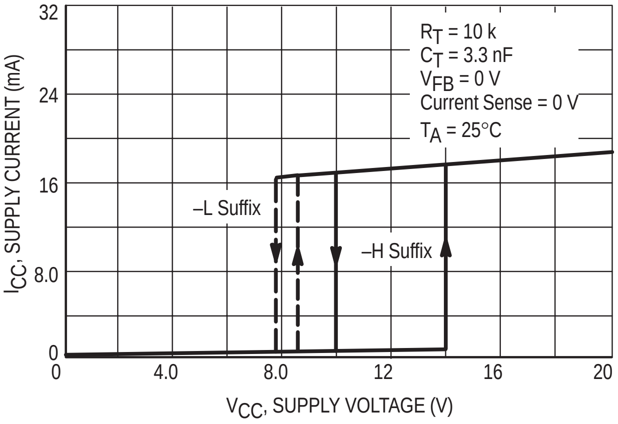


Figure 14. Supply Current versus Supply Voltage



OPERATING DESCRIPTION

The MC34065–H,L series are high performance, fixed frequency, dual channel current mode controllers specifically designed for Off–Line and dc–to–dc converter applications. These devices offer the designer a cost effective solution with minimal external components where independent regulation of two power converters is required. The Representative Block Diagram is shown in Figure 15. Each channel contains a high gain error amplifier, current sensing comparator, pulse width modulator latch, and totem pole output driver. The oscillator, reference regulator, and undervoltage lock–out circuits are common to both channels.

Oscillator

The unique oscillator configuration employed features precise frequency and duty cycle control. The frequency is programmed by the values selected for the timing components R_T and C_T. Capacitor C_T is charged and discharged by an equal magnitude internal current source and sink, generating a symmetrical 50 percent duty cycle waveform at Pin 2. The oscillator peak and valley thresholds are 3.5 V and 1.6 V respectively. The source/sink current magnitude is controlled by resistor R_T. For proper operation over temperature it must be in the range of 4.0 kΩ to 16 kΩ as shown in Figure 1.

As C_T charges and discharges, an internal blanking pulse is generated that alternately drives the center inputs of the upper and lower NOR gates high. This, in conjunction with a precise amount of delay time introduced into each channel, produces well defined non–overlapping output duty cycles. Output 2 is enabled while C_T is charging, and Output 1 is enabled during the discharge. Figure 2 shows the Maximum Output Duty Cycle versus Oscillator Frequency. Note that even at 500 kHz, each output is capable of approximately 44% on–time, making this controller suitable for high frequency power conversion applications.

In many noise sensitive applications it may be desirable to frequency–lock the converter to an external system clock. This can be accomplished by applying a clock signal as shown in Figure 17. For reliable locking, the free–running oscillator frequency should be set about 10% less than the clock frequency. Referring to the timing diagram shown in Figure 16, the rising edge of the clock signal applied to the Sync input, terminates charging of C_T and Drive Output 2 conduction. By tailoring the clock waveform symmetry, accurate duty cycle clamping of either output can be achieved. A circuit method for this, and multi–unit synchronization, is shown in Figure 18.

Error Amplifier

Each channel contains a fully–compensated Error Amplifier with access to the inverting input and output. The amplifier features a typical dc voltage gain of 100 dB, and a unity gain bandwidth of 1.0 MHz with 71° of phase margin (Figure 5). The noninverting input is internally biased at 2.5 V and is not pinned out. The converter output voltage is typically divided down and monitored by the inverting input through a resistor divider. The maximum input bias current is –1.0 µA which will cause an output voltage error that is equal to the product of the input bias current and the equivalent input divider source resistance.

The Error Amp output (Pin 5, 12) is provided for external loop compensation. The output voltage is offset by two diode drops (≈1.4 V) and divided by three before it connects to the inverting input of the Current Sense Comparator. This guarantees that no pulses appear at the Drive Output (Pin 7, 10) when the error amplifier output is at its lowest state (V_{OL}). This occurs when the power supply is operating and the load is removed, or at the beginning of a soft–start interval (Figures 20, 21).

The minimum allowable Error Amp feedback resistance is limited by the amplifier's source current (0.5 mA) and the output voltage (V_{OH}) required to reach the comparator's 1.0 V clamp level with the inverting input at ground. This condition happens during initial system startup or when the sensed output is shorted:

$$R_{f(min)} \approx \frac{3.0\ (1.0\ V)\ +\ 1.4\ V}{0.5\ mA} = 8800\ \Omega$$

Current Sense Comparator and PWM Latch

The MC34065 operates as a current mode controller, whereby output switch conduction is initiated by the oscillator and terminated when the peak inductor current reaches the threshold level established by the Error Amplifier output. Thus the error signal controls the peak inductor current on a cycle–by–cycle basis. The Current Sense Comparator–PWM Latch configuration used ensures that only a single pulse appears at the Drive Output during any given oscillator cycle. The inductor current is converted to a voltage by inserting a ground–referenced sense resistor R_S in series with the source of output switch Q1. This voltage is monitored by the Current Sense Input (Pin 6, 11) and compared to a level derived from the Error Amp output. The peak inductor current under normal operating conditions is controlled by the voltage at Pin 5, 12 where:

$$I_{pk} = \frac{V_{(Pin\ 5,\ 12)} - 1.4\ V}{3\ R_S}$$

Abnormal operating conditions occur when the power supply output is overloaded or if output voltage sensing is lost. Under these conditions, the Current Sense Comparator threshold will be internally clamped to 1.0 V. Therefore the maximum peak switch current is:

$$I_{pk(max)} = \frac{1.0\ V}{R_S}$$

When designing a high power switching regulator it may be desirable to reduce the internal clamp voltage in order to keep the power dissipation of R_S to a reasonable level. A simple method to adjust this voltage is shown in Figure 19. The two external diodes are used to compensate the internal diodes, yielding a constant clamp voltage over temperature. Erratic operation due to noise pickup can result if there is an excessive reduction of the $I_{pk(max)}$ clamp voltage.

A narrow spike on the leading edge of the current waveform can usually be observed and may cause the power supply to exhibit an instability when the output is lightly loaded. This spike is due to the power transformer interwinding capacitance and output rectifier recovery time. The addition of an RC filter on the Current Sense input with a time constant that approximates the spike duration will usually eliminate the instability, refer to Figure 24.

Undervoltage Lockout

Two Undervoltage Lockout comparators have been incorporated to guarantee that the IC is fully functional before the output stages are enabled. The positive power supply terminal (V_{CC}) and the reference output (V_{ref}) are each monitored by separate comparators. Each has built–in hysteresis to prevent erratic output behavior as their respective thresholds are crossed. The V_{CC} comparator upper and lower thresholds are 14 V/10 V for –H suffix, and 8.4 V/7.6 V for –L suffix. The V_{ref} comparator upper and lower thresholds are 3.6 V/3.4 V respectively. The large hysteresis and low startup current of the –H suffix version makes it ideally suited in off–line converter applications where efficient bootstrap startup techniques are required (Figure 28). The –L suffix version is intended for lower voltage dc–to–dc converter applications. The minimum operating voltage for the –H suffix is 11 V and 8.2 V for the –L suffix.

Drive Outputs and Drive Ground

Each section contains a single totem–pole output stage that is specifically designed for direct drive of power MOSFETs. The Drive Outputs are capable of up to ±400 mA peak current with a typical rise and fall time of 50 ns with a 1.0 nF load. Additional internal circuitry has been added to keep the outputs in a sinking mode whenever an Undervoltage Lockout is active. This characteristic eliminates the need for an external pull–down resistor. The totem–pole output has been optimized to minimize cross–conduction current in high speed operation. The addition of two 10 Ω resistors, one in series with the source output transistor and one in series with the sink output transistor, reduces the cross–conduction current to minimal levels, as shown in Figure 13.

Although the Drive Outputs were optimized for MOSFETs, they can easily supply the negative base current required by bipolar NPN transistors for enhanced turn–off (Figure 25).

Figure 15. Representative Block Diagram

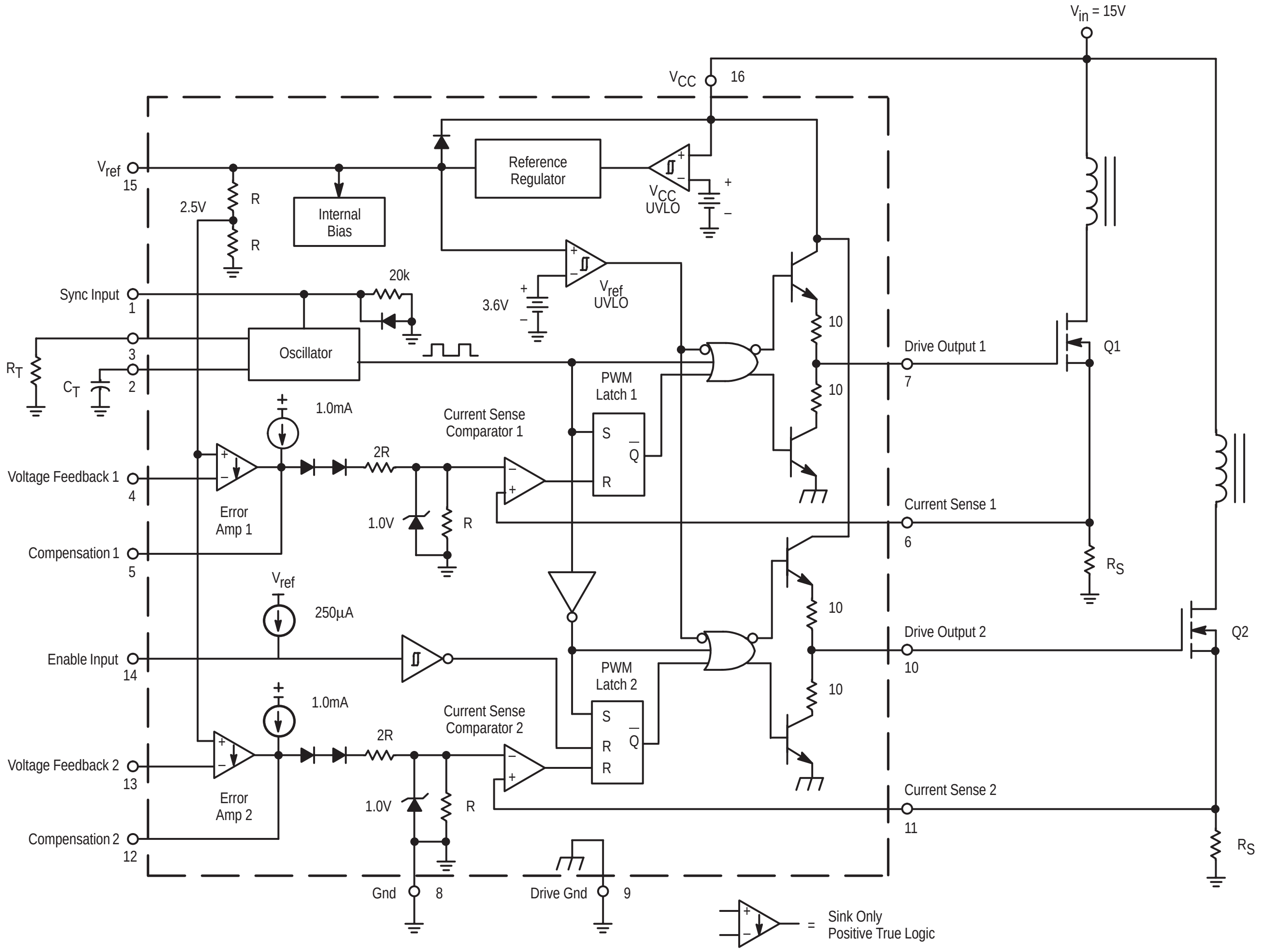
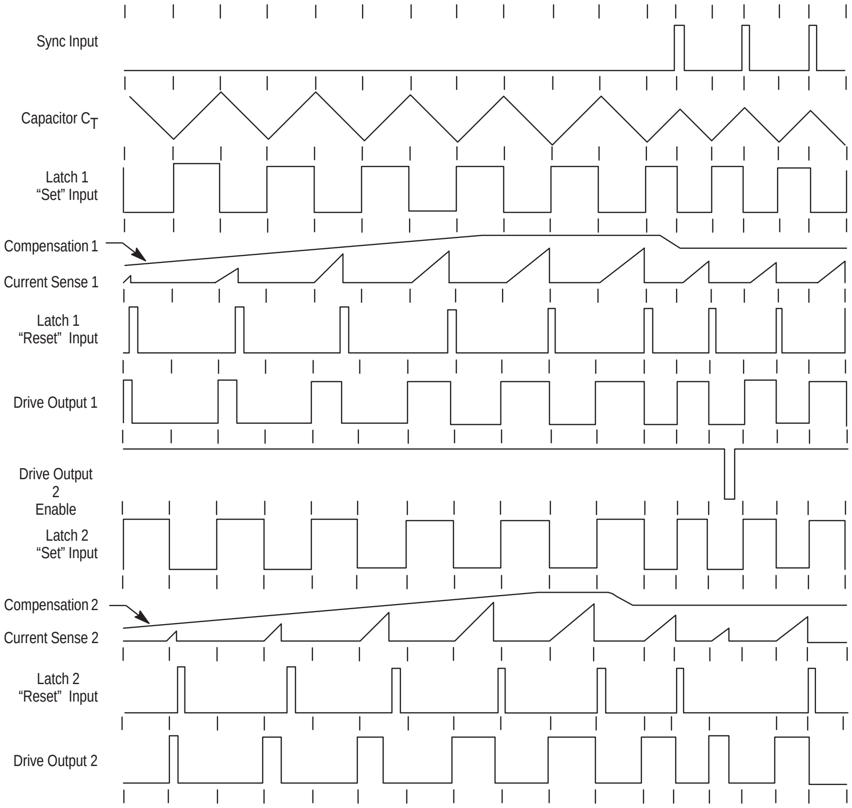


Figure 16. Timing Diagram



The outputs do not contain internal current limiting, therefore an external series resistor may be required to prevent the peak output current from exceeding the ±400 mA maximum rating. The sink saturation (V_{OL}) is less than 0.75 V at 50 mA.

A separate Drive Ground pin is provided and, with proper implementation, will significantly reduce the level of switching transient noise imposed on the control circuitry. This becomes particularly useful when reducing the $I_{pk(max)}$ clamp level. Figure 23 shows the proper ground connections required for current sensing power MOSFET applications.

Drive Output 2 Enable Pin

This input is used to enable Drive Output 2. Drive Output 1 can be used to control circuitry that must run continuously such as volatile memory and the system clock, or a remote controlled receiver, while Drive Output 2 controls the high power circuitry that is occasionally turned off.

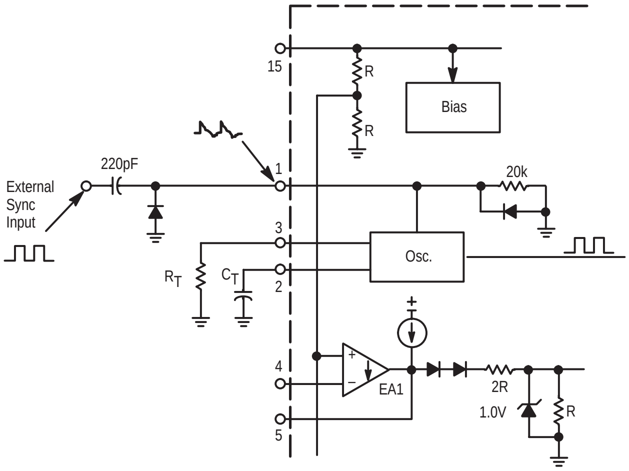
Reference

The 5.0 V bandgap reference is trimmed to ±2.0% tolerance at T_J = 25°C. The reference has short circuit protection and is capable of providing in excess of 30 mA for powering any additional control system circuitry.

Design Considerations

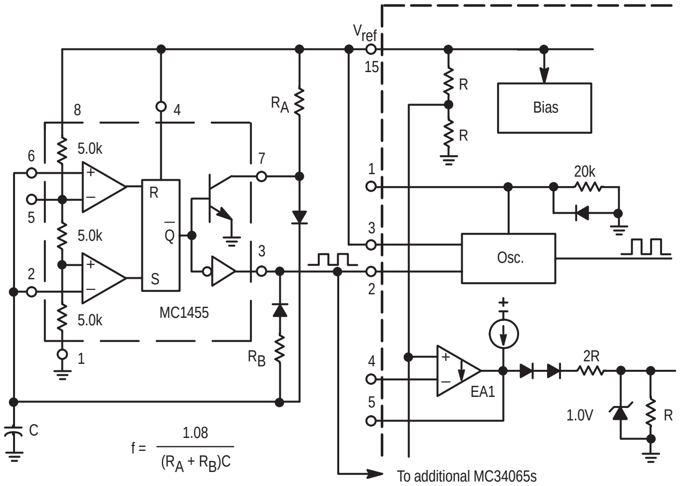
Do not attempt to construct the converter on wire–wrap or plug–in prototype boards. High frequency circuit layout techniques are imperative to prevent pulse–width jitter. This is usually caused by excessive noise pick–up imposed on the Current Sense or Voltage Feedback inputs. Noise immunity can be improved by lowering circuit impedances at these points. The printed circuit layout should contain a ground plane with low current signal and high current switch and output grounds returning on separate paths back to the input filter capacitor. Ceramic bypass capacitors (0.1 μF) connected directly to V_{CC} and V_{ref} may be required depending upon circuit layout. This provides a low impedance path for filtering the high frequency noise. All high current loops should be kept as short as possible using heavy copper runs to minimize radiated EMI. The Error Amp compensation circuitry and the converter output voltage–divider should be located close to the IC and as far as possible from the power switch and other noise generating components.

Figure 17. External Clock Synchronization



The external diode clamp is required if the negative Sync current is greater than –5.0 mA.

Figure 18. External Duty Cycle Clamp and Multi–Unit Synchronization



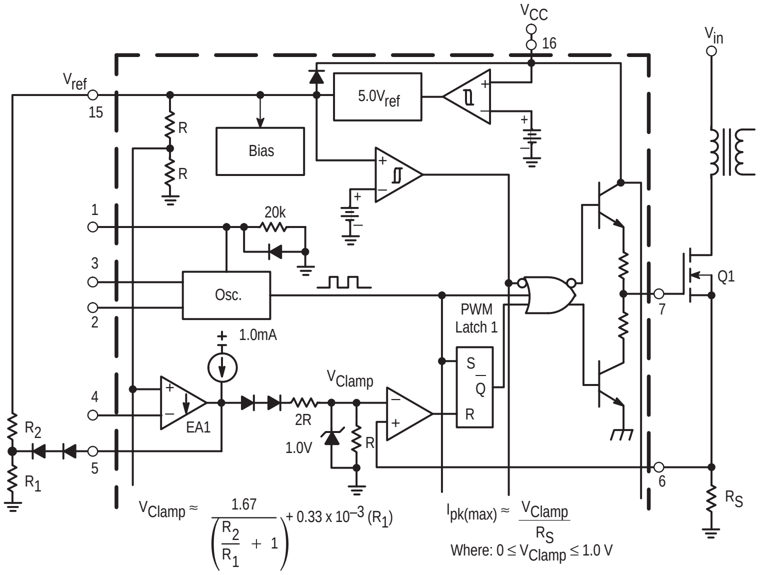
$$f = \frac{1.08}{(R_A + R_B)C}$$

$$D_{max}\ \text{Drive Output 1} = \frac{R_B}{R_A + R_B} \qquad D_{max}\ \text{Drive Output 2} = \frac{R_A}{R_A + R_B}$$

PIN FUNCTION DESCRIPTION

Pin	Function	Description
1	Sync Input	A narrow rectangular waveform applied to this input will synchronize the oscillator. A dc voltage within the range of 2.4 V to 5.5 V will inhibit the oscillator.
2	C_T	Timing capacitor C_T connects from this pin to ground setting the free–running oscillator frequency range.
3	R_T	Resistor R_T connects from this pin to ground precisely setting the charge current for C_T. R_T must be between 4.0 k and 16 k.
4	Voltage Feedback 1	This pin is the inverting input of Error Amplifier 1. It is normally connected to the switching power supply output through a resistor divider.
5	Compensation 1	This pin is the output of Error Amplifier 1 and is made available for loop compensation.
6	Current Sense 1	A voltage proportional to the inductor current is connected to this input. PWM 1 uses this information to terminate conduction of output switch Q1.
7	Drive Output 1	This pin directly drives the gate of a power MOSFET Q1. Peak currents up to 400 mA are sourced and sunk by this pin.
8	Gnd	This pin is the control circuitry ground return and is connected back to the source ground.
9	Drive Gnd	This pin is a separate power ground return that is connected back to the power source. It is used to reduce the effects of switching transient noise on the control circuitry.
10	Drive Output 2	This pin directly drives the gate of a power MOSFET Q2. Peak currents up to 400 mA are sourced and sunk by this pin.
11	Current Sense 2	A voltage proportional to inductor current is connected to this input. PWM 2 uses this information to terminate conduction of output switch Q2.
12	Compensation 2	This pin is the output of Error Amplifier 2 and is made available for loop compensation.
13	Voltage Feedback 2	This pin is the inverting input of Error Amplifier 2. It is normally connected to the switching power supply output through a resistor divider.
14	Drive Output 2 Enable	A logic low at this input disables Drive Output 2.
15	V_{ref}	This is the 5.0 V reference output. It can provide bias for any additional system circuitry.
16	V_{CC}	This pin is the positive supply of the control IC. The minimum operating voltage range after startup is 11 V to 15.5 V for the –H suffix, 8.2 V to 9.5 V for the –L suffix.

Figure 19. Adjustable Reduction of Clamp Level

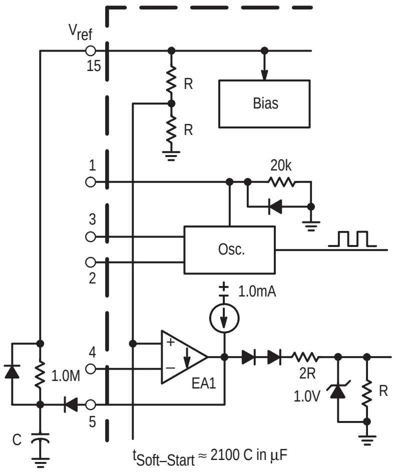


$$V_{Clamp} \approx \frac{1.67}{\left(\frac{R_2}{R_1} + 1\right)} + 0.33 \times 10^{-3}\,(R_1)$$

$$I_{pk(max)} \approx \frac{V_{Clamp}}{R_S}$$

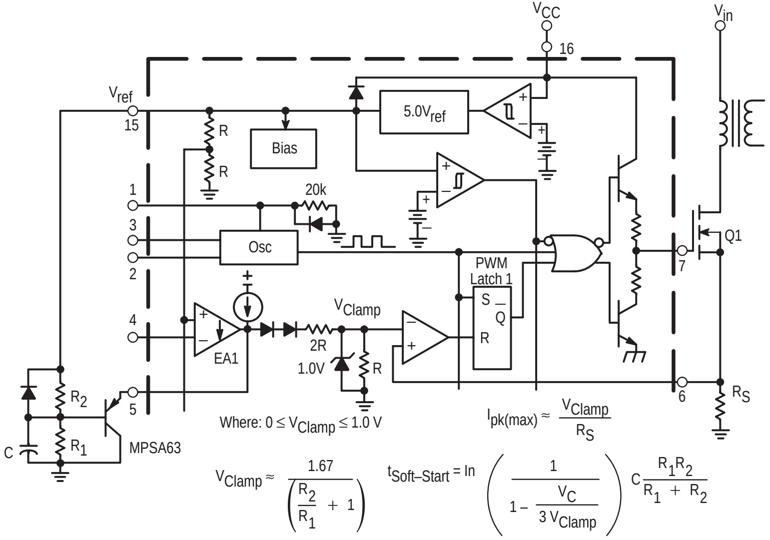
Where: $0 \le V_{Clamp} \le 1.0$ V

Figure 20. Soft–Start Circuit



$t_{Soft–Start} \approx 2100$ C in µF

Figure 21. Adjustable Reduction of Clamp Level with Soft–Start

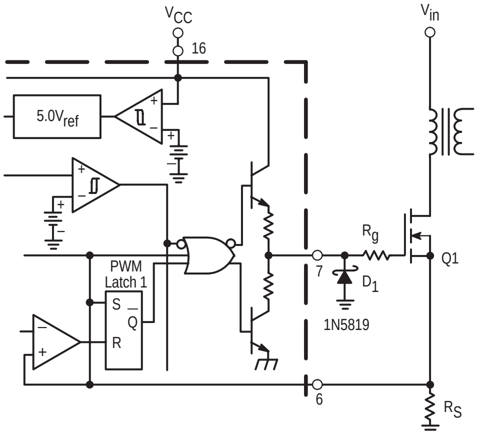


Where: $0 \le V_{Clamp} \le 1.0$ V

$$I_{pk(max)} \approx \frac{V_{Clamp}}{R_S}$$

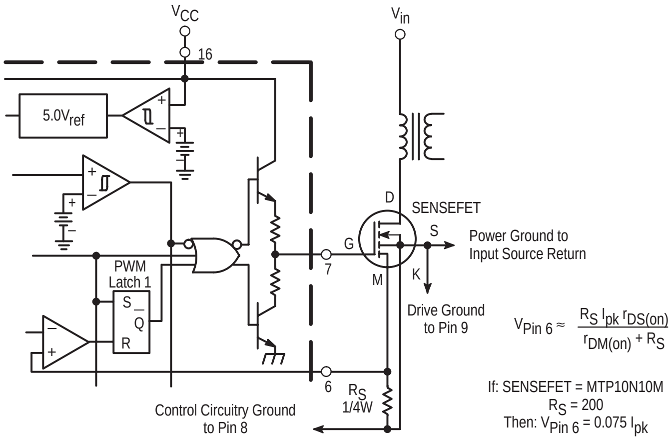
$$V_{Clamp} \approx \frac{1.67}{\left(\frac{R_2}{R_1} + 1\right)} \qquad t_{Soft–Start} = \ln\left(\frac{1}{1 - \frac{V_C}{3\,V_{Clamp}}}\right) C\,\frac{R_1R_2}{R_1 + R_2}$$

Figure 22. MOSFET Parasitic Oscillations



Series gate resistor R_g may be needed to damp high frequency parasitic oscillations caused by the MOSFET input capacitance and any series wiring inductance in the gate–source circuit. R_g will decrease the MOSFET switching speed. Schottky diode D_1 is required if circuit ringing drives the output pin below ground.

Figure 23. Current Sensing Power MOSFET

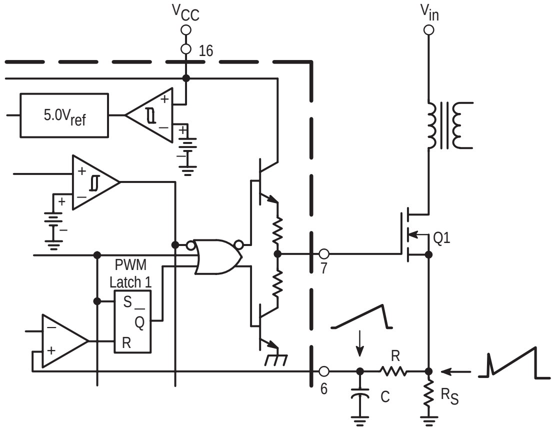


$$V_{Pin\ 6} \approx \frac{R_S\, I_{pk}\, r_{DS(on)}}{r_{DM(on)} + R_S}$$

If: SENSEFET = MTP10N10M
$R_S = 200$
Then: $V_{Pin\ 6} = 0.075\ I_{pk}$

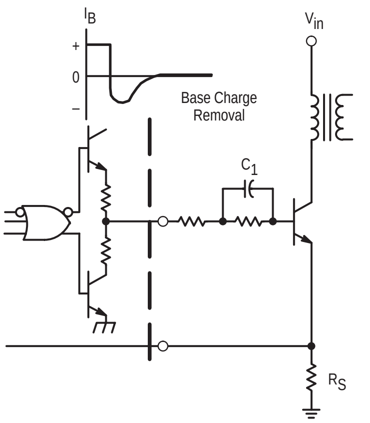
Virtually lossless current sensing can be achieved with the implementation of a SENSEFET power switch. For proper operation during over current conditions, a reduction of the $I_{pk(max)}$ clamp level must be implemented. Refer to Figures 19 and 21.

Figure 24. Current Waveform Spike Suppression



The addition of the RC filter will eliminate instability caused by the leading edge spike on the current waveform.

Figure 25. Bipolar Transistor Drive



The totem–pole outputs can furnish negative base current for enhanced transistor turn–off, with the addition of capacitor C_1.

Figure 26. Isolated MOSFET Drive

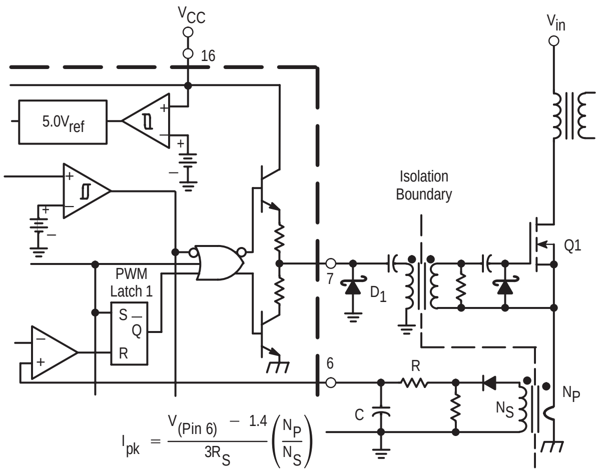
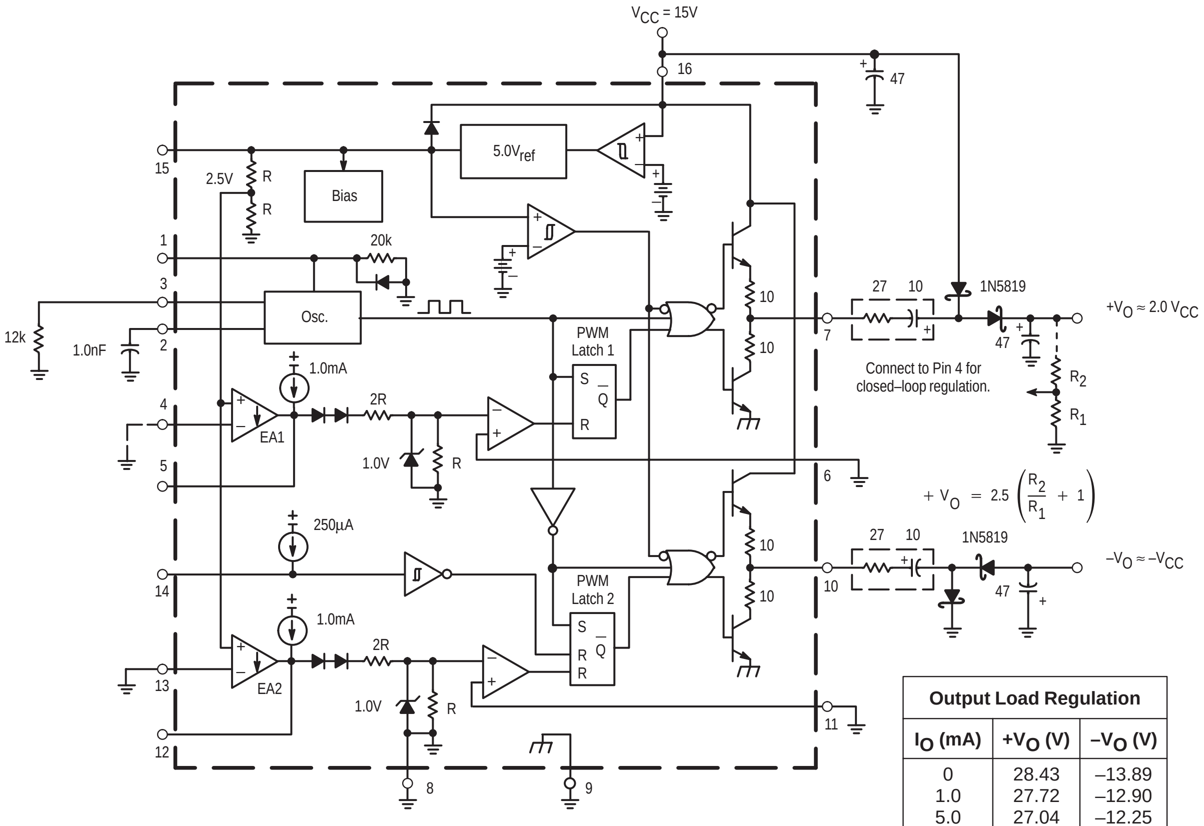


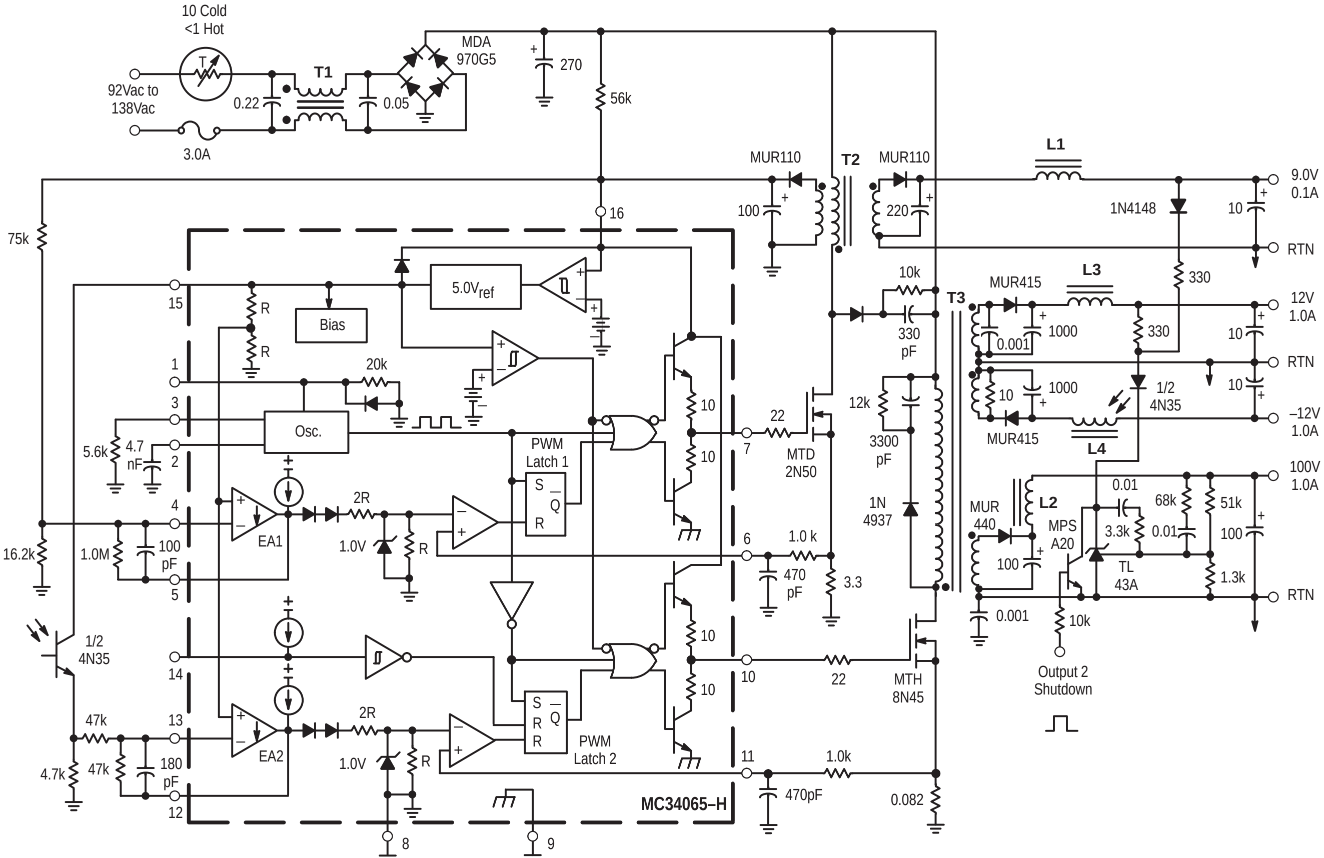
Figure 27. Dual Charge Pump Converter



Output Load Regulation		
I_O (mA)	$+V_O$ (V)	$–V_O$ (V)
0	28.43	–13.89
1.0	27.72	–12.90
5.0	27.04	–12.25
10	26.20	–11.44
50	20.52	–5.80

The capacitor's equivalent series resistance must limit the Drive Output current to 400 mA. An additional series resistor may be required when using tantalum or other low ESR capacitors. The positive output can provide excellent line and load regulation by connecting the R_2/R_1 resistor divider as shown.

Figure 28. 125 Watt Off–Line Converter



Test	Conditions	Results
Line Regulation 100 V Output ±12 V Outputs 9.0 V Output	V_{in} = 92 Vac to 138 Vac I_O = 1.0 A I_O = ±1.0 A I_O = 0.1 A	Δ = 40 mV or ±0.02% Δ = 32 mV or ±0.13% Δ = 55 mV or ±0.31%
Load Regulation 100 V Output ±12 V Outputs 9.0 V Output	V_{in} = 115 Vac I_O = 0.25 A to 1.0 A I_O = ±0.25 A to ±1.0 A I_O = 0.08 A to 0.1 A	Δ = 50 mV or ±0.025% Δ = 320 mV or ±1.2% Δ = 234 mV or ±1.3%
Output Ripple 100 V Output ±12 V Outputs 9.0 V Output	V_{in} = 115 Vac I_O = 1.0 A I_O = ±1.0 A I_O = 0.1 A	40 mVpp 100 mVpp 60 mVpp
Short Circuit Current 100 V Output ±12 V Outputs 9.0 V Output	V_{in} = 115 Vac, R_L = 0.1 Ω	4.3 A 17 A Output Hiccups
Efficiency	Vin = 115 Vac, PO = 125 W	86%

T1 – 468 µH per section at 2.5 A, Coilcraft E3496A.

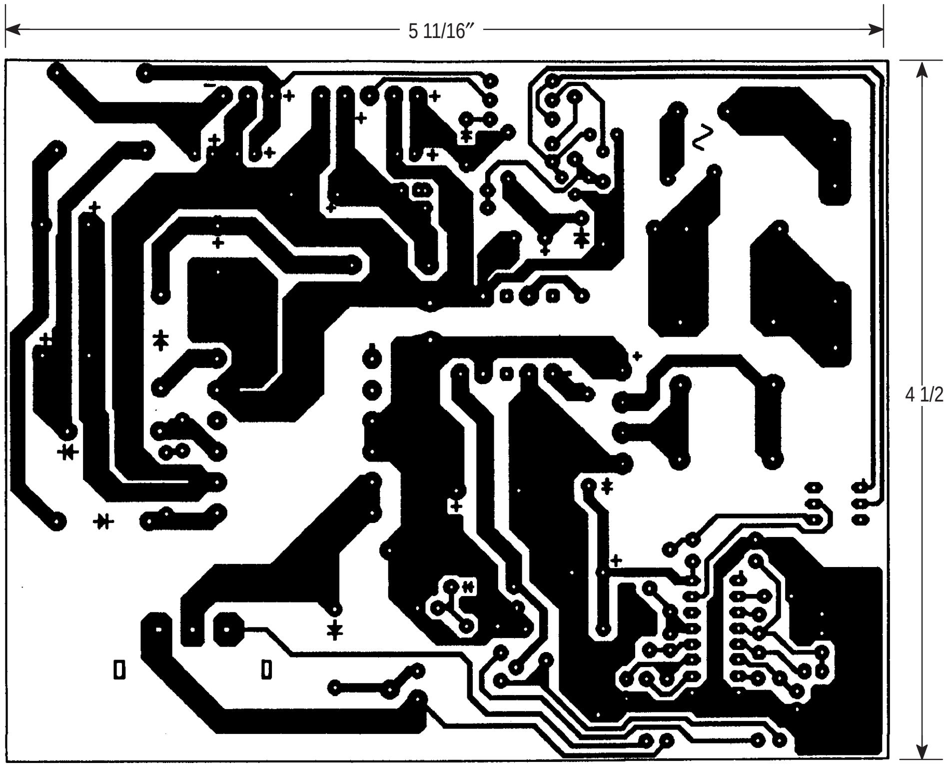
T2 – Primary: 156 Turns, #34 AWG
Primary Feedback: 19 Turns, #34 AWG
Secondary: 17 Turns, #28 AWG
Core: TDK PC30 EE22–Z
Bobbin: BE22–118CP
Gap: ≈0.001″ for a primary inductance of 6.8 mH

T3 – Primary: 56 Turns, #23 AWG (2 strands) Bifiliar Wound
Secondary: ±12 V, 4 Turns, #23 AWG (4 strands) Quadfiliar Wound
Secondary 100 V: 32 Turns, #23 AWG (2 strands) Bifiliar Wound
Core: TDK PC30 EER40 G0.76
Bobbin: BEER40–1112CP
Gap: ≈0.030″ for a primary inductance of 212 µH

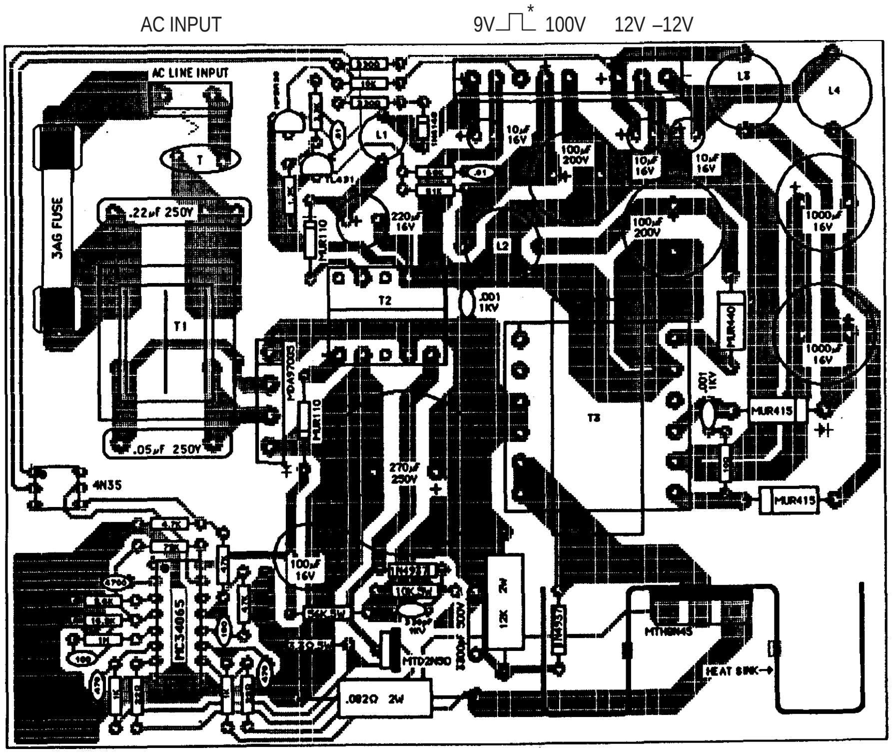
L1, L3, L4 – 25 µH at 1.0 A, Coilcraft Z7157.

L2 – 10 µH at 3.0 A, Coilcraft PCV–0–010–03.

Figure 29. PC Board Circuit Side and Component View



(CIRCUIT VIEW)



(COMPONENT VIEW)

*100 V and ±12 V Shutdown

MOTOROLA

MC34066
MC33066

High Performance Resonant Mode Controllers

The MC34066/MC33066 are high performance resonant mode controllers designed for off–line and dc–to–dc converter applications that utilize frequency modulated constant on–time or constant off–time control. These integrated circuits feature a variable frequency oscillator with programmable deadtime, precision retriggerable one–shot timer, temperature compensated reference, high gain wide–bandwidth error amplifier with a precision output clamp, steering flip–flop, and dual high current totem pole outputs ideally suited for driving power MOSFETs.

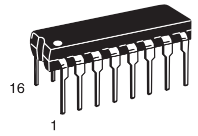
Also included are protective features consisting of a high speed fault comparator and latch, programmable soft–start circuitry, input undervoltage lockout with selectable thresholds, and reference undervoltage lockout.

These devices are available in dual–in–line and surface mount packages.

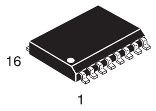
- Variable Frequency Oscillator with a Control Range Exceeding 1000:1
- Programmable Oscillator Deadtime Allows Constant Off–Time Operation
- Precision Retriggerable One–Shot Timer
- Internally Trimmed Bandgap Reference
- 5.0 MHz Error Amplifier with Precision Output Clamp
- Dual High Current Totem Pole Outputs
- Selectable Undervoltage Lockout Thresholds with Hysteresis
- Enable Input
- Programmable Soft–Start Circuitry
- Low Startup Current for Off–Line Operation

HIGH PERFORMANCE RESONANT MODE CONTROLLERS

SEMICONDUCTOR TECHNICAL DATA

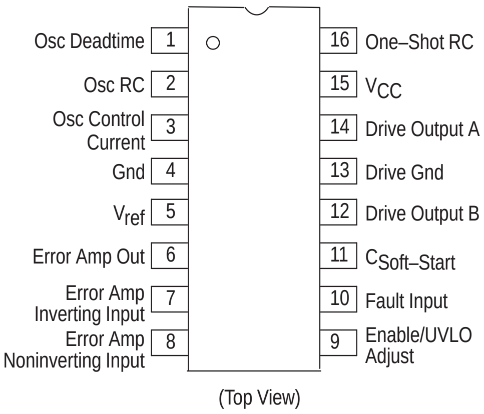


P SUFFIX
PLASTIC PACKAGE
CASE 648



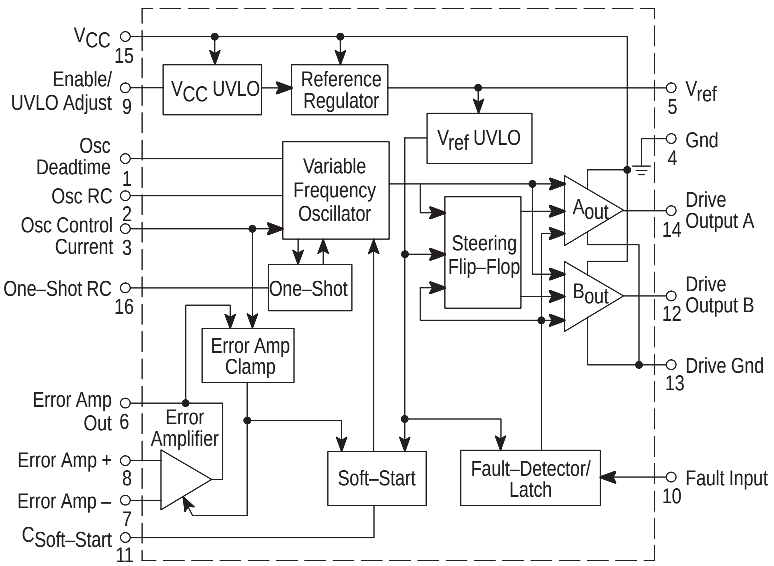
DW SUFFIX
PLASTIC PACKAGE
CASE 751G
(SO–16L)

PIN CONNECTIONS



(Top View)

Simplified Block Diagram



ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC34066DW	T_A = 0° to +70°C	SO–16L
MC34066P		Plastic DIP
MC33066DW	T_A = –40° to +85°C	SO–16L
MC33066P		Plastic DIP

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Input Supply Voltage	V_{CC}	20	V
Drive Output Current, Source or Sink (Note 1) Continuous Pulsed (0.5 µs, 25% Duty Cycle)	I_O	 0.3 1.5	A
Error Amplifier, Fault, One–Shot, Oscillator, and Soft–Start Inputs	V_{in}	–1.0 to +6.0	V
UVLO Adjust Input	$V_{in(UVLO)}$	–1.0 to V_{CC}	V
Soft–Start Discharge Current	I_{dchg}	20	mA
Power Dissipation and Thermal Characteristics DW Suffix Package, Case 751G Maximum Power Dissipation @ T_A = 25°C Thermal Resistance, Junction–to–Air P Suffix Package, Case 648 Maximum Power Dissipation @ T_A = 25°C Thermal Resistance, Junction–to–Air	 P_D $R_{\theta JA}$ P_D $R_{\theta JA}$	 862 145 1.25 100	 mW °C/W W °C/W
Operating Junction Temperature	T_J	+150	°C
Operating Ambient Temperature MC34066 MC33066	T_A	 0 to +70 –40 to +85	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 12 V [Note 2], R_{OSC} = 95.3 k, R_{DT} = 0 Ω, R_{VFO} = 5.62 k, C_{OSC} = 300 pF, R_T = 14.3 k, C_T = 300 pF, C_L = 1.0 nF, for typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies [Note 3], unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
REFERENCE SECTION					
Reference Output Voltage (I_O = 0 mA, T_A = 25°C)	V_{ref}	5.0	5.1	5.2	V
Line Regulation (V_{CC} = 10 V to 18 V)	Reg_{line}	–	1.0	20	mV
Load Regulation (I_O = 0 mA to 10 mA)	Reg_{load}	–	1.0	20	mV
Total Output Variation over Line, Load, and Temperature	V_{ref}	4.9	–	5.3	mV
Output Short Circuit Current	I_O	25	100	190	mA
Reference Undervoltage Lockout Threshold	V_{th}	3.8	4.3	4.8	V
ERROR AMPLIFIER					
Input Offset Voltage (V_{CM} = 1.5 V)	V_{IO}	–	1.0	10	mV
Input Bias Current (V_{CM} = 1.5 V)	I_{IB}	–	0.2	1.0	µA
Input Offset Current (V_{CM} = 1.5 V)	I_{IO}	–	0	0.5	µA
Open Loop Voltage Gain (V_{CM} = 1.5 V, V_O = 2.0 V)	A_{VOL}	70	100	–	dB
Gain Bandwidth Product (f = 100 kHz)	GBW	2.5	4.2	–	MHz
Input Common Mode Rejection Ratio (V_{CM} = 1.5 V to 5.0 V)	CMRR	70	95	–	dB
Power Supply Rejection Ratio (V_{CC} = 10 V to 18 V, f = 120 Hz)	PSRR	80	100	–	dB
Output Voltage Swing High State with Respect to Pin 3 (I_{Source} = 2.0 mA) Low State with Respect to Ground (I_{Sink} = 1.0 mA)	 V_{OH} V_{OL}	 2.3 –	 2.7 0.4	 3.1 0.6	V

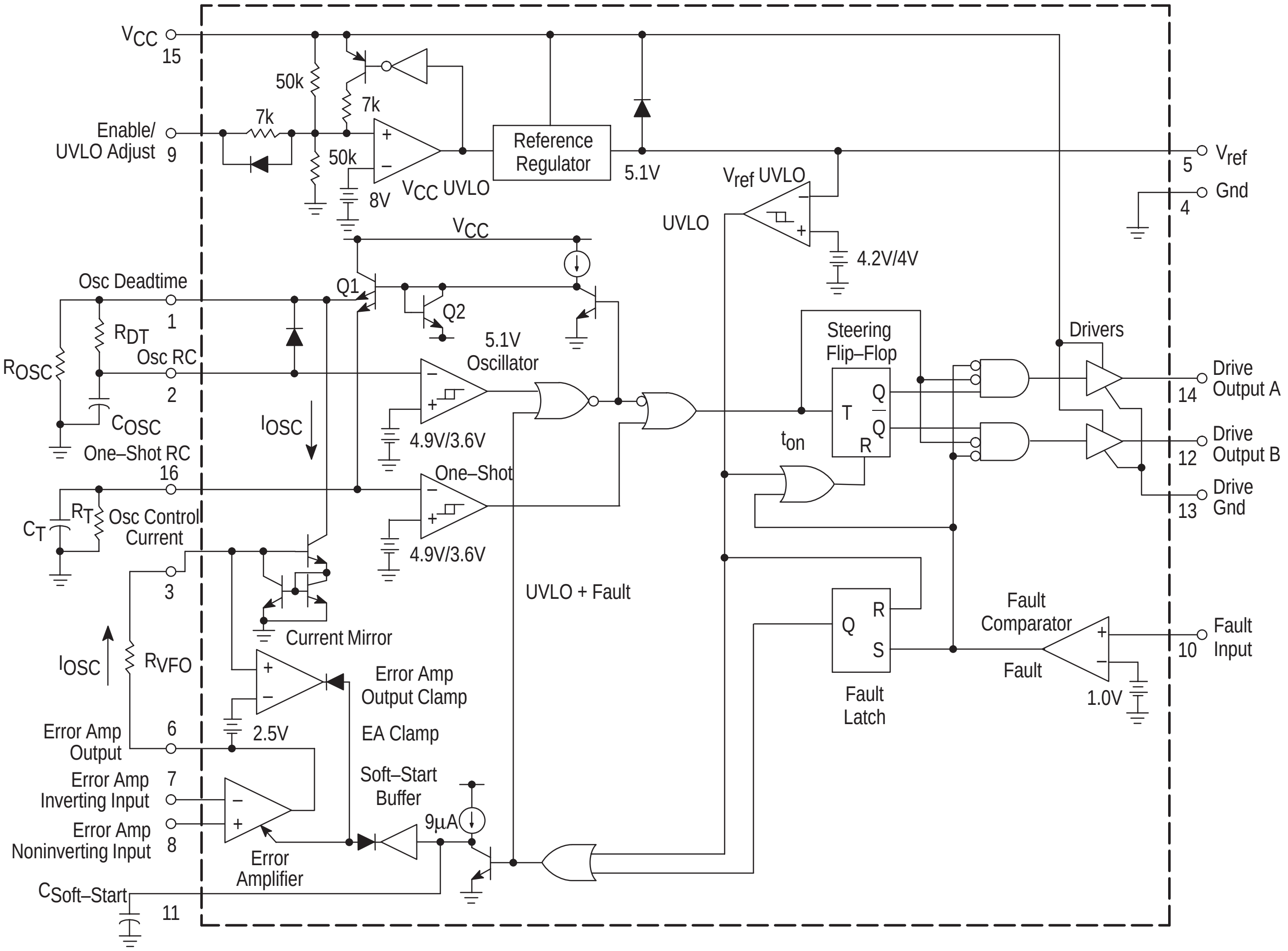
NOTES: 1. Maximum package power dissipation limits must be observed.
2. Adjust V_{CC} above the Startup threshold before setting to 12 V.
3. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
T_{low} = 0°C for MC34066 T_{high} = +70°C for MC34066
–40°C for MC33066 +85°C for MC33066

ELECTRICAL CHARACTERISTICS (continued) (V_{CC} = 12 V [Note 2], R_{OSC} = 95.3 k, R_{DT} = 0 Ω, R_{VFO} = 5.62 k, C_{OSC} = 300 pF, R_T = 14.3 k, C_T = 300 pF, C_L = 1.0 nF, for typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies [Note 3], unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
OSCILLATOR					
Frequency (Error Amp Output Low)	$f_{OSC(low)}$				kHz
T_A = 25°C		90	100	110	
Total Variation (V_{CC} = 10 V to 18 V, T_A = T_{Low} to T_{High})		85	–	115	
Frequency (Error Amp Output High)	$f_{OSC(high)}$				kHz
T_A = 25°C		900	1000	1100	
Total Variation (V_{CC} = 10 V to 18 V, T_A = T_{Low} to T_{High})		850	–	1150	
Oscillator Control Input Voltage, Pin 3 (I_{Sink} = 0.5 mA, T_A = 25°C)	V_{in}	1.3	1.4	1.5	V
Output Deadtime (Error Amp Output High)	DT				ns
R_{DT} = 0 Ω		–	70	100	
R_{DT} = 1.0 k		600	700	800	
ONE–SHOT					
Drive Output On–Time (R_{DT} = 1.0 k)	t_{OS}				µs
T_A = 25°C		1.43	1.5	1.57	
Total Variation (V_{CC} = 10 V to 18 V, T_A = T_{Low} to T_{High})		1.4	–	1.6	
DRIVE OUTPUTS					
Output Voltage					V
Low State (I_{Sink} = 20 mA)	V_{OL}	–	0.8	1.2	
(I_{Sink} = 200 mA)		–	1.5	2.0	
High State (I_{Source} = 20 mA)	V_{OH}	9.5	10.3	–	
(I_{Source} = 200 mA)		9.0	9.8	–	
Output Voltage with UVLO Activated (V_{CC} = 6.0 V, I_{Sink} = 1.0 mA)	$V_{OL(UVLO)}$	–	0.8	1.2	V
Output Voltage Rise Time (C_L = 1.0 nF)	t_r	–	20	50	ns
Output Voltage Fall Time (C_L = 1.0 nF)	t_f	–	20	50	ns
FAULT COMPARATOR					
Input Threshold	V_{th}	0.95	1.0	1.05	V
Input Bias Current ($V_{Pin\ 10}$ = 0 V)	I_{IB}	–	–2.0	–10	µA
Propagation Delay to Drive Outputs (100 mV Overdrive)	$t_{PLH(In/Out)}$	–	60	100	ns
SOFT–START					
Capacitor Charge Current ($V_{Pin\ 11}$ = 2.5 V)	I_{chg}	4.5	8.1	14	µA
Capacitor Discharge Current ($V_{Pin\ 11}$ = 2.5 V)	I_{dchg}	1.0	8.0	–	mA
UNDERVOLTAGE LOCKOUT					
Startup Threshold, V_{CC} Increasing	$V_{th(UVLO)}$				V
Enable/UVLO Adjust Pin Open		14.8	16	17.2	
Enable/UVLO Adjust Pin Connected to V_{CC}		8.0	9.0	10	
Minimum Operating Voltage after Turn–On	$V_{CC(min)}$				V
Enable/UVLO Adjust Pin Open		8.0	9.0	10	
Enable/UVLO Adjust Pin Connected to V_{CC}		7.6	8.6	9.6	
Enable/UVLO Adjust Shutdown Threshold Voltage	$V_{th(Enable)}$	6.0	7.0	–	V
Enable/UVLO Adjust Input Current (Pin 9 = 0V)	$I_{in(Enable)}$	–	–0.2	–1.0	mA
TOTAL DEVICE					
Power Supply Current (Enable/UVLO Adjust Pin Open)	I_{CC}				mA
Startup (V_{CC} = 13.5 V)		–	0.45	0.6	
Operating (f_{OSC} = 100 kHz) (Note 2)		–	21	30	

NOTES: 2. Adjust V_{CC} above the Startup threshold before setting to 12 V.
3. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
T_{low} = 0°C for MC34066 T_{high} = +70°C for MC34066
–40°C for MC33066 +85°C for MC33066

Figure 1. MC34066 Representative Block Diagram



OPERATING DESCRIPTION

Introduction

As power supply designers have strived to increase power conversion efficiency and reduce passive component size, high frequency resonant mode power converters have emerged as attractive alternatives to conventional square–wave control. When compared to square–wave converters, resonant mode control offers several benefits including lower switching losses, higher efficiency, lower EMI emission, and smaller size. This integrated circuit has been developed to support new trends in power supply design. The MC34066 Resonant Mode Controller is a high performance bipolar IC dedicated to variable frequency power control at frequencies exceeding 1.0 MHz. This integrated circuit provides the features, performance and flexibility for a wide variety of resonant mode power supply applications.

The primary purpose of the control chip is to supply precise pulses to the gates of external power MOSFETs at a repetition rate regulated by a feedback control loop. The MC34066 can be operated in any of three modes as follows: 1) fixed on–time, variable frequency; 2) fixed off–time, variable frequency; and 3) combinations of 1 and 2 that change from fixed on–time to fixed off–time as the frequency increases. Additional features of the IC ensure that system startup and fault conditions are administered in a safe, controlled manner.

A simplified block diagram of the IC is shown on the first page of this data sheet, which identifies the main functional blocks and the block–to–block interconnects. Figure 1 is a detailed functional diagram which accurately represents the internal circuitry. The various functions can be divided into two sections. The first section includes the primary control path which produces precise output pulses at the desired frequency Oscillator, a One–Shot, a pulse Steering Flip–Flop, a pair of power MOSFET Drivers, and a wide bandwidth Error Amplifier. The second section provides several peripheral support functions including a voltage reference, undervoltage lockout, Soft–Start circuit, and a fault detector.

Primary Control Path

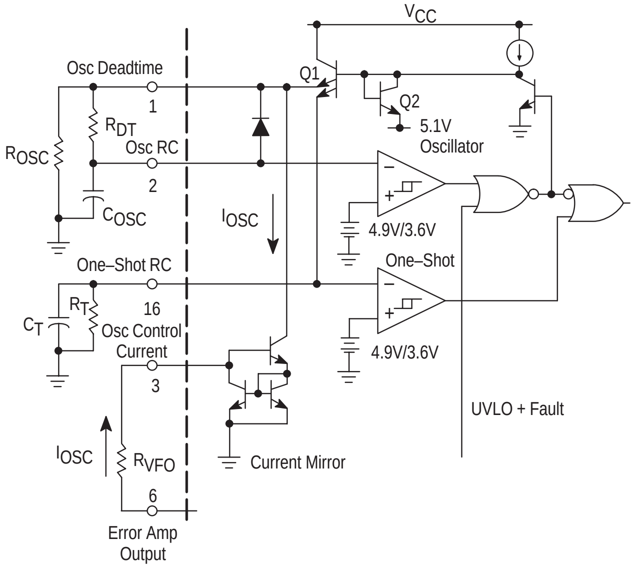
The output pulse width and repetition rate are regulated through the interaction of the variable frequency Oscillator, One–Shot timer and Error Amplifier. The Oscillator triggers the One–Shot which generates a pulse that is alternately steered to a pair of totem–pole output drivers by a toggle Flip–Flop. The Error Amplifier monitors the output of the regulator and modulates the frequency of the Oscillator. High–speed Schottky logic is used throughout the primary control channel to minimize delays and enhance high frequency characteristics.

Oscillator

The characteristics of the variable frequency Oscillator are crucial for precise controller performance at high operating frequencies. In addition to triggering the One–Shot timer and initiating the output pulse, the Oscillator also determines the initial voltage for the One–Shot capacitor and defines the minimum deadtime between output pulses. The Oscillator is designed to operate at frequencies exceeding 1.0 MHz. The Error Amplifier can control the oscillator frequency over a 1000:1 frequency range, and both the minimum and maximum frequencies are easily and accurately programmed by the proper selection of external components. The Oscillator also includes an adjustable deadtime feature for applications requiring additional time between output pulses.

The functional diagram of the Oscillator and One–Shot timer is shown in Figure 2. The oscillator capacitor C_{OSC} is initially charged by transistor Q1 through the optional deadtime resistor R_{DT}. When C_{OSC} exceeds the 4.9 V upper threshold of the oscillator comparator, the base of Q1 is pulled low allowing C_{OSC} to discharge through the external resistors and the internal Current Mirror. When the voltage on C_{OSC} falls below the comparator's 3.6 V lower threshold, Q1 turns on and again charges C_{OSC}.

Figure 2. Oscillator and One–Shot Timer



If R_{DT} is 0 Ω, C_{OSC} charges from 3.6 V to 5.1 V in less than 50 ns. The high slew rate of C_{OSC} and the propagation delay of the comparator make it difficult to control the peak voltage. This accuracy issue is overcome by clamping the base of Q1 through diode Q2 to a voltage reference. The peak voltage of the oscillator waveform is thereby precisely set at 5.1 V.

The frequency of the Oscillator is modulated by varying the current I_{OSC} flowing through R_{VFO} into the Osc Control Current pin. The control current drives a unity gain Current Mirror which pulls an identical current from the C_{OSC} capacitor. As I_{OSC} increases, C_{OSC} discharges faster thus decreasing the Oscillator period and increasing the frequency. The maximum frequency occurs when the Error Amplifier output is at the upper clamp level, nominally 2.5 V above the voltage at the Osc Control Current pin. The minimum discharge time for C_{OSC}, which corresponds to the maximum oscillator frequency, is given by Equation 1.

$$t_{dchg(min)} = (R_{DT} + R_{OSC})C_{OSC}\ln\left[\frac{\frac{2.5\mathrm{ROSC}}{\mathrm{RVFO}} + 5.1}{\frac{2.5\mathrm{ROSC}}{\mathrm{RVFO}} + 3.6}\right] \quad (1)$$

The minimum oscillator frequency will result when the I_{OSC} current is zero, and C_{OSC} is discharged through the external resistors R_{OSC} and R_{DT}. This occurs when the Error Amplifier output voltage is less than the two diode drops required to bias the input of the Current Mirror. The maximum oscillator discharge time is given by Equation 2.

$$t_{dchg(max)} = (R_{DT} + R_{OSC})\ C_{OSC}\ln\left(\frac{5.1}{3.6}\right) \quad (2)$$

The outputs of the control IC are off whenever the oscillator capacitor C_{OSC} is being charged by transistor Q1. The minimum time between output pulses (deadtime) can be programmed by controlling the charge time of C_{OSC}. Resistor R_{DT} reduces the current delivered by Q1 to C_{OSC}, thus increasing the charge time and output deadtime. Varying R_{DT} from 0 Ω to 1000 Ω will increase the output deadtime from 80 ns to 680 ns with C_{OSC} equal to 300 pF. The general expression for the oscillator charge time is give by Equation 3.

$$t_{chg(max)} = R_{DT}\ C_{OSC}\ \ln\left(\frac{5.1–3.6}{5.1–4.9}\right) + 80\ \mathrm{ns} \quad (3)$$

The minimum and maximum oscillator frequencies are programmed by the proper selection of resistor R_{OSC} and R_{VFO}. After selecting R_{DT} for the desired deadtime, the minimum frequency is programmed by R_{OSC} using Equations 2 and 3 in Equation 4:

$$\frac{1}{f_{OSC(min)}} = t_{dchg(max)} + t_{chg} \quad (4)$$

The maximum oscillator frequency is set by resistor R_{VFO} in a similar fashion using Equations 1 and 3 in Equation 5:

$$\frac{1}{f_{OSC(max)}} = t_{dchg(min)} + t_{chg} \quad (5)$$

The value chosen for resistor R_{DT} will affect the peak voltage of the oscillator waveform. As R_{DT} is increased from zero, the time required to charge C_{OSC} becomes large with respect to the propagation delay through the oscillator comparator. Consequently, the overshoot of the upper threshold is reduced and the peak voltage on the oscillator waveform drops from 5.1 V to 4.9 V. The best frequency accuracy is achieved when R_{DT} is zero ohms.

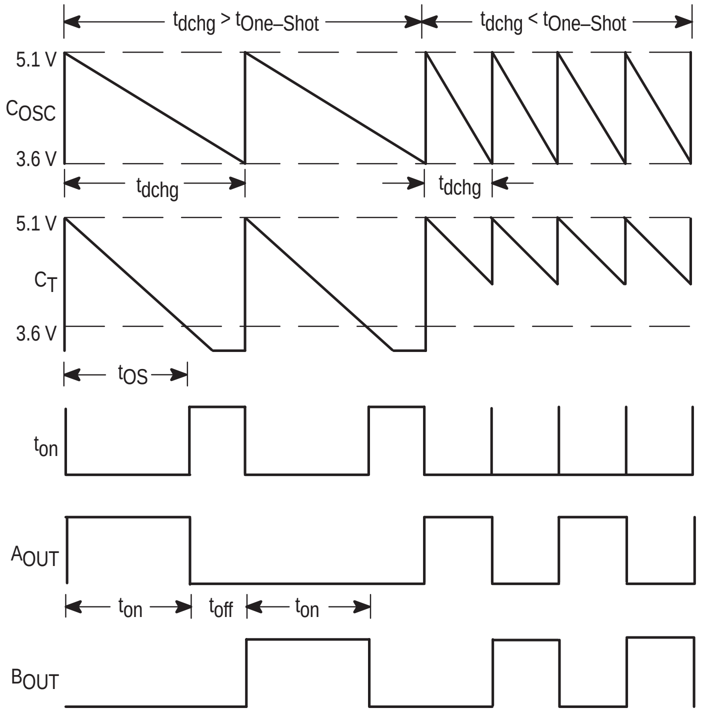
One–Shot Timer

The One–Shot capacitor C_T is charged concurrently with the oscillator capacitor by transistor Q1, as shown in Figure 2. The One–Shot period begins when the oscillator comparator turns off Q1, allowing C_T to discharge. The period ends when resistor R_T discharges C_T to the threshold of the One–Shot comparator. Discharging C_T from an initial voltage of 5.1 V to a threshold voltage of 3.6 V results in the One–Shot period given by Equation 6.

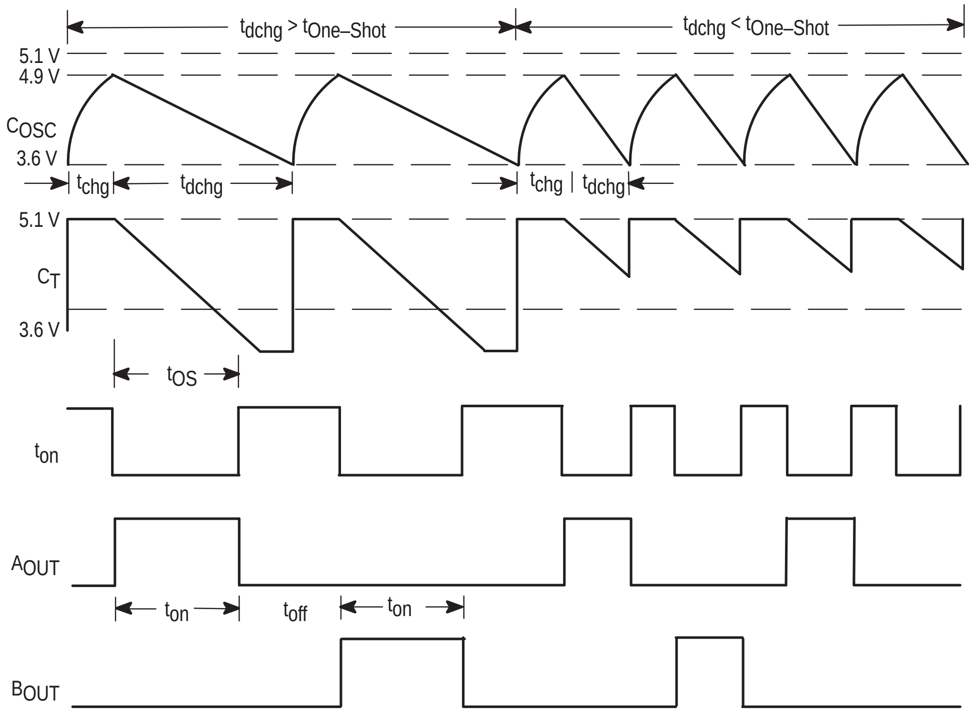
$$t_{OS} = R_T\ C_T\ \ln\left(\frac{5.1}{3.6}\right) = 0.348\ R_T\ C_T \quad (6)$$

Figure 3. Timing Waveforms

$R_{DT} = 0$



$R_{DT} = 1.0\ k$



Errors in the threshold voltage and propagation delays through the output drivers will affect the One–Shot period. To guarantee accuracy, the output pulse of the control ship is trimmed to within 5% of 1.5 µs with nominal values of R_T and C_T.

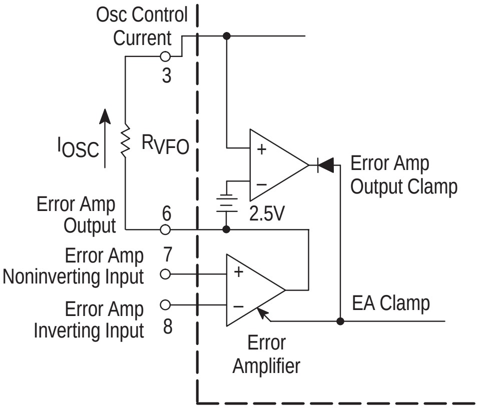
The outputs of the Oscillator and One–Shot comparators are OR'd together to produce the pulse t_{on}, which drives the Flip–Flop and output drivers. The output pulse t_{on} is initiated by the Oscillator, but either the oscillator comparator or the One–Shot comparator can terminate the pulse. When the oscillator discharge time exceeds the one–shot period, the complete one–shot period is delivered to the output section. If the oscillator discharge time is less than the one–shot period, then the oscillator comparator terminates the pulse prematurely and retriggers the One–Shot. The waveforms on the left side of Figure 3 correspond to nonretriggered operation with constant on–time and variable off–times. The right side of Figure 3 represents retriggered operation with variable on–time and constant off–time.

Error Amplifier

A fully accessible high performance Error Amplifier is provided for feedback control of the power supply system. The Error Amplifier is internally compensated and features dc open loop gain greater than 70 dB, input offset voltage less than 10 mV and guaranteed minimum gain–bandwidth product of 2.5 MHz. The input common mode range extends from 1.5 V to 5.1 V, which includes the reference voltage. For common mode voltages below 1.5 V, the Error Amplifier output is forced low providing minimum oscillator frequency.

The Oscillator Control Current pin is biased by the Error Amplifier output voltage through R_{VFO} as illustrated in Figure 4. The output swing of the Error Amplifier is restricted by a clamp circuit to limit the maximum oscillator frequency. The clamp circuit limits the voltage across R_{VFO} to 2.5 V, thus limiting I_{OSC} to 2.5 V/R_{VFO}. Oscillator accuracy is improved by trimming the clamp voltage to obtain the $f_{OSC(high)}$ specification of 1.0 MHz with nominal value external components.

Figure 4. Error Amplifier and Clamp

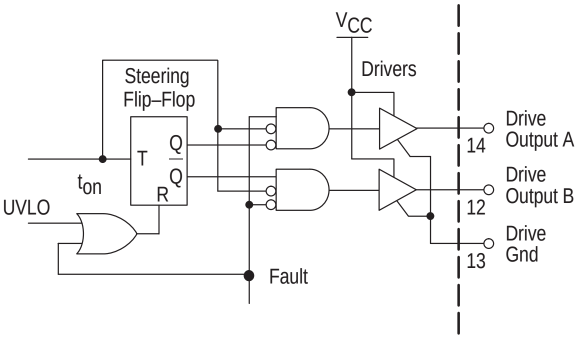


Output Section

The pulse, t_{on}, generated by the Oscillator and One–Shot timer is gated to dual totem pole output drives by the Steering Flip–Flop shown in Figure 5. Positive transitions of t_{on} toggle the Flip–Flop, which causes the pulses to alternate between Output A and Output B. The flip–flop is reset by the undervoltage lockout circuit during startup to guarantee that the first pulse appears at Output A.

The totem–pole output drives are ideally suited for driving power MOSFETs and are capable of sourcing and sinking 1.5 A. Rise and fall times are typically 20 ns when driving a 1.0 nF load. High source/sink capability in a totem–pole driver normally increases the risk of high cross conduction current during output transitions. The MC34066 utilizes a unique design that virtually eliminates cross conduction, thus controlling the chip power dissipation at high frequencies. A separate ground terminal is provided for the output drivers to isolate the sensitive analog circuitry from large transient currents.

Figure 5. Steering Flip–Flop and Output Drivers



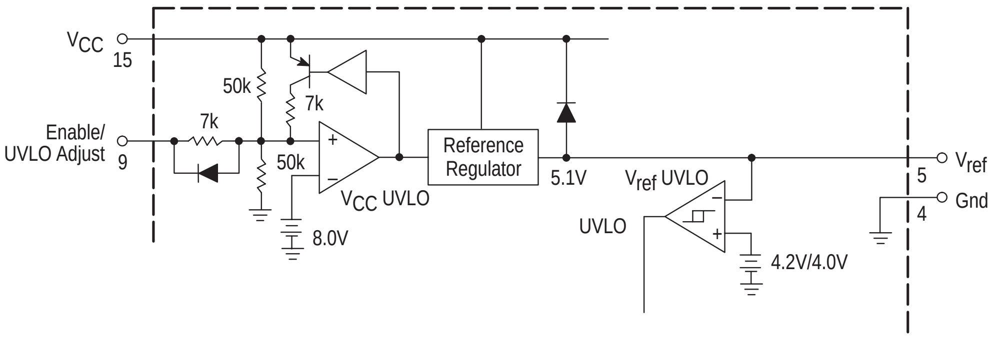
PERIPHERAL SUPPORT FUNCTIONS

The MC34066 Resonant Controller provides a number of support and protection functions including a precision voltage reference, undervoltage lockout comparators, soft–start circuitry, and a fault detector. These peripheral circuits ensure that the power supply can be turned on and off in a safe, controlled manner and that the system will be quickly disabled when a fault condition occurs.

Undervoltage Lockout and Voltage Reference

Separate undervoltage lockout comparators sense the input V_{CC} voltage and the regulated reference voltage as illustrated in Figure 6. When V_{CC} increases to the upper threshold voltage, the V_{CC} UVLO comparator enables the Reference Regulator. After the V_{ref} output of the Reference Regulator rises to 4.2 V, the V_{ref} UVLO comparator switches the UVLO signal to a logic zero state enabling the primary control path. Reducing V_{CC} to the lower threshold voltage causes the V_{CC} UVLO comparator to disable the Reference Regulator. The V_{ref} UVLO comparator then switches the UVLO output to a logic one state disabling the controller.

Figure 6. Undervoltage Lockout and Reference



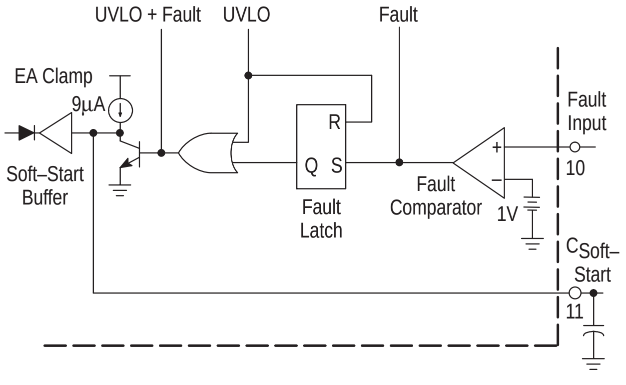
The Enable/UVLO Adjust terminal allows the power supply designer to select the V_{CC} UVLO threshold voltages. When this pin is open, the comparator switches the controller on at 16 V and off at 9.0 V. If this pin is connected to the V_{CC} terminal, the upper and lower thresholds are reduced to 9.0 V and 8.6 V, respectively. Forcing the Enable/UVLO Adjust pin low will pull the V_{CC} UVLO comparator input low (through an internal diode) turning off the controller.

The Reference Regulator provides a precise 5.1 V reference to internal circuitry and can deliver up to 10 mA to external loads. The reference is trimmed to better than 2% initial accuracy and includes active short circuit protection.

Fault Detector

The high–speed Fault Comparator and Latch illustrated in Figure 7 can protect a power supply from destruction under fault conditions. The Fault Input pin connects to the input of the Fault Comparator. If this input exceeds the 1.0 V threshold of the comparator, the Fault Latch is set and two logic signals simultaneously disable the primary control path. The signal labeled Fault at the output of the Fault Comparator is connected directly to the output drivers. This direct path reduces the propagation delay from the Fault Input to the A and B outputs to typically 70 ns. The Fault Latch output is OR'd with UVLO output from the V_{ref} UVLO comparator to produce the logic output labeled UVLO + Fault. This signal disables the Oscillator and One–Shot by forcing both the C_{OSC} and C_T capacitors to be continually charged.

Figure 7. Fault Detector and Soft–Start



The Fault Latch is reset during startup by a logic one at the UVLO output of the V_{ref} UVLO comparator. The latch can also be reset after startup by pulling the Enable/UVLO Adjust pin momentarily low to disable the Reference Regulator.

Soft–Start Circuit

The Soft–Start circuit shown in Figure 7 forces the variable frequency Oscillator to start at the minimum frequency and ramp upward until regulated by the feedback control loop. The external capacitor at the $C_{Soft–Start}$ terminal is initially discharged by the UVLO + Fault signal. The low voltage on the capacitor pass through the Soft–Start Buffer to hold the Error Amplifier output low. After UVLO + Fault switches to a logic zero, the soft–start capacitor is charged by a 9.0 µA current source. The buffer allows the Error Amplifier output to follow the soft–start capacitor until it is regulated by the Error Amplifier inputs (or reaches the 2.5 V clamp). The soft–start function is generally applicable to controllers operating below resonance and can be disabled by simply opening the $C_{Soft–Start}$ terminal.

APPLICATIONS

The MC34066 can be used for the control of series, parallel or higher order half/full bridge resonant converters. The IC is designed to provide control in discontinuous conduction mode (DCM) or continuous conduction mode (CCM) or a combination of the two. For example, in a parallel resonant converter (PRC) operating in the DCM, the IC is programmed to operate in fixed on–time, variable frequency mode of operation. For a PRC operating in the CCM, the IC can be programmed to operate in the variable frequency mode with a fixed off–time.

When operating with a wide input voltage range, such as a universal input power supply, a PRC can operate in the DCM for high input voltage and in the CCM for low input voltage. In this particular case, on–time is programmed corresponding to DCM. The deadtime of the chip is programmed to provide the desired off–time in the CCM. The frequency range is chosen to cover the complete frequency range from the DCM to the CCM. When programmed as such, the controller will operate in the fixed on–time, variable frequency mode at low frequencies. At the frequency which causes the Oscillator to retrigger the One–Shot, the control law changes to variable frequency with fixed off–time. At higher frequencies the supply will operate in the CCM with this control law.

Although the IC is designed and optimized for double ended push–pull type converters, it can also be used for single ended applications, such as forward and flyback resonant converters.

MOTOROLA

MC34067
MC33067

High Performance Resonant Mode Controllers

HIGH PERFORMANCE ZERO VOLTAGE SWITCH RESONANT MODE CONTROLLERS

SEMICONDUCTOR TECHNICAL DATA

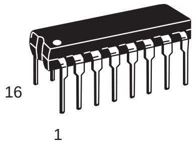
The MC34067/MC33067 are high performance zero voltage switch resonant mode controllers designed for off–line and dc–to–dc converter applications that utilize frequency modulated constant off–time or constant deadtime control. These integrated circuits feature a variable frequency oscillator, a precise retriggerable one–shot timer, temperature compensated reference, high gain wide bandwidth error amplifier, steering flip–flop, and dual high current totem pole outputs ideally suited for driving power MOSFETs.

Also included are protective features consisting of a high speed fault comparator and latch, programmable soft–start circuitry, input undervoltage lockout with selectable thresholds, and reference undervoltage lockout.

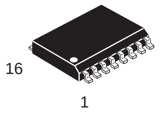
These devices are available in dual–in–line and surface mount packages.

- Zero Voltage Switch Resonant Mode Operation
- Variable Frequency Oscillator with a Control Range Exceeding 1000:1
- Precision One–Shot Timer for Controlled Off–Time
- Internally Trimmed Bandgap Reference
- 4.0 MHz Error Amplifier
- Dual High Current Totem Pole Outputs
- Selectable Undervoltage Lockout Thresholds with Hysteresis
- Enable Input
- Programmable Soft–Start Circuitry
- Low Startup Current for Off–Line Operation

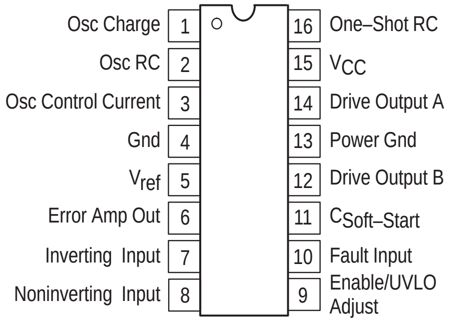
P SUFFIX
PLASTIC PACKAGE
CASE 648



DW SUFFIX
PLASTIC PACKAGE
CASE 751G
(SO–16L)

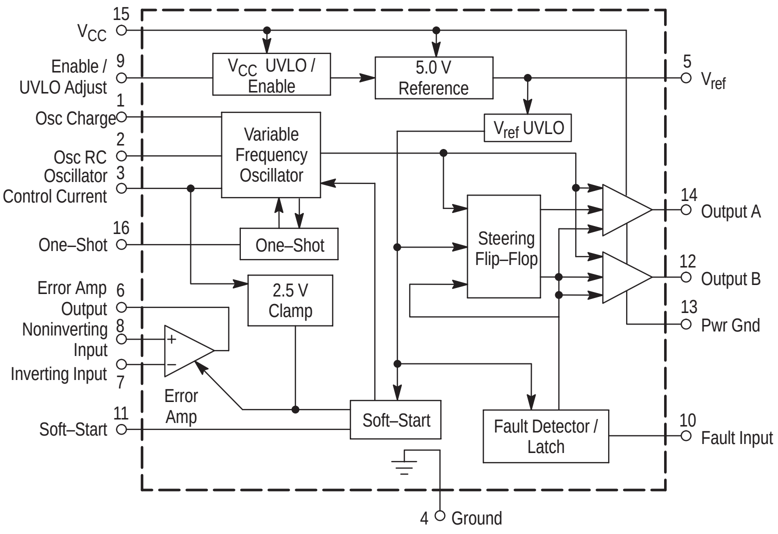


PIN CONNECTIONS



(Top View)

Simplified Block Diagram



ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC34067DW	T_A = 0 to + 70°C	SO–16L
MC34067P		Plastic DIP
MC33067DW	T_A = – 40° to + 85°C	SO–16L
MC33067P		Plastic DIP

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	20	V
Drive Output Current, Source or Sink (Note 1)			A
Continuous	I_O	0.3	
Pulsed (0.5 µs, 25% Duty Cycle		1.5	
Error Amplifier, Fault, One–Shot, Oscillator and Soft–Start Inputs	V_{in}	– 1.0 to + 6.0	V
UVLO Adjust Input	$V_{in(UVLO)}$	– 1.0 to V_{CC}	V
Power Dissipation and Thermal Characteristics			
DW Suffix, Plastic Package, Case 751G			
T_A = 25°C	P_D	862	mW
Thermal Resistance, Junction–to–Air	$R_{\theta JA}$	145	°C/W
P Suffix, Plastic Package, Case 648			
T_A = 25°C	P_D	1.25	W
Thermal Resistance, Junction–to–Air	$R_{\theta JA}$	100	°C/W
Operating Junction Temperature	T_J	+ 150	°C
Operating Ambient Temperature	T_A		°C
MC34067		0 to + 70	
MC33067		– 40 to + 85	
Storage Temperature	T_{stg}	– 55 to + 150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 12 V [Note 2], R_{OSC}= 18.2 k, R_{VFO} = 2940, C_{OSC} = 300 pF, R_T = 2370 k, C_T = 300 pF, C_L = 1.0 nF. For typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies [Note 3], unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
REFERENCE SECTION					
Reference Output Voltage (I_O = 0 mA, T_J = 25°C)	V_{ref}	5.0	5.1	5.2	V
Line Regulation (V_{CC} = 10 TO 18 V)	Reg_{line}	–	1.0	20	mV
Load Regulation (I_O = 0 mA to 10 mA)	Reg_{load}	–	1.0	20	mV
Total Output Variation Over Line, Load, and Temperature	V_{ref}	4.9	–	5.3	V
Output Short Circuit Current	I_O	25	100	190	mA
Reference Undervoltage Lockout Threshold	V_{th}	3.8	4.3	4.8	V
ERROR AMPLIFIER					
Input Offset Voltage (V_{CM} = 1.5 V)	V_{IO}	–	1.0	10	mV
Input Bias Current (V_{CM} = 1.5 V)	I_{IB}	–	0.2	1.0	µA
Input Offset Current (V_{CM} = 1.5 V)	I_{IO}	–	0	0.5	µA
Open Loop Voltage Gain (V_{CM} = 1.5 V, V_O = 2.0 V)	A_{VOL}	70	100	–	dB
Gain Bandwidth Product (f = 100 kHz)	GBW	3.0	5.0	–	MHz
Input Common Mode Rejection Ratio (V_{CM} = 1.5 to 5.0 V)	CMR	70	95	–	dB
Power Supply Rejection Ratio (V_{CC} = 10 to 18 V, f = 120 Hz)	PSR	80	100	–	dB
Output Voltage Swing					V
High State	V_{OH}	2.8	3.2	–	
Low State	V_{OL}	–	0.6	0.8	

NOTES: 1. Maximum package power dissipation limits must be observed.
2. Adjust V_{CC} above the Startup threshold before setting to 12 V.
3. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
T_{low} = 0°C for the MC34067 T_{high} = + 70°C for MC34067
= – 40°C for the MC33067 = + 85°C for MC33067

ELECTRICAL CHARACTERISTICS (V_{CC} = 12 V [Note 2], R_{OSC}= 18.2 k, R_{VFO} = 2940, C_{OSC} = 300 pF, R_T = 2370 k, C_T = 300 pF, C_L = 1.0 nF. For typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies [Note 3], unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OSCILLATOR					
Frequency (Error Amp Output Low)					kHz
T_A = 25°C	$f_{OSC(low)}$	500	525	540	
Total Variation (V_{CC} = 10 to 18 V, T_A = T_{Low} to T_{High}		490	–	550	
Frequency (Error Amp Output High)					kHz
T_A = 25°C	$f_{OSC(high)}$	1900	2050	2150	
Total Variation (V_{CC} = 10 to 18 V, T_A = T_{Low} to T_{High}		1850	–	2200	
Oscillator Control Input Voltage, Pin 3 @ 25°C	V_{in}	–	2.5	–	V
ONE–SHOT					
Drive Output Off–Time					ns
T_A = 25°C	t_{Blank}	235	250	270	
Total Variation (V_{CC} = 10 to 18 V, T_A = T_{Low} to T_{High}		225	–	280	
DRIVE OUTPUTS					
Output Voltage					V
Low State (I_{Sink} = 20 mA)	V_{OL}	–	0.8	1.2	
(I_{Sink} = 200 mA)		–	1.5	2.0	
High State (I_{Source} = 20 mA)	V_{OH}	9.5	10.3	–	
(I_{Source} = 200 mA)		9.0	9.7	–	
Output Voltage with UVLO Activated (V_{CC} = 6.0 V, I_{Sink} = 1.0 mA)	$V_{OL(UVLO)}$	–	0.8	1.2	V
Output Voltage Rise Time (C_L = 1.0 nF)	t_r	–	20	50	ns
Output Voltage Fall Time (C_L = 1.0 nF)	t_f	–	15	50	ns
FAULT COMPARATOR					
Input Threshold	V_{th}	0.93	1.0	1.07	V
Input Bias Current ($V_{Pin\ 10}$ = 0 V)	I_{IB}	–	– 2.0	– 10	µA
Propagation Delay to Drive Outputs (100 mV Overdrive)	$t_{PLH(In/Out)}$	–	60	100	ns
SOFT–START					
Capacitor Charge Current ($V_{Pin\ 11}$ = 2.5 V)	I_{chg}	4.5	9.0	14	µA
Capacitor Discharge Current ($V_{Pin\ 11}$ = 2.5 V)	I_{dischg}	3.0	8.0	–	mA
UNDERVOLTAGE LOCKOUT					
Startup Threshold, V_{CC} Increasing					V
Enable/UVLO Adjust Pin Open	$V_{th(UVLO)}$	14.8	16	17.2	
Enable/UVLO Adjust Pin Connected to V_{CC}		8.0	9.0	10	
Minimum Operating Voltage After Turn–On					V
Enable/UVLO Adjust Pin Open	$V_{CC(min)}$	8.0	9.0	10	
Enable/UVLO Adjust Pin Connected to V_{CC}		7.6	8.6	9.6	
Enable/UVLO Adjust Shutdown Threshold Voltage	$V_{th(Enable)}$	6.0	7.0	–	V
Enable/UVLO Adjust Input Current (Pin 9 = 0 V)	$I_{in(Enable)}$	–	– 0.2	– 1.0	mA
TOTAL DEVICE					
Power Supply Current (Enable/UVLO Adjust Pin Open)					mA
Startup (V_{CC} = 13.5 V)	I_{CC}	–	0.5	0.8	
Operating (f_{OSC} = 500 kHz) (Note 2)		–	27	35	

NOTES: 1. Maximum package power dissipation limits must be observed.
2. Adjust V_{CC} above the Startup threshold before setting to 12 V.
3. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
T_{low} = 0°C for the MC34067 T_{high} = + 70°C for MC34067
= – 40°C for the MC33067 = + 85°C for MC33067

Figure 1. Oscillator Timing Resistor versus Discharge Time

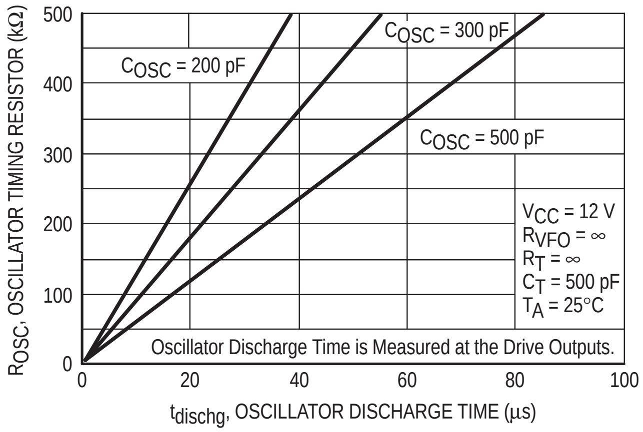


Figure 2. Oscillator Frequency versus Oscillator Control Current

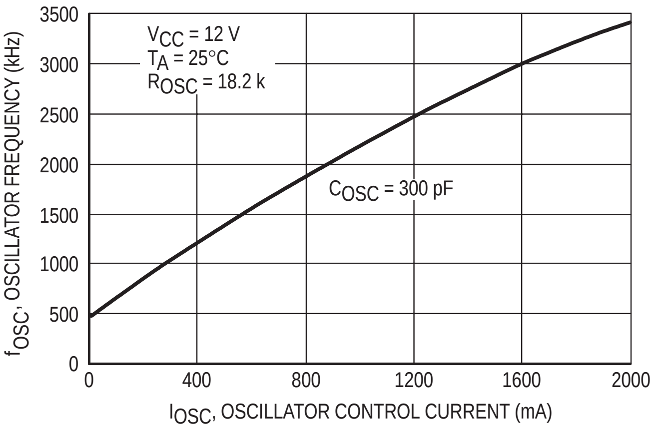


Figure 3. Error Amp Output Saturation Voltage versus Oscillator Control Current

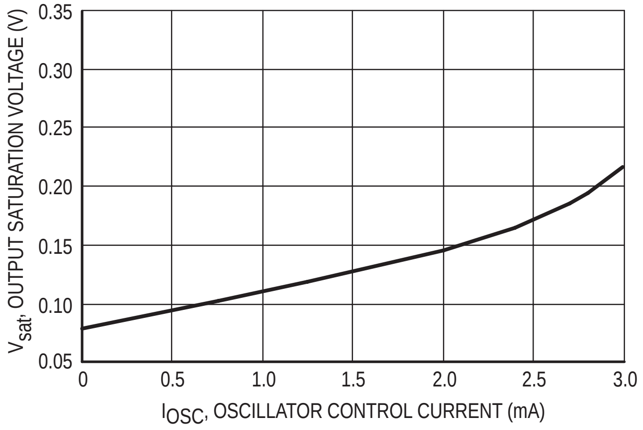


Figure 4. One–Shot Timing Resistor versus Period

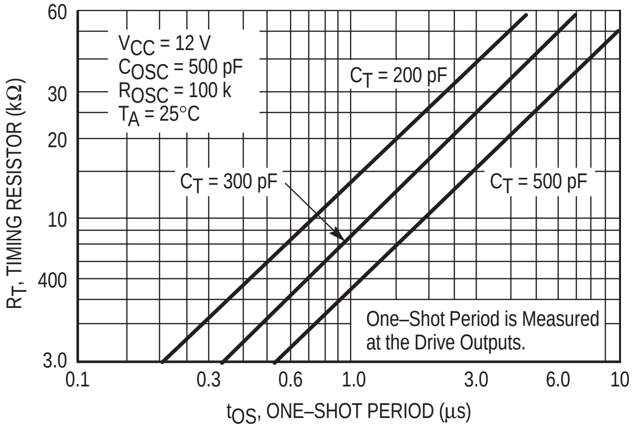


Figure 5. Open Loop Voltage Gain and Phase versus Frequency

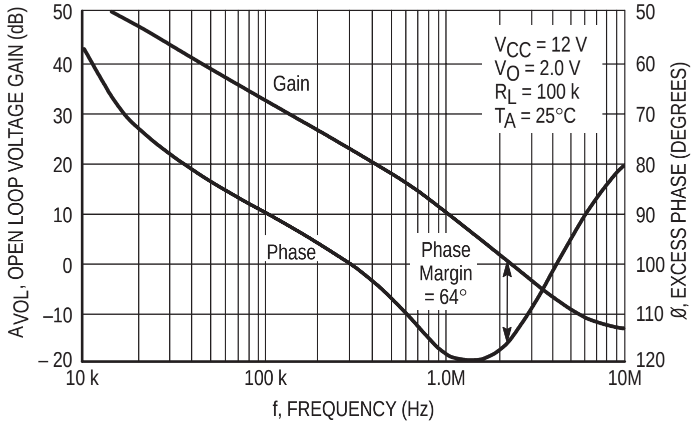


Figure 6. Reference Output Voltage Change versus Temperature

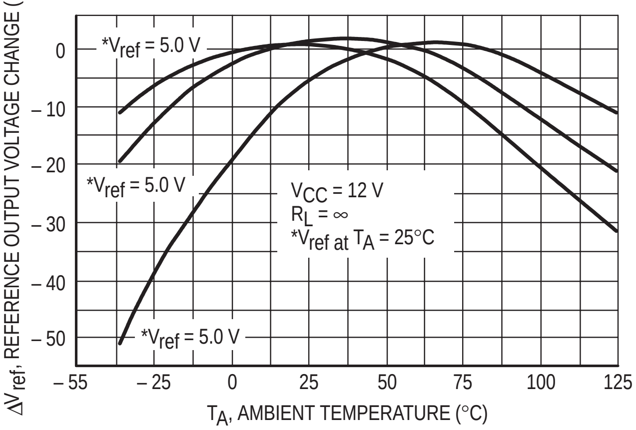


Figure 7. Reference Voltage Change versus Source Current

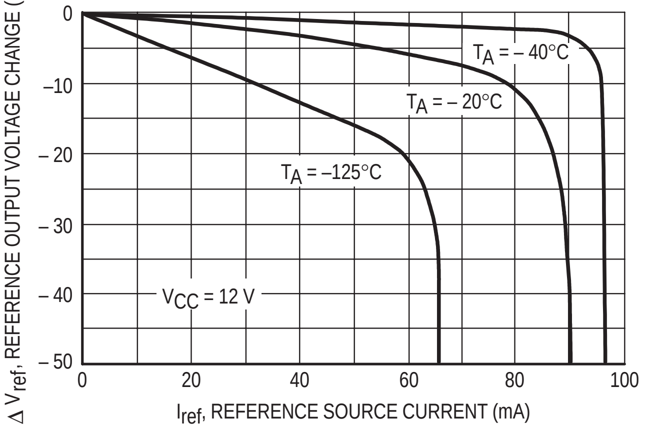


Figure 8. Drive Output Saturation Voltage versus Load Current

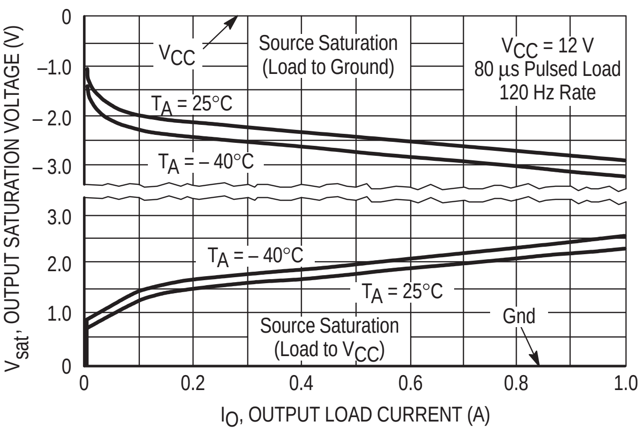


Figure 9. Drive Output Waveform

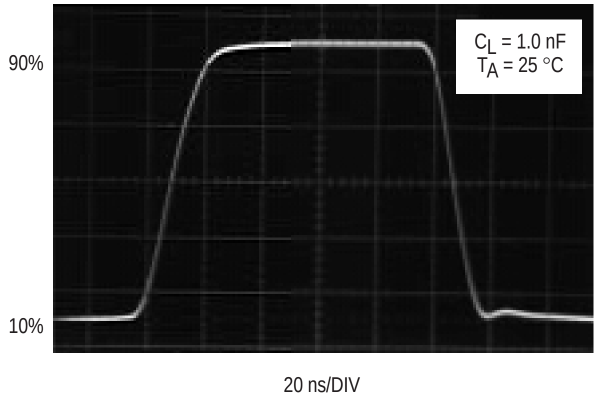


Figure 10. Soft–Start Saturation Voltage versus Capacitor Discharge Current

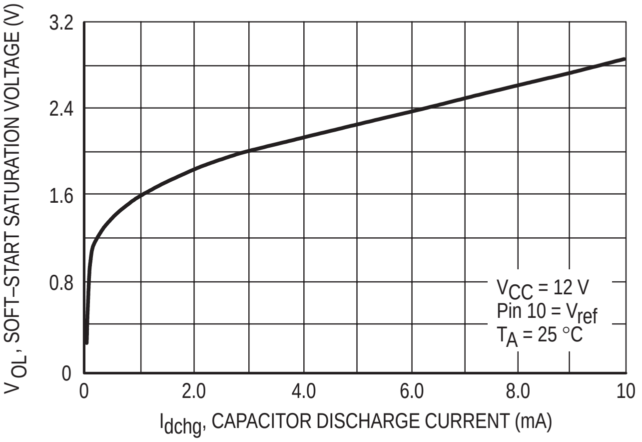


Figure 11. Operating Frequency versus Supply Current

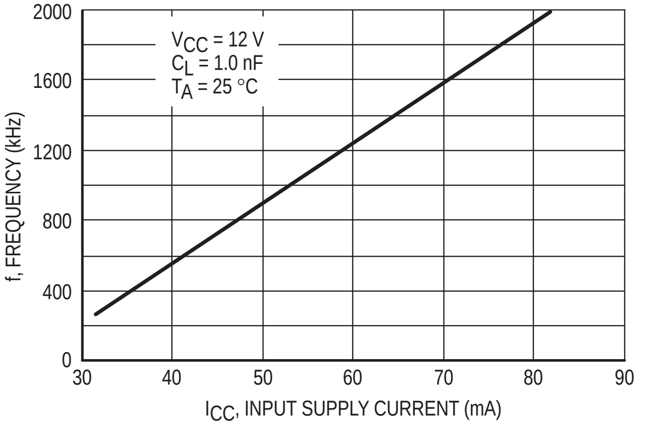


Figure 12. Supply Current versus Supply Voltage

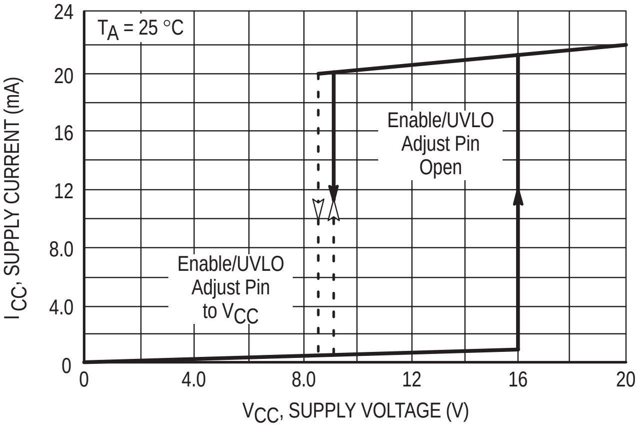
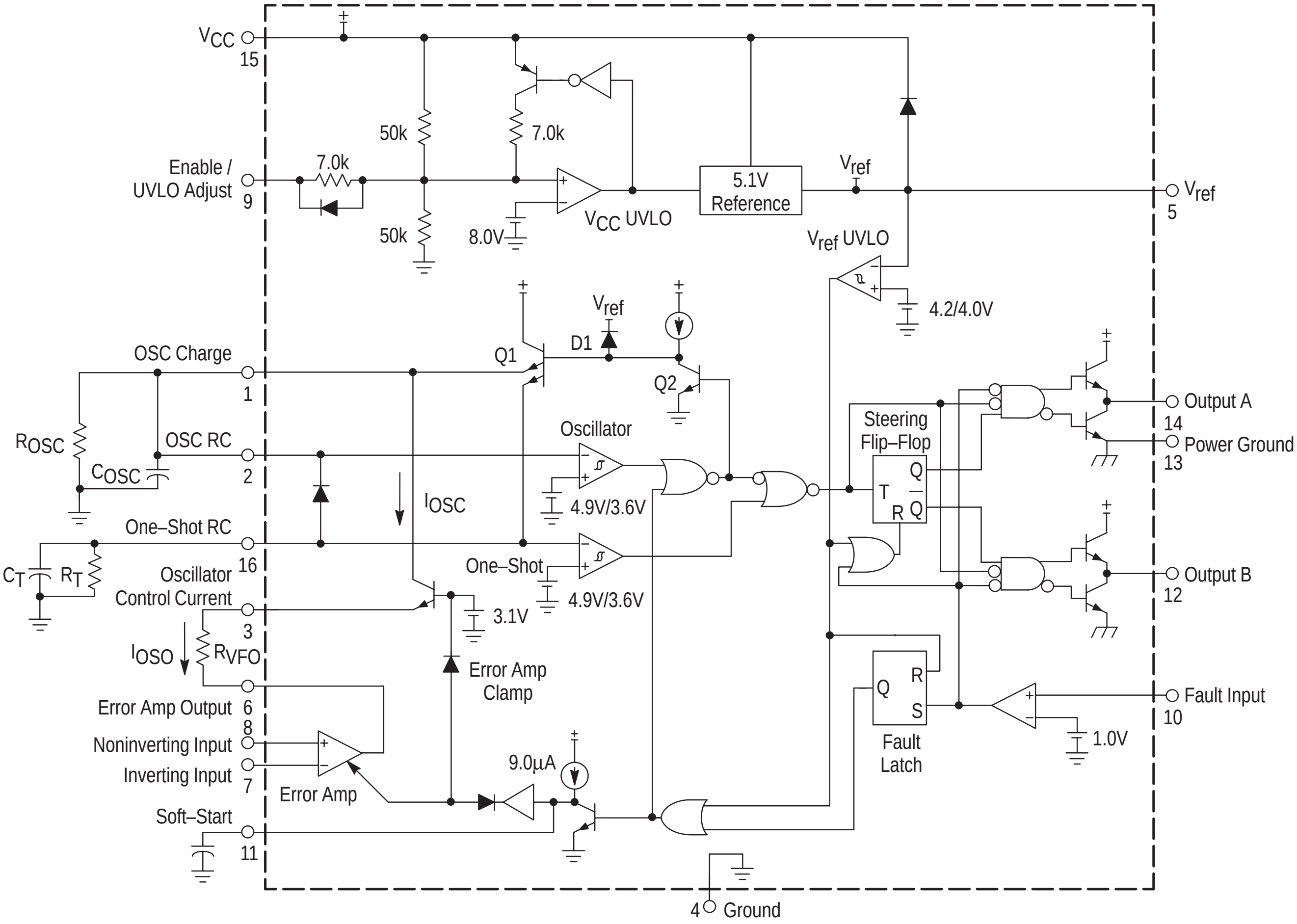
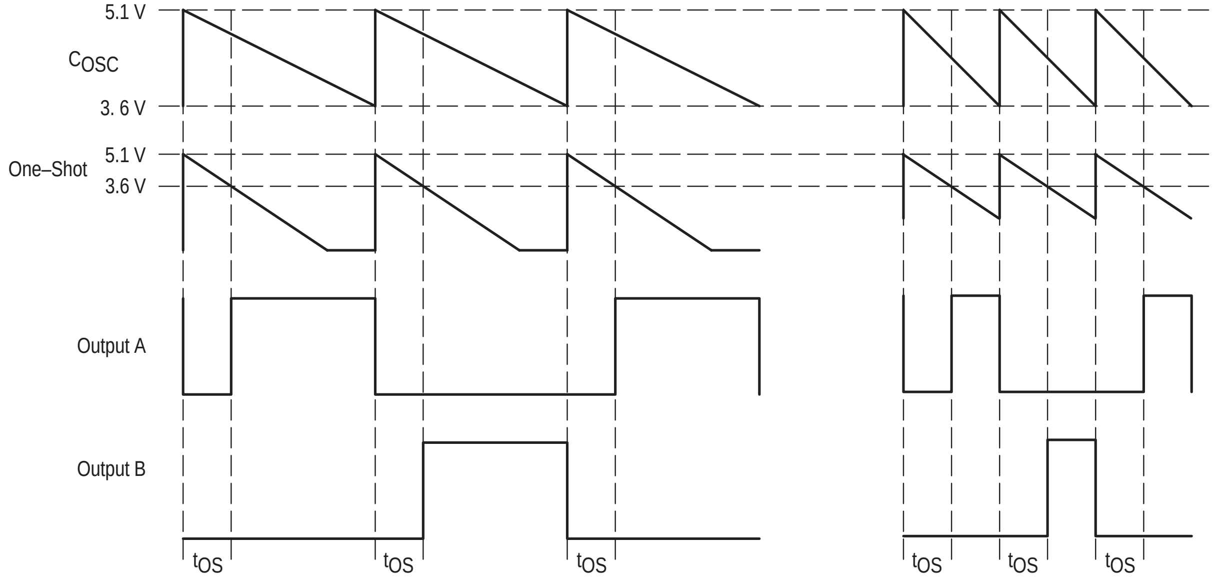


Figure 13. MC34067 Representative Block Diagram



Timing Diagram



Error Amp output high, minimum I_{OSC} current occurring at minimum input voltage, maximum load.

Error Amp output low, maximum I_{OSC} current occurring at maximum input voltage, minimum load.

OPERATING DESCRIPTION

Introduction

As power supply designers have strived to increase power conversion efficiency and reduce passive component size, high frequency resonant mode power converters have emerged as attractive alternatives to conventional pulse–width modulated control. When compared to pulse–width modulated converters, resonant mode control offers several benefits including lower switching losses, higher efficiency, lower EMI emission, and smaller size. A new integrated circuit has been developed to support this trend in power supply design. The MC34067 Resonant Mode Controller is a high performance bipolar IC dedicated to variable frequency power control at frequencies exceeding 1.0 MHz. This integrated circuit provides the features and performance specifically for zero voltage switching resonant mode power supply applications.

The primary purpose of the control chip is to provide a fixed off–time to the gates of external power MOSFETs at a repetition rate regulated by a feedback control loop. Additional features of the IC ensure that system startup and fault conditions are administered in a safe, controlled manner.

A simplified block diagram of the IC is shown on the front page, which identifies the main functional blocks and the block–to–block interconnects. Figure 13 is a detailed functional diagram which accurately represents the internal circuitry. The various functions can be divided into two sections. The first section includes the primary control path which produces precise output pulses at the desired frequency. Included in this section are a variable frequency Oscillator, a One–Shot, a pulse Steering Flip–Flop, a pair of power MOSFET Drivers, and a wide bandwidth Error Amplifier. The second section provides several peripheral support functions including a voltage reference, undervoltage lockout, Soft–Start circuit, and a fault detector.

Primary Control Path

The output pulse width and repetition rate are regulated through the interaction of the variable frequency Oscillator, One–Shot timer and Error Amplifier. The Oscillator triggers the One–Shot which generates a pulse that is alternately steered to a pair of totem pole output drivers by a toggle Flip–Flop. The Error Amplifier monitors the output of the regulator and modulates the frequency of the Oscillator. High speed Schottky logic is used throughout the primary control channel to minimize delays and enhance high frequency characteristics.

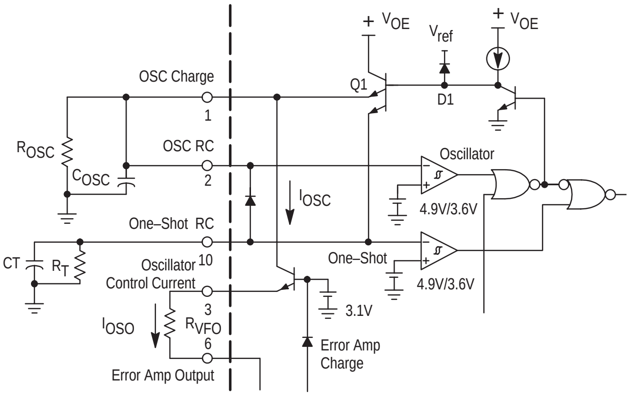
Oscillator

The characteristics of the variable frequency Oscillator are crucial for precise controller performance at high operating frequencies. In addition to triggering the One–Shot timer and initiating the output deadtime, the oscillator also determines the initial voltage for the one–shot capacitor. The Oscillator is designed to operate at frequencies exceeding 1.0 MHz. The Error Amplifier can control the oscillator frequency over a 1000:1 frequency range, and both the minimum and maximum frequencies are easily and accurately programmed by the proper selection of external components.

The functional diagram of the Oscillator and One–Shot timer is shown in Figure 14. The oscillator capacitor (C_{OSC}) is initially charged by transistor Q1. When C_{OSC} exceeds the 4.9 V upper threshold of the oscillator comparator, the base of Q1 is pulled low allowing C_{OSC} to discharge through the external resistor, (R_{OSC}), and the oscillator control current, (I_{OSC}). When the voltage on C_{OSC} falls below the comparator's 3.6 V lower threshold, Q1 turns on and again charges C_{OSC}.

C_{OSC} charges from 3.6 V to 5.1 V in less than 50 ns. The high slew rate of C_{OSC} and the propagation delay of the comparator make it difficult to control the peak voltage. This accuracy issue is overcome by clamping the base of Q1 through a diode to a voltage reference. The peak voltage of the oscillator waveform is thereby precisely set at 5.1 V.

Figure 14. Oscillator and One–Shot Timer



The frequency of the Oscillator is modulated by varying the current flowing out of the Oscillator Control Current (I_{OSC}) pin. The I_{OSC} pin is the output of a voltage regulator. The input of the voltage regulator is tied to the variable frequency oscillator. The discharge current of the Oscillator increases by increasing the current out of the I_{OSC} pin. Resistor R_{VFO} is used in conjunction with the Error Amp output to change the I_{OSC} current. Maximum frequency occurs when the Error Amplifier output is at its low state with a saturation voltage of 0.1 V at 1.0 mA.

The minimum oscillator frequency will result when the I_{OSC} current is zero, and C_{OSC} is discharged through the external resistor (R_{OSC}). This occurs when the Error Amplifier output is at its high state of 2.5 V. The minimum and maximum oscillator frequencies are programmed by the proper selection of resistor R_{OSC} and R_{VFO}. The minimum frequency is programmed by R_{OSC} using Equation 1:

$$R_{OSC} = \frac{\dfrac{1}{f_{(min)}} - t_{PD}}{C_{OSC}\ \ell n\left(\dfrac{5.1}{3.6}\right)} = \frac{t_{(max)} - 70\ \text{ns}}{0.348\ C_{OSC}} \qquad (1)$$

where t_{PD} is the internal propagation delay.

The maximum oscillator frequency is set by the current through resistor R_{VFO}. The current required to discharge C_{OSC} at the maximum oscillator frequency can be calculated by Equation 2:

$$I_{(max)} = C_{OSC} \frac{5.1 - 3.6}{\frac{1}{f_{(max)}}} = 1.5 C_{OSC} f_{(max)} \qquad (2)$$

The discharge current through R_{OSC} must also be known and can be calculated by Equation 3:

$$I_{R_{OSC}} = \frac{5.1 - 3.6}{R_{OSC}} \varepsilon^{\left(-\frac{\frac{1}{f_{(min)}}}{R_{OSC}C_{OSC}}\right)} = \frac{1.5}{R_{OSC}} \varepsilon^{\left(-\frac{1}{f_{(min)} R_{OSC} C_{OSC}}\right)} \qquad (3)$$

Resistor R_{VFO} can now be calculated by Equation 4:

$$R_{VFO} = \frac{2.5 - V_{EAsat}}{I_{(max)} - I_{R_{OSC}}} \qquad (4)$$

One–Shot Timer

The One–Shot is designed to disable both outputs simultaneously providing a deadtime before either output is enabled. The One–Shot capacitor (C_T) is charged concurrently with the oscillator capacitor by transistor Q1, as shown in Figure 14. The one–shot period begins when the oscillator comparator turns off Q1, allowing C_T to discharge. The period ends when resistor R_T discharges C_T to the threshold of the One–Shot comparator. The lower threshold of the One–Shot is 3.6 V. By choosing C_T, R_T can by solved by Equation 5:

$$R_T = \frac{t_{OS}}{C_T \ \ell n \left(\frac{5.1}{3.6}\right)} = \frac{t_{OS}}{0.348 \ C_T} \qquad (5)$$

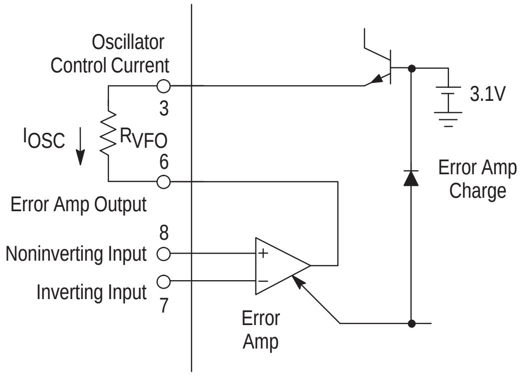
Errors in the threshold voltage and propagation delays through the output drivers will affect the One–Shot period. To guarantee accuracy, the output pulse of the control chip is trimmed to within 5% of 250 ns with nominal values of R_T and C_T.

The outputs of the Oscillator and One–Shot comparators are OR'd together to produce the pulse t_{OS}, which drives the Flip–Flop and output drivers. The output pulse (t_{OS}) is initiated by the Oscillator and terminated by the One–Shot comparator. With zero–voltage resonant mode converters, the oscillator discharge time should never be set less than the one–shot period.

Error Amplifier

A fully accessible high performance Error Amplifier is provided for feedback control of the power supply system. The Error Amplifier is internally compensated and features dc open loop gain greater than 70 dB, input offset voltage of less than 10 mV and a guaranteed minimum gain–bandwidth product of 2.5 MHz. The input common mode range extends from 1.5 V to 5.1 V, which includes the reference voltage.

Figure 15. Error Amplifier and Clamp

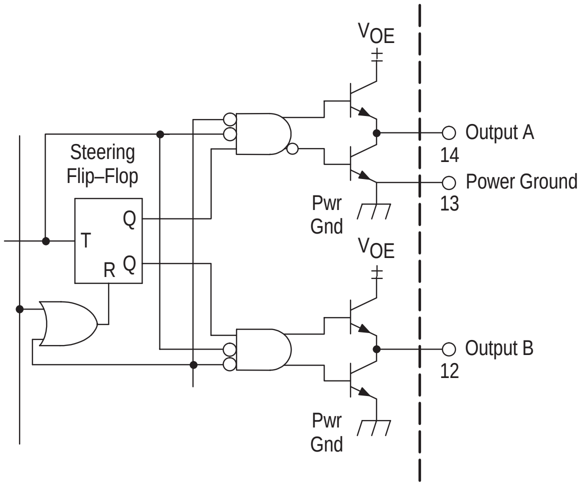


When the Error Amplifier output is coupled to the I_{OSC} pin by R_{VFO}, as illustrated in Figure 15, it provides the Oscillator Control Current, I_{OSC}. The output swing of the Error Amplifier is restricted by a clamp circuit to improve its transient recovery time.

Output Section

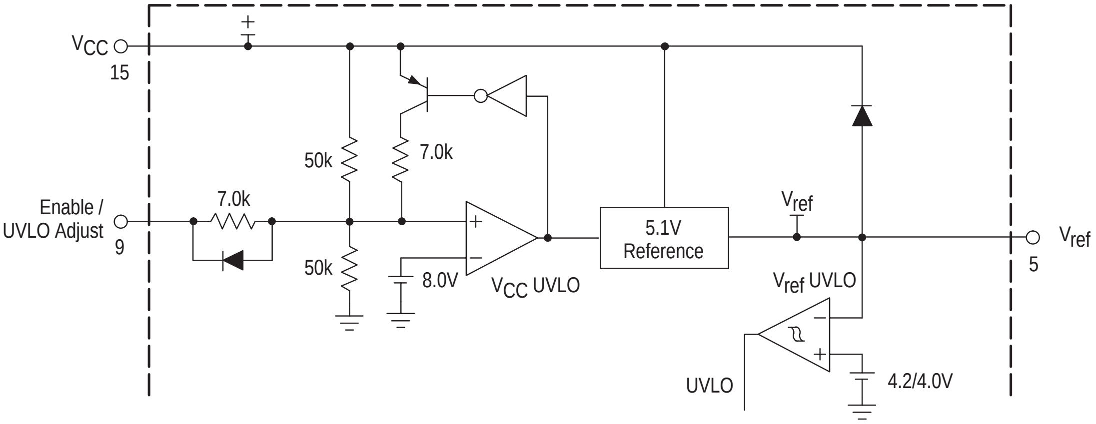
The pulse(t_{OS}), generated by the Oscillator and One–Shot timer is gated to dual totem–pole output drives by the Steering Flip–Flop shown in Figure 16. Positive transitions of t_{OS} toggle the Flip–Flop, which causes the pulses to alternate between Output A and Output B. The flip–flop is reset by the undervoltage lockout circuit during startup to guarantee that the first pulse appears at Output A.

Figure 16. Steering Flip–Flop and Output Drivers



The totem–pole output drivers are ideally suited for driving power MOSFETs and are capable of sourcing and sinking 1.5 A. Rise and fall times are typically 20 ns when driving a 1.0 nF load. High source/sink capability in a totem–pole driver normally increases the risk of high cross conduction current during output transitions. The MC34067 utilizes a unique design that virtually eliminates cross conduction, thus controlling the chip power dissipation at high frequencies. A separate power ground pin is provided to isolate the sensitive analog circuitry from large transient currents.

Figure 17. Undervoltage Lockout and Reference



PERIPHERAL SUPPORT FUNCTIONS

The MC34067 Resonant Controller provides a number of support and protection functions including a precision voltage reference, undervoltage lockout comparators, soft–start circuitry, and a fault detector. These peripheral circuits ensure that the power supply can be turned on and off in a controlled manner and that the system will be quickly disabled when a fault condition occurs.

Undervoltage Lockout and Voltage Reference

Separate undervoltage lockout comparators sense the input V_{CC} voltage and the regulated reference voltage as illustrated in Figure 17. When V_{CC} increases to the upper threshold voltage, the V_{CC} UVLO comparator enables the Reference Regulator. After the V_{ref} output of the Reference Regulator rises to 4.2 V, the V_{ref} UVLO comparator switches the UVLO signal to a logic zero state enabling the primary control path. Reducing V_{CC} to the lower threshold voltage causes the V_{CC} UVLO comparator to disable the Reference Regulator. The V_{ref} UVLO comparator then switches the UVLO output to a logic one state disabling the controller.

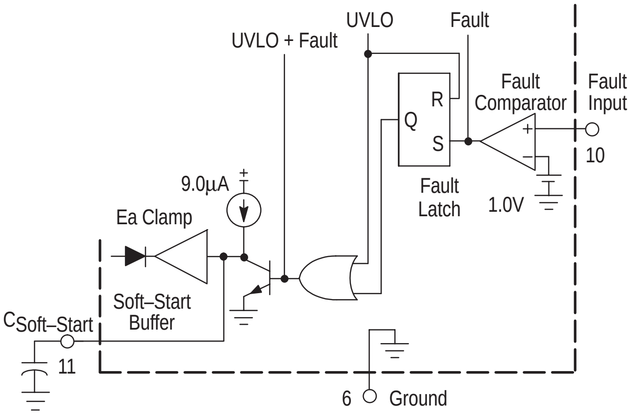
The Enable/UVLO Adjust pin allows the power supply designer to select the V_{CC} UVLO threshold voltages. When this pin is open, the comparator switches the controller on at 16 V and off at 9.0 V. If this pin is connected to the V_{CC} terminal, the upper and lower thresholds are reduced to 9.0 V and 8.6 V, respectively. Forcing the Enable/UVLO Adjust pin low will pull the V_{CC} UVLO comparator input low (through an internal diode) turning off the controller.

The Reference Regulator provides a precise 5.1 V reference to internal circuitry and can deliver up to 10 mA to external loads. The reference is trimmed to better than 2% initial accuracy and includes active short circuit protection.

Fault Detector

The high speed Fault Comparator and Latch illustrated in Figure 18 can protect a power supply from destruction under fault conditions. The Fault Input pin connects to the input of the Fault Comparator. If this input exceeds the 1.0 V threshold of the comparator, the Fault Latch is set and two logic signals simultaneously disable the primary control path. The signal labeled “Fault” at the output of the Fault Comparator is connected directly to the output drivers. This direct path reduces the propagation delay from the Fault Input to the A and B outputs to typically 70 ns. The Fault Latch output is OR’d with the UVLO output from the V_{ref} UVLO comparator to produce the logic output labeled “UVLO+Fault”. This signal disables the Oscillator and One–Shot by forcing both the C_{OSC} and C_T capacitors to be continually charged.

Figure 18. Fault Detector and Soft–Start



The Fault Latch is reset during startup by a logic “1” at the UVLO output of the V_{ref} UVLO comparator. The latch can also be reset after startup by pulling the Enable/UVLO Adjust pin momentarily low to disable the Reference Regulator.

Soft–Start Circuit

The Soft–Start circuit shown in Figure 18 forces the variable frequency Oscillator to start at the maximum frequency and ramp downward until regulated by the feedback control loop. The external capacitor at the $C_{Soft–Start}$ terminal is initially discharged by the UVLO+Fault signal. The low voltage on the capacitor passes through the Soft–Start Buffer to hold the Error Amplifier output low. After UVLO+Fault switches to a logic zero, the soft–start capacitor is charged by a 9.0 µA current source. The buffer allows the Error Amplifier output to follow the soft–start capacitor until it is regulated by the Error Amplifier inputs. The soft–start function is generally applicable to controllers operating below resonance and can be disabled by simply opening the $C_{Soft–Start}$ terminal.

APPLICATIONS INFORMATION

The MC34067 is specifically designed for zero voltage switching (ZVS) quasi–resonant converter (QRC) applications. The IC is optimized for double–ended push–pull or bridge type converters operating in continuous conduction mode. Operation of this type of ZVS with resonant properties is similar to standard push–pull or bridge circuits in that the energy is transferred during the transistor on–time. The difference is that a series resonant tank is usually introduced to shape the voltage across the power transistor prior to turn–on. The resonant tank in this topology is not used to deliver energy to the output as is the case with zero current switch topologies. When the power transistor is enabled the voltage across it should already be zero, yielding minimal switching loss. Figure 19 shows a timing diagram for a half–bridge ZVS QRC. An application circuit is shown in Figure 20. The circuit built is a dc to dc half–bridge converter delivering 75 W to the output from a 48 V source.

When building a zero voltage switch (ZVS) circuit, the objective is to waveshape the power transistor's voltage waveform so that the voltage across the transistor is zero when the device is turned on. The purpose of the control IC is to allow a resonant tank to waveshape the voltage across the power transistor while still maintaining regulation. This is accomplished by maintaining a fixed deadtime and by varying the frequency; thus the effective duty cycle is changed.

Primary side resonance can be used with ZVS circuits. In the application circuit, the elements that make the resonant tank are the primary leakage inductance of the transformer (L_L) and the average output capacitance (C_{OSS}) of a power MOSFET (C_R). The desired resonant frequency for the application circuit is calculated by Equation 6:

$$f_r = \frac{1}{2\pi\sqrt{L_L\,2C_R}} \qquad (6)$$

In the application circuit, the operating voltage is low and the value of C_{OSS} versus Drain Voltage is known. Because the C_{OSS} of a MOSFET changes with drain voltage, the value of the C_R is approximated as the average C_{OSS} of the MOSFET. For the application circuit the average C_{OSS} can be calculated by Equation 7:

$$C_R = \sqrt{2} * C_{OSS} \text{ measured at } \frac{1}{2} V_{in} \qquad (7)$$

The MOSFET chosen fixes C_R and that L_L is adjusted to achieve the desired resonant frequency.

However, the desired resonant frequency is less critical than the leakage inductance. Figure 19 shows the primary current ramping toward its peak value during the resonant transition. During this time, there is circulating current flowing through the secondary inductance, which effectively makes the primary inductance appear shorted. Therefore, the current through the primary will ramp to its peak value at a rate controlled by the leakage inductance and the applied voltage. Energy is not transferred to the secondary during this stage, because the primary current has not overcome the circulating current in the secondary. The larger the leakage inductance, the longer it takes for the primary current to slew. The practical effect of this is to lower the duty cycle, thus reducing the operating range.

The maximum duty cycle is controlled by the leakage inductance, not by the MC34067. The One–Shot in the MC34067 only assures that the power switch is turned on under a zero voltage condition. Adjust the one–shot period so that the output switch is activated while the primary current is slewing but before the current changes polarity. The resonant stage should then be designed to be as long as the time for the primary current to go to zero amps.

Figure 19. Application Timing Diagram

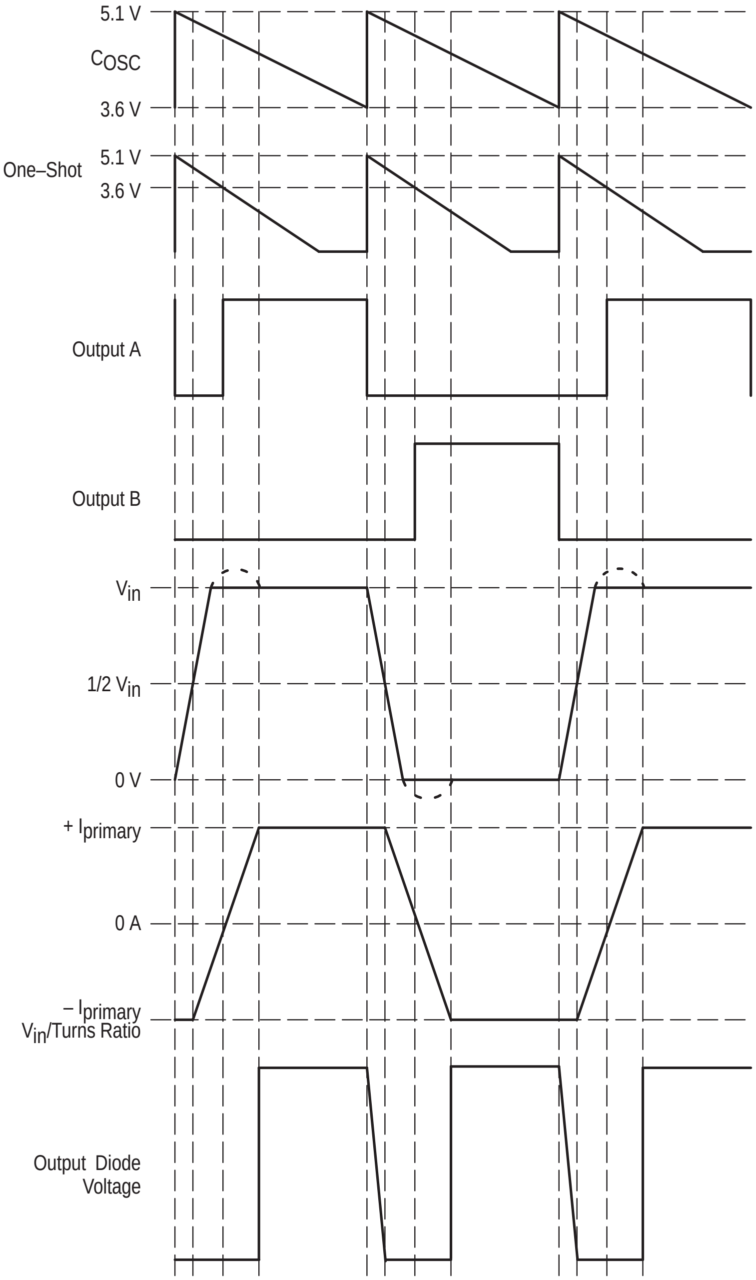
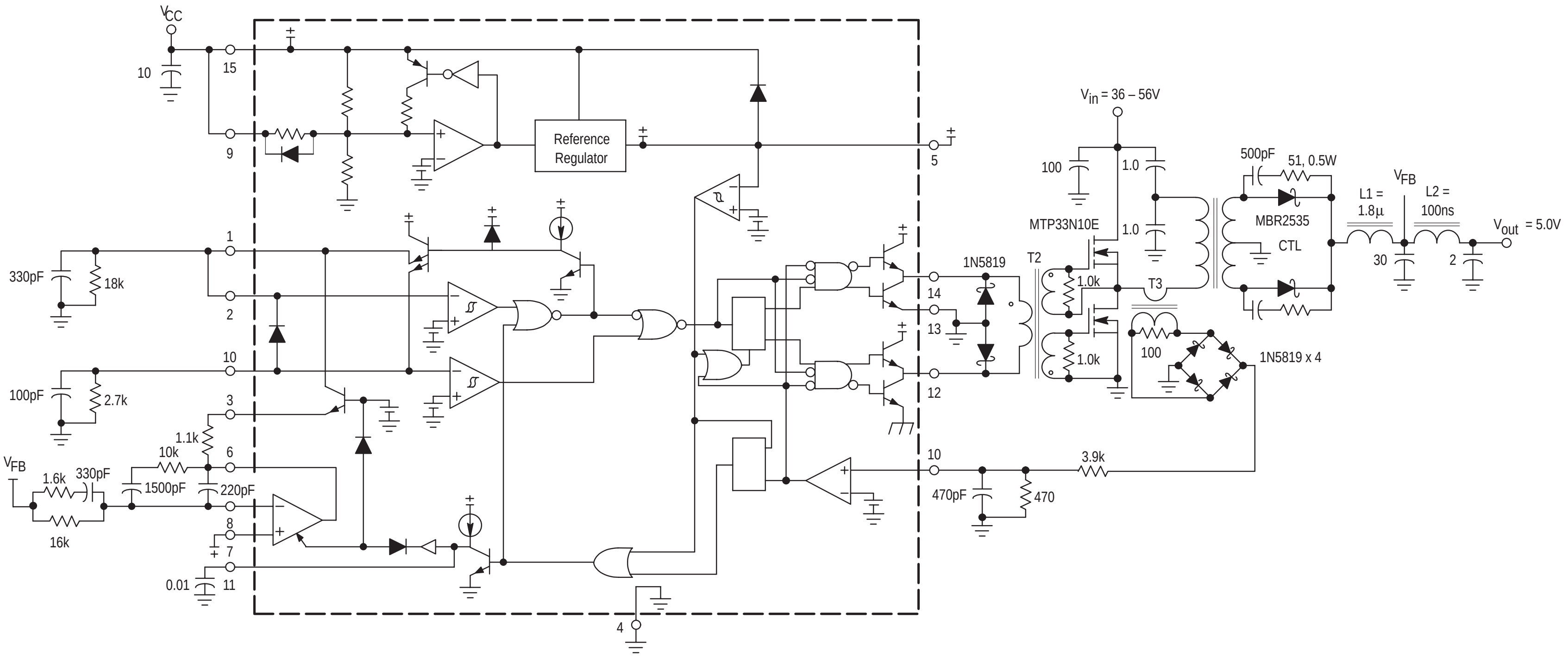


Figure 20. Application Circuit



T1 = Primary: 12 turns #48 AWG (1300 strands litz wire)
Secondary: 6 turns center tapped #48 AWG (1300 strands litz wire)
Core: Philips 3F3 4312 020 4124
Bobbin: Philips 4322 021 3525
Primary Leakage Inductance = 1.0 µH

T2 = All windings: 8 turns #36 AWG
Core: Philips 3F3 EP7–3F3
Bobbin: Philips EP7PCB1–6

T3 = Coilcraft D1870 (100 turns)

L1 = 2 turns #48 AWG (1300 strands litz wire)
Core: Philips 3F3 EP10–3F3
Bobbin: Philips EP10PCB1–8
Inductance = 1.8 µH

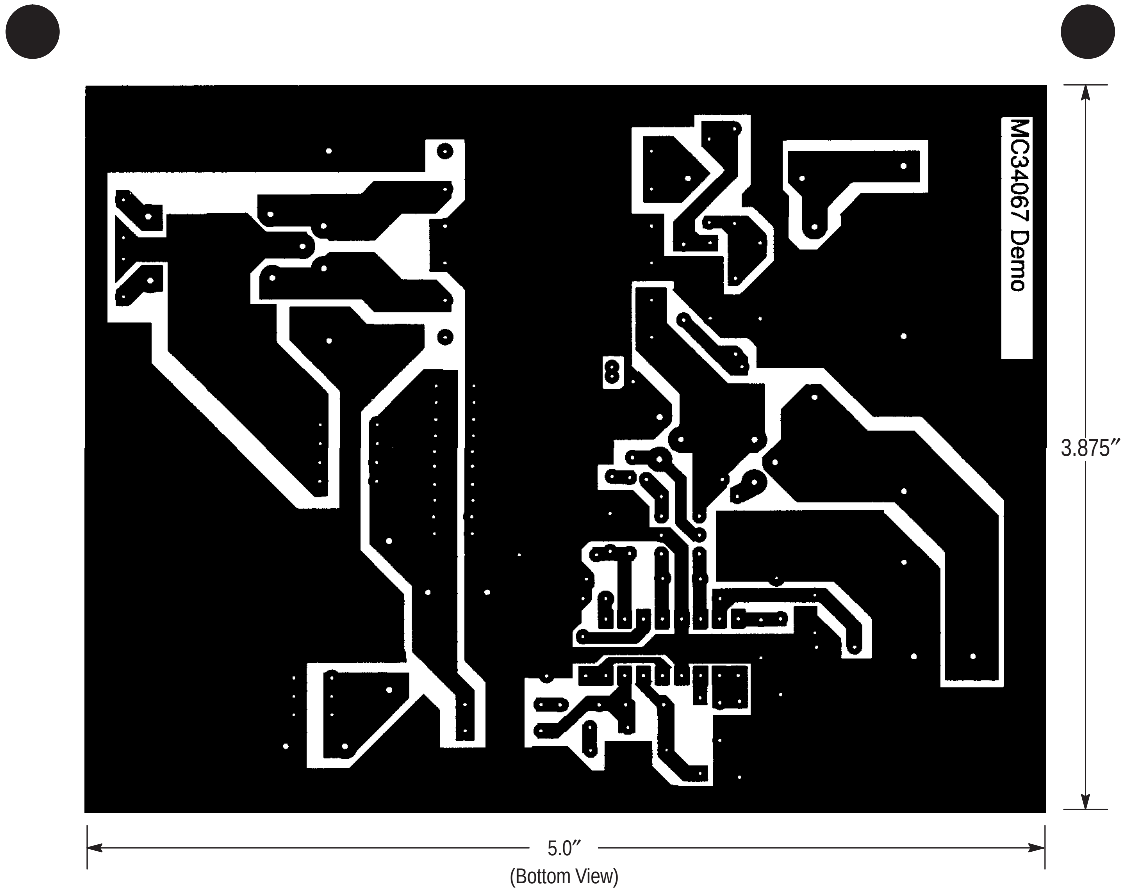
L2 = 5 turns #48 AWG (1300 strands litz wire)
Core: 0.5″ diameter air code
Inductance = 100 nH

Heatsinks = AAVID Engineering Inc. 533402B02552 with clip MC34067–5803

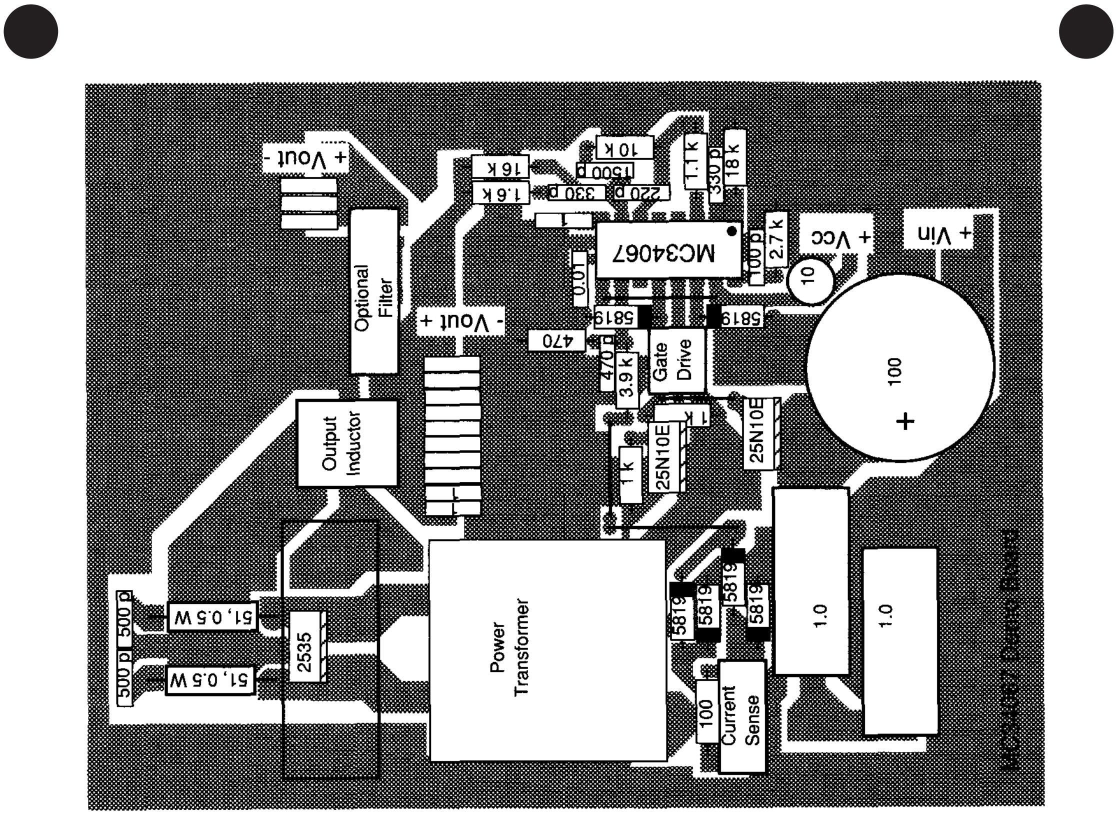
Insulators = Berquist Sil–Pad 1500

Test	Conditions	Results
Line Regulation	V_{in} = 40 V to 56 V, I_O =15 A	20 mV = ±0.198%
Load Regulation	V_{in} = 48 V, I_O = 10 A to 15 A	4.0 mV = ±0.039%
Output Ripple	V_{in} = 48 V, I_O = 15 A, f_{switch} = 1.0 MHz	25 $mV_{p–p}$
Efficiency	V_{in} = 48 V, I_O = 10 A, f_{switch} = 1.7 MHz V_{in} = 48 V, I_O = 15 A, f_{switch} = 1.0 MHz	83.5% 84.2%

Figure 21. Printed Circuit Board and Component Layout



(Bottom View)



(Top View)

MOTOROLA

MC34129
MC33129

High Performance Current Mode Controllers

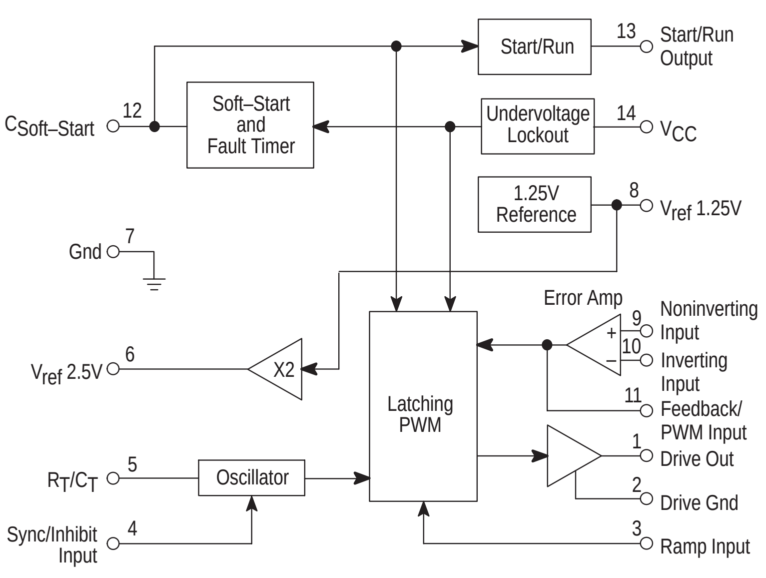
The MC34129/MC33129 are high performance current mode switching regulators specifically designed for use in low power digital telephone applications. These integrated circuits feature a unique internal fault timer that provides automatic restart for overload recovery. For enhanced system efficiency, a start/run comparator is included to implement bootstrapped operation of V_{CC}. Other functions contained are a temperature compensated reference, reference amplifier, fully accessible error amplifier, sawtooth oscillator with sync input, pulse width modulator comparator, and a high current totem pole driver ideally suited for driving a power MOSFET.

Also included are protective features consisting of soft–start, undervoltage lockout, cycle–by–cycle current limiting, adjustable deadtime, and a latch for single pulse metering.

Although these devices are primarily intended for use in digital telephone systems, they can be used cost effectively in many other applications.

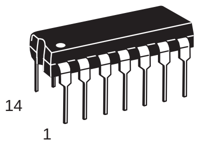
- Current Mode Operation to 300 kHz
- Automatic Feed Forward Compensation
- Latching PWM for Cycle–by–Cycle Current Limiting
- Continuous Retry after Fault Timeout
- Soft–Start with Maximum Peak Switch Current Clamp
- Internally Trimmed 2% Bandgap Reference
- High Current Totem Pole Driver
- Input Undervoltage Lockout
- Low Startup and Operating Current
- Direct Interface with Motorola SENSEFET Products

Simplified Block Diagram

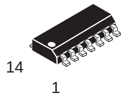


HIGH PERFORMANCE CURRENT MODE CONTROLLERS

SEMICONDUCTOR TECHNICAL DATA

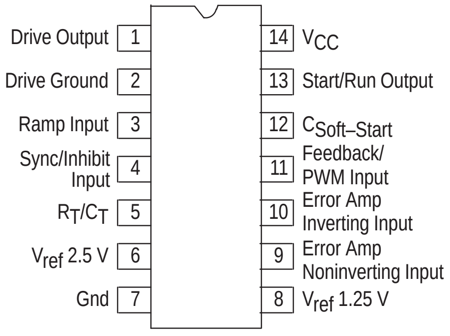


P SUFFIX
PLASTIC PACKAGE
CASE 646



D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO–14)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC34129D	T_A = 0° to +70°C	SO–14
MC34129P		Plastic DIP
MC33129D	T_A = –40° to +85°C	SO–14
MC33129P		Plastic DIP

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
V_{CC} Zener Current	$I_{Z(VCC)}$	50	mA
Start/Run Output Zener Current	$I_{Z(Start/Run)}$	50	mA
Analog Inputs (Pins 3, 5, 9, 10, 11, 12)	–	–0.3 to 5.5	V
Sync Input Voltage	V_{sync}	–0.3 to V_{CC}	V
Drive Output Current, Source or Sink	I_{DRV}	1.0	A
Current, Reference Outputs (Pins 6, 8)	I_{ref}	20	mA
Power Dissipation and Thermal Characteristics D Suffix, Plastic Package Case 751A Maximum Power Dissipation @ T_A = 70°C Thermal Resistance, Junction–to–Air P Suffix, Plastic Package Case 646 Maximum Power Dissipation @ T_A = 70°C Thermal Resistance, Junction–to–Air	 P_D $R_{\theta JA}$ P_D $R_{\theta JA}$	 552 145 800 100	 mW °C/W mW °C/W
Operating Junction Temperature	T_J	+150	°C
Operating Ambient Temperature MC34129 MC33129	T_A	 0 to +70 –40 to +85	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 10 V, T_A = 25°C [Note 1], unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
REFERENCE SECTIONS					
Reference Output Voltage, T_A = 25°C 1.25 V Ref., I_L = 0 mA 2.50 V Ref., I_L = 1.0 mA	V_{ref}	 1.225 2.375	 1.250 2.500	 1.275 2.625	V
Reference Output Voltage, T_A = T_{low} to T_{high} 1.25 V Ref., I_L = 0 mA 2.50 V Ref., I_L = 1.0 mA	V_{ref}	 1.200 2.250	 – –	 1.300 2.750	V
Line Regulation (V_{CC} = 4.0 V to 12 V) 1.25 V Ref., I_L = 0 mA 2.50 V Ref., I_L = 1.0 mA	Reg_{line}	 – –	 2.0 10	 12 50	mV
Load Regulation 1.25 V Ref., I_L = –10 µA to +500 µA 2.50 V Ref., I_L = –0.1 mA to +1.0 mA	Reg_{load}	 – –	 1.0 3.0	 12 25	mV
ERROR AMPLIFIER					
Input Offset Voltage (V_{in} = 1.25 V) T_A = 25°C T_A = T_{low} to T_{high}	V_{IO}	 – –	 1.5 –	 – 10	mV
Input Offset Current (V_{in} = 1.25 V)	I_{IO}	–	10	–	nA
Input Bias Current (V_{in} = 1.25 V) T_A = 25°C T_A = T_{low} to T_{high}	I_{IB}	 – –	 25 –	 – 200	nA
Input Common Mode Voltage Range	V_{ICR}	–	0.5 to 5.5	–	V
Open Loop Voltage Gain (V_O = 1.25 V)	A_{VOL}	65	87	–	dB
Gain Bandwidth Product (V_O = 1.25 V, f = 100 kHz)	GBW	500	750	–	kHz
Power Supply Rejection Ratio (V_{CC} = 5.0 V to 10 V)	PSRR	65	85	–	dB
Output Source Current (V_O = 1.5 V)	I_{Source}	40	80	–	µA
Output Voltage Swing High State (I_{Source} = 0 µA) Low State (I_{Sink} = 500 µA)	 V_{OH} V_{OL}	 1.75 –	 1.96 0.1	 2.25 0.15	V

NOTE: 1. T_{low} = 0°C for MC34129 / –40°C for MC33129; T_{high} = +70°C for MC34129 / +85°C for MC33129

ELECTRICAL CHARACTERISTICS (V_{CC} = 10 V, T_A = 25°C [Note 1], unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
PWM COMPARATOR					
Input Offset Voltage (V_{in} = 1.25 V)	V_{IO}	150	275	400	mV
Input Bias Current	I_{IB}	–	–120	–250	µA
Propagation Delay, Ramp Input to Drive Output	$t_{PLH(IN/DRV)}$	–	250	–	ns
SOFT–START					
Capacitor Charge Current (Pin 12 = 0 V)	I_{chg}	0.75	1.2	1.50	µA
Buffer Input Offset Voltage (V_{in} = 1.25 V)	V_{IO}	–	15	40	mV
Buffer Output Voltage (I_{Sink} = 100 µA)	V_{OL}	–	0.15	0.225	V
FAULT TIMER					
Restart Delay Time	t_{DLY}	200	400	600	µs
START/RUN COMPARATOR					
Threshold Voltage (Pin 12)	V_{th}	–	2.0	–	V
Threshold Hysteresis Voltage (Pin 12)	V_H	–	350	–	mV
Output Voltage (I_{Sink} = 500 µA)	V_{OL}	9.0	10	10.3	V
Output Off–State Leakage Current (V_{OH} = 15 V)	$I_{S/R(leak)}$	–	0.4	2.0	µA
Output Zener Voltage (I_Z = 10 mA)	V_Z	–	(V_{CC} + 7.6)	–	V
OSCILLATOR					
Frequency (R_T = 25.5 kΩ, C_T = 390 pF)	f_{OSC}	80	100	120	kHz
Capacitor C_T Discharge Current (Pin 5 = 1.2 V)	I_{dischg}	240	350	460	µA
Sync Input Current					µA
High State (V_{in} = 2.0 V)	I_{IH}	–	40	125	
Low State (V_{in} = 0.8 V)	I_{IL}	–	15	35	
Sync Input Resistance	R_{in}	12.5	32	50	kΩ
DRIVE OUTPUT					
Output Voltage					V
High State (I_{Source} = 200 mA)	V_{OH}	8.3	8.9	–	
Low State (I_{Source} = 200 mA)	V_{OL}	–	1.4	1.8	
Low State Holding Current	I_H	–	225	–	µA
Output Voltage Rise Time (C_L = 500 pF)	t_r	–	390	–	ns
Output Voltage Fall Time (C_L = 500 pF)	t_f	–	30	–	ns
Output Pull–Down Resistance	R_{PD}	100	225	350	kΩ
UNDERVOLTAGE LOCKOUT					
Startup Threshold	V_{th}	3.0	3.6	4.2	V
Hysteresis	V_H	5.0	10	15	%
TOTAL DEVICE					
Power Supply Current R_T = 25.5 kΩ, C_T = 390 pF, C_L = 500 pF	I_{CC}	1.0	2.5	4.0	mA
Power Supply Zener Voltage (I_Z = 10 mA)	V_Z	12	14.3	–	V

NOTE: 1. T_{low} = 0°C for MC34129 T_{high} = +70°C for MC34129
–40°C for MC33129 +85°C for MC33129

Figure 1. Timing Resistor versus Oscillator Frequency

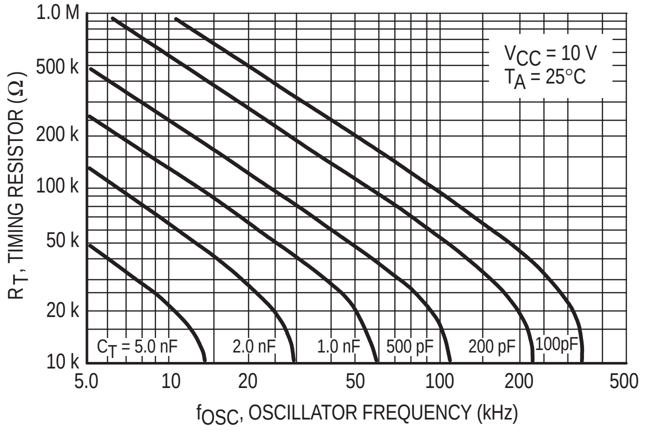


Figure 2. Output Deadtime versus Oscillator Frequency

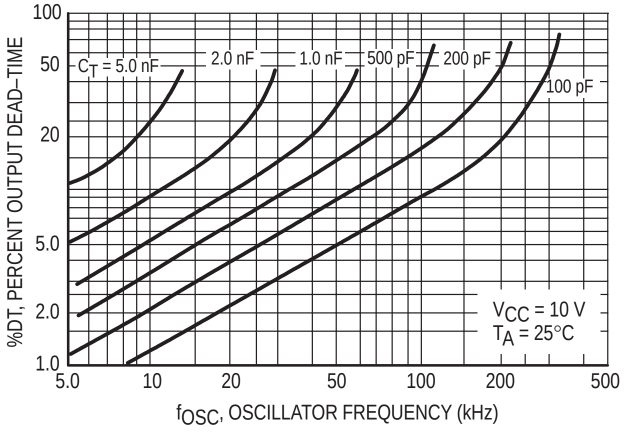


Figure 3. Oscillator Frequency Change versus Temperature

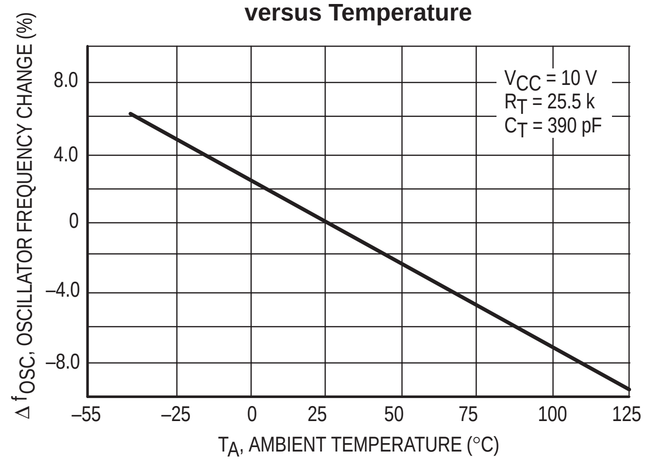


Figure 4. Error Amp Open Loop Gain and Phase versus Frequency

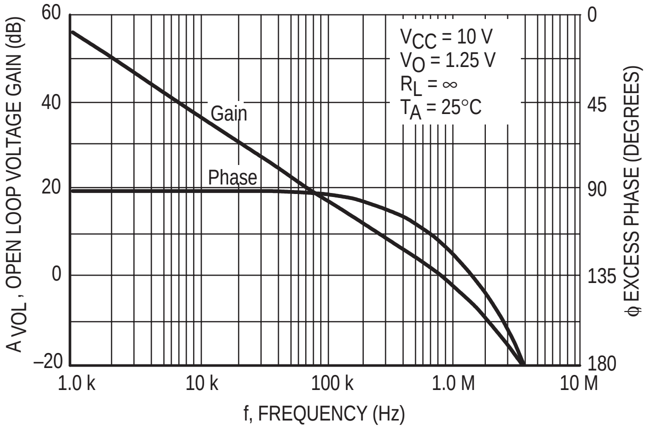


Figure 5. Error Amp Small–Signal Transient Response

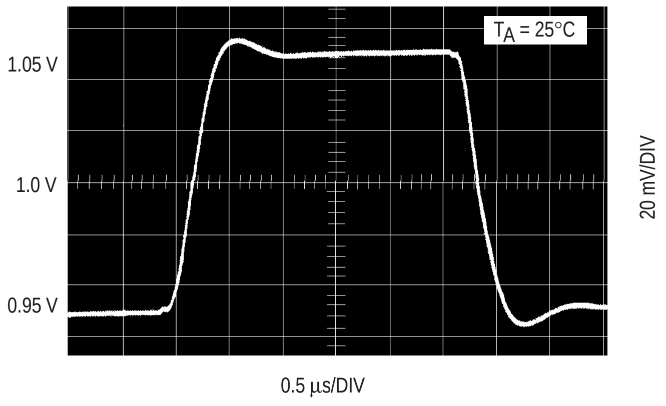


Figure 6. Error Amp Large–Signal Transient Response

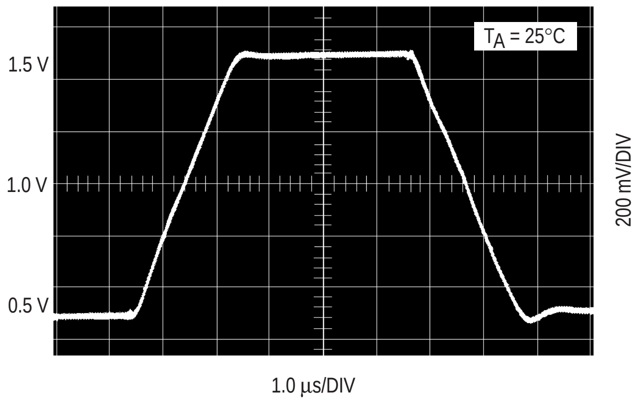


Figure 7. Error Amp Open Loop DC Gain versus Load Resistance

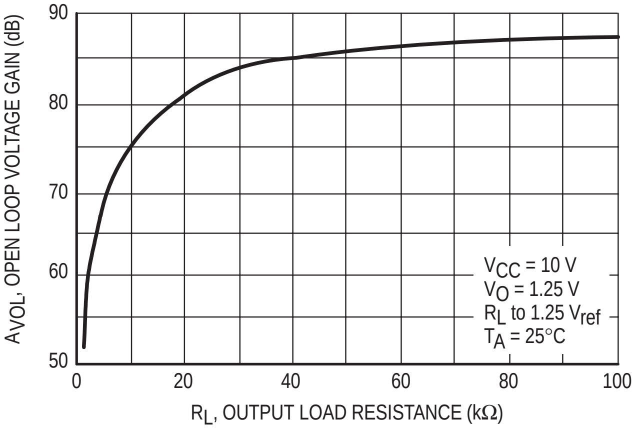


Figure 8. Error Amp Output Saturation versus Sink Current

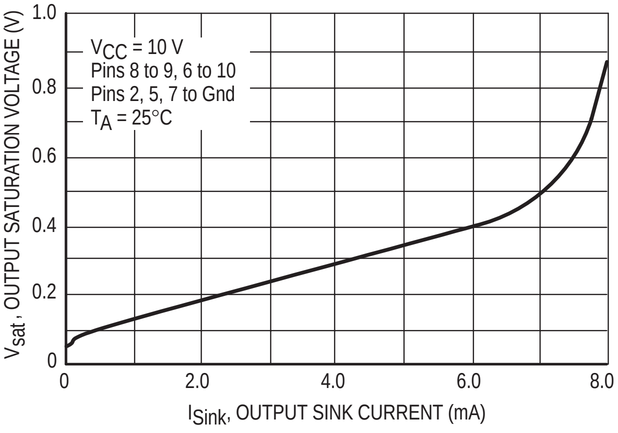


Figure 9. Soft–Start Buffer Output Saturation versus Sink Current

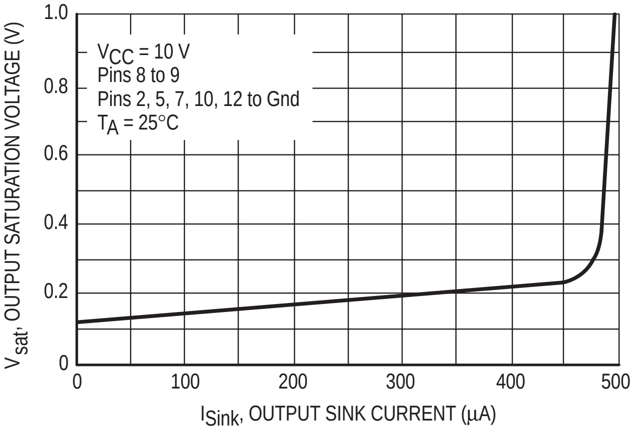


Figure 10. Reference Output Voltage versus Supply Voltage

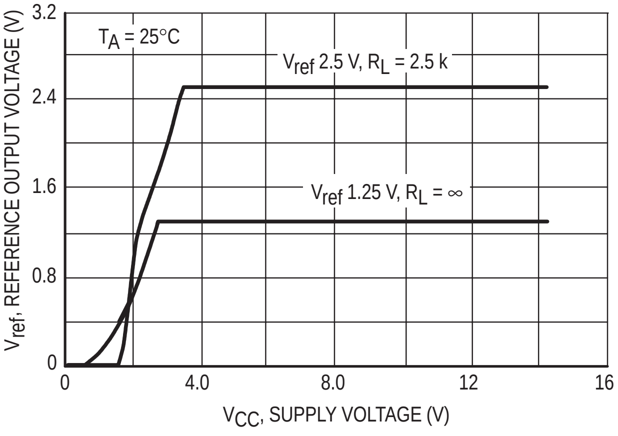


Figure 11. 1.25 V Reference Output Voltage Change versus Source Current

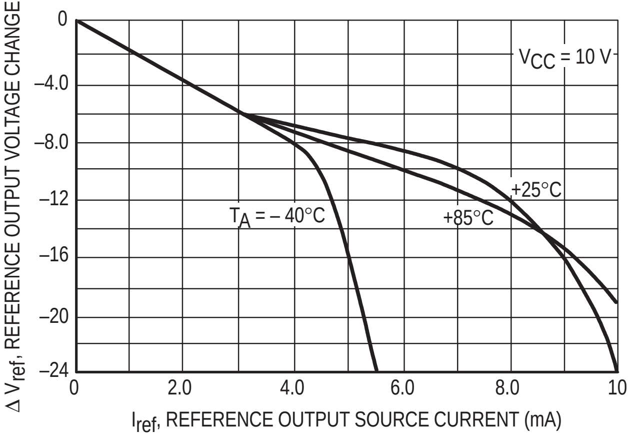


Figure 12. 2.5 V Reference Output Voltage Change versus Source Current

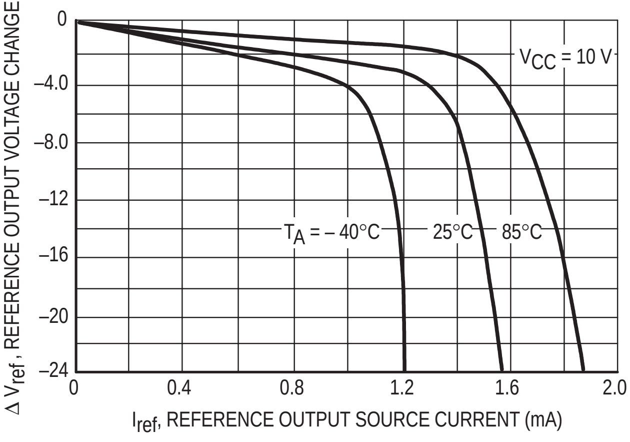


Figure 13. 1.25 V Reference Output Voltage versus Temperature

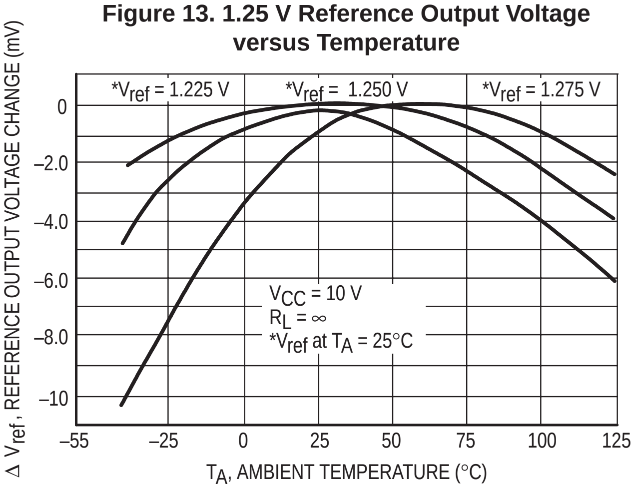


Figure 14. 2.5 V Reference Output Voltage versus Temperature

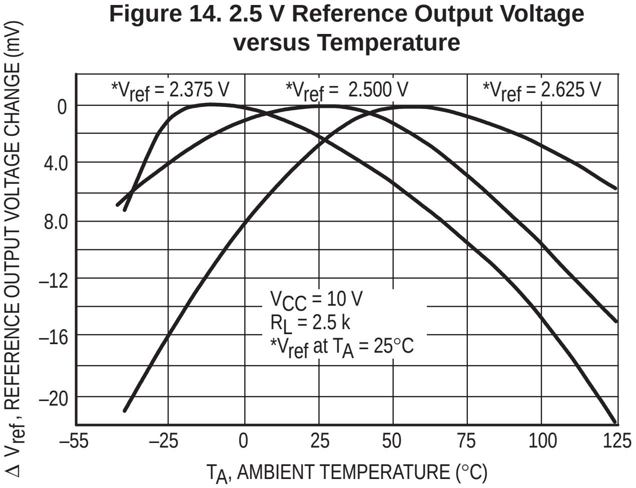


Figure 15. Drive Output Saturation versus Load Current

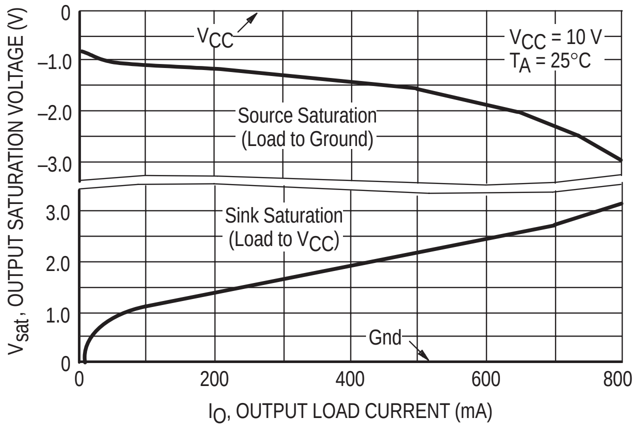


Figure 16. Drive Output Waveform

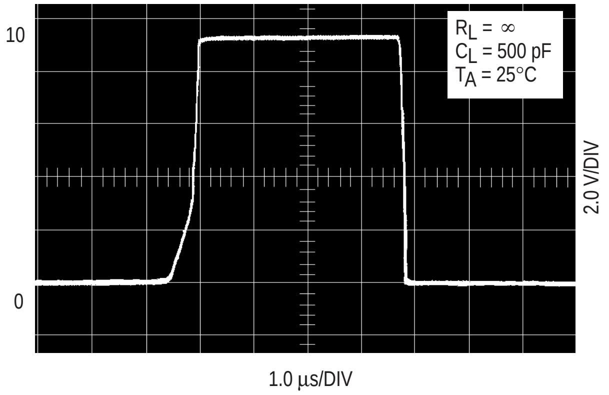
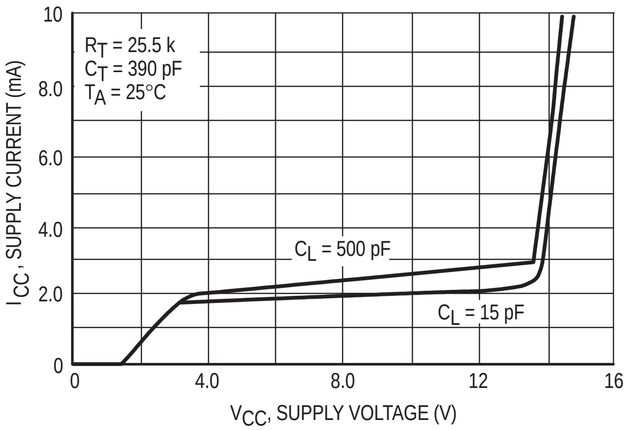


Figure 17. Supply Current versus Supply Voltage



PIN FUNCTION DESCRIPTION

Pin	Function	Description
1	Drive Output	This output directly drives the gate of a power MOSFET. Peak currents up to 1.0 A are sourced and sinked by this pin.
2	Drive Ground	This pin is a separate power ground return that is connected back to the power source. It is used to reduce the effects of switching transient noise on the control circuitry.
3	Ramp Input	A voltage proportional to the inductor current is connected to this input. The PWM uses this information to terminate output switch conduction.
4	Sync/Inhibit Input	A rectangular waveform applied to this input will synchronize the Oscillator and limit the maximum Drive Output duty cycle. A dc voltage within the range of 2.0 V to V_{CC} will inhibit the controller.
5	R_T/C_T	The free–running Oscillator frequency and maximum Drive Output duty cycle are programmed by connecting resistor R_T to V_{ref} 2.5 V and capacitor C_T to Ground. Operation to 300 kHz is possible.
6	V_{ref} 2.50 V	This output is derived from V_{ref} 1.25 V. It provides charging current for capacitor C_T through resistor R_T.
7	Ground	This pin is the control circuitry ground return and is connected back to the source ground.
8	V_{ref} 1.25 V	This output furnishes a voltage reference for the Error Amplifier noninverting input.
9	Error Amp Noninverting Input	This is the noninverting input of the Error Amplifier. It is normally connected to the 1.25 V reference.
10	Error Amp Inverting Input	This is the inverting input of the Error Amplifier. It is normally connected to the switching power supply output through a resistor divider.
11	Feedback/PWM Input	This pin is available for loop compensation. It is connected to the Error Amplifier and Soft–Start Buffer outputs, and the Pulse Width Modulator input.
12	$C_{Soft–Start}$	A capacitor $C_{Soft–Start}$ is connected from this pin to Ground for a controlled ramp–up of peak inductor current during startup.
13	Start/Run Output	This output controls the state of an external bootstrap transistor. During the start mode, operating bias is supplied by the transistor from V_{in}. In the run mode, the transistor is switched off and bias is supplied by an auxiliary power transformer winding.
14	V_{CC}	This pin is the positive supply of the control IC. The controller is functional over a minimum V_{CC} range of 4.2 V to 12 V.

OPERATING DESCRIPTION

The MC34129 series are high performance current mode switching regulator controllers specifically designed for use in low power telecommunication applications. Implementation will allow remote digital telephones and terminals to shed their power cords and derive operating power directly from the twisted pair used for data transmission. Although these devices are primarily intended for use in digital telephone systems, they can be used cost effectively in a wide range of converter applications. A representative block diagram is shown in Figure 18.

Oscillator

The oscillator frequency is programmed by the values selected for the timing components R_T and C_T. Capacitor C_T is charged from the 2.5 V reference through resistor R_T to approximately 1.25 V and discharged by an internal current sink to ground. During the discharge of C_T, the oscillator generates an internal blanking pulse that holds the lower input of the NOR gate high. This causes the Drive Output to be in a low state, thus producing a controlled amount of output deadtime. Figure 1 shows Oscillator Frequency versus R_T and Figure 2 Output Deadtime versus Frequency, both for given values of C_T. Note that many values of R_T and C_T will give the same oscillator frequency but only one combination will yield a specific output deadtime at a give frequency. In many noise sensitive applications it may be desirable to frequency–lock one or more switching regulators to an external system clock. This can be accomplished by applying the clock signal to the Synch/Inhibit Input. For reliable locking, the free–running oscillator frequency should be about 10% less than the clock frequency. Referring to the timing diagram shown Figure 19, the rising edge of the clock signal applied to the Sync/Inhibit Input, terminates charging of C_T and Drive Output conduction. By tailoring the clock waveform, accurate duty cycle clamping of the Drive Output can be achieved. A circuit method is shown in Figure 20. The Sync/Inhibit Input may also be used as a means for system shutdown by applying a dc voltage that is within the range of 2.0 V to V_{CC}.

PWM Comparator and Latch

The MC34129 operates as a current mode controller whereby output switch conduction is initiated by the oscillator and terminated when the peak inductor current reaches a threshold level established by the output of the Error Amp or Soft–Start Buffer (Pin 11). Thus the error signal controls the peak inductor current on a cycle–by–cycle basis. The PWM Comparator–Latch configuration used, ensures that only a single pulse appears at the Drive Output during any given oscillator cycle. The inductor current is converted to a voltage by inserting the ground–referenced resistor R_S in series with the source of output switch Q_1. The Ramp Input adds an offset of 275 mV to this voltage to guarantee that no pulses appear at the Drive Output when Pin 11 is at its lowest state. This occurs at the beginning of the soft–start interval or when the power supply is operating and the load is removed. The peak inductor current under normal operating conditions is controlled by the voltage at Pin 11 where:

$$I_{pk} = \frac{V_{(Pin\ 11)} - 0.275\ V}{R_S}$$

Abnormal operating conditions occur when the power supply output is overloaded or if output voltage sensing is lost. Under these conditions, the voltage at Pin 11 will be internally clamped to 1.95 V by the output of the Soft–Start Buffer. Therefore the maximum peak switch current is:

$$I_{pk(max)} = \frac{1.95\ V - 0.275}{R_S} = \frac{1.675\ V}{R_S}$$

When designing a high power switching regulator it becomes desirable to reduce the internal clamp voltage in order to keep the power dissipation of R_S to a reasonable level. A simple method which adjusts this voltage in discrete increments is shown in Figure 22. This method is possible because the Ramp Input bias current is always negative (typically –120 μA). A positive temperature coefficient equal to that of the diode string will be exhibited by $I_{pk(max)}$. An adjustable method that is more precise and temperature stable is shown in Figure 23. Erratic operation due to noise pickup can result if there is an excessive reduction of the clamp voltage. In this situation, high frequency circuit layout techniques are imperative.

A narrow spike on the leading edge of the current waveform can usually be observed and may cause the power supply to exhibit an instability when the output is lightly loaded. This spike is due to the power transformer interwinding capacitance and output rectifier recovery time. The addition of an RC filter on the Ramp Input with a time constant that approximates the spike duration will usually eliminate the instability; refer to Figure 25.

Error Amp and Soft–Start Buffer

A fully–compensated Error Amplifier with access to both inputs and output is provided for maximum design flexibility. The Error Amplifier output is common with that of the Soft–Start Buffer. These outputs are open–collector (sink only) and are ORed together at the inverting input of the PWM Comparator. With this configuration, the amplifier that demands lower peak inductor current dominates control of the loop. Soft–Start is mandatory for stable startup when power is provided through a high source impedance such as the long twisted pair used in telecommunications. It effectively removes the load from the output of the switching power supply upon initial startup. The Soft–Start Buffer is configured as a unity gain follower with the noninverting input connected to Pin 12. An internal 1.0 μA current source charges the soft–start capacitor ($C_{Soft–Start}$) to an internally clamped level of 1.95 V. The rate of change of peak inductor current, during startup, is programmed by the capacitor value selected. Either the Fault Timer or the Undervoltage Lockout can discharge the soft–start capacitor.

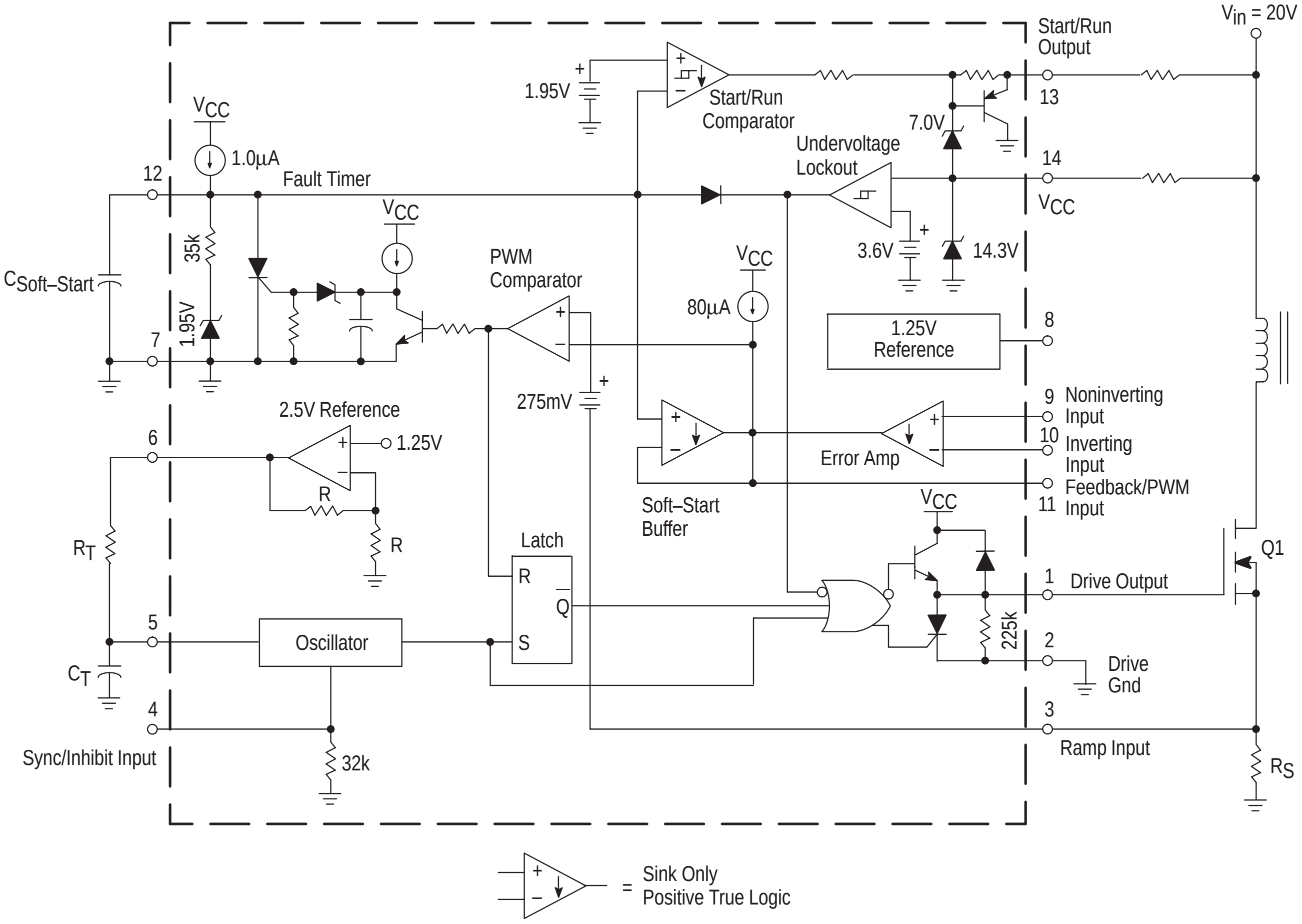


Figure 18. Representative Block Diagram

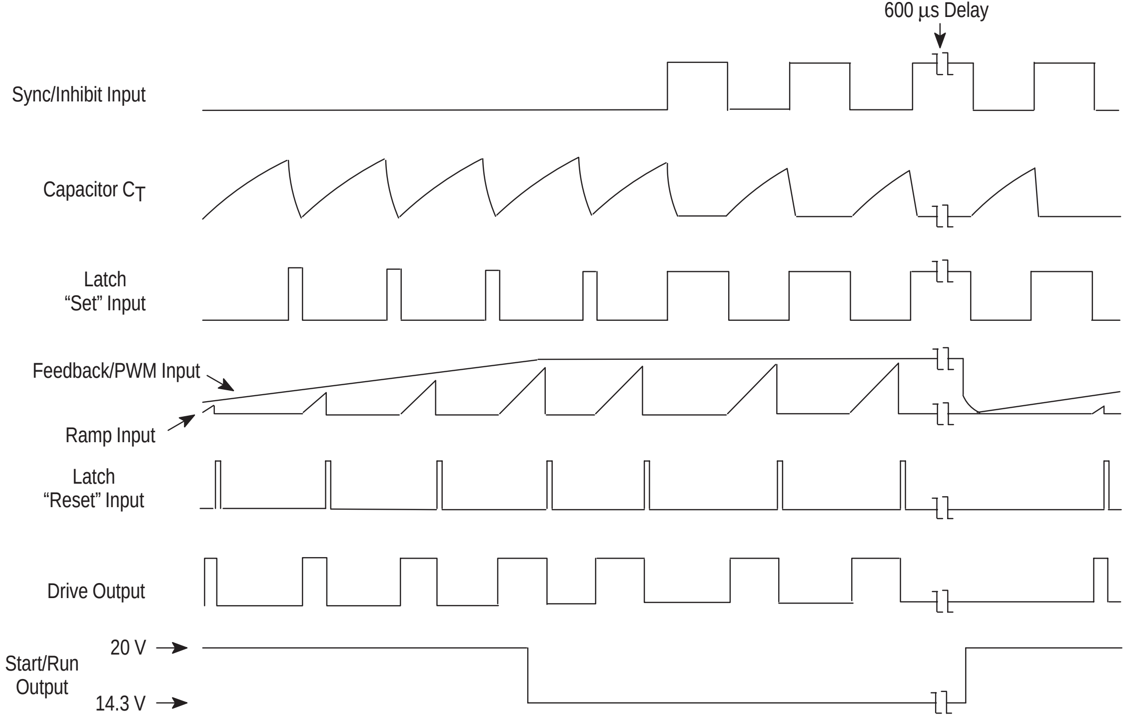


Figure 19. Timing Diagram

Fault Timer

This unique circuit prevents sustained operating in a lockout condition. This can occur with conventional switching control ICs when operating from a power source with a high series impedance. If the power required by the load is greater than that available from the source, the input voltage will collapse, causing the lockout condition. The Fault Timer provides automatic recovery when this condition is detected. Under normal operating conditions, the output of the PWM Comparator will reset the Latch and discharge the internal Fault Timer capacitor on a cycle–by–cycle basis. Under operating conditions where the required power into the load is greater than that available from the source (V_{in}), the Ramp Input voltage (plus offset) will not reach the comparator threshold level (Pin 11), and the output of the PWM Comparator will remain low. If this condition persists for more that 600 µs, the Fault Timer will active, discharging $C_{Soft–Start}$ and initiating a soft–start cycle. The power supply will operate in a skip cycle or hiccup mode until either the load power or source impedance is reduced. The minimum fault timeout is 200 µs, which limits the useful switching frequency to a minimum of 5.0 kHz.

Start/Run Comparator

A bootstrap startup circuit is included to improve system efficiency when operating from a high input voltage. The output of the Start/Run Comparator controls the state of an external transistor. A typical application is shown in Figure 21. While $C_{Soft–Start}$ is charging, startup bias is supplied to V_{CC} (Pin 14) from V_{in} through transistor Q2. When $C_{Soft–Start}$ reaches the 1.95 V clamp level, the Start–Run output switches low (V_{CC} = 50 mV), turning off Q2. Operating bias is now derived from the auxiliary bootstrap winding of the transformer, and all drive power is efficiently converted down from V_{in}. The start time must be long enough for the power supply output to reach regulation. This will ensure that there is sufficient bias voltage at the auxiliary bootstrap winding for sustained operation.

$$t_{Start} = \frac{1.95VC_{Soft–Start}}{1.0\ \mu A} = 1.95\ C_{Soft–Start} \text{ in } \mu F$$

The Start/Run Comparator has 350 mV of hysteresis. The output off–state is clamped to V_{CC} + 7.6 V by the internal zener and PNP transistor base–emitter junction.

Drive Output and Drive Ground

The MC34129 contains a single totem–pole output stage that was specifically designed for direct drive of power MOSFETs. It is capable of up to ±1.0 A peak drive current and has a typical fall time of 30 ns with a 500 pF load. The totem–pole stage consists of an NPN transistor for turn–on drive and a high speed SCR for turn–off. The SCR design requires less average supply current (I_{CC}) when compared to conventional switching control ICs that use an all NPN totem–pole. The SCR accomplishes this during turn–off of the MOSFET, by utilizing the gate charge as regenerative on–bias, whereas the conventional all transistor design requires continuous base current. Conversion efficiency in low power applications is greatly enhanced with this reduction of I_{CC}. The SCR's low–state holding current (I_H) is typically 225 µA. An internal 225 kΩ pull–down resistor is included to shunt the Drive Output off–state leakage to ground when the Undervoltage Lockout is active. A separate Drive Ground is provided to reduce the effects of switching transient noise imposed on the Ramp Input. This feature becomes particularly useful when the $I_{pk(max)}$ clamp level is reduced. Figure 24 shows the proper implementation of the MC34129 with a current sensing power MOSFET.

Undervoltage Lockout

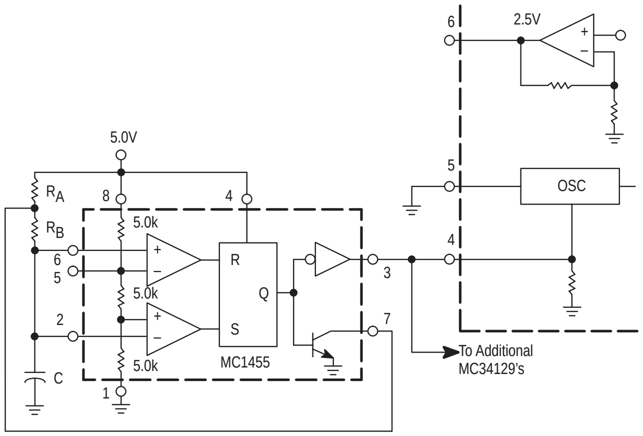
The Undervoltage Lockout comparator holds the Drive Output and $C_{Soft–Start}$ pins in the low state when V_{CC} is less than 3.6 V. This ensures that the MC34129 is fully functional before the output stage is enabled and a soft–start cycle begins. A built–in hysteresis of 350 mV prevents erratic output behavior as V_{CC} crosses the comparator threshold voltage. A 14.3 V zener is connected as a shunt regulator from V_{CC} to ground. Its purpose is to protect the MOSFET gate from excessive drove voltage during system startup. An external 9.1 V zener is required when driving low threshold MOSFETs. Refer to Figure 21. The minimum operating voltage range of the IC is 4.2 V to 12 V.

References

The 1.25 V bandgap reference is trimmed to ±2.0% tolerance at T_A = 25°C. It is intended to be used in conjunction with the Error Amp. The 2.50 V reference is derived from the 1.25 V reference by an internal op amp with a fixed gain of 2.0. It has an output tolerance of ±5.0% at T_A = 25°C and its primary purpose is to supply charging current to the oscillator timing capacitor.

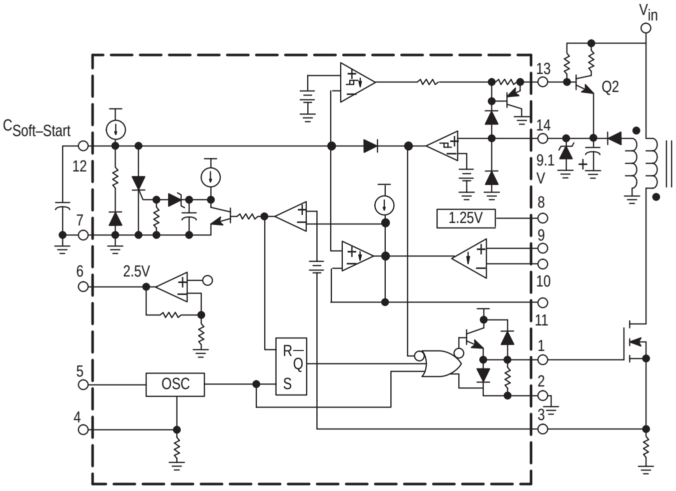
For further information, please refer to AN976.

Figure 20. External Duty Cycle Clamp and Multi–Unit Synchronization



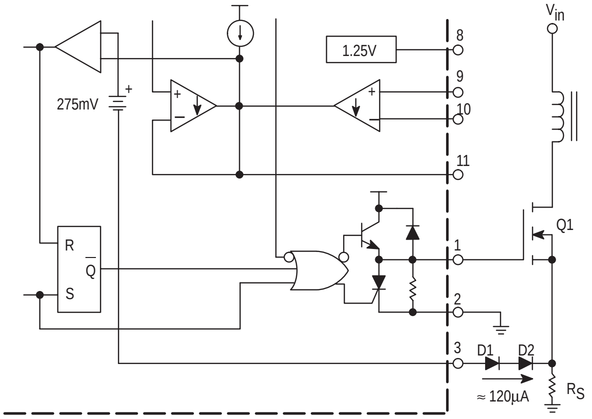
$$f = \frac{1.44}{(R_A + 2R_B)C} \qquad D_{max} = \frac{R_B}{R_A + 2R_B}$$

Figure 21. Bootstrap Startup



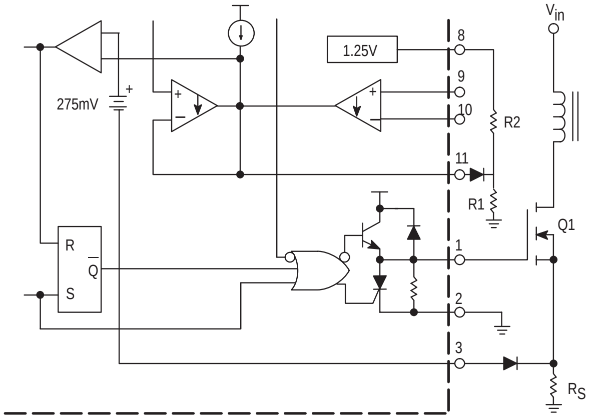
The external 9.1 V zener is required when driving low threshold MOSFETs.

Figure 22. Discrete Step Reduction of Clamp Level



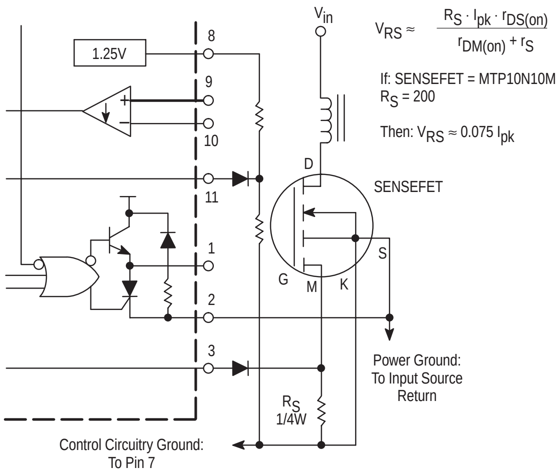
$$I_{pk(max)} = \frac{1.675 - (V_{F(D1)} + V_{F(D2)})}{R_S}$$

Figure 23. Adjustable Reduction of Clamp Level



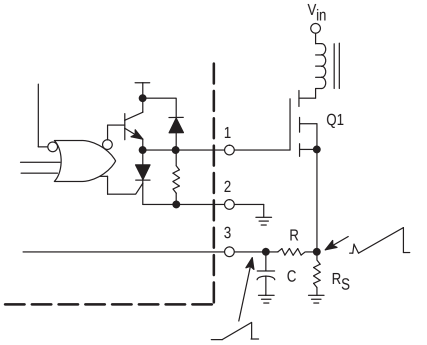
$$\text{If: } \frac{1.25\ \text{V}}{R1 + R2} \geq 1.0\ \text{mA} \qquad \text{Then: } I_{pk(max)} \approx \frac{\dfrac{1.25}{\left(\dfrac{R2}{R1} + 1\right)} - 0.275}{R_S}$$

Figure 24. Current Sensing Power MOSFET



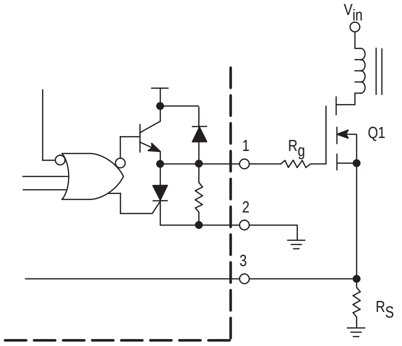
Virtually lossless current sensing can be achieved with the implementation of a SENSEFET power switch.

Figure 25. Current Waveform Spike Suppression



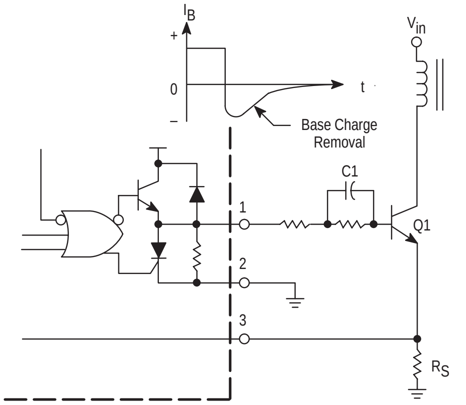
The addition of the RC filter will eliminate instability caused by the leading edge spike on the current waveform.

Figure 26. MOSFET Parasitic Oscillations



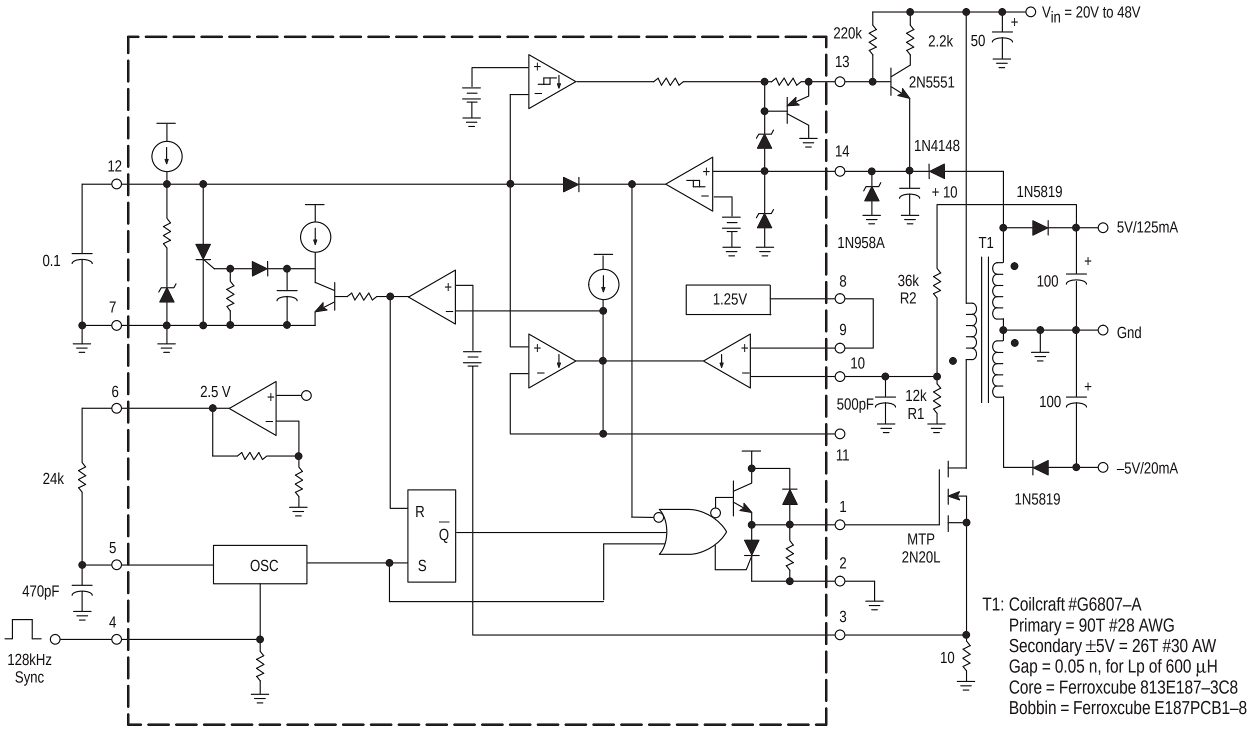
Series gate resistor R_g will damp any high frequency parasitic oscillations caused by the MOSFET input capacitance and any series wiring inductance in the gate–source circuit.

Figure 27. Bipolar Transistor Drive



The totem–pole output can furnish negative base current for enhanced transistor turn–off, with the addition of capacitor C1.

Figure 28. Non–Isolated 725 mW Flyback Regulator

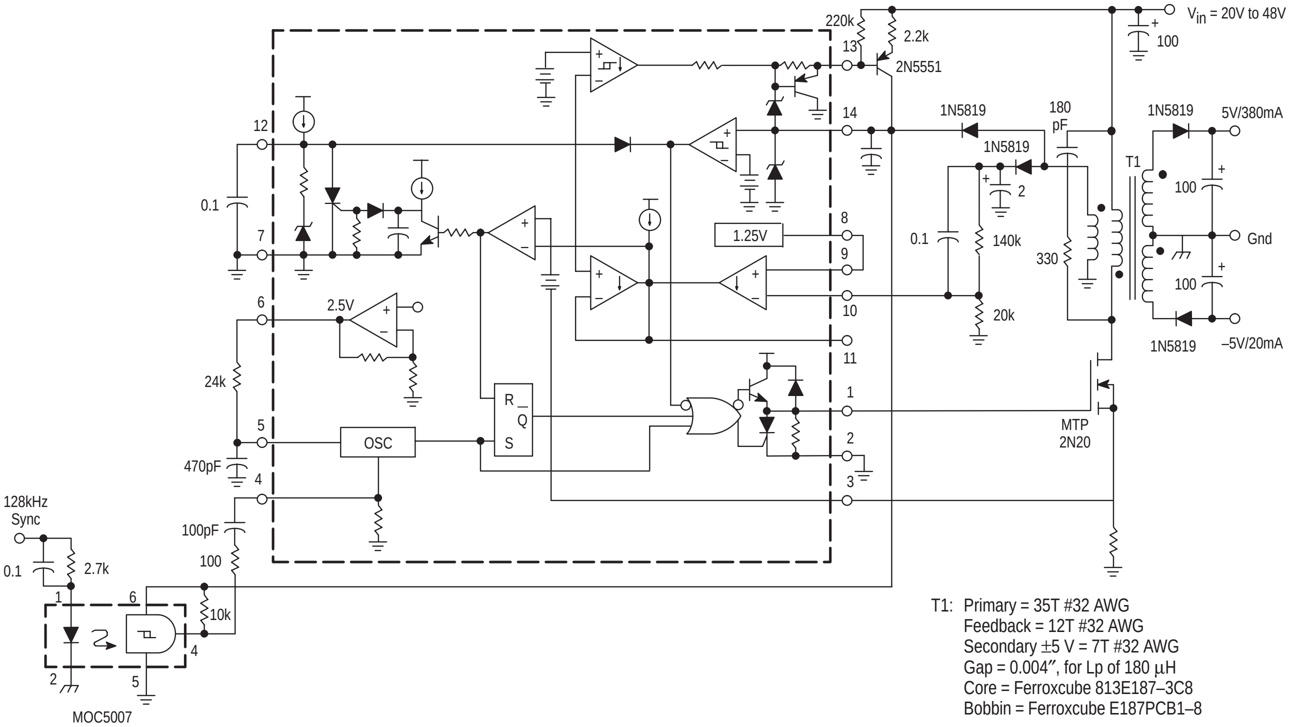


T1: Coilcraft #G6807–A
Primary = 90T #28 AWG
Secondary ±5V = 26T #30 AW
Gap = 0.05 n, for Lp of 600 µH
Core = Ferroxcube 813E187–3C8
Bobbin = Ferroxcube E187PCB1–8

Test	Conditions	Results
Line Regulation 5.0 V	V_{in} = 20 V to 40 V, I_{out} 5.0 V = 125 mA, I_{out} –5.0 V = 20 mA	Δ = 1.0 mV
Load Regulation 5.0 V	V_{in} = 30 V, I_{out} 5.0 V = 0 mA to 150 mA, I_{out} –5.0 V = 20 mA	Δ = 2.0 mV
Output Ripple 5.0 V	V_{in} = 30 V, I_{out} 5.0 V = 125 mA, I_{out} –5.0 V = 20 mA	150 mVpp
Efficiency	V_{in} = 30 V, I_{out} 5.0 V = 125 mA, I_{out} –5.0 V = 20 mA	77%

$$V_{out} = 1.25\left(\frac{R2}{R1} + 1\right)$$

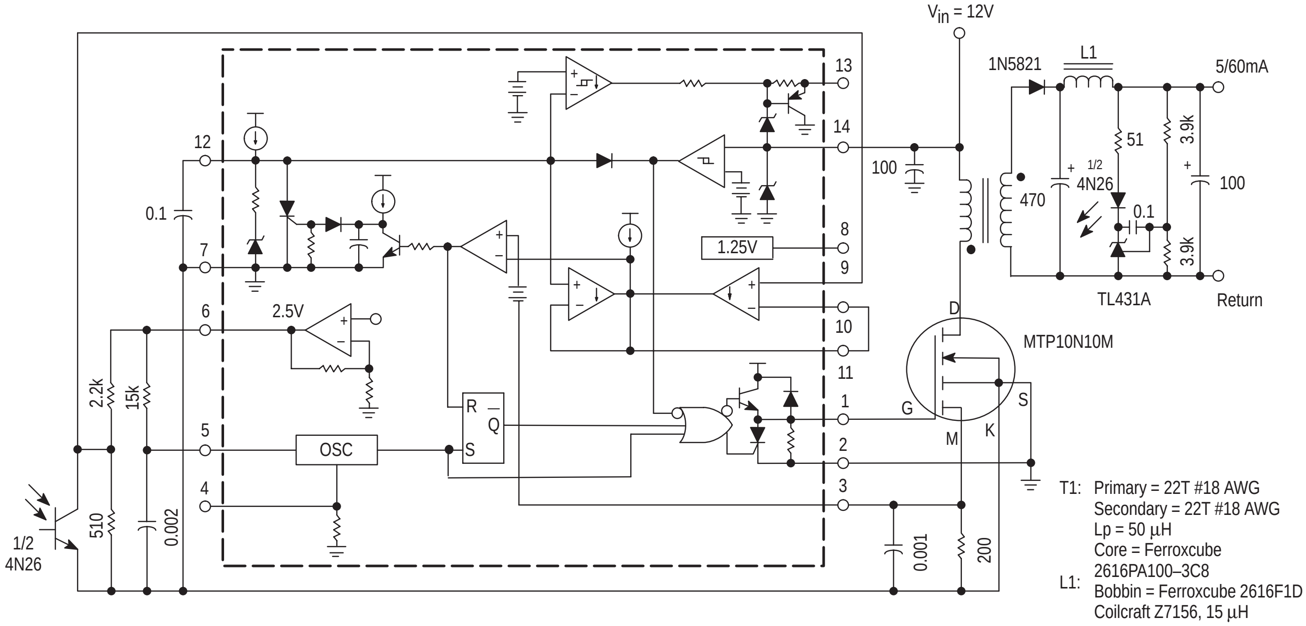
Figure 29. Isolated 2.0 W Flyback Regulator



T1: Primary = 35T #32 AWG
Feedback = 12T #32 AWG
Secondary ±5 V = 7T #32 AWG
Gap = 0.004″, for Lp of 180 µH
Core = Ferroxcube 813E187–3C8
Bobbin = Ferroxcube E187PCB1–8

Test	Conditions	Results
Line Regulation 5.0 V	V_{in} = 20 V to 40 V, I_{out} 5.0 V = 380 mA, I_{out} –5.0 V = 20 mA	Δ = 1.0 mV
Load Regulation 5.0 V	V_{in} = 30 V, I_{out} 5.0 V = 100 mA to 380 mA, I_{out} –5.0 V = 20 mA	Δ = 15 mV
Output Ripple 5.0 V	V_{in} = 30 V, I_{out} 5.0 V = 380 mA, I_{out} –5.0 V = 20 mA	150 mVpp
Efficiency	V_{in} = 30 V, I_{out} 5.0 V = 380 mA, I_{out} –5.0 V = 20 mA	73%

Figure 30. Isolated 3.0 W Flyback Regulator with Secondary Side Sensing



Test	Conditions	Results
Line Regulation	V_{in} = 8.0 V to 12 V, I_{out} 600 mA	Δ = 1.0 mV
Load Regulation	V_{in} = 12 V, I_{out} = 100 mA to 600 mA	Δ = 8.0 mV
Output Ripple	V_{in} = 12 V, I_{out} = 600 mA	20 mVpp
Efficiency	V_{in} = 12 V, I_{out} = 600 mA	81%

An economical method of achieving secondary sensing is to combine the TL431A with a 4N26 optocoupler.

MC34151
MC33151

High Speed Dual MOSFET Drivers

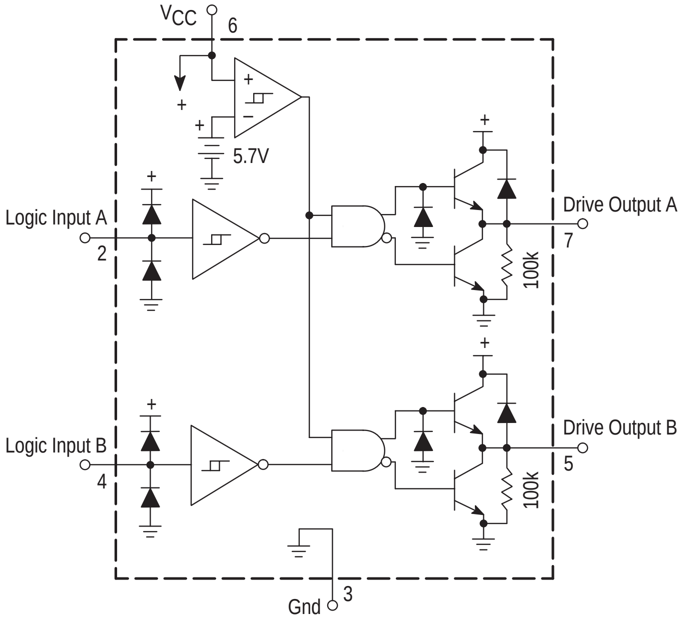
The MC34151/MC33151 are dual inverting high speed drivers specifically designed for applications that require low current digital circuitry to drive large capacitive loads with high slew rates. These devices feature low input current making them CMOS and LSTTL logic compatible, input hysteresis for fast output switching that is independent of input transition time, and two high current totem pole outputs ideally suited for driving power MOSFETs. Also included is an undervoltage lockout with hysteresis to prevent erratic system operation at low supply voltages.

Typical applications include switching power supplies, dc to dc converters, capacitor charge pump voltage doublers/inverters, and motor controllers.

These devices are available in dual–in–line and surface mount packages.

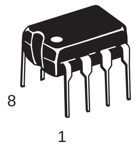
- Two Independent Channels with 1.5 A Totem Pole Output
- Output Rise and Fall Times of 15 ns with 1000 pF Load
- CMOS/LSTTL Compatible Inputs with Hysteresis
- Undervoltage Lockout with Hysteresis
- Low Standby Current
- Efficient High Frequency Operation
- Enhanced System Performance with Common Switching Regulator Control ICs
- Pin Out Equivalent to DS0026 and MMH0026

Representative Block Diagram

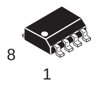


HIGH SPEED DUAL MOSFET DRIVERS

SEMICONDUCTOR TECHNICAL DATA

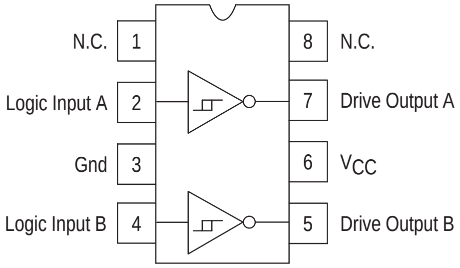


P SUFFIX
PLASTIC PACKAGE
CASE 626



D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC34151D	T_A = 0° to +70°C	SO–8
MC34151P		Plastic DIP
MC33151D	T_A = –40° to +85°C	SO–8
MC33151P		Plastic DIP

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	20	V
Logic Inputs (Note 1)	V_{in}	–0.3 to V_{CC}	V
Drive Outputs (Note 2) Totem Pole Sink or Source Current Diode Clamp Current (Drive Output to V_{CC})	 I_O $I_{O(clamp)}$	 1.5 1.0	A
Power Dissipation and Thermal Characteristics D Suffix SO–8 Package Case 751 Maximum Power Dissipation @ T_A = 50°C Thermal Resistance, Junction–to–Air P Suffix 8–Pin Package Case 626 Maximum Power Dissipation @ T_A = 50°C Thermal Resistance, Junction–to–Air	 P_D $R_{\theta JA}$ P_D $R_{\theta JA}$	 0.56 180 1.0 100	 W °C/W W °C/W
Operating Junction Temperature	T_J	+150	°C
Operating Ambient Temperature MC34151 MC33151	T_A	 0 to +70 –40 to +85	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

ELECTRICAL CHARACTERISTICS

(V_{CC} = 12 V, for typical values T_A = 25°C, for min/max values T_A is the only operating ambient temperature range that applies [Note 3], unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
LOGIC INPUTS					
Input Threshold Voltage – High State Logic 1 – Low State Logic 0	V_{IH} V_{IL}	2.6 –	1.75 1.58	– 0.8	V
Input Current – High State (V_{IH} = 2.6 V) – Low State (V_{IL} = 0.8 V)	I_{IH} I_{IL}	– –	200 20	500 100	µA
DRIVE OUTPUT					
Output Voltage – Low State (I_{Sink} = 10 mA) (I_{Sink} = 50 mA) (I_{Sink} = 400 mA) – High State (I_{Source} = 10 mA) (I_{Source} = 50 mA) (I_{Source} = 400 mA)	V_{OL} V_{OH}	– – – 10.5 10.4 9.5	0.8 1.1 1.7 11.2 11.1 10.9	1.2 1.5 2.5 – – –	V
Output Pull–Down Resistor	R_{PD}	–	100	–	kΩ
SWITCHING CHARACTERISTICS (T_A = 25°C)					
Propagation Delay (10% Input to 10% Output, C_L = 1.0 nF) Logic Input to Drive Output Rise Logic Input to Drive Output Fall	 $t_{PLH(in/out)}$ $t_{PHL(in/out)}$	 – –	 35 36	 100 100	ns
Drive Output Rise Time (10% to 90%) C_L = 1.0 nF C_L = 2.5 nF	t_r	– –	14 31	30 –	ns
Drive Output Fall Time (90% to 10%) C_L = 1.0 nF C_L = 2.5 nF	t_f	– –	16 32	30 –	ns
TOTAL DEVICE					
Power Supply Current Standby (Logic Inputs Grounded) Operating (C_L = 1.0 nF Drive Outputs 1 and 2, f = 100 kHz)	I_{CC}	 – –	 6.0 10.5	 10 15	mA
Operating Voltage	V_{CC}	6.5	–	18	V

NOTES: 1. For optimum switching speed, the maximum input voltage should be limited to 10 V or V_{CC}, whichever is less.
2. Maximum package power dissipation limits must be observed.
3. T_{low} = 0°C for MC34151 T_{high} = +70°C for MC34151
–40°C for MC33151 +85°C for MC33151

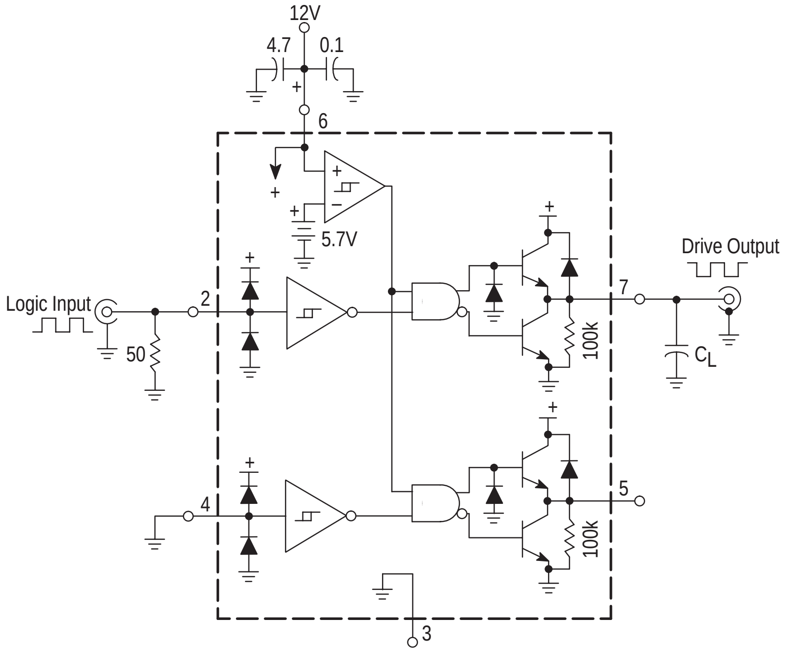


Figure 1. Switching Characteristics Test Circuit

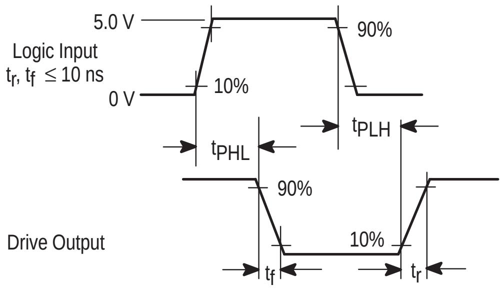


Figure 2. Switching Waveform Definitions

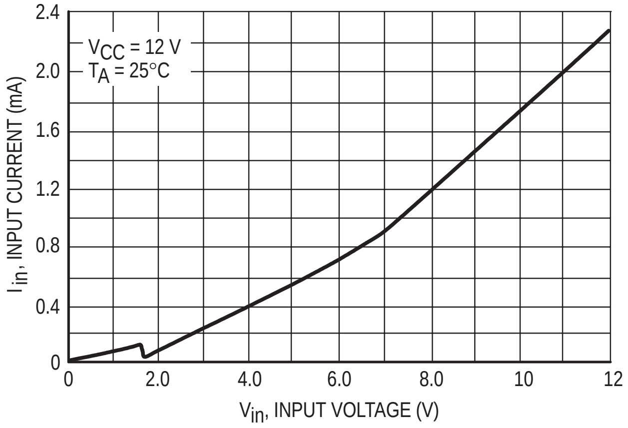


Figure 3. Logic Input Current versus Input Voltage

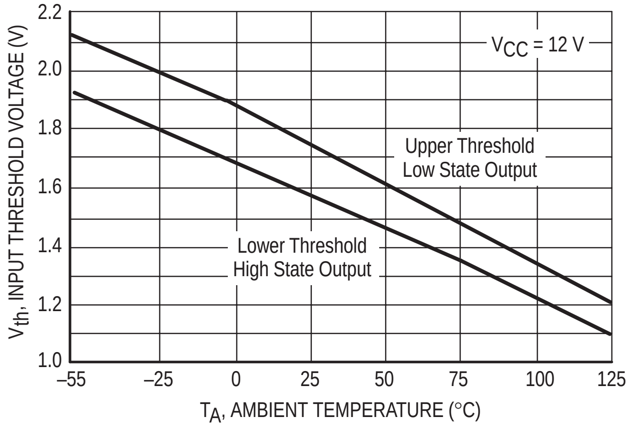


Figure 4. Logic Input Threshold Voltage versus Temperature

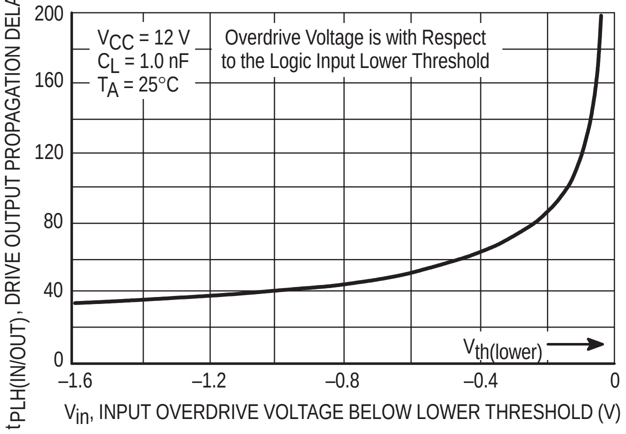


Figure 5. Drive Output Low–to–High Propagation Delay versus Logic Overdrive Voltage

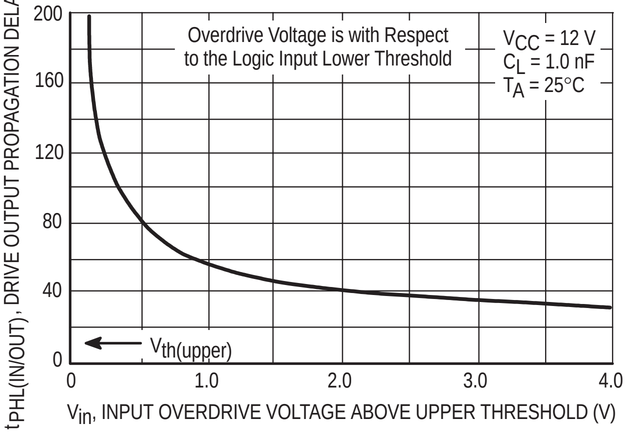


Figure 6. Drive Output High–to–Low Propagation Delay versus Logic Input Overdrive Voltage

Figure 7. Propagation Delay

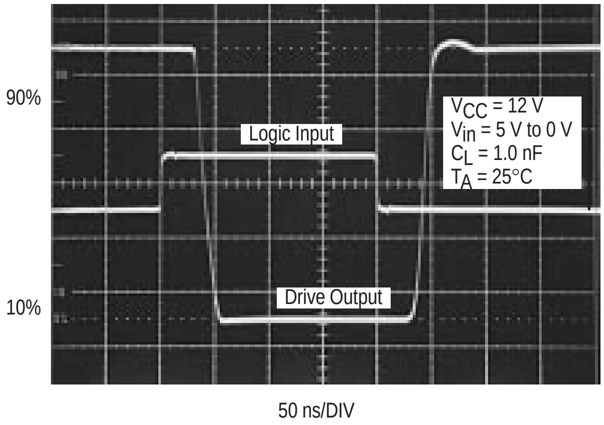


Figure 8. Drive Output Clamp Voltage versus Clamp Current

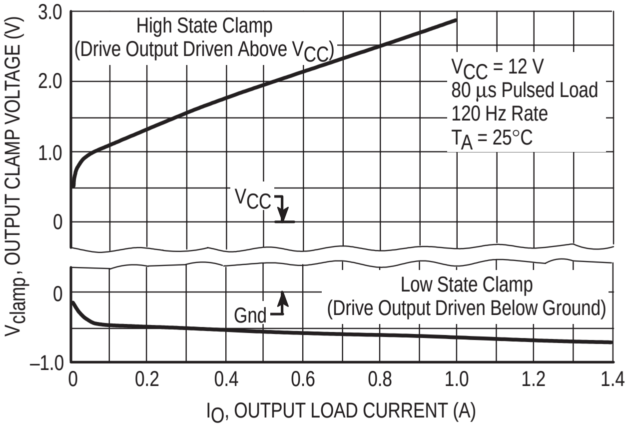


Figure 9. Drive Output Saturation Voltage versus Load Current

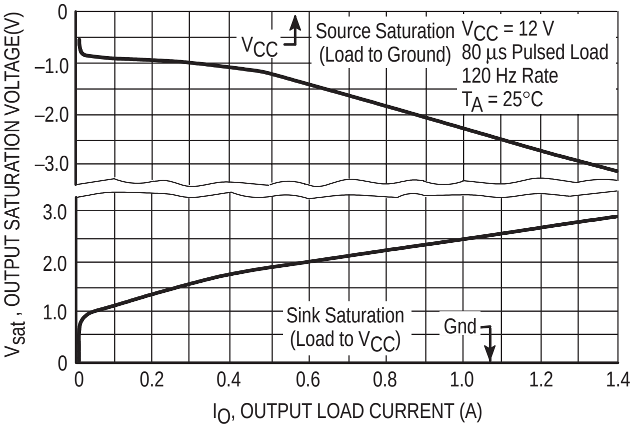


Figure 10. Drive Output Saturation Voltage versus Temperature

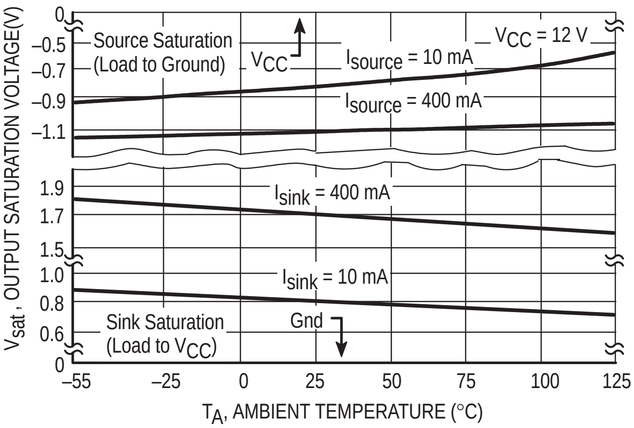


Figure 11. Drive Output Rise Time

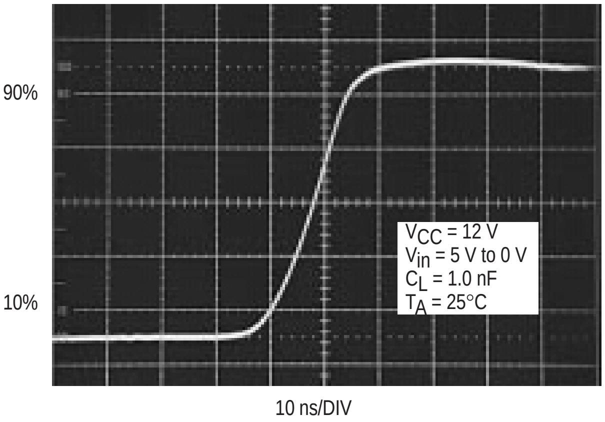


Figure 12. Drive Output Fall Time

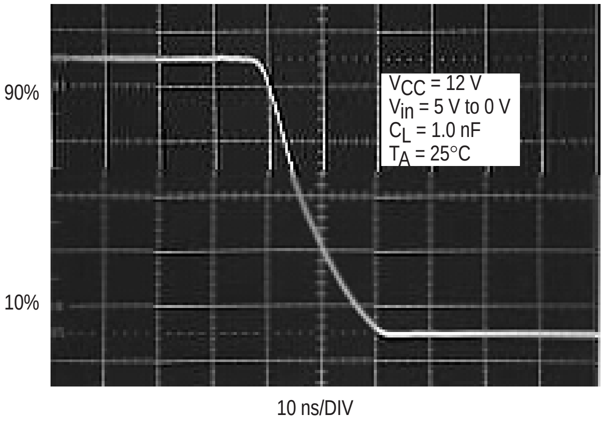


Figure 13. Drive Output Rise and Fall Time versus Load Capacitance

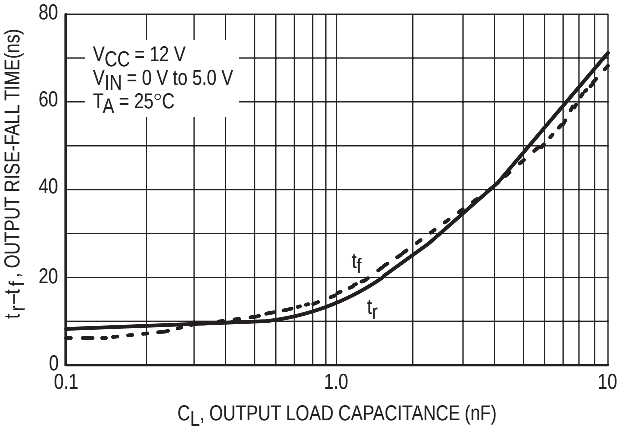


Figure 14. Supply Current versus Drive Output Load Capacitance

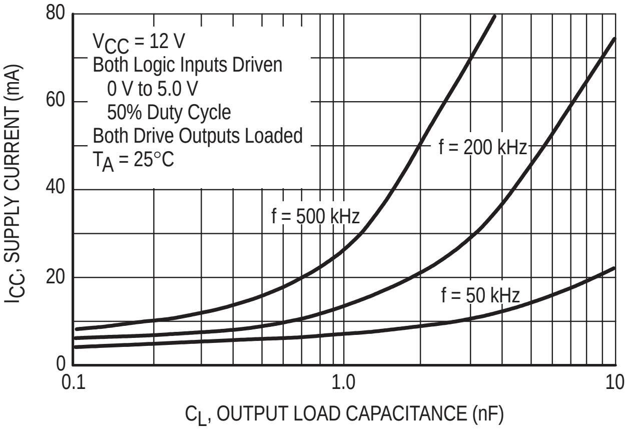


Figure 15. Supply Current versus Input Frequency

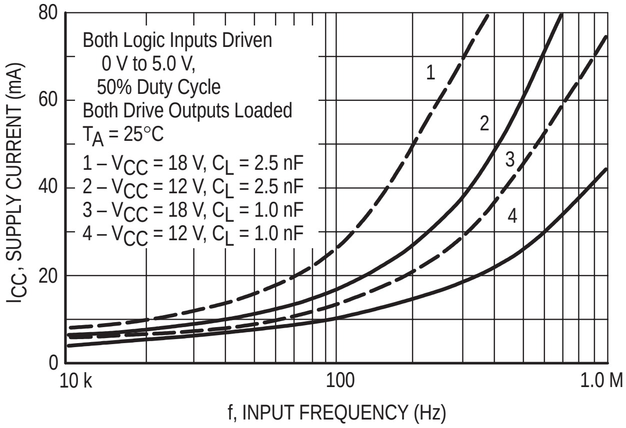
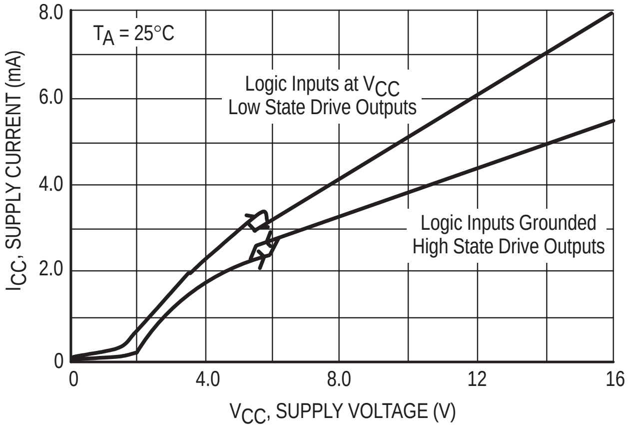


Figure 16. Supply Current versus Supply Voltage



APPLICATIONS INFORMATION

Description

The MC34151 is a dual inverting high speed driver specifically designed to interface low current digital circuitry with power MOSFETs. This device is constructed with Schottky clamped Bipolar Analog technology which offers a high degree of performance and ruggedness in hostile industrial environments.

Input Stage

The Logic Inputs have 170 mV of hysteresis with the input threshold centered at 1.67 V. The input thresholds are insensitive to V_{CC} making this device directly compatible with CMOS and LSTTL logic families over its entire operating voltage range. Input hysteresis provides fast output switching that is independent of the input signal transition time, preventing output oscillations as the input thresholds are crossed. The inputs are designed to accept a signal amplitude ranging from ground to V_{CC}. This allows the output of one channel to directly drive the input of a second channel for master–slave operation. Each input has a 30 kΩ pull–down resistor so that an unconnected open input will cause the associated Drive Output to be in a known high state.

Output Stage

Each totem pole Drive Output is capable of sourcing and sinking up to 1.5 A with a typical 'on' resistance of 2.4 Ω at 1.0 A. The low 'on' resistance allows high output currents to be attained at a lower V_{CC} than with comparative CMOS drivers. Each output has a 100 kΩ pull–down resistor to keep the MOSFET gate low when V_{CC} is less than 1.4 V. No over current or thermal protection has been designed into the device, so output shorting to V_{CC} or ground must be avoided.

Parasitic inductance in series with the load will cause the driver outputs to ring above V_{CC} during the turn–on transition, and below ground during the turn–off transition. With CMOS drivers, this mode of operation can cause a destructive output latch–up condition. The MC34151 is immune to output latch–up. The Drive Outputs contain an internal diode to V_{CC} for clamping positive voltage transients. When operating with V_{CC} at 18 V, proper power supply bypassing must be observed to prevent the output ringing from exceeding the maximum 20 V device rating. Negative output transients are clamped by the internal NPN pull–up transistor. Since full supply voltage is applied across the NPN pull–up during the negative output transient, power dissipation at high frequencies can become excessive. Figures 19, 20, and 21 show a method of using external Schottky diode clamps to reduce driver power dissipation.

Undervoltage Lockout

An undervoltage lockout with hysteresis prevents erratic system operation at low supply voltages. The UVLO forces the Drive Outputs into a low state as V_{CC} rises from 1.4 V to the 5.8 V upper threshold. The lower UVLO threshold is 5.3 V, yielding about 500 mV of hysteresis.

Power Dissipation

Circuit performance and long term reliability are enhanced with reduced die temperature. Die temperature increase is directly related to the power that the integrated circuit must dissipate and the total thermal resistance from the junction to ambient. The formula for calculating the junction temperature with the package in free air is:

$T_J = T_A + P_D\,(R_{\theta JA})$

where: T_J = Junction Temperature
T_A = Ambient Temperature
P_D = Power Dissipation
$R_{\theta JA}$ = Thermal Resistance Junction to Ambient

There are three basic components that make up total power to be dissipated when driving a capacitive load with respect to ground. They are:

$P_D = P_Q + P_C + P_T$

where: P_Q = Quiescent Power Dissipation
P_C = Capacitive Load Power Dissipation
P_T = Transition Power Dissipation

The quiescent power supply current depends on the supply voltage and duty cycle as shown in Figure 16. The device's quiescent power dissipation is:

$$P_Q = V_{CC}\left(I_{CCL}\,(1–D) + I_{CCH}\,(D)\right)$$

where: I_{CCL} = Supply Current with Low State Drive Outputs
I_{CCH} = Supply Current with High State Drive Outputs
D = Output Duty Cycle

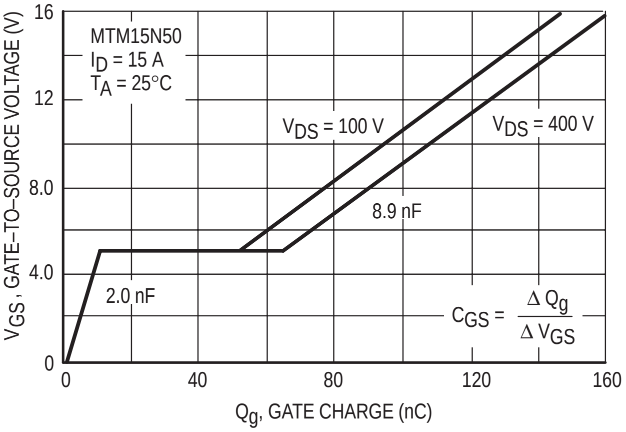
The capacitive load power dissipation is directly related to the load capacitance value, frequency, and Drive Output voltage swing. The capacitive load power dissipation per driver is:

$P_C = V_{CC}\,(V_{OH} – V_{OL})\,C_L\,f$

where: V_{OH} = High State Drive Output Voltage
V_{OL} = Low State Drive Output Voltage
C_L = Load Capacitance
f = frequency

When driving a MOSFET, the calculation of capacitive load power P_C is somewhat complicated by the changing gate to source capacitance C_{GS} as the device switches. To aid in this calculation, power MOSFET manufacturers provide gate charge information on their data sheets. Figure 17 shows a curve of gate voltage versus gate charge for the Motorola MTM15N50. Note that there are three distinct slopes to the curve representing different input capacitance values. To completely switch the MOSFET 'on', the gate must be brought to 10 V with respect to the source. The graph shows that a gate charge Q_g of 110 nC is required when operating the MOSFET with a drain to source voltage V_{DS} of 400 V.

Figure 17. Gate–To–Source Voltage versus Gate Charge



The capacitive load power dissipation is directly related to the required gate charge, and operating frequency. The capacitive load power dissipation per driver is:

$P_{C(MOSFET)} = V_C\,Q_g\,f$

The flat region from 10 nC to 55 nC is caused by the drain–to–gate Miller capacitance, occuring while the MOSFET is in the linear region dissipating substantial amounts of power. The high output current capability of the MC34151 is able to quickly deliver the required gate charge for fast power efficient MOSFET switching. By operating the MC34151 at a higher V_{CC}, additional charge can be provided to bring the gate above 10 V. This will reduce the 'on' resistance of the MOSFET at the expense of higher driver dissipation at a given operating frequency.

The transition power dissipation is due to extremely short simultaneous conduction of internal circuit nodes when the Drive Outputs change state. The transition power dissipation per driver is approximately:

$P_T \approx V_{CC}\,(1.08\,V_{CC}\,C_L\,f – 8 \times 10^{–4})$
P_T must be greater than zero.

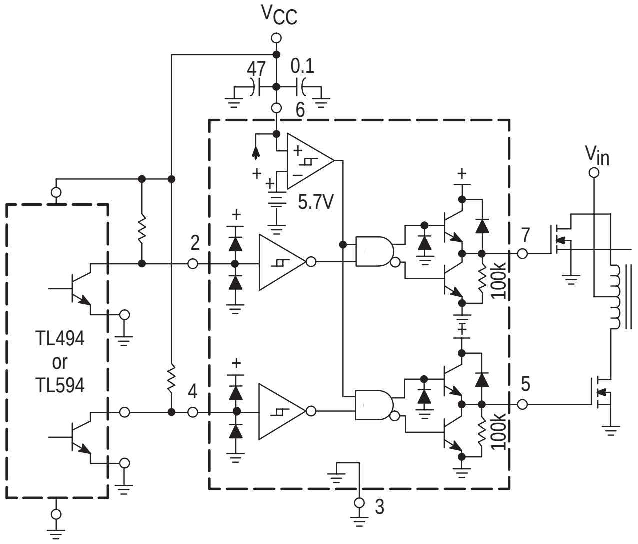
Switching time characterization of the MC34151 is performed with fixed capacitive loads. Figure 13 shows that for small capacitance loads, the switching speed is limited by transistor turn–on/off time and the slew rate of the internal nodes. For large capacitance loads, the switching speed is limited by the maximum output current capability of the integrated circuit.

LAYOUT CONSIDERATIONS

High frequency printed circuit layout techniques are imperative to prevent excessive output ringing and overshoot. **Do not attempt to construct the driver circuit on wire–wrap or plug–in prototype boards.** When driving large capacitive loads, the printed circuit board must contain a low inductance ground plane to minimize the voltage spikes induced by the high ground ripple currents. All high current loops should be kept as short as possible using heavy copper runs to provide a low impedance high frequency path. For optimum drive performance, it is recommended that the initial circuit design contains dual power supply bypass capacitors connected with short leads as close to the V_{CC} pin and ground as the layout will permit. Suggested capacitors are a low inductance 0.1 µF ceramic in parallel with a 4.7 µF tantalum. Additional bypass capacitors may be required depending upon Drive Output loading and circuit layout.

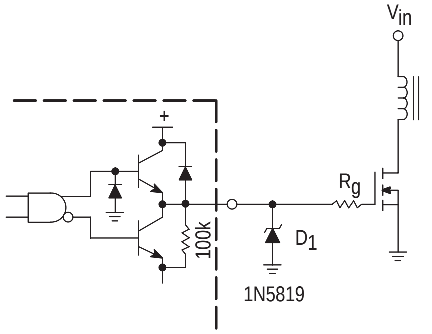
Proper printed circuit board layout is extremely critical and cannot be over emphasized.

Figure 18. Enhanced System Performance with Common Switching Regulators



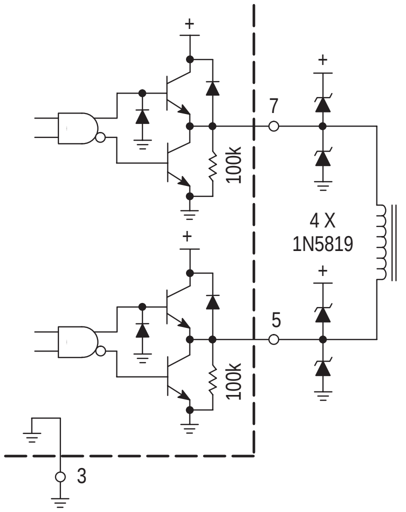
The MC34151 greatly enhances the drive capabilities of common switching regulators and CMOS/TTL logic devices.

Figure 19. MOSFET Parasitic Oscillations



Series gate resistor R_g may be needed to damp high frequency parasitic oscillations caused by the MOSFET input capacitance and any series wiring inductance in the gate–source circuit. R_g will decrease the MOSFET switching speed. Schottky diode D_1 can reduce the driver's power dissipation due to excessive ringing, by preventing the output pin from being driven below ground.

Figure 20. Direct Transformer Drive



Output Schottky diodes are recommended when driving inductive loads at high frequencies. The diodes reduce the driver's power dissipation by preventing the output pins from being driven above V_{CC} and below ground.

Figure 21. Isolated MOSFET Drive

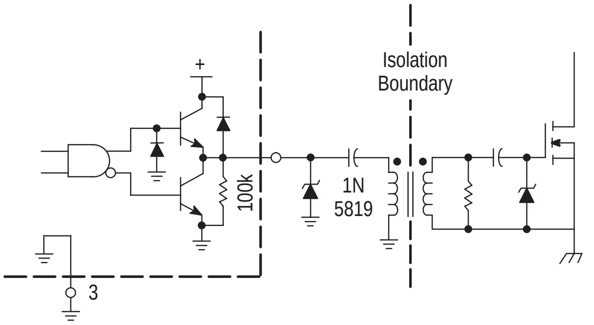
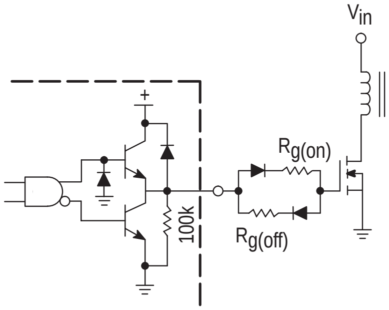
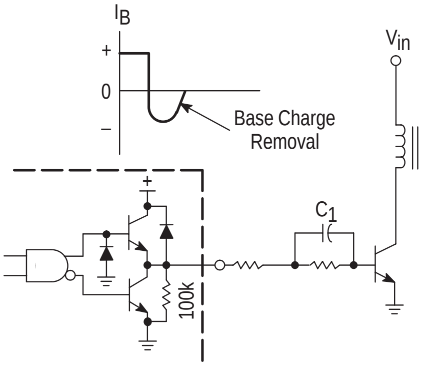


Figure 22. Controlled MOSFET Drive



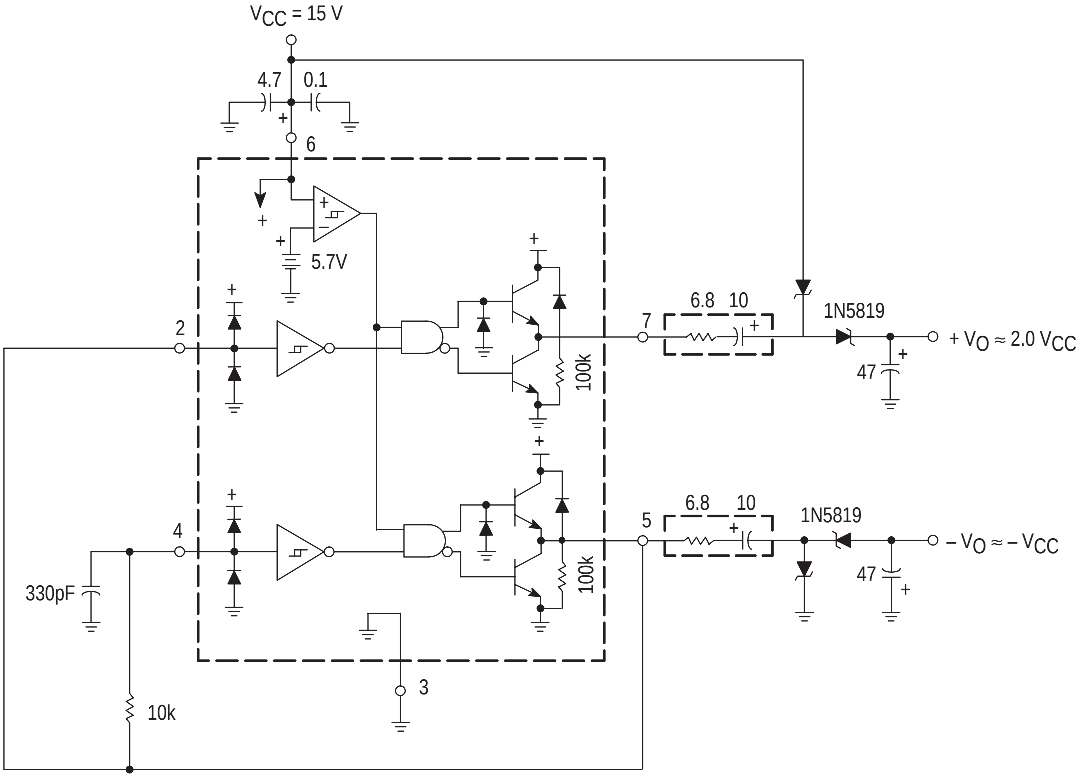
In noise sensitive applications, both conducted and radiated EMI can be reduced significantly by controlling the MOSFET's turn–on and turn–off times.

Figure 23. Bipolar Transistor Drive



The totem–pole outputs can furnish negative base current for enhanced transistor turn–off, with the addition of capacitor C_1.

Figure 24. Dual Charge Pump Converter



The capacitor's equivalent series resistance limits the Drive Output Current to 1.5 A. An additional series resistor may be required when using tantalum or other low ESR capacitors.

Output Load Regulation		
I_O (mA)	$+V_O$ (V)	$–V_O$ (V)
0	27.7	–13.3
1.0	27.4	–12.9
10	26.4	–11.9
20	25.5	–11.2
30	24.6	–10.5
50	22.6	–9.4

MOTOROLA

MC34152
MC33152

High Speed Dual MOSFET Drivers

The MC34152/MC33152 are dual noninverting high speed drivers specifically designed for applications that require low current digital signals to drive large capacitive loads with high slew rates. These devices feature low input current making them CMOS/LSTTL logic compatible, input hysteresis for fast output switching that is independent of input transition time, and two high current totem pole outputs ideally suited for driving power MOSFETs. Also included is an undervoltage lockout with hysteresis to prevent system erratic operation at low supply voltages.

Typical applications include switching power supplies, dc–to–dc converters, capacitor charge pump voltage doublers/inverters, and motor controllers.

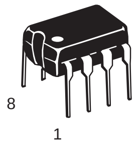
This device is available in dual–in–line and surface mount packages.

- Two Independent Channels with 1.5 A Totem Pole Outputs
- Output Rise and Fall Times of 15 ns with 1000 pF Load
- CMOS/LSTTL Compatible Inputs with Hysteresis
- Undervoltage Lockout with Hysteresis
- Low Standby Current
- Efficient High Frequency Operation
- Enhanced System Performance with Common Switching Regulator Control ICs

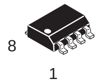
HIGH SPEED DUAL MOSFET DRIVERS

SEMICONDUCTOR TECHNICAL DATA

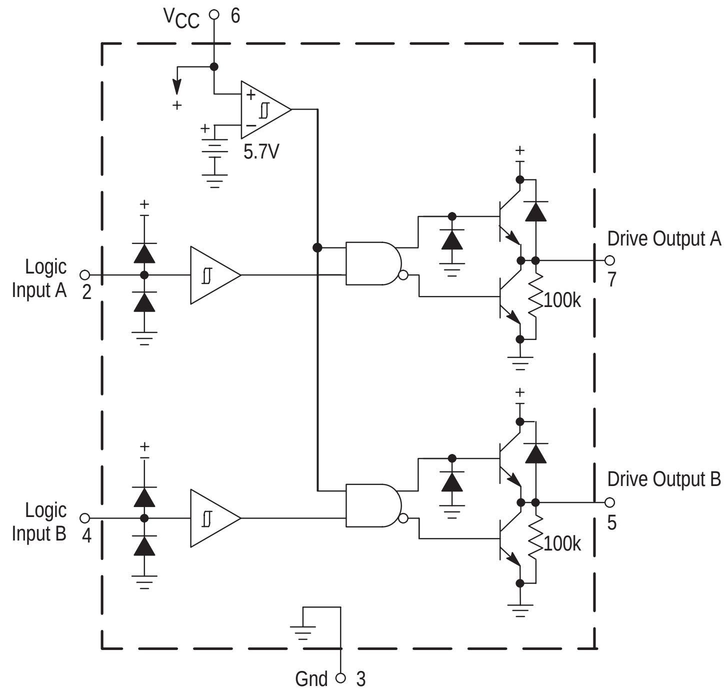
P SUFFIX
PLASTIC PACKAGE
CASE 626



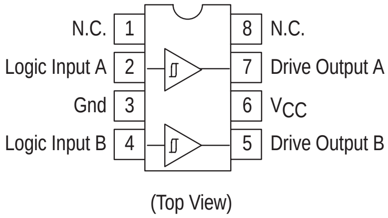
D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)



Representative Diagram



PIN CONNECTIONS



ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC34152D	T_A = 0° to +70°C	SO–8
MC34152P		Plastic DIP
MC33152D	T_A = –40° to +85°C	SO–8
MC33152P		Plastic DIP

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	20	V
Logic Inputs (Note 1)	V_{in}	–0.3 to $+V_{CC}$	V
Drive Outputs (Note 2) Totem Pole Sink or Source Current Diode Clamp Current (Drive Output to V_{CC})	 I_O $I_{O(clamp)}$	 1.5 1.0	A
Power Dissipation and Thermal Characteristics D Suffix, Plastic Package Case 751 Maximum Power Dissipation @ T_A = 50°C Thermal Resistance, Junction–to–Air P Suffix, Plastic Package, Case 626 Maximum Power Dissipation @ T_A = 50°C Thermal Resistance, Junction–to–Air	 P_D $R_{\theta JA}$ P_D $R_{\theta JA}$	 0.56 180 1.0 100	 W °C/W W °C/W
Operating Junction Temperature	T_J	+150	°C
Operating Ambient Temperature MC34152 MC33152	T_A	0 to +70 –40 to +85	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 12 V, for typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies [Note 3], unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
LOGIC INPUTS					
Input Threshold Voltage High State Logic 1 Low State Logic 0	 V_{IH} V_{IL}	 2.6 –	 1.75 1.58	 – 0.9	V
Input Current High State (V_{IH} = 2.6 V) Low State (V_{IL} = 0.8 V)	 I_{IH} I_{IL}	 – –	 100 20	 300 100	μA
DRIVE OUTPUT					
Output Voltage Low State (I_{sink} = 10 mA) (I_{sink} = 50 mA) (I_{sink} = 400 mA) High State (I_{source} = 10 mA) (I_{source} = 50 mA) (I_{source} = 400 mA)	 V_{OL} V_{OH} 	 – – – 10.5 10.4 10	 0.8 1.1 1.8 11.2 11.1 10.8	 1.2 1.5 2.5 – – –	V
Output Pull–Down Resistor	R_{PD}	–	100	–	kΩ
SWITCHING CHARACTERISTICS (T_A = 25°C)					
Propagation Delay (C_L = 1.0 nF) Logic Input to: Drive Output Rise (10% Input to 10% Output) Drive Output Fall (90% Input to 90% Output)	 $t_{PLH\ (IN/OUT)}$ $t_{PHL\ (IN/OUT)}$	 – –	 55 40	 120 120	ns
Drive Output Rise Time (10% to 90%) C_L = 1.0 nF C_L = 2.5 nF	t_r	– –	14 36	30 –	ns
Drive Output Fall Time (90% to 10%) C_L = 1.0 nF C_L = 2.5 nF	t_f	– –	15 32	30 –	ns
TOTAL DEVICE					
Power Supply Current Standby (Logic Inputs Grounded) Operating (C_L = 1.0 nF Drive Outputs 1 and 2, f = 100 kHz)	I_{CC}	 – –	 6.0 10.5	 8.0 15	mA
Operating Voltage	V_{CC}	6.5	–	18	V

NOTES: 1. For optimum switching speed, the maximum input voltage should be limited to 10 V or V_{CC}, whichever is less.
2. Maximum package power dissipation limits must be observed.
3. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
T_{low} = 0°C for MC34152 T_{high} = +70°C for MC34152
= –40°C for MC33152 = +85°C for MC33152

Figure 1. Switching Characteristics Test CIrcuit

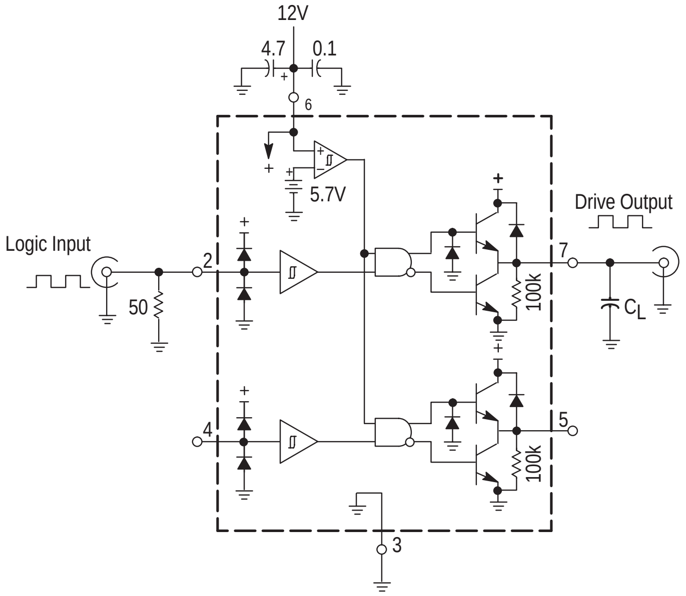


Figure 2. Switching Waveform Definitions

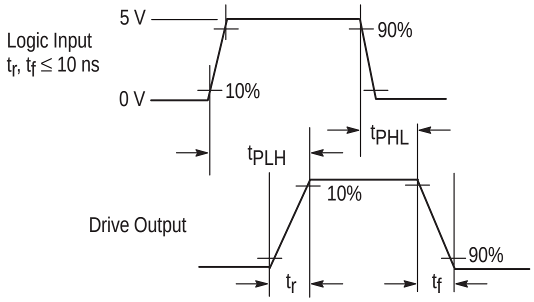


Figure 3. Logic Input Current versus Input Voltage

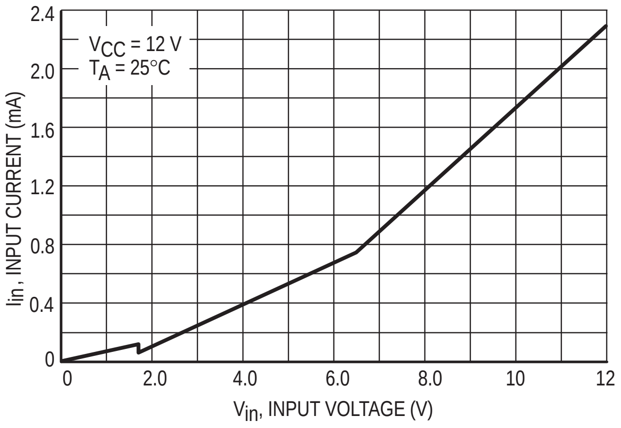


Figure 4. Logic Input Threshold Voltage versus Temperature

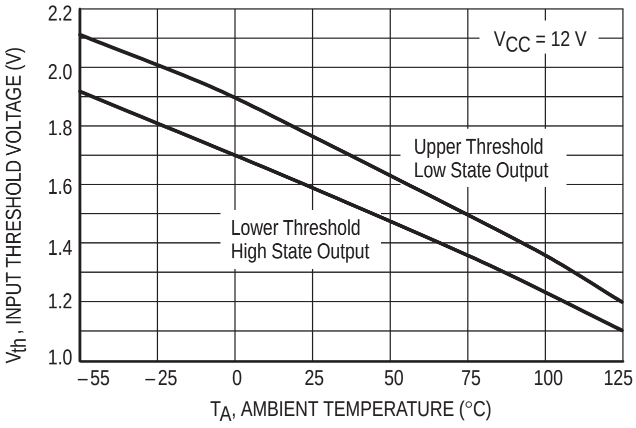


Figure 5. Drive Output High to Low Propagation Delay versus Logic Input Overdrive Voltage

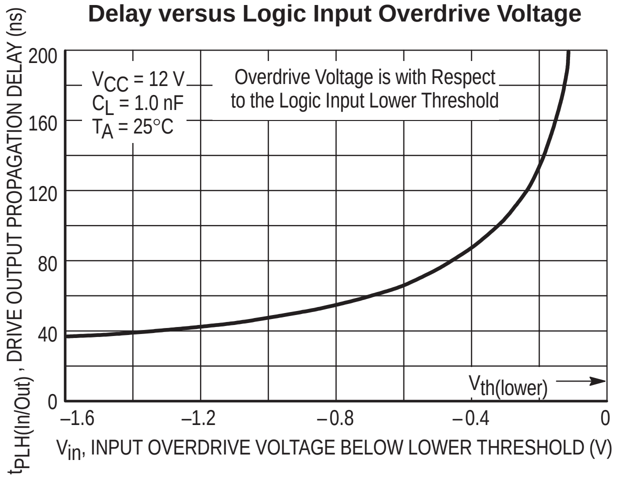


Figure 6. Drive Output Low to High Propagation Delay versus Logic Input Overdrive Voltage

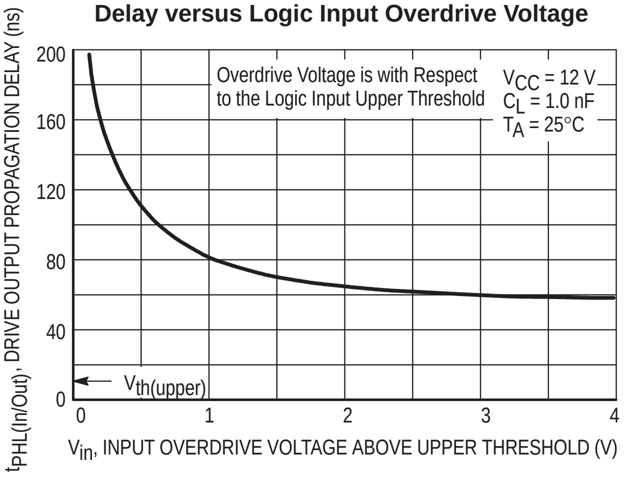


Figure 7. Propagation Delay

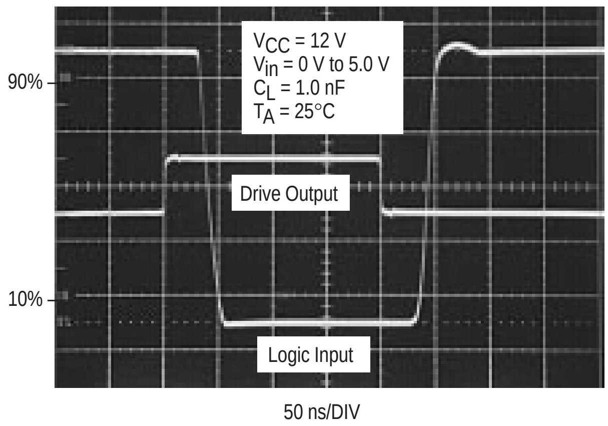


Figure 8. Drive Output Clamp Voltage versus Clamp Current

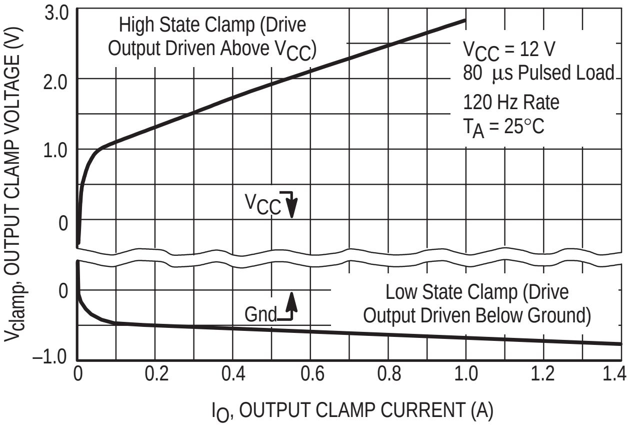


Figure 9. Drive Output Saturation Voltage versus Load Current

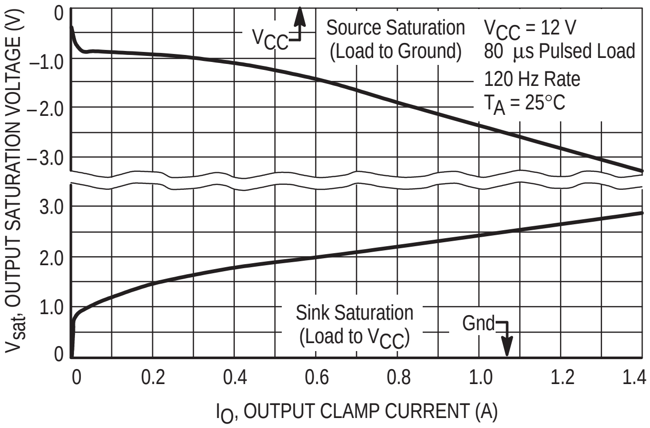


Figure 10. Drive Output Saturation Voltage versus Temperature

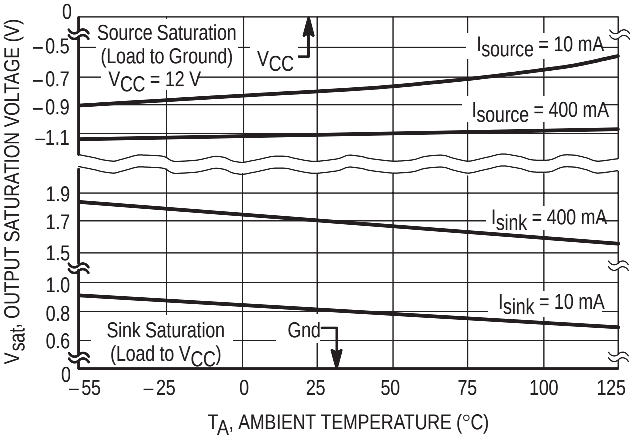


Figure 11. Drive Output Rise Time

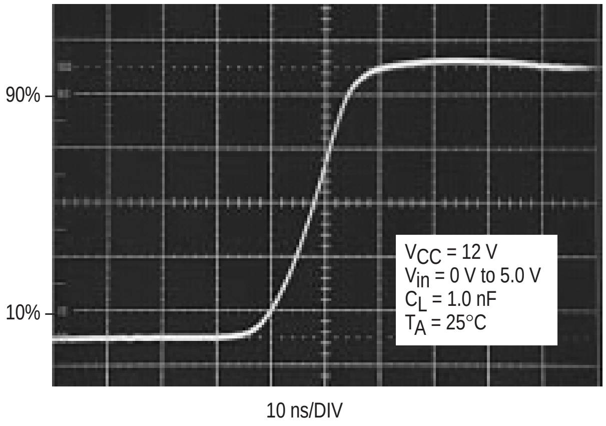


Figure 12. Drive Output Fall Time

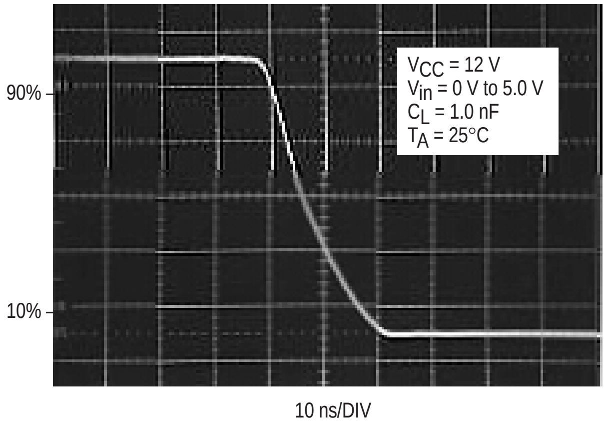


Figure 13. Drive Output Rise and Fall Time versus Load Capacitance

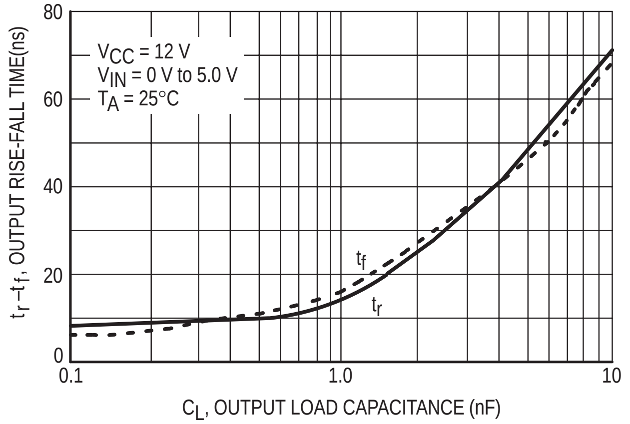


Figure 14. Supply Current versus Drive Output Load Capacitance

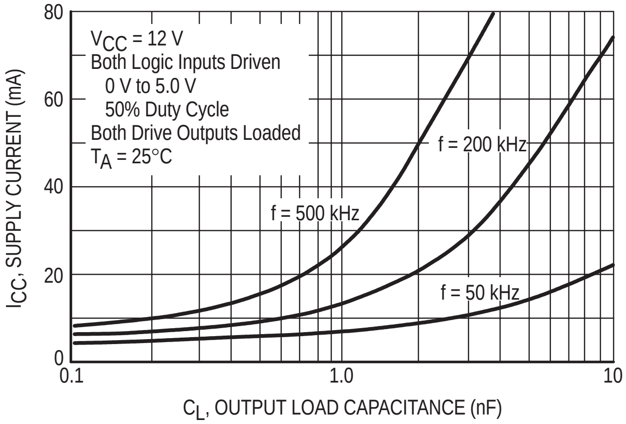


Figure 15. Supply Current versus Input Frequency

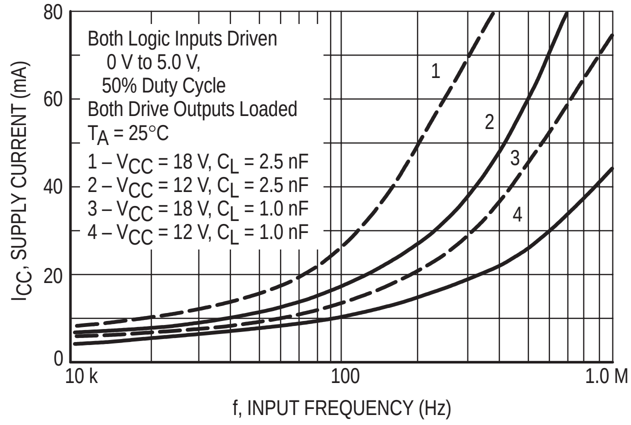
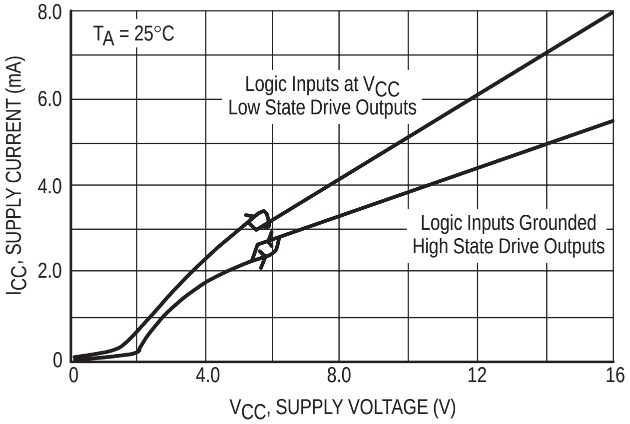


Figure 16. Supply Current versus Supply Voltage



APPLICATIONS INFORMATION

Description

The MC34152 is a dual noninverting high speed driver specifically designed to interface low current digital circuitry with power MOSFETs. This device is constructed with Schottky clamped Bipolar Analog technology which offers a high degree of performance and ruggedness in hostile industrial environments.

Input Stage

The Logic Inputs have 170 mV of hysteresis with the input threshold centered at 1.67 V. The input thresholds are insensitive to V_{CC} making this device directly compatible with CMOS and LSTTL logic families over its entire operating voltage range. Input hysteresis provides fast output switching that is independent of the input signal transition time, preventing output oscillations as the input thresholds are crossed. The inputs are designed to accept a signal amplitude ranging from ground to V_{CC}. This allows the output of one channel to directly drive the input of a second channel for master–slave operation. Each input has a 30 kΩ pull–down resistor so that an unconnected open input will cause the associated Drive Output to be in a known low state.

Output Stage

Each totem pole Drive Output is capable of sourcing and sinking up to 1.5 A with a typical 'on' resistance of 2.4 Ω at 1.0 A. The low 'on' resistance allows high output currents to be attained at a lower V_{CC} than with comparative CMOS drivers. Each output has a 100 kΩ pull–down resistor to keep the MOSFET gate low when V_{CC} is less than 1.4 V. No over current or thermal protection has been designed into the device, so output shorting to V_{CC} or ground must be avoided.

Parasitic inductance in series with the load will cause the driver outputs to ring above V_{CC} during the turn–on transition, and below ground during the turn–off transition. With CMOS drivers, this mode of operation can cause a destructive output latch–up condition. The MC34152 is immune to output latch–up. The Drive Outputs contain an internal diode to V_{CC} for clamping positive voltage transients. When operating with V_{CC} at 18 V, proper power supply bypassing must be observed to prevent the output ringing from exceeding the maximum 20 V device rating. Negative output transients are clamped by the internal NPN pull–up transistor. Since full supply voltage is applied across the NPN pull–up during the negative output transient, power dissipation at high frequencies can become excessive. Figures 19, 20, and 21 show a method of using external Schottky diode clamps to reduce driver power dissipation.

Undervoltage Lockout

An undervoltage lockout with hysteresis prevents erratic system operation at low supply voltages. The UVLO forces the Drive Outputs into a low state as V_{CC} rises from 1.4 V to the 5.8 V upper threshold. The lower UVLO threshold is 5.3 V, yielding about 500 mV of hysteresis.

Power Dissipation

Circuit performance and long term reliability are enhanced with reduced die temperature. Die temperature increase is directly related to the power that the integrated circuit must dissipate and the total thermal resistance from the junction to ambient. The formula for calculating the junction temperature with the package in free air is:

$$T_J = T_A + P_D (R_{\theta JA})$$

where: T_J = Junction Temperature
T_A = Ambient Temperature
P_D = Power Dissipation
$R_{\theta JA}$ = Thermal Resistance Junction to Ambient

There are three basic components that make up total power to be dissipated when driving a capacitive load with respect to ground. They are:

$$P_D = P_Q + P_C + P^T$$

where: P_Q = Quiescent Power Dissipation
P_C = Capacitive Load Power Dissipation
P_T = Transition Power Dissipation

The quiescent power supply current depends on the supply voltage and duty cycle as shown in Figure 16. The device's quiescent power dissipation is:

$$P_Q = V_{CC} (I_{CCL} [1–D] + I_{CCH} [D])$$

where: I_{CCL} = Supply Current with Low State Drive Outputs
I_{CCH} = Supply Current with High State Drive Outputs
D = Output Duty Cycle

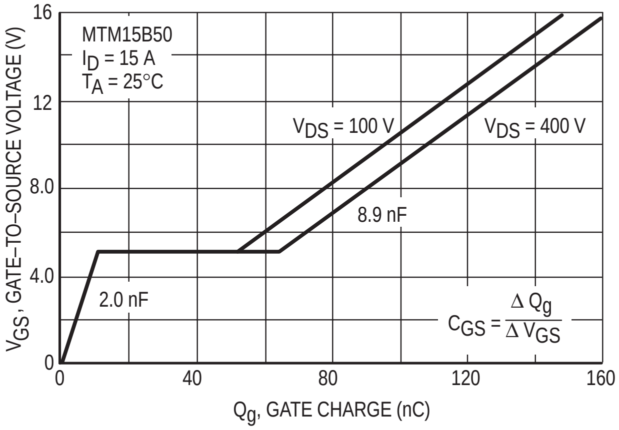
The capacitive load power dissipation is directly related to the load capacitance value, frequency, and Drive Output voltage swing. The capacitive load power dissipation per driver is:

$$P_C = V_{CC} (V_{OH} – V_{OL}) C_L f$$

where: V_{OH} = High State Drive Output Voltage
V_{OL} = Low State Drive Output Voltage
C_L = Load Capacitance
f = Frequency

When driving a MOSFET, the calculation of capacitive load power P_C is somewhat complicated by the changing gate to source capacitance C_{GS} as the device switches. To aid in this calculation, power MOSFET manufacturers provide gate charge information on their data sheets. Figure 17 shows a curve of gate voltage versus gate charge for the Motorola MTM15N50. Note that there are three distinct slopes to the curve representing different input capacitance values. To completely switch the MOSFET 'on,' the gate must be brought to 10 V with respect to the source. The graph shows that a gate charge Q_g of 110 nC is required when operating the MOSFET with a drain to source voltage V_{DS} of 400 V.

Figure 17. Gate–to–Source Voltage versus Gate charge



The capacitive load power dissipation is directly related to the required gate charge, and operating frequency. The capacitive load power dissipation per driver is:

$$P_{C(MOSFET)} = V_{CC}\ Q_g\ f$$

The flat region from 10 nC to 55 nC is caused by the drain–to–gate Miller capacitance, occurring while the MOSFET is in the linear region dissipating substantial amounts of power. The high output current capability of the MC34152 is able to quickly deliver the required gate charge for fast power efficient MOSFET switching. By operating the MC34152 at a higher V_{CC}, additional charge can be provided to bring the gate above 10 V. This will reduce the 'on' resistance of the MOSFET at the expense of higher driver dissipation at a given operating frequency.

The transition power dissipation is due to extremely short simultaneous conduction of internal circuit nodes when the Drive Outputs change state. The transition power dissipation per driver is approximately:

$$P_T \approx V_{CC} (1.08\ V_{CC}\ C_L\ f – 8 \times 10^{–4})$$

P_T must be greater than zero.

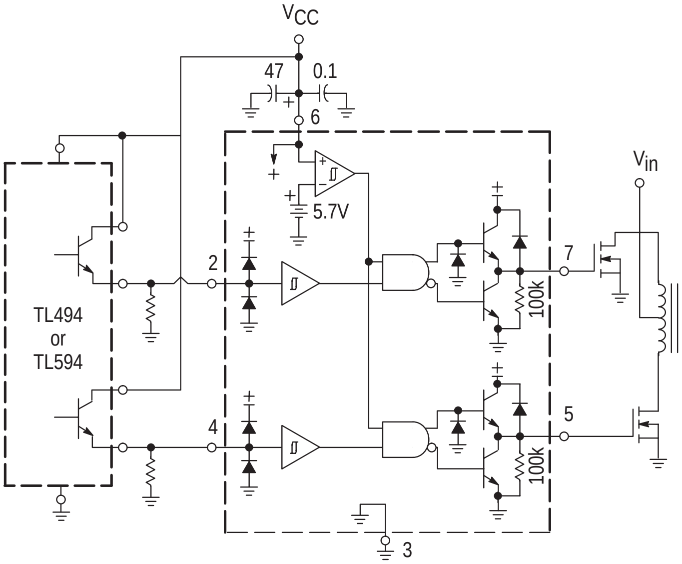
Switching time characterization of the MC34152 is performed with fixed capacitive loads. Figure 13 shows that for small capacitance loads, the switching speed is limited by transistor turn–on/off time and the slew rate of the internal nodes. For large capacitance loads, the switching speed is limited by the maximum output current capability of the integrated circuit.

LAYOUT CONSIDERATIONS

High frequency printed circuit layout techniques are imperative to prevent excessive output ringing and overshoot. **Do not attempt to construct the driver circuit on wire–wrap or plug–in prototype boards.** When driving large capacitive loads, the printed circuit board must contain a low inductance ground plane to minimize the voltage spikes induced by the high ground ripple currents. All high current loops should be kept as short as possible using heavy copper runs to provide a low impedance high frequency path. For optimum drive performance, it is recommended that the initial circuit design contains dual power supply bypass capacitors connected with short leads as close to the V_{CC} pin and ground as the layout will permit. Suggested capacitors are a low inductance 0.1 µF ceramic in parallel with a 4.7 µF tantalum. Additional bypass capacitors may be required depending upon Drive Output loading and circuit layout.

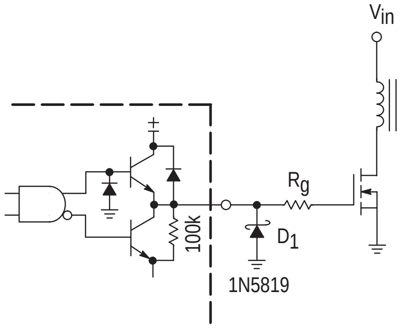
Proper printed circuit board layout is extremely critical and cannot be over emphasized.

Figure 18. Enhanced System Performance with Common Switching Regulators



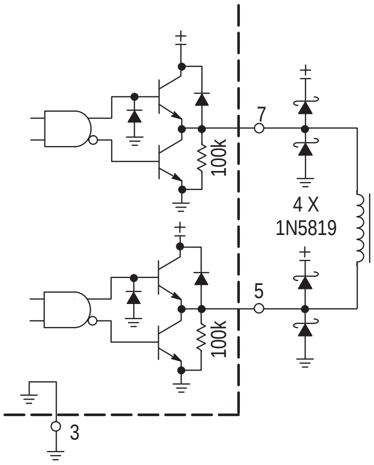
The MC34152 greatly enhances the drive capabilities of common switching regulators and CMOS/TTL logic devices.

Figure 19. MOSFET Parasitic Oscillations



Series gate resistor R_g may be needed to damp high frequency parasitic oscillations caused by the MOSFET input capacitance and any series wiring inductance in the gate–source circuit. R_g will decrease the MOSFET switching speed. Schottky diode D_1 can reduce the driver's power dissipation due to excessive ringing, by preventing the output pin from being driven below ground.

Figure 20. Direct Transformer Drive



Output Schottky diodes are recommended when driving inductive loads at high frequencies. The diodes reduce the driver's power dissipation by preventing the output pins from being driven above V_{CC} and below ground.

Figure 21. Isolated MOSFET Drive

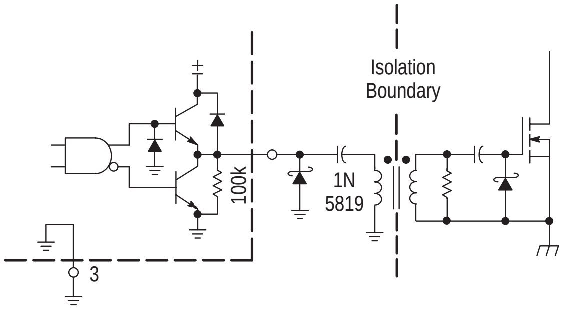
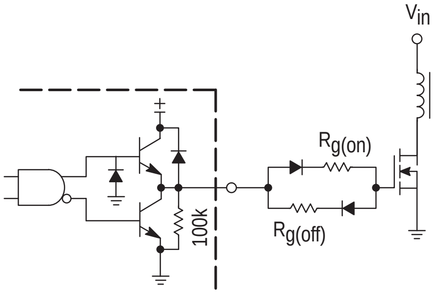
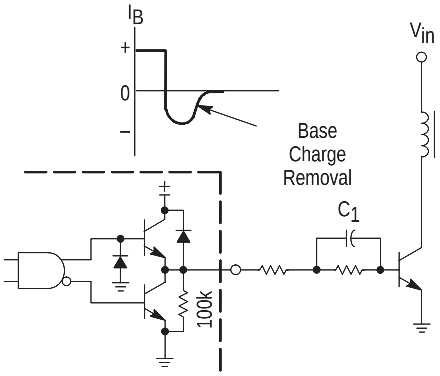


Figure 22. Controlled MOSFET Drive



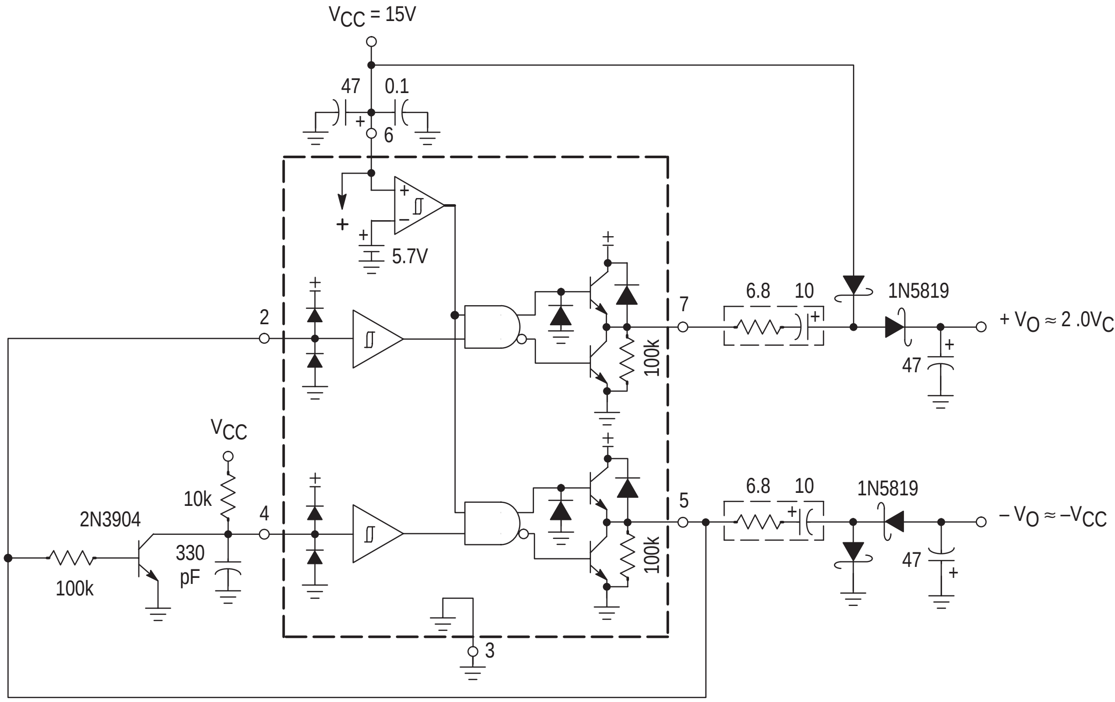
In noise sensitive applications, both conducted and radiated EMI can be reduced significantly by controlling the MOSFET's turn–on and turn–off times.

Figure 23. Bipolar Transistor Drive



The totem–pole outputs can furnish negative base current for enhanced transistor turn–off, with the addition of capacitor C_1.

Figure 24. Dual Charge Pump Converter



The capacitor's equivalent series resistance limits the Drive Output Current to 1.5 A. An additional series resistor may be required when using tantalum or other low ESR capacitors.

Output Load Regulation

I_O (mA)	$+V_O$ (V)	$–V_O$ (V)
0	27.7	–13.3
1.0	27.4	–12.9
10	26.4	–11.9
20	25.5	–11.2
30	24.6	–10.5
50	22.6	–9.4

MC34160
MC33160

Microprocessor Voltage Regulator and Supervisory Circuit

The MC34160 Series is a voltage regulator and supervisory circuit containing many of the necessary monitoring functions required in microprocessor based systems. It is specifically designed for appliance and industrial applications, offering the designer a cost effective solution with minimal external components. These integrated circuits feature a 5.0 V/100 mA regulator with short circuit current limiting, pinned out 2.6 V bandgap reference, low voltage reset comparator, power warning comparator with programmable hysteresis, and an uncommitted comparator ideally suited for microprocessor line synchronization.

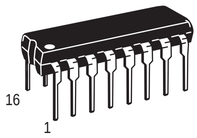
Additional features include a chip disable input for low standby current, and internal thermal shutdown for over temperature protection.

These devices are contained in a 16 pin dual–in–line heat tab plastic package for improved thermal conduction.

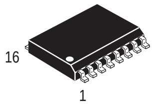
- 5.0 V Regulator Output Current in Excess of 100 mA
- Internal Short Circuit Current Limiting
- Pinned Out 2.6 V Reference
- Low Voltage Reset Comparator
- Power Warning Comparator with Programmable Hysteresis
- Uncommitted Comparator
- Low Standby Current
- Internal Thermal Shutdown Protection
- Heat Tab Power Package

MICROPROCESSOR VOLTAGE REGULATOR/ SUPERVISORY CIRCUIT

SEMICONDUCTOR TECHNICAL DATA

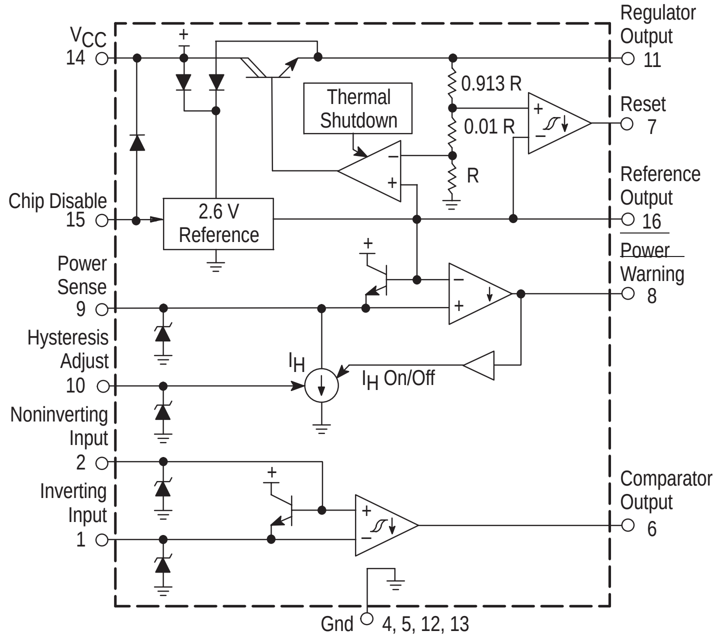


P SUFFIX
PLASTIC PACKAGE
CASE 648C
(DIP–16)



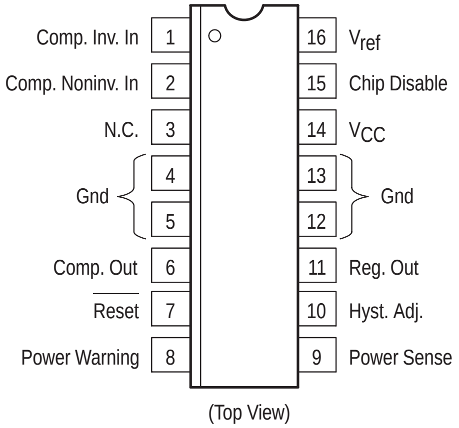
DW SUFFIX
PLASTIC PACKAGE
CASE 751G
(SOP–16L)

Representative Block Diagram



This device contains 72 active transistors.

PIN CONNECTIONS



ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC34160DW	$T_A = 0°$ to $+70°C$	SOP–16L
MC34160P		DIP–16
MC33160DW	$T_A = -40°$ to $+85°C$	SOP–16L
MC33160P		DIP–16

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	40	V
Chip Disable Input Voltage (Pin 15, Note 1)	V_{CD}	–0.3 to V_{CC}	V
Comparator Input Current (Pins 1, 2, 9)	I_{in}	–2.0 to +2.0	mA
Comparator Output Voltage (Pins 6, 7, 8)	V_O	40	V
Comparator Output Sink Current (Pins 6, 7, 8)	I_{Sink}	10	mA
Power Dissipation and Thermal Characteristics			°C/W
P Suffix, Dual–In–Line Case 648C			
Thermal Resistance, Junction–to–Air	$R_{\theta JA}$	80	
Thermal Resistance, Junction–to–Case (Pins 4, 5, 12, 13)	$R_{\theta JC}$	15	
DW Suffix, Surface Mount Case 751G			
Thermal Resistance, Junction–to–Air	$R_{\theta JA}$	94	
Thermal Resistance, Junction–to–Case (Pins 4, 5, 12, 13)	$R_{\theta JC}$	18	
Operating Junction Temperature	T_J	+150	°C
Operating Ambient Temperature	T_A		°C
MC34160		0 to +70	
MC33160		–40 to +85	
Storage Temperature Range	T_{stg}	–65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 30 V, I_O = 10 mA, I_{ref} = 100 µA) For typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies [Notes 2 and 3], unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
REGULATOR SECTION					
Total Output Variation (V_{CC} = 7.0 V to 40 V, I_O = 1.0 mA to 100 mA, T_A = T_{low} to T_{high})	V_O	4.75	5.0	5.25	V
Line Regulation (V_{CC} = 7.0 V to 40 V, T_A = 25°C)	Reg_{line}	–	5.0	40	mV
Load Regulation (I_O = 1.0 V to 100 mA, T_A = 25°C)	Reg_{load}	–	20	50	mV
Ripple Rejection (V_{CC} = 25 V to 35 V, I_O = 40 mA, f = 120 Hz, T_A = 25°C)	RR	50	6.5	–	dB
REFERENCE SECTION					
Total Output Variation (V_{CC} = 7.0 to 40 V, I_O = 0.1 mA to 2.0 mA, T_A = T_{low} to T_{high})	V_{ref}	2.47	2.6	2.73	V
Line Regulation (V_{CC} = 5.0 V to 40 V, T_A = 25°C)	Reg_{line}	–	2.0	20	mV
Load Regulation (I_O = 0.1 mA to 2.0 mA, T_A = 25°C)	Reg_{load}	–	4.0	30	mV
RESET COMPARATOR					
Threshold Voltage					V
High State Output (Pin 11 Increasing)	V_{IH}	–	(V_O–0.11)	(V_O–0.05)	
Low State Output (Pin 11 Decreasing)	V_{IL}	4.55	(V_O–0.18)	–	
Hysteresis	V_H	0.02	0.07	–	
Output Sink Saturation (V_{CC} = 4.5 V, I_{Sink} = 2.0 mA)	V_{OL}	–	–	0.4	V
Output Off–State Leakage (V_{OH} = 40 V)	I_{OH}	–	–	4.0	µA

NOTES: 1. The maximum voltage range is –0.3 V to V_{CC} or +35 V, whichever is less.
2. T_{low} = 0°C for MC34160 –40°C for MC33160; T_{high} = 70°C for MC34160 85°C for MC33160
3. Low duty cycle pulse testing techniques are used during test to maintain junction temperature as close to ambient as possible.

ELECTRICAL CHARACTERISTICS (continued) (V_{CC} = 30 V, I_O = 10 mA, I_{ref} = 100 µA) For typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies [Notes 2 and 3], unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
POWER WARNING COMPARATOR					
Input Offset Voltage	V_{IO}	–	1.2	10	mV
Input Bias Current ($V_{Pin\ 9}$ = 3.0 V)	I_{IB}	–	–	0.5	µA
Input Hysteresis Current ($V_{Pin\ 9}$ = V_{ref} – 100 mV) $R_{Pin\ 10}$ = 24 k $R_{Pin\ 10}$ = ∞	I_H	 40 4.5	 50 7.5	 60 11	µA
Output Sink Saturation (I_{Sink} = 2.0 mA)	V_{OL}	–	0.13	0.4	V
Output Off–State Leakage (V_{OH} = 40 V)	I_{OH}	–	–	4.0	µA
UNCOMMITTED COMPARATOR					
Input Offset Voltage (Output Transition Low to High)	V_{IO}	–	–	20	mV
Input Hysteresis Voltage (Output Transition High to Low)	I_H	140	200	260	mV
Input Bias Current ($V_{Pin\ 1,\ 2}$ = 2.6 V)	I_{IB}	–	–	–1.0	µA
Input Common Mode Voltage Range	V_{ICR}	0.6 to 5.0	–	–	V
Output Sink Saturation (I_{Sink} = 2.0 mA)	V_{OL}	–	0.13	0.4	V
Output Off–State Leakage (V_{OH} = 40 V)	I_{OH}	–	–	4.0	µA
TOTAL DEVICE					
Chip Disable Threshold Voltage (Pin 15) High State (Chip Disabled) Low State (Chip Enabled)	 V_{IH} V_{IL}	 2.5 –	 – –	 – 0.8	V
Chip Disable Input Current (Pin 15) High State (V_{in} = 2.5 V) Low State (V_{in} = 0.8 V)	 I_{IH} I_{IL}	 – –	 – –	 100 30	µA
Chip Disable Input Resistance (Pin 15)	R_{in}	50	100	–	kΩ
Operating Voltage Range V_O (Pin 11) Regulated V_{ref} (Pin 16) Regulated	V_{CC}	 7.0 to 40 5.0 to 40	 – –	 – –	V
Power Supply Current Standby (Chip Disable High State) Operating (Chip Disable Low State)	I_{CC}	 – –	 0.18 1.5	 0.35 3.0	mA

NOTES: 1. The maximum voltage range is –0.3 V to V_{CC} or +35 V, whichever is less.
2. T_{low} = 0°C for MC34160 –40°C for MC33160; T_{high} = 70°C for MC34160 85°C for MC33160
3. Low duty cycle pulse testing techniques are used during test to maintain junction temperature as close to ambient as possible.

Figure 1. Regulator Output Voltage Change versus Source Current

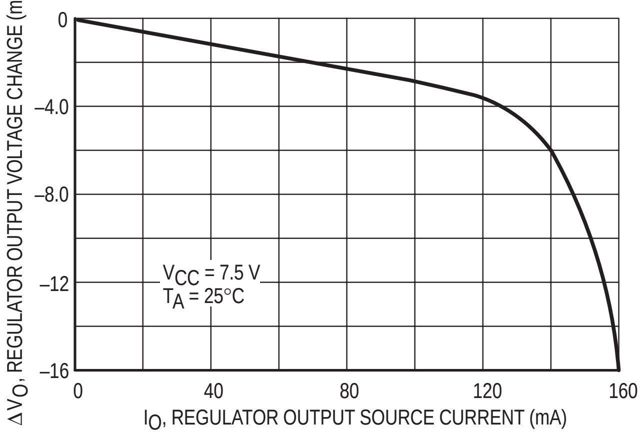


Figure 2. Reference and Regulator Output versus Supply Voltage

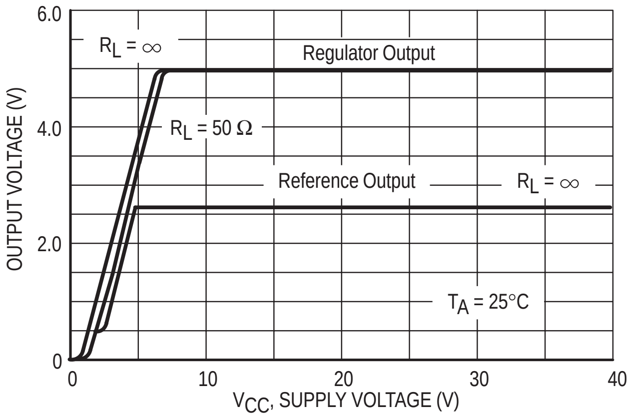


Figure 3. Reference Output Voltage Change versus Source Current

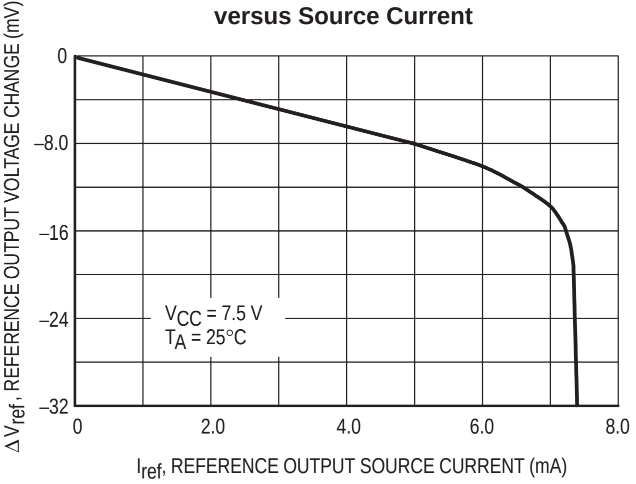


Figure 4. Power Warning Hysteresis Current versus Programming Resistor

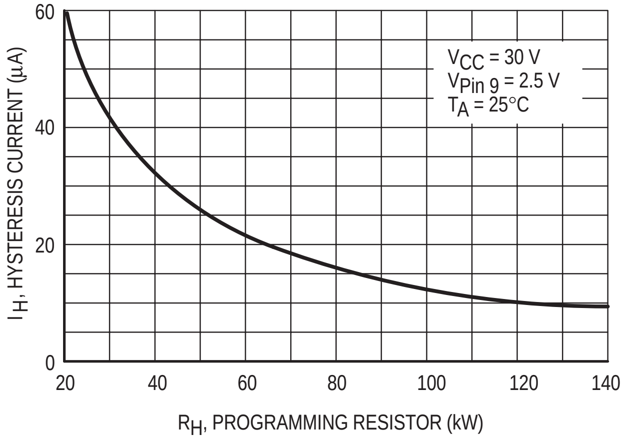


Figure 5. Power Warning Comparator Delay versus Temperature

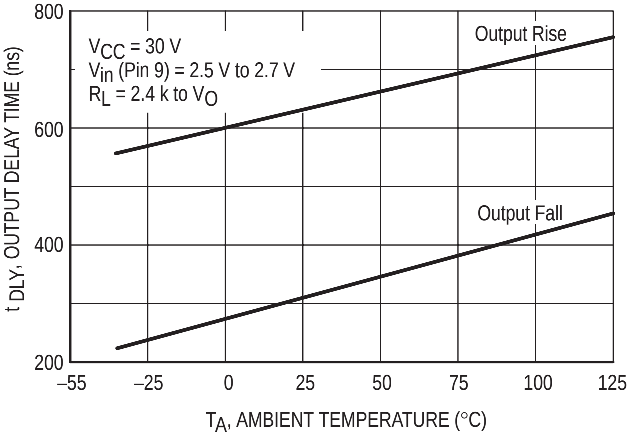


Figure 6. Uncommitted Comparator Delay versus Temperature

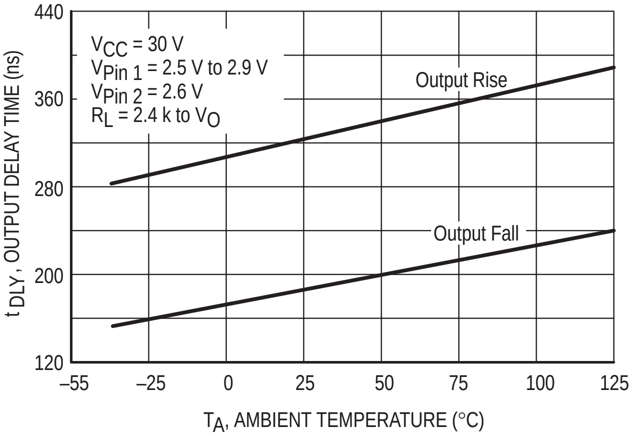


Figure 7. Comparator Output Saturation versus Sink Current

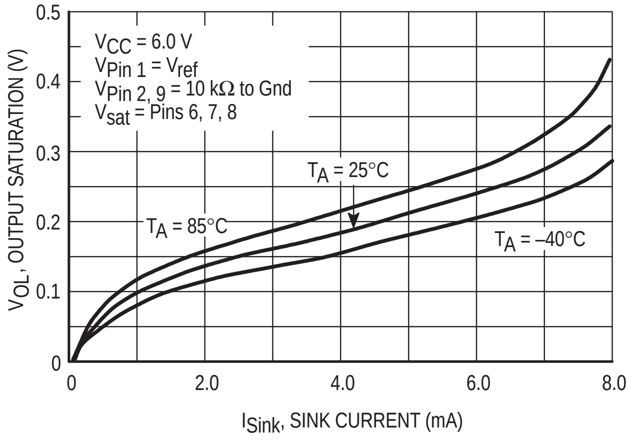


Figure 8. P Suffix (DIP–16) Thermal Resistance and Maximum Power DIssipation versus P.C.B. Copper Length

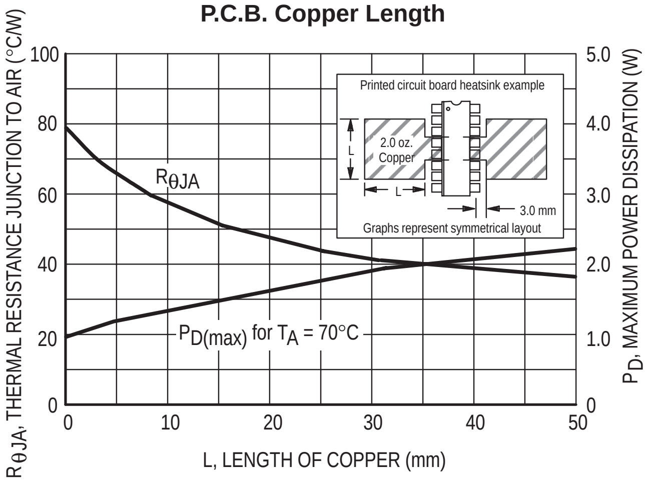
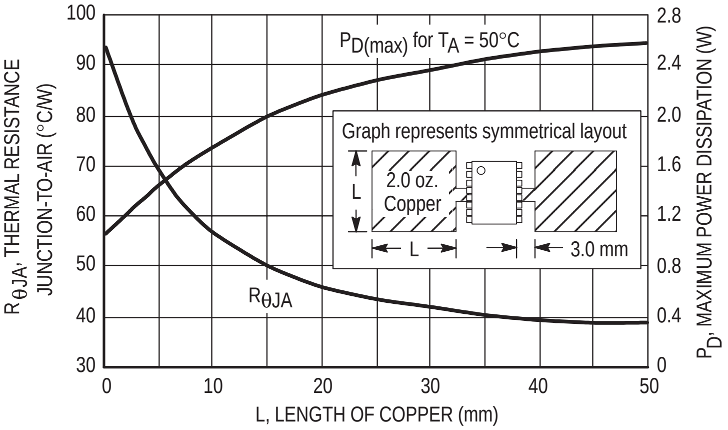


Figure 9. DW Suffix (SOP–16L) Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length



PIN FUNCTION DESCRIPTION

Pin	Function	Description
1	Comparator Inverting Input	This is the Uncommitted Comparator Inverting input. It is typically connected to a resistor divider to monitor a voltage.
2	Comparator Noninverting Input	This is the Uncommitted Comparator Noninverting input. It is typically connected to a reference voltage.
3	N.C.	No connection. This pin is not internally connected.
4, 5, 12, 13	Gnd	These pins are the control circuit grounds and are connected to the source and load ground returns. They are part of the IC lead frame and can be used for heatsinking.
6	Comparator Output	This is the Uncommitted Comparator output. It is an open collector sink–only output requiring a pull–up resistor.
7	Reset	This is the Reset Comparator output. It is an open collector sink–only output requiring a pull–up resistor.
8	Power Warning	This is the Power Warning Comparator output. It is an open collector sink–only output requiring a pull–up resistor.
9	Power Sense	This is the Power Warning Comparator noninverting input. It is typically connected to a resistor divider to monitor the input power source voltage.
10	Hysteresis Adjust	The Power Warning Comparator hysteresis is programmed by a resistor connected from this pin to ground.
11	Regulator Output	This is the 5.0 V Regulator output.
14	V_{CC}	This pin is the positive supply input of the control IC.
15	Chip Disable	This input is used to switch the IC into a standby mode turning off all outputs.
16	V_{ref}	This is the 2.6 V Reference output. It is intended to be used in conjunction with the Power Warning and Uncommitted comparators.

OPERATING DESCRIPTION

The MC34160 series is a monolithic voltage regulator and supervisory circuit containing many of the necessary monitoring functions required in microprocessor based systems. It is specifically designed for appliance and industrial applications, offering the designer a cost effective solution with minimal external components. These devices are specified for operation over an input voltage of 7.0 V to 40 V, and with a junction temperature of –40° to +150°C. A typical microprocessor application is shown in Figure 10.

Regulator

The 5.0 V regulator is designed to source in excess of 100 mA output current and is short circuit protected. The output has a guaranteed tolerance of ±5.0% over line, load, and temperature. Internal thermal shutdown circuitry is included to limit the maximum junction temperature to a safe level. When activated, typically at 170°C, the regulator output turns off.

In specific situations a combination of input and output bypass capacitors may be required for regulator stability. If the regulator is located an appreciable distance (≥ 4″) from the supply filter, an input bypass capacitor (C_{in}) of 0.33 μF or greater is suggested. Output capacitance values of less than 5.0 nF may cause regulator instability at light load (≤ 1.0 mA) and cold temperature. An output bypass capacitor of 0.1 μF or greater is recommended to ensure stability under all load conditions. The capacitors selected must provide good high frequency characteristics.

Good construction techniques should be used to minimize ground loops and lead resistance drops since the regulator does not have external sense inputs.

Reference

The 2.6 V bandgap reference is short circuit protected and has a guaranteed output tolerance of ±5.0% over line, load, and temperature. It is intended to be used in conjunction with the Power Warning and Uncommitted comparator. The reference can source in excess of 2.0 mA and sink a maximum of 10 µA. For additional current sinking capability, an external load resistor to ground must be used.

Reference biasing is internally derived from either V_{CC} or V_O, allowing proper operation if either drops below nominal.

Chip Disable

This input is used to switch the IC into a standby mode. When activated, internal biasing for the entire die is removed causing all outputs to turn off. This reduces the power supply current (I_{CC}) to less than 0.3 mA.

Comparators

Three separate comparators are incorporated for voltage monitoring. Their outputs can provide diagnostic information to the microprocessor, preventing system malfunctions.

The Reset Comparator Inverting Input is internally connected to the 2.6 V reference while the Noninverting Input monitors V_O. The Reset Output is active low when V_O falls approximately 180 mV below its regulated voltage. To prevent erratic operation when crossing the comparator threshold, 70 mV of hysteresis is provided.

The Power Warning Comparator is typically used to detect an impending loss of system power. The Inverting Input is internally connected to the reference, fixing the threshold at 2.6 V. The input power source V_{in} is monitored by the Noninverting Input through the R_1/R_2 divider (Figure 10). This input features an adjustable 10 µA to 50 µA current sink I_H that is programmed by the value selected for resistor R_H. A default current of 6.5 µA is provided if R_H is omitted. When the comparator input falls below 2.6 V, the current sink is activated. This produces hysteresis if V_{in} is monitored through a series resistor (R_1). The comparator thresholds are defined as follows:

$$V_{th(lower)} = V_{ref}\left(1 + \frac{R1}{R_2}\right) - I_{IB}\,R_1$$

$$V_{th(upper)} = V_{ref}\left(1 + \frac{R1}{R_2}\right) + I_H\,R_1$$

The nominal hysteresis current I_H equals 1.2 V/R_H (Figure 4).

The Uncommitted Comparator can be used to synchronize the microprocessor with the ac line signal for timing functions, or for synchronous load switching. It can also be connected as a line loss detector as shown in Figure 11. The comparator contains 200 mV of hysteresis preventing erractic output behavior when crossing the input threshold.

The Power Warning and Uncommitted Comparators each have a transistor base–emitter connected across their inputs. The base input normally connects to a voltage reference while the emitter input connects to the voltage to be monitored. The transistor limits the negative excursion on the emitter input to – 0.7 V below the base input by supply current from V_{CC}. This clamp current will prevent forward biasing the IC substrate. Zener diodes are connected to the comparator inputs to enhance the ICs electrostatic discharge capability. Resistors R_1 and R_{in} must limit the input current to a maximum of ±2.0 mA.

Each comparator output consists of an open collector NPN transistor capable of sinking 2.0 mA with a saturation voltage less than 0.4 V, and standing off 40 V with minimal leakage. Internal bias for the Reset and Power Warning Comparators is derived from either V_{CC} or the regulator output to ensure functionality when either is below nominal.

Heat Tab Package

The MC34160 is contained in a 16 lead plastic dual–in–line package in which the die is mounted on a special Heat Tab copper alloy lead frame. This tab consists of the four center ground pins that are specifically designed to improve thermal conduction from the die to the surrounding air. The pictorial in Figure 8 shows a simple but effective method of utilizing the printed circuit board medium as a heat dissipator by soldering these tabs to an adequate area of copper foil. This permits the use of standard board layout and mounting practices while having the ability to more than halve the junction to air thermal resistance. The example and graph are for a symmetrical layout on a single sided board with one ounce per square foot copper.

Figure 10. Typical Microprocessor Application

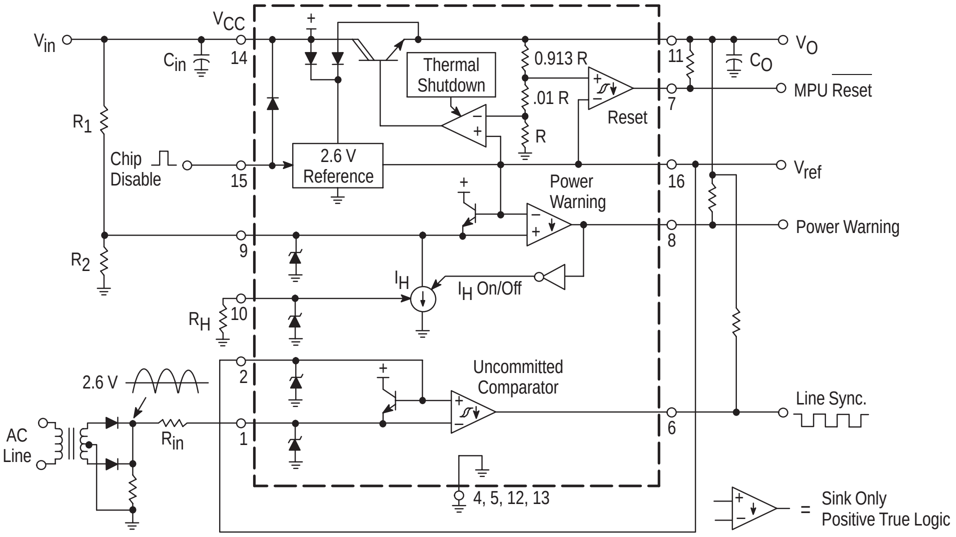
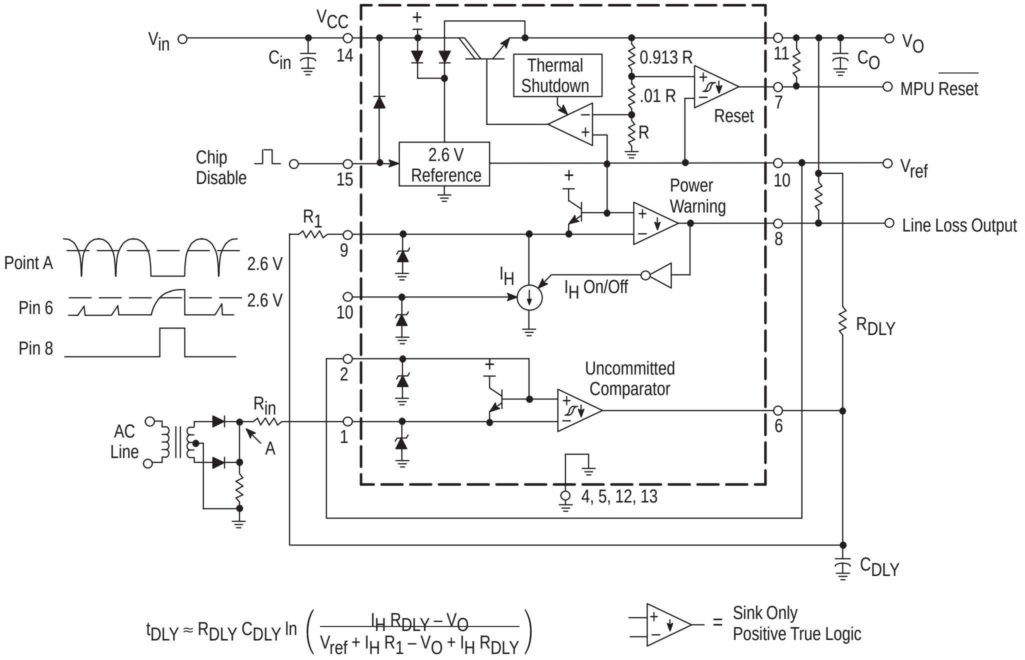
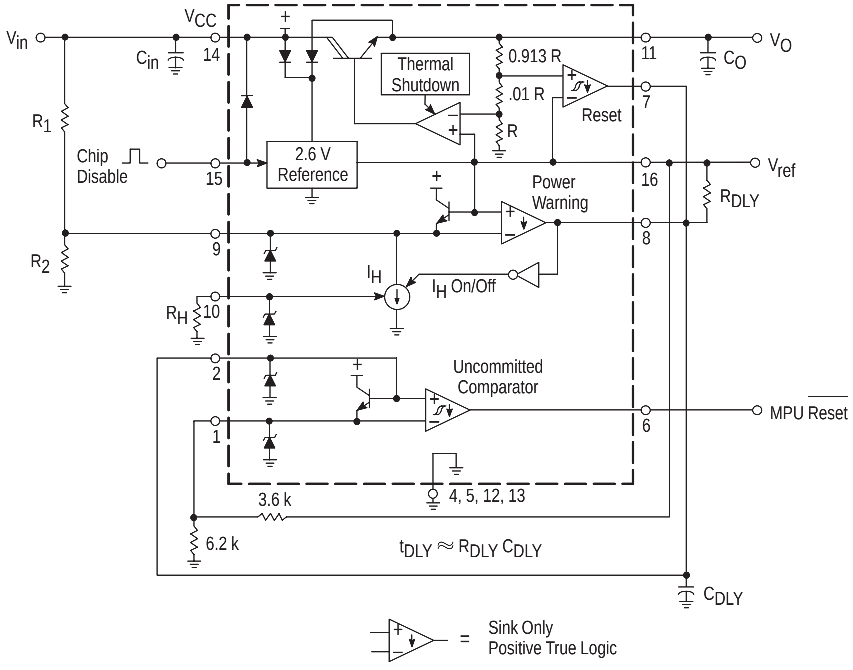


Figure 11. Line Loss Detector Application



$$t_{DLY} \approx R_{DLY}\,C_{DLY}\ln\left(\frac{I_H R_{DLY} - V_O}{V_{ref} + I_H R_1 - V_O + I_H R_{DLY}}\right)$$

Figure 12. Time Delayed Microprocessor Reset



$t_{DLY} \approx R_{DLY}\,C_{DLY}$

MOTOROLA

MC34161
MC33161

Universal Voltage Monitors

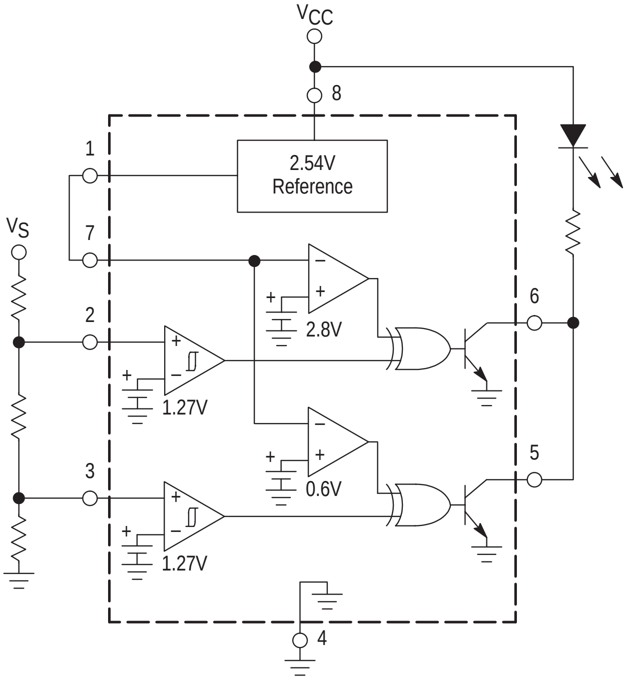
The MC34161/MC33161 are universal voltage monitors intended for use in a wide variety of voltage sensing applications. These devices offer the circuit designer an economical solution for positive and negative voltage detection. The circuit consists of two comparator channels each with hysteresis, a unique Mode Select Input for channel programming, a pinned out 2.54 V reference, and two open collector outputs capable of sinking in excess of 10 mA. Each comparator channel can be configured as either inverting or noninverting by the Mode Select Input. This allows over, under, and window detection of positive and negative voltages. The minimum supply voltage needed for these devices to be fully functional is 2.0 V for positive voltage sensing and 4.0 V for negative voltage sensing.

Applications include direct monitoring of positive and negative voltages used in appliance, automotive, consumer, and industrial equipment.

- Unique Mode Select Input Allows Channel Programming
- Over, Under, and Window Voltage Detection
- Positive and Negative Voltage Detection
- Fully Functional at 2.0 V for Positve Voltage Sensing and 4.0 V for Negative Voltage Sensing
- Pinned Out 2.54 V Reference with Current Limit Protection
- Low Standby Current
- Open Collector Outputs for Enhanced Device Flexibility

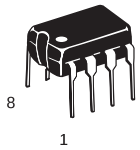
Simplified Block Diagram

(Positive Voltage Window Detector Application)

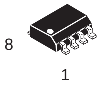


UNIVERSAL VOLTAGE MONITORS

SEMICONDUCTOR TECHNICAL DATA

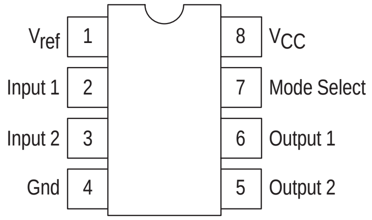


P SUFFIX
PLASTIC PACKAGE
CASE 626



D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

PIN CONNECTIONS



(TOP VIEW)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC34161D	T_A = 0° to +70°C	SO–8
MC34161P		Plastic DIP
MC33161D	T_A = –40° to +85°C	SO–8
MC33161P		Plastic DIP

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Input Voltage	V_{CC}	40	V
Comparator Input Voltage Range	V_{in}	– 1.0 to +40	V
Comparator Output Sink Current (Pins 5 and 6) (Note 1)	I_{Sink}	20	mA
Comparator Output Voltage	V_{out}	40	V
Power Dissipation and Thermal Characteristics (Note 1)			
P Suffix, Plastic Package, Case 626			
Maximum Power Dissipation @ T_A = 70°C	P_D	800	mW
Thermal Resistance, Junction–to–Air	$R_{\theta JA}$	100	°C/W
D Suffix, Plastic Package, Case 751			
Maximum Power Dissipation @ T_A = 70°C	P_D	450	mW
Thermal Resistance, Junction–to–Air	$R_{\theta JA}$	178	°C/W
Operating Junction Temperature	T_J	+150	°C
Operating Ambient Temperature (Note 3)	T_A		°C
MC34161		0 to +70	
MC33161		– 40 to +85	
Storage Temperature Range	T_{stg}	– 55 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, for typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies [Notes 2 and 3], unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
COMPARATOR INPUTS					
Threshold Voltage, V_{in} Increasing (T_A = 25°C) (T_A = T_{min} to T_{max})	V_{th}	1.245 1.235	1.27 –	1.295 1.295	V
Threshold Voltage Variation (V_{CC} = 2.0 V to 40 V)	ΔV_{th}	–	7.0	15	mV
Threshold Hysteresis, V_{in} Decreasing	V_H	15	25	35	mV
Threshold Difference $\lvert V_{th1} - V_{th2} \rvert$	V_D	–	1.0	15	mV
Reference to Threshold Difference ($V_{ref} - V_{in1}$), ($V_{ref} - V_{in2}$)	V_{RTD}	1.20	1.27	1.32	V
Input Bias Current (V_{in} = 1.0 V) (V_{in} = 1.5 V)	I_{IB}	– –	40 85	200 400	nA
MODE SELECT INPUT					
Mode Select Threshold Voltage (Figure 5) Channel 1 Channel 2	$V_{th(CH\ 1)}$ $V_{th(CH\ 2)}$	V_{ref}+0.15 0.3	V_{ref}+0.23 0.63	V_{ref}+0.30 0.9	V
COMPARATOR OUTPUTS					
Output Sink Saturation Voltage (I_{Sink} = 2.0 mA) (I_{Sink} = 10 mA) (I_{Sink} = 0.25 mA, V_{CC} = 1.0 V)	V_{OL}	– – –	0.05 0.22 0.02	0.3 0.6 0.2	V
Off–State Leakage Current (V_{OH} = 40 V)	I_{OH}	–	0	1.0	µA
REFERENCE OUTPUT					
Output Voltage (I_O = 0 mA, T_A = 25°C)	V_{ref}	2.48	2.54	2.60	V
Load Regulation (I_O = 0 mA to 2.0 mA)	Reg_{load}	–	0.6	15	mV
Line Regulation (V_{CC} = 4.0 V to 40 V)	Reg_{line}	–	5.0	15	mV
Total Output Variation over Line, Load, and Temperature	ΔV_{ref}	2.45	–	2.60	V
Short Circuit Current	I_{SC}	–	8.5	30	mA
TOTAL DEVICE					
Power Supply Current (V_{Mode}, V_{in1}, V_{in2} = Gnd) (V_{CC} = 5.0 V) (V_{CC} = 40 V)	I_{CC}	– –	450 560	700 900	µA
Operating Voltage Range (Positive Sensing) (Negative Sensing)	V_{CC}	2.0 4.0	– –	40 40	V

NOTES: 1. Maximum package power dissipation must be observed.
2. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
3. T_{low} = 0°C for MC34161 T_{high} = +70°C for MC34161
–40°C for MC33161 +85°C for MC33161

Figure 1. Comparator Input Threshold Voltage

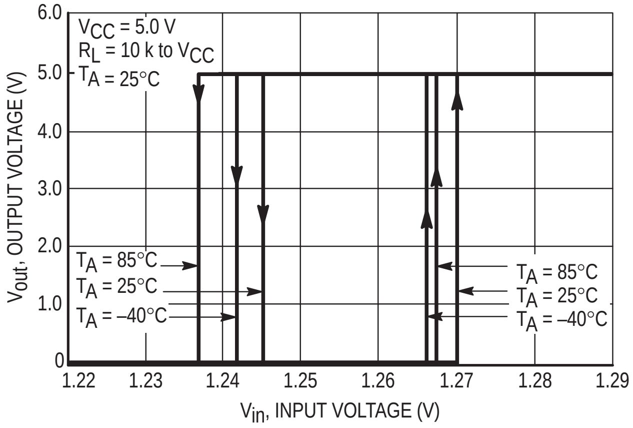


Figure 2. Comparator Input Bias Current versus Input Voltage

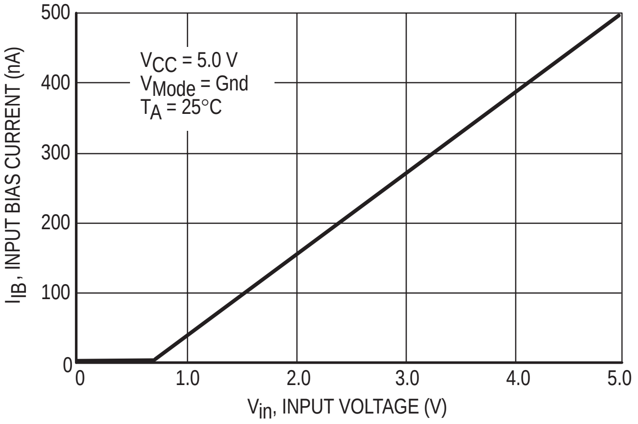


Figure 3. Output Propagation Delay Time versus Percent Overdrive

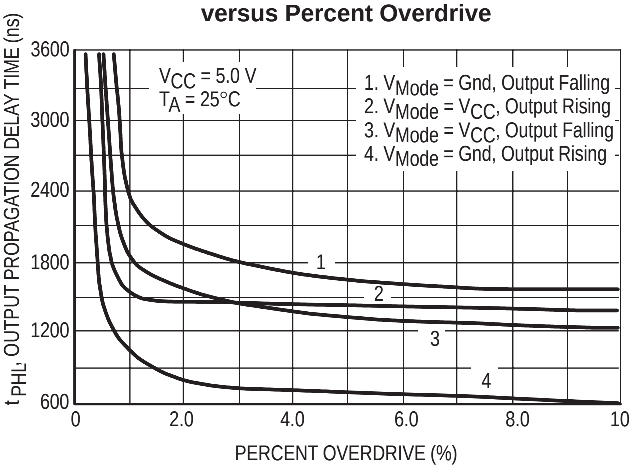


Figure 4. Output Voltage versus Supply Voltage

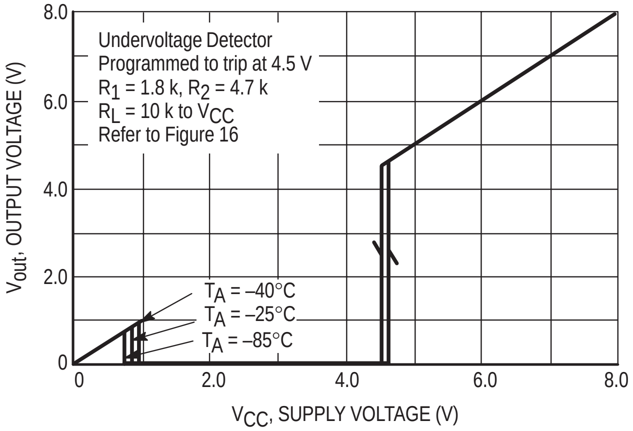


Figure 5. Mode Select Thresholds

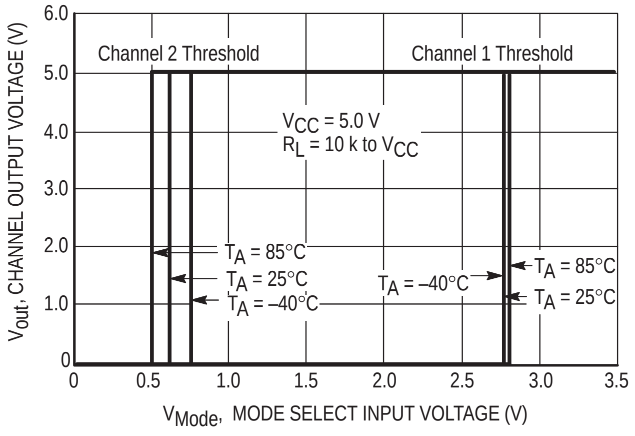


Figure 6. Mode Select Input Current versus Input Voltage

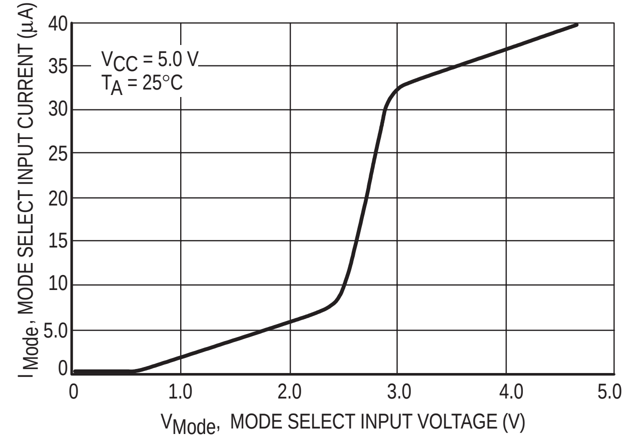


Figure 7. Reference Voltage versus Supply Voltage

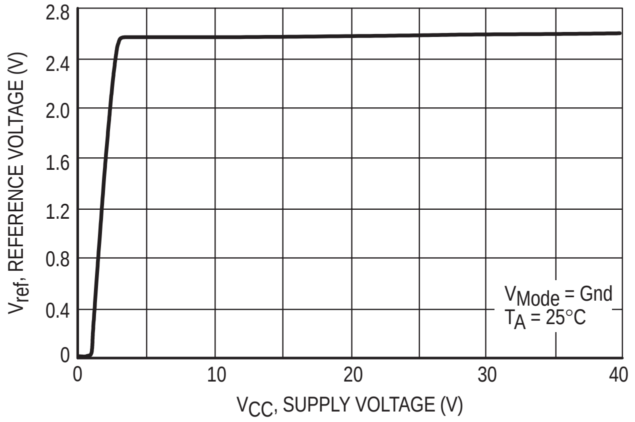


Figure 8. Reference Voltage versus Ambient Temperature

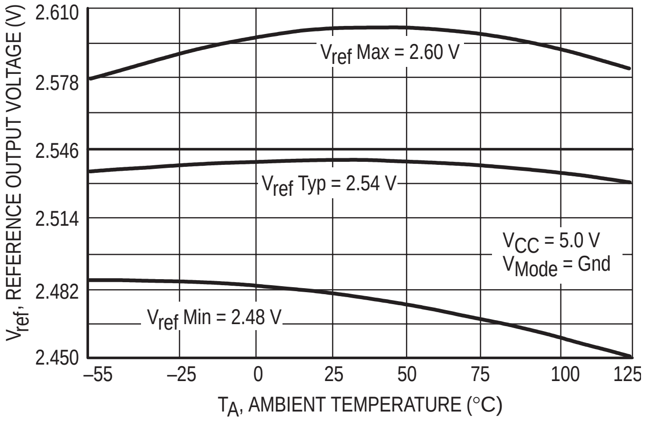


Figure 9. Reference Voltage Change versus Source Current

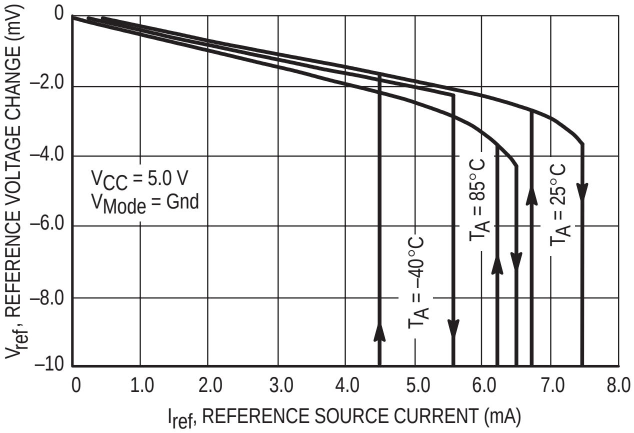


Figure 10. Output Saturation Voltage versus Output Sink Current

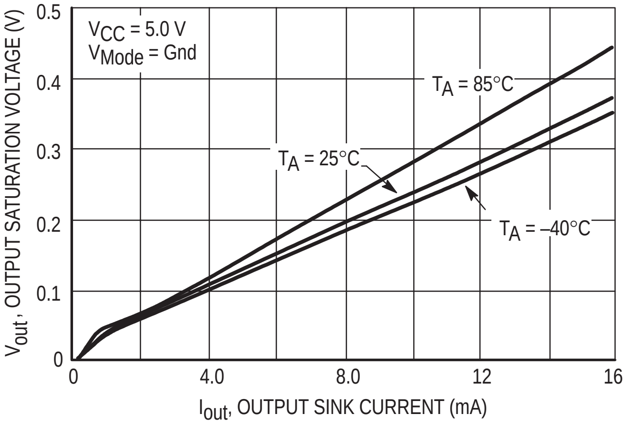


Figure 11. Supply Current versus Supply Voltage

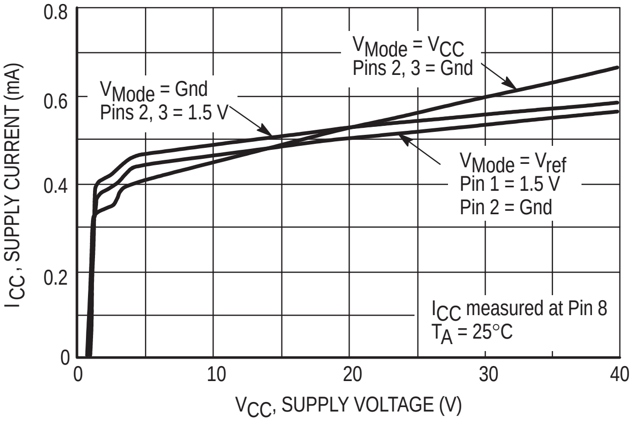


Figure 12. Supply Current versus Output Sink Current

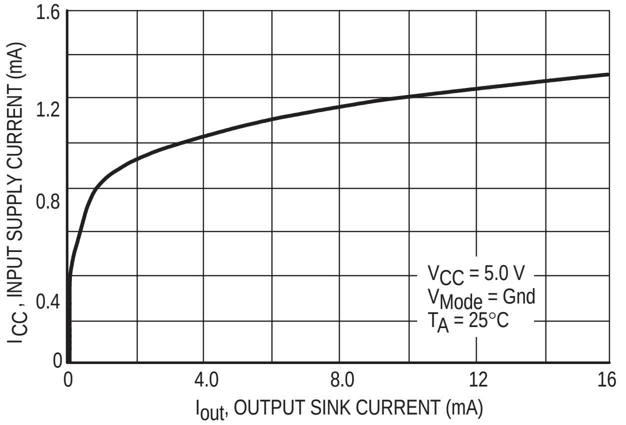


Figure 13. MC34161 Representative Block Diagram

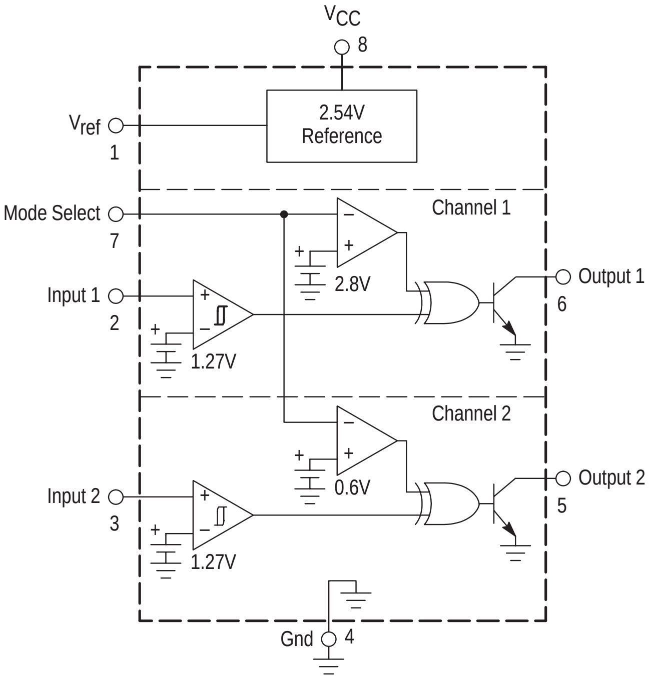


Figure 14. Truth Table

Mode Select Pin 7	Input 1 Pin 2	Output 1 Pin 6	Input 2 Pin 3	Output 2 Pin 5	Comments
GND	0 1	0 1	0 1	0 1	Channels 1 & 2: Noninverting
V_{ref}	0 1	0 1	0 1	1 0	Channel 1: Noninverting Channel 2: Inverting
V_{CC} (>2.0 V)	0 1	1 0	0 1	1 0	Channels 1 & 2: Inverting

FUNCTIONAL DESCRIPTION

Introduction

To be competitive in today's electronic equipment market, new circuits must be designed to increase system reliability with minimal incremental cost. The circuit designer can take a significant step toward attaining these goals by implementing economical circuitry that continuously monitors critical circuit voltages and provides a fault signal in the event of an out–of–tolerance condition. The MC34161, MC33161 series are universal voltage monitors intended for use in a wide variety of voltage sensing applications. The main objectives of this series was to configure a device that can be used in as many voltage sensing applications as possible while minimizing cost. The flexibility objective is achieved by the utilization of a unique Mode Select input that is used in conjunction with traditional circuit building blocks. The cost objective is achieved by processing the device on a standard Bipolar Analog flow, and by limiting the package to eight pins. The device consists of two comparator channels each with hysteresis, a mode select input for channel programming, a pinned out reference, and two open collector outputs. Each comparator channel can be configured as either inverting or noninverting by the Mode Select input. This allows a single device to perform over, under, and window detection of positive and negative voltages. A detailed description of each section of the device is given below with the representative block diagram shown in Figure 13.

Input Comparators

The input comparators of each channel are identical, each having an upper threshold voltage of 1.27 V ±2.0% with 25 mV of hysteresis. The hysteresis is provided to enhance output switching by preventing oscillations as the comparator thresholds are crossed. The comparators have an input bias current of 60 nA at their threshold which approximates a 21.2 MΩ resistor to ground. This high impedance minimizes loading of the external voltage divider for well defined trip points. For all positive voltage sensing applications, both comparator channels are fully functional at a V_{CC} of 2.0 V. In order to provide enhanced device ruggedness for hostile industrial environments, additional circuitry was designed into the inputs to prevent device latch–up as well as to suppress electrostatic discharges (ESD).

Reference

The 2.54 V reference is pinned out to provide a means for the input comparators to sense negative voltages, as well as a means to program the Mode Select input for window detection applications. The reference is capable of sourcing in excess of 2.0 mA output current and has built–in short circuit protection. The output voltage has a guaranteed tolerance of ±2.4% at room temperature.

The 2.54 V reference is derived by gaining up the internal 1.27 V reference by a factor of two. With a power supply voltage of 4.0 V, the 2.54 V reference is in full regulation, allowing the device to accurately sense negative voltages.

Mode Select Circuit

The key feature that allows this device to be flexible is the Mode Select input. This input allows the user to program each of the channels for various types of voltage sensing applications. Figure 14 shows that the Mode Select input has three defined states. These states determine whether Channel 1 and/or Channel 2 operate in the inverting or noninverting mode. The Mode Select thresholds are shown in Figure 5. The input circuitry forms a tristate switch with thresholds at 0.63 V and V_{ref} + 0.23 V. The mode select input current is 10 µA when connected to the reference output, and 42 µA when connected to a V_{CC} of 5.0 V, refer to Figure 6.

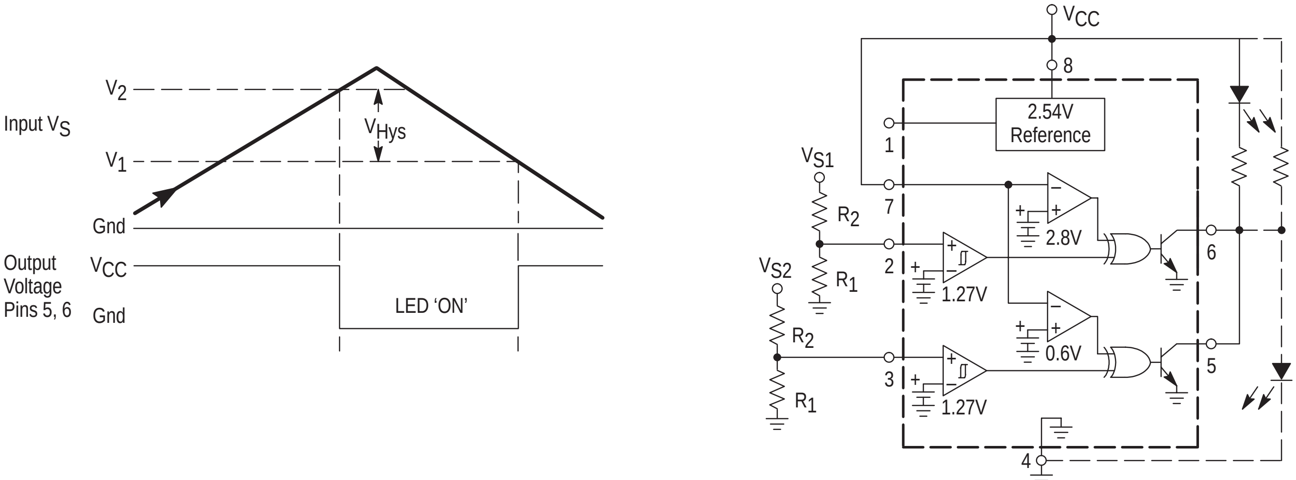
Output Stage

The output stage uses a positive feedback base boost circuit for enhanced sink saturation, while maintaining a relatively low device standby current. Figure 10 shows that the sink saturation voltage is about 0.2 V at 8.0 mA over temperature. By combining the low output saturation characteristics with low voltage comparator operation, this device is capable of sensing positive voltages at a V_{CC} of 1.0 V. These characteristics are important in undervoltage sensing applications where the output must stay in a low state as V_{CC} approaches ground. Figure 4 shows the Output Voltage versus Supply Voltage in an undervoltage sensing application. Note that as V_{CC} drops below the programmed 4.5 V trip point, the output stays in a well defined active low state until V_{CC} drops below 1.0 V.

APPLICATIONS

The following circuit figures illustrate the flexibility of this device. Included are voltage sensing applications for over, under, and window detectors, as well as three unique configurations. Many of the voltage detection circuits are shown with the open collector outputs of each channel connected together driving a light emitting diode (LED). This 'ORed' connection is shown for ease of explanation and it is only required for window detection applications. Note that many of the voltage detection circuits are shown with a dashed line output connection. This connection gives the inverse function of the solid line connection. For example, the solid line output connection of Figure 15 has the LED 'ON' when input voltage V_S is above trip voltage V_2, for overvoltage detection. The dashed line output connection has the LED 'ON' when V_S is below trip voltage V_2, for undervoltage detection.

Figure 15. Dual Postive Overvoltage Detector



The above figure shows the MC34161 configured as a dual positive overvoltage detector. As the input voltage increases from ground, the LED will turn 'ON' when V_{S1} or V_{S2} exceeds V_2. With the dashed line output connection, the circuit becomes a dual positive undervoltage detector. As the input voltage decreases from the peak towards ground, the LED will turn 'ON' when V_{S1} or V_{S2} falls below V_1.

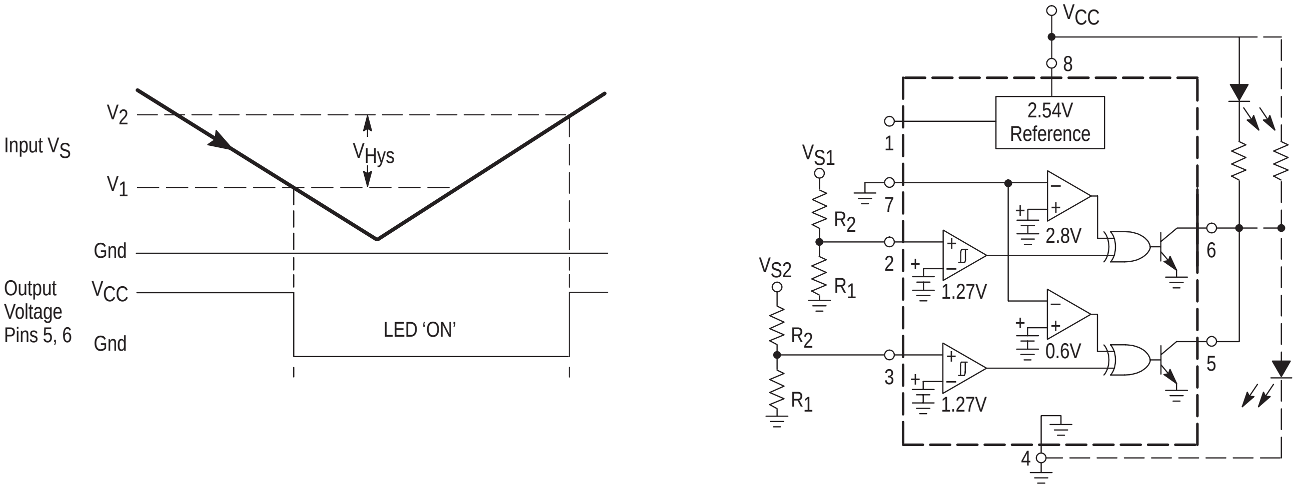
For known resistor values, the voltage trip points are:

$$V_1 = (V_{th} - V_H)\left(\frac{R_2}{R_1} + 1\right) \qquad V_2 = V_{th}\left(\frac{R_2}{R_1} + 1\right)$$

For a specific trip voltage, the required resistor ratio is:

$$\frac{R_2}{R_1} = \frac{V_1}{V_{th} - V_H} - 1 \qquad \frac{R_2}{R_1} = \frac{V_2}{V_{th}} - 1$$

Figure 16. Dual Postive Undervoltage Detector



The above figure shows the MC34161 configured as a dual positive undervoltage detector. As the input voltage decreases towards ground, the LED will turn 'ON' when V_{S1} or V_{S2} falls below V_1. With the dashed line output connection, the circuit becomes a dual positive overvoltage detector. As the input voltage increases from ground, the LED will turn 'ON' when V_{S1} or V_{S2} exceeds V_2.

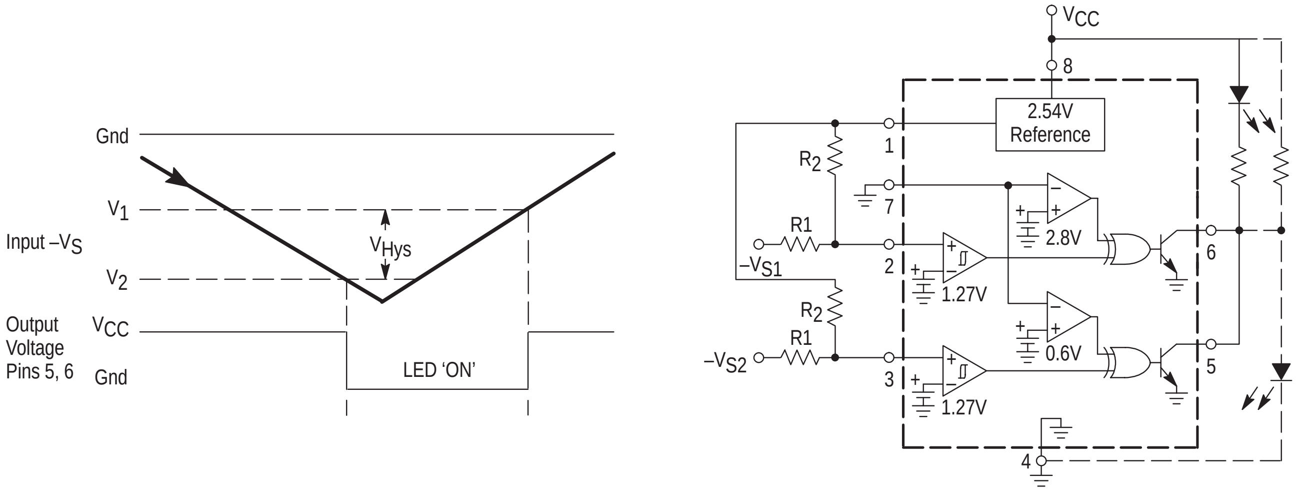
For known resistor values, the voltage trip points are:

$$V_1 = (V_{th} - V_H)\left(\frac{R_2}{R_1} + 1\right) \qquad V_2 = V_{th}\left(\frac{R_2}{R_1} + 1\right)$$

For a specific trip voltage, the required resistor ratio is:

$$\frac{R_2}{R_1} = \frac{V_1}{V_{th} - V_H} - 1 \qquad \frac{R_2}{R_1} = \frac{V_2}{V_{th}} - 1$$

Figure 17. Dual Negative Overvoltage Detector



The above figure shows the MC34161 configured as a dual negative overvoltage detector. As the input voltage increases from ground, the LED will turn 'ON' when $-V_{S1}$ or $-V_{S2}$ exceeds V_2. With the dashed line output connection, the circuit becomes a dual negative undervoltage detector. As the input voltage decreases from the peak towards ground, the LED will turn 'ON' when $-V_{S1}$ or $-V_{S2}$ falls below V_1.

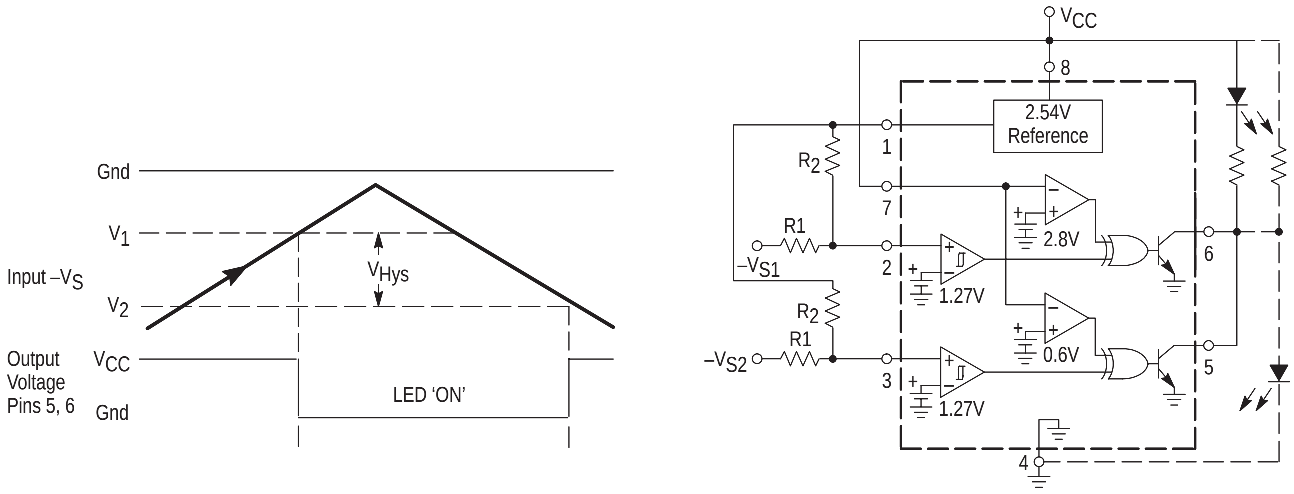
For known resistor values, the voltage trip points are:

$$V_1 = \frac{R_1}{R_2}(V_{th} - V_{ref}) + V_{th} \qquad V_2 = \frac{R_1}{R_2}(V_{th} - V_H - V_{ref}) + V_{th} - V_H$$

For a specific trip voltage, the required resistor ratio is:

$$\frac{R_1}{R_2} = \frac{V_1 - V_{th}}{V_{th} - V_{ref}} \qquad \frac{R_1}{R_2} = \frac{V_2 - V_{th} + V_H}{V_{th} - V_H - V_{ref}}$$

Figure 18. Dual Negative Undervoltage Detector



The above figure shows the MC34161 configured as a dual negative undervoltage detector. As the input voltage decreases towards ground, the LED will turn 'ON' when $-V_{S1}$ or $-V_{S2}$ falls below V_1. With the dashed line output connection, the circuit becomes a dual negative overvoltage detector. As the input voltage increases from ground, the LED will turn 'ON' when $-V_{S1}$ or $-V_{S2}$ exceeds V_2.

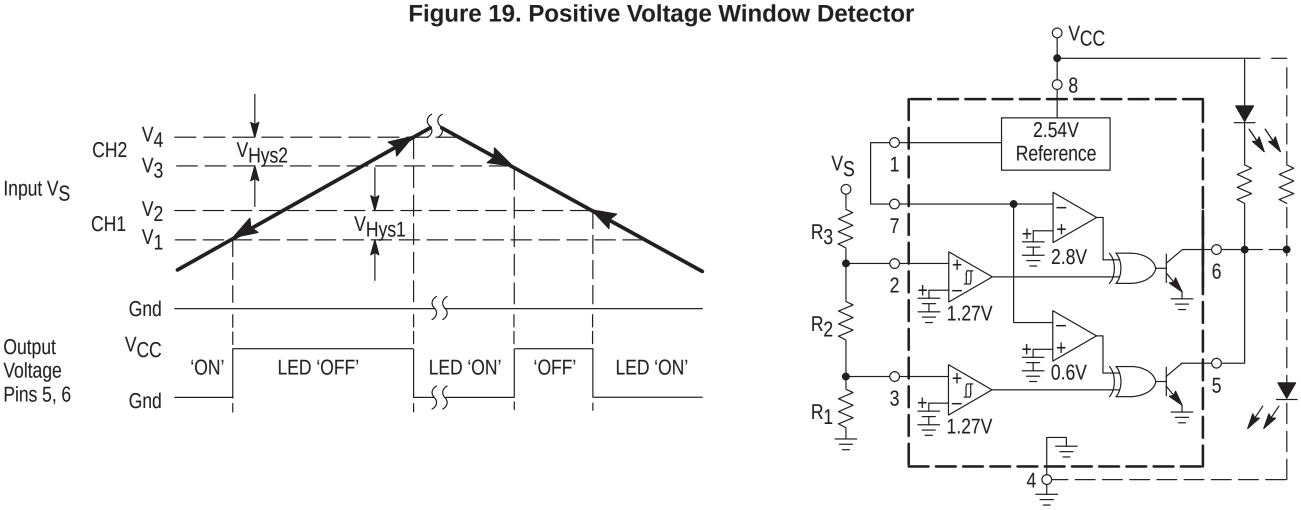
For known resistor values, the voltage trip points are:

$$V_1 = \frac{R_1}{R_2}(V_{th} - V_{ref}) + V_{th} \qquad V_2 = \frac{R_1}{R_2}(V_{th} - V_H - V_{ref}) + V_{th} - V_H$$

For a specific trip voltage, the required resistor ratio is:

$$\frac{R_1}{R_2} = \frac{V_1 - V_{th}}{V_{th} - V_{ref}} \qquad \frac{R_1}{R_2} = \frac{V_2 - V_{th} + V_H}{V_{th} - V_H - V_{ref}}$$

Figure 19. Positive Voltage Window Detector



The above figure shows the MC34161 configured as a positive voltage window detector. This is accomplished by connecting channel 1 as an undervoltage detector, and channel 2 as an overvoltage detector. When the input voltage V_S falls out of the window established by V_1 and V_4, the LED will turn ‘ON’. As the input voltage falls within the window, V_S increasing from ground and exceeding V_2, or V_S decreasing from the peak towards ground and falling below V_3, the LED will turn ‘OFF’. With the dashed line output connection, the LED will turn ‘ON’ when the input voltage V_S is within the window.

For known resistor values, the voltage trip points are:

$$V_1 = (V_{th1} - V_{H1})\left(\frac{R_3}{R_1 + R_2} + 1\right) \qquad V_3 = (V_{th2} - V_{H2})\left(\frac{R_2 + R_3}{R_1} + 1\right)$$

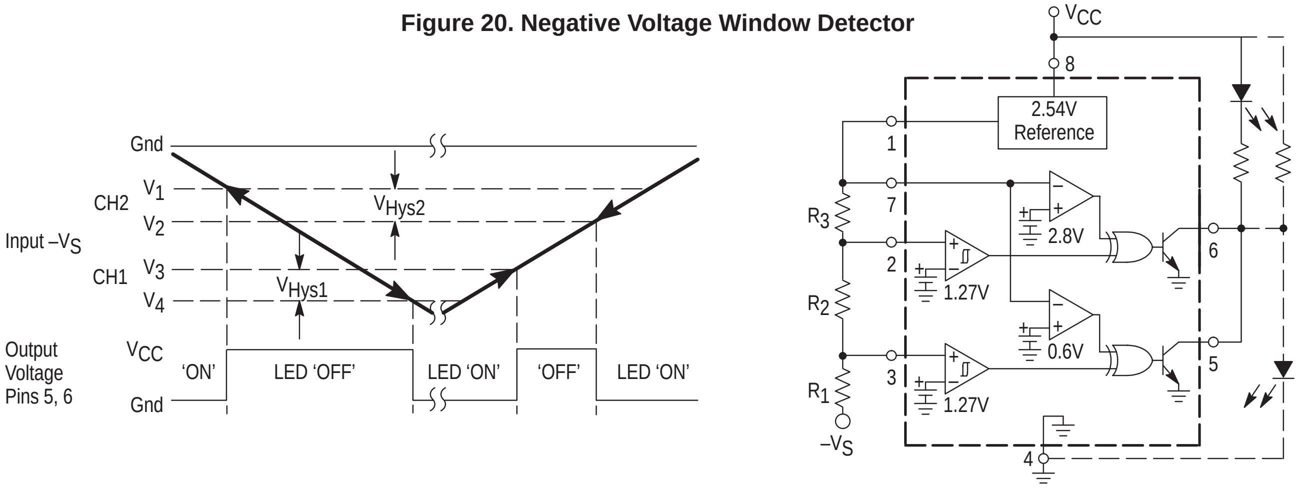
$$V_2 = V_{th1}\left(\frac{R_3}{R_1 + R_2} + 1\right) \qquad V_4 = V_{th2}\left(\frac{R_2 + R_3}{R_1} + 1\right)$$

For a specific trip voltage, the required resistor ratio is:

$$\frac{R_2}{R_1} = \frac{V_3(V_{th2} - V_{H2})}{V_1(V_{th1} - V_{H1})} - 1 \qquad \frac{R_3}{R_1} = \frac{V_3(V_1 - V_{th1} + V_{H1})}{V_1(V_{th2} - V_{H2})}$$

$$\frac{R_2}{R_1} = \frac{V_4 \text{ x } V_{th2}}{V_2 \text{ x } V_{th1}} - 1 \qquad \frac{R_3}{R_1} = \frac{V_4(V_2 - V_{th1})}{V_2 \text{ x } V_{th2}}$$

Figure 20. Negative Voltage Window Detector



The above figure shows the MC34161 configured as a negative voltage window detector. When the input voltage $-V_S$ falls out of the window established by V_1 and V_4, the LED will turn ‘ON’. As the input voltage falls within the window, $-V_S$ increasing from ground and exceeding V_2, or $-V_S$ decreasing from the peak towards ground and falling below V_3, the LED will turn ‘OFF’. With the dashed line output connection, the LED will turn ‘ON’ when the input voltage $-V_S$ is within the window.

For known resistor values, the voltage trip points are:

$$V_1 = \frac{R_1(V_{th2} - V_{ref})}{R_2 + R_3} + V_{th2}$$

$$V_2 = \frac{R_1(V_{th2} - V_{H2} - V_{ref})}{R_2 + R_3} + V_{th2} - V_{H2}$$

$$V_3 = \frac{(R_1 + R_2)(V_{th1} - V_{ref})}{R_3} + V_{th1}$$

$$V_4 = \frac{(R_1 + R_2)(V_{th1} - V_{H1} - V_{ref})}{R_3} + V_{th1} - V_{H1}$$

For a specific trip voltage, the required resistor ratio is:

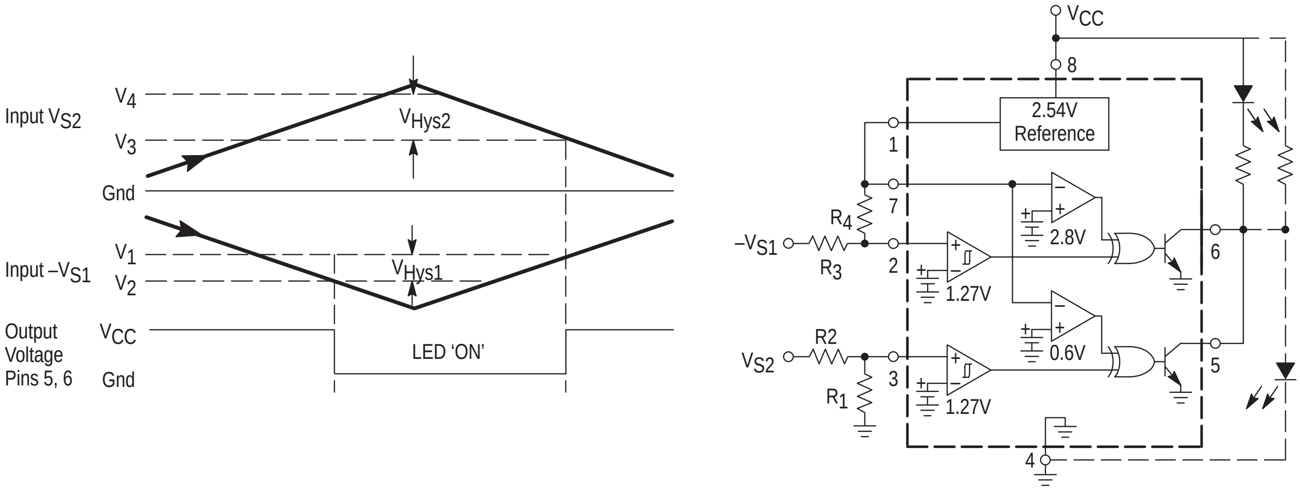
$$\frac{R_1}{R_2 + R_3} = \frac{V_1 - V_{th2}}{V_{th2} - V_{ref}}$$

$$\frac{R_1}{R_2 + R_3} = \frac{V_2 - V_{th2} + V_{H2}}{V_{th2} - V_{H2} - V_{ref}}$$

$$\frac{R_3}{R_1 + R_2} = \frac{V_{th1} - V_{ref}}{V_3 - V_{th1}}$$

$$\frac{R_3}{R_1 + R_2} = \frac{V_{th1} - V_{H1} - V_{ref}}{V_4 + V_{H1} - V_{th1}}$$

Figure 21. Positive and Negative Overvoltage Detector



The above figure shows the MC34161 configured as a positive and negative overvoltage detector. As the input voltage increases from ground, the LED will turn 'ON' when either $-V_{S1}$ exceeds V_2, or V_{S2} exceeds V_4. With the dashed line output connection, the circuit becomes a positive and negative undervoltage detector. As the input voltage decreases from the peak towards ground, the LED will turn 'ON' when either V_{S2} falls below V_3, or $-V_{S1}$ falls below V_1.

For known resistor values, the voltage trip points are:

$$V_1 = \frac{R_3}{R_4}(V_{th1} - V_{ref}) + V_{th1} \qquad V_3 = (V_{th2} - V_{H2})\left(\frac{R_2}{R_1} + 1\right)$$

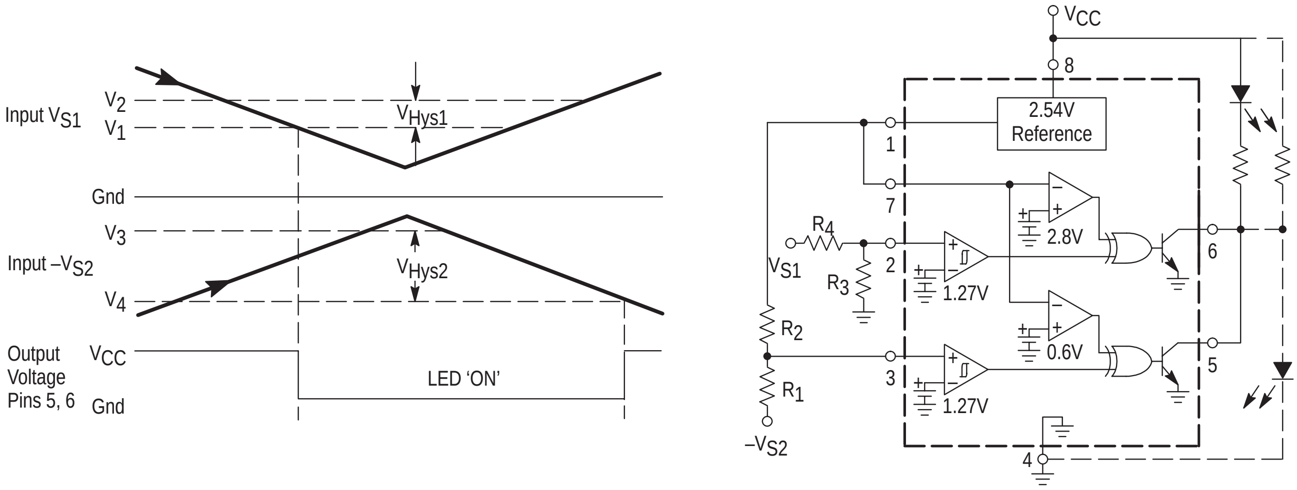
$$V_2 = \frac{R_3}{R_4}(V_{th1} - V_{H1} - V_{ref}) + V_{th1} - V_{H1} \qquad V_4 = V_{th2}\left(\frac{R_2}{R_1} + 1\right)$$

For a specific trip voltage, the required resistor ratio is:

$$\frac{R_3}{R_4} = \frac{(V_1 - V_{th1})}{(V_{th1} - V_{ref})} \qquad \frac{R_2}{R_1} = \frac{V_4}{V_{th2}} - 1$$

$$\frac{R_3}{R_4} = \frac{(V_2 - V_{th1} + V_{H1})}{(V_{th1} - V_{H1} - V_{ref})} \qquad \frac{R_2}{R_1} = \frac{V_3}{V_{th2} - V_{H2}} - 1$$

Figure 22. Positive and Negative Undervoltage Detector



The above figure shows the MC34161 configured as a positive and negative undervoltage detector. As the input voltage decreases toward ground, the LED will turn 'ON' when either V_{S1} falls below V_1, or $-V_{S2}$ falls below V_3. With the dashed line output connection, the circuit becomes a positive and negative overvoltage detector. As the input voltage increases from the ground, the LED will turn 'ON' when either V_{S1} exceeds V_2, or $-V_{S1}$ exceeds V_1.

For known resistor values, the voltage trip points are:

$$V_1 = (V_{th1} - V_{H1})\left(\frac{R_4}{R_3} + 1\right) \qquad V_3 = \frac{R_1}{R_2}(V_{th} - V_{ref}) + V_{th2}$$

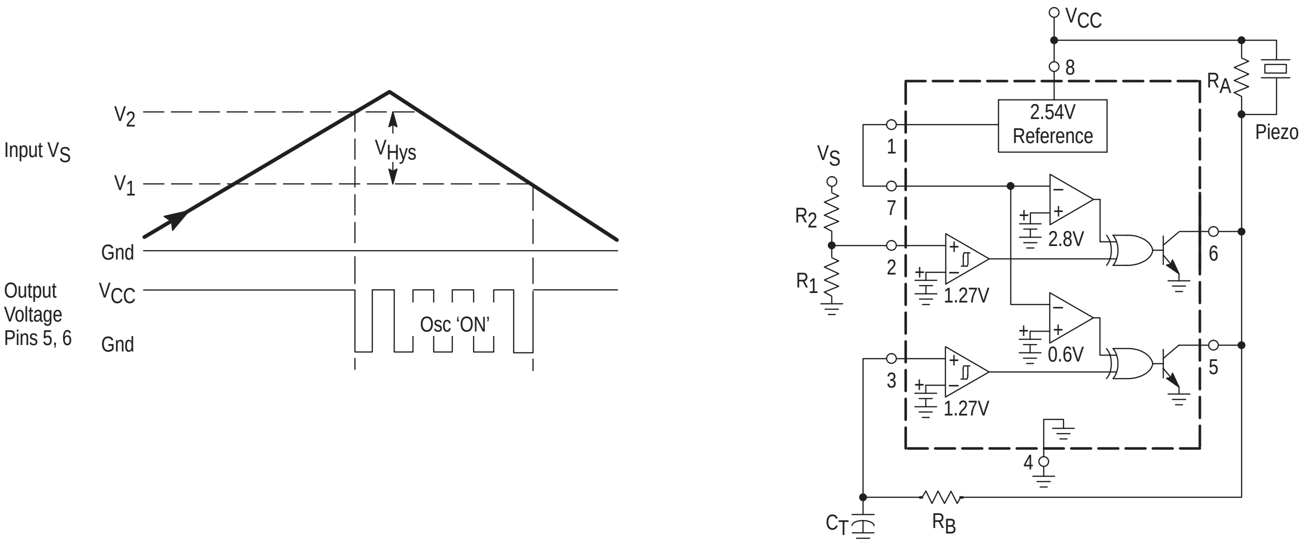
$$V_2 = V_{th1}\left(\frac{R_4}{R_3} + 1\right) \qquad V_4 = \frac{R_1}{R_2}(V_{th} - V_{H2} - V_{ref}) + V_{th2} - V_{H2}$$

For a specific trip voltage, the required resistor ratio is:

$$\frac{R_4}{R_3} = \frac{V_2}{V_{th1}} - 1 \qquad \frac{R_1}{R_2} = \frac{V_4 + V_{H2} - V_{th2}}{V_{th2} - V_{H2} - V_{ref}}$$

$$\frac{R_4}{R_3} = \frac{V_1}{V_{th1} - V_{H1}} - 1 \qquad \frac{R_1}{R_2} = \frac{V_3 - V_{th2}}{V_{th2} - V_{ref}}$$

Figure 23. Overvoltage Detector with Audio Alarm



The above figure shows the MC34161 configured as an overvoltage detector with an audio alarm. Channel 1 monitors input voltage V_S while channel 2 is connected as a simple RC oscillator. As the input voltage increases from ground, the output of channel 1 allows the oscillator to turn ‘ON’ when V_S exceeds V_2.

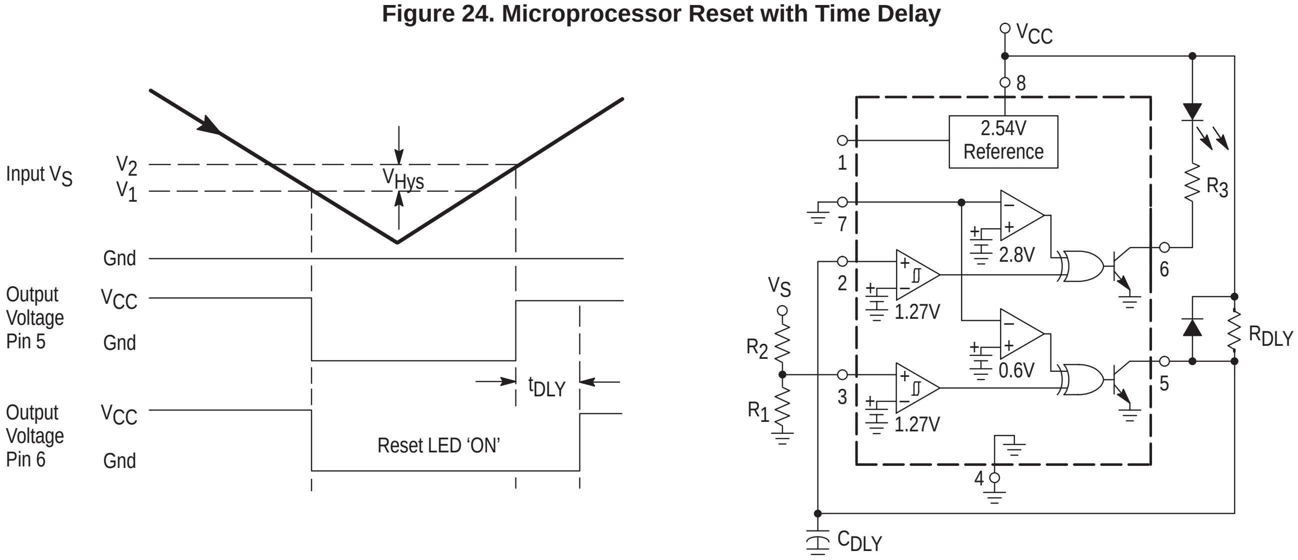
For known resistor values, the voltage trip points are:

$$V_1 = (V_{th} - V_H)\left(\frac{R_2}{R_1} + 1\right) \quad V_2 = V_{th}\left(\frac{R_2}{R_1} + 1\right)$$

For a specific trip voltage, the required resistor ratio is:

$$\frac{R_2}{R_1} = \frac{V_1}{V_{th} - V_H} - 1 \qquad \frac{R_2}{R_1} = \frac{V_2}{V_{th}} - 1$$

Figure 24. Microprocessor Reset with Time Delay



The above figure shows the MC34161 configured as a microprocessor reset with a time delay. Channel 2 monitors input voltage V_S while channel 1 performs the time delay function. As the input voltage decreases towards ground, the output of channel 2 quickly discharges C_{DLY} when V_S falls below V_1. As the input voltage increases from ground, the output of channel 2 allows R_{DLY} to charge C_{DLY} when V_S exceeds V_2.

For known resistor values, the voltage trip points are:

$$V_1 = (V_{th} - V_H)\left(\frac{R_2}{R_1} + 1\right) \quad V_2 = V_{th}\left(\frac{R_2}{R_1} + 1\right)$$

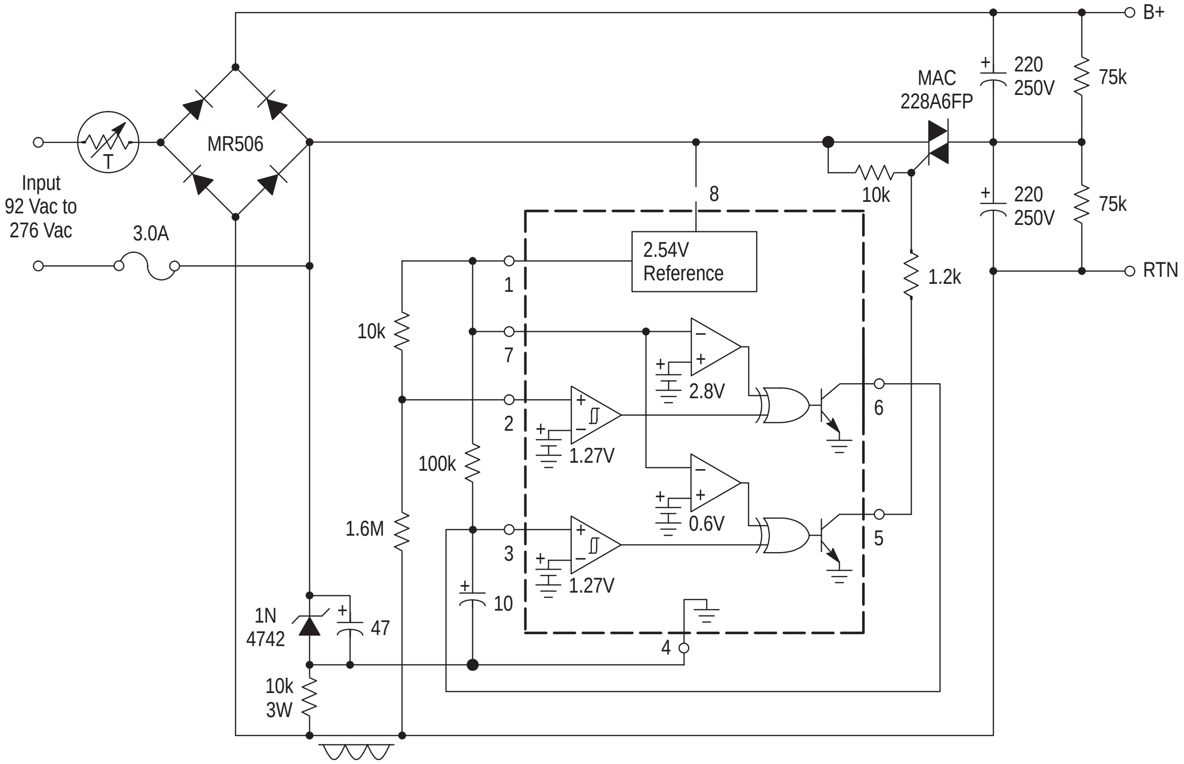
For a specific trip voltage, the required resistor ratio is:

$$\frac{R_2}{R_1} = \frac{V_1}{V_{th} - V_H} - 1 \qquad \frac{R_2}{R_1} = \frac{V_2}{V_{th}} - 1$$

For known R_{DLY} C_{DLY} values, the reset time delay is:

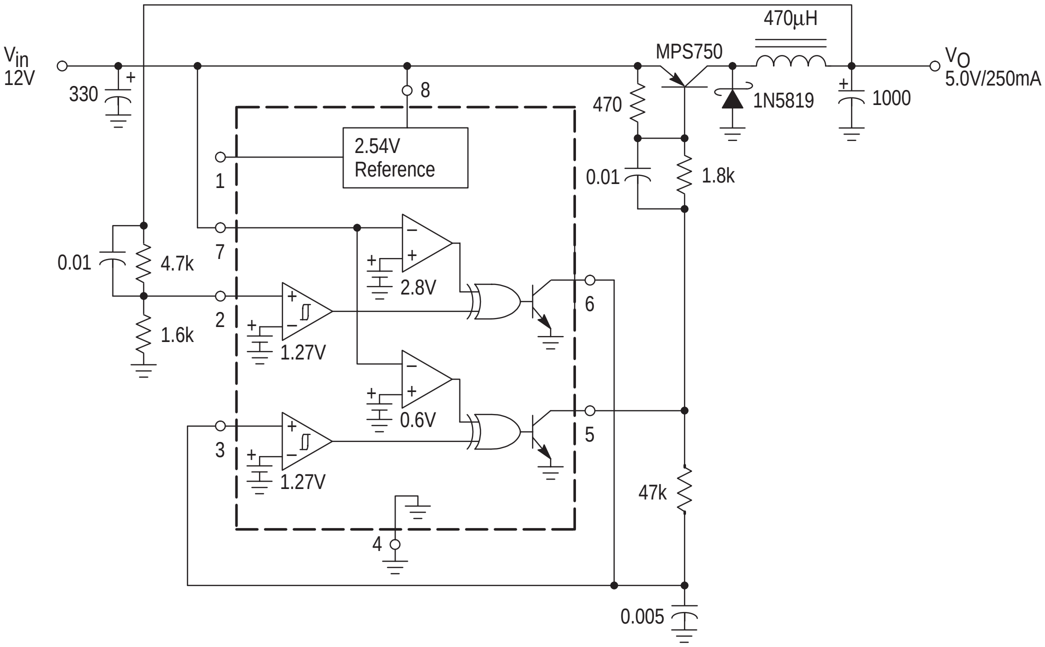
$$t_{DLY} = R_{DLY}C_{DLY} \ln\left(\frac{1}{1 - \frac{V_{th}}{V_{CC}}}\right)$$

Figure 25. Automatic AC Line Voltage Selector



The above circuit shows the MC34161 configured as an automatic line voltage selector. The IC controls the triac, enabling the circuit to function as a fullwave voltage doubler or a fullwave bridge. Channel 1 senses the negative half cycles of the AC line voltage. If the line voltage is less than150 V, the circuit will switch from bridge mode to voltage doubling mode after a preset time delay. The delay is controlled by the 100 kΩ resistor and the 10 μF capacitor. If the line voltage is greater than 150 V, the circuit will immediately return to fullwave bridge mode.

Figure 26. Step–Down Converter



Test	Conditions	Results
Line Regulation	V_{in} = 9.5 V to 24 V, I_O = 250 mA	40 mV = ±0.1%
Load Regulation	V_{in} = 12 V, I_O = 0.25 mA to 250 mA	2.0 mV = ±0.2%
Output Ripple	V_{in} = 12 V, I_O = 250 mA	50 mVpp
Efficiency	V_{in} = 12 V, I_O = 250 mA	87.8%

The above figure shows the MC34161 configured as a step–down converter. Channel 1 monitors the output voltage while Channel 2 performs the oscillator function. Upon initial power–up, the converters output voltage will be below nominal, and the output of Channel 1 will allow the oscillator to run. The external switch transistor will eventually pump–up the output capacitor until its voltage exceeds the input threshold of Channel 1. The output of Channel 1 will then switch low and disable the oscillator. The oscillator will commence operation when the output voltage falls below the lower threshold of Channel 1.

MC34163
MC33163

Power Switching Regulators

The MC34163 series are monolithic power switching regulators that contain the primary functions required for dc–to–dc converters. This series is specifically designed to be incorporated in step–up, step–down, and voltage–inverting applications with a minimum number of external components.

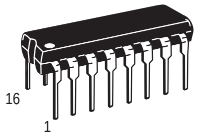
These devices consist of two high gain voltage feedback comparators, temperature compensated reference, controlled duty cycle oscillator, driver with bootstrap capability for increased efficiency, and a high current output switch. Protective features consist of cycle–by–cycle current limiting, and internal thermal shutdown. Also included is a low voltage indicator output designed to interface with microprocessor based systems.

These devices are contained in a 16 pin dual–in–line heat tab plastic package for improved thermal conduction.

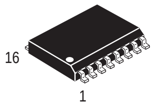
- Output Switch Current in Excess of 3.0 A
- Operation from 2.5 V to 40 V Input
- Low Standby Current
- Precision 2% Reference
- Controlled Duty Cycle Oscillator
- Driver with Bootstrap Capability for Increased Efficiency
- Cycle–by–Cycle Current Limiting
- Internal Thermal Shutdown Protection
- Low Voltage Indicator Output for Direct Microprocessor Interface
- Heat Tab Power Package

POWER SWITCHING REGULATORS

SEMICONDUCTOR
TECHNICAL DATA

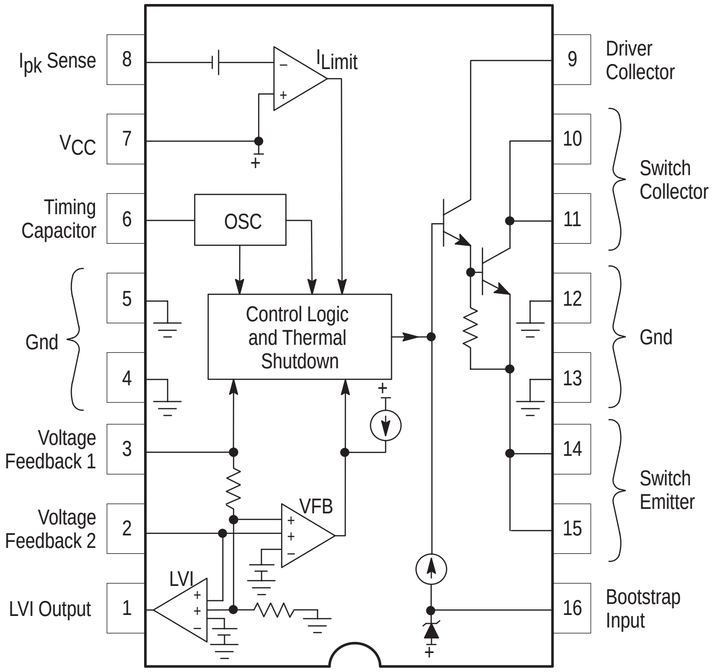


P SUFFIX
PLASTIC PACKAGE
CASE 648C
(DIP–16)



DW SUFFIX
PLASTIC PACKAGE
CASE 751G
(SOP–16L)

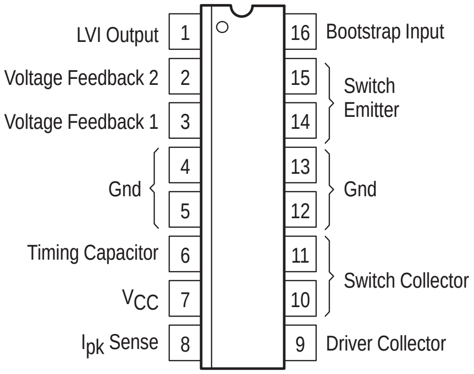
Representative Block Diagram



(Bottom View)

This device contains 114 active transistors.

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC34163DW	T_A = 0° to +70°C	SOP–16L
MC34163P		DIP–16
MC33163DW	T_A = – 40° to +85°C	SOP–16L
MC33163P		DIP–16

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	40	V
Switch Collector Voltage Range	$V_{C(switch)}$	–1.0 to + 40	V
Switch Emitter Voltage Range	$V_{E(switch)}$	– 2.0 to $V_{C(switch)}$	V
Switch Collector to Emitter Voltage	$V_{CE(switch)}$	40	V
Switch Current (Note 1)	I_{SW}	3.4	A
Driver Collector Voltage	$V_{C(driver)}$	–1.0 to +40	V
Driver Collector Current	$I_{C(driver)}$	150	mA
Bootstrap Input Current Range (Note 1)	I_{BS}	–100 to +100	mA
Current Sense Input Voltage Range	$V_{Ipk(Sense)}$	(V_{CC}–7.0) to (V_{CC}+1.0)	V
Feedback and Timing Capacitor Input Voltage Range	V_{in}	–1.0 to + 7.0	V
Low Voltage Indicator Output Voltage Range	$V_{C(LVI)}$	–1.0 to + 40	V
Low Voltage Indicator Output Sink Current	$I_{C(LVI)}$	10	mA
Thermal Characteristics			°C/W
P Suffix, Dual–In–Line Case 648C			
Thermal Resistance, Junction–to–Air	$R_{\theta JA}$	80	
Thermal Resistance, Junction–to–Case (Pins 4, 5, 12, 13)	$R_{\theta JC}$	15	
DW Suffix, Surface Mount Case 751G			
Thermal Resistance, Junction–to–Air	$R_{\theta JA}$	94	
Thermal Resistance, Junction–to–Case (Pins 4, 5, 12, 13)	$R_{\theta JC}$	18	
Operating Junction Temperature	T_J	+150	°C
Operating Ambient Temperature (Note 3)	T_A		°C
MC34163		0 to +70	
MC33163		– 40 to + 85	
Storage Temperature Range	T_{stg}	– 65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V, Pin 16 = V_{CC}, C_T = 620 pF, for typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies (Note 3), unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OSCILLATOR					
Frequency	f_{OSC}				kHz
T_A = 25°C		46	50	54	
Total Variation over V_{CC} = 2.5 V to 40 V, and Temperature		45	–	55	
Charge Current	I_{chg}	–	225	–	µA
Discharge Current	I_{dischg}	–	25	–	µA
Charge to Discharge Current Ratio	I_{chg}/I_{dischg}	8.0	9.0	10	–
Sawtooth Peak Voltage	$V_{OSC(P)}$	–	1.25	–	V
Sawtooth Valley Voltage	$V_{OSC(V)}$	–	0.55	–	V
FEEDBACK COMPARATOR 1					
Threshold Voltage	$V_{th(FB1)}$				
T_A = 25°C		4.9	5.05	5.2	V
Line Regulation (V_{CC} = 2.5 V to 40 V, T_A = 25°C)		–	0.008	0.03	%/V
Total Variation over Line, and Temperature		4.85	–	5.25	V
Input Bias Current (V_{FB1} = 5.05 V)	$I_{IB(FB1)}$	–	100	200	µA

NOTES: 1. Maximum package power dissipation limits must be observed.
2. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
3. T_{low} = 0°C for MC34163 T_{high} = + 70°C for MC34163
= – 40°C for MC33163   = + 85°C for MC33163

ELECTRICAL CHARACTERISTICS (continued) (V_{CC} = 15 V, Pin 16 = V_{CC}, C_T = 620 pF, for typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies (Note 3), unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
FEEDBACK COMPARATOR 2					
Threshold Voltage	$V_{th(FB2)}$				
T_A = 25°C		1.225	1.25	1.275	V
Line Regulation (V_{CC} = 2.5 V to 40 V, T_A = 25°C)		–	0.008	0.03	%/V
Total Variation over Line, and Temperature		1.213	–	1.287	V
Input Bias Current (V_{FB2} = 1.25 V)	$I_{IB(FB2)}$	– 0.4	0	0.4	µA
CURRENT LIMIT COMPARATOR					
Threshold Voltage	$V_{th(Ipk\ Sense)}$				mV
T_A = 25°C		–	250	–	
Total Variation over V_{CC} = 2.5 V to 40 V, and Temperature		230	–	270	
Input Bias Current ($V_{Ipk\ (Sense)}$ = 15 V)	$I_{IB(sense)}$	–	1.0	20	µA
DRIVER AND OUTPUT SWITCH (Note 2)					
Sink Saturation Voltage (I_{SW} = 2.5 A, Pins 14, 15 grounded)	$V_{CE(sat)}$				V
Non–Darlington Connection ($R_{Pin\ 9}$ = 110 Ω to V_{CC}, $I_{SW}/I_{DRV} \approx 20$)		–	0.6	1.0	
Darlington Connection (Pins 9, 10, 11 connected)		–	1.0	1.4	
Collector Off–State Leakage Current (V_{CE} = 40 V)	$I_{C(off)}$	–	0.02	100	µA
Bootstrap Input Current Source (V_{BS} = V_{CC} + 5.0 V)	$I_{source(DRV)}$	0.5	2.0	4.0	mA
Bootstrap Input Zener Clamp Voltage (I_Z = 25 mA)	V_Z	V_{CC} + 6.0	V_{CC} + 7.0	V_{CC} + 9.0	V
LOW VOLTAGE INDICATOR					
Input Threshold (V_{FB2} Increasing)	V_{th}	1.07	1.125	1.18	V
Input Hysteresis (V_{FB2} Decreasing)	V_H	–	15	–	mV
Output Sink Saturation Voltage (I_{sink} = 2.0 mA)	$V_{OL(LVI)}$	–	0.15	0.4	V
Output Off–State Leakage Current (V_{OH} = 15 V)	I_{OH}	–	0.01	5.0	µA
TOTAL DEVICE					
Standby Supply Current (V_{CC} = 2.5 V to 40 V, Pin 8 = V_{CC}, Pins 6, 14, 15 = Gnd, remaining pins open)	I_{CC}	–	6.0	10	mA

NOTES: 1. Maximum package power dissipation limits must be observed.
2. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
3. T_{low} = 0°C for MC34163 T_{high} = + 70°C for MC34163
= – 40°C for MC33163   = + 85°C for MC33163

Figure 1. Output Switch On–Off Time versus Oscillator Timing Capacitor

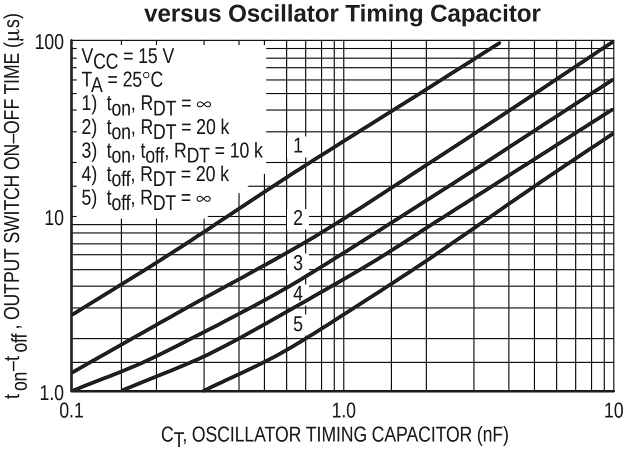


Figure 2. Oscillator Frequency Change versus Temperature

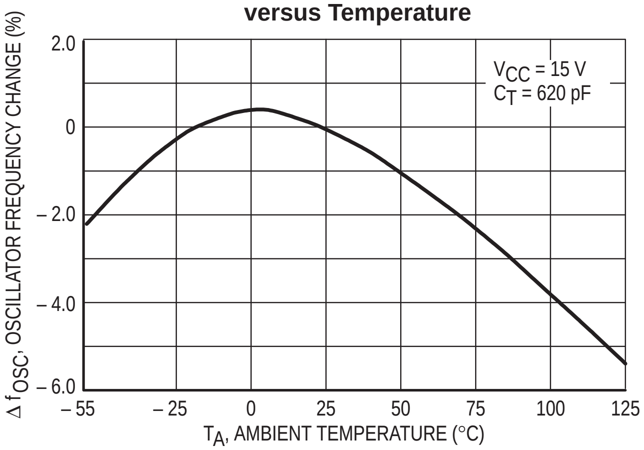


Figure 3. Feedback Comparator 1 Input Bias Current versus Temperature

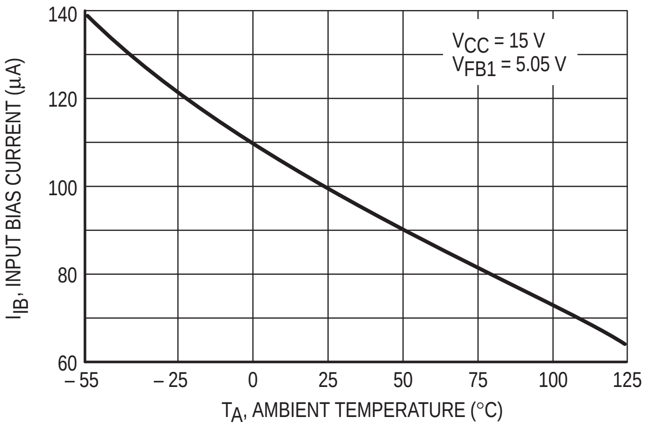


Figure 4. Feedback Comparator 2 Threshold Voltage versus Temperature

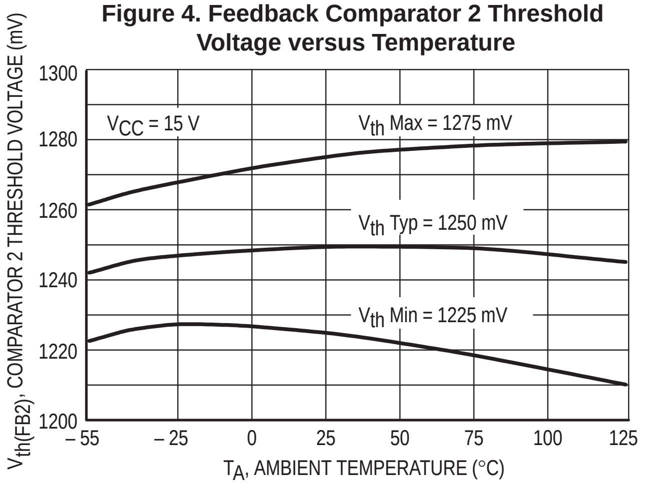


Figure 5. Bootstrap Input Current Source versus Temperature

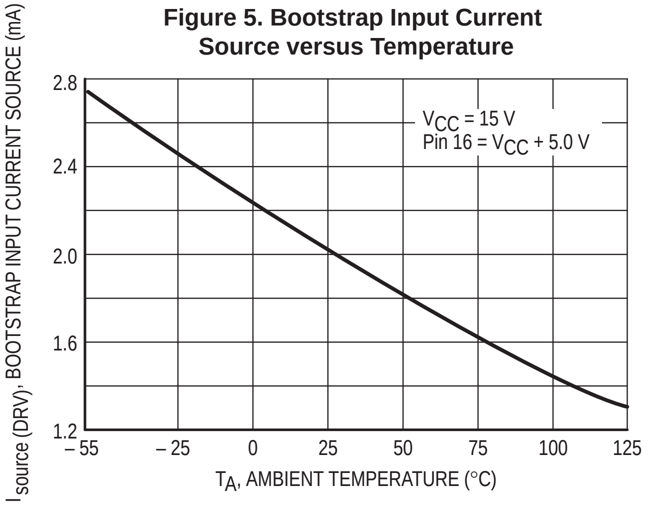


Figure 6. Bootstrap Input Zener Clamp Voltage versus Temperature

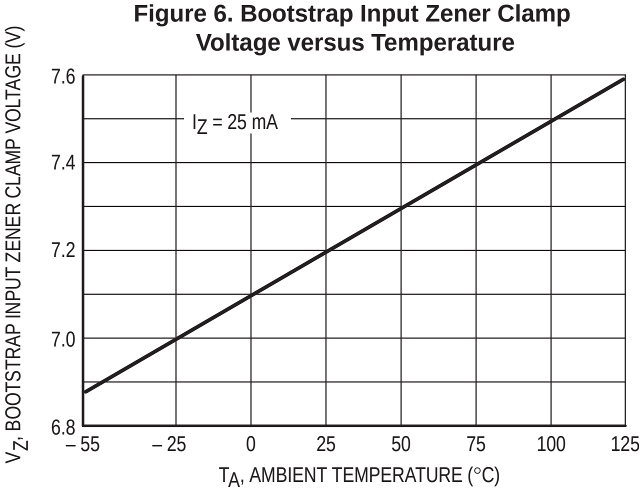


Figure 7. Output Switch Source Saturation versus Emitter Current

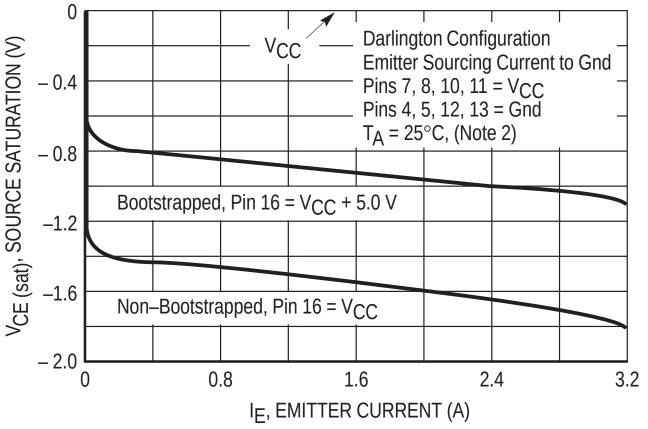


Figure 8. Output Switch Sink Saturation versus Collector Current

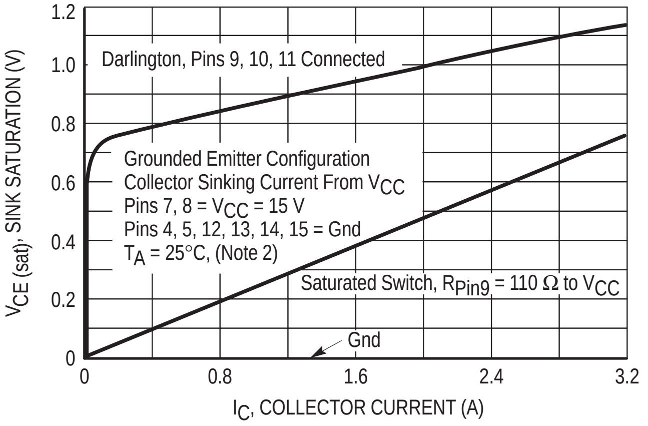


Figure 9. Output Switch Negative Emitter Voltage versus Temperature

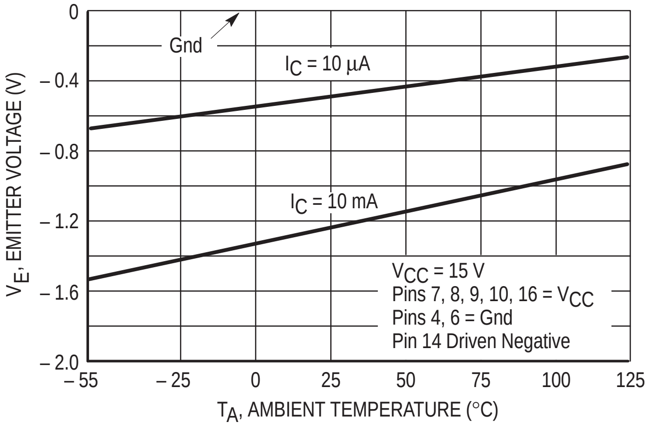


Figure 10. Low Voltage Indicator Output Sink Saturation Voltage versus Sink Current

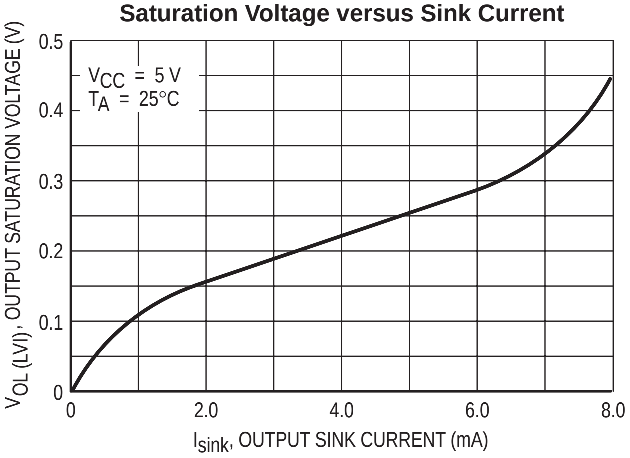


Figure 11. Current Limit Comparator Threshold Voltage versus Temperature

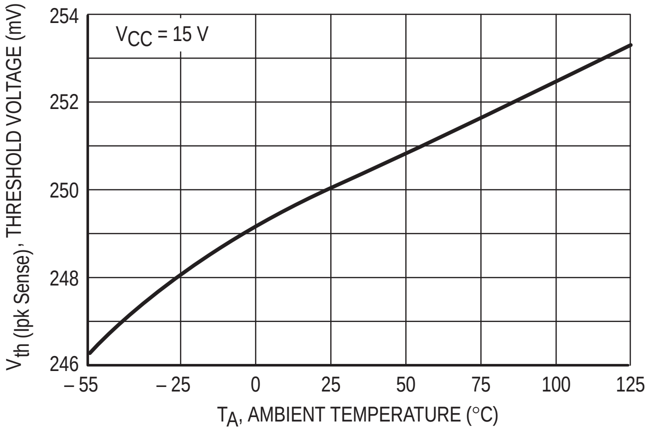


Figure 12. Current Limit Comparator Input Bias Current versus Temperature

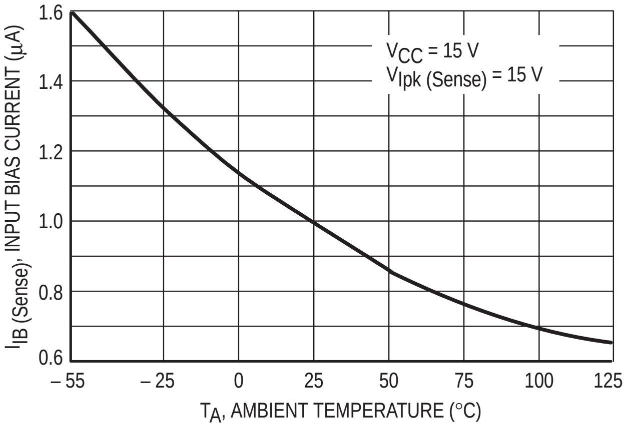


Figure 13. Standby Supply Current versus Supply Voltage

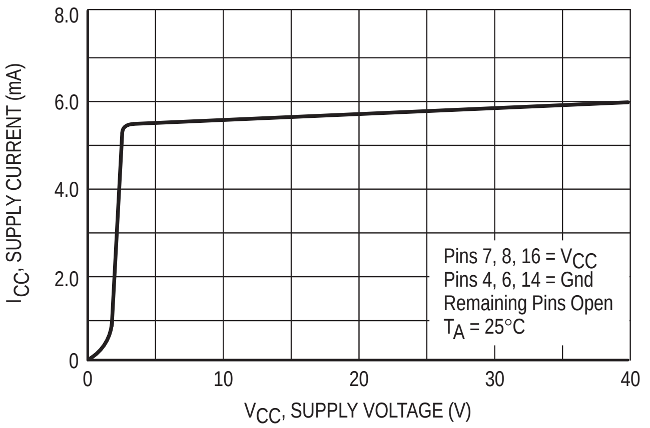


Figure 14. Standby Supply Current versus Temperature

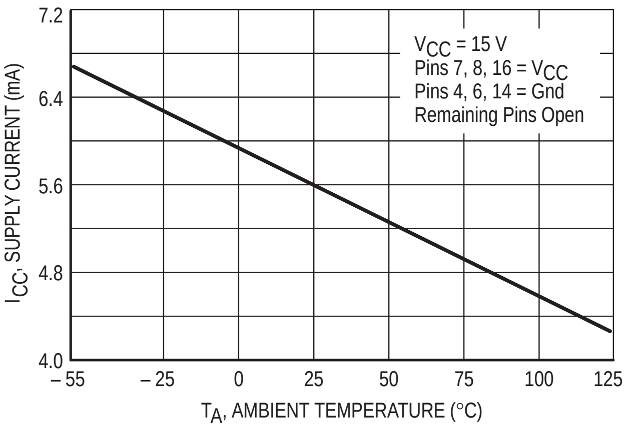


Figure 15. Minimum Operating Supply Voltage versus Temperature

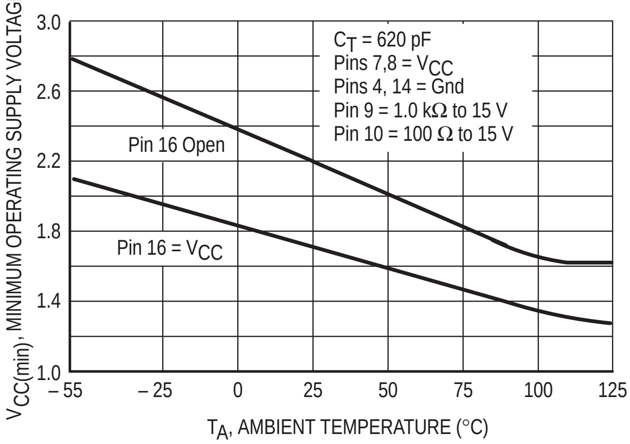


Figure 16. P Suffix (DIP–16) Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length

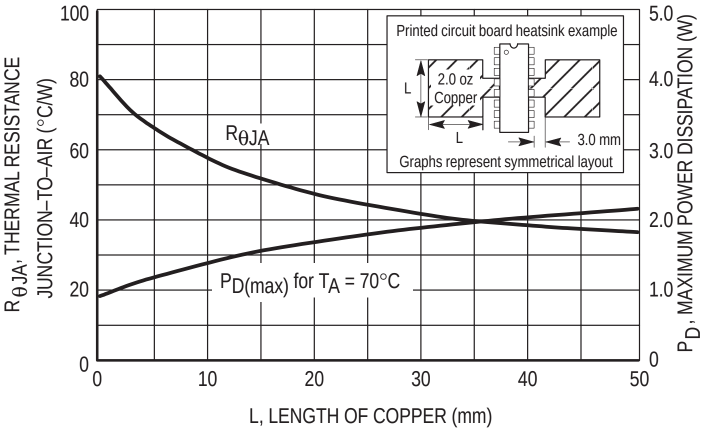


Figure 17. DW Suffix (SOP–16L) Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length

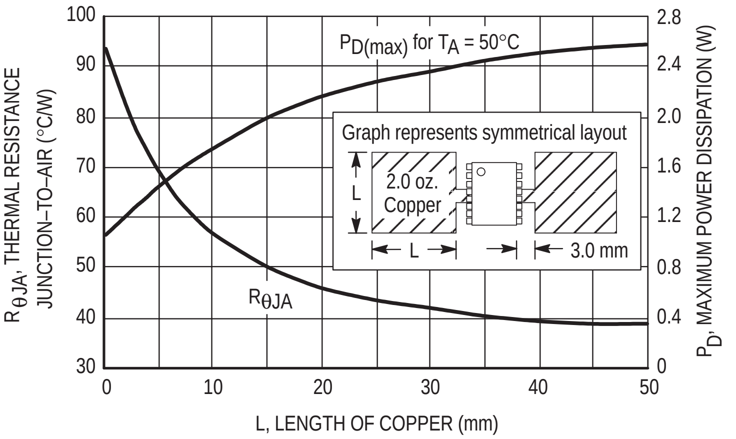


Figure 18. Representative Block Diagram

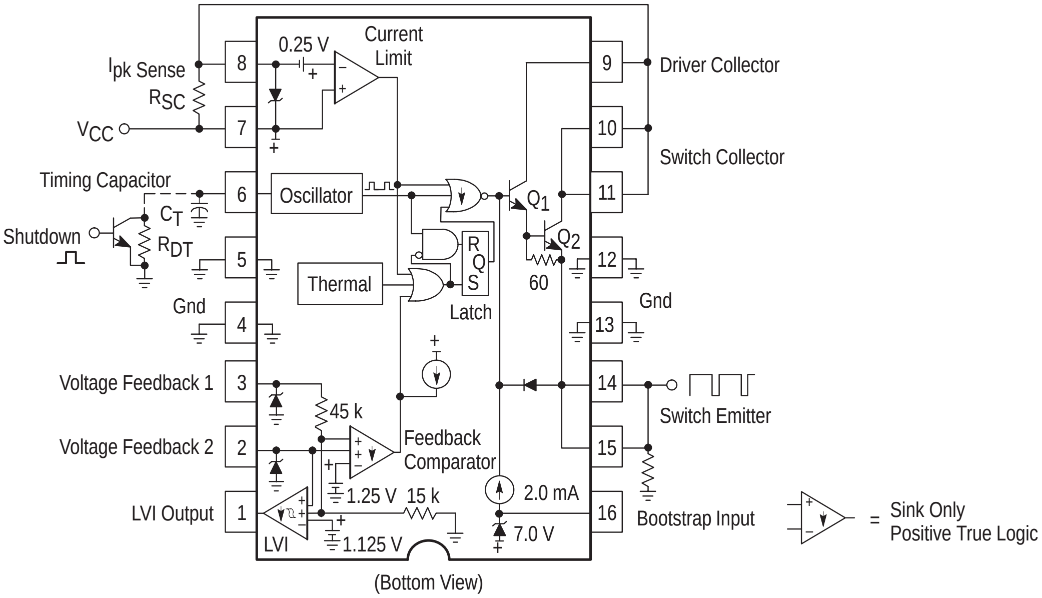
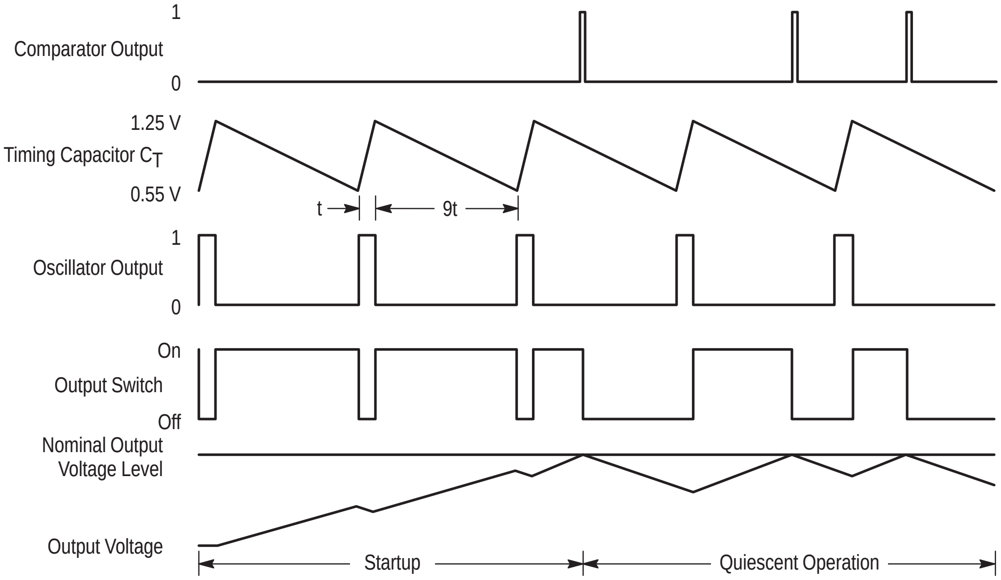


Figure 19. Typical Operating Waveforms



INTRODUCTION

The MC34163 series are monolithic power switching regulators optimized for dc–to–dc converter applications. The combination of features in this series enables the system designer to directly implement step–up, step–down, and voltage–inverting converters with a minimum number of external components. Potential applications include cost sensitive consumer products as well as equipment for the automotive, computer, and industrial markets. A Representative Block Diagram is shown in Figure 18.

OPERATING DESCRIPTION

The MC34163 operates as a fixed on–time, variable off–time voltage mode ripple regulator. In general, this mode of operation is somewhat analogous to a capacitor charge pump and does not require dominant pole loop compensation for converter stability. The Typical Operating Waveforms are shown in Figure 19. The output voltage waveform shown is for a step–down converter with the ripple and phasing exaggerated for clarity. During initial converter startup, the feedback comparator senses that the output voltage level is below nominal. This causes the output switch to turn on and off at a frequency and duty cycle controlled by the oscillator, thus pumping up the output filter capacitor. When the output voltage level reaches nominal, the feedback comparator sets the latch, immediately terminating switch conduction. The feedback comparator will inhibit the switch until the load current causes the output voltage to fall below nominal. Under these conditions, output switch conduction can be inhibited for a partial oscillator cycle, a partial cycle plus a complete cycle, multiple cycles, or a partial cycle plus multiple cycles.

Oscillator

The oscillator frequency and on–time of the output switch are programmed by the value selected for timing capacitor C_T. Capacitor C_T is charged and discharged by a 9 to 1 ratio internal current source and sink, generating a negative going sawtooth waveform at Pin 6. As C_T charges, an internal pulse is generated at the oscillator output. This pulse is connected to the NOR gate center input, preventing output switch conduction, and to the AND gate upper input, allowing the latch to be reset if the comparator output is low. Thus, the output switch is always disabled during ramp–up and can be enabled by the comparator output only at the start of ramp–down. The oscillator peak and valley thresholds are 1.25 V and 0.55 V, respectively, with a charge current of 225 µA and a discharge current of 25 µA, yielding a maximum on–time duty cycle of 90%. A reduction of the maximum duty cycle may be required for specific converter configurations. This can be accomplished with the addition of an external deadtime resistor (R_{DT}) placed across C_T. The resistor increases the discharge current which reduces the on–time of the output switch. A graph of the Output Switch On–Off Time versus Oscillator Timing Capacitance for various values of R_{DT} is shown in Figure 1. Note that the maximum output duty cycle, $t_{on}/t_{on} + t_{off}$, remains constant for values of C_T greater than 0.2 nF. The converter output can be inhibited by clamping C_T to ground with an external NPN small–signal transistor.

Feedback and Low Voltage Indicator Comparators

Output voltage control is established by the Feedback comparator. The inverting input is internally biased at 1.25 V and is not pinned out. The converter output voltage is typically divided down with two external resistors and monitored by the high impedance noninverting input at Pin 2. The maximum input bias current is ±0.4 µA, which can cause an output voltage error that is equal to the product of the input bias current and the upper divider resistance value. For applications that require 5.0 V, the converter output can be directly connected to the noninverting input at Pin 3. The high impedance input, Pin 2, must be grounded to prevent noise pickup. The internal resistor divider is set for a nominal voltage of 5.05 V. The additional 50 mV compensates for a 1.0% voltage drop in the cable and connector from the converter output to the load. The Feedback comparator's output state is controlled by the highest voltage applied to either of the two noninverting inputs.

The Low Voltage Indicator (LVI) comparator is designed for use as a reset controller in microprocessor–based systems. The inverting input is internally biased at 1.125 V, which sets the noninverting input thresholds to 90% of nominal. The LVI comparator has 15 mV of hysteresis to prevent erratic reset operation. The Open Collector output is capable of sinking in excess of 6.0 mA (see Figure 10). An external resistor (R_{LVI}) and capacitor (C_{DLY}) can be used to program a reset delay time (t_{DLY}) by the formula shown below, where $V_{th(MPU)}$ is the microprocessor reset input threshold. Refer to Figure 20.

$$t_{DLY} = R_{LVI}\, C_{DLY} \ln \left(\frac{1}{1 - \frac{V_{th(MPU)}}{V_{out}}} \right)$$

Current Limit Comparator, Latch and Thermal Shutdown

With a voltage mode ripple converter operating under normal conditions, output switch conduction is initiated by the oscillator and terminated by the Voltage Feedback comparator. Abnormal operating conditions occur when the converter output is overloaded or when feedback voltage sensing is lost. Under these conditions, the Current Limit comparator will protect the Output Switch.

The switch current is converted to a voltage by inserting a fractional ohm resistor, R_{SC}, in series with V_{CC} and output switch transistor Q_2. The voltage drop across R_{SC} is monitored by the Current Sense comparator. If the voltage drop exceeds 250 mV with respect to V_{CC}, the comparator will set the latch and terminate output switch conduction on a cycle–by–cycle basis. This Comparator/Latch configuration ensures that the Output Switch has only a single on–time during a given oscillator cycle. The calculation for a value of R_{SC} is:

$$R_{SC} = \frac{0.25\ V}{I_{pk\,(Switch)}}$$

Figures 11 and 12 show that the Current Sense comparator threshold is tightly controlled over temperature and has a typical input bias current of 1.0 µA. The propagation delay from the comparator input to the Output Switch is typically 200 ns. The parasitic inductance associated with R_{SC} and the circuit layout should be minimized. This will prevent unwanted voltage spikes that may falsely trip the Current Limit comparator.

Internal thermal shutdown circuitry is provided to protect the IC in the event that the maximum junction temperature is exceeded. When activated, typically at 170°C, the Latch is forced into the "Set" state, disabling the Output Switch. This feature is provided to prevent catastrophic failures from accidental device overheating. It is not intended to be used as a replacement for proper heatsinking.

Driver and Output Switch

To aid in system design flexibility and conversion efficiency, the driver current source and collector, and output switch collector and emitter are pinned out separately. This allows the designer the option of driving the output switch into saturation with a selected force gain or driving it near saturation when connected as a Darlington. The output switch has a typical current gain of 70 at 2.5 A and is designed to switch a maximum of 40 V collector to emitter, with up to 3.4 A peak collector current. The minimum value for R_{SC} is:

$$R_{SC(min)} = \frac{0.25\,V}{3.4\ A} = 0.0735\ \Omega$$

When configured for step–down or voltage–inverting applications, as in Figures 20 and 24, the inductor will forward bias the output rectifier when the switch turns off. Rectifiers with a high forward voltage drop or long turn–on delay time should not be used. If the emitter is allowed to go sufficiently negative, collector current will flow, causing additional device heating and reduced conversion efficiency.

Figure 9 shows that by clamping the emitter to 0.5 V, the collector current will be in the range 10 µA over temperature. A 1N5822 or equivalent Schottky barrier rectifier is recommended to fulfill these requirements.

A bootstrap input is provided to reduce the output switch saturation voltage in step–down and voltage–inverting converter applications. This input is connected through a series resistor and capacitor to the switch emitter and is used to raise the internal 2.0 mA bias current source above V_{CC}. An internal zener limits the bootstrap input voltage to V_{CC} +7.0 V. The capacitor's equivalent series resistance must limit the zener current to less than 100 mA. An additional series resistor may be required when using tantalum or other low ESR capacitors. The equation below is used to calculate a minimum value bootstrap capacitor based on a minimum zener voltage and an upper limit current source.

$$C_{B(min)} = I\,\frac{\Delta t}{\Delta V} = 4.0\ mA\ \frac{t_{on}}{4.0\,V} = 0.001\,t_{on}$$

Parametric operation of the MC34163 is guaranteed over a supply voltage range of 2.5 V to 40 V. When operating below 3.0 V, the Bootstrap Input should be connected to V_{CC}. Figure 15 shows that functional operation down to 1.7 V at room temperature is possible.

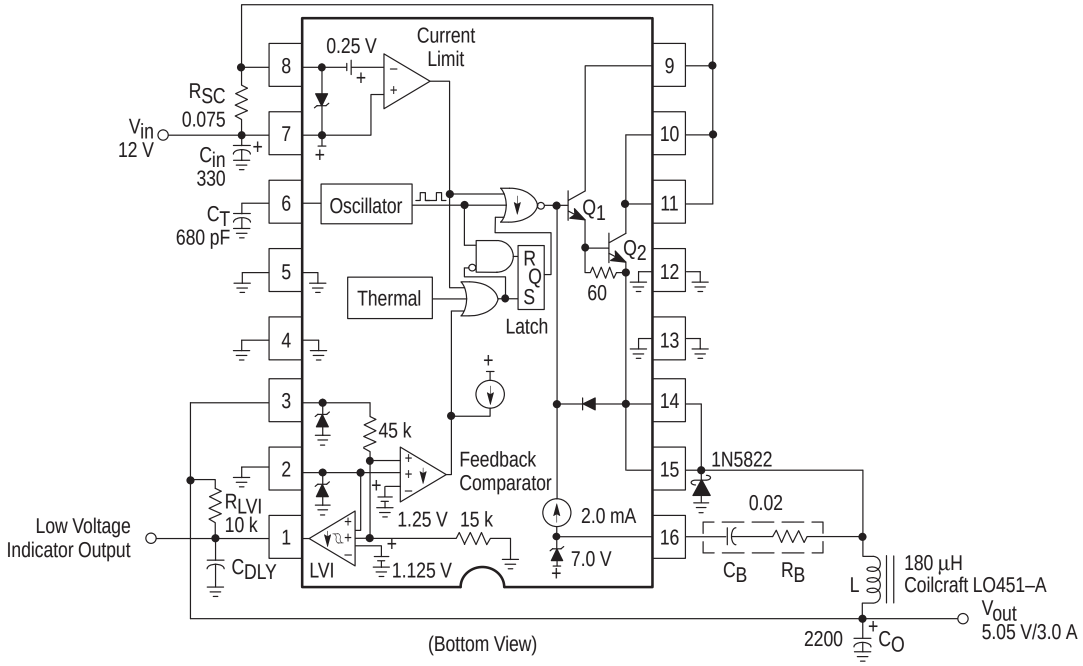
Package

The MC34163 is contained in a heatsinkable 16–lead plastic dual–in–line package in which the die is mounted on a special heat tab copper alloy lead frame. This tab consists of the four center ground pins that are specifically designed to improve thermal conduction from the die to the circuit board. Figures 16 and 17 show a simple and effective method of utilizing the printed circuit board medium as a heat dissipater by soldering these pins to an adequate area of copper foil. This permits the use of standard layout and mounting practices while having the ability to halve the junction–to–air thermal resistance. These examples are for a symmetrical layout on a single–sided board with two ounce per square foot of copper.

APPLICATIONS

The following converter applications show the simplicity and flexibility of this circuit architecture. Three main converter topologies are demonstrated with actual test data shown below each of the circuit diagrams.

Figure 20. Step–Down Converter



Test	Condition	Results
Line Regulation	V_{in} = 8.0 V to 24 V, I_O = 3.0 A	6.0 mV = ± 0.06%
Load Regulation	V_{in} = 12 V, I_O = 0.6 A to 3.0 A	2.0 mV = ± 0.02%
Output Ripple	V_{in} = 12 V, I_O = 3.0 A	36 mVpp
Short Circuit Current	V_{in} = 12 V, R_L = 0.1 Ω	3.3 A
Efficiency, Without Bootstrap	V_{in} = 12 V, I_O = 3.0 A	76.7%
Efficiency, With Bootstrap	V_{in} = 12 V, I_O = 3.0 A	81.2%

Figure 21. External Current Boost Connections for $I_{pk\ (Switch)}$ Greater Than 3.4 A

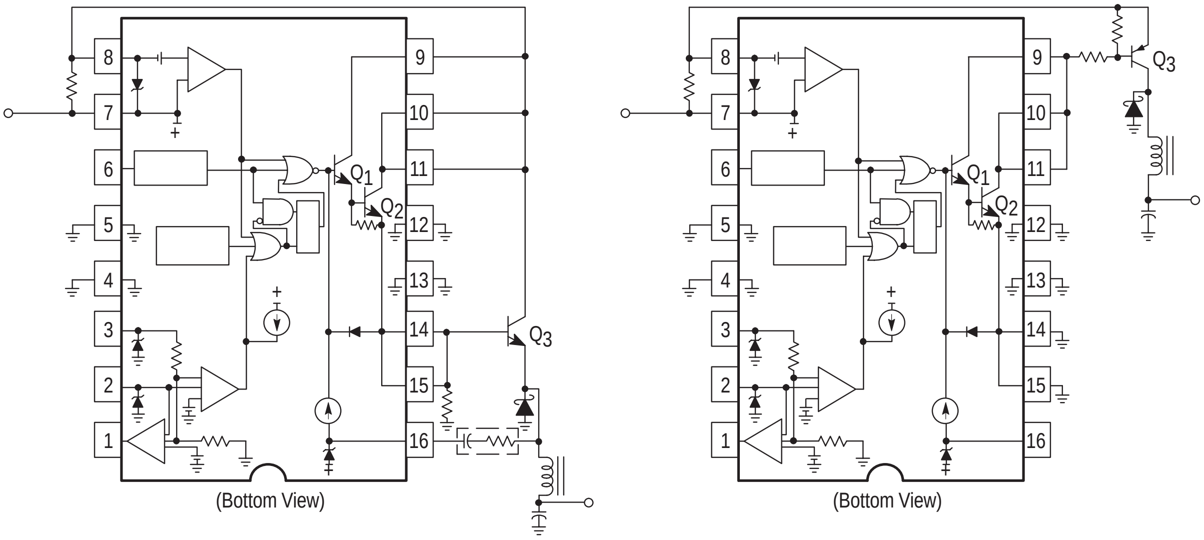
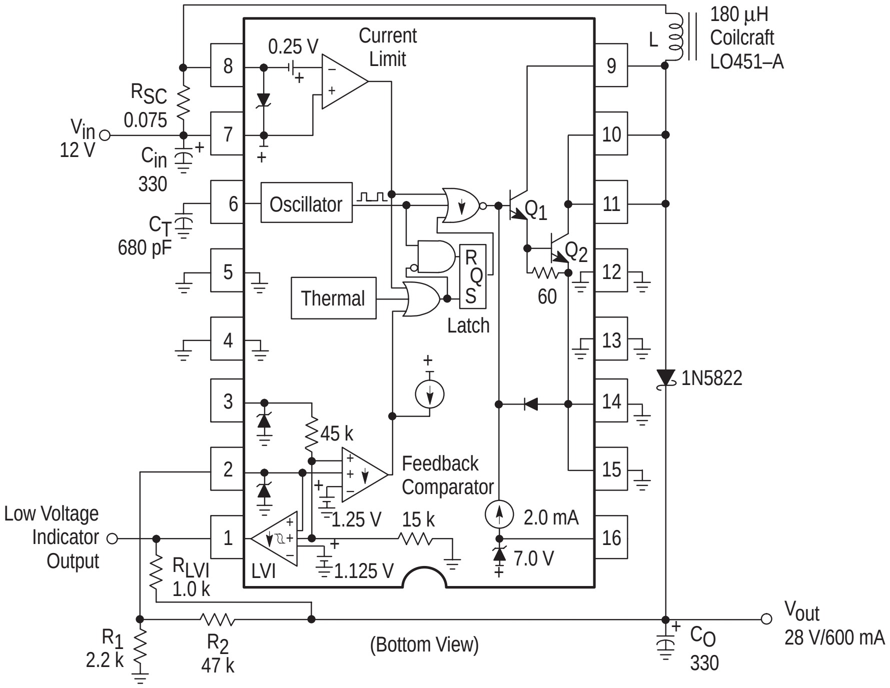


Figure 21A. External NPN Switch

Figure 21B. External PNP Saturated Switch

Figure 22. Step–Up Converter



Test	Condition	Results
Line Regulation	V_{in} = 9.0 V to 16 V, I_O = 0.6 A	30 mV = ± 0.05%
Load Regulation	V_{in} = 12 V, I_O = 0.1 A to 0.6 A	50 mV = ± 0.09%
Output Ripple	V_{in} = 12 V, I_O = 0.6 A	140 mVpp
Efficiency	V_{in} = 12 V, I_O = 0.6 A	88.1%

Figure 23. External Current Boost Connections for $I_{pk\ (Switch)}$ Greater Than 3.4 A

Figure 23A. External NPN Switch

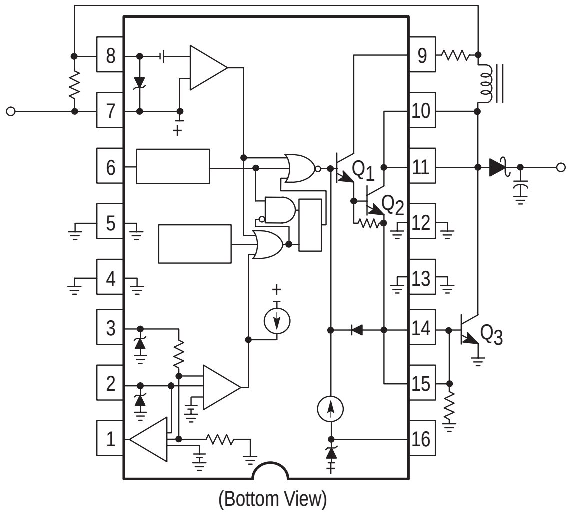


Figure 23B. External PNP Saturated Switch

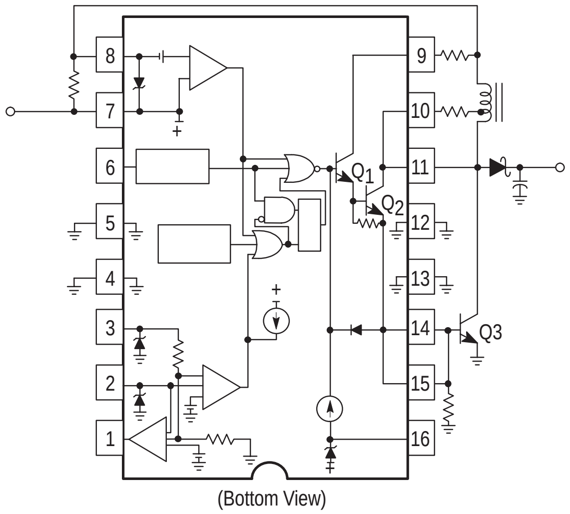
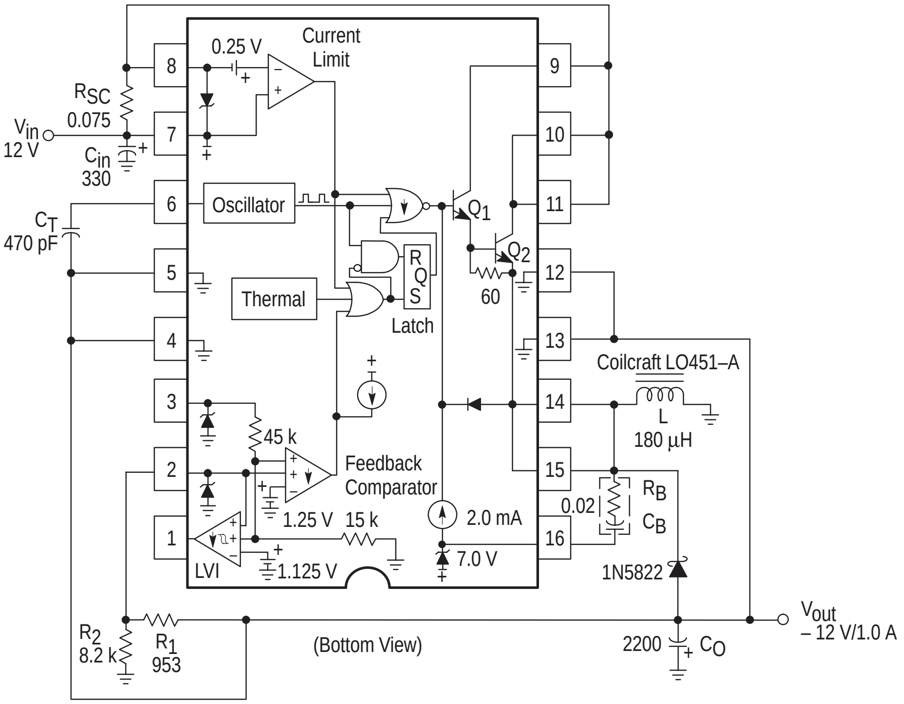


Figure 24. Voltage–Inverting Converter



Test	Condition	Results
Line Regulation	V_{in} = 9.0 V to 16 V, I_O = 1.0 A	5.0 mV = ± 0.02%
Load Regulation	V_{in} = 12 V, I_O = 0.6 A to 1.0 A	2.0 mV = ± 0.01%
Output Ripple	V_{in} = 12 V, I_O = 1.0 A	130 mVpp
Short Circuit Current	V_{in} = 12 V, R_L = 0.1 Ω	3.2 A
Efficiency, Without Bootstrap	V_{in} = 12 V, I_O = 1.0 A	73.1%
Efficiency, With Bootstrap	V_{in} = 12 V, I_O = 1.0 A	77.5%

Figure 25. External Current Boost Connections for $I_{pk\ (Switch)}$ Greater Than 3.4 A

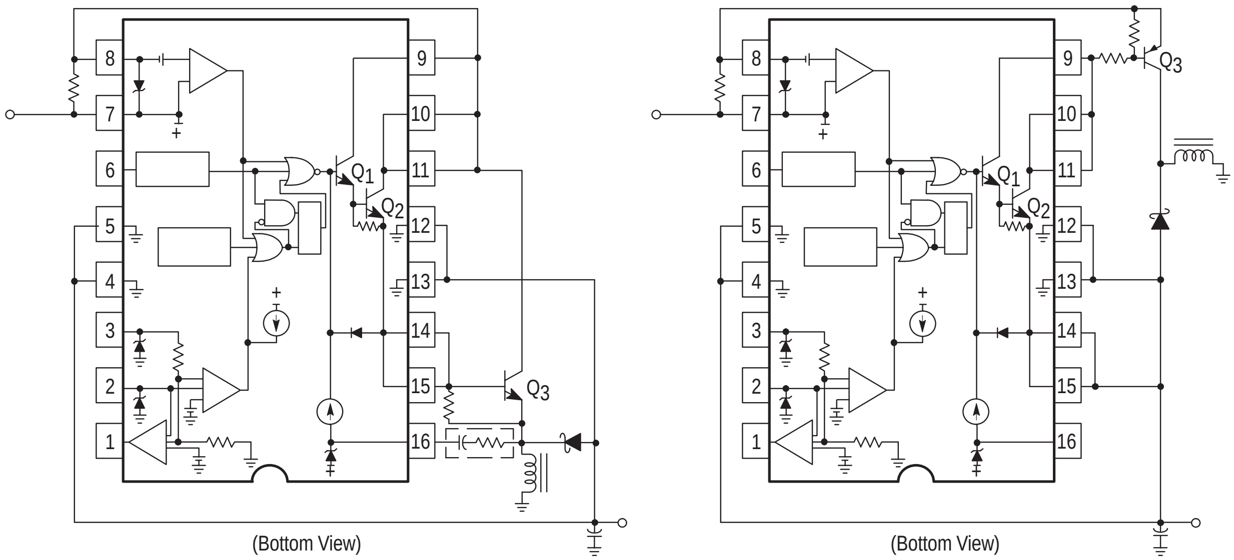
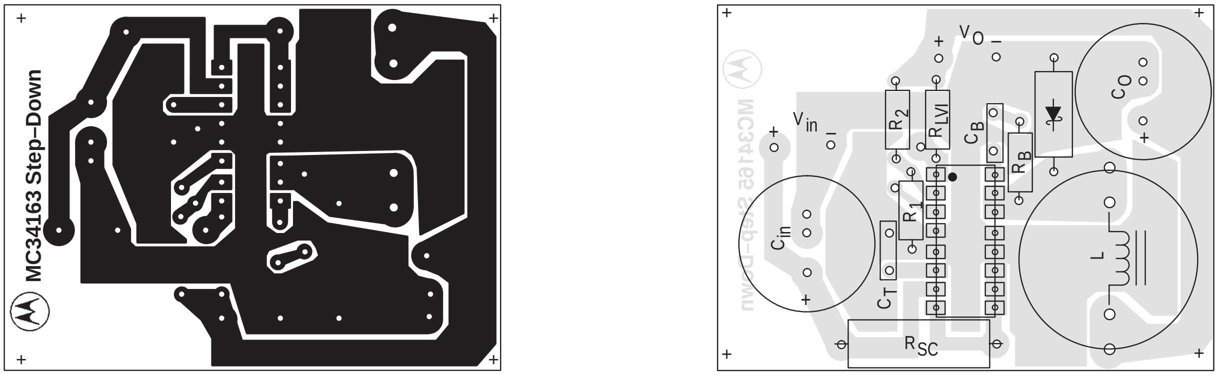


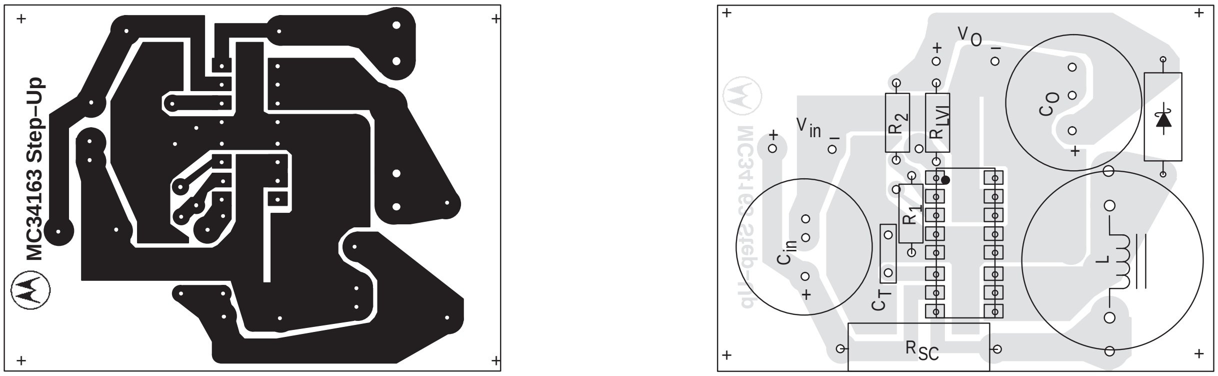
Figure 25A. External NPN Switch

Figure 25B. External PNP Saturated Switch

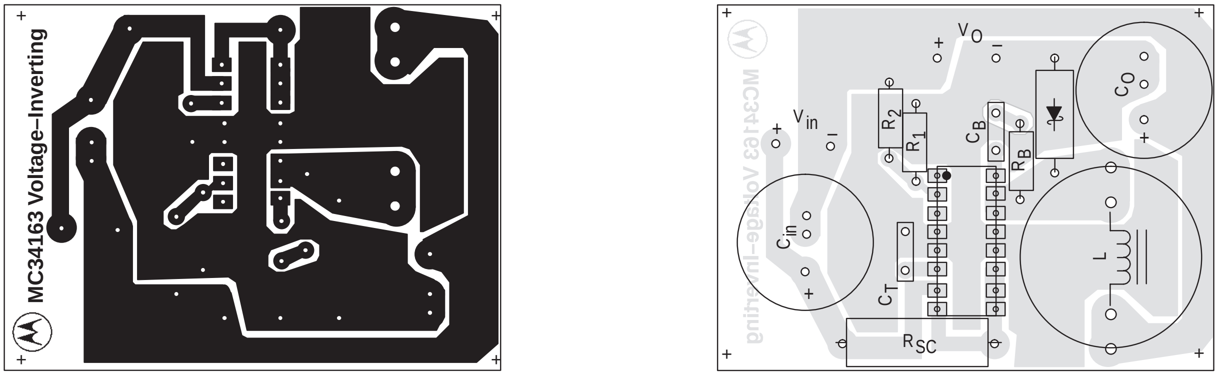
Figure 26. Printed Circuit Board and Component Layout
(Circuits of Figures 20, 22, 24)



Bottom View Top View



Bottom View Top View



Bottom View Top View

All printed circuit boards are 2.58” in width by 1.9” in height.

Figure 27. Design Equations

Calculation	Step–Down	Step–Up	Voltage–Inverting
$\frac{t_{on}}{t_{off}}$ (Notes 1, 2, 3)	$\frac{V_{out} + V_F}{V_{in} - V_{sat} - V_{out}}$	$\frac{V_{out} + V_F - V_{in}}{V_{in} - V_{sat}}$	$\frac{\lvert V_{out} \rvert + V_F}{V_{in} - V_{sat}}$
t_{on}	$\frac{\frac{t_{on}}{t_{off}}}{f\left(\frac{t_{on}}{t_{off}} + 1\right)}$	$\frac{\frac{t_{on}}{t_{off}}}{f\left(\frac{t_{on}}{t_{off}} + 1\right)}$	$\frac{\frac{t_{on}}{t_{off}}}{f\left(\frac{t_{on}}{t_{off}} + 1\right)}$
C_T	$\frac{32.143 \cdot 10^{-6}}{f}$	$\frac{32.143 \cdot 10^{-6}}{f}$	$\frac{32.143 \cdot 10^{-6}}{f}$
$I_{L(avg)}$	I_{out}	$I_{out}\left(\frac{t_{on}}{t_{off}} + 1\right)$	$I_{out}\left(\frac{t_{on}}{t_{off}} + 1\right)$
I_{pk} (Switch)	$I_{L(avg)} + \frac{\Delta I_L}{2}$	$I_{L(avg)} + \frac{\Delta I_L}{2}$	$I_{L(avg)} + \frac{\Delta I_L}{2}$
R_{SC}	$\frac{0.25}{I_{pk}\ (\text{Switch})}$	$\frac{0.25}{I_{pk}\ (\text{Switch})}$	$\frac{0.25}{I_{pk}\ (\text{Switch})}$
L	$\left(\frac{V_{in} - V_{sat} - V_{out}}{\Delta I_L}\right) t_{on}$	$\left(\frac{V_{in} - V_{sat}}{\Delta I_L}\right) t_{on}$	$\left(\frac{V_{in} - V_{sat}}{\Delta I_L}\right) t_{on}$
$V_{ripple(pp)}$	$\Delta I_L \sqrt{\left(\frac{1}{8 f C_O}\right)^2 + (ESR)^2}$	$\approx \frac{t_{on}\, I_{out}}{C_O}$	$\approx \frac{t_{on}\, I_{out}}{C_O}$
V_{out}	$V_{ref}\left(\frac{R_2}{R_1} + 1\right)$	$V_{ref}\left(\frac{R_2}{R_1} + 1\right)$	$V_{ref}\left(\frac{R_2}{R_1} + 1\right)$

The following Converter Characteristics must be chosen:

V_{in} – Nominal operating input voltage.
V_{out} – Desired output voltage.
I_{out} – Desired output current.
ΔI_L – Desired peak–to–peak inductor ripple current. For maximum output current it is suggested that ΔI_L be chosen to be less than 10% of the average inductor current $I_{L(avg)}$. This will help prevent $I_{pk\ (Switch)}$ from reaching the current limit threshold set by R_{SC}. If the design goal is to use a minimum inductance value, let $\Delta I_L = 2(I_{L(avg)})$. This will proportionally reduce converter output current capability.
f – Maximum output switch frequency.
$V_{ripple(pp)}$ – Desired peak–to–peak output ripple voltage. For best performance the ripple voltage should be kept to a low value since it will directly affect line and load regulation. Capacitor C_O should be a low equivalent series resistance (ESR) electrolytic designed for switching regulator applications.

NOTES:
1. V_{sat} – Saturation voltage of the output switch, refer to Figures 7 and 8.
2. V_F – Output rectifier forward voltage drop. Typical value for 1N5822 Schottky barrier rectifier is 0.5 V.
3. The calculated t_{on}/t_{off} must not exceed the minimum guaranteed oscillator charge to discharge ratio of 8, at the minimum operating input voltage.

MC34164
MC33164

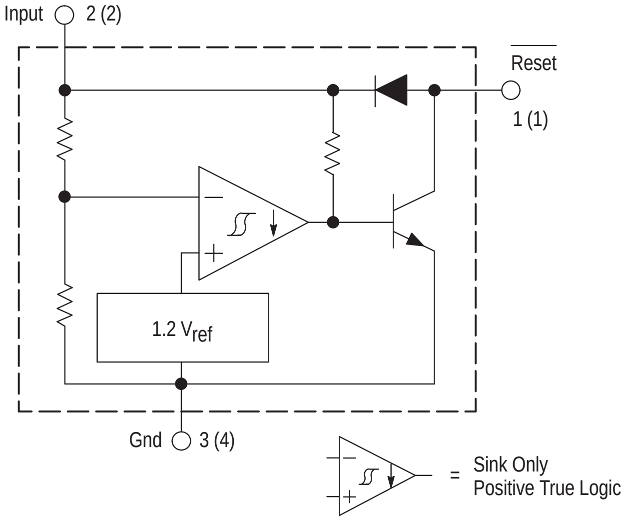
Micropower Undervoltage Sensing Circuits

The MC34164 series are undervoltage sensing circuits specifically designed for use as reset controllers in portable microprocessor based systems where extended battery life is required. These devices offer the designer an economical solution for low voltage detection with a single external resistor. The MC34164 series features a bandgap reference, a comparator with precise thresholds and built–in hysteresis to prevent erratic reset operation, an open collector reset output capable of sinking in excess of 6.0 mA, and guaranteed operation down to 1.0 V input with extremely low standby current. These devices are packaged in 3–pin TO–226AA, 8–pin SO–8 and Micro–8 surface mount packages.

Applications include direct monitoring of the 3.0 or 5.0 V MPU/logic power supply used in appliance, automotive, consumer, and industrial equipment.

- Temperature Compensated Reference
- Monitors 3.0 V (MC34164–3) or 5.0 V (MC34164–5) Power Supplies
- Precise Comparator Thresholds Guaranteed Over Temperature
- Comparator Hysteresis Prevents Erratic Reset
- Reset Output Capable of Sinking in Excess of 6.0 mA
- Internal Clamp Diode for Discharging Delay Capacitor
- Guaranteed Reset Operation With 1.0 V Input
- Extremely Low Standby Current: As Low as 9.0 µA
- Economical TO–226AA, SO–8 and Micro–8 Surface Mount Packages

Representative Block Diagram



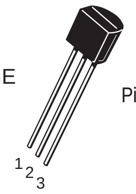
Pin numbers adjacent to terminals are for the 3–pin TO–226AA package.
Pin numbers in parenthesis are for the 8–lead packages.

This device contains 28 active transistors.

MICROPOWER UNDERVOLTAGE SENSING CIRCUITS

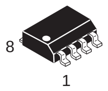
SEMICONDUCTOR TECHNICAL DATA

P SUFFIX
PLASTIC PACKAGE
CASE 29
(TO–226AA)

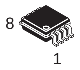


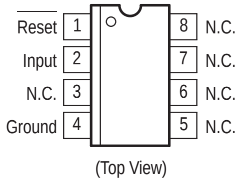
Pin 1. $\overline{\text{Reset}}$
2. Input
3. Ground

D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)



DM SUFFIX
PLASTIC PACKAGE
CASE 846A
(Micro–8)





ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC34164D–3	T_A = 0° to +70°C	SO–8
MC34164D–5		
MC34164DM–3		Micro–8
MC34164DM–5		
MC34164P–3		TO–226AA
MC34164P–5		
MC33164D–3	T_A = –40° to +125°C	SO–8
MC33164D–5		
MC33164DM–3		Micro–8
MC33164DM–5		
MC33164P–3		TO–226AA
MC33164P–5		

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Input Supply Voltage	V_{in}	–1.0 to 12	V
$\overline{\text{Reset}}$ Output Voltage	V_O	–1.0 to 12	V
$\overline{\text{Reset}}$ Output Sink Current	I_{Sink}	Internally Limited	mA
Clamp Diode Forward Current, Pin 1 to 2 (Note 1)	I_F	100	mA
Power Dissipation and Thermal Characteristics			
P Suffix, Plastic Package			
Maximum Power Dissipation @ T_A = 25°C	P_D	700	mW
Thermal Resistance, Junction–to–Air	$R_{\theta JA}$	178	°C/W
D Suffix, Plastic Package			
Maximum Power Dissipation @ T_A = 25°C	P_D	700	mW
Thermal Resistance, Junction–to–Air	$R_{\theta JA}$	178	°C/W
DM Suffix, Plastic Package			
Maximum Power Dissipation @ T_A = 25°C	P_D	520	mW
Thermal Resistance, Junction–to–Air	$R_{\theta JA}$	240	°C/W
Operating Junction Temperature	T_J	+150	°C
Operating Ambient Temperature Range	T_A		°C
MC34164 Series		0 to +70	
MC33164 Series		– 40 to + 85	
Storage Temperature Range	T_{stg}	– 65 to +150	°C

NOTE: ESD data available upon request.

MC34164–3, MC33164–3 SERIES

ELECTRICAL CHARACTERISTICS (For typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies [Notes 2 & 3], unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
COMPARATOR					
Threshold Voltage					V
High State Output (V_{in} Increasing)	V_{IH}	2.55	2.71	2.80	
Low State Output (V_{in} Decreasing)	V_{IL}	2.55	2.65	2.80	
Hysteresis (I_{Sink} = 100 μA)	V_H	0.03	0.06	–	
$\overline{\text{RESET}}$ OUTPUT					
Output Sink Saturation	V_{OL}				V
(V_{in} = 2.4 V, I_{Sink} = 1.0 mA)		–	0.14	0.4	
(V_{in} = 1.0 V, I_{Sink} = 0.25 mA)		–	0.1	0.3	
Output Sink Current (V_{in}, $\overline{\text{Reset}}$ = 2.4 V)	I_{Sink}	6.0	12	30	mA
Output Off–State Leakage	$I_{\overline{R}(leak)}$				μA
(V_{in}, $\overline{\text{Reset}}$ = 3.0 V)		–	0.02	0.5	
(V_{in}, $\overline{\text{Reset}}$ = 10 V)		–	0.02	1.0	
Clamp Diode Forward Voltage, Pin 1 to 2 (I_F = 5.0 mA)	V_F	6.0	0.9	1.2	V
TOTAL DEVICE					
Operating Input Voltage Range	V_{in}	1.0 to 10	–	–	V
Quiescent Input Current	I_{in}				μA
V_{in} = 3.0 V		–	9.0	15	
V_{in} = 6.0 V		–	24	40	

NOTES: 1. Maximum package power dissipation limits must be observed.
2. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
3. T_{low} = 0°C for MC34164 T_{high} = + 70°C for MC34164
– 40°C for MC33164 = + 85°C for MC33164

MC34164–5, MC33164–5 SERIES

ELECTRICAL CHARACTERISTICS (For typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies [Notes 2 & 3], unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
COMPARATOR					
Threshold Voltage					V
High State Output (V_{in} Increasing)	V_{IH}	4.15	4.33	4.45	
Low State Output (V_{in} Decreasing)	V_{IL}	4.15	4.27	4.45	
Hysteresis (I_{Sink} = 100 μA)	V_H	0.02	0.09	–	
RESET OUTPUT					
Output Sink Saturation	V_{OL}				V
(V_{in} = 4.0 V, I_{Sink} = 1.0 mA)		–	0.14	0.4	
(V_{in} = 1.0 V, I_{Sink} = 0.25 mA)		–	0.1	0.3	
Output Sink Current (V_{in}, Reset = 4.0 V)	I_{Sink}	7.0	20	50	mA
Output Off–State Leakage	$I_{\overline{R}(leak)}$				μA
(V_{in}, Reset = 5.0 V)		–	0.02	0.5	
(V_{in}, Reset = 10 V)		–	0.02	2.0	
Clamp Diode Forward Voltage, Pin 1 to 2 (I_F = 5.0 mA)	V_F	0.6	0.9	1.2	V
TOTAL DEVICE					
Operating Input Voltage Range	V_{in}	1.0 to 10	–	–	V
Quiescent Input Current	I_{in}				μA
V_{in} = 5.0 V		–	12	20	
V_{in} = 10 V		–	32	50	

NOTES: 2. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
3. T_{low} = 0°C for MC34164 T_{high} = + 70°C for MC34164
– 40°C for MC33164 = + 85°C for MC33164

Figure 1. MC3X164–3 Reset Output Voltage versus Input Voltage

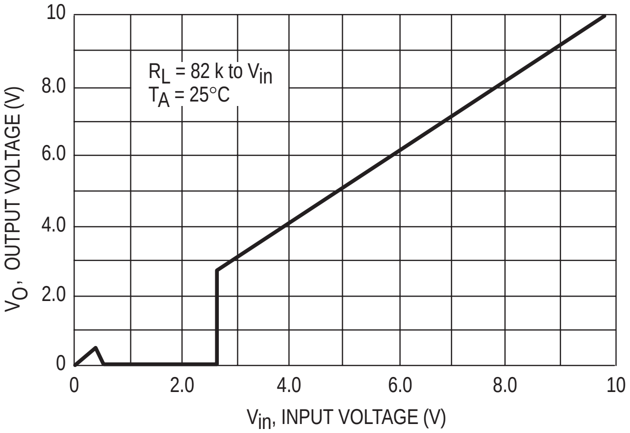


Figure 2. MC3X164–5 Reset Output Voltage versus Input Voltage

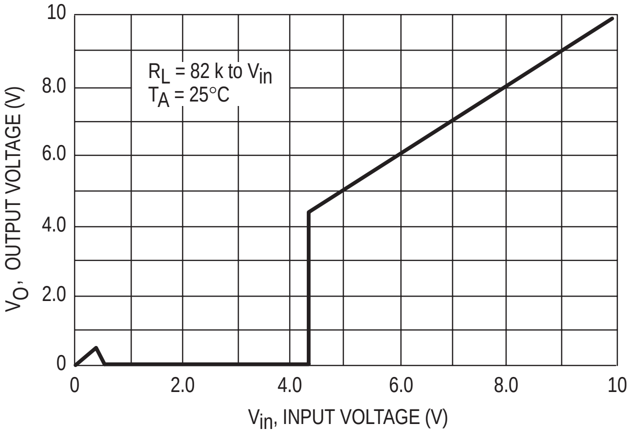


Figure 3. MC3X164–3 Reset Output Voltage versus Input Voltage

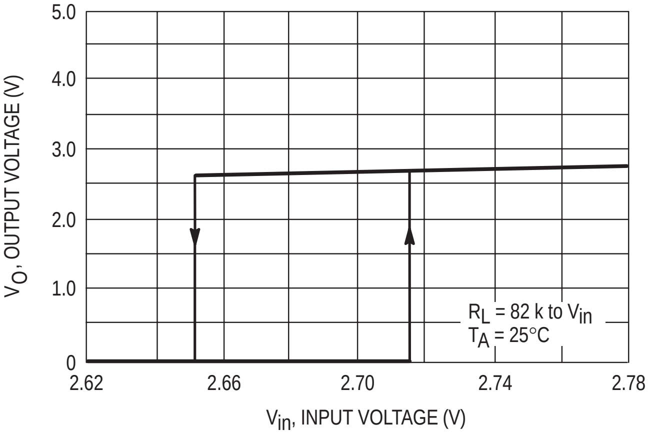


Figure 4. MC3X164–5 Reset Output Voltage versus Input Voltage

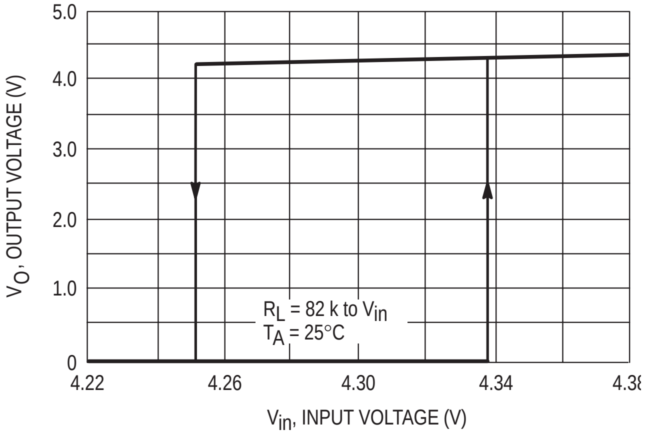


Figure 5. MC3X164–3 Comparator Threshold Voltage versus Temperature

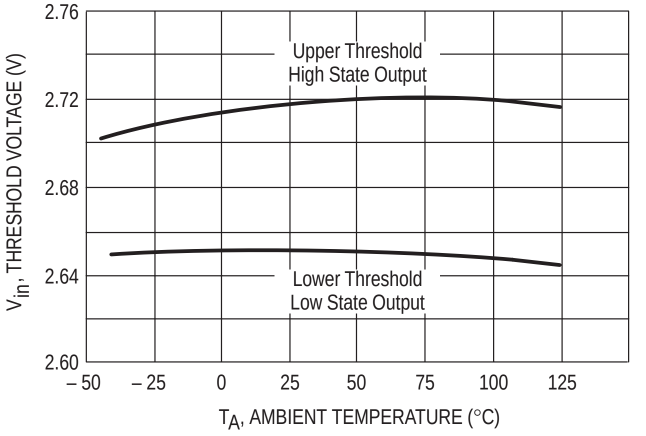


Figure 6. MC3X164–5 Comparator Threshold Voltage versus Temperature

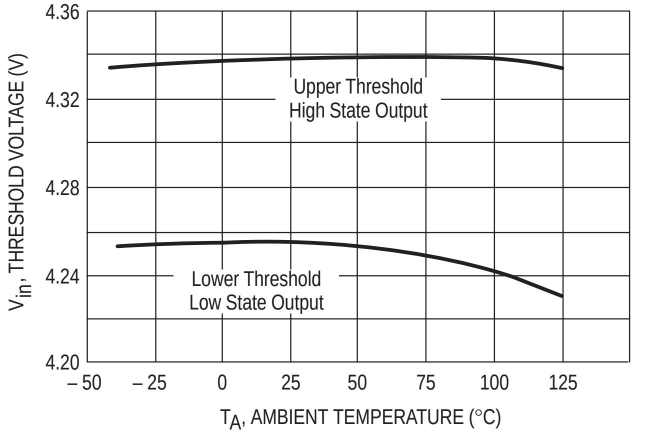


Figure 7. MC3X164–3 Input Current versus Input Voltage

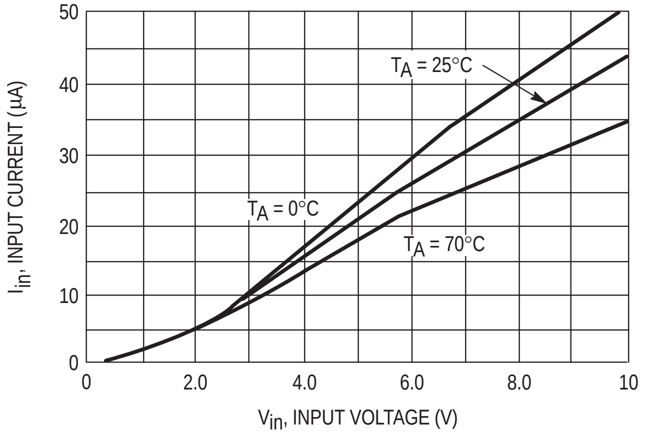


Figure 8. MC3X164–5 Input Current versus Input Voltage

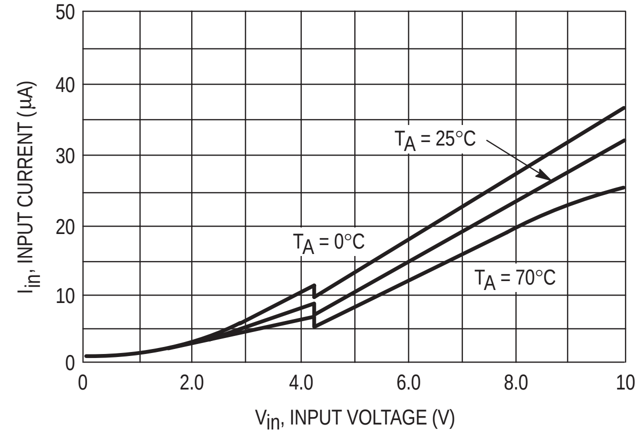


Figure 9. MC3X164–3 Reset Output Saturation versus Sink Current

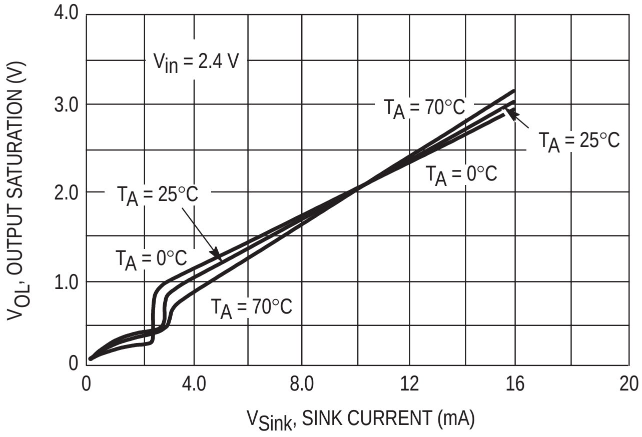


Figure 10. MC3X164–5 Reset Output Saturation versus Sink Current

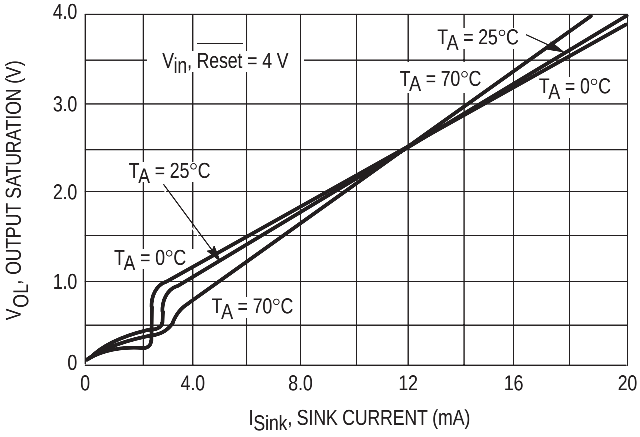


Figure 11. Clamp Diode Forward Current versus Voltage

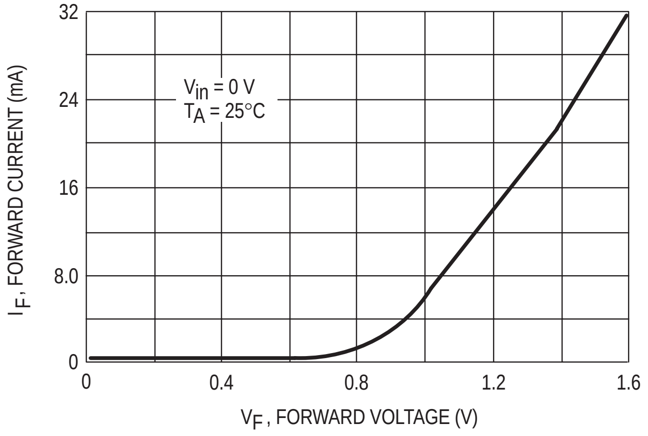


Figure 12. $\overline{\text{Reset}}$ Delay Time (MC3X164–5 Shown)

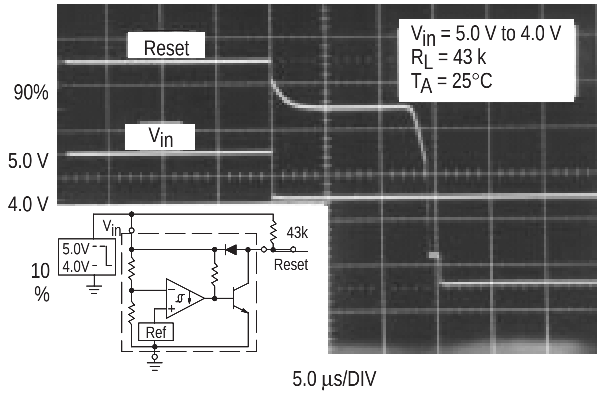
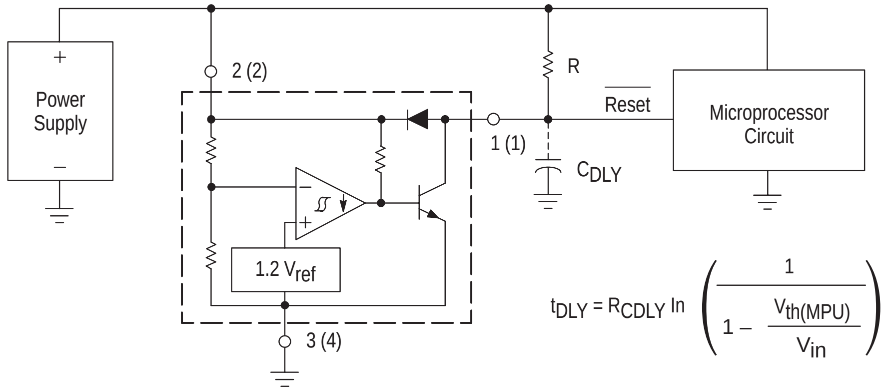


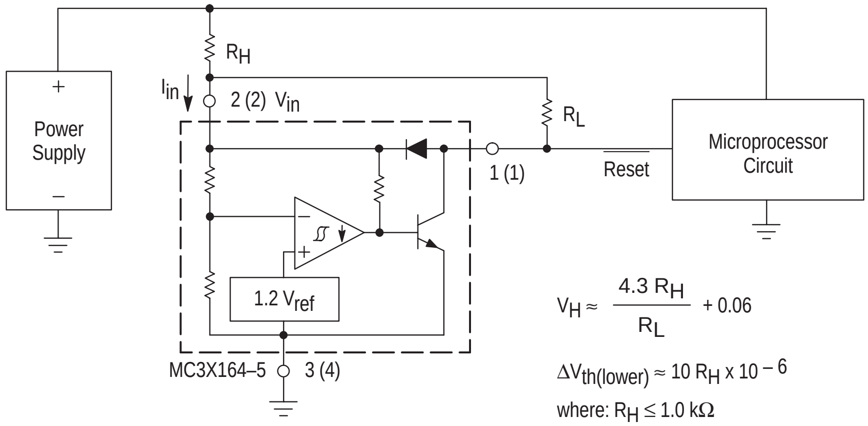
Figure 13. Low Voltage Microprocessor Reset



$$t_{DLY} = RC_{DLY} \ln \left(\frac{1}{1 - \frac{V_{th(MPU)}}{V_{in}}} \right)$$

A time delayed reset can be accomplished with the addition of C_{DLY}. For systems with extremely fast power supply rise times (< 500 ns) it is recommended that the RCDLY time constant be greater than 5.0 µs. $V_{th(MPU)}$ is the microprocessor reset input threshold.

Figure 14. Low Voltage Microprocessor Reset With Additional Hysteresis (MC3X164–5 Shown)



$V_H \approx \frac{4.3\ R_H}{R_L} + 0.06$

$\Delta V_{th(lower)} \approx 10\ R_H \times 10^{-6}$

where: $R_H \le 1.0\ k\Omega$

$43\ k\Omega \ge R_L \ge 4.3\ k\Omega$

Test Data			
V_H (mV)	ΔV_{th} (mV)	R_H (Ω)	R_L (kΩ)
60	0	0	43
103	1.0	100	10
123	1.0	100	6.8
160	1.0	100	4.3
155	2.2	220	10
199	2.2	220	6.8
280	2.2	220	4.3
262	4.7	470	10
306	4.7	470	8.2
357	4.7	470	6.8
421	4.7	470	5.6
530	4.7	470	4.3

Comparator hysteresis can be increased with the addition of resistor R_H. The hysteresis equation has been simplified and does not account for the change of input current I_{in} as V_{in} crosses the comparator threshold (Figure 8). An increase of the lower threshold $\Delta V_{th(lower)}$ will be observed due to I_{in} which is typically 10 µA at 4.3 V. The equations are accurate to ±10% with R_H less than 1.0 kΩ and R_L between 4.3 kΩ and 43 kΩ.

Figure 15. Voltage Monitor

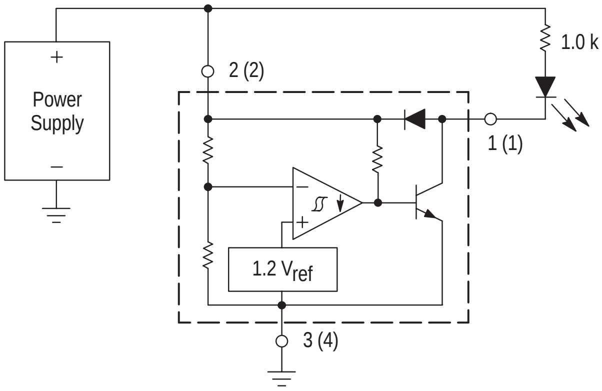


Figure 16. Solar Powered Battery Charger

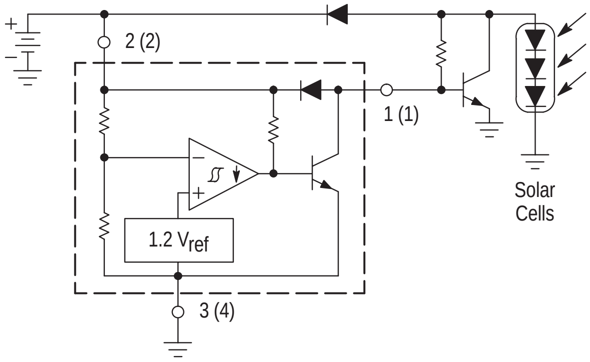
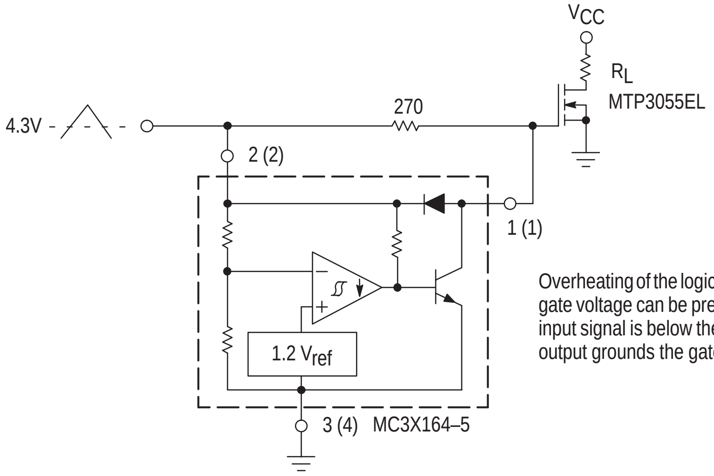


Figure 17. MOSFET Low Voltage Gate Drive Protection Using the MC3X164–5



Overheating of the logic level power MOSFET due to insufficient gate voltage can be prevented with the above circuit. When the input signal is below the 4.3 V threshold of the MC3X164–5, its output grounds the gate of the L^2 MOSFET.

MOTOROLA

MC34165
MC33165

Power Switching Regulators

POWER SWITCHING REGULATORS

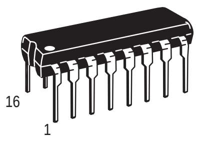
SEMICONDUCTOR TECHNICAL DATA

The MC34165 series are monolithic power switching regulators that contain the primary functions required for DC–to–DC converters. This series is specifically designed to be incorporated in step–up, step–down, and voltage–inverting applications with a minimum number of external components.

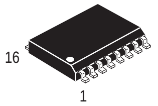
These devices consist of two high gain voltage feedback comparators, temperature compensated reference, controlled duty cycle oscillator, driver with bootstrap capability for increased efficiency, and a high current output switch. Protective features consist of cycle–by–cycle current limiting, and internal thermal shutdown. Also included is a low voltage indicator output designed to interface with microprocessor based systems.

These devices are contained in a 16 pin dual–in–line heat tab plastic package for improved thermal conduction.

- Output Switch Current in Excess of 1.5 A
- Operation from 3.0 V to 65 V Input
- Low Standby Current
- Precision 2% Reference
- Controlled Duty Cycle Oscillator
- Driver with Bootstrap Capability for Increased Efficiency
- Cycle–by–Cycle Current Limiting
- Internal Thermal Shutdown Protection
- Low Voltage Indicator Output for Direct Microprocessor Interface
- Heat Tab Power Package

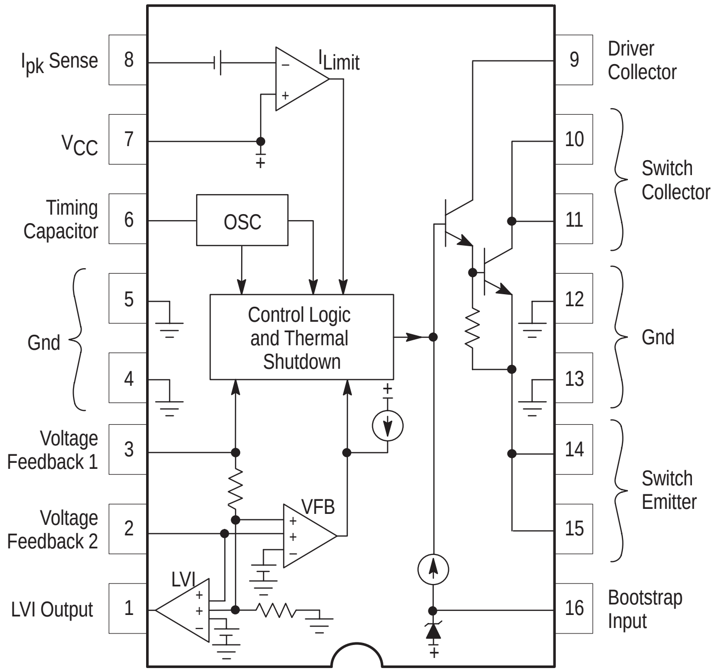


P SUFFIX
PLASTIC PACKAGE
CASE 648C
(DIP–16)



DW SUFFIX
PLASTIC PACKAGE
CASE 751G
(SOP–16L)

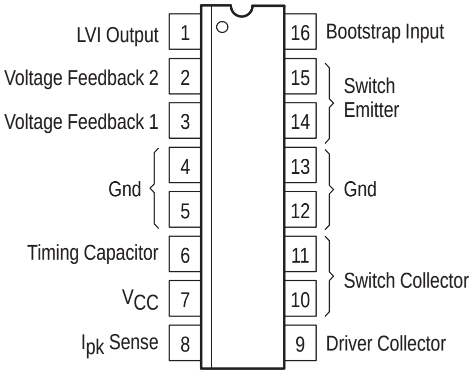
Representative Block Diagram



(Bottom View)

This device contains 114 active transistors.

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Tested Operating Temperature Range	Package
MC34165DW	T_A = 0° to +70°C	SOP–16L
MC34165P		DIP–16
MC33165DW	T_A = – 40° to +85°C	SOP–16L
MC33165P		DIP–16

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Input Voltage	V_{CC}	65	V
Switch Collector Voltage Range	$V_{C(switch)}$	–1.0 to + 65	V
Switch Emitter Voltage Range	$V_{E(switch)}$	– 2.0 to $V_{C(switch)}$	V
Switch Collector to Emitter Voltage	$V_{CE(switch)}$	65	V
Switch Current (Note 1)	I_{SW}	1.5	A
Driver Collector Voltage	$V_{C(driver)}$	–1.0 to +65	V
Driver Collector Current	$I_{C(driver)}$	70	mA
Bootstrap Input Current Range (Note 1)	I_{BS}	–100 to +100	mA
Current Sense Input Voltage Range	$V_{Ipk(Sense)}$	(V_{CC}–7.0) to (V_{CC}+1.0)	V
Feedback and Timing Capacitor Input Voltage Range	V_{in}	–1.0 to + 7.0	V
Low Voltage Indicator Output Voltage Range	$V_{C(LVI)}$	–1.0 to + 65	V
Low Voltage Indicator Output Sink Current	$I_{C(LVI)}$	10	mA
Thermal Characteristics			°C/W
P Suffix, Dual In Line Case 648C			
Thermal Resistance, Junction–to–Air	$R_{\theta JA}$	80	
Thermal Resistance, Junction–to–Case (Pins 4, 5, 12, 13)	$R_{\theta JC}$	15	
DW Suffix, Surface Mount Case 751G			
Thermal Resistance, Junction–to–Air	$R_{\theta JA}$	94	
Thermal Resistance, Junction–to–Case (Pins 4, 5, 12, 13)	$R_{\theta JC}$	18	
Operating Junction Temperature	T_J	+150	°C
Operating Ambient Temperature (Note 3)	T_A		°C
MC34165		0 to +70	
MC33165		– 40 to + 85	
Storage Temperature Range	T_{stg}	– 65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V, Pin 16 = V_{CC}, C_T = 620 pF, for typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies (Note 3), unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OSCILLATOR					
Frequency	f_{OSC}				kHz
T_A = 25°C		46	50	54	
Total Variation over V_{CC} = 3.0 V to 65 V, and Temperature		45	–	55	
Charge Current	I_{chg}	–	225	–	µA
Discharge Current	I_{dischg}	–	25	–	µA
Charge to Discharge Current Ratio	I_{chg}/I_{dischg}	7.5	9.0	10	–
Sawtooth Peak Voltage	$V_{OSC(P)}$	–	1.25	–	V
Sawtooth Valley Voltage	$V_{OSC(V)}$	–	0.55	–	V
FEEDBACK COMPARATOR 1					
Threshold Voltage	$V_{th(FB1)}$				
T_A = 25°C		4.9	5.05	5.2	V
Line Regulation (V_{CC} = 3.0 V to 65 V, T_A = 25°C)		–	0.008	0.03	%/V
Total Variation over Line, and Temperature		4.85	–	5.25	V
Input Bias Current (V_{FB1} = 5.05 V)	$I_{IB(FB1)}$	–	100	200	µA

NOTES:
1. Maximum package power dissipation limits must be observed.
2. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
3. T_{low} = 0°C for MC34165 T_{high} = + 70°C for MC34165
= – 40°C for MC33165 = + 85°C for MC33165
4. The Low Voltage Indicator threshold tracks $V_{th(FB2)}$ and is expressed as a percent of the $V_{th(FB2)}$ threshold.

ELECTRICAL CHARACTERISTICS (continued) (V_{CC} = 15 V, Pin 16 = V_{CC}, C_T = 620 pF, for typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies (Note 3), unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
FEEDBACK COMPARATOR 2					
Threshold Voltage	$V_{th(FB2)}$				
T_A = 25°C		1.225	1.25	1.275	V
Line Regulation (V_{CC} = 3.0 V to 65 V, T_A = 25°C)		–	0.008	0.03	%/V
Total Variation over Line, and Temperature		1.220	–	1.280	V
Input Bias Current (V_{FB2} = 1.25 V)	$I_{IB(FB2)}$	– 0.4	0	0.4	µA
CURRENT LIMIT COMPARATOR					
Threshold Voltage	$V_{th(Ipk\ Sense)}$				mV
T_A = 25°C		–	245	–	
Total Variation over V_{CC} = 3.0 V to 65 V, and Temperature		225	–	270	
Input Bias Current ($V_{Ipk\ (Sense)}$ = 15 V)	$I_{IB(sense)}$	–	1.0	5.0	µA
DRIVER AND OUTPUT SWITCH (Note 2)					
Sink Saturation Voltage (I_{SW} = 1.0 A, Pins 14, 15 grounded)	$V_{CE(sat)}$				V
Non–Darlington Connection ($R_{Pin\ 9}$ = 110 Ω to V_{CC}, $I_{SW}/I_{DRV} \approx 8$)		–	0.3	0.7	
Darlington Connection (Pins 9, 10, 11 connected)		–	1.1	1.4	
Collector Off–State Leakage Current (V_{CE} = 65 V)	$I_{C(off)}$	–	0.02	100	µA
Bootstrap Input Current Source (V_{BS} = V_{CC} + 5.0 V)	$I_{source(DRV)}$	0.5	2.0	4.0	mA
Bootstrap Input Zener Clamp Voltage (I_Z = 25 mA)	V_Z	V_{CC} + 6.0	V_{CC} + 7.0	V_{CC} + 9.0	V
LOW VOLTAGE INDICATOR					
LVI Threshold (Percent of V_{FB}, Note 4)	$V_{th(LVI)}$				%
V_{FB2} Decreasing		87	88.3	90	
V_{FB2} Increasing		88	89.9	92	
Hysteresis	V_H	–	20	–	mV
Output Sink Saturation Voltage (I_{sink} = 0.5 mA)	$V_{OL(LVI)}$	–	0.15	0.4	V
Output Off–State Leakage Current (V_{OH} = 15 V)	I_{OH}	–	0.01	1.0	µA
TOTAL DEVICE					
Standby Supply Current (V_{CC} = 3.0 V to 65 V, Pin 8 = V_{CC}, Pins 6, 14, 15 = Gnd, remaining pins open)	I_{CC}	–	6.0	10	mA

NOTES: 1. Maximum package power dissipation limits must be observed.
2. Low duty cycle pulse techniques are used during test to maintain as close to ambient as possible.
3. T_{low} = 0°C for MC34165 T_{high} = + 70°C for MC34165
= – 40°C for MC33165 = + 85°C for MC33165
4. The Low Voltage Indicator threshold tracks $V_{th(FB2)}$ and is expressed as a percent of the V_{FB2} threshold.

Figure 1. Output Switch On–Off Time versus Oscillator Timing Capacitor

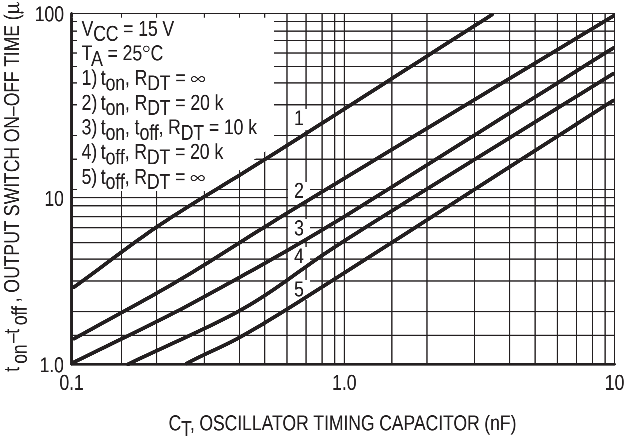
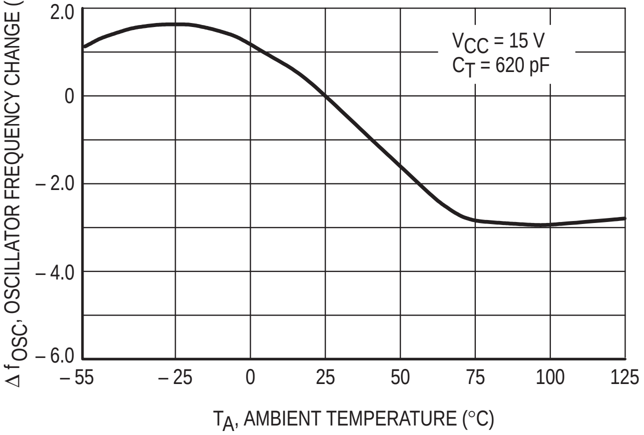


Figure 2. Oscillator Frequency Change versus Temperature



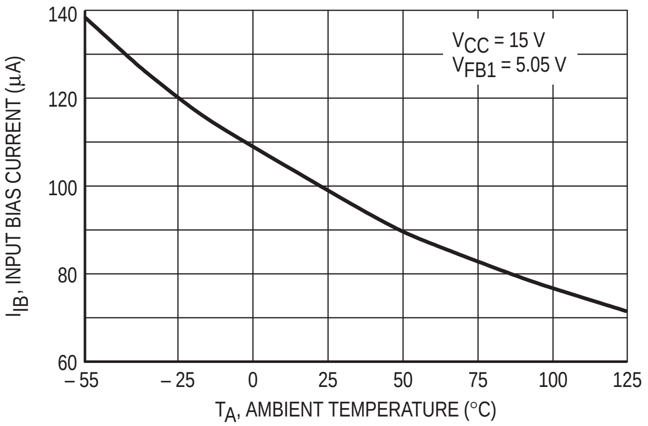


Figure 3. Feedback Comparator 1 Input Bias Current versus Temperature

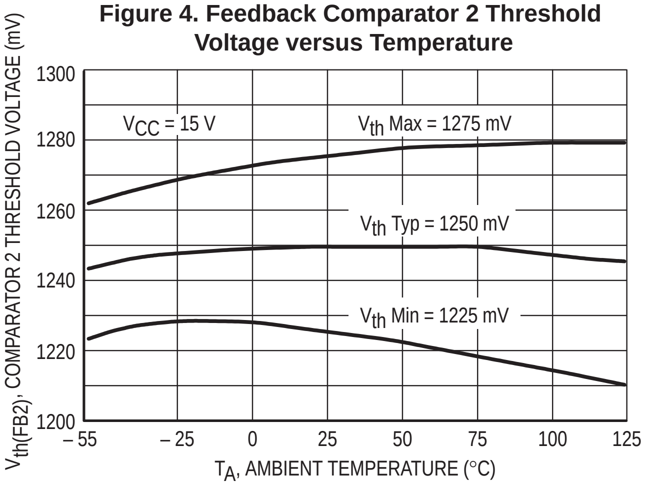


Figure 4. Feedback Comparator 2 Threshold Voltage versus Temperature

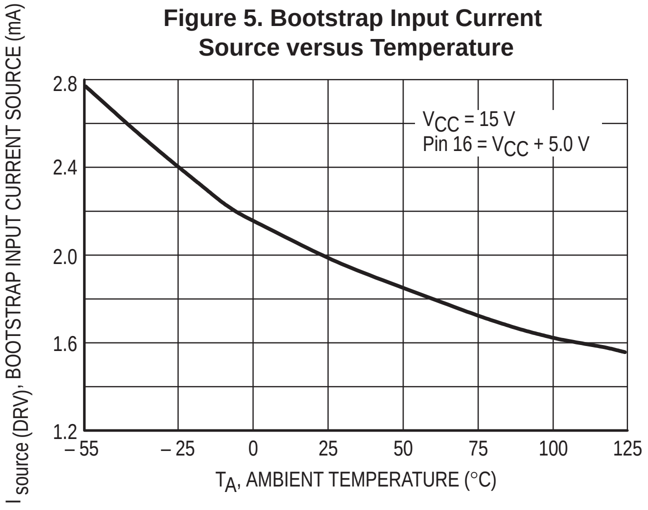


Figure 5. Bootstrap Input Current Source versus Temperature

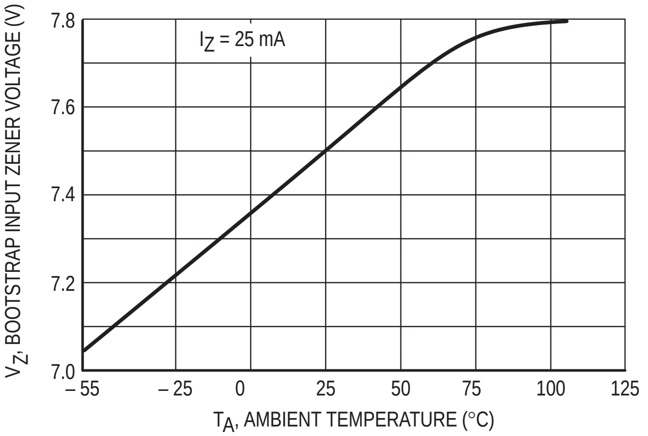


Figure 6. Bootstrap Input Zener Clamp Voltage versus Temperature

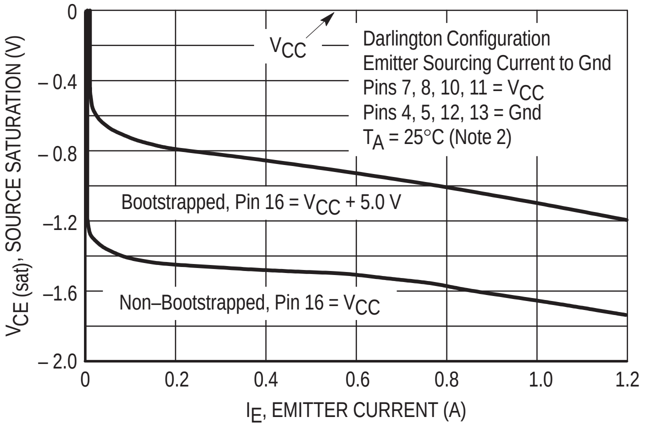


Figure 7. Output Switch Source Saturation versus Emitter Current

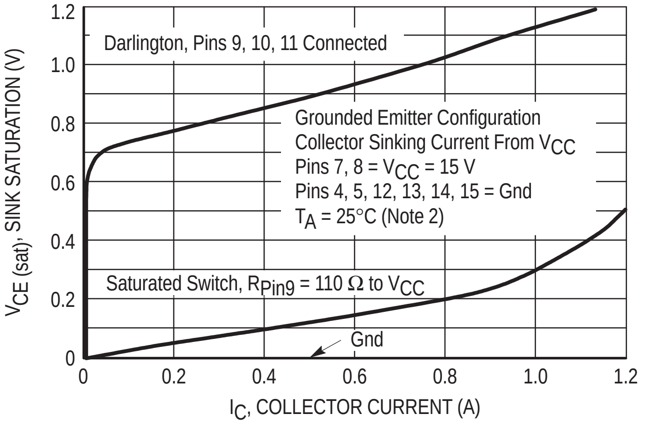


Figure 8. Output Switch Sink Saturation versus Collector Current

Figure 9. Output Switch Negative Emitter Voltage versus Temperature

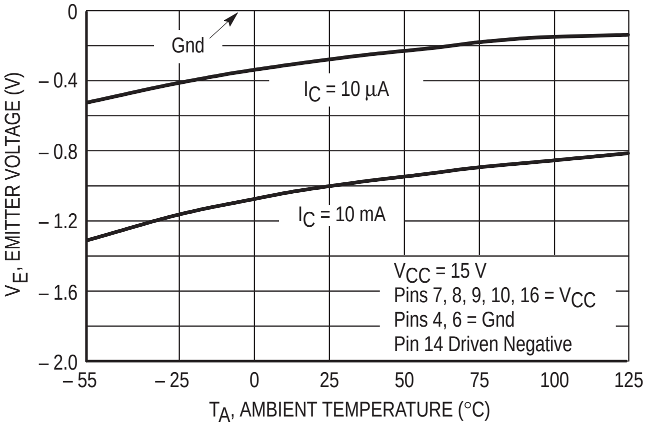


Figure 10. Low Voltage Indicator Output Sink Saturation Voltage versus Sink Current

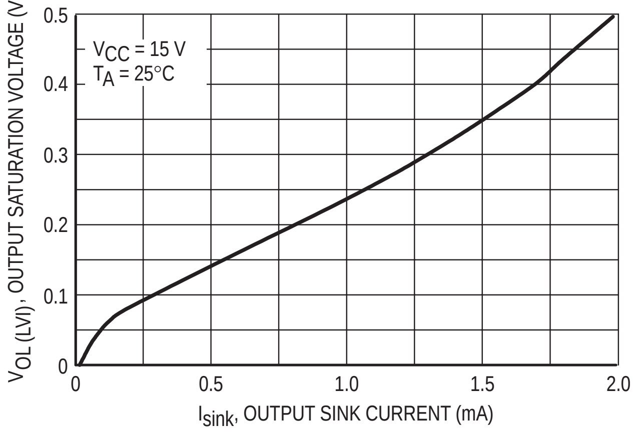


Figure 11. Current Limit Comparator Threshold Voltage versus Temperature

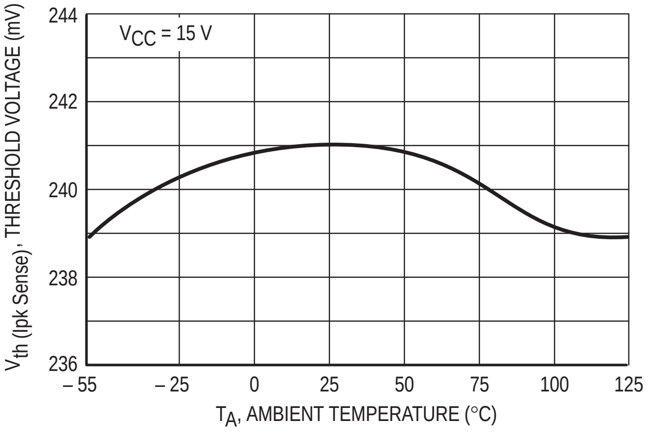


Figure 12. Current Limit Comparator Input Bias Current versus Temperature

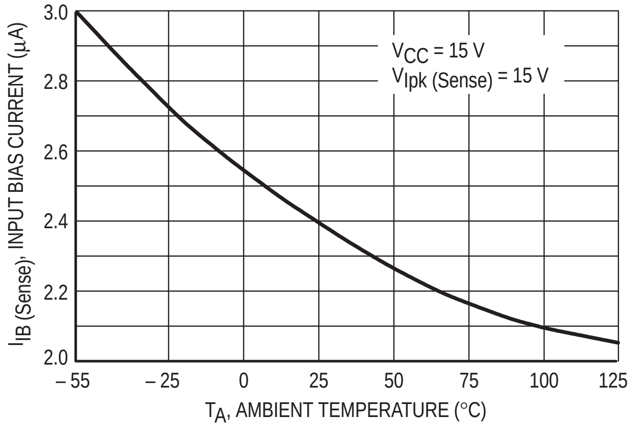


Figure 13. Standby Supply Current versus Supply Voltage

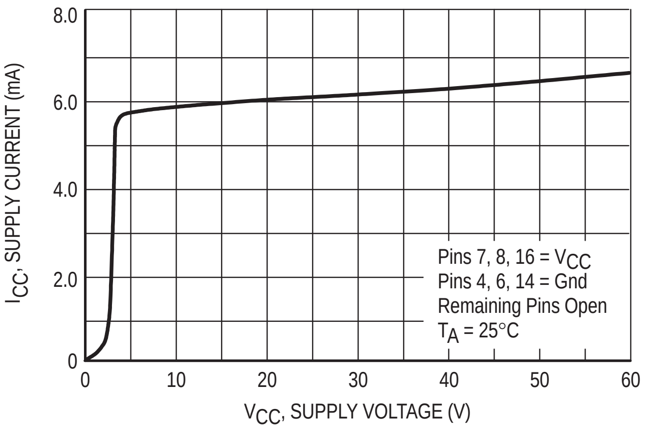


Figure 14. Standby Supply Current versus Temperature

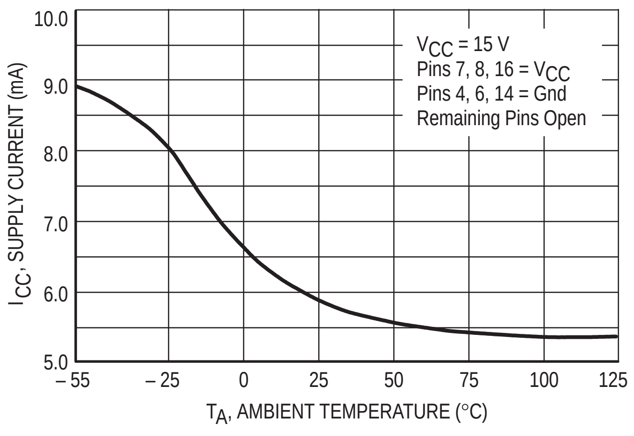


Figure 15. Minimum Operating Supply Voltage versus Temperature

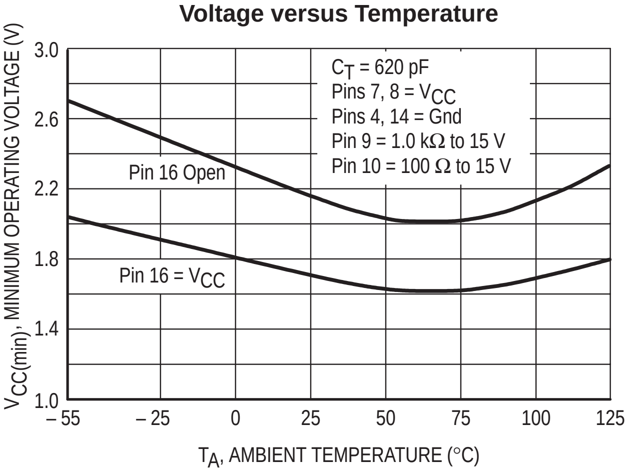


Figure 16. P Suffix (DIP–16) Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length

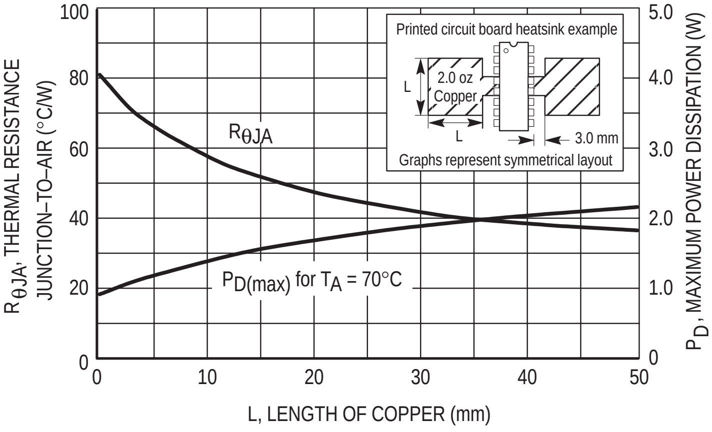
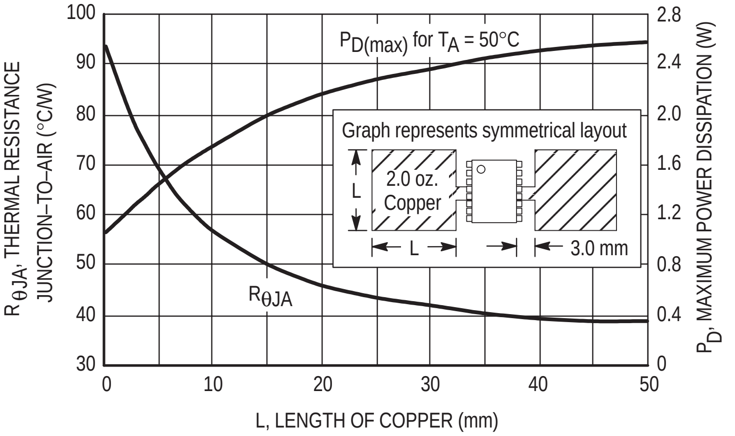


Figure 17. DW Suffix (SOP–16L) Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length



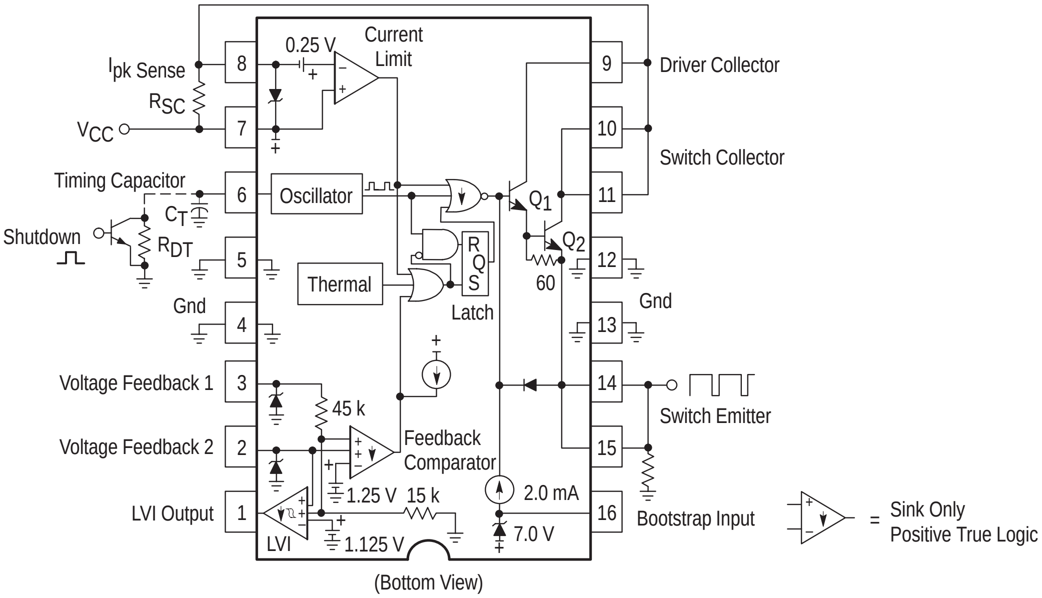


Figure 18. Representative Block Diagram

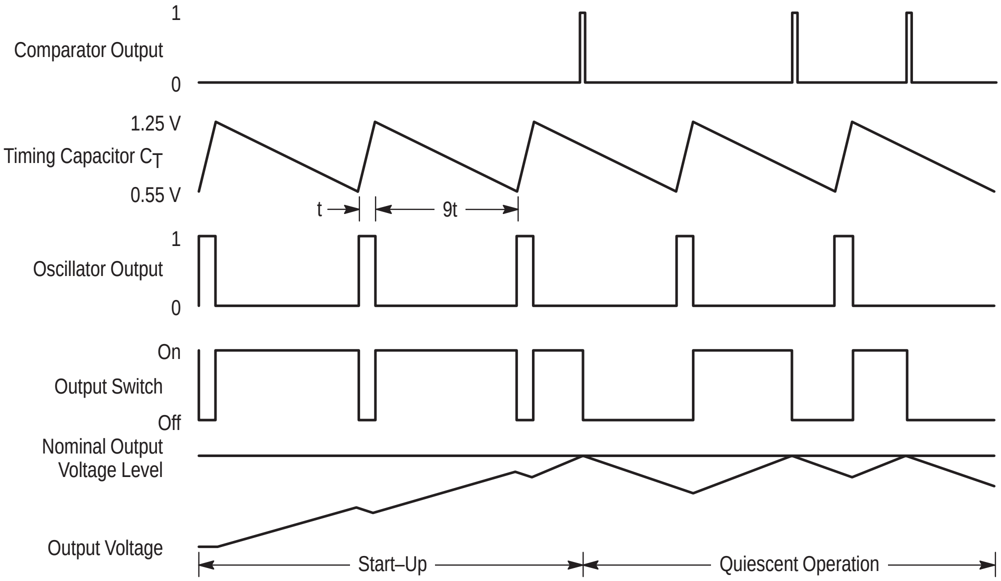


Figure 19. Typical Operating Waveforms

INTRODUCTION

The MC34165 series are monolithic power switching regulators optimized for DC–to–DC converter applications. The combination of features in this series enables the system designer to directly implement step–up, step–down, and voltage–inverting converters with a minimum number of external components. This series is constructed on a special high voltage process making it ideal for telecommunication applications. Other potential applications include cost sensitive consumer products as well as equipment for the automotive, computer, and industrial markets. The Representative Block Diagram is shown in Figure 18.

OPERATING DESCRIPTION

The MC34165 operates as a fixed on–time, variable off–time voltage mode ripple regulator. In general, this mode of operation is somewhat analogous to a capacitor charge pump and does not require dominant pole loop compensation for converter stability. The Typical Operating Waveforms are shown in Figure 19. The output voltage waveform shown is for a step–down converter, with the ripple and phasing exaggerated for clarity. During initial converter start–up, the feedback comparator senses that the output voltage level is below nominal. This causes the output switch to turn on and off at a frequency and duty cycle controlled by the oscillator, thus pumping up the output filter capacitor. When the output voltage level reaches nominal, the feedback comparator sets the latch, immediately terminating switch conduction. The feedback comparator will inhibit the switch until the load current causes the output voltage to fall below nominal. Under these conditions, output switch conduction can be inhibited for a partial oscillator cycle, a partial cycle plus a complete cycle, multiple cycles, or a partial cycle plus multiple cycles.

Oscillator

The oscillator frequency and on–time of the output switch are programmed by the value selected for timing capacitor C_T. Capacitor C_T is charged and discharged by a 9 to 1 ratio internal current source and sink, generating a negative going sawtooth waveform at Pin 6. As C_T charges, an internal pulse is generated at the oscillator output. This pulse is connected to the NOR gate center input, preventing output switch conduction, and to the AND gate upper input, allowing the latch to be reset if the comparator output is low. Thus, the output switch is always disabled during ramp–up and can be enabled by the comparator output only at the start of ramp–down. The oscillator peak and valley thresholds are 1.25 V and 0.55 V, respectively, with a charge current of 225 μA and a discharge current of 25 μA, yielding a maximum on–time duty cycle of 90%. Since the MC34165 is a ripple mode regulator, the switch frequency will vary with line and load. The value selected for C_T will set the maximum switching frequency of the converter. A reduction of the maximum duty cycle may be required for specific converter configurations. This can be accomplished with the addition of an external dead–time resistor (R_{DT}) placed across C_T. The resistor increases the discharge current which reduces the on–time of the output switch. A graph of the Output Switch On–Off Time versus Oscillator Timing Capacitance for various values of R_{DT} is shown in Figure 1. Note that the maximum output duty cycle, $t_{on}/t_{on} + t_{off}$, remains constant for values of C_T greater than 0.2 nF. The converter output can be inhibited by clamping C_T to ground with an external NPN small–signal transistor.

Feedback and Low Voltage Indicator Comparators

Output voltage control is established by the Feedback comparator. The inverting input is internally biased at 1.25 V and is not pinned out. The converter output voltage is typically divided down with two external resistors and monitored by the high impedance noninverting input at Pin 2. The maximum input bias current is ±0.4 μA, which can cause an output voltage error that is equal to the product of the input bias current and the upper divider resistance value. For applications that require 5.0 V, the converter output can be directly connected to the noninverting input at Pin 3. The high impedance input, Pin 2, must be grounded to prevent noise pickup. The internal resistor divider is set for a nominal voltage of 5.05 V. The additional 50 mV compensates for a 1.0% voltage drop in the cable and connector from the converter output to the load. The Feedback comparator's output state is controlled by the highest voltage applied to either of the two noninverting inputs.

The Low Voltage Indicator (LVI) comparator is designed for use as a reset controller in microprocessor–based systems. The inverting input is internally biased at 1.125 V, which sets the noninverting input thresholds to 90% of nominal. The LVI comparator has 15 mV of hysteresis to prevent erratic reset operation. The open collector output is capable of sinking in excess of 1.5 mA (see Figure 10). An external resistor (R_{LVI}) and capacitor (C_{DLY}) can be used to program a reset delay time (t_{DLY}) by the formula shown below, where $V_{th(MPU)}$ is the microprocessor reset input threshold.

$$t_{DLY} = R_{LVI}\, C_{DLY} \ln\left(\frac{1}{1 - \dfrac{V_{th(MPU)}}{V_{out}}}\right)$$

Current Limit Comparator, Latch and Thermal Shutdown

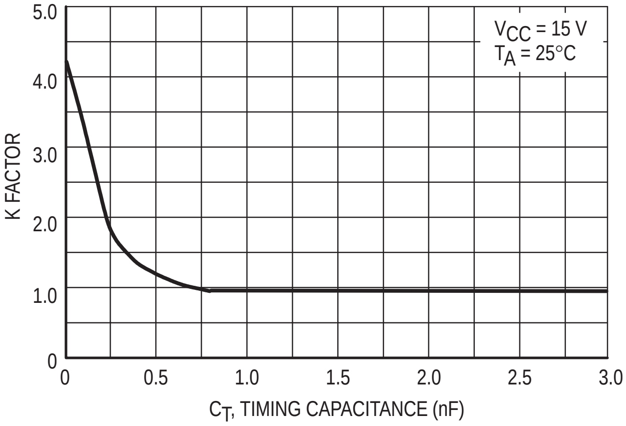
With a voltage mode ripple converter operating under normal conditions, output switch conduction is initiated by the oscillator and terminated by the Voltage Feedback comparator. Abnormal operating conditions occur when the converter output is overloaded or when feedback voltage sensing is lost. Under these conditions, the Current Limit comparator will protect the Output Switch.

The switch current is converted to a voltage by inserting a fractional ohm resistor, R_{SC}, in series with V_{CC} and output switch transistor Q_2. The voltage drop across R_{SC} is monitored by the Current Sense comparator. If the voltage drop exceeds 250 mV with respect to V_{CC}, the comparator will set the latch and terminate output switch conduction on a cycle–by–cycle basis. This Comparator/Latch configuration ensures that the Output Switch has only a single on–time during a given oscillator cycle. The calculation for a value of R_{SC} is:

$$R_{SC} = \frac{0.25\ \text{V} \cdot \text{K}}{I_{pk\,(Switch)}}$$

The K factor was added to the previous equation in order to account for a 200 ns propagation delay that occurs from the Current Limit comparator input to the output switch. This propagation delay can cause the actual peak switch current to rise above the calculated peak switch current for small values of C_T. The following figure shows the relationship of the ratio $I_{pk(actual)}/I_{pk\ (Switch)}$, expressed as K versus C_T. Note the ratio rises above 1.0 for C_T values less than 1.0 nF.

Figure 20. K Factor versus Timing Capacitance



When analyzing a design, the actual short circuit current must be measured to verify that it is less than the maximum rating of the device.

Figures 11 and 12 show that the Current Sense comparator threshold is tightly controlled over temperature and has a typical input bias current of 1.0 µA. The parasitic inductance associated with R_{SC} and the circuit layout should be minimized. This will prevent unwanted voltage spikes that may falsely trip the Current Limit comparator.

Internal thermal shutdown circuitry is provided to protect the IC in the event that the maximum junction temperature is exceeded. When activated, typically at 170°C, the Latch is forced into the “Set” state, disabling the Output Switch. This feature is provided to prevent catastrophic failures from accidental device overheating. It is not intended to be used as a replacement for proper heatsinking.

Driver and Output Switch

To aid in system design flexibility and conversion efficiency, the driver current source and collector, and output switch collector and emitter are pinned out separately. This allows the designer the option of driving the output switch into saturation with a selected force gain or driving it near saturation when connected as a Darlington. The output switch is designed to switch a maximum of 65 V collector to emitter, with up to 1.5 A peak collector current. The minimum value for R_{SC} is:

$$R_{SC(min)} = \frac{0.25\ V}{1.5\ A} = 0.166\ \Omega$$

When configured for step–down or voltage–inverting applications, as in Figures 20 and 24, the inductor will forward bias the output rectifier when the switch turns off. Rectifiers with a high forward voltage drop or long turn–on delay time should not be used. If the emitter is allowed to go sufficiently negative, collector current will flow, causing additional device heating and reduced conversion efficiency.

Figure 9 shows that by clamping the emitter to less than 0.5 V, the collector current will be in the range 10 µA over temperature. A MBR160 or equivalent Schottky barrier rectifier is recommended to fulfill these requirements.

A bootstrap input is provided to reduce the output switch saturation voltage in step–down and voltage–inverting converter applications. This input is connected through a series resistor and capacitor to the switch emitter and is used to raise the internal 2.0 mA bias current source above V_{CC}. An internal zener limits the bootstrap input voltage to V_{CC} +7.0 V. The capacitor’s equivalent series resistance may be large enough to limit the zener current to less than the maximum 100 mA rating. However, in most high voltage applications, an additional series resistor will probably be required. It is recommended that this resistor limit the zener current to approximately 25 mA for optimal performance. The circuit can be optimized by adjusting the zener current (R_B) during operation, while observing the circuit’s efficiency. The value of the series resistor can be calculated as follows:

$$R_B \approx \frac{V_{in(max)}}{I_Z}$$

The equation below is used to calculate a minimum value bootstrap capacitor based on a minimum zener voltage and an upper limit current source.

$$C_{B(min)} = I\ \frac{\Delta t}{\Delta V} = 4.0\ \text{mA}\ \frac{t_{on}}{4.0\ V} = 0.001\ t_{on}$$

Parametric operation of the MC34165 is guaranteed over a supply voltage range of 3.0 V to 65 V. When operating below 3.0 V, the Bootstrap Input should be connected to V_{CC}. Figure 15 shows that non–parametric operation down to 1.7 V at room temperature is possible.

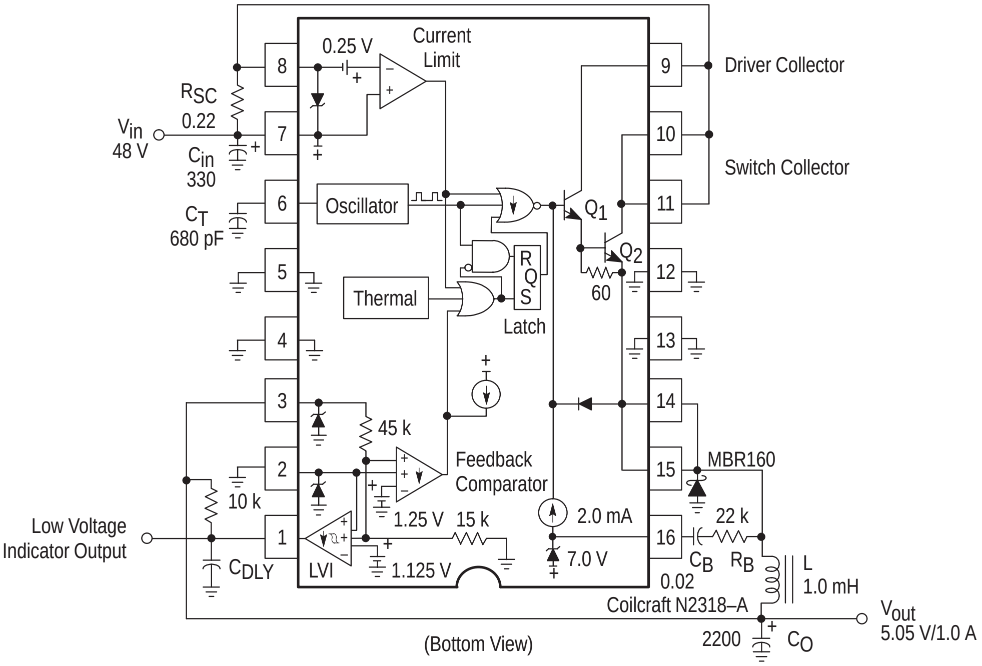
Package

The MC34165 is contained in a heatsinkable 16–lead plastic dual–in–line power package in which the die is mounted on a special heat tab copper alloy lead frame. This tab consists of the four center ground pins that are specifically designed to improve thermal conduction from the die to the circuit board. Figures 16 and 17 show a simple and effective method of utilizing the printed circuit board medium as a heat dissipater by soldering these pins to an adequate area of copper foil. This permits the use of standard layout and mounting practices while having the ability to halve the junction–to–air thermal resistance. These examples are for a symmetrical layout on a single–sided board with two ounce per square foot of copper.

APPLICATIONS

The following converter applications show the simplicity and flexibility of this circuit architecture. Three main converter topologies are demonstrated with actual test data shown below each of the circuit diagrams.

Figure 21. Step–Down Converter



Test	Condition	Results
Line Regulation	V_{in} = 12 V to 56 V, I_O = 1.0 A	9.0 mV = ± 0.049%
Load Regulation	V_{in} = 48 V, I_O = 0.1 A to 1.0 A	9.0 mV = ± 0.049%
Output Ripple	V_{in} = 48 V, I_O = 1.0 A	20 mVp–p
Short Circuit Current	V_{in} = 48 V, R_L = 0.1 Ω	1.23 A
Efficiency, Without Bootstrap	V_{in} = 48 V, I_O = 1.0 A	74.9%
Efficiency, With Bootstrap	V_{in} = 48 V, I_O = 1.0 A	75.5%

L = 65 turns of # 18 AWG on Magenetics Inc. 55345–A2 core.

Figure 22. External Current Boost Connections for $I_{pk\ (Switch)}$ Greater Than 1.5 A

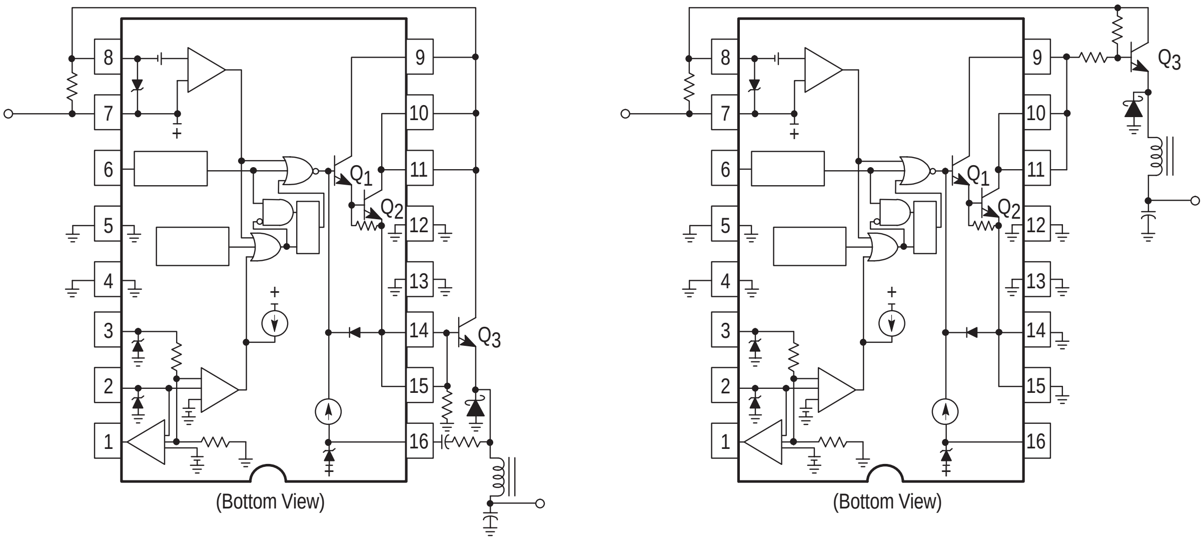
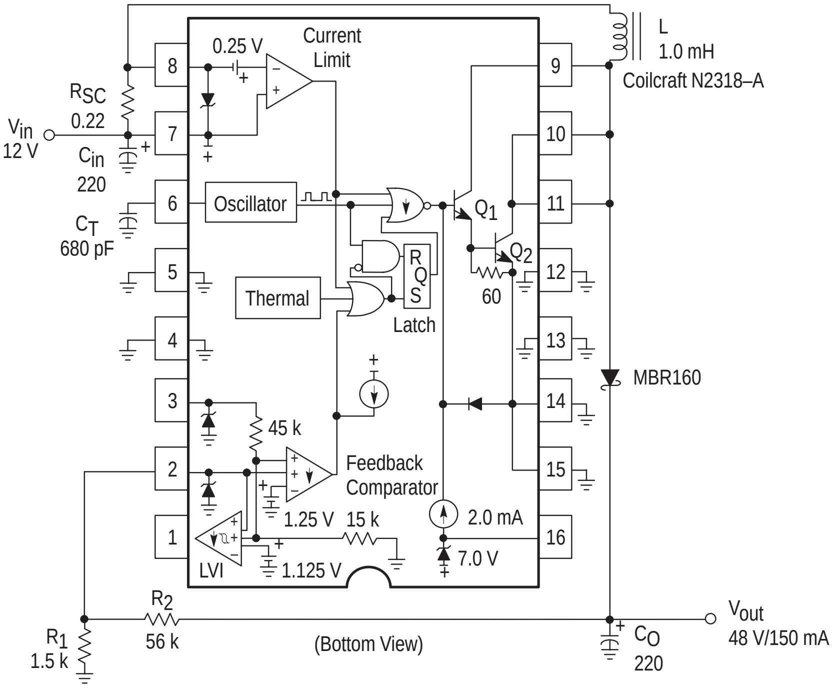


Figure 22A. External NPN Switch

Figure 22B. External PNP Saturated Switch

Figure 23. Step–Up Converter



Test	Condition	Results
Line Regulation	V_{in} = 10 V to 20 V, I_O = 150 mA	11 mV = ± 0.11%
Load Regulation	V_{in} = 12 V, I_O = 15 mA to 150 mA	9.0 mV = ± 0.09%
Output Ripple	V_{in} = 12 V, I_O = 150 mA	125 mVp–p
Efficiency	V_{in} = 12 V, I_O = 150 mA	85.8%

L = 65 turns of # 18 AWG on Magenetics Inc. 55345–A2 core.

Figure 24. External Current Boost Connections for $I_{pk\ (Switch)}$ Greater Than 1.5 A

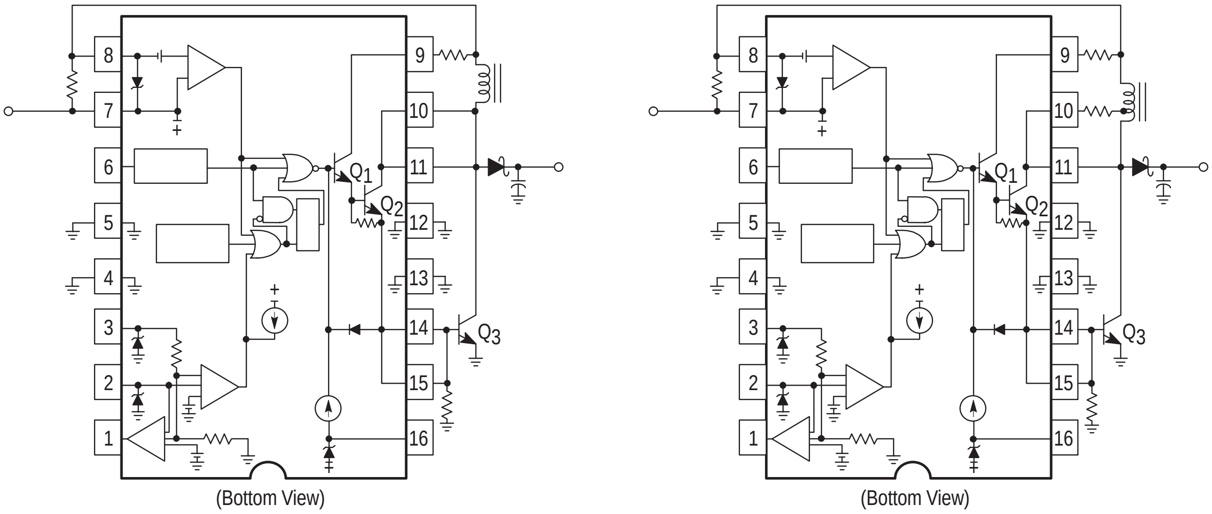


Figure 24A. External NPN Switch

Figure 24B. External NPN Saturated Switch

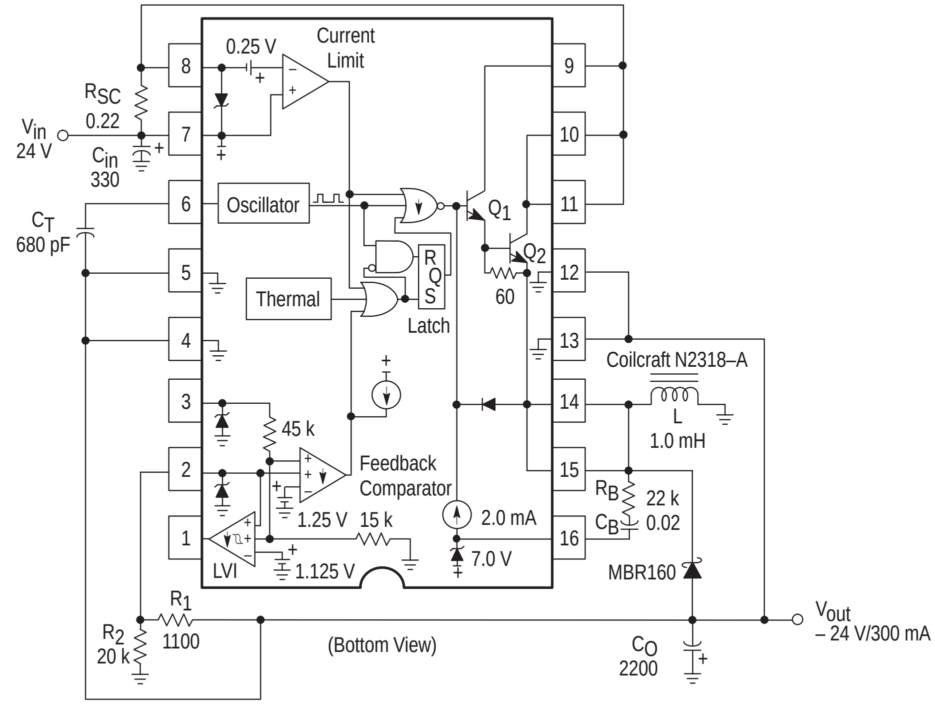


Figure 25. Voltage–Inverting Converter

Test	Condition	Results
Line Regulation	V_{in} = 15 V to 30 V, I_O = 300 mA	3.0 mV = ± 0.06%
Load Regulation	V_{in} = 24 V, I_O = 30 mA to 300 mA	1.0 mV = ± 0.02%
Output Ripple	V_{in} = 24 V, I_O = 300 mA	50 mVp–p
Short Circuit Current	V_{in} = 24 V, R_L = 0.1 Ω	1.12 A
Efficiency, Without Bootstrap	V_{in} = 24 V, I_O = 300 mA	81.3%
Efficiency, With Bootstrap	V_{in} = 24 V, I_O = 300 mA	82.7%

L = 65 turns of # 18 AWG on Magenetics Inc. 55345–A2 core.

Figure 26. External Current Boost Connections for $I_{pk\ (Switch)}$ Greater Than 1.5 A

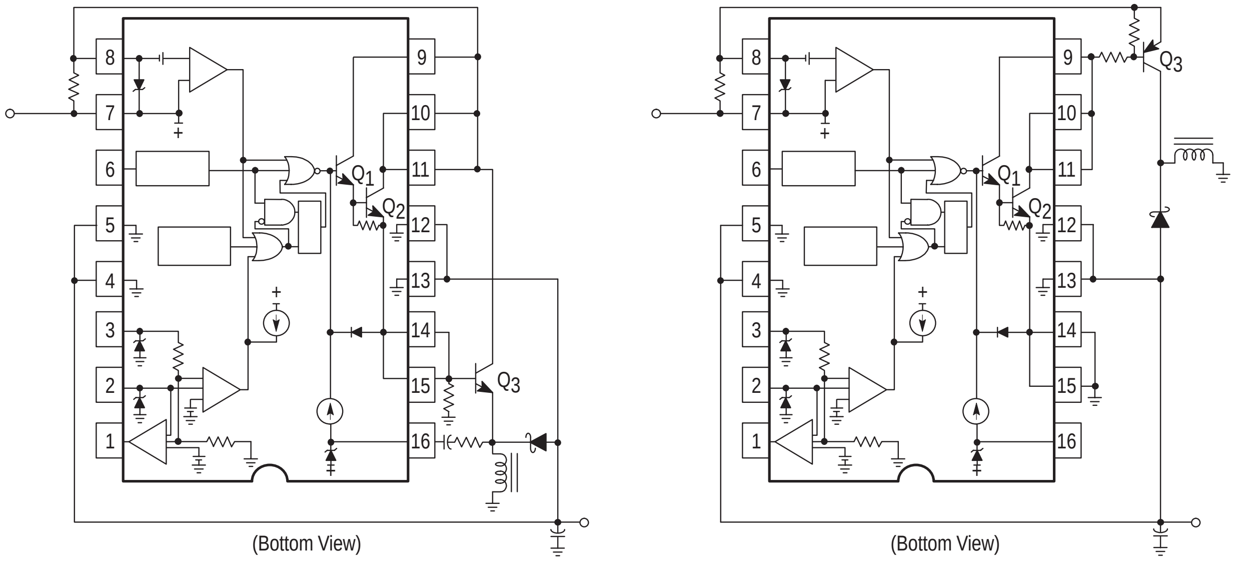
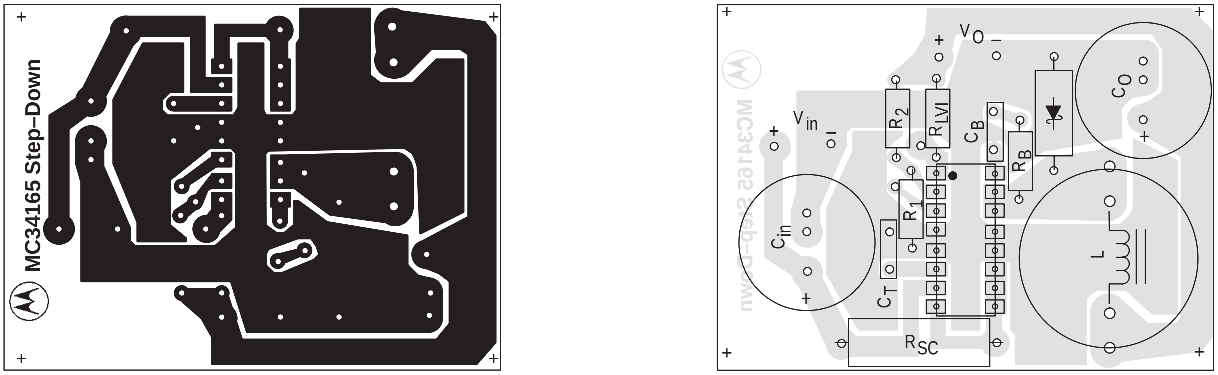


Figure 26A. External NPN Switch

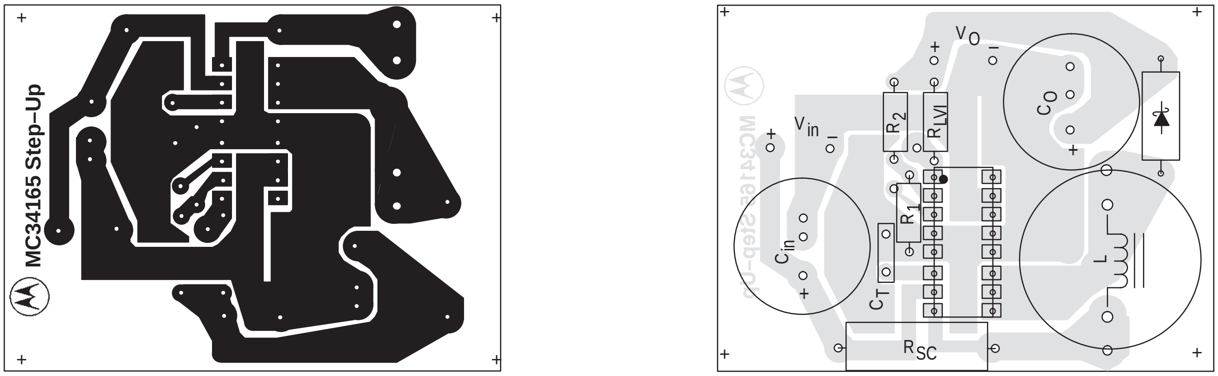
Figure 26B. External PNP Saturated Switch

Figure 27. Printed Circuit Board and Component Layout (Circuits of Figures 21, 23, 25)



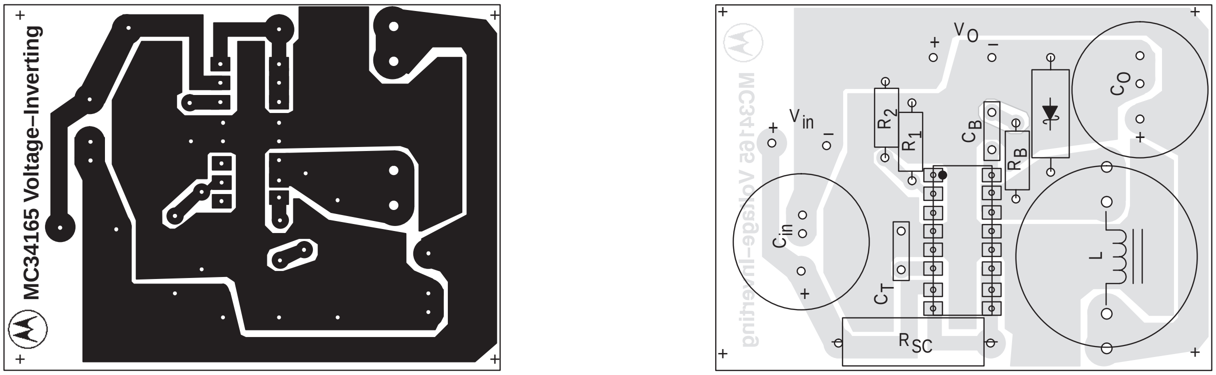
Bottom View

Top View



Bottom View

Top View



Bottom View

Top View

All printed circuit boards are 2.58” in width by 1.9” in height.

Table 1. Design Equations

Calculation	Step–Down	Step–Up	Voltage–Inverting
$\frac{t_{on}}{t_{off}}$ (Notes 1, 2, 3)	$\frac{V_{out} + V_F}{V_{in} - V_{sat} - V_{out}}$	$\frac{V_{out} + V_F - V_{in}}{V_{in} - V_{sat}}$	$\frac{\lvert V_{out}\rvert + V_F}{V_{in} - V_{sat}}$
t_{on}	$\frac{\frac{t_{on}}{t_{off}}}{f\left(\frac{t_{on}}{t_{off}} + 1\right)}$	$\frac{\frac{t_{on}}{t_{off}}}{f\left(\frac{t_{on}}{t_{off}} + 1\right)}$	$\frac{\frac{t_{on}}{t_{off}}}{f\left(\frac{t_{on}}{t_{off}} + 1\right)}$
C_T	$\frac{32.143 \cdot 10^{-6}}{f}$	$\frac{32.143 \cdot 10^{-6}}{f}$	$\frac{32.143 \cdot 10^{-6}}{f}$
$I_{L(avg)}$	I_{out}	$I_{out}\left(\frac{t_{on}}{t_{off}} + 1\right)$	$I_{out}\left(\frac{t_{on}}{t_{off}} + 1\right)$
$I_{pk\ (Switch)}$	$I_{L(avg)} + \frac{\Delta I_L}{2}$	$I_{L(avg)} + \frac{\Delta I_L}{2}$	$I_{L(avg)} + \frac{\Delta I_L}{2}$
R_{SC}	$\frac{0.25 \cdot K}{I_{pk\ (Switch)}}$	$\frac{0.25 \cdot K}{I_{pk\ (Switch)}}$	$\frac{0.25 \cdot K}{I_{pk\ (Switch)}}$
L	$\left(\frac{V_{in} - V_{sat} - V_{out}}{\Delta I_L}\right) t_{on}$	$\left(\frac{V_{in} - V_{sat}}{\Delta I_L}\right) t_{on}$	$\left(\frac{V_{in} - V_{sat}}{\Delta I_L}\right) t_{on}$
$V_{ripple(p-p)}$	$\Delta I_L \sqrt{\left(\frac{1}{8 f C_O}\right)^2 + (ESR)^2}$	$\approx \frac{t_{on}\ I_{out}}{C_O}$	$\approx \frac{t_{on}\ I_{out}}{C_O}$
V_{out}	$V_{ref}\left(\frac{R_2}{R_1} + 1\right)$	$V_{ref}\left(\frac{R_2}{R_1} + 1\right)$	$V_{ref}\left(\frac{R_2}{R_1} + 1\right)$

The following Converter Characteristics must be chosen:

V_{in} – Nominal operating input voltage.
V_{out} – Desired output voltage.
I_{out} – Desired output current.
ΔI_L – Desired peak–to–peak inductor ripple current. For maximum output current, it is suggested that ΔI_L be chosen to be less than 10% of the average inductor current $I_{L(avg)}$. This will help prevent $I_{pk\ (Switch)}$ from reaching the current threshold set by R_{SC}. If the design goal is to use a minimum inductance value, let $\Delta I_L = 2(I_{L(avg)})$. This will proportionally reduce converter output current capability.
f – Maximum output switch frequency.
$V_{ripple(p-p)}$ – Desired peak–to–peak output ripple voltage. For best performance, the ripple voltage should be kept to a low value since it will directly affect line and load regulation. Capacitor C_O should be a low equivalent series resistance (ESR) electrolytic designed for switching regulator applications.
K – Multiplier number as determined by Figure 20, for determining the appropriate value for R_{SC}.

NOTES: 1. V_{sat} – Saturation voltage of the output switch, refer to Figures 7 and 8.
2. V_F – Output rectifier forward voltage drop. Typical value for MBR160 Schottky barrier rectifier is 0.6 V.
3. The calculated t_{on}/t_{off} must not exceed the minimum guaranteed oscillator charge to discharge ratio of 8, at the minimum operating input voltage.

MOTOROLA

MC34166
MC33166

Power Switching Regulators

The MC34166, MC33166 series are high performance fixed frequency power switching regulators that contain the primary functions required for dc–to–dc converters. This series was specifically designed to be incorporated in step–down and voltage–inverting configurations with a minimum number of external components and can also be used cost effectively in step–up applications.

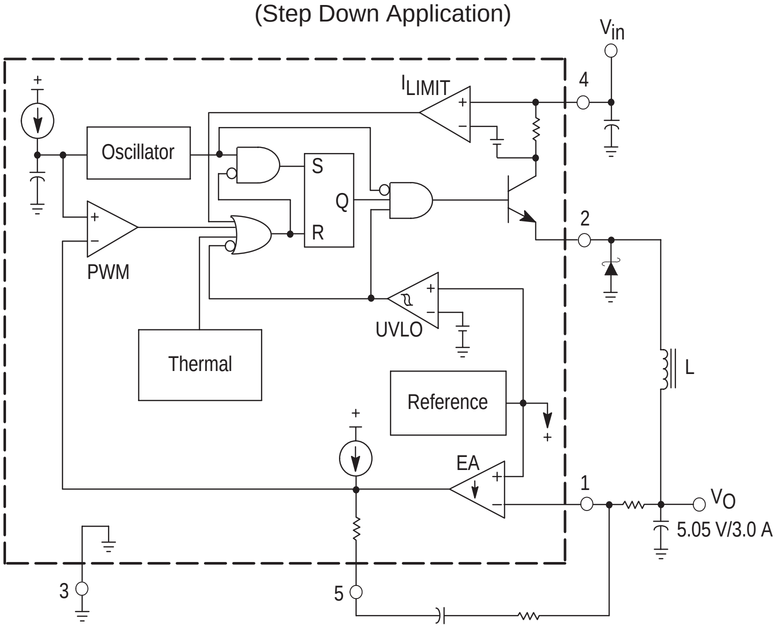
These devices consist of an internal temperature compensated reference, fixed frequency oscillator with on–chip timing components, latching pulse width modulator for single pulse metering, high gain error amplifier, and a high current output switch.

Protective features consist of cycle–by–cycle current limiting, undervoltage lockout, and thermal shutdown. Also included is a low power standby mode that reduces power supply current to 36 µA.

- Output Switch Current in Excess of 3.0 A
- Fixed Frequency Oscillator (72 kHz) with On–Chip Timing
- Provides 5.05 V Output without External Resistor Divider
- Precision 2% Reference
- 0% to 95% Output Duty Cycle
- Cycle–by–Cycle Current Limiting
- Undervoltage Lockout with Hysteresis
- Internal Thermal Shutdown
- Operation from 7.5 V to 40 V
- Standby Mode Reduces Power Supply Current to 36 µA
- Economical 5–Lead TO–220 Package with Two Optional Leadforms
- Also Available in Surface Mount D^2PAK Package

Simplified Block Diagram

(Step Down Application)

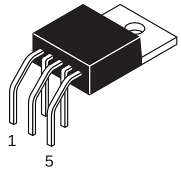


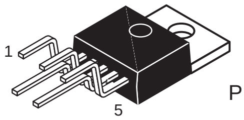
This device contains 143 active transistors.

POWER SWITCHING REGULATORS

SEMICONDUCTOR TECHNICAL DATA

TH SUFFIX
PLASTIC PACKAGE
CASE 314A

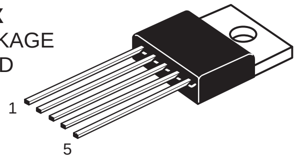




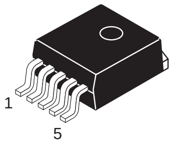
TV SUFFIX
PLASTIC PACKAGE
CASE 314B

Heatsink surface connected to Pin 3.

T SUFFIX
PLASTIC PACKAGE
CASE 314D



Pin 1. Voltage Feedback Input
2. Switch Output
3. Ground
4. Input Voltage/V_{CC}
5. Compensation/Standby



D2T SUFFIX
PLASTIC PACKAGE
CASE 936A
(D^2PAK)

Heatsink surface (shown as terminal 6
in case outline drawing) is connected to Pin 3.

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC33166D2T	T_A = – 40° to + 85°C	Surface Mount
MC33166T		Straight Lead
MC33166TH		Horiz. Mount
MC33166TV		Vertical Mount
MC34166D2T	T_A = 0° to + 70°C	Surface Mount
MC34166T		Straight Lead
MC34166TH		Horiz. Mount
MC34166TV		Vertical Mount

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Input Voltage	V_{CC}	40	V
Switch Output Voltage Range	$V_{O(switch)}$	–1.5 to + V_{in}	V
Voltage Feedback and Compensation Input Voltage Range	V_{FB}, V_{Comp}	–1.0 to + 7.0	V
Power Dissipation Case 314A, 314B and 314D (T_A = +25°C) Thermal Resistance, Junction–to–Ambient Thermal Resistance, Junction–to–Case Case 936A (D^2PAK) (T_A = +25°C) Thermal Resistance, Junction–to–Ambient Thermal Resistance, Junction–to–Case	 P_D θ_{JA} θ_{JC} P_D θ_{JA} θ_{JC}	 Internally Limited 65 5.0 Internally Limited 70 5.0	 W °C/W °C/W W °C/W °C/W
Operating Junction Temperature	T_J	+150	°C
Operating Ambient Temperature (Note 3) MC34166 MC33166	T_A	 0 to + 70 – 40 to + 85	°C
Storage Temperature Range	T_{stg}	– 65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 12 V, for typical values T_A = +25°C, for min/max values T_A is the operating ambient temperature range that applies [Notes 2, 3], unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OSCILLATOR					
Frequency (V_{CC} = 7.5 V to 40 V) T_A = +25°C T_A = T_{low} to T_{high}	f_{OSC}	65 62	72 –	79 81	kHz
ERROR AMPLIFIER					
Voltage Feedback Input Threshold T_A = +25°C T_A = T_{low} to T_{high}	$V_{FB(th)}$	4.95 4.85	5.05 –	5.15 5.2	V
Line Regulation (V_{CC} = 7.5 V to 40 V, T_A = +25°C)	Reg_{line}	–	0.03	0.078	%/V
Input Bias Current (V_{FB} = $V_{FB(th)}$ + 0.15 V)	I_{IB}	–	0.15	1.0	µA
Power Supply Rejection Ratio (V_{CC} = 10 V to 20 V, f = 120 Hz)	PSRR	60	80	–	dB
Output Voltage Swing High State (I_{Source} = 75 µA, V_{FB} = 4.5 V) Low State (I_{Sink} = 0.4 mA, V_{FB} = 5.5 V)	 V_{OH} V_{OL}	 4.2 –	 4.9 1.6	 – 1.9	V
PWM COMPARATOR					
Duty Cycle Maximum (V_{FB} = 0 V) Minimum (V_{Comp} = 1.9 V)	 $DC_{(max)}$ $DC_{(min)}$	 92 0	 95 0	 100 0	%
SWITCH OUTPUT					
Output Voltage Source Saturation (V_{CC} = 7.5 V, I_{Source} = 3.0 A)	V_{sat}	–	(V_{CC} –1.5)	(V_{CC} –1.8)	V
Off–State Leakage (V_{CC} = 40 V, Pin 2 = Gnd)	$I_{sw(off)}$	–	0	100	µA
Current Limit Threshold	$I_{pk(switch)}$	3.3	4.3	6.0	A
Switching Times (V_{CC} = 40 V, I_{pk} = 3.0 A, L = 375 µH, T_A = +25°C) Output Voltage Rise Time Output Voltage Fall Time	 t_r t_f	 – –	 100 50	 200 100	ns
UNDERVOLTAGE LOCKOUT					
Startup Threshold (V_{CC} Increasing, T_A = +25°C)	$V_{th(UVLO)}$	5.5	5.9	6.3	V
Hysteresis (V_{CC} Decreasing, T_A = +25°C)	$V_{H(UVLO)}$	0.6	0.9	1.2	V
TOTAL DEVICE					
Power Supply Current (T_A = +25°C) Standby (V_{CC} = 12 V, V_{Comp} < 0.15 V) Operating (V_{CC} = 40 V, Pin 1 = Gnd for maximum duty cycle)	I_{CC}	 – –	 36 31	 100 55	 µA mA

NOTES: 1. Maximum package power dissipation limits must be observed to prevent thermal shutdown activation.
2. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
3. T_{low} = 0°C for MC34166 T_{high} = + 70°C for MC34166
= – 40°C for MC33166 = + 85°C for MC33166

Figure 1. Voltage Feedback Input Threshold versus Temperature

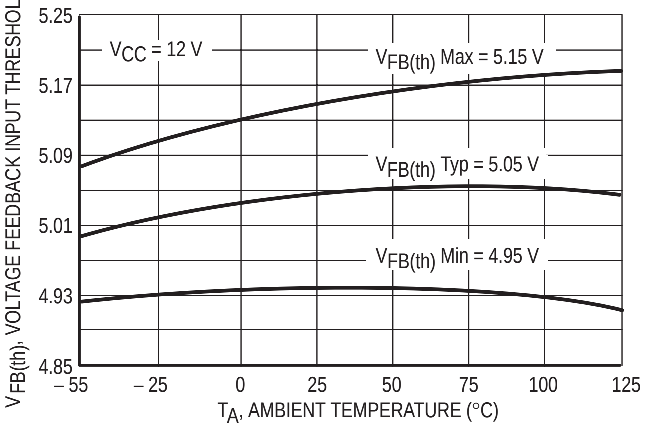


Figure 2. Voltage Feedback Input Bias Current versus Temperature

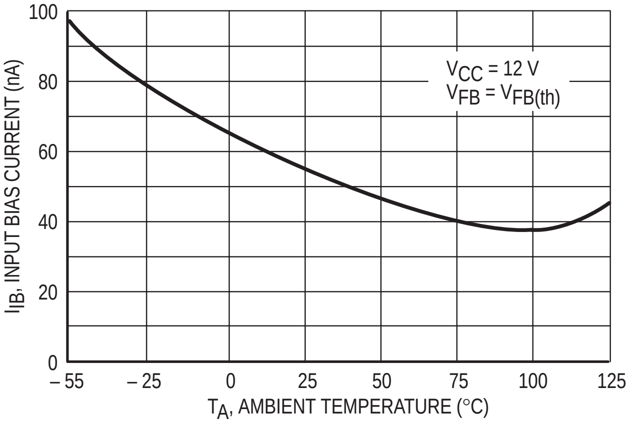


Figure 3. Error Amp Open Loop Gain and Phase versus Frequency

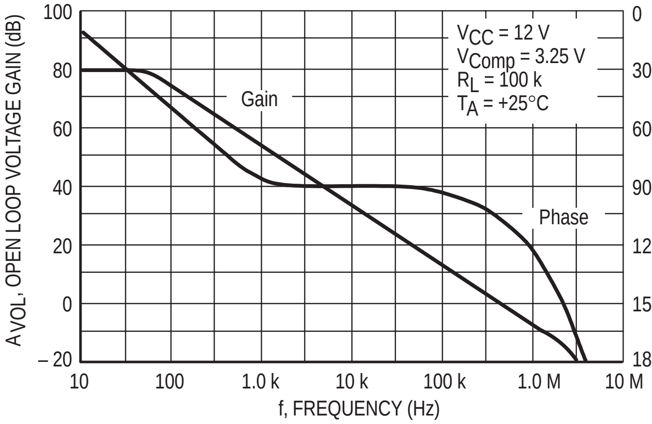


Figure 4. Error Amp Output Saturation versus Sink Current

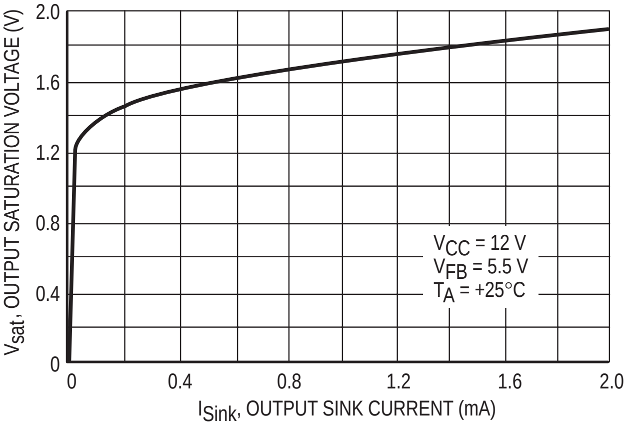


Figure 5. Oscillator Frequency Change versus Temperature

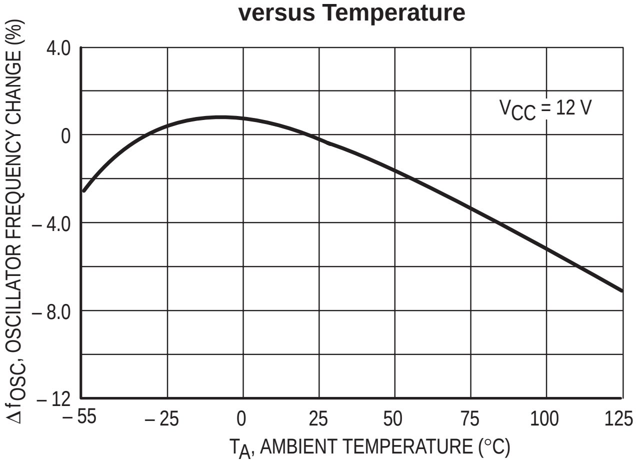


Figure 6. Switch Output Duty Cycle versus Compensation Voltage

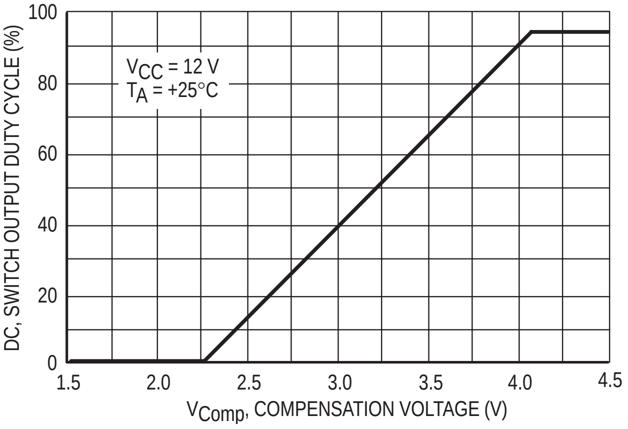


Figure 7. Switch Output Source Saturation versus Source Current

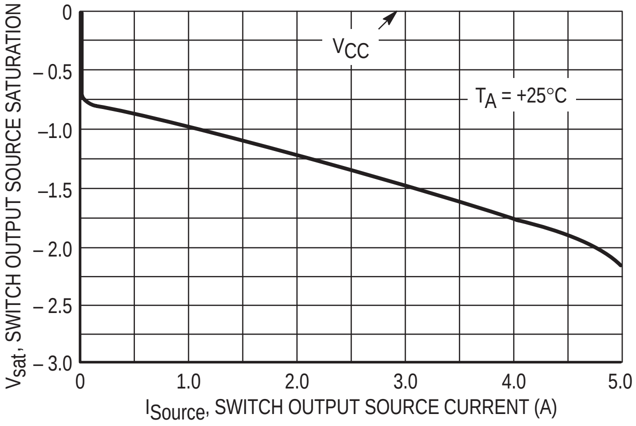


Figure 8. Negative Switch Output Voltage versus Temperature

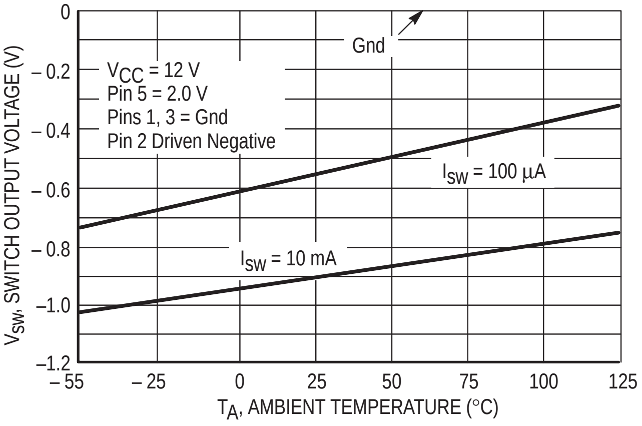


Figure 9. Switch Output Current Limit Threshold versus Temperature

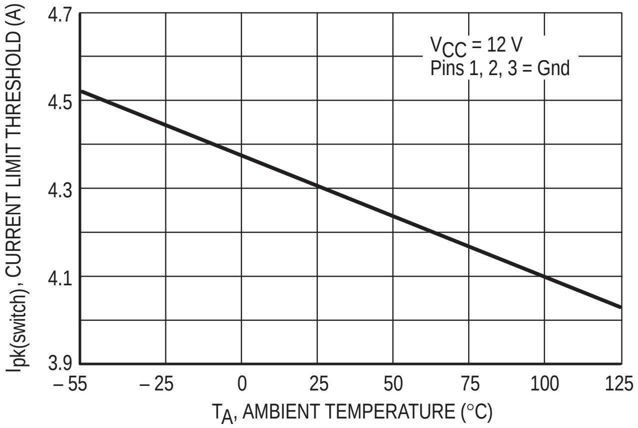


Figure 10. Standby Supply Current versus Supply Voltage

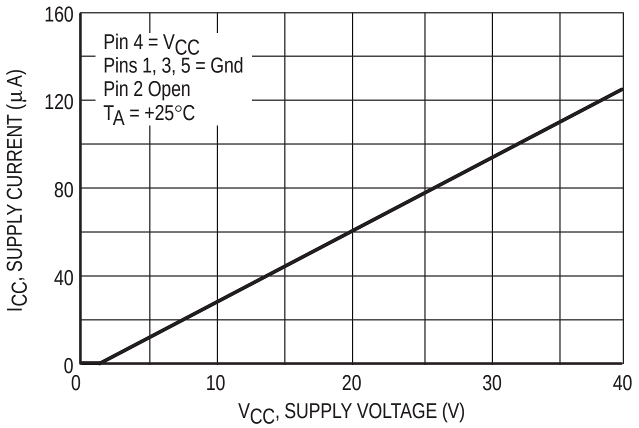


Figure 11. Undervoltage Lockout Threshold versus Temperature

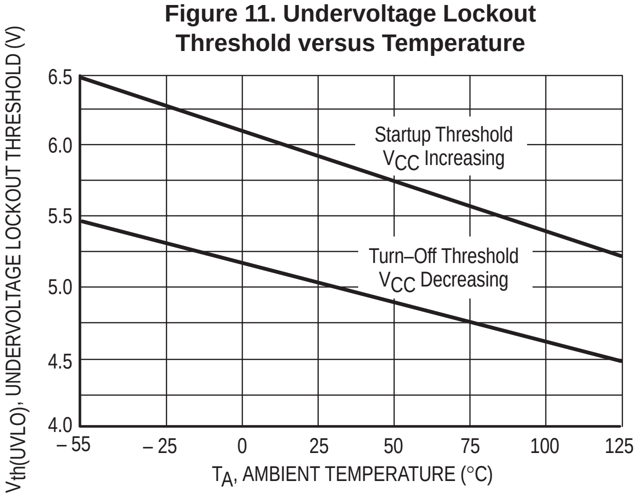


Figure 12. Operating Supply Current versus Supply Voltage

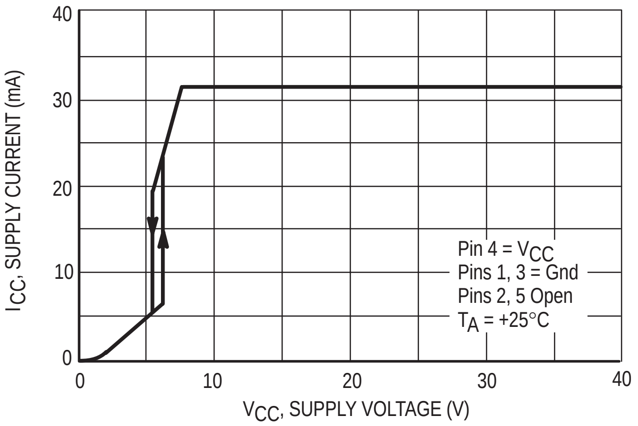


Figure 13. MC34166 Representative Block Diagram

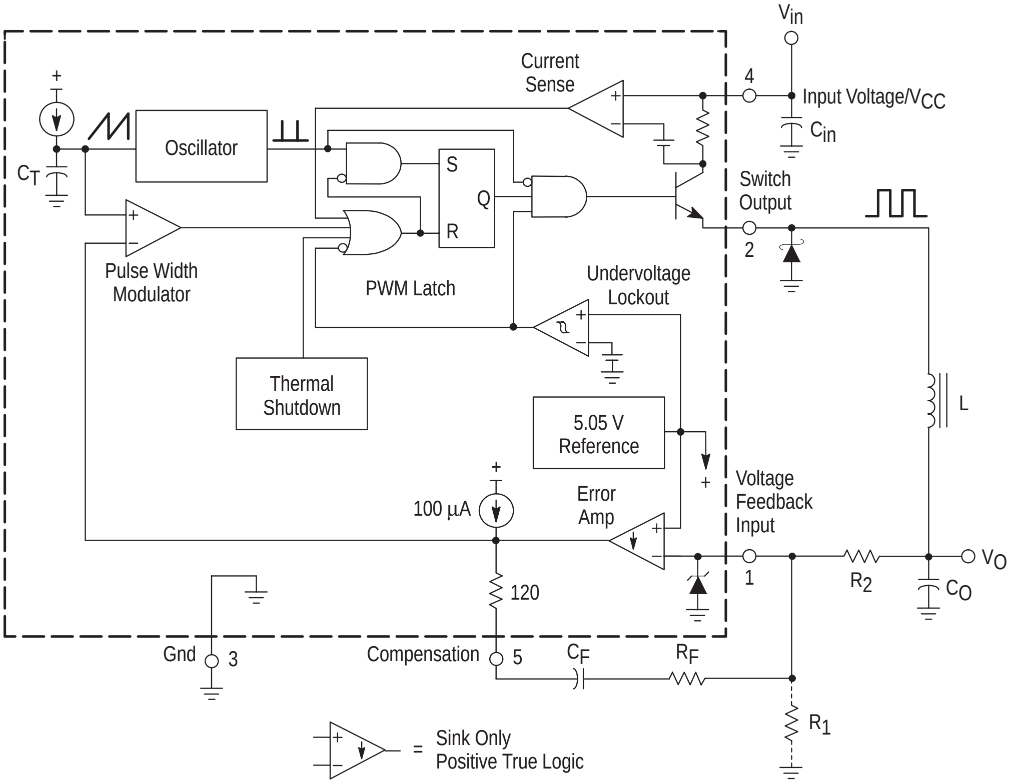
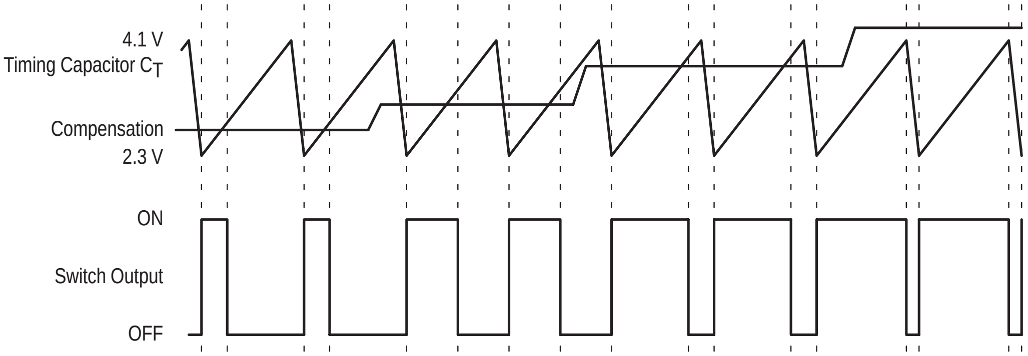


Figure 14. Timing Diagram



INTRODUCTION

The MC34166, MC33166 series are monolithic power switching regulators that are optimized for dc–to–dc converter applications. These devices operate as fixed frequency, voltage mode regulators containing all the active functions required to directly implement step–down and voltage–inverting converters with a minimum number of external components. They can also be used cost effectively in step–up converter applications. Potential markets include automotive, computer, industrial, and cost sensitive consumer products. A description of each section of the device is given below with the representative block diagram shown in Figure 13.

Oscillator

The oscillator frequency is internally programmed to 72 kHz by capacitor C_T and a trimmed current source. The charge to discharge ratio is controlled to yield a 95% maximum duty cycle at the Switch Output. During the discharge of C_T, the oscillator generates an internal blanking pulse that holds the inverting input of the AND gate high, disabling the output switch transistor. The nominal oscillator peak and valley thresholds are 4.1 V and 2.3 V respectively.

Pulse Width Modulator

The Pulse Width Modulator consists of a comparator with the oscillator ramp voltage applied to the noninverting input, while the error amplifier output is applied into the inverting input. Output switch conduction is initiated when C_T is discharged to the oscillator valley voltage. As C_T charges to a voltage that exceeds the error amplifier output, the latch resets, terminating output transistor conduction for the duration of the oscillator ramp–up period. This PWM/Latch combination prevents multiple output pulses during a given oscillator clock cycle. Figures 6 and 14 illustrate the switch output duty cycle versus the compensation voltage.

Current Sense

The MC34166 series utilizes cycle–by–cycle current limiting as a means of protecting the output switch transistor from overstress. Each on–cycle is treated as a separate situation. Current limiting is implemented by monitoring the output switch transistor current buildup during conduction, and upon sensing an overcurrent condition, immediately turning off the switch for the duration of the oscillator ramp–up period.

The collector current is converted to a voltage by an internal trimmed resistor and compared against a reference by the Current Sense comparator. When the current limit threshold is reached, the comparator resets the PWM latch. The current limit threshold is typically set at 4.3 A. Figure 9 illustrates switch output current limit threshold versus temperature.

Error Amplifier and Reference

A high gain Error Amplifier is provided with access to the inverting input and output. This amplifier features a typical dc voltage gain of 80 dB, and a unity gain bandwidth of 600 kHz with 70 degrees of phase margin (Figure 3). The noninverting input is biased to the internal 5.05 V reference and is not pinned out. The reference has an accuracy of ± 2.0% at room temperature. To provide 5.0 V at the load, the reference is programmed 50 mV above 5.0 V to compensate for a 1.0% voltage drop in the cable and connector from the converter output. If the converter design requires an output voltage greater than 5.05 V, resistor R_1 must be added to form a divider network at the feedback input as shown in Figures 13 and 18. The equation for determining the output voltage with the divider network is:

$$V_{out} = 5.05 \left(\frac{R_2}{R_1} + 1\right)$$

External loop compensation is required for converter stability. A simple low–pass filter is formed by connecting a resistor (R_2) from the regulated output to the inverting input, and a series resistor–capacitor (R_F, C_F) between Pins 1 and 5. The compensation network component values shown in each of the applications circuits were selected to provide stability over the tested operating conditions. The step–down converter (Figure 18) is the easiest to compensate for stability. The step–up (Figure 20) and voltage–inverting (Figure 22) configurations operate as continuous conduction flyback converters, and are more difficult to compensate. The simplest way to optimize the compensation network is to observe the response of the output voltage to a step load change, while adjusting R_F and C_F for critical damping. The final circuit should be verified for stability under four boundary conditions. These conditions are minimum and maximum input voltages, with minimum and maximum loads.

By clamping the voltage on the error amplifier output (Pin 5) to less than 150 mV, the internal circuitry will be placed into a low power standby mode, reducing the power supply current to 36 µA with a 12 V supply voltage. Figure 10 illustrates the standby supply current versus supply voltage.

The Error Amplifier output has a 100 µA current source pull–up that can be used to implement soft–start. Figure 17 shows the current source charging capacitor C_{SS} through a series diode. The diode disconnects C_{SS} from the feedback loop when the 1.0 M resistor charges it above the operating range of Pin 5.

Switch Output

The output transistor is designed to switch a maximum of 40 V, with a minimum peak collector current of 3.3 A. When configured for step–down or voltage–inverting applications, as in Figures 18 and 22, the inductor will forward bias the output rectifier when the switch turns off. Rectifiers with a high forward voltage drop or long turn–on delay time should not be used. If the emitter is allowed to go sufficiently negative, collector current will flow, causing additional device heating and reduced conversion efficiency. Figure 8 shows that by clamping the emitter to 0.5 V, the collector current will be in the range of 100 µA over temperature. A 1N5822 or equivalent Schottky barrier rectifier is recommended to fulfill these requirements.

Undervoltage Lockout

An Undervoltage Lockout comparator has been incorporated to guarantee that the integrated circuit is fully functional before the output stage is enabled. The internal 5.05 V reference is monitored by the comparator which enables the output stage when V_{CC} exceeds 5.9 V. To prevent erratic output switching as the threshold is crossed, 0.9 V of hysteresis is provided.

Thermal Protection

Internal Thermal Shutdown circuitry is provided to protect the integrated circuit in the event that the maximum junction temperature is exceeded. When activated, typically at 170°C, the latch is forced into a ‘reset’ state, disabling the output switch. This feature is provided to prevent catastrophic failures from accidental device overheating. **It is not intended to be used as a substitute for proper heatsinking.** The MC34166 is contained in a 5–lead TO–220 type package. The tab of the package is common with the center pin (Pin 3) and is normally connected to ground.

DESIGN CONSIDERATIONS

Do not attempt to construct a converter on wire–wrap or plug–in prototype boards. Special care should be taken to separate ground paths from signal currents and ground paths from load currents. All high current loops should be kept as short as possible using heavy copper runs to minimize ringing and radiated EMI. For best operation, a tight component layout is recommended. Capacitors C_{IN}, C_O, and all feedback components should be placed as close to the IC as physically possible. It is also imperative that the Schottky diode connected to the Switch Output be located as close to the IC as possible.

Figure 15. Low Power Standby Circuit

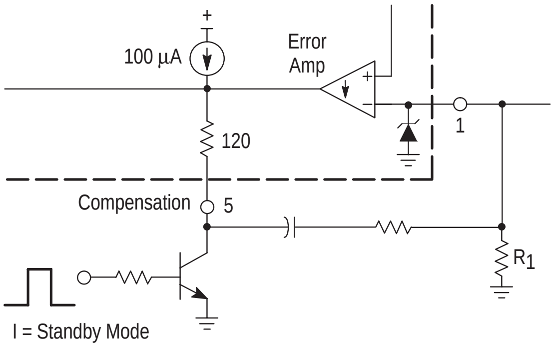
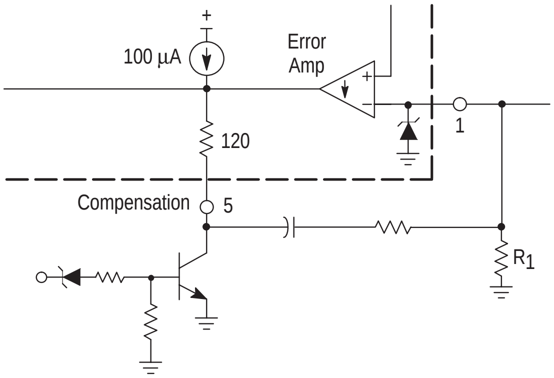
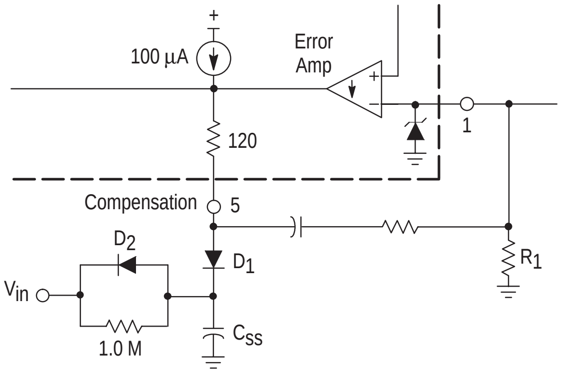


Figure 16. Over Voltage Shutdown Circuit



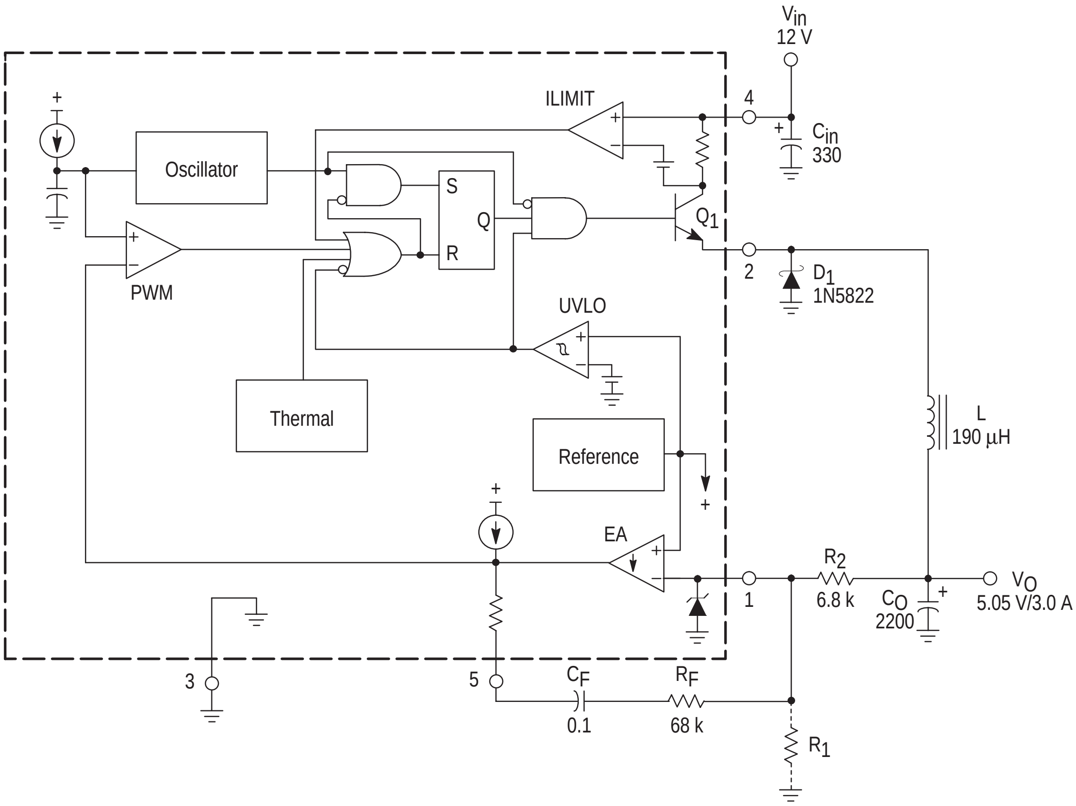
$V_{Shutdown} = V_{Zener} + 0.7$

Figure 17. Soft–Start Circuit



$t_{Soft–Start} \approx 35{,}000\ C_{SS}$

Figure 18. Step–Down Converter

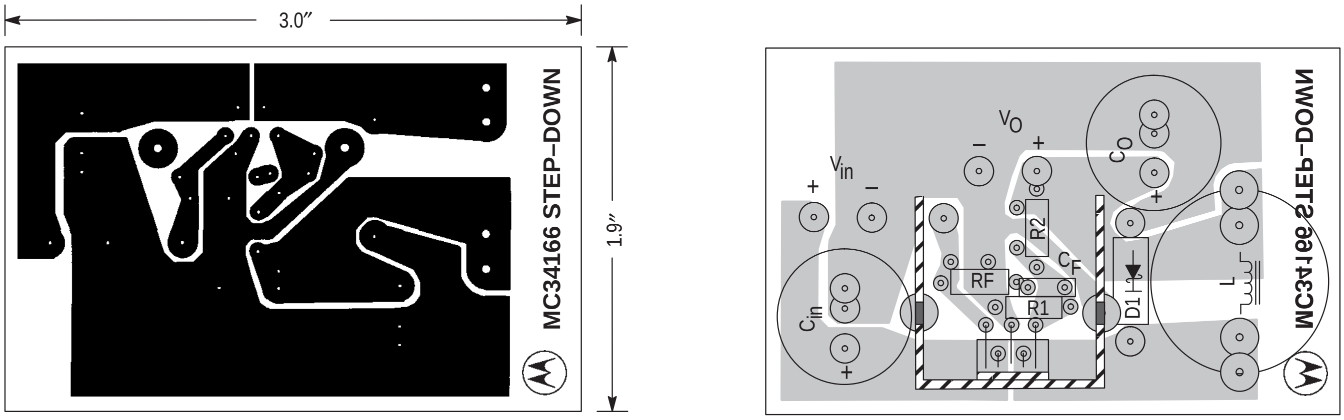


Test	Conditions	Results
Line Regulation	V_{in} = 8.0 V to 36 V, I_O = 3.0 A	5.0 mV = ± 0.05%
Load Regulation	V_{in} = 12 V, I_O = 0.25 A to 3.0 A	2.0 mV = ± 0.02%
Output Ripple	V_{in} = 12 V, I_O = 3.0 A	10 mV_{pp}
Short Circuit Current	V_{in} = 12 V, R_L = 0.1 Ω	4.3 A
Efficiency	V_{in} = 12 V, I_O = 3.0 A	82.8%

L = Coilcraft M1496–A or General Magnetics Technology GMT–0223, 42 turns of #16 AWG on Magnetics Inc. 58350–A2 core. Heatsink = AAVID Engineering Inc. 5903B, or 5930B.

The Step–Down Converter application is shown in Figure 18. The output switch transistor Q_1 interrupts the input voltage, generating a squarewave at the LC_O filter input. The filter averages the squarewaves, producing a dc output voltage that can be set to any level between V_{in} and V_{ref} by controlling the percent conduction time of Q_1 to that of the total oscillator cycle time. If the converter design requires an output voltage greater than 5.05 V, resistor R_1 must be added to form a divider network at the feedback input.

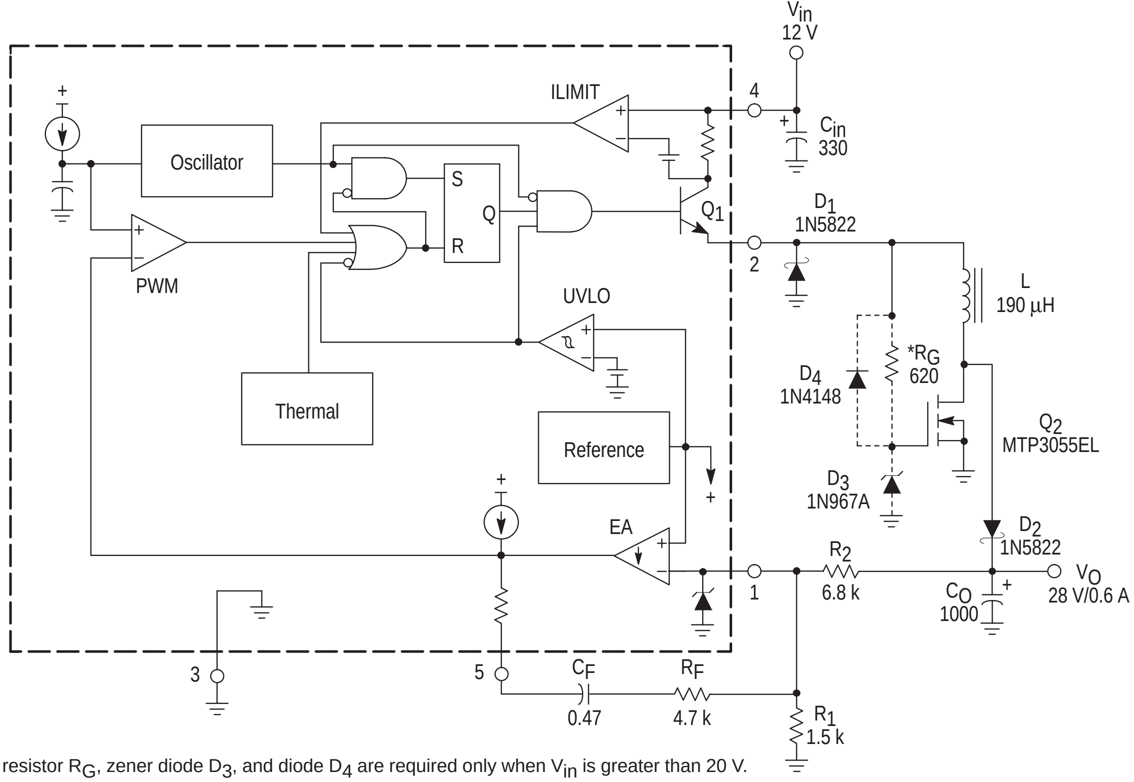
Figure 19. Step–Down Converter Printed Circuit Board and Component Layout



(Bottom View)

(Top View)

Figure 20. Step–Up/Down Converter



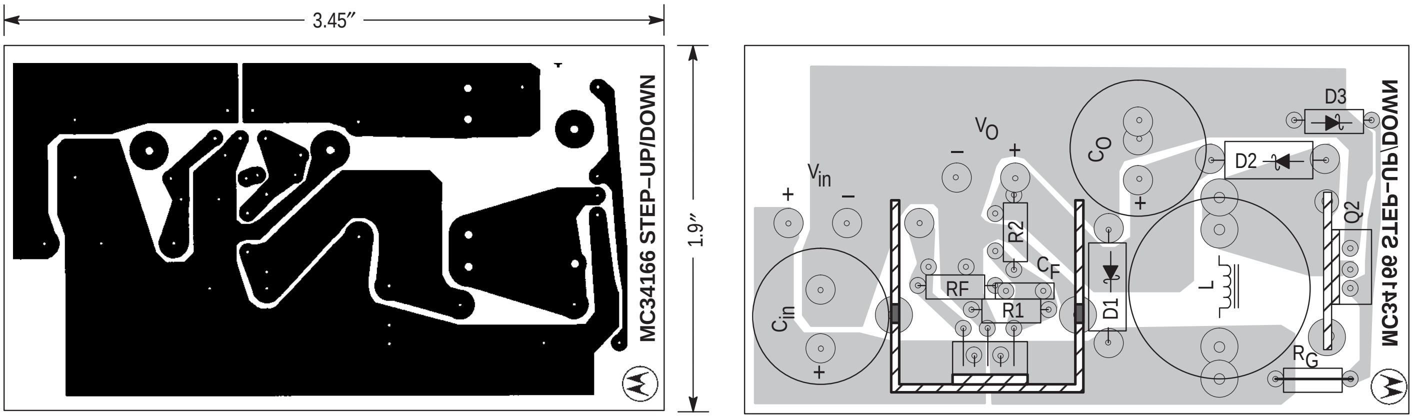
*Gate resistor R_G, zener diode D_3, and diode D_4 are required only when V_{in} is greater than 20 V.

Test	Conditions	Results
Line Regulation	V_{in} = 8.0 V to 24 V, I_O = 0.6 A	23 mV = ± 0.41%
Load Regulation	V_{in} = 12 V, I_O = 0.1 A to 0.6 A	3.0 mV = ± 0.005%
Output Ripple	V_{in} = 12 V, I_O = 0.6 A	100 mV_{pp}
Short Circuit Current	V_{in} = 12 V, R_L = 0.1 Ω	4.0 A
Efficiency	V_{in} = 12 V, I_O = 0.6 A	82.8%

L = Coilcraft M1496–A or General Magnetics Technology GMT–0223, 42 turns of #16 AWG on Magnetics Inc. 58350–A2 core.
Heatsink = AAVID Engineering Inc.
MC34166: 5903B, or 5930B
MTP3055EL: 5925B

Figure 20 shows that the MC34166 can be configured as a step–up/down converter with the addition of an external power MOSFET. Energy is stored in the inductor during the on–time of transistors Q_1 and Q_2. During the off–time, the energy is transferred, with respect to ground, to the output filter capacitor and load. This circuit configuration has two significant advantages over the basic step–up converter circuit. The first advantage is that output short–circuit protection is provided by the MC34166, since Q_1 is directly in series with V_{in} and the load. Second, the output voltage can be programmed to be less than V_{in}. Notice that during the off–time, the inductor forward biases diodes D_1 and D_2, transferring its energy with respect to ground rather than with respect to V_{in}. When operating with V_{in} greater than 20 V, a gate protection network is required for the MOSFET. The network consists of components R_G, D_3, and D_4.

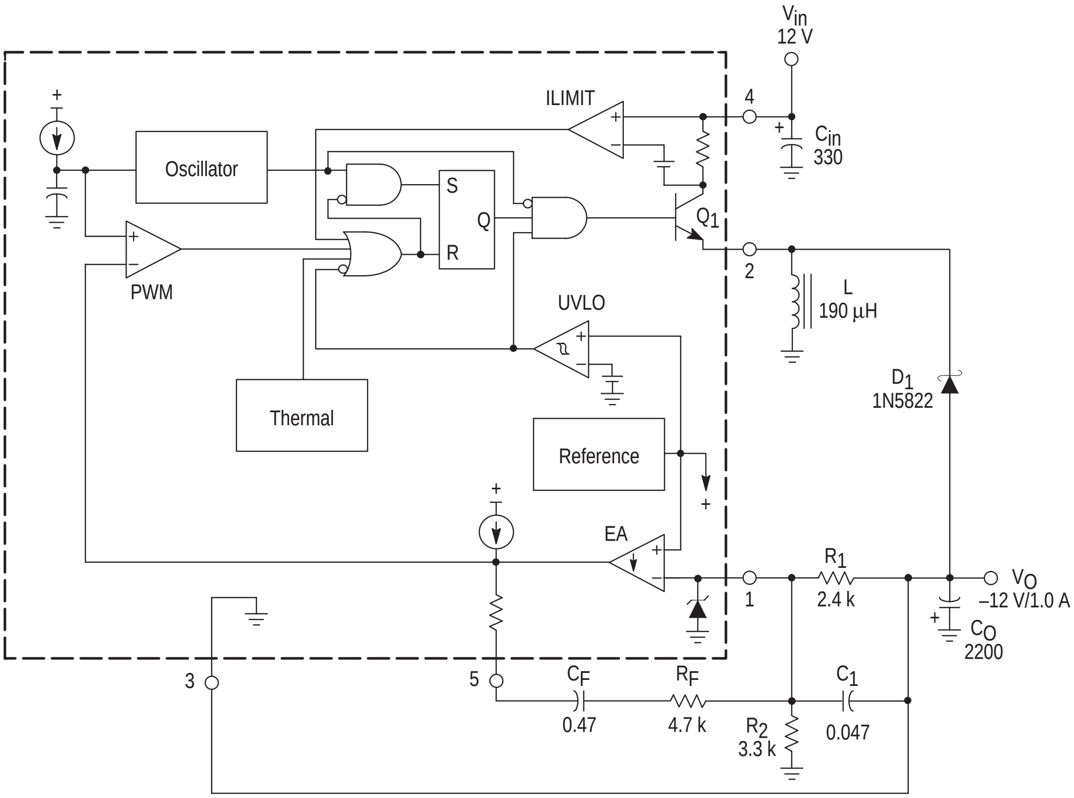
Figure 21. Step–Up/Down Converter Printed Circuit Board and Component Layout



(Bottom View)

(Top View)

Figure 22. Voltage–Inverting Converter

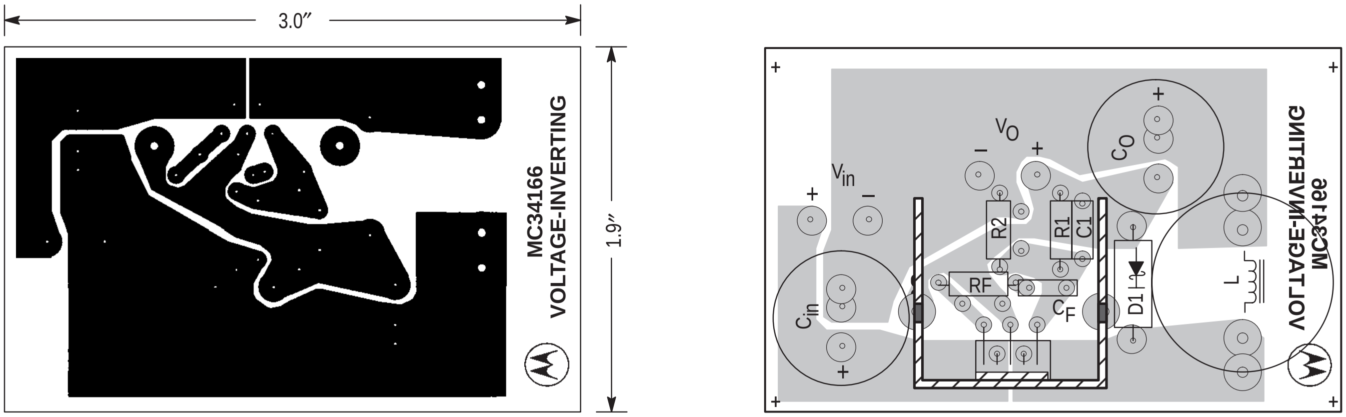


Test	Conditions	Results
Line Regulation	V_{in} = 8.0 V to 24 V, I_O = 1.0 A	3.0 mV = ± 0.01%
Load Regulation	V_{in} = 12 V, I_O = 0.1 A to 1.0 A	4.0 mV = ± 0.017%
Output Ripple	V_{in} = 12 V, I_O = 1.0 A	80 mV_{pp}
Short Circuit Current	V_{in} = 12 V, R_L = 0.1 Ω	3.74 A
Efficiency	V_{in} = 12 V, I_O = 1.0 A	81.2%

L = Coilcraft M1496–A or General Magnetics Technology GMT–0223, 42 turns of #16 AWG on Magnetics Inc. 58350–A2 core. Heatsink = AAVID Engineering Inc. 5903B, or 5930B.

Two potential problems arise when designing the standard voltage–inverting converter with the MC34166. First, the Switch Output emitter is limited to –1.5 V with respect to the ground pin and second, the Error Amplifier's noninverting input is internally committed to the reference and is not pinned out. Both of these problems are resolved by connecting the IC ground pin to the converter's negative output as shown in Figure 22. This keeps the emitter of Q_1 positive with respect to the ground pin and has the effect of reversing the Error Amplifier inputs. Note that the voltage drop across R_1 is equal to 5.05 V when the output is in regulation.

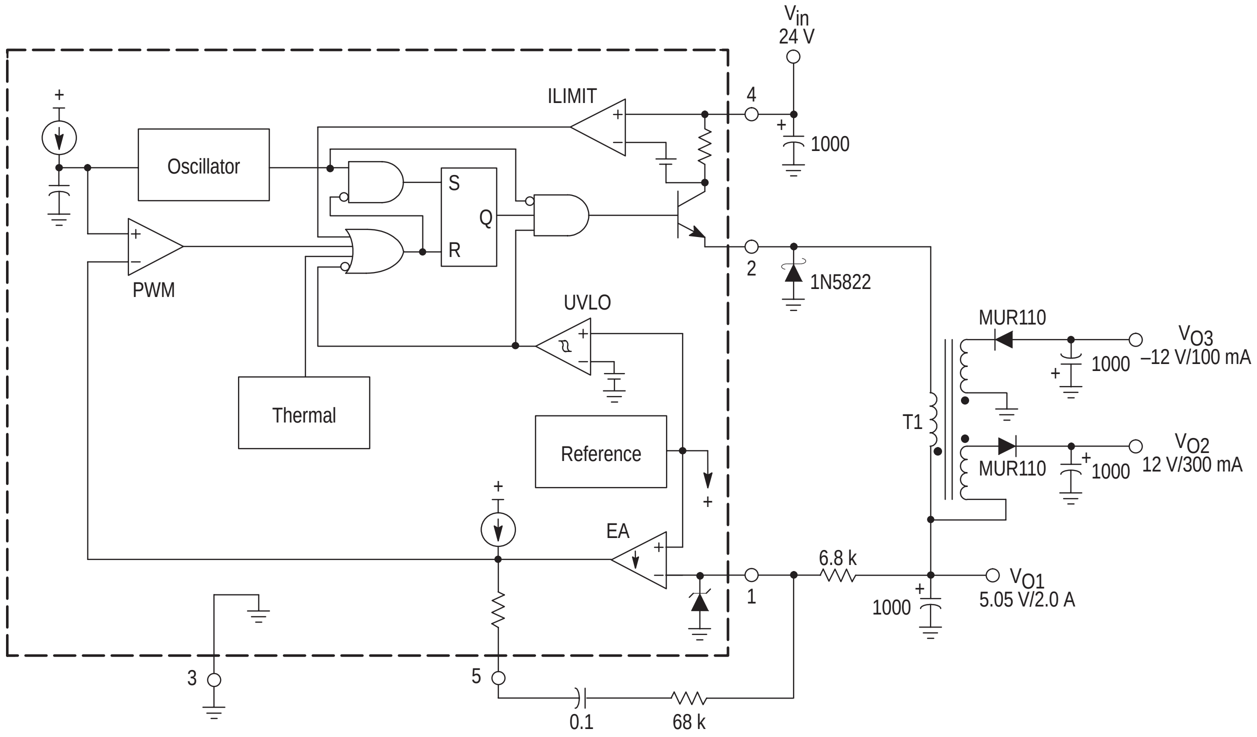
Figure 23. Voltage–Inverting Converter Printed Circuit Board and Component Layout



(Bottom View)

(Top View)

Figure 24. Triple Output Converter



Tests		Conditions	Results
Line Regulation	5.0 V 12 V –12 V	V_{in} = 15 V to 30 V, I_{O1} = 2.0 A, I_{O2} = 300 mA, I_{O3} = 100 mA	4.0 mV = ± 0.04% 450 mV = ±1.9% 350 mV = ±1.5%
Load Regulation	5.0 V 12 V –12 V	V_{in} = 24 V, I_{O1} = 500 mA to 2.0 A, I_{O2} = 300 mA, I_{O3} = 100 mA V_{in} = 24 V, I_{O1} = 2.0 A, I_{O2} = 100 mA to 300 mA, I_{O3} = 100 mA V_{in} = 24 V, I_{O1} = 2.0 A, I_{O2} = 300 mA, I_{O3} = 30 mA to 100 mA	2.0 mV = ± 0.02% 420 mV = ±1.7% 310 mV = ±1.3%
Output Ripple	5.0 V 12 V –12 V	V_{in} = 24 V, I_{O1} = 2.0 A, I_{O2} = 300 mA, I_{O3} = 100 mA	50 mV_{pp} 25 mV_{pp} 10 mV_{pp}
Short Circuit Current	5.0 V 12 V –12 V	V_{in} = 24 V, R_L = 0.1 Ω	4.3 A 1.83 A 1.47 A
Efficiency	TOTAL	V_{in} = 24 V, I_{O1} = 2.0 A, I_{O2} = 300 mA, I_{O3} = 100 mA	83.3%

T1 = Primary: Coilcraft M1496-A or General Magnetics Technology GMT–0223, 42 turns of #16 AWG on Magnetics Inc. 58350-A2 core.
Secondary: V_{O2} — 65 turns of #26 AWG
V_{O3} — 96 turns of #28 AWG
Heatsink = AAVID Engineering Inc. 5903B, or 5930B.

Multiple auxiliary outputs can easily be derived by winding secondaries on the main output inductor to form a transformer. The secondaries must be connected so that the energy is delivered to the auxiliary outputs when the Switch Output turns off. During the OFF time, the voltage across the primary winding is regulated by the feedback loop, yielding a constant Volts/Turn ratio. The number of turns for any given secondary voltage can be calculated by the following equation:

$$\#\ \text{TURNS}_{(SEC)} = \frac{V_{O(SEC)} + V_{F(SEC)}}{\left(\dfrac{V_{O(PRI)} + V_{F(PRI)}}{\#\text{TURNS}_{(PRI)}}\right)}$$

Note that the 12 V winding is stacked on top of the 5.0 V output. This reduces the number of secondary turns and improves lead regulation. For best auxiliary regulation, the auxiliary outputs should be less than 33% of the total output power.

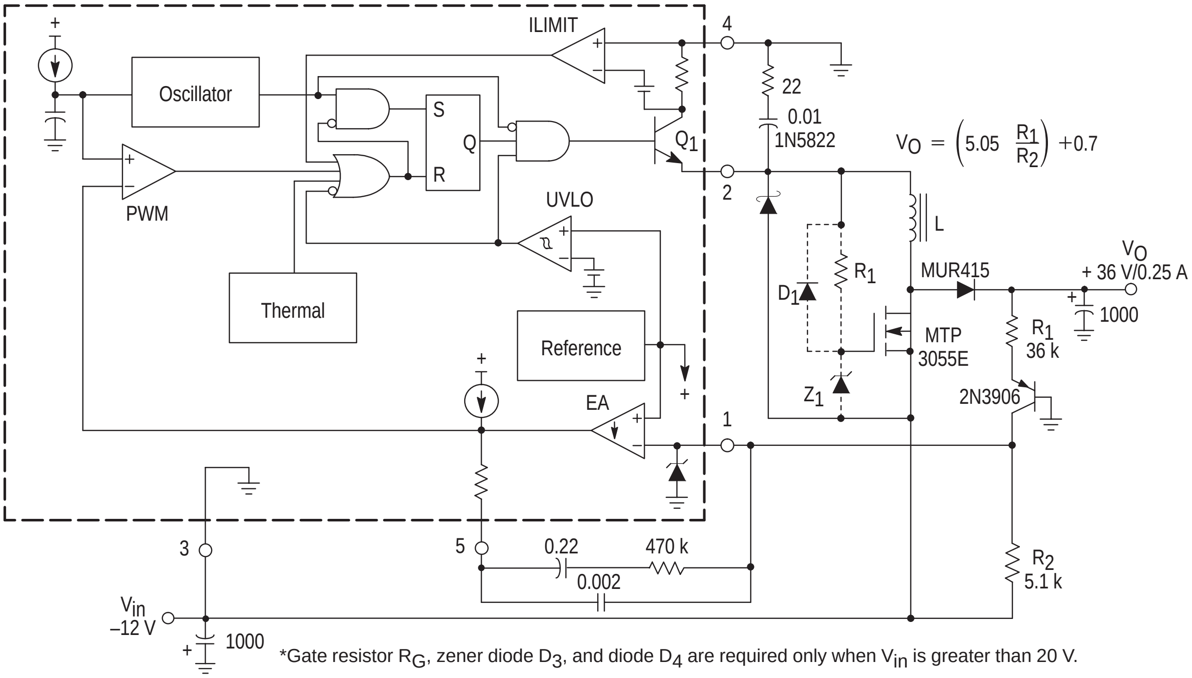


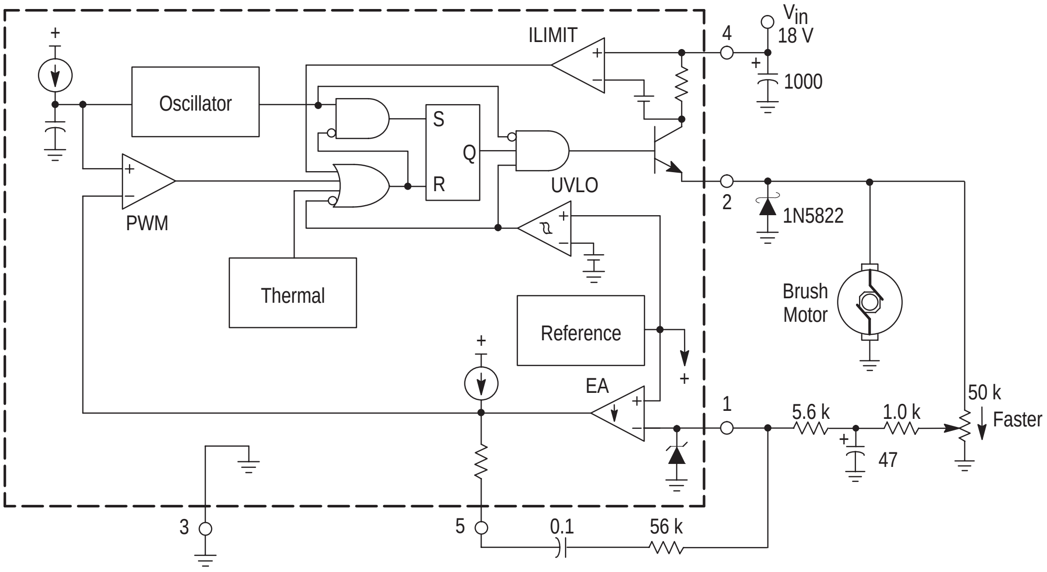
Figure 25. Negative Input/Positive Output Regulator

*Gate resistor R_G, zener diode D_3, and diode D_4 are required only when V_{in} is greater than 20 V.

Test	Conditions	Results
Line Regulation	V_{in} = –10 V to – 20 V, I_O = 0.25 A	250 mV = ± 0.35%
Load Regulation	V_{in} = –12 V, I_O = 0.025 A to 0.25 A	790 mV = ±1.19%
Output Ripple	V_{in} = –12 V, I_O = 0.25 A	80 mV_{pp}
Efficiency	V_{in} = –12 V, I_O = 0.25 A	79.2%

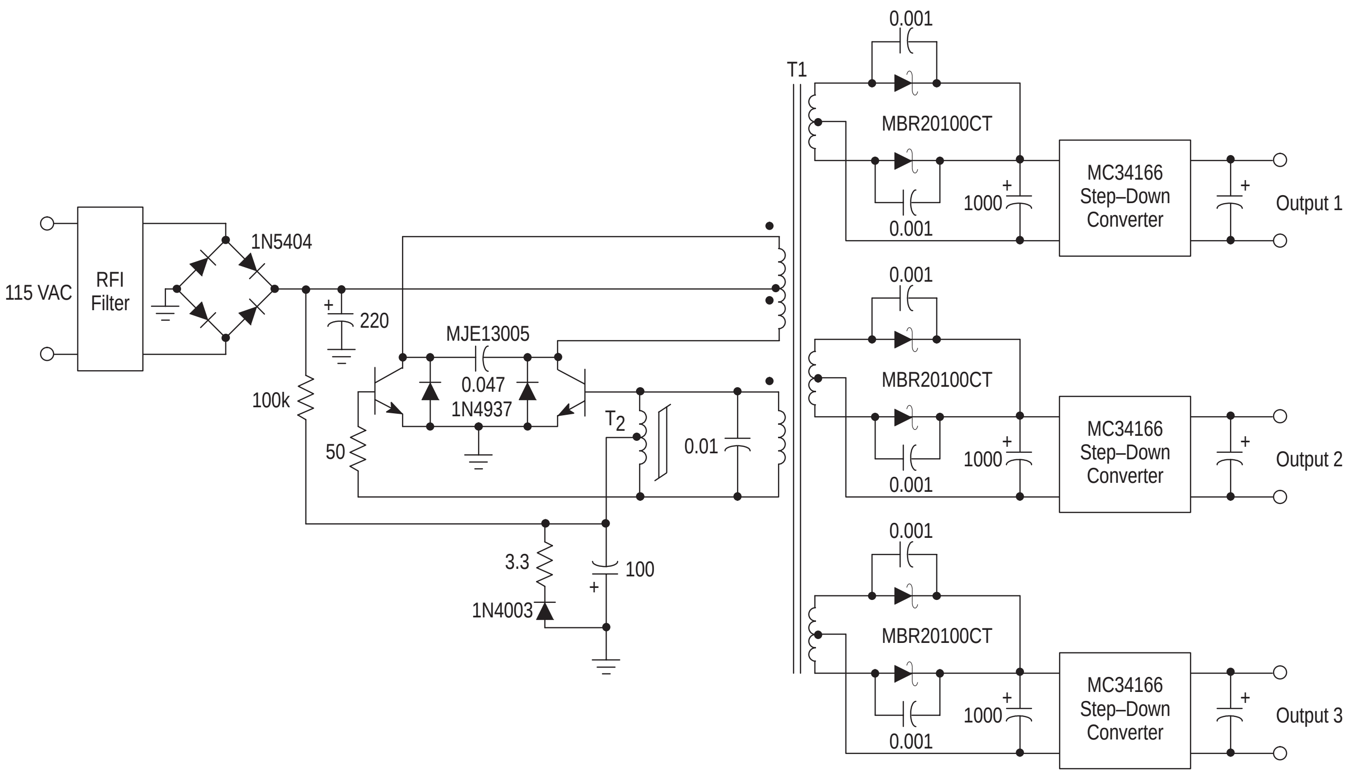
L = Coilcraft M1496–A or ELMACO CHK1050, 42 turns of #16 AWG on Magnetics Inc. 58350–A2 core.
Heatsink = AAVID Engineering Inc. 5903B or 5930B

Figure 26. Variable Motor Speed Control with EMF Feedback Sensing



Test	Conditions	Results
Low Speed Line Regulation	V_{in} = 12 V to 24 V	1760 RPM ±1%
High Speed Line Regulation	V_{in} = 12 V to 24 V	3260 RPM ± 6%

Figure 27. Off–Line Preconverter



T_1 = Core and Bobbin – Coilcraft PT3595
Primary – 104 turns #26 AWG
Base Drive – 3 turns #26 AWG
Secondaries – 16 turns #16 AWG
Total Gap – 0.002″

T_2 = Core – TDK T6 x 1.5 x 3 H5C2
14 turns center tapped #30 AWG
Heatsink = AAVID Engineering Inc.
MC34166 and MJE13005 – 5903B
MBR20100CT – 5925B

The MC34166 can be used cost effectively in off–line applications even though it is limited to a maximum input voltage of 40 V. Figure 27 shows a simple and efficient method for converting the AC line voltage down to 24 V. This preconverter has a total power rating of 125 W with a conversion efficiency of 90%. Transformer T_1 provides output isolation from the AC line and isolation between each of the secondaries. The circuit self–oscillates at 50 kHz and is controlled by the saturation characteristics of T_2. Multiple MC34166 post regulators can be used to provide accurate independently regulated outputs for a distributed power system.

Figure 28. D²PAK Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length

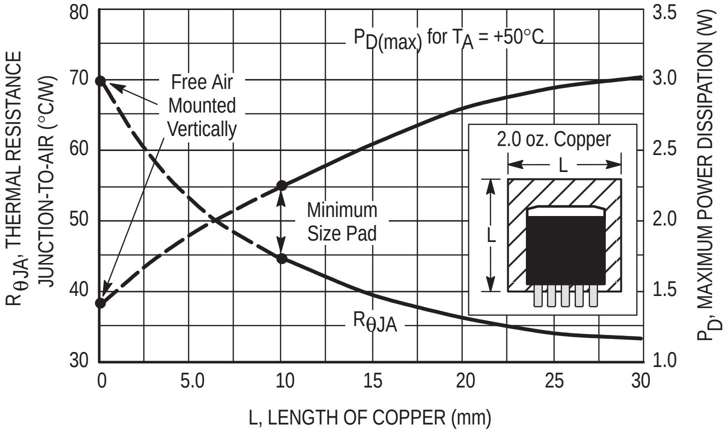


Table 1. Design Equations

Calculation	Step–Down	Step–Up/Down	Voltage–Inverting
$\frac{t_{on}}{t_{off}}$ (Notes 1, 2)	$\frac{V_{out} + V_F}{V_{in} - V_{sat} - V_{out}}$	$\frac{V_{out} + V_{F1} + V_{F2}}{V_{in} - V_{satQ1} - V_{satQ2}}$	$\frac{\lvert V_{out} \rvert + V_F}{V_{in} - V_{sat}}$
t_{on}	$\frac{\frac{t_{on}}{t_{off}}}{f_{osc}\left(\frac{t_{on}}{t_{off}} + 1\right)}$	$\frac{\frac{t_{on}}{t_{off}}}{f_{osc}\left(\frac{t_{on}}{t_{off}} + 1\right)}$	$\frac{\frac{t_{on}}{t_{off}}}{f_{osc}\left(\frac{t_{on}}{t_{off}} + 1\right)}$
Duty Cycle (Note 3)	$t_{on}\ f_{osc}$	$t_{on}\ f_{osc}$	$t_{on}\ f_{osc}$
$I_{L\ avg}$	I_{out}	$I_{out}\left(\frac{t_{on}}{t_{off}} + 1\right)$	$I_{out}\left(\frac{t_{on}}{t_{off}} + 1\right)$
$I_{pk(switch)}$	$I_{L\ avg} + \frac{\Delta I_L}{2}$	$I_{L\ avg} + \frac{\Delta I_L}{2}$	$I_{L\ avg} + \frac{\Delta I_L}{2}$
L	$\left(\frac{V_{in} - V_{sat} - V_{out}}{\Delta I_L}\right)t_{on}$	$\left(\frac{V_{in} - V_{satQ1} - V_{satQ2}}{\Delta I_L}\right)t_{on}$	$\left(\frac{V_{in} - V_{sat}}{\Delta I_L}\right)t_{on}$
$V_{ripple(pp)}$	$\Delta I_L \sqrt{\left(\frac{1}{8f_{osc}C_O}\right)^2 + (ESR)^2}$	$\left(\frac{t_{on}}{t_{off}} + 1\right)\sqrt{\left(\frac{1}{f_{osc}C_O}\right)^2 + (ESR)^2}$	$\left(\frac{t_{on}}{t_{off}} + 1\right)\sqrt{\left(\frac{1}{f_{osc}C_O}\right)^2 + (ESR)^2}$
V_{out}	$V_{ref}\left(\frac{R_2}{R_1} + 1\right)$	$V_{ref}\left(\frac{R_2}{R_1} + 1\right)$	$V_{ref}\left(\frac{R_2}{R_1} + 1\right)$

NOTES: 1. V_{sat} – Switch Output source saturation voltage, refer to Figure 7.
2. V_F – Output rectifier forward voltage drop. Typical value for 1N5822 Schottky barrier rectifier is 0.5 V.
3. Duty cycle is calculated at the minimum operating input voltage and must not exceed the guaranteed minimum $DC_{(max)}$ specification of 0.92.

The following converter characteristics must be chosen:

V_{out} – Desired output voltage.
I_{out} – Desired output current.
ΔI_L – Desired peak–to–peak inductor ripple current. For maximum output current especially when the duty cycle is greater than 0.5, it is suggested that ΔI_L be chosen to be less than 10% of the average inductor current $I_{L\ avg}$. This will help prevent $I_{pk(switch)}$ from reaching the guaranteed minimum current limit threshold of 3.3 A. If the design goal is to use a minimum inductance value, let $\Delta I_L = 2\ (I_{L\ avg})$. This will proportionally reduce the converter’s output current capability.
$V_{ripple(pp)}$ – Desired peak–to–peak output ripple voltage. For best performance, the ripple voltage should be kept to less than 2% of V_{out}. Capacitor C_O should be a low equivalent series resistance (ESR) electrolytic designed for switching regulator applications.

MOTOROLA

MC34167
MC33167

Power Switching Regulators

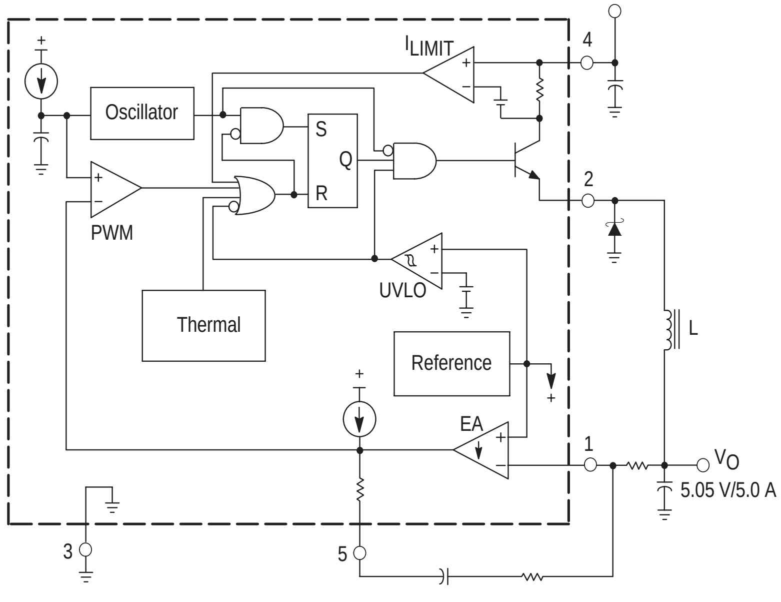
The MC34167, MC33167 series are high performance fixed frequency power switching regulators that contain the primary functions required for dc–to–dc converters. This series was specifically designed to be incorporated in step–down and voltage–inverting configurations with a minimum number of external components and can also be used cost effectively in step–up applications.

These devices consist of an internal temperature compensated reference, fixed frequency oscillator with on–chip timing components, latching pulse width modulator for single pulse metering, high gain error amplifier, and a high current output switch.

Protective features consist of cycle–by–cycle current limiting, undervoltage lockout, and thermal shutdown. Also included is a low power standby mode that reduces power supply current to 36 µA.

- Output Switch Current in Excess of 5.0 A
- Fixed Frequency Oscillator (72 kHz) with On–Chip Timing
- Provides 5.05 V Output without External Resistor Divider
- Precision 2% Reference
- 0% to 95% Output Duty Cycle
- Cycle–by–Cycle Current Limiting
- Undervoltage Lockout with Hysteresis
- Internal Thermal Shutdown
- Operation from 7.5 V to 40 V
- Standby Mode Reduces Power Supply Current to 36 µA
- Economical 5–Lead TO–220 Package with Two Optional Leadforms
- Also Available in Surface Mount D^{2}PAK Package

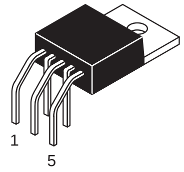
Simplified Block Diagram
(Step Down Application)



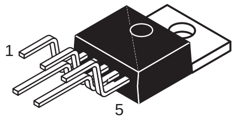
This device contains 143 active transistors.

POWER SWITCHING REGULATORS

SEMICONDUCTOR TECHNICAL DATA

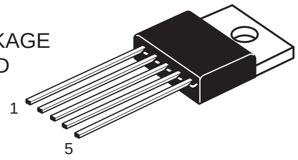


TH SUFFIX
PLASTIC PACKAGE
CASE 314A



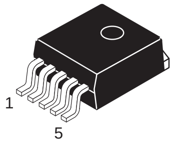
TV SUFFIX
PLASTIC PACKAGE
CASE 314B

Heatsink surface connected to Pin 3.



T SUFFIX
PLASTIC PACKAGE
CASE 314D

Pin 1. Voltage Feedback Input
2. Switch Output
3. Ground
4. Input Voltage/V_{CC}
5. Compensation/Standby



D2T SUFFIX
PLASTIC PACKAGE
CASE 936A
(D^{2}PAK)

Heatsink surface (shown as terminal 6
in case outline drawing) is connected to Pin 3.

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC33167D2T	T_A = –40° to +85°C	Surface Mount
MC33167T		Straight Lead
MC33167TH		Horiz. Mount
MC33167TV		Vertical Mount
MC34167D2T	T_A = 0° to + 70°C	Surface Mount
MC34167T		Straight Lead
MC34167TH		Horiz. Mount
MC34167TV		Vertical Mount

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Input Voltage	V_{CC}	40	V
Switch Output Voltage Range	$V_{O(switch)}$	–2.0 to + V_{in}	V
Voltage Feedback and Compensation Input Voltage Range	V_{FB},V_{Comp}	–1.0 to + 7.0	V
Power Dissipation Case 314A, 314B and 314D (T_A = +25°C) Thermal Resistance, Junction–to–Ambient Thermal Resistance, Junction–to–Case Case 936A (D^2PAK) (T_A = +25°C) Thermal Resistance, Junction–to–Ambient Thermal Resistance, Junction–to–Case	 P_D θ_{JA} θ_{JC} P_D θ_{JA} θ_{JC}	 Internally Limited 65 5.0 Internally Limited 70 5.0	 W °C/W °C/W W °C/W °C/W
Operating Junction Temperature	T_J	+150	°C
Operating Ambient Temperature (Note 3) MC34167 MC33167	T_A	 0 to + 70 – 40 to + 85	°C
Storage Temperature Range	T_{stg}	– 65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 12 V, for typical values T_A = +25°C, for min/max values T_A is the operating ambient temperature range that applies [Notes 2, 3], unless otherwise noted.)

Characteristic		Symbol	Min	Typ	Max	Unit
OSCILLATOR						
Frequency (V_{CC} = 7.5 V to 40 V)	T_A = +25°C T_A = T_{low} to T_{high}	f_{OSC}	65 62	72 –	79 81	kHz
ERROR AMPLIFIER						
Voltage Feedback Input Threshold	T_A =+ 25°C T_A = T_{low} to T_{high}	$V_{FB(th)}$	4.95 4.85	5.05 –	5.15 5.20	V
Line Regulation (V_{CC} = 7.5 V to 40 V, T_A = +25°C)		Reg_{line}	–	0.03	0.078	%/V
Input Bias Current (V_{FB} = $V_{FB(th)}$ + 0.15 V)		I_{IB}	–	0.15	1.0	µA
Power Supply Rejection Ratio (V_{CC} = 10 V to 20 V, f = 120 Hz)		PSRR	60	80	–	dB
Output Voltage Swing	High State (I_{Source} = 75 µA, V_{FB} = 4.5 V) Low State (I_{Sink} = 0.4 mA, V_{FB} = 5.5 V)	V_{OH} V_{OL}	4.2 –	4.9 1.6	– 1.9	V
PWM COMPARATOR						
Duty Cycle (V_{CC} = 20 V)	Maximum (V_{FB} = 0 V) Minimum (V_{Comp} = 1.9 V)	$DC_{(max)}$ $DC_{(min)}$	92 0	95 0	100 0	%
SWITCH OUTPUT						
Output Voltage Source Saturation (V_{CC} = 7.5 V, I_{Source} = 5.0 A)		V_{sat}	–	(V_{CC} –1.5)	(V_{CC} –1.8)	V
Off–State Leakage (V_{CC} = 40 V, Pin 2 = Gnd)		$I_{sw(off)}$	–	0	100	µA
Current Limit Threshold (V_{CC} = 7.5 V)		$I_{pk(switch)}$	5.5	6.5	8.0	A
Switching Times (V_{CC} = 40 V, I_{pk} = 5.0 A, L = 225 µH, T_A = +25°C) Output Voltage Rise Time Output Voltage Fall Time		 t_r t_f	 – –	 100 50	 200 100	ns
UNDERVOLTAGE LOCKOUT						
Startup Threshold (V_{CC} Increasing, T_A = +25°C)		$V_{th(UVLO)}$	5.5	5.9	6.3	V
Hysteresis (V_{CC} Decreasing, T_A = +25°C)		$V_{H(UVLO)}$	0.6	0.9	1.2	V
TOTAL DEVICE						
Power Supply Current (T_A = +25°C) Standby (V_{CC} = 12 V, V_{Comp} < 0.15 V) Operating (V_{CC} = 40 V, Pin 1 = Gnd for maximum duty cycle)		I_{CC}	 – –	 36 40	 100 60	 µA mA

NOTES: 1. Maximum package power dissipation limits must be observed to prevent thermal shutdown activation.
2. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
3. T_{low} = 0°C for MC34167 T_{high} = + 70°C for MC34167
= – 40°C for MC33167 = + 85°C for MC33167

Figure 1. Voltage Feedback Input Threshold versus Temperature

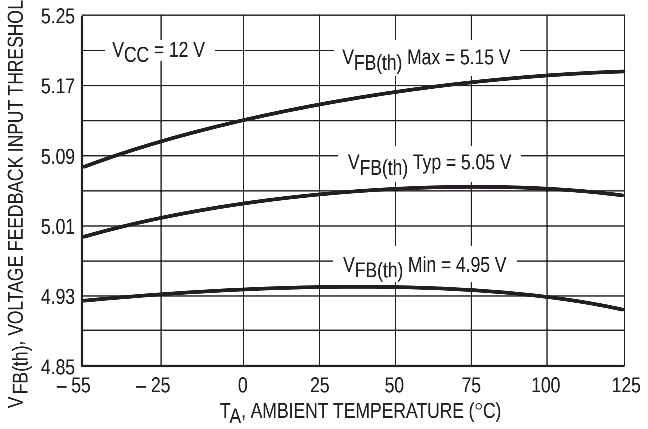


Figure 2. Voltage Feedback Input Bias Current versus Temperature

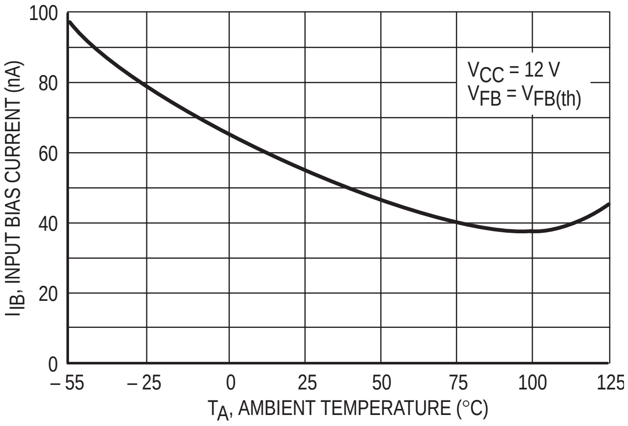


Figure 3. Error Amp Open Loop Gain and Phase versus Frequency

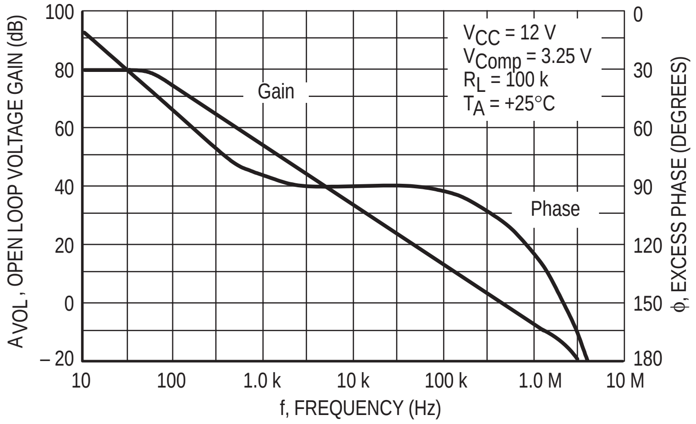


Figure 4. Error Amp Output Saturation versus Sink Current

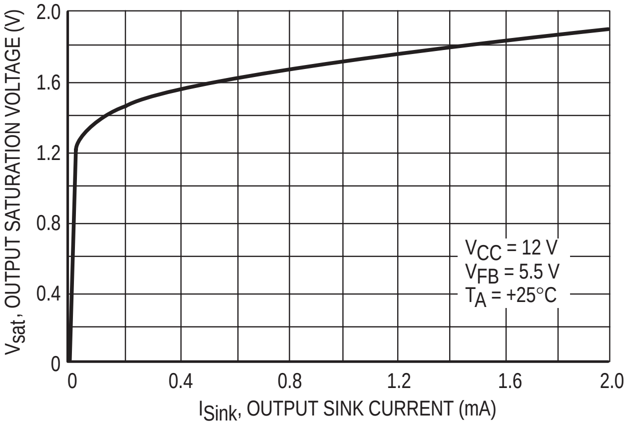


Figure 5. Oscillator Frequency Change versus Temperature

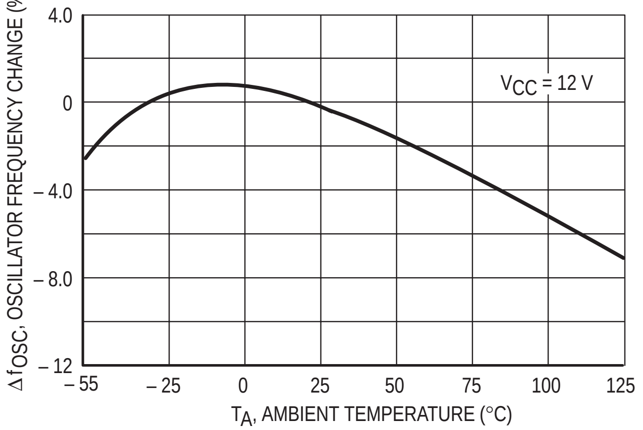


Figure 6. Switch Output Duty Cycle versus Compensation Voltage

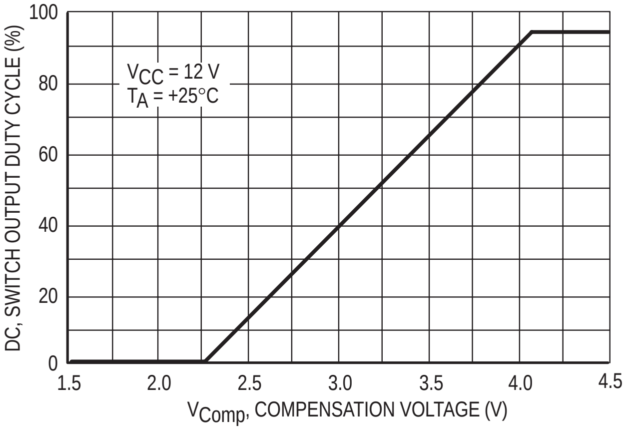


Figure 7. Switch Output Source Saturation versus Source Current

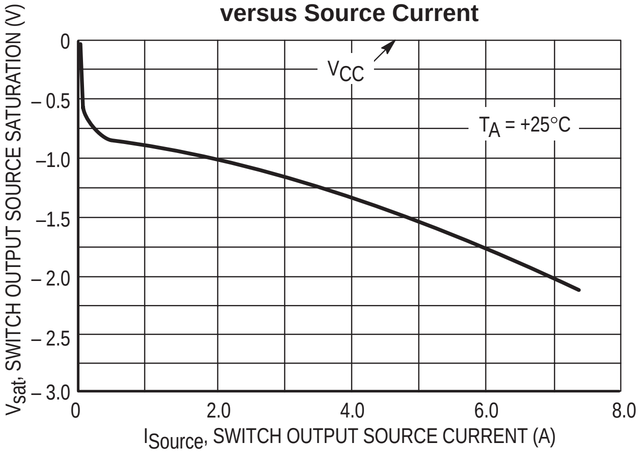


Figure 8. Negative Switch Output Voltage versus Temperature

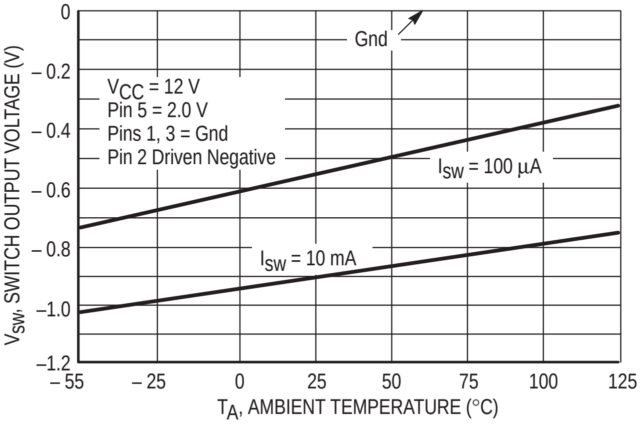


Figure 9. Switch Output Current Limit Threshold versus Temperature

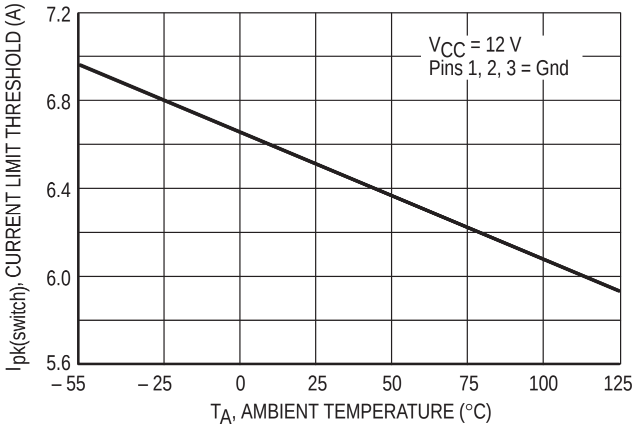


Figure 10. Standby Supply Current versus Supply Voltage

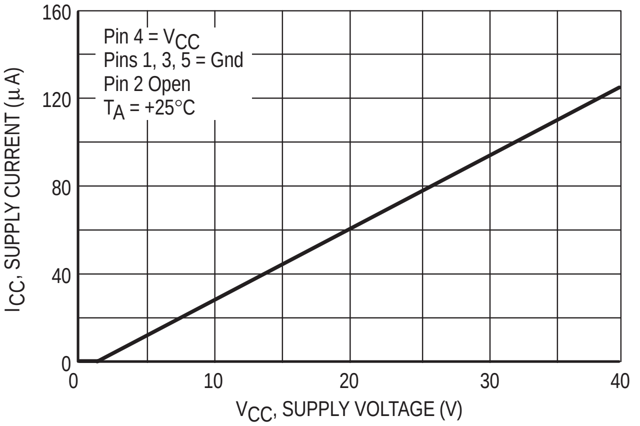


Figure 11. Undervoltage Lockout Thresholds versus Temperature

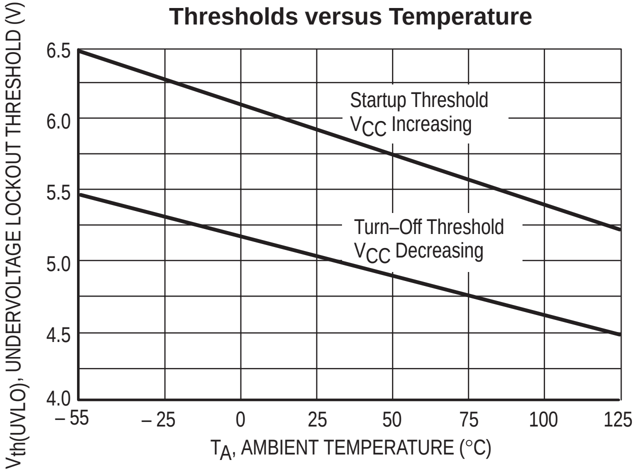


Figure 12. Operating Supply Current versus Supply Voltage

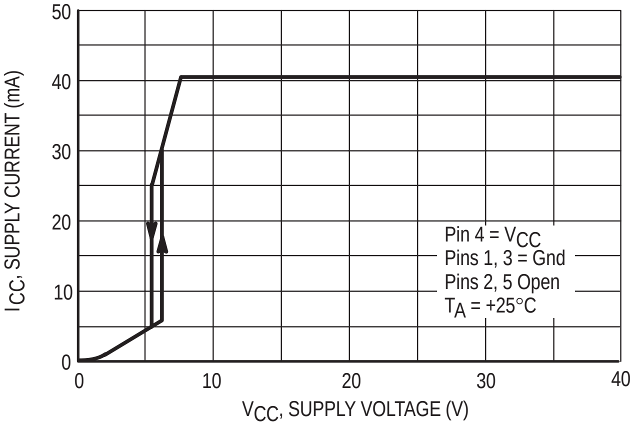


Figure 13. MC34167 Representative Block Diagram

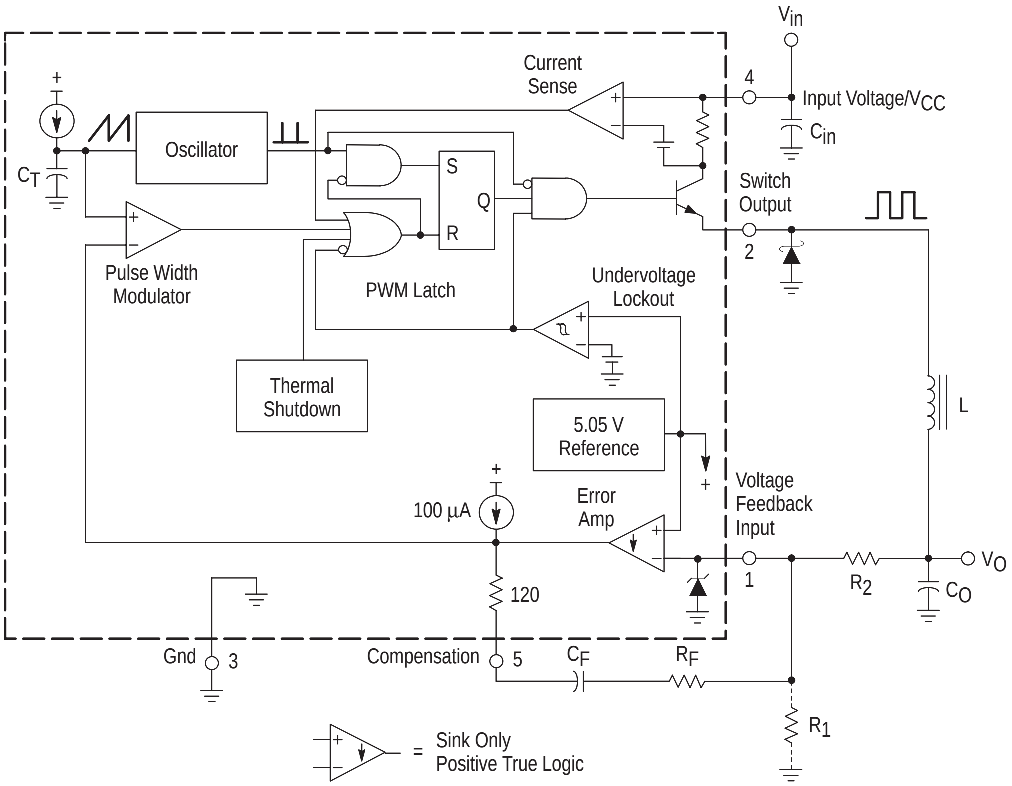
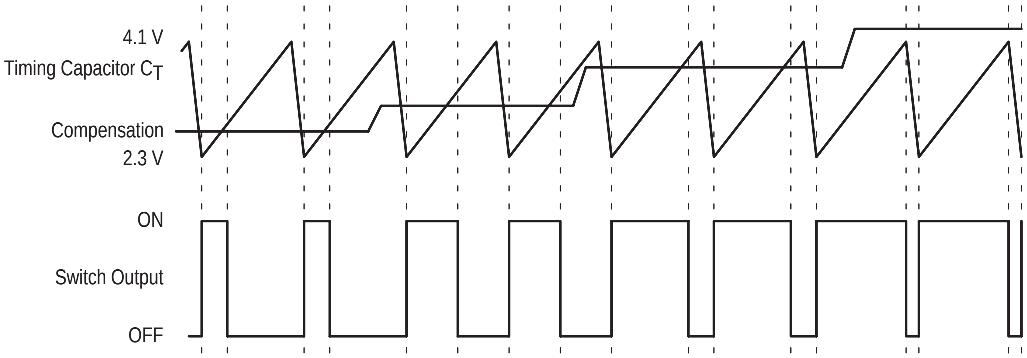


Figure 14. Timing Diagram



INTRODUCTION

The MC34167, MC33167 series are monolithic power switching regulators that are optimized for dc–to–dc converter applications. These devices operate as fixed frequency, voltage mode regulators containing all the active functions required to directly implement step–down and voltage–inverting converters with a minimum number of external components. They can also be used cost effectively in step–up converter applications. Potential markets include automotive, computer, industrial, and cost sensitive consumer products. A description of each section of the device is given below with the representative block diagram shown in Figure 13.

Oscillator

The oscillator frequency is internally programmed to 72 kHz by capacitor C_T and a trimmed current source. The charge to discharge ratio is controlled to yield a 95% maximum duty cycle at the Switch Output. During the discharge of C_T, the oscillator generates an internal blanking pulse that holds the inverting input of the AND gate high, disabling the output switch transistor. The nominal oscillator peak and valley thresholds are 4.1 V and 2.3 V respectively.

Pulse Width Modulator

The Pulse Width Modulator consists of a comparator with the oscillator ramp voltage applied to the noninverting input, while the error amplifier output is applied into the inverting input. Output switch conduction is initiated when C_T is discharged to the oscillator valley voltage. As C_T charges to a voltage that exceeds the error amplifier output, the latch resets, terminating output transistor conduction for the duration of the oscillator ramp–up period. This PWM/Latch combination prevents multiple output pulses during a given oscillator clock cycle. Figures 6 and 14 illustrate the switch output duty cycle versus the compensation voltage.

Current Sense

The MC34167 series utilizes cycle–by–cycle current limiting as a means of protecting the output switch transistor from overstress. Each on cycle is treated as a separate situation. Current limiting is implemented by monitoring the output switch transistor current buildup during conduction, and upon sensing an overcurrent condition, immediately turning off the switch for the duration of the oscillator ramp–up period.

The collector current is converted to a voltage by an internal trimmed resistor and compared against a reference by the Current Sense comparator. When the current limit threshold is reached, the comparator resets the PWM latch. The current limit threshold is typically set at 6.5 A. Figure 9 illustrates switch output current limit threshold versus temperature.

Error Amplifier and Reference

A high gain Error Amplifier is provided with access to the inverting input and output. This amplifier features a typical dc voltage gain of 80 dB, and a unity gain bandwidth of 600 kHz with 70 degrees of phase margin (Figure 3). The noninverting input is biased to the internal 5.05 V reference and is not pinned out. The reference has an accuracy of ± 2.0% at room temperature. To provide 5.0 V at the load, the reference is programmed 50 mV above 5.0 V to compensate for a 1.0% voltage drop in the cable and connector from the converter output. If the converter design requires an output voltage greater than 5.05 V, resistor R_1 must be added to form a divider network at the feedback input as shown in Figures 13 and 18. The equation for determining the output voltage with the divider network is:

$$V_{out} = 5.05\left(\frac{R_2}{R_1} + 1\right)$$

External loop compensation is required for converter stability. A simple low–pass filter is formed by connecting a resistor (R_2) from the regulated output to the inverting input, and a series resistor–capacitor (R_F, C_F) between Pins 1 and 5. The compensation network component values shown in each of the applications circuits were selected to provide stability over the tested operating conditions. The step–down converter (Figure 18) is the easiest to compensate for stability. The step–up (Figure 20) and voltage–inverting (Figure 22) configurations operate as continuous conduction flyback converters, and are more difficult to compensate. The simplest way to optimize the compensation network is to observe the response of the output voltage to a step load change, while adjusting R_F and C_F for critical damping. The final circuit should be verified for stability under four boundary conditions. These conditions are minimum and maximum input voltages, with minimum and maximum loads.

By clamping the voltage on the error amplifier output (Pin 5) to less than 150 mV, the internal circuitry will be placed into a low power standby mode, reducing the power supply current to 36 µA with a 12 V supply voltage. Figure 10 illustrates the standby supply current versus supply voltage.

The Error Amplifier output has a 100 µA current source pull–up that can be used to implement soft–start. Figure 17 shows the current source charging capacitor C_{SS} through a series diode. The diode disconnects C_{SS} from the feedback loop when the 1.0 M resistor charges it above the operating range of Pin 5.

Switch Output

The output transistor is designed to switch a maximum of 40 V, with a minimum peak collector current of 5.5 A. When configured for step–down or voltage–inverting applications, as in Figures 18 and 22, the inductor will forward bias the output rectifier when the switch turns off. Rectifiers with a high forward voltage drop or long turn on delay time should not be used. If the emitter is allowed to go sufficiently negative, collector current will flow, causing additional device heating and reduced conversion efficiency. Figure 8 shows that by clamping the emitter to 0.5 V, the collector current will be in the range of 100 µA over temperature. A 1N5825 or equivalent Schottky barrier rectifier is recommended to fulfill these requirements.

Undervoltage Lockout

An Undervoltage Lockout comparator has been incorporated to guarantee that the integrated circuit is fully functional before the output stage is enabled. The internal reference voltage is monitored by the comparator which enables the output stage when V_{CC} exceeds 5.9 V. To prevent erratic output switching as the threshold is crossed, 0.9 V of hysteresis is provided.

Thermal Protection

Internal Thermal Shutdown circuitry is provided to protect the integrated circuit in the event that the maximum junction temperature is exceeded. When activated, typically at 170°C, the latch is forced into a ‘reset’ state, disabling the output switch. This feature is provided to prevent catastrophic failures from accidental device overheating. **It is not intended to be used as a substitute for proper heatsinking.** The MC34167 is contained in a 5–lead TO–220 type package. The tab of the package is common with the center pin (Pin 3) and is normally connected to ground.

DESIGN CONSIDERATIONS

Do not attempt to construct a converter on wire–wrap or plug–in prototype boards. Special care should be taken to separate ground paths from signal currents and ground paths from load currents. All high current loops should be kept as short as possible using heavy copper runs to minimize ringing and radiated EMI. For best operation, a tight component layout is recommended. Capacitors C_{in}, C_O, and all feedback components should be placed as close to the IC as physically possible. It is also imperative that the Schottky diode connected to the Switch Output be located as close to the IC as possible.

Figure 15. Low Power Standby Circuit

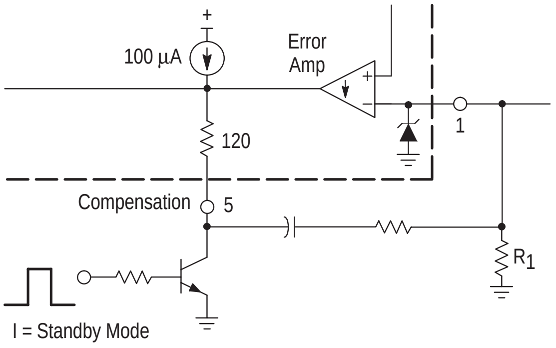
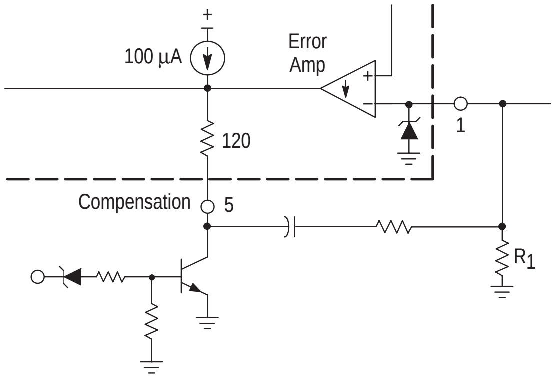
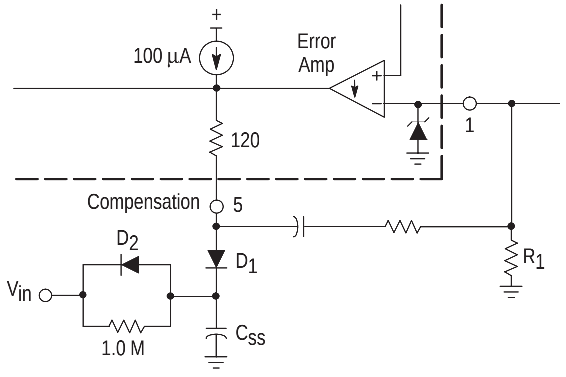


Figure 16. Over Voltage Shutdown Circuit



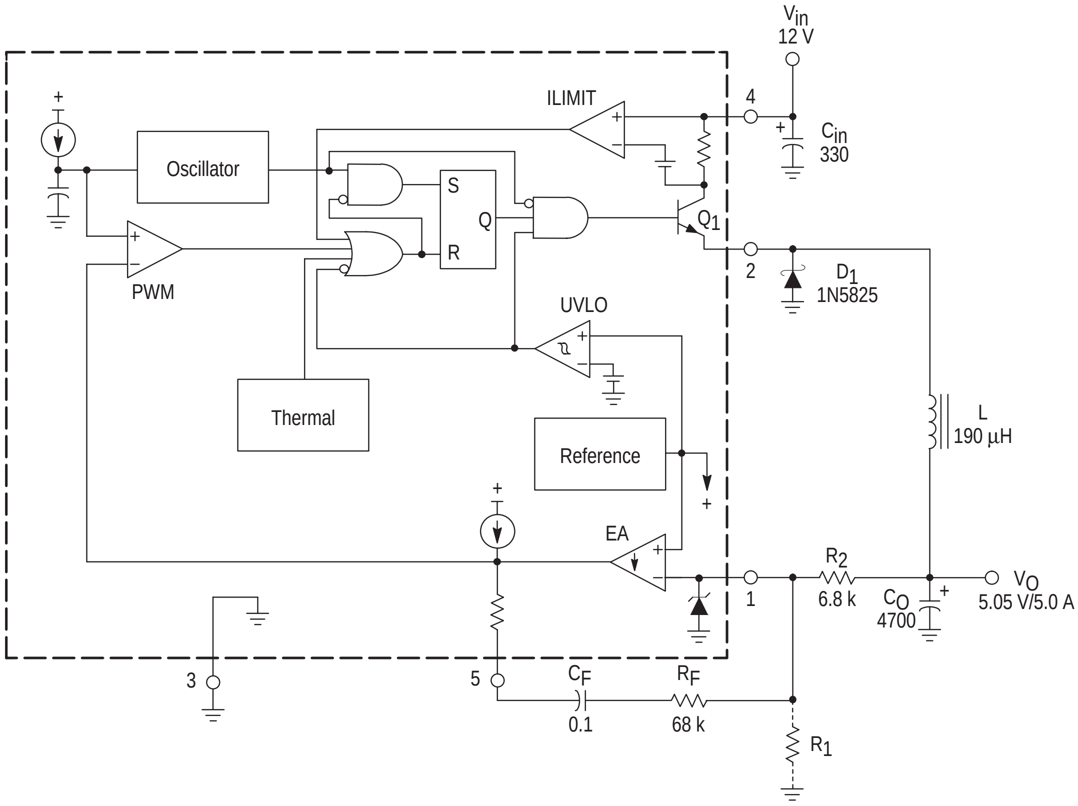
$V_{Shutdown} = V_{Zener} + 0.7$

Figure 17. Soft–Start Circuit



$t_{Soft–Start} \approx 35{,}000\ C_{SS}$

Figure 18. Step–Down Converter

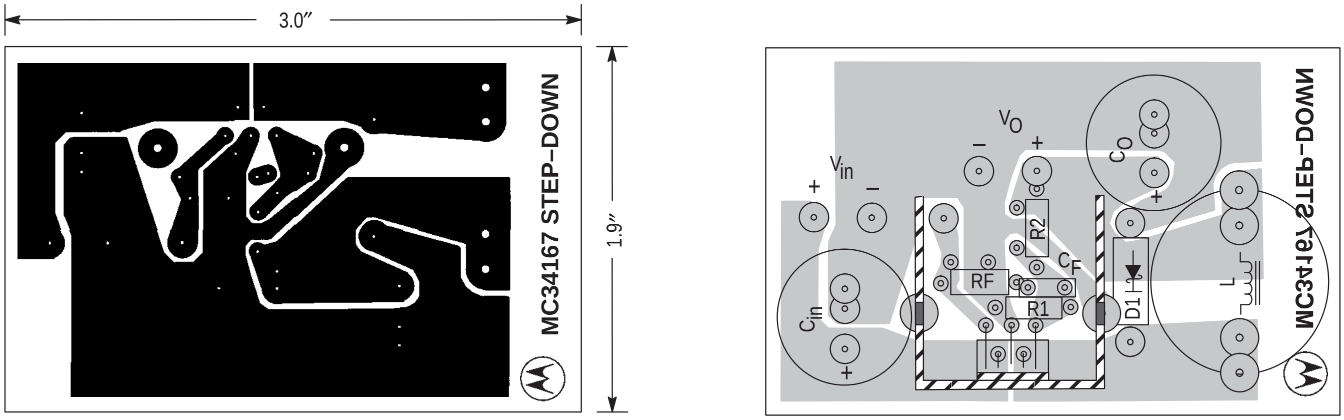


Test	Conditions	Results
Line Regulation	V_{in} = 10 V to 36 V, I_O = 5.0 A	4.0 mV = ± 0.039%
Load Regulation	V_{in} = 12 V, I_O = 0.25 A to 5.0 A	1.0 mV = ± 0.01%
Output Ripple	V_{in} = 12 V, I_O = 5.0 A	20 mV_{pp}
Short Circuit Current	V_{in} = 12 V, R_L = 0.1 Ω	6.5 A
Efficiency	V_{in} = 12 V, I_O = 5.0 A V_{in} = 24 V, I_O = 5.0 A	78.9% 82.6%

L = Coilcraft M1496–A or General Magnetics Technology GMT–0223, 42 turns of #16 AWG on Magnetics Inc. 58350–A2 core. Heatsink = AAVID Engineering Inc. 5903B, or 5930B.

The Step–Down Converter application is shown in Figure 18. The output switch transistor Q_1 interrupts the input voltage, generating a squarewave at the LC_O filter input. The filter averages the squarewaves, producing a dc output voltage that can be set to any level between V_{in} and V_{ref} by controlling the percent conduction time of Q_1 to that of the total oscillator cycle time. If the converter design requires an output voltage greater than 5.05 V, resistor R_1 must be added to form a divider network at the feedback input.

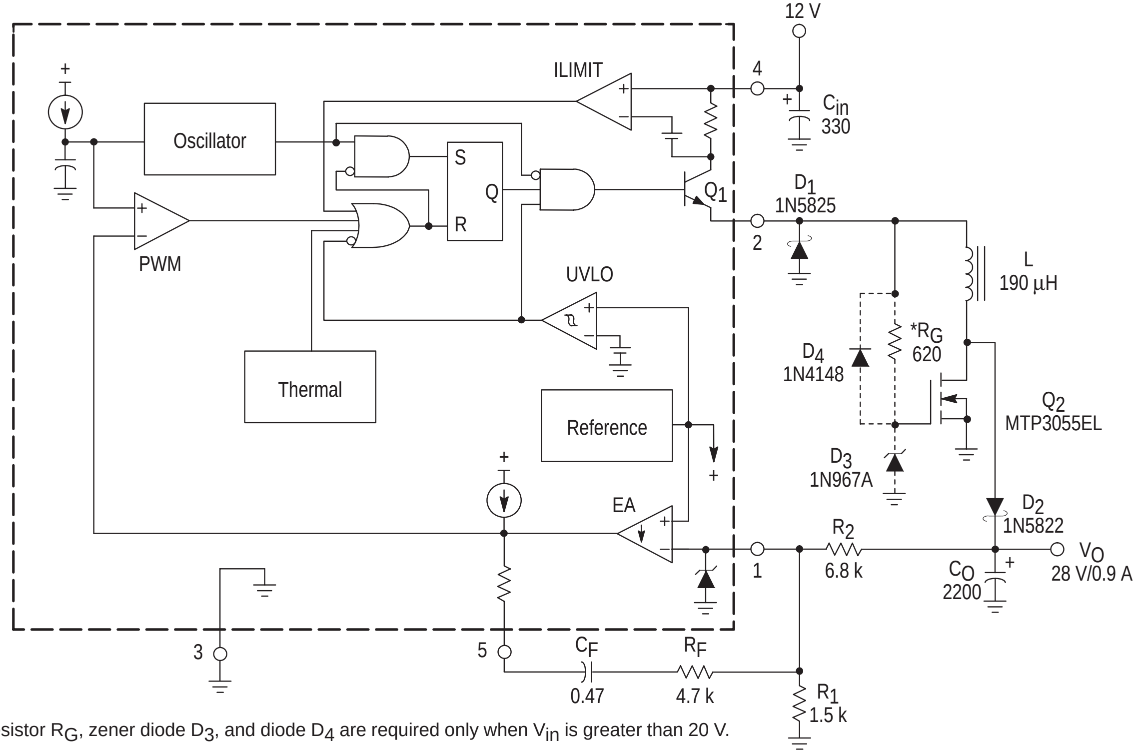
Figure 19. Step–Down Converter Printed Circuit Board and Component Layout



(Bottom View)

(Top View)

Figure 20. Step–Up/Down Converter



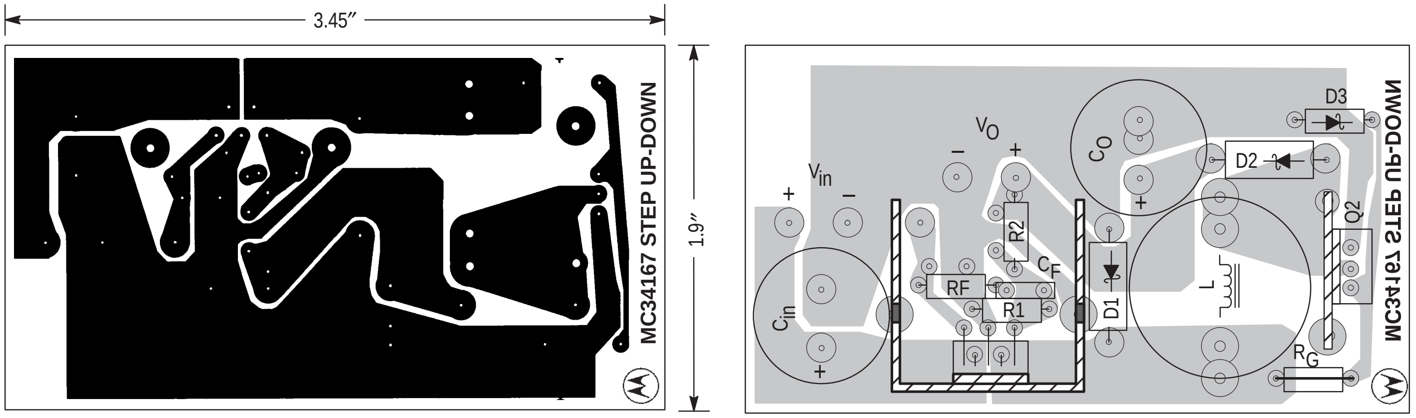
*Gate resistor R_G, zener diode D_3, and diode D_4 are required only when V_{in} is greater than 20 V.

Test	Conditions	Results
Line Regulation	V_{in} = 10 V to 24 V, I_O = 0.9 A	10 mV = ± 0.017%
Load Regulation	V_{in} = 12 V, I_O = 0.1 A to 0.9 A	30 mV = ± 0.053%
Output Ripple	V_{in} = 12 V, I_O = 0.9 A	140 mV_{pp}
Short Circuit Current	V_{in} = 12 V, R_L = 0.1 Ω	6.0 A
Efficiency	V_{in} = 12 V, I_O = 0.9 A V_{in} = 24 V, I_O = 0.9 A	80.1% 87.8%

L = Coilcraft M1496–A or General Magnetics Technology GMT–0223, 42 turns of #16 AWG on Magnetics Inc. 58350–A2 core.
Heatsink = AAVID Engineering Inc.
MC34167: 5903B, or 5930B
MTP3055EL: 5925B

Figure 20 shows that the MC34167 can be configured as a step–up/down converter with the addition of an external power MOSFET. Energy is stored in the inductor during the ON time of transistors Q_1 and Q_2. During the OFF time, the energy is transferred, with respect to ground, to the output filter capacitor and load. This circuit configuration has two significant advantages over the basic step–up converter circuit. The first advantage is that output short circuit protection is provided by the MC34167, since Q_1 is directly in series with V_{in} and the load. Second, the output voltage can be programmed to be less than V_{in}. Notice that during the OFF time, the inductor forward biases diodes D_1 and D_2, transferring its energy with respect to ground rather than with respect to V_{in}. When operating with V_{in} greater than 20 V, a gate protection network is required for the MOSFET. The network consists of components R_G, D_3, and D_4.

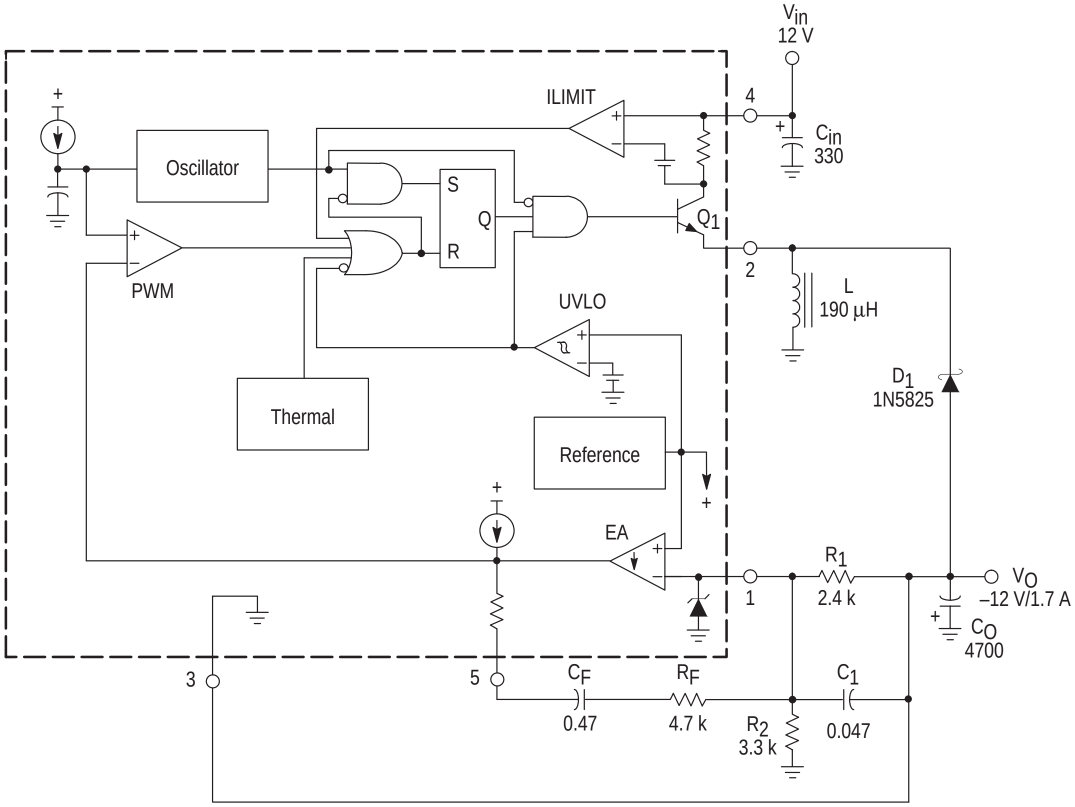
Figure 21. Step–Up/Down Converter Printed Circuit Board and Component Layout



(Bottom View)

(Top View)

Figure 22. Voltage–Inverting Converter

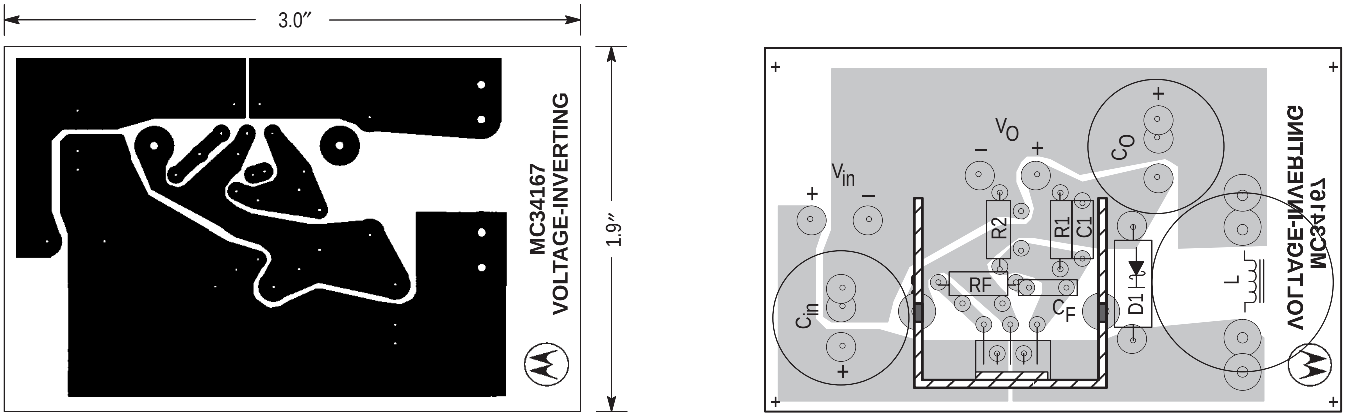


Test	Conditions	Results
Line Regulation	V_{in} = 10 V to 24 V, I_O = 1.7 A	15 mV = ± 0.61%
Load Regulation	V_{in} = 12 V, I_O = 0.1 A to 1.7 A	4.0 mV = ± 0.020%
Output Ripple	V_{in} = 12 V, I_O = 1.7 A	78 mV_{pp}
Short Circuit Current	V_{in} = 12 V, R_L = 0.1 Ω	5.7 A
Efficiency	V_{in} = 12 V, I_O = 1.7 A V_{in} = 24 V, I_O = 1.7 A	79.5% 86.2%

L = Coilcraft M1496–A or General Magnetics Technology GMT–0223, 42 turns of #16 AWG on Magnetics Inc. 58350–A2 core. Heatsink = AAVID Engineering Inc. 5903B, or 5930B.

Two potential problems arise when designing the standard voltage–inverting converter with the MC34167. First, the Switch Output emitter is limited to –1.5 V with respect to the ground pin and second, the Error Amplifier's noninverting input is internally committed to the reference and is not pinned out. Both of these problems are resolved by connecting the IC ground pin to the converter's negative output as shown in Figure 22. This keeps the emitter of Q_1 positive with respect to the ground pin and has the effect of reversing the Error Amplifier inputs. Note that the voltage drop across R_1 is equal to 5.05 V when the output is in regulation.

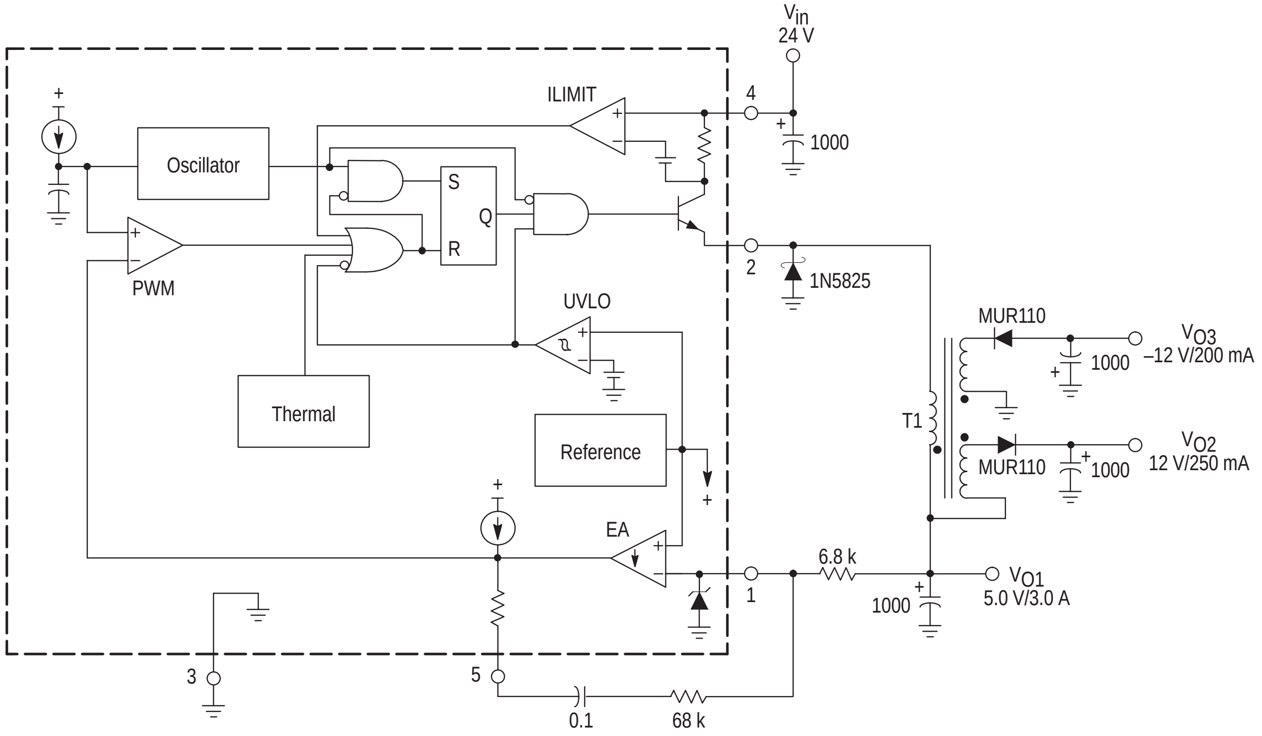
Figure 23. Voltage–Inverting Converter Printed Circuit Board and Component Layout



(Bottom View)

(Top View)

Figure 24. Triple Output Converter



Tests		Conditions	Results
Line Regulation	5.0 V 12 V –12 V	V_{in} = 15 V to 30 V, I_{O1} = 3.0 A, I_{O2} = 250 mA, I_{O3} = 200 mA	3.0 mV = ± 0.029% 572 mV = ± 2.4% 711 mV = ± 2.9%
Load Regulation	5.0 V 12 V –12 V	V_{in} = 24 V, I_{O1} = 30 mA to 3.0 A, I_{O2} = 250 mA, I_{O3} = 200 mA V_{in} = 24 V, I_{O1} = 3.0 A, I_{O2} = 100 mA to 250 mA, I_{O3} = 200 mA V_{in} = 24 V, I_{O1} = 3.0 A, I_{O2} = 250 mA, I_{O3} = 75 mA to 200 mA	1.0 mV = ± 0.009% 409 mV = ±1.5% 528 mV = ± 2.0%
Output Ripple	5.0 V 12 V –12 V	V_{in} = 24 V, I_{O1} = 3.0 A, I_{O2} = 250 mA, I_{O3} = 200 mA	75 mV_{pp} 20 mV_{pp} 20 mV_{pp}
Short Circuit Current	5.0 V 12 V –12 V	V_{in} = 24 V, R_L = 0.1 Ω	6.5 A 2.7 A 2.2 A
Efficiency	TOTAL	V_{in} = 24 V, I_{O1} = 3.0 A, I_{O2} = 250 mA, I_{O3} = 200 mA	84.2%

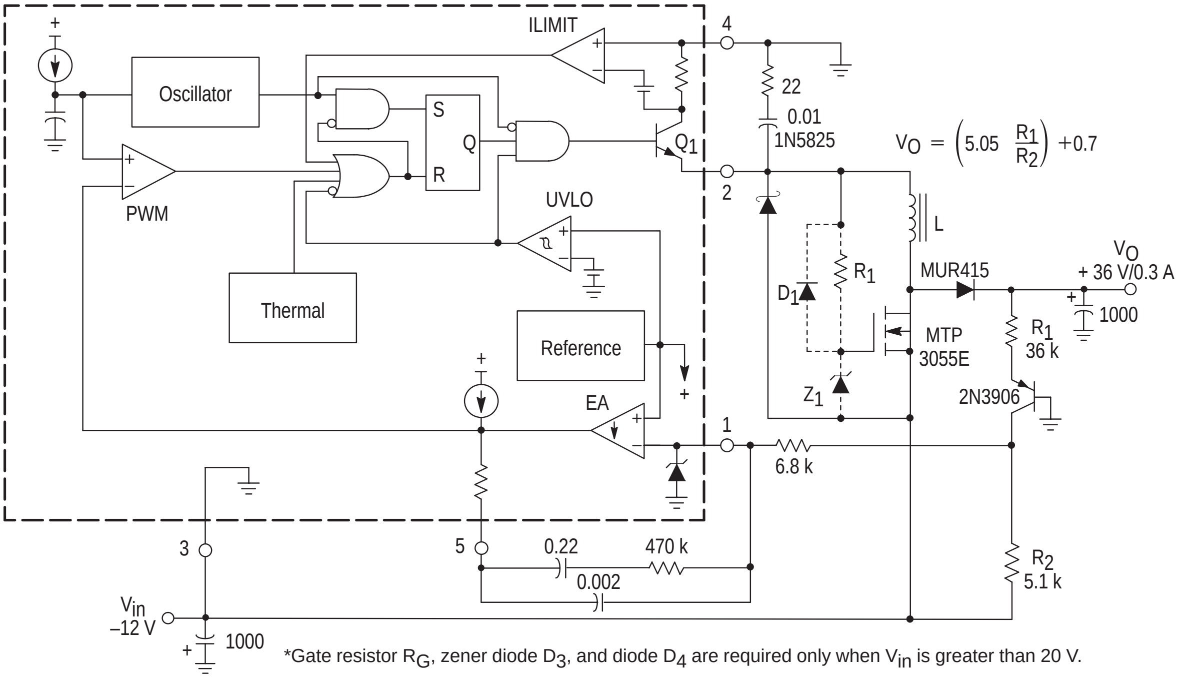
T1 = Primary: Coilcraft M1496–A or General Magnetics Technology GMT–0223, 42 turns of #16 AWG on Magnetics Inc. 58350–A2 core.
Secondary: V_{O2} – 69 turns of #26 AWG
V_{O3} – 104 turns of #28 AWG
Heatsink = AAVID Engineering Inc. 5903B, or 5930B.

Multiple auxiliary outputs can easily be derived by winding secondaries on the main output inductor to form a transformer. The secondaries must be connected so that the energy is delivered to the auxiliary outputs when the Switch Output turns off. During the OFF time, the voltage across the primary winding is regulated by the feedback loop, yielding a constant Volts/Turn ratio. The number of turns for any given secondary voltage can be calculated by the following equation:

$$\#\ \text{TURNS}_{(SEC)} = \frac{V_{O(SEC)} + V_{F(SEC)}}{\left(\dfrac{V_{O(PRI)} + V_{F(PRI)}}{\#\text{TURNS}_{(PRI)}}\right)}$$

Note that the 12 V winding is stacked on top of the 5.0 V output. This reduces the number of secondary turns and improves lead regulation. For best auxiliary regulation, the auxiliary outputs should be less than 33% of the total output power.

Figure 25. Negative Input/Positive Output Regulator

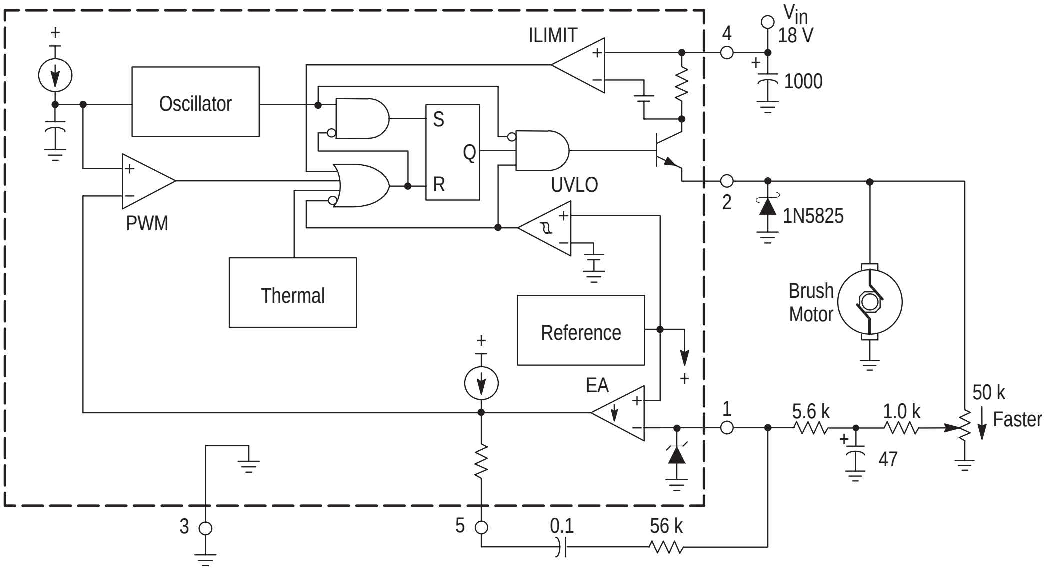


*Gate resistor R_G, zener diode D_3, and diode D_4 are required only when V_{in} is greater than 20 V.

Test	Conditions	Results
Line Regulation	V_{in} = –10 V to – 20 V, I_O = 0.3 A	266 mV = ± 0.38%
Load Regulation	V_{in} = –12 V, I_O = 0.03 A to 0.3 A	7.90 mV = ±1.1%
Output Ripple	V_{in} = –12 V, I_O = 0.3 A	100 mV_{pp}
Efficiency	V_{in} = –12 V, I_O = 0.3 A	78.4%

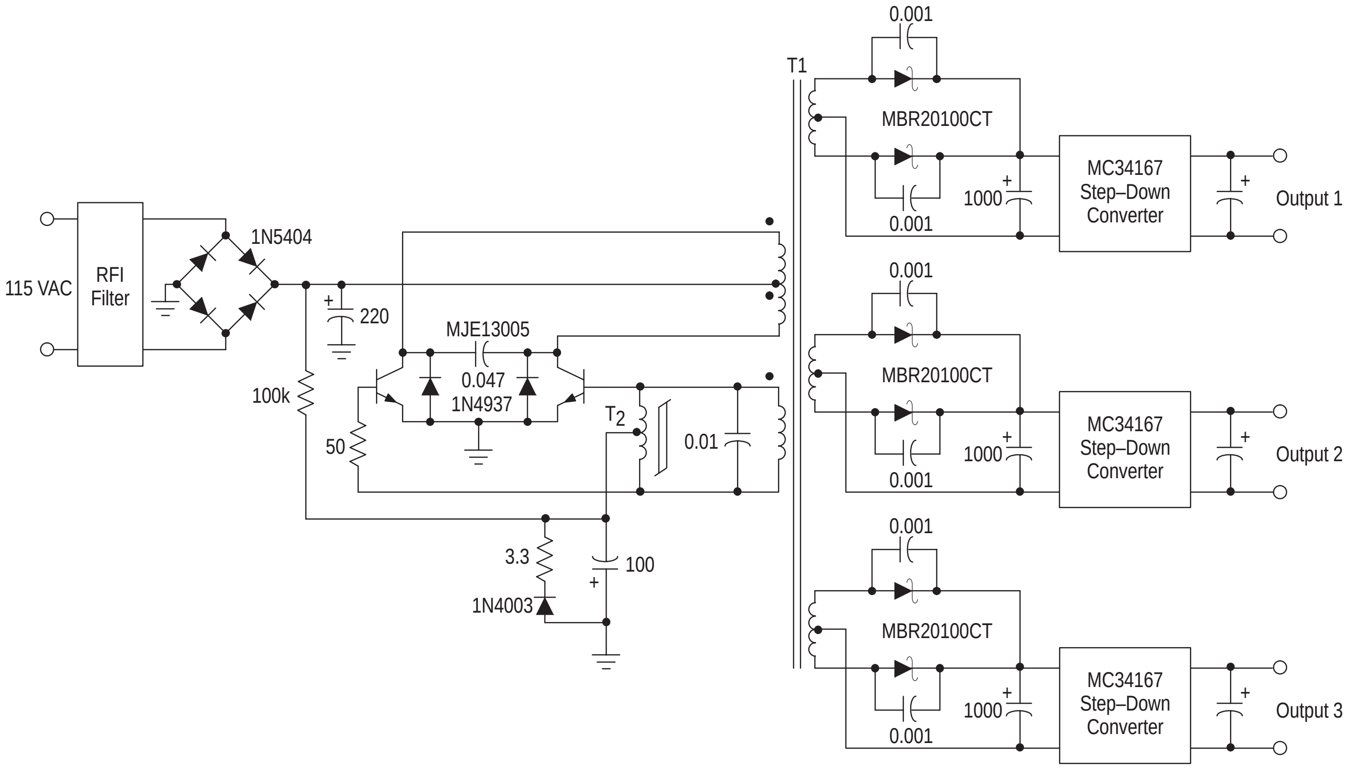
L = General Magnetics Technology GMT–0223, 42 turns of #16 AWG on Magnetics Inc. 58350–A2 core. Heatsink = AAVID Engineering Inc. 5903B or 5930B

Figure 26. Variable Motor Speed Control with EMF Feedback Sensing



Test	Conditions	Results
Low Speed Line Regulation	V_{in} = 12 V to 24 V	1760 RPM ±1%
High Speed Line Regulation	V_{in} = 12 V to 24 V	3260 RPM ± 6%

Figure 27. Off–Line Preconverter



T_1 = Core and Bobbin – Coilcraft PT3595
Primary – 104 turns #26 AWG
Base Drive – 3 turns #26 AWG
Secondaries – 16 turns #16 AWG
Total Gap – 0.002,

T_2 = Core – TDK T6 x 1.5 x 3 H5C2
14 turns center tapped #30 AWG
Heatsink = AAVID Engineering Inc.
MC34167 and MJE13005 – 5903B
MBR20100CT – 5925B

The MC34167 can be used cost effectively in off–line applications even though it is limited to a maximum input voltage of 40 V. Figure 27 shows a simple and efficient method for converting the AC line voltage down to 24 V. This preconverter has a total power rating of 125 W with a conversion efficiency of 90%. Transformer T_1 provides output isolation from the AC line and isolation between each of the secondaries. The circuit self–oscillates at 50 kHz and is controlled by the saturation characteristics of T_2. Multiple MC34167 post regulators can be used to provide accurate independently regulated outputs for a distributed power system.

Figure 28. D^2PAK Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length

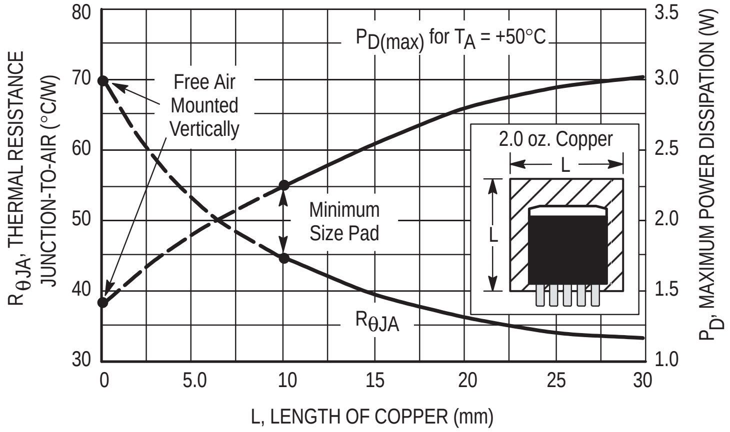


Table 1. Design Equations

Calculation	Step–Down	Step–Up/Down	Voltage–Inverting
$\frac{t_{on}}{t_{off}}$ (Notes 1, 2)	$\frac{V_{out} + V_F}{V_{in} - V_{sat} - V_{out}}$	$\frac{V_{out} + V_{F1} + V_{F2}}{V_{in} - V_{satQ1} - V_{satQ2}}$	$\frac{\lvert V_{out}\rvert + V_F}{V_{in} - V_{sat}}$
t_{on}	$\frac{\frac{t_{on}}{t_{off}}}{f_{osc}\left(\frac{t_{on}}{t_{off}} + 1\right)}$	$\frac{\frac{t_{on}}{t_{off}}}{f_{osc}\left(\frac{t_{on}}{t_{off}} + 1\right)}$	$\frac{\frac{t_{on}}{t_{off}}}{f_{osc}\left(\frac{t_{on}}{t_{off}} + 1\right)}$
Duty Cycle (Note 3)	$t_{on}\,f_{osc}$	$t_{on}\,f_{osc}$	$t_{on}\,f_{osc}$
$I_{L\ avg}$	I_{out}	$I_{out}\left(\frac{t_{on}}{t_{off}} + 1\right)$	$I_{out}\left(\frac{t_{on}}{t_{off}} + 1\right)$
$I_{pk(switch)}$	$I_{L\ avg} + \frac{\Delta I_L}{2}$	$I_{L\ avg} + \frac{\Delta I_L}{2}$	$I_{L\ avg} + \frac{\Delta I_L}{2}$
L	$\left(\frac{V_{in} - V_{sat} - V_{out}}{\Delta I_L}\right)t_{on}$	$\left(\frac{V_{in} - V_{satQ1} - V_{satQ2}}{\Delta I_L}\right)t_{on}$	$\left(\frac{V_{in} - V_{sat}}{\Delta I_L}\right)t_{on}$
$V_{ripple(pp)}$	$\Delta I_L \sqrt{\left(\frac{1}{8f_{osc}C_O}\right)^2 + (ESR)^2}$	$\left(\frac{t_{on}}{t_{off}} + 1\right)\sqrt{\left(\frac{1}{f_{osc}C_O}\right)^2 + (ESR)^2}$	$\left(\frac{t_{on}}{t_{off}} + 1\right)\sqrt{\left(\frac{1}{f_{osc}C_O}\right)^2 + (ESR)^2}$
V_{out}	$V_{ref}\left(\frac{R_2}{R_1} + 1\right)$	$V_{ref}\left(\frac{R_2}{R_1} + 1\right)$	$V_{ref}\left(\frac{R_2}{R_1} + 1\right)$

NOTES: 1. V_{sat} – Switch Output source saturation voltage, refer to Figure 7.
2. V_F – Output rectifier forward voltage drop. Typical value for 1N5822 Schottky barrier rectifier is 0.35 V.
3. Duty cycle is calculated at the minimum operating input voltage and must not exceed the guaranteed minimum $DC_{(max)}$ specification of 0.92.

The following converter characteristics must be chosen:

V_{out} – Desired output voltage.
I_{out} – Desired output current.
ΔI_L – Desired peak–to–peak inductor ripple current. For maximum output current especially when the duty cycle is greater than 0.5, it is suggested that ΔI_L be chosen minimum current limit threshold of 5.5 A. If the design goal is to use a minimum inductance value, let $\Delta I_L = 2\ (I_{L\ avg})$. This will proportionally reduce the converter’s output current capability.
$V_{ripple(pp)}$ – Desired peak–to–peak output ripple voltage. For best performance, the ripple voltage should be kept to less than 2% of V_{out}. Capacitor C_O should be a low equivalent series resistance (ESR) electrolytic designed for switching regulator applications.

MOTOROLA

MC34261
MC33261

Power Factor Controllers

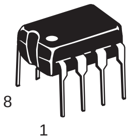
The MC34261/MC33261 are active power factor controllers specifically designed for use as a preconverter in electronic ballast and in off–line power converter applications. These integrated circuits feature an internal startup timer, a one quadrant multiplier for near unity power factor, zero current detector to ensure critical conduction operation, high gain error amplifier, trimmed internal bandgap reference, current sensing comparator, and a totem pole output ideally suited for driving a power MOSFET.

Also included are protective features consisting of input undervoltage lockout with hysteresis, cycle–by–cycle current limiting, and a latch for single pulse metering. These devices are available in dual–in–line and surface mount plastic packages.

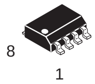
- Internal Startup Timer
- One Quadrant Multiplier
- Zero Current Detector
- Trimmed 2% Internal Bandgap Reference
- Totem Pole Output
- Undervoltage Lockout with Hysteresis
- Low Startup and Operating Current
- Pinout Equivalent to the SG3561
- Functional Equivalent to the TDA4817

POWER FACTOR CONTROLLERS

SEMICONDUCTOR TECHNICAL DATA

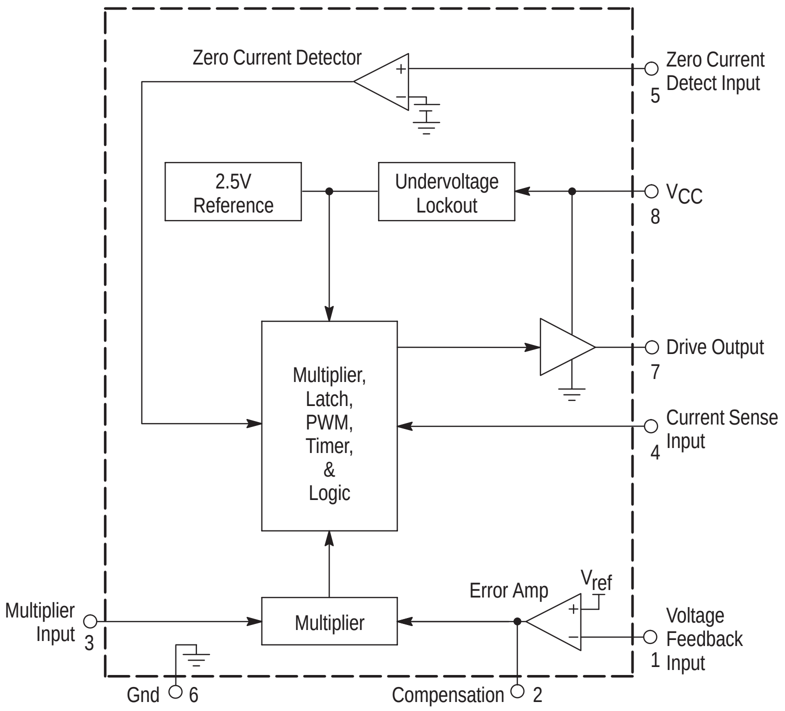


P SUFFIX
PLASTIC PACKAGE
CASE 626

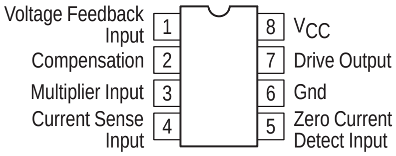


D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

Simplified Block Diagram



PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC34261D	T_A = 0° to +70°C	SO–8
MC34261P		Plastic DIP
MC33261D	T_A = –40° to +85°C	SO–8
MC33261P		Plastic DIP

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Total Power Supply and Zener Current	$(I_{CC} + I_Z)$	30	mA
Output Current, Source or Sink (Note 1)	I_O	500	mA
Current Sense, Multiplier, and Voltage Feedback Inputs	V_{in}	–1.0 to 10	V
Zero Current Detect Input	I_{in}		mA
High State Forward Current		50	
Low State Reverse Current		–10	
Power Dissipation and Thermal Characteristics			
P Suffix, Plastic Package Case 626			
Maximum Power Dissipation @ T_A = 70°C	P_D	800	mW
Thermal Resistance, Junction–to–Air	$R_{\theta JA}$	100	°C/W
D Suffix, Plastic Package Case 626			
Maximum Power Dissipation @ T_A = 70°C	P_D	450	mW
Thermal Resistance, Junction–to–Air	$R_{\theta JA}$	178	°C/W
Operating Junction Temperature	T_J	+150	°C
Operating Ambient Temperature (Note 3)	T_A		°C
MC34261		0 to +70	
MC33261		–40 to +85	
Storage Temperature	T_{stg}	–55 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 12 V, for typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies [Note 3], unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
ERROR AMPLIFIER					
Voltage Feedback Input Threshold	V_{FB}				V
T_A = 25°C		2.465	2.5	2.535	
$T_A = T_{low}$ to T_{high} (V_{CC} = 12 V to 28 V)		2.44		2.54	
Line Regulation (V_{CC} = 12 V to 28 V, T_A = 25°C)	Reg_{line}	–	1.0	10	mV
Input Bias Current (V_{FB} = 0 V)	I_{IB}	–	–0.3	–1.0	µA
Open Loop Voltage Gain	A_{VOL}	65	85	–	dB
Gain Bandwidth Product (T_A = 25°C)	GBW	0.7	1.0	–	MHz
Output Source Current (V_O = 4.0 V, V_{FB} = 2.3 V)	I_{Source}	0.25	0.5	0.75	mA
Output Voltage Swing					V
High State (I_{Source} = 0.2 mA, V_{FB} = 2.3 V)	V_{OH}	5.0	5.7	–	
Low State (I_{Sink} = 0.4 mA, V_{FB} = 2.7 V)	V_{OL}	–	2.1	2.44	
MULTIPLIER					
Dynamic Input Voltage Range					V
Multiplier Input (Pin 3)	$V_{Pin\ 3}$	0 to 2.5	0 to 3.5	–	
Compensation (Pin 2)	$V_{Pin\ 2}$	V_{FB} to (V_{FB} + 1.0)	V_{FB} to (V_{FB} + 1.5)	–	
Input Bias Current (V_{FB} = 0 V)	I_{IB}	–	–0.3	–1.0	µA
Multiplier Gain ($V_{Pin\ 3}$ = 0.5 V, $V_{Pin\ 2} = V_{FB}$ + 1.0 V) (Note 2)	K	0.4	0.62	0.8	1/V
ZERO CURRENT DETECTOR					
Input Threshold Voltage (V_{in} Increasing)	V_{th}	1.3	1.6	1.8	V
Hysteresis (V_{in} Decreasing)	V_H	40	110	200	mV
Input Clamp Voltage					V
High State (I_{DET} = 3.0 mA)	V_{IH}	6.1	6.7	–	
Low State (I_{DET} = –3.0 mA)	V_{IL}	0.3	0.7	1.0	

NOTES: 1. Maximum package power dissipation limits must be observed.

2. $K = \dfrac{\text{Pin 4 Threshold Voltage}}{V_{Pin\ 3}(V_{Pin\ 2} - V_{FB})}$

3. T_{low} = 0°C for MC34261 T_{high} = +70°C for MC34261
= –40°C for MC33261 = +85°C for MC33261

ELECTRICAL CHARACTERISTICS (V_{CC} = 12 V, for typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies [Note 3], unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
CURRENT SENSE COMPARATOR					
Input Bias Current ($V_{Pin\ 4}$ = 0 V)	I_{IB}	–	–0.5	–2.0	µA
Input Offset Voltage ($V_{Pin\ 2}$ = 1.1 V, $V_{Pin\ 3}$ = 0 V)	V_{IO}	–	3.5	15	mV
Delay to Output	$t_{PHL\ (in/out)}$	–	200	400	ns
DRIVE OUTPUT					
Output Voltage (V_{CC} = 12 V)					V
Low State (I_{Sink} = 20 mA)	V_{OL}	–	0.3	0.8	
(I_{Sink} = 200 mA)		1.8	2.4	3.3	
High State (I_{Source} = 20 mA)	V_{OH}	9.8	10.3	–	
(I_{Source} = 200 mA)		7.8	8.3	8.8	
Output Voltage (V_{CC} = 30 V) High State (I_{Source} = 20 mA, C_L = 15 pF)	$V_{O(max)}$	14	16	18	V
Output Voltage Rise Time (C_L = 1.0 nF)	t_r	–	50	120	ns
Output Voltage Fall Time (C_L = 1.0 nF)	t_f	–	50	120	ns
Output Voltage with UVLO Activated (V_{CC} = 7.0 V, I_{Sink} = 1.0 mA)	$V_{OH(UVLO)}$	–	0.2	0.8	V
RESTART TIMER					
Restart Time Delay	t_{DLY}	150	400	–	µs
UNDERVOLTAGE LOCKOUT					
Startup Threshold (V_{CC} Increasing)	V_{th}	9.2	10.0	10.8	V
Minimum Operating Voltage After Turn–On (V_{CC} Decreasing)	$V_{Shutdown}$	7.0	8.0	9.0	V
Hysteresis	V_H	1.75	2.0	2.5	V
TOTAL DEVICE					
Power Supply Current	I_{CC}				mA
Startup (V_{CC} = 7.0 V)		–	0.3	0.5	
Operating		–	7.1	12	
Dynamic Operating (50 kHz, C_L = 1.0 nF)		–	9.0	20	
Power Supply Zener Voltage	V_Z	30	36	–	V

NOTES: 1. Maximum package power dissipation limits must be observed.

2. $K = \dfrac{\text{Pin 4 Threshold Voltage}}{V_{Pin\ 3}(V_{Pin\ 2} - V_{FB})}$

3. T_{low} = 0°C for MC34261 T_{high} = +70°C for MC34261
= –40°C for MC33261 = +85°C for MC33261

Figure 1. Current Sense Input Threshold versus Multiplier Input

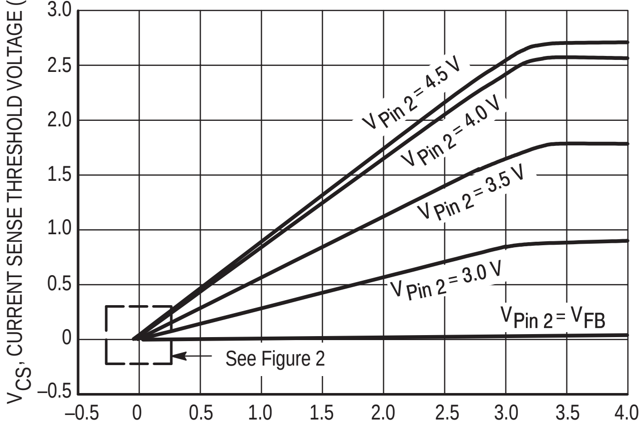


Figure 2. Current Sense Input Threshold versus Multiplier Input

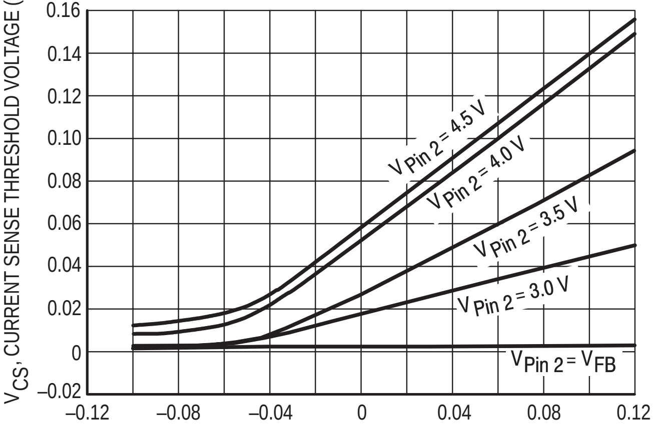


Figure 3. Voltage Feedback Input Threshold Change versus Temperature

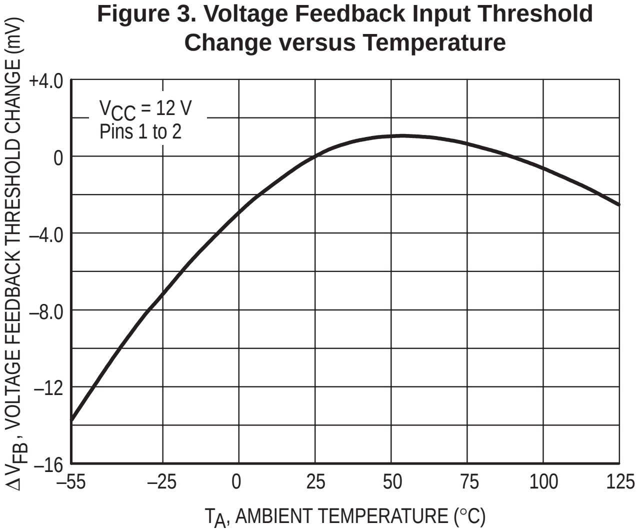


Figure 4. Error Amp Open Loop Gain and Phase versus Frequency

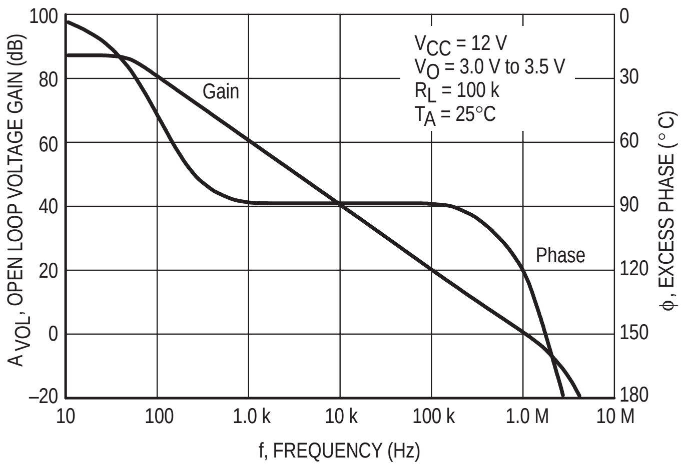


Figure 5. Error Amp Small Signal Transient Response

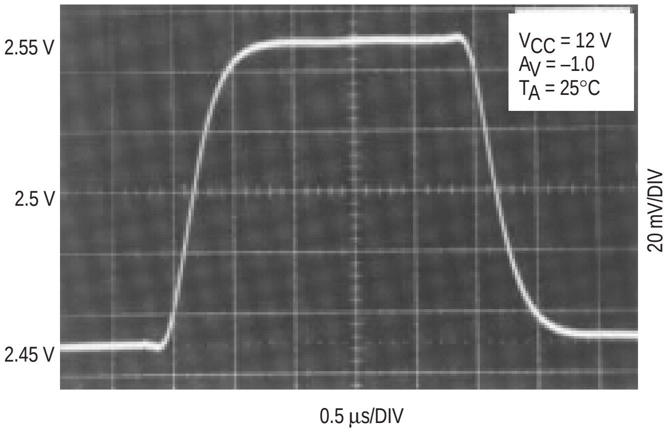


Figure 6. Error Amp Large Signal Transient Response

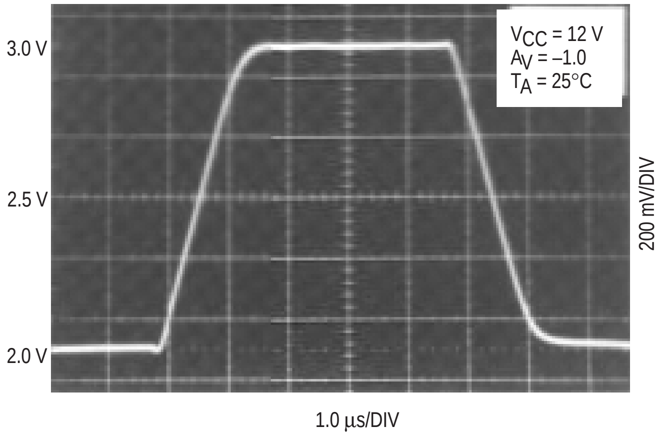


Figure 7. Error Amp Output Saturation versus Sink Current

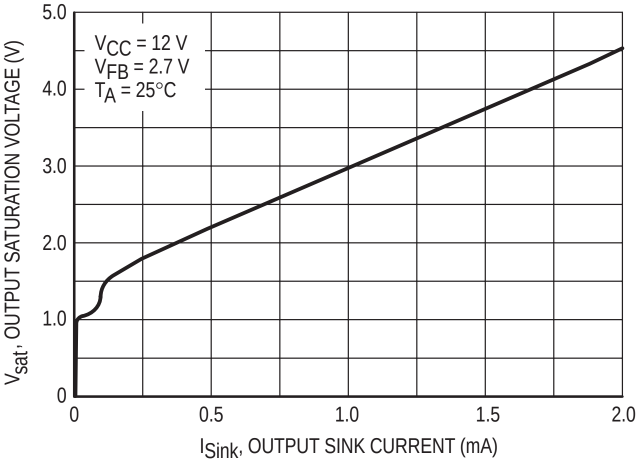


Figure 8. Restart Time Delay versus Temperature

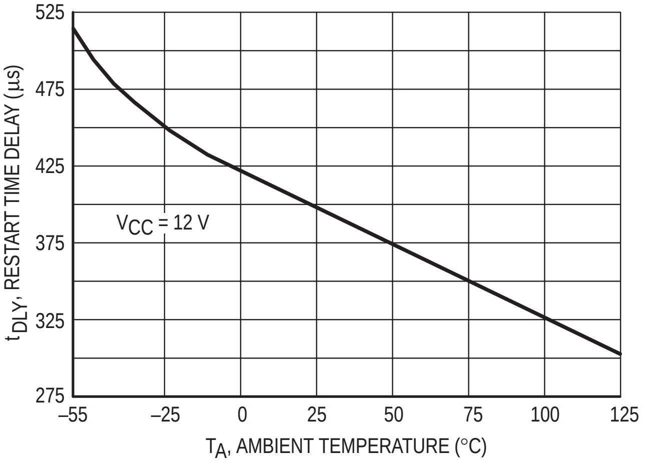


Figure 9. Zero Current Detector Input Threshold Voltage Change versus Temperature

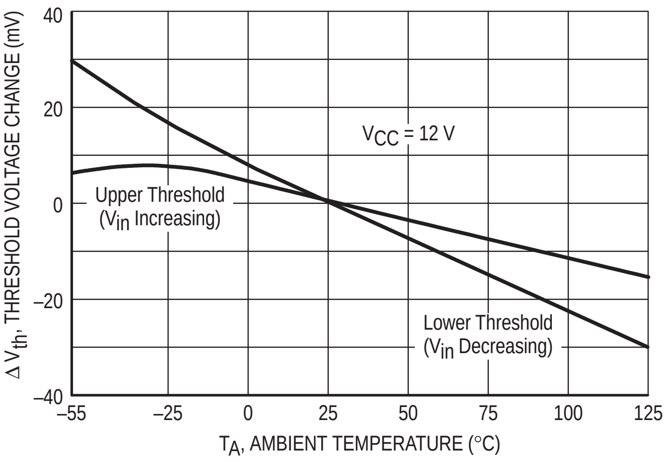


Figure 10. Output Saturation Voltage versus Load Current

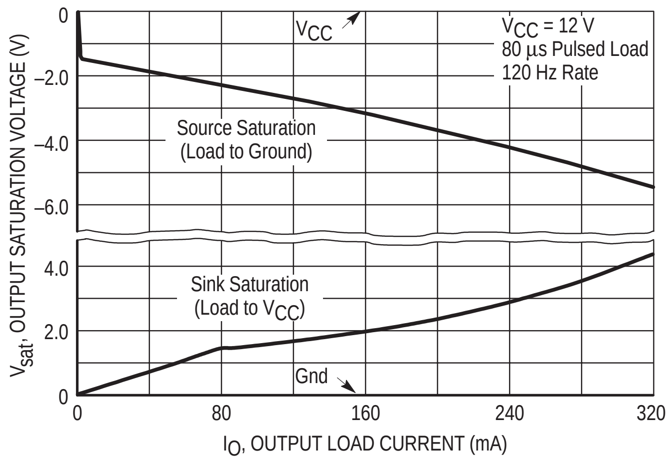


Figure 11. Drive Output Waveform

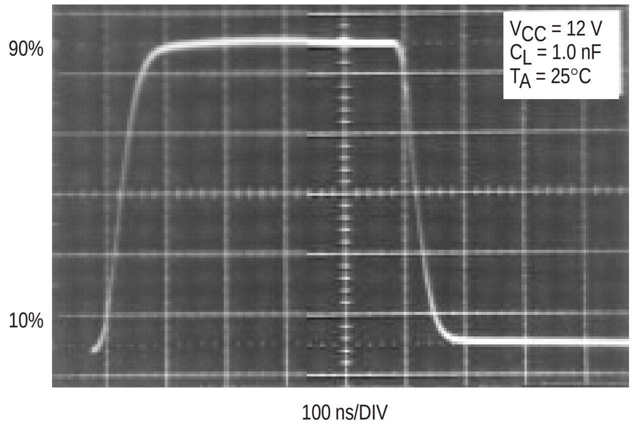


Figure 12. Drive Output Cross Conduction

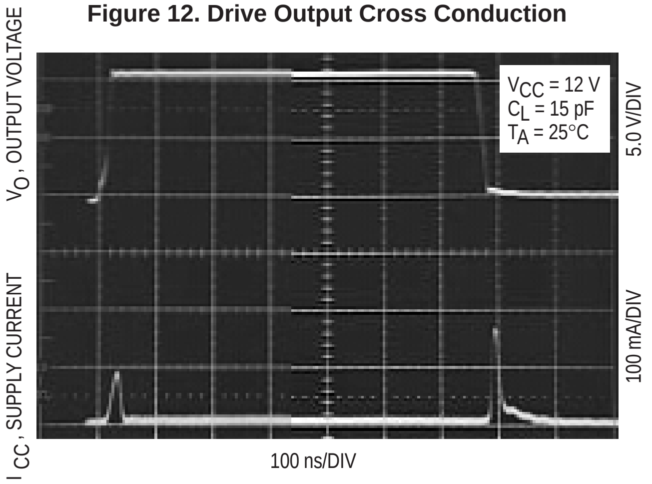


Figure 13. Supply Current versus Supply Voltage

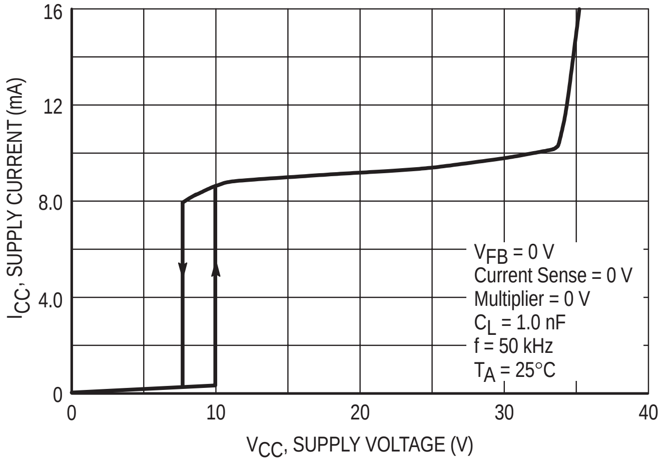
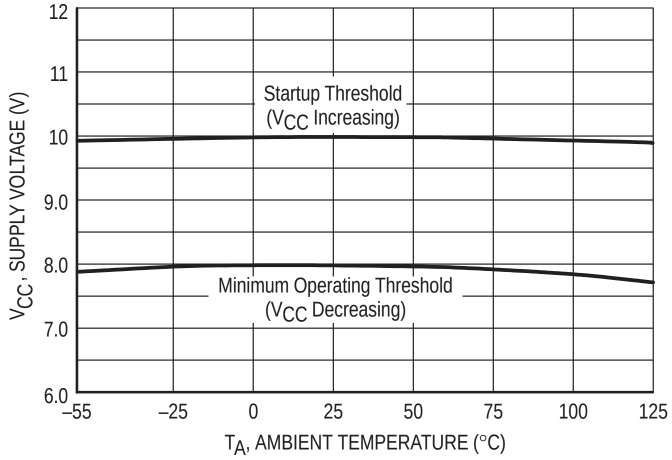


Figure 14. Undervoltage Lockout Thresholds versus Temperature



FUNCTIONAL DESCRIPTION

Introduction

Most electronic ballasts and switching power supplies use a bridge rectifier and a filter capacitor to derive raw dc voltage from the utility ac line. This simple rectifying circuit draws power from the line when the instantaneous ac voltage exceeds the capacitor's voltage. This occurs near the line voltage peak and results in a high charge current spike. Since power is only taken near the line voltage peaks, the resulting spikes of current are extremely nonsinusoidal with a high content of harmonics. This results in a poor power factor condition where the apparent input power is much higher than the real power.

The MC34261, MC33261 are high performance, critical conduction, current mode power factor controllers specifically designed for use in off–line active preconverters. These devices provide the necessary features required to significantly enhance poor power factor loads by keeping the ac line current sinusoidal and in phase with the line voltage. With proper control of the preconverter, almost any complex load can be made to appear resistive to the ac line, thus significantly reducing the harmonic current content.

Operating Description

The MC34261, MC33261 contains many of the building blocks and protection features that are employed in modern high performance current mode power supply controllers. There are, however, two areas where there is a major difference when compared to popular devices such as the UC3842 series. Referring to the block diagram in Figure 15, note that a multiplier has been added to the current sense loop and that this device does not contain an oscillator. A description of each of the functional blocks is given below.

Error Amplifier

A fully compensated Error Amplifier with access to the inverting input and output is provided. It features a typical dc voltage gain of 85 dB, and a unity gain bandwidth of 1.0 MHz with 58° of phase margin (Figure 4). The noninverting input is internally biased at 2.5 V ±2.0% and is not pinned out. The output voltage of the power factor converter is typically divided down and monitored by the inverting input. The maximum input bias current is –1.0 µA which can cause an output voltage error that is equal to the product of the input bias current and the value of the upper divider resistor R_2. The Error Amp Output is internally connected to the Multiplier and is pinned out (Pin 2) for external loop compensation. Typically, the bandwidth is set below 20 Hz, so that the Error Amp output voltage is relatively constant over a given ac line cycle. The output stage consists of a 500 µA current source pull–up with a Darlington transistor pull–down. It is capable of swinging from 2.1 V to 5.7 V, assuring that the Multiplier can be driven over its entire dynamic range.

Multiplier

A single quadrant, two input multiplier is the critical element that enables this device to control power factor. The ac haversines are monitored at Pin 3 with respect to ground while the Error Amp output at Pin 2 is monitored with respect to the Voltage Feedback Input threshold. A graph of the Multiplier transfer curve is shown in Figure 1. Note that both inputs are extremely linear over a wide dynamic range, 0 V to 3.2 V for the Multiplier input (Pin 3), and 2.5 V to 4.0 V for the Error Amp output (Pin 2). The Multiplier output controls the Current Sense Comparator threshold (Pin 4) as the ac voltage traverses sinusoidally from zero to peak line. This has the effect of forcing the MOSFET peak current to track the input line voltage, thus making the preconverter load appear to be resistive.

$$\text{Pin 4 Threshold} \approx 0.62(V_{\text{Pin 2}} - V_{FB})V_{\text{Pin 3}}$$

Zero Current Detector

The MC34261 operates as a critical conduction current mode controller, whereby output switch conduction is initiated by the Zero Current Detector and terminated when the peak inductor current reaches the threshold level established by the Multiplier output. The Zero Current Detector initiates the next on–time by setting the RS Latch at the instant the inductor current reaches zero. This critical conduction mode of operation has two significant benefits. First, since the MOSFET cannot turn on until the inductor current reaches zero, the output rectifier's reverse recovery time becomes less critical allowing the use of an inexpensive rectifier. Second, since there are no deadtime gaps between cycles, the ac line current is continuous thus limiting the peak switch to twice the average input current.

The Zero Current Detector indirectly senses the inductor current by monitoring when the auxiliary winding voltage falls below 1.6 V. To prevent false tripping, 110 mV of hysteresis is provided. The Zero Current Detector input is internally protected by two clamps. The upper 6.7 V clamp prevents input overvoltage breakdown while the lower 0.7 V clamp prevents substrate injection. Device destruction can result if this input is shorted to ground. An external resistor must be used in series with the auxiliary winding to limit the current through the clamps.

Current Sense Comparator and RS Latch

The Current Sense Comparator RS Latch configuration ensures that only a single pulse appears at the Drive Output during a given cycle. The inductor current is converted to a voltage by inserting a ground referenced sense resistor R_9 in series with the source of output switch Q1. This voltage is monitored by the Current Sense Input and compared to the Multiplier output voltage. The peak inductor current is controlled by the threshold voltage of Pin 4 where:

$$I_{pk} = \frac{\text{Pin 4 Threshold}}{R_9}$$

With the component values shown in Figure 16, the Current Sense Comparator threshold, at the peak of the haversine varies from 1.1 V at 90 Vac to 100 mV at 268 Vac. The Current Sense Input to Drive Output propagation delay is typically 200 ns.

Timer

A watchdog timer function was added to the IC to eliminate the need for an external oscillator when used in stand alone applications. The Timer provides a means to automatically start or restart the preconverter if the Drive Output has been off for more than 400 µs after the inductor current reaches zero.

Undervoltage Lockout

An Undervoltage Lockout comparator guarantees that the IC is fully functional before enabling the output stage. The positive power supply terminal (V_{CC}) is monitored by the UVLO comparator with the upper threshold set at 10 V and the lower threshold at 8.0 V (Figure 14). In the standby mode, with V_{CC} at 7.0 V, the required supply current is less than 0.5 mA (Figure 13). This hysteresis and low startup current allow the implementation of efficient bootstrap startup techniques, making these devices ideally suited for wide input range off line preconverter applications. An internal 36 V clamp has been added from V_{CC} to ground to protect the IC and capacitor C_5 from an overvoltage condition. This feature is desirable if external circuitry is used to delay the startup of the preconverter.

Output

The MC34261/MC33261 contain a single totem pole output stage specifically designed for direct drive of power MOSFETs. The Drive Output is capable of up to ±500 mA peak current with a typical rise and fall time of 50 ns with a 1.0 nF load. Additional internal circuitry has been added to keep the Drive Output in a sinking mode whenever the Undervoltage Lockout is active. This characteristic eliminates the need for an external gate pull–down resistor. The totem pole output has been optimized to minimize cross conduction current during high speed operation. The addition of two 10 Ω resistors, one in series with the source output transistor and one in series with the sink output transistor, reduces the cross conduction current, as shown in Figure 12. A 16 V clamp has been incorporated into the output stage to limit the high state V_{OH}. This prevents rupture of the MOSFET gate when V_{CC} exceeds 20 V.

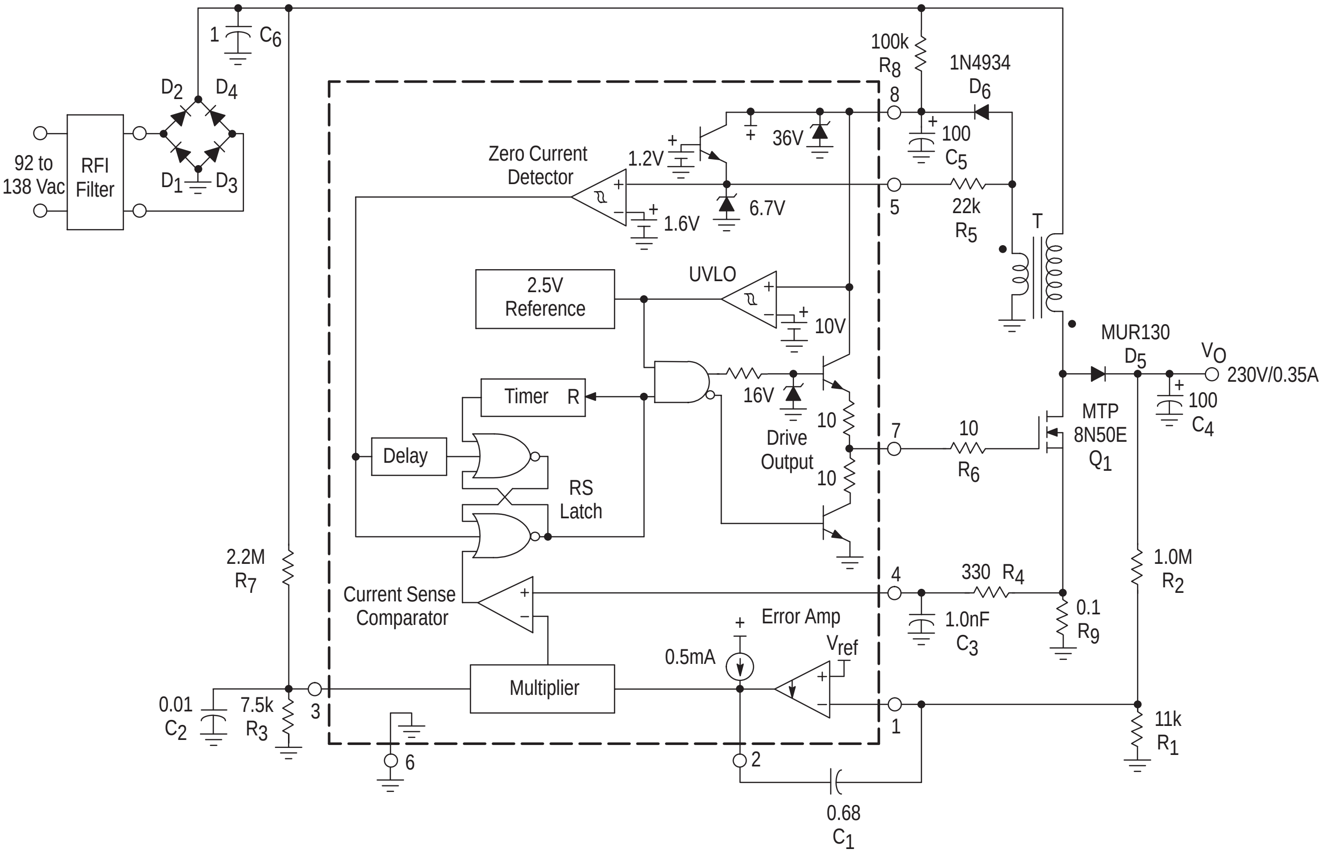
Table 1. Design Equations

Notes	Calculation	Formula
Calculate the maximum required output power.	Required Converter Output Power	$P_O = V_O I_O$
Calculated at the minimum required ac line for regulation. Let the efficiency n = 0.95.	Peak Inductor Current	$I_{L(pk)} = \frac{2\sqrt{2}\,P_O}{\eta Vac_{(LL)}}$
Let the switching cycle t = 20 µs.	Inductance	$L = \frac{2t\left(\frac{V_O}{\sqrt{2}} - Vac\right)Vac^2}{V_O\,Vac_{(LL)}\,I_{L(pk)}}$
In theory the on–time t_{on} is constant. In practice t_{on} tends to increase at the ac line zero crossings due to the charge on capacitor C_6.	Switch On–Time	$t_{on} = \frac{2\,P_O\,L}{\eta\,Vac^2}$
The off–time t_{off} is greatest at peak ac line and approaches zero at the ac line zero crossings. Theta (θ) represents the angle of the ac line voltage.	Switch Off–Time	$t_{off} = \frac{t_{on}}{\frac{V_O}{\sqrt{2}\,Vac\,\lvert\sin\theta\rvert} - 1}$
The minimum switching frequency occurs at peak ac line and increases as t_{off} decreases.	Switching Frequency	$f = \frac{1}{t_{on} + t_{off}}$
Set the current sense threshold V_{CS} to 1.0 V for universal input (85 Vac to 265 Vac) operation and to 0.5 V for fixed input (92 Vac to 138 Vac, or 184 to 276 Vac) operation.	Peak Switch Current	$R_9 = \frac{V_{CS}}{I_{L(pk)}}$
Set the multiplier input voltage V_M to 3.0 V at high line. Empirically adjust V_M for the lowest distortion over the ac line range while guaranteeing startup at minimum line.	Multiplier Input Voltage	$V_M = \frac{Vac\,\sqrt{2}}{\left(\frac{R_7}{R_3} + 1\right)}$
The I_{IB} R_1 error term can be minimized with a divider current in excess of 100 µA.	Converter Output Voltage	$V_O = V_{ref}\left(\frac{R_2}{R_1} + 1\right) - I_{IB}\,R_2$
The bandwidth is typically set to 20 Hz for minimum output ripple over the ac line haversine.	Error Amplifier Bandwidth	$BW = \frac{1}{2\pi\,\frac{R_1 R_2}{R_1 + R_2}\,C_1}$

The following converter characteristics must be chosen:

V_O – Desired output voltage	Vac – AC RMS line voltage
I_O – Desired output current	$Vac_{(LL)}$ – AC RMS low line voltage

Figure 15. 80 W Power Factor Controller



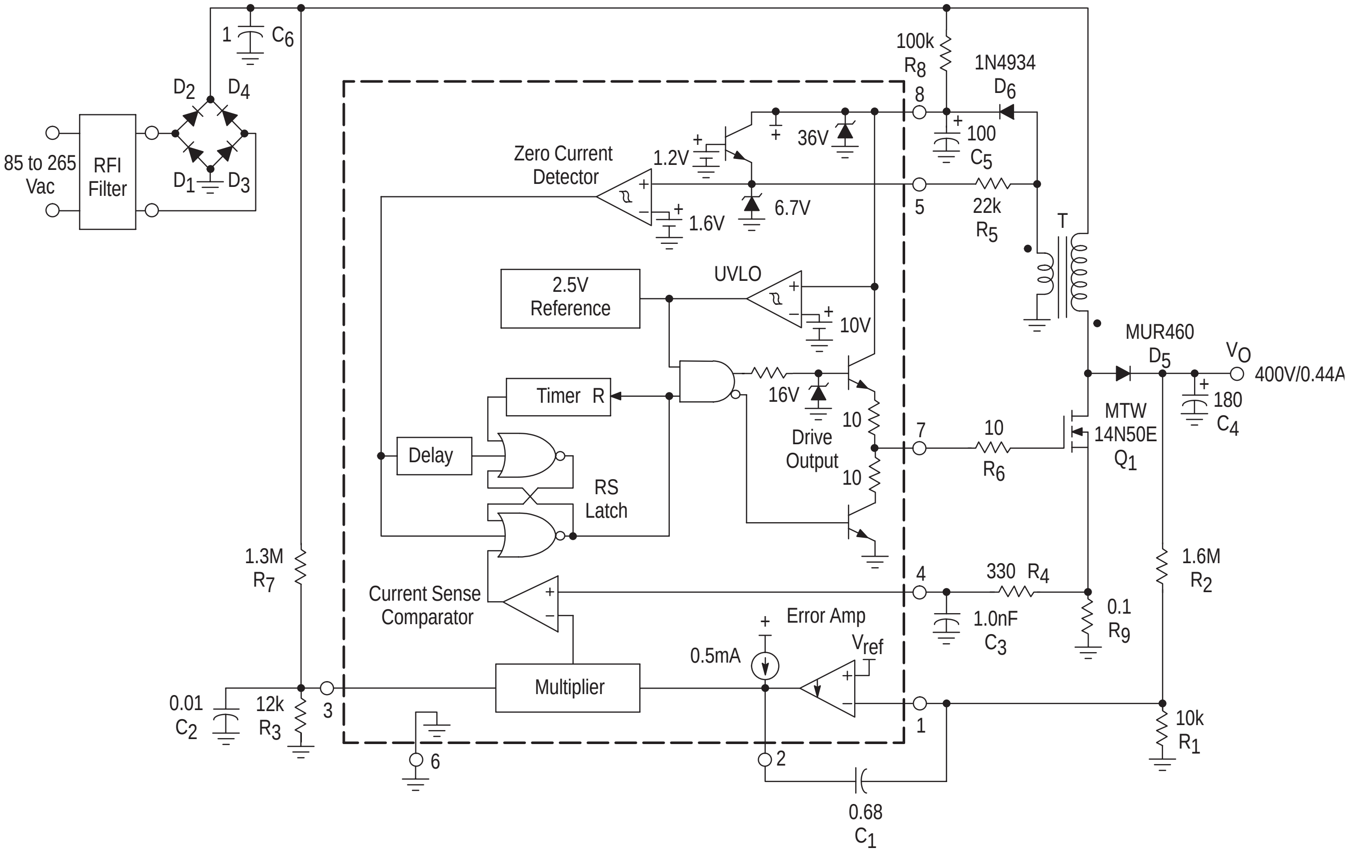
Power Factor Controller Test Data

AC Line Input								DC Output				
			Current Harmonic Distortion (%)									
V_{rms}	P_{in}	PF	THD	2	3	5	7	$V_{O(pp)}$	V_O	I_O	P_O	n(%)
90	85.6	–0.998	2.4	0.11	0.52	1.3	0.67	10.0	230	0.350	80.5	94.0
100	85.1	–0.997	5.0	0.13	1.7	2.4	1.4	10.1	230	0.350	80.5	94.6
110	84.8	–0.997	5.3	0.12	2.5	2.6	1.5	10.2	230	0.350	80.5	94.9
120	84.5	–0.997	5.8	0.12	3.2	2.7	1.4	10.2	230	0.350	80.5	95.3
130	84.2	–0.996	6.6	0.12	4.0	2.8	1.5	10.2	230	0.350	80.5	95.6
138	84.1	–0.995	7.2	0.13	4.5	3.0	1.6	10.2	230	0.350	80.5	95.7

This data was taken with the test set–up shown in Figure 17.

T = Coilcraft N2881–A
Primary: 62 turns of # 22 AWG
Secondary: 5 turns of # 22 AWG
Core: Coilcraft PT2510, EE 25
Gap: 0.072″ total for a primary inductance of 320 µH
Heatsink = AAVID Engineering Inc. 5903B, or 5930B

Figure 16. 175 W Universal Input Power Factor Controller



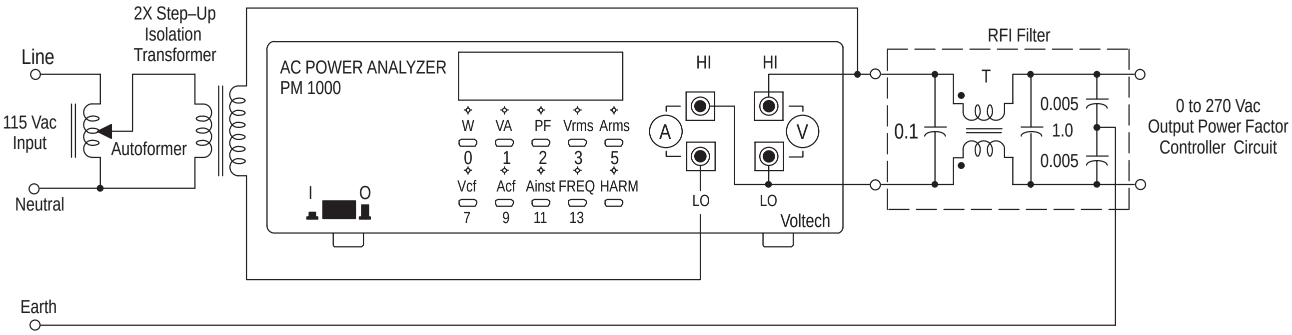
Power Factor Controller Test Data

AC Line Input								DC Output				
			Current Harmonic Distortion (%)									
V_{rms}	P_{in}	PF	THD	2	3	5	7	$V_{O(pp)}$	V_O	I_O	P_O	n(%)
90	187.5	–0.998	2.0	0.10	0.98	0.90	0.78	8.0	400.7	0.436	174.7	93.2
120	184.6	–0.997	1.8	0.09	1.3	1.3	0.93	8.0	400.7	0.436	174.7	94.6
138	183.6	–0.997	2.3	0.05	1.6	1.5	1.0	8.0	400.7	0.436	174.7	95.2
180	181.0	–0.995	4.3	0.16	2.5	2.0	1.2	8.0	400.6	0.436	174.7	95.6
240	179.3	–0.993	6.0	0.08	3.7	2.7	1.4	8.0	400.6	0.436	174.7	97.4
268	178.6	–0.992	6.7	0.16	2.8	3.7	1.7	8.0	400.6	0.436	174.7	97.8

This data was taken with the test set–up shown in Figure 17.

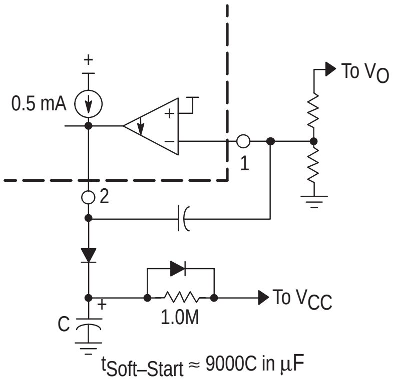
T = Coilcraft N2880–A
Primary: 78 turns of # 16 AWG
Secondary: 6 turns of # 18 AWG
Core: Coilcraft PT4215, EE 42–15
Gap: 0.104″ total for a primary inductance of 870 µH
Heatsink = AAVID Engineering Inc. 5903B

Figure 17. Power Factor Test Set–Up



An RFI filter is required for best performance when connecting the preconverter directly to the AC line. Commercially available two stage filters such as the Delta Electronics 03DPCG5 work excellent. The simple single stage test filter shown above can easily be constructed with a common mode transformer. Transformer (T) is a Coilcraft CMT3–28–2 with 28 mH minimum inductance and a 2.0 A maximum current rating.

Figure 18. Soft–Start Circuit



Startup overshoot can be eliminated with the addition of a Soft–Start circuit.

Figure 19. Error Amp Compensation

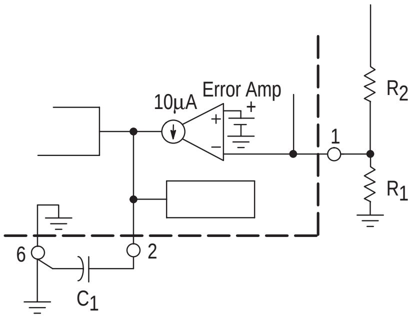
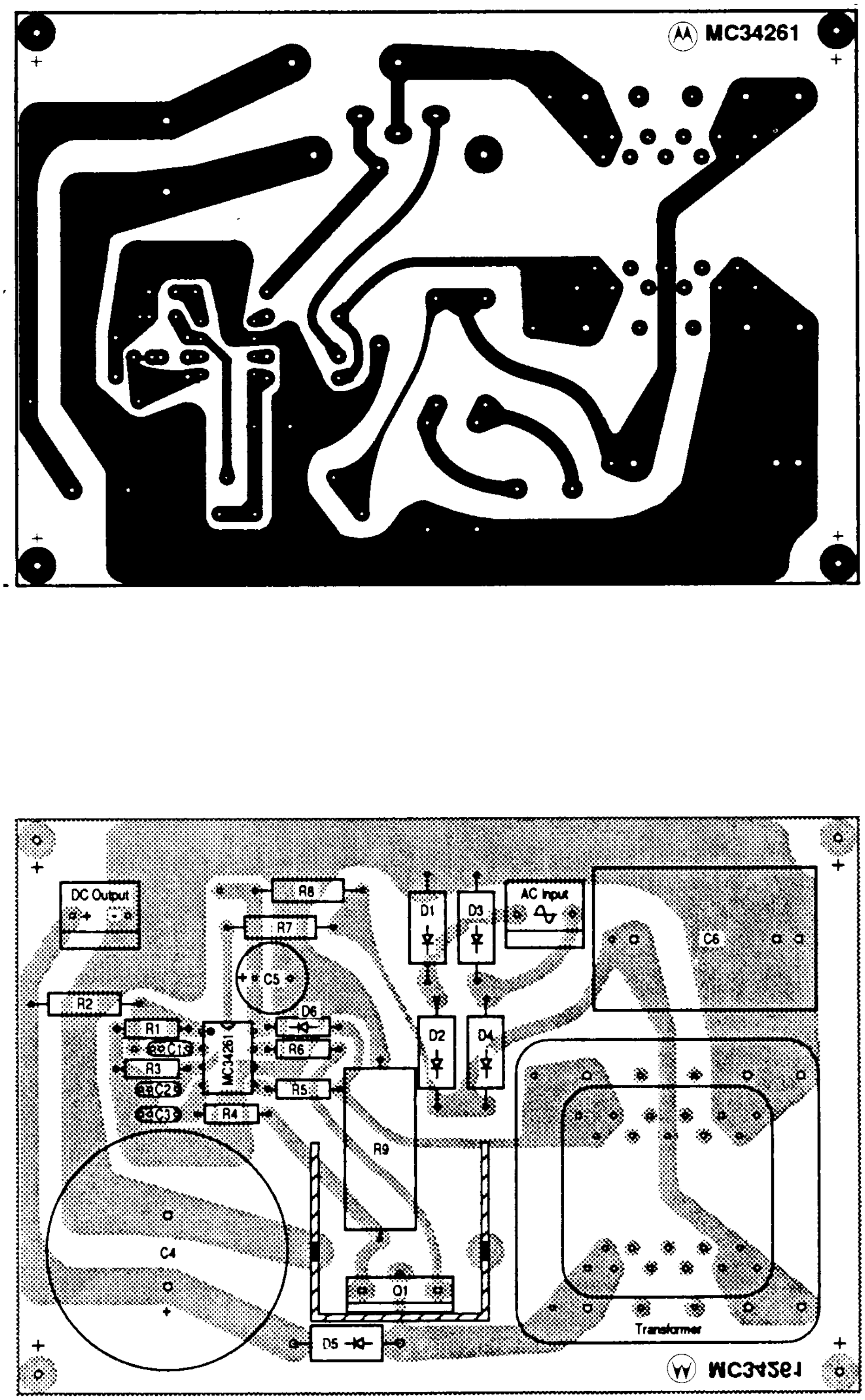


Figure 20. Printed Circuit Board and Component Layout
(Circuits of Figures 15 and 16)



MOTOROLA

MC34262
MC33262

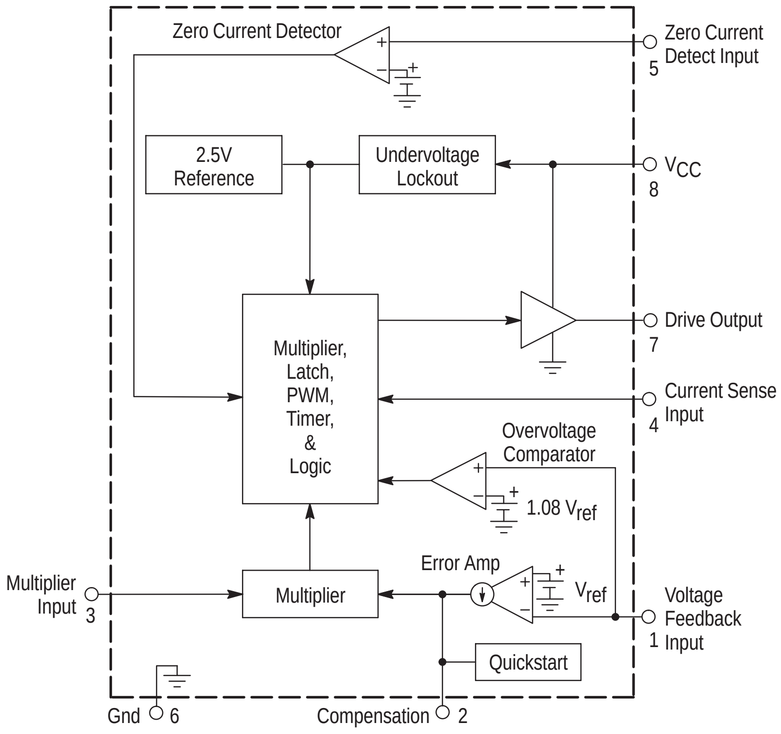
Power Factor Controllers

The MC34262/MC33262 are active power factor controllers specifically designed for use as a preconverter in electronic ballast and in off–line power converter applications. These integrated circuits feature an internal startup timer for stand–alone applications, a one quadrant multiplier for near unity power factor, zero current detector to ensure critical conduction operation, transconductance error amplifier, quickstart circuit for enhanced startup, trimmed internal bandgap reference, current sensing comparator, and a totem pole output ideally suited for driving a power MOSFET.

Also included are protective features consisting of an overvoltage comparator to eliminate runaway output voltage due to load removal, input undervoltage lockout with hysteresis, cycle–by–cycle current limiting, multiplier output clamp that limits maximum peak switch current, an RS latch for single pulse metering, and a drive output high state clamp for MOSFET gate protection. These devices are available in dual–in–line and surface mount plastic packages.

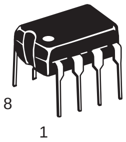
- Overvoltage Comparator Eliminates Runaway Output Voltage
- Internal Startup Timer
- One Quadrant Multiplier
- Zero Current Detector
- Trimmed 2% Internal Bandgap Reference
- Totem Pole Output with High State Clamp
- Undervoltage Lockout with 6.0 V of Hysteresis
- Low Startup and Operating Current
- Supersedes Functionality of SG3561 and TDA4817

Simplified Block Diagram

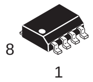


POWER FACTOR CONTROLLERS

SEMICONDUCTOR TECHNICAL DATA

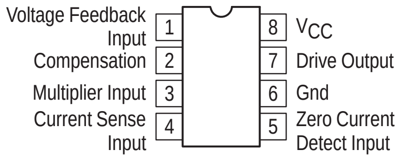


P SUFFIX
PLASTIC PACKAGE
CASE 626



D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC34262D	T_A = 0° to +85°C	SO–8
MC34262P		Plastic DIP
MC33262D	T_A = –40° to +105°C	SO–8
MC33262P		Plastic DIP

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Total Power Supply and Zener Current	$(I_{CC} + I_Z)$	30	mA
Output Current, Source or Sink (Note 1)	I_O	500	mA
Current Sense, Multiplier, and Voltage Feedback Inputs	V_{in}	–1.0 to +10	V
Zero Current Detect Input	I_{in}		mA
High State Forward Current		50	
Low State Reverse Current		–10	
Power Dissipation and Thermal Characteristics			
P Suffix, Plastic Package, Case 626			
Maximum Power Dissipation @ T_A = 70°C	P_D	800	mW
Thermal Resistance, Junction–to–Air	$R_{\theta JA}$	100	°C/W
D Suffix, Plastic Package, Case 751			
Maximum Power Dissipation @ T_A = 70°C	P_D	450	mW
Thermal Resistance, Junction–to–Air	$R_{\theta JA}$	178	°C/W
Operating Junction Temperature	T_J	+150	°C
Operating Ambient Temperature (Note 3)	T_A		°C
MC34262		0 to + 85	
MC33262		– 40 to +105	
Storage Temperature	T_{stg}	– 65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 12 V (Note 2), for typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies [Note 3], unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
ERROR AMPLIFIER					
Voltage Feedback Input Threshold	V_{FB}				V
T_A = 25°C		2.465	2.5	2.535	
$T_A = T_{low}$ to T_{high} (V_{CC} = 12 V to 28 V)		2.44	—	2.54	
Line Regulation (V_{CC} = 12 V to 28 V, T_A = 25°C)	Reg_{line}	—	1.0	10	mV
Input Bias Current (V_{FB} = 0 V)	I_{IB}	—	– 0.1	– 0.5	µA
Transconductance (T_A = 25°C)	g_m	80	100	130	µmho
Output Current	I_O				µA
Source (V_{FB} = 2.3 V)		—	10	—	
Sink (V_{FB} = 2.7 V)		—	10	—	
Output Voltage Swing					V
High State (V_{FB} = 2.3 V)	$V_{OH(ea)}$	5.8	6.4	—	
Low State (V_{FB} = 2.7 V)	$V_{OL(ea)}$	—	1.7	2.4	
OVERVOLTAGE COMPARATOR					
Voltage Feedback Input Threshold	$V_{FB(OV)}$	1.065 V_{FB}	1.08 V_{FB}	1.095 V_{FB}	V
MULTIPLIER					
Input Bias Current, Pin 3 (V_{FB} = 0 V)	I_{IB}	—	– 0.1	– 0.5	µA
Input Threshold, Pin 2	$V_{th(M)}$	1.05 $V_{OL(EA)}$	1.2 $V_{OL(EA)}$	—	V
Dynamic Input Voltage Range					V
Multiplier Input (Pin 3)	$V_{Pin\ 3}$	0 to 2.5	0 to 3.5	—	
Compensation (Pin 2)	$V_{Pin\ 2}$	$V_{th(M)}$ to ($V_{th(M)}$ + 1.0)	$V_{th(M)}$ to ($V_{th(M)}$ + 1.5)	—	
Multiplier Gain ($V_{Pin\ 3}$ = 0.5 V, $V_{Pin\ 2} = V_{th(M)}$ + 1.0 V) (Note 4)	K	0.43	0.65	0.87	1/V
ZERO CURRENT DETECTOR					
Input Threshold Voltage (V_{in} Increasing)	V_{th}	1.33	1.6	1.87	V
Hysteresis (V_{in} Decreasing)	V_H	100	200	300	mV
Input Clamp Voltage					V
High State (I_{DET} = + 3.0 mA)	V_{IH}	6.1	6.7	—	
Low State (I_{DET} = – 3.0 mA)	V_{IL}	0.3	0.7	1.0	

ELECTRICAL CHARACTERISTICS (V_{CC} = 12 V (Note 2), for typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies (Note 3), unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
CURRENT SENSE COMPARATOR					
Input Bias Current ($V_{Pin\ 4}$ = 0 V)	I_{IB}	—	– 0.15	–1.0	µA
Input Offset Voltage ($V_{Pin\ 2}$ = 1.1 V, $V_{Pin\ 3}$ = 0 V)	V_{IO}	—	9.0	25	mV
Maximum Current Sense Input Threshold (Note 5)	$V_{th(max)}$	1.3	1.5	1.8	V
Delay to Output	$t_{PHL(in/out)}$	—	200	400	ns
DRIVE OUTPUT					
Output Voltage (V_{CC} = 12 V)					V
Low State (I_{Sink} = 20 mA) (I_{Sink} = 200 mA)	V_{OL}	— —	0.3 2.4	0.8 3.3	
High State (I_{Source} = 20 mA) (I_{Source} = 200 mA)	V_{OH}	9.8 7.8	10.3 8.4	— —	
Output Voltage (V_{CC} = 30 V) High State (I_{Source} = 20 mA, C_L = 15 pF)	$V_{O(max)}$	14	16	18	V
Output Voltage Rise Time (C_L = 1.0 nF)	t_r	—	50	120	ns
Output Voltage Fall Time (C_L = 1.0 nF)	t_f	—	50	120	ns
Output Voltage with UVLO Activated (V_{CC} = 7.0 V, I_{Sink} = 1.0 mA)	$V_{O(UVLO)}$	—	0.1	0.5	V
RESTART TIMER					
Restart Time Delay	t_{DLY}	200	620	—	µs
UNDERVOLTAGE LOCKOUT					
Startup Threshold (V_{CC} Increasing)	$V_{th(on)}$	11.5	13	14.5	V
Minimum Operating Voltage After Turn–On (V_{CC} Decreasing)	$V_{Shutdown}$	7.0	8.0	9.0	V
Hysteresis	V_H	3.8	5.0	6.2	V
TOTAL DEVICE					
Power Supply Current	I_{CC}				mA
Startup (V_{CC} = 7.0 V) Operating Dynamic Operating (50 kHz, C_L = 1.0 nF)		— — —	0.25 6.5 9.0	0.4 12 20	
Power Supply Zener Voltage (I_{CC} = 25 mA)	V_Z	30	36	—	V

NOTES: 1. Maximum package power dissipation limits must be observed.
2. Adjust V_{CC} above the startup threshold before setting to 12 V.
3. T_{low} = 0°C for MC34262 = – 40°C for MC33262; T_{high} = + 85°C for MC34262 = +105°C for MC33262
4. $K = \dfrac{\text{Pin 4 Threshold}}{V_{Pin\ 3}\,(V_{Pin\ 2} - V_{th(M)})}$
5. This parameter is measured with V_{FB} = 0 V, and $V_{Pin\ 3}$ = 3.0 V

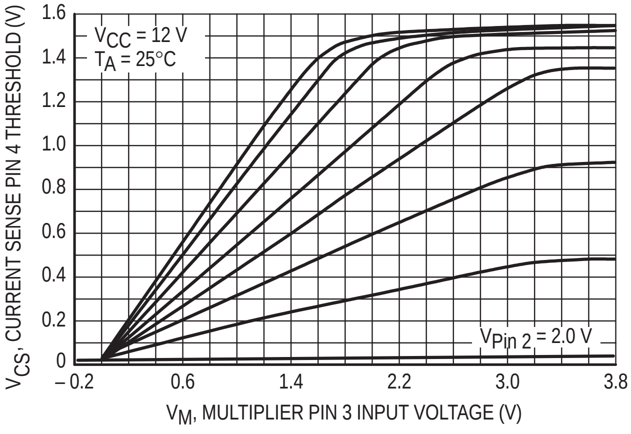


Figure 1. Current Sense Input Threshold versus Multiplier Input

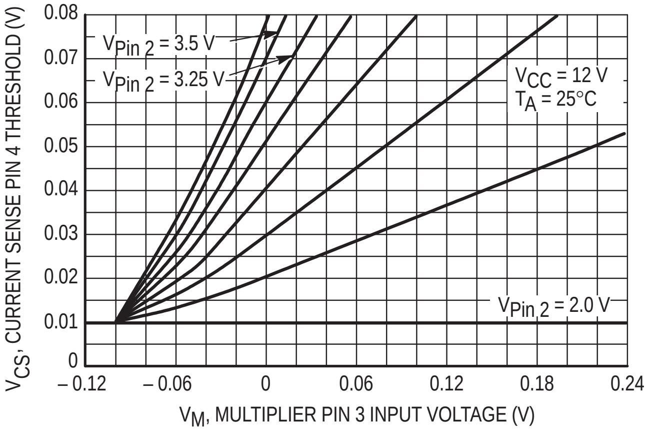


Figure 2. Current Sense Input Threshold versus Multiplier Input, Expanded View

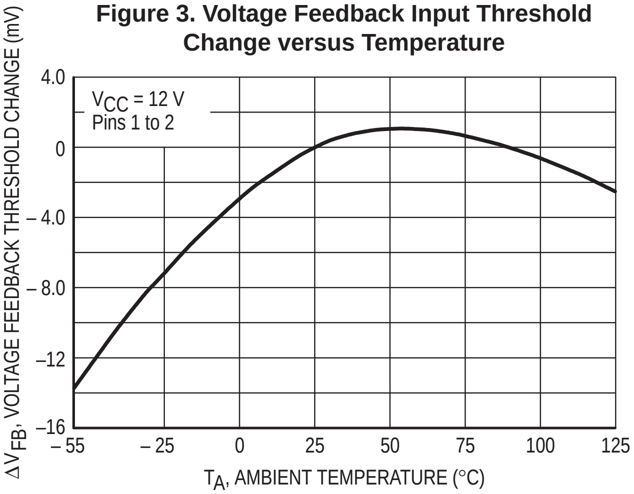


Figure 3. Voltage Feedback Input Threshold Change versus Temperature

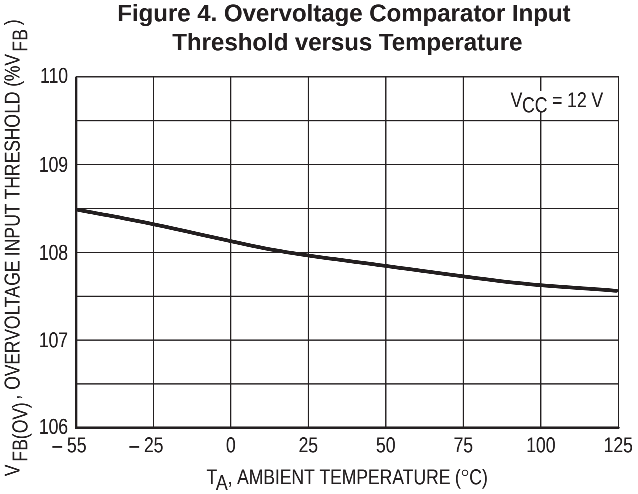


Figure 4. Overvoltage Comparator Input Threshold versus Temperature

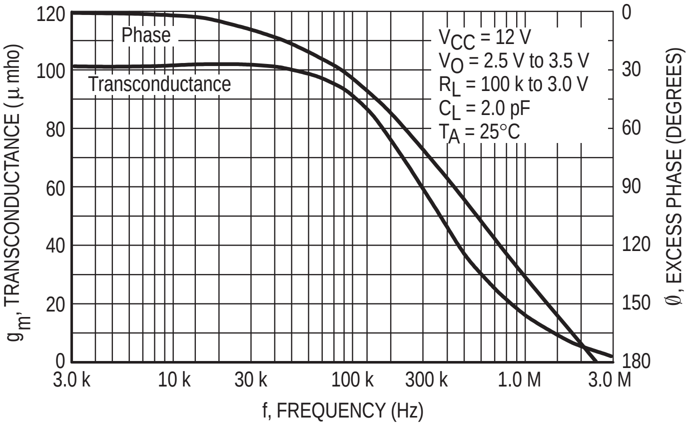


Figure 5. Error Amp Transconductance and Phase versus Frequency

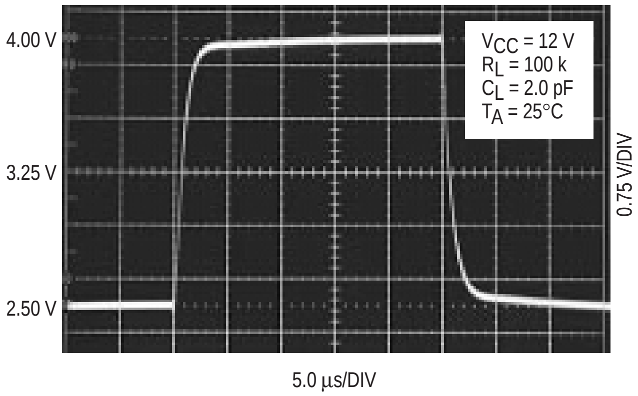


Figure 6. Error Amp Transient Response

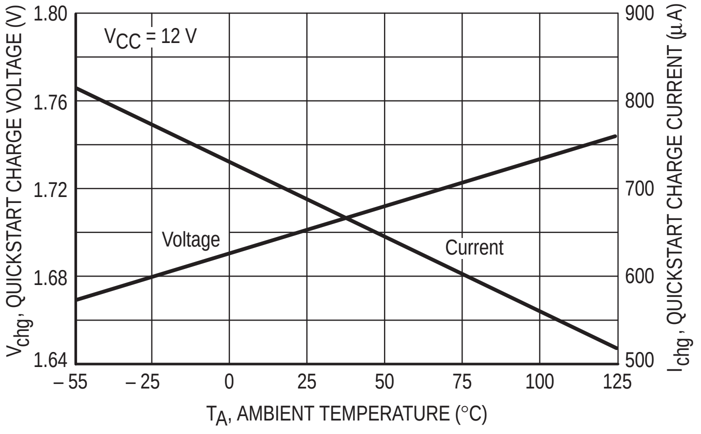


Figure 7. Quickstart Charge Current versus Temperature

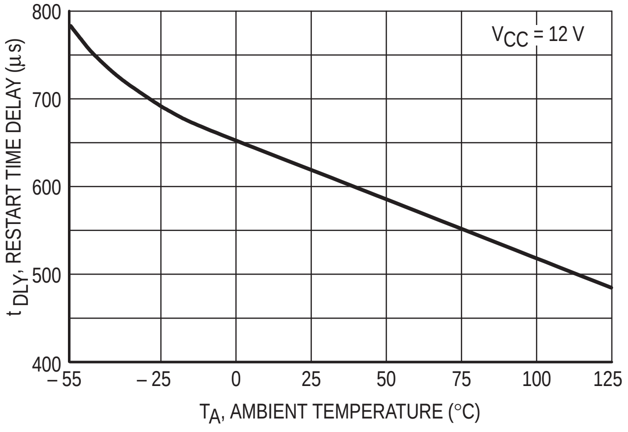


Figure 8. Restart Timer Delay versus Temperature

Figure 9. Zero Current Detector Input Threshold Voltage versus Temperature

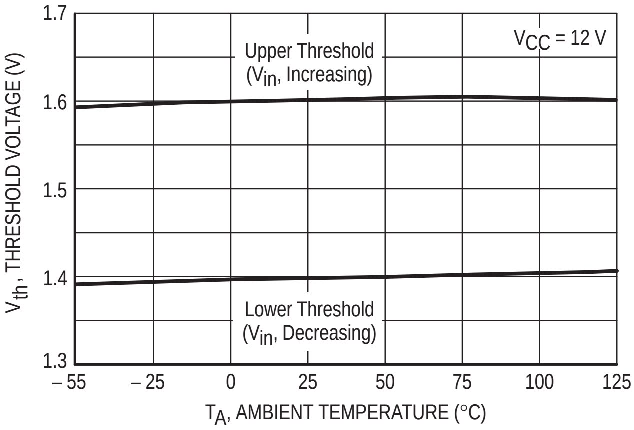


Figure 10. Output Saturation Voltage versus Load Current

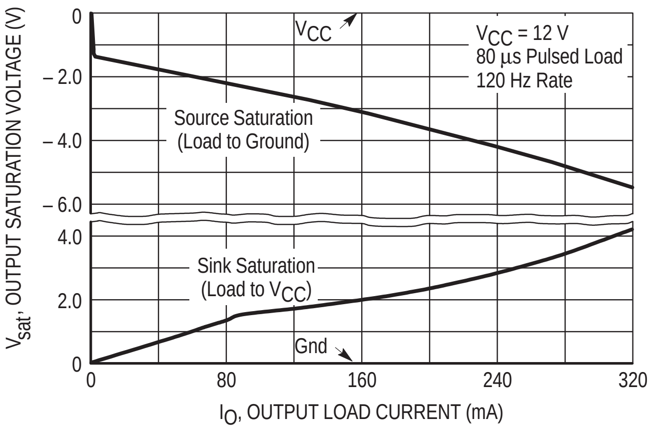


Figure 11. Drive Output Waveform

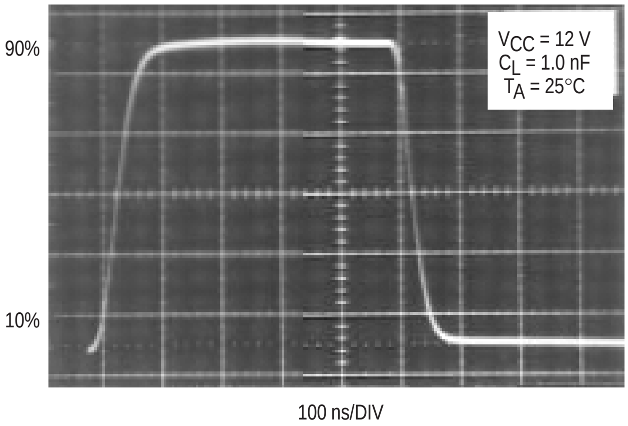


Figure 12. Drive Output Cross Conduction

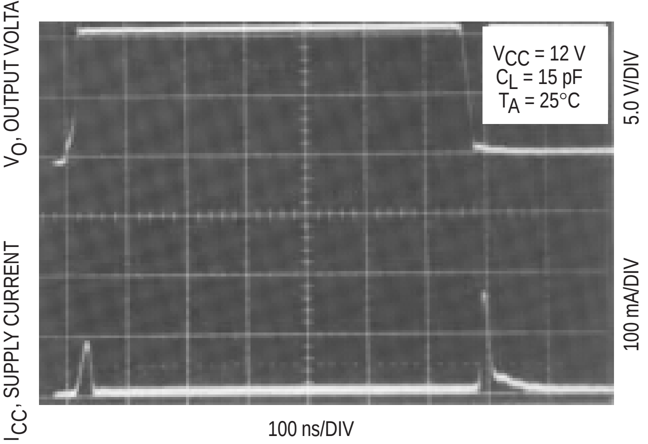


Figure 13. Supply Current versus Supply Voltage

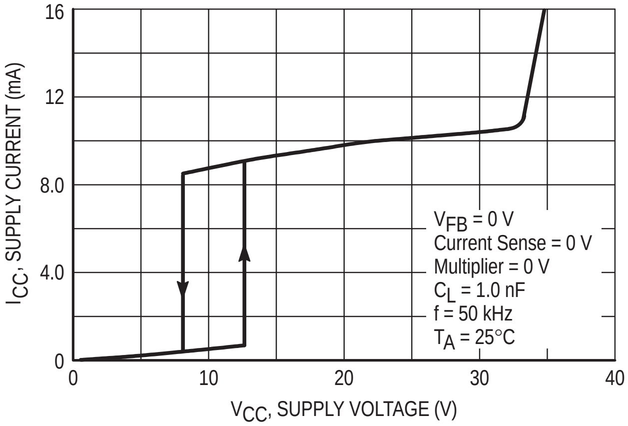
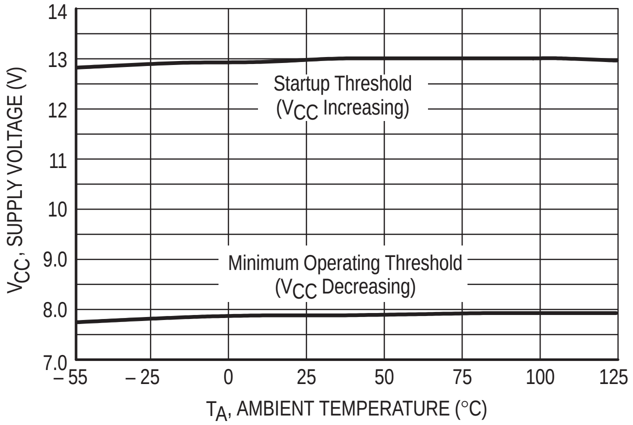


Figure 14. Undervoltage Lockout Thresholds versus Temperature



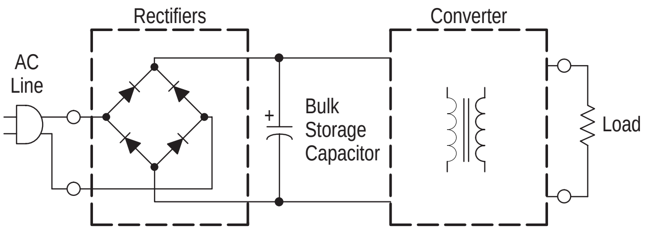
FUNCTIONAL DESCRIPTION

Introduction

With the goal of exceeding the requirements of legislation on line–current harmonic content, there is an ever increasing demand for an economical method of obtaining a unity power factor. This data sheet describes a monolithic control IC that was specifically designed for power factor control with minimal external components. It offers the designer a simple, cost–effective solution to obtain the benefits of active power factor correction.

Most electronic ballasts and switching power supplies use a bridge rectifier and a bulk storage capacitor to derive raw dc voltage from the utility ac line, Figure 15.

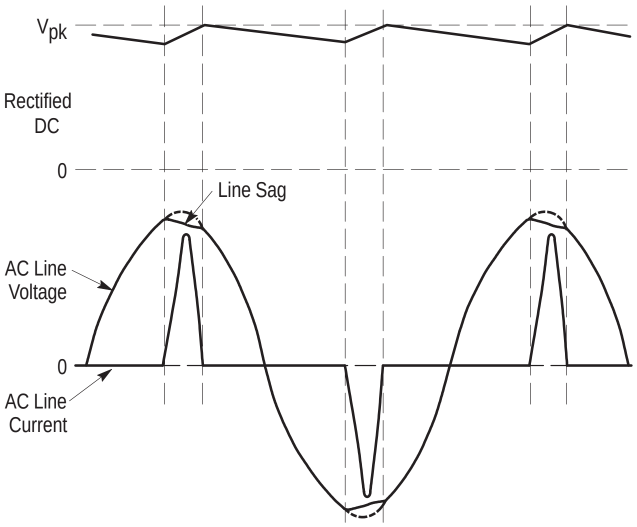
Figure 15. Uncorrected Power Factor Circuit



This simple rectifying circuit draws power from the line when the instantaneous ac voltage exceeds the capacitor voltage. This occurs near the line voltage peak and results in a high charge current spike, Figure 16. Since power is only taken near the line voltage peaks, the resulting spikes of current are extremely nonsinusoidal with a high content of harmonics. This results in a poor power factor condition where the apparent input power is much higher than the real power. Power factor ratios of 0.5 to 0.7 are common.

Power factor correction can be achieved with the use of either a passive or an active input circuit. Passive circuits usually contain a combination of large capacitors, inductors, and rectifiers that operate at the ac line frequency. Active circuits incorporate some form of a high frequency switching converter for the power processing, with the boost converter being the most popular topology, Figure 17. Since active input circuits operate at a frequency much higher than that of the ac line, they are smaller, lighter in weight, and more efficient than a passive circuit that yields similar results. With proper control of the preconverter, almost any complex load can be made to appear resistive to the ac line, thus significantly reducing the harmonic current content.

Figure 16. Uncorrected Power Factor Input Waveforms

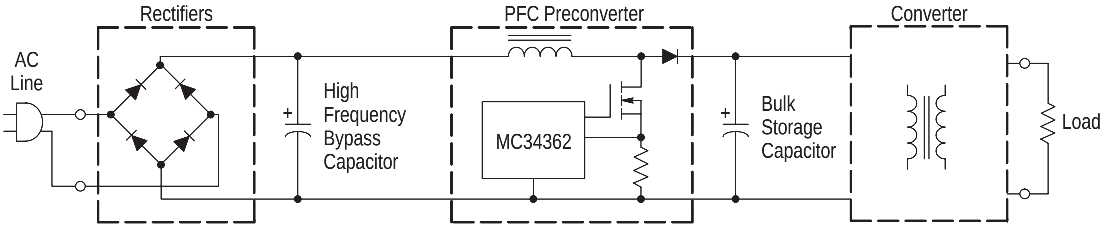


The MC34262, MC33262 are high performance, critical conduction, current–mode power factor controllers specifically designed for use in off–line active preconverters. These devices provide the necessary features required to significantly enhance poor power factor loads by keeping the ac line current sinusoidal and in phase with the line voltage.

Operating Description

The MC34262, MC33262 contain many of the building blocks and protection features that are employed in modern high performance current mode power supply controllers. There are, however, two areas where there is a major difference when compared to popular devices such as the UC3842 series. Referring to the block diagram in Figure 19, note that a multiplier has been added to the current sense loop and that this device does not contain an oscillator. The reasons for these differences will become apparent in the following discussion. A description of each of the functional blocks is given below.

Figure 17. Active Power Factor Correction Preconverter



Error Amplifier

An Error Amplifier with access to the inverting input and output is provided. The amplifier is a transconductance type, meaning that it has high output impedance with controlled voltage–to–current gain. The amplifier features a typical gm of 100 µmhos (Figure 5). The noninverting input is internally biased at 2.5 V ± 2.0% and is not pinned out. The output voltage of the power factor converter is typically divided down and monitored by the inverting input. The maximum input bias current is – 0.5 µA, which can cause an output voltage error that is equal to the product of the input bias current and the value of the upper divider resistor R_2. The Error Amp output is internally connected to the Multiplier and is pinned out (Pin 2) for external loop compensation. Typically, the bandwidth is set below 20 Hz, so that the amplifier's output voltage is relatively constant over a given ac line cycle. In effect, the error amp monitors the average output voltage of the converter over several line cycles. The Error Amp output stage was designed to have a relatively constant transconductance over temperature. This allows the designer to define the compensated bandwidth over the intended operating temperature range. The output stage can sink and source 10 µA of current and is capable of swinging from 1.7 V to 6.4 V, assuring that the Multiplier can be driven over its entire dynamic range.

A key feature to using a transconductance type amplifier, is that the input is allowed to move independently with respect to the output, since the compensation capacitor is connected to ground. This allows dual usage of of the Voltage Feedback Input pin by the Error Amplifier and by the Overvoltage Comparator.

Overvoltage Comparator

An Overvoltage Comparator is incorporated to eliminate the possibility of runaway output voltage. This condition can occur during initial startup, sudden load removal, or during output arcing and is the result of the low bandwidth that must be used in the Error Amplifier control loop. The Overvoltage Comparator monitors the peak output voltage of the converter, and when exceeded, immediately terminates MOSFET switching. The comparator threshold is internally set to 1.08 V_{ref}. In order to prevent false tripping during normal operation, the value of the output filter capacitor C_3 must be large enough to keep the peak–to–peak ripple less than 16% of the average dc output. The Overvoltage Comparator input to Drive Output turn–off propagation delay is typically 400 ns. A comparison of startup overshoot without and with the Overvoltage Comparator circuit is shown in Figure 23.

Multiplier

A single quadrant, two input multiplier is the critical element that enables this device to control power factor. The ac full wave rectified haversines are monitored at Pin 3 with respect to ground while the Error Amp output at Pin 2 is monitored with respect to the Voltage Feedback Input threshold. The Multiplier is designed to have an extremely linear transfer curve over a wide dynamic range, 0 V to 3.2 V for Pin 3, and 2.0 V to 3.75 V for Pin 2, Figure 1. The Multiplier output controls the Current Sense Comparator threshold as the ac voltage traverses sinusoidally from zero to peak line, Figure 18. This has the effect of forcing the MOSFET on–time to track the input line voltage, resulting in a fixed Drive Output on–time, thus making the preconverter load appear to be resistive to the ac line. An approximation of the Current Sense Comparator threshold can be calculated from the following equation. This equation is accurate only under the given test condition stated in the electrical table.

$$V_{CS}\text{, Pin 4 Threshold} \approx 0.65\,(V_{Pin\ 2} - V_{th(M)})\,V_{Pin\ 3}$$

A significant reduction in line current distortion can be attained by forcing the preconverter to switch as the ac line voltage crosses through zero. The forced switching is achieved by adding a controlled amount of offset to the Multiplier and Current Sense Comparator circuits. The equation shown below accounts for the built–in offsets and is accurate to within ten percent. Let $V_{th(M)} = 1.991$ V

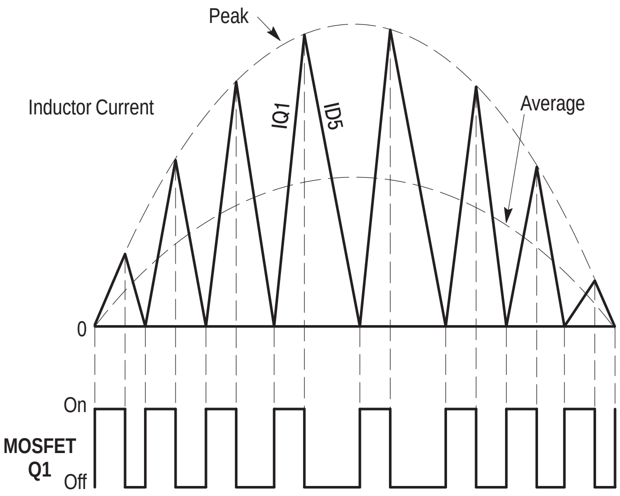
$$V_{CS}\text{, Pin 4 Threshold} = 0.544\,(V_{Pin\ 2} - V_{th(M)})\,V_{Pin\ 3} + 0.0417\,(V_{Pin\ 2} - V_{th(M)})$$

Zero Current Detector

The MC34262 operates as a critical conduction current mode controller, whereby output switch conduction is initiated by the Zero Current Detector and terminated when the peak inductor current reaches the threshold level established by the Multiplier output. The Zero Current Detector initiates the next on–time by setting the RS Latch at the instant the inductor current reaches zero. This critical conduction mode of operation has two significant benefits. First, since the MOSFET cannot turn–on until the inductor current reaches zero, the output rectifier reverse recovery time becomes less critical, allowing the use of an inexpensive rectifier. Second, since there are no deadtime gaps between cycles, the ac line current is continuous, thus limiting the peak switch to twice the average input current.

The Zero Current Detector indirectly senses the inductor current by monitoring when the auxiliary winding voltage falls below 1.4 V. To prevent false tripping, 200 mV of hysteresis is provided. Figure 9 shows that the thresholds are well–defined over temperature. The Zero Current Detector input is internally protected by two clamps. The upper 6.7 V clamp prevents input overvoltage breakdown while the lower 0.7 V clamp prevents substrate injection. Current limit protection of the lower clamp transistor is provided in the event that the input pin is accidentally shorted to ground. The Zero Current Detector input to Drive Output turn–on propagation delay is typically 320 ns.

Figure 18. Inductor Current and MOSFET Gate Voltage Waveforms



Current Sense Comparator and RS Latch

The Current Sense Comparator RS Latch configuration used ensures that only a single pulse appears at the Drive Output during a given cycle. The inductor current is converted to a voltage by inserting a ground–referenced sense resistor R_7 in series with the source of output switch Q1. This voltage is monitored by the Current Sense Input and compared to a level derived from the Multiplier output. The peak inductor current under normal operating conditions is controlled by the threshold voltage of Pin 4 where:

$$I_{L(pk)} = \frac{\text{Pin 4 Threshold}}{R_7}$$

Abnormal operating conditions occur during preconverter startup at extremely high line or if output voltage sensing is lost. Under these conditions, the Multiplier output and Current Sense threshold will be internally clamped to 1.5 V. Therefore, the maximum peak switch current is limited to:

$$I_{pk(max)} = \frac{1.5\text{ V}}{R_7}$$

An internal RC filter has been included to attenuate any high frequency noise that may be present on the current waveform. This filter helps reduce the ac line current distortion especially near the zero crossings. With the component values shown in Figure 20, the Current Sense Comparator threshold, at the peak of the haversine varies from 1.1 V at 90 Vac to 100 mV at 268 Vac. The Current Sense Input to Drive Output turn–off propagation delay is typically less than 200 ns.

Timer

A watchdog timer function was added to the IC to eliminate the need for an external oscillator when used in stand–alone applications. The Timer provides a means to automatically start or restart the preconverter if the Drive Output has been off for more than 620 μs after the inductor current reaches zero. The restart time delay versus temperature is shown in Figure 8.

Undervoltage Lockout and Quickstart

An Undervoltage Lockout comparator has been incorporated to guarantee that the IC is fully functional before enabling the output stage. The positive power supply terminal (V_{CC}) is monitored by the UVLO comparator with the upper threshold set at 13 V and the lower threshold at 8.0 V. In the stand–by mode, with V_{CC} at 7.0 V, the required supply current is less than 0.4 mA. This large hysteresis and low startup current allow the implementation of efficient bootstrap startup techniques, making these devices ideally suited for wide input range off–line preconverter applications. An internal 36 V clamp has been added from V_{CC} to ground to protect the IC and capacitor C_4 from an overvoltage condition. This feature is desirable if external circuitry is used to delay the startup of the preconverter. The supply current, startup, and operating voltage characteristics are shown in Figures 13 and 14.

A Quickstart circuit has been incorporated to optimize converter startup. During initial startup, compensation capacitor C_1 will be discharged, holding the error amp output below the Multiplier threshold. This will prevent Drive Output switching and delay bootstrapping of capacitor C_4 by diode D_6. If Pin 2 does not reach the multiplier threshold before C_4 discharges below the lower UVLO threshold, the converter will “hiccup” and experience a significant startup delay. The Quickstart circuit is designed to precharge C_1 to 1.7 V, Figure 7. This level is slightly below the Pin 2 Multiplier threshold, allowing immediate Drive Output switching and bootstrap operation when C_4 crosses the upper UVLO threshold.

Drive Output

The MC34262/MC33262 contain a single totem–pole output stage specifically designed for direct drive of power MOSFETs. The Drive Output is capable of up to ± 500 mA peak current with a typical rise and fall time of 50 ns with a 1.0 nF load. Additional internal circuitry has been added to keep the Drive Output in a sinking mode whenever the Undervoltage Lockout is active. This characteristic eliminates the need for an external gate pull–down resistor. The totem–pole output has been optimized to minimize cross–conduction current during high speed operation. The addition of two 10 Ω resistors, one in series with the source output transistor and one in series with the sink output transistor, helps to reduce the cross–conduction current and radiated noise by limiting the output rise and fall time. A 16 V clamp has been incorporated into the output stage to limit the high state V_{OH}. This prevents rupture of the MOSFET gate when V_{CC} exceeds 20 V.

APPLICATIONS INFORMATION

The application circuits shown in Figures 19, 20 and 21 reveal that few external components are required for a complete power factor preconverter. Each circuit is a peak detecting current–mode boost converter that operates in critical conduction mode with a fixed on–time and variable off–time. A major benefit of critical conduction operation is that the current loop is inherently stable, thus eliminating the need for ramp compensation. The application in Figure 19 operates over an input voltage range of 90 Vac to 138 Vac and provides an output power of 80 W (230 V at 350 mA) with an associated power factor of approximately 0.998 at nominal line. Figures 20 and 21 are universal input preconverter examples that operate over a continuous input voltage range of 90 Vac to 268 Vac. Figure 20 provides an output power of 175 W (400 V at 440 mA) while Figure 21 provides 450 W (400 V at 1.125 A). Both circuits have an observed worst–case power factor of approximately 0.989. The input current and voltage waveforms of Figure 20 are shown in Figure 22 with operation at 115 Vac and 230 Vac. The data for each of the applications was generated with the test set–up shown in Figure 24.

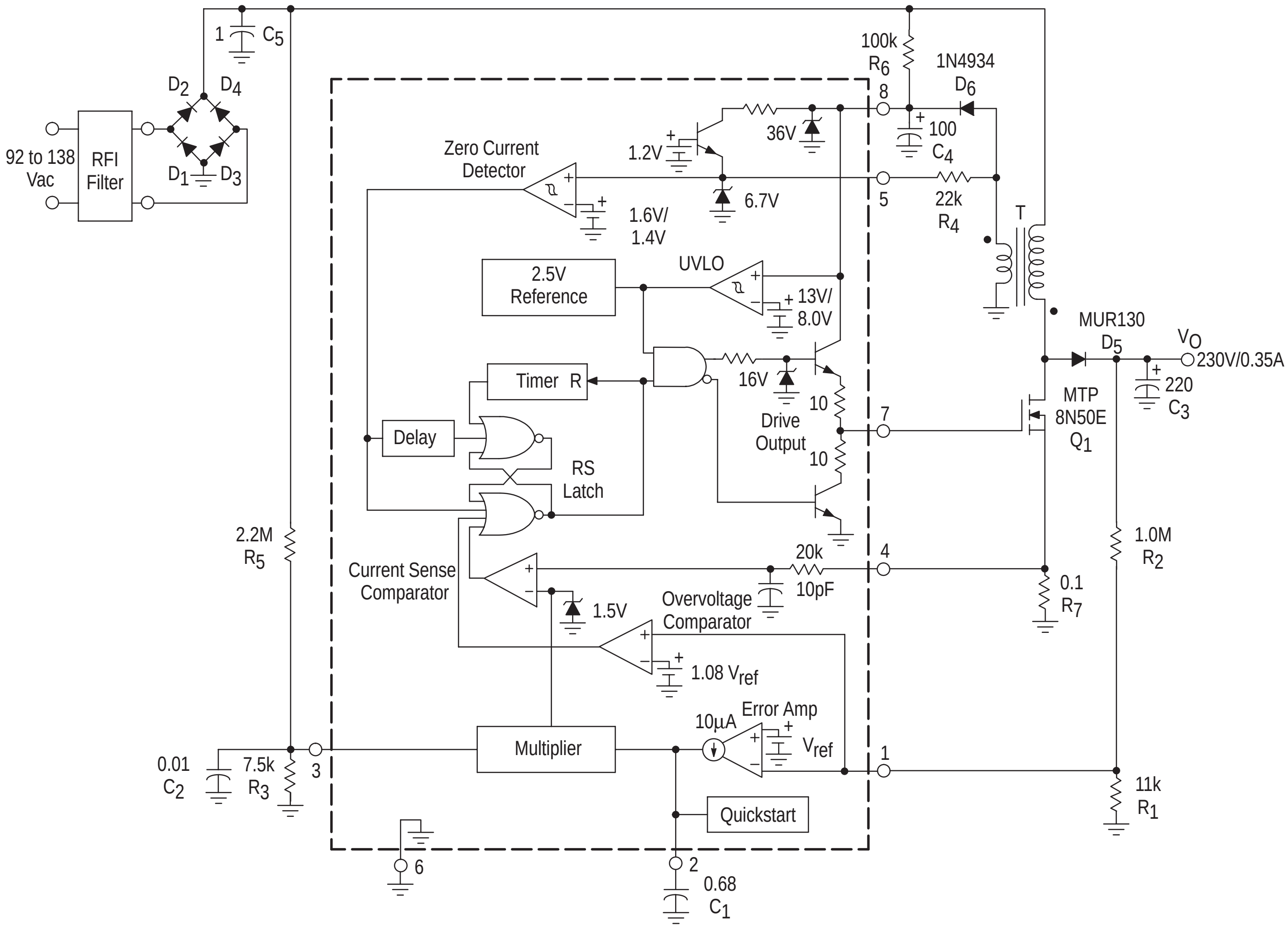
Table 1. Design Equations

Notes	Calculation	Formula
Calculate the maximum required output power.	Required Converter Output Power	$P_O = V_O I_O$
Calculated at the minimum required ac line voltage for output regulation. Let the efficiency η = 0.92 for low line operation.	Peak Inductor Current	$I_{L(pk)} = \frac{2\sqrt{2}\,P_O}{\eta Vac_{(LL)}}$
Let the switching cycle t = 40 µs for universal input (85 to 265 Vac) operation and 20 µs for fixed input (92 to 138 Vac, or 184 to 276 Vac) operation.	Inductance	$L_P = \frac{t\left(\frac{V_O}{\sqrt{2}} - Vac_{(LL)}\right)\eta\, Vac_{(LL)}^2}{\sqrt{2}\,V_O P_O}$
In theory the on–time t_{on} is constant. In practice t_{on} tends to increase at the ac line zero crossings due to the charge on capacitor C_5. Let Vac = $Vac_{(LL)}$ for initial t_{on} and t_{off} calculations.	Switch On–Time	$t_{on} = \frac{2 P_O L_P}{\eta\, Vac^2}$
The off–time t_{off} is greatest at the peak of the ac line voltage and approaches zero at the ac line zero crossings. Theta (θ) represents the angle of the ac line voltage.	Switch Off–Time	$t_{off} = \frac{t_{on}}{\frac{V_O}{\sqrt{2}\,Vac\,\lvert \sin\theta \rvert} - 1}$
The minimum switching frequency occurs at the peak of the ac line voltage. As the ac line voltage traverses from peak to zero, t_{off} approaches zero producing an increase in switching frequency.	Switching Frequency	$f = \frac{1}{t_{on} + t_{off}}$
Set the current sense threshold V_{CS} to 1.0 V for universal input (85 Vac to 265 Vac) operation and to 0.5 V for fixed input (92 Vac to 138 Vac, or 184 Vac to 276 Vac) operation. Note that V_{CS} must be <1.4 V.	Peak Switch Current	$R_7 = \frac{V_{CS}}{I_{L(pk)}}$
Set the multiplier input voltage V_M to 3.0 V at high line. Empirically adjust V_M for the lowest distortion over the ac line voltage range while guaranteeing startup at minimum line.	Multiplier Input Voltage	$V_M = \frac{Vac\,\sqrt{2}}{\left(\frac{R_5}{R_3} + 1\right)}$
The I_{IB} R_1 error term can be minimized with a divider current in excess of 50 µA.	Converter Output Voltage	$V_O = V_{ref}\left(\frac{R_2}{R_1} + 1\right) - I_{IB} R_2$
The calculated peak–to–peak ripple must be less than 16% of the average dc output voltage to prevent false tripping of the Overvoltage Comparator. Refer to the Overvoltage Comparator text. ESR is the equivalent series resistance of C_3	Converter Output Peak to Peak Ripple Voltage	$\Delta V_{O(pp)} = I_O \sqrt{\left(\frac{1}{2\pi f_{ac} C_3}\right)^2 + ESR^2}$
The bandwidth is typically set to 20 Hz. When operating at high ac line, the value of C_1 may need to be increased. (See Figure 25)	Error Amplifier Bandwidth	$BW = \frac{gm}{2\pi C_1}$

The following converter characteristics must be chosen:

V_O — Desired output voltage
I_O — Desired output current
ΔV_O — Converter output peak–to–peak ripple voltage
Vac — AC RMS line voltage
$Vac_{(LL)}$ — AC RMS low line voltage

Figure 19. 80 W Power Factor Controller



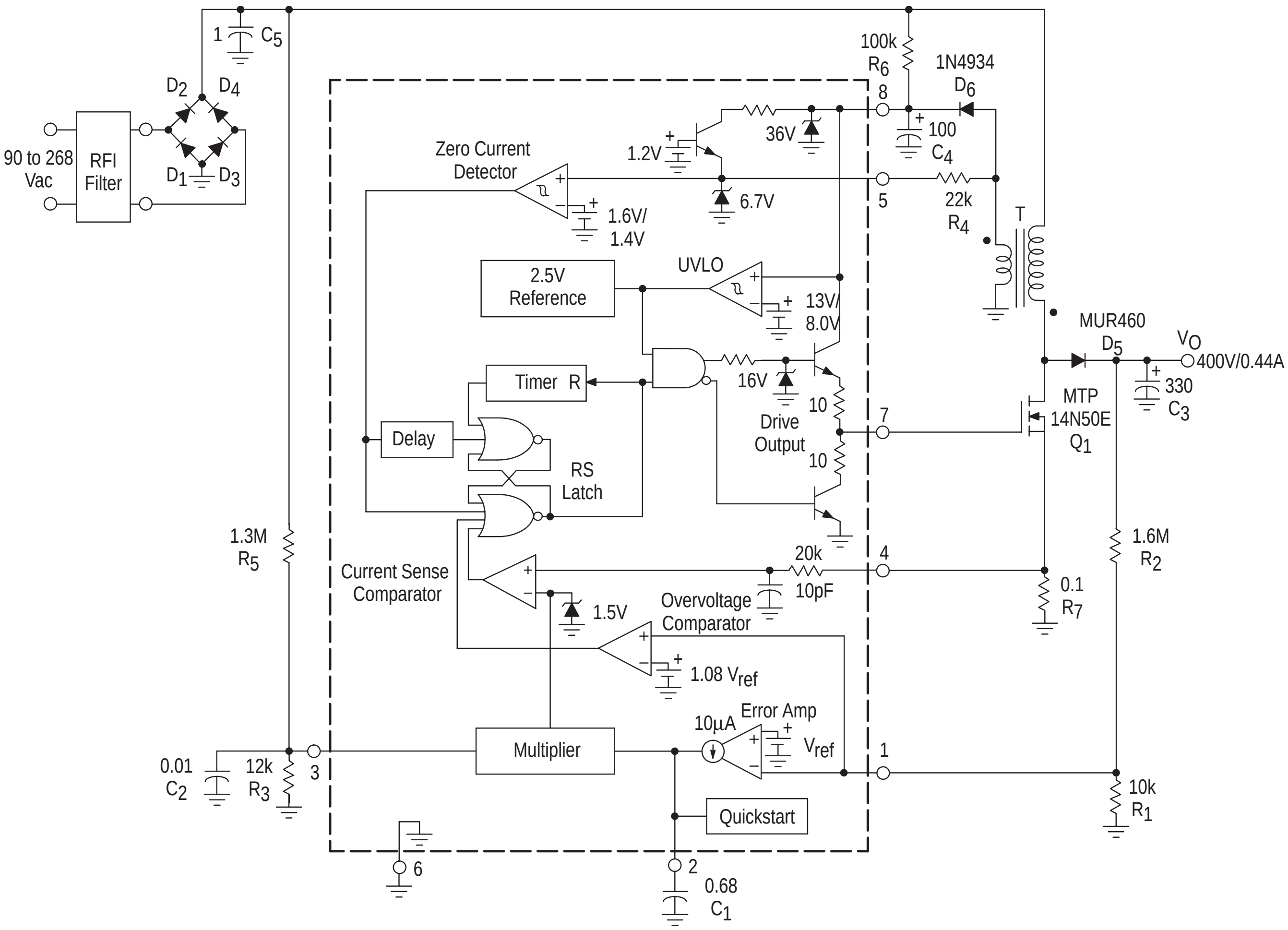
Power Factor Controller Test Data

AC Line Input									DC Output				
				Current Harmonic Distortion (% I_{fund})									
V_{rms}	P_{in}	PF	I_{fund}	THD	2	3	5	7	$V_{O(pp)}$	V_O	I_O	P_O	η(%)
90	85.9	0.999	0.93	2.6	0.08	1.6	0.84	0.95	4.0	230.7	0.350	80.8	94.0
100	85.3	0.999	0.85	2.3	0.13	1.0	1.2	0.73	4.0	230.7	0.350	80.8	94.7
110	85.1	0.998	0.77	2.2	0.10	0.58	1.5	0.59	4.0	230.7	0.350	80.8	94.9
120	84.7	0.998	0.71	3.0	0.09	0.73	1.9	0.58	4.1	230.7	0.350	80.8	95.3
130	84.4	0.997	0.65	3.9	0.12	1.7	2.2	0.61	4.1	230.7	0.350	80.8	95.7
138	84.1	0.996	0.62	4.6	0.16	2.4	2.3	0.60	4.1	230.7	0.350	80.8	96.0

This data was taken with the test set–up shown in Figure 24.

T = Coilcraft N2881–A
Primary: 62 turns of # 22 AWG
Secondary: 5 turns of # 22 AWG
Core: Coilcraft PT2510, EE 25
Gap: 0.072″ total for a primary inductance (L_P) of 320 µH
Heatsink = AAVID Engineering Inc. 590302B03600, or 593002B03400

Figure 20. 175 W Universal Input Power Factor Controller



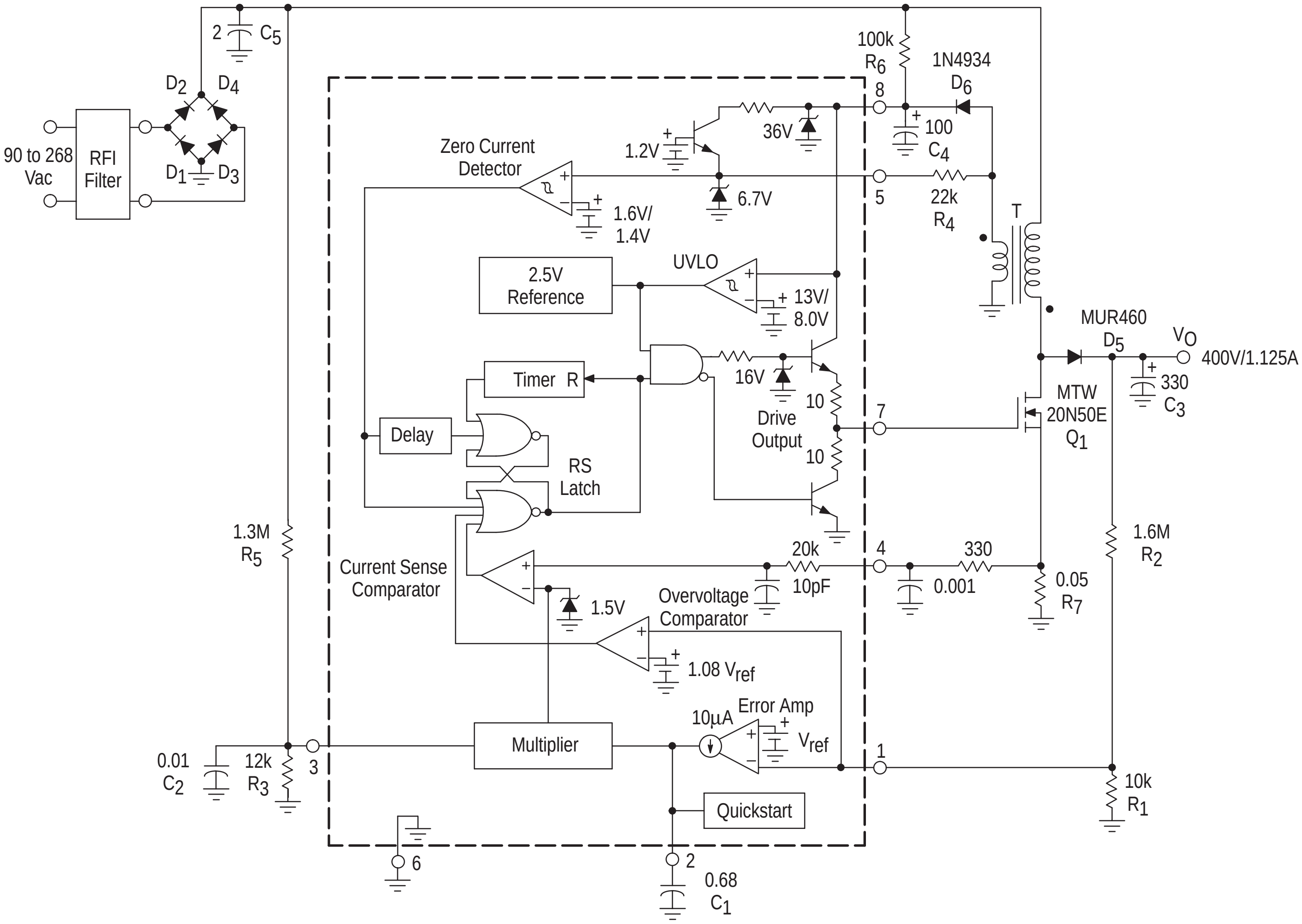
Power Factor Controller Test Data

AC Line Input									DC Output				
				Current Harmonic Distortion (% I_{fund})									
V_{rms}	P_{in}	PF	I_{fund}	THD	2	3	5	7	$V_{O(pp)}$	V_O	I_O	P_O	η(%)
90	193.3	0.991	2.15	2.8	0.18	2.6	0.55	1.0	3.3	402.1	0.44	176.9	91.5
120	190.1	0.998	1.59	1.6	0.10	1.4	0.23	0.72	3.3	402.1	0.44	176.9	93.1
138	188.2	0.999	1.36	1.2	0.12	1.3	0.65	0.80	3.3	402.1	0.44	176.9	94.0
180	184.9	0.998	1.03	2.0	0.10	0.49	1.2	0.82	3.4	402.1	0.44	176.9	95.7
240	182.0	0.993	0.76	4.4	0.09	1.6	2.3	0.51	3.4	402.1	0.44	176.9	97.2
268	180.9	0.989	0.69	5.9	0.10	2.3	2.9	0.46	3.4	402.1	0.44	176.9	97.8

This data was taken with the test set–up shown in Figure 24.

T = Coilcraft N2880–A
Primary: 78 turns of # 16 AWG
Secondary: 6 turns of # 18 AWG
Core: Coilcraft PT4215, EE 42–15
Gap: 0.104″ total for a primary inductance (L_P) of 870 µH
Heatsink = AAVID Engineering Inc. 590302B03600

Figure 21. 450 W Universal Input Power Factor Controller



Power Factor Controller Test Data

AC Line Input									DC Output				
				Current Harmonic Distortion (% I_{fund})									
V_{rms}	P_{in}	PF	I_{fund}	THD	2	3	5	7	$V_{O(pp)}$	V_O	I_O	P_O	η(%)
90	489.5	0.990	5.53	2.2	0.10	1.5	0.25	0.83	8.8	395.5	1.14	450.9	92.1
120	475.1	0.998	3.94	2.5	0.12	0.29	0.62	0.52	8.8	395.5	1.14	450.9	94.9
138	470.6	0.998	3.38	2.1	0.06	0.70	1.1	0.41	8.8	395.5	1.14	450.9	95.8
180	463.4	0.998	2.57	4.1	0.21	2.0	1.6	0.71	8.9	395.5	1.14	450.9	97.3
240	460.1	0.996	1.91	4.8	0.14	4.3	2.2	0.63	8.9	395.5	1.14	450.9	98.0
268	459.1	0.995	1.72	5.8	0.10	5.0	2.5	0.61	8.9	395.5	1.14	450.9	98.2

This data was taken with the test set–up shown in Figure 24.

T = Coilcraft P3657–A
Primary: 38 turns Litz wire, 1300 strands of #48 AWG, Kerrigan–Lewis, Chicago, IL
Secondary: 3 turns of # 20 AWG
Core: Coilcraft PT4220, EE 42–20
Gap: 0.180″ total for a primary inductance (L_P) of 190 µH
Heatsink = AAVID Engineering Inc. 604953B04000 Extrusion

Figure 22. Power Factor Corrected Input Waveforms
(Figure 20 Circuit)

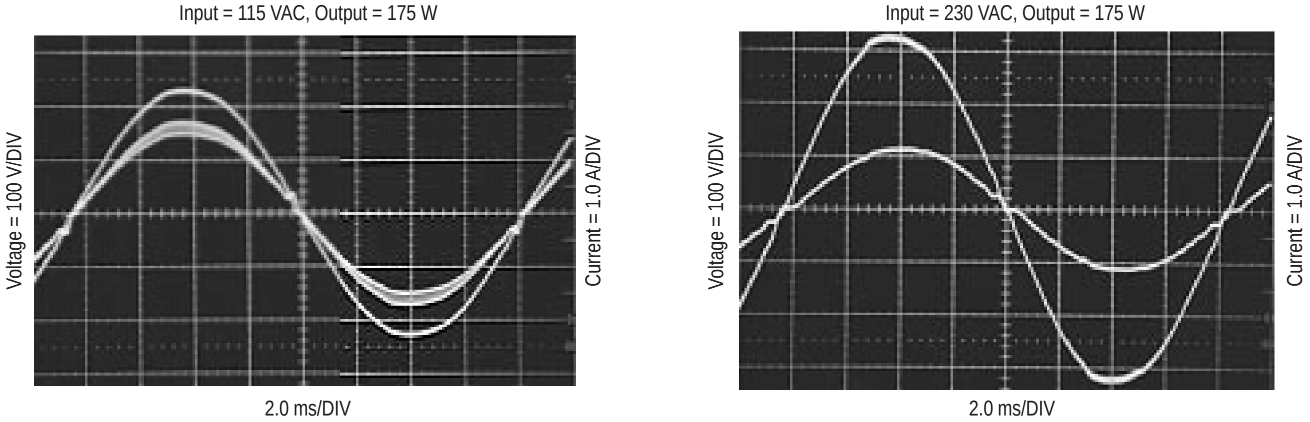


Figure 23. Output Voltage Startup Overshoot
(Figure 20 Circuit)

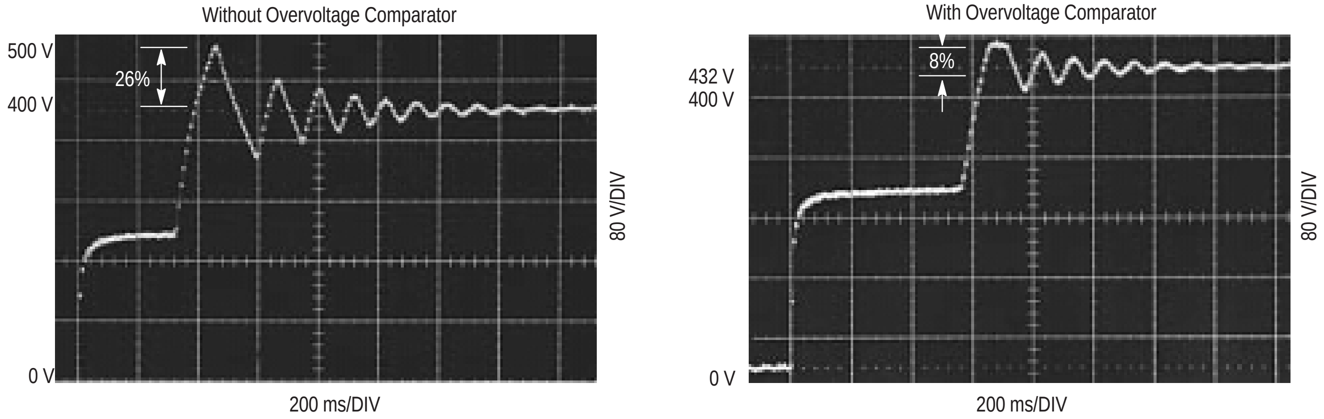
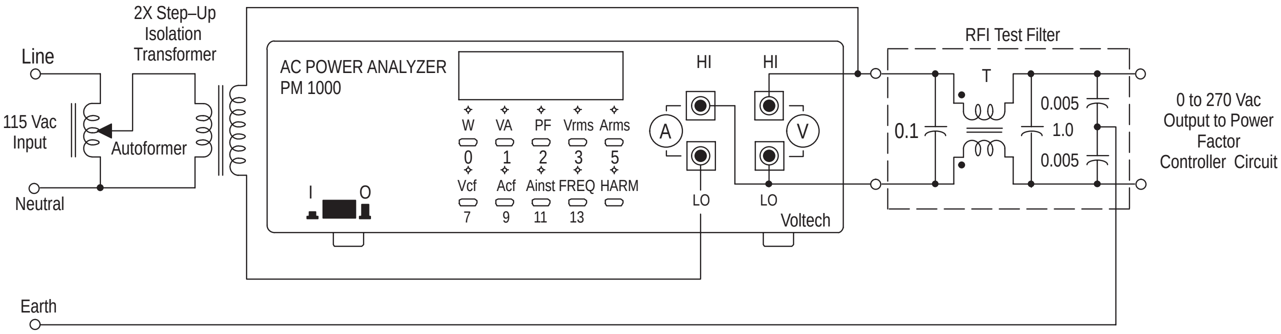
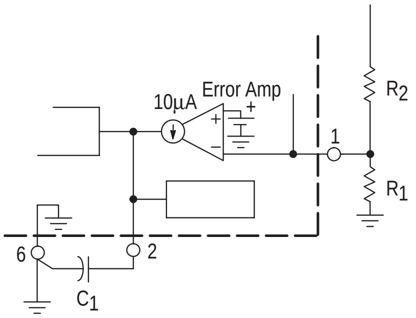


Figure 24. Power Factor Test Set–Up



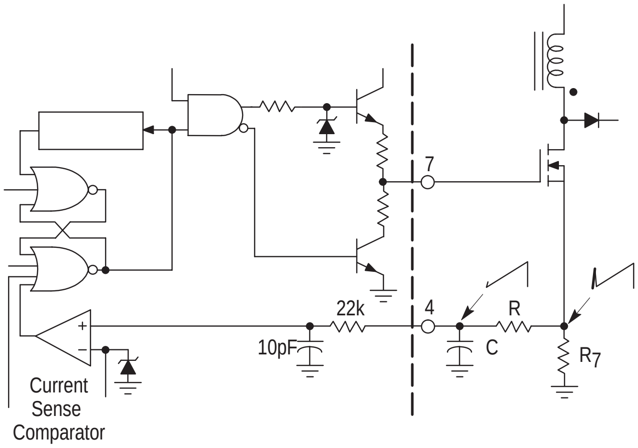
An RFI filter is required for best performance when connecting the preconverter directly to the ac line. The filter attenuates the level of high frequency switching that appears on the ac line current waveform. Figures 19 and 20 work well with commercially available two stage filters such as the Delta Electronics 03DPCG5. Shown above is a single stage test filter that can easily be constructed with four ac line rated capacitors and a common–mode transformer. Coilcraft CMT3–28–2 was used to test Figures 19 and 20. It has a minimum inductance of 28 mH and a maximum current rating of 2.0 A. Coilcraft CMT4–17–9 was used to test Figure 21. It has a minimum inductance of 17 mH and a maximum current rating of 9.0 A. Circuit conversion efficiency η (%) was calculated without the power loss of the RFI filter.

Figure 25. Error Amp Compensation



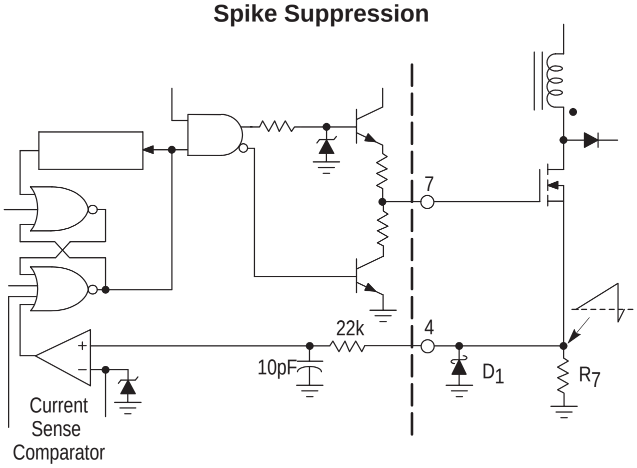
The Error Amp output is a high impedance node and is susceptible to noise pickup. To minimize pickup, compensation capacitor C_1 must be connected as close to Pin 2 as possible with a short, heavy ground returning directly to Pin 6. When operating at high ac line, the voltage at Pin 2 may approach the lower threshold of the Multiplier, ≈ 2.0 V. If there is excessive ripple on Pin 2, the Multiplier will be driven into cut–off causing circuit instability, high distortion and poor power factor. This problem can be eliminated by increasing the value of C_1.

Figure 26. Current Waveform Spike Suppression



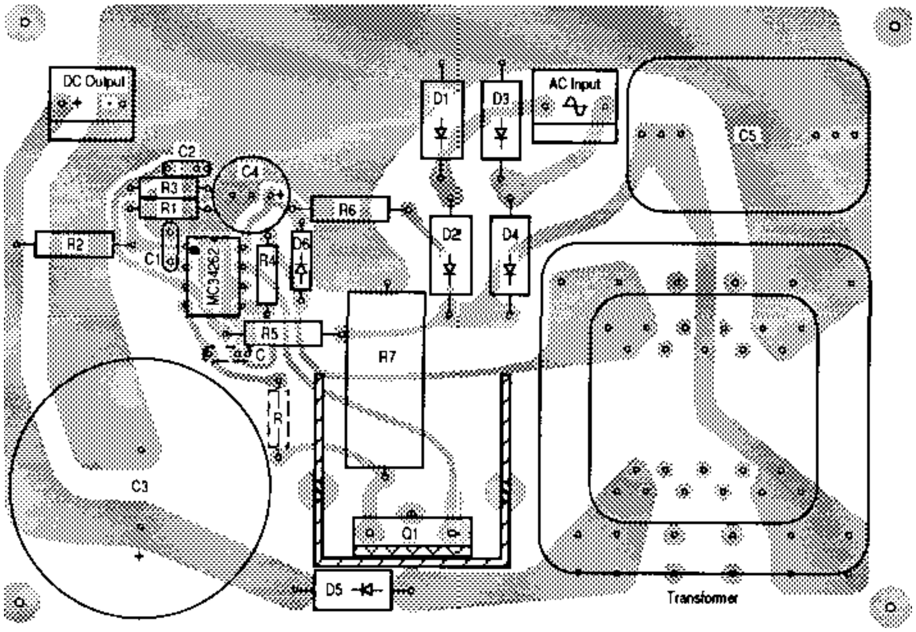
A narrow turn–on spike is usually present on the leading edge of the current waveform and can cause circuit instability. The MC34262 provides an internal RC filter with a time constant of 220 ns. An additional external RC filter may be required in universal input applications that are above 200 W. It is suggested that the external filter be placed directly at the Current Sense Input and have a time constant that approximates the spike duration.

Figure 27. Negative Current Waveform Spike Suppression

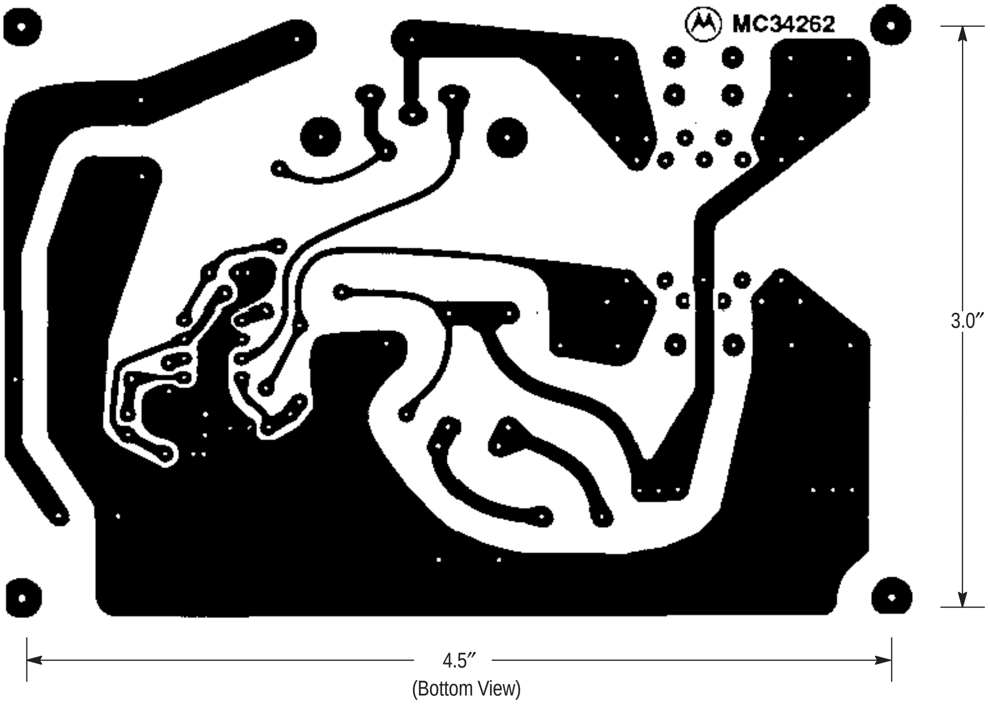


A negative turn–off spike can be observed on the trailing edge of the current waveform. This spike is due to the parasitic inductance of resistor R_7, and if it is excessive, it can cause circuit instability. The addition of Shottky diode D_1 can effectively clamp the negative spike. The addition of the external RC filter shown in Figure 26 may provide sufficient spike attenuation.

Figure 28. Printed Circuit Board and Component Layout
(Circuits of Figures 15 and 16)



(Top View)



(Bottom View)

NOTE: Use 2 oz. copper laminate for optimum circuit performance.

MOTOROLA

MC34268

SCSI-2 Active Terminator Regulator

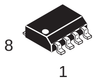
The MC34268 is a medium current, low dropout positive voltage regulator specifically designed for use in SCSI–2 active termination circuits. This device offers the circuit designer an economical solution for precision voltage regulation, while keeping power losses to a minimum. The regulator consists of a 1.0 V dropout composite PNP/NPN pass transistor, current limiting, and thermal limiting. These devices are packaged in the 8–pin SOP–8 and 3–pin DPAK surface mount power packages.

Applications include active SCSI–2 terminators and post regulation of switching power supplies.

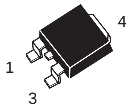
- 2.85 V Output Voltage for SCSI–2 Active Termination
- 1.0 V Dropout
- Output Current in Excess of 800 mA
- Thermal Protection
- Short Circuit Protection
- Output Trimmed to 1.4% Tolerance
- No Minimum Load Required
- Space Saving DPAK and SOP–8 Surface Mount Power Packages

SCSI–2 ACTIVE TERMINATOR REGULATOR

SEMICONDUCTOR TECHNICAL DATA

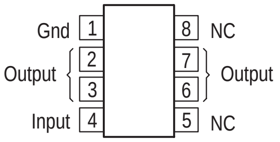


D SUFFIX
PLASTIC PACKAGE
CASE 751
(SOP–8)

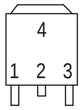


DT SUFFIX
PLASTIC PACKAGE
CASE 369A
(DPAK)

PIN CONNECTIONS



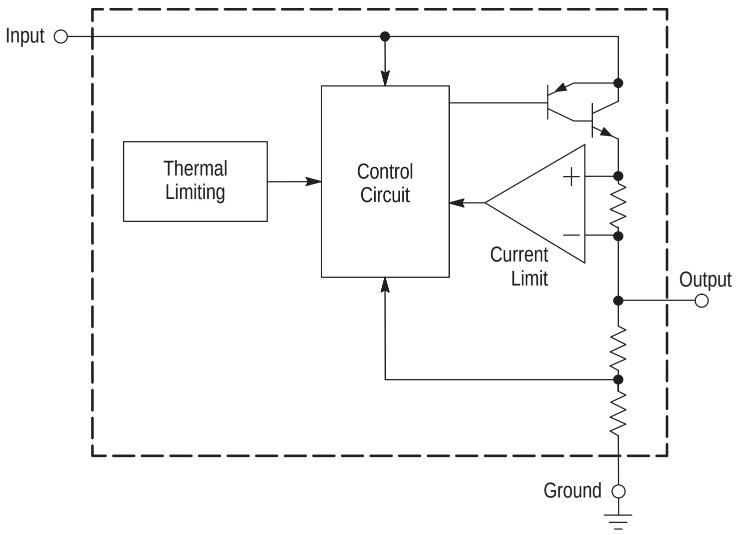
(Top View)



Pin 1. Ground
2. Output
3. Input
4. Output

(Top View)

Simplified Block Diagram



ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC34268D	T_J = 0° to +125°C	SOP–8
MC34268DT		DPAK

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Input Voltage	V_{in}	15	V
Power Dissipation and Thermal Characteristics DT Suffix, Plastic Package, Case 369A T_A = 25°C, Derate Above T_A = 25°C Thermal Resistance, Junction–to–Case Thermal Resistance, Junction–to–Air D Suffix, Plastic Package, Case 751 T_A = 25°C, Derate Above T_A = 25°C Thermal Resistance, Junction–to–Case Thermal Resistance, Junction–to–Air	 P_D $R_{\theta JC}$ $R_{\theta JA}$ P_D $R_{\theta JC}$ $R_{\theta JA}$	 Internally Limted 5.0 87 Internally Limited 22 140	 W °C/W °C/W W °C/W °C/W
Operating Junction Temperature Range	T_J	0 to +150	°C
Storage Temperature	T_{stg}	– 55 to +150	°C

ELECTRICAL CHARACTERISTICS

(V_{in} = 4.25 V, C_O = 10 µF, for typical values T_J = 25°C, for min/max values T_J = 0°C to +125°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = 25°C, I_O = 0 mA) Output Voltage, over Line, Load, and Temperature (V_{in} = 3.9 V to 15 V, I_O = 0 mA to 490 mA)	V_O	2.81 2.76	2.85 2.85	2.89 2.93	V
Line Regulation (V_{in} = 4.25 V to 15 V, I_O = 0 mA, T_J = 25°C)	Reg_{line}	—	—	0.3	%
Load Regulation (I_O = 0 mA to 800 mA, T_J = 25°C)	Reg_{load}	—	—	0.5	%
Dropout Voltage (I_O = 490 mA)	$V_{in} – V_O$	—	0.95	1.1	V
Ripple Rejection (f = 120 Hz)	RR	55	—	—	dB
Maximum Output Current (V_{in} = 5.0 V)	$I_{(max)}$	800	—	—	mA
Bias Current (V_{in} = 4.25 V, I_O = 0 mA)	I_B	—	5.0 to 3.0	8.0	mA
Minimum Load Current to maintain Regulation (V_{in} = 15 V)	$I_{L(min)}$	—	—	0	mA

Figure 1. Dropout Voltage versus Output Load Current

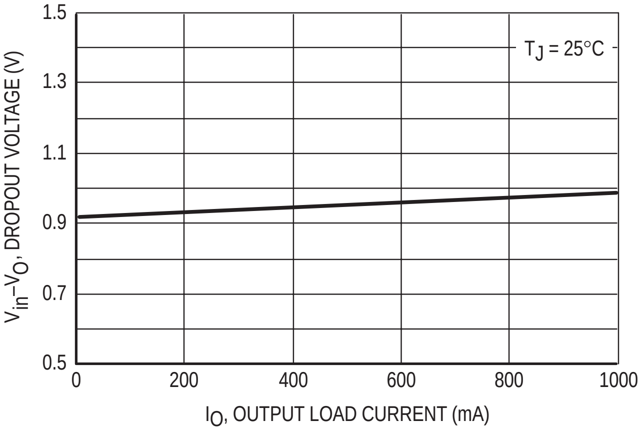


Figure 2. Transient Load Regulation

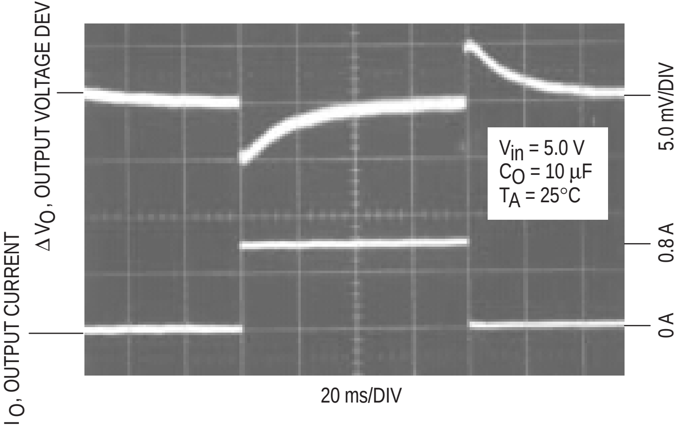


Figure 3. Typical SCSI Application

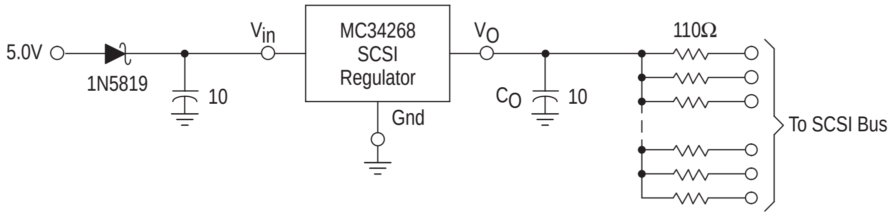


Figure 3 is a circuit of a typical SCSI terminator application. The MC34268 is designed specifically to provide 2.85 V required to drive a SCSI–2 bus. The output current capability of the regulator is in excess of 800 mA; enough to drive standard SCSI–2, fast SCSI–2, and some wide SCSI–2 applications. The typical dropout voltage is less than 1.0 V, allowing the IC to regulate to input voltages less than 4.0 V. Internal protective features include current and thermal limiting.

The MC34268 requires an external 10 μF capacitor with an ESR of less than 10 Ω for stability over temperature. With economical electrolytic capacitors, cold temperature operation can pose a stability problem. As temperature decreases, the capacitance also decreases and the ESR increases, which could cause the circuit to oscillate. Tantalum capacitors may be a better choice if small size is a requirement. Also, the capacitance and ESR of a tantalum capacitor is more stable over temperature.

Figure 4. SOP–8 Thermal Resistance versus P.C.B. Copper Length

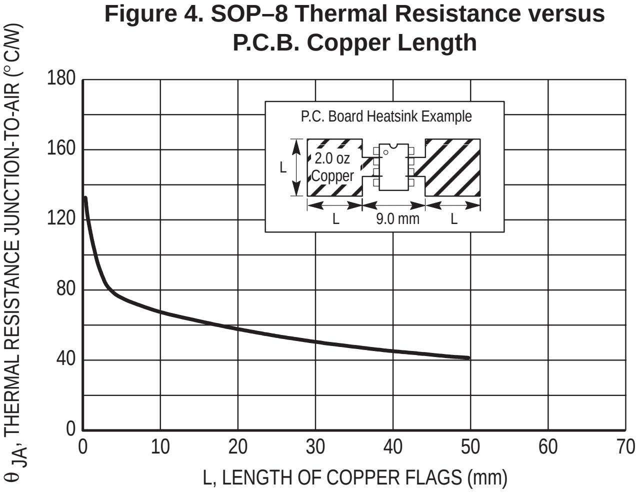
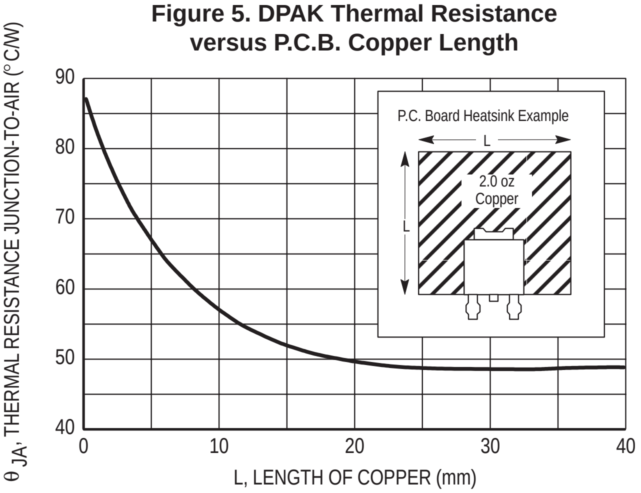


Figure 5. DPAK Thermal Resistance versus P.C.B. Copper Length



MOTOROLA

MC34270
MC34271

Liquid Crystal Display and Backlight Integrated Controller

The MC34270 and MC34271 are low power dual switching voltage regulators, specifically designed for handheld and laptop applications, to provide several regulated output voltages using a minimum of external parts. Two uncommitted switching regulators feature a very low standby bias current of 5.0 µA, and an operating current of 7.0 mA capable of supplying output currents in excess of 200 mA.

Both devices have three additional features. The first is an ELD Output that can be used to drive a backlight or a liquid crystal display. The ELD output frequency is the clock divided by 256. The second feature allows four additional output bias voltages, in specific proportions to V_B, one of the switching regulated output voltages. It allows use of mixed logic circuitry and provides a voltage bias for N–Channel load control MOSFETs™. The third feature is an Enable input that allows a logic level signal to turn–“off” or turn–“on” both switching regulators.

Due to the low bias current specifications, these devices are ideally suited for battery powered computer, consumer, and industrial equipment where an extension of useful battery life is desirable.

MC34270 and MC34271 Features:

- Low Standby Bias Current of 5.0 µA
- Uncommitted Switching Regulators Allow Both Positive and Negative Supply Voltages
- Logic Enable Allows Microprocessor Control of All Outputs
- Synchronizable to External Clock
- Mode Commandable for ELD and LCD Interface
- Frequency Synchronizable
- Auxiliary Output Bias Voltages Enable Load Control via N–Channel FETs

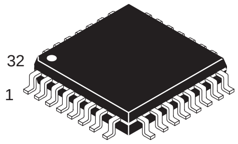
MOSFET is a trademark of Motorola, Inc.

MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted.)

Rating	Symbol	Value	Unit
Input Voltage	V_{DD}	16	Vdc
Power Dissipation and Thermal Characteristics			
Maximum Power Dissipation	P_D	1.43	W
Case 873			
Thermal Resistance, Junction–to–Ambient	$R_{\theta JA}$	100	°C/W
Thermal Resistance, Junction–to–Case	$R_{\theta JC}$	60	°C/W
Output #1 and #2 Switch Current	I_{SL} & I_{SB}	500	mA
Output #1 and #2 “Off”–State Voltage	V_{SL}	60	Vdc
Feedback Enable MOSFETs “Off”–State Voltage	V_{LF}	20	Vdc
Operating Junction Temperature	T_J	125	°C
Operating Ambient Temperature	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	–55 to +150	°C

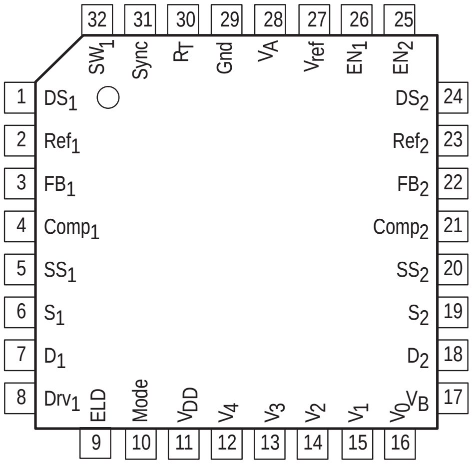
LIQUID CRYSTAL DISPLAY AND BACKLIGHT INTEGRATED CONTROLLER

SEMICONDUCTOR TECHNICAL DATA



FB SUFFIX
PLASTIC PACKAGE
CASE 873

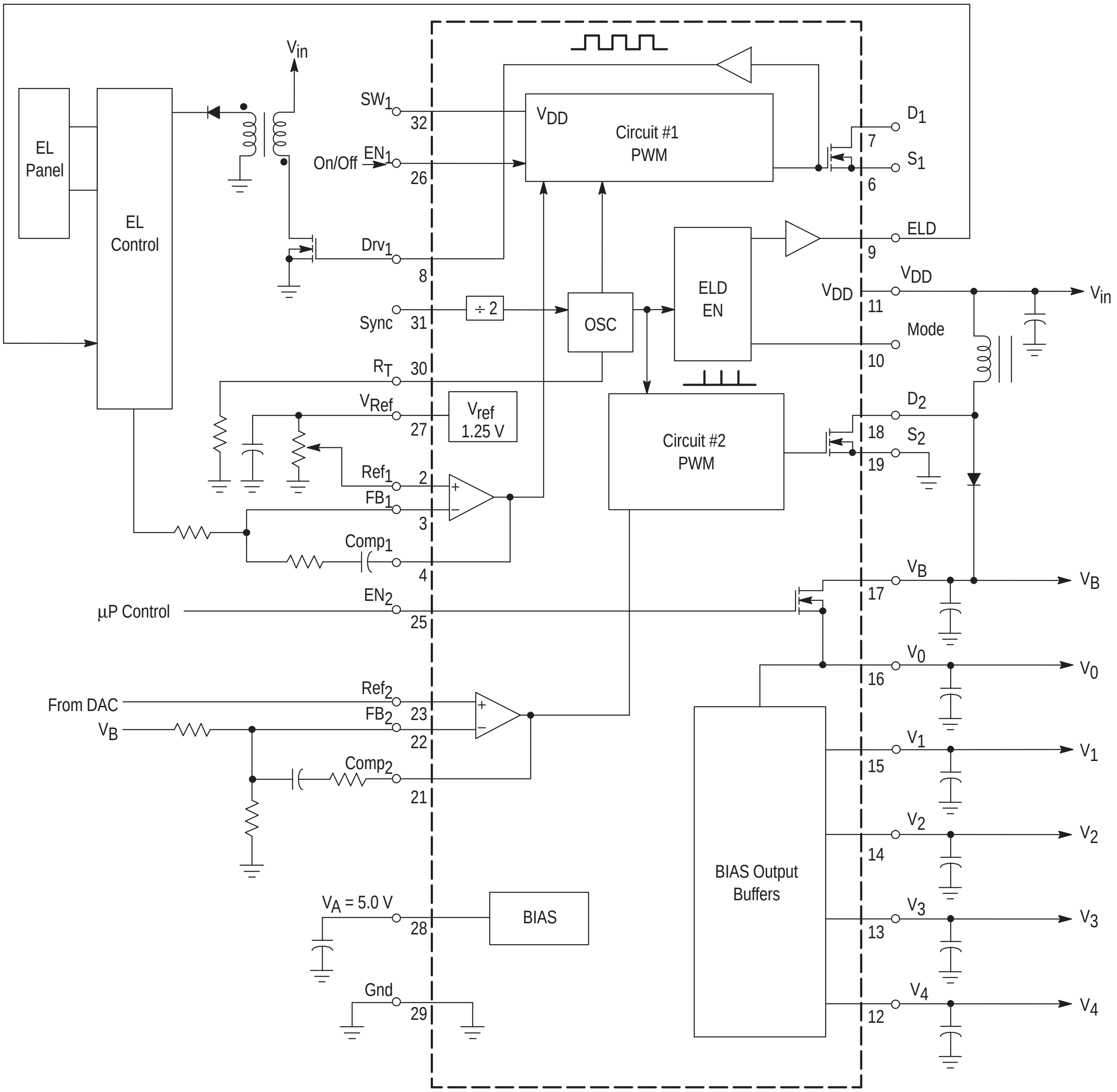
PIN CONNECTIONS



ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC34270FB	T_A = 0° to +70°C	QFP–32
MC34271FB		QFP–32

Representative Block Diagram



This device contains 350 active transistors.

ELECTRICAL CHARACTERISTICS (V_{DD} = 6.0 V, for typical values T_A = Low to High [Note 1], for min/max values T_A is the operating ambient temperature range that applies, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
REFERENCE SECTION					
Reference Voltage (T_J = 25°C)	V_{ref}	1.225	1.250	1.275	V
Line Regulation (V_{DD} = 5.0 V to 12.5 V)	Reg_{line}	–	2.0	10	mV
Load Regulation (I_O = 0 to 120 µA)	Reg_{load}	–	2.0	10	mV
Total Variation (Line, Load and Temperature)	V_{ref}	1.215	–	1.285	V
ERROR AMPLIFIERS					
Input Offset Voltage (V_{CM} = 1.25 V)	V_{IO}	–	1.0	10	mV
Input Bias Current (V_{CM} = 1.25 V)	I_{IB}	–	120	600	nA
Open Loop Voltage Gain (V_{CM} = 1.25 V, V_{COMP} = 2.0 V)	A_{VOL}	80	100	–	dB
Output Voltage Swing					V
High State (I_{OH} = –100 µA)	Ve_{OH}	V_A–1.5	4.0	5.5	
Low State (I_{OL} = 100 µA)	Ve_{OL}	0	–	1.0	
BIAS VOLTAGE					
Voltage (V_{DD} = 5.0 V to 12.5 V, I_O = 0)	V_A	4.6	5.0	5.4	V
OSCILLATOR AND PWM SECTIONS					
Total Frequency Variation Over Line and Temperature	f_{OSC}				kHz
V_{DD} = 5.0 V to 10 V, T_A = 0° to 70°C, R_T = 169 k		90	115	140	
Duty Cycle at Each Output					%
Maximum	DC_{max}	92	95	–	
Minimum	DC_{min}	–	–	0	
Sync Input					
Input Resistance (V_{sync} = 3.5 V)	R_{sync}	25	50	100	kΩ
Minimum Sync Pulse Width	T_p	–	1.0	–	µs
OUTPUT MOSFETs					
Output Voltage – "On"–State (I_{sink} = 200 mA)	V_{OL}	–	150	250	mV
Output Current – "Off"–State (V_{OH} = 40 V)	I_{OH}	–	0.1	1.0	µA
Rise and Fall Times	t_r, t_f	–	50	–	ns
EL DISCHARGE OUTPUT (ELD) AND DRV_1					
Output Voltage – "On"–State (I_{sink} = 100 µA)	V_{OL}	–	30	100	mV
Output Voltage – "On"–State (I_{sink} = 50 mA)	V_{OL}	–	2.0	2.5	V
Output Voltage – "Off"–State (I_{source} = –100 µA)	V_{OH}	V_{DD}–0.5	5.9	–	V
Output Voltage – "Off"–State (I_{source} = –50 mA)	V_{OH}	V_{DD}–3.5	3.3	–	V
FEEDBACK ENABLE SWITCHES (DS_1, DS_2)					
Output Voltage – "Low"–State (I_{sink} = 1.0 mA)	Vfe_{OL}	–	10	100	mV
Output Current – "Off"–State (V_{OH} = 12.5 V)	Ife_{OH}	–	0.6	1.0	µA
SWITCHED V_{DD} OUTPUT (SW_1)					
Output Voltage					V
Switch "On" (EN_1 = 1, I_{source} = 100 µA)	Vsw_{OH}	5.5	5.9	6.0	
Switch "Off" (EN_1 = 0, I_{sink} = 100 µA)	Vsw_{OL}	0	0.1	0.2	
AUXILIARY VOLTAGE OUTPUTS					
V_0 Enable Switch					
"On"–Resistance: V_B to V_0	Rds	0	2.0	10	Ω
"Off"–State Leakage Current (V_B = 10 V)	I_{lkg}	0	0.1	2.0	µA
V_0 Voltage (V_B = 30 V, I_{source} = 0 mA)	V_0	29.5	29.9	30	V
V_0 Resistance (I_{source} = 4.0 mA)	R_0	20	40	60	Ω

NOTE: 1. Low duty pulse techniques are used during test to maintain junction temperature as close to ambient as possible.

ELECTRICAL CHARACTERISTICS (continued) (V_{DD} = 6.0 V, for typical values T_A = Low to High [Note 1], for min/max values T_A is the operating ambient temperature range that applies, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
AUXILIARY VOLTAGE OUTPUTS					
V_1, V_2, V_3, V_4 Outputs					
$1–V_1/V_0$ Ratio: MC34270		0.0565	0.0580	0.0595	
MC34271		0.0500	0.0520	0.0535	
$1–V_2/V_0$ Ratio: MC34270		0.1135	0.1160	0.1185	
MC34271		0.1010	0.1035	0.1065	
V_3/V_0 Ratio: MC34270		0.1135	0.1160	0.1185	
MC34271		0.1010	0.1035	0.1065	
V_4/V_0 Ratio: MC34270		0.0565	0.0580	0.0595	
MC34271		0.0500	0.0520	0.0535	
Output Resistance (I_{source} = 4.0 mA)	R_o	20	40	60	Ω
Output Short Circuit Current	I_{SS}	5.0	10	20	mA
LOGIC INPUTS (EN_1, EN_2, MODE)					
Input Low State	V_{IL}	0	–	0.8	V
Input High State	V_{IH}	2.0	–	6.0	V
Input Impedance	R_{in}	25	50	100	kΩ
SOFT START CONTROL (SS_1,SS_2)					
Charge Current (Capacitor Voltage = 1.0 V to 4.0 V)	I_{chg}	0.5	1.0	2.5	µA
Discharge Current (Capacitor Voltage = 1.0 V)	I_{dschg}	250	650	–	µA
TOTAL SUPPLY CURRENT					
V_{DD} Current Standby Mode (EN_1 = EN_2 = 0) V_{DD} = 6.0 V	I_{CC}	–	2.0	5.0	µA
V_{DD} = 16 V		–	3.0	15	
V_{DD} Current Backlight "On" (EN_1 = 1; EN_2 = 0)	I_{CC}	–	0.7	3.0	mA
V_{DD} Current LCD "On" (No Inductor) (EN_1 = 0; EN_2 = 1)	I_{CC}	–	0.9	2.0	mA
V_B Current (V_0 = 35 V)	I_O	–	1.2	3.0	mA

NOTE: 1. Low duty pulse techniques are used during test to maintain junction temperature as close to ambient as possible.

Figure 1. Switch Output Duty Cycle versus Compensation Voltage

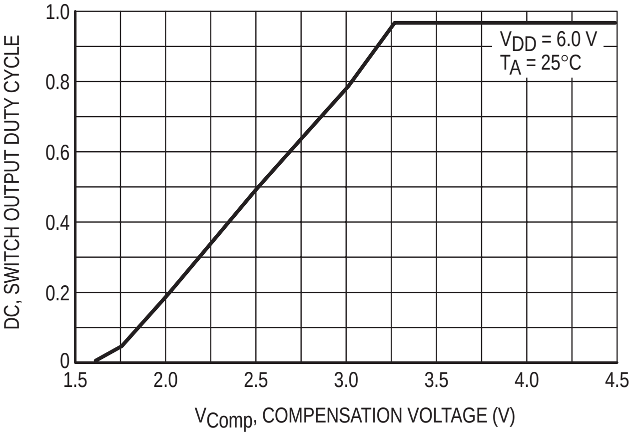


Figure 2. Error Amp Open Loop Gain and Phase versus Frequency

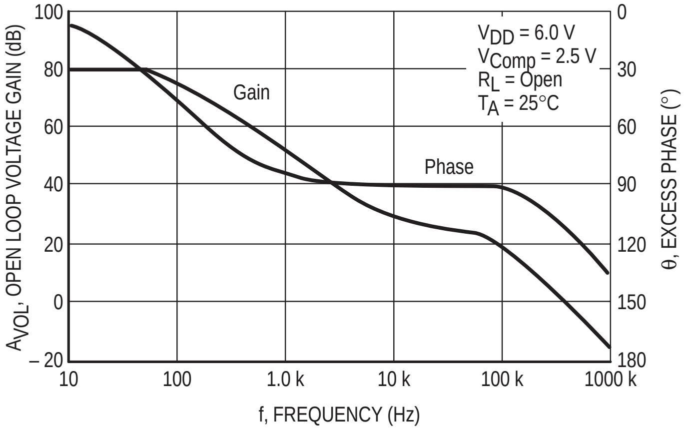


Figure 3. Reference Voltage Change versus Reference Current

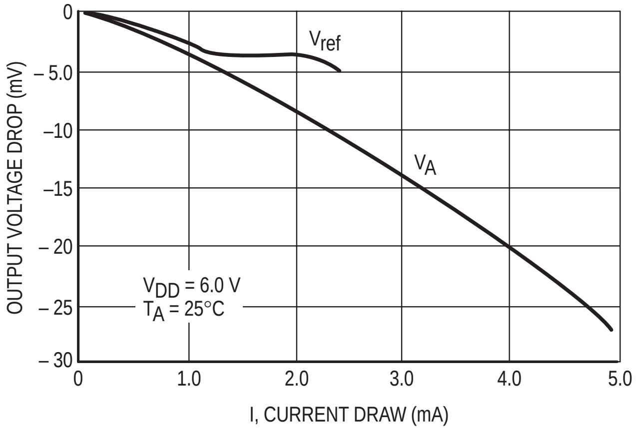


Figure 4. Quiescent Current versus Supply Voltage

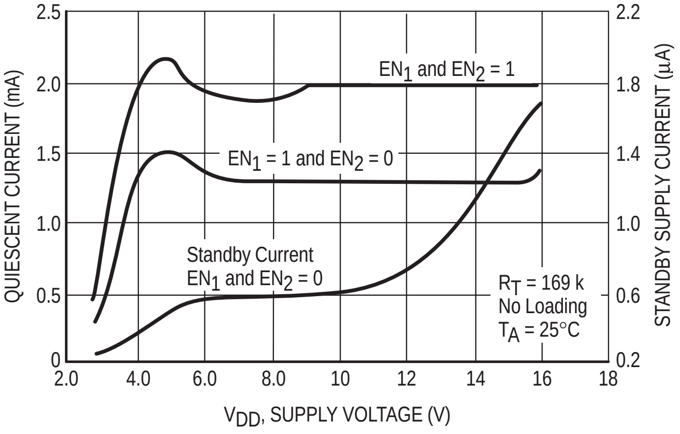


Figure 5. FET Drain Voltage versus Sink Current

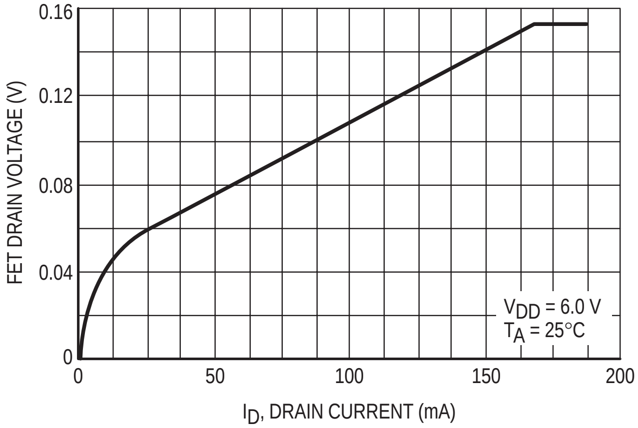


Figure 6. ELD and DRV1 Switch Output Source and Sink Saturation versus Current

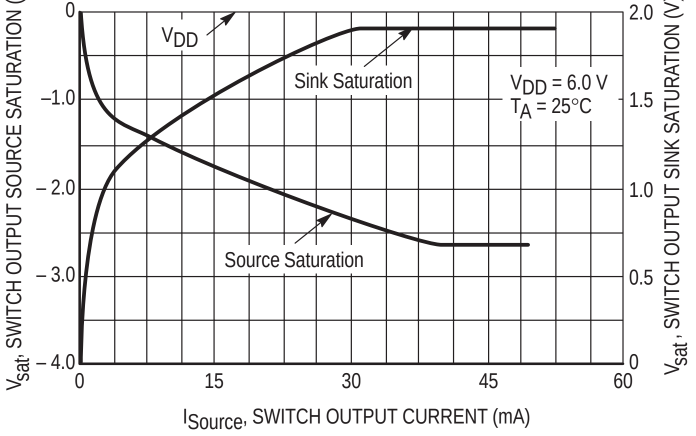


Figure 7. V_{ref} and V_A Variation versus Temperature

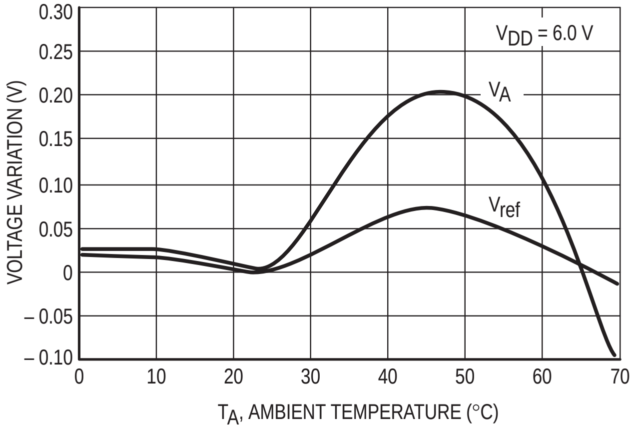


Figure 8. Oscillator Frequency Variation versus Temperature

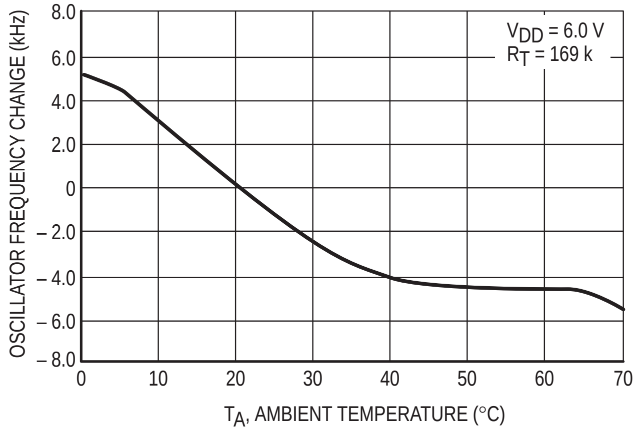


Figure 9. Frequency versus Timing

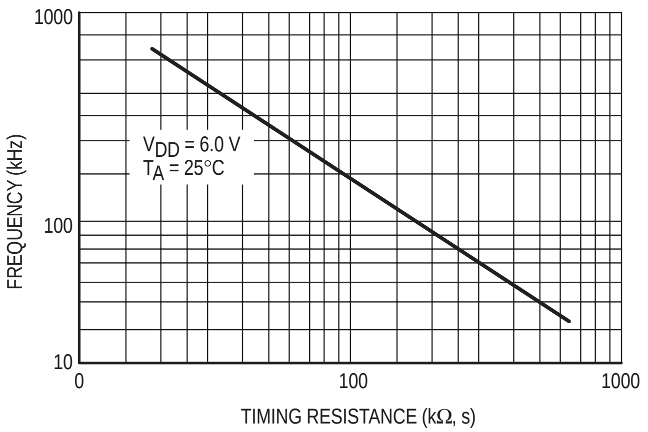
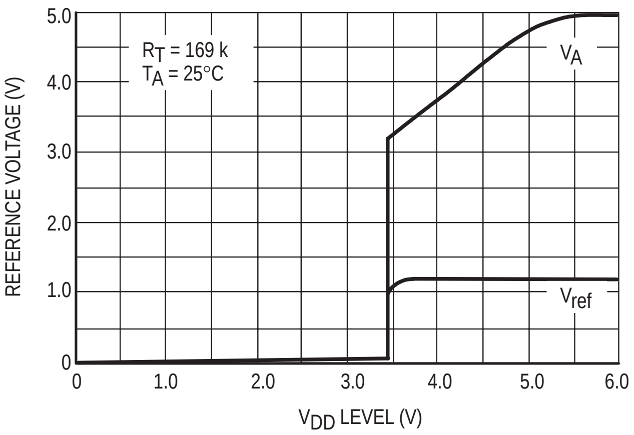


Figure 10. V_A, V_{ref} versus V_{DD}



OPERATING DESCRIPTION

The MC34270 and MC34271 series are monolithic, fixed frequency power switching regulators specifically designed for dc to dc converter and battery powered applications. These devices operate as fixed frequency, voltage mode regulators containing all the active functions required to directly implement step–up, step–down and voltage inverting converters with a minimum number of external components. Potential markets include battery powered, handheld, automotive, computer, industrial and cost sensitive consumer products. A description of each section is given below with the representative block diagram shown in Figure 9.

Oscillator

The oscillator frequency is programmed by resistor R_T. The charge to discharge ratio is controlled to yield a 95% maximum duty cycle at the switch outputs. During the fall time of the internal sawtooth waveform, the oscillator generates an internal blanking pulse that holds the inverting input of the AND gates high, disabling the output switching MOSFETs. The internal sawtooth waveform has a nominal peak voltage of 3.3 V and a valley voltage of 1.7 V.

Pulse Width Modulators

Both pulse width modulators consist of a comparator with the oscillator ramp voltage applied to the noninverting input, while the error amplifier output is applied to the inverting input. A third input to the comparator has a 0.5 mA typical current source that can be used to implement soft start. Output switch conduction is initiated when the ramp waveform is discharged to the valley voltage. As the ramp voltage increases to a voltage that exceeds the error amplifier output, the latch resets, terminating output MOSFET conduction for the duration of the oscillator ramp. This PWM/latch combination prevents multiple output pulses during a given oscillator cycle.

Each PWM circuit is enabled by a logic input. When disabled, the entire block is turned off, drawing only leakage current from the power source. Shared circuits, like the reference and oscillator, can be activated by either EN_1 or EN_2.

Circuit #1 has an ELD output which may be used to drive an LCD or backlight. Its output frequency is the oscillator frequency divided by 1024.

Error Amplifiers and Reference

Each error amplifier is provided with access to both inverting and noninverting inputs, and the output. The Error Amplifiers’ Common Mode Input Range is 0 to 2.5 V. The amplifiers have a minimum dc voltage gain of 60 dB. The 1.25 V reference has an accuracy of ±4.0% at room temperature.

External loop compensation is required for converter stability. A simple low–pass filter is formed by connecting a resistive divider from the output to the error amplifier inverting input, and a series resistor–capacitor from the error amplifier output also to the to the inverting input. The step down converter is easiest to compensate for stability. The step–up and voltage inverting configurations, when operated as continuous conduction boost or flyback converters, are more difficult to compensate, and may require a lower loop design bandwidth.

MOSFET Switch Outputs

The output MOSFETs are designed to switch a maximum of 60 V, with a peak drain current capability of 500 mA. In circuit #1 an additional DRV_1 output is provided for interfacing with an external MOSFET.The gates of the MOSFETs are held low when the circuit is disabled.

Auxiliary Output Voltages

Output voltages V_0 through V_4 are provided for use as references or bias voltages. V_0 is the circuit #2 output voltage, when an internal FET switch is activated. The other auxiliary output voltages are proportional to V_B. The amplifiers for V_1 and V_2 are powered from V_0, while the amplifiers for V_3 and V_4 are powered from V_{DD}.

Figure 11. Representative Block Diagram Electroluminescent Backlight Configuration

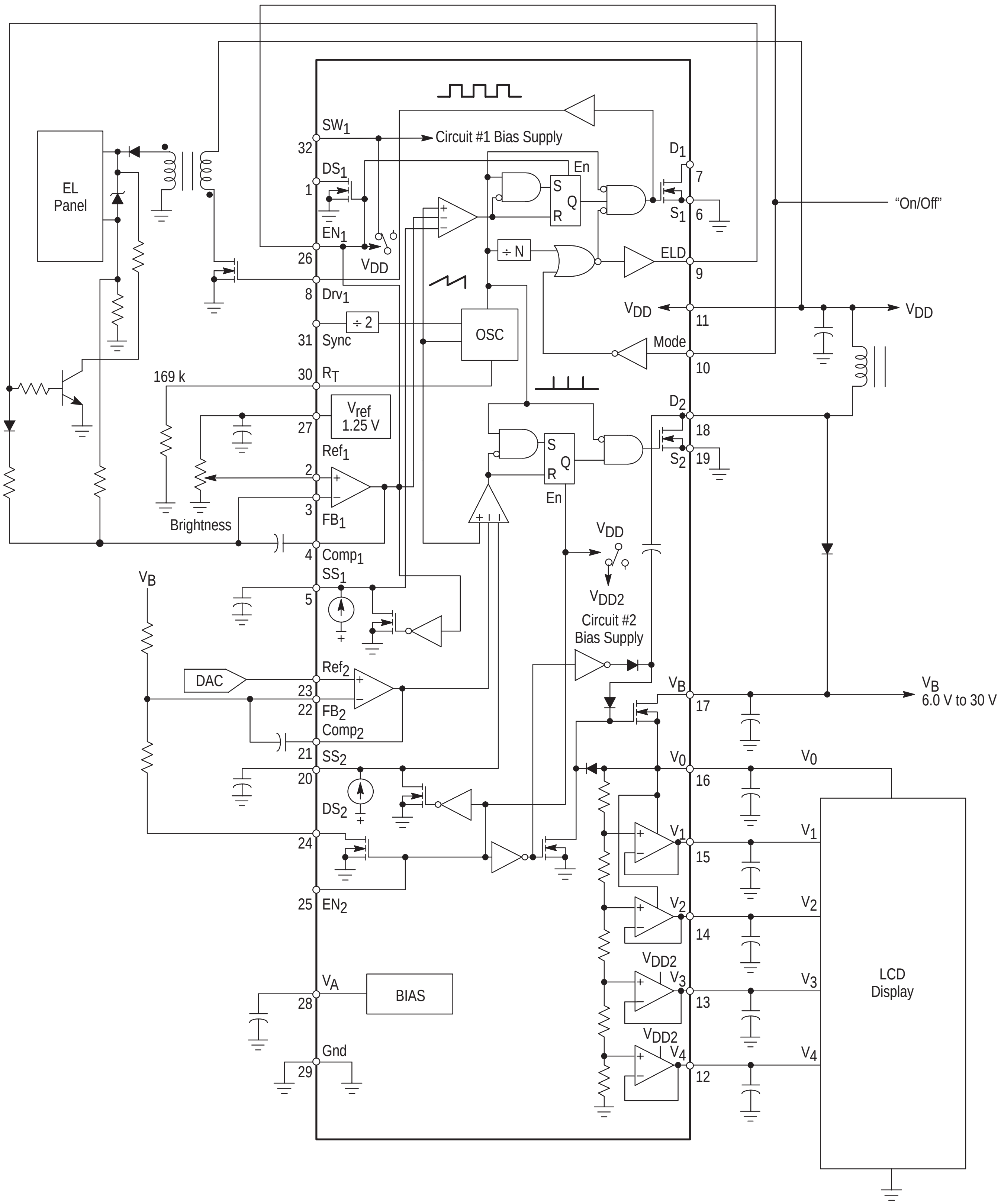


Figure 12. Auxiliary Supply Configuration

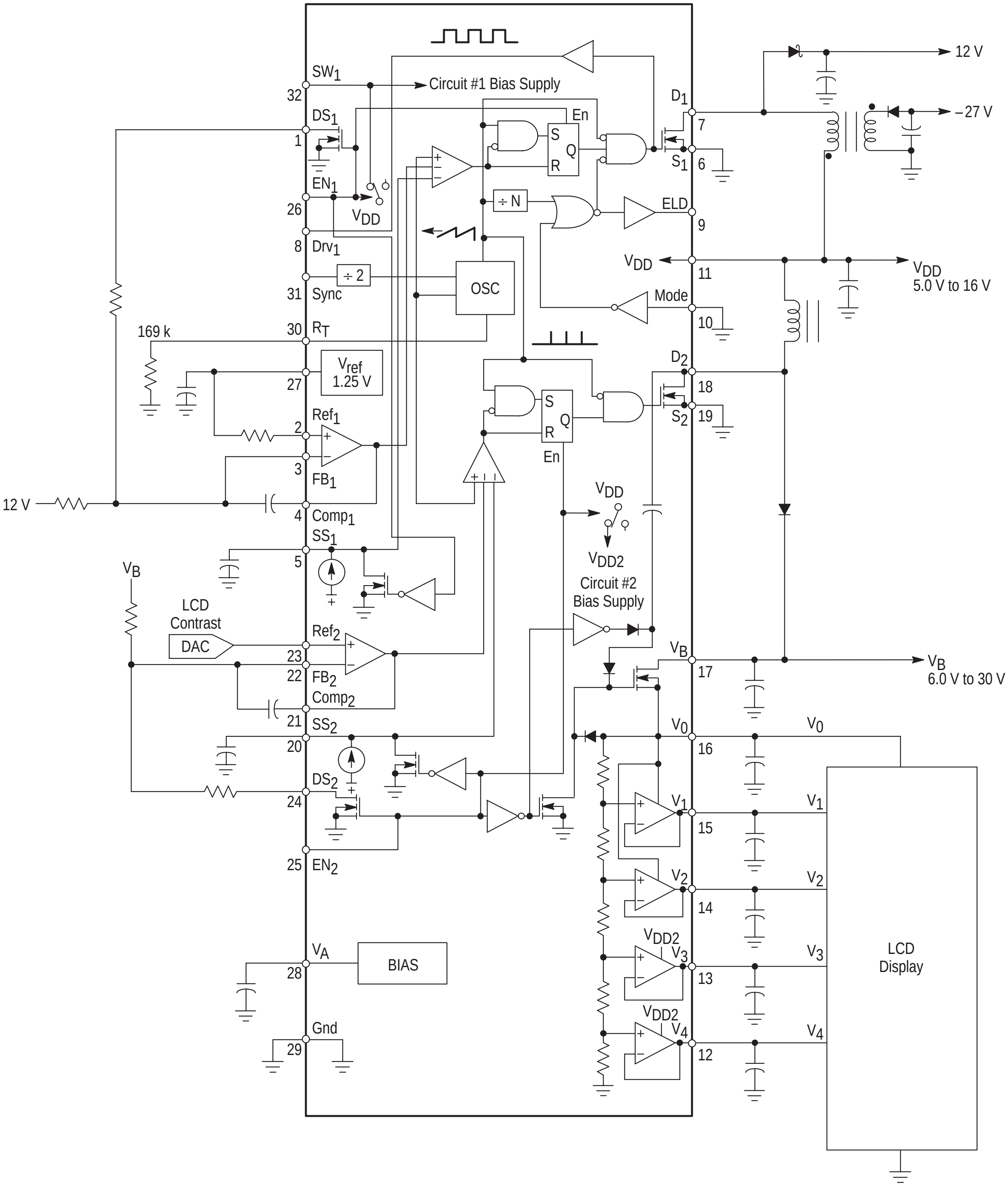


Figure 13. MC34270 Incandescent Backlight Configuration

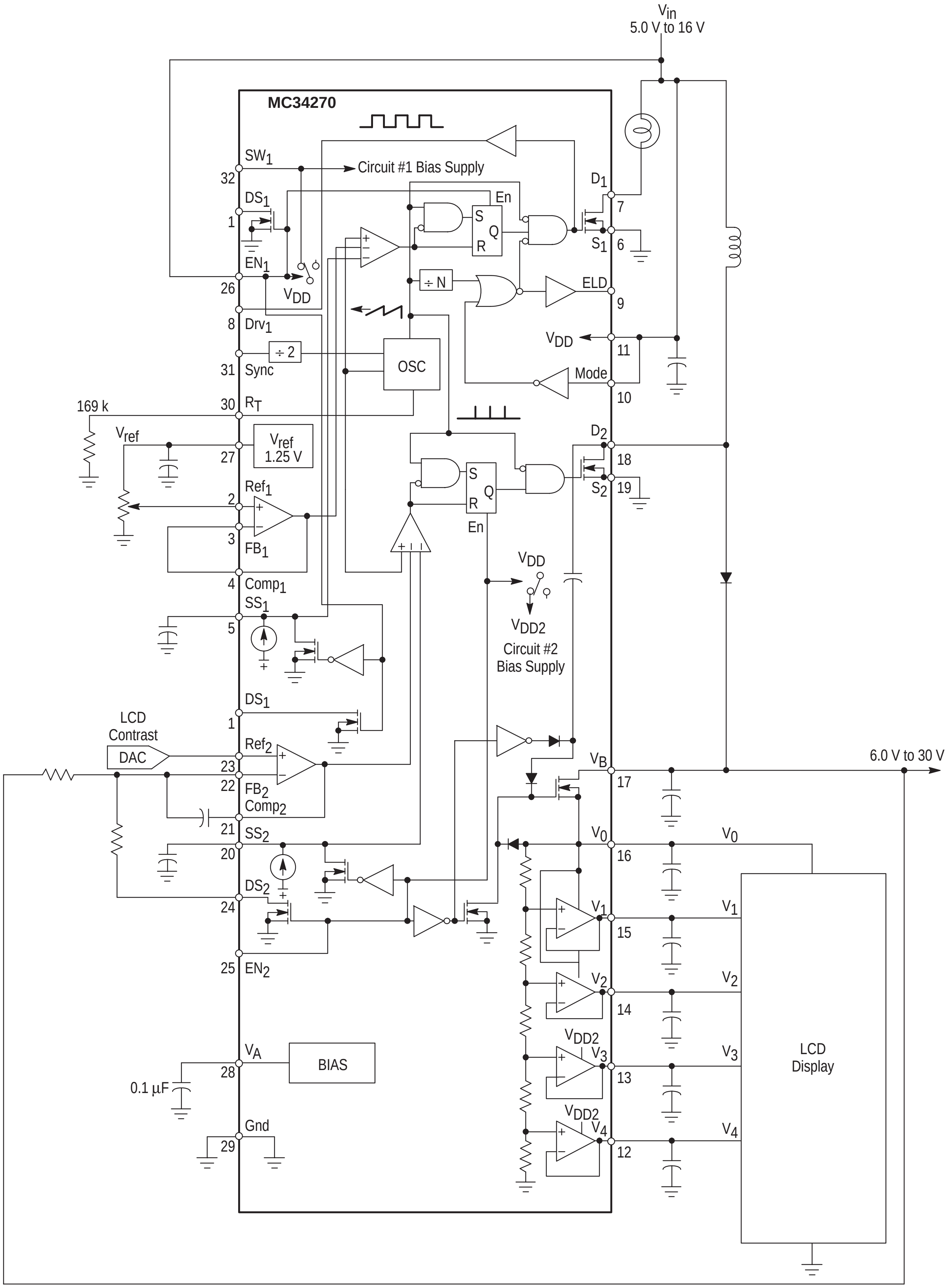
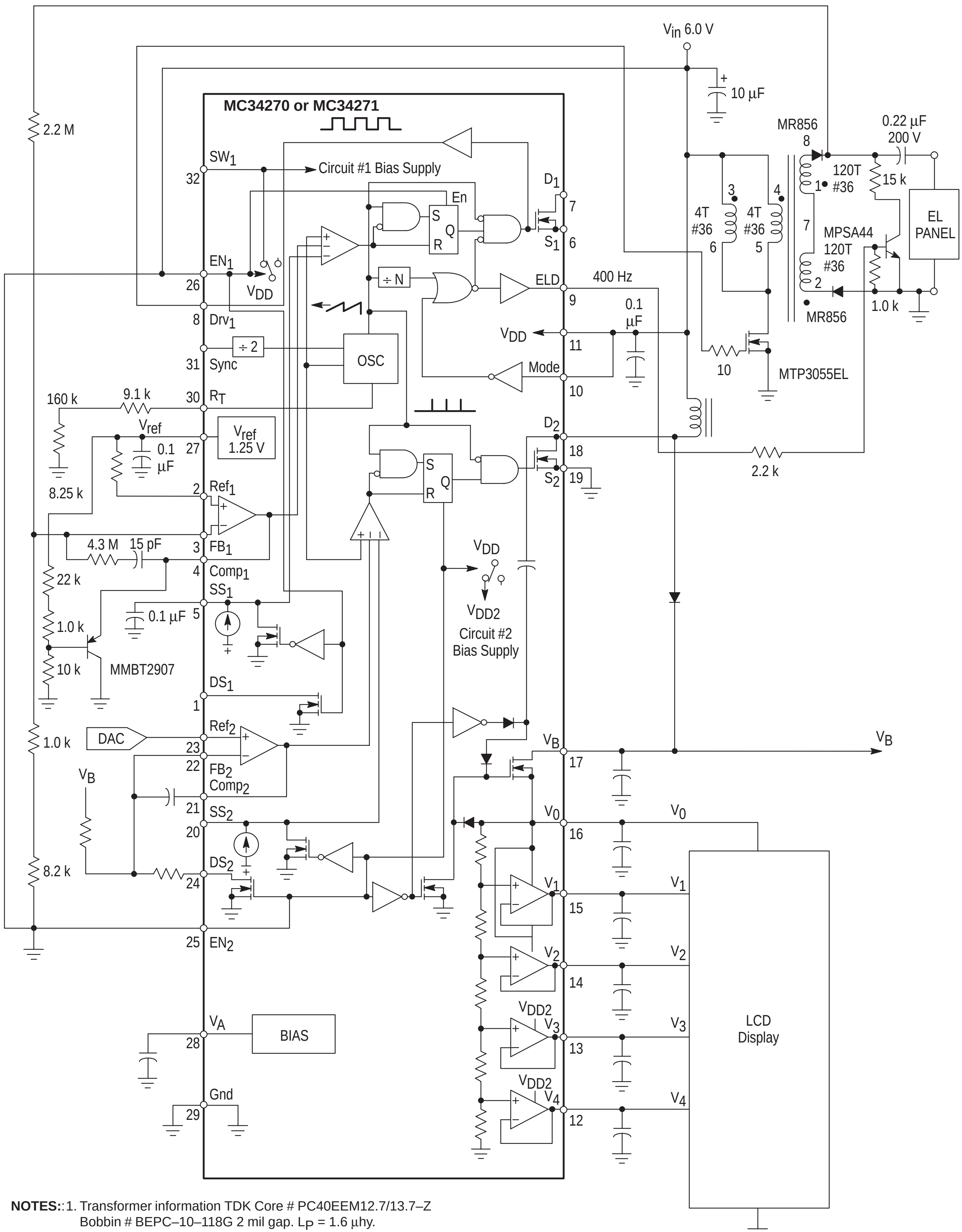


Figure 14. EL PANEL Drive Circuit



NOTES:: 1. Transformer information TDK Core # PC40EEM12.7/13.7–Z
Bobbin # BEPC–10–118G 2 mil gap. L_P = 1.6 µhy.
2. EL PANEL: DUREL™ 3/SL ORANGE

MOTOROLA

MC44602

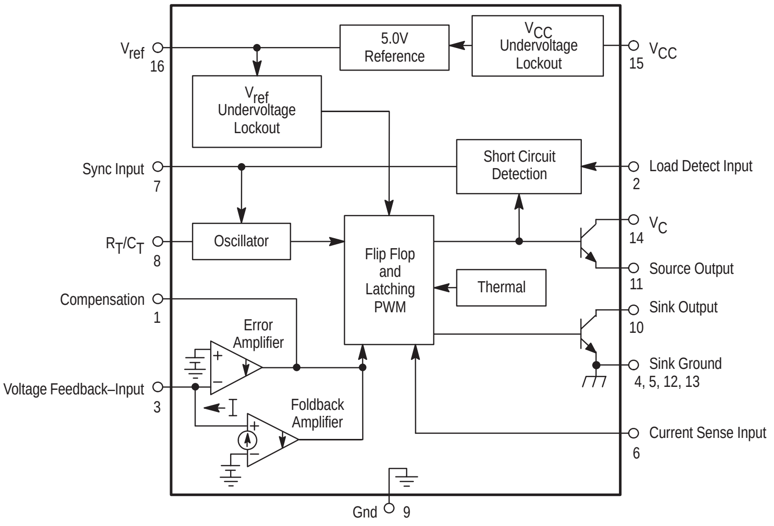
High Performance Current Mode Controller

The MC44602 is an enhanced high performance fixed frequency current mode controller that is specifically designed for off–line and high voltage dc–to–dc converter applications. This device has the unique ability of changing operating modes if the converter output is overloaded or shorted, offering the designer additional protection for increased system reliability. The MC44602 has several distinguishing features when compared to conventional current mode controllers. These features consist of a foldback amplifier for overload detection, valid load and demag comparators with a fault latch for short circuit detection, thermal shutdown, and separate high current source and sink outputs that are ideally suited for driving a high voltage bipolar power transistor, such as the MJE18002, MJE18004, or MJE18006.

Standard features include an oscillator with a sync input, a temperature compensated reference, high gain error amplifier, and a current sensing comparator. Protective features consist of input and reference undervoltage lockouts each with hysteresis, cycle–by–cycle current limiting, a latch for single pulse metering, and a flip–flop which blanks the output off every other oscillator cycle, allowing output deadtimes to be programmed from 50% to 70%. This device is manufactured in a 16 pin dual–in–line heat tab package for improved thermal conduction.

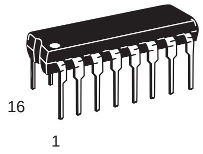
- Separate High Current Source and Sink Outputs Ideally Suited for Driving Bipolar Power Transistors: 1.0 A Source, 1.5 A Sink
- Unique Overload and Short Circuit Protection
- Thermal Protection
- Oscillator with Sync Input
- Current Mode Operation to 500 kHz Output Switching Frequency
- Output Deadtime Adjustable from 50% to 70%
- Automatic Feed Forward Compensation
- Latching PWM for Cycle–By–Cycle Current Limiting
- Input and Reference Undervoltage Lockouts with Hysteresis
- Low Startup and Operating Current

Simplified Block Diagram



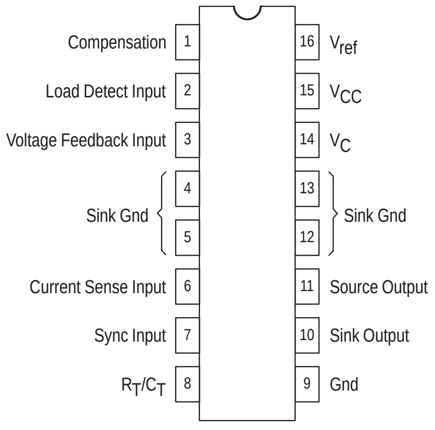
HIGH PERFORMANCE CURRENT MODE CONTROLLER

SEMICONDUCTOR TECHNICAL DATA



P2 SUFFIX
PLASTIC PACKAGE
CASE 648C
DIP (12 + 2 + 2)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC44602	T_A = –25 to 85°C	DIP (12 + 2 + 2)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Total Power Supply and Zener Current	$(I_{CC} + I_Z)$	30	mA
Sink Ground Voltage with Respect to Gnd (Pin 9)	$V_{Sink(neg)}$	–5.0	V
Output Supply Voltage with Respect to Sink Gnd (Pins 4, 5, 12, 13)	V_C	20	V
Output Current (Note 1)			A
Source	$I_{O(Source)}$	1.0	
Sink	$I_{O(Sink)}$	1.5	
Output Energy (Capacitive Load per Cycle)	W	5.0	µJ
Current Sense and Voltage Feedback Inputs	V_{in}	–0.3 to 5.5	V
Sync Input			
High State Voltage	V_{IH}	5.5	V
Low State Reverse Current	I_{IL}	–20	mA
Load Detect Input Current	I_{in}	–20 to +10	mA
Error Amplifier Output Sink Current	$I_{EA\ (Sink)}$	10	mA
Power Dissipation and Thermal Characteristics			
Maximum Power Dissipation at T_A = 25°C	P_D	2.5	W
Thermal Resistance, Junction–to–Air	$R_{\theta JA}$	80	°C/W
Thermal Resistance, Junction–to–Case	$R_{\theta JC}$	15	°C/W
Operating Junction Temperature	T_J	150	°C
Operating Ambient Temperature	T_A	–25 to +85	°C

NOTE: 1. Maximum package power dissipation limits must be observed.

ELECTRICAL CHARACTERISTICS (V_{CC} and V_C = 12 V [Note 2], R_T = 10k, C_T = 1.0 nF, for typical values T_A = 25°C, for min/max values T_A = –25°C to +85°C [Note 3] unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
ERROR AMPLIFIER SECTION					
Voltage Feedback Input (V_O = 2.5V)	V_{FB}	2.45	2.5	2.65	V
Input Bias Current (V_{FB} = 2.5 V)	I_{IB}	–	–0.6	–2.0	µA
Open Loop Voltage Gain (V_O = 2.0 V to 4.0 V)	A_{VOL}	65	90	–	dB
Unity Gain Bandwidth	BW				MHz
T_J = 25°C		1.0	1.4	1.8	
T_A = –25 to +85°C		0.8	–	2.0	
Power Supply Rejection Ratio (V_{CC} = 10 V to 16 V)	PSRR	65	70	–	dB
Output Current					mA
Sink (V_O = 1.5 V, V_{FB} = 2.7 V)	I_{Sink}				
T_J = 25°C		–	5.0	–	
T_A = –25 to +85°C		1.5	–	10	
Source (V_O = 5.0 V, V_{FB} = 2.3 V)	I_{Source}				
T_J = 25°C		–	–1.1	–	
T_A = –25 to +85°C		–2.0	–	–0.2	
Output Voltage Swing					V
High State ($I_{O(Source)}$ = 0.5 mA, V_{FB} = 2.3 V)	V_{OH}	6.0	7.0	–	
Low State ($I_{O(Sink)}$ = 0.33 mA, V_{FB} = 2.7 V)	V_{OL}	–	1.0	1.1	

NOTES: 2. Adjust V_{CC} above the startup threshold before setting to 12V.
3. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.

ELECTRICAL CHARACTERISTICS (V_{CC} and V_C = 12 V [Note 2], R_T = 10k, C_T = 1.0 nF, for typical values T_A = 25°C, for min/max values T_A = –25°C to +85°C [Note 3] unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OSCILLATOR SECTION					
Frequency	f_{OSC}				kHz
T_J = 25°C		168	180	192	
T_A = –25°C to +85°C		160	–	200	
Frequency Change with Voltage (V_{CC} = 12 V to 18 V)	$\Delta f_{OSC}/\Delta V$	–	0.1	0.2	%/V
Frequency Change with Temperature	$\Delta f_{OSC}/\Delta T$	–	0.05	–	%/°C
Oscillator Voltage Swing (Peak–to–Peak)	$V_{OSC(pp)}$	1.3	1.6	–	V
Discharge Current (V_{OSC} = 3.0 V)	I_{dischg}				mA
T_J = 25°C		6.5	10	13.5	
T_A = –25°C to +85°C		6.0	–	14	
Sync Input Threshold Voltage					V
High State	V_{IH}	2.5	2.8	3.2	
Low State	V_{IL}	1.0	1.3	1.7	
Sync Input Resistance	R_{in}				kΩ
T_J = 25°C		6.5	10	13.5	
T_A = –25°C to +85°C		6.0	–	18	
REFERENCE SECTION					
Reference Output Voltage (I_O = 1.0 mA)	V_{ref}	4.7	5.0	5.3	V
Line Regulation (V_{CC} = 12 V to 18 V)	Reg_{line}	–	1.0	10	mV
Load Regulation (I_O = 1.0 mA to 20 mA)	Reg_{load}	–	3.0	15	mV
Temperature Stability	T_S	–	0.2	–	mV/°C
Total Output Variation over Line, Load and Temperature	V_{ref}	4.65	–	5.35	V
Output Noise Voltage (f = 10 Hz to 10 kHz, T_J = 25°C)	V_n	–	50	–	µV
Long Term Stability (T_A = 125°C for 1000 Hours)	S	–	5.0	–	mV
Output Short Circuit Current	I_{SC}				mA
T_J = 25°C		–	–130	–	
T_A = –25°C to +85°C		–70	–	–180	
CURRENT SENSE SECTION					
Current Sense Input Voltage Gain (Notes 4 & 5)	A_V				V/V
T_J = 25°C		2.85	3.0	3.15	
T_A = –25°C to +85°C		2.7	–	3.2	
Maximum Current Sense Input Threshold (Note 4)	V_{th}	0.9	1.0	1.1	V
Input Bias Current	I_{IB}	–	–4.0	–10	µA
Propagation Delay (Current Sense Input to Sink Output)	$t_{PLH(in/out)}$	–	100	150	ns
UNDERVOLTAGE LOCKOUT SECTIONS					
Startup Threshold (V_{CC} Increasing)	V_{th}	13	14.1	15	V
Minimum Operating Voltage After Turn–On (V_{CC} Decreasing)	$V_{CC(min)}$	9.0	10.2	11	V
Reference Undervoltage Threshold (V_{ref} Decreasing)	$V_{ref(UVLO)}$	3.0	3.35	3.7	V

NOTES: 2. Adjust V_{CC} above the startup threshold before setting to 12V.
3. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
4. This parameter is measured at the latch trip point with I_{FB} = –5.0 µA, refer to Figure 9.
5. Comparator gain is defined as $A_V = \frac{\Delta V \text{ Compensation}}{\Delta V \text{ Current Sense Input}}$

ELECTRICAL CHARACTERISTICS (V_{CC} and V_C = 12 V [Note 2], R_T = 10k, C_T = 1.0 nF, for typical values T_A = 25°C, for min/max values T_A = –25°C to +85°C [Note 3] unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OUTPUT SECTION					
Output Voltage (T_A = 25°C)					V
Low State (I_{Sink} = 100 mA)	V_{OL}	–	0.6	0.3	
(I_{Sink} = 1.0A)		–	1.8	2.0	
(I_{Sink} = 1.5 A)		–	2.1	2.6	
High State (I_{Source} = 50 mA)	(V_{CC}–V_{OH})	–	1.4	1.7	
(I_{Source} = 0.5 A)		–	1.7	2.0	
(I_{Source} = 0.75 A)		–	1.8	2.2	
Output Voltage with UVLO Activated (V_{CC} = 6.0 V, I_{Sink} = 1.0 mA)	$V_{OL(UVLO)}$	–	0.1	1.1	V
Output Voltage Rise Time (C_L = 1.0 nF, T_J = 25°C)	t_r	–	50	150	ns
Output Voltage Fall Time (C_L = 1.0 nF, T_J = 25°C)	t_f	–	50	150	ns
PWM SECTION					
Duty Cycle					%
Maximum	$DC_{(max)}$	46	48	50	
Minimum	$DC_{(min)}$	–	–	0	
TOTAL DEVICE					
Power Supply Current	I_{CC}				mA
Startup (V_{CC} = 5 V)		–	0.2	0.5	
Operating (Note 2)					
T_J = 25° C		–	17	20	
T_A = –25°C to +85° C		10	–	22	
Power Supply Zener Voltage (I_{CC} = 25 mA)	V_Z	18	20	23	V
OVERLOAD AND SHORT CIRCUIT PROTECTION					
Foldback Amplifier Threshold (Figures 9,10)	ΔV_{FB}	(V_{FB}–100)	(V_{FB}–200)	(V_{FB}–300)	mV
Load Detect Input					
Valid Load Comparator Threshold ($V_{Pin\ 2}$ Increasing)	$V_{th(VL)}$	2.0	2.5	3.0	V
Demag Comparator Threshold ($V_{Pin\ 2}$ Decreasing)	$V_{th(Demag)}$	50	88	120	mV
Propagation Delay (Input to Sink or Source Output)	$t_{PLH(in/out)}$	–	1.1	1.6	µS
Input Resistance	R_{in}	12	18	30	kΩ

NOTES: 2. Adjust V_{CC} above the startup threshold before setting to 12V.
3. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.

Figure 1. Timing Resistor versus Oscillator Frequency

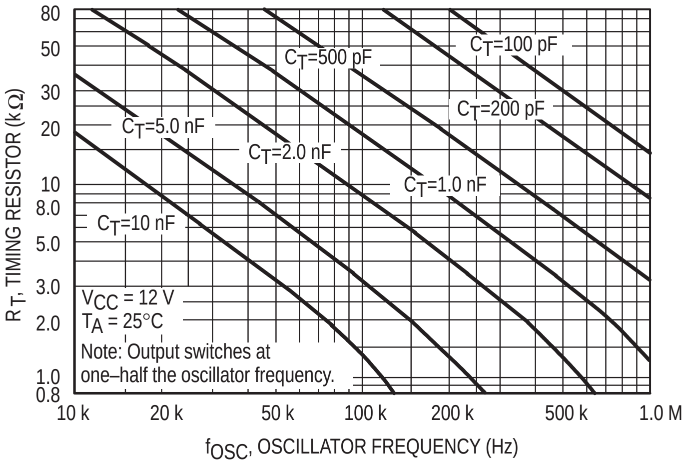


Figure 2. Output Deadtime versus Oscillator Frequency

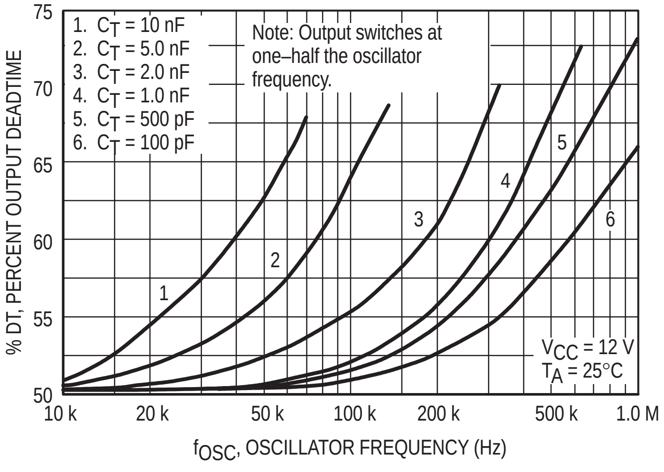


Figure 3. Oscillator Discharge Current versus Temperature

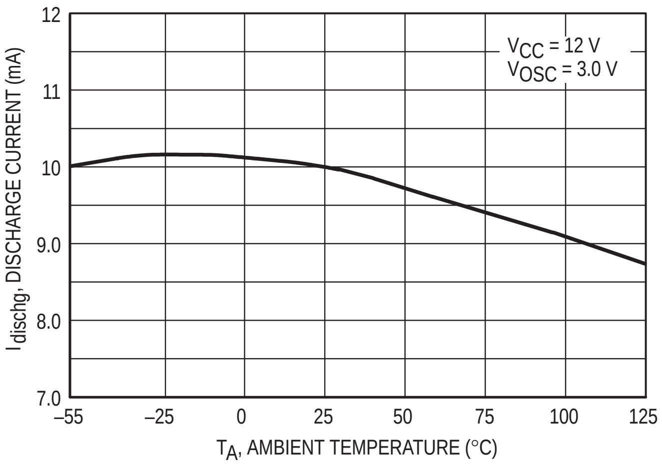


Figure 4. Oscillator Voltage Swing versus Temperature

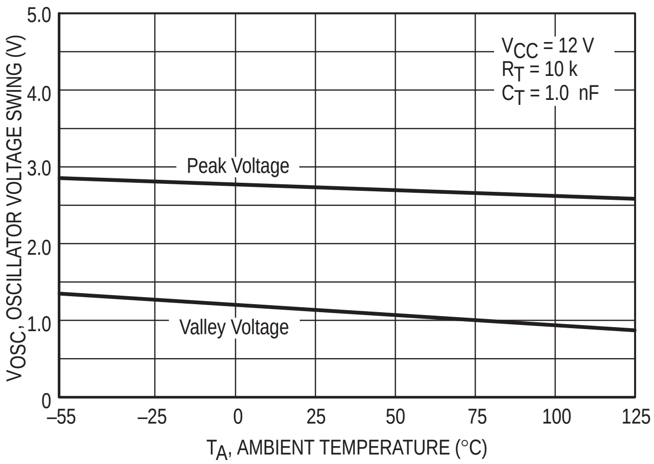


Figure 5. Error Amp Small Signal Transient Response

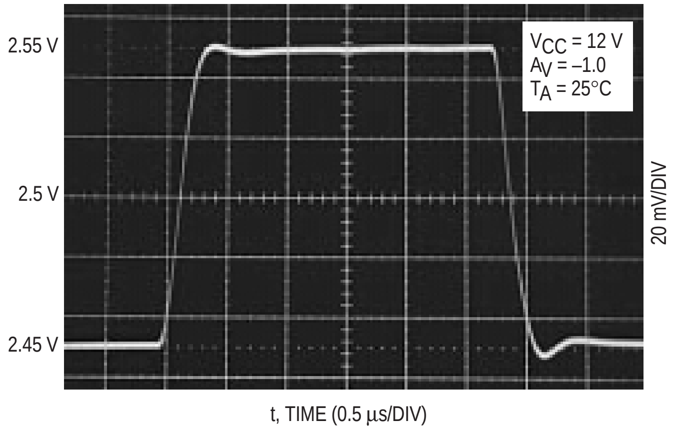


Figure 6. Error Amp Large Signal Transient Response

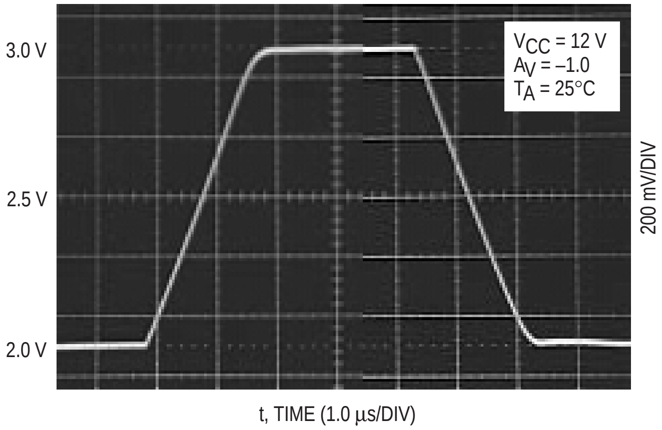


Figure 7. Error Amp Open Loop Gain and Phase versus Frequency

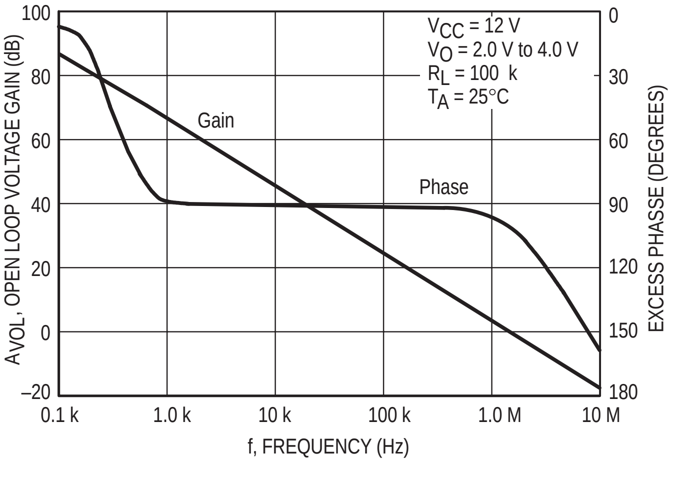


Figure 8. Current Sense Input Threshold versus Error Amp Output Voltage

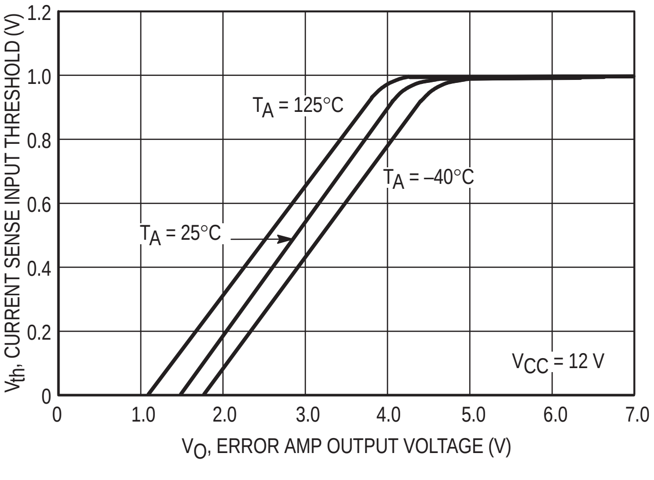


Figure 9. Voltage Feedback Input, Voltage versus Current

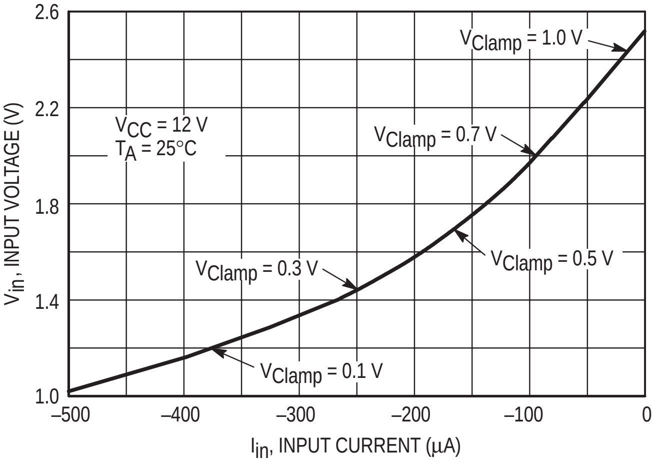


Figure 10. Voltage Feedback Input versus Current Sense Clamp Level

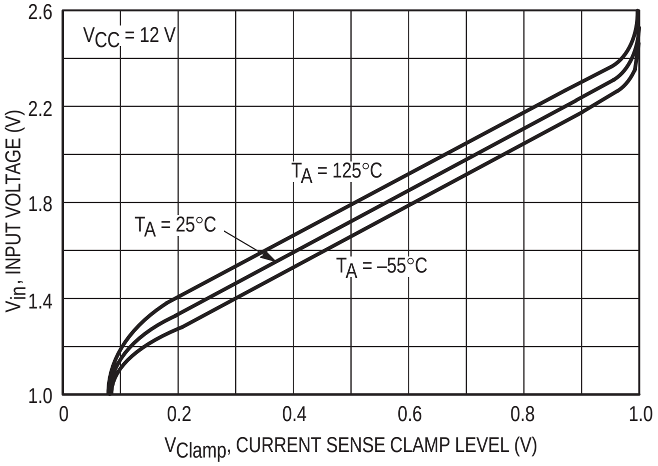


Figure 11. Reference Short Circuit Current versus Temperature

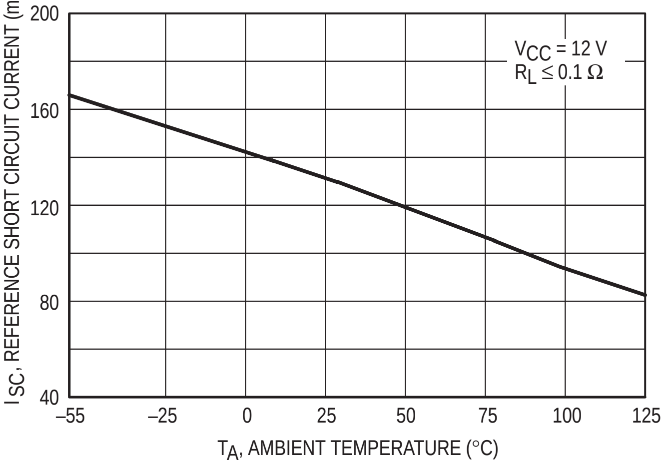


Figure 12. Reference Line and Load Regulation versus Temperature

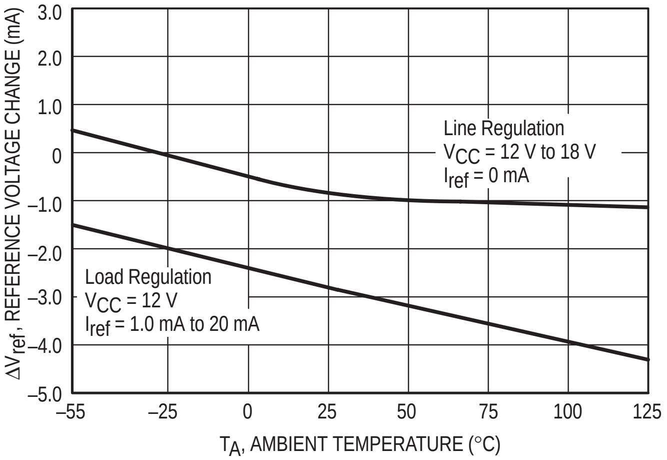


Figure 13. Reference Voltage Change versus Source Current

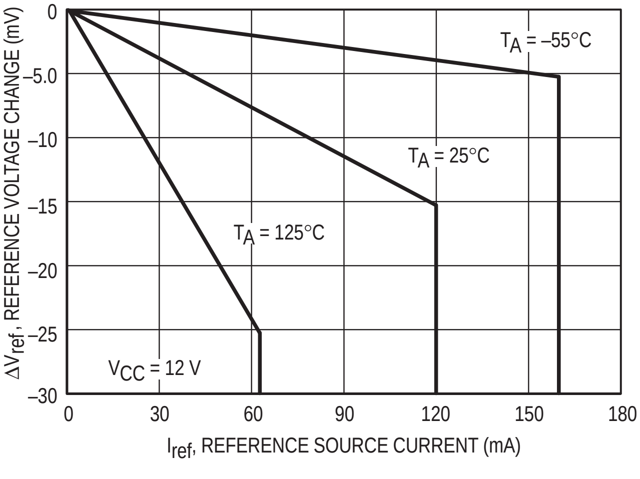
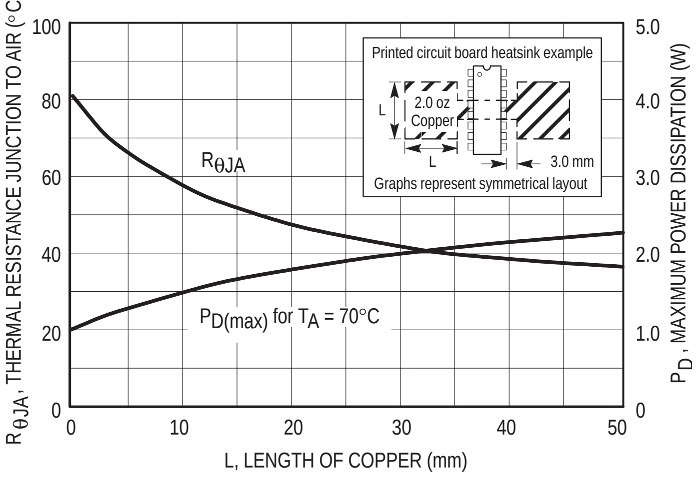


Figure 14. Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length



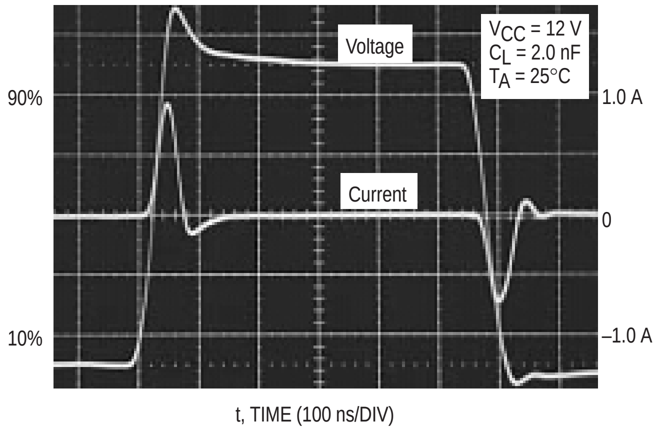


Figure 15. Output Waveform

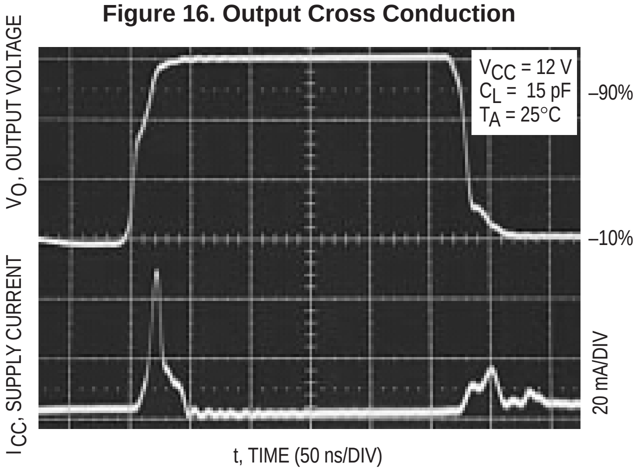


Figure 16. Output Cross Conduction

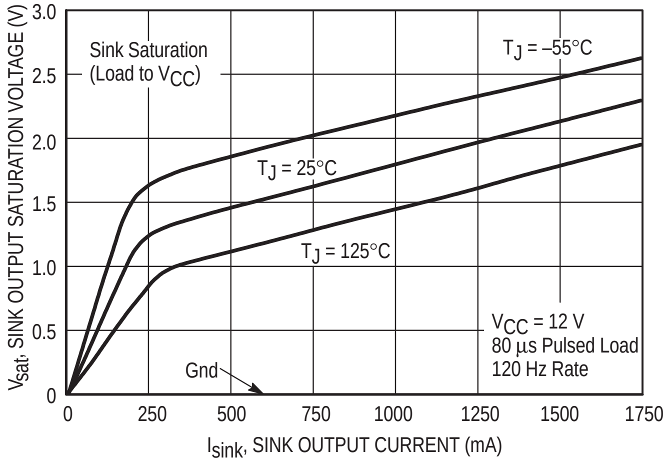


Figure 17. Sink Output Saturation Voltage versus Sink Current

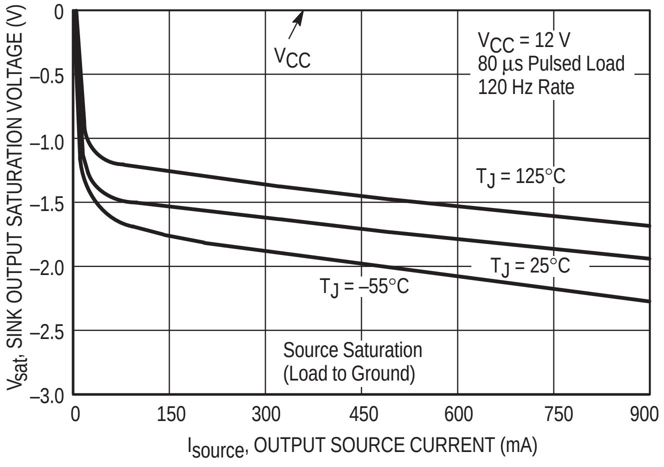


Figure 18. Source Output Saturation Voltage versus Load Current

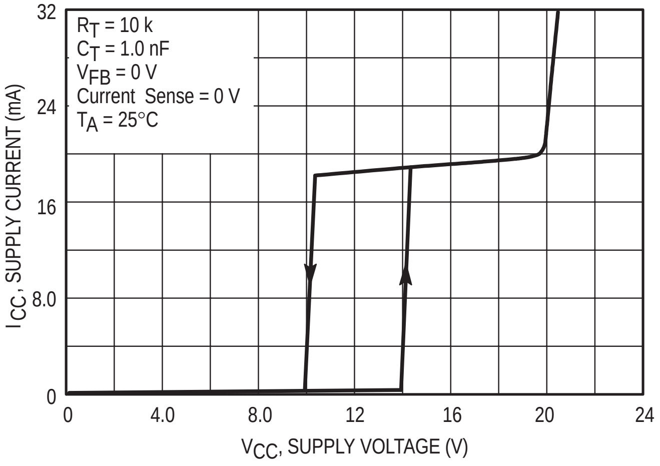


Figure 19. Supply Current versus Supply Voltage

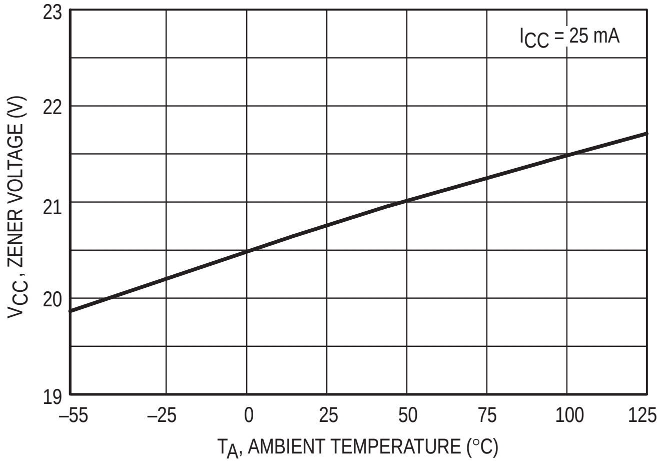


Figure 20. Power Supply Zener Voltage versus Temperature

Figure 21. Valid Load Comparator Threshold versus Temperature

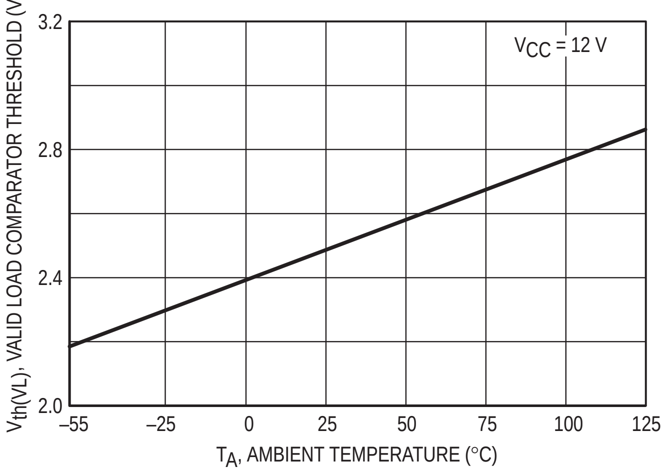


Figure 22. Demag Comparator Threshold versus Temperature

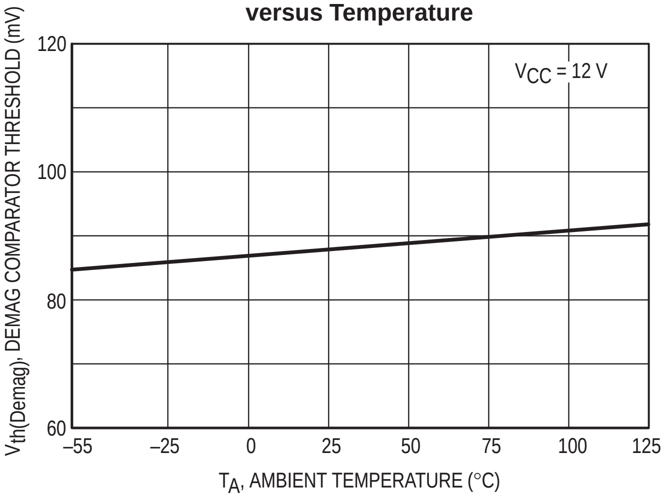


Figure 23. Load Detect Input Propagation Delay versus Temperature

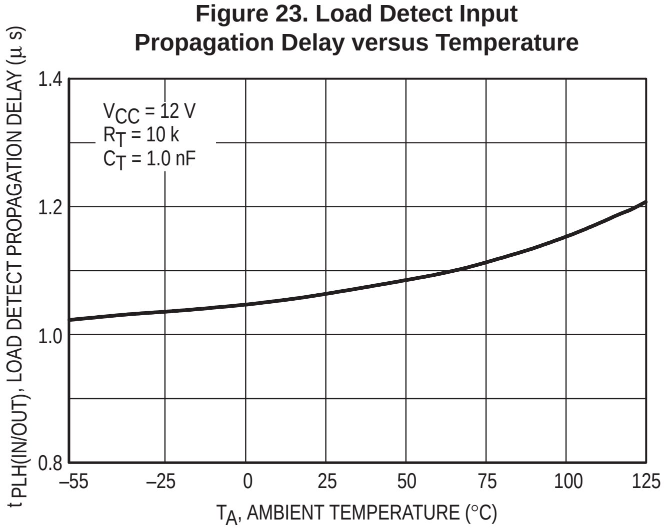


Figure 24. Startup Threshold Voltage versus Temperature

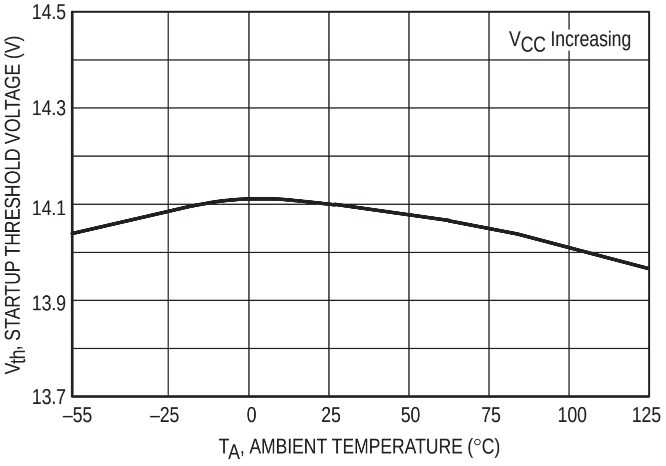


Figure 25. Minimum Operating Voltage After Turn–On versus Temperature

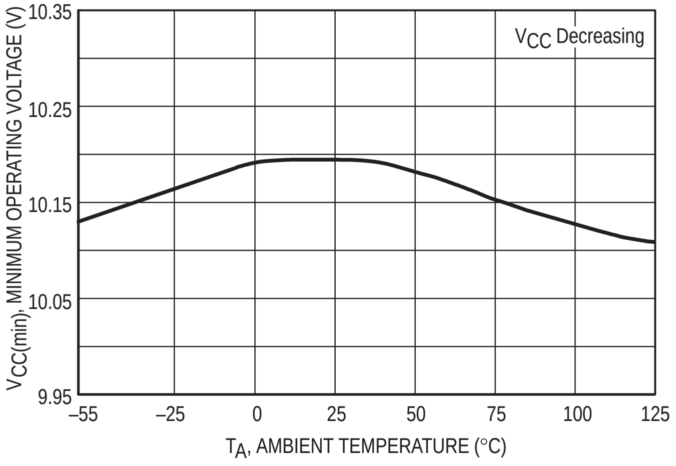


Figure 26. Reference Undervoltage Threshold versus Temperature

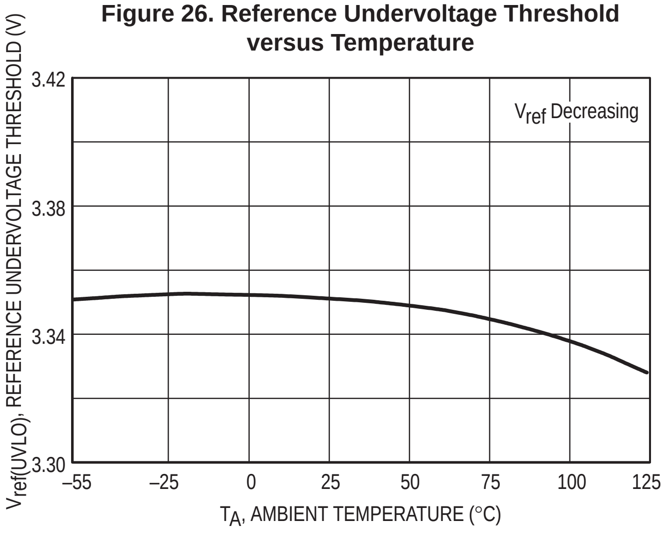


Figure 27. Representative Block Diagram

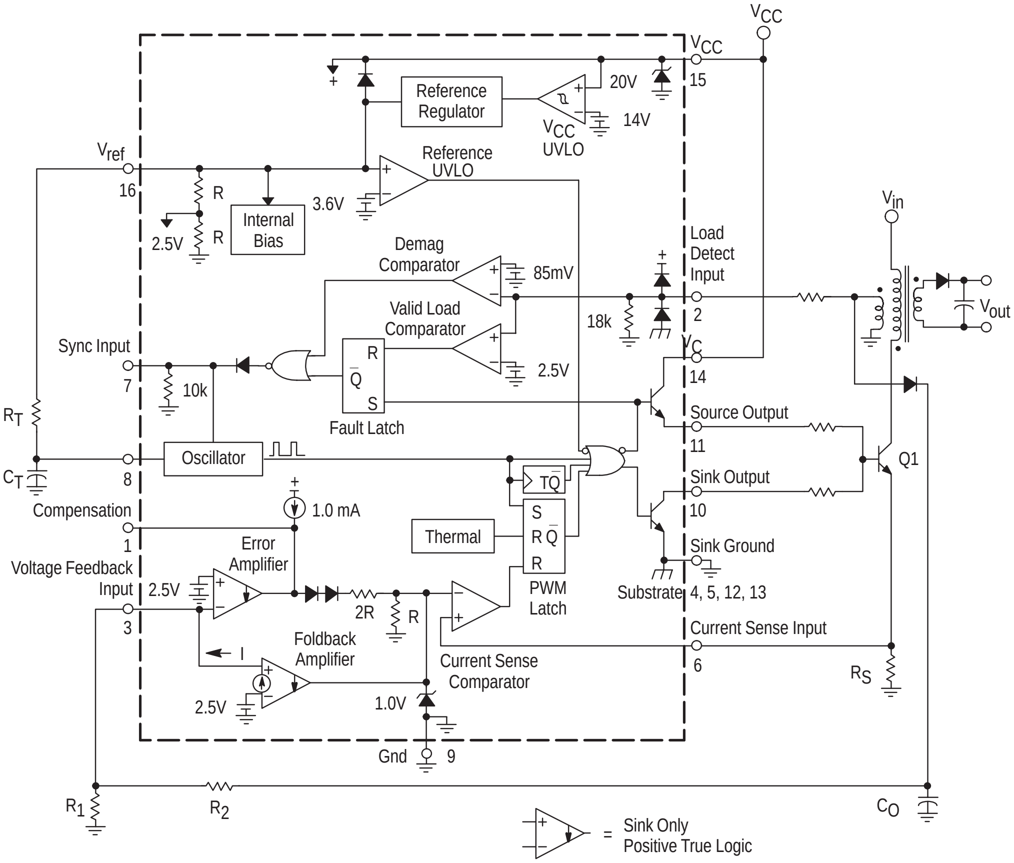
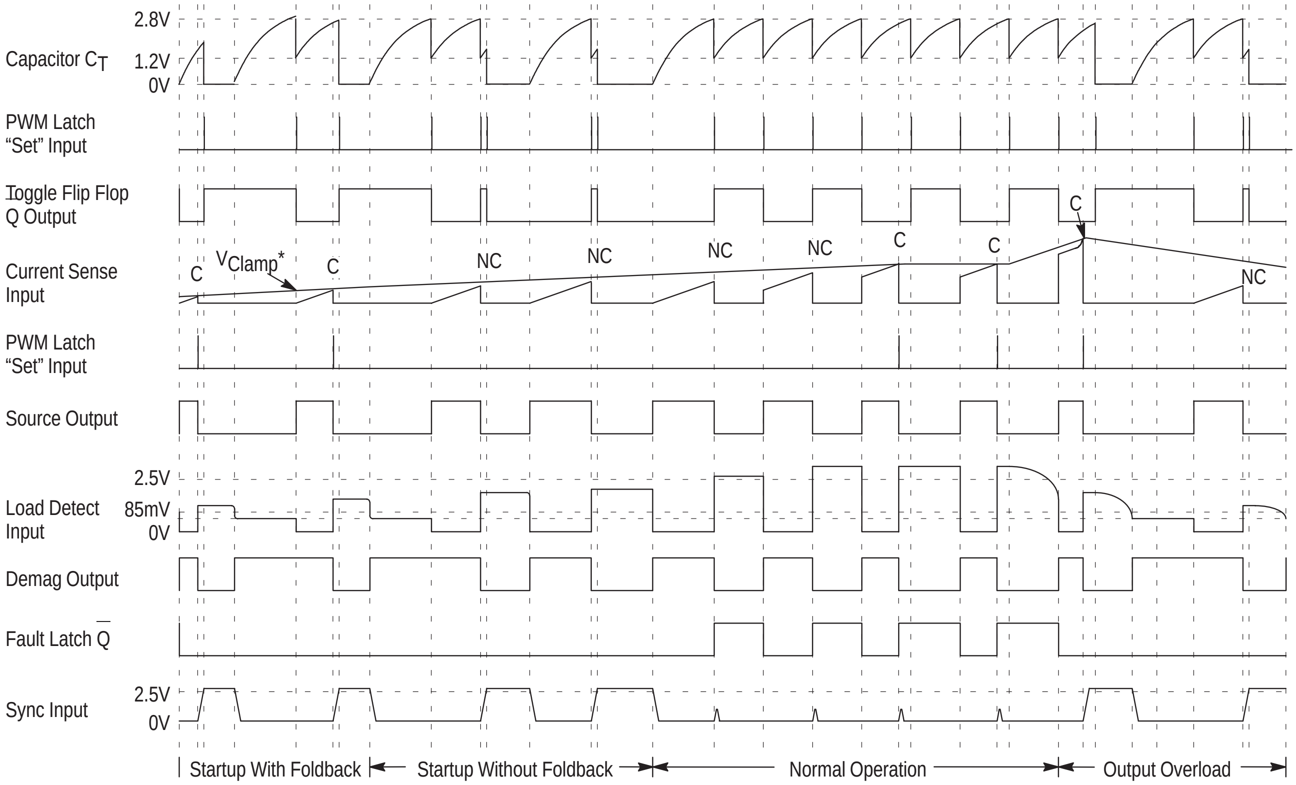


Figure 28. Timing Diagram



*C = Comparison of Current Sense Input With V_{Clamp} NC = No Comparison of Current Sense Input With V_{Clamp}

OPERATING DESCRIPTION

The MC44602 is a high performance, fixed frequency, current mode controller specifically designed to directly drive a bipolar power switch in off–line and high voltage dc–to–dc converter applications. This device offers the designer a cost effective solution with minimal external components. The representative block and timing diagrams are shown in Figures 27 and 28.

Oscillator

The oscillator frequency is programmed by the values selected for the timing components R_T and C_T. Capacitor C_T is charged from the 5.0 V reference through resistor R_T to approximately 2.8 V and discharged to 1.2 V by an internal current sink. During the discharge of C_T, the oscillator generates an internal blanking pulse that holds one of the inputs of the NOR gate high. This causes the Source and Sink outputs to be in a low state, thus producing a controlled amount of output deadtime. An internal toggle flip–flop has been incorporated in the MC44602 which blanks the output off every other clock cycle by holding one of the inputs of the NOR gate high. This in combination with the C_T discharge period yields output deadtimes programmable from 50% to 70%. Figure 1 shows R_T versus Oscillator Frequency and Figure 2, Output Deadtime versus Frequency, both for a given value of C_T. Note that many values of R_T and C_T will give the same oscillator frequency but only one combination will yield a specific output deadtime at a given frequency.

In many noise sensitive applications it may be desirable to frequency–lock the converter to an external system clock. This can be accomplished by applying a narrow rectangular clock signal with an amplitude of 3.2 V to 5.5 V to the Sync Input (Pin 7). For reliable locking, the free–running oscillator frequency should be set about 10% less than the clock frequency. If the clock signal is ac coupled through a capacitor, an external clamp diode may be required if the negative sync input current is greater than –5.0 mA. Connecting Pin 7 to V_{ref} will cause C_T to discharge to 0 V, inhibiting the Oscillator and conduction of the Source Output. Multi–unit synchronization can be accomplished by connecting the C_T pin of each IC to a single MC1455 timer.

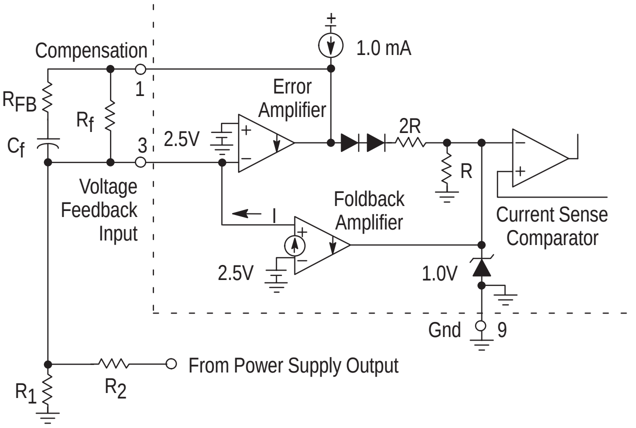
Error Amplifier

A fully compensated Error Amplifier with access to the inverting input and output is provided. It features a typical dc voltage gain of 90 dB, and a unity gain bandwith of 1.0 MHz with 57 degrees of phase margin (Figure 7). The noninverting input is internally biased at 2.5 V and is not pinned out. The converter output voltage is typically divided down and monitored by the inverting input. The maximum input bias current with the inverting input at 2.5 V is –2.0 µA. This can cause an output voltage error that is equal to the product of the input bias current and the equivalent input divider source resistance.

The Error Amp Output (Pin 1) is provided for external loop compensation (Figure 29). The output voltage is offset by two diodes drops (≈1.4 V) and divided by three before it connects to the inverting input of the Current Sense Comparator. This guarantees that no drive pulses appear at the Source Output (Pin 11) when Pin 1 is at its lowest state (V_{OL}). This occurs when the power supply is operating and the load is removed, or at the beginning of a soft–start interval. The Error Amp minimum feedback resistance is limited by the amplifier's minimum source current (0.5 mA) and the required output voltage (V_{OH}) to reach the comparator's 1.0 V clamp level:

$$R_{f(min)} \approx \frac{3.0\ (1.0\ V)\ +\ 1.4\ V}{0.5 mA}\ =\ 8800\ \Omega$$

Figure 29. Error Amplifier Compensation



Current Sense Comparator and PWM Latch

The MC44602 operates as a current mode controller, where output switch conduction is initiated by the oscillator and terminated when the peak inductor current reaches the threshold level established by the Error Amplifier output (Pin 1). Thus the error signal controls the peak inductor current on a cycle–by–cycle basis. The Current Sense Comparator PWM Latch configuration used ensures that only a single pulse appears at the Source Output during the appropriate oscillator cycle. The inductor current is converted to a voltage by inserting the ground referenced sense resistor R_S in series with the emitter of output switch Q1. This voltage is monitored by the Current Sense Input (Pin 6) and compared to a level derived from the Error Amp output. The peak inductor current under normal operating conditions is controlled by the voltage at Pin 1 where:

$$I_{pk} \approx \frac{V\ (Pin1)\ -\ 1.4V}{3\ R_S}$$

Abnormal operating conditions occur when the power supply output is overloaded or if output voltage sensing is lost. Under these conditions, the Current Sense Comparator threshold will be internally clamped to 1.0 V. Therefore the maximum peak switch current is:

$$I_{pk(max)} \approx \frac{1.0\ V}{R_S}$$

A narrow spike on the leading edge of the current waveform can usually be observed and may cause the power supply to exhibit an instability when the output is lightly loaded. This spike is due to the power transformer interwinding capacitance and the output rectifier recovery time. The addition of an RC filter on the Current Sense Input with a time constant that approximates the spike duration will usually eliminate the instability; refer to Figure 30.

Undervoltage Lockout

Two undervoltage lockout comparators have been incorporated to guarantee that the IC is fully functional before the output stage is enabled. The positive power supply terminal (V_{CC}) and the reference output (V_{ref}) are each monitored by separate comparators. Each has built–in hysteresis to prevent erratic output behavior as their respective thresholds are crossed. The V_{CC} comparator upper and lower thresholds are 14.1 V/10.2 V. The V_{ref} comparator upper and lower thresholds are 3.6 V/3.3 V. The large hysteresis and low startup current of the MC44602 make it ideally suited for off–line converter applications (Figures 33, 34) where efficient bootstrap startup techniques are required.

A 20 V zener is connected as a shunt regulator from V_{CC} to ground. Its purpose is to protect the IC from excessive voltage that can occur during system startup. The upper limit for the minimum operating voltage of the MC44602 is 11V.

Outputs

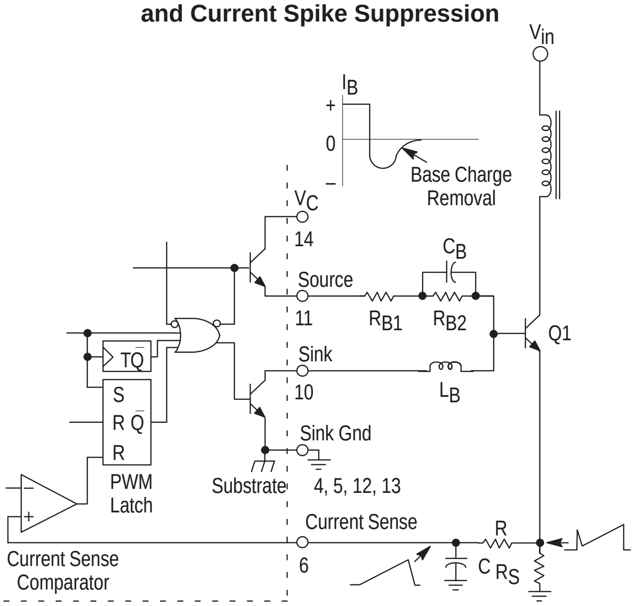
The MC44602 contains a high current split totem pole output that was specifically designed for direct drive of Bipolar Power Transistors. By splitting the totem pole into separate source and sink outputs, the power supply designer has the ability to independently adjust the turn–on and turn–off base drive to the external power transistor for optimal switching. The Source and Sink outputs are capable of up to 1.0 A and 1.5 A respectively and feature 50 ns switching times with a 1.0 nF load. Additional internal circuitry has been added to keep the Source Output “Off” and the Sink Output “On” whenever an undervoltage lockout is active. This feature eliminates the need for an external pull–down resistor and guarantees that the power transistor will be held in the “Off” state.

Separate output stage power and ground pins are provided to give the designer added flexibility in tailoring the base drive circuitry for a specific application. The Source Output high–state is controlled by applying a positive voltage to V_C (Pin 14) and is independent of V_{CC}. A zener clamp is typically connected to this input when driving power MOSFETs in systems where V_{CC} is greater than 20V. The Sink Output low–state is controlled by applying a negative voltage to the Sink Ground (Pins 4, 5, 12, 13). The Sink Ground can be biased as much as 5.0 V negative with respect to Ground (Pin 7). Proper implementation of the V_C and Sink Ground pins will significantly reduce the level of switching transient noise imposed on the control circuitry. This becomes particularly useful when reducing the $I_{pk(max)}$ clamp level.

Reference

The 5.0 V bandgap reference has a tolerance of ±6.0% over a junction temperature range of –25°C to 85°C. Its primary purpose is to supply charging current to the oscillator timing capacitor. The reference has short circuit protection and is capable of providing in excess of 20 mA for powering additional control system circuitry.

Figure 30. Bipolar Transistor Drive and Current Spike Suppression



Thermal Protection and Package

Internal Thermal Shutdown circuitry is provided to protect the integrated circuit in the event that the maximum junction temperature is exceeded. When activated, typically at 160°C, the PWM Latch is held in the “reset” state, forcing the Source Output “Off” and the Sink Output “On”. This feature is provided to prevent catastrophic failures from accidental device overheating. It is not intended to be used as a substitute for proper heatsinking.

The MC44602 is contained in a heatsinkable 16–lead plastic dual–in–line package in which the die is mounted on a special heat tab copper alloy lead frame. This tab consists of the four center Sink Ground pins that are specifically designed to improve the thermal conduction from the die to the circuit board. Figure 14 shows a simple and effective method of utilizing the printed circuit medium as a heat dissipater by soldering these pins to an adequate area of copper foil. This permits the use of standard layout and mounting practices while having the ability to halve the junction to air thermal resistance. This example is for a symmetrical layout on a single–sided board with two ounce per square foot of copper.

Design Considerations

Do not attempt to construct the converter on wire–wrap or plug–in prototype boards. High frequency circuit layout techniques are imperative to prevent pulse–width jitter. This is usually caused by excessive noise pick–up imposed on the Current Sense or Voltage Feedback inputs. Noise immunity can be improved by lowering circuit impedances at these points. The printed circuit layout should contain a ground plane with low–current signal, and high current switch and output grounds returning on separate paths back to the input filter capacitor. Ceramic bypass capacitors (0.1 µF) connected directly to V_{CC}, V_C, and V_{ref} may be required depending upon circuit layout. This provides a low impedance path for filtering the high frequency noise. All high current loops should be kept as short as possible using heavy copper runs to minimize radiated EMI. The Error Amp compensation circuitry and the converter output voltage divider should be located close to the IC and as far as possible from the power switch and other noise generating components.

PROTECTION MODES

The MC44602 operates as a conventional fixed frequency current mode controller when the power supply output load is less than the design limit. For enhanced system reliability, this device has the unique ability of changing operating modes if the power supply output is overloaded or shorted.

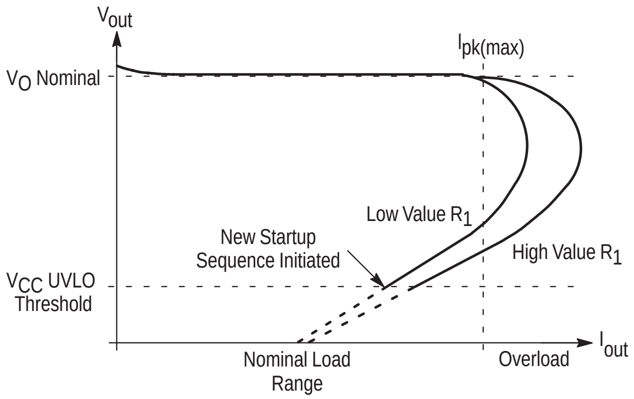
Overload Protection

Power supply overload protection is provided by the Foldback Amplifier. As the output load gradually increases, the Error Amplifier senses that the voltage at Pin 3 is less than the 2.5 V threshold. This causes the voltage at Pin 1 to rise, increasing the Current Sense Comparator threshold in order to maintain output regulation. As the load further increases, the inverting input of the Current Sense Comparator reaches the internal 1.0 V clamp level, limiting the switch current to the calculated $I_{pk(max)}$. At this point any further increase in load will cause the power supply output to fall out of regulation. As the voltage at Pin 3 falls below 2.5 V, current will flow out of the Foldback Amplifier input, and the internal clamp level will be proportionally reduced (Figures 9, 10). The increase in current flowing out of the Foldback Amplifier input in conjunction with the reduced clamp level, causes the power supply output voltage to fall at a faster rate than the voltage at Pin 3. This results in the output foldback characteristic shown in Figure 31. The shape of the current limit “knee” can be modified by the value of resistor R_1 in the feedback divider. Lower values of R_1 will reduce the $I_{pk(max)}$ clamp level at a faster rate.

Improper operation of the Foldback Amp can be encountered when the Error Amp compensation capacitor C_f exceeds 2.0 nF. The problem appears at Startup when the output voltage of the power supply is below nominal, causing the Error Amp output to rise quickly. The rapid change in output voltage will be coupled through C_f to the Inverting Input (Pin 3), keeping it at its 2.5 V threshold as the 1.0 mA Error Amp current source charges C_f. This has the effect of disabling the Foldback Amp by preventing Pin 3 and the clamp level at the inverting input of the Current Sense Comparator, from rising in proportion to the power supply output voltage. By adding resistor R_{FB} in series with C_f, the voltage at Pin 3 can be held to 1.0 V, corresponding to a Current Sense clamp level of 0.08 V (Figure 10), while allowing the Error Amp output to reach its high state V_{OH} of 7.0 V. The required resistor to keep Pin 3 below 1.0 V during initial Startup is:

$$\frac{R_{FB}\,R_f}{R_{FB} + R_f} \geq 6\left(\frac{R_1\,R_2}{R_1 + R_2}\right)$$

Figure 31. Output Foldback Characteristic



Short Circuit Protection

Short circuit protection for the power supply is provided by the Valid Load Comparator, Fault Latch, and Demag Comparator. Figure 32 shows the logic truth table of the functional blocks. When operating the power supply with nominal output loading, the Fault Latch is “Set” by the NOR gate driver during the Power Transistor “On” time and “Reset” by the Fault Comparator during the “Off” time. When a severe overload or short circuit occurs on any output, the voltage during the “Off” time (flyback voltage) at the Load Detect Input, is unable to reach the 2.5 V threshold of the Valid Load Comparator. This causes the Fault Latch to remain in the “Set” state with output Q “Low”. During the “Off” time the Demag Comparator output will also be “Low”. This causes the NOR gate to internally hold the Sync Input “High”, inhibiting the next fixed frequency Oscillator cycle and switching of the Power Transistor. As the load dissipates the stored transformer energy, the voltage at the Load Detect Input will fall. When this voltage reaches 85 mV, the Demag Comparator output goes “High”, allowing the Sync Input to go “Low”, and the Power Transistor to turn “On”.

Note that as long as there is an output short, the switching frequency will shift to a much lower frequency than that set by R_T/C_T. The frequency shift has the effect of lowering the duty cycle, resulting in a significant reduction in Power Transistor and Output Rectifier heating when compared to conventional current mode controllers. The extended “On” time is the result of C_T charging from 0 V to 2.8 V instead of 1.2 V to 2.8 V. The extended “Off” time is the result of the output short time constant. The time constant consists of the output filter capacitance, and the equivalent series resistance (ESR) of the capacitor plus the associated wire resistance.

Figure 32. Logic Truth Table of Functional Blocks

Output Load	Power Transistor	Demag		Fault Latch			Sync	Operating Comments
		Input	Out	S	R	$\overline{Q}$	Input	
Nominal	On	<85mV	1	1	0	0	0	NOR gate driver sets Fault Latch.
	At Turn–Off	>85 mV, <2.5 V	0	0	0	0		Narrow spike at Sync Input (<2.5 V) as transformer voltage rises quickly, Oscillator is not affected.
	Off	>2.5 V	0	0	1	1	0	Valid Load Comparator resets Fault Latch.
Short	On	<85 mV	1	1	0	0	0	Short is not detected until transistor turn–off.
	At Turn–Off	>85 mV, <2.5 V	0	0	0	0	1	Valid Load Comparator fails to reset Fault Latch, Pulse at Sync Input exceeds 2.5 V, Oscillator is disabled.
	Off	<85 mV	1	0	0	0	0	Load dissipates transformer energy, Oscillator enabled.

During the initial power supply startup the controller sequences through the Short Circuit and Overload Protection modes as the output filter capacitors charge–up. If an output is shorted and the auxiliary feedback winding is used to power the control IC as in Figure 33, the V_{CC} UVLO lower threshold level will be reached after several cycles, disabling the IC and initiating a new startup sequence. The Short Circuit Protection mode can be disabled by grounding the Sync Input. Narrow switching spikes are present on this pin during normal operation. These spikes are caused by the rise time of the flyback voltage from the 85 mV Demag Comparator threshold to the 2.5 V Valid Load Comparator threshold. In high power applications, the increased negative current at the Load Detect Input can extend the switching spikes to the point where they exceed the Sync Input threshold. This problem can be eliminated by placing an external small signal clamp diode at the Load Detect Input. The diode is connected with the cathode at Pin 2 and the anode at ground.

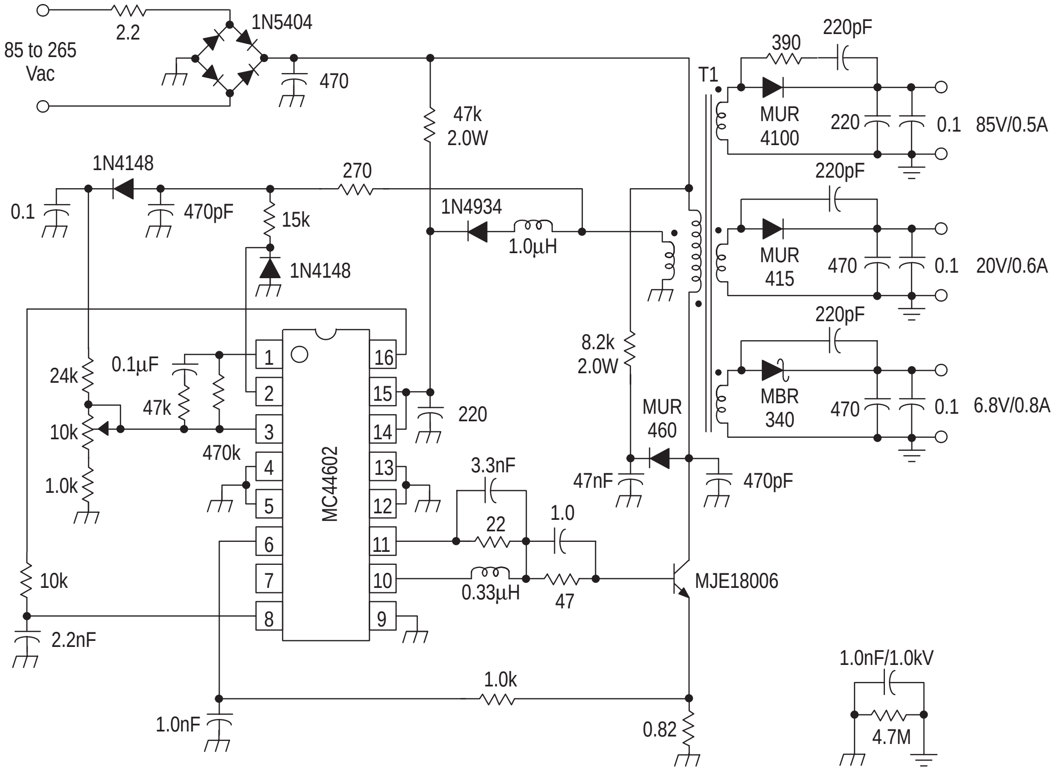
The divide–by–two toggle flip–flop will appear not to function properly during power supply startup without foldback, or operation with an overloaded output. This phenomena appears at the end of the oscillator cycle if there was not a current sense comparison, and after the flyback voltage at the Load Detect Input failed to exceed 2.5 V. Under these conditions, the Sync input will go high approximately 1.0 µs after the Load Detect Input exceeds the 85 mV Demag Comparator threshold. This causes C_T to discharge down towards ground, generating a second negative going edge on the oscillator waveform. This second edge results in the divide–by–two flip–flop being clocked twice for each “On” time of the switch transistor. During initial startup, this effect can be eliminated by insuring that the Foldback Amplifier is fully active with the addition of resistor R_{FB}. With the Foldback Amplifier active, the clamp level at the inverting input of the Current Sense Comparator will be low, allowing a comparison to take place during the switch transistor “On” time. When the Load Detect Input exceeds 85 mV, the Sync Input will go high, discharging C_T to ground after 1.0 µs, thus eliminating the second negative edge. Operation with the output overloaded will cause the toggle flip–flop to be clocked twice for each “On” time. This should not be a problem since the next “On” time is delayed by the Demag Comparator until the load dissipates the transformers energy.

The point where the IC detects that there is a severe output overload, or that the transformer has reached zero current, is controlled by the voltage of the auxiliary winding and a resistor divider. The divider consists of an external series resistor and an internal shunt resistor. The shunt resistor is nominally 18 kΩ but can range from 12 kΩ to 30 kΩ due to process variations. If more precise overload and zero current detection is required, the internal resistor variations can be swamped out by connecting a low value external resistor (≤2.7 kΩ) from Pin 2 to ground.

PIN FUNCTION DESCRIPTION

Pin	Function	Description
1	Compensation	This pin is the Error Amplifier output and is made available for loop compensation.
2	Load Detect Input	A voltage indicating a severe overload or short circuit condition at any output of the switching power supply is connected to this input. The Oscillator is controlled by this information making the power supply short circuit proof.
3	Voltage Feedback Input	This is the inverting input of the Error Amplifier and the noninverting input of the Foldback Amplifier. It is normally connected to the switching power supply output through a resistor divider.
4, 5, 12, 13	Sink Ground	The Sink Ground pins form a single power return that is typically connected back to the power source on a separate path from Pin 9 Ground, to reduce the effects of switching transient noise on the control circuitry. These pins can be used to enhance the package power capabilities (Figure 14). The Sink Output low state (V_{OL}) can be modified by applying a negative voltage to these pins with respect to Ground (Pin 9) to optimize turn–off of a bipolar junction transistor.
6	Current Sense Input	A voltage proportional to inductor current is connected to this input. The PWM uses this information to terminate conduction of the output switch transistor.
7	Sync Input	A narrow rectangular waveform applied to this input will synchronize the Oscillator. A dc voltage within the range of 3.2 V to 5.5 V will inhibit the Oscillator.
8	R_T/C_T	The Oscillator frequency and maximum Output duty cycle are programmed at this pin by connecting resistor R_T to V_{ref} and capacitor C_T to ground.
9	Ground	This pin is the control circuitry ground and is typically connected back to the power source on a separate path from the Sink Ground (Pins 4, 5, 12, 13).
10	Sink Output	Peak currents up to 1.5 A are sunk by this output suiting it ideally for turning–off a bipolar junction transistor. The output switches at one–half the oscillator frequency.
11	Source Output	Peak currents up to 1.0 A are sourced by this output suiting it ideally for turning–on a bipolar junction transistor. The output switches at one–half the oscillator frequency.
14	V_C	The Output high state (V_{OH}) is set by the voltage applied to this pin. With a separate connection to the power source, it can reduce the effects of switching transient noise on the control circuitry.
15	V_{CC}	This pin is the positive supply of the control IC. The minimum operating voltage range after startup is 11 V to 18 V.
16	V_{ref}	This is the 5.0 V reference output. It provides charging current for capacitor C_T through resistor R_T and can be used to bias any additional system circuitry.

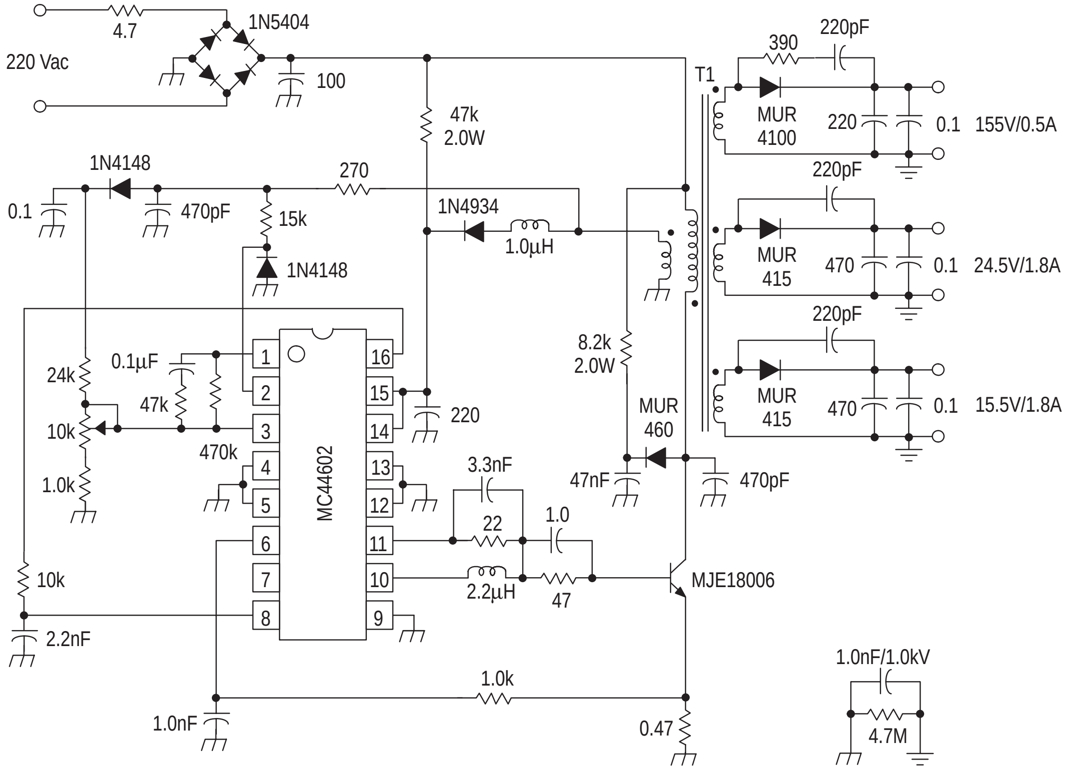
Figure 33. 60 Watt Off–Line Flyback Regulator



Test	Conditions	Results
Line Regulation	V_{in} = 85 Vac to 265 Vac	
85V	I_O = 0.5 A	Δ = 1.0 V or ± 0.6%
20V	I_O = 0.5 A	Δ = 0.04 V or ± 0.1%
6.8V	I_O = 0.8 A	Δ = 0.07 V or ± 0.5%
Load Regulation	V_{in} = 220 Vac	
85V	I_O = 0.1 A to 0.5 A	Δ = 1.0 V or ± 0.6%
20V	I_O = 0.1 A to 0.5 A	Δ = 0.4 V or ± 1.0%
6.8V	I_O = 0.1 A to 0.8 A	Δ = 0.2 V or ± 1.5%
Efficiency	V_{in} = 110 Vac, P_O = 58 W	81%
Standby Power	V_{in} = 110 Vac, P_O = 0 W	2.0 W

T1 – Orega SMT2 (G4787–01)
Primary: 41 Turns, #25AWG
Auxiliary Feedback: 12 Turns, #25AWG
Secondary: 85 V – 60 Turns, #25AWG
20 V – 15 Turns, #25AWG (2 Strands) Bifiliar Wound
6.8 V – 5 Turns, #25AWG (2 Strands) Bifiliar Wound
Core – ETD39 34x17x11 B52
Gap – ≈ 0.020″ for a primary inductance of 750 µH, A_L = 500 nH/Turn^2

Figure 34. 150 Watt Off–Line Flyback Regulator



Test	Conditions	Results
Line Regulation	V_{in} = 185 Vac to 265 Vac	
155V	I_O = 0.5 A	Δ = 1.0 V or ± 0.3%
24.5V	I_O = 1.0. A	Δ = 0.4 V or ± 0.8%
15.5V	I_O = 1.0 A	Δ = 0.3 V or ± 1.0%
Load Regulation	V_{in} = 220 Vac	
155V	I_O = 0.1 A to 0.5 A	Δ = 2.0 V or ± 0.7%
24.5V	I_O = 0.1 A to 1.0 A	Δ = 0.4 V or ± 0.8%
15.5V	I_O = 0.1 A to 1.0 A	Δ = 0.2 V or ± 0.7%
Efficiency	V_{in} = 220 Vac, P_O = 117.5 W	83%
Standby Power	V_{in} = 220 Vac, P_O = 0 W	5.0 W

T1 – Orega SMT2 (G4717–01)
Primary: 55 Turns, #25AWG
Auxiliary Feedback: 6 Turns, #25AWG
Secondary: 155 V – 52 Turns, #25AWG
24.5 V – 9 Turns, #25AWG (2 Strands) Bifiliar Wound
15.5 V – 6 Turns, #25AWG (2 Strands) Bifiliar Wound
Core – GETV 53x18x18 B52
Gap – ≈ 0.020″ for a primary inductance of 1.35 µH, A_L = 450 nH/Turn^2

MOTOROLA

MC44603

Advance Information

Mixed Frequency Mode GreenLine™ PWM Controller:

Fixed Frequency, Variable Frequency, Standby Mode

The MC44603 is an enhanced high performance controller that is specifically designed for off–line and dc–to–dc converter applications. This device has the unique ability of automatically changing operating modes if the converter output is overloaded, unloaded, or shorted, offering the designer additional protection for increased system reliability. The MC44603 has several distinguishing features when compared to conventional SMPS controllers. These features consist of a foldback facility for overload protection, a standby mode when the converter output is slightly loaded, a demagnetization detection for reduced switching stresses on transistor and diodes, and a high current totem pole output ideally suited for driving a power MOSFET. It can also be used for driving a bipolar transistor in low power converters (< 150 W). It is optimized to operate in discontinuous mode but can also operate in continuous mode. Its advanced design allows use in current mode or voltage mode control applications.

Current or Voltage Mode Controller

- Operation up to 250 kHz Output Switching Frequency
- Inherent Feed Forward Compensation
- Latching PWM for Cycle–by–Cycle Current Limiting
- Oscillator with Precise Frequency Control

High Flexibility

- Externally Programmable Reference Current
- Secondary or Primary Sensing
- Synchronization Facility
- High Current Totem Pole Output
- Undervoltage Lockout with Hysteresis

Safety/Protection Features

- Overvoltage Protection Against Open Current and Open Voltage Loop
- Protection Against Short Circuit on Oscillator Pin
- Fully Programmable Foldback
- Soft–Start Feature
- Accurate Maximum Duty Cycle Setting
- Demagnetization (Zero Current Detection) Protection
- Internally Trimmed Reference

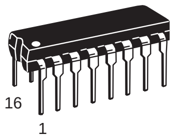
GreenLine Controller: Low Power Consumption in Standby Mode

- Low Startup and Operating Current
- Fully Programmable Standby Mode
- Controlled Frequency Reduction in Standby Mode
- Low dV/dT for Low EMI Radiations

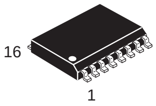
MIXED FREQUENCY MODE GREENLINE PWM* CONTROLLER:

VARIABLE FREQUENCY, FIXED FREQUENCY, STANDBY MODE

* PWM = Pulse Width Modulation

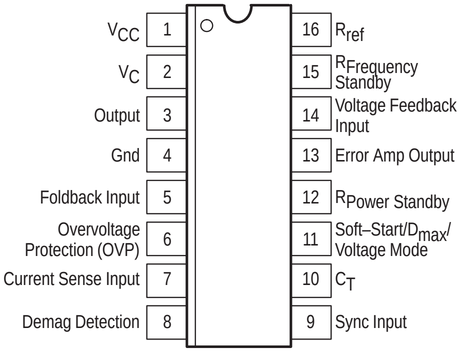


P SUFFIX
PLASTIC PACKAGE
CASE 648



DW SUFFIX
PLASTIC PACKAGE
CASE 751G
(SOP–16L)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC44603P	T_A = –25° to +85°C	Plastic DIP–16
MC44603DW		SOP–16L

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Total Power Supply and Zener Current	$(I_{CC} + I_Z)$	30	mA
Supply Voltage with Respect to Ground (Pin 4)	V_C V_{CC}	18	V
Output Current (Note 1)			mA
Source	$I_{O(Source)}$	–750	
Sink	$I_{O(Sink)}$	750	
Output Energy (Capacitive Load per Cycle)	W	5.0	µJ
$R_{F\ Stby}$, C_T, Soft–Start, R_{ref}, $R_{P\ Stby}$ Inputs	V_{in}	–0.3 to 5.5	V
Foldback Input, Current Sense Input, E/A Output, Voltage Feedback Input, Overvoltage Protection, Synchronization Input	V_{in}	–0.3 to V_{CC} + 0.3	V
Synchronization Input			
High State Voltage	V_{IH}	V_{CC} + 0.3	V
Low State Reverse Current	V_{IL}	–20	mA
Demagnetization Detection Input Current			mA
Source	$I_{demag–ib\ (Source)}$	–4.0	
Sink	$I_{demag–ib\ (Sink)}$	10	
Error Amplifier Output Sink Current	$I_{E/A\ (Sink)}$	20	mA
Power Dissipation and Thermal Characteristics			
P Suffix, Dual–In–Line, Case 648			
Maximum Power Dissipation at T_A = 85°C	P_D	0.6	W
Thermal Resistance, Junction–to–Air	$R_{\theta JA}$	100	°C/W
DW Suffix, Surface Mount, Case 751G			
Maximum Power Dissipation at T_A = 85°C	P_D	0.45	W
Thermal Resistance, Junction–to–Air	$R_{\theta JA}$	145	°C/W
Operating Junction Temperature	T_J	150	°C
Operating Ambient Temperature	T_A	–25 to +85	°C

NOTES: 1. Maximum package power dissipation limits must be observed.
2. ESD data available upon request.

ELECTRICAL CHARACTERISTICS (V_{CC} and V_C = 12 V, [Note 3], R_{ref} = 10 kΩ, C_T = 820 pF, for typical values T_A = 25°C, for min/max values T_A = –25° to +85°C [Note 4], unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OUTPUT SECTION					
Output Voltage (Note 5)					V
Low State (I_{Sink} = 100 mA)	V_{OL}	–	1.0	1.2	
(I_{Sink} = 500 mA)		–	1.4	2.0	
High State (I_{Source} = 200 mA)	V_{OH}	–	1.5	2.0	
(I_{Source} = 500 mA)		–	2.0	2.7	
Output Voltage During Initialization Phase	V_{OL}				V
V_{CC} = 0 to 1.0 V, I_{Sink} = 10 µA		–	–	1.0	
V_{CC} = 1.0 to 5.0 V, I_{Sink} = 100 µA		–	0.1	1.0	
V_{CC} = 5.0 to 13 V, I_{Sink} = 1.0 mA		–	0.1	1.0	
Output Voltage Rising Edge Slew–Rate (C_L = 1.0 nF, T_J = 25°C)	dVo/dT	–	300	–	V/µs
Output Voltage Falling Edge Slew–Rate (C_L = 1.0 nF, T_J = 25°C)	dVo/dT	–	–300	–	V/µs
ERROR AMPLIFIER SECTION					
Voltage Feedback Input ($V_{E/A\ out}$ = 2.5 V)	V_{FB}	2.42	2.5	2.58	V
Input Bias Current (V_{FB} = 2.5 V)	$I_{FB–ib}$	–2.0	–0.6	–	µA
Open Loop Voltage Gain ($V_{E/A\ out}$ = 2.0 to 4.0 V)	A_{VOL}	65	70	–	dB

NOTES: 3. Adjust V_{CC} above the startup threshold before setting to 12 V.
4. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
5. V_C must be greater than 5.0 V.

ELECTRICAL CHARACTERISTICS (continued) (V_{CC} and V_C = 12 V, [Note 3], R_{ref} = 10 kΩ, C_T = 820 pF, for typical values T_A = 25°C, for min/max values T_A = –25° to +85°C [Note 4], unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
ERROR AMPLIFIER SECTION (continued)					
Unity Gain Bandwidth	BW				MHz
T_J = 25°C		–	4.0	–	
T_J = –25° to +85°C		–	–	5.5	
Voltage Feedback Input Line Regulation (V_{CC} = 10 to 15 V)	$V_{FBline–reg}$	–10	–	10	mV
Output Current					mA
Sink ($V_{E/A\ out}$ = 1.5 V, V_{FB} = 2.7 V) T_A = –25° to +85°C	I_{Sink}	2.0	12	–	
Source ($V_{E/A\ out}$ = 5.0 V, V_{FB} = 2.3 V) T_A = –25° to +85°C	I_{Source}	–2.0	–	–0.2	
Output Voltage Swing					V
High State ($I_{E/A\ out\ (source)}$ = 0.5 mA, V_{FB} = 2.3 V)	V_{OH}	5.5	6.5	7.5	
Low State ($I_{E/A\ out\ (sink)}$ = 0.33 mA, V_{FB} = 2.7 V)	V_{OL}	–	1.0	1.1	
REFERENCE SECTION					
Reference Output Voltage (V_{CC} = 10 to 15 V)	V_{ref}	2.4	2.5	2.6	V
Reference Current Range (I_{ref} = V_{ref}/R_{ref}, R = 5.0 k to 25 kΩ)	I_{ref}	–500	–	–100	µA
Reference Voltage Over I_{ref} Range	ΔV_{ref}	–40	–	40	mV
OSCILLATOR AND SYNCHRONIZATION SECTION					
Frequency	f_{OSC}				kHz
T_A = 0° to +70°C		44.5	48	51.5	
T_A = –25° to +85°C		44	–	52	
Frequency Change with Voltage (V_{CC} = 10 to 15 V)	$\Delta f_{OSC}/\Delta V$	–	0.05	–	%/V
Frequency Change with Temperature (T_A = –25° to +85°C)	$\Delta f_{OSC}/\Delta T$	–	0.05	–	%/°C
Oscillator Voltage Swing (Peak–to–Peak)	$V_{OSC(pp)}$	1.65	1.8	1.95	V
Ratio Charge Current/Reference Current	I_{charge}/I_{ref}				–
T_A = 0° to +70°C (V_{CT} = 2.0 V)		0.375	0.4	0.425	
T_A = –25° to +85°C		0.37	–	0.43	
Fixed Maximum Duty Cycle = $I_{discharge}/(I_{discharge} + I_{charge})$	D	78	80	82	%
Ratio Standby Discharge Current versus $I_{R\ F\ Stby}$ (Note 6)	$I_{disch–Stby}/$ $I_{R\ F\ Stby}$				–
T_A = 0° to +70°C		0.46	0.53	0.6	
T_A = –25° to +85°C (Note 8)		0.43	–	0.63	
$V_{R\ F\ Stby}$ ($I_{R\ F\ Stby}$ = 100 µA)	$V_{R\ F\ Stby}$	2.4	2.5	2.6	V
Frequency in Standby Mode ($R_{F\ Stby}$ (Pin 15) = 25 kΩ)	F_{Stby}	18	21	24	kHz
Current Range	$I_{R\ F\ Stby}$	–200	–	–50	µA
Synchronization Input Threshold Voltage (Note 7)	V_{inthH}	3.2	3.7	4.3	V
	V_{inthL}	0.45	0.7	0.9	
Synchronization Input Current	$I_{Sync–in}$	–5.0	–	0	µA
Minimum Synchronization Pulse Width (Note 8)	T_{Sync}	–	–	0.5	µs
UNDERVOLTAGE LOCKOUT SECTION					
Startup Threshold	$V_{stup–th}$	13.6	14.5	15.4	V
Output Disable Voltage After Threshold Turn–On (UVLO 1)	$V_{disable1}$				V
T_A = 0° to +70°C		8.6	9.0	9.4	
T_A = –25° to +85°C		8.3	–	9.6	
Reference Disable Voltage After Threshold Turn–On (UVLO 2)	$V_{disable2}$	7.0	7.5	8.0	V

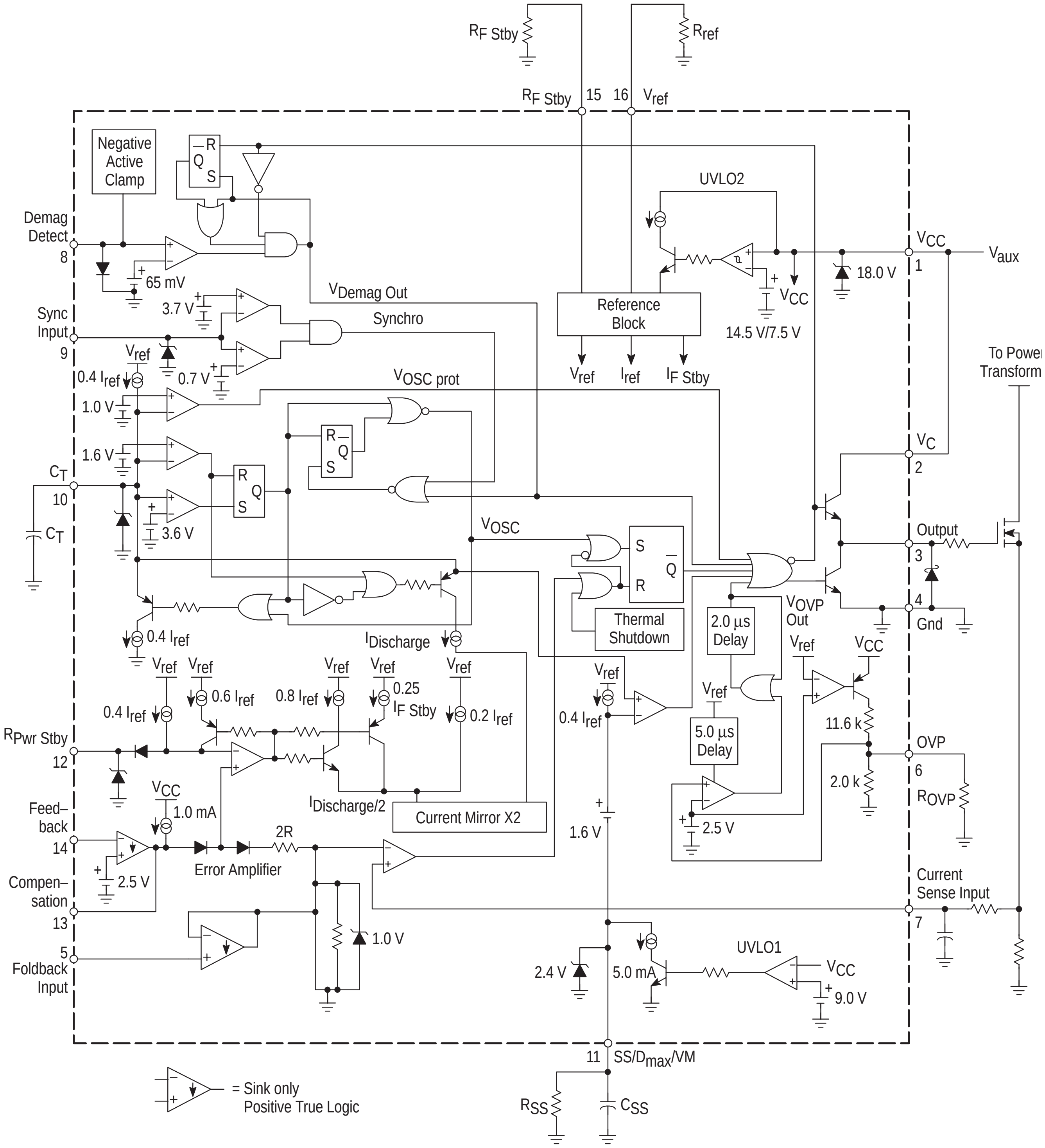
NOTES: 3. Adjust V_{CC} above the startup threshold before setting to 12 V.
4. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
6. Standby is disabled for $V_{R\ P\ Stby}$ < 25 mV typical.
7. If not used, Synchronization input must be connected to Ground.
8. Synchronization Pulse Width must be shorter than $T_{OSC} = 1/f_{OSC}$.

ELECTRICAL CHARACTERISTICS (continued) (V_{CC} and V_C = 12 V, [Note 3], R_{ref} = 10 kΩ, C_T = 820 pF, for typical values T_A = 25°C, for min/max values T_A = –25° to +85°C [Note 4], unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
DEMAGNETIZATION DETECTION SECTION (Note 9)					
Demagnetization Detect Input					
Demagnetization Comparator Threshold ($V_{Pin\ 9}$ Decreasing)	$V_{demag–th}$	50	65	80	mV
Propagation Delay (Input to Output, Low to High)	–	–	0.25	–	µs
Input Bias Current (V_{demag} = 65 mV)	$I_{demag–Ib}$	–0.5	–	–	µA
Negative Clamp Level (I_{demag} = –2.0 mA)	$C_{L(neg)}$	–	–0.38	–	V
Positive Clamp Level (I_{demag} = 2.0 mA)	$C_{L(pos)}$	–	0.72	–	V
SOFT–START SECTION (Note 11)					
Ratio Charge Current/I_{ref}	$I_{ss(ch)}/I_{ref}$				–
T_A = 0° to +70°C		0.37	0.4	0.43	
T_A = –25° to +85°C		0.36	–	0.44	
Discharge Current ($V_{soft–start}$ = 1.0 V)	$I_{discharge}$	1.5	5.0	–	mA
Clamp Level	$V_{ss(CL)}$	2.2	2.4	2.6	V
Duty Cycle ($R_{soft–start}$ = 12 kΩ)	$D_{soft–start\ 12k}$	36	42	49	%
($V_{soft–start\ (Pin\ 11)}$ = 0.1 V)	$D_{soft–start}$	–	–	0	
OVERVOLTAGE SECTION					
Protection Threshold Level on V_{OVP}	$V_{OVP–th}$	2.42	2.5	2.58	V
Propagation Delay (V_{OVP} > 2.58 V to V_{out} Low)		1.0	–	3.0	µs
Protection Level on V_{CC}	$V_{CC\ prot}$				V
T_A = 0° to +70°C		16.1	17	17.9	
T_A = –25° to +85°C		15.9	–	18.1	
Input Resistance	–				kΩ
T_A = 0° to +70°C		1.5	2.0	3.0	
T_A = –25° to +85°C		1.4	–	3.4	
FOLDBACK SECTION (Note 10)					
Current Sense Voltage Threshold ($V_{foldback\ (Pin\ 5)}$ = 0.9 V)	$V_{CS–th}$	0.86	0.89	0.9	V
Foldback Input Bias Current ($V_{foldback\ (Pin\ 5)}$ = 0 V)	$I_{foldback–Ib}$	–6.0	–2.0	–	µA
STANDBY SECTION					
Ratio $I_{R\ P\ Stby}/I_{ref}$	$I_{R\ P\ Stby}/I_{ref}$				–
T_A = 0° to +70°C		0.37	0.4	0.43	
T_A = –25° to +85°C		0.36	–	0.44	
Ratio Hysteresis (V_h Required to Return to Normal Operation from Standby Operation)	$V_h/V_{R\ P\ Stby}$				–
T_A = 0° to +70°C		1.42	1.5	1.58	
T_A = –25° to +85°C		1.4	–	1.6	
Current Sense Voltage Threshold ($V_{R\ P\ Stby\ (Pin\ 12)}$ = 1.0 V)	$V_{CS–Stby}$	0.28	0.31	0.34	V
CURRENT SENSE SECTION					
Maximum Current Sense Input Threshold ($V_{feedback\ (Pin\ 14)}$ = 2.3 V and $V_{foldback\ (Pin\ 6)}$ = 1.2 V)	$V_{CS–th}$	0.96	1.0	1.04	V
Input Bias Current	$I_{CS–ib}$	–10	–2.0	–	µA
Propagation Delay (Current Sense Input to Output at V_{TH} of MOS transistor = 3.0 V)	–	–	120	200	ns
TOTAL DEVICE					
Power Supply Current	I_{CC}				mA
Startup (V_{CC} = 13 V with V_{CC} Increasing)		–	0.3	0.45	
Operating T_A = –25° to +85°C (Note 3)		13	17	20	
Power Supply Zener Voltage (I_{CC} = 25 mA)	V_Z	18.5	–	–	V
Thermal Shutdown	–	–	155	–	°C

NOTES:
3. Adjust V_{CC} above the startup threshold before setting to 12 V.
4. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
9. This function can be inhibited by connecting Pin 8 to Gnd. This allows a continuous current mode operation.
10. This function can be inhibited by connecting Pin 5 to V_{CC}.
11. The MC44603 can be shut down by connecting the Soft–Start pin (Pin 11) to Ground.

Representative Block Diagram



This device contains 243 active transistors.

Figure 1. Timing Resistor versus Oscillator Frequency

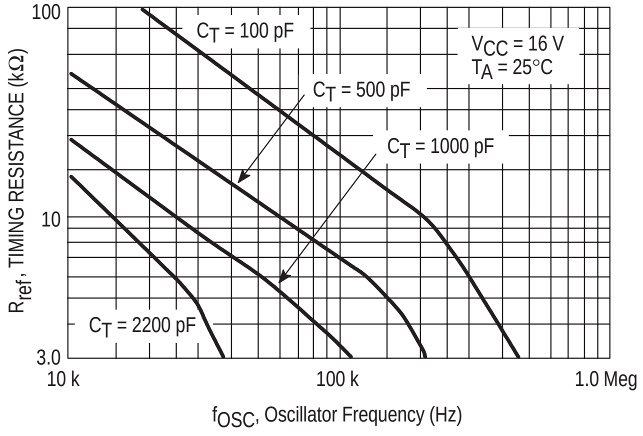


Figure 2. Standby Mode Timing Capacitor versus Oscillator Frequency

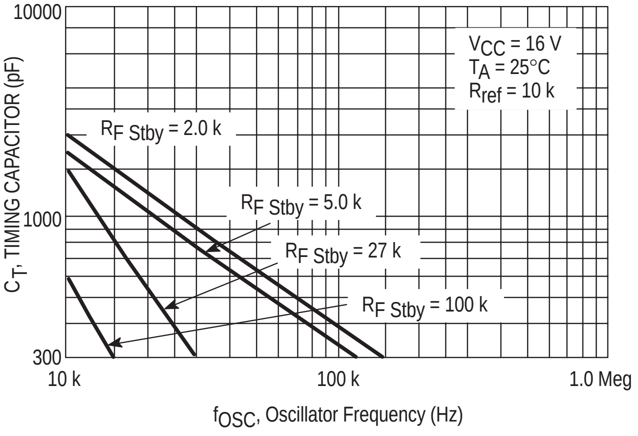


Figure 3. Oscillator Frequency versus Temperature

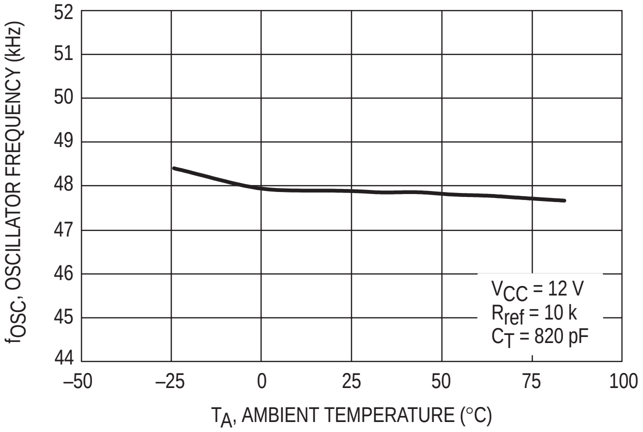


Figure 4. Ratio Charge Current/Reference Current versus Temperature

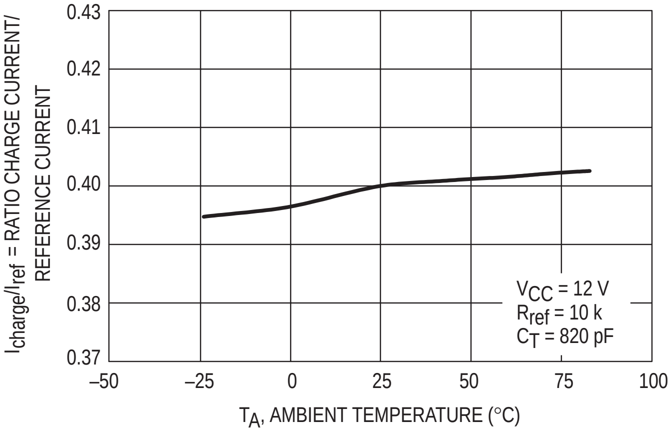


Figure 5. Output Waveform

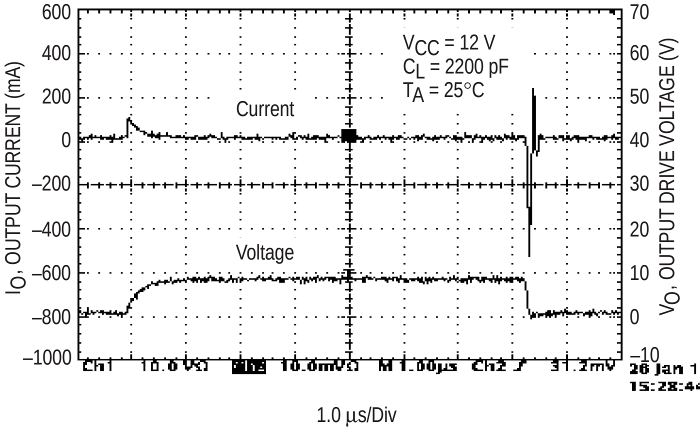


Figure 6. Output Cross Conduction

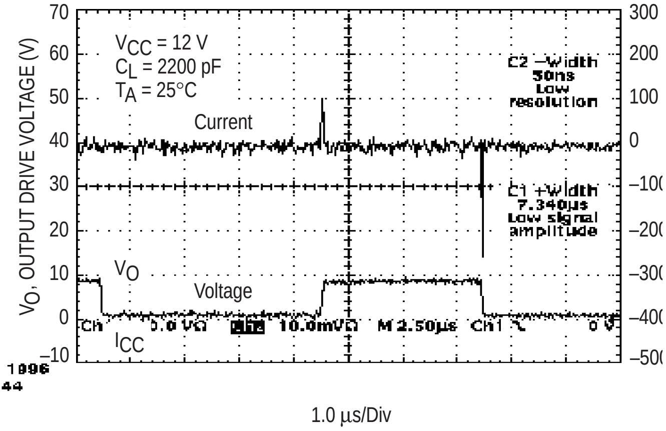


Figure 7. Oscillator Discharge Current versus Temperature

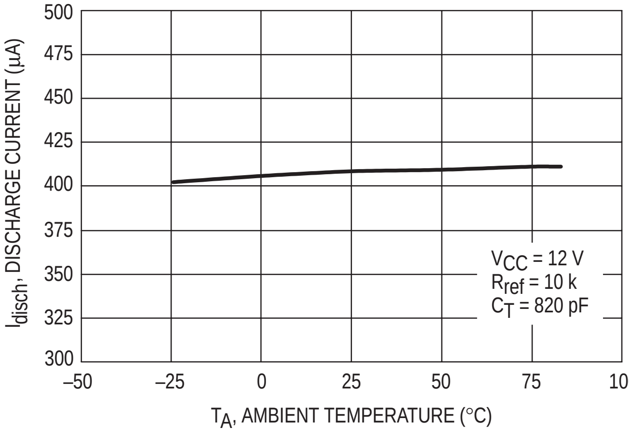


Figure 8. Source Output Saturation Voltage versus Load Current

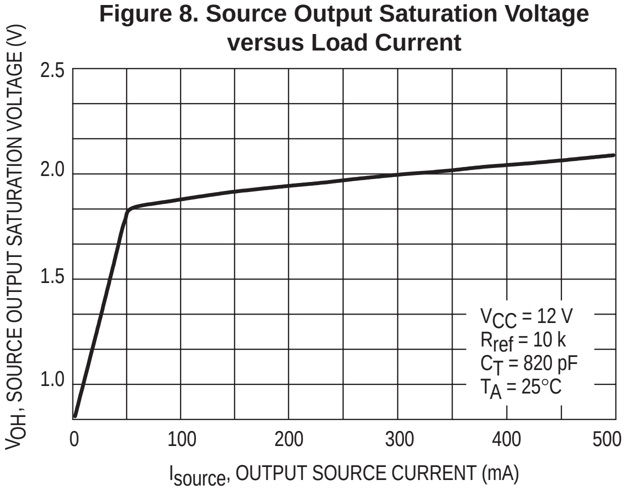


Figure 9. Sink Output Saturation Voltage versus Sink Current

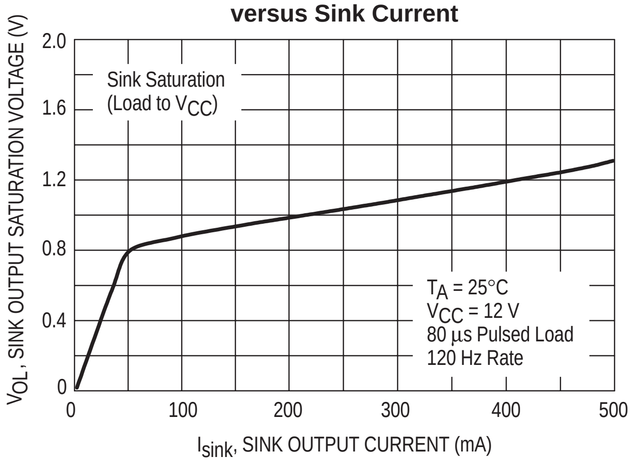


Figure 10. Error Amplifier Gain and Phase versus Frequency

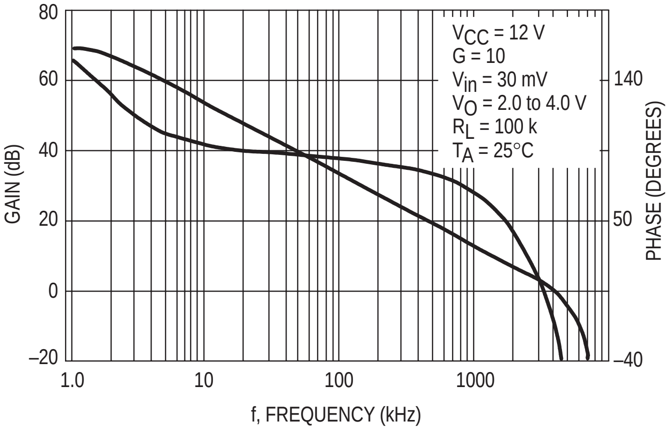


Figure 11. Voltage Feedback Input versus Temperature

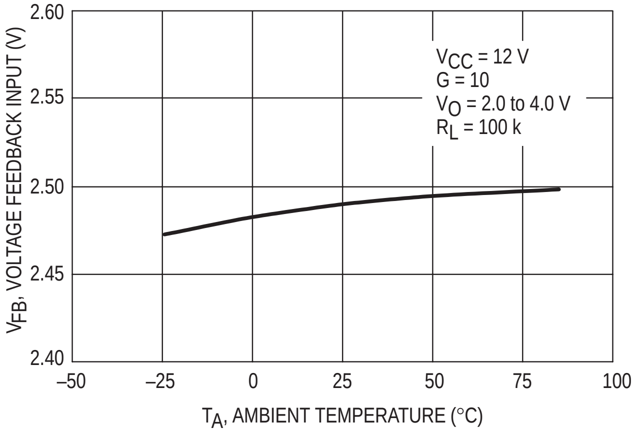


Figure 12. Demag Comparator Threshold versus Temperature

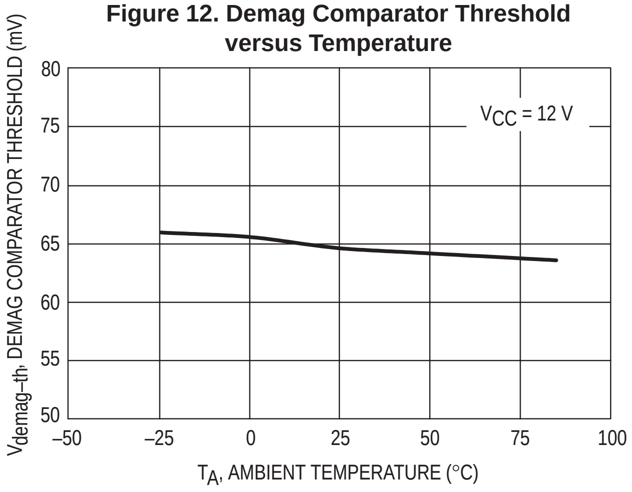


Figure 13. Current Sense Gain versus Temperature

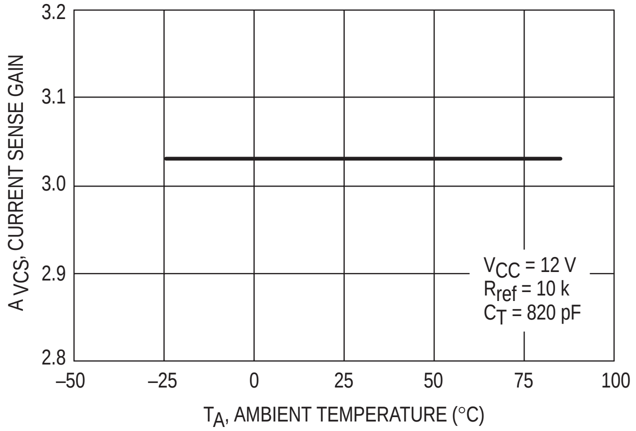


Figure 14. Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length

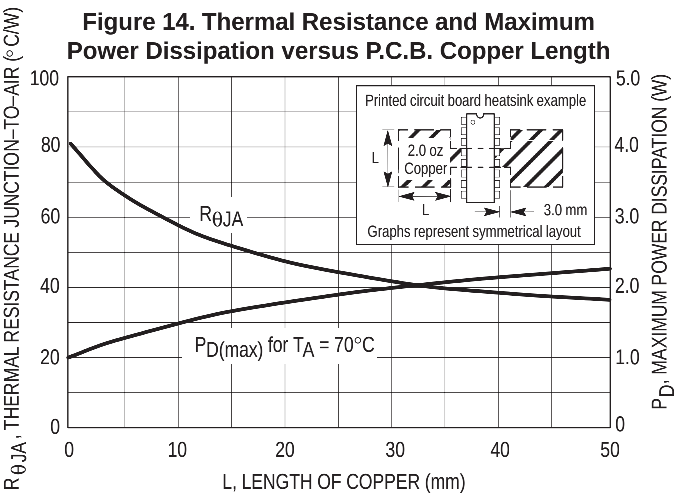


Figure 15. Propagation Delay Current Sense Input to Output versus Temperature

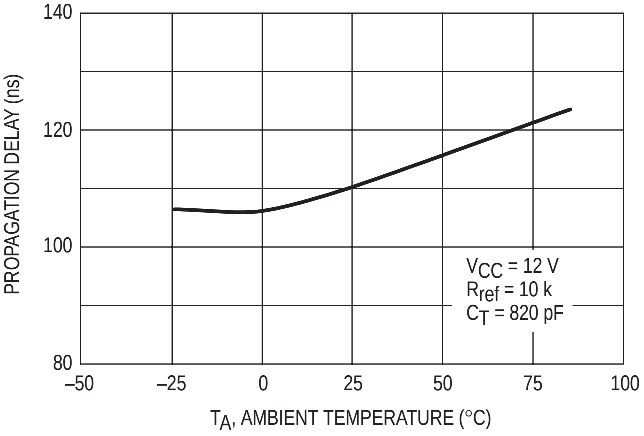


Figure 16. Startup Current versus V_{CC}

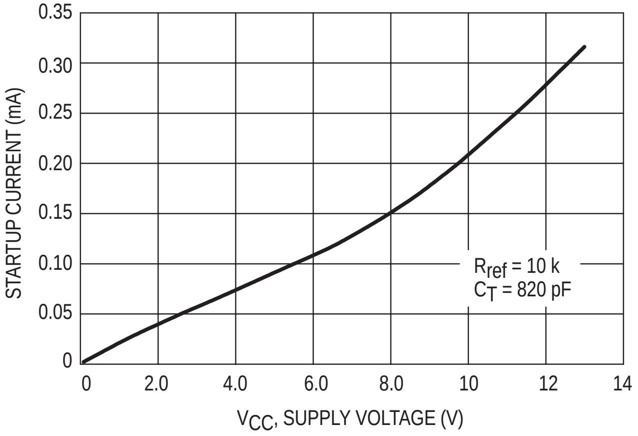


Figure 17. Supply Current versus Supply Voltage

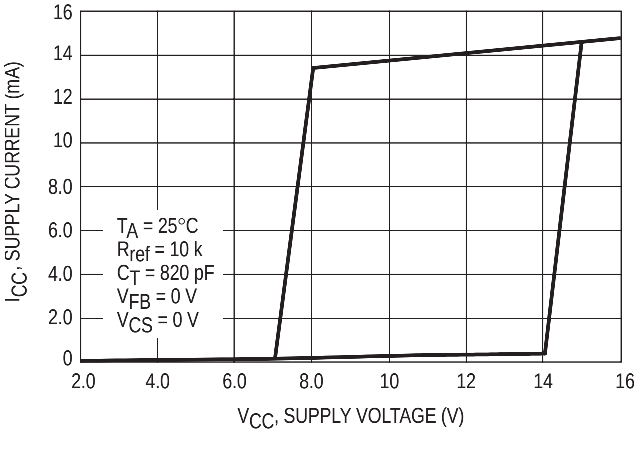


Figure 18. Power Supply Zener Voltage versus Temperature

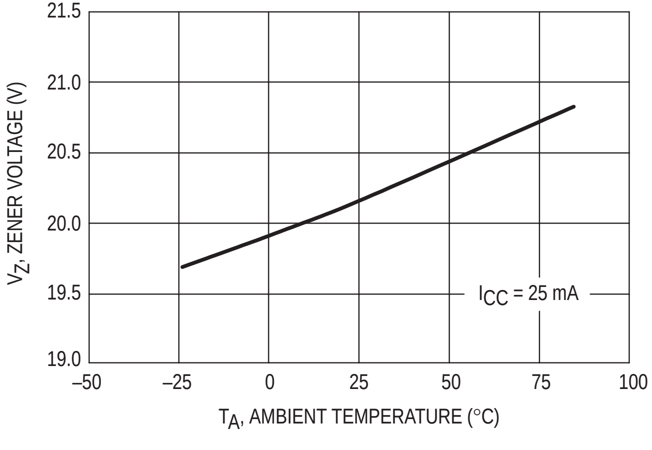


Figure 19. Startup Threshold Voltage versus Temperature

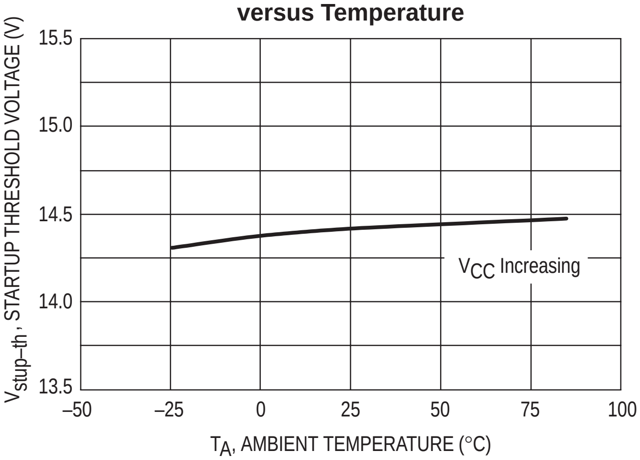


Figure 20. Disable Voltage After Threshold Turn–On (UVLO1) versus Temperature

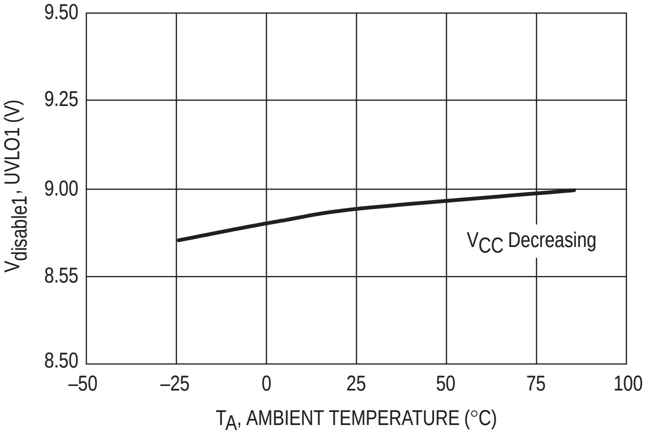


Figure 21. Disable Voltage After Threshold Turn–On (UVLO2) versus Temperature

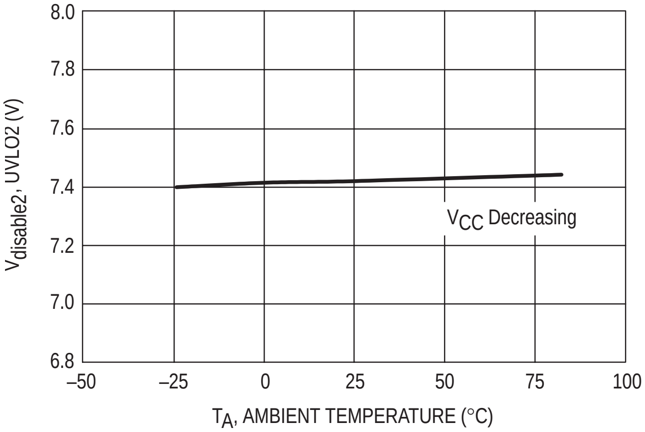


Figure 22. Protection Threshold Level on V_{OVP} versus Temperature

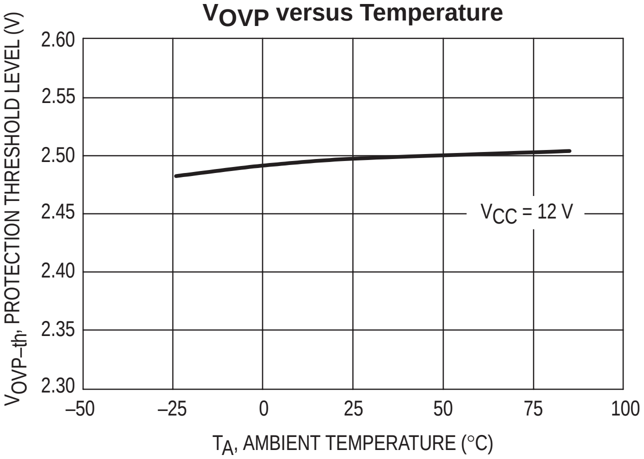


Figure 23. Protection Level on V_{CC} versus Temperature

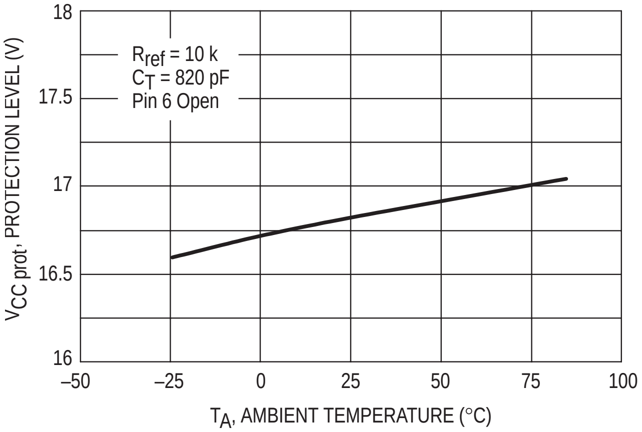


Figure 24. Propagation Delay (V_{OVP} > 2.58 V to V_{out} Low) versus Temperature

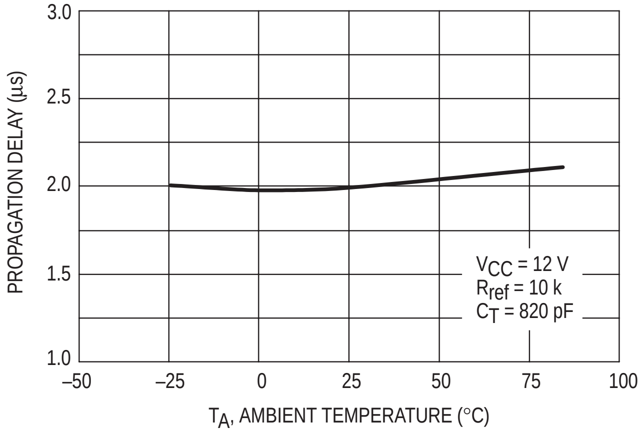


Figure 25. Standby Reference Current versus Temperature

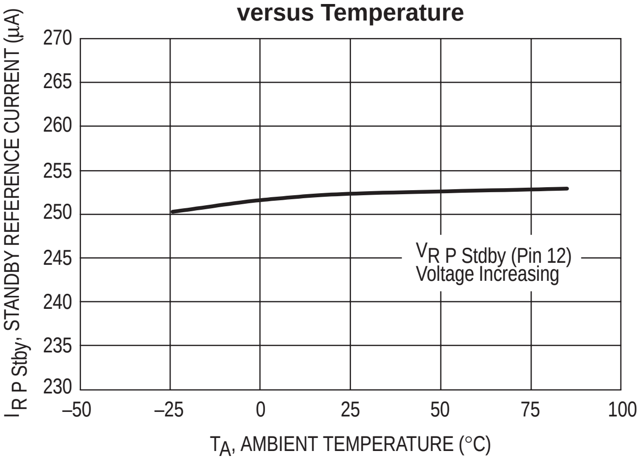
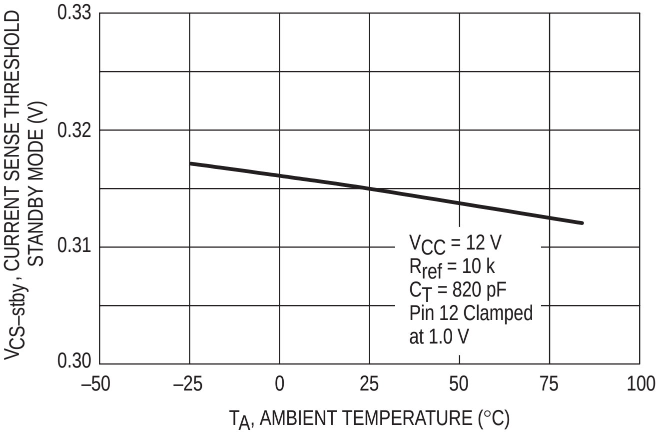


Figure 26. Current Sense Voltage Threshold Standby Mode versus Temperature



PIN FUNCTION DESCRIPTION

Pin	Name	Description
1	V_{CC}	This pin is the positive supply of the IC. The operating voltage range after startup is 9.0 to 14.5 V.
2	V_C	The output high state (V_{OH}) is set by the voltage applied to this pin. With a separate connection to the power source, it can reduce the effects of switching noise on the control circuitry.
3	Output	Peak currents up to 750 mA can be sourced or sunk, suitable for driving either MOSFET or Bipolar transistors. This output pin must be shunted by a Schottky diode, 1N5819 or equivalent.
4	Gnd	The ground pin is a single return, typically connected back to the power source; it is used as control and power ground.
5	Foldback Input	The foldback function provides overload protection. Feeding the foldback input with a portion of the V_{CC} voltage (1.0 V max) establishes on the system control loop a foldback characteristic allowing a smoother startup and sharper overload protection. Above 1.0 V the foldback input is inactive.
6	Overvoltage Protection	When the overvoltage protection pin receives a voltage greater than 17 V, the device is disabled and requires a complete restart sequence. The overvoltage level is programmable.
7	Current Sense Input	A voltage proportional to the current flowing into the power switch is connected to this input. The PWM latch uses this information to terminate the conduction of the output buffer when working in a current mode of operation. A maximum level of 1.0 V allows either current or voltage mode operation.
8	Demagnetization Detection	A voltage delivered by an auxiliary transformer winding provides to the demagnetization pin an indication of the magnetization state of the flyback transformer. A zero voltage detection corresponds to complete core saturation. The demagnetization detection ensures a discontinuous mode of operation. This function can be inhibited by connecting Pin 8 to Gnd.
9	Synchronization Input	The synchronization input pin can be activated with either a negative pulse going from a level between 0.7 V and 3.7 V to Gnd or a positive pulse going from a level between 0.7 V and 3.7 V up to a level higher than 3.7 V. The oscillator runs free when Pin 9 is connected to Gnd.
10	C_T	The normal mode oscillator frequency is programmed by the capacitor C_T choice together with the R_{ref} resistance value. C_T, connected between Pin 10 and Gnd, generates the oscillator sawtooth.
11	Soft–Start/D_{max}/ Voltage–Mode	A capacitor, resistor or a voltage source connected to this pin limits the switching duty–cycle. This pin can be used as a voltage mode control input. By connecting Pin 11 to Ground, the MC44603 can be shut down.
12	$R_{P\ Standby}$	A voltage level applied to the $R_{P\ Standby}$ pin determines the output power level at which the oscillator will turn into the reduced frequency mode of operation (i.e. standby mode). An internal hysteresis comparator allows to return in the normal mode at a higher output power level.
13	E/A Out	The error amplifier output is made available for loop compensation.
14	Voltage Feedback	This is the inverting input of the Error Amplifier. It can be connected to the switching power supply output through an optical (or other) feedback loop.
15	$R_{F\ Standby}$	The reduced frequency or standby frequency programming is made by the $R_{F\ Standby}$ resistance choice.
16	R_{ref}	R_{ref} sets the internal reference current. The internal reference current ranges from 100 µA to 500 µA. This requires that 5.0 kΩ ≤ R_{ref} ≤ 25 kΩ.

Figure 27. Starting Behavior and Overvoltage Management

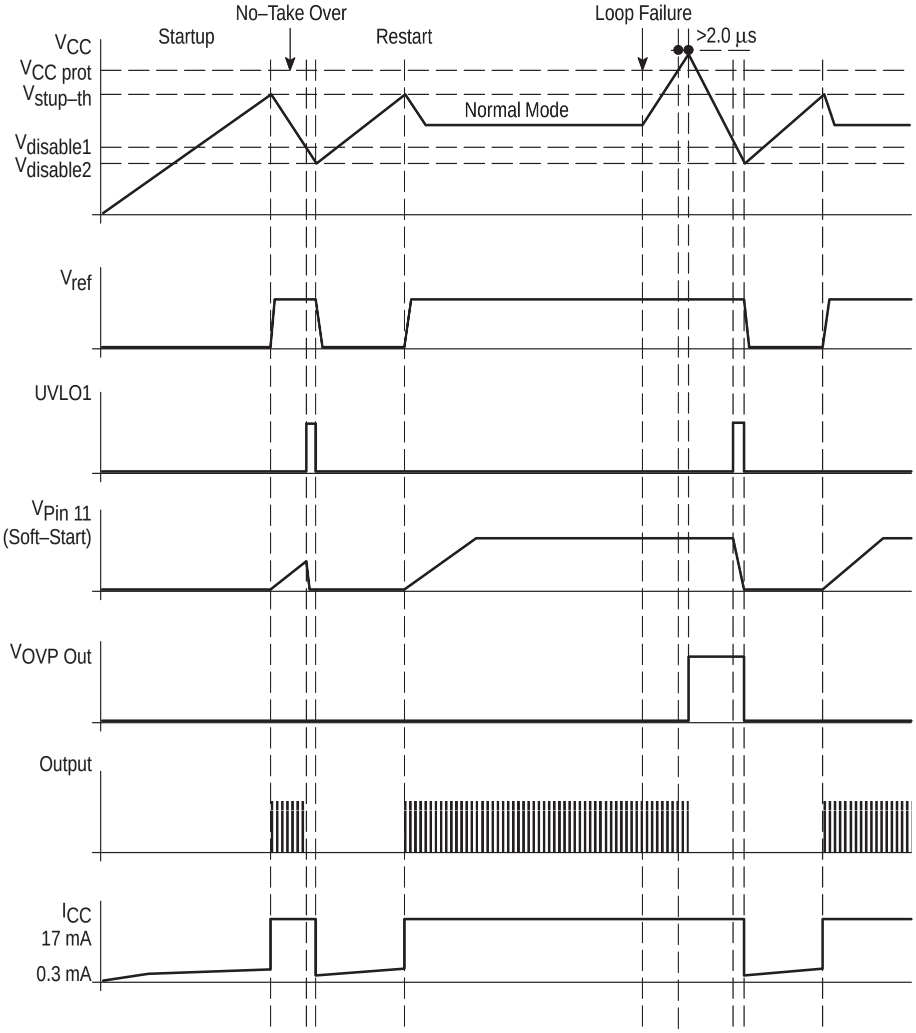


Figure 28. Demagnetization

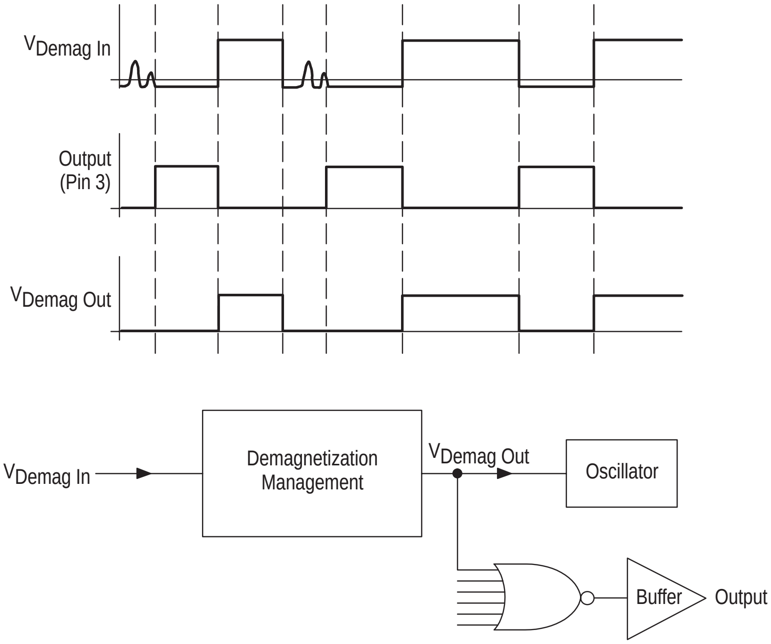


Figure 29. Switching Off Behavior

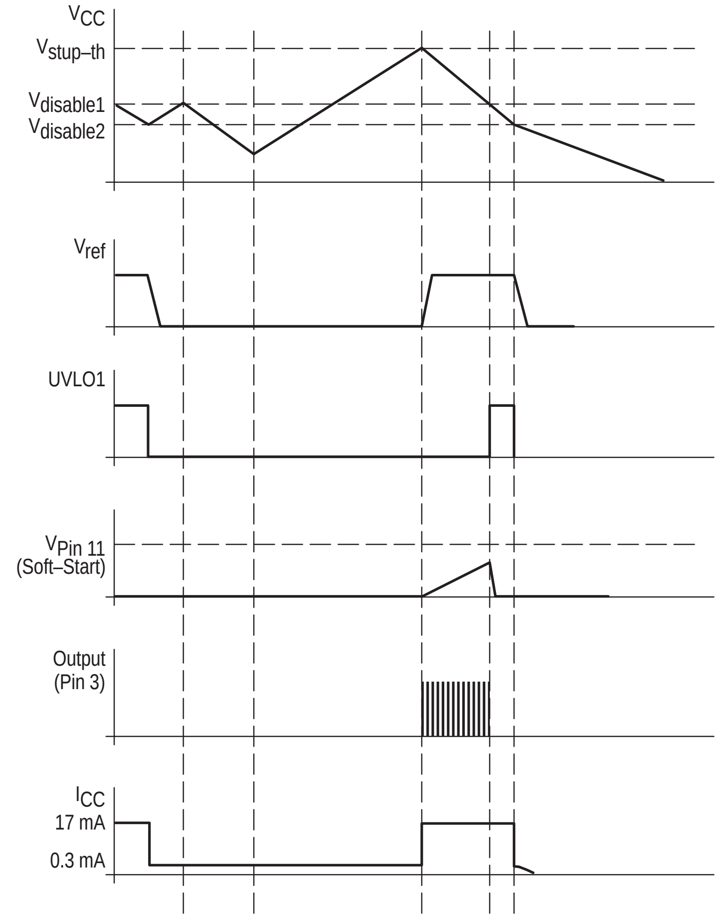
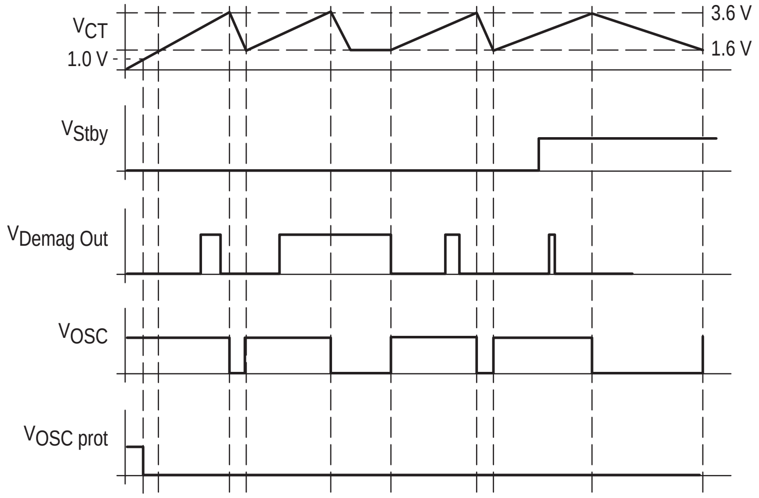


Figure 30. Oscillator



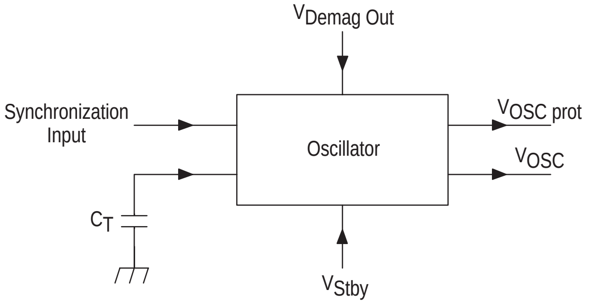
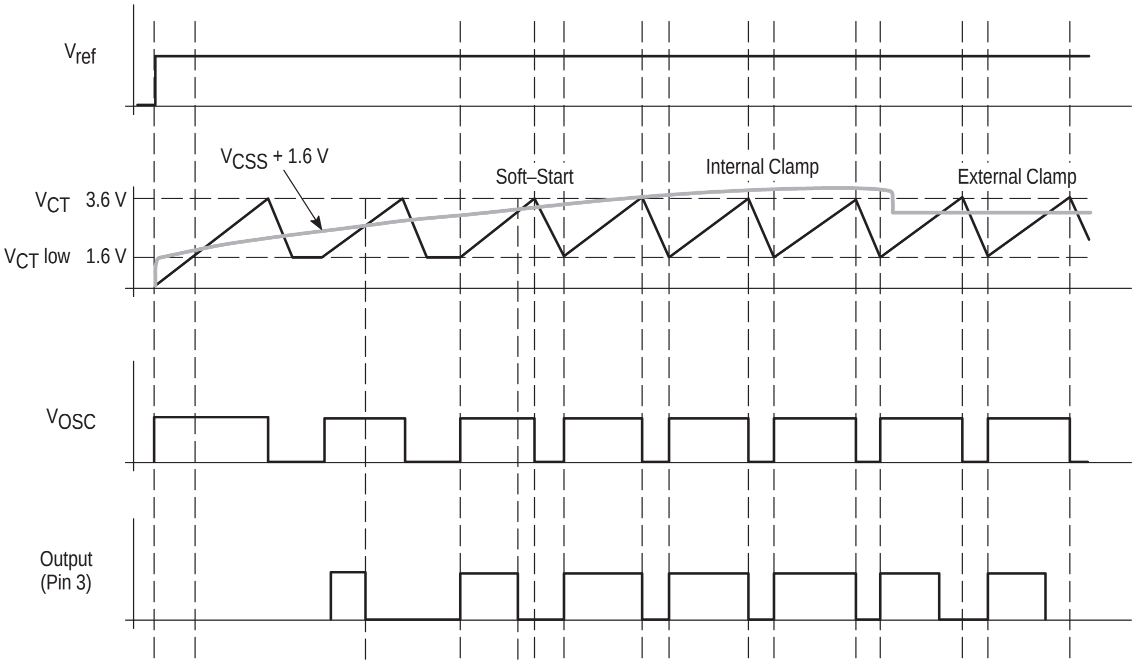


Figure 31. Soft–Start & D_{max}



OPERATING DESCRIPTION

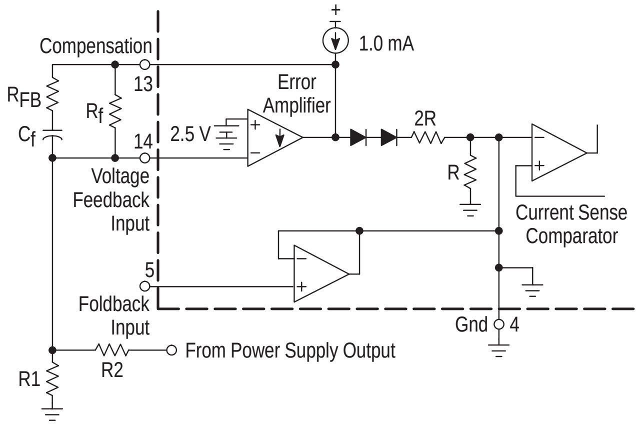
Error Amplifier

A fully compensated Error Amplifier with access to the inverting input and output is provided. It features a typical dc voltage gain of 70 dB. The noninverting input is internally biased at 2.5 V and is not pinned out. The converter output voltage is typically divided down and monitored by the inverting input. The maximum input bias current with the inverting input at 2.5 V is –2.0 µA. This can cause an output voltage error that is equal to the product of the input bias current and the equivalent input divider source resistance.

The Error Amp output (Pin 13) is provided for external loop compensation. The output voltage is offset by two diode drops (≈ 1.4 V) and divided by three before it connects to the inverting input of the Current Sense Comparator. This guarantees that no drive pulses appear at the Output (Pin 3) when Pin 13 is at its lowest state (V_{OL}). The Error Amp minimum feedback resistance is limited by the amplifier's minimum source current (0.2 mA) and the required output voltage (V_{OH}) to reach the current sense comparator's 1.0 V clamp level:

$$R_{f(min)} \approx \frac{3.0\ (1.0\ V) + 1.4\ V}{0.2\ mA} = 22\ k\Omega$$

Figure 32. Error Amplifier Compensation



Current Sense Comparator and PWM Latch

The MC44603 can operate as a current mode controller or as a voltage mode controller. In current mode operation, the MC44603 uses the current sense comparator. The output switch conduction is initiated by the oscillator and terminated when the peak inductor current reaches the threshold level established by the Error Amplifier output (Pin 13). Thus, the error signal controls the peak inductor current on a cycle–by–cycle basis. The Current Sense Comparator PWM Latch ensures that only a single pulse appears at the Source Output during the appropriate oscillator cycle.

The inductor current is converted to a voltage by inserting the ground referenced sense resistor R_S in series with the power switch Q1.

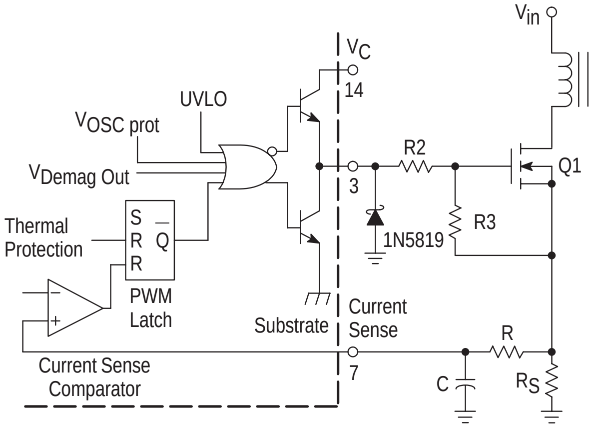
This voltage is monitored by the Current Sense Input (Pin 7) and compared to a level derived from the Error Amp output. The peak inductor current under normal operating conditions is controlled by the voltage at Pin 13 where:

$$I_{pk} \approx \frac{V_{(Pin\ 13)} - 1.4\ V}{3\ R_S}$$

The Current Sense Comparator threshold is internally clamped to 1.0 V. Therefore, the maximum peak switch current is:

$$I_{pk(max)} \approx \frac{1.0\ V}{R_S}$$

Figure 33. Output Totem Pole



Oscillator

The oscillator is a very accurate sawtooth generator that can work either in free mode or in synchronization mode. In this second mode, the oscillator stops in the low state and waits for a demagnetization or a synchronization pulse to start a new charging cycle.

- **The Sawtooth Generation:**

In the steady state, the oscillator voltage varies between about 1.6 V and 3.6 V.

The sawtooth is obtained by charging and discharging an external capacitor C_T (Pin 10), using two distinct current sources = I_{charge} and $I_{discharge}$. In fact, C_T is permanently connected to the charging current source (0.4 I_{ref}) and so, the discharge current source has to be higher than the charge current to be able to decrease the C_T voltage (refer to Figure 35).

This condition is performed, its value being (2.0 I_{ref}) in normal working and (0.4 I_{ref} + 0.5 $I_{F\ Stby}$ in standby mode).

Figure 34. Oscillator

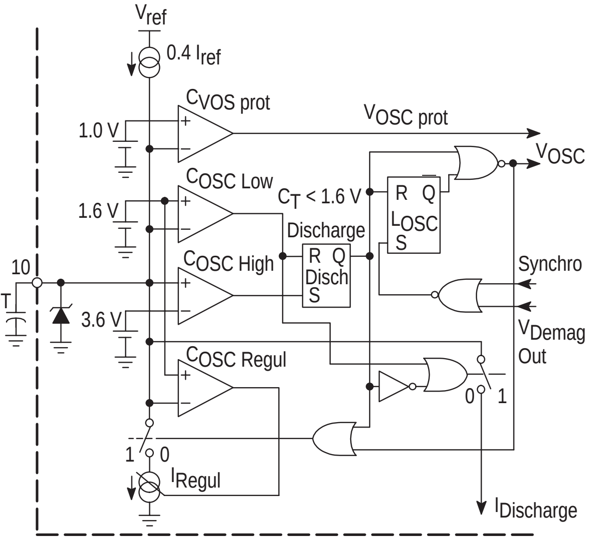
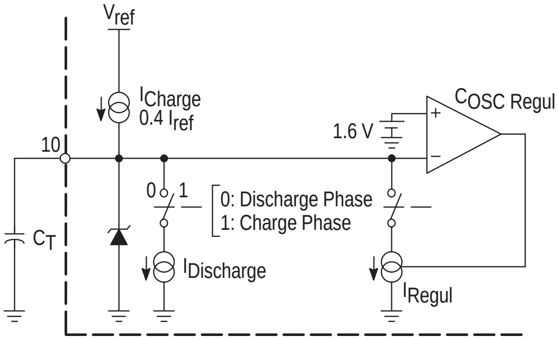


Figure 35. Simplified Block Oscillator



Two comparators are used to generate the sawtooth. They compare the C_T voltage to the oscillator valley (1.6 V) and peak reference (3.6 V) values. A latch (L_{disch}) memorizes the oscillator state.

In addition to the charge and discharge cycles, a third state can exist. This phase can be produced when, at the end of the discharge phase, the oscillator has to wait for a synchronization or demagnetization pulse before restarting. During this delay, the C_T voltage must remain equal to the oscillator valley value (≃1.6 V). So, a third regulated current source I_{Regul} controlled by $C_{OSC\ Regul}$, is connected to C_T in order to perfectly compensate the (0.4 I_{ref}) current source that permanently supplies C_T.

The maximum duty cycle is 80%. Indeed, the on–time is allowed only during the oscillator capacitor charge.

Consequently:

$T_{charge} = C_T \times \Delta V / I_{charge}$
$T_{discharge} = C_T \times \Delta V / I_{discharge}$

where:

T_{charge} is the oscillator charge time
ΔV is the oscillator peak–to–peak value
I_{charge} is the oscillator charge current

and

$T_{discharge}$ is the oscillator discharge time
$I_{discharge}$ is the oscillator discharge current

So, as $f_S = 1 / (T_{charge} + T_{discharge})$ when the Regul arrangement is not activated, the operating frequency can be obtained from the graph in Figure 1.

NOTE: The output is disabled by the signal $V_{OSC\ prot}$ when V_{CT} is lower than 1.0 V (refer to Figure 30).

Synchronization and Demagnetization Blocks

To enable the output, the L_{OSC} latch complementary output must be low. Reset is activated by the L_{disch} output during the discharge phase. To restart, the L_{OSC} has to be set (refer to Figure 34). To perform this, the demagnetization signal and the synchronization must be low.

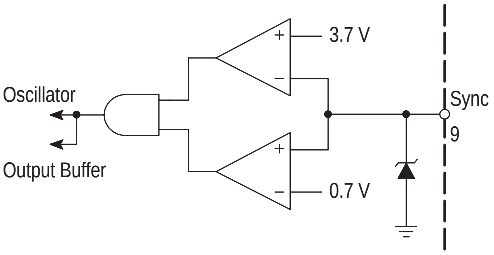
- **Synchronization:**

The synchronization block consists of two comparators that compare the synchronization signal (external) to 0.7 and 3.7 V (typical values). The comparators' outputs are connected to the input of an AND gate so that the final output of the block should be :

– high when 0.7 < SYNC < 3.7 V
– low in the other cases.

As a low level is necessary to enable the output, synchronized low level pulses have to be generated on the output of the synchronization block. If synchronization is not required, the Pin 9 must be connected to the ground.

Figure 36. Synchronization



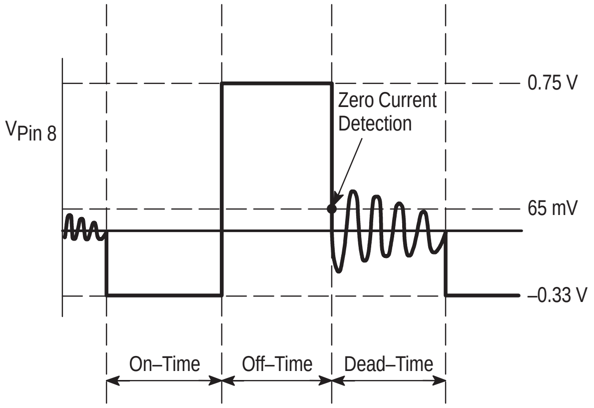
- **Demagnetization:**

In flyback applications, a good means to detect magnetic saturation of the transformer core, or demagnetization, consists in using the auxiliary winding voltage. This voltage is:

– negative during the on–time,
– positive during the off–time,
– equal to zero for the dead–time with generally some ringing (refer to Figure 37).

That is why, the MC44603 demagnetization detection consists of a comparator that can compare the auxiliary winding voltage to a reference that is typically equal to 65 mV.

Figure 37. Demagnetization Detection



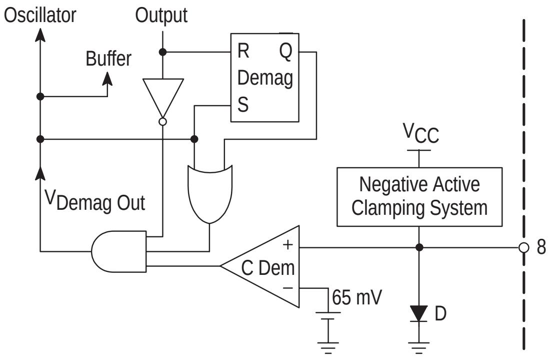
A diode D has been incorporated to clamp the positive applied voltages while an active clamping system limits the negative voltages to typically –0.33 V. This negative clamp level is sufficient to avoid the substrate diode switching on.

In addition to the comparator, a latch system has been incorporated in order to keep the demagnetization block output level low as soon as a voltage lower than 65 mV is detected and as long as a new restart is produced (high level on the output) (refer to Figure 38). This process prevents ringing on the signal at Pin 8 from disrupting the demagnetization detection. This results in a very accurate demagnetization detection.

The demagnetization block output is also directly connected to the output, disabling it during the demagnetization phase (refer to Figure 33).

NOTE: The demagnetization detection can be inhibited by connecting Pin 8 to the ground.

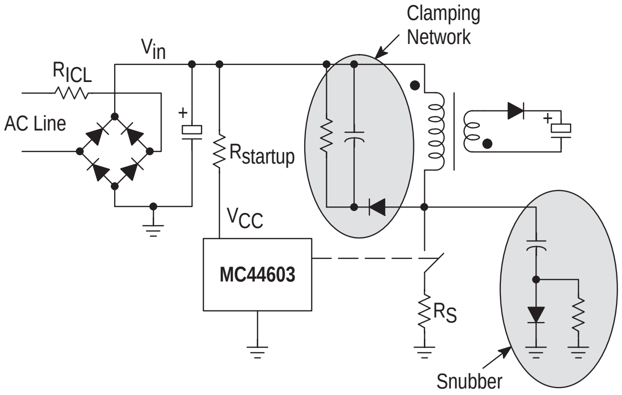
Figure 38. Demagnetization Block



Standby

- **Power Losses in a Classical Flyback Structure**

Figure 39. Power Losses in a Classical Flyback Structure



In a classical flyback (as depicted in Figure 39), the standby losses mainly consist of the energy waste due to:

– the startup resistor $R_{startup}$ → $P_{startup}$
– the consumption of the IC and the power switch control → $P_{control}$
– the inrush current limitation resistor R_{ICL} → P_{ICL}
– the switching losses in the power switch → P_{SW}
– the snubber and clamping network → $P_{SN–CLN}$

$P_{startup}$ is nearly constant and is equal to:

$$\left((V_{in} - V_{CC})^2 / R_{startup}\right)$$

P_{ICL} only depends on the current drawn from the mains. Losses can be considered constant. This waste of energy decreases when the standby losses are reduced.

$P_{control}$ increases when the oscillator frequency is increased (each switching requires some energy to turn on the power switch).

P_{SW} and $P_{SN–CLN}$ are proportional to the switching frequency.

Consequently, standby losses can be minimized by decreasing the switching frequency as much as possible.

The MC44603 was designed to operate at a standby frequency lower than the normal working one.

- **Standby Power Calculations with MC44603**

During a switching period, the energy drawn by the transformer during the on–time to be transferred to the output during the off–time, is equal to:

$$E = \frac{1}{2} \times L \times I_{pk}^2$$

where:

– L is the transformer primary inductor,
– I_{pk} is the inductor peak current.

Input power is labelled P_{in}:

$$P_{in} = 0.5 \times L \times I_{pk}^2 \times f_S$$

where f_S is the normal working switching frequency.

Also,

$$I_{pk} = \frac{V_{CS}}{R_S}$$

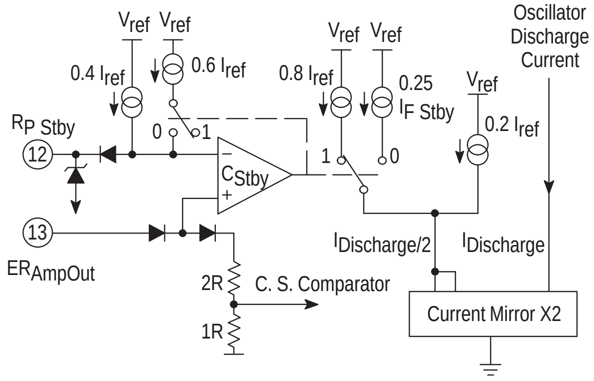
where R_S is the resistor used to measure the power switch current.

Thus, the input power is proportional to V_{CS}^2 (V_{CS} being the internal current sense comparator input).

That is why the standby detection is performed by creating a V_{CS} threshold. An internal current source (0.4 x I_{ref}) sets the threshold level by connecting a resistor to Pin 12.

As depicted in Figure 40, the standby comparator noninverting input voltage is typically equal to (3.0 x V_{CS} + V_F) while the inverter input value is ($V_{R\ P\ Stby}$ + V_F).

Figure 40. Standby



The V_{CS} threshold level is typically equal to [($V_{R\ P\ Stby}$)/3] and if the corresponding power threshold is labelled P_{thL}:

$$P_{thL} = 0.5 \times L \times \left(\frac{V_{R\ P\ Stby}}{3.0\ R_S}\right)^2 \times f_S$$

And as:

$$V_{R\ P\ Stby} = R_{P\ Stby} \times 0.4 \times I_{ref}$$

$$= R_{R\ P\ Stby} \times 0.4 \times \frac{V_{ref}}{R_{ref}}$$

$$R_{P\ Stby} = \frac{10.6 \times R_S \times R_{ref}}{V_{ref}} \times \sqrt{\frac{P_{thL}}{L \times f_S}}$$

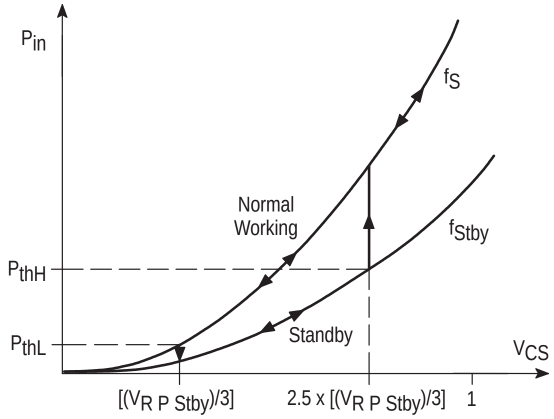
Thus, when the power drawn by the converter decreases, V_{CS} decreases and when V_{CS} becomes lower than [$V_{CS–th}$ x ($V_{R\ P\ Stby}$)/3], the standby mode is activated. This results in an oscillator discharge current reduction in order to increase the oscillator period and to diminish the switching frequency. As it is represented in Figure 40, the (0.8 x I_{ref}) current source is disconnected and is replaced by a lower value one (0.25 x $I_{F\ Stby}$).

Where: $I_{F\ Stby} = V_{ref}/R_{F\ Stby}$

In order to prevent undesired mode switching when power is close to the threshold value, a hysteresis that is proportional to $V_{R\ P\ Stby}$ is incorporated creating a second V_{CS} threshold level that is equal to [2.5 x ($V_{R\ P\ Stby}$)/3]. When the standby comparator output is high, a second current source (0.6 x I_{ref}) is connected to Pin 12.

Finally, the standby mode function can be shown graphically in Figure 41.

Figure 41. Dynamic Mode Change



This curve shows that there are two power threshold levels:

– the low one:

P_{thL} fixed by $V_{R\ P\ Stby}$

– the high one:

$$P_{thH} = (2.5)^2 \times P_{thL} \times \frac{f_{Stby}}{f_S}$$

$$P_{thH} = 6.25 \times P_{thL} \times \frac{f_{Stby}}{f_S}$$

Maximum Duty Cycle and Soft–Start Control

Maximum duty cycle can be limited to values less than 80% by utilizing the D_{max} and soft–start control. As depicted in Figure 42, the Pin 11 voltage is compared to the oscillator sawtooth.

Figure 42. D_{max} and Soft–Start

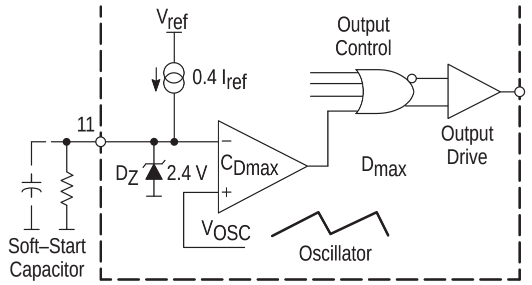
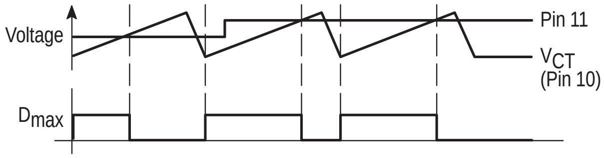


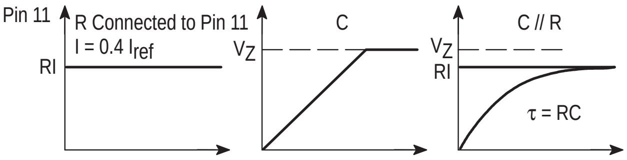
Figure 43. Maximum Duty Cycle Control



Using the internal current source (0.4 I_{ref}), the Pin 11 voltage can easily be set by connecting a resistor to this pin.

If a capacitor is connected to Pin 11, the voltage increases from 0 to its maximum value progressively (refer to Figure 44), thereby, implementing a soft–start. The soft–start capacitor is discharged internally when the V_{CC} (Pin 1) voltage drops below 9.0 V.

Figure 44. Different Possible Uses of Pin 11



If no external component is connected to Pin 11, an internal zener diode clamps the Pin 11 voltage to a value V_Z that is higher than the oscillator peak value, disabling soft–start and maximum duty cycle limitation.

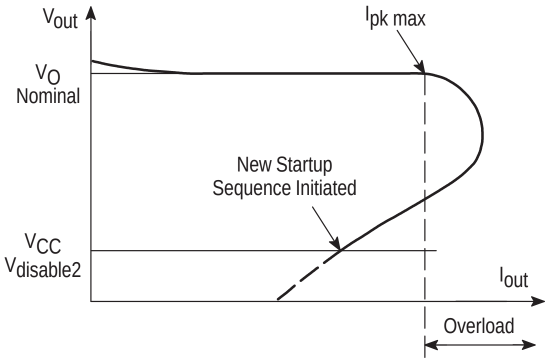
Foldback

As depicted in Fgure 32, the foldback input (Pin 5) can be used to reduce the maximum V_{CS} value, providing foldback protection. The foldback arrangement is a programmable peak current limitation.

If the output load is increased, the required converter peak current becomes higher and V_{CS} increases until it reaches its maximum value (normally, $V_{CS\ max} = 1.0$ V).

Then, if the output load keeps on increasing, the system is unable to supply enough energy to maintain the output voltages in regulation. Consequently, the decreasing output can be applied to Pin 5, in order to limit the maximum peak current. In this way, the well known foldback characteristic can be obtained (refer to Figure 45).

Figure 45. Foldback Characteristic



NOTE: Foldback is disabled by connecting Pin 5 to V_{CC}.

Overvoltage Protection

The overvoltage arrangement consists of a comparator that compares the Pin 6 voltage to V_{ref} (2.5 V) (refer to Figure 46).

If no external component is connected to Pin 6, the comparator noninverting input voltage is nearly equal to:

$$\left(\frac{2.0\ \text{k}\Omega}{11.6\ \text{k}\Omega + 2.0\ \text{k}\Omega}\right) \text{x}\ V_{CC}$$

The comparator output is high when:

$$\left(\frac{2.0\ \text{k}\Omega}{11.6\ \text{k}\Omega + 2.0\ \text{k}\Omega}\right) \text{x}\ V_{CC} \geq 2.5\ \text{V}$$

$$\Leftrightarrow V_{CC} \geq 17\ \text{V}$$

A delay latch (2.0 µs) is incorporated in order to sense overvoltages that last at least 2.0 µs.

If this condition is achieved, $V_{OVP\ out}$, the delay latch output, becomes high. As this level is brought back to the input through an OR gate, $V_{OVP\ out}$ remains high (disabling the IC output) until V_{ref} is disabled.

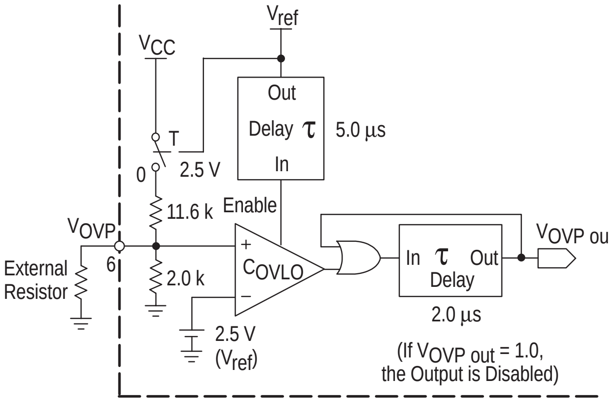
Consequently, when an overvoltage longer than 2.0 µs is detected, the output is disabled until V_{CC} is removed and then re–applied.

The V_{CC} is connected after V_{ref} has reached steady state in order to limit the circuit startup consumption.

The overvoltage section is enabled 5.0 µs after the regulator has started to allow the reference V_{ref} to stabilize.

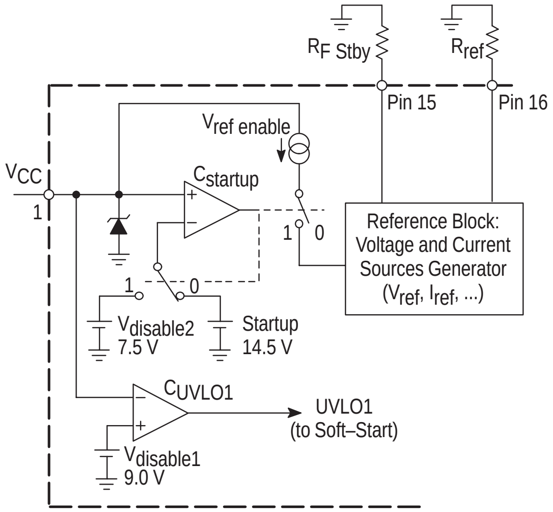
By connecting an external resistor to Pin 6, the threshold V_{CC} level can be changed.

Figure 46. Overvoltage Protection



Undervoltage Lockout Section

Figure 47. V_{CC} Management



As depicted in Figure 47, an undervoltage lockout has been incorporated to garantee that the IC is fully functional before allowing system operation.

This block particularly, produces V_{ref} (Pin 16 voltage) and I_{ref} that is determined by the resistor R_{ref} connected between Pin 16 and the ground:

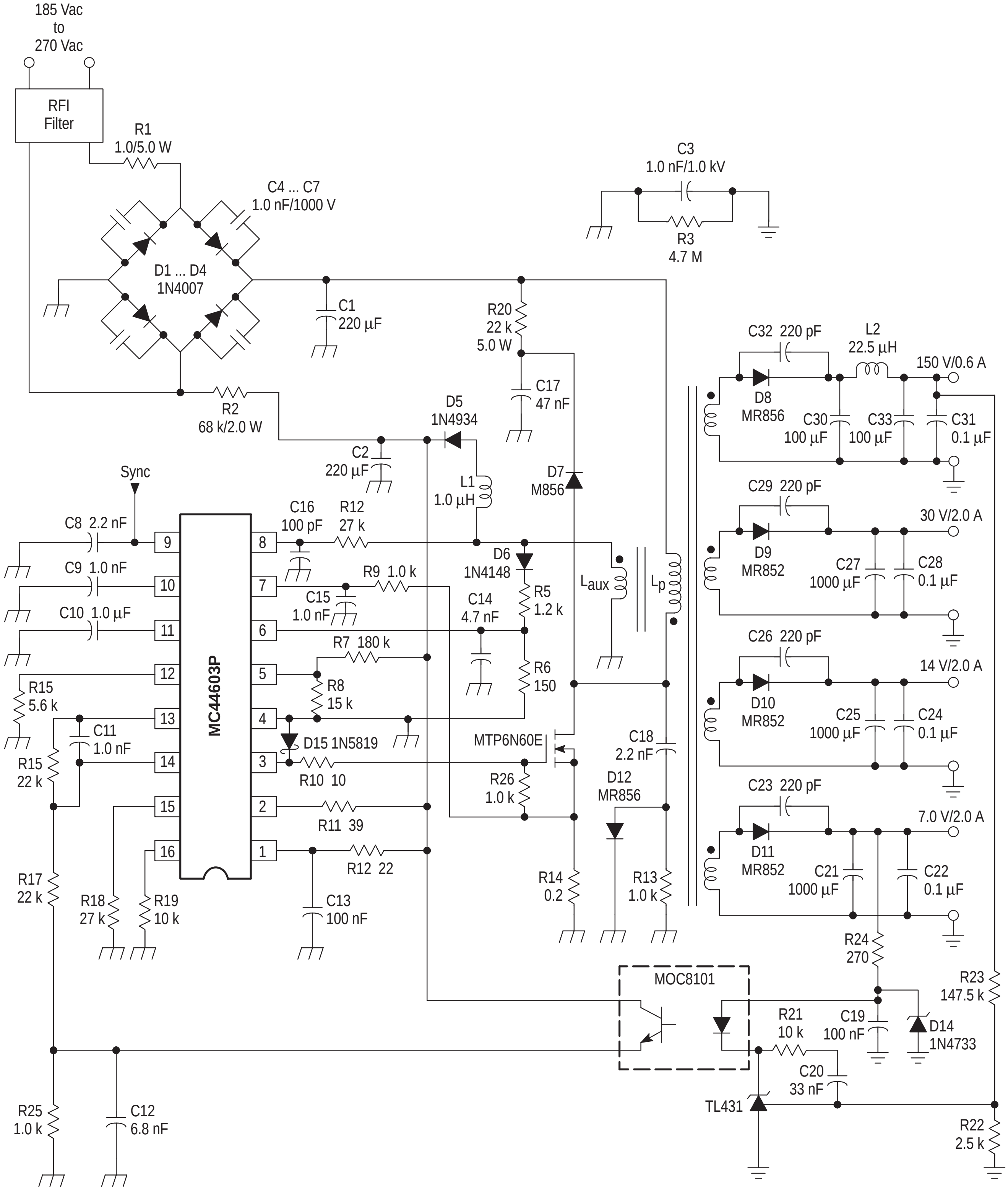
$$I_{ref} = \frac{V_{ref}}{R_{ref}} \text{ where } V_{ref} = 2.5 \text{ V (typically)}$$

Another resistor is connected to the Reference Block: $R_{F\ Stby}$ that is used to fix the standby frequency.

In addition to this, V_{CC} is compared to a second threshold level that is nearly equal to 9.0 V ($V_{disable1}$). UVLO1 is generated to reset the maximum duty cycle and soft–start block disabling the output stage as soon as V_{CC} becomes lower than $V_{disable1}$. In this way, the circuit is reset and made ready for the next startup, before the reference block is disabled (refer to Figure 29). Finally, the upper limit for the minimum normal operating voltage is 9.4 V (maximum value of $V_{disable1}$) and so the minimum hysteresis is 4.2 V. ($(V_{stup–th})_{min} = 13.6$ V).

The large hysteresis and the low startup current of the MC44603 make it ideally suited for off–line converter applications where efficient bootstrap startup techniques are required.

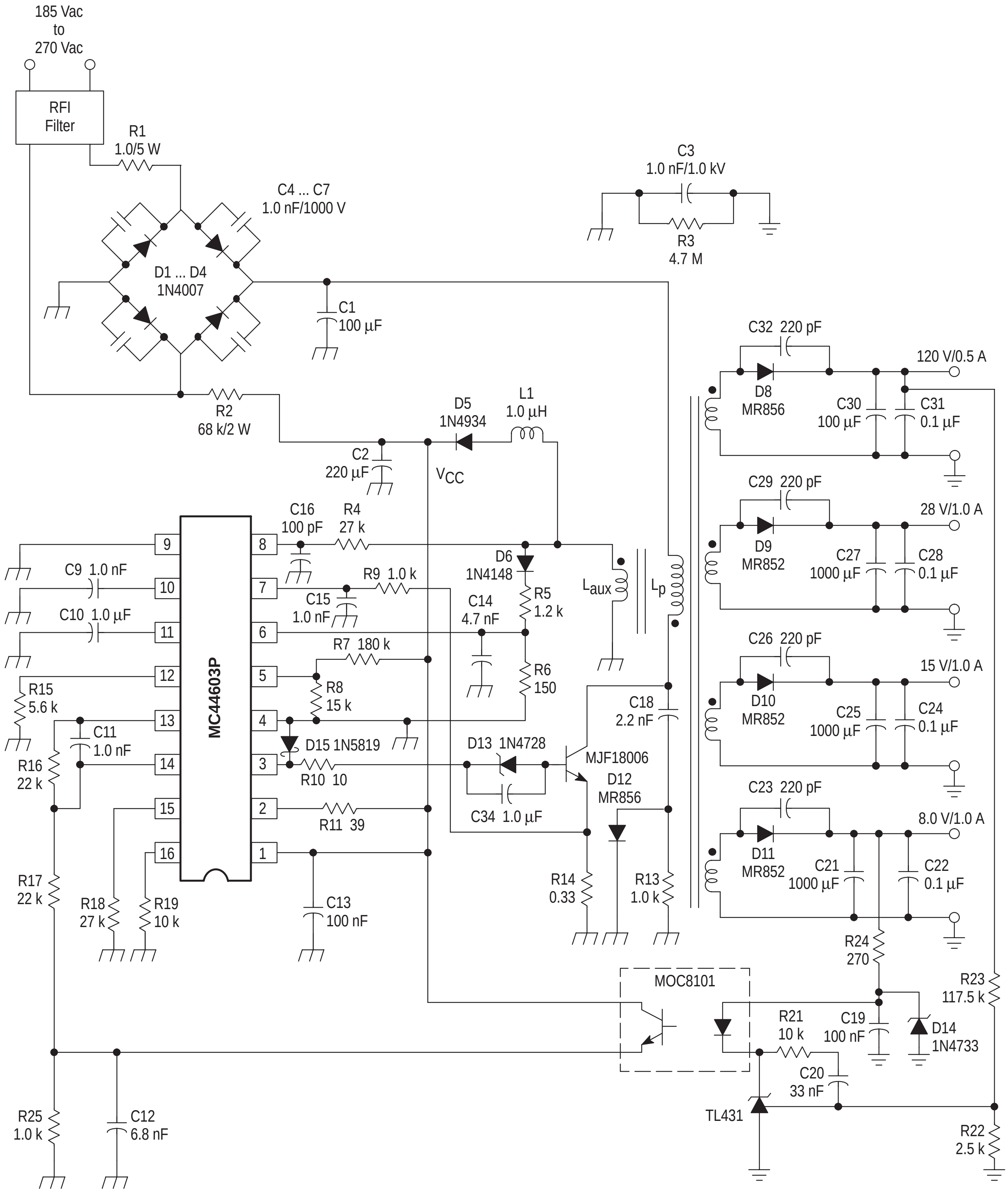
Figure 48. 250 W Input Power Off–Line Flyback Converter with MOSFET Switch



250 W Input Power Fly–Back Converter
185 V – 270 V Mains Range
MC44603P & MTP6N60E

Tests	Conditions	Results
Line Regulation	V_{in} = 185 Vac to 270 Vac F_{mains} = 50 Hz	
150 V	I_{out} = 0.6 A	10 mV
30 V	I_{out} = 2.0 A	10 mV
14 V	I_{out} = 2.0 A	10 mV
7.0 V	I_{out} = 2.0 A	20 mV
Load Regulation	V_{in} = 220 Vac	
150 V	I_{out} = 0.3 A to 0.6 A	50 mV
Cross Regulation	V_{in} = 220 Vac I_{out} (150 V) = 0.6 A I_{out} (30 V) = 0 A to 2.0 A I_{out} (14 V) = 2.0 A I_{out} (7.0 V) = 2.0 A	
150 V		< 1.0 mV
Efficiency	V_{in} = 220 Vac, P_{in} = 250 W	81%
Standby Mode		
P input	V_{in} = 220 Vac, P_{out} = 0 W	3.3 W
Switching Frequency		20 kHz fully stable
Output Short Circuit	$P_{out\ (max)}$ = 270 W	Safe on all outputs
Startup	P_{in} = 250 W	Vac = 160 V

Figure 49. 125 W Input Power Off–Line Flyback Converter with Bipolar Switch



125 W Input Power Fly–Back Converter
185 V – 270 V Mains Range
MC44603P & MJF18006

Tests	Conditions	Results
Line Regulation	V_{in} = 185 Vac to 270 Vac F_{mains} = 60 Hz	
120 V	I_{out} = 0.5 A	10 mV
28 V	I_{out} = 1.0 A	10 mV
15 V	I_{out} = 1.0 A	10 mV
8.0 V	I_{out} = 1.0 A	20 mV
Load Regulation	V_{in} = 220 Vac	
120 V	I_{out} = 0.2 A to 0.5 A	= 0.05 V
Cross Regulation	V_{in} = 220 Vac I_{out} (120 V) = 0.5 A I_{out} (28 V) = 0 A to 1.0 A I_{out} (15 V) = 1.0 A I_{out} (8.0 V) = 1.0 A	
120 V		< 1.0 mV
Efficiency	V_{in} = 220 Vac, P_{in} = 125 W	85%
Standby Mode		
P input	V_{in} = 220 Vac, P_{out} = 0 W	2.46 W
Switching Frequency		20 kHz fully stable
Output Short Circuit	$P_{out\ (max)}$ = 140 W	Safe on all outputs
Startup	P_{in} = 125 W	Vac = 150 V

MC44604

Product Preview

High Safety Standby Ladder Mode GreenLine™ PWM Controller

The MC44604 is an enhanced high performance controller that is specifically designed for off–line and dc–to–dc converter applications.

The MC44604 is a modification of the MC44603. The MC44604 offers enhanced safety and reliable power management in its protection features (foldback, overvoltage detection, soft–start, accurate demagnetization detection). Its high current totem pole output is also ideally suited for driving a power MOSFET but can also be used for driving a bipolar transistor in low power converters (< 150 W).

In addition, the MC44604 offers a new efficient way to reduce the standby operating power by means of a patented standby ladder mode operation of the converter significantly reducing the converter consumption in standby mode.

Current or Voltage Mode Controller

- Operation Up to 250 kHz Output Switching Frequency
- Inherent Feed Forward Compensation
- Latching PWM for Cycle–by–Cycle Current Limiting
- Oscillator with Precise Frequency Control

High Flexibility

- Externally Programmable Reference Current
- Secondary or Primary Sensing
- High Current Totem Pole Output
- Undervoltage Lockout with Hysteresis

Safety/Protection Features

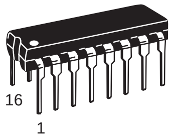
- Overvoltage Protection Facility Against Open Loop
- Protection Against Short Circuit on Oscillator Pin
- Fully Programmable Foldback
- Soft–Start Feature
- Accurate Maximum Duty Cycle Setting
- Demagnetization (Zero Current Detection) Protection
- Internally Trimmed Reference

GreenLine™ Controller:

- Low Startup and Operating Current
- Patented Standby Ladder Mode for Low Standby Losses
- Low dV/dT for Low EMI

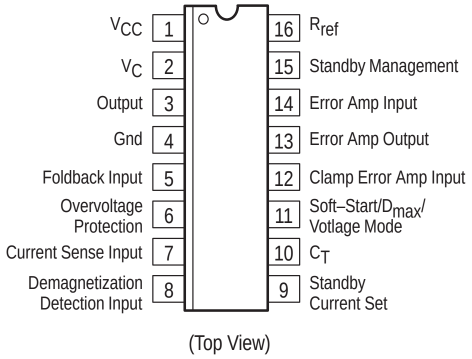
HIGH SAFETY STANDBY LADDER MODE GREENLINE™ PWM CONTROLLER

SEMICONDUCTOR
TECHNICAL DATA



P SUFFIX
PLASTIC PACKAGE
CASE 648

PIN CONNECTIONS



ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC44604P	T_A = –25° to +85°C	Plastic DIP

MOTOROLA

Product Preview

High Safety Latched Mode GreenLine™ PWM Controller for (Multi)Synchronized Applications

The MC44605 is a high performance current mode controller that is specifically designed for off–line converters. The MC44605 has several distinguishing features that make it particularly suitable for multisynchronized monitor applications.

The MC44605 synchronization arrangement enables operation from 16 kHz up to 130 kHz. This product was optimized to operate with universal ac mains voltage from 80 V to 280 V, and its high current totem pole output makes it ideally suited for driving a power MOSFET.

The MC44605 protections provide well controlled, safe power management. Safety enhancements detect four different fault conditions and provide protection through a disabling latch.

Current or Voltage Mode Controller

- Current Mode Operation Up to 250 kHz Output Switching Frequency
- Inherent Feed Forward Compensation
- Latching PWM for Cycle–by–Cycle Current Limiting
- Oscillator with Precise Frequency Control
- Externally Programmable Reference Current
- Secondary or Primary Sensing (Availability of Error Amplifier Output)
- Synchronization Facility
- High Current Totem Pole Output
- Undervoltage Lockout with Hysteresis
- Low Output dV/dT for Low EMI
- Low Startup and Operating Current

Safety/Protection Features

- Soft–Start Feature
- Demagnetization (Zero Current Detection) Protection
- Overvoltage Protection Facility Against Open Loop
- EHT Overvoltage Protection (E.H.T.OVP): Protection Against Excessive Amplitude Synchronization Pulses
- Winding Short Circuit Detection (W.S.C.D.)
- Limitation of the Maximum Input Power (M.P.L.): Calculation of Input Power for Overload Protection
- Over Heating Detection (O.H.D.): to Prevent the Power Switch from Excessive Heating

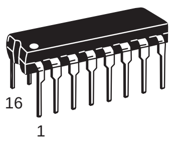
Latched Disabling Mode

- When one of the following faults is detected: EHT overvoltage, Winding Short Circuit (WSCD), excessive input power (M.P.L.), power switch over heating (O.H.D.), a counter is activated
- If the counter is activated for a time that is long enough, the circuit gets definitively disabled. The latch can only be reset by removing and then re–applying power

MC44605

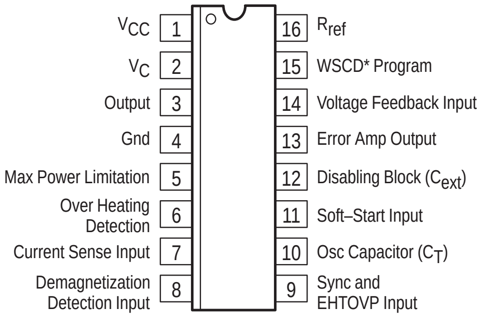
HIGH SAFETY LATCHED MODE GREENLINE™ PWM CONTROLLER FOR (MULTI)SYNCHRONIZED APPLICATIONS

SEMICONDUCTOR TECHNICAL DATA



P SUFFIX
PLASTIC PACKAGE
CASE 648

PIN CONNECTIONS



(Top View)

* Winding Short Circuit Detection

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC44605P	T_A = –25° to +85°C	Plastic DIP

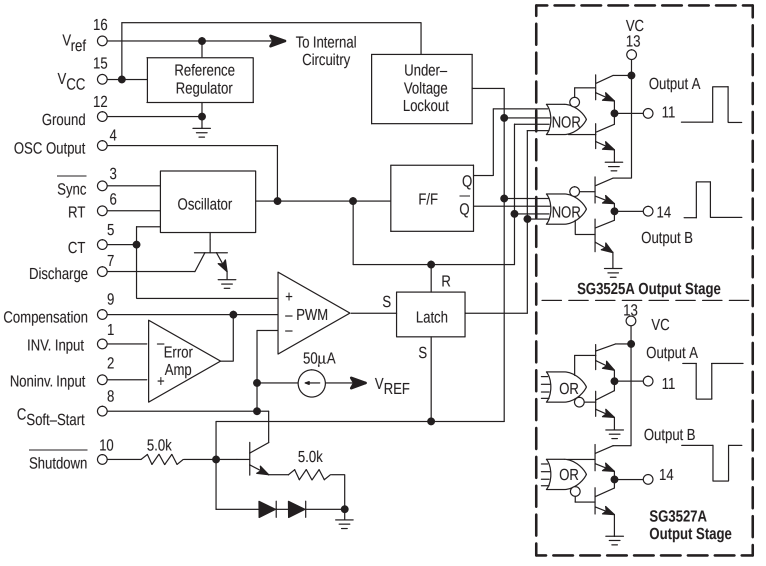
SG3525A
SG3527A

Pulse Width Modulator Control Circuits

The SG3525A, SG3527A pulse width modulator control circuits offer improved performance and lower external parts count when implemented for controlling all types of switching power supplies. The on–chip +5.1 V reference is trimmed to ±1% and the error amplifier has an input common–mode voltage range that includes the reference voltage, thus eliminating the need for external divider resistors. A sync input to the oscillator enables multiple units to be slaved or a single unit to be synchronized to an external system clock. A wide range of deadtime can be programmed by a single resistor connected between the C_T and Discharge pins. These devices also feature built–in soft–start circuitry, requiring only an external timing capacitor. A shutdown pin controls both the soft–start circuitry and the output stages, providing instantaneous turn off through the PWM latch with pulsed shutdown, as well as soft–start recycle with longer shutdown commands. The under voltage lockout inhibits the outputs and the changing of the soft–start capacitor when V_{CC} is below nominal. The output stages are totem–pole design capable of sinking and sourcing in excess of 200 mA. The output stage of the SG3525A features NOR logic resulting in a low output for an off–state while the SG3527A utilized OR logic which gives a high output when off.

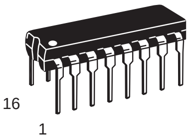
- 8.0 V to 35 V Operation
- 5.1 V ± 1.0% Trimmed Reference
- 100 Hz to 400 kHz Oscillator Range
- Separate Oscillator Sync Pin
- Adjustable Deadtime Control
- Input Undervoltage Lockout
- Latching PWM to Prevent Multiple Pulses
- Pulse–by–Pulse Shutdown
- Dual Source/Sink Outputs: ±400 mA Peak

Representative Block Diagram

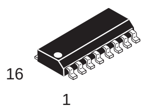


PULSE WIDTH MODULATOR CONTROL CIRCUITS

SEMICONDUCTOR TECHNICAL DATA

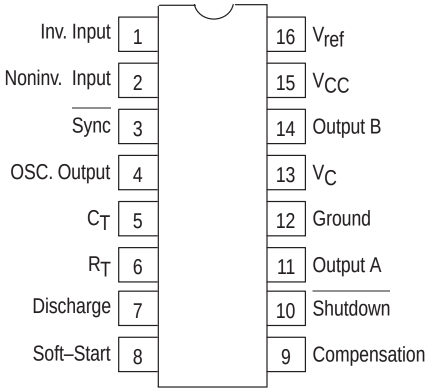


N SUFFIX
PLASTIC PACKAGE
CASE 648



DW SUFFIX
PLASTIC PACKAGE
CASE 751B
(SO–16L)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
SG3525AN	T_A = 0° to +70°C	Plastic DIP
SG3525ADW		SO–16L
SG3527AN		Plastic DIP

MAXIMUM RATINGS (Note 1)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	+40	Vdc
Collector Supply Voltage	V_C	+40	Vdc
Logic Inputs		–0.3 to +5.5	V
Analog Inputs		–0.3 to V_{CC}	V
Output Current, Source or Sink	I_O	±500	mA
Reference Output Current	I_{ref}	50	mA
Oscillator Charging Current		5.0	mA
Power Dissipation (Plastic & Ceramic Package) T_A = +25°C (Note 2) T_C = +25°C (Note 3)	P_D	 1000 2000	mW
Thermal Resistance Junction–to–Air	$R_{\theta JA}$	100	°C/W
Thermal Resistance Junction–to–Case	$R_{\theta JC}$	60	°C/W
Operating Junction Temperature	T_J	+150	°C
Storage Temperature Range	T_{stg}	–55 to +125	°C
Lead Temperature (Soldering, 10 seconds)	T_{Solder}	+300	°C

NOTES: 1. Values beyond which damage may occur.
2. Derate at 10 mW/°C for ambient temperatures above +50°C.
3. Derate at 16 mW/°C for case temperatures above +25°C.

RECOMMENDED OPERATING CONDITIONS

Characteristics	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	8.0	35	Vdc
Collector Supply Voltage	V_C	4.5	35	Vdc
Output Sink/Source Current (Steady State) (Peak)	I_O	 0 0	 ±100 ±400	mA
Reference Load Current	I_{ref}	0	20	mA
Oscillator Frequency Range	f_{osc}	0.1	400	kHz
Oscillator Timing Resistor	R_T	2.0	150	kΩ
Oscillator Timing Capacitor	C_T	0.001	0.2	µF
Deadtime Resistor Range	R_D	0	500	Ω
Operating Ambient Temperature Range	T_A	0	+70	°C

APPLICATION INFORMATION

Shutdown Options (See Block diagram, front page)

Since both the compensation and soft–start terminals (Pins 9 and 8) have current source pull–ups, either can readily accept a pull–down signal which only has to sink a maximum of 100 µA to turn off the outputs. This is subject to the added requirement of discharging whatever external capacitance may be attached to these pins.

An alternate approach is the use of the shutdown circuitry of Pin 10 which has been improved to enhance the available shutdown options. Activating this circuit by applying a positive signal on Pin 10 performs two functions: the PWM latch is immediately set providing the fastest turn–off signal to the outputs; and a 150 µA current sink begins to discharge the external soft–start capacitor. If the shutdown command is short, the PWM signal is terminated without significant discharge of the soft–start capacitor, thus, allowing, for example, a convenient implementation of pulse–by–pulse current limiting. Holding Pin 10 high for a longer duration, however, will ultimately discharge this external capacitor, recycling slow turn–on upon release.

Pin 10 should not be left floating as noise pickup could conceivably interrupt normal operation.

ELECTRICAL CHARACTERISTICS (V_{CC} = +20 Vdc, T_A = T_{low} to T_{high} [Note 4], unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
REFERENCE SECTION					
Reference Output Voltage (T_J = +25°C)	V_{ref}	5.00	5.10	5.20	Vdc
Line Regulation (+8.0 V ≤ V_{CC} ≤ +35 V)	Reg_{line}	–	10	20	mV
Load Regulation (0 mA ≤ I_L ≤ 20 mA)	Reg_{load}	–	20	50	mV
Temperature Stability	$\Delta V_{ref}/\Delta T$	–	20	–	mV
Total Output Variation Includes Line and Load Regulation over Temperature	ΔV_{ref}	4.95	–	5.25	Vdc
Short Circuit Current (V_{ref} = 0 V, T_J = +25°C)	I_{SC}	–	80	100	mA
Output Noise Voltage (10 Hz ≤ f ≤ 10 kHz, T_J = +25°C)	V_n	–	40	200	μV_{rms}
Long Term Stability (T_J = +125°C) (Note 5)	S	–	20	50	mV/khr
OSCILLATOR SECTION (Note 6, unless otherwise noted.)					
Initial Accuracy (T_J = +25°C)		–	±2.0	±6.0	%
Frequency Stability with Voltage (+8.0 V ≤ V_{CC} ≤ +35 V)	$\frac{\Delta f_{osc}}{D\ V_{CC}}$	–	±1.0	±2.0	%
Frequency Stability with Temperature	$\frac{\Delta f_{osc}}{D\ \ T}$	–	±0.3	–	%
Minimum Frequency (R_T = 150 kΩ, C_T = 0.2 µF)	f_{min}	–	50	–	Hz
Maximum Frequency (R_T = 2.0 kΩ, C_T = 1.0 nF)	f_{max}	400	–	–	kHz
Current Mirror (I_{RT} = 2.0 mA)		1.7	2.0	2.2	mA
Clock Amplitude		3.0	3.5	–	V
Clock Width (T_J = +25°C)		0.3	0.5	1.0	µs
Sync Threshold		1.2	2.0	2.8	V
Sync Input Current (Sync Voltage = +3.5 V)		–	1.0	2.5	mA
ERROR AMPLIFIER SECTION (V_{CM} = +5.1 V)					
Input Offset Voltage	V_{IO}	–	2.0	10	mV
Input Bias Current	I_{IB}	–	1.0	10	µA
Input Offset Current	I_{IO}	–	–	1.0	µA
DC Open Loop Gain (R_L ≥ 10 MΩ)	A_{VOL}	60	75	–	dB
Low Level Output Voltage	V_{OL}	–	0.2	0.5	V
High Level Output Voltage	V_{OH}	3.8	5.6	–	V
Common Mode Rejection Ratio (+1.5 V ≤ V_{CM} ≤ +5.2 V)	CMRR	60	75	–	dB
Power Supply Rejection Ratio (+8.0 V ≤ V_{CC} ≤ +35 V)	PSRR	50	60	–	dB
PWM COMPARATOR SECTION					
Minimum Duty Cycle	DC_{min}	–	–	0	%
Maximum Duty Cycle	DC_{max}	45	49	–	%
Input Threshold, Zero Duty Cycle (Note 6)	V_{th}	0.6	0.9	–	V
Input Threshold, Maximum Duty Cycle (Note 6)	V_{th}	–	3.3	3.6	V
Input Bias Current	I_{IB}	–	0.05	1.0	µA

NOTES: 4. T_{low} = 0° for SG3525A, 3527A T_{high} = +70°C for SG3525A, 3527A
5. Since long term stability cannot be measured on each device before shipment, this specification is an engineering estimate of average stability from lot to lot.
6. Tested at f_{osc} = 40 kHz (R_T = 3.6 kΩ, C_T = 0.01 µF, R_D = 0Ω).

ELECTRICAL CHARACTERISTICS (Continued)

Characteristics	Symbol	Min	Typ	Max	Unit
SOFT–START SECTION					
Soft–Start Current ($V_{shutdown}$ = 0 V)		25	50	80	µA
Soft–Start Voltage ($V_{shutdown}$ = 2.0 V)		–	0.4	0.6	V
Shutdown Input Current ($V_{shutdown}$ = 2.5 V)		–	0.4	1.0	mA
OUTPUT DRIVERS (Each Output, V_{CC} = +20 V)					
Output Low Level (I_{sink} = 20 mA) (I_{sink} = 100 mA)	V_{OL}	 – –	 0.2 1.0	 0.4 2.0	V
Output High Level (I_{source} = 20 mA) (I_{source} = 100 mA)	V_{OH}	 18 17	 19 18	 – –	V
Under Voltage Lockout (V8 and V9 = High)	V_{UL}	6.0	7.0	8.0	V
Collector Leakage, V_C = +35 V (Note 7)	$I_{C(leak)}$	–	–	200	µA
Rise Time (C_L = 1.0 nF, T_J = 25°C)	t_r	–	100	600	ns
Fall Time (C_L = 1.0 nF, T_J = 25°C)	t_f	–	50	300	ns
Shutdown Delay (V_{DS} = +3.0 V, C_S = 0, T_J = +25°C)	t_{ds}	–	0.2	0.5	µs
Supply Current (V_{CC} = +35 V)	I_{CC}	–	14	20	mA

NOTE: 7. Applies to SG3525A only, due to polarity of output pulses.

Lab Test Fixture

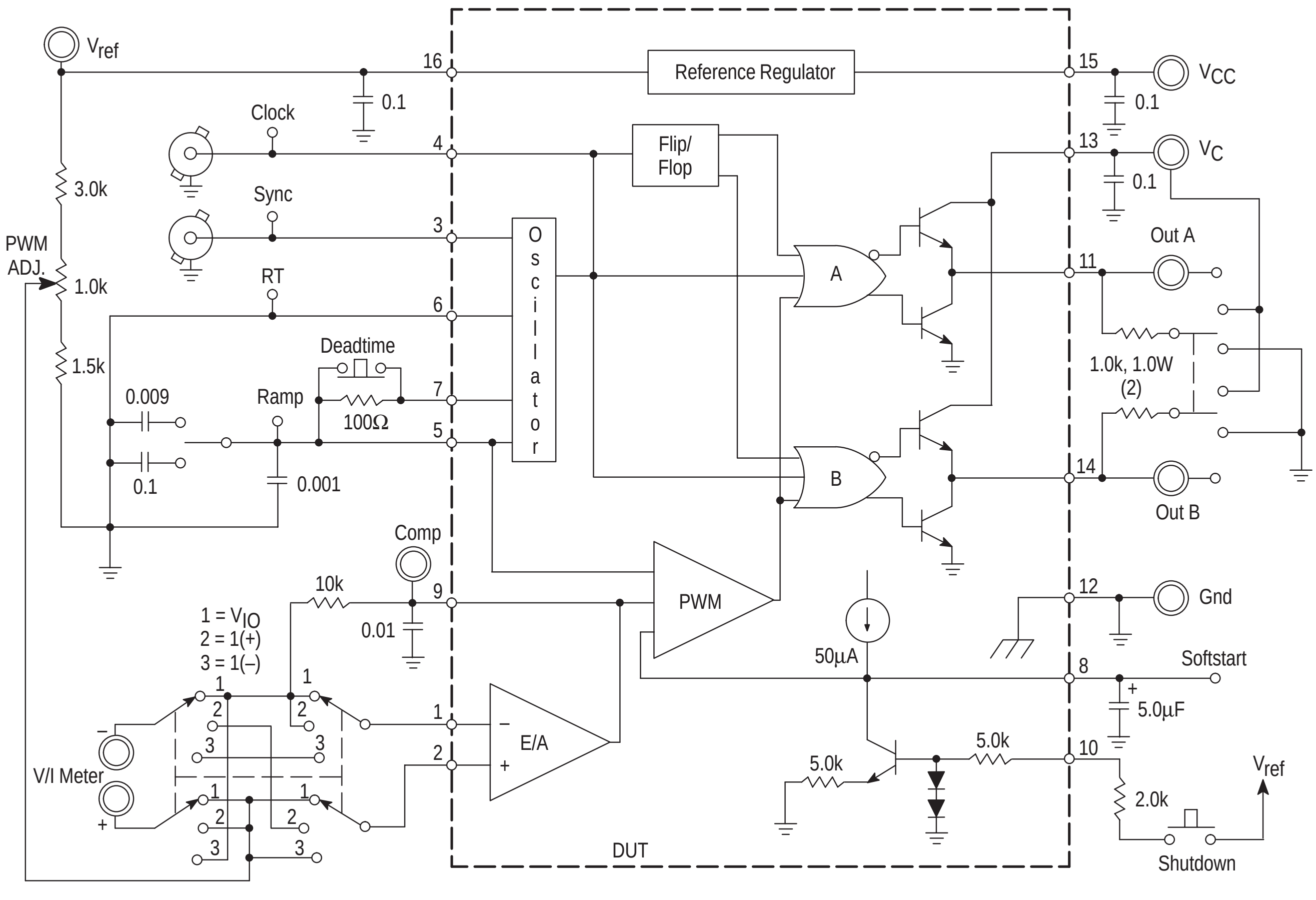


Figure 1. Oscillator Charge Time versus R_T

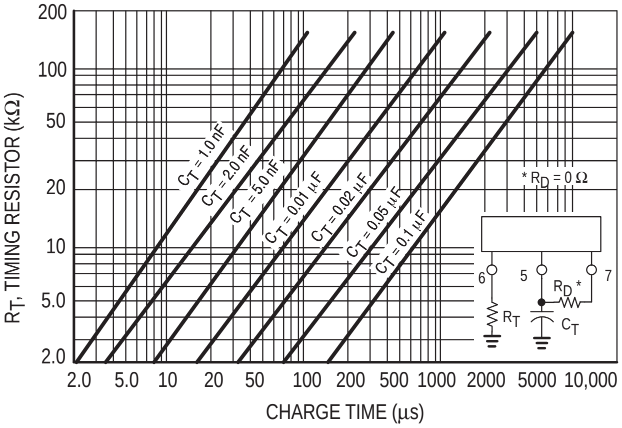


Figure 2. Oscillator Discharge Time versus R_D

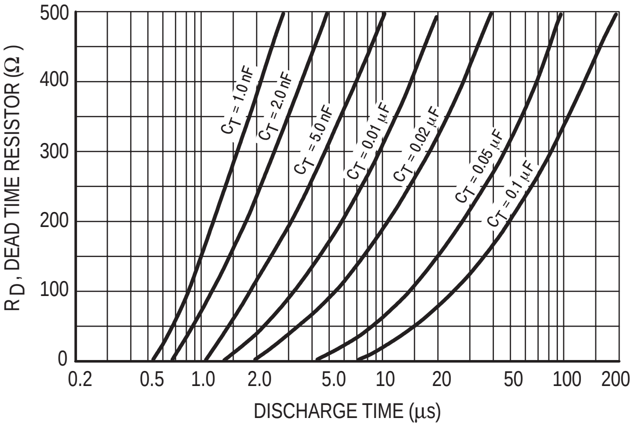


Figure 3. Error Amplifier Open Loop Frequency Response

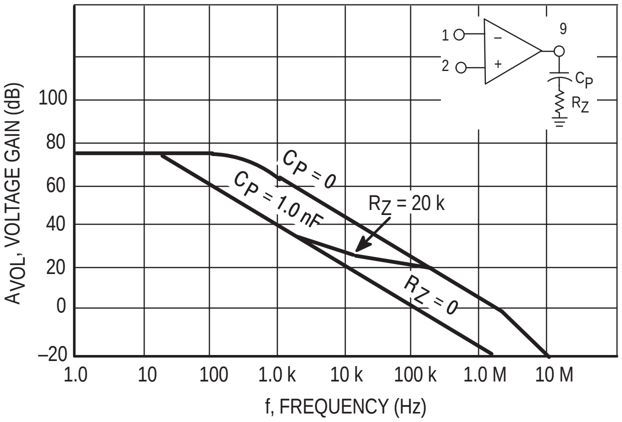


Figure 4. Output Saturation Characteristics (SG3525A)

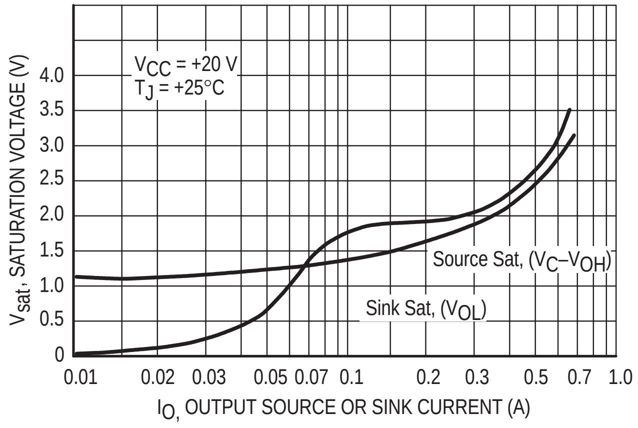


Figure 5. Oscillator Schematic (SG3525A)

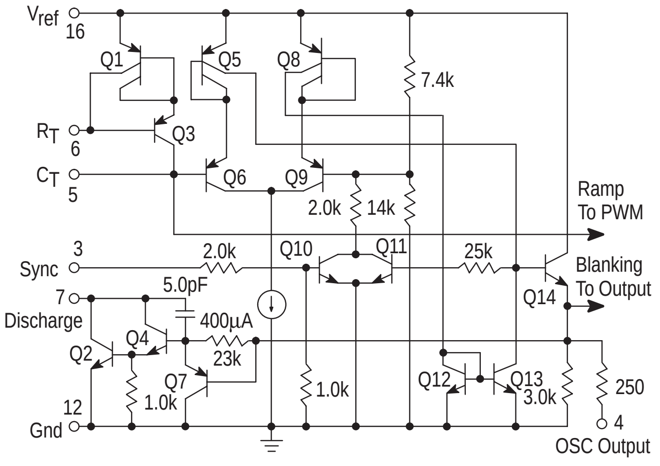


Figure 6. Error Amplifier Schematic (SG3525A)

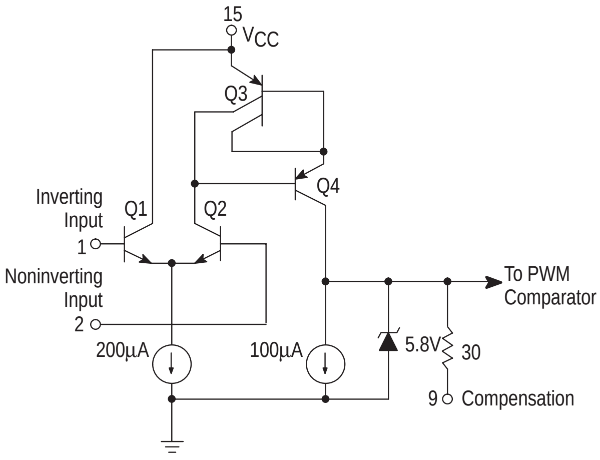


Figure 7. SG3525A Output Circuit
(1/2 Circuit Shown)

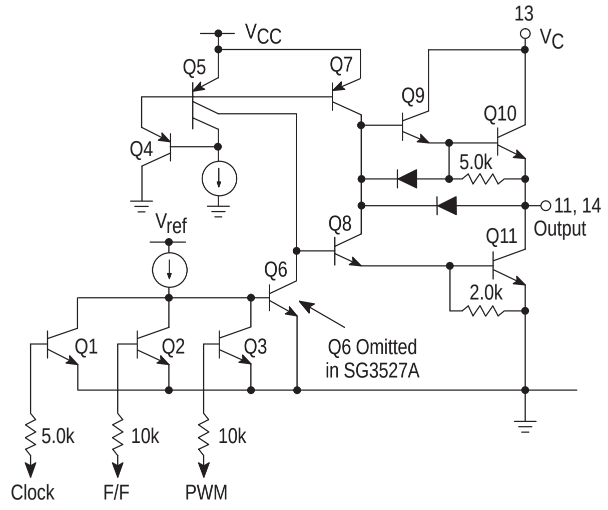
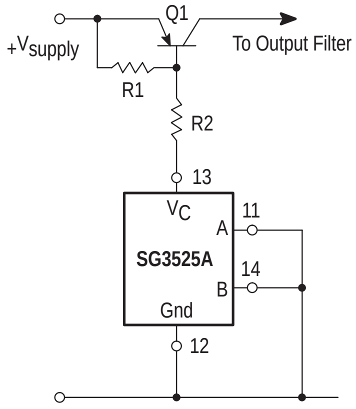
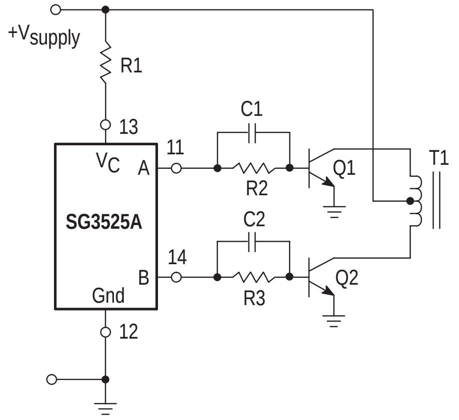


Figure 8. Single–Ended Supply



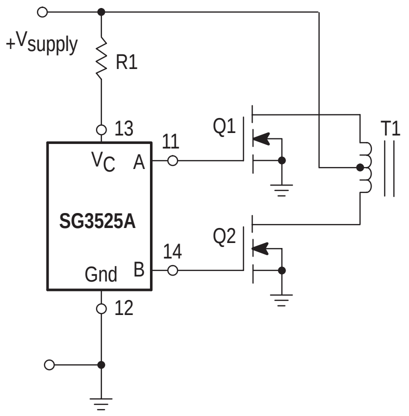
For single–ended supplies, the driver outputs are grounded. The V_C terminal is switched to ground by the totem–pole source transistors on alternate oscillator cycles.

Figure 9. Push–Pull Configuration



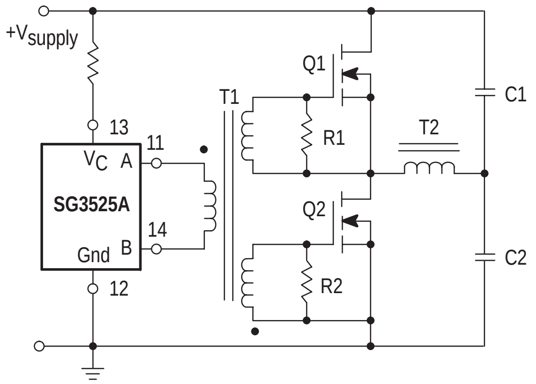
In conventional push–pull bipolar designs, forward base drive is controlled by R1–R3. Rapid turn–off times for the power devices are achieved with speed–up capacitors C1 and C2.

Figure 10. Driving Power FETS



The low source impedance of the output drivers provides rapid charging of power FET input capacitance while minimizing external components.

Figure 11. Driving Transformers in a Half–Bridge Configuration



Low power transformers can be driven directly by the SG3525A. Automatic reset occurs during deadtime, when both ends of the primary winding are switched to ground.

MOTOROLA

SG3526

Pulse Width Modulation Control Circuit

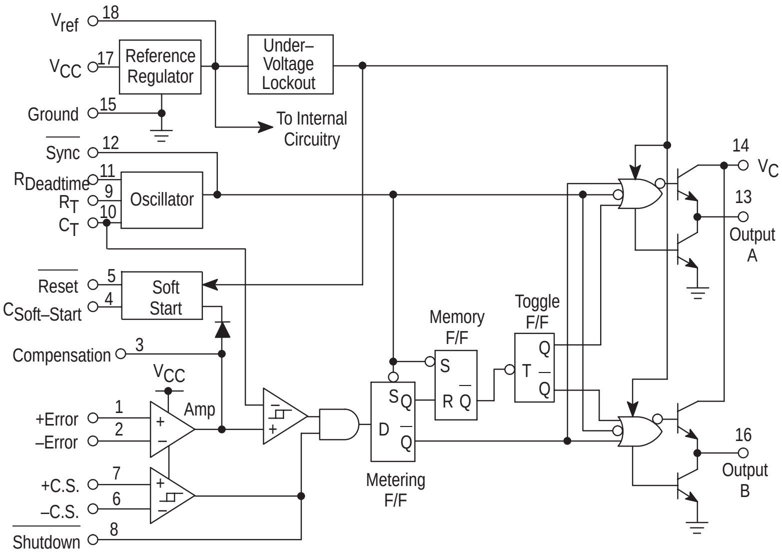
The SG3526 is a high performance pulse width modulator integrated circuit intended for fixed frequency switching regulators and other power control applications.

Functions included in this IC are a temperature compensated voltage reference, sawtooth oscillator, error amplifier, pulse width modulator, pulse metering and steering logic, and two high current totem pole outputs ideally suited for driving the capacitance of power FETs at high speeds.

Additional protective features include soft start and undervoltage lockout, digital current limiting, double pulse inhibit, adjustable dead time and a data latch for single pulse metering. All digital control ports are TTL and B–series CMOS compatible. Active low logic design allows easy wired–OR connections for maximum flexibility. The versatility of this device enables implementation in single–ended or push–pull switching regulators that are transformerless or transformer coupled. The SG3526 is specified over a junction temperature range of 0° to +125°C.

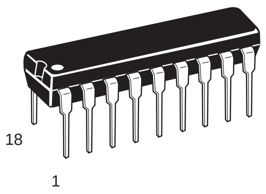
- 8.0 V to 35 V Operation
- 5.0 V ±1% Trimmed Reference
- 1.0 Hz to 400 kHz Oscillator Range
- Dual Source/Sink Current Outputs: ±100 mA
- Digital Current Limiting
- Programmable Dead Time
- Undervoltage Lockout
- Single Pulse Metering
- Programmable Soft–Start
- Wide Current Limit Common Mode Range
- Guaranteed 6 Unit Synchronization

Representative Block Diagram



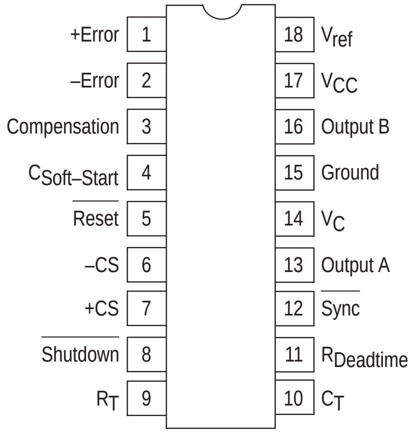
PULSE WIDTH MODULATION CONTROL CIRCUIT

SEMICONDUCTOR TECHNICAL DATA



N SUFFIX
PLASTIC PACKAGE
CASE 707

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
SG3526N	T_J = 0° to +125°C	Plastic DIP

MAXIMUM RATINGS (Note 1)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	+40	Vdc
Collector Supply Voltage	V_C	+40	Vdc
Logic Inputs		–0.3 to +5.5	V
Analog Inputs		–0.3 to V_{CC}	V
Output Current, Source or Sink	I_O	±200	mA
Reference Load Current (V_{CC} = 40 V, Note 2)	I_{ref}	50	mA
Logic Sink Current		15	mA
Power Dissipation T_A = +25°C (Note 3) T_C = +25°C (Note 4)	P_D	 1000 3000	mW
Thermal Resistance Junction–to–Air	$R_{\theta JA}$	100	°C/W
Thermal Resistance Junction–to–Case	$R_{\theta JC}$	42	°C/W
Operating Junction Temperature	T_J	+150	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Lead Temperature (Soldering, 10 Seconds)	T_{Solder}	±300	°C

NOTES: 1. Values beyond which damage may occur.
2. Maximum junction temperature must be observed.
3. Derate at 10 mW/°C for ambient temperatures above +50°C.
4. Derate at 24 mW/°C for case temperatures above +25°C.

RECOMMENDED OPERATING CONDITIONS

Characteristics	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	8.0	35	Vdc
Collector Supply Voltage	V_C	4.5	35	Vdc
Output Sink/Source Current (Each Output)	I_O	0	±100	mA
Reference Load Current	I_{ref}	0	20	mA
Oscillator Frequency Range	f_{osc}	0.001	400	kHz
Oscillator Timing Resistor	R_T	2.0	150	kΩ
Oscillator Timing Capacitor	C_T	0.001	20	µF
Available Deadtime Range (40 kHz)	–	3.0	50	%
Operating Junction Temperature Range	T_J	0	+125	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 Vdc, $T_J = T_{low}$ to T_{high} [Note 5], unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
REFERENCE SECTION (Note 6)					
Reference Output Voltage (T_J = +25°C)	V_{ref}	4.90	5.00	5.10	V
Line Regulation (+8.0 V ≤ V_{CC} ≤ +35 V)	Reg_{line}	–	10	30	mV
Load Regulation (0 mA ≤ I_L ≤ 20 mA)	Reg_{load}	–	10	50	mV
Temperature Stability	$\Delta V_{ref}/\Delta T$	–	10	–	mV
Total Reference Output Voltage Variation (+8.0 V ≤ V_{CC} ≤ +35 V, 0 mA ≤ I_L ≤ 20 mA)	ΔV_{ref}	4.85	5.00	5.15	V
Short Circuit Current (V_{ref} = 0 V) (Note 2)	I_{SC}	25	80	125	mA
UNDERVOLTAGE LOCKOUT					
$\overline{\text{Reset}}$ Output Voltage (V_{ref} = +3.8 V)		–	0.2	0.4	V
$\overline{\text{Reset}}$ Output Voltage (V_{ref} = +4.8 V)		2.4	4.8	–	V
OSCILLATOR SECTION (Note 7)					
Initial Accuracy (T_J = +25°C)		–	±3.0	±8.0	%
Frequency Stability over Power Supply Range (+8.0 V ≤ V_{CC} ≤ +35 V)	$\frac{\Delta f_{osc}}{\Delta\ V_{CC}}$	–	0.5	1.0	%
Frequency Stability over Temperature ($\Delta T_J = T_{low}$ to T_{high})	$\frac{\Delta f_{osc}}{\Delta\ T_J}$	–	2.0	–	%
Minimum Frequency (R_T = 150 kΩ, C_T = 20 μF)	f_{min}	–	0.5	–	Hz
Maximum Frequency (R_T = 2.0 kΩ, C_T = 0.001 μF)	f_{max}	400	–	–	kHz
Sawtooth Peak Voltage (V_{CC} = +35 V)	$V_{osc}(P)$	–	3.0	3.5	V
Sawtooth Valley Voltage (V_{CC} = +8.0 V)	$V_{osc}(V)$	0.45	0.8	–	V
ERROR AMPLIFIER SECTION (Note 8)					
Input Offset Voltage (R_S ≤ 2.0 kΩ)	V_{IO}	–	2.0	10	mV
Input Bias Current	I_{IB}	–	–350	–2000	nA
Input Offset Current	I_{IO}	–	35	200	nA
DC Open Loop Gain (R_L ≥ 10 MΩ)	A_{VOL}	60	72	–	dB
High Output Voltage ($V_{Pin\ 1}–V_{Pin\ 2}$ ≥ +150 mV, I_{source} = 100 μA)	V_{OH}	3.6	4.2	–	V
Low Output Voltage ($V_{Pin\ 2}–V_{Pin\ 1}$ ≥ +150 mV, I_{sink} = 100 μA)	V_{OL}	–	0.2	0.4	V
Common Mode Rejection Ratio (R_S ≤ 2.0 kΩ)	CMRR	70	94	–	dB
Power Supply Rejection Ratio (+12 V ≤ V_{CC} ≤ +18 V)	PSRR	66	80	–	dB

NOTES: 2. Maximum junction temperature must be observed.
5. T_{low} = 0°C T_{high} = +125°C
6. I_L = 0 mA unless otherwise noted.
7. f_{osc} = 40 kHz (R_T = 4.12 kΩ ± 1%, C_T = 0.01 μF ± 1%, R_D = 0 Ω)
8. 0 V ≤ V_{CM} ≤ +5.2 V.

ELECTRICAL CHARACTERISTICS (continued)

Characteristics	Symbol	Min	Typ	Max	Unit
PWM COMPARATOR SECTION (Note 7)					
Minimum Duty Cycle ($V_{Compensation}$ = +0.4 V)	DC_{min}	–	–	0	%
Maximum Duty Cycle ($V_{Compensation}$ = +3.6 V)	DC_{max}	45	49	–	%
DIGITAL PORTS ($\overline{\text{SYNC}}$, $\overline{\text{SHUTDOWN}}$, $\overline{\text{RESET}}$)					
Output Voltage (High Logic Level) (I_{source} = 40 µA) (Low Logic Level) (I_{sink} = 3.6 mA)	 V_{OH} V_{OL}	 2.4 –	 4.0 0.2	 – 0.4	V
Input Current — High Logic Level (High Logic Level) (V_{IH} = +2.4 V) (Low Logic Level) (V_{IL} = +0.4 V)	 I_{IH} I_{IL}	 – –	 –125 –225	 –200 –360	µA
CURRENT LIMIT COMPARATOR SECTION (Note 9)					
Sense Voltage ($R_S \leq 50\ \Omega$)	V_{sense}	80	100	120	mA
Input Bias Current	I_{IB}	—	–3.0	–10	µA
SOFT–START SECTION					
Error Clamp Voltage ($\overline{\text{Reset}}$ = +0.4 V)		–	0.1	0.4	V
$C_{Soft–Start}$ Charging Current ($\overline{\text{Reset}}$ = +2.4 V)	I_{CS}	50	100	150	µA
OUTPUT DRIVERS (Each Output, V_C = +15 Vdc, unless otherwise noted.)					
Output High Level I_{source} = 20 mA I_{source} = 100 mA	V_{OH}	 12.5 12	 13.5 13	 – –	V
Output Low Level I_{sink} = 20 mA I_{sink} = 100 mA	V_{OL}	 – –	 0.2 1.2	 0.3 2.0	V
Collector Leakage, V_C = +40 V	$I_{C(leak)}$	–	50	150	µA
Rise Time (C_L = 1000 pF)	t_r	–	0.3	0.6	µs
Fall Time (C_L = 1000 pF)	t_f	–	0.1	0.2	µs
Supply Current (Shutdown = +0.4 V, V_{CC} = +35 V, R_T = 4.12 kΩ)	I_{CC}	–	18	30	mA

NOTES: 7. f_{osc} = 40 kHz (R_T = 4.12 kΩ ± 1%, C_T = 0.01 µF ± 1%, R_D = 0 Ω)
8. 0 V ≤ V_{CM} ≤ +5.2 V
9. 0 V ≤ V_{CM} ≤ +12 V

Figure 1. Reference Stability over Temperature

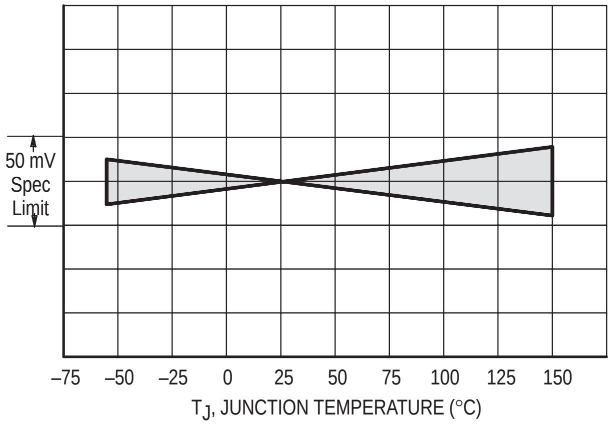


Figure 2. Reference Voltage as a Function Supply Voltage

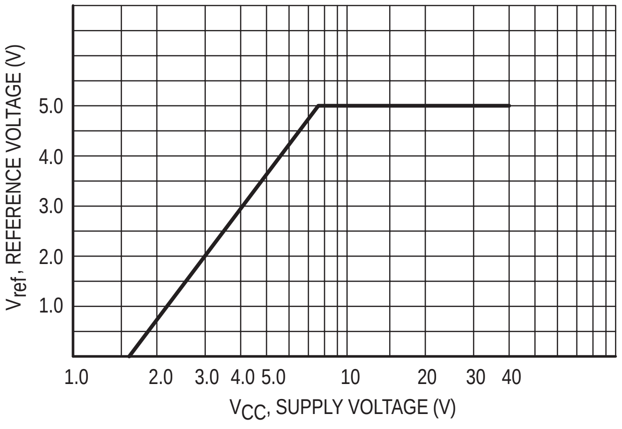


Figure 3. Error Amplifier Open Loop Frequency Response

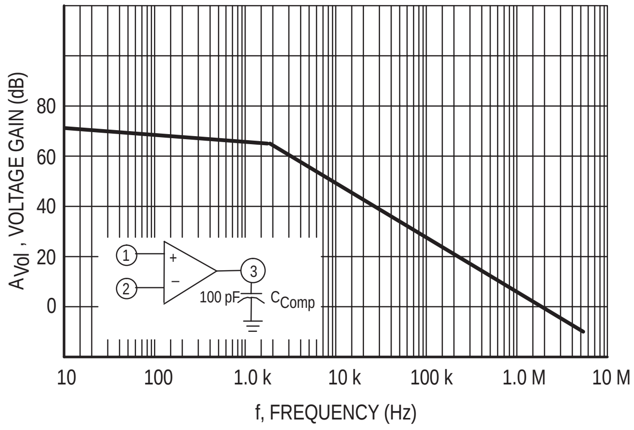


Figure 4. Current Limit Comparator Threshold

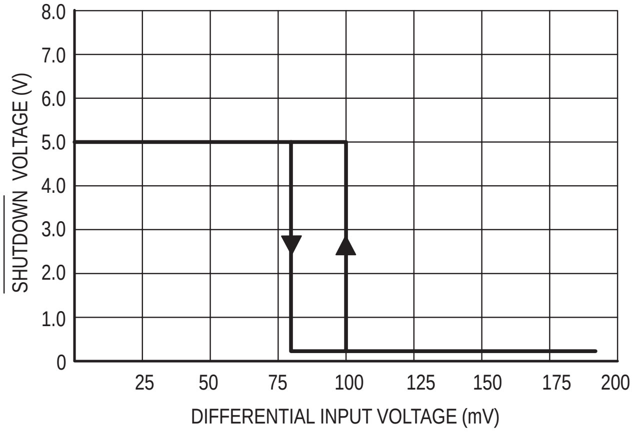


Figure 5. Undervoltage Lockout Characteristic

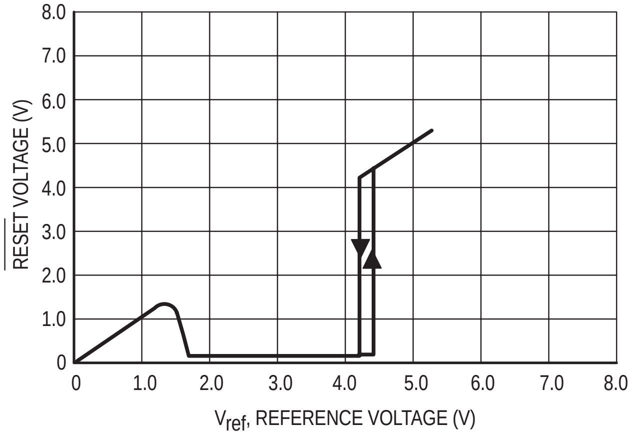


Figure 6. Output Driver Saturation Voltage as a Function of Sink Current

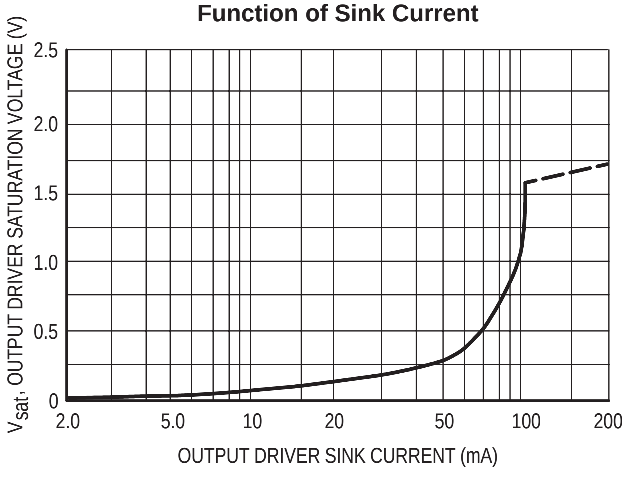


Figure 7. V_C Saturation Voltage as a Function of Sink Current

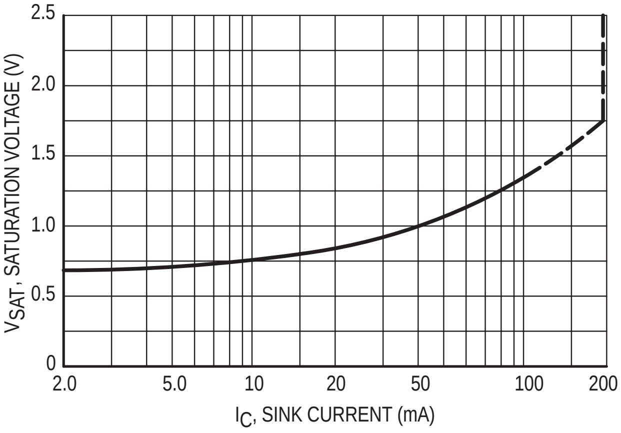


Figure 8. Oscillator Period

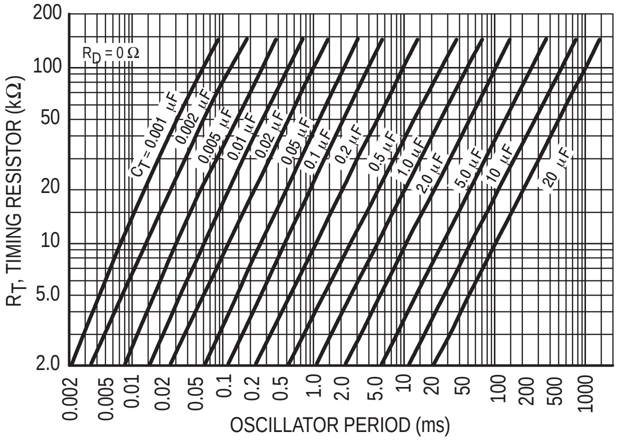


Figure 9. Error Amplifier

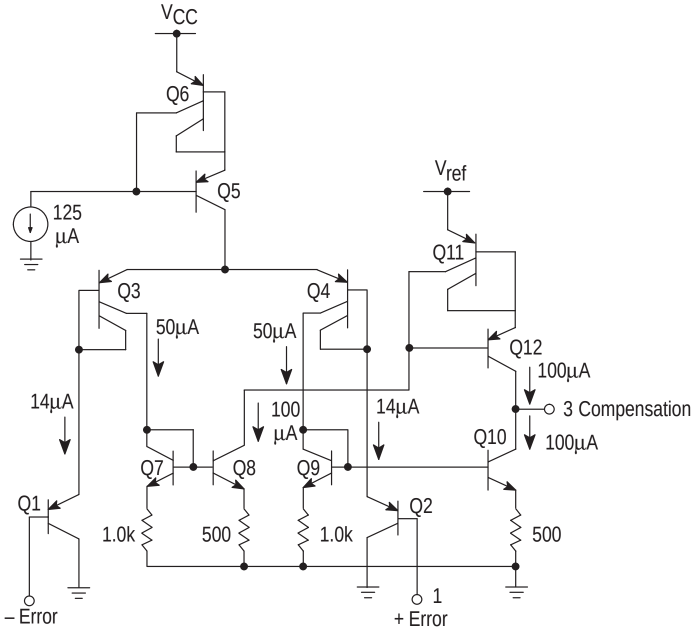


Figure 10. Undervoltage Lockout

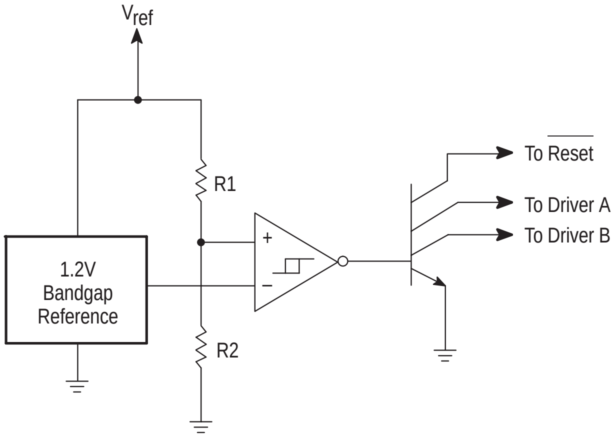
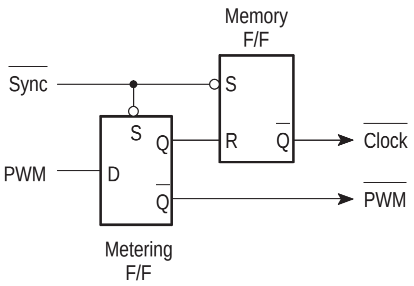


Figure 11. Pulse Processing Logic

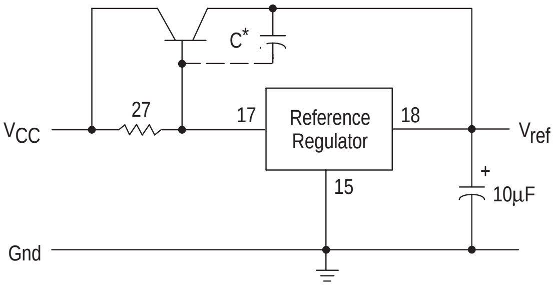


The metering Flip–Flop is an asynchronous data latch which suppresses high frequency oscillations by allowing only one PWM pulse per oscillator cycle.

The memory Flip–Flop prevents double pulsing in a push–pull configuration by remembering which output produced the last pulse.

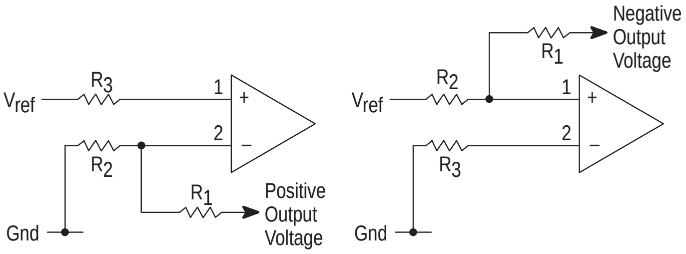
APPLICATIONS INFORMATION

Figure 12. Extending Reference Output Current Capability



* May be required with some types of transistors

Figure 13. Error Amplifier Connections



$$V_{out} = V_{ref}\left(\frac{R_1 + R_2}{R2}\right) \qquad V_{out} = V_{ref}\left(\frac{R_1}{R_2}\right)$$

$$R_3 = \left(\frac{R_1 R_2}{R_1 + R_2}\right)$$

Figure 14. Oscillator Connections

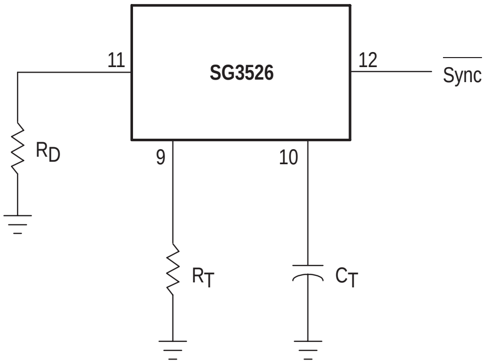
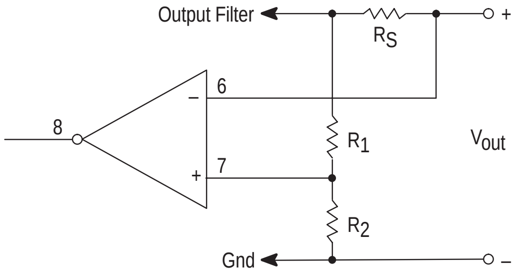


Figure 15. Foldback Current Limiting



$$I_{(max)} = \frac{\left(0.1\ V + \frac{V_{out}\,R_1}{R1 + R2}\right)}{R_S} \qquad I_{SC} = \left(\frac{0.1\ V}{R_S}\right)$$

Figure 16. Soft–Start Circuitry

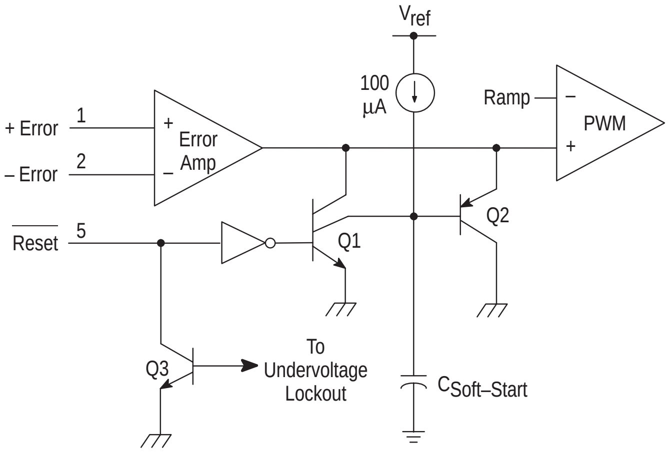
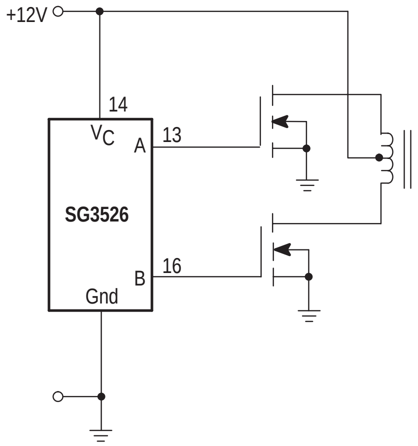


Figure 17. Driving VMOS Power FETs



The totem pole output drivers of the SG3526 are ideally suited for driving the input capacitance of power FETs at high speeds.

Figure 18. Half–Bridge Configuration

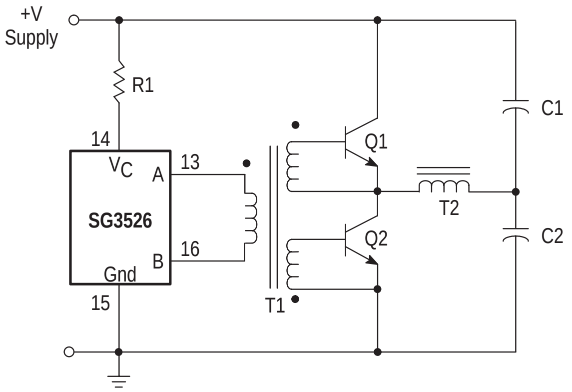
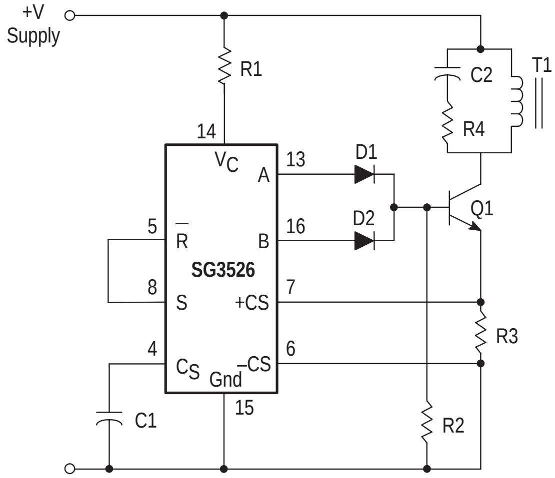


Figure 19. Flyback Converter with Current Limiting



In the above circuit, current limiting is accomplished by using the current limit comparator output to reset the soft–start capacitor.

Figure 20. Single–Ended Configuration

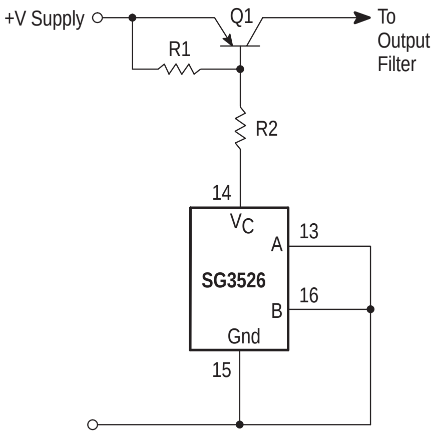
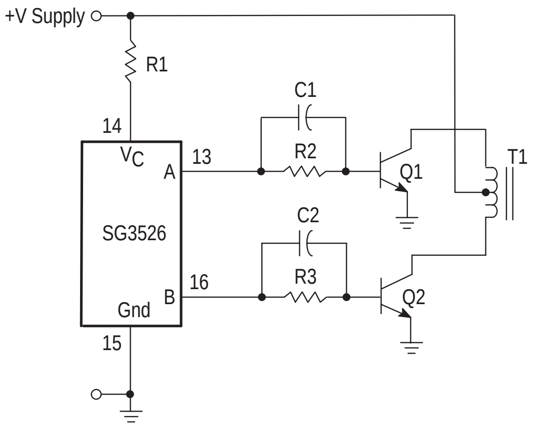


Figure 21. Push–Pull Configuration



TCA5600
TCF5600

Universal Microprocessor Power Supply/Controllers

The TCA5600, TCF5600 are versatile power supply control circuits for microprocessor based systems and are mainly intended for automotive applications and battery powered instruments. To cover a wide range of applications, the devices offer high circuit flexibility with a minimum of external components.

Functions included in this IC are a temperature compensated voltage reference, on–chip dc/dc converter, programmable and remote controlled voltage regulator, fixed 5.0 V supply voltage regulator with external PNP power device, undervoltage detection circuit, power–on RESET delay and watchdog feature for safe and hazard free microprocessor operations.

- 6.0 V to 30 V Operation Range
- 2.5 V Reference Voltage Accessible for Other Tasks
- Fixed 5.0 V ± 4% Microprocessor Supply Regulator Including Current Limitation, Overvoltage Protection and Undervoltage Monitor.
- Programmable 6.0 V to 30 V Voltage Regulator Exhibiting High Peak Current (150mA), Current Limiting and Thermal Protection.
- Two Remote Inputs to Select the Regulator’s Operation Mode:
  - OFF = 5.0 V, 5.0 V Standby
  - Programmable Output Voltage
- Self–Contained dc/dc Converter Fully Controlled by the Programmable Regulator to Guarantee Safe Operation Under All Working Conditions
- Programmable Power–On RESET Delay
- Watchdog Select Input
- Negative Edge Triggered Watchdog Input
- Low Current Consumption in the V_{CC1} Standby Mode
- All Digital Control Ports are TTL and MOS–Compatible

Applications Include:

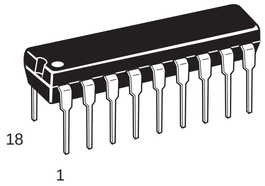
- Microprocessor Systems with E^2PROMs
- High Voltage Crystal and Plasma Displays
- Decentralized Power Supplies in Computer Telecom Systems

RECOMMENDED OPERATING CONDITIONS

Characteristics	Symbol	Min	Max	Unit
Power Supply Voltage	V_{CC1} V_{CC2}	5.0 5.5	30 30	V
Collector Current	I_C	—	800	mA
Output Voltage	V_{out2}	6.0	30	V
Reference Source Current	I_{ref}	0	2.0	mA

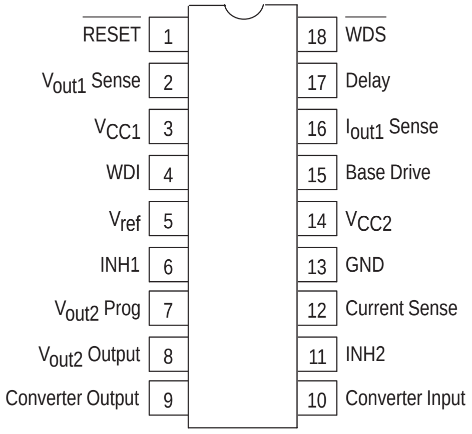
UNIVERSAL MICROPROCESSOR POWER SUPPLY/CONTROLLERS

SEMICONDUCTOR TECHNICAL DATA



PLASTIC PACKAGE
CASE 707

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

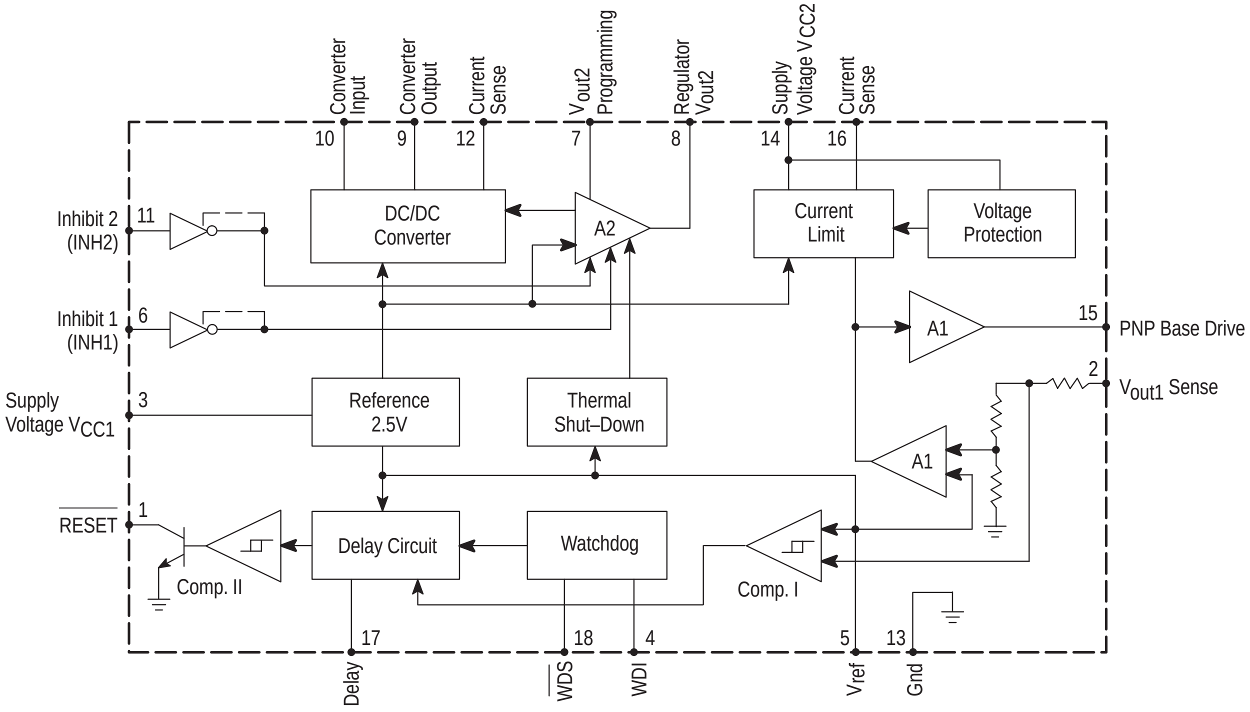
Device	Operating Temperature Range	Package
TCA5600	T_J = 0° to +125°C	Plastic DIP
TCF5600	T_J = – 40° to +150°C	Plastic DIP

MAXIMUM RATINGS (T_A = +25°C [Note 1], unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage (Pin 3,14)	V_{CC1}, V_{CC2}	35	Vdc
Base Drive Current (Pin 15)	I_B	20	mA
Collector Current (Pin 10)	I_C	1.0	A
Forward Rectifier Current (Pin 10 to Pin 9)	I_F	1.0	A
Logic Inputs INH1, INH2, $\overline{\text{WDS}}$ (Pin 6, 11, 18)	V_{INP}	–0.3 V to V_{CC1}	Vdc
Logic Input Current WDI (Pin 4)	I_{WDI}	±0.5	mA
Output Sink Current $\overline{\text{RESET}}$ (Pin 1)	I_{RES}	10	mA
Analog Inputs (Pin 2) (Pin 7)		–0.3 to 10 –0.3 to 5.0	V
Reference Source Current (Pin 5)	I_{ref}	5.0	mA
Power Dissipation (Note 2) T_A = +75°C TCA5600 T_A = +85°C TCF5600	P_D	 500 650	mW
Thermal Resistance, Junction–to–Air	$R_{\theta JA}$	100	°C/W
Operating Ambient Temperature Range TCA5600 TCF5600	T_A	 0 to +75 –40 to +85	°C
Operating Junction Temperature Range TCA5600 TCF5600	T_J	 +125 +150	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

NOTES: 1. Values beyond which damage may occur.
2. Derate at 10 mW/°C for junction temperature above +75°C (TCA5600).
Derate at 10 mW/°C for junction temperature above +85°C (TCF5600).

Representative Block Diagram



ELECTRICAL CHARACTERISTICS (V_{CC1} = V_{CC2} = 12 V; T_J = 25°C; I_{ref} = 0; I_{out1} = 0 [Note 3]; R_{SC} = 0.5 Ω; INH = High INH2 = High; WDS = High; I_{out2} = 0 [Note 4]; unless otherwise noted.)

Characteristics	Figure	Symbol	Min	Typ	Max	Unit
REFERENCE SECTION						
Nominal Reference Voltage	1	$V_{ref\ nom}$	2.42	2.5	2.58	V
Reference Voltage I_{ref} = 0.5 mA, $T_{low} \le T_J \le T_{high}$ (Note 5), 6.0 V ≤ V_{CC1} ≤ 18 V		V_{ref}	2.4	—	2.6	V
Line Regulation (6.0 V ≤ V_{CC2} ≤ 18 V)		Reg_{line}	—	2.0	15	mV
Average Temperature Coefficient $T_{low} \le T_J \le T_{high}$ (Note 5)	2	$\frac{\Delta V_{ref}}{\Delta T_J}$	—	—	±0.5	mV/°C
Ripple Rejection Ratio f = 1.0 kHz, V_{sin} = 1.0 V_{pp}	3	RR	60	70	—	dB
Output Impedance 0 ≤ I_{ref} ≤ 2.0 mA		Z_O	—	1.0	—	Ω
Standby Current Consumption V_{CC2} = Open	4	I_{CC1}	—	3.0	—	mA
5.0 V MICROPROCESSOR VOLTAGE REGULATOR SECTION						
Nominal Output Voltage		$V_{out1(nom)}$	4.8	5.0	5.2	V
Output Voltage 5.0 mA ≤ I_{out1} ≤ 300 mA, $T_{low} \le T_J \le T_{high}$ (Note 5) 6.0 V ≤ V_{CC2} ≤ 18 V	 5 6	V_{out1}	4.75	—	5.25	V
Line Regulation (6.0 V ≤ V_{CC2} ≤ 18 V)		Reg_{line}	—	10	50	mV
Load Regulation (5.0 mA ≤ I_{out1} ≤ 300 mA)		Reg_{load}	—	20	100	mV
Base Current Drive (V_{CC2} = 6.0 V, V_{15} = 4.0 V)		I_B	10	15	—	mA
Ripple Rejection Ratio f = 1.0 kHz, V_{sin} = 1.0 V_{pp}	3	RR	50	65	—	dB
Undervoltage Detection Level (R_{SC} = 5.0 Ω)	7	V_{low}	4.5	0.93 × V_{out1}	—	V
Current Limitation Threshold (R_{SC} = 5.0 Ω)		V_{RSC}	210	250	290	mV
Average Temperature Coefficient $T_{low} \le T_J \le T_{high}$ (Note 5)		$\frac{\Delta V_{out1}}{\Delta T_J}$	—	—	±1.0	mV/°C
DC/DC CONVERTER SECTION						
Collector Current Detection Level High RC = 10 k Low	9	$V_{12}(H)$ $V_{12}(L)$	350 —	400 50	450 —	mV
Collector Saturation Voltage I_C = 600 mA (Note 6)	10	$V_{CE(sat)}$	—	—	1.6	V
Rectifier Forward Voltage Drop I_F = 600 mA (Note 6)	11	V_F	—	—	1.4	V

NOTES: 3. The external PNP power transistor satisfies the following minimum specifications:
$h_{FE} \ge 60$ at I_C = 500 mA and V_{CE} = 5.0 V;
$V_{CE(sat)} \le$ 300 mV at I_B = 10 mA and I_C = 300 mA
4. Regulator V_{out2} programmed for nominal 24 V output by means of R4, R5 (see Figure 1).
5. T_{low} = 0°C for TCA5600 T_{low} = –40°C for TCF5600
T_{high} = +125°C for TCA5600 T_{high} = +150°C for TCF5600
6. Pulse tested $t_p \le 300$ µs.

ELECTRICAL CHARACTERISTICS (V_{CC1} = V_{CC2} = 12 V; T_J = 25°C; I_{ref} = 0; I_{out1} = 0 [Note 3]; R_{SC} = 0.5 Ω; INH = High INH2 = High; $\overline{\text{WDS}}$ = High; I_{out2} = 0 [Note 4]; unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
PROGRAMMABLE VOLTAGE REGULATOR SECTION (Note 6)					
Nominal Output Voltage	$V_{out2(nom)}$	23	24	25	V
Output Voltage (Figure 8) 1.0 mA ≤ I_{out2} ≤ 100 mA, T_{low} ≤ T_J ≤ T_{high} (Notes 5, 7)	V_{out2}	22.8	—	25.2	V
Load Regulation 1.0 mA ≤ I_{out2} ≤ 100 mA (Note 7)	Reg_{load}	—	40	200	mV
DC Output Current	I_{out2}	100	—	—	mA
Peak Output Current (Internally Limited)	$I_{out2\ p}$	150	200	—	mA
Ripple Rejection Ratio f = 20 kHz, V = 0.4 V_{pp}	RR	45	55	—	dB
Output Voltage (Fixed 5.0 V) 1.0 mA ≤ I_{out2} ≤ 20 mA, T_{low} ≤ T_J ≤ T_{high} INH1 = HIGH (Note 5)	$V_{out2(5.0\ V)}$	4.75	—	5.25	V
Off State Output Impedance (INH2 = Low)	R_{out1}	—	10	—	kΩ
Average Temperature Coefficient T_{low} ≤ T_J ≤ T_{high} (Note 5)	$\frac{\Delta V_{out2}}{\Delta T_J V_{out2}}$	—	—	±0.25	mV/°C V
WATCHDOG AND $\overline{\text{RESET}}$ CIRCUIT SECTION					
Threshold Voltage High (Static) Low	$V_{C5(H)}$ $V_{C5(L)}$	— —	2.5 1.0	— —	V
Current Source T_{low} ≤ T_J ≤ T_{high} (Note 5) Power–Up $\overline{\text{RESET}}$ Watchdog Time Out Watchdog $\overline{\text{RESET}}$	I_{C5}	 –1.8 — —	 –2.5 5×I_{C5} –50×I_{C5}	 –3.2 — —	µA
Watchdog Input Voltage Swing	V_{WDI}	—	—	±5.5	V
Watchdog Input Impedance	r_i	12	15	—	kΩ
Watchdog Reset Pulse Width (C8 = 1.0 nF) (Note 9)	t_p	—	—	10	µs
DIGITAL PORTS: $\overline{\text{WDS}}$, INH 1, INH 2, $\overline{\text{RESET}}$ (Note 8)					
Input Voltage Range	V_{INP}	—	—	–0.3 to V_{CC1}	V
Input High Current 2.0 V ≤ V_{IH} ≤ 5.5 V 5.5 V ≤ V_{IH} ≤ V_{CC1}	I_{IH}	 — —	 — —	 100 150	µA
Input Low Current –0.3 V ≤ V_{IL} ≤ 0.8 V for INH1, INH2, –0.3 V ≤ V_{IL} ≤ 0.4 V for $\overline{\text{WDS}}$	I_{IL}	 —	 —	 –100	µA
Leakage Current Immunity (INH2, High “Z” State) (Figure 12)	I_Z	±20	—	—	µA
Output Low Voltage $\overline{\text{RESET}}$ (I_{OL} = 6.0 mA)	V_{OL}	—	—	0.4	V
Output High Voltage $\overline{\text{RESET}}$ (V_{OH} = 5.5 V)	V_{OH}	—	—	20	µA

NOTES: 3. The external PNP power transistor satisfies the following minimum specifications:
h_{FE} ≥ 60 at I_C = 500 mA and V_{CE} = 5.0 V;
$V_{CE(sat)}$ ≤ 300 mV at I_B = 10 mA and I_C = 300 mA
4. Regulator V_{out2} programmed for nominal 24 V output by means of R4, R5 (see Figure 1).
5. T_{low} = 0°C for TCA5600 T_{low} = –40°C for TCF5600
T_{high} = +125°C for TCA5600 T_{high} = +150°C for TCF5600
6. V_9 = 28 V, INH1 = LOW for this Electrical Characteristic section unless otherwise noted.
7. Pulse tested t_p ≤ 300 µs.
8. Temperature range T_{low} ≤ T_J ≤ T_{high} applies to this Electrical Characteristics section.
9. For test purposes, a negative pulse is applied to Pin 4 (–2.5 V ≥ V_4 ≥ –5.5 V).

Figure 1. Reference Voltage versus Supply Voltage

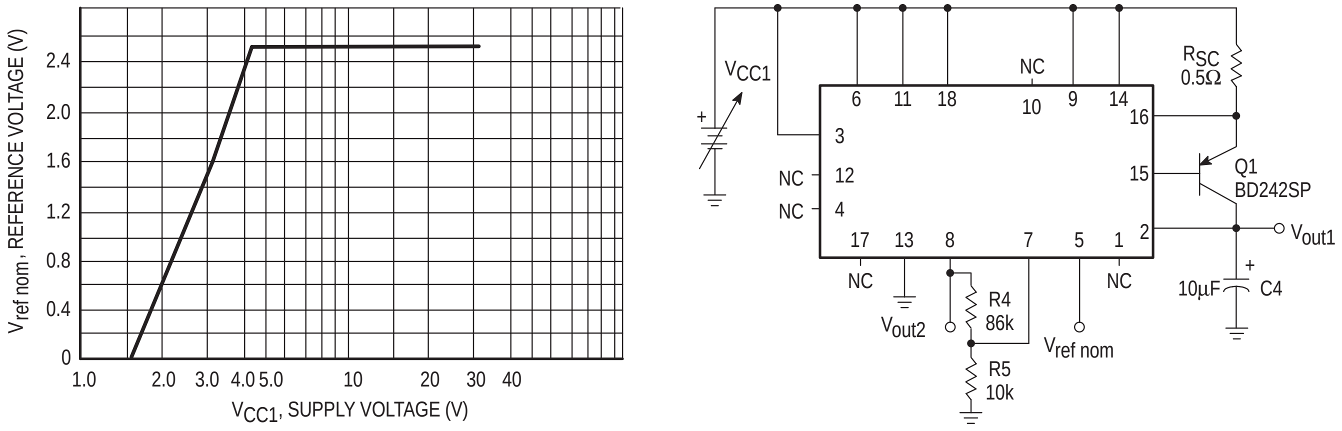


Figure 2. Reference Stability versus Temperature

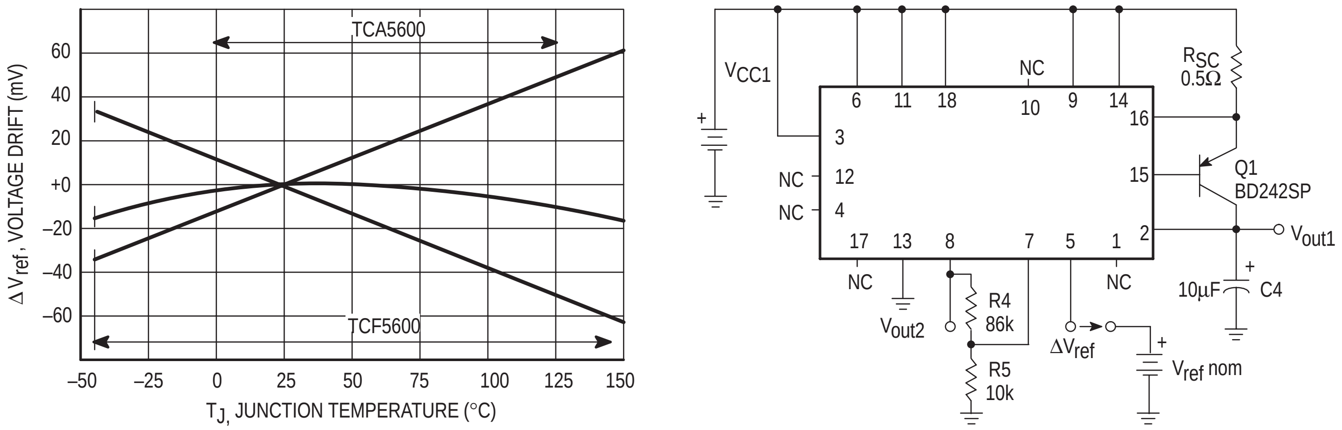


Figure 3. Ripple Rejection versus Frequency

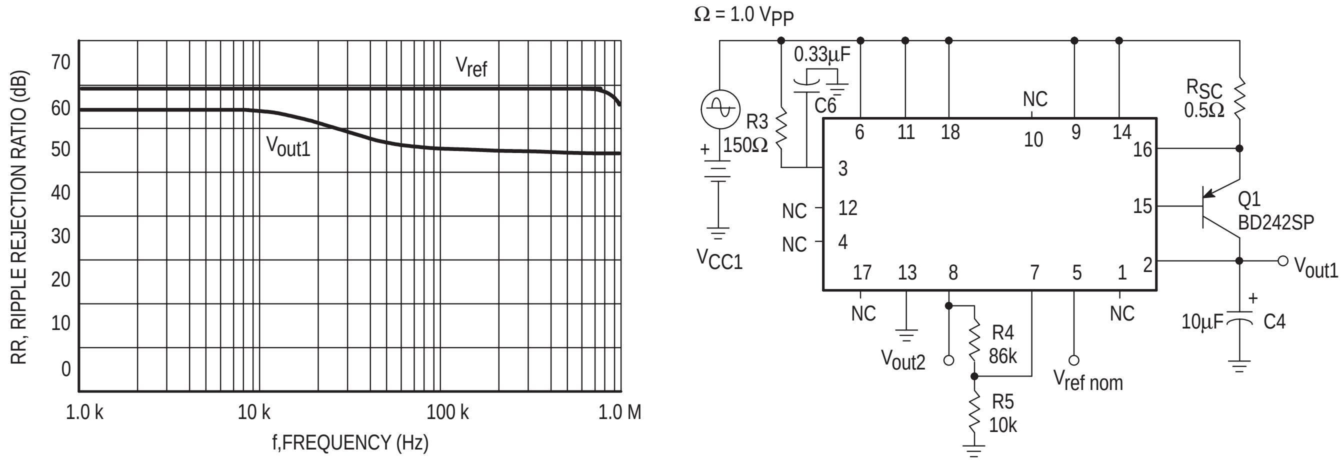


Figure 4. Standby Current versus Supply Voltage

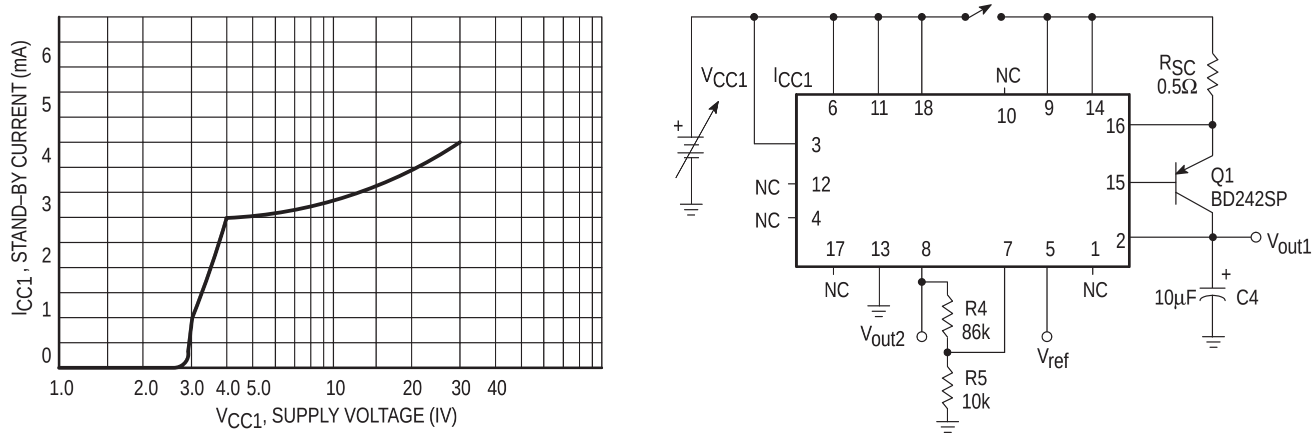


Figure 5. Power–Up Behavior of the 5.0 V Regulator

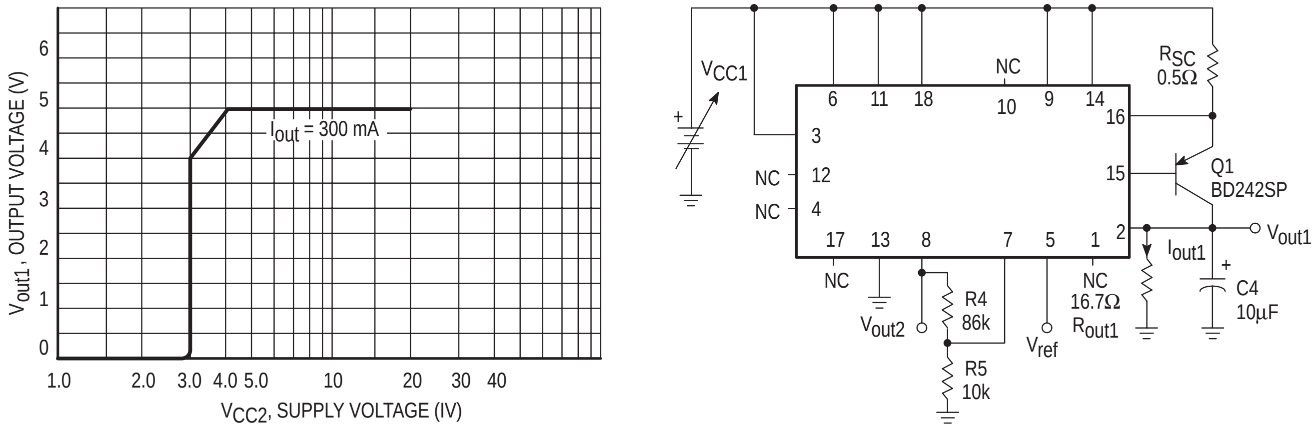


Figure 6. Foldback Characteristics of the 5.0 V Regulator

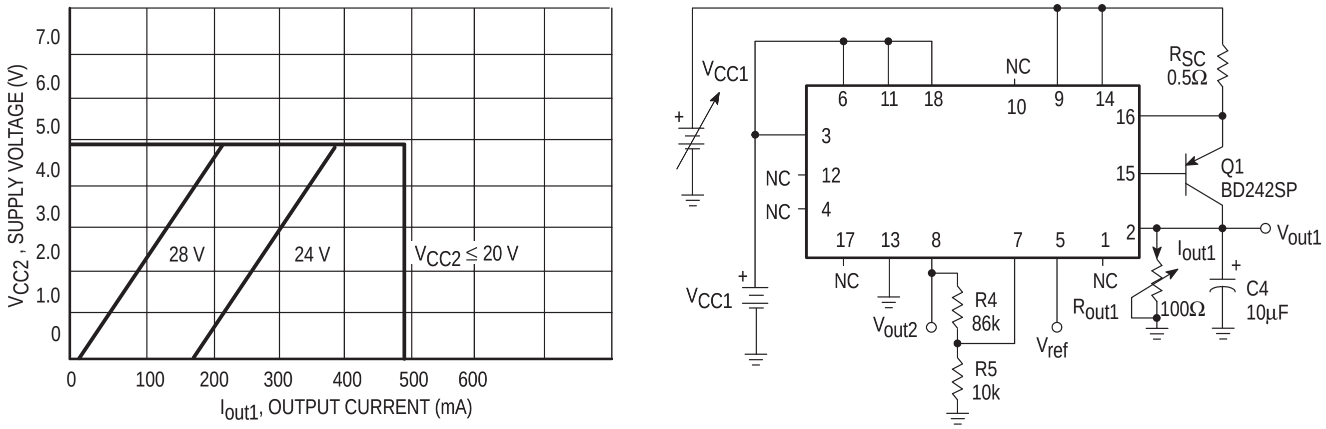


Figure 7. Undervoltage Lockout Characteristics

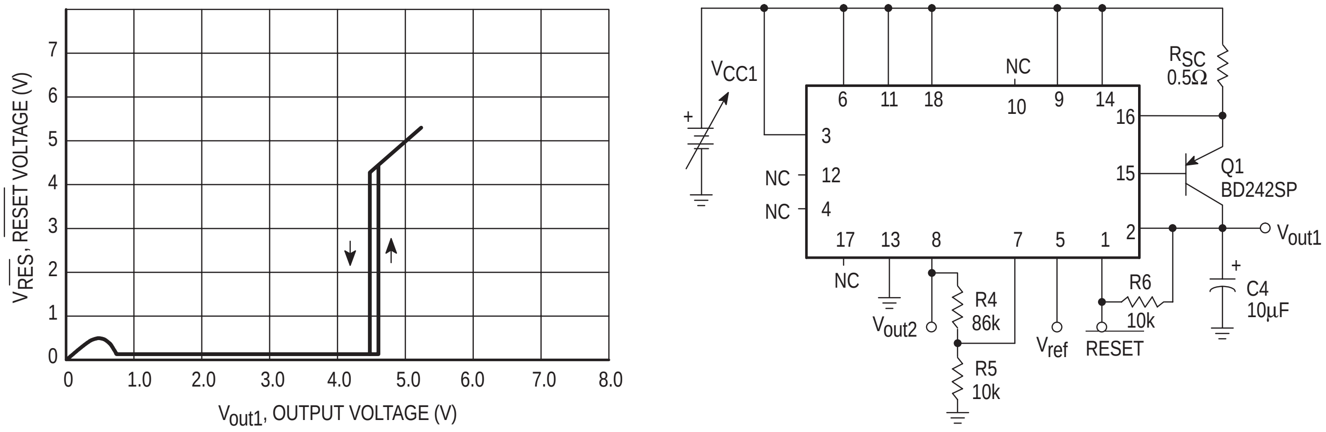


Figure 8. Output Current Capability of the Programming Regulator

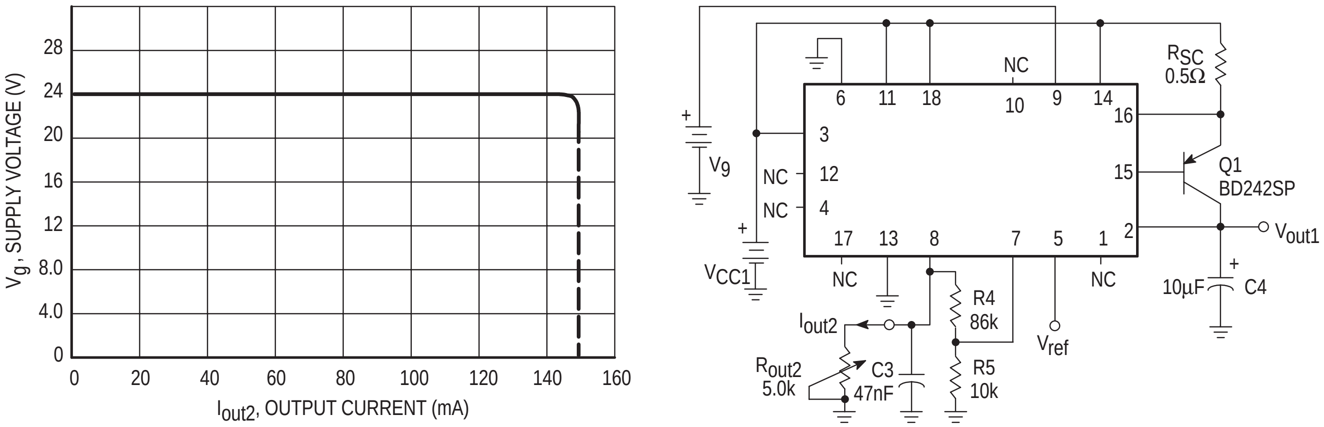


Figure 9. Collector Current Detection Level

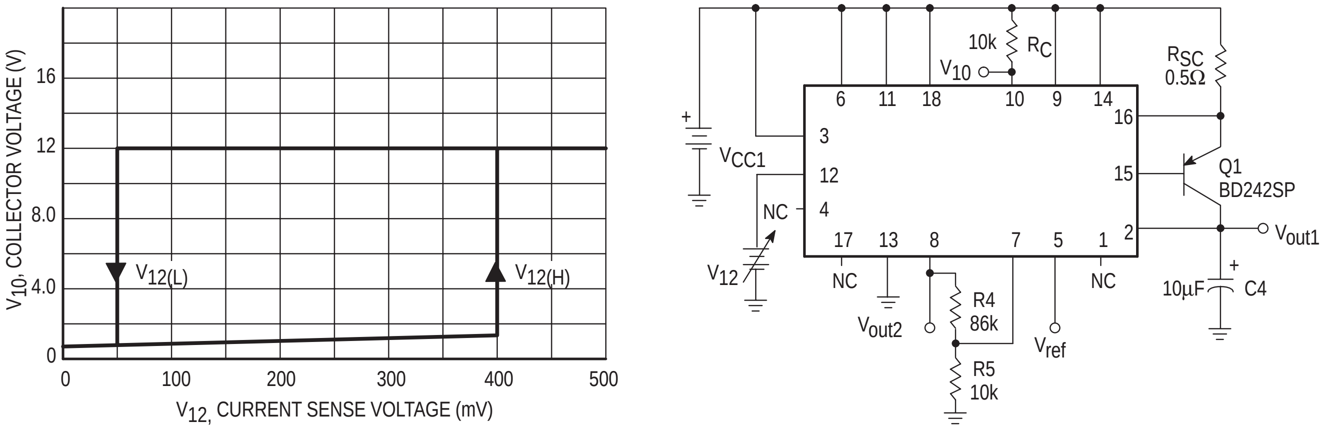


Figure 10. Power Switch Characteristics

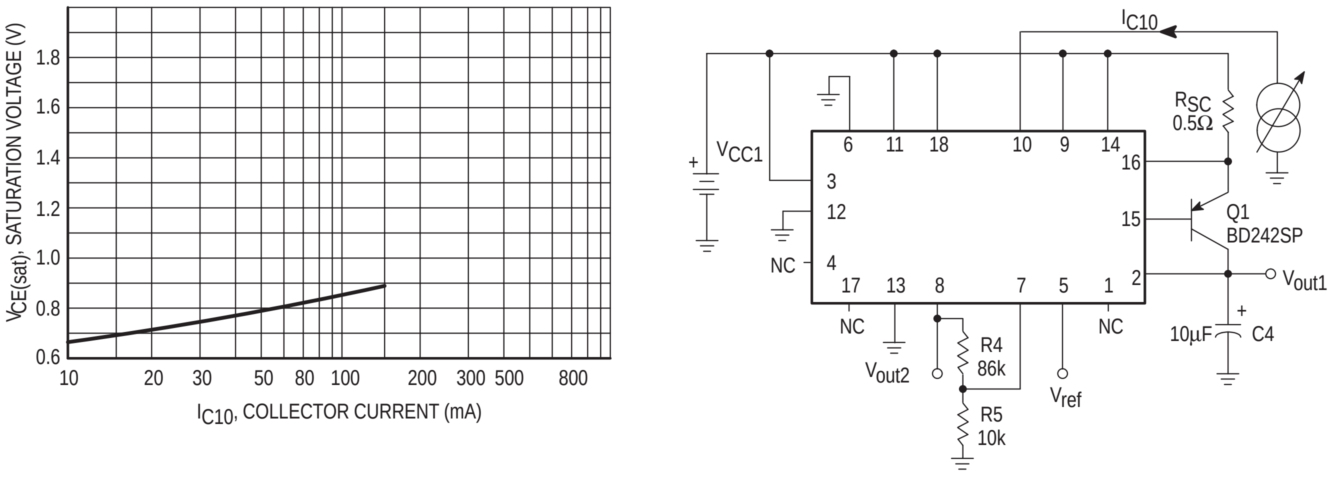


Figure 11. Rectifier Characteristics

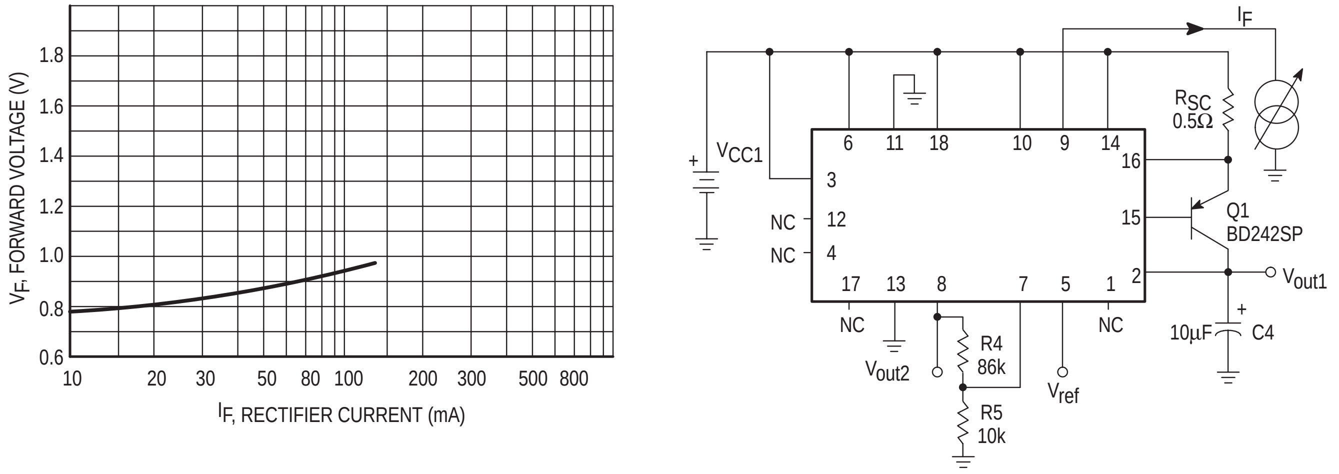
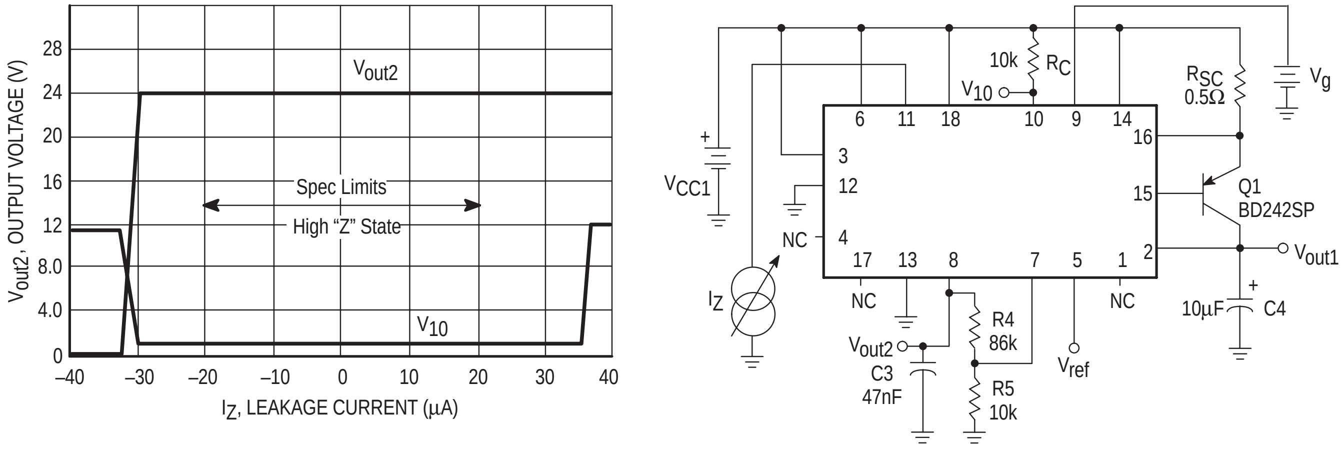


Figure 12. INH 2 Leakage Current Immunity



APPLICATIONS INFORMATION

(See Figure 18)

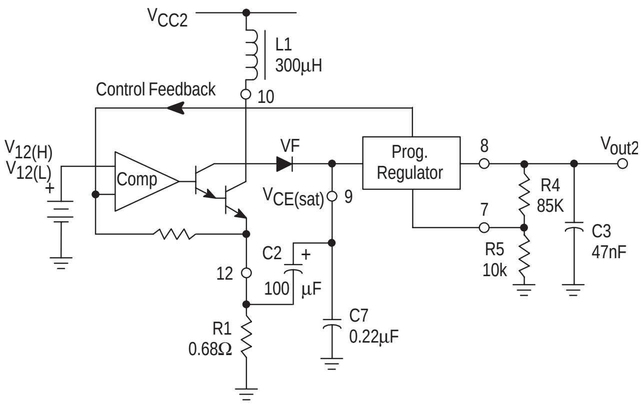
Voltage Reference (V_{ref})

The voltage reference V_{ref} is based upon a highly stable bandgap voltage reference and is accessible on Pin 5 for additional tasks. This circuit part has its own supply connection on Pin 3 and is, therefore, able to operate in standby mode. The RC network R3, C6 improves the ripple rejection on both regulators.

DC/DC Converter

The dc/dc converter performs according to the flyback principle and does not need a time base circuit. The maximum coil current is well defined by means of the current sensing resistor R1 under all working conditions (startup phase, circuit overload, wide supply voltage range and extreme load current change). Figure 13 shows the Simplified Converter Schematic.

Figure 13. Simplified Converter Schematic



A simplified method on “how to calculate the coil inductance” is given below. The operation point at minimum supply voltage (V_{CC2}) and max. output current (I_{out2}) for a fixed output voltage (V_{out2}) determines the coil data. Figure 14 shows the typical voltage and current waveforms on the coil L1 (coil losses neglected).

Equations (1) and (2) yield the respective coil voltage V_L – and V_L + (see Figure 14):

$$V_L+ = V_{out2} + \Delta V_{(Pin\ 9\ -\ Pin\ 8)} + V_F - V_{CC2} \quad (1)$$
$$V_L- = V_{CC2} - V_{CE(sat)} - V_{12(H)} \quad (2)$$

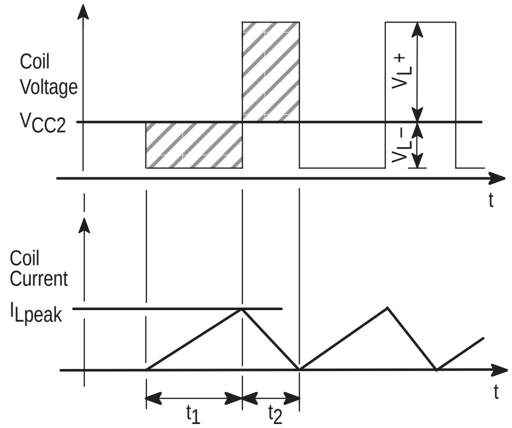
[$\Delta V_{(Pin\ 9\ –\ Pin\ 8)}$: input/output voltage drop of the regulator, 2.5 V typical]

[V_F, $V_{CE(sat)}$, $V_{12(H)}$: see Electrical Characteristics Table]

The time ratio α for the charging time to dumping time is defined by Equation (3):

$$\alpha = \frac{t_1}{t_2} = \frac{V_L+}{V_L-} \quad (3)$$

Figure 14. Voltage and Current Waveform on the Coil (not to scale)



The coil charging time t_1 is found using Equation (4):

$$t_1 = \frac{1}{(1 + \frac{1}{\alpha}) \cdot f} \quad (4)$$

[f : minimum oscillation frequency which should be chosen above the audio frequency band (e.g. 20 kHz)]

Knowing the dc output current I_{out2} of the programmable regulator, the peak coil current $I_{L(peak)}$ can now be calculated:

$$I_{L(peak)} = 2 \cdot (I_{out2}) (1 + \alpha) \quad (5)$$

The coil inductance L1 of the nonsaturated coil is given by Equation (6):

$$L1 = \frac{t_1}{I_{L(peak)}} (V_L-) \quad (6)$$

The formula (6a) yields the current sensing resistor R1 for a defined peak coil current $I_{L(peak)}$:

$$R1 = \frac{V_{12(H)}}{I_{L(peak)}} \quad (6a)$$

In order to limit the by–pass current through capacitor C7 during the energy dumping phase the value C2>>C7 should be implemented.

For all other operation conditions, the feedback signal from the programmable voltage regulator controls the activity of the converter.

Programmable Voltage Regulator

This series voltage regulator is programmable by the voltage divider R4, R5 for a nominal output voltage of $6.0\ V \leq V_{out2} \leq 30\ V$.

$$R4 = \frac{(V_{out2} - V_{ref\ nom}) \bullet R5}{V_{ref\ nom}} \qquad (7)$$

$$[R5 = 10\ k,\ V_{ref\ nom} = 2.5\ V]$$

Current limitation and thermal shutdown capability are standard features of this regulator. The voltage drop $\Delta V_{(Pin\ 9 - Pin\ 8)}$ across the series pass transistor generates the feedback signal to control the dc/dc converter (see Figure 13).

Control Inputs INH1, INH2

The dc/dc converter and/or the regulator V_{out2} are remote controllable through the TTL, MOS compatible inhibit inputs INH1 and INH2 where the latter is a three–level detector (Logic "0", High Impedance "Z", Logic "1"). Both inputs are set–up to provide the following truth table:

Figure 15. INH1, INH2 TruthTable

Mode	INH1	INH2	V_{out2}	DC/DC
1	0	0	OFF	INT
2	0	High "Z"	V_{out2}	ON
3	0	1	V_{out2}	INT
4	1	0	OFF	INT
5	1	High "Z"	5.0 V	ON
6	1	1	5.0 V	INT

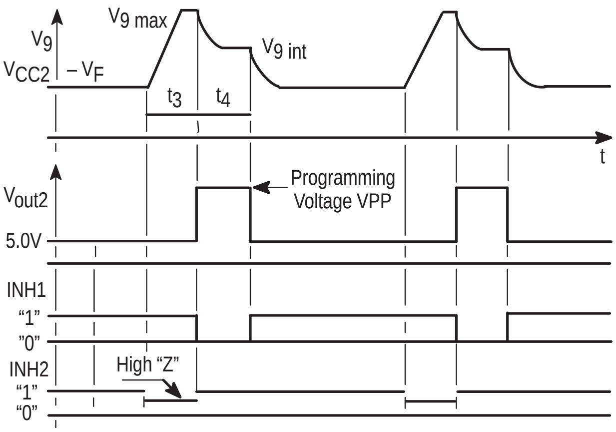
INT: Intermittent operation of the converter means that the converter operates only if $V_{CC2} < V_{out2}$.

ON: The converter loads the storage capacitor C2 to its full charge (V_9 = 33 V), allowing fast response time of the regulator V_{out2} when addressed by the control software.

OFF: High impedance (internal resistor 10 k to ground)

Figure 16 represents a typical timing diagram for an E^2PROM programming sequence in a microprocessor based system. The High "Z" state enables the dc/dc converter to ramp during t_3 to the voltage V_9 at Pin 9 to a high level before the write cycle takes place in the memory.

Figure 16. Typical E^2PROM Programming Sequence
(not to scale)



Microprocessor Supply Regulator

Together with an external PNP power transistor (Q1), a 5.0 V supply exhibiting low voltage drop is obtained to power microprocessor systems and auxiliary circuits. Using a power Darlington with adequate heat sink in the output stage boosts the output current I_{out1} above 1.0 A.

The current limitation circuit measures the emitter current of Q1 by means of the sensing resistor, R_{SC}:

$$R_{SC} = \frac{V_{RSC}}{I_E} \qquad (8)$$

[I_E: emitter current of Q1]

[V_{RSC}: threshold voltage (see Electrical Characteristics Table)]

The voltage protection circuit performs a foldback characteristic above a nominal operating voltage, $V_{CC2} \geq 18\ V$.

Delay and Watchdog Circuit

The undervoltage monitor supervises the power supply V_{out1} and releases the delay circuit RESET as soon as the regulator output reaches the microprocessor operating a range [e.g., $V_{low} \geq 0.93 \bullet V_{out1(nom)}$]. The RESET output has an open–collector and may be connected in a "wired–OR" configuration.

The watchdog circuit consists of a retriggerable monostable with a negative edge sensitive control input WDI. The watchdog feature may be disabled by means of the watchdog select input WDS driven to a "1". Figure 17 displays the Typical RESET Timing Diagram.

The commuted current source I_{C5} on Pin 17, threshold voltage $V_{C5(L)}$, $V_{C5(H)}$ and an external capacitor C5 define the RESET delay and the watchdog timing. The relationship of the timing signals are indicated by the Equations (9) to (11).

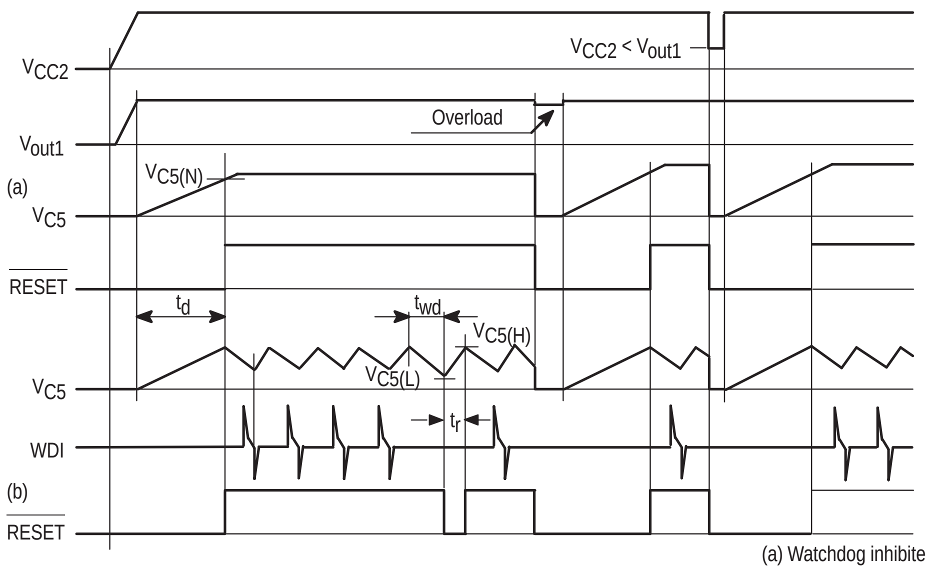
$$\overline{\text{RESET}}\ \text{delay:}\quad t_d = \frac{C5 \bullet V_{C5(H)}}{|I_{C5}|} \qquad (9)$$

$$\text{Watchdog timeout:}\quad t_{wd} = \frac{C5 \bullet (V_{C5(H)} - V_{C5(L)})}{5 \bullet I_{C5}} \qquad (10)$$

$$\text{Watchdog}\ \overline{\text{RESET}}\text{:}\quad t_r = \frac{C5 \bullet (V_{C5(H)} - V_{C5(L)})}{50 \bullet |I_{C5}|} \qquad (11)$$

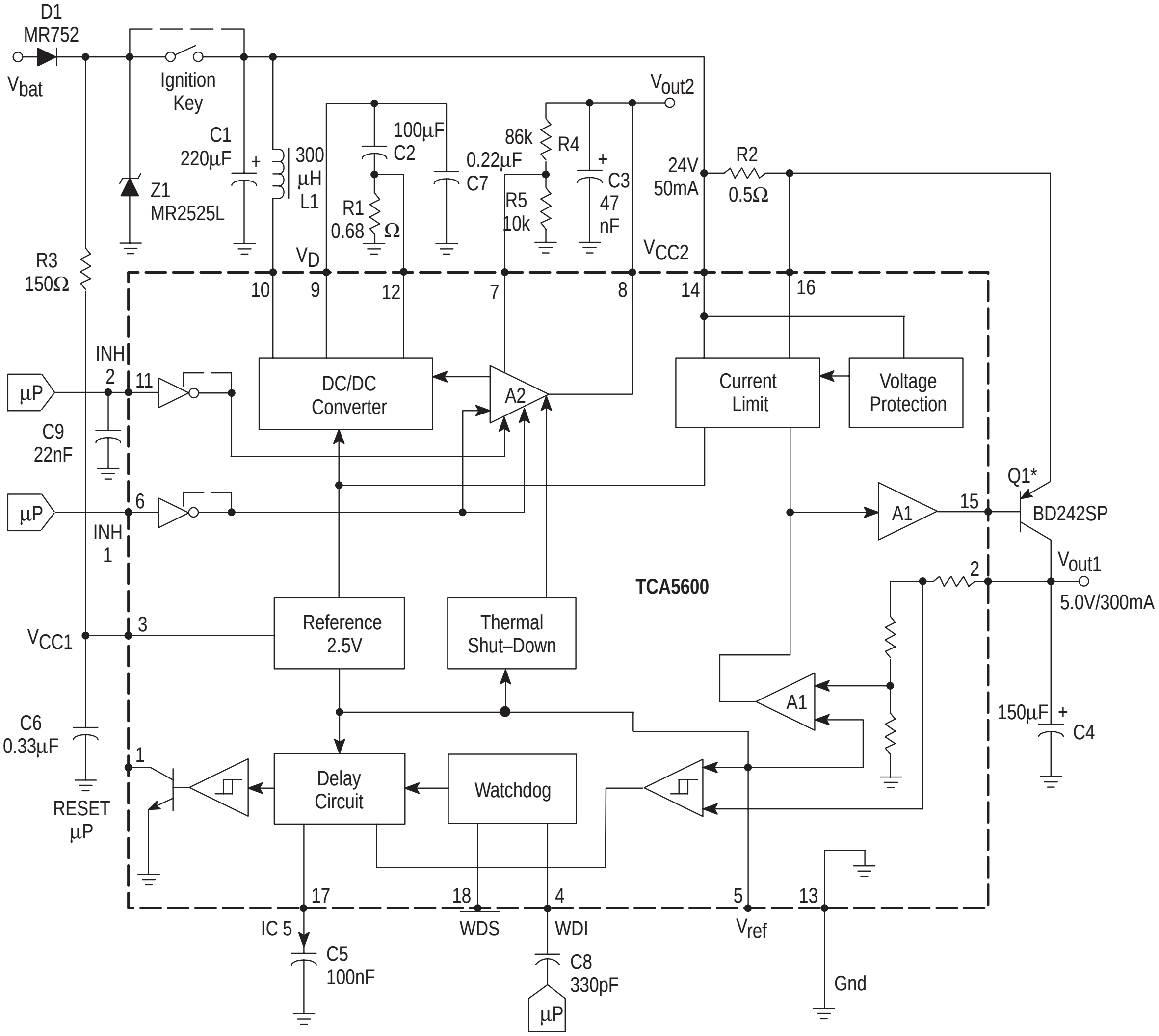
[I_{C5}, $V_{C5(H)}$, $V_{C5(L)}$: see Electrical Characteristics Table]

Figure 17. Typical $\overline{\text{RESET}}$ Timing Diagram (not to scale)



(a) Watchdog inhibited, $\overline{\text{WDS}}$ = “1”
(b) Watchdog operational, WDS = “0”

Figure 18. Typical Automative Application



MOTOROLA

TL494

SWITCHMODE™ Pulse Width Modulation Control Circuit

The TL494 is a fixed frequency, pulse width modulation control circuit designed primarily for SWITCHMODE power supply control.

- Complete Pulse Width Modulation Control Circuitry
- On–Chip Oscillator with Master or Slave Operation
- On–Chip Error Amplifiers
- On–Chip 5.0 V Reference
- Adjustable Deadtime Control
- Uncommitted Output Transistors Rated to 500 mA Source or Sink
- Output Control for Push–Pull or Single–Ended Operation
- Undervoltage Lockout

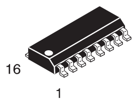
MAXIMUM RATINGS (Full operating ambient temperature range applies, unless otherwise noted.)

Rating	Symbol	TL494C	TL494I	Unit
Power Supply Voltage	V_{CC}	42		V
Collector Output Voltage	V_{C1}, V_{C2}	42		V
Collector Output Current (Each transistor) (Note 1)	I_{C1}, I_{C2}	500		mA
Amplifier Input Voltage Range	V_{IR}	–0.3 to +42		V
Power Dissipation @ $T_A \leq 45°C$	P_D	1000		mW
Thermal Resistance, Junction–to–Ambient	$R_{\theta JA}$	80		°C/W
Operating Junction Temperature	T_J	125		°C
Storage Temperature Range	T_{stg}	–55 to +125		°C
Operating Ambient Temperature Range TL494C TL494I	T_A	 0 to +70 –25 to +85		°C
Derating Ambient Temperature	T_A	45		°C

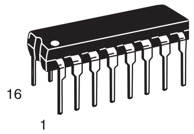
NOTE: 1. Maximum thermal limits must be observed.

SWITCHMODE
PULSE WIDTH MODULATION
CONTROL CIRCUIT

SEMICONDUCTOR
TECHNICAL DATA

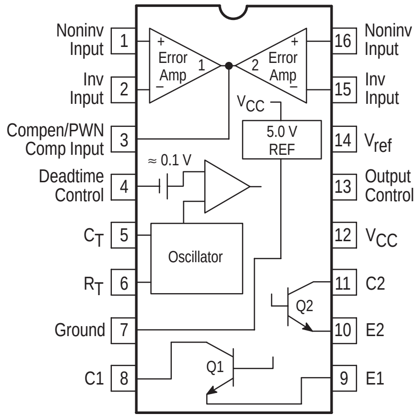


D SUFFIX
PLASTIC PACKAGE
CASE 751B
(SO–16)



N SUFFIX
PLASTIC PACKAGE
CASE 648

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
TL494CD	T_A = 0° to +70°C	SO–16
TL494CN		Plastic
TL494IN	T_A = – 25° to +85°C	Plastic

RECOMMENDED OPERATING CONDITIONS

Characteristics	Symbol	Min	Typ	Max	Unit
Power Supply Voltage	V_{CC}	7.0	15	40	V
Collector Output Voltage	V_{C1}, V_{C2}	–	30	40	V
Collector Output Current (Each transistor)	I_{C1}, I_{C2}	–	–	200	mA
Amplified Input Voltage	V_{in}	–0.3	–	V_{CC} – 2.0	V
Current Into Feedback Terminal	I_{fb}	–	–	0.3	mA
Reference Output Current	I_{ref}	–	–	10	mA
Timing Resistor	R_T	1.8	30	500	kΩ
Timing Capacitor	C_T	0.0047	0.001	10	µF
Oscillator Frequency	f_{osc}	1.0	40	200	kHz

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V, C_T = 0.01 µF, R_T = 12 kΩ, unless otherwise noted.)

For typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies, unless otherwise noted.

Characteristics	Symbol	Min	Typ	Max	Unit
REFERENCE SECTION					
Reference Voltage (I_O = 1.0 mA)	V_{ref}	4.75	5.0	5.25	V
Line Regulation (V_{CC} = 7.0 V to 40 V)	Reg_{line}	–	2.0	25	mV
Load Regulation (I_O = 1.0 mA to 10 mA)	Reg_{load}	–	3.0	15	mV
Short Circuit Output Current (V_{ref} = 0 V)	I_{SC}	15	35	75	mA
OUTPUT SECTION					
Collector Off–State Current (V_{CC} = 40 V, V_{CE} = 40 V)	$I_{C(off)}$	–	2.0	100	µA
Emitter Off–State Current V_{CC} = 40 V, V_C = 40 V, V_E = 0 V)	$I_{E(off)}$	–	–	–100	µA
Collector–Emitter Saturation Voltage (Note 2)					V
Common–Emitter (V_E = 0 V, I_C = 200 mA)	$V_{sat(C)}$	–	1.1	1.3	
Emitter–Follower (V_C = 15 V, I_E = –200 mA)	$V_{sat(E)}$	–	1.5	2.5	
Output Control Pin Current					
Low State (V_{OC} ≤ 0.4 V)	I_{OCL}	–	10	–	µA
High State (V_{OC} = V_{ref})	I_{OCH}	–	0.2	3.5	mA
Output Voltage Rise Time	t_r				ns
Common–Emitter (See Figure 12)		–	100	200	
Emitter–Follower (See Figure 13)		–	100	200	
Output Voltage Fall Time	t_f				ns
Common–Emitter (See Figure 12)		–	25	100	
Emitter–Follower (See Figure 13)		–	40	100	

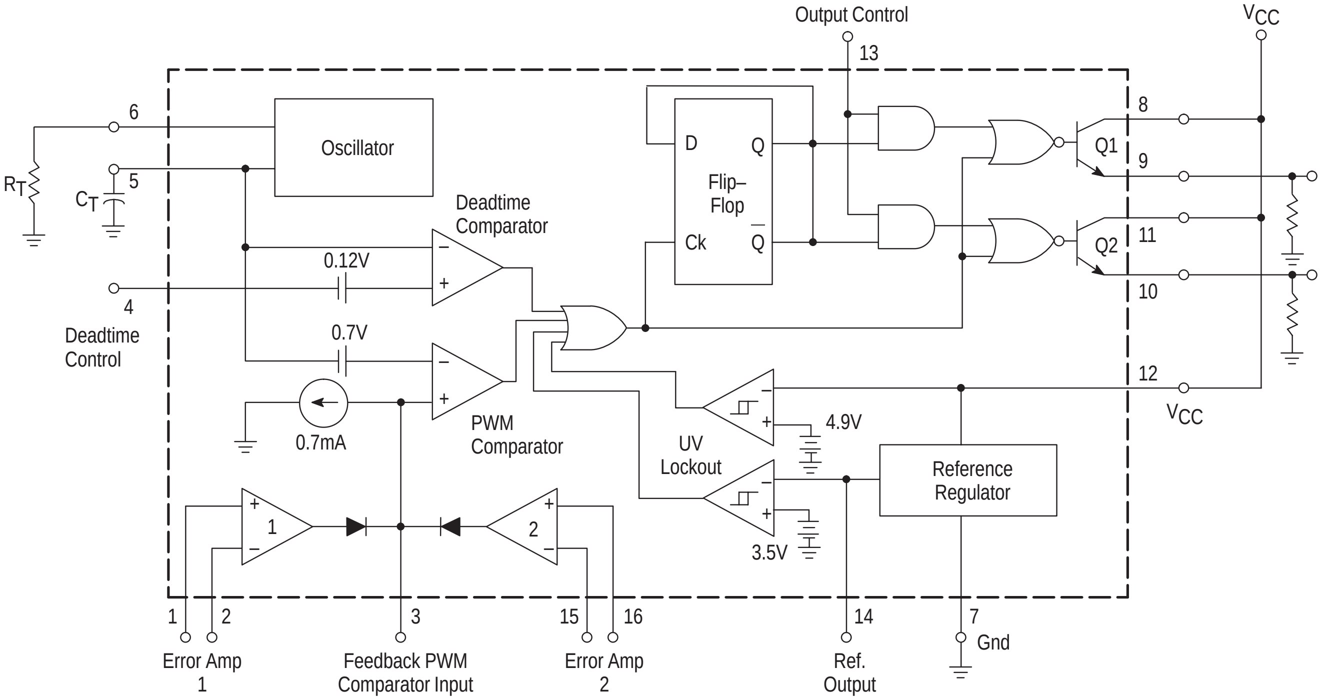
NOTE: 2. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient temperature as possible.

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V, C_T = 0.01 µF, R_T = 12 kΩ, unless otherwise noted.)
For typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies, unless otherwise noted.

Characteristics	Symbol	Min	Typ	Max	Unit
ERROR AMPLIFIER SECTION					
Input Offset Voltage ($V_{O\,(Pin\,3)}$ = 2.5 V)	V_{IO}	–	2.0	10	mV
Input Offset Current ($V_{O\,(Pin\,3)}$ = 2.5 V)	I_{IO}	–	5.0	250	nA
Input Bias Current ($V_{O\,(Pin\,3)}$ = 2.5 V)	I_{IB}	–	–0.1	–1.0	µA
Input Common Mode Voltage Range (V_{CC} = 40 V, T_A = 25°C)	V_{ICR}	–0.3 to V_{CC}–2.0			V
Open Loop Voltage Gain (ΔV_O = 3.0 V, V_O = 0.5 V to 3.5 V, R_L = 2.0 kΩ)	A_{VOL}	70	95	–	dB
Unity–Gain Crossover Frequency (V_O = 0.5 V to 3.5 V, R_L = 2.0 kΩ)	f_{C-}	–	350	–	kHz
Phase Margin at Unity–Gain (V_O = 0.5 V to 3.5 V, R_L = 2.0 kΩ)	ϕ_m	–	65	–	deg.
Common Mode Rejection Ratio (V_{CC} = 40 V)	CMRR	65	90	–	dB
Power Supply Rejection Ratio (ΔV_{CC} = 33 V, V_O = 2.5 V, R_L = 2.0 kΩ)	PSRR	–	100	–	dB
Output Sink Current ($V_{O\,(Pin\,3)}$ = 0.7 V)	I_{O-}	0.3	0.7	–	mA
Output Source Current ($V_{O\,(Pin\,3)}$ = 3.5 V)	I_{O+}	2.0	–4.0	–	mA
PWM COMPARATOR SECTION (Test Circuit Figure 11)					
Input Threshold Voltage (Zero Duty Cycle)	V_{TH}	–	2.5	4.5	V
Input Sink Current ($V_{(Pin\,3)}$ = 0.7 V)	I_{I-}	0.3	0.7	–	mA
DEADTIME CONTROL SECTION (Test Circuit Figure 11)					
Input Bias Current (Pin 4) ($V_{Pin\,4}$ = 0 V to 5.25 V)	$I_{IB\,(DT)}$	–	–2.0	–10	µA
Maximum Duty Cycle, Each Output, Push–Pull Mode	DC_{max}				%
($V_{Pin\,4}$ = 0 V, C_T = 0.01 µF, R_T = 12 kΩ)		45	48	50	
($V_{Pin\,4}$ = 0 V, C_T = 0.001 µF, R_T = 30 kΩ)		–	45	50	
Input Threshold Voltage (Pin 4)	V_{th}				V
(Zero Duty Cycle)		–	2.8	3.3	
(Maximum Duty Cycle)		0	–	–	
OSCILLATOR SECTION					
Frequency (C_T = 0.001 µF, R_T = 30 kΩ)	f_{osc}	–	40	–	kHz
Standard Deviation of Frequency* (C_T = 0.001 µF, R_T = 30 kΩ)	σf_{osc}	–	3.0	–	%
Frequency Change with Voltage (V_{CC} = 7.0 V to 40 V, T_A = 25°C)	Δf_{osc} (ΔV)	–	0.1	–	%
Frequency Change with Temperature (ΔT_A = T_{low} to T_{high}) (C_T = 0.01 µF, R_T = 12 kΩ)	Δf_{osc} (ΔT)	–	–	12	%
UNDERVOLTAGE LOCKOUT SECTION					
Turn–On Threshold (V_{CC} increasing, I_{ref} = 1.0 mA)	V_{th}	5.5	6.43	7.0	V
TOTAL DEVICE					
Standby Supply Current (Pin 6 at V_{ref}, All other inputs and outputs open)	I_{CC}				mA
(V_{CC} = 15 V)		–	5.5	10	
(V_{CC} = 40 V)		–	7.0	15	
Average Supply Current (C_T = 0.01 µF, R_T = 12 kΩ, $V_{(Pin\,4)}$ = 2.0 V) (V_{CC} = 15 V) (See Figure 12)		–	7.0	–	mA

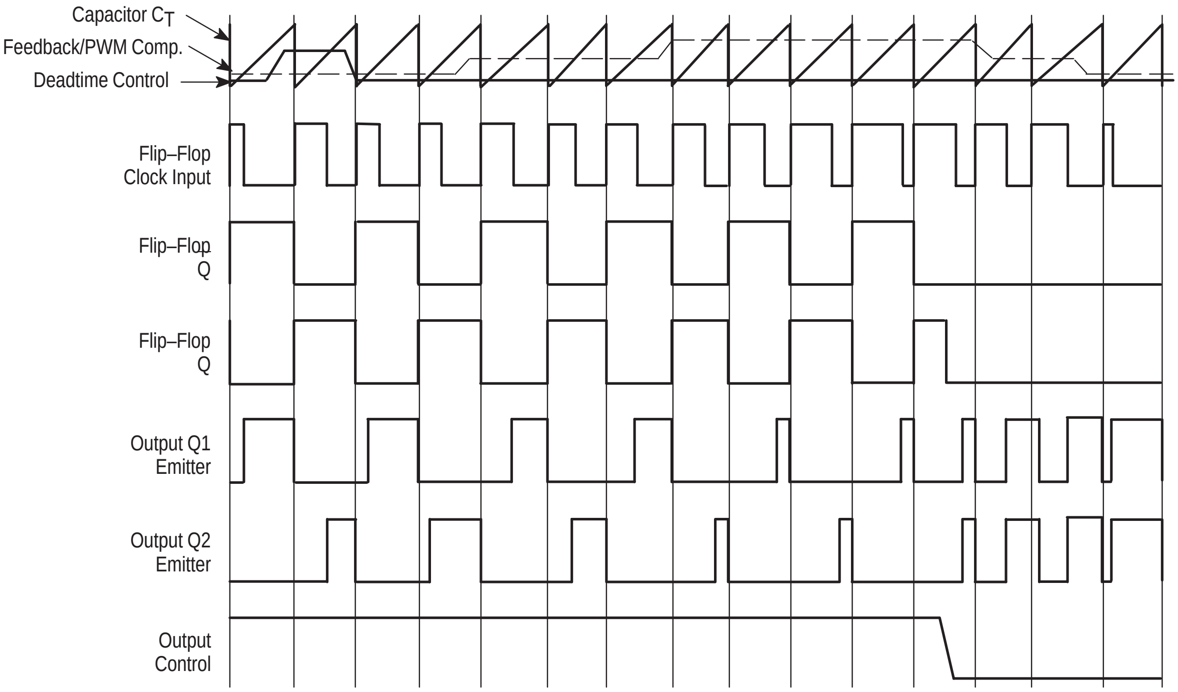
* Standard deviation is a measure of the statistical distribution about the mean as derived from the formula, $\sigma \sqrt{\frac{\sum_{n=1}^{N}(X_n - \overline{X})^2}{N-1}}$

Figure 1. Representative Block Diagram



This device contains 46 active transistors.

Figure 2. Timing Diagram



APPLICATIONS INFORMATION

Description

The TL494 is a fixed–frequency pulse width modulation control circuit, incorporating the primary building blocks required for the control of a switching power supply. (See Figure 1.) An internal–linear sawtooth oscillator is frequency–programmable by two external components, R_T and C_T. The approximate oscillator frequency is determined by:

$$f_{OSC} \approx \frac{1.1}{R_T \bullet C_T}$$

For more information refer to Figure 3.

Output pulse width modulation is accomplished by comparison of the positive sawtooth waveform across capacitor C_T to either of two control signals. The NOR gates, which drive output transistors Q1 and Q2, are enabled only when the flip–flop clock–input line is in its low state. This happens only during that portion of time when the sawtooth voltage is greater than the control signals. Therefore, an increase in control–signal amplitude causes a corresponding linear decrease of output pulse width. (Refer to the Timing Diagram shown in Figure 2.)

The control signals are external inputs that can be fed into the deadtime control, the error amplifier inputs, or the feedback input. The deadtime control comparator has an effective 120 mV input offset which limits the minimum output deadtime to approximately the first 4% of the sawtooth–cycle time. This would result in a maximum duty cycle on a given output of 96% with the output control grounded, and 48% with it connected to the reference line. Additional deadtime may be imposed on the output by setting the deadtime–control input to a fixed voltage, ranging between 0 V to 3.3 V.

Functional Table

Input/Output Controls	Output Function	$\frac{f_{out}}{f_{osc}} =$
Grounded	Single–ended PWM @ Q1 and Q2	1.0
@ V_{ref}	Push–pull Operation	0.5

The pulse width modulator comparator provides a means for the error amplifiers to adjust the output pulse width from the maximum percent on–time, established by the deadtime control input, down to zero, as the voltage at the feedback pin varies from 0.5 V to 3.5 V. Both error amplifiers have a common mode input range from –0.3 V to (V_{CC} – 2V), and may be used to sense power–supply output voltage and current. The error–amplifier outputs are active high and are ORed together at the noninverting input of the pulse–width modulator comparator. With this configuration, the amplifier that demands minimum output on time, dominates control of the loop.

When capacitor C_T is discharged, a positive pulse is generated on the output of the deadtime comparator, which clocks the pulse–steering flip–flop and inhibits the output transistors, Q1 and Q2. With the output–control connected to the reference line, the pulse–steering flip–flop directs the modulated pulses to each of the two output transistors alternately for push–pull operation. The output frequency is equal to half that of the oscillator. Output drive can also be taken from Q1 or Q2, when single–ended operation with a maximum on–time of less than 50% is required. This is desirable when the output transformer has a ringback winding with a catch diode used for snubbing. When higher output–drive currents are required for single–ended operation, Q1 and Q2 may be connected in parallel, and the output–mode pin must be tied to ground to disable the flip–flop. The output frequency will now be equal to that of the oscillator.

The TL494 has an internal 5.0 V reference capable of sourcing up to 10 mA of load current for external bias circuits. The reference has an internal accuracy of ±5.0% with a typical thermal drift of less than 50 mV over an operating temperature range of 0° to 70°C.

Figure 3. Oscillator Frequency versus Timing Resistance

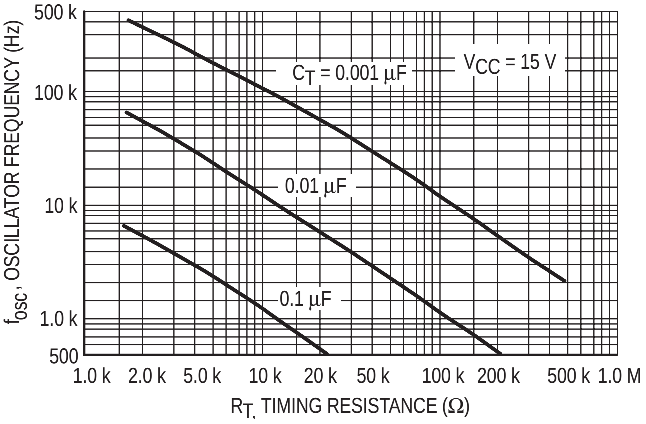


Figure 4. Open Loop Voltage Gain and Phase versus Frequency

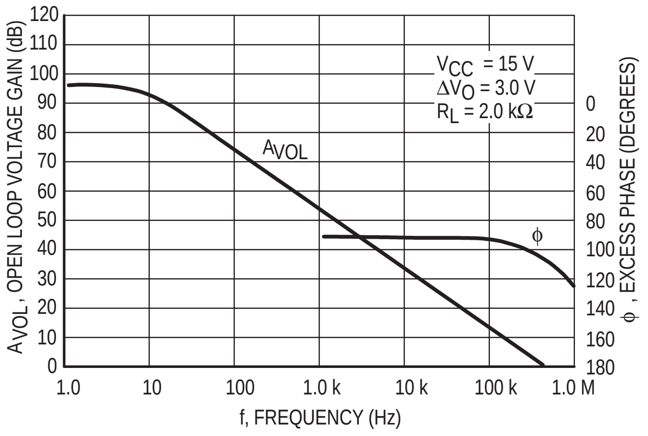


Figure 5. Percent Deadtime versus Oscillator Frequency

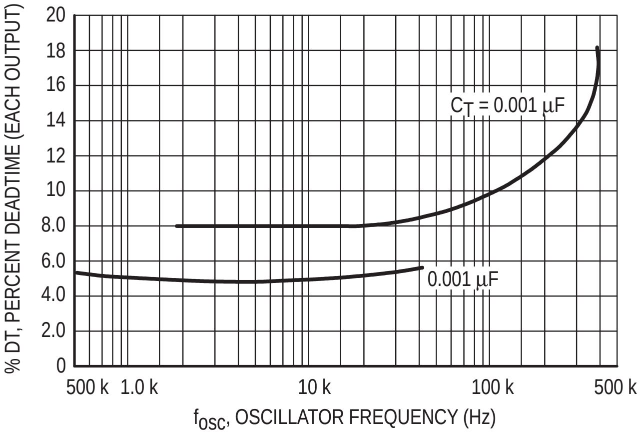


Figure 6. Percent Duty Cycle versus Deadtime Control Voltage

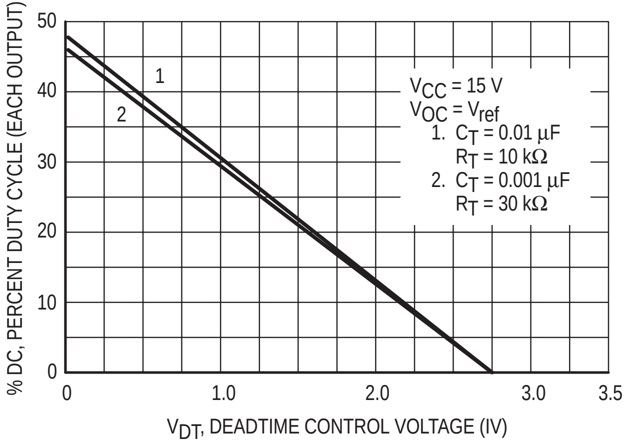


Figure 7. Emitter–Follower Configuration Output Saturation Voltage versus Emitter Current

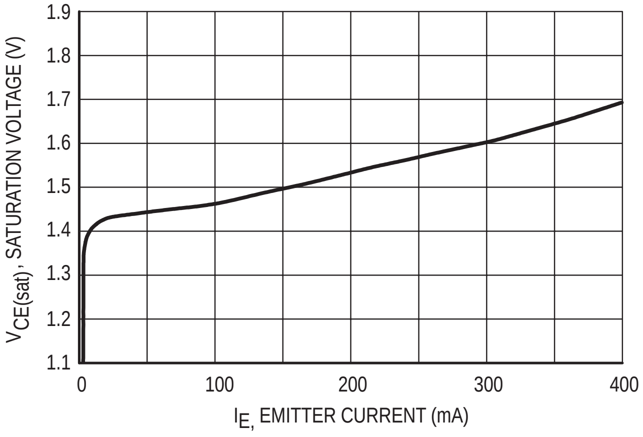


Figure 8. Common–Emitter Configuration Output Saturation Voltage versus Collector Current

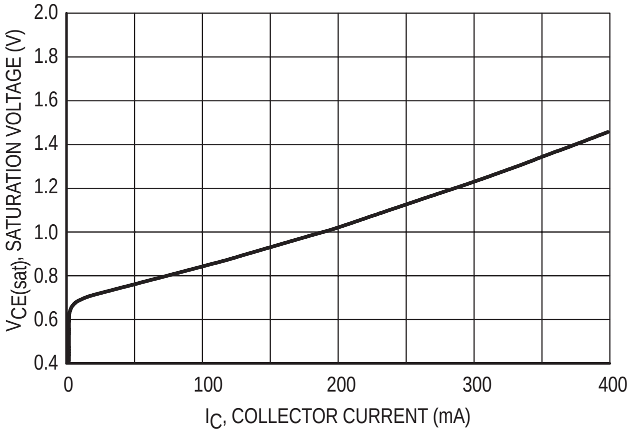


Figure 9. Standby Supply Current versus Supply Voltage

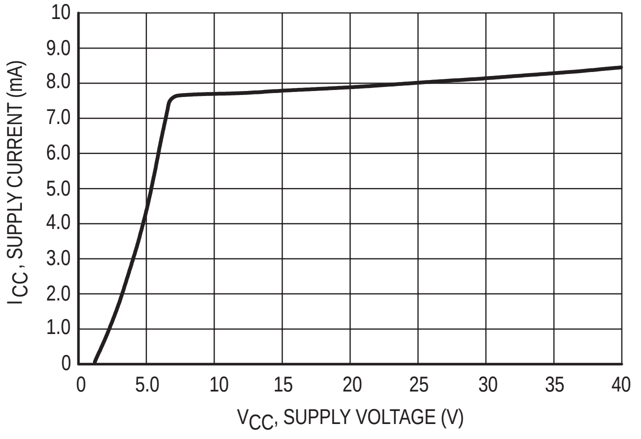


Figure 10. Error–Amplifier Characteristics

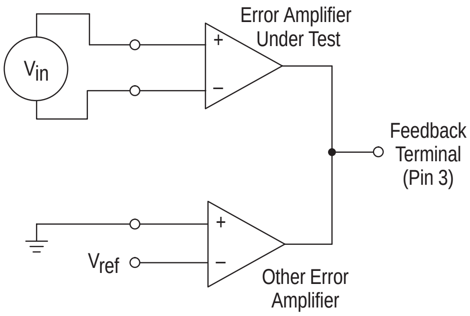


Figure 11. Deadtime and Feedback Control Circuit

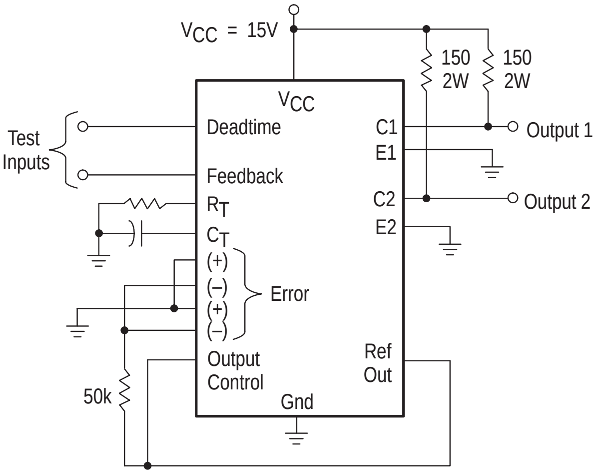


Figure 12. Common–Emitter Configuration Test Circuit and Waveform

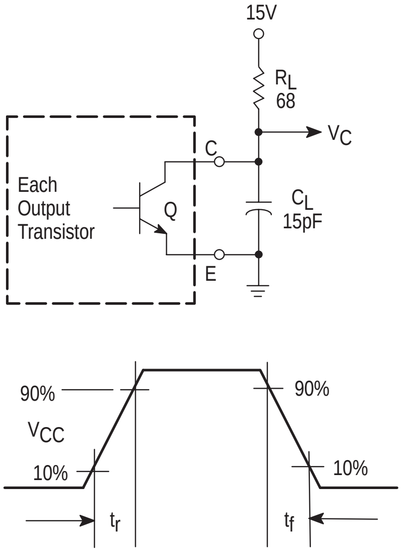


Figure 13. Emitter–Follower Configuration Test Circuit and Waveform

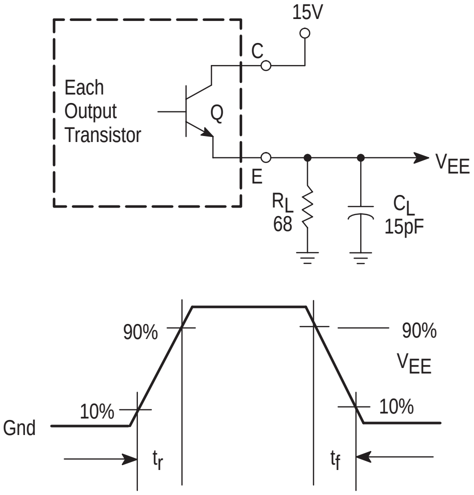


Figure 14. Error–Amplifier Sensing Techniques

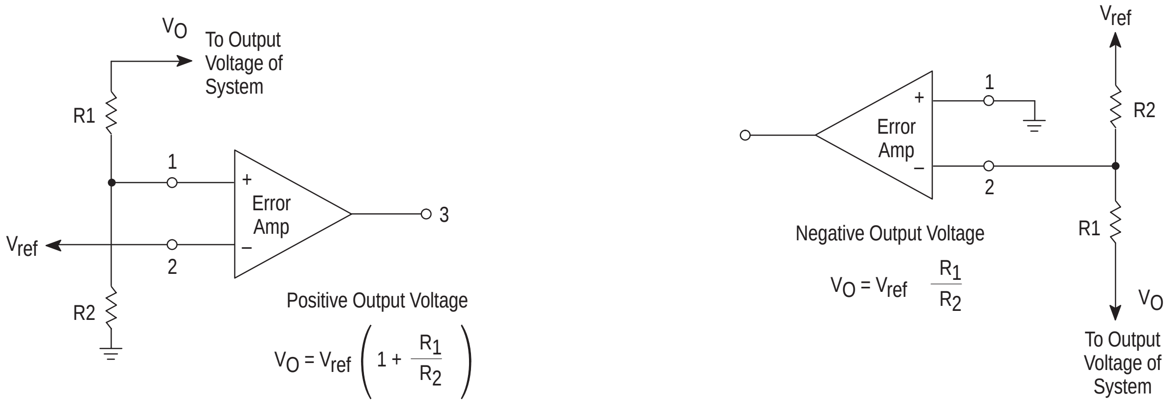
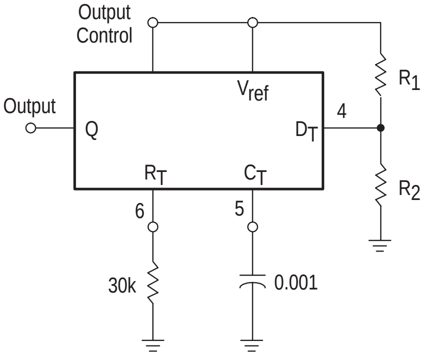


Figure 15. Deadtime Control Circuit



$$\text{Max. \% on Time, each output} \approx 45 - \left(\frac{80}{1 + \frac{R1}{R2}}\right)$$

Figure 16. Soft–Start Circuit

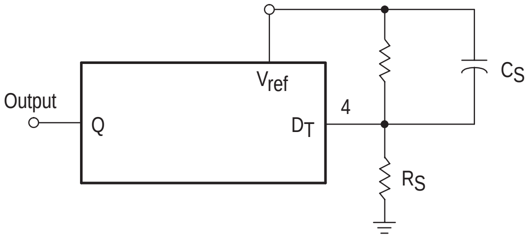


Figure 17. Output Connections for Single–Ended and Push–Pull Configurations

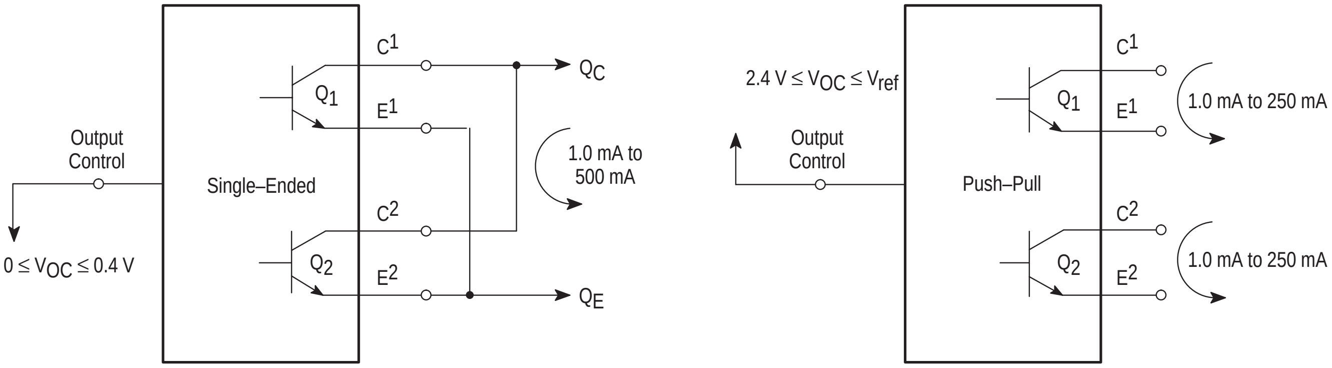


Figure 18. Slaving Two or More Control Circuits

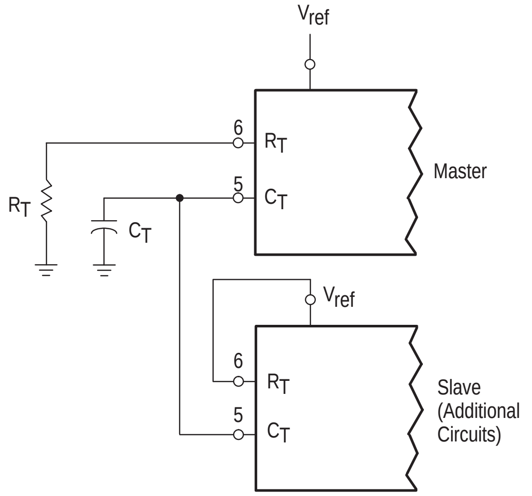


Figure 19. Operation with V_{in} > 40 V Using External Zener

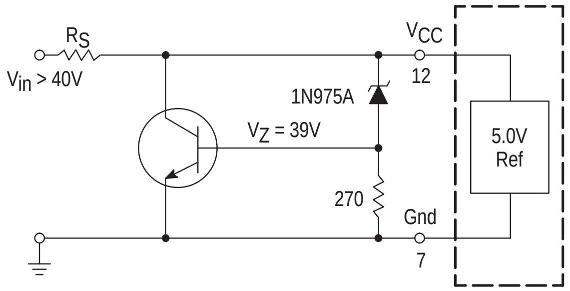
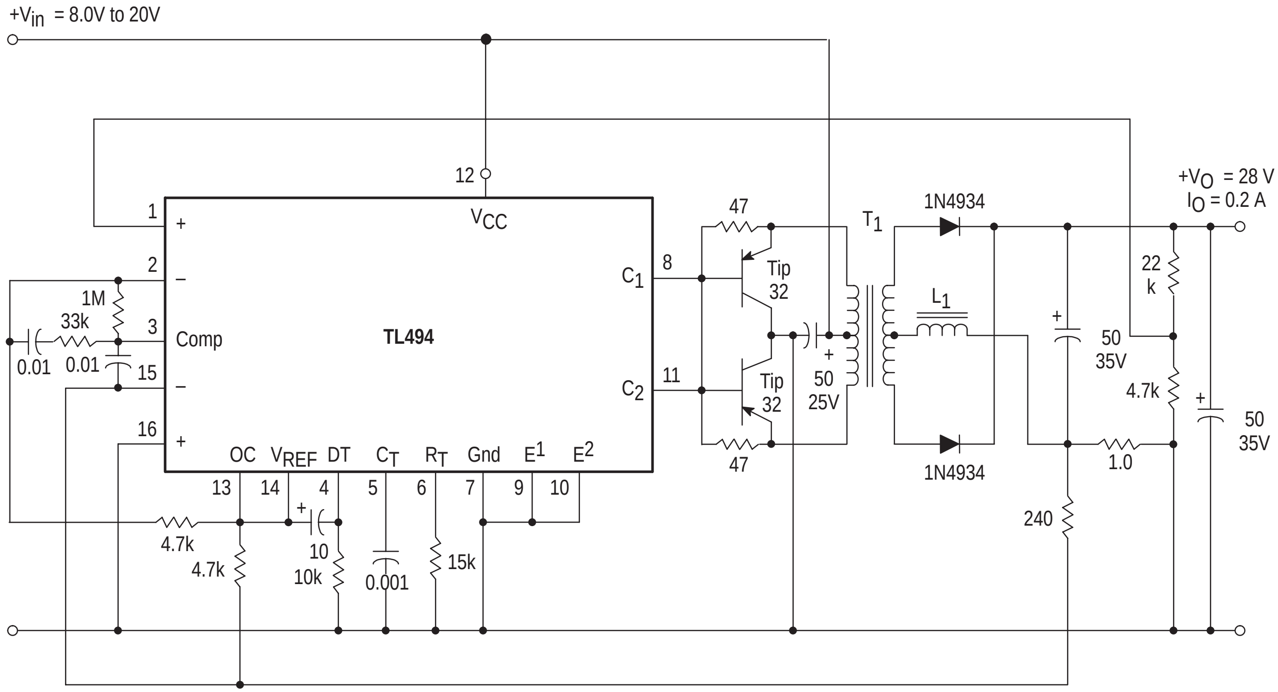


Figure 20. Pulse Width Modulated Push–Pull Converter



All capacitors in µF

Test	Conditions	Results
Line Regulation	V_{in} = 10 V to 40 V	14 mV 0.28%
Load Regulation	V_{in} = 28 V, I_O = 1.0 mA to 1.0 A	3.0 mV 0.06%
Output Ripple	V_{in} = 28 V, I_O = 1.0 A	65 mV pp P.A.R.D.
Short Circuit Current	V_{in} = 28 V, R_L = 0.1 Ω	1.6 A
Efficiency	V_{in} = 28 V, I_O = 1.0 A	71%

L1 – 3.5 mH @ 0.3 A
T1 – Primary: 20T C.T. #28 AWG
Secondary: 12OT C.T. #36 AWG
Core: Ferroxcube 1408P–L00–3CB

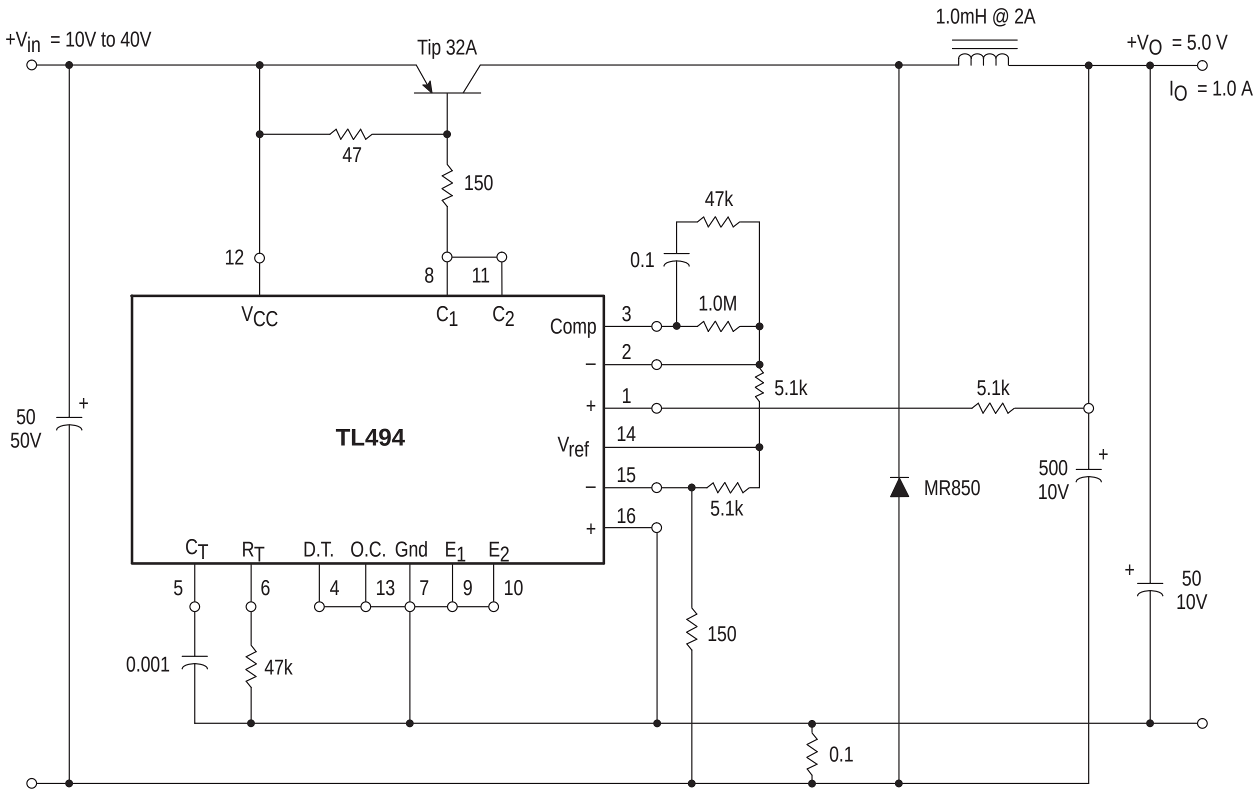


Figure 21. Pulse Width Modulated Step–Down Converter

Test	Conditions	Results
Line Regulation	V_{in} = 8.0 V to 40 V	3.0 mV 0.01%
Load Regulation	V_{in} = 12.6 V, I_O = 0.2 mA to 200 mA	5.0 mV 0.02%
Output Ripple	V_{in} = 12.6 V, I_O = 200 mA	40 mV pp P.A.R.D.
Short Circuit Current	V_{in} = 12.6 V, R_L = 0.1 Ω	250 mA
Efficiency	V_{in} = 12.6 V, I_O = 200 mA	72%

MOTOROLA

TL594

Precision Switchmode Pulse Width Modulation Control Circuit

The TL594 is a fixed frequency, pulse width modulation control circuit designed primarily for Switchmode power supply control.

- Complete Pulse Width Modulation Control Circuitry
- On–Chip Oscillator with Master or Slave Operation
- On–Chip Error Amplifiers
- On–Chip 5.0 V Reference, 1.5% Accuracy
- Adjustable Deadtime Control
- Uncommitted Output Transistors Rated to 500 mA Source or Sink
- Output Control for Push–Pull or Single–Ended Operation
- Undervoltage Lockout

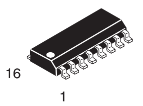
MAXIMUM RATINGS (Full operating ambient temperature range applies, unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	42	V
Collector Output Voltage	V_{C1}, V_{C2}	42	V
Collector Output Current (each transistor) (Note 1)	I_{C1}, I_{C2}	500	mA
Amplifier Input Voltage Range	V_{IR}	–0.3 to +42	V
Power Dissipation @ $T_A \leq 45°C$	P_D	1000	mW
Thermal Resistance, Junction–to–Ambient	$R_{\theta JA}$	80	°C/W
Operating Junction Temperature	T_J	125	°C
Storage Temperature Range	T_{stg}	–55 to +125	°C
Operating Ambient Temperature Range TL594ID, CN TL594CD, IN	T_A	 0 to +70 –25 to +85	°C
Derating Ambient Temperature	T_A	45	°C

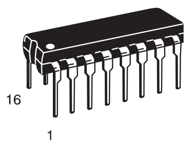
NOTES: 1. Maximum thermal limits must be observed.

PRECISION SWITCHMODE PULSE WIDTH MODULATION CONTROL CIRCUIT

SEMICONDUCTOR TECHNICAL DATA

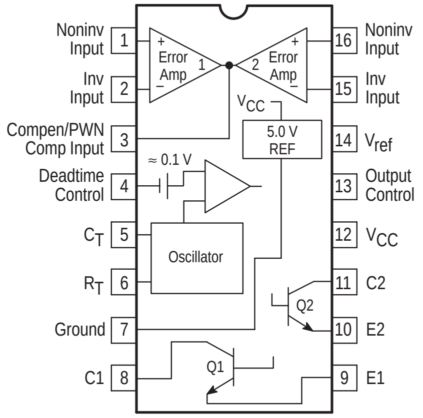


D SUFFIX
PLASTIC PACKAGE
CASE 751B
(SO–16)



N SUFFIX
PLASTIC PACKAGE
CASE 648

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
TL594CD	$T_A = 0°$ to $+70°C$	SO–16
TL594CN		Plastic
TL594IN	$T_A = –25°$ to $+85°C$	Plastic

RECOMMENDED OPERATING CONDITIONS

Characteristics	Symbol	Min	Typ	Max	Unit
Power Supply Voltage	V_{CC}	7.0	15	40	V
Collector Output Voltage	V_{C1}, V_{C2}	–	30	40	V
Collector Output Current (Each transistor)	I_{C1}, I_{C2}	–	–	200	mA
Amplified Input Voltage	V_{in}	0.3	–	V_{CC} – 2.0	V
Current Into Feedback Terminal	I_{fb}	–	–	0.3	mA
Reference Output Current	I_{ref}	–	–	10	mA
Timing Resistor	R_T	1.8	30	500	kΩ
Timing Capacitor	C_T	0.0047	0.001	10	µF
Oscillator Frequency	f_{osc}	1.0	40	200	kHz
PWM Input Voltage (Pins 3, 4, 13)	–	0.3	–	5.3	V

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V, C_T = 0.01 µF, R_T = 12 kΩ, unless otherwise noted.)
For typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies, unless otherwise noted.

Characteristics	Symbol	Min	Typ	Max	Unit
REFERENCE SECTION					
Reference Voltage	V_{ref}				V
(I_O = 1.0 mA, T_A = 25°C)		4.925	5.0	5.075	
(I_O = 1.0 mA)		4.9	–	5.1	
Line Regulation (V_{CC} = 7.0 V to 40 V)	Reg_{line}	–	2.0	25	mV
Load Regulation (I_O = 1.0 mA to 10 mA)	Reg_{load}	–	2.0	15	mV
Short Circuit Output Current (V_{ref} = 0 V)	I_{SC}	15	40	75	mA
OUTPUT SECTION					
Collector Off–State Current (V_{CC} = 40 V, V_{CE} = 40 V)	$I_{C(off)}$	–	2.0	100	µA
Emitter Off–State Current (V_{CC} = 40 V, V_C = 40 V, V_E = 0 V)	$I_{E(off)}$	–	–	–100	µA
Collector–Emitter Saturation Voltage (Note 2)					V
Common–Emitter (V_E = 0 V, I_C = 200 mA)	$V_{SAT(C)}$	–	1.1	1.3	
Emitter–Follower (V_C = 15 V, I_E = –200 mA)	$V_{SAT(E)}$	–	1.5	2.5	
Output Control Pin Current					µA
Low State (V_{OC} ≤ 0.4 V)	I_{OCL}	–	0.1	–	
High State (V_{OC} = V_{ref})	I_{OCH}	–	2.0	20	
Output Voltage Rise Time	t_r				ns
Common–Emitter (See Figure 13)		–	100	200	
Emitter–Follower (See Figure 14)		–	100	200	
Output Voltage Fall Time	t_f				ns
Common–Emitter (See Figure 13)		–	40	100	
Emitter–Follower (See Figure 14)		–	40	100	
ERROR AMPLIFIER SECTION					
Input Offset Voltage ($V_{O\ (Pin\ 3)}$ = 2.5 V)	V_{IO}	–	2.0	10	mV
Input Offset Current ($V_{O\ (Pin\ 3)}$ = 2.5 V)	I_{IO}	–	5.0	250	nA
Input Bias Current ($V_{O\ (Pin\ 3)}$ = 2.5 V)	I_{IB}	–	–0.1	–1.0	µA
Input Common Mode Voltage Range (V_{CC} = 40 V, T_A = 25°C)	V_{ICR}	0 to V_{CC}–2.0			V
Inverting Input Voltage Range	$V_{IR(INV)}$	–0.3 to V_{CC}–2.0			V
Open Loop Voltage Gain (ΔV_O = 3.0 V, V_O = 0.5 V to 3.5 V, R_L = 2.0 kΩ)	A_{VOL}	70	95	–	dB
Unity–Gain Crossover Frequency (V_O = 0.5 V to 3.5 V, R_L = 2.0 kΩ)	f_C	–	700	–	kHz
Phase Margin at Unity–Gain (V_O = 0.5 V to 3.5 V, R_L = 2.0 kΩ)	ϕm	–	65	–	deg.
Common Mode Rejection Ratio (V_{CC} = 40 V)	CMRR	65	90	–	dB
Power Supply Rejection Ratio (ΔV_{CC} = 33 V, V_O = 2.5 V, R_L = 2.0 kΩ)	PSRR	–	100	–	dB
Output Sink Current ($V_{O\ (Pin\ 3)}$ = 0.7 V)	I_O-	0.3	0.7	–	mA
Output Source Current ($V_{O\ (Pin\ 3)}$ = 3.5 V)	I_O+	–2.0	–4.0	–	mA

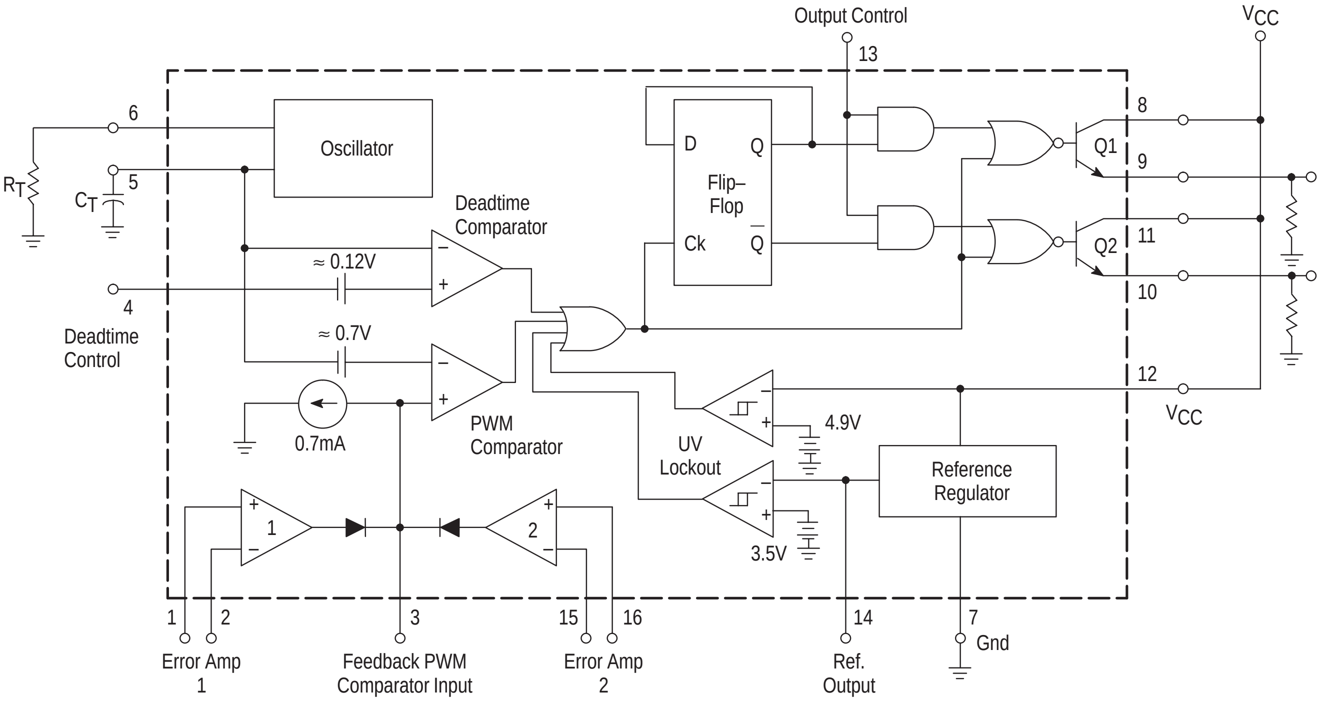
NOTE: 2. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient temperature as possible.

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V, C_T = 0.01 µF, R_T = 12 kΩ, unless otherwise noted.)
For typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies, unless otherwise noted.

Characteristics	Symbol	Min	Typ	Max	Unit
PWM COMPARATOR SECTION (Test Circuit Figure 11)					
Input Threshold Voltage (Zero Duty Cycle)	V_{TH}	–	3.6	4.5	V
Input Sink Current ($V_{Pin\ 3}$ = 0.7 V)	$I_{I–}$	0.3	0.7	–	mA
DEADTIME CONTROL SECTION (Test Circuit Figure 11)					
Input Bias Current (Pin 4) ($V_{Pin\ 4}$ = 0 V to 5.25 V)	$I_{IB\ (DT)}$	–	–2.0	–10	µA
Maximum Duty Cycle, Each Output, Push–Pull Mode	DC_{max}				%
($V_{Pin\ 4}$ = 0 V, C_T = 0.01 µF, R_T = 12 kΩ)		45	48	50	
($V_{Pin\ 4}$ = 0 V, C_T = 0.001 µF, R_T = 30 kΩ)		–	45	–	
Input Threshold Voltage (Pin 4)	V_{TH}				V
(Zero Duty Cycle)		–	2.8	3.3	
(Maximum Duty Cycle)		0	–	–	
OSCILLATOR SECTION					
Frequency	f_{osc}				kHz
(C_T = 0.001 µF, R_T = 30 kΩ)		–	40	–	
(C_T = 0.01 µF, R_T = 12 kΩ, T_A = 25°C)		9.2	10	10.8	
(C_T = 0.01 µF, R_T = 12 kΩ, T_A = T_{low} to T_{high})		9.0	–	12	
Standard Deviation of Frequency* (C_T = 0.001 µF, R_T = 30 kΩ)	σf_{osc}	–	1.5	–	%
Frequency Change with Voltage (V_{CC} = 7.0 V to 40 V, T_A = 25°C)	Δf_{osc} (ΔV)	–	0.2	1.0	%
Frequency Change with Temperature (ΔT_A = T_{low} to T_{high}, C_T = 0.01 µF, R_T = 12 kΩ)	Δf_{osc} (ΔT)	–	4.0	–	%
UNDERVOLTAGE LOCKOUT SECTION					
Turn–On Threshold (V_{CC} Increasing, I_{ref} = 1.0 mA)	V_{th}				V
T_A = 25°C		4.0	5.2	6.0	
T_A = T_{low} to T_{high}		3.5	–	6.5	
Hysteresis	V_H				mV
TL594C,I		100	150	300	
TL594M		50	150	300	
TOTAL DEVICE					
Standby Supply Current (Pin 6 at V_{ref}, All other inputs and outputs open)	I_{CC}				mA
(V_{CC} = 15 V)		–	8.0	15	
(V_{CC} = 40 V)		–	8.0	18	
Average Supply Current ($V_{Pin\ 4}$ = 2.0 V, C_T = 0.01 µF, R_T = 12 kΩ, V_{CC} = 15 V, See Figure 11)		–	11	–	mA

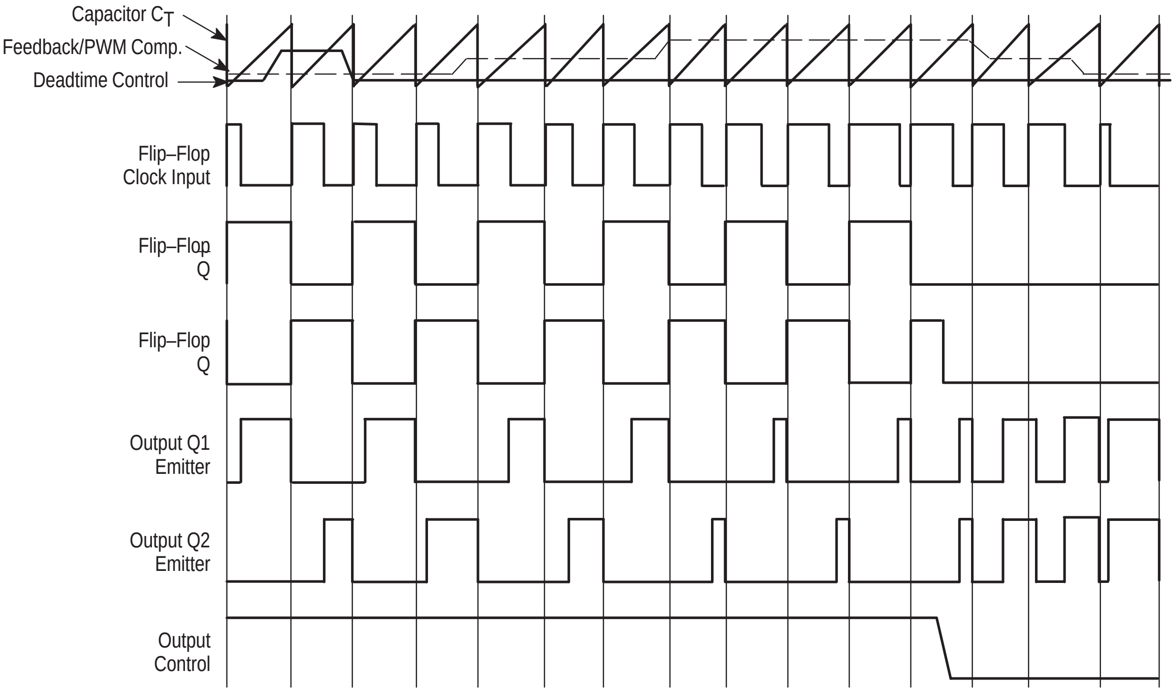
* Standard deviation is a measure of the statistical distribution about the mean as derived from the formula, $\sigma \sqrt{\frac{\sum_{n=1}^{N}(X_n-\overline{X})^2}{N-1}}$

Figure 1. Representative Block Diagram



This device contains 46 active transistors.

Figure 2. Timing Diagram



APPLICATIONS INFORMATION

Description

The TL594 is a fixed–frequency pulse width modulation control circuit, incorporating the primary building blocks required for the control of a switching power supply. (See Figure 1.) An internal–linear sawtooth oscillator is frequency–programmable by two external components, R_T and C_T. The approximate oscillator frequency is determined by:

$$f_{osc} \approx \frac{1.1}{R_T \bullet C_T}$$

For more information refer to Figure 3.

Output pulse width modulation is accomplished by comparison of the positive sawtooth waveform across capacitor C_T to either of two control signals. The NOR gates, which drive output transistors Q1 and Q2, are enabled only when the flip–flop clock–input line is in its low state. This happens only during that portion of time when the sawtooth voltage is greater than the control signals. Therefore, an increase in control–signal amplitude causes a corresponding linear decrease of output pulse width. (Refer to the Timing Diagram shown in Figure 2.)

The control signals are external inputs that can be fed into the deadtime control, the error amplifier inputs, or the feedback input. The deadtime control comparator has an effective 120 mV input offset which limits the minimum output deadtime to approximately the first 4% of the sawtooth–cycle time. This would result in a maximum duty cycle on a given output of 96% with the output control grounded, and 48% with it connected to the reference line. Additional deadtime may be imposed on the output by setting the deadtime–control input to a fixed voltage, ranging between 0 V to 3.3 V.

The pulse width modulator comparator provides a means for the error amplifiers to adjust the output pulse width from the maximum percent on–time, established by the deadtime control input, down to zero, as the voltage at the feedback pin varies from 0.5 V to 3.5 V. Both error amplifiers have a common–mode input range from –0.3 V to (V_{CC} – 2 V), and may be used to sense power–supply output voltage and current. The error–amplifier outputs are active high and are ORed together at the noninverting input of the pulse–width modulator comparator. With this configuration, the amplifier that demands minimum output on time, dominates control of the loop.

Functional Table

Input/Output Controls	Output Function	$\frac{f_{out}}{f_{osc}}$ =
Grounded	Single–ended PWM @ Q1 and Q2	1.0
@ V_{ref}	Push–pull Operation	0.5

When capacitor C_T is discharged, a positive pulse is generated on the output of the deadtime comparator, which clocks the pulse–steering flip–flop and inhibits the output transistors, Q1 and Q2. With the output–control connected to the reference line, the pulse–steering flip–flop directs the modulated pulses to each of the two output transistors alternately for push–pull operation. The output frequency is equal to half that of the oscillator. Output drive can also be taken from Q1 or Q2, when single–ended operation with a maximum on–time of less than 50% is required. This is desirable when the output transformer has a ringback winding with a catch diode used for snubbing. When higher output–drive currents are required for single–ended operation, Q1 and Q2 may be connected in parallel, and the output–mode pin must be tied to ground to disable the flip–flop. The output frequency will now be equal to that of the oscillator.

The TL594 has an internal 5.0 V reference capable of sourcing up to 10 mA of load current for external bias circuits. The reference has an internal accuracy of ±1.5% with a typical thermal drift of less than 50 mV over an operating temperature range of 0° to 70°C.

Figure 3. Oscillator Frequency versus Timing Resistance

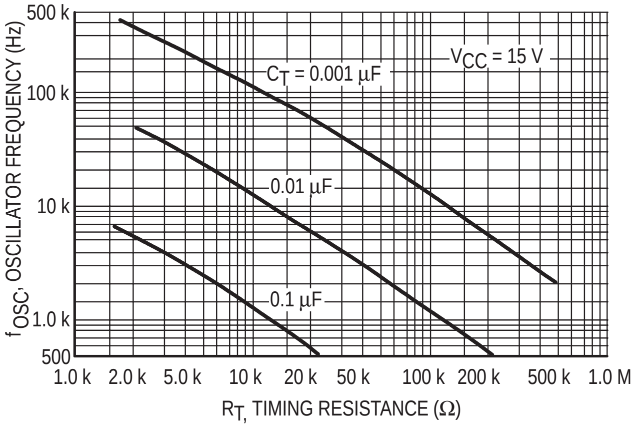


Figure 4. Open Loop Voltage Gain and Phase versus Frequency

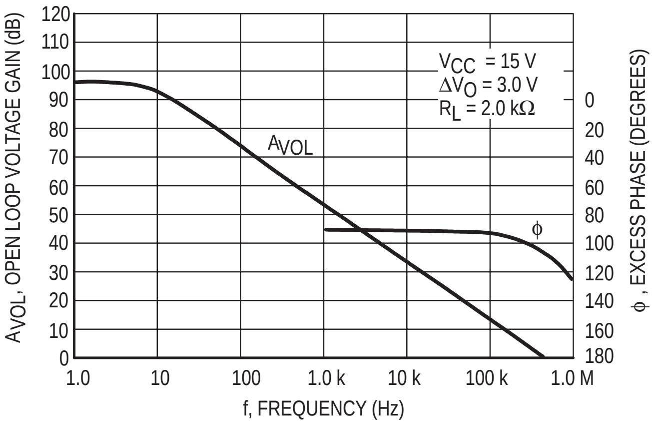


Figure 5. Percent Deadtime versus Oscillator Frequency

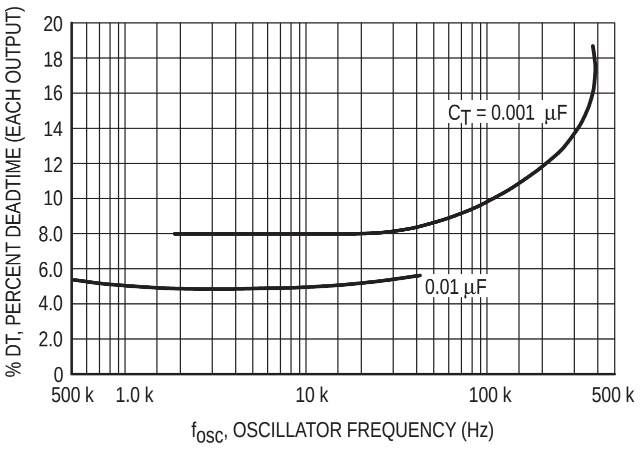


Figure 6. Percent Duty Cycle versus Deadtime Control Voltage

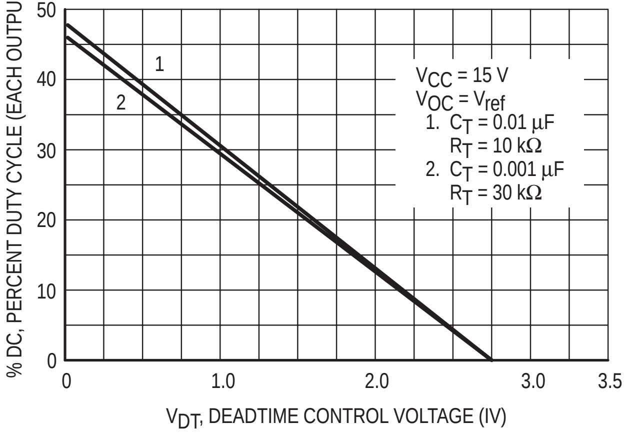


Figure 7. Emitter–Follower Configuration Output Saturation Voltage versus Emitter Current

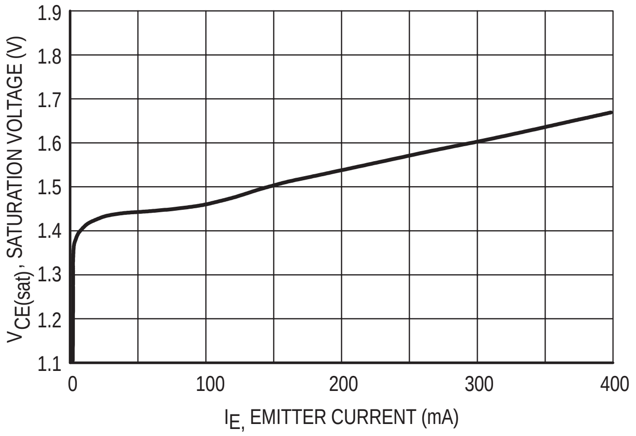


Figure 8. Common–Emitter Configuration Output Saturation Voltage versus Collector Current

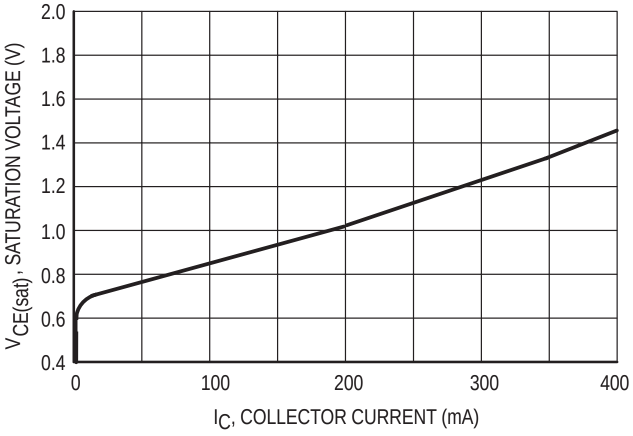


Figure 9. Standby Supply Current versus Supply Voltage

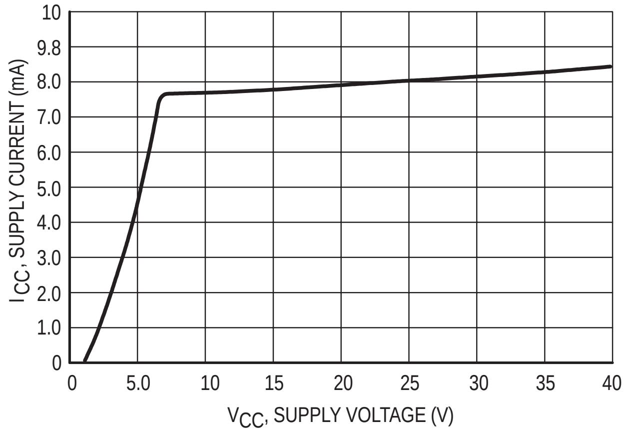


Figure 10. Undervoltage Lockout Thresholds versus Reference Load Current

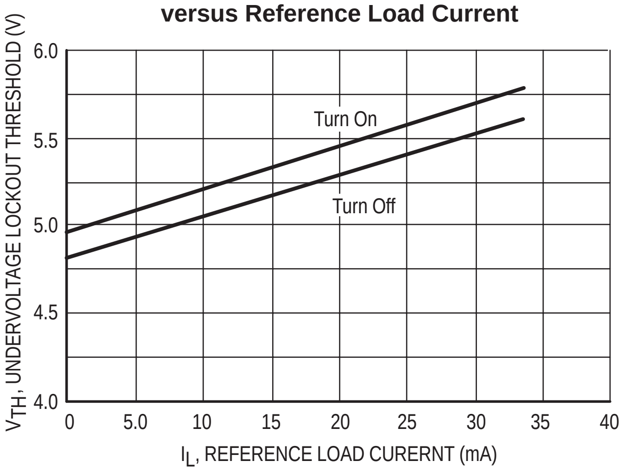


Figure 11. Error–Amplifier Characteristics

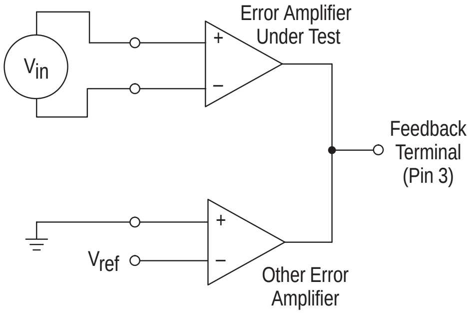


Figure 12. Deadtime and Feedback Control Circuit

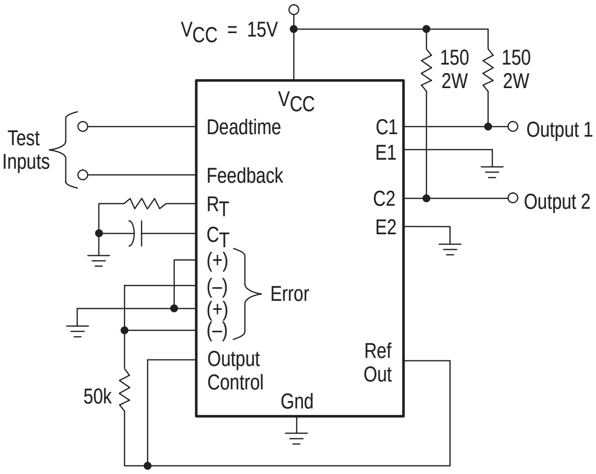


Figure 13. Common–Emitter Configuration Test Circuit and Waveform

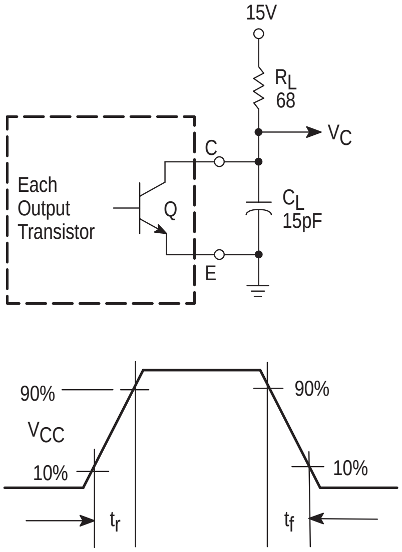


Figure 14. Emitter–Follower Configuration Test Circuit and Waveform

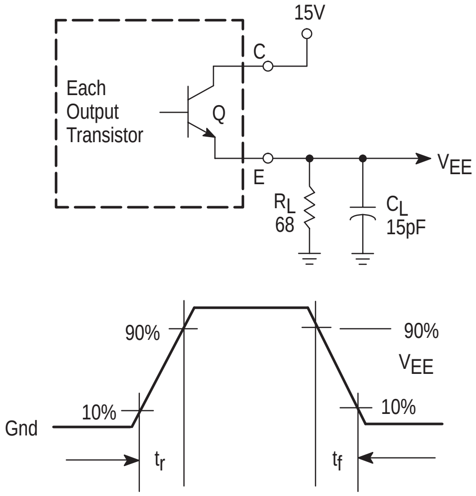


Figure 15. Error–Amplifier Sensing Techniques

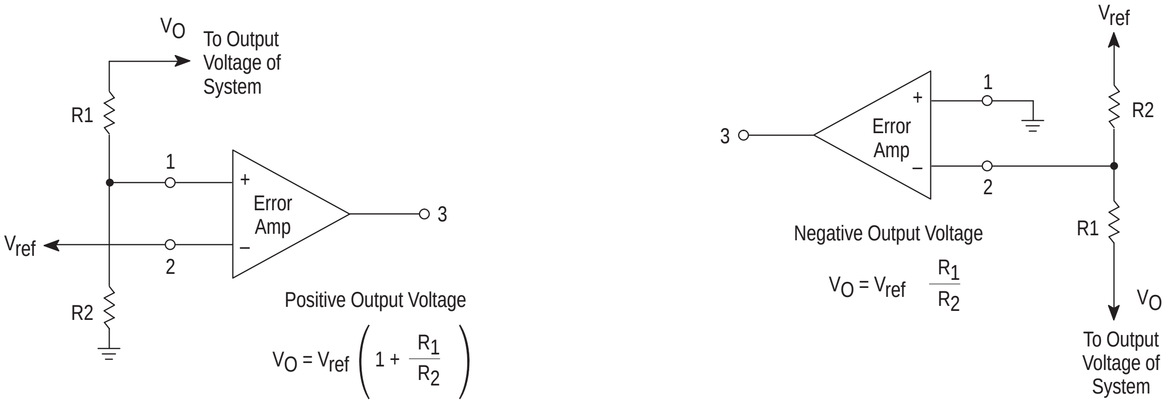
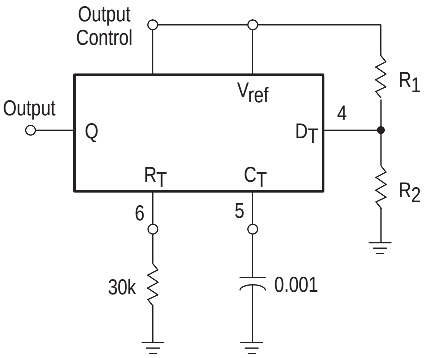


Figure 16. Deadtime Control Circuit



$$\text{Max. \% on Time, each output} \approx 45 - \left(\frac{80}{1 + \frac{R1}{R2}}\right)$$

Figure 17. Soft–Start Circuit

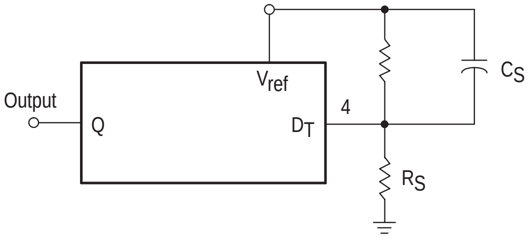


Figure 18. Output Connections for Single–Ended and Push–Pull Configurations

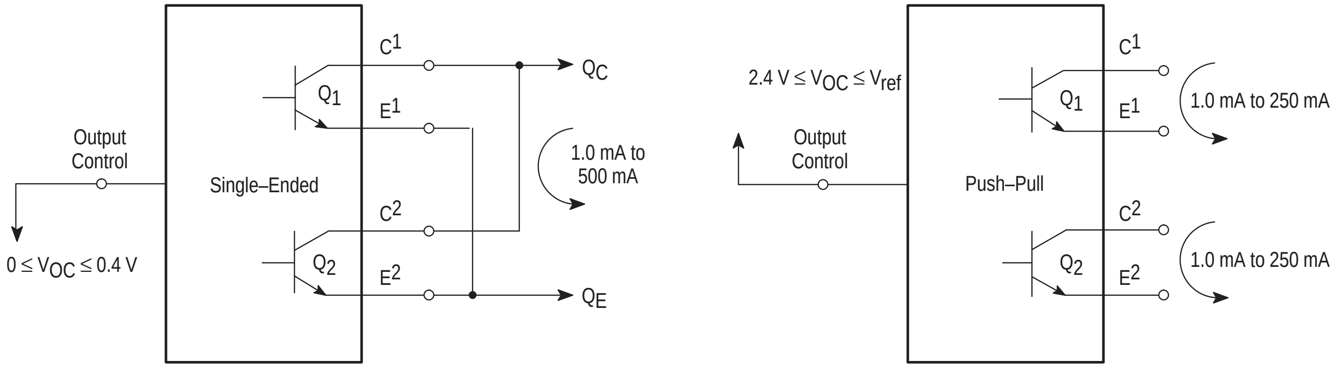


Figure 19. Slaving Two or More Control Circuits

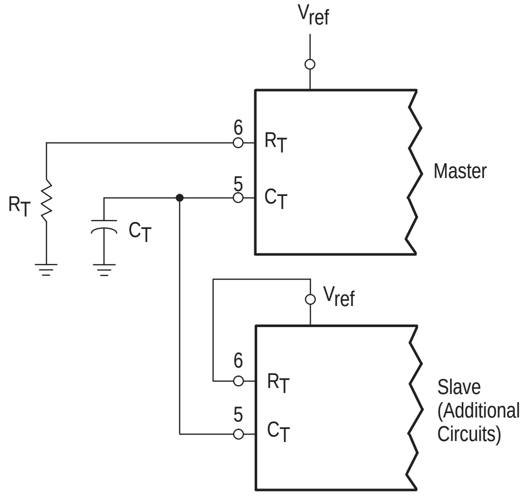


Figure 20. Operation with V_{in} > 40 V Using External Zener

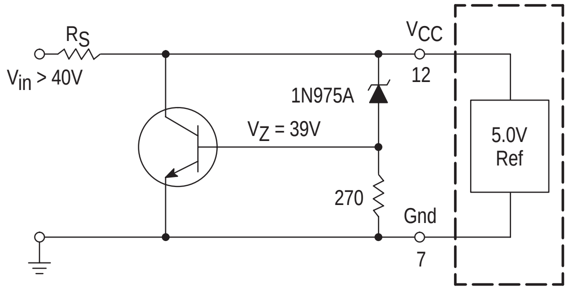
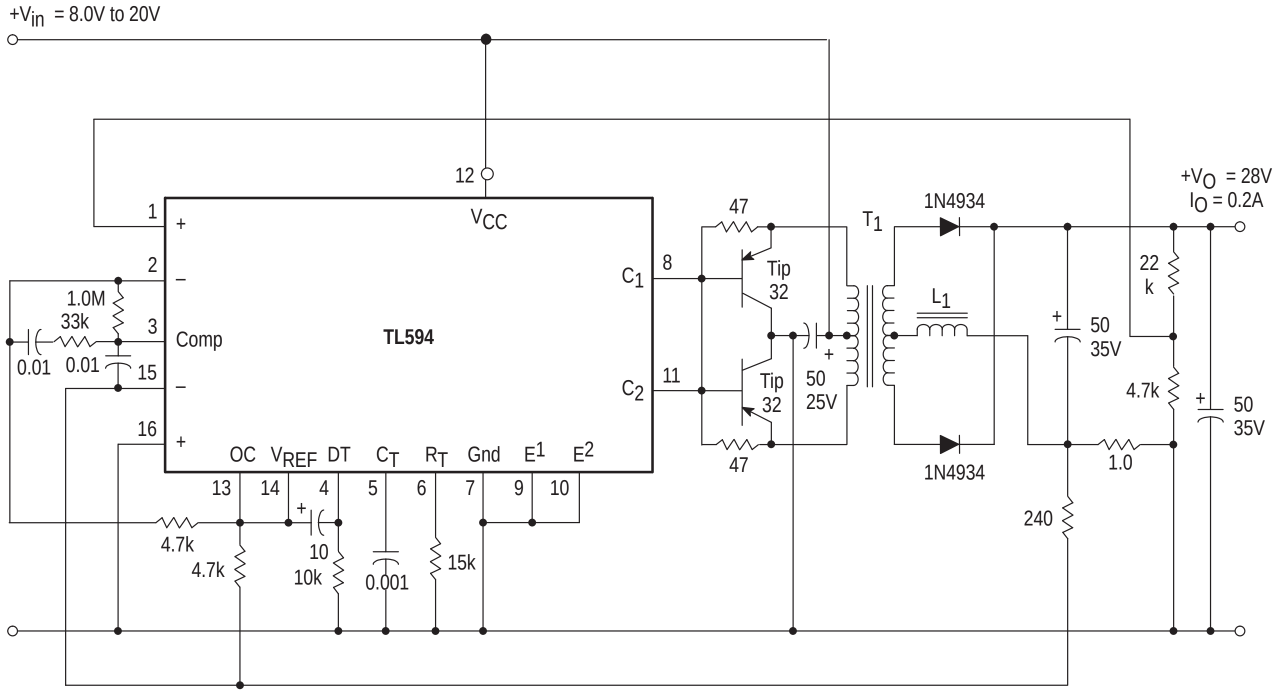


Figure 21. Pulse Width Modulated Push–Pull Converter

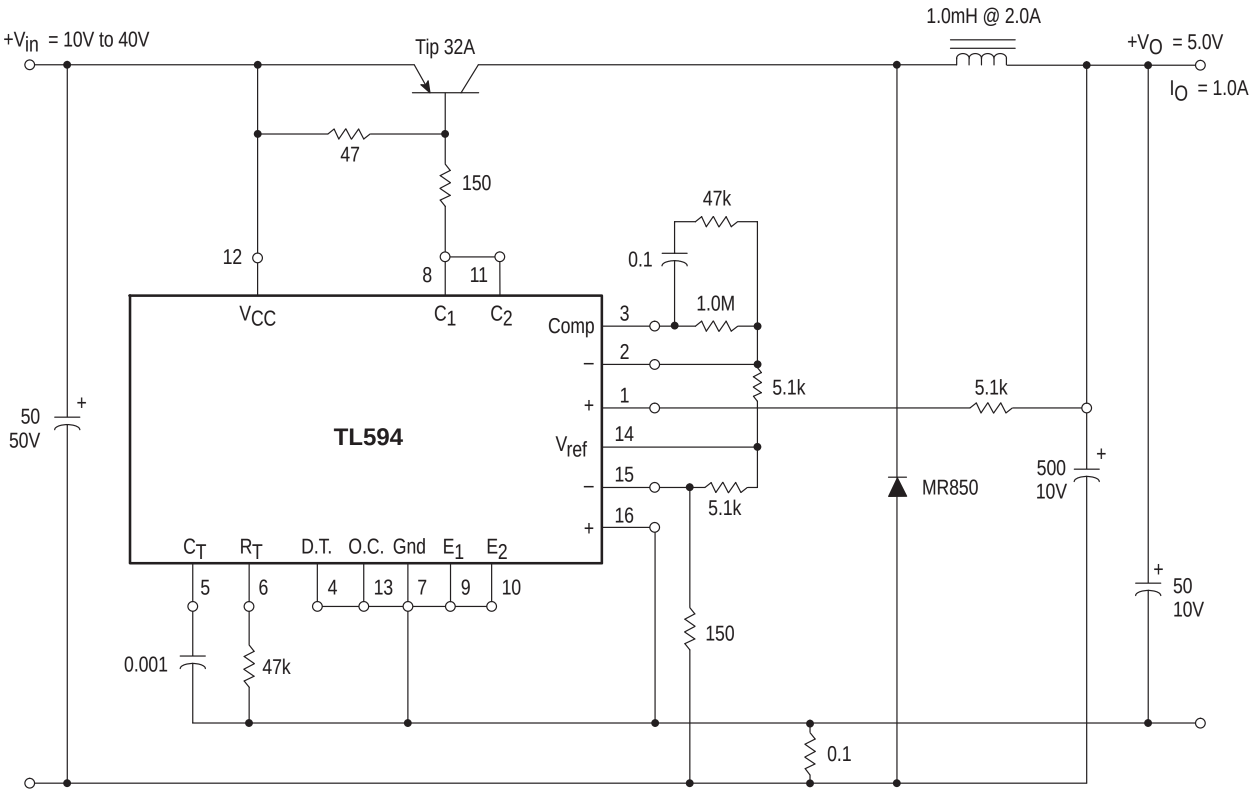


All capacitors in µF

Test	Conditions	Results
Line Regulation	V_{in} = 10 V to 40 V	14 mV 0.28%
Load Regulation	V_{in} = 28 V, I_O = 1.0 mA to 1.0 A	3.0 mV 0.06%
Output Ripple	V_{in} = 28 V, I_O = 1.0 A	65 mVpp P.A.R.D.
Short Circuit Current	V_{in} = 28 V, R_L = 0.1 Ω	1.6 A
Efficiency	V_{in} = 28 V, I_O = 1.0 A	71%

L1 – 3.5 mH @ 0.3 A
T1 – Primary: 20T C.T. #28 AWG
Secondary: 12OT C.T. #36 AWG
Core: Ferroxcube 1408P–L00–3CB

Figure 22. Pulse Width Modulated Step–Down Converter



Test	Conditions	Results
Line Regulation	V_{in} = 8.0 V to 40 V	3.0 mV 0.01%
Load Regulation	V_{in} = 12.6 V, I_O = 0.2 mA to 200 mA	5.0 mV 0.02%
Output Ripple	V_{in} = 12.6 V, I_O = 200 mA	40 mVpp P.A.R.D.
Short Circuit Current	V_{in} = 12.6 V, R_L = 0.1 Ω	250 mA
Efficiency	V_{in} = 12.6 V, I_O = 200 mA	72%

MOTOROLA

TL780 Series

Three-Terminal Positive Fixed Voltage Regulators

This family of precision fixed voltage regulators are monolithic integrated circuits capable of driving loads in excess of 1.5 A. Innovative design concepts, coupled with advanced thermal layout techniques have resulted in improved accuracy and excellent load, line and thermal regulation characteristics. Internal current limiting, thermal shutdown and safe–area compensation are employed, making these devices extremely rugged and virtually immune to overload.

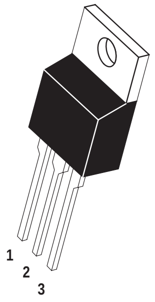
- ±1% Output Voltage Tolerance @ 25°C
- ±2% Output Voltage Tolerance over Full Operating Temperature Range
- Internal Short Circuit Current Limiting
- Internal Thermal Overload Protection
- Output Transistor Safe–Area Compensation
- No External Components Required
- Pinout Compatible with MC7800 Series

THREE–TERMINAL POSITIVE FIXED VOLTAGE REGULATORS

SEMICONDUCTOR TECHNICAL DATA

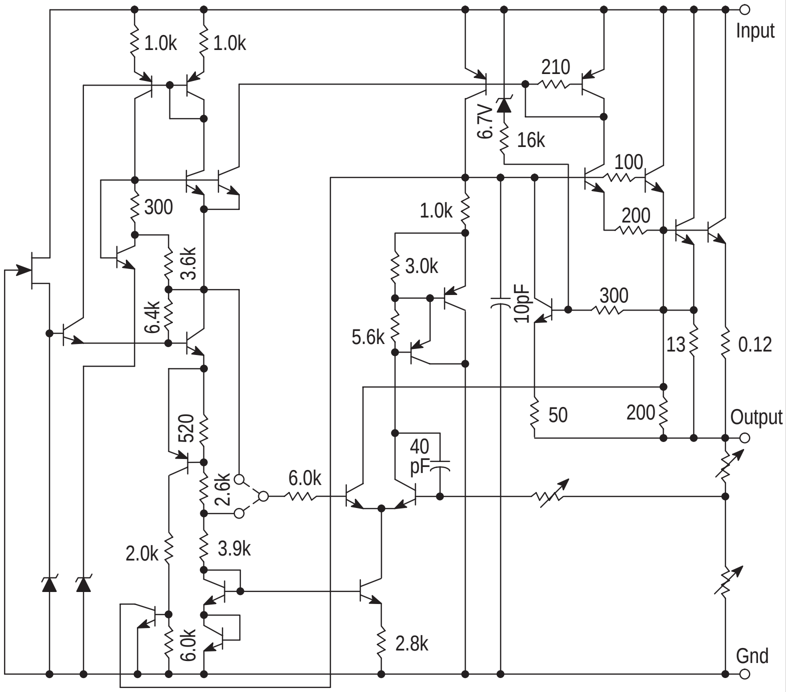
KC SUFFIX
PLASTIC PACKAGE
CASE 221A

Pin 1. Input
2. Ground
3. Output

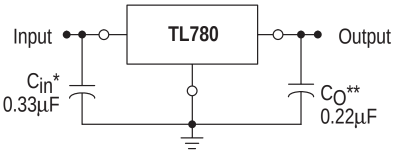


Heatsink surface is connected to Pin 2.

Representative Schematic Diagram



STANDARD APPLICATION



A common ground is required between the input and the output voltages. The input voltage must remain typically 2.0 V above the output voltage even during the low point on the input ripple voltage.

(XX), these two digits of the type number indicate voltage.

* C_{in} is required if regulator is located an appreciable distance from power supply filter.
** C_O is not needed for stability; however, it does improve transient response.

ORDERING INFORMATION

Nominal Output	Device	Operating Temperature Range
5.0 V	TL780–05CKC	T_J = 0° to 125°C
12 V	TL780–12CKC	
15 V	TL780–15CKC	

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage	V_{in}	35	Vdc
Power Dissipation and Thermal Characteristics			
T_A = +25°C	P_D	2.0	W
Derate above T_A = +25°C	$1/\theta_{JA}$	16	mW/°C
Thermal Resistance, Junction–to–Air	θ_{JA}	62.5	°C/W
T_A = +25°C	P_D	15	W
Derate above T_C = +75°C (See Figure 1)	$1/\theta_{JC}$	200	mW/°C
Thermal Resistance, Junction–to–Case	θ_{JC}	5.0	°C/W
Operating Junction Temperature Range	T_J	0 to +150	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{in} = 10 V, I_O = 500 mA, 0°C ≤ T_J ≤ +125°C, unless otherwise noted [Note 1].)

Characteristics	Symbol	TL780–05C			Unit
		Min	Typ	Max	
Output Voltage	V_O				V
5.0 mA ≤ I_O ≤ 1.0 A, P ≤ 15 W					
7.0 V ≤ V_{in} ≤ 20 V					
T_J = +25°C		4.95	5.0	5.05	
0°C ≤ T_J ≤ +125°C		4.90	—	5.10	
Line Regulation (T_J = +25°C)	Reg_{line}				mV
7.0 V ≤ V_{in} ≤ 25 V		—	0.5	5.0	
8.0 V ≤ V_{in} ≤ 12 V		—	0.5	5.0	
Load Regulation (T_J = +25°C)	Reg_{load}				mV
5.0 mA ≤ I_O ≤ 1.5 A		—	4.0	25	
250 mA ≤ I_O ≤ 750 mA		—	1.5	15	
Ripple Rejection	RR				dB
8.0 V ≤ V_{in} ≤ 18 V, f = 120 Hz		70	80	—	
Output Resistance (f = 1.0 kHz)	r_O	—	0.0035	—	W
Average Temperature Coefficient of Output Voltage	TCV_O				mV°C
I_O = 5.0 mA		—	0.06	—	
Output Noise Voltage (T_J = +25°C)	V_n				µV
10 Hz ≤ f ≤ 100 kHz		—	75	—	
Dropout Voltage (T_J = +25°C)	$V_{in}–V_O$				V
I_O = 1.0 mA		—	2.0	—	
Bias Current (T_J = +25°C)	I_B	—	3.5	8.0	mA
Bias Current Change	ΔI_B				mA
7.0 V ≤ V_{in} ≤ 25 V, I_O = 500 mA		—	0.7	1.3	
5.0 mA ≤ I_O ≤ 1.0 A, V_{in} ≤ 10 V		—	0.03	0.5	
Short Circuit Output Current (T_J = +25°C)	I_{SC}				mA
V_{in} = 35 V		—	200	—	
Peak Output Current (T_J = +25°C)	I_P	—	2.2	—	A

NOTE: 1. Line and load regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

ELECTRICAL CHARACTERISTICS (V_{in} = 19 V, I_O = 500 mA, 0°C ≤ T_J ≤ +125°C, unless otherwise noted [Note 1].)

Characteristics	Symbol	TL780–12C			Unit
		Min	Typ	Max	
Output Voltage	V_O				V
5.0 mA ≤ I_O ≤ 1.0 A, P ≤ 15 W, 14.5 ≤ V_{in} ≤ 27 V					
T_J = +25°C		11.88	12	12.12	
0°C ≤ T_J ≤ +125°C		11.76	—	12.24	
Line Regulation (T_J = +25°C)	Reg_{line}				mV
14.5 V ≤ V_{in} ≤ 30		—	1.2	12	
16 V ≤ V_{in} ≤ 22		—	1.2	12	

ELECTRICAL CHARACTERISTICS (V_{in} = 19 V, I_O = 500 mA, 0°C ≤ T_J ≤ +125°C, unless otherwise noted [Note 1].)

Characteristics	Symbol	TL780–12C			Unit
		Min	Typ	Max	
Load Regulation (T_J = +25°C)	Reg_{load}				mV
5.0 mA ≤ I_O ≤ 1.5 A		—	6.5	60	
250 mA ≤ I_O ≤ 750 mA		—	2.5	36	
Ripple Rejection	RR				dB
15 V ≤ V_{in} ≤ 25 V, f = 120 Hz		65	77	—	
Output Resistance (f = 1.0 kHz)	r_O	—	0.0035	—	W
Average Temperature Coefficient of Output Voltage	TCV_O				mV°C
I_O = 5.0 mA		—	0.15	—	
Output Noise Voltage (T_J = +25°C)	V_n				µV
10 Hz ≤ f ≤ 100 kHz		—	180	—	
Dropout Voltage (T_J = +25°C)	$V_{in}–V_O$				V
I_O = 1.0 mA		—	2.0	—	
Bias Current (T_J = +25°C)	I_B	—	3.5	8.0	mA
Bias Current Change	ΔI_B				mA
14.5 V ≤ V_{in} ≤ 30 V, I_O = 500 mA		—	0.4	1.3	
5.0 mA ≤ I_O ≤ 1.0 A, V_{in} ≤ 19 V		—	0.03	0.5	
Short Circuit Output Current (T_J = +25°C)	I_{SC}				mA
V_{in} = 35 V		—	200	—	
Peak Output Current (T_J = +25°C)	I_P	—	2.2	—	A

ELECTRICAL CHARACTERISTICS (V_{in} = 23 V, I_O = 500 mA, 0°C ≤ T_J ≤ +125°C, unless otherwise noted [Note 1].)

Characteristics	Symbol	TL780–15C			Unit
		Min	Typ	Max	
Output Voltage	V_O				V
5.0 mA ≤ I_O ≤ 1.0 A, P ≤ 15 W, 17.5 V ≤ V_{in} ≤ 30 V					
T_J = +25°C		14.85	15	15.15	
0°C ≤ T_J ≤ +125°C		14.70	—	15.30	
Line Regulation (T_J = +25°C)	Reg_{line}				mV
17.5 V ≤ V_{in} ≤ 30 V		—	1.5	15	
20 V ≤ V_{in} ≤ 26 V		—	1.5	15	
Load Regulation (T_J = +25°C)	Reg_{load}				mV
5.0 mA ≤ I_O ≤ 1.5 A		—	7.0	75	
250 mA ≤ I_O ≤ 750 mA		—	2.5	45	
Ripple Rejection	RR				dB
18.5 V ≤ V_{in} ≤ 28.5 V, f = 120 Hz		60	75	—	
Output Resistance (f = 1.0 kHz)	r_O	—	0.0035	—	W
Average Temperature Coefficient of Output Voltage	TCV_O				mV°C
I_O = 5.0 mA		—	0.18	—	
Output Noise Voltage (T_J = +25°C)	V_n				µV
10 Hz ≤ f ≤ 100 kHz		—	225	—	
Dropout Voltage (T_J = +25°C)	$V_{in}–V_O$				V
I_O = 1.0 A		—	2.0	—	
Bias Current (T_J = +25°C)	I_B	—	3.6	8.0	mA
Bias Current Change	ΔI_B				mA
17.5 V ≤ V_{in} ≤ 30 V, I_O = 500 mA		—	0.4	1.3	
5.0 mA ≤ I_O ≤ 1.0 A, V_{in} ≤ 23 V		—	0.02	0.5	
Short Circuit Output Current (T_J = +25°C)	I_{SC}				mA
V_{in} = 35 V		—	200	—	
Peak Output Current (T_J = +25°C)	I_P	—	2.2	—	A

NOTE: 1. Line and load regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

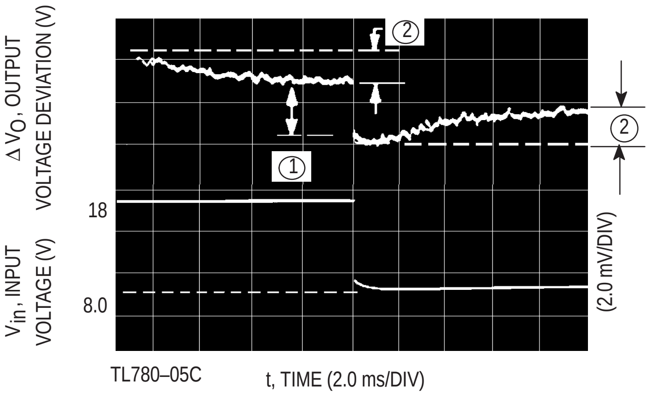
VOLTAGE REGULATOR PERFORMANCE

The performance of a voltage regulator is specified by its immunity to changes in load, input voltage, power dissipation, and temperature. Line and load regulation are tested with a pulse of short duration (< 100 µs) and are strictly a function of electrical gain. However, pulse widths of longer duration (> 1.0 ms) are sufficient to affect temperature gradients across the die. These temperature gradients can cause a change in the output voltage, in addition to changes by line and load regulation. Longer pulse widths and thermal gradients make it desirable to specify thermal regulation.

Thermal regulation is defined as the change in output voltage caused by a change in dissipated power for a specified time, and is expressed as a percentage output voltage change per watt. The change in dissipated power can be caused by a change in either the input voltage or the load current. Thermal regulation is a function of IC layout and die attach techniques, and usually occurs within 10 ms of a change in power dissipation. After 10 ms, additional changes in the output voltage are due to the temperature coefficient of the device.

Figure 1 shows the line and thermal regulation response of a typical TL780–05C to a 10 W input pulse. The variation of the output voltage due to line regulation is labeled ① and the thermal regulation component is labeled ②. Figure 2 shows the load and thermal regulation response of a typical TL780–05C to a 15 W load pulse. The output voltage variation due to load regulation is labeled ① and the thermal regulation component is labeled ②.

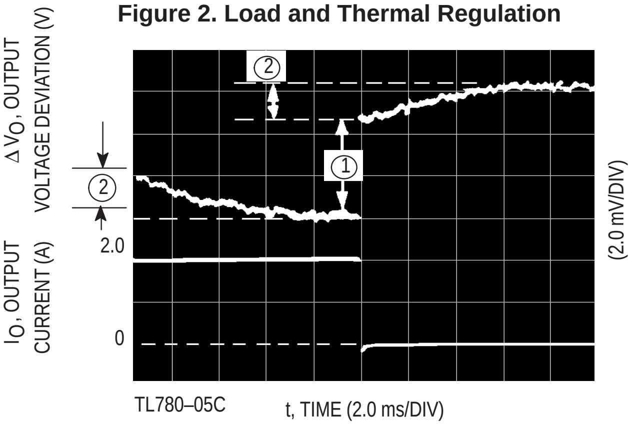
Figure 1. Line and Thermal Regulation



V_{out} = 5.0 V
V_{in} = 8.0 V → 18 V → 8.0 V
I_{out} = 1.0 A

① = Reg_{line} = 2.4 mV
② = Reg_{therm} = 0.0030% V_O/W

Figure 2. Load and Thermal Regulation



V_{out} = 5.0 V
V_{in} = 15 V
I_{out} = 0 A → 1.5 A → 0 A

① = Reg_{line} = 4.4 mV
② = Reg_{therm} = 0.0020% V_O/W

Figure 3. Temperature Stability

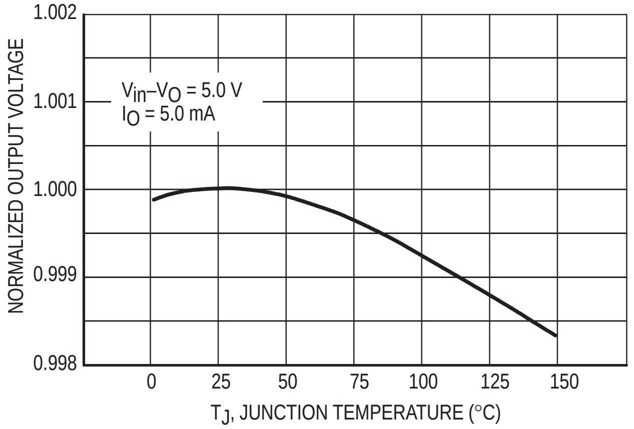


Figure 4. Output Impedance

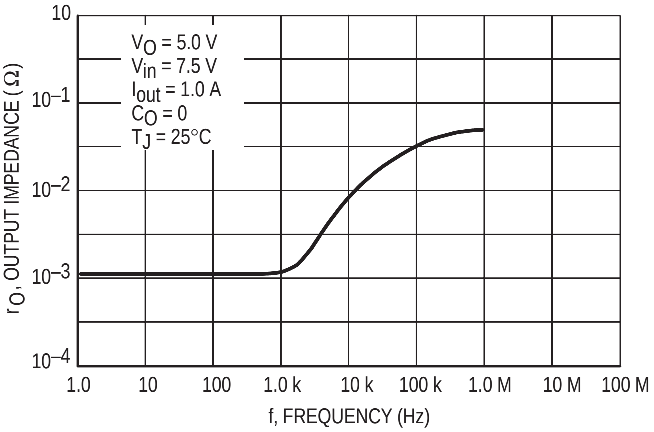


Figure 5. Ripple Rejection versus Frequency

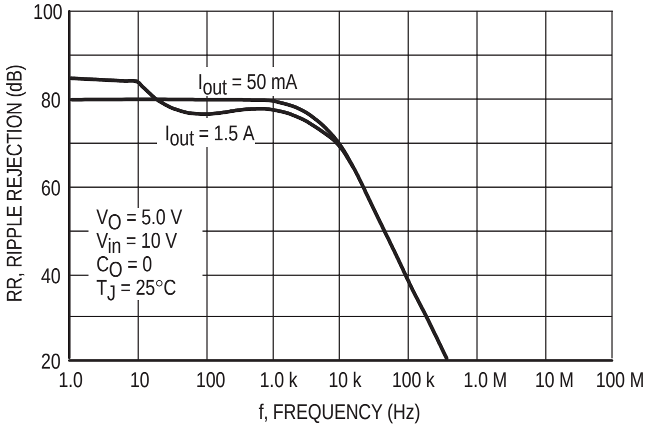


Figure 6. Ripple Rejection versus Output Current

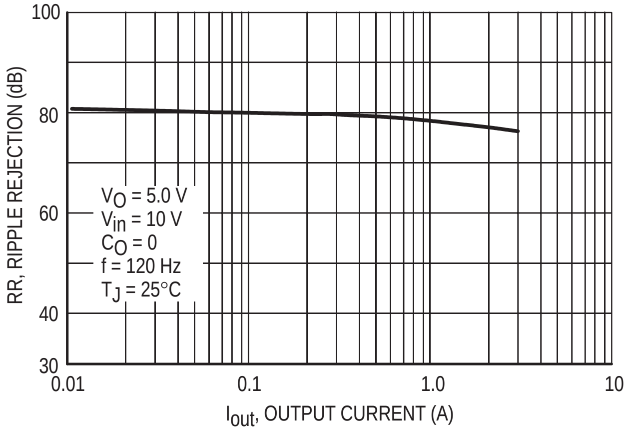


Figure 7. Bias Current versus Input Voltage

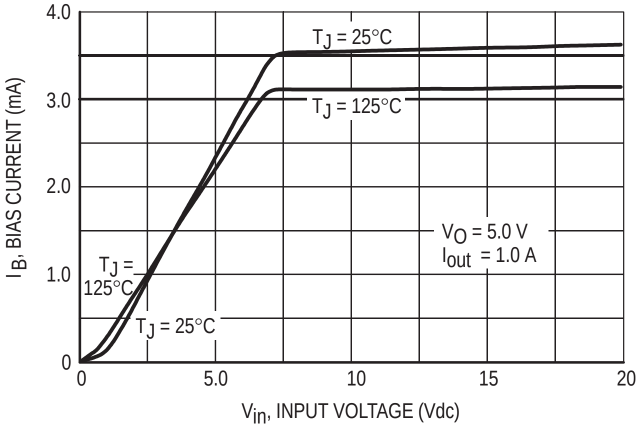


Figure 8. Bias Current versus Output Current

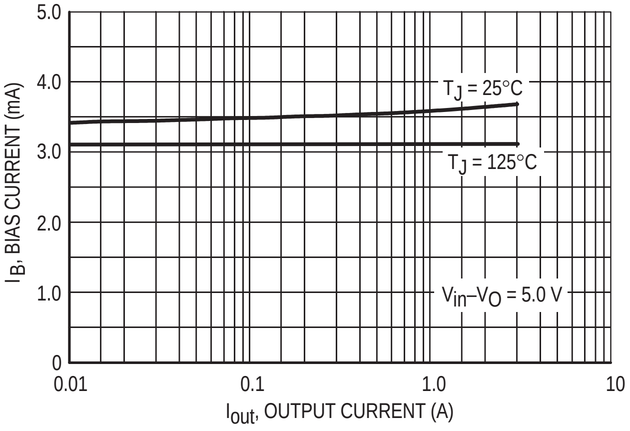


Figure 9. Dropout Voltage

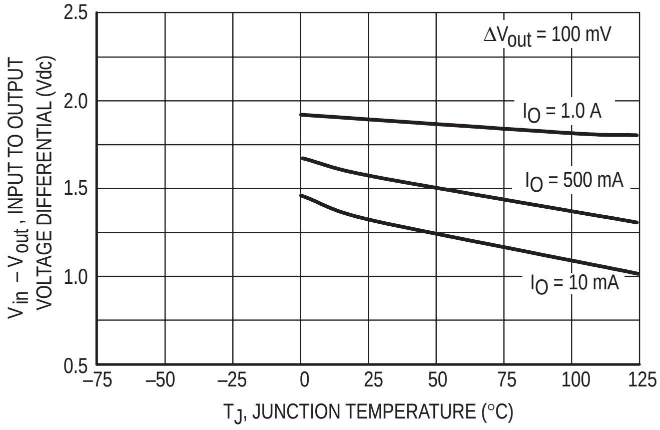
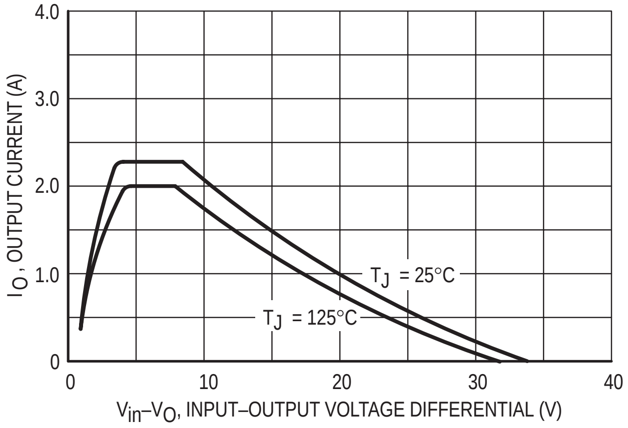


Figure 10. Peak Output Current



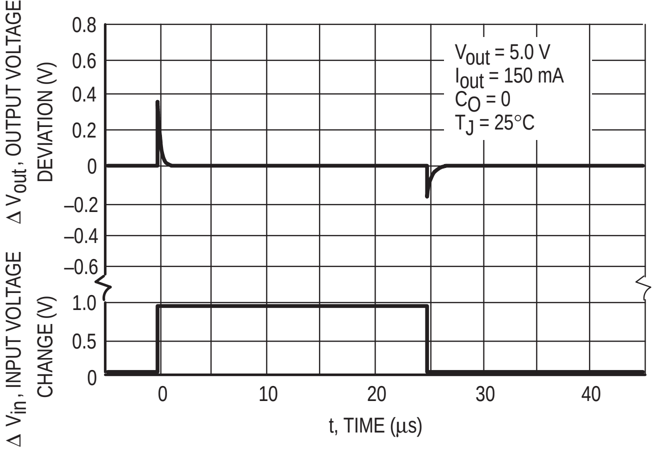


Figure 11. Line Transient Response

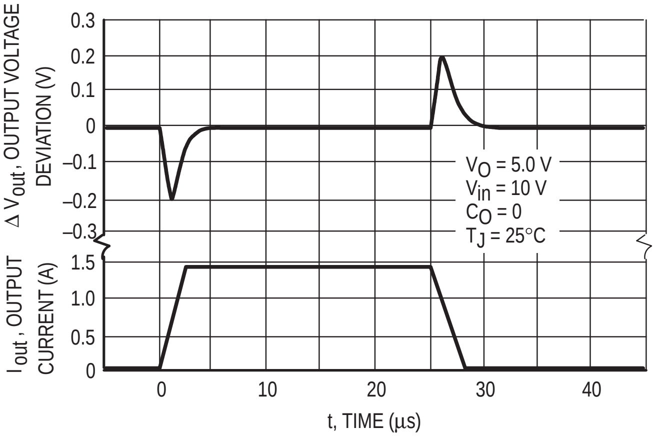


Figure 12. Load Transient Response

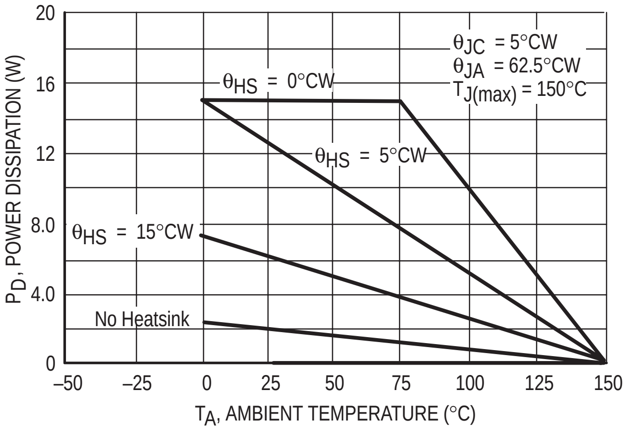


Figure 13. Worst Case Power Dissipation versus Ambient Temperature

UC3842A, 43A
UC2842A, 43A

High Performance Current Mode Controllers

The UC3842A, UC3843A series of high performance fixed frequency current mode controllers are specifically designed for off–line and dc–to–dc converter applications offering the designer a cost effective solution with minimal external components. These integrated circuits feature a trimmed oscillator for precise duty cycle control, a temperature compensated reference, high gain error amplifier, current sensing comparator, and a high current totem pole output ideally suited for driving a power MOSFET.

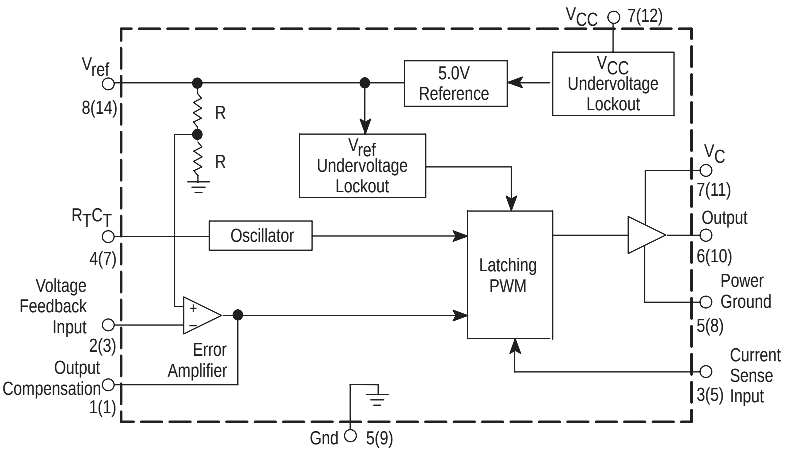
Also included are protective features consisting of input and reference undervoltage lockouts each with hysteresis, cycle–by–cycle current limiting, programmable output deadtime, and a latch for single pulse metering.

These devices are available in an 8–pin dual–in–line plastic package as well as the 14–pin plastic surface mount (SO–14). The SO–14 package has separate power and ground pins for the totem pole output stage.

The UCX842A has UYLO thresholds of 16 V (on) and 10 V (off), ideally suited for off–line converters. The UCX843A is tailored for lower voltage applications having UVLO thresholds of 8.5 V (on) and 7.6 V (off).

- Trimmed Oscillator Discharge Current for Precise Duty Cycle Control
- Current Mode Operation to 500 kHz
- Automatic Feed Forward Compensation
- Latching PWM for Cycle–By–Cycle Current Limiting
- Internally Trimmed Reference with Undervoltage Lockout
- High Current Totem Pole Output
- Undervoltage Lockout with Hysteresis
- Low Startup and Operating Current
- Direct Interface with Motorola SENSEFET Products

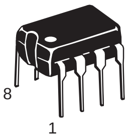
Simplified Block Diagram



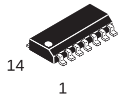
Pin numbers in parenthesis are for the D suffix SO–14 package.

HIGH PERFORMANCE CURRENT MODE CONTROLLERS

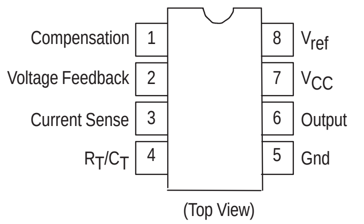
N SUFFIX
PLASTIC PACKAGE
CASE 626

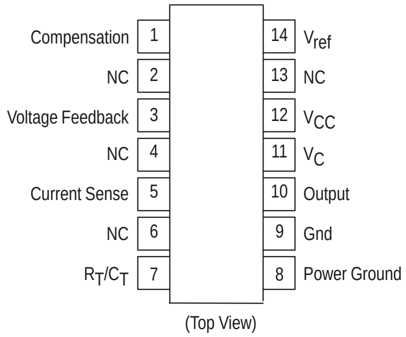


D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO–14)



PIN CONNECTIONS





ORDERING INFORMATION

Device	Operating Temperature Range	Package
UC3842AD	T_A = 0° to +70°C	SO–14
UC3843AD		SO–14
UC3842AN		Plastic
UC3843AN		Plastic
UC2842AD	T_A = – 25° to +85°C	SO–14
UC2843AD		SO–14
UC2842AN		Plastic
UC2843AN		Plastic

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Total Power Supply and Zener Current	$(I_{CC} + I_Z)$	30	mA
Output Current, Source or Sink (Note 1)	I_O	1.0	A
Output Energy (Capacitive Load per Cycle)	W	5.0	µJ
Current Sense and Voltage Feedback Inputs	V_{in}	– 0.3 to + 5.5	V
Error Amp Output Sink Current	I_O	10	mA
Power Dissipation and Thermal Characteristics D Suffix, Plastic Package Maximum Power Dissipation @ T_A = 25°C Thermal Resistance, Junction–to–Air N Suffix, Plastic Package Maximum Power Dissipation @ T_A = 25°C Thermal Resistance, Junction–to–Air	 P_D $R_{\theta JA}$ P_D $R_{\theta JA}$	 862 145 1.25 100	 mW °C/W W °C/W
Operating Junction Temperature	T_J	+ 150	°C
Operating Ambient Temperature UC3842A, UC3843A UC2842A, UC2843A	T_A	 0 to + 70 – 25 to + 85	°C
Storage Temperature Range	T_{stg}	– 65 to + 150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V, [Note 2], R_T = 10 k, C_T = 3.3 nF, $T_A = T_{low}$ to T_{high} [Note 3], unless otherwise noted.)

Characteristics	Symbol	UC284XA			UC384XA			Unit
		Min	Typ	Max	Min	Typ	Max	
REFERENCE SECTION								
Reference Output Voltage (I_O = 1.0 mA, T_J = 25°C)	V_{ref}	4.95	5.0	5.05	4.9	5.0	5.1	V
Line Regulation (V_{CC} = 12 V to 25 V)	Reg_{line}	–	2.0	20	–	2.0	20	mV
Load Regulation (I_O = 1.0 mA to 20 mA)	Reg_{load}	–	3.0	25	–	3.0	25	mV
Temperature Stability	T_S	–	0.2	–	–	0.2	–	mV/°C
Total Output Variation over Line, Load, Temperature	V_{ref}	4.9	–	5.1	4.82	–	5.18	V
Output Noise Voltage (f = 10 Hz to 10 kHz, T_J = 25°C)	V_n	–	50	–	–	50	–	µV
Long Term Stability (T_A = 125°C for 1000 Hours)	S	–	5.0	–	–	5.0	–	mV
Output Short Circuit Current	I_{SC}	– 30	– 85	– 180	– 30	– 85	– 180	mA
OSCILLATOR SECTION								
Frequency T_J = 25°C $T_A = T_{low}$ to T_{high}	f_{osc}	 47 46	 52 –	 57 60	 47 46	 52 –	 57 60	kHz
Frequency Change with Voltage (V_{CC} = 12 V to 25 V)	$\Delta f_{osc}/\Delta V$	–	0.2	1.0	–	0.2	1.0	%
Frequency Change with Temperature $T_A = T_{low}$ to T_{high}	$\Delta f_{osc}/\Delta T$	–	5.0	–	–	5.0	–	%
Oscillator Voltage Swing (Peak–to–Peak)	V_{osc}	–	1.6	–	–	1.6	–	V
Discharge Current (V_{osc} = 2.0 V) T_J = 25°C $T_A = T_{low}$ to T_{high}	I_{dischg}	 7.5 7.2	 8.4 –	 9.3 9.5	 7.5 7.2	 8.4 –	 9.3 9.5	mA

NOTES: 1. Maximum Package power dissipation limits must be observed.
2. Adjust V_{CC} above the Startup threshold before setting to 15 V.
3. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible
T_{low} = 0°C for UC3842A, UC3843A T_{high} = +70°C for UC3842A, UC3843A
–25°C for UC2842A, UC2843A +85°C for UC2842A, UC2843A

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V, [Note 2], R_T = 10 k, C_T = 3.3 nF, T_A = T_{low} to T_{high} [Note 3], unless otherwise noted.)

Characteristics	Symbol	UC284XA			UC384XA			Unit
		Min	Typ	Max	Min	Typ	Max	
ERROR AMPLIFIER SECTION								
Voltage Feedback Input (V_O = 2.5 V)	V_{FB}	2.45	2.5	2.55	2.42	2.5	2.58	V
Input Bias Current (V_{FB} = 2.7 V)	I_{IB}	–	–0.1	–1.0	–	–0.1	–2.0	µA
Open Loop Voltage Gain (V_O = 2.0 V to 4.0 V)	A_{VOL}	65	90	–	65	90	–	dB
Unity Gain Bandwidth (T_J = 25°C)	BW	0.7	1.0	–	0.7	1.0	–	MHz
Power Supply Rejection Ratio (V_{CC} = 12 V to 25 V)	PSRR	60	70	–	60	70	–	dB
Output Current								mA
Sink (V_O = 1.1 V, V_{FB} = 2.7 V)	I_{Sink}	2.0	12	–	2.0	12	–	
Source (V_O = 5.0 V, V_{FB} = 2.3 V)	I_{Source}	–0.5	–1.0	–	–0.5	–1.0	–	
Output Voltage Swing								V
High State (R_L = 15 k to ground, V_{FB} = 2.3 V)	V_{OH}	5.0	6.2	–	5.0	6.2	–	
Low State (R_L = 15 k to V_{ref}, V_{FB} = 2.7 V)	V_{OL}	–	0.8	1.1	–	0.8	1.1	
CURRENT SENSE SECTION								
Current Sense Input Voltage Gain (Notes 4 & 5)	A_V	2.85	3.0	3.15	2.85	3.0	3.15	V/V
Maximum Current Sense Input Threshold (Note 4)	V_{th}	0.9	1.0	1.1	0.9	1.0	1.1	V
Power Supply Rejection Ratio V_{CC} = 12 to 25 V (Note 4)	PSRR	–	70	–	–	70	–	dB
Input Bias Current	I_{IB}	–	–2.0	–10	–	–2.0	–10	µA
Propagation Delay (Current Sense Input to Output)	$t_{PLH(in/out)}$	–	150	300	–	150	300	ns
OUTPUT SECTION								
Output Voltage								V
Low State (I_{Sink} = 20 mA)	V_{OL}	–	0.1	0.4	–	0.1	0.4	
(I_{Sink} = 200 mA)		–	1.6	2.2	–	1.6	2.2	
High State (I_{Sink} = 20 mA)	V_{OH}	13	13.5	–	13	13.5	–	
(I_{Sink} = 200 mA)		12	13.4	–	12	13.4	–	
Output Voltage with UVLO Activated V_{CC} = 6.0 V, I_{Sink} = 1.0 mA	$V_{OL(UVLO)}$	–	0.1	1.1	–	0.1	1.1	V
Output Voltage Rise Time (C_L = 1.0 nF, T_J = 25°C)	t_r	–	50	150	–	50	150	ns
Output Voltage Fall Time (C_L = 1.0 nF, T_J = 25°C)	t_f	–	50	150	–	50	150	ns
UNDERVOLTAGE LOCKOUT SECTION								
Startup Threshold	V_{th}							V
UCX842A		15	16	17	14.5	16	17.5	
UCX843A		7.8	8.4	9.0	7.8	8.4	9.0	
Minimum Operating Voltage After Turn–On	$V_{CC(min)}$							V
UCX842A		9.0	10	11	8.5	10	11.5	
UCX843A		7.0	7.6	8.2	7.0	7.6	8.2	
PWM SECTION								
Duty Cycle								%
Maximum	DC_{max}	94	96	–	94	96	–	
Minimum	DC_{min}	–	–	0	–	–	0	
TOTAL DEVICE								
Power Supply Current (Note 2)	I_{CC}							mA
Startup: (V_{CC} = 6.5 V for UCX843A,		–	0.5	1.0	–	0.5	1.0	
14 V for UCX842A) Operating		–	12	17	–	12	17	
Power Supply Zener Voltage (I_{CC} = 25 mA)	V_Z	30	36	–	30	36	–	V

NOTES: 2. Adjust V_{CC} above the Startup threshold before setting to 15 V.

3. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible

T_{low} = 0°C for UC3842A, UC3843A T_{high} = +70°C for UC3842A, UC3843A

–25°C for UC2842A, UC2843A +85°C for UC2842A, UC2843A

4. This parameter is measured at the latch trip point with V_{FB} = 0 V.

5. Comparator gain is defined as: $A_V \frac{\Delta V \text{ Output Compensation}}{\Delta V \text{ Current Sense Input}}$

Figure 1. Timing Resistor versus Oscillator Frequency

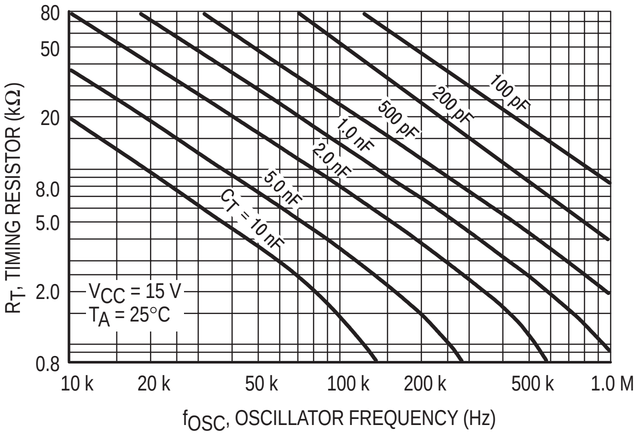


Figure 2. Output Deadtime versus Oscillator Frequency

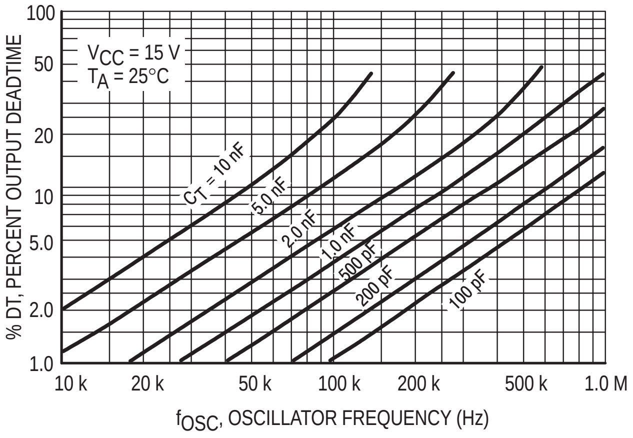


Figure 3. Oscillator Discharge Current versus Temperature

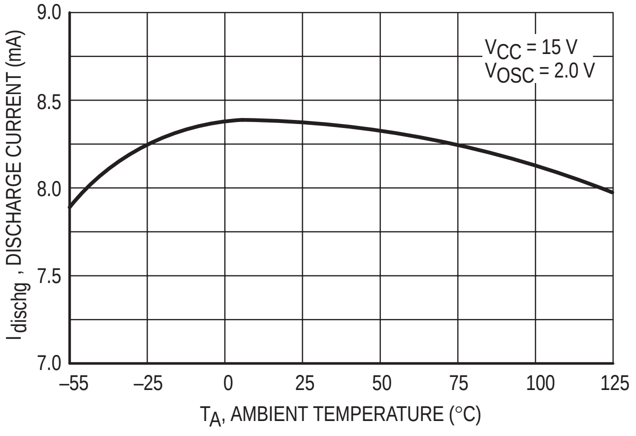


Figure 4. Maximum Output Duty Cycle versus Timing Resistor

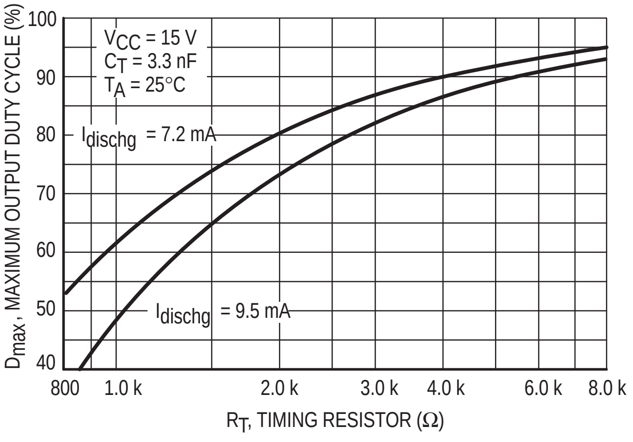


Figure 5. Error Amp Small Signal Transient Response

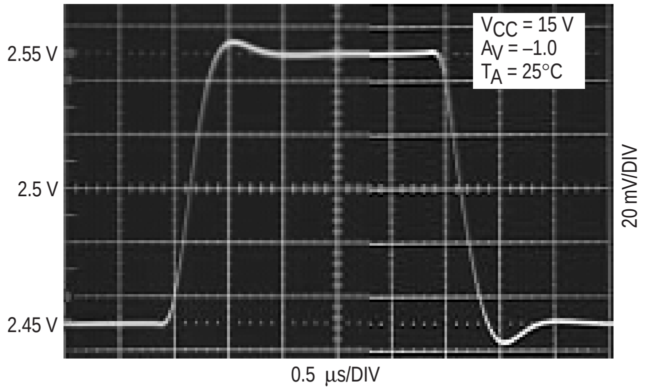


Figure 6. Error Amp Large Signal Transient Response

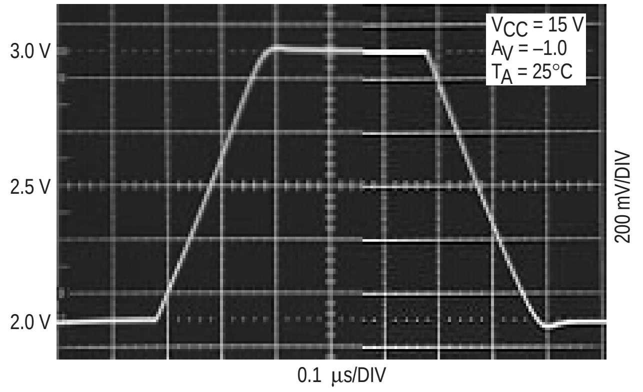


Figure 7. Error Amp Open Loop Gain and Phase versus Frequency

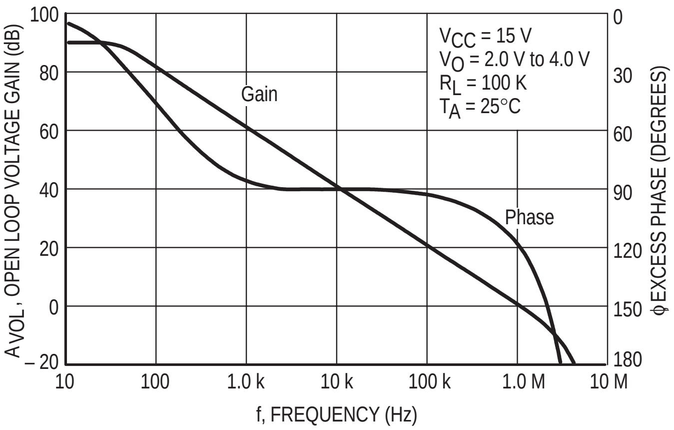


Figure 8. Current Sense Input Threshold versus Error Amp Output Voltage

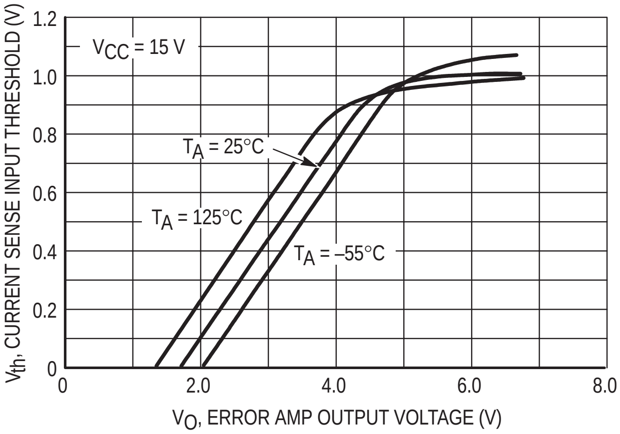


Figure 9. Reference Voltage Change versus Source Current

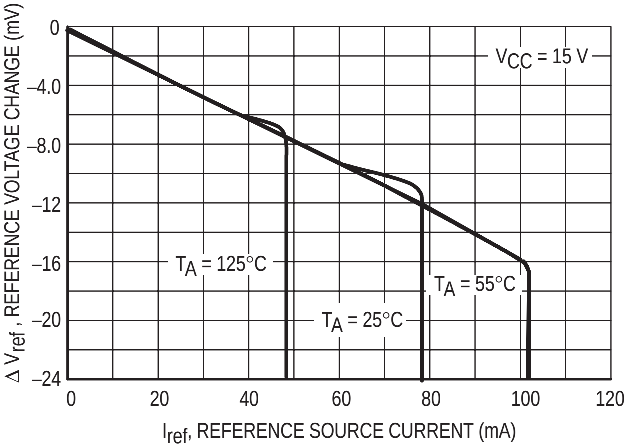


Figure 10. Reference Short Circuit Current versus Temperature

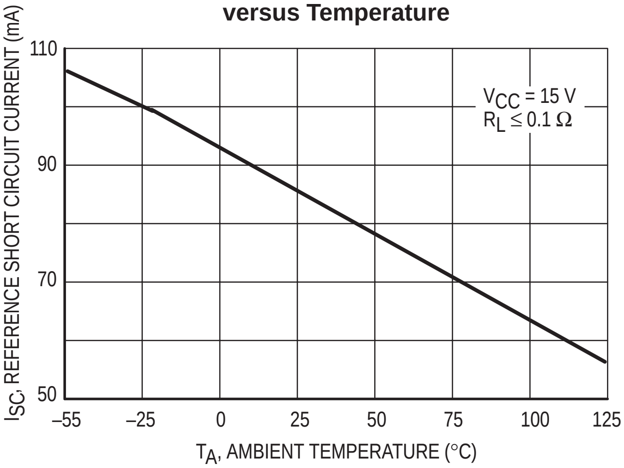


Figure 11. Reference Load Regulation

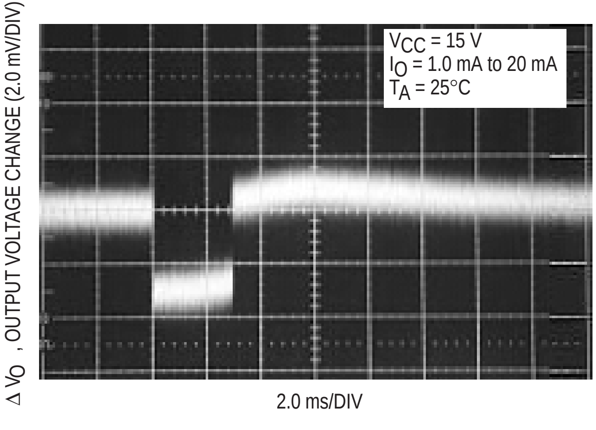


Figure 12. Reference Line Regulation

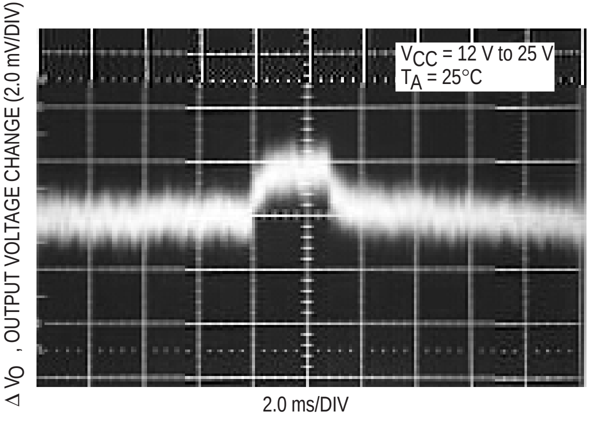


Figure 13. Output Saturation Voltage versus Load Current

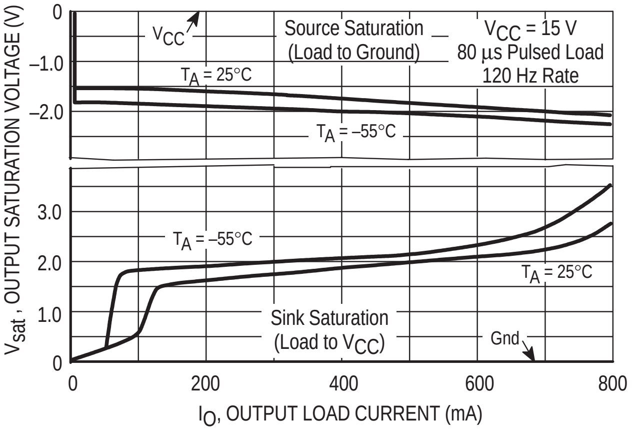


Figure 14. Output Waveform

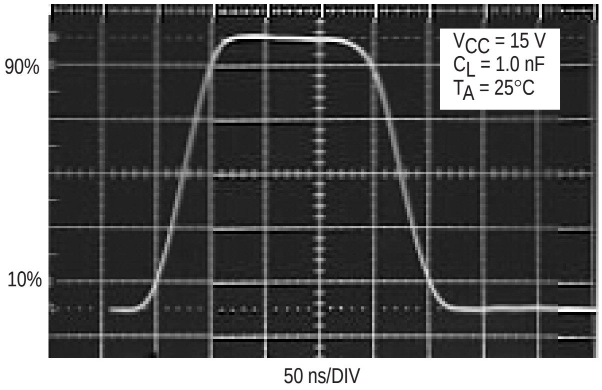


Figure 15. Output Cross Conduction

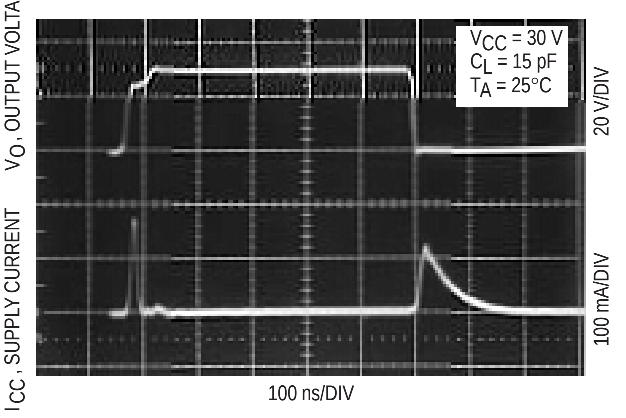


Figure 16. Supply Current versus Supply Voltatage

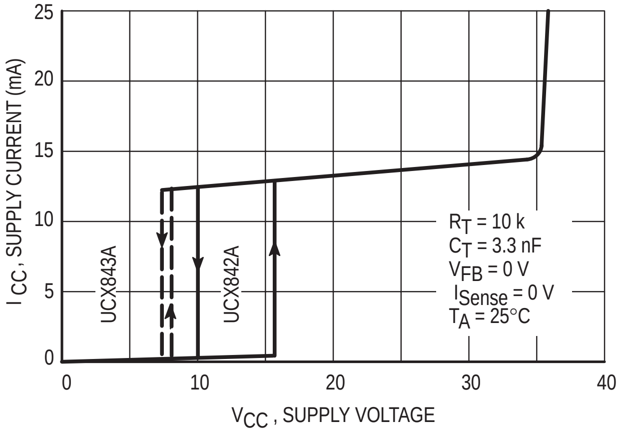
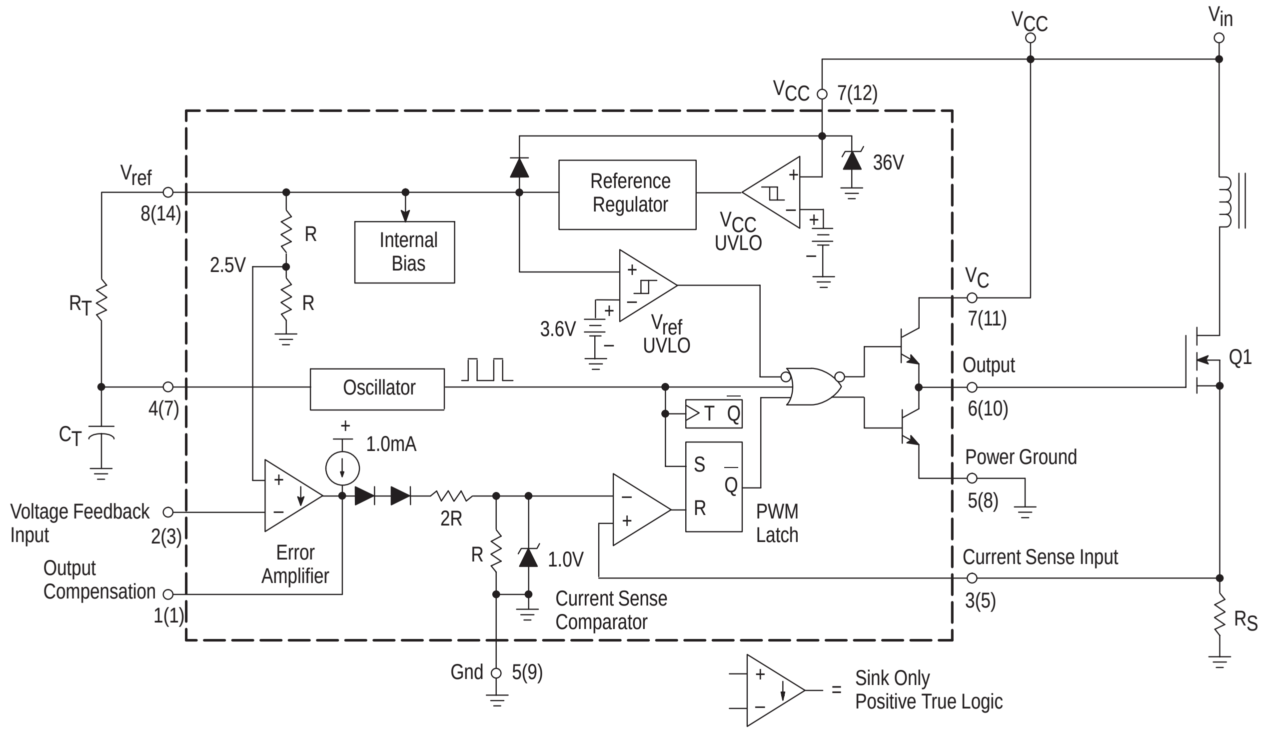
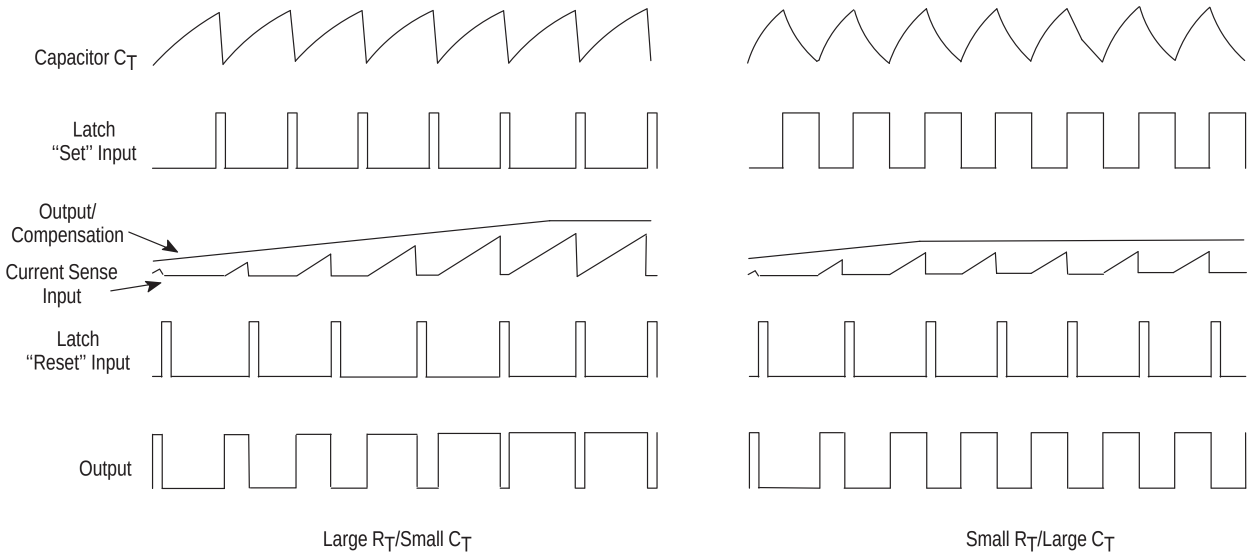


Figure 17. Representative Block Diagram



Pin numbers in parenthesis are for the D suffix SO–14 package.

Figure 18. Timing Diagram



OPERATING DESCRIPTION

The UC3842A, UC3843A series are high performance, fixed frequency, current mode controllers. They are specifically designed for Off–Line and dc–to–dc converter applications offering the designer a cost effective solution with minimal external components. A representative block diagram is shown in Figure 17.

Oscillator

The oscillator frequency is programmed by the values selected for the timing components R_T and C_T. Capacitor C_T is charged from the 5.0 V reference through resistor R_T to approximately 2.8 V and discharged to 1.2 V by an internal current sink. During the discharge of C_T, the oscillator generates and internal blanking pulse that holds the center input of the NOR gate high. This causes the Output to be in a low state, thus producing a controlled amount of output deadtime. Figure 1 shows R_T versus Oscillator Frequency and Figure 2, Output Deadtime versus Frequency, both for given values of C_T. Note that many values of R_T and C_T will give the same oscillator frequency but only one combination will yield a specific output deadtime at a given frequency. The oscillator thresholds are temperature compensated, and the discharge current is trimmed and guaranteed to within ± 10% at T_J = 25°C. These internal circuit refinements minimize variations of oscillator frequency and maximum output duty cycle. The results are shown in Figures 3 and 4.

In many noise sensitive applications it may be desirable to frequency–lock the converter to an external system clock. This can be accomplished by applying a clock signal to the circuit shown in Figure 20. For reliable locking, the free–running oscillator frequency should be set about 10% less than the clock frequency. A method for multi unit synchronization is shown in Figure 21. By tailoring the clock waveform, accurate Output duty cycle clamping can be achieved.

Error Amplifier

A fully compensated Error Amplifier with access to the inverting input and output is provided. It features a typical dc voltage gain of 90 dB, and a unity gain bandwidth of 1.0 MHz with 57 degrees of phase margin (Figure 7). The noninverting input is internally biased at 2.5 V and is not pinned out. The converter output voltage is typically divided down and monitored by the inverting input. The maximum input bias current is –2.0 µA which can cause an output voltage error that is equal to the product of the input bias current and the equivalent input divider source resistance.

The Error Amp Output (Pin 1) is provide for external loop compensation (Figure 30). The output voltage is offset by two diode drops (≈ 1.4 V) and divided by three before it connects to the inverting input of the Current Sense Comparator. This guarantees that no drive pulses appear at the Output (Pin 6) when Pin 1 is at its lowest state (V_{OL}). This occurs when the power supply is operating and the load is removed, or at the beginning of a soft–start interval (Figures 23, 24). The Error Amp minimum feedback resistance is limited by the amplifier's source current (0.5 mA) and the required output voltage (V_{OH}) to reach the comparator's 1.0 V clamp level:

$$R_{f(min)} \approx \frac{3.0\ (1.0\ V) + 1.4\ V}{0.5\ mA} = 8800\ \Omega$$

Current Sense Comparator and PWM Latch

The UC3842A, UC3843A operate as a current mode controller, whereby output switch conduction is initiated by the oscillator and terminated when the peak inductor current reaches the threshold level established by the Error Amplifier Output/Compensation (Pin1). Thus the error signal controls the peak inductor current on a cycle–by–cycle basis. The current Sense Comparator PWM Latch configuration used ensures that only a single pulse appears at the Output during any given oscillator cycle. The inductor current is converted to a voltage by inserting the ground referenced sense resistor R_S in series with the source of output switch Q1. This voltage is monitored by the Current Sense Input (Pin 3) and compared a level derived from the Error Amp Output. The peak inductor current under normal operating conditions is controlled by the voltage at pin 1 where:

$$I_{pk} = \frac{V_{(Pin\ 1)} - 1.4\ V}{3\ R_S}$$

Abnormal operating conditions occur when the power supply output is overloaded or if output voltage sensing is lost. Under these conditions, the Current Sense Comparator threshold will be internally clamped to 1.0 V. Therefore the maximum peak switch current is:

$$I_{pk(max)} = \frac{1.0\ V}{R_S}$$

When designing a high power switching regulator it becomes desirable to reduce the internal clamp voltage in order to keep the power dissipation of R_S to a reasonable level. A simple method to adjust this voltage is shown in Figure 22. The two external diodes are used to compensate the internal diodes yielding a constant clamp voltage over temperature. Erratic operation due to noise pickup can result if there is an excessive reduction of the $I_{pk(max)}$ clamp voltage.

A narrow spike on the leading edge of the current waveform can usually be observed and may cause the power supply to exhibit an instability when the output is lightly loaded. This spike is due to the power transformer interwinding capacitance and output rectifier recovery time. The addition of an RC filter on the Current Sense Input with a time constant that approximates the spike duration will usually eliminate the instability; refer to Figure 26.

PIN FUNCTION DESCRIPTION

Pin		Function	Description
8–Pin	14–Pin		
1	1	Compensation	This pin is Error Amplifier output and is made available for loop compensation.
2	3	Voltage Feedback	This is the inverting input of the Error Amplifier. It is normally connected to the switching power supply output through a resistor divider.
3	5	Current Sense	A voltage proportional to inductor current is connected to this input. The PWM uses this information to terminate the output switch conduction.
4	7	R_T/C_T	The Oscillator frequency and maximum Output duty cycle are programmed by connecting resistor R_T to V_{ref} and capacitor C_T to ground. Operation to 500 kHz is possible.
5	–	Gnd	This pin is the combined control circuitry and power ground (8–pin package only).
6	10	Output	This output directly drives the gate of a power MOSFET. Peak currents up to 1.0 A are sourced and sunk by this pin.
7	12	V_{CC}	This pin is the positive supply of the control IC.
8	14	V_{ref}	This is the reference output. It provides charging current for capacitor C_T through resistor R_T.
–	8	Power Ground	This pin is a separate power ground return (14–pin package only) that is connected back to the power source. It is used to reduce the effects of switching transient noise on the control circuitry.
–	11	V_C	The Output high state (V_{OH}) is set by the voltage applied to this pin (14–pin package only). With a separate power source connection, it can reduce the effects of switching transient noise on the control circuitry.
–	9	Gnd	This pin is the control circuitry ground return (14–pin package only) and is connected back to the power source ground.
–	2,4,6,13	NC	No connection (14–pin package only). These pins are not internally connected.

Undervoltage Lockout

Two undervoltage lockout comparators have been incorporated to guarantee that the IC is fully functional before the output stage is enabled. The positive power supply terminal (V_{CC}) and the reference output (V_{ref}) are each monitored by separate comparators. Each has built–in hysteresis to prevent erratic output behavior as their respective thresholds are crossed. The V_{CC} comparator upper and lower thresholds are 16 V/10 V for the UCX842A, and 8.4 V/7.6 V for the UCX843A. The V_{ref} comparator upper and lower thresholds are 3.6V/3.4 V. The large hysteresis and low startup current of the UCX842A makes it ideally suited in off–line converter applications where efficient bootstrap startup techniques are required (Figure 33). The UCX843A is intended for lower voltage dc to dc converter applications. A 36 V zener is connected as a shunt regulator form V_{CC} to ground. Its purpose is to protect the IC from excessive voltage that can occur during system startup. The minimum operating voltage for the UCX842A is 11 V and 8.2 V for the UCX843A.

Output

These devices contain a single totem pole output stage that was specifically designed for direct drive of power MOSFETs. It is capable of up to ±1.0 A peak drive current and has a typical rise and fall time of 50 ns with a 1.0 nF load. Additional internal circuitry has been added to keep the Output in a sinking mode whenever an undervoltage lockout is active. This characteristic eliminates the need for an external pull–down resistor.

The SO–14 surface mount package provides separate pins for V_C (output supply) and Power Ground. Proper implementation will significantly reduce the level of switching transient noise imposed on the control circuitry. This becomes particularly useful when reducing the $I_{pk(max)}$ clamp level. The separate V_C supply input allows the designer added flexibility in tailoring the drive voltage independent of V_{CC}. A zener clamp is typically connected to this input when driving power MOSFETs in systems where V_{CC} is greater that 20 V. Figure 25 shows proper power and control ground connections in a current sensing power MOSFET application.

Reference

The 5.0 V bandgap reference is trimmed to ±1.0% tolerance at T_J = 25°C on the UC284XA, and ± 2.0% on the UC384XA. Its primary purpose is to supply charging current to the oscillator timing capacitor. The reference has short circuit protection and is capable of providing in excess of 20 mA for powering additional control system circuitry.

DESIGN CONSIDERATIONS

Do not attempt to construct the converter on wire–wrap or plug–in prototype boards. High Frequency circuit layout techniques are imperative to prevent pulsewidth jitter. This is usually caused by excessive noise pick–up imposed on the Current Sense or Voltage Feedback inputs. Noise immunity can be improved by lowering circuit impedances at these points. The printed circuit layout should contain a ground plane with low–current signal and high–current switch and output grounds returning on separate paths back to the input filter capacitor. Ceramic bypass capacitors (0.1 μF) connected directly to V_{CC}, V_C, and V_{ref} may be required depending upon circuit layout. This provides a low impedance path for filtering the high frequency noise. All high current loops should be kept as short as possible using heavy copper runs to minimize radiated EMI. The Error Amp compensation circuitry and the converter output voltage divider should be located close to the IC and as far as possible from the power switch and other noise generating components.

Current mode converters can exhibit subharmonic oscillations when operating at a duty cycle greater than 50% with continuous inductor current. This instability is independent of the regulators closed–loop characteristics and is caused by the simultaneous operating conditions of fixed frequency and peak current detecting. Figure 19A shows the phenomenon graphically. At t_0, switch conduction begins, causing the inductor current to rise at a slope of m_1. This slope is a function of the input voltage divided by the inductance. At t_1, the Current Sense Input reaches the threshold established by the control voltage. This causes the switch to turn off and the current to decay at a slope of m_2 until the next oscillator cycle. The unstable condition can be shown if a pertubation is added to the control voltage, resulting in a small ΔI (dashed line). With a fixed oscillator period, the current decay time is reduced, and the minimum current at switch turn–on (t_2) is increased by ΔI + ΔI m2/m1. The minimum current at the next cycle (t_3) decreases to $(\Delta I + \Delta I\, m_2/m_1)\,(m_2/m_1)$. This pertubation is multiplied by $m_2.m_1$ on each succeeding cycle, alternately increasing and decreasing the inductor current at switch turn–on. Several oscillator cycles may be required before the inductor current reaches zero causing the process to commence again. If m_2/m_1 is greater than 1, the converter will be unstable. Figure 19B shows that by adding an artificial ramp that is synchronized with the PWM clock to the control voltage, the ΔI pertubation will decrease to zero on succeeding cycles. This compensation ramp (m_3) must have a slope equal to or slightly greater than $m_2/2$ for stability. With $m_2/2$ slope compensation, the average inductor current follows the control voltage yielding true current mode operation. The compensating ramp can be derived from the oscillator and added to either the Voltage Feedback or Current Sense inputs (Figure 32).

Figure 19. Continuous Current Waveforms

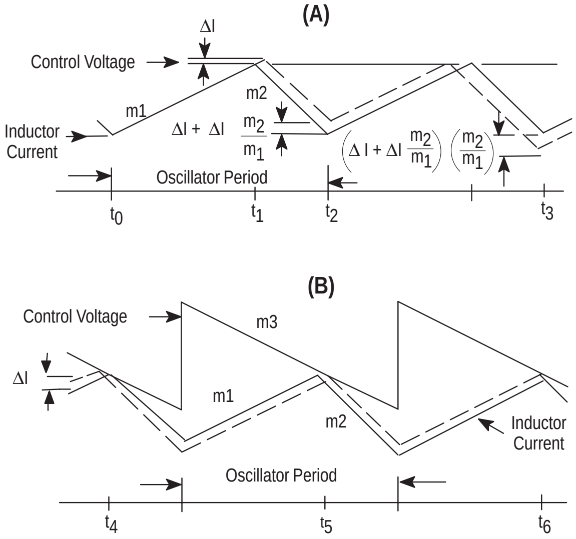
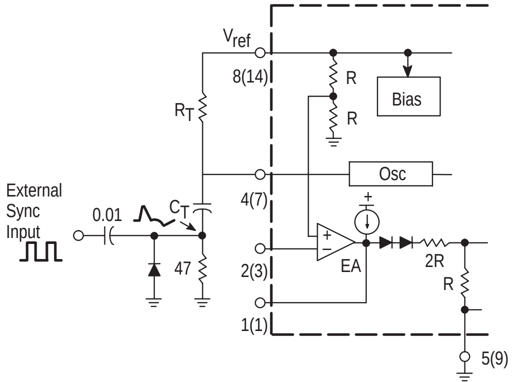
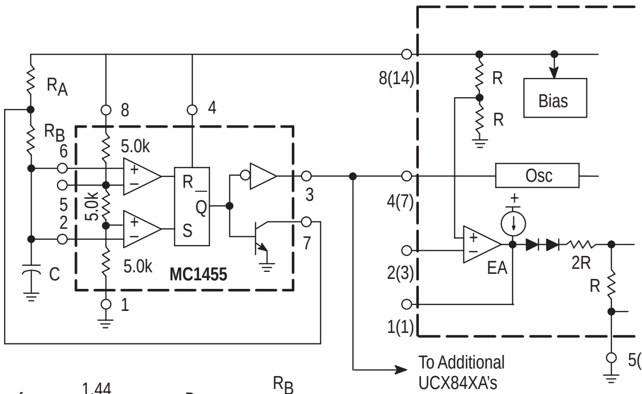


Figure 20. External Clock Synchronization



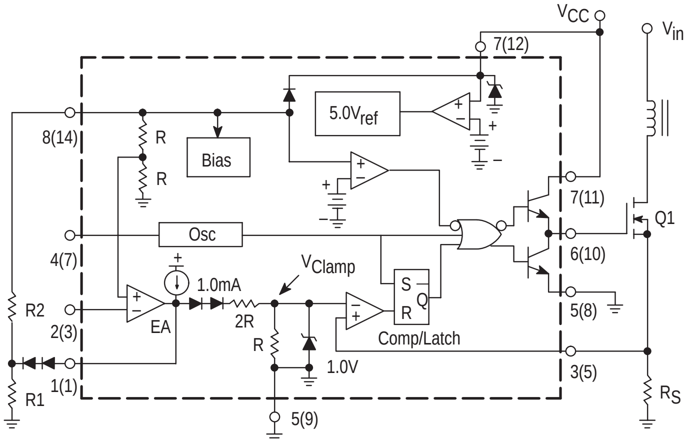
The diode clamp is required if the Sync amplitude is large enough to cause the bottom side of CT to go more than 300 mV below ground.

Figure 21. External Duty Cycle Clamp and Multi Unit Synchronization



$f = \frac{1.44}{(R_A + 2R_B)C}$ $D_{max} = \frac{R_B}{R_A + 2R_B}$

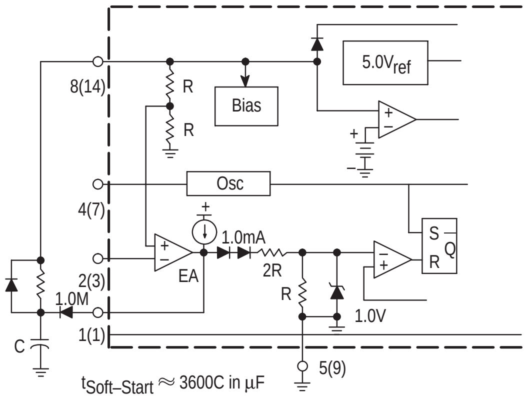
Figure 22. Adjustable Reduction of Clamp Level



$V_{Clamp} = \frac{1.67}{\left(\frac{R_2}{R_1} + 1\right)} + 0.33 \times 10^{-3} \left(\frac{R_1 R_2}{R_1 + R_2}\right)$ $I_{pk(max)} = \frac{V_{Clamp}}{RS}$

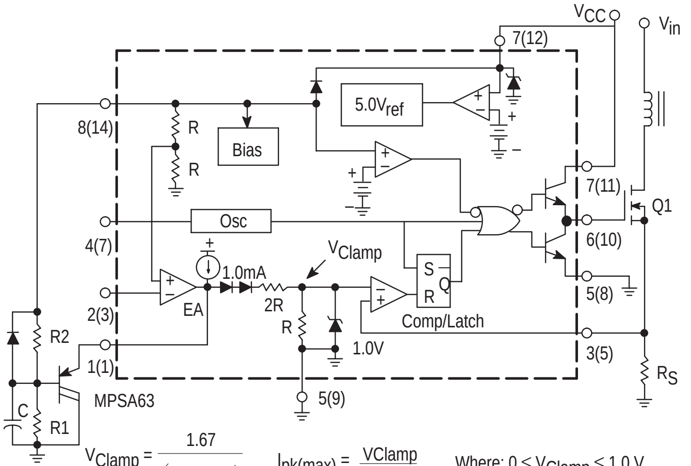
Where: $0 \le V_{Clamp} \le 1.0$ V

Figure 23. Soft–Start Circuit



$t_{Soft–Start} \approx 3600C$ in µF

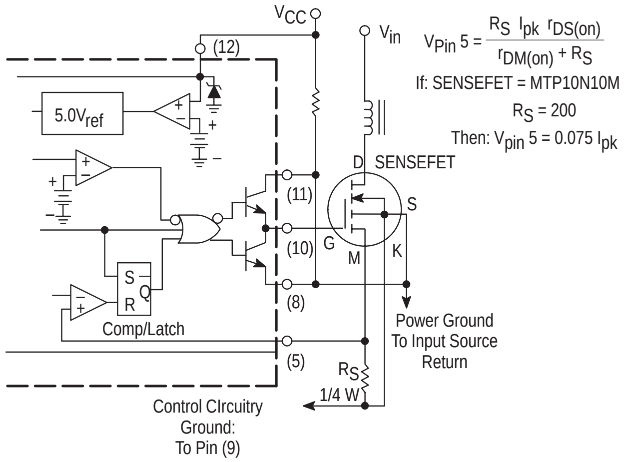
Figure 24. Adjustable Buffered Reduction of Clamp Level with Soft–Start



$V_{Clamp} = \frac{1.67}{\left(\frac{R_2}{R_1} + 1\right)}$ $I_{pk(max)} = \frac{V_{Clamp}}{RS}$ Where: $0 \le V_{Clamp} \le 1.0$ V

$t_{Softstart} = -\ln\left[1 - \frac{V_C}{3V_{Clamp}}\right] C \left(\frac{R_1 R_2}{R_1 + R_2}\right)$

Figure 25. Current Sensing Power MOSFET



$V_{Pin\,5} = \frac{R_S\; I_{pk}\; r_{DS(on)}}{r_{DM(on)} + R_S}$

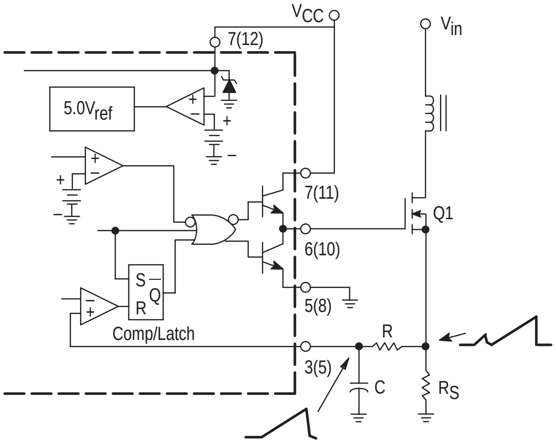
If: SENSEFET = MTP10N10M

$R_S = 200$

Then: $V_{pin\,5} = 0.075\; I_{pk}$

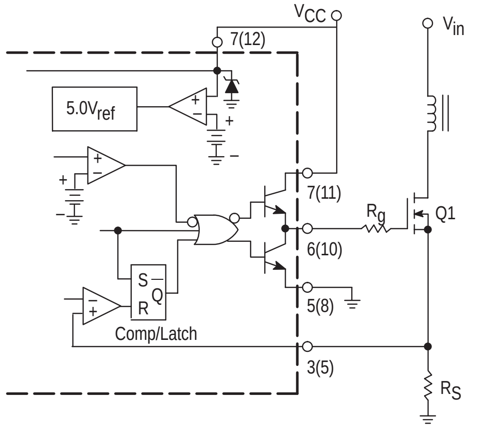
Virtually lossless current sensing can be achieved with the implementation of a SENSEFET power switch. For proper operation during over current conditions, a reduction of the $I_{pk(max)}$ clamp level must be implemented. Refer to Figures 22 and 24.

Figure 26. Current Waveform Spike Suppression



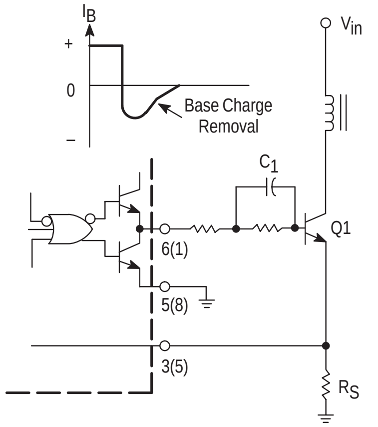
The addition of the RC filter will eliminate instability caused by the leading edge spike on the current waveform.

Figure 27. MOSFET Parasitic Oscillations



Series gate resistor R_g will damp any high frequency parasitic oscillations caused by the MOSFET input capacitance and any series wiring inductance in the gate–source circuit.

Figure 28. Bipolar Transistor Drive



The totem–pole output can furnish negative base current for enhanced transistor turn–off, with the addition of capacitor C_1.

Figure 29. Isolated MOSFET Drive

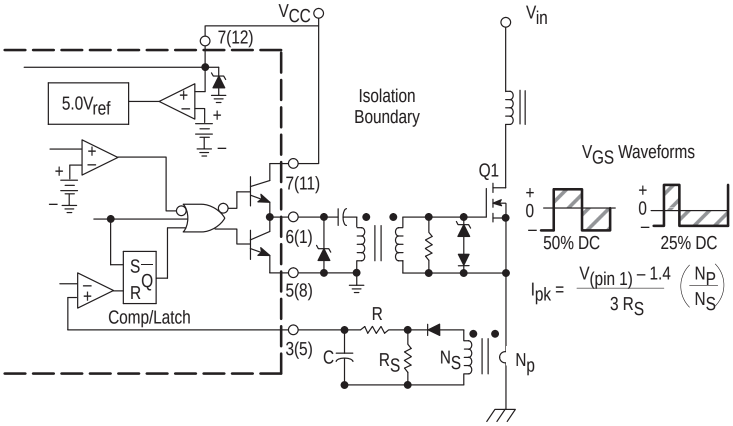
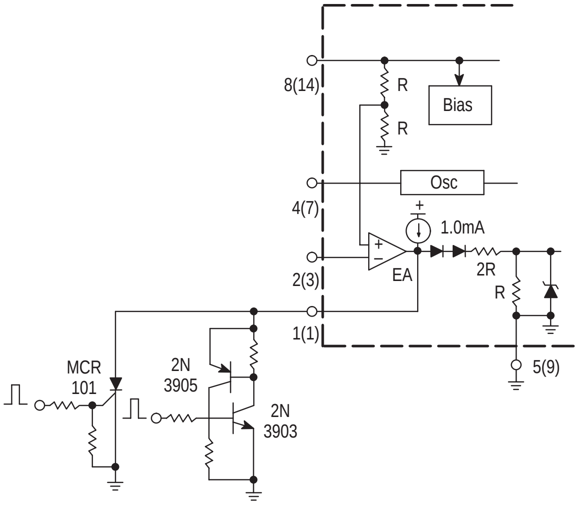
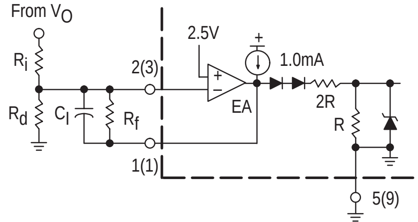


Figure 30. Latched Shutdown

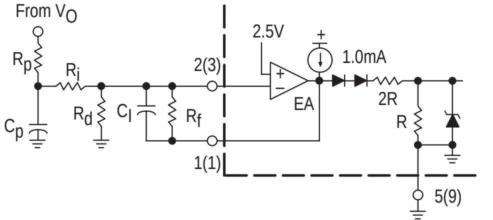


The MCR101 SCR must be selected for a holding of less than 0.5 mA at $T_{A(min)}$. The simple two transistor circuit can be used in place of the SCR as shown. All resistors are 10 k.

Figure 31. Error Amplifier Compensation

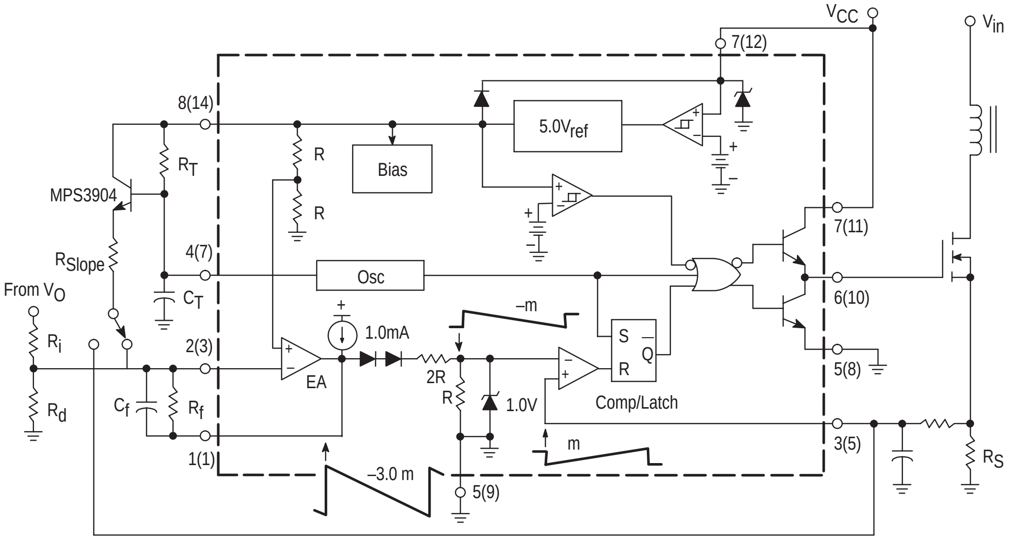


Error Amp compensation circuit for stabilizing any current–mode topology except for boost and flyback converters operating with continuous inductor current.



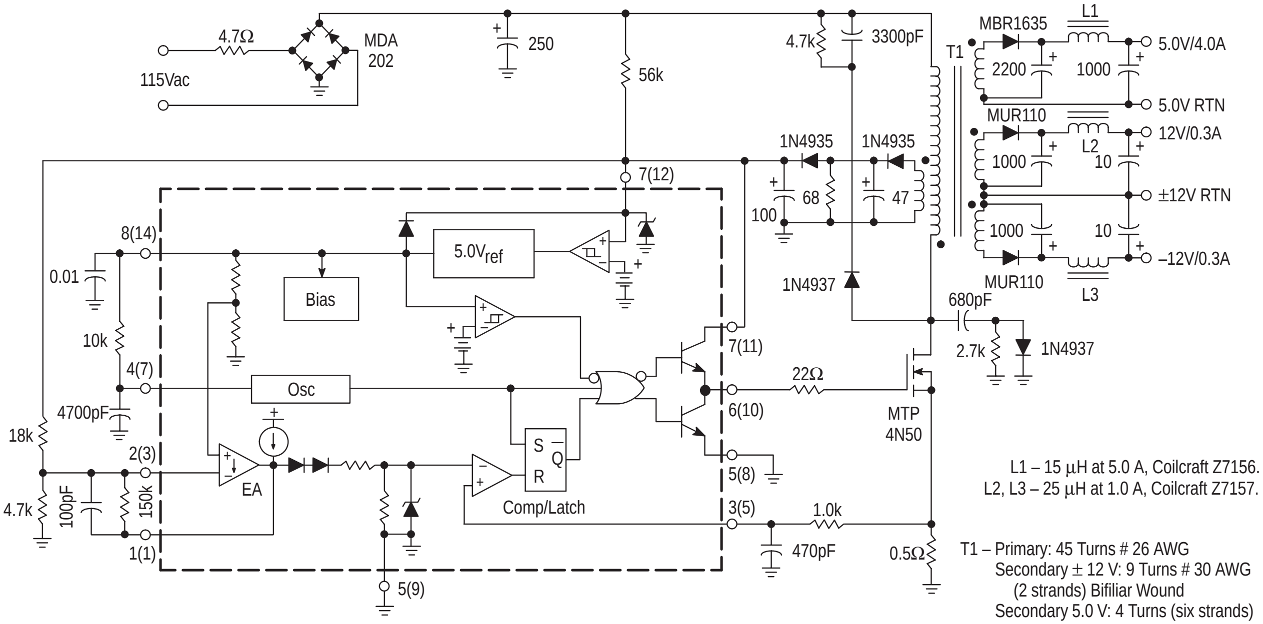
Error Amp compensation circuit for stabilizing current–mode boost and flyback topologies operating with continuous inductor current.

Figure 32. Slope Compensation



The buffered oscillator ramp can be resistively summed with either the voltage feedback or current sense inputs to provide slope compensation.

Figure 33. 27 Watt Off–Line Flyback Regulator



L1 – 15 µH at 5.0 A, Coilcraft Z7156.
L2, L3 – 25 µH at 1.0 A, Coilcraft Z7157.

T1 – Primary: 45 Turns # 26 AWG
Secondary ± 12 V: 9 Turns # 30 AWG
(2 strands) Bifiliar Wound
Secondary 5.0 V: 4 Turns (six strands)
#26 Hexfiliar Wound
Secondary Feedback: 10 Turns #30 AWG
(2 strands) Bifiliar Wound
Core: Ferroxcube EC35–3C8
Bobbin: Ferroxcube EC35PCB1
Gap ≈ 0.01" for a primary inductance of 1.0 mH

Test		Conditions	Results
Line Regulation:	5.0 V ± 12 V	V_{in} = 95 Vac to 130 Vac	Δ = 50 mV or ± 0.5% Δ = 24 mV or ± 0.1%
Load Regulation:	5.0 V ± 12 V	V_{in} = 115 Vac, I_{out} = 1.0 A to 4.0 A V_{in} = 115 Vac, I_{out} = 100 mA to 300 mA	Δ = 300 mV or ± 3.0% Δ = 60 mV or ± 0.25%
Output Ripple:	5.0 V ± 12 V	V_{in} = 115 Vac	40 mV_{pp} 80 mV_{pp}
Efficiency		V_{in} = 115 Vac	70%

All outputs are at nominal load currents, unless otherwise noted.

MOTOROLA

UC3842B, 43B
UC2842B, 43B

High Performance Current Mode Controllers

The UC3842B, UC3843B series are high performance fixed frequency current mode controllers. They are specifically designed for Off–Line and dc–to–dc converter applications offering the designer a cost–effective solution with minimal external components. These integrated circuits feature a trimmed oscillator for precise duty cycle control, a temperature compensated reference, high gain error amplifier, current sensing comparator, and a high current totem pole output ideally suited for driving a power MOSFET.

Also included are protective features consisting of input and reference undervoltage lockouts each with hysteresis, cycle–by–cycle current limiting, programmable output deadtime, and a latch for single pulse metering.

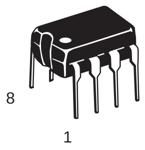
These devices are available in an 8–pin dual–in–line and surface mount (SO–8) plastic package as well as the 14–pin plastic surface mount (SO–14). The SO–14 package has separate power and ground pins for the totem pole output stage.

The UCX842B has UVLO thresholds of 16 V (on) and 10 V (off), ideally suited for off–line converters. The UCX843B is tailored for lower voltage applications having UVLO thresholds of 8.5 V (on) and 7.6 V (off).

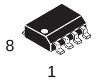
- Trimmed Oscillator for Precise Frequency Control
- Oscillator Frequency Guaranteed at 250 kHz
- Current Mode Operation to 500 kHz
- Automatic Feed Forward Compensation
- Latching PWM for Cycle–By–Cycle Current Limiting
- Internally Trimmed Reference with Undervoltage Lockout
- High Current Totem Pole Output
- Undervoltage Lockout with Hysteresis
- Low Startup and Operating Current

HIGH PERFORMANCE CURRENT MODE CONTROLLERS

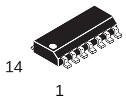
N SUFFIX
PLASTIC PACKAGE
CASE 626



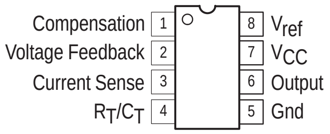
D1 SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)



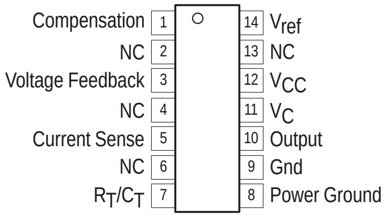
D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO–14)



PIN CONNECTIONS



(Top View)



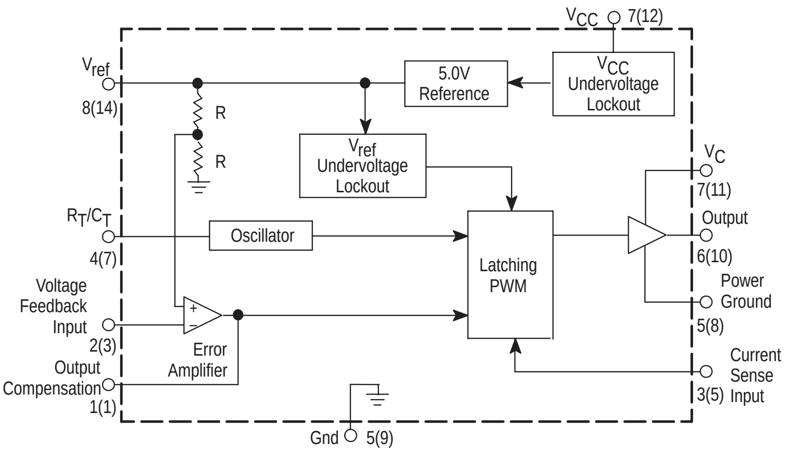
(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
UC384XBD	T_A = 0° to +70°C	SO–14
UC384XBD1		SO–8
UC384XBN		Plastic
UC284XBD	T_A = – 25° to +85°C	SO–14
UC284XBD1		SO–8
UC284XBN		Plastic
UC384XBVD	T_A = –40° to +105°C	SO–14
UC384XBVD1		SO–8
UC384XBVN		Plastic

X indicates either a 2 or 3 to define specific device part numbers.

Simplified Block Diagram



Pin numbers in parenthesis are for the D suffix SO–14 package.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Total Power Supply and Zener Current	$(I_{CC} + I_Z)$	30	mA
Output Current, Source or Sink (Note 1)	I_O	1.0	A
Output Energy (Capacitive Load per Cycle)	W	5.0	µJ
Current Sense and Voltage Feedback Inputs	V_{in}	– 0.3 to + 5.5	V
Error Amp Output Sink Current	I_O	10	mA
Power Dissipation and Thermal Characteristics			
D Suffix, Plastic Package, SO–14 Case 751A			
Maximum Power Dissipation @ T_A = 25°C	P_D	862	mW
Thermal Resistance, Junction–to–Air	$R_{\theta JA}$	145	°C/W
D1 Suffix, Plastic Package, SO–8 Case 751			
Maximum Power Dissipation @ T_A = 25°C	P_D	702	mW
Thermal Resistance, Junction–to–Air	$R_{\theta JA}$	178	°C/W
N Suffix, Plastic Package, Case 626			
Maximum Power Dissipation @ T_A = 25°C	P_D	1.25	W
Thermal Resistance, Junction–to–Air	$R_{\theta JA}$	100	°C/W
Operating Junction Temperature	T_J	+150	°C
Operating Ambient Temperature	T_A		°C
UC3842B, UC3843B		0 to + 70	
UC2842B, UC2843B		– 25 to + 85	
UC3842BV, UC3843BV		–40 to +105	
Storage Temperature Range	T_{stg}	– 65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V [Note 2], R_T = 10 k, C_T = 3.3 nF. For typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies [Note 3], unless otherwise noted.)

Characteristics	Symbol	UC284XB			UC384XB, XBV			Unit
		Min	Typ	Max	Min	Typ	Max	
REFERENCE SECTION								
Reference Output Voltage (I_O = 1.0 mA, T_J = 25°C)	V_{ref}	4.95	5.0	5.05	4.9	5.0	5.1	V
Line Regulation (V_{CC} = 12 V to 25 V)	Reg_{line}	–	2.0	20	–	2.0	20	mV
Load Regulation (I_O = 1.0 mA to 20 mA)	Reg_{load}	–	3.0	25	–	3.0	25	mV
Temperature Stability	T_S	–	0.2	–	–	0.2	–	mV/°C
Total Output Variation over Line, Load, and Temperature	V_{ref}	4.9	–	5.1	4.82	–	5.18	V
Output Noise Voltage (f = 10 Hz to 10 kHz, T_J = 25°C)	V_n	–	50	–	–	50	–	µV
Long Term Stability (T_A = 125°C for 1000 Hours)	S	–	5.0	–	–	5.0	–	mV
Output Short Circuit Current	I_{SC}	– 30	– 85	–180	– 30	– 85	–180	mA
OSCILLATOR SECTION								
Frequency	f_{OSC}							kHz
T_J = 25°C		49	52	55	49	52	55	
$T_A = T_{low}$ to T_{high}		48	–	56	48	–	56	
T_J = 25°C (R_T = 6.2 k, C_T = 1.0 nF)		225	250	275	225	250	275	
Frequency Change with Voltage (V_{CC} = 12 V to 25 V)	$\Delta f_{OSC}/\Delta V$	–	0.2	1.0	–	0.2	1.0	%
Frequency Change with Temperature $T_A = T_{low}$ to T_{high}	$\Delta f_{OSC}/\Delta T$	–	1.0	–	–	0.5	–	%
Oscillator Voltage Swing (Peak–to–Peak)	V_{OSC}	–	1.6	–	–	1.6	–	V
Discharge Current (V_{OSC} = 2.0 V)	I_{dischg}							mA
T_J = 25°C		7.8	8.3	8.8	7.8	8.3	8.8	
$T_A = T_{low}$ to T_{high} (UC284XB, UC384XB)		7.5	–	8.8	7.6	–	8.8	
(UC384XBV)		–	–	–	7.2	–	8.8	

NOTES: 1. Maximum Package power dissipation limits must be observed.
2. Adjust V_{CC} above the Startup threshold before setting to 15 V.
3. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.

T_{low} = 0°C for UC3842B, UC3843B
–25°C for UC2842B, UC2843B
–40°C for UC3842BV, UC3843BV

T_{high} = +70°C for UC3842B, UC3843B
+85°C for UC2842B, UC2843B
+105°C for UC3842BV, UC3843BV

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V [Note 2], R_T = 10 k, C_T = 3.3 nF. For typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies [Note 3], unless otherwise noted.)

Characteristics	Symbol	UC284XB			UC384XB, XBV			Unit
		Min	Typ	Max	Min	Typ	Max	
ERROR AMPLIFIER SECTION								
Voltage Feedback Input (V_O = 2.5 V)	V_{FB}	2.45	2.5	2.55	2.42	2.5	2.58	V
Input Bias Current (V_{FB} = 5.0 V)	I_{IB}	–	– 0.1	–1.0	–	– 0.1	– 2.0	µA
Open Loop Voltage Gain (V_O = 2.0 V to 4.0 V)	A_{VOL}	65	90	–	65	90	–	dB
Unity Gain Bandwidth (T_J = 25°C)	BW	0.7	1.0	–	0.7	1.0	–	MHz
Power Supply Rejection Ratio (V_{CC} = 12 V to 25 V)	PSRR	60	70	–	60	70	–	dB
Output Current								mA
Sink (V_O = 1.1 V, V_{FB} = 2.7 V)	I_{Sink}	2.0	12	–	2.0	12	–	
Source (V_O = 5.0 V, V_{FB} = 2.3 V)	I_{Source}	– 0.5	–1.0	–	– 0.5	–1.0	–	
Output Voltage Swing								V
High State (R_L = 15 k to ground, V_{FB} = 2.3 V)	V_{OH}	5.0	6.2	–	5.0	6.2	–	
Low State (R_L = 15 k to V_{ref}, V_{FB} = 2.7 V)	V_{OL}							
(UC284XB, UC384XB)		–	0.8	1.1	–	0.8	1.1	
(UC384XBV)		–	–	–	–	0.8	1.2	
CURRENT SENSE SECTION								
Current Sense Input Voltage Gain (Notes 4 & 5)	A_V							V/V
(UC284XB, UC384XB)		2.85	3.0	3.15	2.85	3.0	3.15	
(UC384XBV)		–	–	–	2.85	3.0	3.25	
Maximum Current Sense Input Threshold (Note 4)	V_{th}							V
(UC284XB, UC384XB)		0.9	1.0	1.1	0.9	1.0	1.1	
(UC384XBV)		–	–	–	0.85	1.0	1.1	
Power Supply Rejection Ratio V_{CC} = 12 V to 25 V, Note 4	PSRR	–	70	–	–	70	–	dB
Input Bias Current	I_{IB}	–	– 2.0	–10	–	– 2.0	–10	µA
Propagation Delay (Current Sense Input to Output)	$t_{PLH(In/Out)}$	–	150	300	–	150	300	ns
OUTPUT SECTION								
Output Voltage								V
Low State (I_{Sink} = 20 mA)	V_{OL}	–	0.1	0.4	–	0.1	0.4	
(I_{Sink} = 200 mA) (UC284XB, UC384XB)		–	1.6	2.2	–	1.6	2.2	
(UC384XBV)		–	–	–	–	1.6	2.3	
High State (I_{Source} = 20 mA) (UC284XB, UC384XB)	V_{OH}	13	13.5	–	13	13.5	–	
(UC384XBV)		–	–	–	12.9	13.5	–	
(I_{Source} = 200 mA)		12	13.4	–	12	13.4	–	
Output Voltage with UVLO Activated V_{CC} = 6.0 V, I_{Sink} = 1.0 mA	$V_{OL(UVLO)}$	–	0.1	1.1	–	0.1	1.1	V
Output Voltage Rise Time (C_L = 1.0 nF, T_J = 25°C)	t_r	–	50	150	–	50	150	ns
Output Voltage Fall Time (C_L = 1.0 nF, T_J = 25°C)	t_f	–	50	150	–	50	150	ns
UNDERVOLTAGE LOCKOUT SECTION								
Startup Threshold (V_{CC})	V_{th}							V
UCX842B, BV		15	16	17	14.5	16	17.5	
UCX843B, BV		7.8	8.4	9.0	7.8	8.4	9.0	
Minimum Operating Voltage After Turn–On (V_{CC})	$V_{CC(min)}$							V
UCX842B, BV		9.0	10	11	8.5	10	11.5	
UCX843B, BV		7.0	7.6	8.2	7.0	7.6	8.2	

NOTES: 2. Adjust V_{CC} above the Startup threshold before setting to 15 V.

3. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.

T_{low} =		T_{high} =	
	0°C for UC3842B, UC3843B		+70°C for UC3842B, UC3843B
	–25°C for UC2842B, UC2843B		+85°C for UC2842B, UC2843B
	–40°C for UC3842BV, UC3843BV		+105°C for UC3842BV, UC3843BV

4. This parameter is measured at the latch trip point with V_{FB} = 0 V.

5. Comparator gain is defined as: $A_V \frac{\Delta V \text{ Output Compensation}}{\Delta V \text{ Current Sense Input}}$

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V [Note 2], R_T = 10 k, C_T = 3.3 nF, for typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies [Note 3], unless otherwise noted.)

Characteristics	Symbol	UC284XB			UC384XB, BV			Unit
		Min	Typ	Max	Min	Typ	Max	
PWM SECTION								
Duty Cycle								%
Maximum (UC284XB, UC384XB)	$DC_{(max)}$	94	96	–	94	96	–	
(UC384XBV)		–	–	–	93	96	–	
Minimum	$DC_{(min)}$	–	–	0	–	–	0	
TOTAL DEVICE								
Power Supply Current	$I_{CC} + I_C$							mA
Startup (V_{CC} = 6.5 V for UCX843B, (V_{CC} 14 V for UCX842B, BV)		–	0.3	0.5	–	0.3	0.5	
Operating (Note 2)		–	12	17	–	12	17	
Power Supply Zener Voltage (I_{CC} = 25 mA)	V_Z	30	36	–	30	36	–	V

NOTES: 2. Adjust V_{CC} above the Startup threshold before setting to 15 V.
3. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.

T_{low} = 0°C for UC3842B, UC3843B
–25°C for UC2842B, UC2843B
–40°C for UC3842BV, UC3843BV

T_{high} = +70°C for UC3842B, UC3843B
+85°C for UC2842B, UC2843B
+105°C for UC3842BV, UC3843BV

Figure 1. Timing Resistor versus Oscillator Frequency

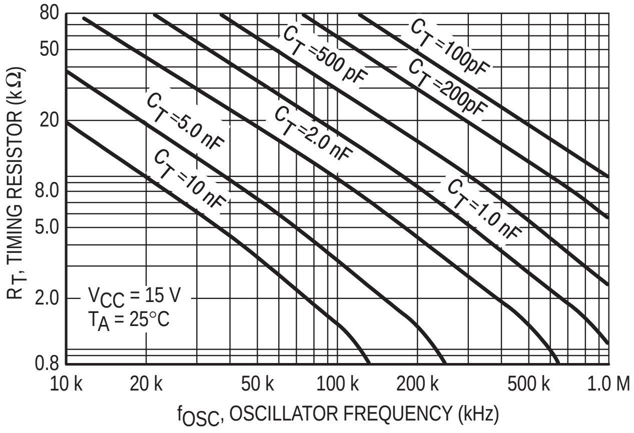


Figure 2. Output Deadtime versus Oscillator Frequency

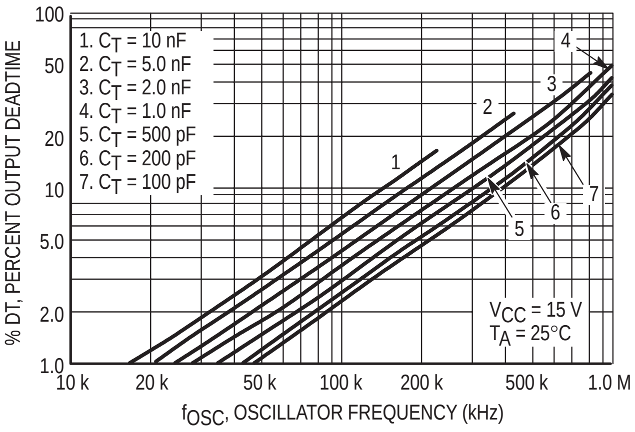


Figure 3. Oscillator Discharge Current versus Temperature

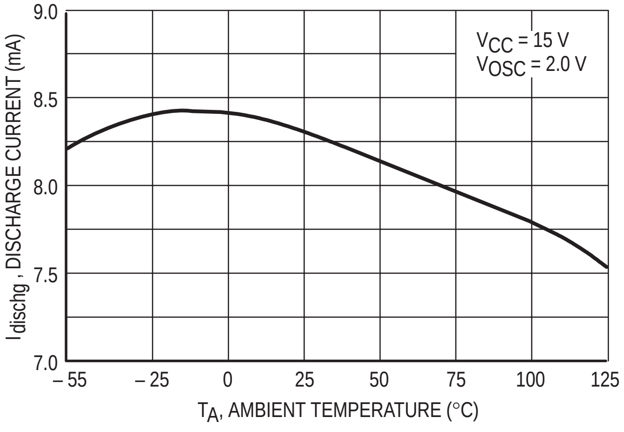


Figure 4. Maximum Output Duty Cycle versus Timing Resistor

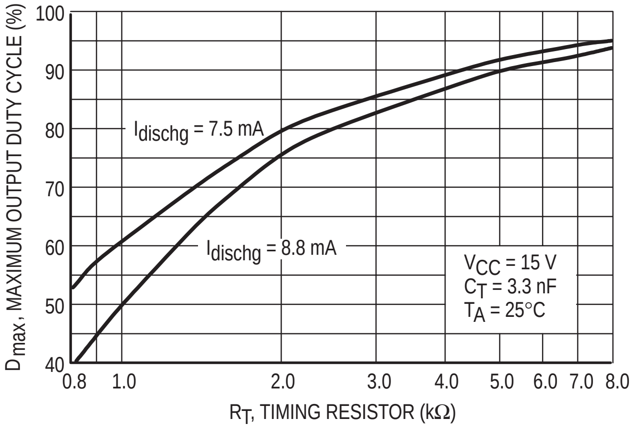


Figure 5. Error Amp Small Signal Transient Response

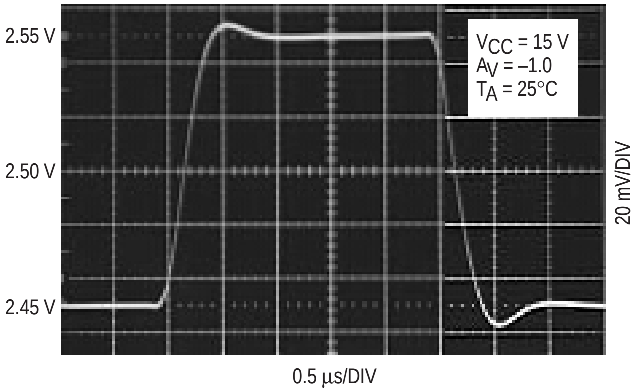


Figure 6. Error Amp Large Signal Transient Response

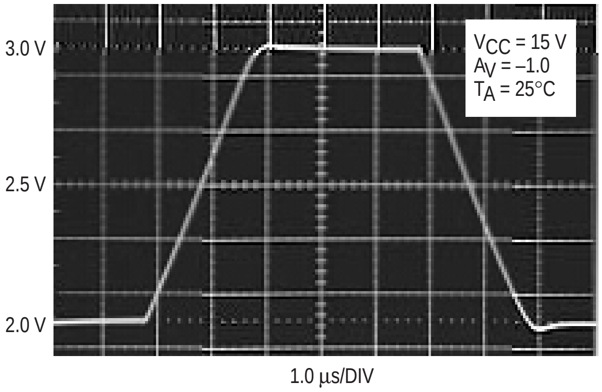


Figure 7. Error Amp Open Loop Gain and Phase versus Frequency

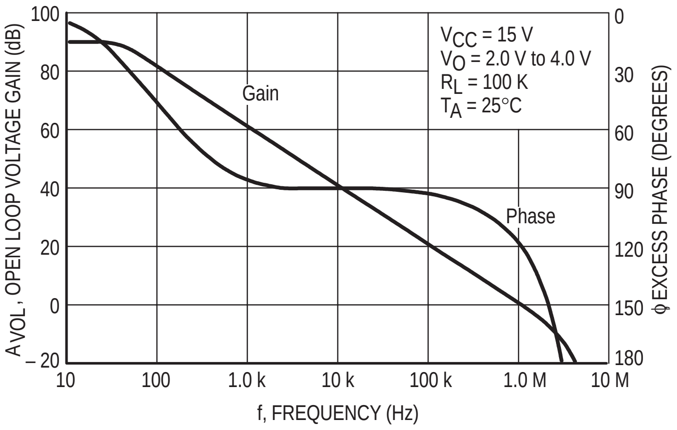


Figure 8. Current Sense Input Threshold versus Error Amp Output Voltage

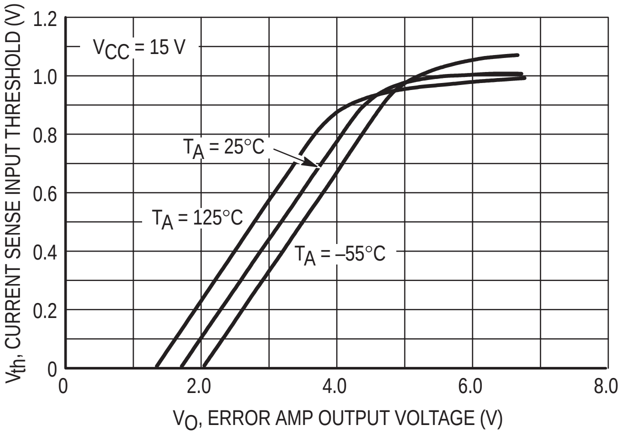


Figure 9. Reference Voltage Change versus Source Current

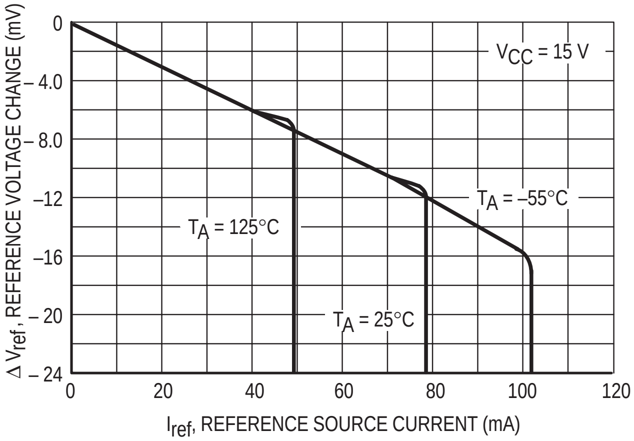


Figure 10. Reference Short Circuit Current versus Temperature

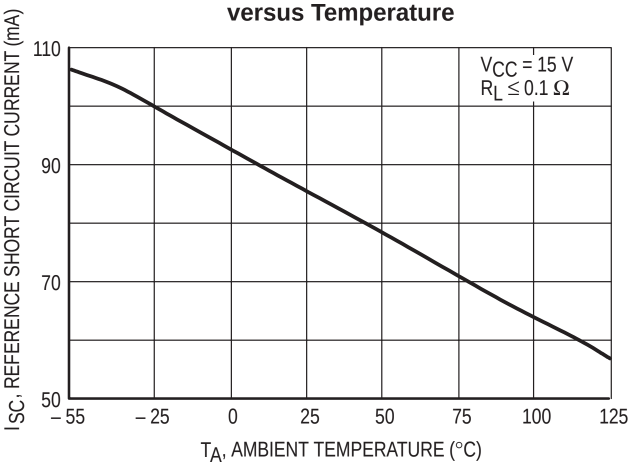


Figure 11. Reference Load Regulation

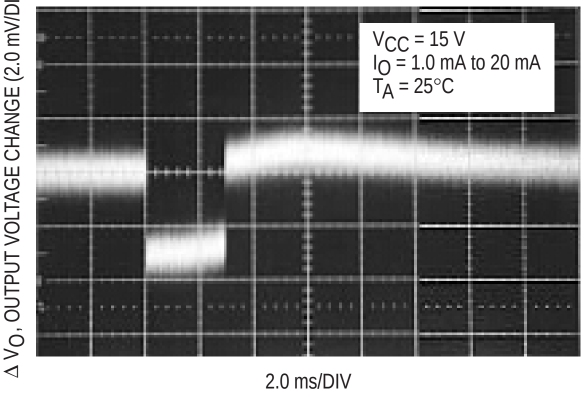


Figure 12. Reference Line Regulation

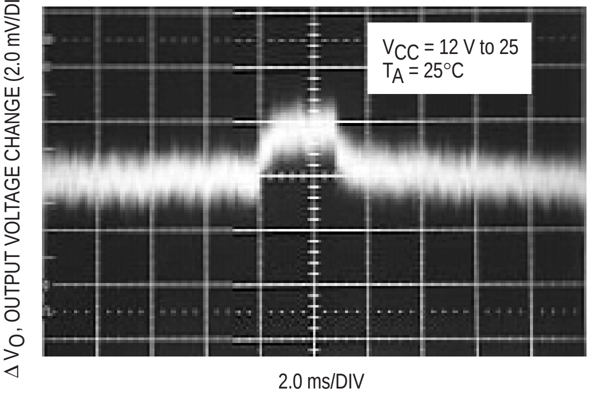


Figure 13. Output Saturation Voltage versus Load Current

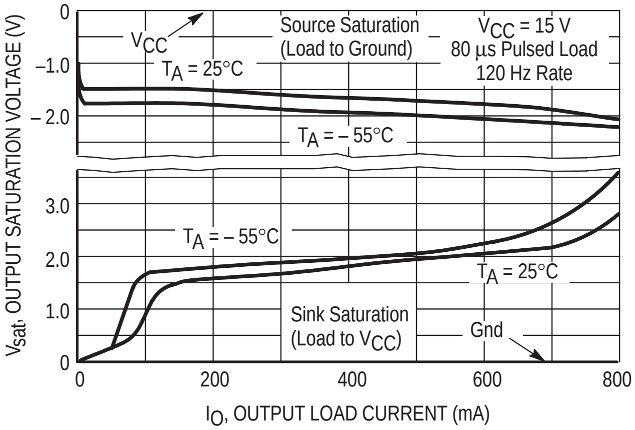


Figure 14. Output Waveform

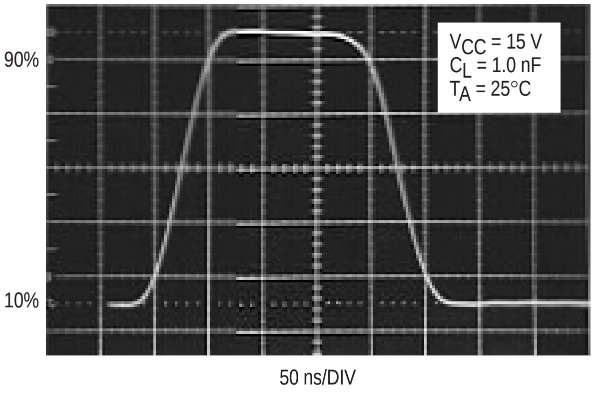


Figure 15. Output Cross Conduction

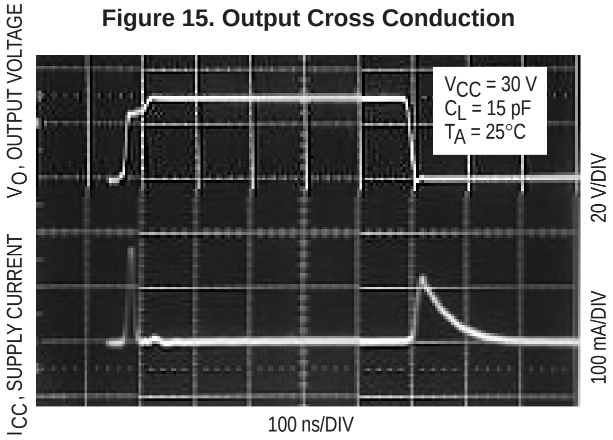
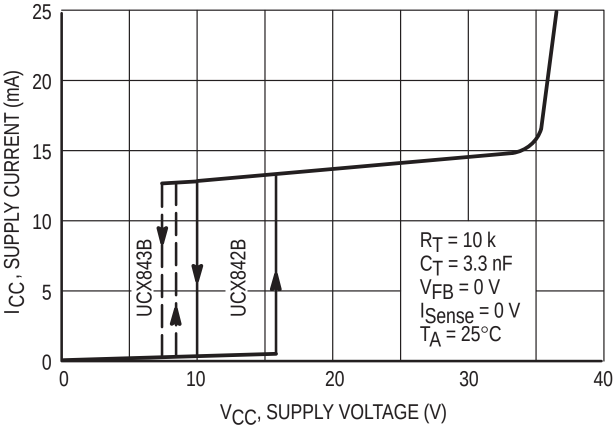


Figure 16. Supply Current versus Supply Voltage



PIN FUNCTION DESCRIPTION

Pin		Function	Description
8–Pin	14–Pin		
1	1	Compensation	This pin is the Error Amplifier output and is made available for loop compensation.
2	3	Voltage Feedback	This is the inverting input of the Error Amplifier. It is normally connected to the switching power supply output through a resistor divider.
3	5	Current Sense	A voltage proportional to inductor current is connected to this input. The PWM uses this information to terminate the output switch conduction.
4	7	R_T/C_T	The Oscillator frequency and maximum Output duty cycle are programmed by connecting resistor R_T to V_{ref} and capacitor C_T to ground. Operation to 500 kHz is possible.
5		Gnd	This pin is the combined control circuitry and power ground.
6	10	Output	This output directly drives the gate of a power MOSFET. Peak currents up to 1.0 A are sourced and sunk by this pin.
7	12	V_{CC}	This pin is the positive supply of the control IC.
8	14	V_{ref}	This is the reference output. It provides charging current for capacitor C_T through resistor R_T.
	8	Power Ground	This pin is a separate power ground return that is connected back to the power source. It is used to reduce the effects of switching transient noise on the control circuitry.
	11	V_C	The Output high state (V_{OH}) is set by the voltage applied to this pin. With a separate power source connection, it can reduce the effects of switching transient noise on the control circuitry.
	9	Gnd	This pin is the control circuitry ground return and is connected back to the power source ground.
	2,4,6,13	NC	No connection. These pins are not internally connected.

OPERATING DESCRIPTION

The UC3842B, UC3843B series are high performance, fixed frequency, current mode controllers. They are specifically designed for Off–Line and dc–to–dc converter applications offering the designer a cost–effective solution with minimal external components. A representative block diagram is shown in Figure 17.

Oscillator

The oscillator frequency is programmed by the values selected for the timing components R_T and C_T. Capacitor C_T is charged from the 5.0 V reference through resistor R_T to approximately 2.8 V and discharged to 1.2 V by an internal current sink. During the discharge of C_T, the oscillator generates an internal blanking pulse that holds the center input of the NOR gate high. This causes the Output to be in a low state, thus producing a controlled amount of output deadtime. Figure 1 shows R_T versus Oscillator Frequency and Figure 2, Output Deadtime versus Frequency, both for given values of C_T. Note that many values of R_T and C_T will give the same oscillator frequency but only one combination will yield a specific output deadtime at a given frequency. The oscillator thresholds are temperature compensated to within ±6% at 50 kHz. Also because of industry trends moving the UC384X into higher and higher frequency applications, the UC384XB is guaranteed to within ±10% at 250 kHz. These internal circuit refinements minimize variations of oscillator frequency and maximum output duty cycle. The results are shown in Figures 3 and 4.

In many noise–sensitive applications it may be desirable to frequency–lock the converter to an external system clock. This can be accomplished by applying a clock signal to the circuit shown in Figure 20. For reliable locking, the free–running oscillator frequency should be set about 10% less than the clock frequency. A method for multi–unit synchronization is shown in Figure 21. By tailoring the clock waveform, accurate Output duty cycle clamping can be achieved.

Error Amplifier

A fully compensated Error Amplifier with access to the inverting input and output is provided. It features a typical dc voltage gain of 90 dB, and a unity gain bandwidth of 1.0 MHz with 57 degrees of phase margin (Figure 7). The non–inverting input is internally biased at 2.5 V and is not pinned out. The converter output voltage is typically divided down and monitored by the inverting input. The maximum input bias current is –2.0 µA which can cause an output voltage error that is equal to the product of the input bias current and the equivalent input divider source resistance.

The Error Amp Output (Pin 1) is provided for external loop compensation (Figure 31). The output voltage is offset by two diode drops (≈1.4 V) and divided by three before it connects to the non–inverting input of the Current Sense Comparator. This guarantees that no drive pulses appear at the Output (Pin 6) when pin 1 is at its lowest state (V_{OL}). This occurs when the power supply is operating and the load is removed, or at the beginning of a soft–start interval (Figures 23, 24). The Error Amp minimum feedback resistance is limited by the amplifier's source current (0.5 mA) and the required output voltage (V_{OH}) to reach the comparator's 1.0 V clamp level:

$$R_{f(min)} \approx \frac{3.0\ (1.0\ V) + 1.4\ V}{0.5\ mA} = 8800\ \Omega$$

Current Sense Comparator and PWM Latch

The UC3842B, UC3843B operate as a current mode controller, whereby output switch conduction is initiated by the oscillator and terminated when the peak inductor current reaches the threshold level established by the Error Amplifier Output/Compensation (Pin 1). Thus the error signal controls the peak inductor current on a cycle–by–cycle basis. The Current Sense Comparator PWM Latch configuration used ensures that only a single pulse appears at the Output during any given oscillator cycle. The inductor current is converted to a voltage by inserting the ground–referenced sense resistor R_S in series with the source of output switch Q1. This voltage is monitored by the Current Sense Input (Pin 3) and compared to a level derived from the Error Amp Output. The peak inductor current under normal operating conditions is controlled by the voltage at pin 1 where:

$$I_{pk} = \frac{V_{(Pin\ 1)} - 1.4\ V}{3\ R_S}$$

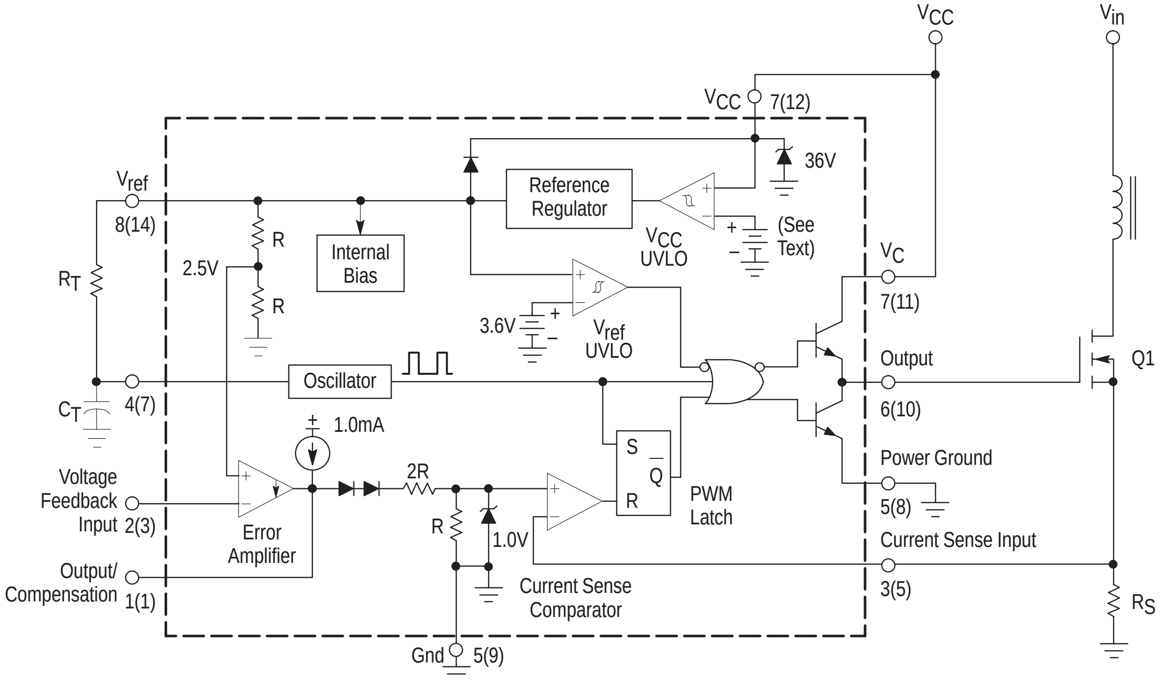
Abnormal operating conditions occur when the power supply output is overloaded or if output voltage sensing is lost. Under these conditions, the Current Sense Comparator threshold will be internally clamped to 1.0 V. Therefore the maximum peak switch current is:

$$I_{pk(max)} = \frac{1.0\ V}{R_S}$$

When designing a high power switching regulator it becomes desirable to reduce the internal clamp voltage in order to keep the power dissipation of R_S to a reasonable level. A simple method to adjust this voltage is shown in Figure 22. The two external diodes are used to compensate the internal diodes, yielding a constant clamp voltage over temperature. Erratic operation due to noise pickup can result if there is an excessive reduction of the $I_{pk(max)}$ clamp voltage.

A narrow spike on the leading edge of the current waveform can usually be observed and may cause the power supply to exhibit an instability when the output is lightly loaded. This spike is due to the power transformer interwinding capacitance and output rectifier recovery time. The addition of an RC filter on the Current Sense Input with a time constant that approximates the spike duration will usually eliminate the instability (refer to Figure 26).

Figure 17. Representative Block Diagram



Pin numbers adjacent to terminals are for the 8–pin dual–in–line package.
Pin numbers in parenthesis are for the D suffix SO–14 package.

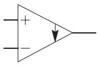
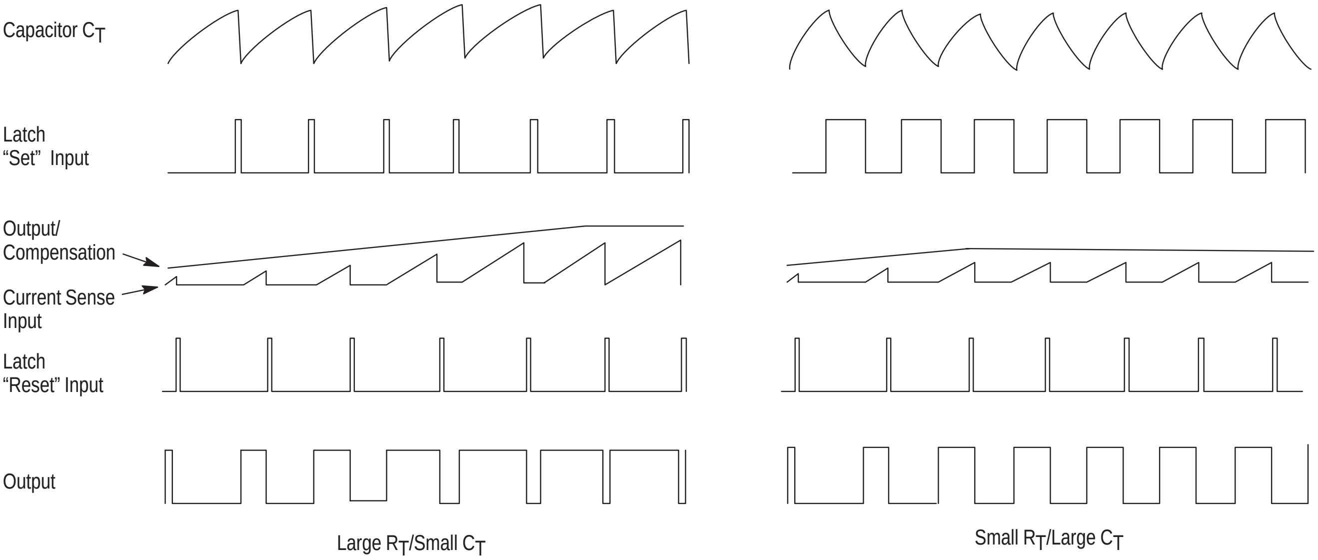

= Sink Only Positive True Logic

Figure 18. Timing Diagram



Undervoltage Lockout

Two undervoltage lockout comparators have been incorporated to guarantee that the IC is fully functional before the output stage is enabled. The positive power supply terminal (V_{CC}) and the reference output (V_{ref}) are each monitored by separate comparators. Each has built–in hysteresis to prevent erratic output behavior as their respective thresholds are crossed. The V_{CC} comparator upper and lower thresholds are 16 V/10 V for the UCX842B, and 8.4 V/7.6 V for the UCX843B. The V_{ref} comparator upper and lower thresholds are 3.6 V/3.4 V. The large hysteresis and low startup current of the UCX842B makes it ideally suited in off–line converter applications where efficient bootstrap startup techniques are required (Figure 33). The UCX843B is intended for lower voltage dc–to–dc converter applications. A 36 V zener is connected as a shunt regulator from V_{CC} to ground. Its purpose is to protect the IC from excessive voltage that can occur during system startup. The minimum operating voltage (V_{CC}) for the UCX842B is 11 V and 8.2 V for the UCX843B.

These devices contain a single totem pole output stage that was specifically designed for direct drive of power MOSFETs. It is capable of up to ±1.0 A peak drive current and has a typical rise and fall time of 50 ns with a 1.0 nF load. Additional internal circuitry has been added to keep the Output in a sinking mode whenever an undervoltage lockout is active. This characteristic eliminates the need for an external pull–down resistor.

The SO–14 surface mount package provides separate pins for V_C (output supply) and Power Ground. Proper implementation will significantly reduce the level of switching transient noise imposed on the control circuitry. This becomes particularly useful when reducing the $I_{pk(max)}$ clamp level. The separate V_C supply input allows the designer added flexibility in tailoring the drive voltage independent of V_{CC}. A zener clamp is typically connected to this input when driving power MOSFETs in systems where V_{CC} is greater than 20 V. Figure 25 shows proper power and control ground connections in a current–sensing power MOSFET application.

Reference

The 5.0 V bandgap reference is trimmed to ±1.0% tolerance at $T_J = 25°C$ on the UC284XB, and ±2.0% on the UC384XB. Its primary purpose is to supply charging current to the oscillator timing capacitor. The reference has short–circuit protection and is capable of providing in excess of 20 mA for powering additional control system circuitry.

Design Considerations

Do not attempt to construct the converter on wire–wrap or plug–in prototype boards. High frequency circuit layout techniques are imperative to prevent pulse–width jitter. This is usually caused by excessive noise pick–up imposed on the Current Sense or Voltage Feedback inputs. Noise immunity can be improved by lowering circuit impedances at these points. The printed circuit layout should contain a ground plane with low–current signal and high–current switch and output grounds returning on separate paths back to the input filter capacitor. Ceramic bypass capacitors (0.1 μF) connected directly to V_{CC}, V_C, and V_{ref} may be required depending upon circuit layout. This provides a low impedance path for filtering the high frequency noise. All high current loops should be kept as short as possible using heavy copper runs to minimize radiated EMI. The Error Amp compensation circuitry and the converter output voltage divider should be located close to the IC and as far as possible from the power switch and other noise–generating components.

Current mode converters can exhibit subharmonic oscillations when operating at a duty cycle greater than 50% with continuous inductor current. This instability is independent of the regulator's closed loop characteristics and is caused by the simultaneous operating conditions of fixed frequency and peak current detecting. Figure 19A shows the phenomenon graphically. At t_0, switch conduction begins, causing the inductor current to rise at a slope of m_1. This slope is a function of the input voltage divided by the inductance. At t_1, the Current Sense Input reaches the threshold established by the control voltage. This causes the switch to turn off and the current to decay at a slope of m_2, until the next oscillator cycle. The unstable condition can be shown if a perturbation is added to the control voltage, resulting in a small ΔI (dashed line). With a fixed oscillator period, the current decay time is reduced, and the minimum current at switch turn–on (t_2) is increased by $\Delta I + \Delta I\, m_2/m_1$. The minimum current at the next cycle (t_3) decreases to $(\Delta I + \Delta I\, m_2/m_1)\,(m_2/m_1)$. This perturbation is multiplied by m_2/m_1 on each succeeding cycle, alternately increasing and decreasing the inductor current at switch turn–on. Several oscillator cycles may be required before the inductor current reaches zero causing the process to commence again. If m_2/m_1 is greater than 1, the converter will be unstable. Figure 19B shows that by adding an artificial ramp that is synchronized with the PWM clock to the control voltage, the ΔI perturbation will decrease to zero on succeeding cycles. This compensating ramp (m_3) must have a slope equal to or slightly greater than $m_2/2$ for stability. With $m_2/2$ slope compensation, the average inductor current follows the control voltage, yielding true current mode operation. The compensating ramp can be derived from the oscillator and added to either the Voltage Feedback or Current Sense inputs (Figure 32).

Figure 19. Continuous Current Waveforms

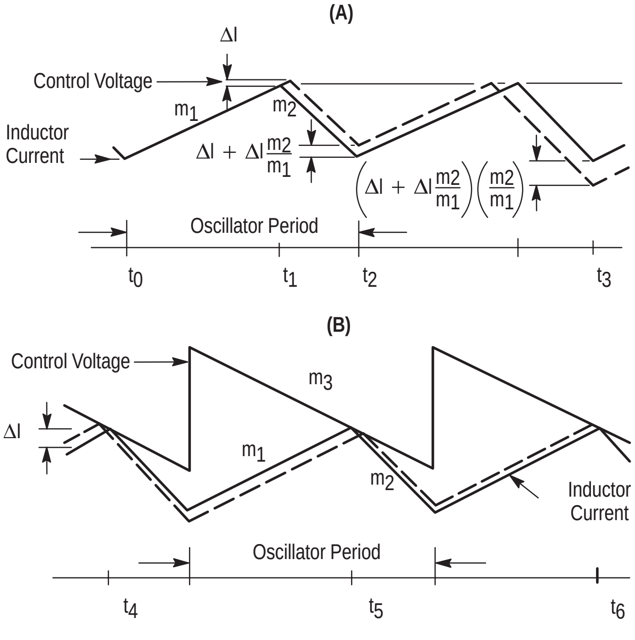
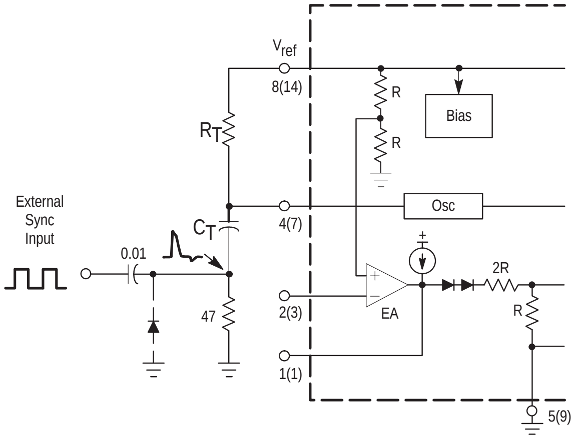
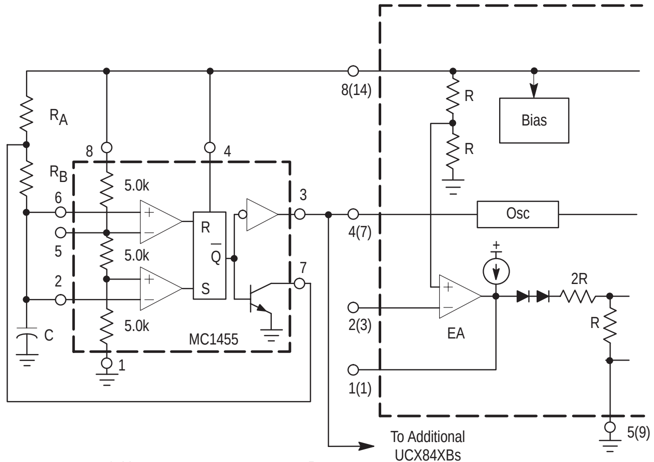


Figure 20. External Clock Synchronization



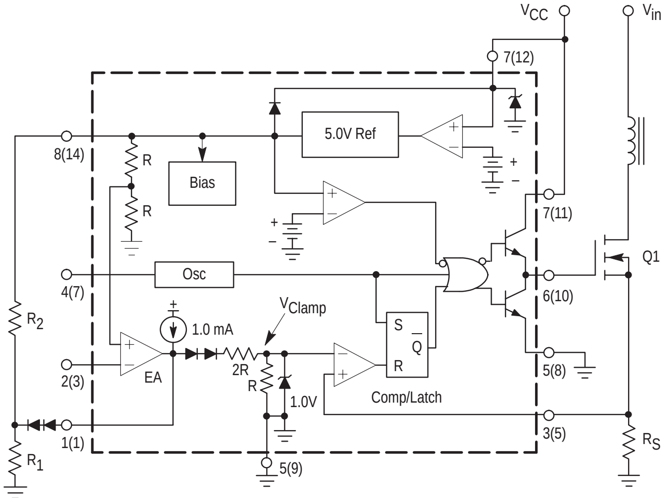
The diode clamp is required if the Sync amplitude is large enough to cause the bottom side of C_T to go more than 300 mV below ground.

Figure 21. External Duty Cycle Clamp and Multi–Unit Synchronization



$$f = \frac{1.44}{(R_A + 2R_B)C} \qquad D_{(max)} = \frac{R_B}{R_A + 2R_B}$$

Figure 22. Adjustable Reduction of Clamp Level

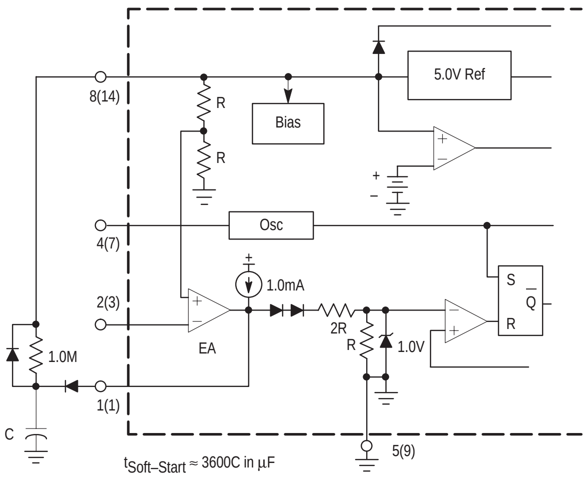


$$V_{Clamp} \approx \frac{1.67}{\left(\frac{R_2}{R_1} + 1\right)} + 0.33\text{x}10^{-3} \left(\frac{R_1 R_2}{R_1 + R_2}\right)$$

Where: $0 \leq V_{Clamp} \leq 1.0$ V

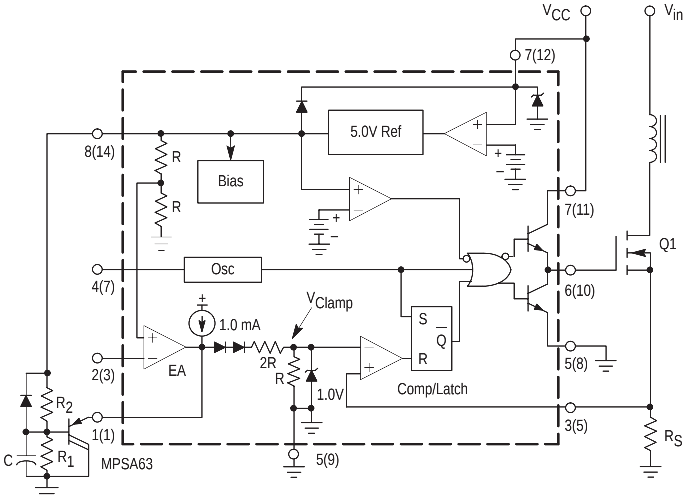
$$I_{pk(max)} \approx \frac{V_{Clamp}}{R_S}$$

Figure 23. Soft–Start Circuit



$t_{Soft–Start} \approx 3600C$ in µF

Figure 24. Adjustable Buffered Reduction of Clamp Level with Soft–Start



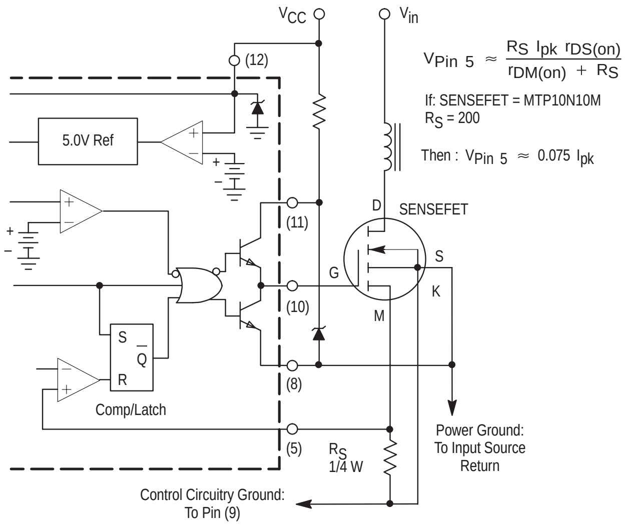
$$V_{Clamp} \approx \frac{1.67}{\left(\frac{R_2}{R_1} + 1\right)}$$

Where: $0 \leq V_{Clamp} \leq 1.0\ V$

$$t_{Soft\text{-}Start} = -\ln\left[1 - \frac{V_C}{3\ V_{Clamp}}\right] C \frac{R_1\ R_2}{R_1 + R_2}$$

$$I_{pk(max)} \approx \frac{V_{Clamp}}{R_S}$$

Figure 25. Current Sensing Power MOSFET



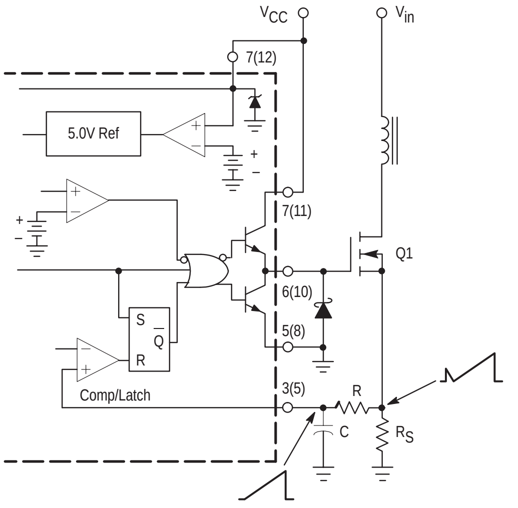
$$V_{Pin\ 5} \approx \frac{R_S\ I_{pk}\ r_{DS(on)}}{r_{DM(on)} + R_S}$$

If: SENSEFET = MTP10N10M
$R_S = 200$

Then : $V_{Pin\ 5} \approx 0.075\ I_{pk}$

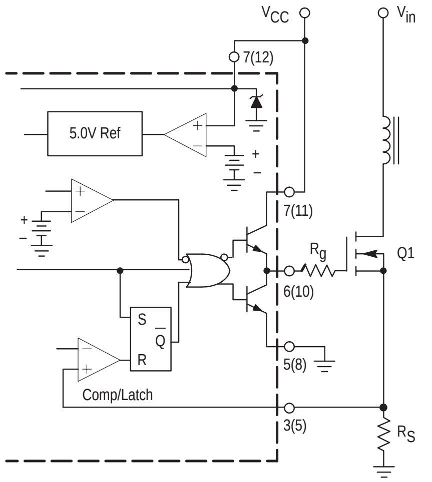
Virtually lossless current sensing can be achieved with the implementation of a SENSEFET power switch. For proper operation during over–current conditions, a reduction of the $I_{pk(max)}$ clamp level must be implemented. Refer to Figures 22 and 24.

Figure 26. Current Waveform Spike Suppression



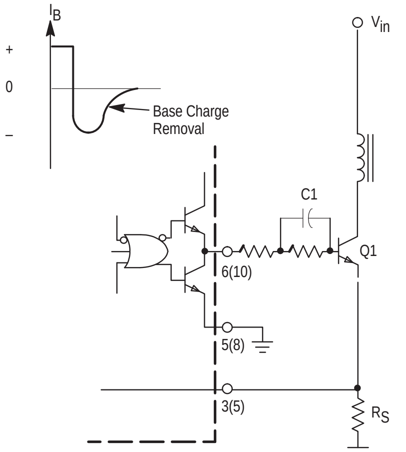
The addition of the RC filter will eliminate instability caused by the leading edge spike on the current waveform.

Figure 27. MOSFET Parasitic Oscillations



Series gate resistor R_g will damp any high frequency parasitic oscillations caused by the MOSFET input capacitance and any series wiring inductance in the gate–source circuit.

Figure 28. Bipolar Transistor Drive



The totem pole output can furnish negative base current for enhanced transistor turn–off, with the addition of capacitor C_1.

Figure 29. Isolated MOSFET Drive

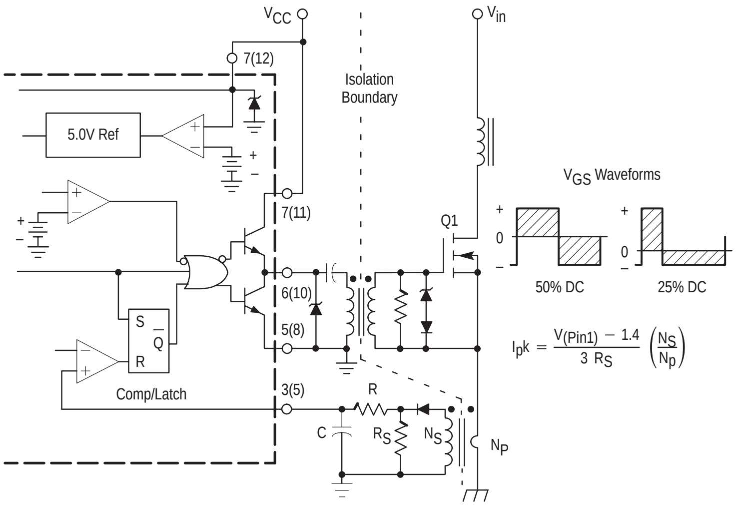
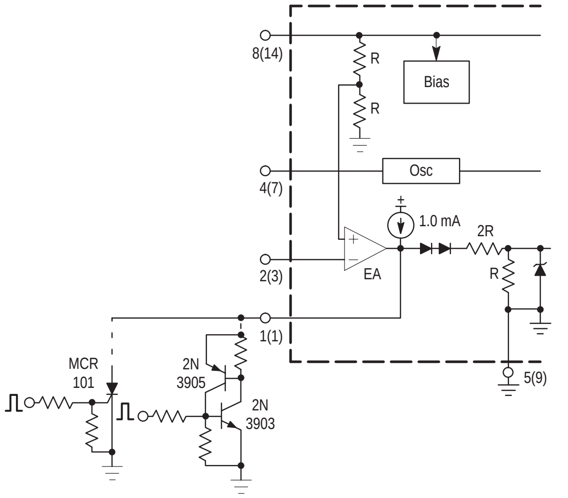
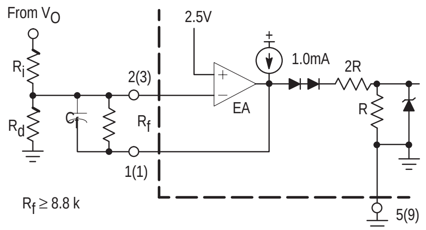


Figure 30. Latched Shutdown

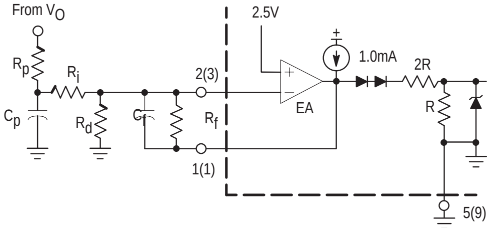


The MCR101 SCR must be selected for a holding of < 0.5 mA @ $T_{A(min)}$. The simple two transistor circuit can be used in place of the SCR as shown. All resistors are 10 k.

Figure 31. Error Amplifier Compensation

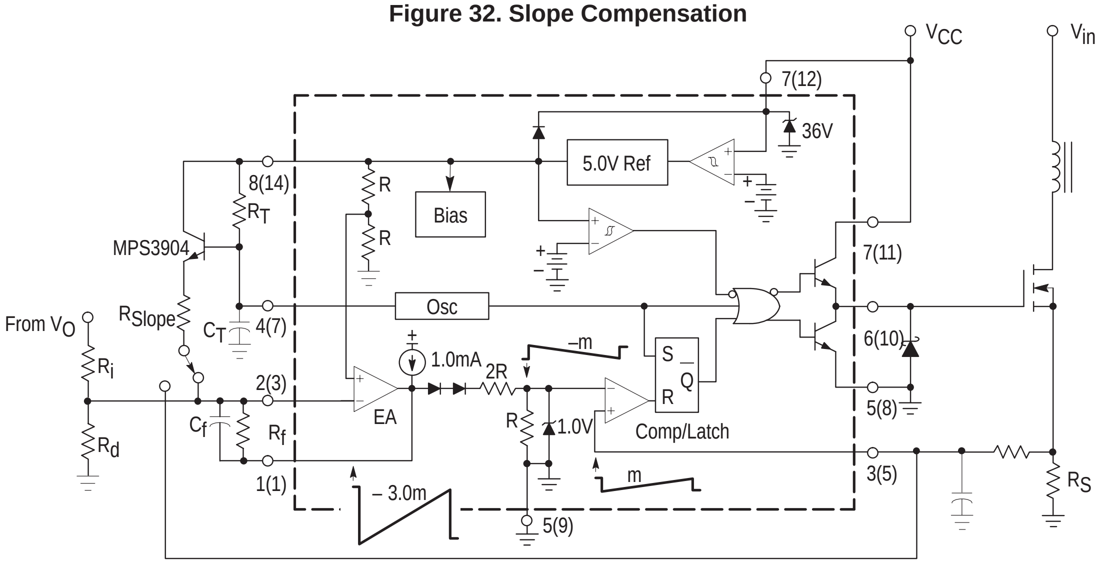


Error Amp compensation circuit for stabilizing any current mode topology except for boost and flyback converters operating with continuous inductor current.



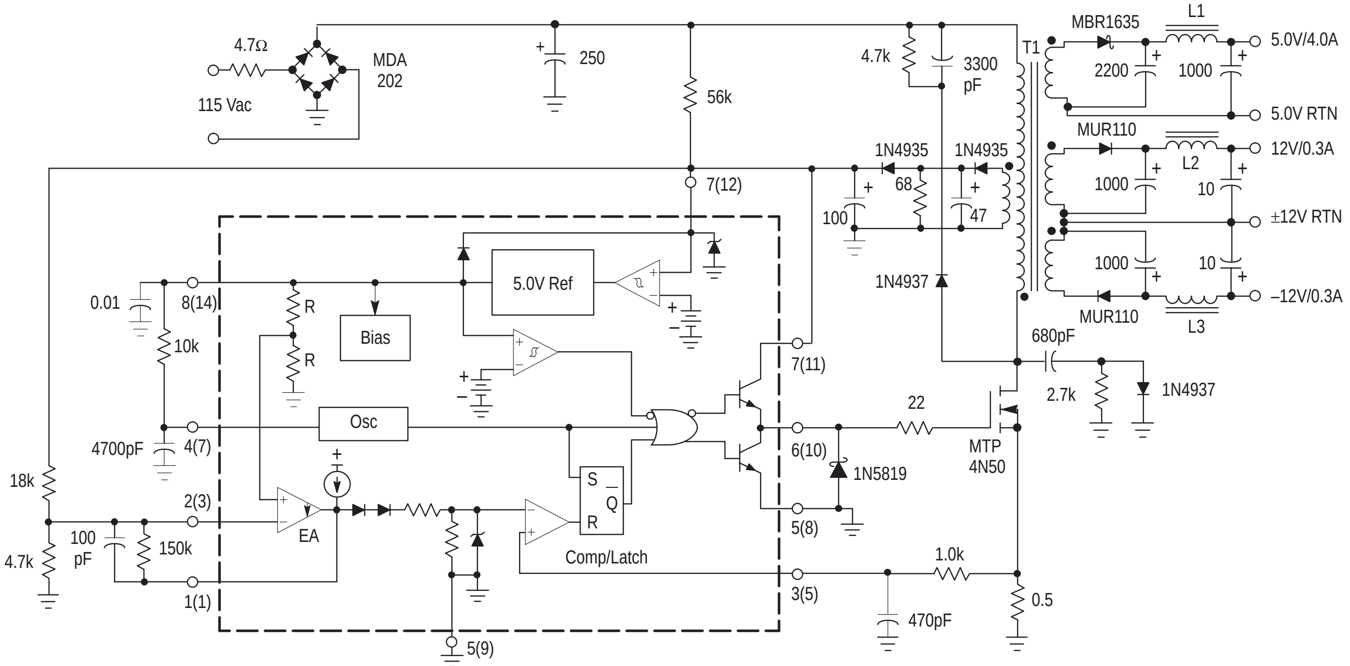
Error Amp compensation circuit for stabilizing current mode boost and flyback topologies operating with continuous inductor current.

Figure 32. Slope Compensation



The buffered oscillator ramp can be resistively summed with either the voltage feedback or current sense inputs to provide slope compensation.

Figure 33. 27 W Off–Line Flyback Regulator



L1 – 15 µH at 5.0 A, Coilcraft Z7156
L2, L3 – 25 µH at 5.0 A, Coilcraft Z7157

Test	Conditions	Results
Line Regulation: 5.0 V ±12 V	V_{in} = 95 to 130 Vac	Δ = 50 mV or ± 0.5% Δ = 24 mV or ± 0.1%
Load Regulation: 5.0 V	V_{in} = 115 Vac, I_{out} = 1.0 A to 4.0 A	Δ = 300 mV or ± 3.0%
±12 V	V_{in} = 115 Vac, I_{out} = 100 mA to 300 mA	Δ = 60 mV or ± 0.25%
Output Ripple: 5.0 V ±12 V	V_{in} = 115 Vac	40 mV_{pp} 80 mV_{pp}
Efficiency	V_{in} = 115 Vac	70%

All outputs are at nominal load currents, unless otherwise noted

T1 – Primary: 45 Turns #26 AWG
Secondary ±12 V: 9 Turns #30 AWG (2 Strands) Bifiliar Wound
Secondary 5.0 V: 4 Turns (six strands) #26 Hexfiliar Wound
Secondary Feedback: 10 Turns #30 AWG (2 strands) Bifiliar Wound
Core: Ferroxcube EC35–3C8
Bobbin: Ferroxcube EC35PCB1
Gap: ≈ 0.10” for a primary inductance of 1.0 mH

MOTOROLA

UC3844, 45
UC2844, 45

HIGH PERFORMANCE CURRENT MODE CONTROLLERS

High Performance Current Mode Controllers

The UC3844, UC3845 series are high performance fixed frequency current mode controllers. They are specifically designed for Off–Line and dc–to–dc converter applications offering the designer a cost effective solution with minimal external components. These integrated circuits feature an oscillator, a temperature compensated reference, high gain error amplifier, current sensing comparator, and a high current totem pole output ideally suited for driving a power MOSFET.

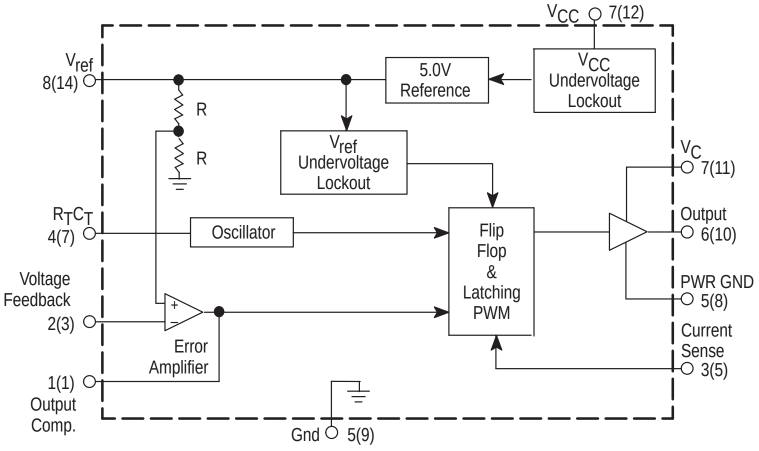
Also included are protective features consisting of input and reference undervoltage lockouts each with hysteresis, cycle–by–cycle current limiting, a latch for single pulse metering, and a flip–flop which blanks the output off every other oscillator cycle, allowing output deadtimes to be programmed for 50% to 70%.

These devices are available in an 8–pin dual–in–line plastic package as well as the 14–pin plastic surface mount (SO–14). The SO–14 package has separate power and ground pins for the totem pole output stage.

The UCX844 has UVLO thresholds of 16 V (on) and 10 V (off), ideally suited for off–line converters. The UCX845 is tailored for lower voltage applications having UVLO thresholds of 8.5 V (on) and 7.6 V (off).

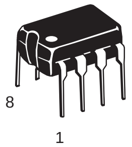
- Current Mode Operation to 500 kHz Output Switching Frequency
- Output Deadtime Adjustable from 50% to 70%
- Automatic Feed Forward Compensation
- Latching PWM for Cycle–By–Cycle Current Limiting
- Internally Trimmed Reference with Undervoltage Lockout
- High Current Totem Pole Output
- Input Undervoltage Lockout with Hysteresis
- Low Startup and Operating Current
- Direct Interface with Motorola SENSEFET Products

Simplified Block Diagram

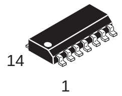


Pin numbers in parenthesis are for the D suffix SO–14 package.

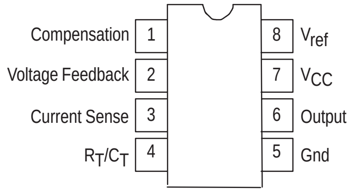
N SUFFIX
PLASTIC PACKAGE
CASE 626



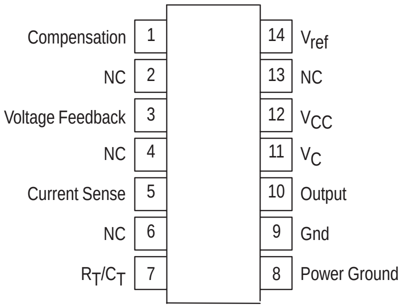
D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO–14)



PIN CONNECTIONS



(Top View)



(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
UC3844D	T_A = 0° to +70°C	SO–14
UC3845D		SO–14
UC3844N		Plastic
UC3845N		Plastic
UC2844D	T_A = – 25° to +85°C	SO–14
UC2845D		SO–14
UC2844N		Plastic
UC2845N		Plastic

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Total Power Supply and Zener Current	$(I_{CC} + I_Z)$	30	mA
Output Current, Source or Sink (Note 1)	I_O	1.0	A
Output Energy (Capacitive Load per Cycle)	W	5.0	μJ
Current Sense and Voltage Feedback Inputs	V_{in}	– 0.3 to + 5.5	V
Error Amp Output Sink Current	I_O	10	mA
Power Dissipation and Thermal Characteristics D Suffix, Plastic Package, Case 751A Maximum Power Dissipation @ T_A = 25°C Thermal Resistance Junction–to–Air N Suffix, Plastic Package, Case 626 Maximum Power Dissipation @ T_A = 25°C Thermal Resistance Junction–to–Air	 P_D $R_{\theta JA}$ P_D $R_{\theta JA}$	 862 145 1.25 100	 mW °C/W W °C/W
Operating Junction Temperature	T_J	+ 150	°C
Operating Ambient Temperature UC3844, UC3845 UC2844, UC2845	T_A	 0 to + 70 – 25 to + 85	°C
Storage Temperature Range	T_{stg}	– 65 to + 150	°C

ELECTRICAL CHARACTERISTICS

(V_{CC} = 15 V, [Note 2], R_T = 10 k, C_T = 3.3 nF, $T_A = T_{low}$ to T_{high} [Note 3], unless otherwise noted.)

Characteristics	Symbol	UC284X			UC384X			Unit
		Min	Typ	Max	Min	Typ	Max	
REFERENCE SECTION								
Reference Output Voltage (I_O = 1.0 mA, T_J = 25°C)	V_{ref}	4.95	5.0	5.05	4.9	5.0	5.1	V
Line Regulation (V_{CC} = 12 V to 25 V)	Reg_{line}	–	2.0	20	–	2.0	20	mV
Load Regulation (I_O = 1.0 mA to 20 mA)	Reg_{load}	–	3.0	25	–	3.0	25	mV
Temperature Stability	T_S	–	0.2	–	–	0.2	–	mV/°C
Total Output Variation over Line, Load, Temperature	V_{ref}	4.9	–	5.1	4.82	–	5.18	V
Output Noise Voltage (f = 10 Hz to kHz, T_J = 25°C)	V_n	–	50	–	–	50	–	μV
Long Term Stability (T_A = 125°C for 1000 Hours)	S	–	5.0	–	–	5.0	–	mV
Output Short Circuit Current	I_{SC}	– 30	– 85	– 180	– 30	– 85	– 180	mA
OSCILLATOR SECTION								
Frequency T_J = 25°C $T_A = T_{low}$ to T_{high}	f_{osc}	 47 46	 52 –	 57 60	 47 46	 52 –	 57 60	kHz
Frequency Change with Voltage (V_{CC} = 12 V to 25 V)	$\Delta f_{osc}/\Delta V$	–	0.2	1.0	–	0.2	1.0	%
Frequency Change with Temperature $T_A = T_{low}$ to T_{high}	$\Delta f_{osc}/\Delta T$	–	5.0	–	–	5.0	–	%
Oscillator Voltage Swing (Peak–to–Peak)	V_{osc}	–	1.6	–	–	1.6	–	V
Discharge Current (V_{osc} = 2.0 V, T_J = 25°C)	I_{dischg}	–	10.8	–	–	10.8	–	mA

NOTES: 1. Maximum Package power dissipation limits must be observed.
2. Adjust V_{CC} above the Startup threshold before setting to 15 V.
3. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible

T_{low} = 0°C for UC3844, UC3845
–25°C for UC2844, UC2845

T_{high} = +70°C for UC3844, UC3845
+85°C for UC2844, UC2845

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V, [Note 2], R_T = 10 k, C_T = 3.3 nF, $T_A = T_{low}$ to T_{high} [Note 3], unless otherwise noted,)

Characteristics	Symbol	UC284X			UC384X			Unit
		Min	Typ	Max	Min	Typ	Max	
ERROR AMPLIFIER SECTION								
Voltage Feedback Input (V_O = 2.5 V)	V_{FB}	2.45	2.5	2.55	2.42	2.5	2.58	V
Input Bias Current (V_{FB} = 2.7 V)	I_{IB}	–	–0.1	–1.0	–	–0.1	–2.0	µA
Open Loop Voltage Gain (V_O = 2.0 V to 4.0 V)	A_{VOL}	65	90	–	65	90	–	dB
Unity Gain Bandwidth (T_J = 25°C)	BW	0.7	1.0	–	0.7	1.0	–	MHz
Power Supply Rejection Ratio (V_{CC} = 12 V to 25 V)	PSRR	60	70	–	60	70	–	dB
Output Current Sink (V_O = 1.1 V, V_{FB} = 2.7 V) Source (V_O = 5.0 V, V_{FB} = 2.3 V)	 I_{Sink} I_{Source}	 2.0 –0.5	 12 –1.0	 – –	 2.0 –0.5	 12 –1.0	 – –	mA
Output Voltage Swing High State (R_L = 15 k to ground, V_{FB} = 2.3 V) Low State (R_L = 15 k to V_{ref}, V_{FB} = 2.7 V)	 V_{OH} V_{OL}	 5.0 –	 6.2 0.8	 – 1.1	 5.0 –	 6.2 0.8	 – 1.1	V
CURRENT SENSE SECTION								
Current Sense Input Voltage Gain (Notes 4 & 5)	A_V	2.85	3.0	3.15	2.85	3.0	3.15	V/V
Maximum Current Sense Input Threshold (Note 4)	V_{th}	0.9	1.0	1.1	0.9	1.0	1.1	V
Power Supply Rejection Ratio V_{CC} = 12 V to 25 V (Note 4)	PSRR	 –	 70	 –	 –	 70	 –	dB
Input Bias Current	I_{IB}	–	–2.0	–10	–	–2.0	–10	µA
Propagation Delay (Current Sense Input to Output)	$t_{PLH(IN/OUT)}$	–	150	300	–	150	300	ns
OUTPUT SECTION								
Output Voltage Low State (I_{Sink} = 20 mA) (I_{Sink} = 200 mA) High State (I_{Sink} = 20 mA) (I_{Sink} = 200 mA)	 V_{OL} V_{OH} 	 – – 12 12	 0.1 1.6 13.5 13.4	 0.4 2.2 – –	 – – 13 12	 0.1 1.6 13.5 13.4	 0.4 2.2 – –	V
Output Voltage with UVLO Activated V_{CC} = 6.0 V, I_{Sink} = 1.0 mA	$V_{OL(UVLO)}$	 –	 0.1	 1.1	 –	 0.1	 1.1	V
Output Voltage Rise Time (C_L = 1.0 nF, T_J = 25°C)	t_r	–	50	150	–	50	150	ns
Output Voltage Fall Time (C_L = 1.0 nF, T_J = 25°C)	t_f	–	50	150	–	50	150	ns
UNDERVOLTAGE LOCKOUT SECTION								
Startup Threshold UCX844 UCX845	V_{th}	 15 7.8	 16 8.4	 17 9.0	 14.5 7.8	 16 8.4	 17.5 9.0	V
Minimum Operating Voltage After Turn–On UCX844 UCX845	$V_{CC(min)}$	 9.0 7.0	 10 7.6	 11 8.2	 8.5 7.0	 10 7.6	 11.5 8.2	V
PWM SECTION								
Duty Cycle Maximum Minimum	 DC_{max} DC_{min}	 46 –	 48 –	 50 0	 47 –	 48 –	 50 0	%
TOTAL DEVICE								
Power Supply Current (Note 2) Startup: (V_{CC} = 6.5 V for UCX845A, 14 V for UCX844) Operating	I_{CC}	 – –	 0.5 12	 1.0 17	 – –	 0.5 12	 1.0 17	mA
Power Supply Zener Voltage (I_{CC} = 25 mA)	V_Z	30	36	–	30	36	–	V

NOTES: 2. Adjust V_{CC} above the Startup threshold before setting to 15 V.

3. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible

T_{low} = 0°C for UC3844, UC3845 T_{high} = +70°C for UC3844, UC3845
–25°C for UC2844, UC2845 +85°C for UC2844, UC2845

4. This parameter is measured at the latch trip point with V_{FB} = 0 V.

5. Comparator gain is defined as: $A_V \dfrac{\Delta V \text{ Output Compensation}}{\Delta V \text{ Current Sense Input}}$

Figure 1. Timing Resistor versus Oscillator Frequency

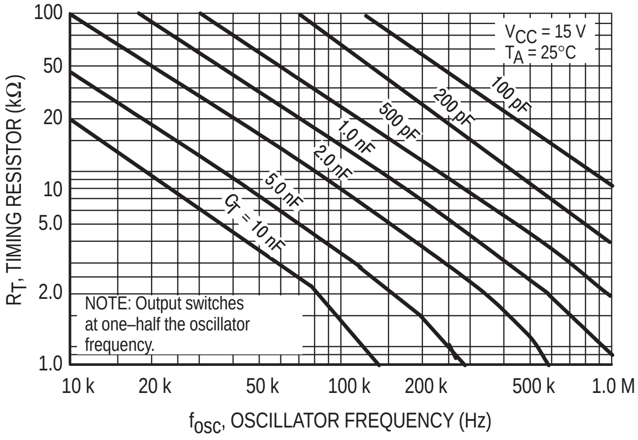


Figure 2. Output Deadtime versus Oscillator Frequency

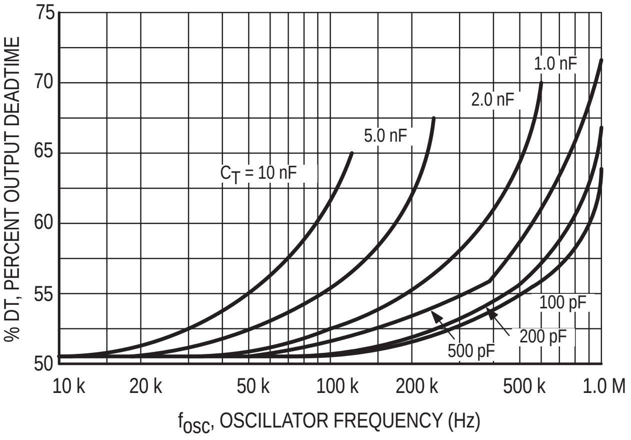


Figure 3. Error Amp Small Signal Transient Response

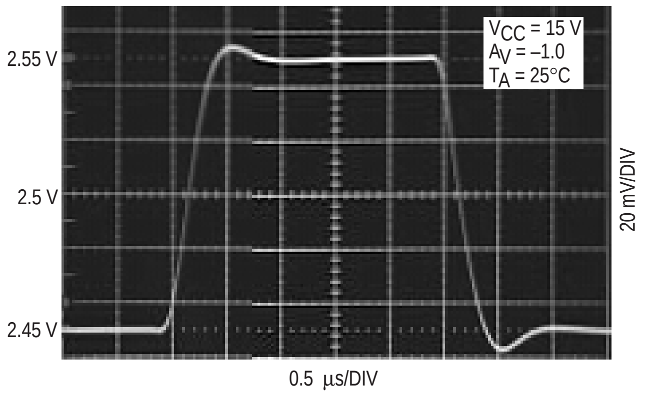


Figure 4. Error Amp Large Signal Transient Response

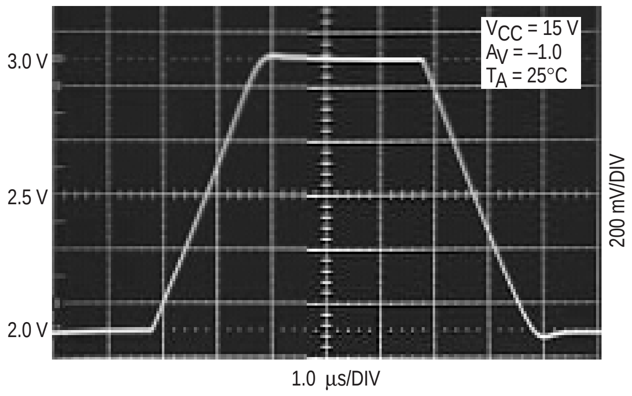


Figure 5. Error Amp Open Loop Gain and Phase versus Frequency

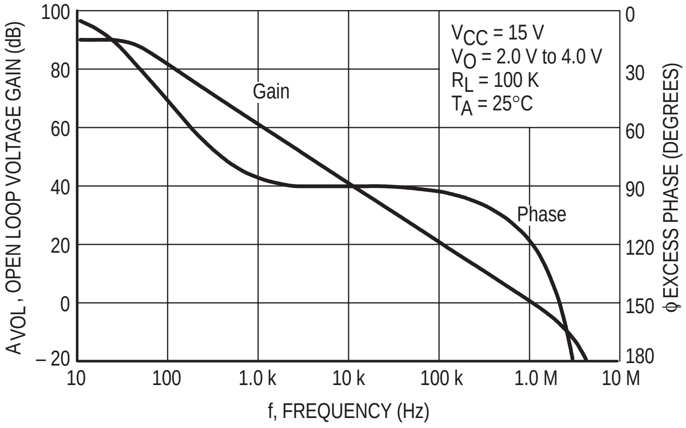
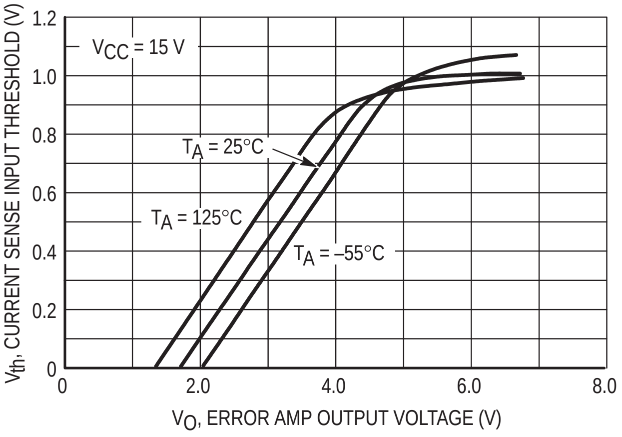


Figure 6. Current Sense Input Threshold versus Error Amp Output Voltage



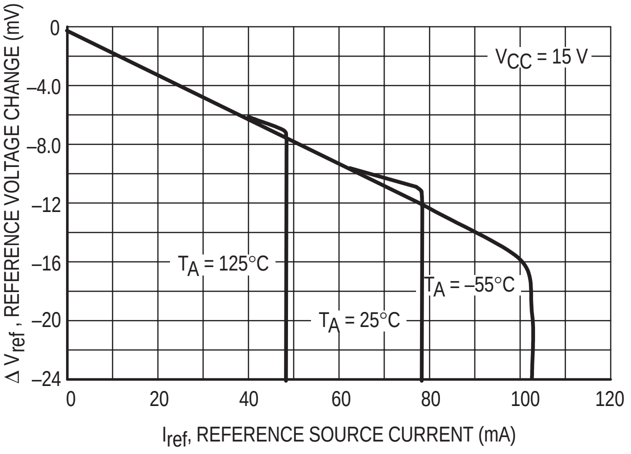


Figure 7. Reference Voltage Change versus Source Current

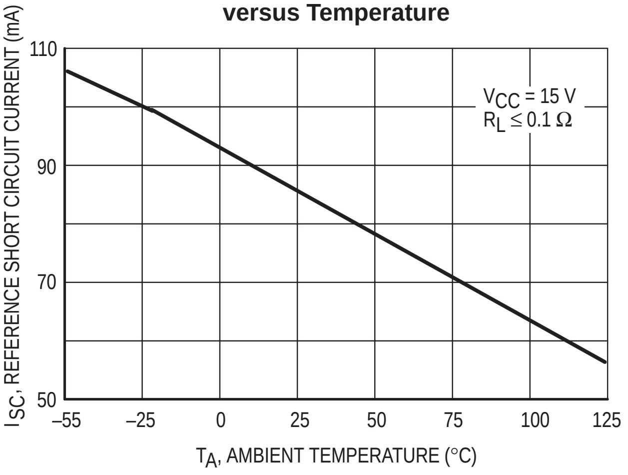


Figure 8. Reference Short Circuit Current versus Temperature

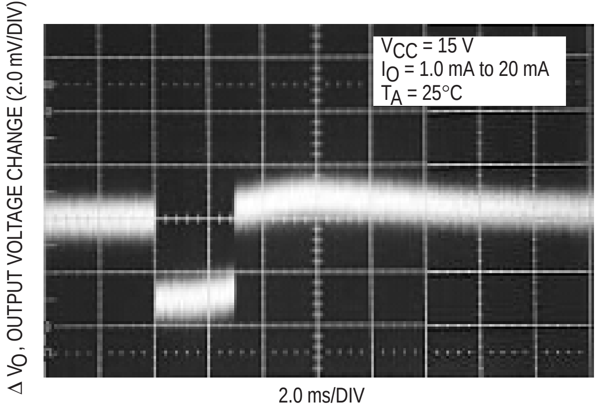


Figure 9. Reference Load Regulation

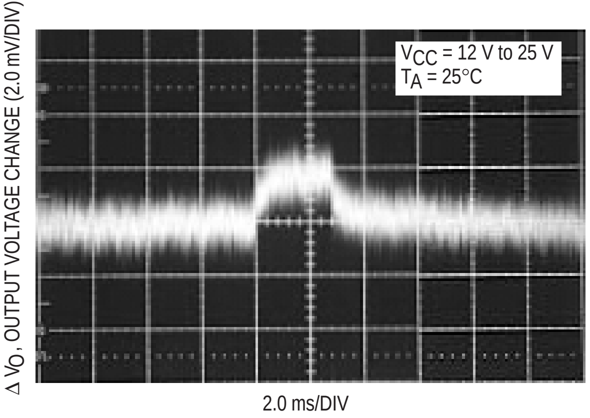


Figure 10. Reference Line Regulation

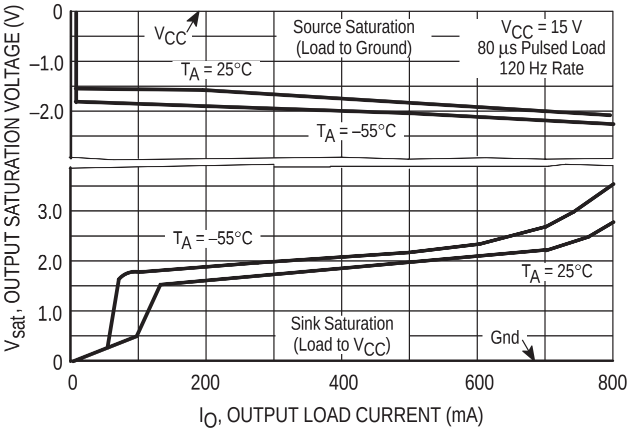


Figure 11. Output Saturation Voltage versus Load Current

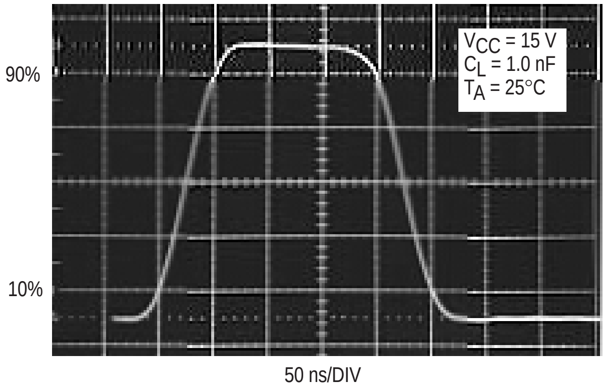


Figure 12. Output Waveform

Figure 13. Output Cross Conduction

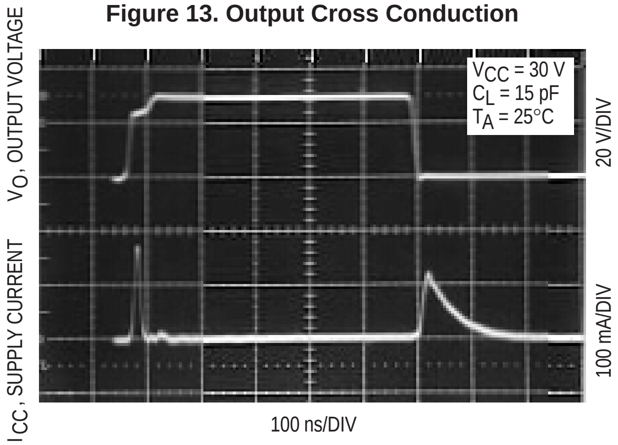
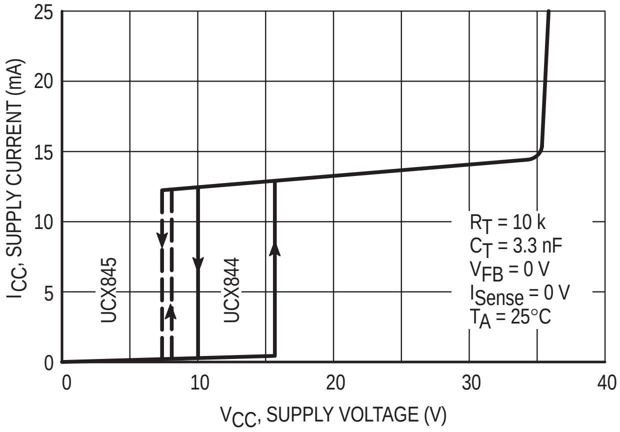


Figure 14. Supply Current versus Supply Voltage



PIN FUNCTION DESCRIPTION

Pin		Function	Description
8–Pin	14–Pin		
1	1	Compensation	This pin is Error Amplifier output and is made available for loop compensation.
2	3	Voltage Feedback	This is the inverting input of the Error Amplifier. It is normally connected to the switching power supply output through a resistor divider.
3	5	Current Sense	A voltage proportional to inductor current is connected to this input. The PWM uses this information to terminate the output switch conduction.
4	7	R_T/C_T	The Oscillator frequency and maximum Output duty cycle are programmed by connecting resistor R_T to V_{ref} and capacitor C_T to ground. Operation to 1.0 MHz is possible.
5	–	Gnd	This pin is combined control circuitry and power ground (8–pin package only).
6	10	Output	This output directly drives the gate of a power MOSFET. Peak currents up to 1.0 A are sourced and sunk by this pin. The output switches at one–half the oscillator frequency.
7	12	V_{CC}	This pin is the positive supply of the control IC.
8	14	V_{ref}	This is the reference output. It provides charging current for capacitor C_T through resistor R_T.
–	8	Power Ground	This pin is a separate power ground return (14–pin package only) that is connected back to the power source. It is used to reduce the effects of switching transient noise on the control circuitry.
–	11	V_C	The Output high state (V_{OH}) is set by the voltage applied to this pin (14–pin package only). With a separate power source connection, it can reduce the effects of switching transient noise on the control circuitry.
–	9	Gnd	This pin is the control circuitry ground return (14–pin package only) and is connected to back to the power source ground.
–	2,4,6,13	NC	No connection (14–pin package only). These pins are not internally connected.

OPERATING DESCRIPTION

The UC3844, UC3845 series are high performance, fixed frequency, current mode controllers. They are specifically designed for Off–Line and dc–to–dc converter applications offering the designer a cost effective solution with minimal external components. A representative block diagram is shown in Figure 15.

Oscillator

The oscillator frequency is programmed by the values selected for the timing components R_T and C_T. Capacitor C_T is charged from the 5.0 V reference through resistor R_T to approximately 2.8 V and discharged to 1.2 V by an internal current sink. During the discharge of C_T, the oscillator generates an internal blanking pulse that holds the center input of the NOR gate high. This causes the Output to be in a low state, thus producing a controlled amount of output deadtime. An internal flip–flop has been incorporated in the UCX844/5 which blanks the output off every other clock cycle by holding one of the inputs of the NOR gate high. This in combination with the C_T discharge period yields output deadtimes programmable from 50% to 70%. Figure 1 shows R_T versus Oscillator Frequency and figure 2, Output Deadtime versus Frequency, both for given values of C_T. Note that many values of R_T and C_T will give the same oscillator frequency but only one combination will yield a specific output deadtime at a given frequency.

In many noise sensitive applications it may be desirable to frequency–lock the converter to an external system clock. This can be accomplished by applying a clock signal to the circuit shown in Figure 17. For reliable locking, the free–running oscillator frequency should be set about 10% less than the clock frequency. A method for multi unit synchronization is shown in Figure 18. By tailoring the clock waveform, accurate Output duty cycle clamping can be achieved to realize output deadtimes of greater than 70%

Error Amplifier

A fully compensated Error Amplifier with access to the inverting input and output is provided. It features a typical dc voltage gain of 90 dB, and a unity gain bandwidth of 1.0 MHz with 57 degrees of phase margin (Figure 5). The noninverting input is internally biased at 2.5 V and is not pinned out. The converter output voltage is typically divided down and monitored by the inverting input. The maximum input bias current is –2.0 µA which can cause an output voltage error that is equal to the product of the input bias current and the equivalent input divider source resistance.

The Error Amp Output (Pin 1) is provide for external loop compensation (Figure 28). The output voltage is offset by two diode drops (≈ 1.4 V) and divided by three before it connects to the inverting input of the Current Sense Comparator. This guarantees that no drive pulses appear at the Output (Pin 6) when Pin 1 is at its lowest state (V_{OL}). This occurs when the power supply is operating and the load is removed, or at the beginning of a soft–start interval (Figures 20, 21). The Error Amp minimum feedback resistance is limited by the amplifier's source current (0.5 mA) and the required output voltage (V_{OH}) to reach the comparator's 1.0 V clamp level:

$$R_{f(min)} \approx \frac{3.0\ (1.0\ V) + 1.4\ V}{0.5\ mA} = 8800\ \Omega$$

Current Sense Comparator and PWM Latch

The UC3844, UC3845 operate as a current mode controller, whereby output switch conduction is initiated by the oscillator and terminated when the peak inductor current reaches the threshold level established by the Error Amplifier Output/Compensation (Pin1). Thus the error signal controls the inductor current on a cycle–by–cycle basis. The current Sense Comparator PWM Latch configuration used ensures that only a single pulse appears at the Output during any given oscillator cycle. The inductor current is converted to a voltage by inserting the ground referenced sense resistor R_S in series with the source of output switch Q1. This voltage is monitored by the Current Sense Input (Pin 3) and compared a level derived from the Error Amp Output. The peak inductor current under normal operating conditions is controlled by the voltage at pin 1 where:

$$I_{pk} = \frac{V_{(Pin\ 1)} - 1.4\ V}{3\ R_S}$$

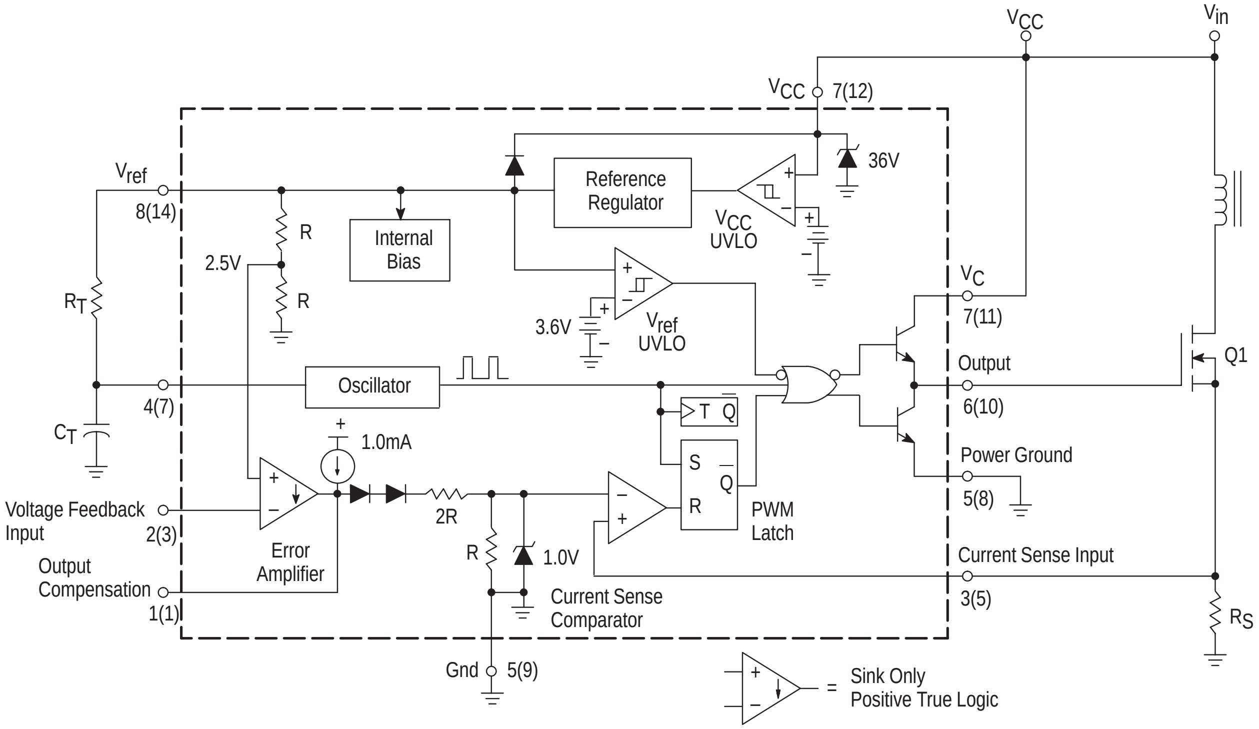
Abnormal operating conditions occur when the power supply output is overloaded or if output voltage sensing is lost. Under these conditions, the Current Sense Comparator threshold will be internally clamped to 1.0 V. Therefore the maximum peak switch current is:

$$I_{pk(max)} = \frac{1.0\ V}{R_S}$$

When designing a high power switching regulator it becomes desirable to reduce the internal clamp voltage in order to keep the power dissipation of R_S to a reasonable level. A simple method to adjust this voltage is shown in Figure 19. The two external diodes are used to compensate the internal diodes yielding a constant clamp voltage over temperature. Erratic operation due to noise pickup can result if there is an excessive reduction of the $I_{pk(max)}$ clamp voltage.

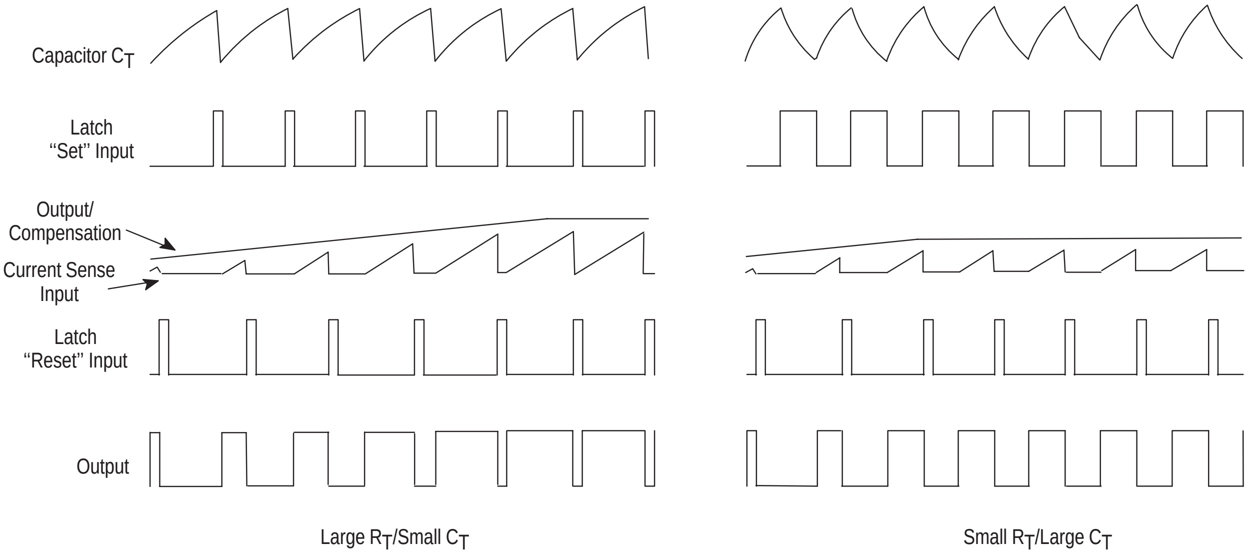
A narrow spike on the leading edge of the current waveform can usually be observed and may cause the power supply to exhibit an instability when the output is lightly loaded. This spike is due to the power transformer interwinding capacitance and output rectifier recovery time. The addition of an RC filter on the Current Sense Input with a time constant that approximates the spike duration will usually eliminate the instability; refer to Figure 23.

Figure 15. Representative Block Diagram



Pin numbers in parenthesis are for the D suffix SO–14 package.

Figure 16. Timing Diagram



Undervoltage Lockout

Two undervoltage lockout comparators have been incorporated to guarantee that the IC is fully functional before the output stage is enabled. The positive power supply terminal (V_{CC} and the reference output (V_{ref}) are each monitored by separate comparators. Each has built–in hysteresis to prevent erratic output behavior as their respective thresholds are crossed. The V_{CC} comparator upper and lower thresholds are 16 V/10 V for the UCX844, and 8.4 V/7.6 V for the UCX845. The V_{ref} comparator upper and lower thresholds are 3.6 V/3/4 V. The large hysteresis and low startup current of the UCX844 makes it ideally suited in off–line converter applications where efficient bootstrap startup techniques later required (Figure 29). The UCX845 is intended for lower voltage dc–to–dc converter applications. A 36 V zener is connected as a shunt regulator from V_{CC} to ground. Its purpose is to protect the IC from excessive voltage that can occur during system startup. The minimum operating voltage for the UCX844 is 11 V and 8.2 V for the UCX845.

Output

These devices contain a single totem pole output stage that was specifically designed for direct drive of power MOSFETs. It is capable of up to ± 1.0 A peak drive current and has a typical rise and fall time of 50 ns with a 1.0 nF load. Additional internal circuitry has been added to keep the Output in a sinking mode whenever and undervoltage lockout is active. This characteristic eliminates the need for an external pull–down resistor.

The SO–14 surface mount package provides separate pins for V_C (output supply) and Power Ground. Proper implementation will significantly reduce the level of switching transient noise imposed on the control circuitry. This becomes particularly useful when reducing the $I_{pk(max)}$ clamp level. The separate V_C supply input allows the designer added flexibility in tailoring the drive voltage independent of V_{CC}. A zener clamp is typically connected to this input when driving power MOSFETs in systems where V_{CC} is greater the 20 V. Figure 22 shows proper power and control ground connections in a current sensing power MOSFET application.

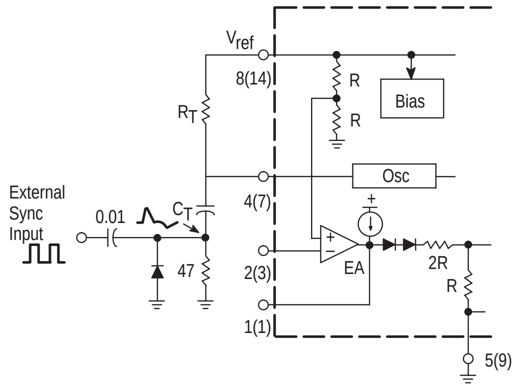
Reference

The 5.0 V bandgap reference is trimmed to ± 1.0% tolerance at T_J = 25°C on the UC284X, and ± 2.0% on the UC384X. Its primary purpose is to supply charging current to the oscillator timing capacitor. The reference has short circuit protection and is capable of providing in excess of 20 mA for powering additional control system circuitry.

Design Considerations

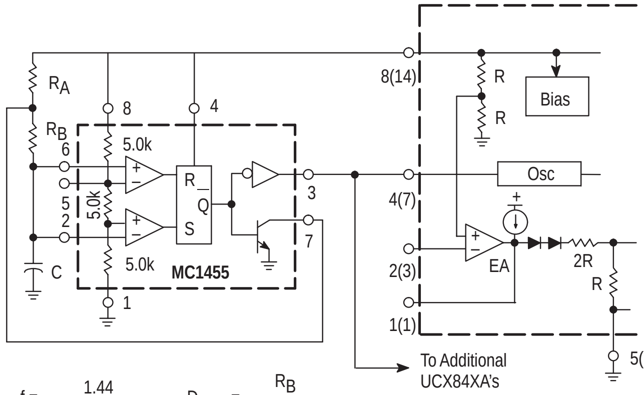
Do not attempt to construct the converter on wire–wrap or plug–in prototype boards. High frequency circuit layout techniques are imperative to prevent pulsewidth jitter. This is usually caused by excessive noise pick–up imposed on the Current Sense or Voltage Feedback inputs. Noise immunity can be improved by lowering circuit impedances at these points. The printed circuit layout should contain a ground plane with low–current signal and high–current switch and output grounds returning on separate paths back to the input filter capacitor. Ceramic bypass capacitors (0.1 µF) connected directly to V_{CC}, V_C, and V_{ref} may be required depending upon circuit layout. This provides a low impedance path for filtering the high frequency noise. All high current loops should be kept as short as possible using heavy copper runs to minimize radiated EMI. The Error Amp compensation circuitry and the converter output voltage divider should be located close to the IC and as far as possible from the power switch and other noise generating components.

Figure 17. External Clock Synchronization



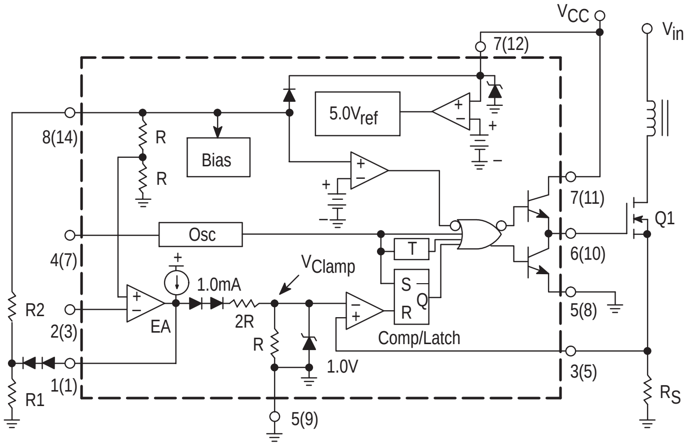
The diode clamp is required if the Sync amplitude is large enough to cause the bottom side of CT to go more than 300 mV below ground.

Figure 18. External Duty Cycle Clamp and Multi–Unit Synchronization



$f = \frac{1.44}{(R_A + 2R_B)C}$ $D_{max} = \frac{R_B}{R_A + 2R_B}$

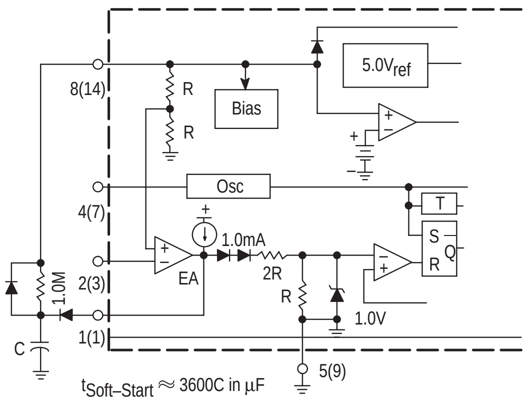
Figure 19. Adjustable Reduction of Clamp Level



$$V_{Clamp}\ \frac{1.67}{\left(\frac{R_2}{R_1}+1\right)} + 0.33 \times 10^{-3}\left(\frac{R_1\ R_2}{R_1+R_2}\right) \qquad I_{pk(max)} \approx \frac{V_{Clamp}}{R_S}$$

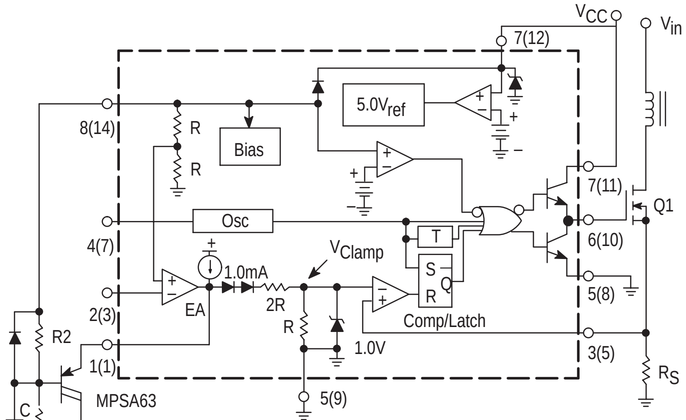
Where: $0 \le V_{Clamp} \le 1.0$ V

Figure 20. Soft–Start Circuit



$t_{Soft-Start} \approx 3600C$ in µF

Figure 21. Adjustable Buffered Reduction of Clamp Level with Soft–Start

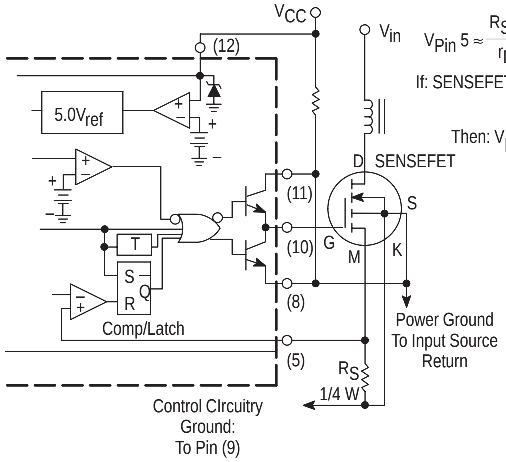


$$V_{Clamp}\ \frac{1.67}{\left(\frac{R_2}{R_1}+1\right)} + 0.33 \times 10^{-3}\ \frac{R_1\ R_2}{R_1+R_2}$$

$I_{pk(max)} \approx \frac{V_{Clamp}}{R_S}$ Where: $0 \le V_{Clamp} \le 1.0$ V

$$t_{Softstart} = -\ln\left[1 - \frac{V_C}{3V_{Clamp}}\right] C\ \frac{R_1\ R_2}{R_1 + R_2}$$

Figure 22. Current Sensing Power MOSFET



$$V_{Pin\ 5} \approx \frac{R_S\ I_{pk}\ r_{DS(on)}}{r_{DM(on)} + R_S}$$

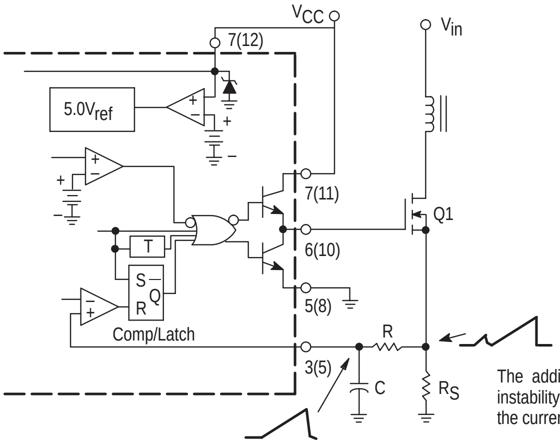
If: SENSEFET = MTP10N10M

$R_S = 200$

Then: $V_{pin\ 5} = 0.075\ I_{pk}$

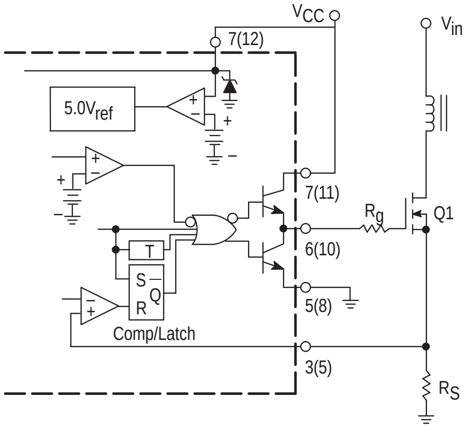
Virtually lossless current sensing can be achieved with the implement of a SENSEFET power switch. For proper operation during over current conditions, a reduction of the $I_{pk(max)}$ clamp level must be implemented. Refer to Figures 19 and 21.

Figure 23. Current Waveform Spike Suppression



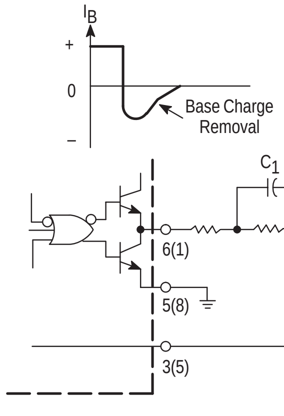
The addition of the RC filter will eliminate instability caused by the leading edge spike on the current waveform.

Figure 24. MOSFET Parasitic Oscillations



Series gate resistor R_g will damp any high frequency parasitic oscillations caused by the MOSFET input capacitance and any series wiring inductance in the gate–source circuit.

Figure 25. Bipolar Transistor Drive



The totem–pole output can furnish negative base current for enhanced transistor turn–off, with the addition of capacitor C_1.

Figure 26. Isolated MOSFET Drive

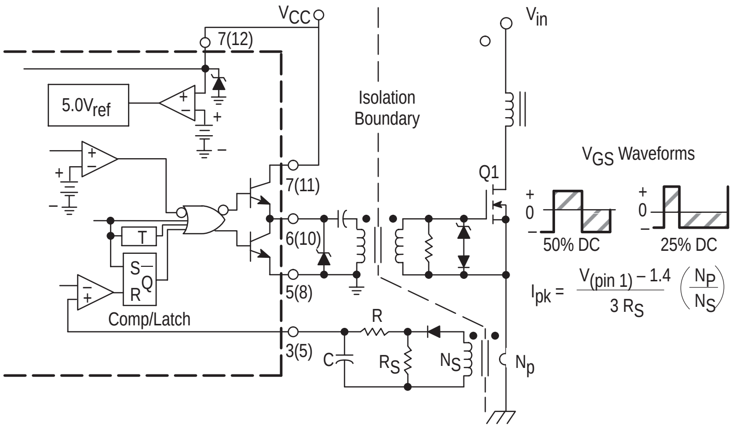
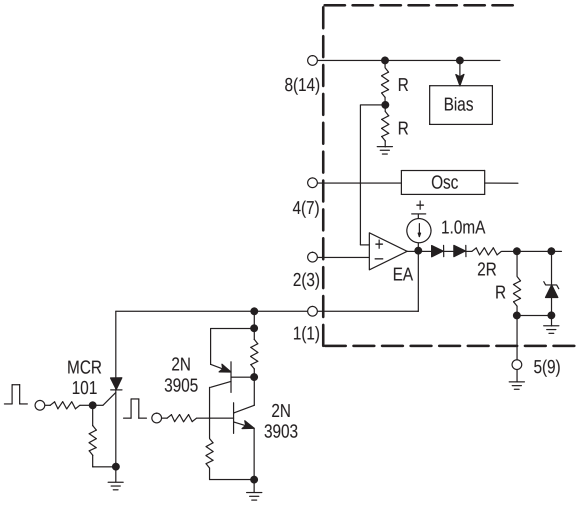
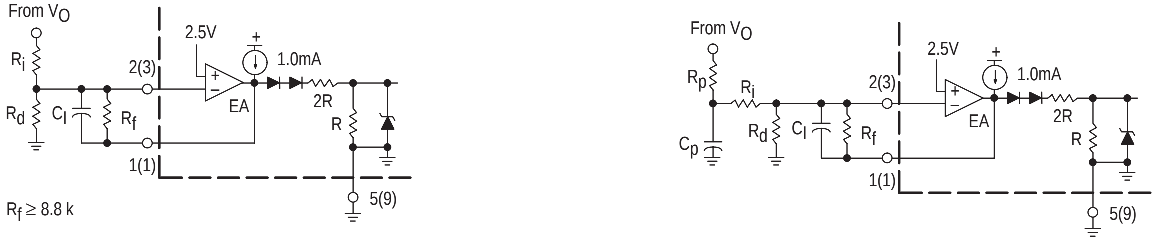


Figure 27. Latched Shutdown



The MCR101 SCR must be selected for a holding of less than 0.5 mA at $T_{A(min)}$. The simple two transistor circuit can be used in place of the SCR as shown. All resistors are 10 k.

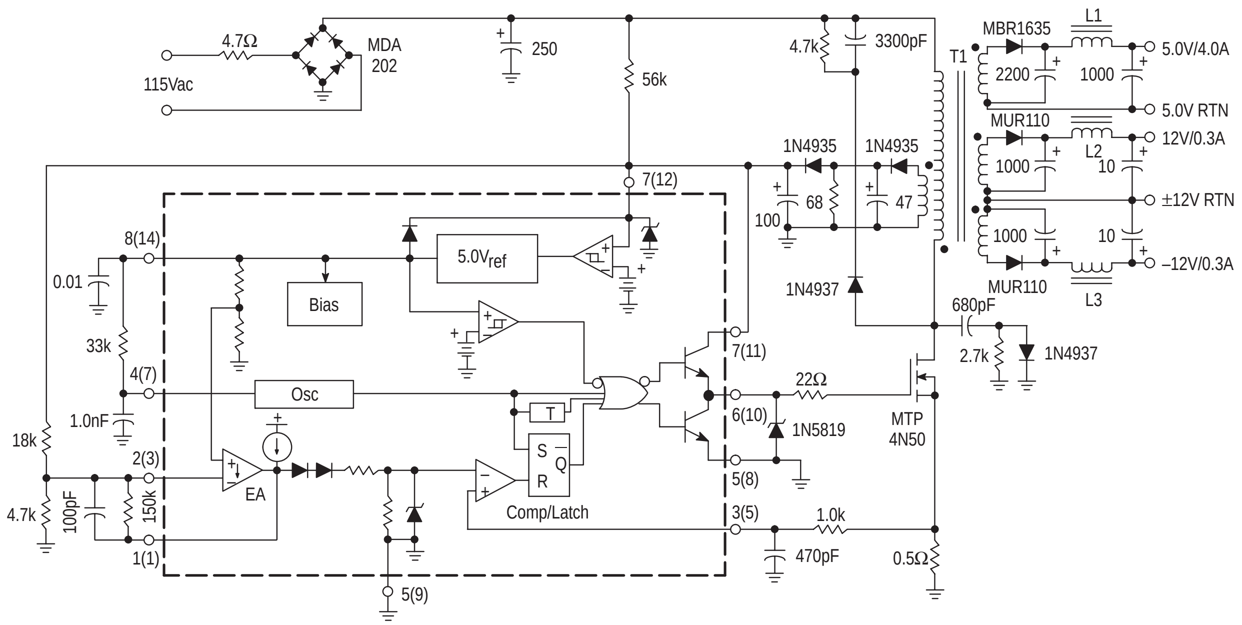
Figure 28. Error Amplifier Compensation



Error Amp compensation circuit for stabilizing any current–mode topology except for boost and flyback converters operating with continuous inductor current.

Error Amp compensation circuit for stabilizing current–mode boost and flyback topologies operating with continuous inductor current.

Figure 29. 27 Watt Off–Line Flyback Regulator



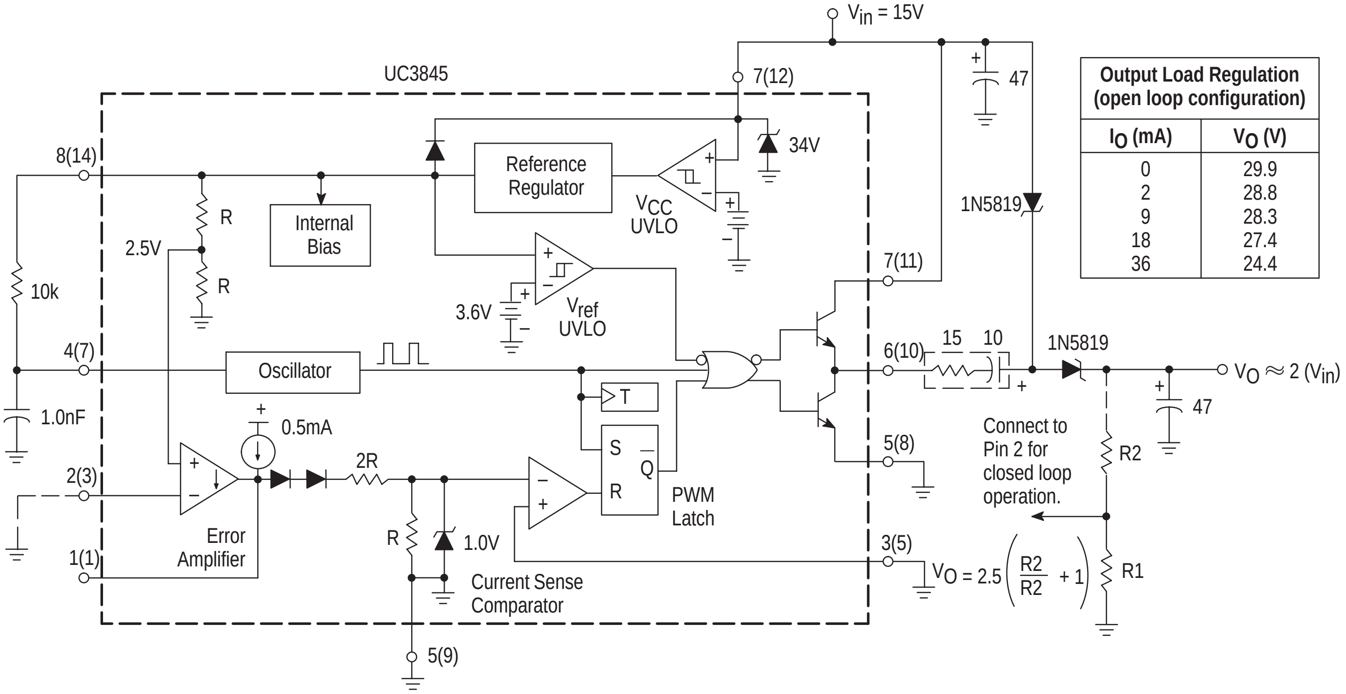
T1 – Primary: 45 Turns # 26 AWG
Secondary ± 12 V: 9 Turns # 30 AWG
(2 strands) Bifiliar Wound
Secondary 5.0 V: 4 Turns (six strands)
#26 Hexfiliar Wound
Secondary Feedback: 10 Turns #30 AWG
(2 strands) Bifiliar Wound
Core: Ferroxcube EC35–3C8
Bobbin: Ferroxcube EC35PCB1
Gap ≈ 0.01" for a primary inductance of 1.0 mH

L1 – 15 µH at 5.0 A, Coilcraft Z7156.
L2, L3 – 25 µH at 1.0 A, Coilcraft Z7157.

Test		Conditions	Results
Line Regulation:	5.0 V ± 12 V	V_{in} = 95 Vac to 130 Vac	Δ = 50 mV or ± 0.5% Δ = 24 mV or ± 0.1%
Load Regulation:	5.0 V ± 12 V	V_{in} = 115 Vac, I_{out} = 1.0 A to 4.0 A V_{in} = 115 Vac, I_{out} = 100 mA to 300 mA	Δ = 300 mV or ± 3.0% Δ = 60 mV or ± 0.25%
Output Ripple:	5.0 V ± 12 V	V_{in} = 115 Vac	40 mV_{pp} 80 mV_{pp}
Efficiency		V_{in} = 115 Vac	70%

All outputs are at nominal load currents, unless otherwise noted.

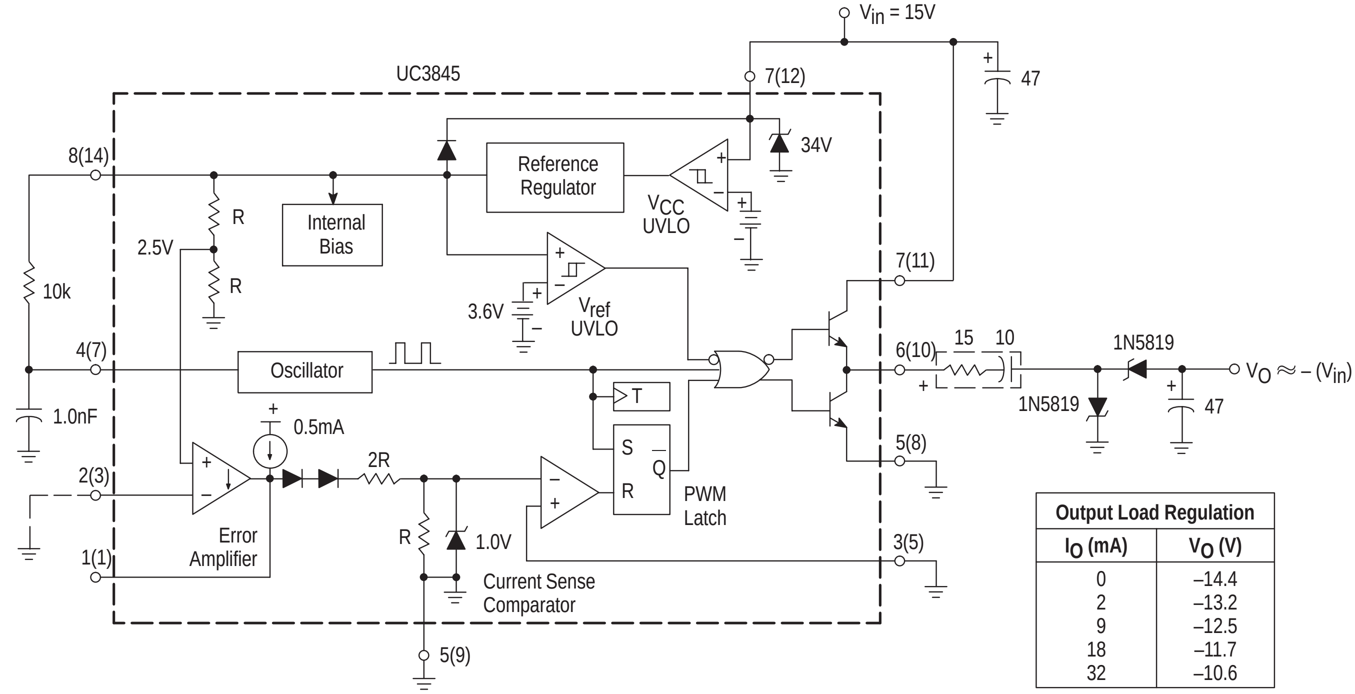
Figure 30. Step–Up Charge Pump Converter



Output Load Regulation (open loop configuration)	
I_O (mA)	V_O (V)
0	29.9
2	28.8
9	28.3
18	27.4
36	24.4

The capacitor's equivalent series resistance must limit the Drive Output current to 1.0 A. An additional series resistor may be required when using tantalum or other low ESR capacitors. The converter's output can provide excellent line and load regulation by connecting the R2/R1 resistor divider as shown.

Figure 31. Voltage–Inverting Charge Pump Converter



Output Load Regulation	
I_O (mA)	V_O (V)
0	–14.4
2	–13.2
9	–12.5
18	–11.7
32	–10.6

The capacitor's equivalent series resistance must limit the Drive Output current to 1.0 A.
An additional series resistor may be required when using tantalum or other low ESR capacitors.

MOTOROLA

UC3844B, 45B
UC2844B, 45B

High Performance Current Mode Controllers

The UC3844B, UC3845B series are high performance fixed frequency current mode controllers. They are specifically designed for Off–Line and dc–to–dc converter applications offering the designer a cost–effective solution with minimal external components. These integrated circuits feature an oscillator, a temperature compensated reference, high gain error amplifier, current sensing comparator, and a high current totem pole output ideally suited for driving a power MOSFET.

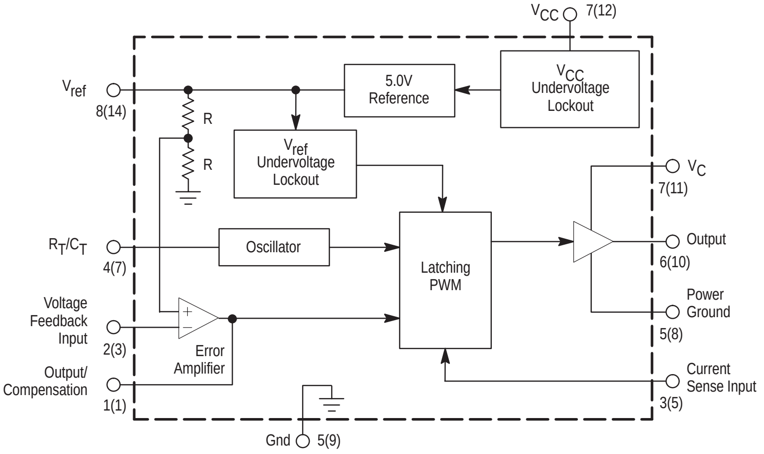
Also included are protective features consisting of input and reference undervoltage lockouts each with hysteresis, cycle–by–cycle current limiting, a latch for single pulse metering, and a flip–flop which blanks the output off every other oscillator cycle, allowing output deadtimes to be programmed from 50% to 70%.

These devices are available in an 8–pin dual–in–line and surface mount (SO–8) plastic package as well as the 14–pin plastic surface mount (SO–14). The SO–14 package has separate power and ground pins for the totem pole output stage.

The UCX844B has UVLO thresholds of 16 V (on) and 10 V (off), ideally suited for off–line converters. The UCX845B is tailored for lower voltage applications having UVLO thresholds of 8.5 V (on) and 7.6 V (off).

- Trimmed Oscillator for Precise Frequency Control
- Oscillator Frequency Guaranteed at 250 kHz
- Current Mode Operation to 500 kHz Output Switching Frequency
- Output Deadtime Adjustable from 50% to 70%
- Automatic Feed Forward Compensation
- Latching PWM for Cycle–By–Cycle Current Limiting
- Internally Trimmed Reference with Undervoltage Lockout
- High Current Totem Pole Output
- Undervoltage Lockout with Hysteresis
- Low Startup and Operating Current

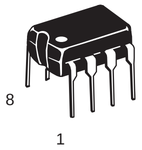
Simplified Block Diagram



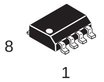
Pin numbers in parenthesis are for the D suffix SO–14 package.

HIGH PERFORMANCE CURRENT MODE CONTROLLERS

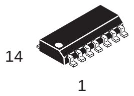
N SUFFIX
PLASTIC PACKAGE
CASE 626



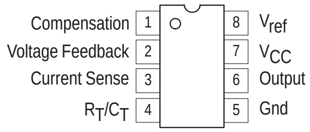
D1 SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)



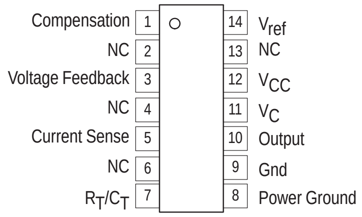
D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO–14)



PIN CONNECTIONS



(Top View)



(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
UC384XBD	T_A = 0° to + 70°C	SO–14
UC384XBD1		SO–8
UC384XBN		Plastic
UC284XBD	T_A = – 25° to + 85°C	SO–14
UC284XBD1		SO–8
UC284XBN		Plastic
UC384XBVD	T_A = – 40° to +105°C	SO–14
UC384XBVD1		SO–8
UC384XBVN		Plastic

X indicates either a 4 or 5 to define specific device part numbers.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Total Power Supply and Zener Current	(I_{CC} + I_Z)	30	mA
Output Current, Source or Sink (Note 1)	I_O	1.0	A
Output Energy (Capacitive Load per Cycle)	W	5.0	µJ
Current Sense and Voltage Feedback Inputs	V_{in}	– 0.3 to + 5.5	V
Error Amp Output Sink Current	I_O	10	mA
Power Dissipation and Thermal Characteristics			
D Suffix, Plastic Package, SO–14 Case 751A			
Maximum Power Dissipation @ T_A = 25°C	P_D	862	mW
Thermal Resistance, Junction–to–Air	$R_{\theta JA}$	145	°C/W
D1 Suffix, Plastic Package, SO–8 Case 751			
Maximum Power Dissipation @ T_A = 25°C	P_D	702	mW
Thermal Resistance, Junction–to–Air	$R_{\theta JA}$	178	°C/W
N Suffix, Plastic Package, Case 626			
Maximum Power Dissipation @ T_A = 25°C	P_D	1.25	W
Thermal Resistance, Junction–to–Air	$R_{\theta JA}$	100	°C/W
Operating Junction Temperature	T_J	+150	°C
Operating Ambient Temperature	T_A		°C
UC3844B, UC3845B		0 to + 70	
UC2844B, UC2845B		– 25 to + 85	
Storage Temperature Range	T_{stg}	– 65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V [Note 2], R_T = 10 k, C_T = 3.3 nF. For typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies [Note 3], unless otherwise noted.)

		UC284XB			UC384XB, XBV			
Characteristic	Symbol	Min	Typ	Max	Min	Typ	Max	Unit
REFERENCE SECTION								
Reference Output Voltage (I_O = 1.0 mA, T_J = 25°C)	V_{ref}	4.95	5.0	5.05	4.9	5.0	5.1	V
Line Regulation (V_{CC} = 12 V to 25 V)	Reg_{line}	–	2.0	20	–	2.0	20	mV
Load Regulation (I_O = 1.0 mA to 20 mA)	Reg_{load}	–	3.0	25	–	3.0	25	mV
Temperature Stability	T_S	–	0.2	–	–	0.2	–	mV/°C
Total Output Variation over Line, Load, and Temperature	V_{ref}	4.9	–	5.1	4.82	–	5.18	V
Output Noise Voltage (f = 10 Hz to 10 kHz, T_J = 25°C)	V_n	–	50	–	–	50	–	µV
Long Term Stability (T_A = 125°C for 1000 Hours)	S	–	5.0	–	–	5.0	–	mV
Output Short Circuit Current	I_{SC}	– 30	– 85	–180	– 30	– 85	–180	mA
OSCILLATOR SECTION								
Frequency	f_{OSC}							kHz
T_J = 25°C		49	52	55	49	52	55	
T_A = T_{low} to T_{high}		48	–	56	48	–	56	
T_J = 25°C (R_T = 6.2 k, C_T = 1.0 nF)		225	250	275	225	250	275	
Frequency Change with Voltage (V_{CC} = 12 V to 25 V)	$\Delta f_{OSC}/\Delta V$	–	0.2	1.0	–	0.2	1.0	%
Frequency Change with Temperature T_A = T_{low} to T_{high}	$\Delta f_{OSC}/\Delta T$	–	1.0	–	–	0.5	–	%
Oscillator Voltage Swing (Peak–to–Peak)	V_{OSC}	–	1.6	–	–	1.6	–	V
Discharge Current (V_{OSC} = 2.0 V)	I_{dischg}							mA
T_J = 25°C		7.8	8.3	8.8	7.8	8.3	8.8	
T_A = T_{low} to T_{high} (UC284XB, UC384XB)		7.5	–	8.8	7.6	–	8.8	
(UC384XBV)		–	–	–	7.2	–	8.8	

NOTES: 1. Maximum package power dissipation limits must be observed.
2. Adjust V_{CC} above the Startup threshold before setting to 15 V.
3. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.

T_{low} = 0°C for UC3844B, UC3845B
= – 25°C for UC2844B, UC2845B
= – 40°C for UC3844BV, UC3845BV

T_{high} = + 70°C for UC3844B, UC3845B
= + 85°C for UC2844B, UC2845B
= +105°C for UC3844BV, UC3845BV

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V [Note 2], R_T = 10 k, C_T = 3.3 nF. For typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies [Note 3], unless otherwise noted.)

Characteristic	Symbol	UC284XB			UC384XB, XBV			Unit
		Min	Typ	Max	Min	Typ	Max	
ERROR AMPLIFIER SECTION								
Voltage Feedback Input (V_O = 2.5 V)	V_{FB}	2.45	2.5	2.55	2.42	2.5	2.58	V
Input Bias Current (V_{FB} = 5.0 V)	I_{IB}	–	– 0.1	–1.0	–	– 0.1	– 2.0	µA
Open Loop Voltage Gain (V_O = 2.0 V to 4.0 V)	A_{VOL}	65	90	–	65	90	–	dB
Unity Gain Bandwidth (T_J = 25°C)	BW	0.7	1.0	–	0.7	1.0	–	MHz
Power Supply Rejection Ratio (V_{CC} = 12 V to 25 V)	PSRR	60	70	–	60	70	–	dB
Output Current								mA
Sink (V_O = 1.1 V, V_{FB} = 2.7 V)	I_{Sink}	2.0	12	–	2.0	12	–	
Source (V_O = 5.0 V, V_{FB} = 2.3 V)	I_{Source}	– 0.5	–1.0	–	– 0.5	–1.0	–	
Output Voltage Swing								V
High State (R_L = 15 k to ground, V_{FB} = 2.3 V)	V_{OH}	5.0	6.2	–	5.0	6.2	–	
Low State (R_L = 15 k to V_{ref}, V_{FB} = 2.7 V)	V_{OL}							
(UC284XB, UC384XB)		–	0.8	1.1	–	0.8	1.1	
(UC384XBV)		–	–	–	–	0.8	1.2	
CURRENT SENSE SECTION								
Current Sense Input Voltage Gain (Notes 4 & 5)	A_V							V/V
(UC284XB, UC384XB)		2.85	3.0	3.15	2.85	3.0	3.15	
(UC384XBV)		–	–	–	2.85	3.0	3.25	
Maximum Current Sense Input Threshold (Note 4)	V_{th}							V
(UC284XB, UC384XB)		0.9	1.0	1.1	0.9	1.0	1.1	
(UC384XBV)		–	–	–	0.85	1.0	1.1	
Power Supply Rejection Ratio (V_{CC} = 12 V to 25 V) (Note 4)	PSRR	–	70	–	–	70	–	dB
Input Bias Current	I_{IB}	–	– 2.0	–10	–	– 2.0	–10	µA
Propagation Delay (Current Sense Input to Output)	$t_{PLH(In/Out)}$	–	150	300	–	150	300	ns
OUTPUT SECTION								
Output Voltage								V
Low State (I_{Sink} = 20 mA)	V_{OL}	–	0.1	0.4	–	0.1	0.4	
(I_{Sink} = 200 mA, UC284XB, UC384XB)		–	1.6	2.2	–	1.6	2.2	
(I_{Sink} = 200 mA, UC384XBV)		–	–	–	–	1.6	2.3	
High State (I_{Source} = 20 mA, UC284XB, UC384XB)	V_{OH}	13	13.5	–	13	13.5	–	
(I_{Source} = 20 mA, UC384XBV)		–	–	–	12.9	–	–	
(I_{Source} = 200 mA)		12	13.4	–	12	13.4	–	
Output Voltage with UVLO Activated V_{CC} = 6.0 V, I_{Sink} = 1.0 mA	$V_{OL(UVLO)}$	–	0.1	1.1	–	0.1	1.1	V
Output Voltage Rise Time (C_L = 1.0 nF, T_J = 25°C)	t_r	–	50	150	–	50	150	ns
Output Voltage Fall Time (C_L = 1.0 nF, T_J = 25°C)	t_f	–	50	150	–	50	150	ns
UNDERVOLTAGE LOCKOUT SECTION								
Startup Threshold	V_{th}							V
UCX844B, BV		15	16	17	14.5	16	17.5	
UCX845B, BV		7.8	8.4	9.0	7.8	8.4	9.0	
Minimum Operating Voltage After Turn–On	$V_{CC(min)}$							V
UCX844B, BV		9.0	10	11	8.5	10	11.5	
UCX845B, BV		7.0	7.6	8.2	7.0	7.6	8.2	

NOTES: 2. Adjust V_{CC} above the Startup threshold before setting to 15 V.

3. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.

T_{low} = 0°C for UC3844B, UC3845B
= – 25°C for UC2844B, UC2845B
= – 40°C for UC3844BV, UC3845BV

T_{high} = + 70°C for UC3844B, UC3845B
= + 85°C for UC2844B, UC2845B
= +105°C for UC3844BV, UC3845BV

4. This parameter is measured at the latch trip point with V_{FB} = 0 V.

5. Comparator gain is defined as: $A_V = \dfrac{\Delta V \text{ Output/Compensation}}{\Delta V \text{ Current Sense Input}}$

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V [Note 2], R_T = 10 k, C_T = 3.3 nF. For typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies [Note 3], unless otherwise noted.)

Characteristic	Symbol	UC284XB			UC384XB, XBV			Unit
		Min	Typ	Max	Min	Typ	Max	
PWM SECTION								
Duty Cycle								%
Maximum (UC284XB, UC384XB)	$DC_{(max)}$	47	48	50	47	48	50	
(UC384XBV)		–	–	–	46	48	50	
Minimum	$DC_{(min)}$	–	–	0	–	–	0	
TOTAL DEVICE								
Power Supply Current	I_{CC}							mA
Startup (V_{CC} = 6.5 V for UCX845B, 14 V for UCX844B, BV)		–	0.3	0.5	–	0.3	0.5	
Operating (Note 2)		–	12	17	–	12	17	
Power Supply Zener Voltage (I_{CC} = 25 mA)	V_Z	30	36	–	30	36	–	V

NOTES: 2. Adjust V_{CC} above the Startup threshold before setting to 15 V.
3. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.

T_{low} = 0°C for UC3844B, UC3845B
= – 25°C for UC2844B, UC2845B
= – 40°C for UC3844BV, UC3845BV

T_{high} = + 70°C for UC3844B, UC3845B
= + 85°C for UC2844B, UC2845B
= +105°C for UC3844BV, UC3845BV

Figure 1. Timing Resistor versus Oscillator Frequency

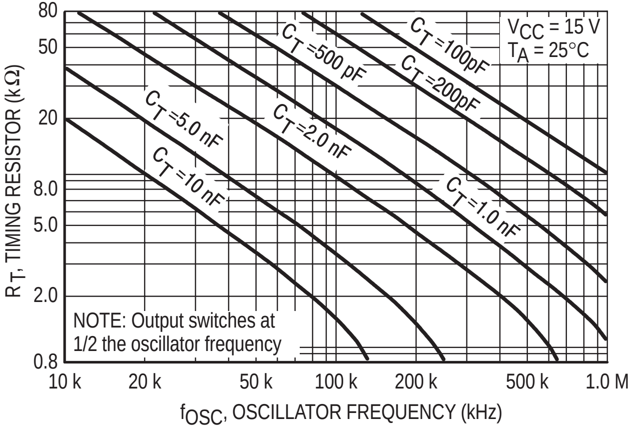


Figure 2. Output Deadtime versus Oscillator Frequency

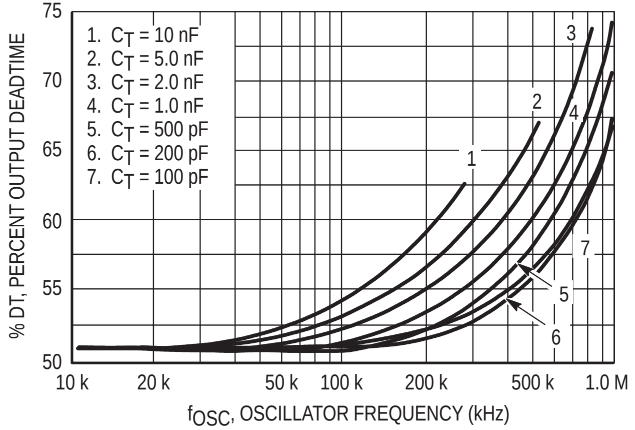


Figure 3. Error Amp Small Signal Transient Response

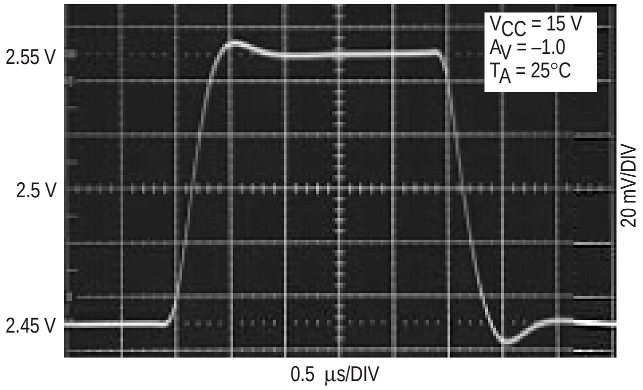


Figure 4. Error Amp Large Signal Transient Response

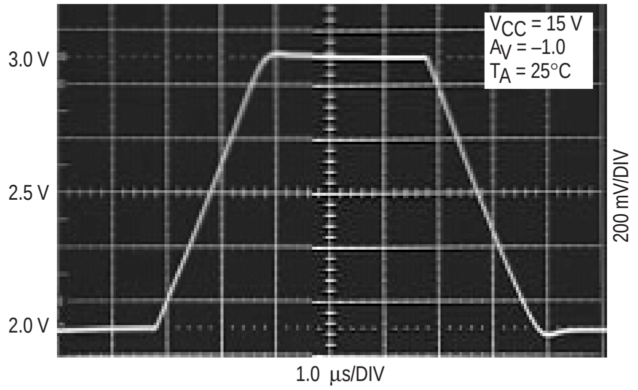


Figure 5. Error Amp Open Loop Gain and Phase versus Frequency

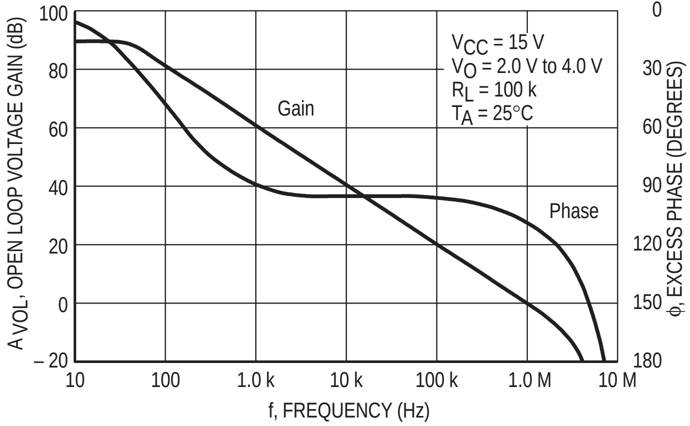


Figure 6. Current Sense Input Threshold versus Error Amp Output Voltage

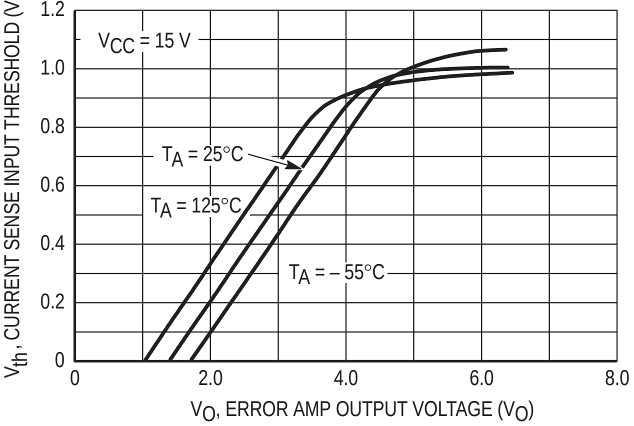


Figure 7. Reference Voltage Change versus Source Current

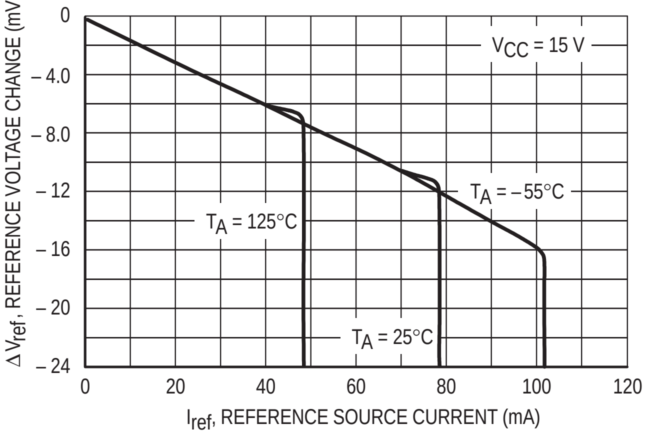


Figure 8. Reference Short Circuit Current versus Temperature

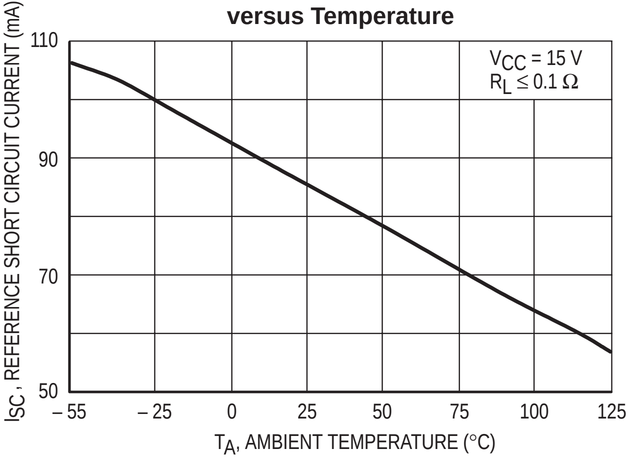


Figure 9. Reference Load Regulation

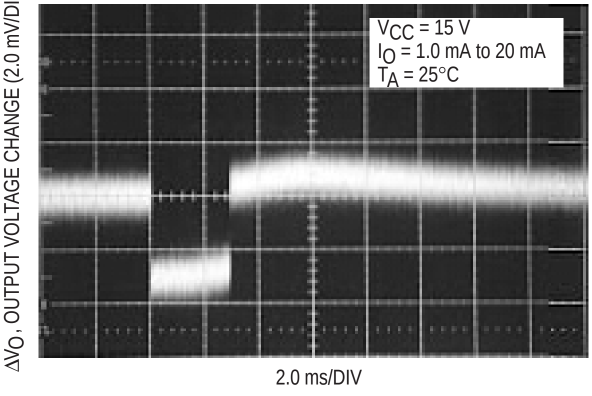


Figure 10. Reference Line Regulation

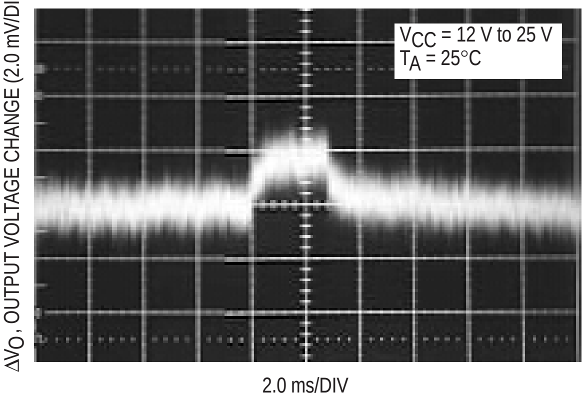


Figure 11. Output Saturation Voltage versus Load Current

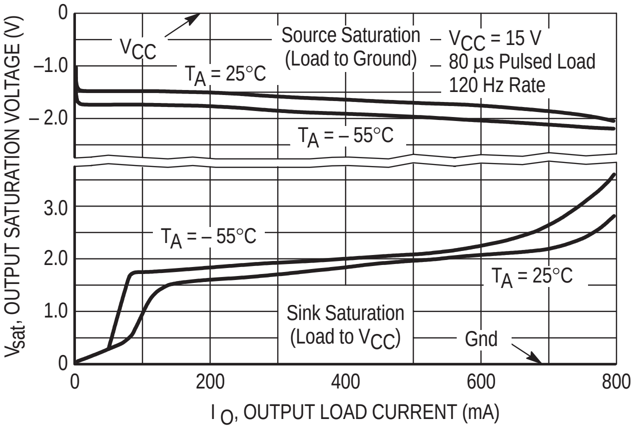


Figure 12. Output Waveform

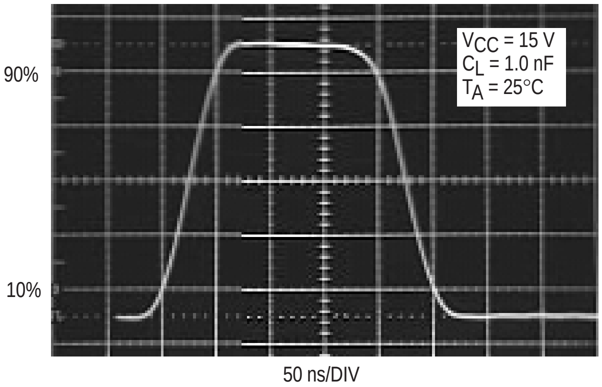


Figure 13. Output Cross Conduction

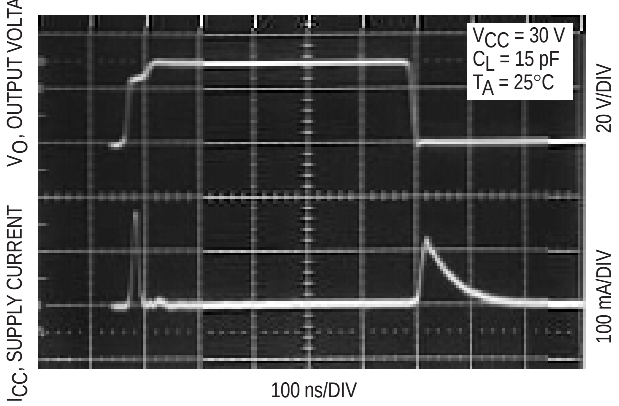
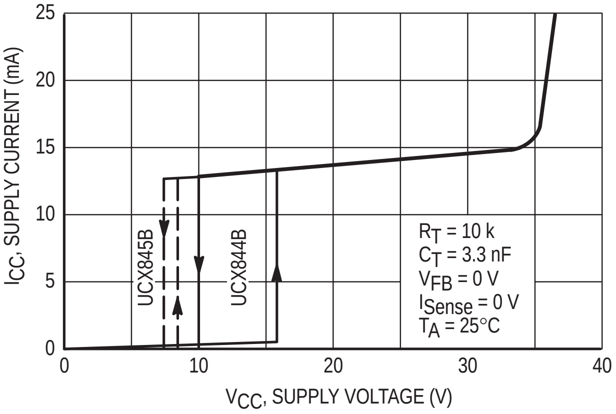


Figure 14. Supply Current versus Supply Voltage



PIN FUNCTION DESCRIPTION

Pin		Function	Description
8–Pin	14–Pin		
1	1	Compensation	This pin is the Error Amplifier output and is made available for loop compensation.
2	3	Voltage Feedback	This is the inverting input of the Error Amplifier. It is normally connected to the switching power supply output through a resistor divider.
3	5	Current Sense	A voltage proportional to inductor current is connected to this input. The PWM uses this information to terminate the output switch conduction.
4	7	R_T/C_T	The Oscillator frequency and maximum Output duty cycle are programmed by connecting resistor R_T to V_{ref} and capacitor C_T to ground. Oscillator operation to 1.0 kHz is possible.
5		Gnd	This pin is the combined control circuitry and power ground.
6	10	Output	This output directly drives the gate of a power MOSFET. Peak currents up to 1.0 A are sourced and sunk by this pin. The output switches at one–half the oscillator frequency.
7	12	V_{CC}	This pin is the positive supply of the control IC.
8	14	V_{ref}	This is the reference output. It provides charging current for capacitor C_T through resistor R_T.
	8	Power Ground	This pin is a separate power ground return that is connected back to the power source. It is used to reduce the effects of switching transient noise on the control circuitry.
	11	V_C	The Output high state (V_{OH}) is set by the voltage applied to this pin. With a separate power source connection, it can reduce the effects of switching transient noise on the control circuitry.
	9	Gnd	This pin is the control circuitry ground return and is connected back to the power source ground.
	2,4,6,13	NC	No connection. These pins are not internally connected.

OPERATING DESCRIPTION

The UC3844B, UC3845B series are high performance, fixed frequency, current mode controllers. They are specifically designed for Off–Line and dc–to–dc converter applications offering the designer a cost–effective solution with minimal external components. A representative block diagram is shown in Figure 15.

Oscillator

The oscillator frequency is programmed by the values selected for the timing components R_T and C_T. Capacitor C_T is charged from the 5.0 V reference through resistor R_T to approximately 2.8 V and discharged to 1.2 V by an internal current sink. During the discharge of C_T, the oscillator generates an internal blanking pulse that holds the center input of the NOR gate high. This causes the Output to be in a low state, thus producing a controlled amount of output deadtime. An internal flip–flop has been incorporated in the UCX844/5B which blanks the output off every other clock cycle by holding one of the inputs of the NOR gate high. This in combination with the C_T discharge period yields output deadtimes programmable from 50% to 70%. Figure 1 shows R_T versus Oscillator Frequency and Figure 2, Output Deadtime versus Frequency, both for given values of C_T. Note that many values of R_T and C_T will give the same oscillator frequency but only one combination will yield a specific output deadtime at a given frequency. The oscillator thresholds are temperature compensated to within ±6% at 50 kHz. Also, because of industry trends moving the UC384X into higher and higher frequency applications, the UC384XB is guaranteed to within ±10% at 250 kHz.

In many noise–sensitive applications it may be desirable to frequency–lock the converter to an external system clock. This can be accomplished by applying a clock signal to the circuit shown in Figure 17. For reliable locking, the free–running oscillator frequency should be set about 10% less than the clock frequency. A method for multi–unit synchronization is shown in Figure 18. By tailoring the clock waveform, accurate Output duty cycle clamping can be achieved to realize output deadtimes of greater than 70%.

Error Amplifier

A fully compensated Error Amplifier with access to the inverting input and output is provided. It features a typical dc voltage gain of 90 dB, and a unity gain bandwidth of 1.0 MHz with 57 degrees of phase margin (Figure 5). The non–inverting input is internally biased at 2.5 V and is not pinned out. The converter output voltage is typically divided down and monitored by the inverting input. The maximum input bias current is –2.0 µA which can cause an output voltage error that is equal to the product of the input bias current and the equivalent input divider source resistance.

The Error Amp Output (Pin 1) is provided for external loop compensation (Figure 28). The output voltage is offset by two diode drops (≈1.4 V) and divided by three before it connects to the inverting input of the Current Sense Comparator. This guarantees that no drive pulses appear at the Output (Pin 6) when Pin 1 is at its lowest state (V_{OL}). This occurs when the power supply is operating and the load is removed, or at the beginning of a soft–start interval (Figures 20, 21). The Error Amp minimum feedback resistance is limited by the amplifier's source current (0.5 mA) and the required output voltage (V_{OH}) to reach the comparator's 1.0 V clamp level:

$$R_{f(min)} \approx \frac{3.0\,(1.0\text{ V}) + 1.4\text{ V}}{0.5\text{ mA}} = 8800\ \Omega$$

Current Sense Comparator and PWM Latch

The UC3844B, UC3845B operate as a current mode controller, whereby output switch conduction is initiated by the oscillator and terminated when the peak inductor current reaches the threshold level established by the Error Amplifier Output/Compensation (Pin 1). Thus the error signal controls the peak inductor current on a cycle–by–cycle basis. The Current Sense Comparator PWM Latch configuration used ensures that only a single pulse appears at the Output during any given oscillator cycle. The inductor current is converted to a voltage by inserting the ground–referenced sense resistor R_S in series with the source of output switch Q1. This voltage is monitored by the Current Sense Input (Pin 3) and compared to a level derived from the Error Amp Output. The peak inductor current under normal operating conditions is controlled by the voltage at Pin 1 where:

$$I_{pk} = \frac{V_{(Pin\ 1)} - 1.4\text{ V}}{3\,R_S}$$

Abnormal operating conditions occur when the power supply output is overloaded or if output voltage sensing is lost. Under these conditions, the Current Sense Comparator threshold will be internally clamped to 1.0 V. Therefore the maximum peak switch current is:

$$I_{pk(max)} = \frac{1.0\text{ V}}{R_S}$$

When designing a high power switching regulator it becomes desirable to reduce the internal clamp voltage in order to keep the power dissipation of R_S to a reasonable level. A simple method to adjust this voltage is shown in Figure 19. The two external diodes are used to compensate the internal diodes, yielding a constant clamp voltage over temperature. Erratic operation due to noise pickup can result if there is an excessive reduction of the $I_{pk(max)}$ clamp voltage.

A narrow spike on the leading edge of the current waveform can usually be observed and may cause the power supply to exhibit an instability when the output is lightly loaded. This spike is due to the power transformer interwinding capacitance and output rectifier recovery time. The addition of an RC filter on the Current Sense Input with a time constant that approximates the spike duration will usually eliminate the instability (refer to Figure 23).

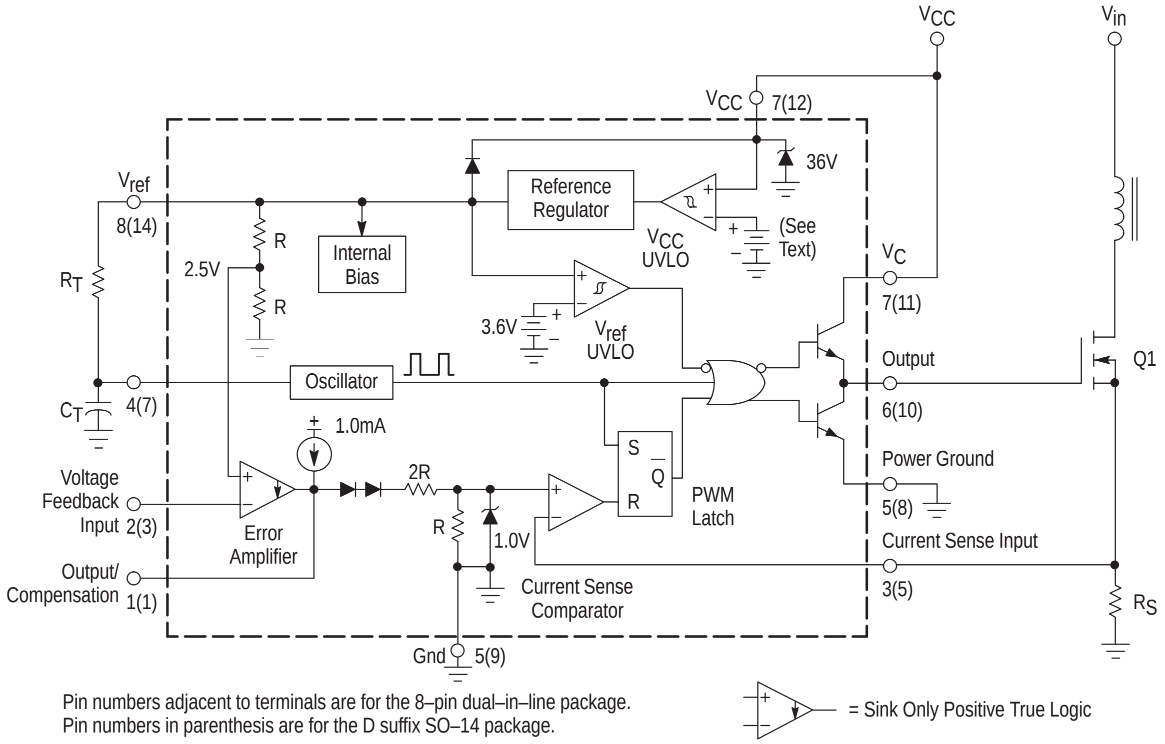


Figure 15. Representative Block Diagram

Pin numbers adjacent to terminals are for the 8–pin dual–in–line package.
Pin numbers in parenthesis are for the D suffix SO–14 package.

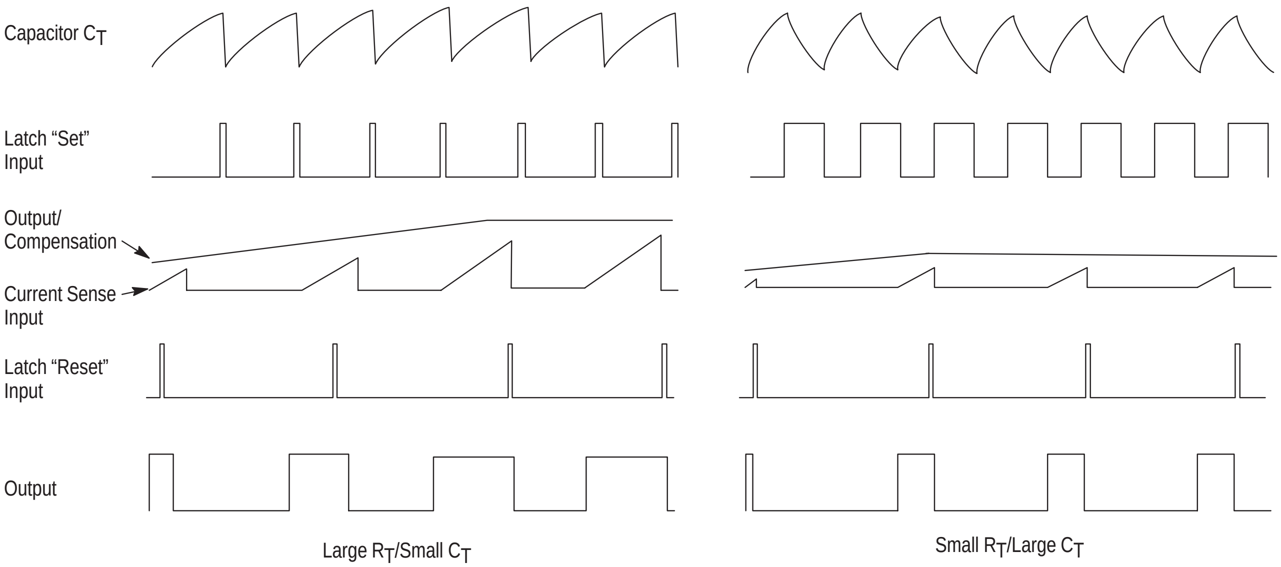


Figure 16. Timing Diagram

Undervoltage Lockout

Two undervoltage lockout comparators have been incorporated to guarantee that the IC is fully functional before the output stage is enabled. The positive power supply terminal (V_{CC}) and the reference output (V_{ref}) are each monitored by separate comparators. Each has built–in hysteresis to prevent erratic output behavior as their respective thresholds are crossed. The V_{CC} comparator upper and lower thresholds are 16 V/10 V for the UCX844B, and 8.4 V/7.6 V for the UCX845B. The V_{ref} comparator upper and lower thresholds are 3.6 V/3.4 V. The large hysteresis and low startup current of the UCX844B makes it ideally suited in off–line converter applications where efficient bootstrap startup techniques are required (Figure 29). The UCX845B is intended for lower voltage dc–to–dc converter applications. A 36 V zener is connected as a shunt regulator from V_{CC} to ground. Its purpose is to protect the IC from excessive voltage that can occur during system startup. The minimum operating voltage for the UCX844B is 11 V and 8.2 V for the UCX845B.

Output

These devices contain a single totem pole output stage that was specifically designed for direct drive of power MOSFETs. It is capable of up to ±1.0 A peak drive current and has a typical rise and fall time of 50 ns with a 1.0 nF load. Additional internal circuitry has been added to keep the Output in a sinking mode whenever an undervoltage lockout is active. This characteristic eliminates the need for an external pull–down resistor.

The SO–14 surface mount package provides separate pins for V_C (output supply) and Power Ground. Proper implementation will significantly reduce the level of switching transient noise imposed on the control circuitry. This becomes particularly useful when reducing the $I_{pk(max)}$ clamp level. The separate V_C supply input allows the designer added flexibility in tailoring the drive voltage independent of V_{CC}. A zener clamp is typically connected to this input when driving power MOSFETs in systems where V_{CC} is greater than 20 V. Figure 22 shows proper power and control ground connections in a current–sensing power MOSFET application.

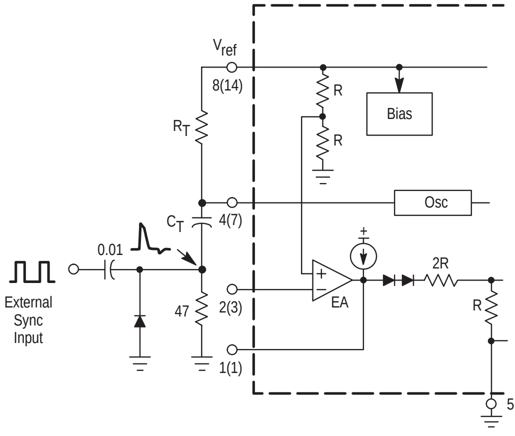
Reference

The 5.0 V bandgap reference is trimmed to ±1.0% tolerance at T_J = 25°C on the UC284XB, and ±2.0% on the UC384XB. Its primary purpose is to supply charging current to the oscillator timing capacitor. The reference has short–circuit protection and is capable of providing in excess of 20 mA for powering additional control system circuitry.

Design Considerations

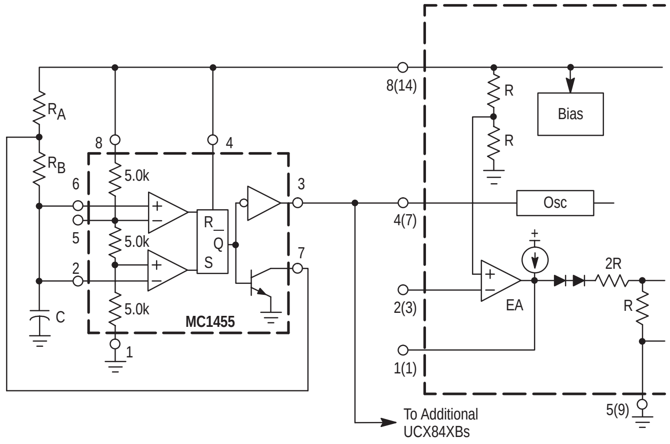
Do not attempt to construct the converter on wire–wrap or plug–in prototype boards. High frequency circuit layout techniques are imperative to prevent pulse–width jitter. This is usually caused by excessive noise pick–up imposed on the Current Sense or Voltage Feedback inputs. Noise immunity can be improved by lowering circuit impedances at these points. The printed circuit layout should contain a ground plane with low–current signal and high–current switch and output grounds returning on separate paths back to the input filter capacitor. Ceramic bypass capacitors (0.1 µF) connected directly to V_{CC}, V_C, and V_{ref} may be required depending upon circuit layout. This provides a low impedance path for filtering the high frequency noise. All high current loops should be kept as short as possible using heavy copper runs to minimize radiated EMI. The Error Amp compensation circuitry and the converter output voltage divider should be located close to the IC and as far as possible from the power switch and other noise–generating components.

Figure 17. External Clock Synchronization



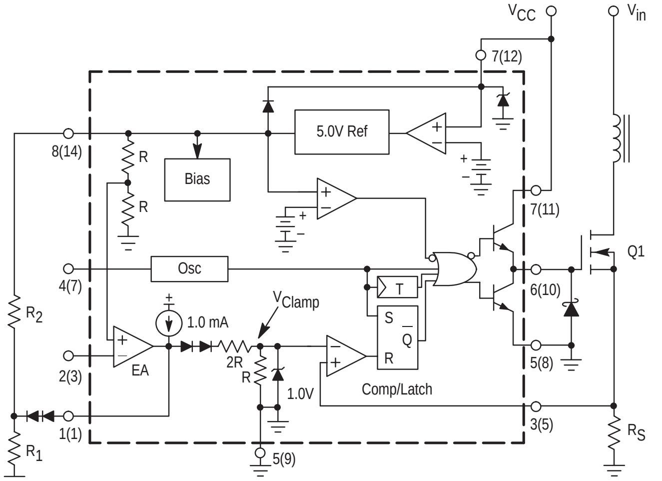
The diode clamp is required if the Sync amplitude is large enough to cause the bottom side of C_T to go more than 300 mV below ground.

Figure 18. External Duty Cycle Clamp and Multi–Unit Synchronization



$$f = \frac{1.44}{(R_A + 2R_B)C} \qquad D_{(max)} = \frac{R_A}{R_A + 2R_B}$$

Figure 19. Adjustable Reduction of Clamp Level

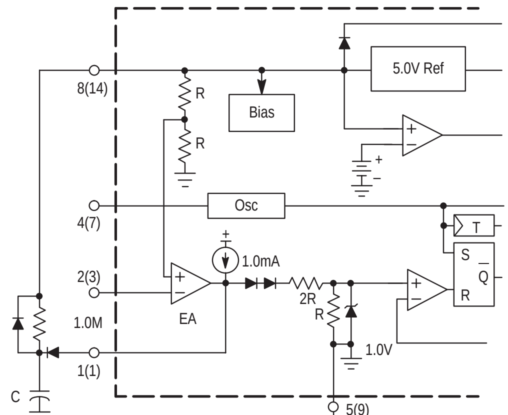


$$V_{Clamp} \approx \frac{1.67}{\left(\frac{R_2}{R_1}+1\right)} + 0.33\text{x}10^{-3}\left(\frac{R_1R_2}{R_1+R_2}\right)$$

Where: $0 \le V_{Clamp} \le 1.0$ V

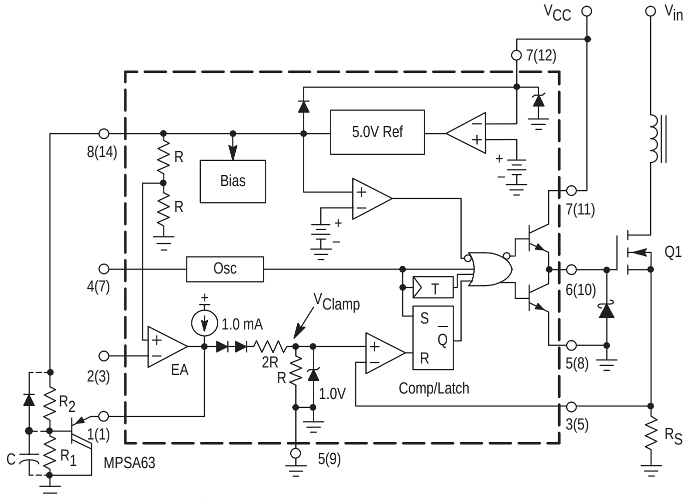
$$I_{pk(max)} \approx \frac{V_{Clamp}}{R_S}$$

Figure 20. Soft–Start Circuit



$t_{Soft–Start} \approx 3600C$ in µF

Figure 21. Adjustable Buffered Reduction of Clamp Level with Soft–Start

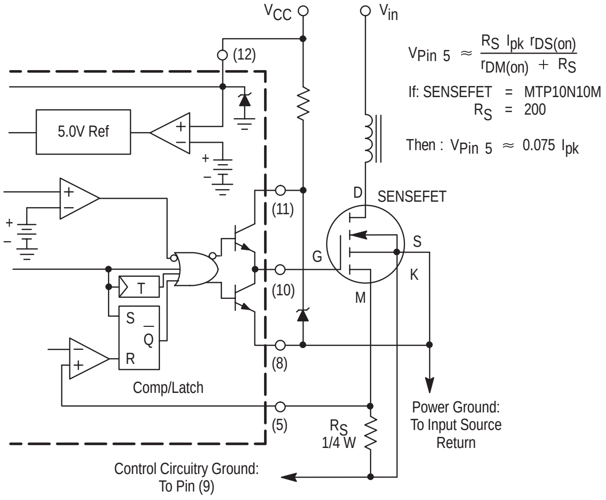


$$V_{Clamp} \approx \frac{1.67}{\left(\frac{R_2}{R_1}+1\right)}$$

Where: $0 \le V_{Clamp} \le 1.0$ V

$$t_{Soft\text{-}Start} = -\ln\left[1 - \frac{V_C}{3V_{Clamp}}\right] C\frac{R_1\ R_2}{R_1 + R_2} \qquad I_{pk(max)} \approx \frac{V_{Clamp}}{R_S}$$

Figure 22. Current Sensing Power MOSFET



$$V_{Pin\ 5} \approx \frac{R_S\ I_{pk}\ r_{DS(on)}}{r_{DM(on)} + R_S}$$

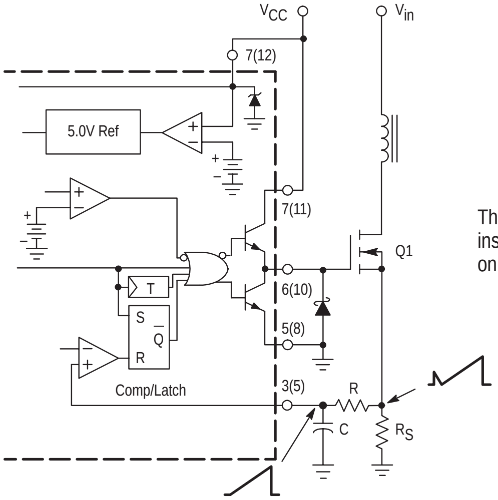
If: SENSEFET = MTP10N10M

$R_S = 200$

Then : $V_{Pin\ 5} \approx 0.075\ I_{pk}$

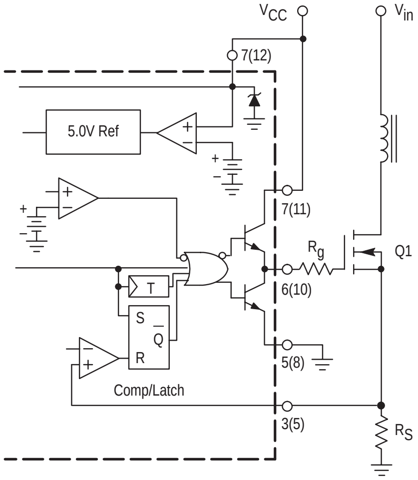
Virtually lossless current sensing can be achieved with the implementation of a SENSEFET power switch. For proper operation during over–current conditions, a reduction of the $I_{pk(max)}$ clamp level must be implemented. Refer to Figures 19 and 21.

Figure 23. Current Waveform Spike Suppression



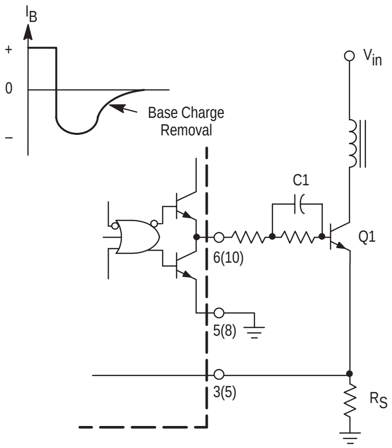
The addition of the RC filter will eliminate instability caused by the leading edge spike on the current waveform.

Figure 24. MOSFET Parasitic Oscillations



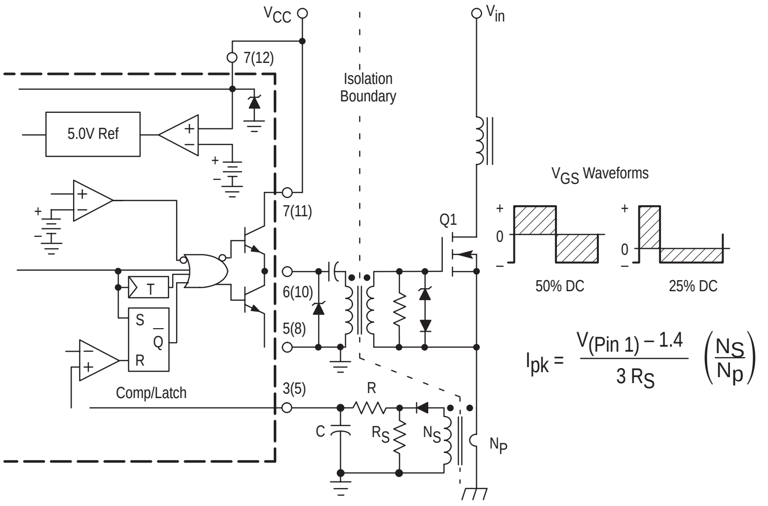
Series gate resistor R_g will damp any high frequency parasitic oscillations caused by the MOSFET input capacitance and any series wiring inductance in the gate–source circuit.

Figure 25. Bipolar Transistor Drive



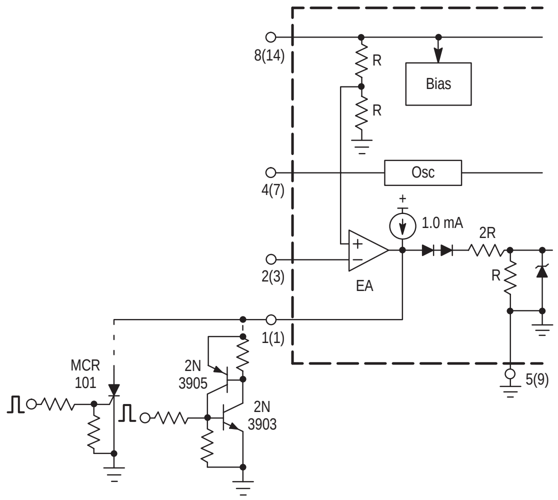
The totem pole output can furnish negative base current for enhanced transistor turn–off, with the addition of capacitor C_1.

Figure 26. Isolated MOSFET Drive



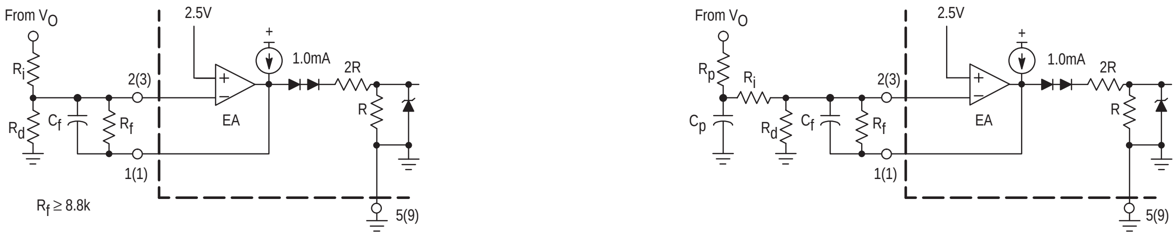
$$I_{pk} = \frac{V_{(Pin\ 1)} - 1.4}{3\ R_S} \left(\frac{N_S}{N_p}\right)$$

Figure 27. Latched Shutdown



The MCR101 SCR must be selected for a holding of < 0.5 mA @ $T_{A(min)}$. The simple two transistor circuit can be used in place of the SCR as shown. All resistors are 10 k.

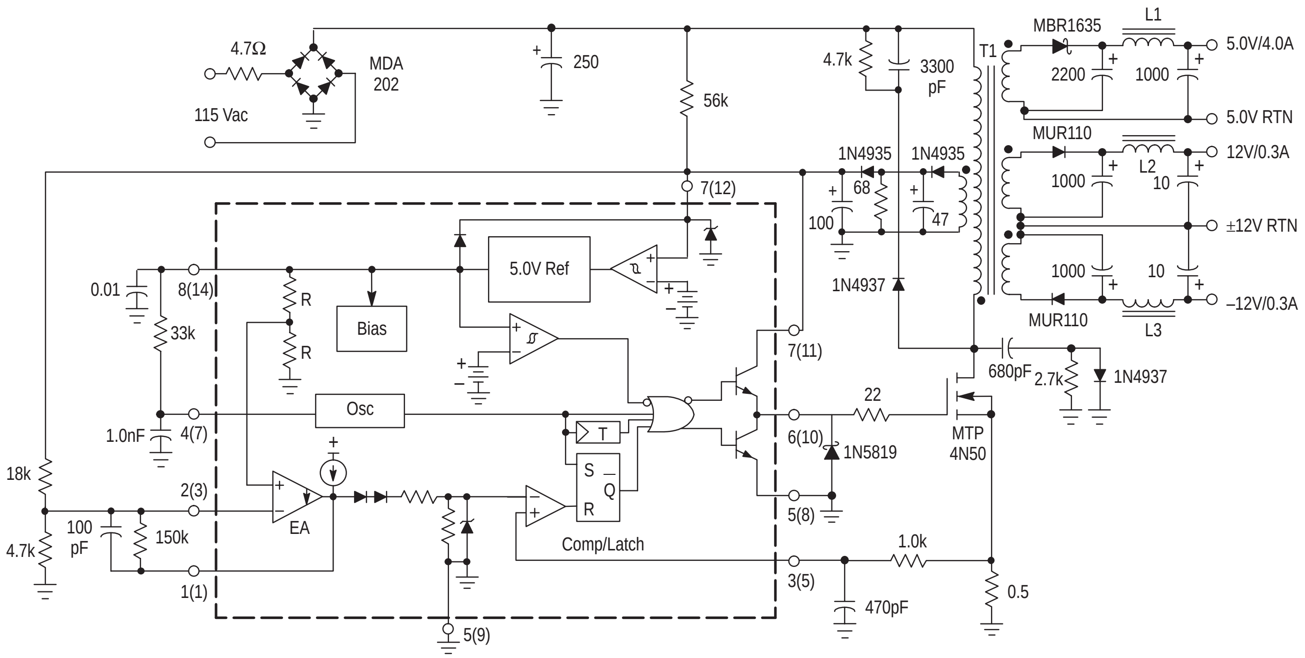
Figure 28. Error Amplifier Compensation



Error Amp compensation circuit for stabilizing any current mode topology except for boost and flyback converters operating with continuous inductor current.

Error Amp compensation circuit for stabilizing current mode boost and flyback topologies operating with continuous inductor current.

Figure 29. 7 W Off–Line Flyback Regulator



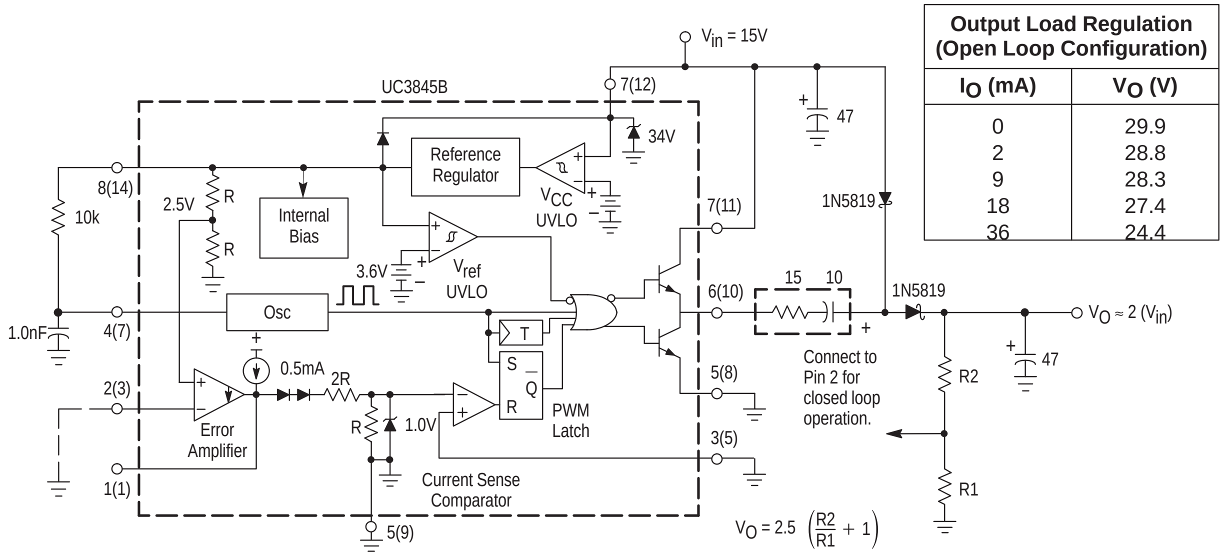
T1 – Primary: 45 Turns #26 AWG
Secondary ±12 V: 9 Turns #30 AWG (2 Strands) Bifiliar Wound
Secondary 5.0 V: 4 Turns (six strands) #26 Hexfiliar Wound
Secondary Feedback: 10 Turns #30 AWG (2 strands) Bifiliar Wound
Core: Ferroxcube EC35–3C8
Bobbin: Ferroxcube EC35PCB1
Gap: ≈ 0.10” for a primary inductance of 1.0 mH

L1 – 15 µH at 5.0 A, Coilcraft Z7156
L2, L3 – 25 µH at 5.0 A, Coilcraft Z7157

Test	Conditions	Results
Line Regulation: 5.0 V ±12 V	V_{in} = 95 Vac to 130 Vac	Δ = 50 mV or ±0.5% Δ = 24 mV or ±0.1%
Load Regulation: 5.0 V ±12 V	V_{in} = 115 Vac, I_{out} = 1.0 A to 4.0 A V_{in} = 115 Vac, I_{out} = 100 mA to 300 mA	Δ = 300 mV or ±3.0% Δ = 60 mV or ±0.25%
Output Ripple: 5.0 V ±12 V	V_{in} = 115 Vac	40 mV_{pp} 80 mV_{pp}
Efficiency	V_{in} = 115 Vac	70%

All outputs are at nominal load currents unless otherwise noted.

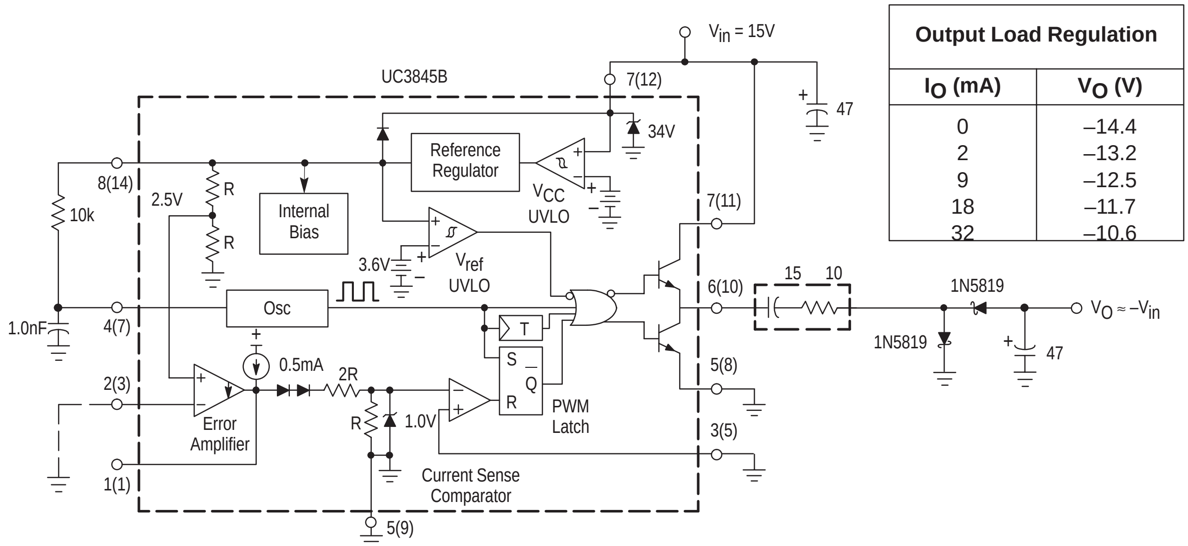
Figure 30. Step–Up Charge Pump Converter



Output Load Regulation (Open Loop Configuration)	
I_O (mA)	V_O (V)
0	29.9
2	28.8
9	28.3
18	27.4
36	24.4

The capacitor's equivalent series resistance must limit the Drive Output current to 1.0 A. An additional series resistor may be required when using tantalum or other low ESR capacitors. The converter's output can provide excellent line and load regulation by connecting the R2/R1 resistor divider as shown.

Figure 31. Voltage–Inverting Charge Pump Converter



Output Load Regulation	
I_O (mA)	V_O (V)
0	–14.4
2	–13.2
9	–12.5
18	–11.7
32	–10.6

The capacitor's equivalent series resistance must limit the Drive Output current to 1.0 A.
An additional series resistor may be required when using tantalum or other low ESR capacitors.

MOTOROLA

μA78S40

Universal Switching Regulator Subsystem

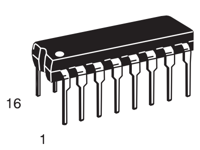
UNIVERSAL SWITCHING REGULATOR SUBSYSTEM

SEMICONDUCTOR TECHNICAL DATA

The μA78S40 is a switching regulator subsystem, consisting of a temperature compensated voltage reference, controlled–duty cycle oscillator with an active current limit circuit, comparator, high–current and high–voltage output switch, capable of 1.5 A and 40 V, pinned–out power diode and an uncommitted operational amplifier, which can be powered up or down independent of the IC supply. The switching output can drive external NPN or PNP transistors when voltages greater the 40 V, or currents in excess of 1.5 A, are required. Some of the features are wide–supply voltage range, low standby current, high efficiency and low drift. The μA78S40 is available in commercial (0° to + 70°C), and automotive (–40° to + 85°C) temperature ranges.

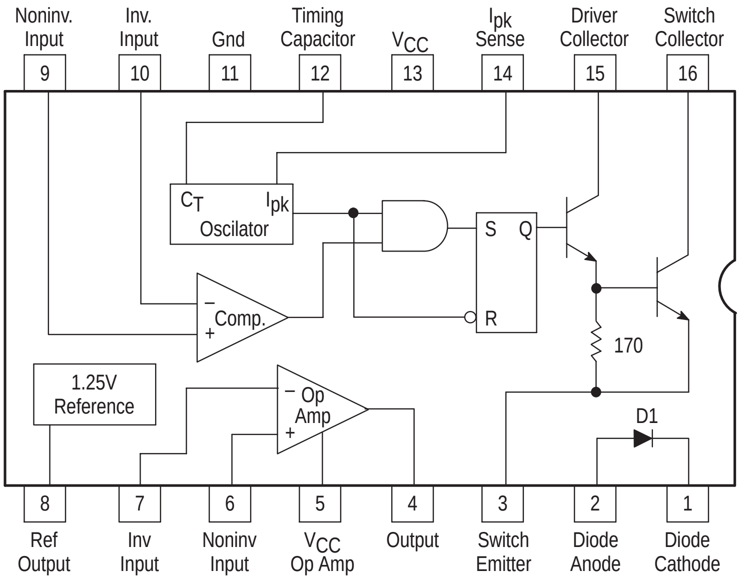
Some of the applications include use in step–up, step–down, and inverting regulators, with extremely good results obtained in battery–operated systems.

- Output Adjustable from 1.25 V to 40 V
- Peak Output Current of 1.5 A Without External Transistor
- 80 dB Line and Load Regulation
- Operation from 2.5 V to 40 V Supply
- Low Standby Current Drain
- High Gain, High Output Current, Uncommitted Op Amp



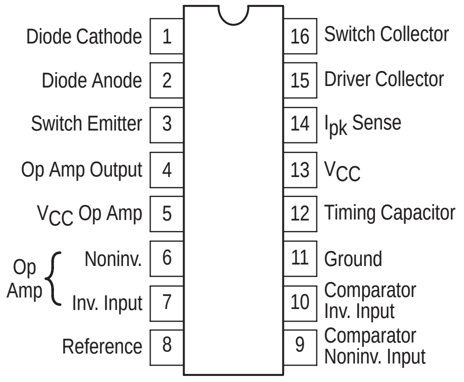
P SUFFIX
PLASTIC PACKAGE
CASE 648

Simplified Block Diagram



(Bottom View)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Temperature Range	Package
μA78S40PC	T_A = 0° to +70°C	Plastic
μA78S40PV	T_A = – 40° to +85°C	Plastic

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	40	V
Op Amp Power Supply Voltage	V_{CC} (Op Amp)	40	V
Common Mode Input Range (Comparator and Op Amp)	V_{ICR}	–0.3 to V_{CC}	V
Differential Input Voltage (Note 2)	V_{ID}	± 30	V
Output Short Circuit Duration (Op Amp)		Continuous	–
Reference Output Current	I_{ref}	10	mA
Voltage from Switch Collectors to Gnd		40	V
Voltage from Switch Emitters to Gnd		40	V
Voltage from Switch Collectors to Emitter		40	V
Voltage from Power Diode to Gnd		40	V
Reverse–Power Diode Voltage	V_{DR}	40	V
Current through Power Switch	I_{SW}	1.5	A
Current through Power Diode	I_D	1.5	A
Power Dissipation and Thermal Characteristics: Plastic Package (T_A = + 25°C) Derate above + 25°C (Note 1)	 P_D $1/R_{\theta JA}$	 1500 14	 mW mW/°C
Storage Temperature Range	T_{stg}	–65 to + 150	°C
Operating Temperature Range μA78S40V μA78S40C	T_A	 –40 to +85 0 to +70	°C

NOTES: 1. T_{low} = –40° for μA78S40PV T_{high} = +85° for μA78S40PV
= 0° for μA78S40PC   = +70° for μA78S40PC
2. For supply voltages less than 30 V the maximum differential input voltage (Error Amp and Op Amp) is equal to the supply voltage.

ELECTRICAL CHARACTERISTICS (V_{CC} = V_{CC} (Op Amp) 5.0 V, T_A = T_{low} to T_{high}, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
GENERAL					
Supply Voltage	V_{CC}	2.5	–	40	V
Supply Current (Op Amp V_{CC}, disconnected) (V_{CC} = 5.0 V) (V_{CC} = 40 V)	I_{CC}	 – –	 1.8 2.3	 3.5 5.0	mA
Supply Current (Op Amp V_{CC}, connected) (V_{CC} = 5.0 V) (V_{CC} = 40 V)	I_{CC}	 – –	 – –	 4.0 5.5	mA
REFERENCE					
Reference Voltage (I_{ref} = 1.0 mA)	V_{ref}	1.180	1.245	1.310	V
Reference Voltage Line Regulation (3.0 V ≤ V_{CC} ≤ 40 V, I_{ref} = 1.0 mA, T_A = 25°C)	Reg_{line}	–	0.04	0.2	mV/V
Reference Voltage Load Regulation (1.0 mA ≤ I_{ref} ≤ 10 mA, T_A = 25°C)	Reg_{load}	–	0.2	0.5	mV/mA

ELECTRICAL CHARACTERISTICS (V_{CC} = V_{CC} (Op Amp) 5.0 V, T_A = T_{low} to T_{high}, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OSCILLATOR					
Charging Current (T_A = 25°C) (V_{CC} = 5.0 V) (V_{CC} = 40 V)	I_{chg}	 20 20	 – –	 50 70	μA
Discharging Current (T_A = 25°C) (V_{CC} = 5.0 V) (V_{CC} = 40 V)	I_{dis}	 150 150	 – –	 250 350	μA
Oscillator Voltage Swing (T_A = 25°C) (V_{CC} = 5.0 V)	V_{osc}	–	0.5	–	V
Ratio of Charge/Discharge Time	t_{chg}/t_{dis}	–	6.0	–	–
CURRENT LIMIT					
Current–Limit Sense Voltage (T_A = 25°C) (V_{CC} – V_{Ipk} Sense)	V_{CLS}	250	–	350	mV
OUTPUT SWITCH					
Output Saturation Voltage 1 (I_{SW} = 1.0 A, Pin 15 tied to Pin 16)	V_{sat1}	–	0.93	1.3	V
Output Saturation Voltage 2 (I_{SW} = 1.0 A, I_{15} = 50 mA)	V_{sat2}	–	0.5	0.7	V
Output Transistor Current Gain (T_A = 25°C) (I_C = 1.0 A, V_{CE} = 5.0 V)	h_{FE}	–	70	–	–
Output Leakage Current (T_A = 25°C) (V_{CE} = 40 V)	$I_{C(off)}$	–	10	–	nA
POWER DIODE					
Forward Voltage Drop (I_D = 1.0 A)	V_D	–	1.25	1.5	V
Diode Leakage Current (T_A = 25°C) (V_{DR} = 40 V)	I_{DR}	–	10	–	nA
COMPARATOR					
Input Offset Voltage (V_{CM} = V_{ref})	V_{IO}	–	1.5	15	mV
Input Bias Current (V_{CM} = V_{ref})	I_{IB}	–	35	200	nA
Input Offset Current (V_{CM} = V_{ref})	I_{IO}	–	5.0	75	nA
Common Mode Voltage Range (T_A = 25°C)	V_{ICR}	0	–	V_{CC} – 2.0	V
Power–Supply Rejection Ratio (T_A = 25°C) ($3.0 \le V_{CC} \le 40$ V)	PSRR	70	96	–	dB
OUTPUT OPERATION AMPLIFIER					
Input Offset Voltage (V_{CM} = 2.5 V)	V_{IO}	–	4.0	15	mV
Input Bias Current (V_{CM} = 2.5 V)	I_{IB}	–	30	200	nA
Input Offset Current (V_{CM} = 2.5 V)	I_{IO}	–	5.0	75	nA
Voltage Gain + (T_A = 25°C) (R_L = 2.0 kΩ to Gnd, $1.0 \text{ V} \le V_O \le 2.5$ V)	$A_{VOL}+$	25	250	–	V/mV
Voltage Gain – (T_A = 25°C) (R_L = 2.0 kΩ to V_{CC} (Op Amp), $1.0 \text{ V} \le V_O \le 2.5$ V)	$A_{VOL}-$	25	250	–	V/mV
Common Mode Voltage Range (T_A = 25°C)	V_{ICR}	0	–	V_{CC} – 2.0	V
Common Mode Rejection Ratio (T_A = 25°C) (V_{CM} = 0 V to 3.0 V)	CMRR	76	100	–	dB
Power–Supply Rejection Ratio (T_A = 25°C) (3.0 V ≤ V_{CC} (Op Amp) ≤ 40 V)	PSRR	76	100	–	dB
Output Source Current (T_A = 25°C)	I_{Source}	75	150	–	mA
Output Sink Current (T_A = 25°C)	I_{Sink}	10	35	–	mA
Slew Rate (T_A = 25°C)	SR	–	0.6	–	V/μs
Output Low Voltage (T_A = 25°C, I_L = –5.0 mA)	V_{OL}	–	–	1.0	V
Output High Voltage (T_A = 25°C, I_L = 50 mA)	V_{OH}	V_{CC}(Op Amp) – 3.0	–	–	V

Figure 1. Output Switch On/Off Time versus Oscillator Timing Capacitor

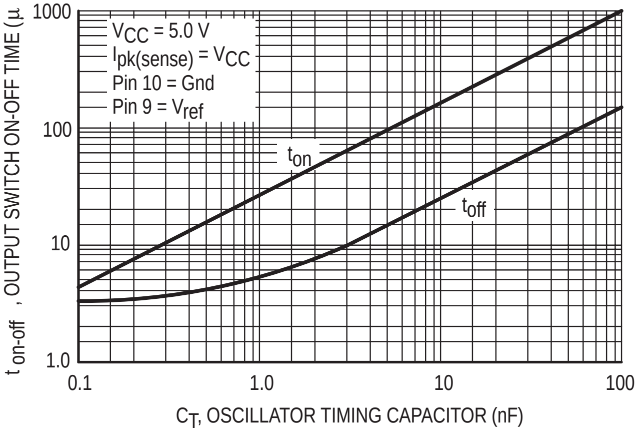


Figure 2. Standby Supply Current versus Supply Voltage

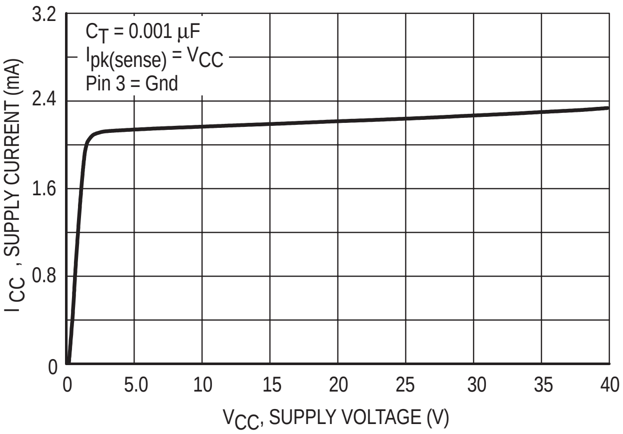


Figure 3. Emitter–Follower Configuration Output Switch Saturation Voltage versus Emitter Current

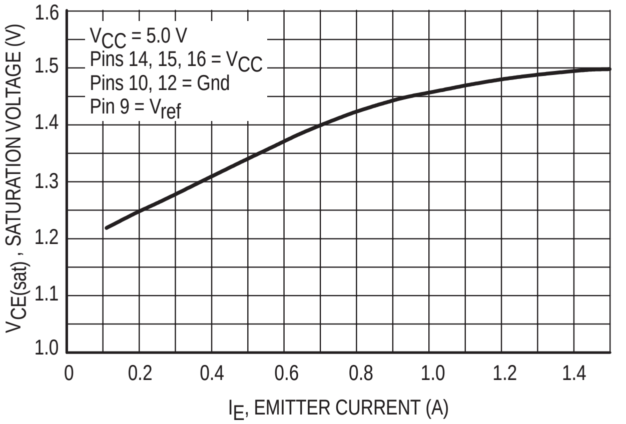


Figure 4. Common–Emitter Configuration Output Switch Saturation Voltage versus Collector Current

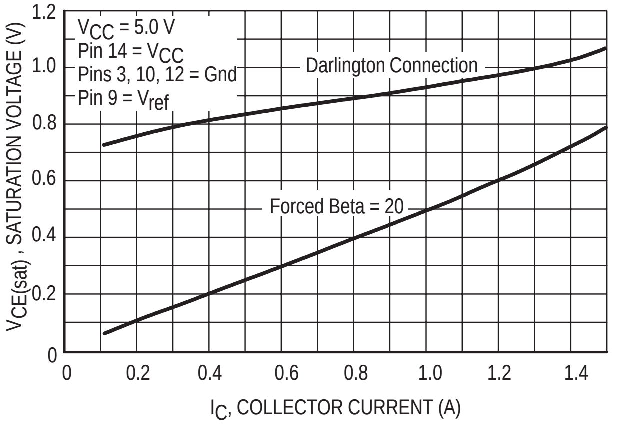
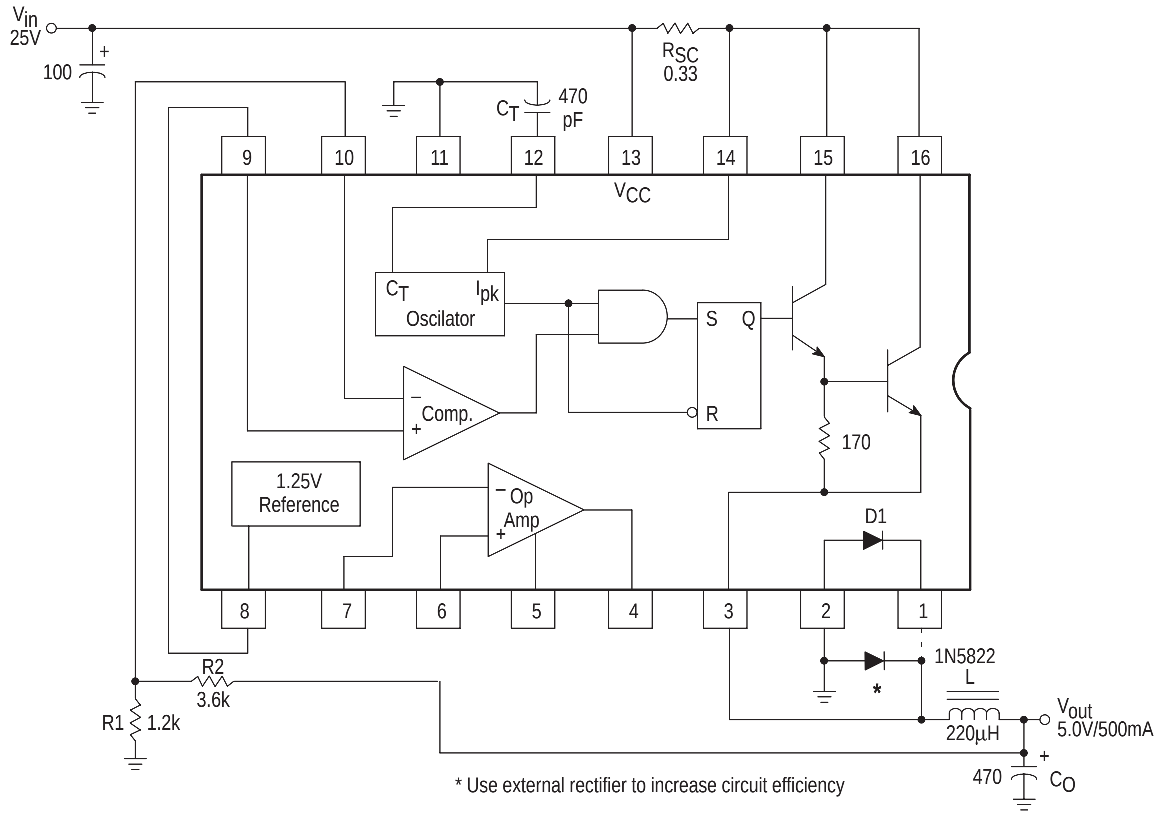
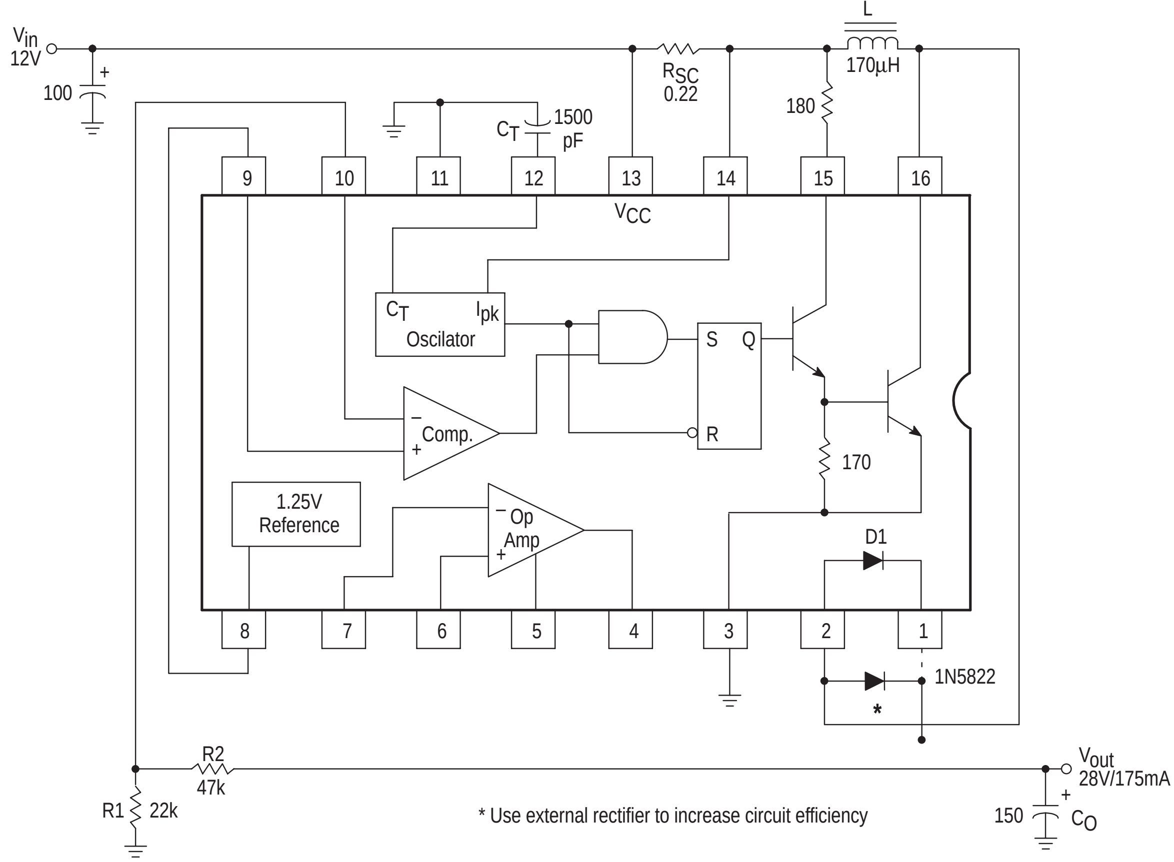


Figure 5. Step–Down Converter



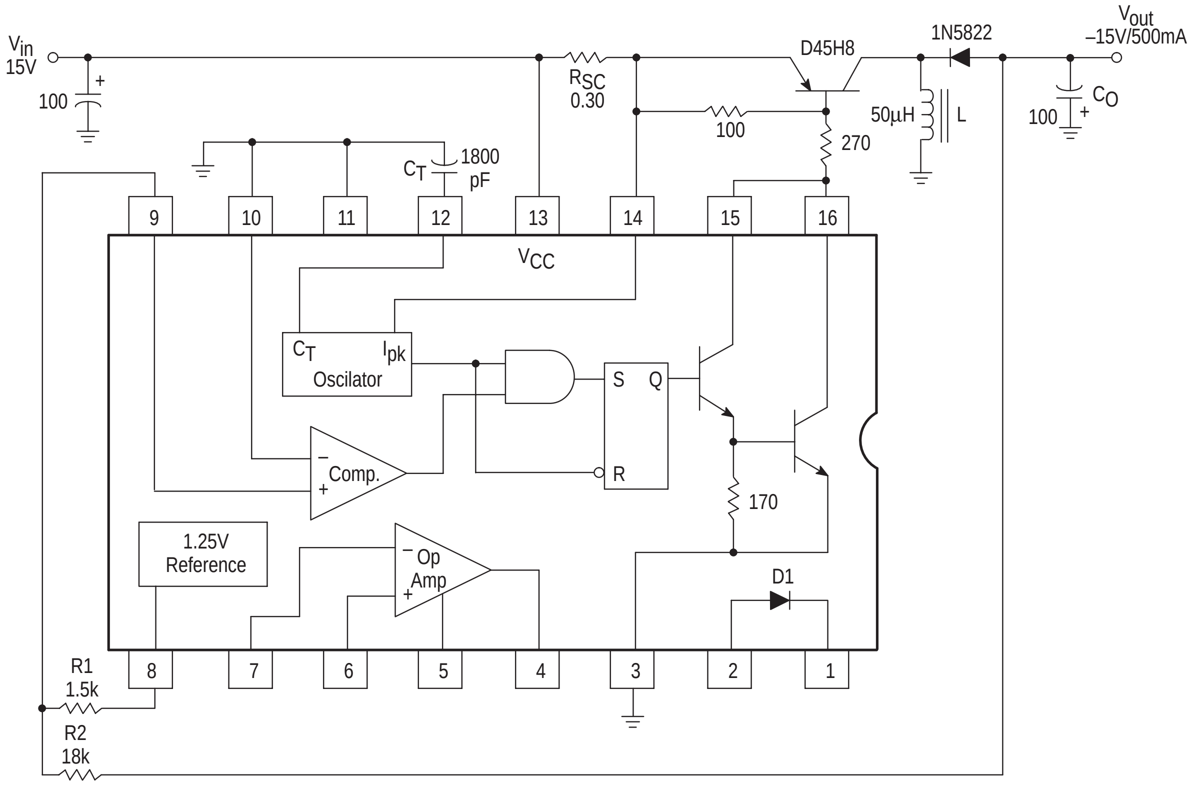
* Use external rectifier to increase circuit efficiency

Figure 6. Step–Up Converter



* Use external rectifier to increase circuit efficiency

Figure 7. Inverting Converter



Design Formula Table

Calculation	Step–Down	Step–Up	Inverting
$\frac{t_{on}}{t_{off}}$	$\frac{V_{out} + V_F}{V_{in(min)} - V_{sat} - V_{out}}$	$\frac{V_{out} - V_F \quad V_{in(min)}}{V_{in(min)} \quad V_{sat}}$	$\frac{V_{out} + V_F}{V_{in(min)} - V_{sat}}$
$(t_{on} + t_{off})$ max	$\frac{I}{f_{min}}$	$\frac{I}{f_{min}}$	$\frac{I}{f_{min}}$
C_T	$4 \times 10^{5}\, t_{on}$	$4 \times 10^{5}\, t_{on}$	$4 \times 10^{5}\, t_{on}$
$I_{pk(switch)}$	$2\, I_{out(max)}$	$2\, I_{out(max)} \left(\frac{t_{on} - t_{off}}{t_{off}}\right)$	$2\, I_{out(max)} \left(\frac{t_{on} + t_{off}}{t_{off}}\right)$
R_{SC}	$\frac{0.33}{I_{pk(switch)}}$	$\frac{0.33}{I_{pk(switch)}}$	$\frac{0.33}{I_{pk(switch)}}$
$L_{(min)}$	$\left(\frac{V_{in(min)} - V_{sat} - V_{out}}{I_{pk(switch)}}\right) t_{on(max)}$	$\left(\frac{V_{in(min)} - V_{sat}}{I_{pk(switch)}}\right) t_{on(max)}$	$\left(\frac{V_{in(min)} - V_{sat}}{I_{pk(switch)}}\right) t_{on(max)}$
C_O	$\frac{I_{pk(switch)}\,(t_{on} + t_{off})}{8\, V_{ripple(pp)}}$	$\approx \frac{I_{out}\, t_{on}}{V_{ripple}}$	$\approx \frac{I_{out}\, t_{on}}{V_{ripple}}$

V_{sat} = Saturation voltage of the output switch. V_F = Forward voltage drop of the ringback rectifier.

The following power supply characteristics must be chosen:

V_{in} – Nominal input voltage. If this voltage is not constant, then use $V_{in(max)}$ for step–down and $V_{in(min)}$ for step–up and inverting convertor.

V_{out} – Desired output voltage: $V_{out} = 1.25 \left(1 + \frac{R_2}{R_1}\right)$ for step–down and step–up: $V_{out} = \frac{1.25\ R_2}{R_1}$ for inverting.

I_{out} – Desired output current.

f_{min} – Minimum desired output switching frequency at the selected values for V_{in} and I_O.

$V_{ripple(pp)}$ – Desired peak–to–peak output ripple voltage. In practice, the calculated value will need to be increased due to the capacitor's equivalent series resistance and board layout. The ripple voltage should be kept to a low value since it will directly effect the line and load regulation.

See Application Note AN920 for further information

Addendum
Linear & Switching Voltage Regulator Applications Information

In Brief . . .

In most electronic systems, voltage regulation is required for various functions. Today's complex electronic systems are requiring greater regulating performance, higher efficiency and lower parts count. Present integrated circuit and power package technology has produced IC voltage regulators which can ease the task of regulated power supply design, provide the performance required and remain cost effective. Available in a growing variety, Motorola offers a wide range of regulator products from fixed and adjustable voltage types to special–function and switching regulator control ICs.

This handbook describes Motorola's voltage regulator products and provides information on applying these products. Basic Linear regulator theory and switching regulator topologies have been included along with practical design examples. Other relevant topics include trade–offs of Linear versus switching regulators, series pass elements for Linear regulators, switching regulator component design considerations, heatsinking, construction and layout, power supply supervision and protection, and reliability.

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SECTION 1

BASIC LINEAR REGULATOR THEORY

A. IC Voltage Regulator

The basic functional block diagram of an integrated circuit voltage regulator is shown in Figure 1–1. It consists of a stable reference, whose output voltage is V_{ref}, and a high gain error amplifier. The output voltage (V_O), is equal to or a multiple of V_{ref}. The regulator will tend to keep V_O constant by sensing any changes in V_O and trying to return it to its original value. Therefore, the ideal voltage regulator could be considered a voltage source with a constant output voltage. However, in practice the IC regulator is better represented by the model shown in Figure 1–2.

In this figure, the regulator is modeled as a voltage source with a positive output impedance (Z_O). The value of the voltage source (V) is not constant; instead it varies with changes in supply voltage (V_{CC}) and with changes in IC junction temperature (T_J) induced by changes in ambient temperature and power dissipation. Also, the regulator output voltage (V_O) is affected by the voltage drop across Z_O, caused by the output current (I_O). In the following text, the reference and amplifier sections will be described, and their contributions to the changes in the output voltage analyzed.

B. Voltage Reference

Naturally, the major requirement for the reference is that it be stable; variations in supply voltage or junction temperature should have little or no effect on the value of the reference voltage (V_{ref}).

1. Zener Diode Reference

The simplest form of a voltage reference is shown in Figure 1–3a. It consists of a resistor and a zener diode. The zener voltage (V_Z) is used as the reference voltage. In order to determine V_Z, consider Figure 1–3b. The zener diode (VR1) of Figure 1–3a has been replaced with its equivalent circuit model and the value of V_Z is therefore given by (at a constant junction temperature):

$$V_Z = V_{BZ} + I_Z Z_Z = V_{BZ} + \left(\frac{V_{CC} - V_{BZ}}{R + Z_Z}\right) Z_Z \qquad (1)$$

where: V_{BZ} = zener breakdown voltage
I_Z = zener current
Z_Z = zener impedance at I_Z.

Note that changes in the supply voltage give rise to changes in the zener current, thereby changing the value of the reference voltage (V_Z).

Figure 1–1. Voltage Regulator Functional Block Diagram

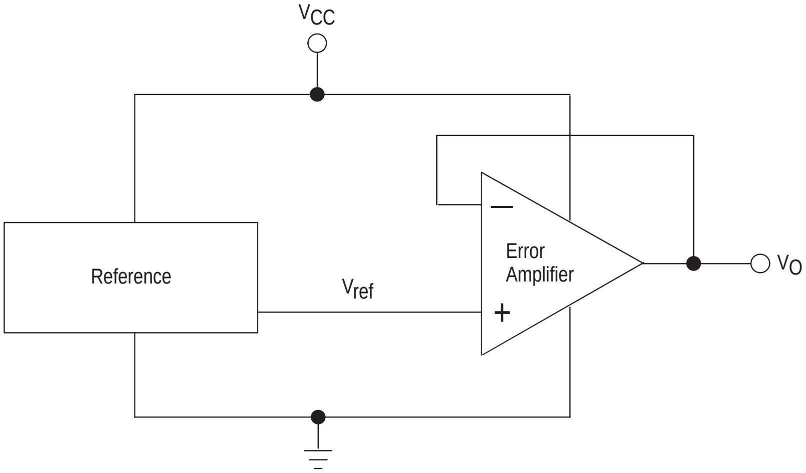


Figure 1–2. Voltage Regulator Equivalent Circuit Model

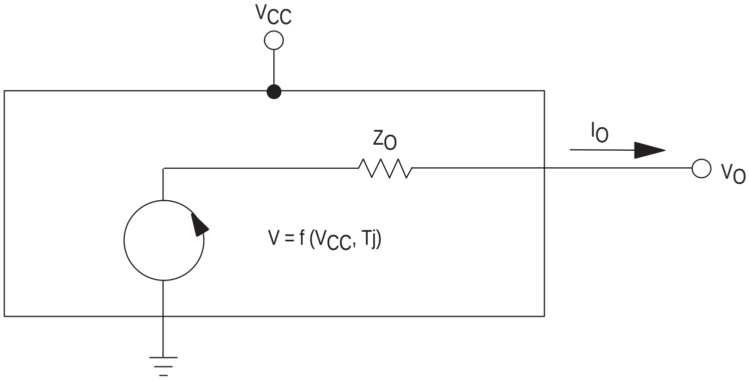
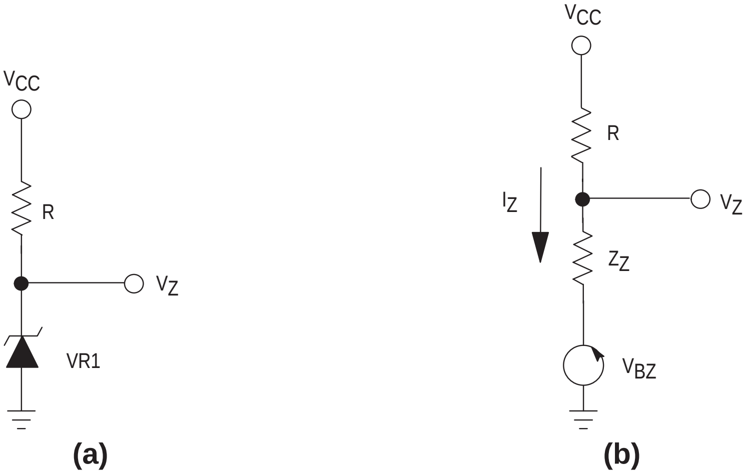


Figure 1–3. Zener Diode Reference



2. Constant Current — Zener Reference

The effect of zener impedance can be minimized by driving the zener diode with a constant current as shown in Figure 1–4. The value of the zener current is largely independent of V_{CC} and is given by:

$$I_Z = \frac{V_{BEQ1}}{R_{SC}} \tag{2}$$

where: V_{BEQ1} = base–emitter voltage of Q1.

This gives a reference voltage of:

$$V_{ref} = V_Z + V_{BEQ1} = V_{BZ} + I_Z Z_Z + V_{BEQ1} \tag{3}$$

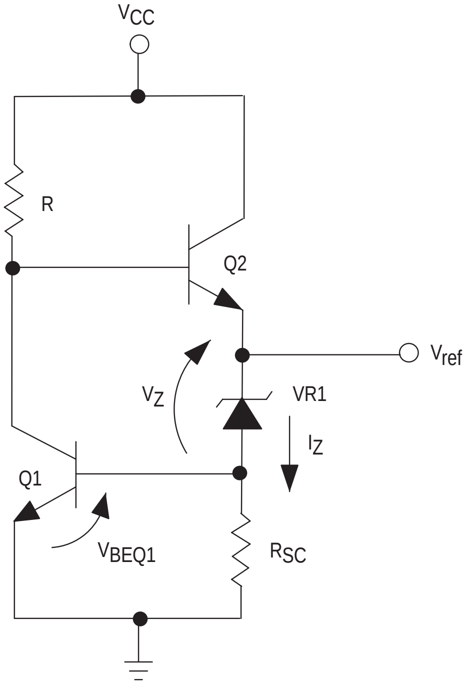
where I_Z is constant and given by Equation 2.

The reference voltage (about 7.0 V) of this configuration is therefore largely independent of supply voltage variations. This configuration has the additional benefit of better temperature stability than that of a simple resistor–zener reference.

Referring back to Figure 1–3a, it can be seen that the reference voltage temperature stability is equal to that of the zener diode, VR1. The stability of zener diodes used in most integrated circuitry is about + 2.2 mV/°C or $\simeq$ 0.04%/°C (for a 6.2 V zener). If the junction temperature varies 100°C, the zener or reference voltage would vary 4%. A variation this large is usually unacceptable.

However, the circuit of Figure 1–4 does not have this drawback. Here the positive 2.2 mV/°C temperature coefficient (TC) of the zener diode is offset by the negative 2.2 mV/°C TC of the V_{BE} of Q1. This results in a reference voltage with very stable temperature characteristics.

Figure 1–4. Constant Current (Zener Reference)



3. Bandgap Reference

Although very stable, the circuit of Figure 1–4 does have a disadvantage in that it requires a supply voltage of 9.0 V or more. Another type of stable reference which requires only a few volts to operate was described by Widlar(1) and is shown in Figure 1–5. In this circuit V_{ref} is given by:

$$V_{ref} = V_{BEQ3} + I_2R_2 \tag{4}$$

where: $I_2 = \dfrac{V_{BEQ1} - V_{BEQ2}}{R_1}$ (neglecting base currents)

The change in V_{ref} with junction temperature is given by:

$$\Delta V_{ref} = \Delta V_{BE3} + \left\{\frac{\Delta V_{BEQ1} - \Delta V_{BEQ2}}{R_1}\right\} R_2 \tag{5}$$

It can be shown that,

$$\Delta V_{BEQ1} = \Delta T_JK \ln I_1 \tag{6}$$

and, $$\Delta V_{BEQ2} = \Delta T_JK \ln I_2 \tag{7}$$

where: K = a constant

ΔT_J = change in junction temperature

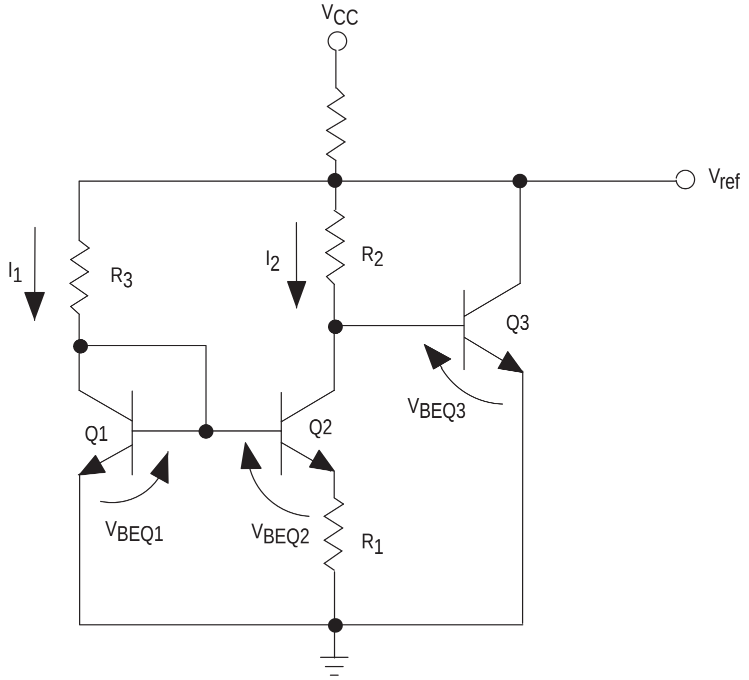
and, $I_1 > I_2$

Combining (5), (6), and (7)

$$\Delta V_{ref} = \Delta V_{BEQ3} + \Delta T_JK\left(\frac{R_2}{R_1}\right) \ln \frac{I_1}{I_2} \tag{8}$$

Since ΔV_{BEQ3} is negative, and with $I_1 > I_2$, $\ln I_1/I_2$ is positive, the net change in V_{ref} with temperature variations can be made to equal zero by appropriately selecting the values of I_1, R_1, and R_2.

Figure 1–5. Bandgap Reference



C. The Error Amplifier

Given a stable reference, the error amplifier becomes the determining factor in integrated circuit voltage regulator performance. Figure 1–6 shows a typical differential error amplifier in a voltage regulator configuration. With a constant supply voltage (V_{CC}) and junction temperature, the output voltage is given by:

$$V_O = A_{VOL}\,\upsilon_i - Z_{OL}\,I_O = A_{VOL}\,\{(V_{ref} \pm V_{IO}) - V_O\,\beta\} - Z_{OL}\,I_O \qquad (9)$$

where: A_{VOL} = amplifier open loop gain

V_{IO} = input offset voltage

Z_{OL} = open loop output impedance

$\beta = \dfrac{R_1}{R_1 + R_2}$ = feedback ratio (β is always ≤ 1)

I_O = output current

υ_i = true differential input voltage

Manipulating Equation 9:

$$V_O = \frac{(V_{ref} \pm V_{IO}) - \dfrac{Z_{OL}}{A_{VOL}}\,I_O}{\beta + \dfrac{1}{A_{VOL}}} \qquad (10)$$

Note that if the amplifier open loop gain is infinite, this expression reduces to:

$$V_O = \frac{1}{\beta}\,(V_{ref} \pm V_{IO}) = (V_{ref} \pm V_{IO})\left(1 + \frac{R_2}{R_1}\right) \qquad (11)$$

The output voltage can thus be set any value equal to or greater than ($V_{ref} \pm V_{IO}$). Note also that if A_{VOL} is not infinite, with constant output current (a non–varying output load), the output voltage can still be "tweaked–in" by varying R_1 and R_2, even though V_O will not exactly equal that given by Equation 11.

Assuming a stable reference and a finite value of A_{VOL}, inaccuracy of the output voltage can be traced to the following amplifier characteristics:

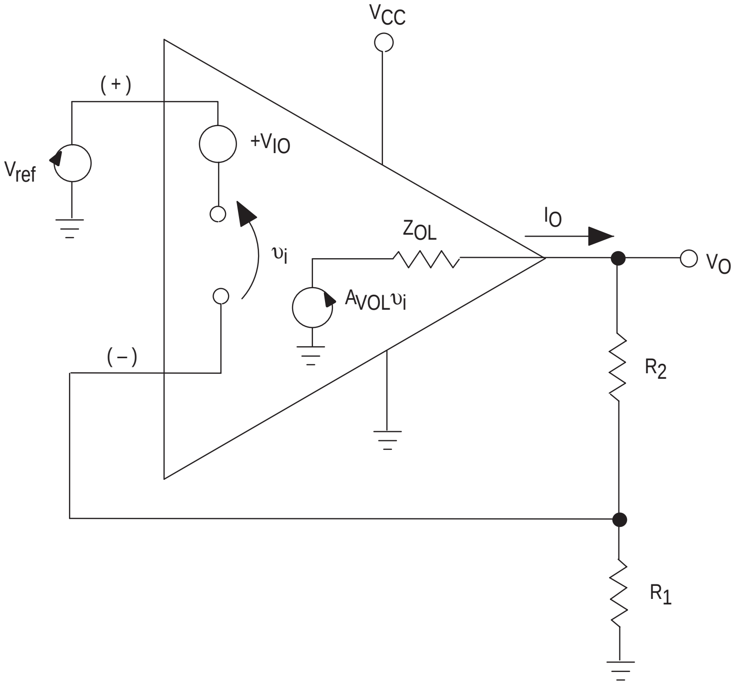
1. Amplifier Input Offset Voltage Drift

The input transistors of integrated circuit amplifiers are usually not perfectly matched. As in operational amplifiers, this is expressed in terms of an input offset voltage (V_{IO}). At a given temperature, this effect can be nulled out of the desired output voltage by adjusting V_{ref} or $1/\beta$. However, V_{IO} drifts with temperature, typically ± 5.0 μV/°C to +15 μV/°C, causing a proportional change in the output voltage. Closer matching of the internal amplifier input transistors minimizes this effect, as does selecting a feedback ratio (β) to be close to unity.

2. Amplifier Power Supply Sensitivity

Changes in regulator output voltage due to power supply voltage variations can be attributed to two amplifier performance parameters: power supply rejection ratio (PSRR) and common mode rejection ratio (CMRR). In modern integrated circuit regulator amplifiers, the utilization of constant current sources gives such large values of PSRR that this effect on V_O can usually be neglected. However, supply voltage changes can affect the output voltage since these changes appear as common mode voltage changes, and they are best measured by the CMRR.

Figure 1–6. Typical Voltage Regulator Configuration

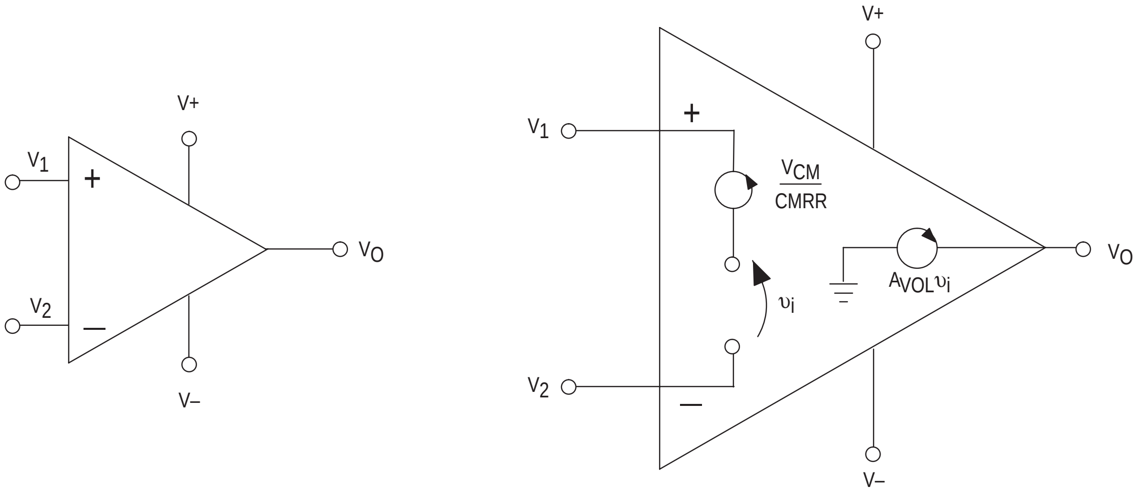


The definition of common mode voltage (V_{CM}), illustrated by Figure 1–7a, is:

$$V_{CM} = \left[\frac{V_1 + V_2}{2}\right] - \left[\frac{(V+) + (V-)}{2}\right] \quad (12)$$

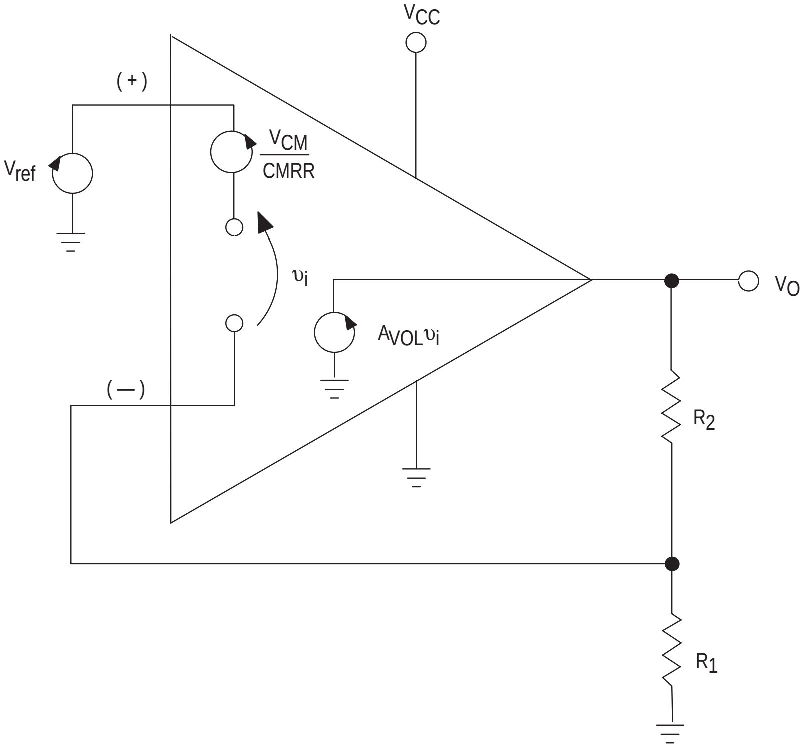
where: V_1 = voltage on amplifier noninverting input
V_2 = voltage on amplifier inverting input
V+ = positive supply voltage
V– = negative supply voltage

Figure 1–7. Definition of Common Mode Voltage Error



(a) **(b)**

Figure 1–8. Common Mode Regulator Effects



In an ideal amplifier, only the differential input voltage ($V_1 – V_2$) has any effect on the output voltage; the value of V_{CM} would not effect the output. In fact, V_{CM} does influence the amplifier output voltage. This effect can be modeled as an additional voltage offset at the amplifier input equal to V_{CM}/CMRR as shown in Figures 1–7b and 1–8. The latter figure is the same configuration as Figure 1–6, with amplifier input offset voltage and output impedance deleted for clarity and common mode voltage effects added. The output voltage of this configuration is given by:

$$V_O = A_{VOL}\,\upsilon_i = A_{VOL}\left(V_{ref} - \frac{V_{CM}}{CMRR} - \beta V_O\right) \tag{13}$$

Manipulating,

$$V_O = \frac{\left(V_{ref} - \frac{V_{CM}}{CMRR}\right)}{\beta + \frac{1}{A_{VOL}}} \tag{14}$$

where: $V_{CM} = V_{ref} - \frac{V_{CC}}{2}$ (15)

and, CMRR = common mode rejection ratio

It can be seen from Equations (14) and (15) that the output can vary when V_{CC} varies. This can be reduced by designing the amplifier to have a high A_{VOL}, a high CMRR, and by choosing the feedback ratio (β) to be unity.

3. Amplifier Output Impedance

Referring back to Equation (9), it can be seen that the equivalent regulator output impedance (Z_O) is given by:

$$Z_O = \frac{\Delta V_O}{\Delta I_O} \simeq \frac{Z_{OL}}{\beta A_{VOL}} \qquad (16)$$

This impedance must be as low as possible, in order to minimize load current effects on the output voltage. This can be accomplished by lowering Z_{OL}, choosing an amplifier with high A_{VOL}, and by selecting the feedback ratio (β) to be unity.

A simple way of lowering the effective value of Z_{OL} is to make an impedance transformation with an emitter follower, as shown in Figure 1–9. Given a change in output current (ΔI_O) the amplifier will see a change of only $\Delta I_O/h_{FEQ1}$ in its output current (I_O'). Therefore, (Z_{OL}) in Equation (16) has been effectively reduced to Z_{OL}/h_{FEQ1}, reducing the overall regulator output impedance (Z_O).

D. The Regulator within a Regulator Approach

In the preceding text, we have analyzed the sections of an integrated circuit voltage regulator and determined how they contribute to its non–ideal performance characteristics. These are shown in Table 1–1 along with procedures which minimize their effects.

It can be seen that in all cases regulator performance can be improved by selecting A_{VOL} as high as possible and $\beta = 1$. Since a limit is soon approached in how much A_{VOL} can be practically obtained in an integrated circuit amplifier, selecting a feedback ratio (β) equal to unity is the only viable way of improving total regulator performance, especially in reducing regulator output impedance. However, this method presents a basic problem to the regulator designer. If the configuration of Figure 1–6 is used, the output voltage cannot be adjusted to a value other than V_{ref}. The solution is to utilize a different regulator configuration known as the *regulator within a regulator* approach.(2) Its greatest benefit is in reducing total regulator output impedance.

Figure 1–9. Emitter Follower Output

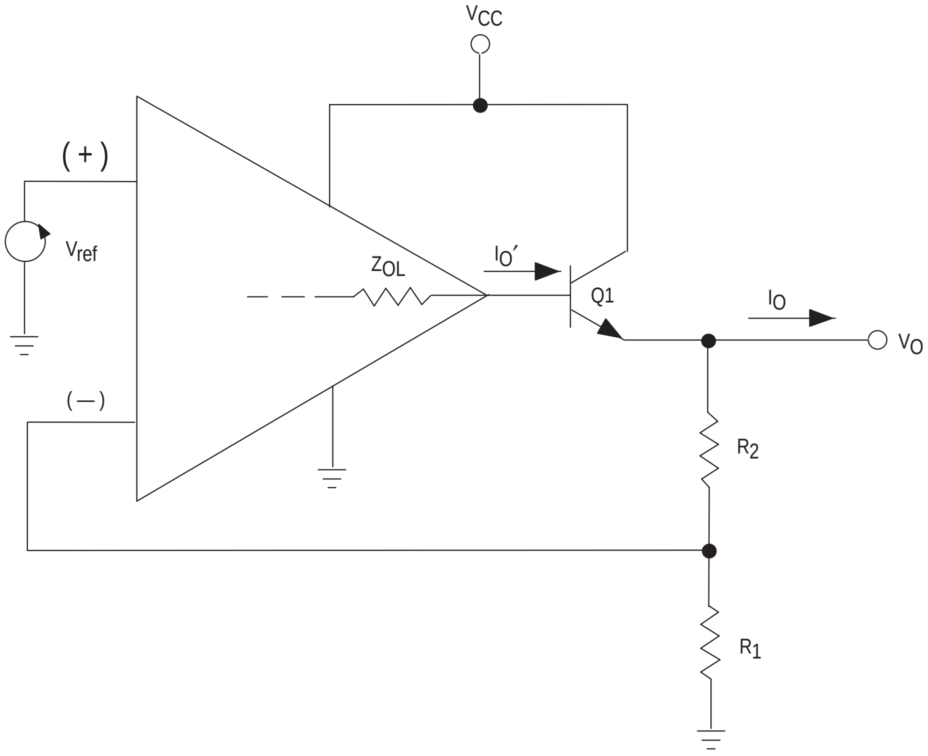


Table 1–1

V_O Changes Section	Effect Can Be Induced By:	Minimized By Selecting:
Reference	V_{CC}	• Constant current–zener method • Bandgap reference
	T_J	• Bandgap reference • TC compensated zener method
Amplifier	V_{CC}	• High CMRR amplifier • High A_{VOL} amplifier • $\beta = 1$
	T_J	• Low V_{IO} drift amplifier • High A_{VOL} amplifier • $\beta = 1$
	I_O	• Low Z_{OL} amplifier • High A_{VOL} amplifier • Additional emitter follower output • $\beta = 1$

As shown in Figure 1–10, amplifier A1 sets up a voltage (V_1) given by:

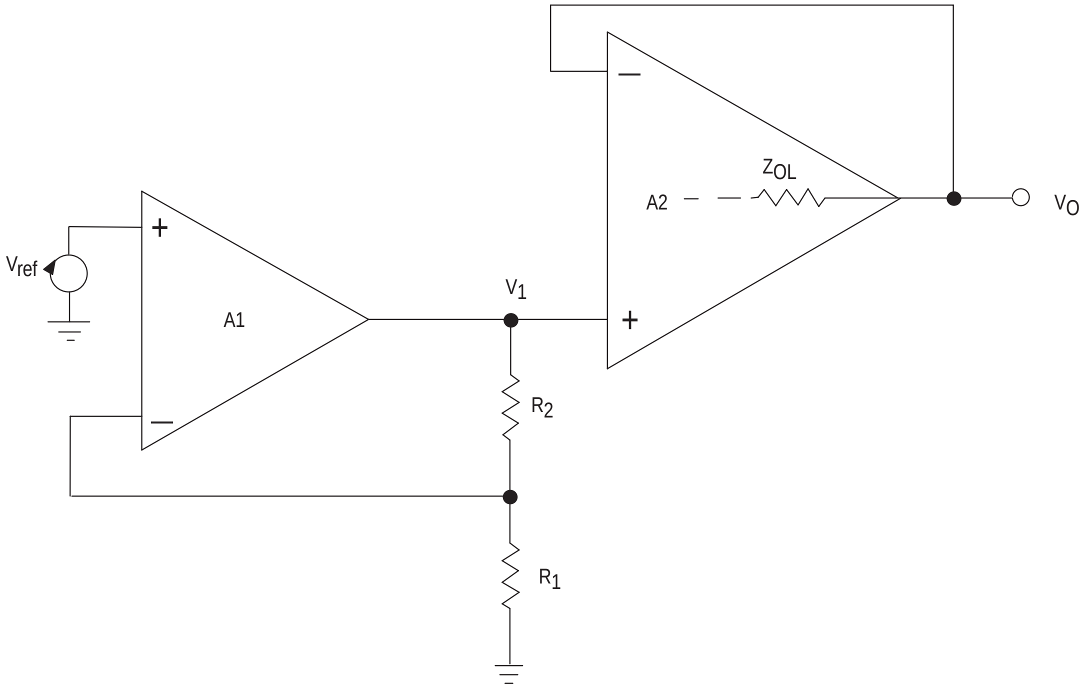
$$V_1 \simeq V_{ref}\left(1 + \frac{R_2}{R_1}\right) \tag{17}$$

V_1 now serves as the reference voltage for amplifier A2, whose output voltage (V_O) is given by:

$$V_O \simeq V_1 \simeq V_{ref}\left(1 + \frac{R_2}{R_1}\right) \tag{18}$$

Note that the output impedance of A2, and therefore the regulator output impedance, has been minimized by selecting A2's feedback factor to be unity; and that output voltage can still be set at voltages greater than V_{ref} by adjusting R_1 and R_2.

Figure 1–10. The "Regulator within a Regulator" Configuration



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(1)Widlar, R. J., *New Developments in IC Voltage Regulators*, IEEE Journal of Solid State Circuits, Feb.1971, Vol. SC–6, pgs. 2–7.

(2)Tom Fredericksen, IEEE Journal of Solid State Circuits, Vol. SC–3, Number 4, Dec. 1968, *A Monolithic High Power Series Voltage Regulator*.

SECTION 2

SELECTING A LINEAR IC VOLTAGE REGULATOR

A. Selecting the Type of Regulator

There are five basic linear regulator types; positive, negative, fixed output, tracking and floating regulators. Each has its own particular characteristics and best uses, and selection depends on the designer's needs and trade–offs in performance and cost.

1. Positive Versus Negative Regulators

In most cases, a positive regulator is used to regulate positive voltages and a negative regulator negative voltages. However, depending on the system's grounding requirements, each regulator type may be used to regulate the "opposite" voltage.

Figures 2–1a and 2–1b show the regulators used in the conventional and obvious mode. Note that the ground reference for each (indicated by the heavy line) is continuous. Several positive regulators could be used with the same input supply to deliver several voltages with common grounds; negative regulators may be utilized in a similar manner.

If no other common supplies or system components operate off the input supply to the regulator, the circuits of Figures 2–1c and 2–1d may be used to regulate positive voltages with a negative regulator and vice versa. In these configurations, the input supply is essentially floated, i.e., neither side of the input is tied to the system ground.

There are methods of utilizing positive regulators to obtain negative output voltages without sacrificing ground bus continuity. However, these methods are only possible at the expense of increased circuit complexity and cost. An example of this technique is shown in Section 3.

2. Three–Terminal, Fixed Output Regulators

These regulators offer the designer a simple, inexpensive way to obtain a source of regulated voltage. They are available in a variety of positive or negative output voltages and current ranges.

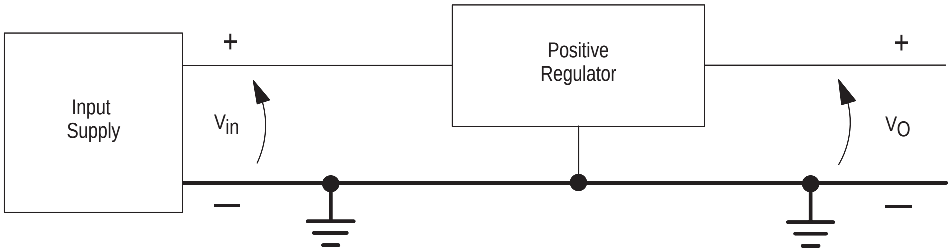
The advantages of these regulators are:

a) Easy to use.
b) Internal overcurrent and thermal protection.
c) No circuit adjustments necessary.
d) Low cost.

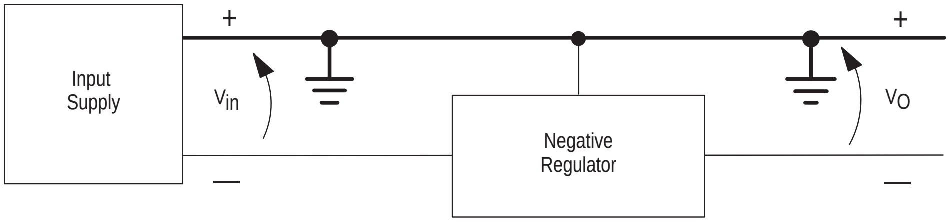
Their disadvantages are:

a) Output voltage cannot be precisely adjusted. (Methods for obtaining adjustable outputs are shown in Section 3).
b) Available only in certain output voltages and currents.
c) Obtaining greater current capability is more difficult than with other regulators. (Methods for obtaining greater output currents are shown in Section 3.)

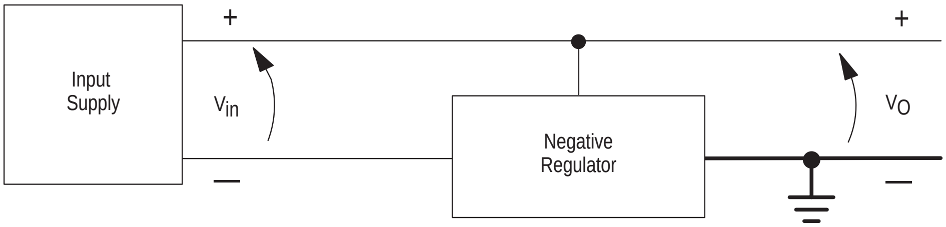
Figure 2–1. Regulator Configurations



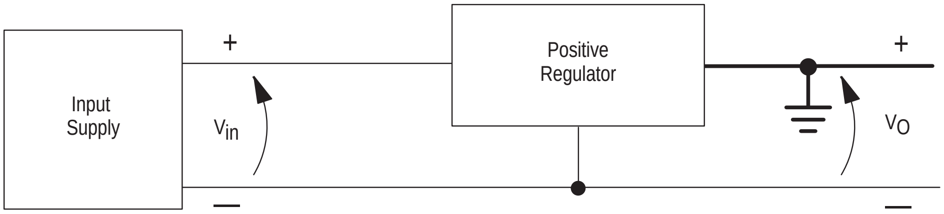
(a) Positive Output Using Positive Regulator



(b) Negative Output Using Negative Regulator



(c) Positive Output Using Negative Regulator



(d) Negative Output Using Positive Regulator

3. Three–Terminal, Adjustable Output Regulators

Like the three–terminal fixed regulators, the three–terminal adjustable regulators are easy and inexpensive to use. These devices provide added flexibility with output voltage adjustable over a wide range, from 1.2 V to nearly 40 V, by means of an external, two–resistor voltage divider. A variety of current ranges from 100 mA to 3.0 A are available.

B. Selecting an IC Regulator

Once the type of regulator is decided upon, the next step is to choose a specific device. To provide higher currents than are available from monolithic technologies, an IC regulator will often be used as a driver to a boost transistor. This complicates the selection and design task, as there are now several overlapping solutions to many of the design problems.

Unfortunately, there is no exact step–by–step procedure that can be followed which will lead to the ideal regulator and circuit configuration for a specific application. The regulating circuit that is finally accepted will be a compromise between such factors as performance, cost, size and complexity. Because of this, the following general design procedure is suggested:

1. Select the regulators which meet or exceed the requirements for line regulation, load regulation, TC of the output voltage and operating ambient temperature range. At this point, do not be overly concerned with the regulator capabilities in terms of output voltage, output current, SOA and special features.

2. Next, select application circuits from Section 3 which meet the requirements for output current, output voltage, special features, etc. Preliminary designs using the chosen regulators and circuit configurations are then possible. From these designs a judgement can be made by the designer as to which regulator circuit configuration combination best meets his or her requirements in terms of cost, size and complexity.

SECTION 3

LINEAR REGULATOR CIRCUIT CONFIGURATION AND DESIGN CONSIDERATIONS

Once the IC regulators, which meet the designer's performance requirements, have been selected, the next step is to determine suitable circuit configurations. Initial designs are devised and compared to determine the IC regulator/circuit configuration that best meets the designer's requirements. In this section, several circuit configurations and design equations are given for the various regulator ICs. Additional circuit configurations can be found on the device data sheets. Organization is first by regulator type and then by variants, such as current boost. Each circuit diagram has component values for a particular voltage and current regulator design.

A. Positive, Adjustable
B. Negative, Adjustable
C. Positive, Fixed
D. Negative, Fixed
E. Tracking
F. Special
    1. Obtaining Extended Output Voltage Range
    2. Electronic Shutdown
G. General Design Considerations

It should be noted that all circuit configurations shown have constant current limiting. If foldback limiting is desired, see Section 4C for techniques and design equations.

A. Positive, Adjustable Output IC Regulator Configurations

1. Basic Regulator Configurations

Positive Three–Terminal Adjustables

These adjustables, comprised of the LM317L, LM317, and LM350 series devices range in output currents of 100 mA, 500 mA, 1.5 A, and 3.0 A respectively. All of these devices utilize the same basic circuit configuration as shown in Figure 3–1A.

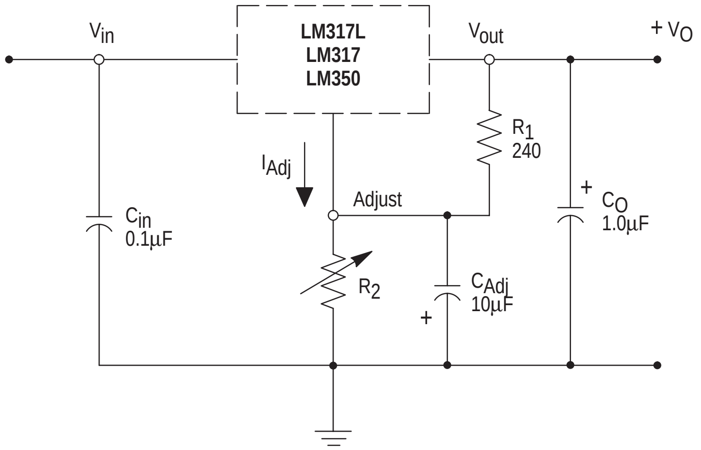
MC1723C

The basic circuit configurations for the MC1723C regulator are shown in Figures 3–2A and 3–3A. For output voltages from $\simeq$ 7.0 V to 37 V the configuration of Figure 3–2A can be used, while Figure 3–3A can be used to obtain output voltages from 2.0 V to $\simeq$ 7.0 V.

2. Output Current Boosting

If output currents greater than those available from the basic circuit configurations are desired, the current boost circuits shown in this section can be used. The output currents which can be obtained with this configurations are limited only by capabilities of the external pass element(s).

Figure 3–1A. Basic Configuration for Positive, Adjustable Output Three–Terminal Regulators



C_{in}: required if regulator is located an appreciable distance from power supply filter.

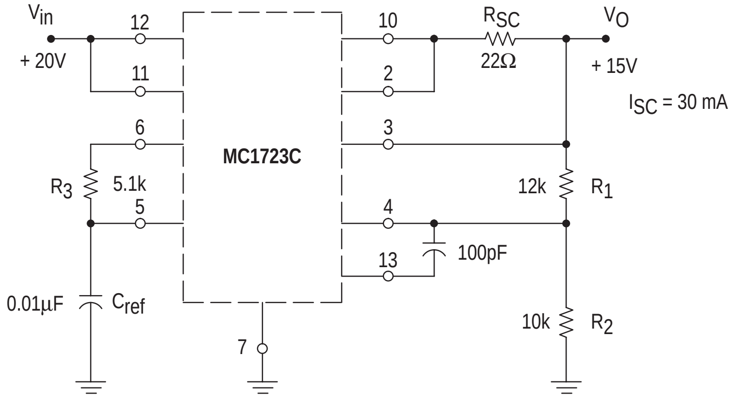
C_O: improves transient response.

C_{Adj}: improves Ripple Rejection.

$$V_{out} = 1.25\ V\ \ 1 + \left(\frac{R_2}{R_1}\right) + I_{Adj}\,R_2$$

Since I_{Adj} is controlled to less than 100 µA, the error associated with this term is negligible in most applications.

Figure 3–2A. MC1723C Basic Circuit Configuration for $V_{ref} \le V_O \le 37$ V



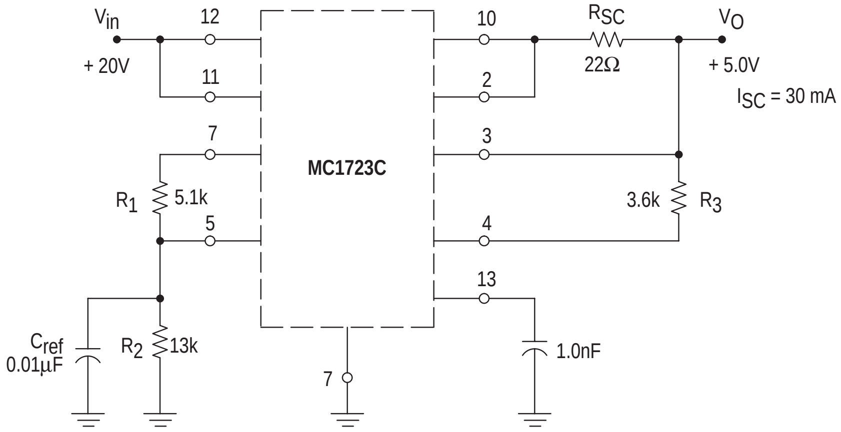
$R_{SC} \cong \frac{0.66\ V}{I_{SC}}$; $10\ k\Omega < R_1 + R_2 < 100\ k\Omega$

$R_3 \cong R_1 \parallel R_2$; $0 \le C_{ref} \le 0.1\ \mu F$

$$R_2 = \frac{V_{ref}}{V_O}\ (R_1 + R_2) \approx \frac{7.0\ V}{V_O}\ (R_1 + R_2)$$

Values shown are for a 15 V, 30 mA regulator using an MC1723CP for a $T_{A(max)}$ = 25°C.

Figure 3–3A. MC1723C Basic Circuit Configuration for 2.0 V ≤ V_O ≤ V_{ref}



$$R_{SC} \simeq \frac{0.66V}{I_{SC}}\ ;\ 10\ k\Omega < R_1 + R_2 < 100\ k\Omega$$

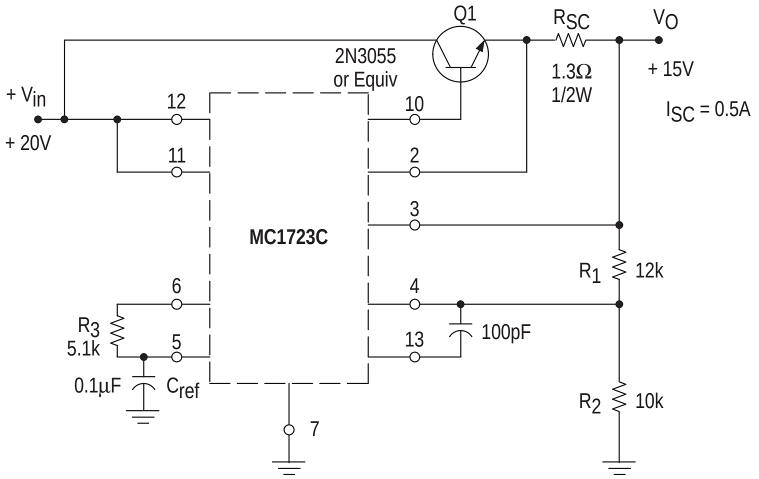
$$R_2 = \frac{V_O}{V_{ref}}\ (R_1 + R_2) \simeq \frac{V_O}{7.0\ V}\ (R_1 + R_2)$$

$$R_3 = R_1 \parallel R_2;\ 0 \le C_{ref} \le 0.1\ \mu F$$

Values shown are for a 5.0 V, 30 mA regulator using an MC1723CP for a $T_{A(max)}$ = 70°C.

To obtain greater output currents with the MC1723C the configurations shown in Figures 3–4A and 3–5A can be used. Figure 3–4A uses an NPN external pass element, while a PNP is used in Figure 3–5A.

Figure 3–4A. MC1723C NPN Boost Configuration



$$R_{SC} \cong \frac{0.66\ V}{I_{SC}}\ ;\ 10\ k\Omega < R_1 + R_2 < 100\ k\Omega$$

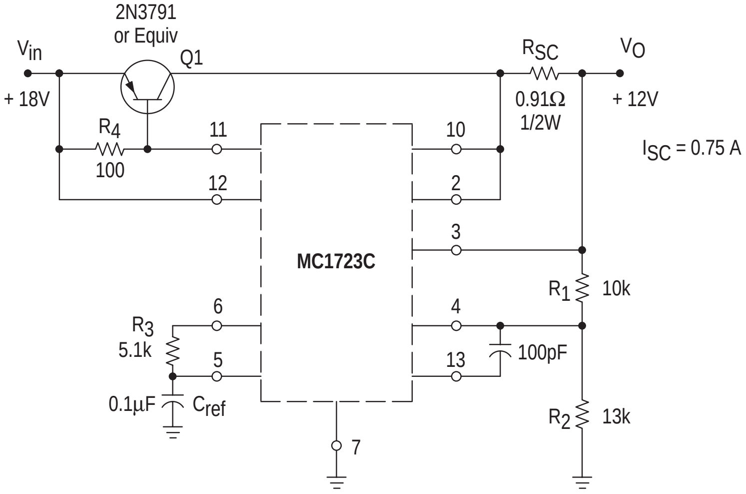
$$R_2 = \frac{V_{ref}}{V_O}\ (R_1 + R_2) \cong \frac{7.0\ V}{V_O}\ (R_1 + R_2)$$

$$0 \le C_{ref} \le 0.1\ \mu F\ ;\ R_3 \cong R_1 \parallel R_2$$

Selection of Q1 based on considerations of Section 4.

Values shown are for a 15 V, 500 mA regulator using an unheatsinked MC1723CP and a 2N3055 on a 6°C/W heatsink for T_A up to + 70°C.

Figure 3–5A. MC1723C PNP Boost Configuration



$R_{SC} \cong \frac{0.66\ V}{I_{SC}}$; $10\ k\Omega < R_1 + R_2 < 100\ k\Omega$; $0 \le C_{ref} \le 0.1\ \mu F$

$R_2 = \frac{V_{ref}}{V_O}(R_1 + R_2) \cong \frac{7.0\ V}{V_O}(R_1 + R_2)$

$R_3 = R_1 \parallel R_2$

$0 < R_4 \le V_{BE_{on\ (Q1)}} / 5.0\ mA$

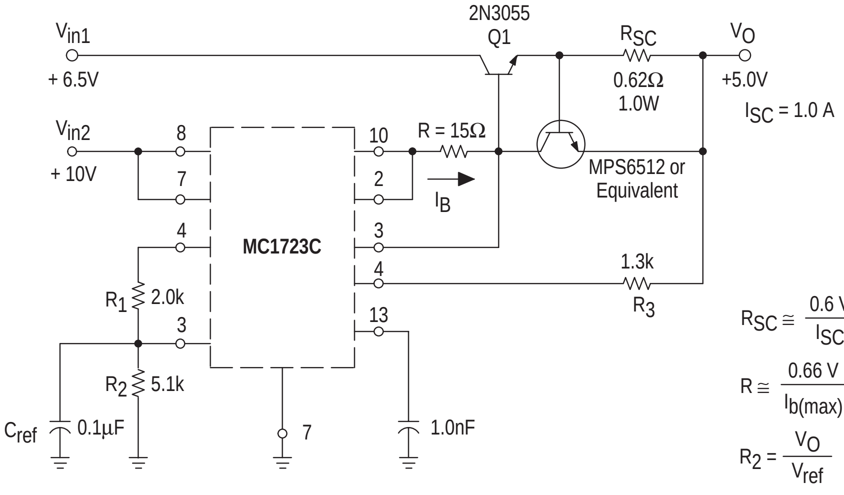
Selection of Q1 based on considerations of Section 4.

Values shown are for a 12 V, 750 mA regulator using an unheatsinked MC1723CP and a 2N3791 on a 4°C/W heatsink for T_A up to + 70°C.

3. High Efficiency Regulator Configurations

When large output currents at voltages under approximately 9.0 V are desired, the configuration of Figure 3–6A can be utilized to obtain increased operating efficiency. This is accomplished by providing a separate low voltage input supply for the pass element. This method, however, usually necessitates that separate short circuit protection be provided for the IC regulator and external pass element. Figure 3–6A shows a high efficiency regulator configuration for the MC1723C.

Figure 3–6A. MC1723C High Efficiency Regulator Configuration



$R_{SC} \cong \frac{0.6\ V}{I_{SC}}$

$R \cong \frac{0.66\ V}{I_{b(max)}}$; $10\ k\Omega < R_1 + R_2 < 100\ k\Omega$

$R_2 = \frac{V_O}{V_{ref}}(R_1 + R_2) \cong \frac{V_O}{7.0\ V}(R_1 + R_2)$

$0 \le C_{ref} \le 0.1\ \mu F$

$R_3 \cong R_1 \parallel R_2$

See Section 3F for general design considerations.
Selection of Q1 based on considerations of Section 4.

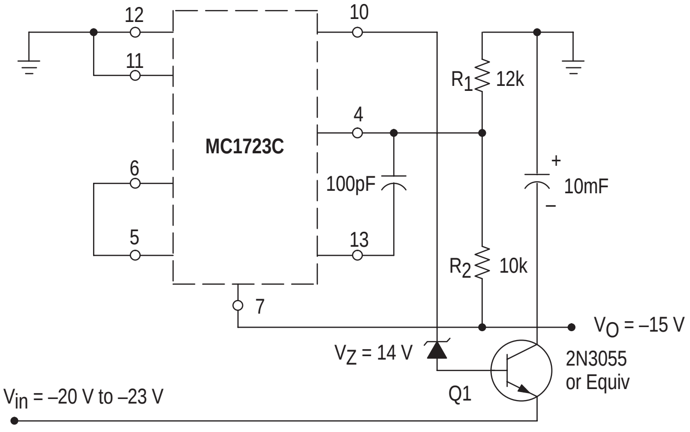
Values shown for a 5.0 V, 1.0 A regulator using an unheatsinked MC1723CP and a 2N3055 on a 10°C/W heatsink for T_A up to + 70°C.

B. Negative, Adjustable Output IC Regulator Configurations

1. Basic Regulator Configurations (MC1723C)

Although a positive regulator, the MC1723C can be used in a negative regulator circuit configuration. This is done by using an external pass element and a zener level shifter as shown in Figure 3–1B. It should be noted that for proper operation, the input supply must not vary over a wide range, since the correct value for V_Z depends directly on this voltage. In addition, it should be noted that this circuit will not operate with a shorted output.

Figure 3–1B. MC1723C Negative Regulator Configuration



$|V_O| \geq 10\ V;\ 10\ k\Omega \leq R_1 + R_2 \leq 100\ k\Omega$

$$R_2 = \frac{V_{ref}}{|V_O|}\ (R_1 + R_2) \cong \frac{7.0\ V}{|V_O|}\ (R_1 + R_2)$$

$V_Z \leq |V_{in}| - V_{BE(Q1)} - 3.0\ V;\ V_Z \geq |V_{in}| - |V_O| - V_{BE(Q1)} + 6.0\ V$

Selection of Q1 based on considerations of Section 4.

Values shown are for a –15 V, 750 mA regulator using the MC1723CP with Q1 mounted on a 20°C/W heatsink at T_A up to +70°C. **Do not short circuit output.**

C. Positive, Fixed Output IC Regulator Configurations

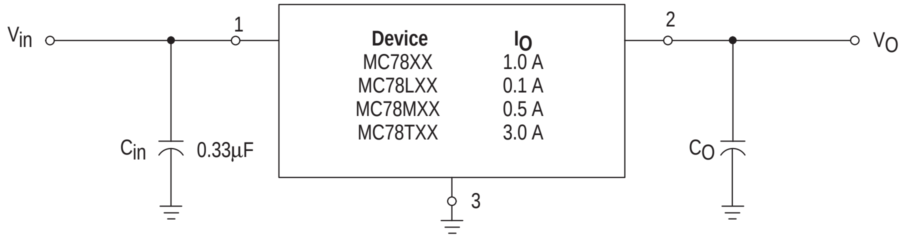
1. Basic Regulator Configuration

The basic current configuration for the positive three–terminal regulators is shown in Figure 3–1C. Depending on which regulator type is used, this configuration can provide output currents in excess of 3.0 A.

2. Output Current Boosting

Figure 3–2C illustrates a method for obtaining greater output currents with the three–terminal positive regulators. Although any of these regulators may be used, usually it is most economical to use the 1.0 A MC7800C in this configuration.

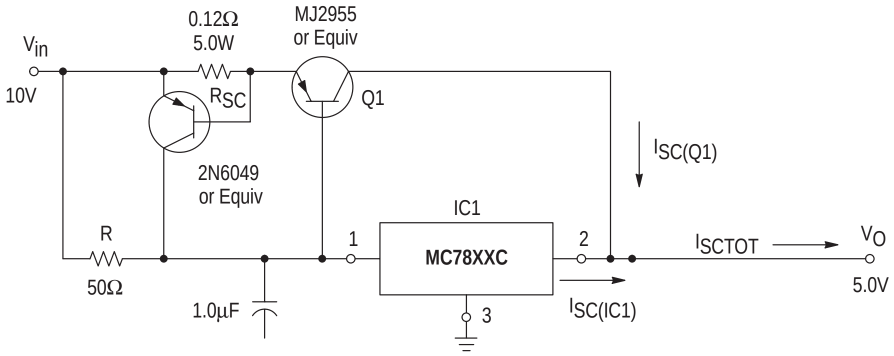
Figure 3–1C. Basic Circuit Configuration for Positive, Fixed Output, Three–Terminal Regulators



C_{in}: required if regulator is located more than a few (≈2 to 4) inches away from input supply capacitor; for long input leads to regulator, up to 1.0 µF may be needed for C_{in}. (C_{in} should be a high frequency type capacitor.)
C_O: improves transient response.
XX: two digits of type number indicating nominal output voltage.

See Section 15 for heatsinking.

Figure 3–2C. Current Boost Configuration for Positive Three–Terminal Regulators



XX: two digits of type number indicating nominal output voltage.
R: used to divert IC regulator bias current and determines at what output current level Q1 begins conducting.

$$0 < R \leq \frac{V_{BE\ on(Q1)}}{I_{Bias\ (IC1)}}\ ;\ R_{SC} \approx \frac{0.6\ V}{I_{SC(Q1)}}\ ;\ I_{SCTOT} = I_{SC(Q1)} + I_{SC(IC1)}$$

Selection of Q1 based on considerations of Section 4.

Values shown are for a 5.0 V, 5.0 A regulator using an MC7805CT on a 2.5°C/W heatsink and Q1 on a 1°C/W heatsink for T_A up to 70°C.

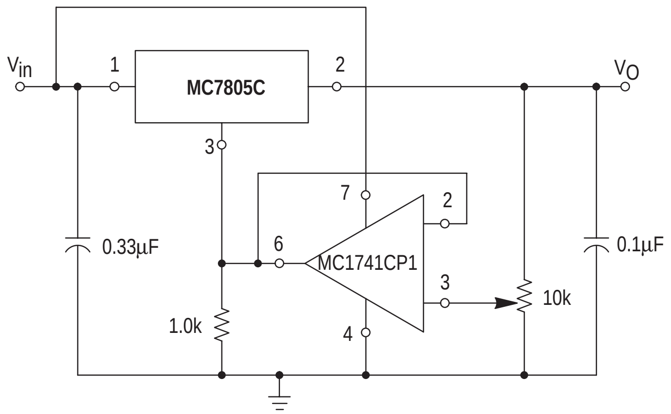
3. Obtaining an Adjustable Output Voltage

With the addition of an op amp, an adjustable output voltage supply can be obtained with the MC7805C. Regulation characteristics of the three–terminal regulators are retained in this configuration, shown in Figure 3–3C. If lower output currents are required, then an MC78M05C (0.5 A) could be used in place of the MC7805C.

4. Current Regulator

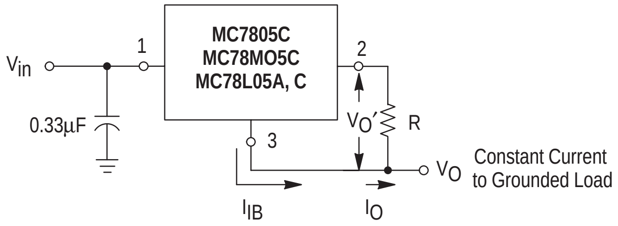
In addition to providing voltage regulation, the three–terminal positive regulators can also be used as current regulators to provide a constant current source. Figure 3–4C shows this configuration. The output current can be adjusted to any value from ≈ 8.0 mA (I_Q, the regulator bias current) up to the available output current of the regulator. Five–volt regulators should be used to obtain the greatest output voltage compliance range for a given input voltage.

Figure 3–3C. Adjustable Output Voltage Configuration Using a Three–Terminal Positive Regulator



V_O = 7.0 V to 33 V
$V_{in} - V_O \geq 2.0$ V
$V_{in} \geq 35$ V

Figure 3–4C. Current Regulator Configuration



$$I_O = \frac{V_O'}{R} + I_{IB}$$

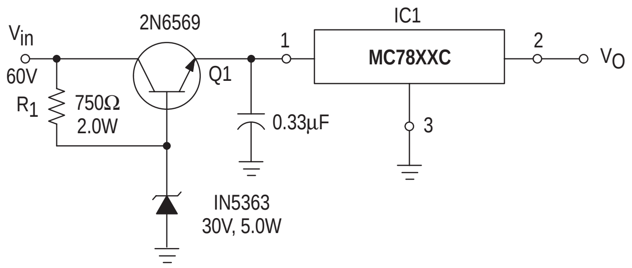
$$\text{Current Reg } \Delta I_O = \frac{\Delta V_O'}{R} + \Delta I_{IB}$$

$$V_O + V_O' + 2.0\text{ V} \leq V_{in} \leq 35\text{ V}$$

5. High Input Voltage

Occasionally, it may be necessary to power a three–terminal regulator from a supply voltage greater than $V_{in(max)}$, 35 V or 40 V. In these cases a preregulator circuit, as shown in Figure 3–5C, may be used.

Figure 3–5C. Preregulator for Input Voltages Above $V_{in(max)}$



$$R_1 = \left(\frac{V_{in} - 30}{1.5}\right) \bullet h_{fe(Q1)}$$

$$V_{CEO(Q1)} \leq V_{in}$$

XX: two digits of type number indicating nominal output voltage.

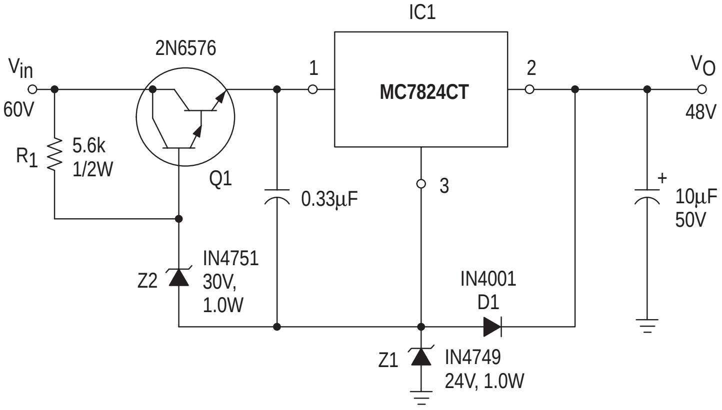
Values shown for V_{in} = 60 V

Q1 should be mounted on a 2°C/W heatsink for operation at T_A up to +70°C. IC1 should be appropriately heatsinked for the package type used.

6. High Output Voltage

If output voltages above 24 V are desired, the circuit configuration of Figure 3–6C may be used. Zener diode (Z1) sets the output voltage, while Q1, Z2, and D1 assure that the MC7824C does not have more than 30 V across it during short circuit conditions.

Figure 3–6C. High Output Voltage Configuration for Three–Terminal Positive Regulators



$$V_O = V_{Z1} + 24;\ R_1 = \left(\frac{V_{in} - (V_{Z1} + V_{Z2})}{1.5}\right) \bullet h_{fe(Q2)}$$

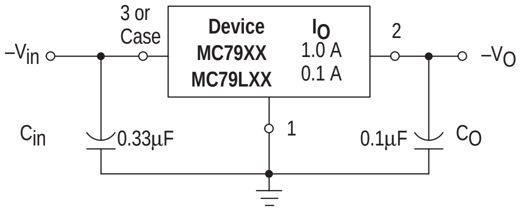
Values shown are for a 48 V, 1.0 A regulator
Q1 mounted on a 10°C/W heatsink
and IC1 mounted on a 2°C/W heatsink for T_A up to +70°C.

D. Negative, Fixed Output IC Regulator Configurations

1. Basic Regulator Configurations

Figure 3–1D gives the basic circuit configuration for the MC79XX and MC79LXX three–terminal negative regulators.

Figure 3–1D. Basic Circuit Configuration for Negative Three–Terminal Regulators



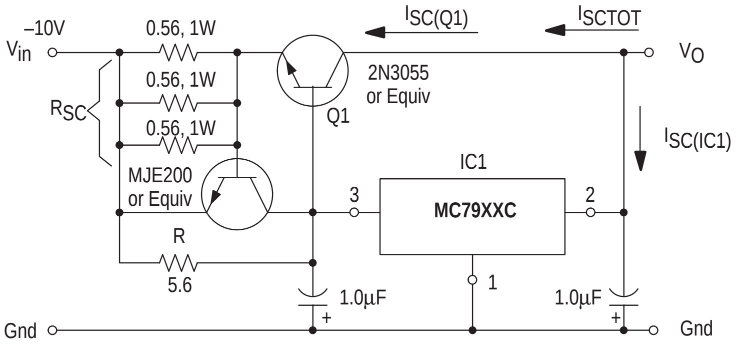
C_{in}: required if regulator is located more than a few (≈ 2 to 4) inches away from input supply capacitor; for long input leads to regulator, up to 1.0 µF may be required. C_{in} should be a high frequency type capacitor.
C_O: improves stability and transient response.
XX: two digits of type number indicating nominal output voltage.

See Section 15 for heatsinking.

Output Current Boosting

In order to obtain increased output current capability from the negative three–terminal regulators, the current boost configuration of Figure 3–2D may be used. Currents which can be obtained with this configuration are limited only by the capabilities of the external pass transistor(s).

Figure 3–2D. Output Current Boost Configuration for Three–Terminal Negative Regulators



XX: two digits of type number indicating output voltage. See Section 2 for available voltages.
R: used to divert regulator bias current and determine at what output current level Q1 begins conducting.

$$O < R \le \frac{V_{BE\ on(Q1)}}{I_{Bias(IC1)}}$$

$$I_{SCTOT} = I_{SC(Q1)} + I_{SC(IC1)}$$

$$R_{SC} \approx \frac{0.6\ V}{I_{SC(Q1)}}$$

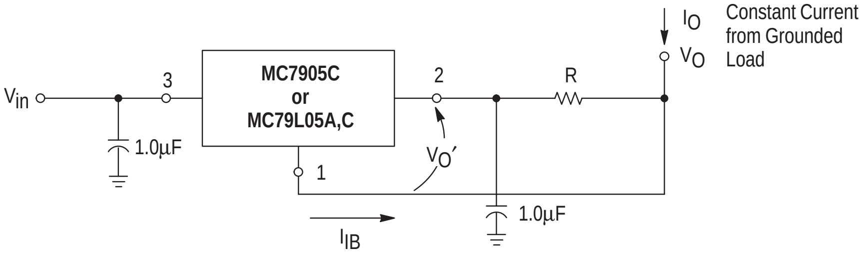
Selection of Q1 based on considerations of Section 4.

Values shown are for a –5.0 V, +4.0 A regulator; using an MC7905CT on a 1.5°C/W heatsink with Q1 mounted on a 1°C/W heatsink for T_A up to +70°C.

2. Current Regulator

The three–terminal negative regulators may also be used to provide a constant current sink, as shown in Figure 3–3D. In order to obtain the greatest output voltage compliance range at a given input voltage, the MC7905C or MC79L05C should be used in this configuration.

Figure 3–3D. Current Regulator Configuration for the Three–Terminal Negative Regulators



$V_{in} \ge -35$ V for MC7905C
$V_{in} \ge -30$ V for MC79L05C
$V_{in} \le V_O + V_O - 2.0$ V

$$I_O = \frac{V_O'}{R} + I_{IB}$$

Current regulation: $\Delta I_O = \dfrac{\Delta V_O'}{R} + \Delta I_{IB}$

F. General Design Considerations

In addition to the design equations given in the regulator circuit configuration panels of Sections 3A–E, there are a few general design considerations which apply to all regulator circuits. These considerations are given below.

1. Regulator Voltages

For any circuit configuration, the worse–case voltages present on each pin of the IC regulator must be within the maximum and/or minimum limits specified on the device data sheets. These limits are instantaneous values, not averages.

They include:
a. $V_{in(min)}$
b. $V_{in(max)}$
c. $(V_{in} - V_{out})$ min
d. $V_{out(min)}$
e. $V_{out(max)}$

For example, the voltage between Pins 12 and 7 (V_{in}) of an MC1723CP must never fall below 9.5 V, even instantaneously, or the regulator will not function properly, (see Figure 3–1B).

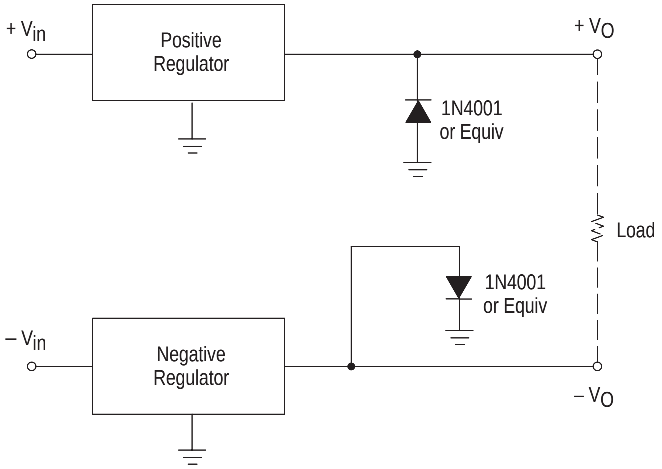
2. Regulator Power Dissipation, Junction Temperature and Safe Operating Area

The junction temperature, power dissipation output current or safe operating area limits of the IC regulator *must never be exceeded*.

3. Operation with a Load Common to a Voltage of Opposite Polarity

In many cases, a regulator powers a load which is not connected to ground but instead is connected to a voltage source of opposite polarity (e.g. op amps, level shifting circuits, etc.). In these cases, a clamp diode should be connected to the regulator output as shown in Figure 3–1F. This protects the regulator, during startup and short circuit operation, from output polarity reversals.

Figure 3–1F. Output Polarity Reversal Protection



4. Reverse Bias Protection

Occasionally, there exists the possibility that the input voltage to the regulator can collapse faster than the output voltage. This could occur, for example, if the input supply is “crowbarred” during an output overvoltage condition. If the output voltage is greater ≈ 7.0 V, the emitter–base junction of the series pass element (internal or external) could break down and be damaged. To prevent this, a diode shunt can be employed, as shown in Figure 3–2F.

Figure 3–3F shows a three–terminal positive–adjustable regulator with the recommended protection diodes for output voltages in excess of 25 V, or high output capacitance values ($C_O > 25\ \mu F$, $C_{Adj} > 10\ \mu F$). Diode D1 prevents C_O from discharging through the regulator during an input short circuit. Diode D2 protects against capacitor C_{Adj} from discharging through the regulator during an output short circuit. The combination of diodes D1 and D2 prevents C_{Adj} from discharging through the regulator during an input short circuit.

Figure 3–2F. Reverse Bias Protection

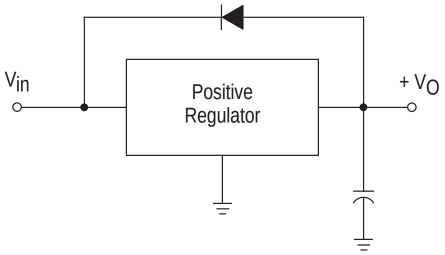
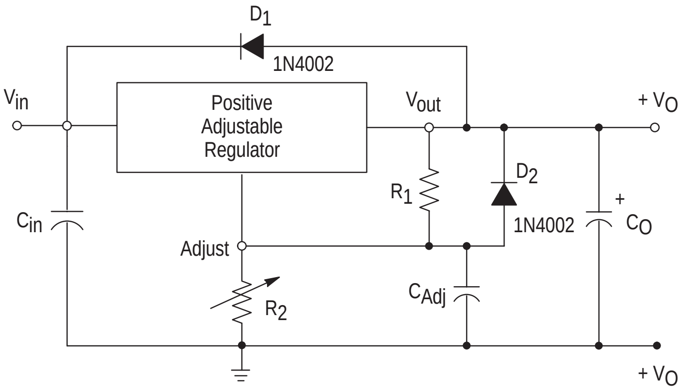


Figure 3–3F. Reverse Bias Protection for Three–Terminal Adjustable Regulators



SECTION 4

SERIES PASS ELEMENT CONSIDERATIONS FOR LINEAR REGULATORS

Presently, most monolithic IC voltage regulators that are available have output current capabilities from 100 mA to 3.0 A. If greater current capability is required, or if the IC regulator does not possess sufficient safe–operating–area (SOA), the addition of an external series pass element is necessary.

In this section, configurations, specifications and current limit techniques for external series pass elements will be considered. For illustrative purposes, pass elements for only positive regulator types will be discussed. However, the same considerations apply for pass elements used with negative regulators.

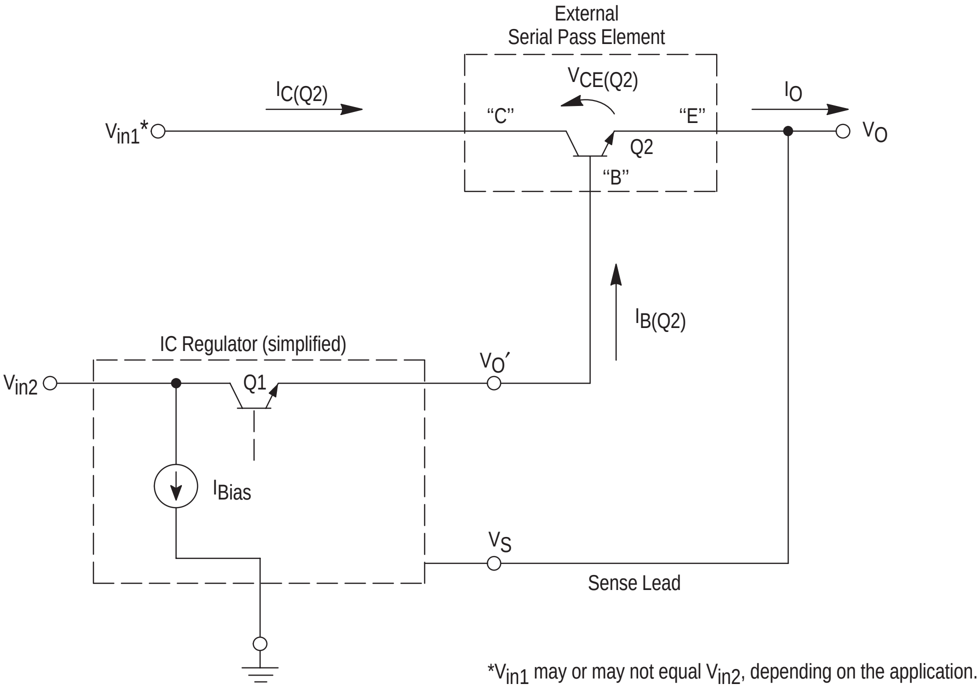
A. Series Pass Element Configurations

Using an NPN Type Transistor

If the IC regulator has an external sense lead, an NPN type series pass element may be used, as shown in Figure 4–1 A. This pass element could be a single transistor or multiple transistors arranged in Darlington and/or paralleled configurations.

In this configuration, the IC regulator supplies the base current (I_B) to the pass element (Q2) which acts as a current amplifier and provides the increased output current (I_O) capability.

Figure 4–1A. NPN Type Series Pass Element Configuration

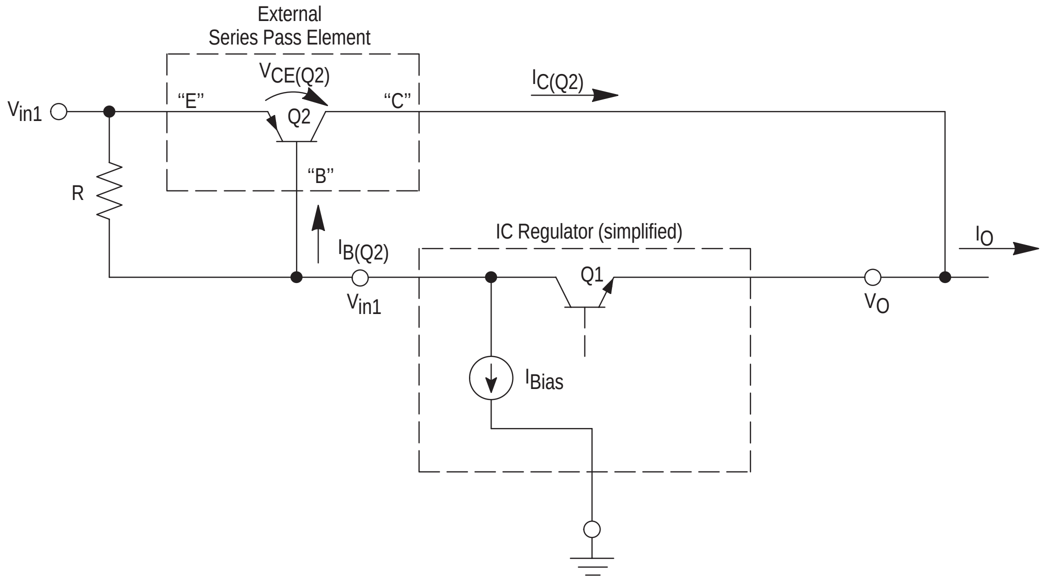


*V_{in1} may or may not equal V_{in2}, depending on the application.

Using a PNP Type Transistor

If the IC regulator does not have an external sense lead, as in the case of the three–terminal fixed output regulators, the configuration of Figure 4–1B can be used. (Regulators which possess an external sense lead may also be used with this configuration.) As before, the PNP type pass element can be a single transistor or multiple transistors.

Figure 4–1B. PNP Type Series Pass Element Configuration



This configuration functions in a similar manner to that of Figure 4–1A, in that the regulator supplies base current to pass element. The resistor (R) serves to route the IC regulator bias current (I_{Bias}) away from the base of Q2. If not included, regulation would be lost at low output currents. The value of R is low enough to prevent Q2 from turning on when I_{Bias} flows through this resistor, and is given by:

$$0 < R \le \frac{V_{BEon}(Q2\ )}{I_{Bias}} \tag{4.0}$$

B. Series Pass Element Specifications

Independent of which configuration is utilized, the transistor or transistors that compose the pass element must have adequate ratings for $I_{C(max)}$, V_{CEO}, h_{fe}, power dissipation, and safe operating area.

1. $I_{C(max)}$ — for the pass element of Figure 4–1A, $I_{C(max)}$ is given by:

$$I_{C(max)(Q2)} \ge I_{O(max)} - I_{B(max)(Q2)} = I_{O(max)} - \frac{I_{C(max)(Q2)}}{h_{fe(Q2)}} \tag{4.1}$$

$$\ge I_{O(max)} \tag{4.2}$$

For the configuration of Figure 4–1B:

$$I_{C(max)(Q2)} \ge I_{O(max)} + I_{B(max)(Q2)} \tag{4.3}$$

$$\ge I_{O(max)} \tag{4.4}$$

2. **V_{CEO} —** since $V_{CE(Q2)}$ is equal to $V_{in1(max)}$ when the output is shorted or during start up:

$$V_{CEO(Q2)} \leq V_{in1(max)} \tag{4.5}$$

3. **h_{fe} —** the minimum DC current gain for Q2 in Figures 4–1A and 4–1B is given by:

$$h_{fe(min)(Q2)} \geq \frac{I_{C(max)(Q2)}}{I_{B(max)(Q2)}} \ @\ V_{CE} = (V_{in1(min)} - V_O) \tag{4.6}$$

4. Maximum Power Dissipation $P_{D(max)}$, and Safe Operating Area (SOA)

For any transistor there are certain combinations of I_C and V_{CE} at which it may safely be operated. When plotted on a graph, whose axes are V_{CE} and I_C, a safe–operating region is formed.

As an example, the safe–operating–area (SOA) curve for the well known 2N3055 NPN silicon power transistor is shown in Figure 4–2. The boundaries of the SOA curve are formed by $I_{C(max)}$, power dissipation, second breakdown and V_{CEO} ratings of the transistor. Notice that the power dissipation and second breakdown ratings are given for a case temperature of +25°C and must be derated at higher case temperatures. (Derating factors may be found in the transistors' data sheets.) These boundaries must never be exceeded during operation, or destruction of the transistor(s) which constitute the pass element may result. (In addition, the maximum operating junction temperature *must not be exceeded*, see Section 15.)

C. Current Limiting Techniques

In order to select a transistor or transistors with adequate SOA, the locus of pass element I_C and V_{CE} operating points must be known. This locus of points is determined by the input voltage (V_{in1}, output voltage (V_O), output current (I_O) and the type of output current limiting technique employed.

In most cases, V_{in1}, V_O, and the required output current are already known. All that is left to determine is how the chosen current limit scheme affects required pass element SOA.

Note, since the external pass element is merely an extension of the IC regulator, the following discussions apply equally well to IC regulators not using an external pass element.

1. Constant Current Limiting

This method is the simplest to implement and is extensively used, especially at the lower output current levels. The basic circuit configuration is shown in Figure 4–3A, and operates in the following manner.

As the output current increases, the voltage drop across R_{SC} increases, proportionately. When the output current has increased to the point that the voltage drop across R_{SC} is equal to the base–emitter ON voltage of Q3 (V_{BEon}(Q3)), Q3 conducts. This diverts base current (I_{Drive}) away from Q1, the IC regulator's internal series pass element. Base drive ($I_{B(Q2)}$) of Q2 is therefore reduced and its collector–emitter voltage increases, thereby reducing the output voltage below its regulated value, V_{out}. The resulting output voltage–current characteristic is shown in Figure 4–3B.

The value of I_{SC} is given by:

$$I_{SC} = \frac{V_{BEon(Q3)}}{R_{SC}} \tag{4.7}$$

Figure 4–2. 2N3055 Safe Operating Area (SOA)

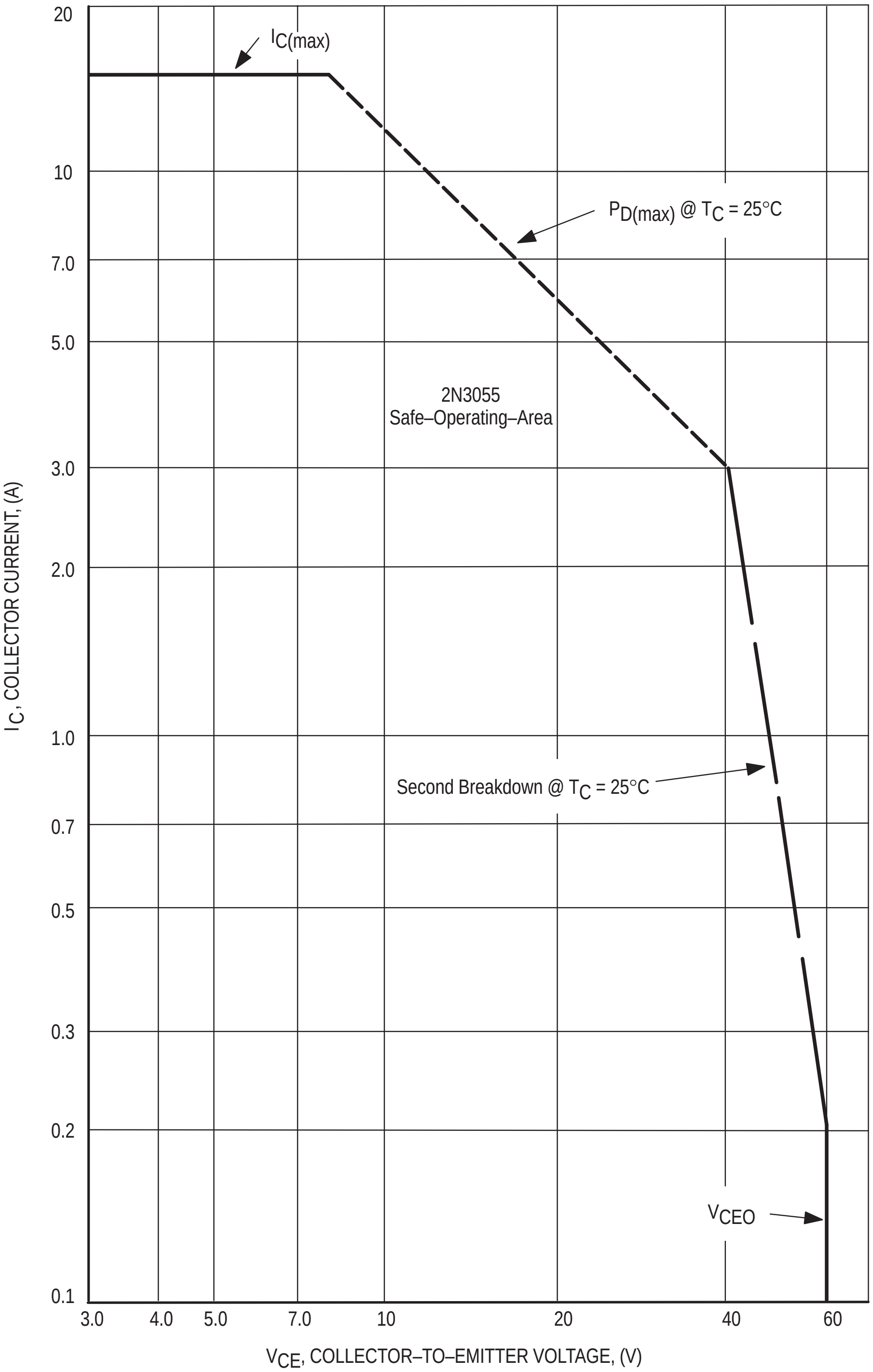
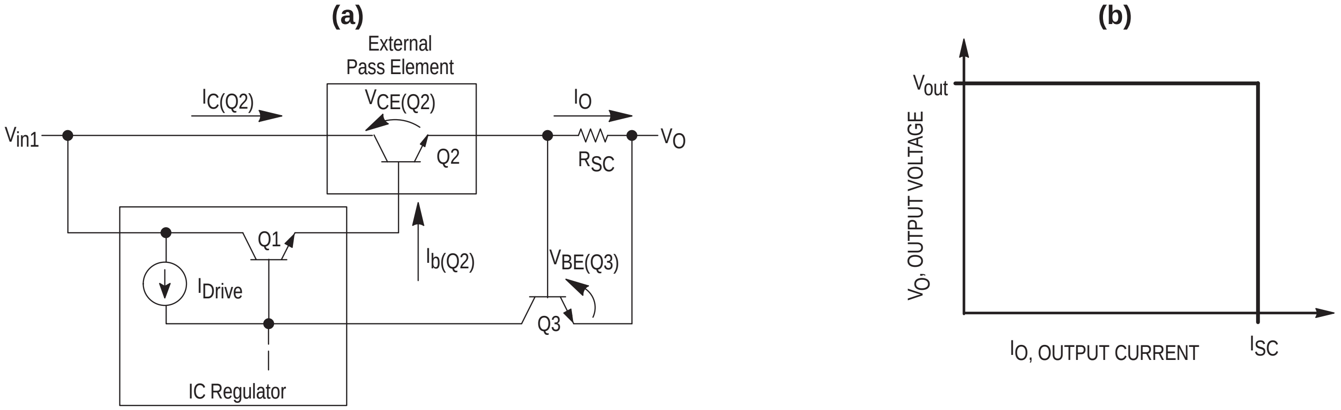


Figure 4–3. Constant Current Limiting



By using the base of Q1 in the IC regulator as a control point, this configuration has the added benefit of limiting the IC regulator output current ($I_{B(Q2)}$) to Isc/$h_{fe(Q2)}$, as well as limiting the collector current of Q2 to I_{SC}. Of course, access to this point is necessary. Fortunately, it is usually available in the form of a separate pin or as the regulator's compensation terminal.(1)

The required safe–operating–area for Q2 can be obtained by plotting the V_{CE} and I_C of Q2 given by:

$$V_{CE(Q2)} = V_{in1} - V_O - I_O R_{SC} \simeq V_{in1} - V_O \tag{4.8}$$

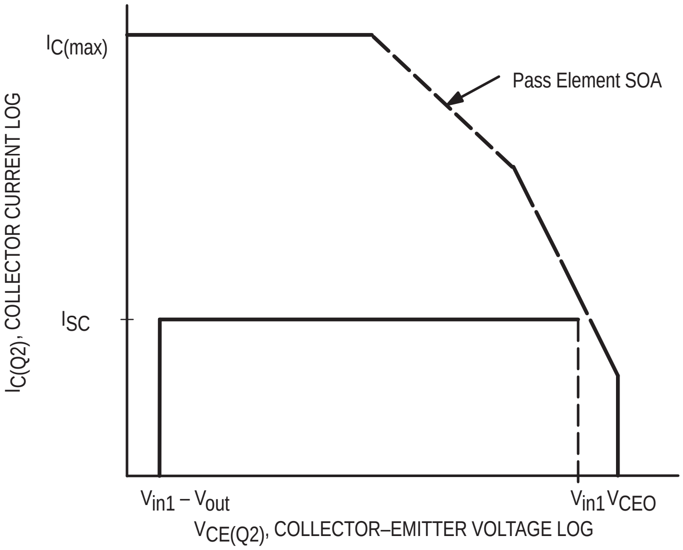
$$I_{C(Q2)} \simeq I_O \tag{4.9}$$

$$\text{where, } V_O = V_{out} \text{ for } 0 \le I_O \le I_{SC} \tag{4.10}$$

$$\text{and, } I_O = I_{SC} \text{ for } 0 \le V_O \le V_{out} \tag{4.11}$$

The resulting plot is shown in Figure 4–4. The transistor chosen for Q2 must have an SOA which encloses this plot, see Figure 4–4. Note that the greatest demand on the transistor's SOA capability occurs when the output of the regulator is short circuited and the pass element must support the full input voltage and short circuit current simultaneously.

Figure 4–4. Constant Current Limit SOA Requirements
(See Section 3 for Circuit Techniques)



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(1) The three–terminal regulators have internal current limiting and therefore do not provide access to this point. If an external pass element is used with these regulators, constant current limiting can still be accomplished by diverting pass element drive.

2. Foldback Current Limiting

A disadvantage of the constant current limit technique is that in order to obtain sufficient SOA the pass element must have a much greater collector current capability than is actually needed. If the short circuit current could be reduced, while still allowing full output current to be obtained during normal regulator operation, more efficient utilization of the pass elements SOA capability would result. This can be done by using a “foldback” current limiting technique instead of constant current limiting.

The basic circuit configuration for this method is shown in Figure 4–5(A). The circuit operates in a manner similar to that of the constant current limiting circuit, in that output current control is obtained by diverting base drive away from Q1 with Q3.

At low output currents, V_A approximately equals V_O and V_{R2} is less than than V_O. Q3 is therefore non–conducting and the output voltage remains constant. As the output current increases, the voltage drop across R_{SC} increases until V_A and V_{R2} are great enough to bias Q3 on. The output current at which this occurs is I_K, the “knee” current.

Figure 4–5. Foldback Current Limiting

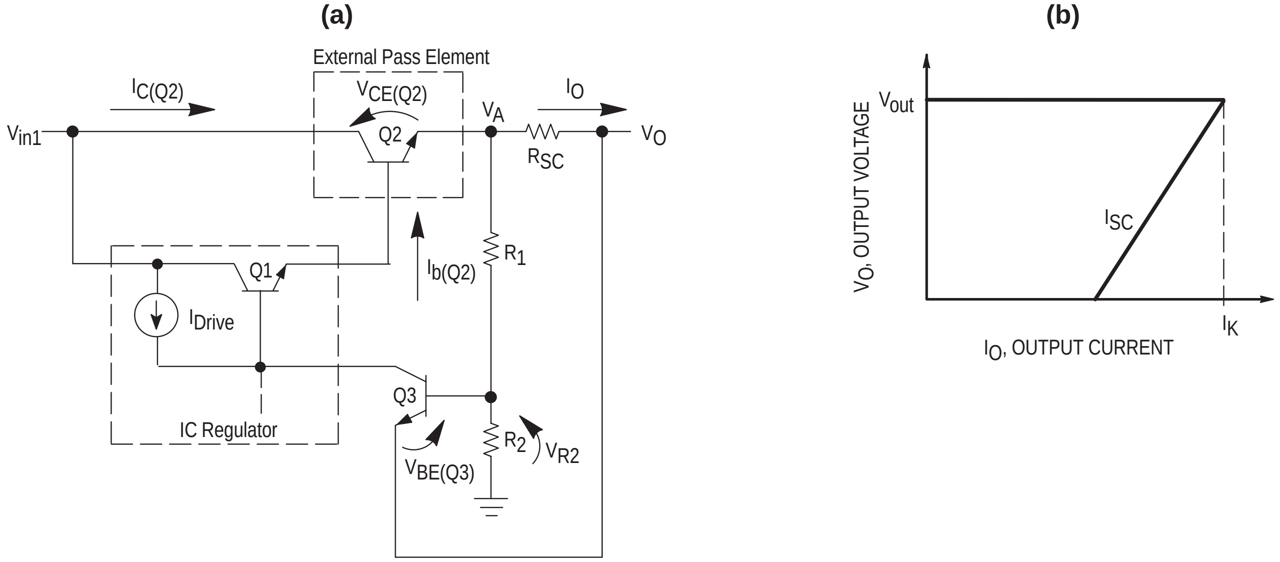
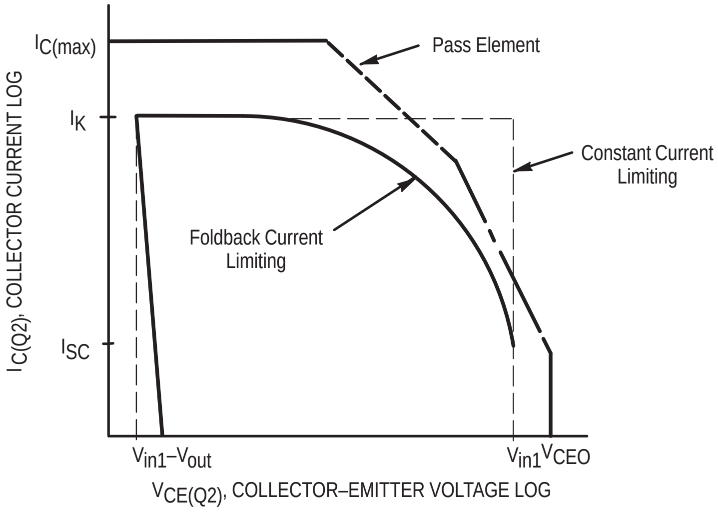


Figure 4–6. Foldback Current Limit SOA Requirements



The output voltage will now decrease. Less output current is now required to keep V_A and V_{R2} at a level sufficient to bias Q3 on since the voltage at its emitter has the tendency to decrease faster than that at its base. The output current will continue to “foldback” as the output voltage decreases, until an output short circuit current level (I_{SC}) is reached when the output voltage is zero. The resulting output current–voltage characteristic is shown in Figure 4–5B. The values for R_1, R_2, and R_{SC} (neglecting base current of Q3) are given by:

$$R_{SC} = \frac{V_{out}/I_{SC}}{\left(1 + \frac{V_{out}}{V_{BEon(Q3)}}\right) - \frac{I_K}{I_{SC}}} \tag{4.12}$$

$$\frac{R_2}{R_1 + R_2} = \frac{V_{BEon(Q3)}}{I_{SC}\,R_{SC}} \tag{4.13}$$

$$\text{and, } R_1 + R_2 \leq \frac{V_{out}}{I_{Drive}} \tag{4.14}$$

where: V_{out} = normal regulator output voltage
I_K = knee current
I_{SC} = short circuit current
I_{Drive} = base drive to regulator’s internal pass element(s)

A plot of Q2 operating points, which result when using this technique, is shown in Figure 4–6. Note that the pass element is required to operate with a collector current of only I_{SC} during short circuit conditions, not the full output current, I_K. This results in a more efficient utilization of the SOA of Q2 allowing the use of a smaller transistor than if constant current limiting were used. Although foldback current limiting allows use of smaller pass element transistors for a given regulator output current than does constant current limiting, it does have a few disadvantages.

Referring to Equation (4.12), as the foldback ratio (I_K/I_{SC}) is increased, the required value of R_{SC} increases. This results in a greater input voltage at higher foldback ratios. In addition, it can be seen for Equation (4.12) that there exists an absolute limit to the foldback ratio equal to:

$$\left(\frac{I_K}{I_{SC(max)}}\right) = 1 + \frac{V_{out}}{V_{BEon(Q3)}} \text{ for } R_{SC} = \infty \tag{4.15}$$

For these reasons, foldback ratios greater than 2:1 or 3:1 are not usually practical for the lower output voltage regulators.

D. Paralleling Pass Element Transistors

Occasionally, it will not be possible to obtain a transistor with sufficient safe–operating–area. In these cases it is necessary to parallel two or more transistors. Even if a single transistor with sufficient capability is available, it is possible that paralleling two smaller transistors is more economical.

In order to insure that the collector currents of the paralleled transistors are approximately equal, the configuration of Figure 4–7 can be used. Emitter–ballasting resistors are used to force collector–current sharing between Q1 and Q2. The collector–current mismatch can be determined by considering the following, from Figure 4–7,

$$V_{BE1} + V_1 = V_{BE2} + V_2 \qquad (4.16)$$

$$\text{and, } \Delta V_{BE} = \Delta V \qquad (4.17)$$

where: $V_{BE} = V_{BE1} - V_{BE2}$ and, $\Delta V = V_2 - V_1$

Assuming $I_{E1} \simeq I_{C1}$ and $I_{E2} \simeq O_{C2}$, the collector–current mismatch is given by,

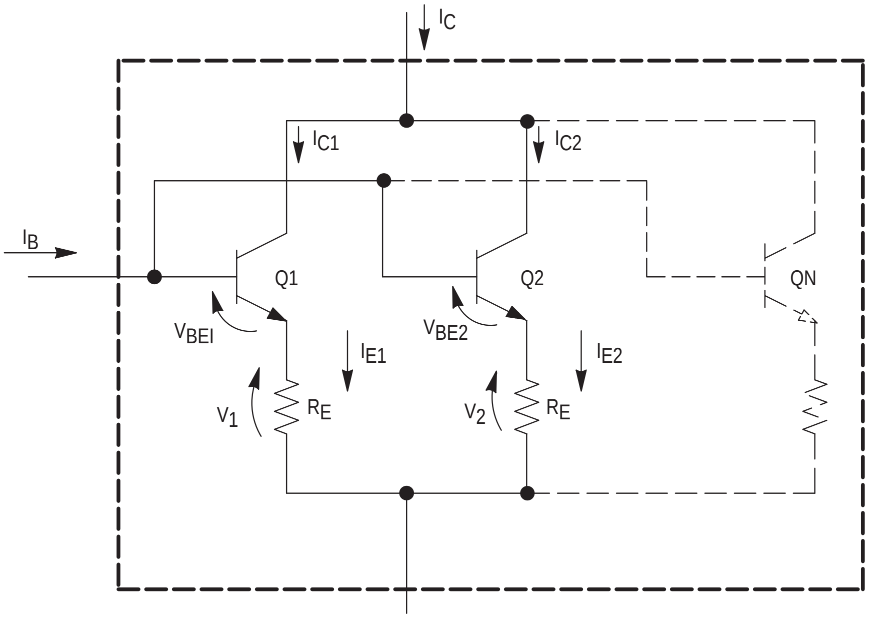
$$\frac{I_{C2} - I_{C1}}{I_{C2}} = \frac{\left(\frac{V_2}{R_E}\right) - \left(\frac{V_1}{R_E}\right)}{\left(\frac{V_2}{R_E}\right)} = \frac{V_2 - V_1}{V_2} = \frac{\Delta V}{V_2} = \frac{\Delta V_{BE}}{V_2} \qquad \begin{matrix}(4.18)\\(4.19)\end{matrix}$$

$$\text{and, percent collector–current mismatch} = \frac{\Delta V_{BE}}{V_2} \times 100\% \qquad (4.20)$$

From Equation (4.20), the collector–current mismatch is dependent on ΔV_{BE} and V_2. Since ΔV_{BE} is usually acceptable, V_2 should be 1.0 V to 0.5 V, respectively. R_E is therefore given by:

$$R_E = \frac{0.5\text{ V to }1.0\text{ V}}{I_{C1}} = \frac{0.5\text{ V to }1.0\text{ V}}{I_{C2}} = \frac{0.5\text{ V to }1.0\text{ V}}{I_C/2} \qquad (4.21)$$

Figure 4–7. Paralleling Pass Element Transistors



SECTION 5

LINEAR REGULATOR CONSTRUCTION AND LAYOUT

An important, and often neglected, aspect of the total regulator circuit design is the actual layout and component placement of the circuit. In order to obtain excellent transient response performance, high frequency transistors are used in modern integrated circuit voltage regulators. Proper attention to circuit layout is therefore necessary to prevent regulator instability or oscillations, or degraded performance.

In this section, guidelines will be given on proper regulator layout and placement of circuit components. In addition, topics such as remote voltage sensing, semiconductor mounting techniques, and thermal system evaluations will also be discussed.

1. General Layout and Component Placement Considerations

As mentioned previously, modern integrated circuit regulators are necessarily high bandwidth devices in order to obtain good transient response characteristics. To insure stable closed–loop operation, all these devices are frequency compensated, either internally or externally. This compensation can easily be upset by unwanted stray circuit capacitances and lead inductances, resulting in spurious oscillations. Therefore, it is important that the circuit lead lengths be short and the layout as tight as possible. Particular attention should be paid to locating the compensation and bypass capacitors as close to the IC as possible. Lead lengths associated with the external pass element(s), if used, should also be minimized.

Often overlooked is the stray inductance associated with the input leads to the regulator circuit. If the lead length from the input supply filter capacitor to the regulator input is more than a couple of inches, a 0.01 μF to 1.0 μF high frequency type capacitor (tantalum, ceramic, etc.) should be used to bypass the supply leads close to the regulator input pins.

2. Ground Loops and Remote Voltage Sensing

Ground Loops — Regulator performance can also suffer if ground loops in the circuit wiring are not avoided. The most common ground loop problem occurs when the return lead of the input supply filter capacitor is improperly located, as shown in Figure 5–1. If this return lead is physically connected between the load return and the regulator circuit ground point (“B”), a ripple voltage component (60 Hz or 120 Hz) can be induced on the load voltage (V_L). This is due to the high peaks of the filter capacitor ripple current (I_{ripple}) flowing through the lead resistance between the load and regulator. These peaks can be 5 to 15 times the value of load current. Since the regulator will only keep constant the voltage between its sense lead and ground point, points “A” and “B” in Figure 5–1, this additional ripple voltage (V_{lead}), will appear at the load.

This problem can be avoided by proper placement and connection of the filter capacitor return load as shown in Figure 5–2.

Remote Voltage Sensing — Closely related to the above ground loop problem is resistance in the current carrying leads to the load. This can cause poorer than expected load regulation in cases where the load currents are large or where the load is located some distance from the regulator. This is illustrated in Figure 5–3. As stated previously, the regulator circuit will keep the voltage present between its sense and ground pins constant. From Figure 5–3 we can see that any lead resistance between these points and the load will cause the load voltage (V_L) to vary with varying load current, I_L. This effectively lowers the load regulation of the circuit.

Figure 5–1. Filter Capacitor Ground Loop — WRONG!

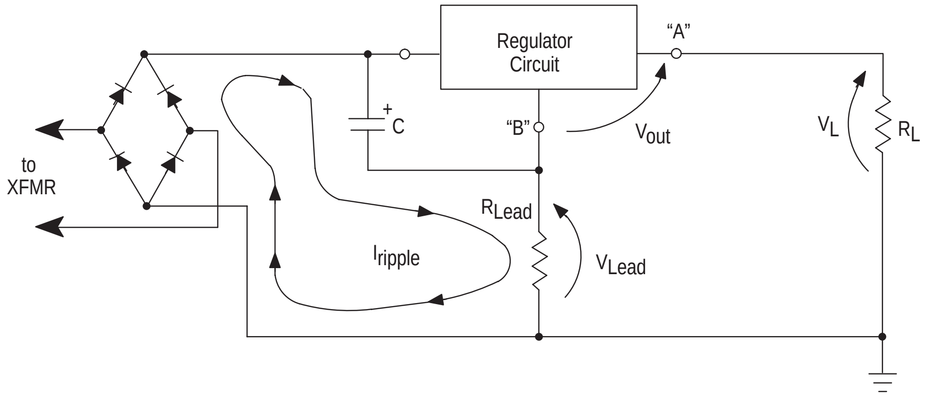
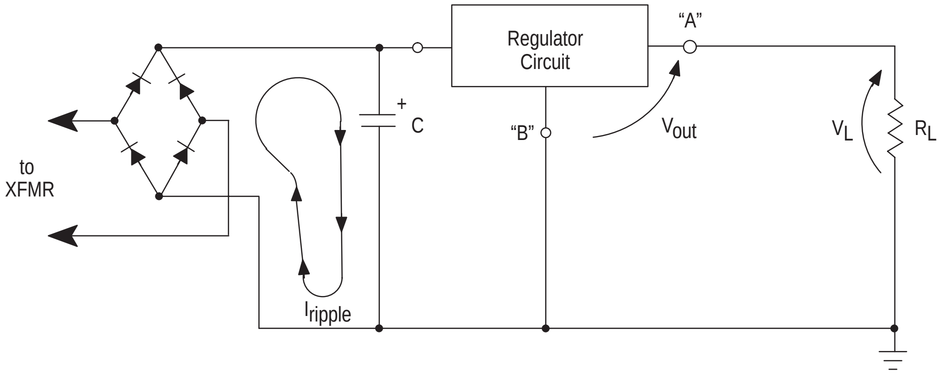


Figure 5–2. Filter Capacitor Ground Loop — RIGHT!



This problem can be avoided by the use of remote Sense leads, as shown in Figure 5–4. The voltage drops in the high current carrying leads now have no effect on the load voltage (V_L). However, since the Sense and Ground leads are usually rather long, care must be exercised that their associated lead inductance is minimized, or loop instability may result. The Ground and Sense leads should be formed into a twisted pair lead to minimize their lead inductance and noise pickup.

Figure 5–3. Effects of Resistance In Output Leads

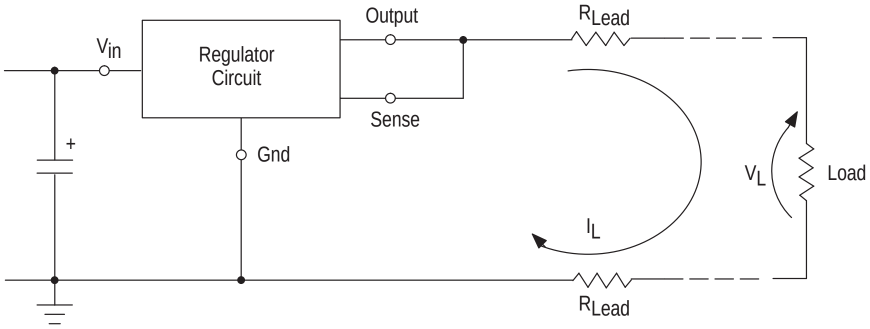
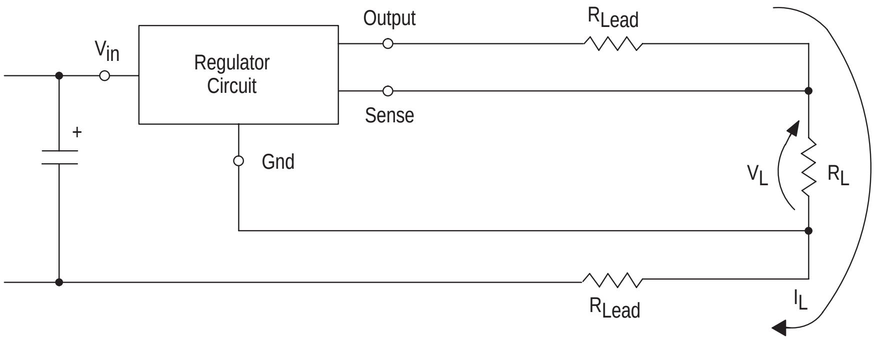


Figure 5–4. Remote Voltage Sensing



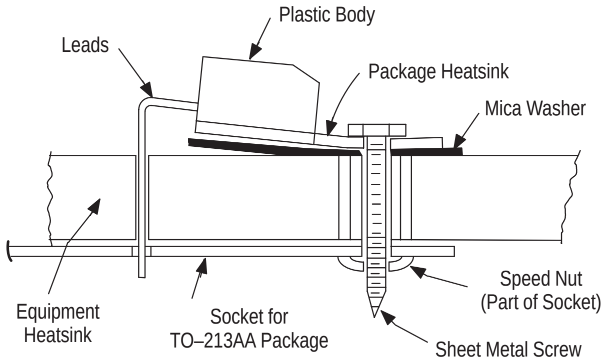
3. Mounting Considerations for Power Semiconductors

Current and power ratings of semiconductors are inseparably linked to their thermal environment. Except for lead–mounted parts used at low currents, a heat exchanger is required to prevent the junction temperature from exceeding its rated limit, thereby running the risk of a high failure rate. Furthermore, the semiconductor industry's field history indicated that the failure rate of most silicon semiconductors decreases approximately by one–half for a decrease in junction temperature from 160° to 135°C.(1) Guidelines for designers of military power supplies impose a 110°C limit upon junction temperature.(2) Proper mounting minimizes the temperature gradient between the semiconductor case and the heat exchanger.

Most early life field failures of power semiconductors can be traced to faulty mounting procedures. With metal packaged devices, faulty mounting generally causes unnecessarily high junction temperature, resulting in reduced component lifetime, although mechanical damage has occurred on occasion from improperly mounting to a warped surface. With the widespread use of various plastic packaged semiconductors, the prospect of mechanical damage is very significant. Mechanical damage can impair the case moisture resistance or crack the semiconductor die.

Figure 5–5 shows an example of doing nearly everything wrong. A tab mount TO–220 package is shown being used as a replacement for a TO–213AA (TO–66) part which was socket mounted. To use the socket, the leads are bent — an operation which, if not properly done, can crack the package, break the internal bonding wires, or crack the die. The package is fastened with a sheet metal screw through a 1/4″ hole containing a fiber–insulating sleeve. The force used to tighten the screw tends to pull the package into the hole, possibly causing enough distortion to crack the die. In addition the contact area is small because of the area consumed by the large hole and the bowing of the package, the result is a much higher junction temperature than expected. If a rough heatsink surface and/or burrs around the hole were displayed in the illustration, most but not all poor mounting practices would be covered.

Figure 5–5. Extreme Case of Improperly Mounting a Semiconductor (Distortion Exaggerated)



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(1) MIL–HANDBOOK — 2178, SECTION 2.2.

(2) *Navy Power Supply Reliability — Design and Manufacturing Guidelines* NAVMAT P4855–1,
Dec. 1982 NAVPUBFORCEN,
5801 Tabor Ave., Philadelphia, PA 19120.

Cho–Therm is a registered trademark of Chromerics, Inc.
Grafoil is a registered trademark of Union Carbide
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Rubber–Duc is a trademark of AAVID Engineering
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In many situations the case of the semiconductor must be electrically isolated from its mounting surface. The isolation material is, to some extent, a thermal isolator as well, which raises junction operating temperatures. In addition, the possibility of arc–over problems is introduced if high voltages are present. Various regulating agencies also impose creepage distance specifications which further complicates design. Electrical isolation thus places additional demands upon the mounting procedure.

Proper mounting procedures usually necessitate orderly attention to the following:

1. Preparing the mounting surface
2. Applying a thermal grease (if required)
3. Installing the insulator (if electrical isolation is desired)
4. Fastening the assembly
5. Connecting the terminals to the circuit

In this note, mounting procedures are discussed in general terms for several generic classes of packages. As newer packages are developed, it is probable that they will fit into the generic classes discussed in this note. Unique requirements are given on data sheets pertaining to the particular package. The following classes are defined:

Flange Mount	Tab Mount
Plastic Body Mount	Surface Mount

Appendix A contains a brief review of thermal resistance concepts.

Appendix B discusses measurement difficulties with interface thermal resistance tests.

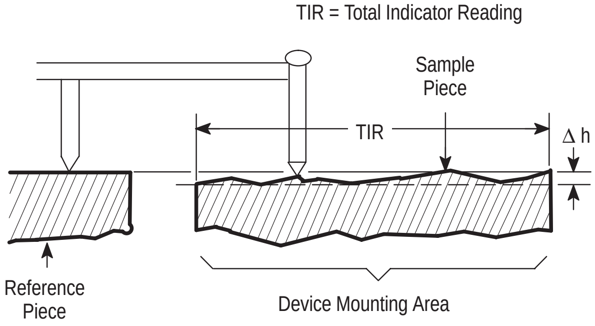
Mounting Surface Preparation

In general, the heatsink mounting surface should have a flatness and finish comparable to that of the semiconductor package. In lower power applications, the heatsink surface is satisfactory if it appears flat against a straight edge and is free from deep scratches. In high power applications, a more detailed examination of the surface is required. Mounting holes and surface treatment must also be considered.

Surface Flatness

Surface flatness is determined by comparing the variance in height (Δh) of the test specimen to that of a reference standard as indicated in Figure 5–6. Flatness is normally specified as a fraction of the Total Indicator Reading (TIR). The mounting surface flatness (i.e, Δh/TIR) if less than 4 mils per inch, normal for extruded aluminum, is satisfactory in most cases.

Figure 5–6. Surface Flatness Measurement



Surface Finish

Surface finish is the average of the deviations both above and below the mean value of surface height. For minimum interface resistance, a finish in the range of 50 µin. to 60 µin. is satisfactory. A finer finish is costly to achieve and does not significantly lower contact resistance. Tests conducted by Thermalloy using a copper TO–204 (TO–3) package with a typical 32 µin. finish, showed that heatsink finishes between 16 µin. and 64 µin. caused less than ±2.5% difference in interface thermal resistance when the voids and scratches were filled with a thermal joint compound.(3) Most commercially available cast or extruded heatsinks will require spotfacing when used in high power applications. In general, milled or machined surfaces are satisfactory if prepared with tools in good working condition.

Mounting Holes

Mounting holes generally should only be large enough to allow clearance of the fastener. The larger thick flange type packages having mounting holes removed from the semiconductor die location, such as the TO–204AA, may successfully be used with larger holes to accommodate an insulating bushing, but many plastic encapsulated packages are intolerant of this condition. For these packages, a smaller screw size must be used such that the hole for the bushing does not exceed the hole in the package.

Punched mounting holes have been a source of trouble because if not properly done, the area around a punched hole is depressed in the process. This "crater" in the heatsink around the mounting hole can cause two problems. The device can be damaged by distortion of the package as the mounting pressure attempts to conform it to the shape of the heatsink indentation, or the device may only bridge the crater and leave a significant percentage of its heat–dissipating surface out of contact with the heatsink. The first effect may often be detected immediately by visual cracks in the package (if plastic), but usually an unnatural stress is imposed, which results in an early–life failure. The second effect results in hotter operation and is not manifested until much later.

Although punched holes are seldom acceptable in the relatively thick material used for extruded aluminum heatsinks, several manufacturers are capable of properly utilizing the capabilities inherent in both fine–edge blanking or sheared–through holes when applied to sheet metal as commonly used for stamped heatsinks. The holes are pierced using Class A progressive dies mounted on four–post die sets equipped with proper pressure pads and holding fixtures.

When mounting holes are drilled, a general practice with extruded aluminum, surface cleanup is important. Chamfers must be avoided because they reduce heat transfer surface and increase mounting stress. However, the edges must be broken to remove burrs which cause poor contact between device and heatsink and may puncture isolation material.

Surface Treatment

Many aluminum heatsinks are black–anodized to improve radiation ability and prevent corrosion. Anodizing results in significant electrical but negligible thermal insulation. It need only be removed from the mounting area when electrical contact is required. Heatsinks are also available which have a nickel plated copper insert under the semiconductor mounting area. No treatment of this surface is necessary.

Another treated aluminum finish is iridite, or chromate–acid dip, which offers low resistance because of its thin surface, yet has good electrical properties because it resists oxidation. It need only be cleaned of the oils and films that collect in the manufacture and storage of the sinks, a practice which should be applied to all heatsinks.

For economy, paint is sometimes used for sinks; removal of the paint where the semiconductor is attached is usually required because of the paint's high thermal resistance. However, when it is necessary to insulate the semiconductor package from the heatsink, hard anodized or painted surfaces allow an easy installation for low voltage applications. Some manufacturers will provide anodized or painted surfaces meeting specific insulation voltage requirements, usually up to 400 V.

It is also necessary that the surface be free from all foreign material, film, and oxide (freshly bared aluminum forms an oxide layer in a few seconds). Immediately prior to assembly, it is a good practice to polish the mounting area with No. 000 steel wool, followed by an acetone or alcohol rinse.

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(3) Catalog #87–HS–9 (1987), page 8, Thermalloy, Inc., P.O. Box 810839, Dallas, Texas 75381–0839.

Interface Decisions

When any significant amount of power is being dissipated, something must be done to fill the air voids between mating surfaces in the thermal path. Otherwise, the interface thermal resistance will be unnecessarily high and quite dependent upon the surface finishes.

For several years, thermal joint compounds, often called grease, have been used in the interface. They have a resistivity of approximately 60°C/W/in whereas air has 1200°C/W/in. Since surfaces are highly pockmarked with minute voids, use of a compound makes a significant reduction in the interface thermal resistance of the joint. However, the grease causes a number of problems, as discussed in the following section. To avoid using grease, manufacturers have developed dry conductive and insulating pads to replace the more traditional materials. These pads are conformal and therefore partially fill voids when under pressure.

Thermal Compounds (Grease)

Joint compounds are a formulation of fine zinc or other conductive particles in a silicone oil or other synthetic base fluid which maintains a grease–like consistency with time and temperature. Since some of these compounds do not spread well, they should be evenly applied in a very thin layer using a spatula or lintless brush, and wiped lightly to remove excess material. Some cyclic rotation of the package will help the compound spread evenly over the entire contact area. Some experimentation is necessary to determine the correct quantity; too little will not fill all the voids, while too much may permit some compound to remain between well mated metal surfaces where it will substantially increase the thermal resistance of the joint.

To determine the correct amount, several semiconductor samples and heatsinks should be assembled with different amounts of grease applied evenly to one side of each mating surface. When the amount is correct, a very small amount of grease should appear around the perimeter of each mating surface as the assembly is slowly torqued to the recommended value. Examination of a dismantled assembly should reveal even wetting across each mating surface. In production, assemblers should be trained to slowly apply the specified torque even though an excessive amount of grease appears at the edges of mating surfaces. Insufficient torque causes a significant increase in the thermal resistance of the interface.

To prevent accumulation of airborne particulate matter, excess compound should be wiped away using a cloth moistened with acetone or alcohol. These solvents should not contact plastic–encapsulated devices, as they may enter the package and cause a leakage path or carry in substances which might attack the semiconductor chip.

Data showing the effect of compounds on several package types under different mounting conditions is shown in Table 5–1. The rougher the surface, the more valuable the grease becomes in lowering contact resistance; therefore, when mica insulating washers are used, use of grease is generally mandatory. The joint compound also improves the breakdown rating of the insulator.

Table 5–1. Approximate Values for Interface Thermal Resistance Data from Measurements Performed In Motorola Applications Engineering Laboratory

Dry interface values are subject to wide variation because of extreme dependence upon surface conditions. Unless otherwise noted the case temperature is monitored by a thermocouple located directly under the die reached through a hole in the heatsink. (See Appendix B for a discussion of Interface Thermal Resistance Measurements.)

Package Type and Data		Interface Thermal Resistance (°C/W)						
			Metal–to–Metal		With Insulator			
JEDEC Outlines	Description	Test Torque In–Lb	Dry	Lubed	Dry	Lubed	Type	See Note
TO–204AA (TO–3)	Diamond Flange	6	0.5	0.1	1.3	0.36	3 mil Mica	1
TO–220AB	Thermowatt	8	1.2	1.0	3.4	1.6	2 mil Mica	1, 2

NOTES: 1. See Figures 5–7 and 5–8 for additional data on TO–204AA and TO–220 packages.
2. Screw not insulated (see Figure 5–12).

Conductive Pads

Because of the difficulty of assembly using grease and the evaporation problem, some equipment manufacturers will not, or cannot, use grease. To minimize the need for grease, several vendors offer dry conductive pads which approximate performance obtained with grease. Data for a greased bare joint and a joint using Grafoil, a dry graphite compound, is shown in the data of Figure 5–7. Grafoil is claimed to be a replacement for grease when no electrical isolation is required; the data indicates it does indeed perform as well as grease. Another conductive pad available from AAVID is called KON–DUX. It is made with a unique, grain oriented, flake–like structure (patent pending). Highly compressible, it becomes formed to the surface roughness of both the heatsink and semiconductor. Manufacturer's data shows it to provide an interface thermal resistance better than a metal interface with filled silicone grease. Similar dry conductive pads are available from other manufacturers. They are a fairly recent development; long term problems, if they exist, have not yet become evident.

Insulation Considerations

Since most power semiconductors use are vertical device construction it is common to manufacture power semiconductors with the output electrode (anode, collector or drain) electrically common to the case; the problem of isolating this terminal from ground is a common one. For lowest overall thermal resistance, which is quite important when high power must be dissipated, it is best to isolate the entire heatsink/semiconductor structure from ground, rather than to use an insulator between the semiconductor and the heatsink. Heatsink isolation is not always possible, however, because of EMI requirements, safety reasons, instances where a chassis serves as a heatsink or where a heatsink is common to several non–isolated packages. In these situations insulators are used to isolate the individual components from the heatsink. Newer packages, such as the Motorola Full Pak and EMS modules, contain the electrical isolation material within, thereby saving the equipment manufacturer the burden of addressing the isolation problem.

Insulator Thermal Resistance

When an insulator is used, thermal grease is of greater importance than with a metal–to–metal contact, because two interfaces exist instead of one and some materials, such as mica, have a hard, markedly uneven surface. With many isolation materials reduction of interface thermal resistance of between 2 to 1 and 3 to 1 are typical when grease is used.

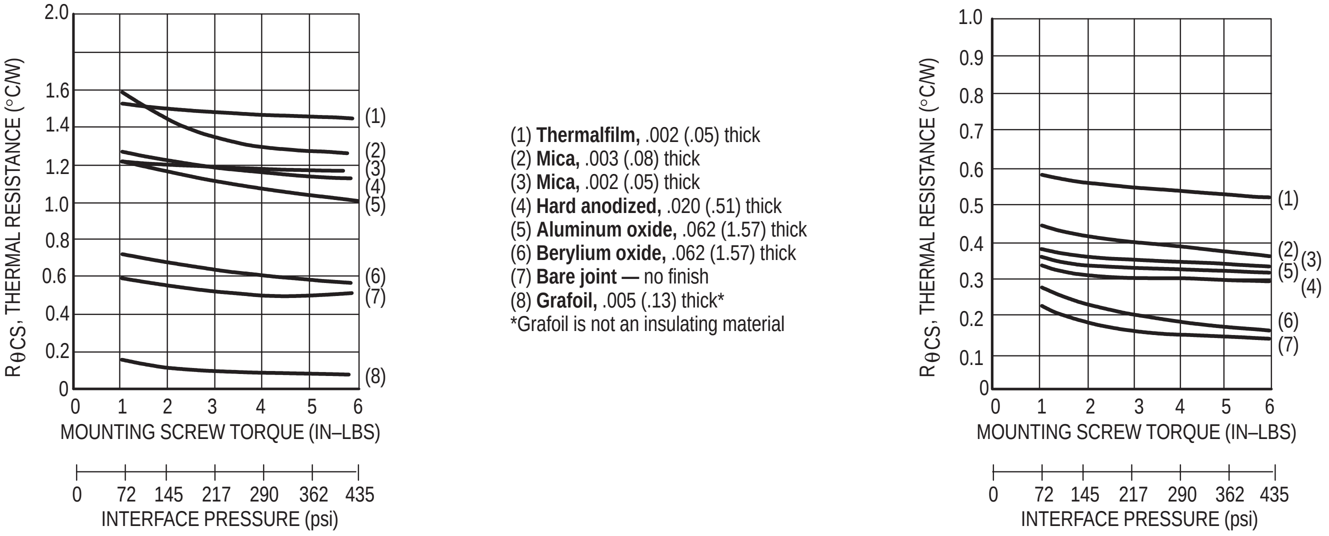
Data obtained by Thermalloy, showing interface resistance for different insulators and torques applied to TO–204 (TO–3) and TO–220 packages, is shown in Figure 5–7, for bare and greased surfaces. Similar materials to those shown are available from several manufacturers. It is obvious that with some arrangements, the interface thermal resistance exceeds that of the semiconductor (junction–to–case).

Referring to Figure 5–7, one may conclude that when high power is handled, beryllium oxide is unquestionably the best. However, it is an expensive choice. (It should not be cut or abraided, as the dust is highly toxic.) Thermafilm is a filled polyimide material which is used for isolation (variation of Kapton). It is a popular material for low power applications because of its low cost ability to withstand high temperatures, and ease of handling in contrast to mica which chips and flakes easily.

A number of other insulating materials are also shown. They cover a wide range of insulation resistance, thermal resistance and ease of handling. Mica has been widely used in the past because it offers high break down voltage and fairly low thermal resistance at a low cost but it certainly should be used with grease.

Silicone rubber insulators have gained favor because they are somewhat conformal under pressure. Their ability to fill in most of the metal voids at the interface reduces the need for thermal grease. When first introduced, they suffered from cut–through after a few years in service. The ones presently available have solved this problem by having imbedded pads of Kapton or fiberglass. By comparing Figures 5–7(c) and 5–7(d), it can be noted that Thermasil, a filled silicone rubber without grease, has about the same interface thermal resistance as greased mica for the TO–220 package.

Figure 5–7. Interface Thermal Resistance Using Different Insulating Materials as a Function of Mounting Screw Torque



(a) TO–204AA (TO–3) Without Thermal Grease

(b) TO–204AA (TO–3) With Thermal Grease

(c) TO–220 Without Thermal Grease

(d) TO–220 With Thermal Grease

Data Courtesy of Thermalloy

A number of manufacturers offer silicone rubber insulators. Table 5–2 shows measured performance of a number of these insulators under carefully controlled, nearly identical conditions. The interface thermal resistance extremes are over 2:1 for the various materials. It is also clear that some of the insulators are much more tolerant than others of out–of–flat surfaces. Since the tests were performed, newer products have been introduced. The Bergquist K–10 pad, for example, is described as having about 2/3 the interface resistance of the Sil Pad 1000 which would place its performance close to the Chomerics 1671 pad. AAVID also offers an isolated pad called Rubber–Duc, however it is only available vulcanized to a heatsink and therefore was not included in the comparison. Published data from AAVID shows $R\theta_{CS}$ below 0.3°C/W for pressures above 500 psi. However, surface flatness and other details are not specified so a comparison cannot be made with other data in this note.

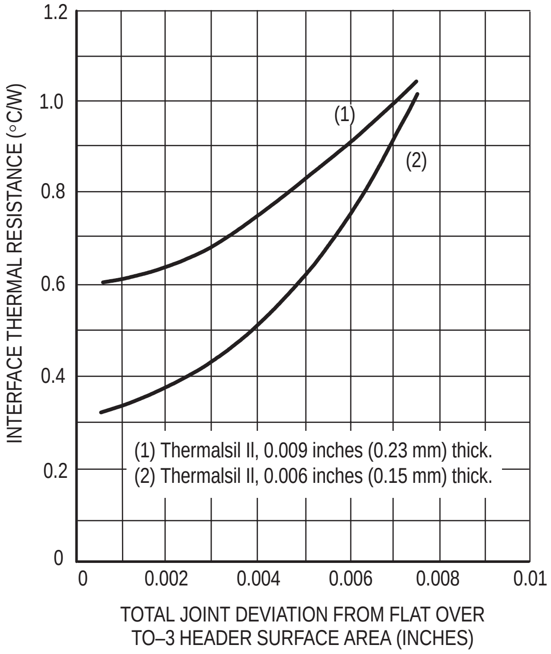
Table 5–2. Thermal Resistance of Silicone Rubber Pads

Manufacturer	Product	$R_{\theta CS}$ @ 3 Mils*	$R_{\theta CS}$ @ 7.5 Mils*
Wakefield	Delta Pad 173–7	0.790	1.175
Bergquist	Sil Pad K–4	0.752	1.470
Stockwell Rubber	1867	0.742	1.015
Bergquist	Sil Pad 400–9	0.735	1.205
Thermalloy	Thermalsil II	0.680	1.045
Shin–Etsu	TC–30AG	0.664	1.260
Bergquist	Sil Pad 400–7	0.633	1.060
Chomerics	1674	0.592	1.190
Wakefield	Delta Pad 174–9	0.574	0.755
Bergquist	Sil Pad 1000	0.529	0.935
Ablestik	Thermal Wafers	0.500	0.990
Thermalloy	Thermalsil III	0.440	1.035
Chomerics	1671	0.367	0.655

*Test Fixture Deviation from flat Thermalloy EIR86–1010.

The thermal resistance of some silicone rubber insulators is sensitive to surface flatness when used under a fairly rigid base package. Data for a TO–204AA (TO–3) package insulated with Thermasil is shown on Figure 5–8. Observe that the "worst case" encountered (7.5 mils) yields results having about twice the thermal resistance of the "typical case" (3 mils), for the more conductive insulator. In order for Thermasil III to exceed the performance of greased mica, total surface flatness must be under 2 mils, a situation that requires spot finishing.

Figure 5–8. Effect of Total Surface Flatness on Interface Resistance Using Silicon Rubber Insulators



Data Courtesy of Thermalloy

Silicon rubber insulators have a number of unusual characteristics. Besides being affected by surface flatness and initial contact pressure, time is a factor. For example, in a study of the Cho–Therm 1688 pad thermal interface impedance dropped from 0.90°C/W to 0.70°C/W at the end of 1000 hours. Most of the change occurred during the first 200 hours where $R\theta_{CS}$ measured 0.74°C/W. The torque on the conventional mounting hardware had decreased to 3 in–lb from an initial 6 in–lb. With non–conformal materials, a reduction in torque would have increased the interface thermal resistance.

Because of the difficulties in controlling all variables affecting tests of interface thermal resistance, data from different manufacturers is not in good agreement. Table 5–3 shows data obtained from two sources. The relative performance is the same, except for mica which varies widely in thickness. Appendix B discusses the variables which need to be controlled. At the time of this writing ASTM Committee D9 is developing a standard for interface measurements.

The conclusions to be drawn from all this data is that some types of silicon rubber pads, mounted dry, will out perform the commonly used mica with grease. Cost may be a determining factor in making a selection.

Table 5–3. Performance of Silicon Rubber Insulators Tested per MIL–I–49456

	Measured Thermal Resistance (°C/W)	
Material	**Thermalloy Data**(1)	**Bergquist Data**(2)
Bare Joint, greased	0.033	0.008
BeO, greased	0.082	—
Cho–Therm, 1617	0.233	—
Q Pad (non–insulated)	—	0.009
Sil–Pad, K–10	0.263	0.200
Thermasil III	0.267	—
Mica, greased	0.329	0.400
Sil–Pad 1000	0.400	0.300
Cho–therm 1674	0.433	—
Thermasil II	0.500	—
Sil–Pad 400	0.533	0.440
Sil–Pad K–4	0.583	0.440

(1) From Thermalloy EIR 87–1030
(2) From Bergquist Data Sheet

Insulation Resistance

When using insulators, care must be taken to keep the mating surfaces clean. Small particles of foreign matter can puncture the insulation, rendering it useless or seriously lowering its dielectric strength. In addition, particularly when voltages higher than 300 V are encountered, problems with creepage may occur. Dust and other foreign material can shorten creepage distances significantly, so having a clean assembly area is important. Surface roughness and humidity also lower insulation resistance. Use of thermal grease usually raises the withstand voltage of the insulation system but excess must be removed to avoid collecting dust. Because of these factors, which are not amenable to analysis, hi–pot testing should be done on prototypes and a large margin of safety employed.

Insulated Electrode Packages

Because of the nuisance of handling and installing the accessories needed for an insulated semiconductor mounting, equipment manufacturers have longed for cost–effective insulated packages since the 1950s. The first to appear were stud mount types which usually have a layer of beryllium oxide between the stud hex and the can. Although effective, the assembly is costly and requires manual mounting and lead wire soldering to terminals on top of the case. In the late eighties, a number of electrically isolated parts became available from various semiconductor manufacturers. These offerings presently consist of multiple chips and integrated circuits as well as the more conventional single chip devices.

The newer insulated packages can be grouped into two categories. The first has insulation between the semiconductor chips and the mounting base; an exposed area of the mounting base is used to secure the part. The second category contains parts which have a plastic overmold covering the metal mounting base. The Full Pak (Case 221C) illustrated in Figure 5–13, is an example of parts in the second category.

Parts in the first category — those with an exposed metal flange or tab — are mounted the same as their non–insulated counterparts. However, as with any mounting system where pressure is bearing on plastic, the overmolded type should be used with a conical compression washer, described later in this note.

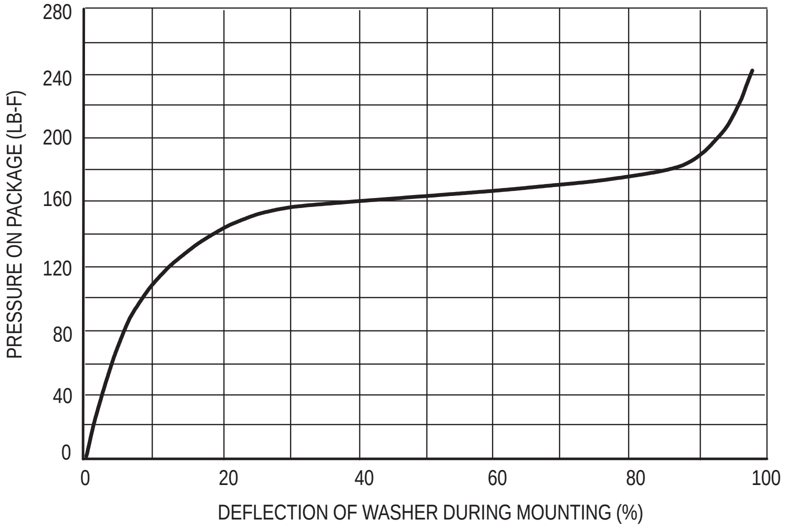
Fastener and Hardware Characteristics

Characteristics of fasteners, associated hardware, and the tools to secure them determine their suitability for use in mounting the various packages. Since many problems have arisen because of improper choices, the basic characteristics of several types of hardware are discussed next.

Compression Hardware

Normal split ring lock washers are not the best choice for mounting power semiconductors. A typical #6 washer flattens at about 50 pounds, whereas 150 to 300 pounds is needed for good heat transfer at the interface. A very useful piece of hardware is the conical, sometimes called a Belleville washer, compression washer. As shown in Figure 5–9, it has the ability to maintain a fairly constant pressure over a wide range of its physical deflection — generally 20% to 80%. When installing, the assembler applies torque until the washer depresses to half its original height. (Tests should be run prior to setting up the assembly line to determine the proper torque for the fastener used to achieve 50% deflection.) The washer will absorb any cyclic expansion of the package, insulating washer or other materials caused by temperature changes. Conical washers are the key to successful mounting of devices requiring strict control of the mounting force or when plastic hardware is used in the mounting scheme. They are used with the large face contacting the packages. A new variation of the conical washer includes it as part of a nut assembly. Called a Sync Nut, the patented device can be soldered to a PC board and the semiconductor mounted with a 6–32 machine screw.(4)

Figure 5–9. Characteristics of the Conical Compression Washers Designed for Use with Plastic Body Mounted Semiconductors



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(4) ITW Shakeproof, St. Charles Road, Elgin, IL 60120.

Clips

Fast assembly is accomplished with clips. When only a few watts are being dissipated, the small board–mounted or free–standing heat dissipators with an integral clip, offered by several manufacturers, result in a low cost assembly. When higher power is being handled, a separate clip may be used with larger heatsinks. In order to provide proper pressure, the clip must be specially designed for a particular heatsink thickness and semiconductor package.

Clips are especially popular with plastic packages such as the TO–220 and TO–126. In addition to fast assembly, the clip provides lower interface thermal resistance than other assembly methods when it is designed for proper pressure to bear on the top of the plastic over the die. The TO–220 package usually is lifted up under the die location when mounted with a single fastener through the hole in the tab because of the high pressure at one end.

Machine Screws

Machine screws, conical washers, and nuts (or Sync Nut) can form a trouble–free fastener system for all types of packages which have mounting holes. However, proper torque is necessary. Torque ratings apply when dry; therefore, care must be exercised when using thermal grease to prevent it from getting on the threads as inconsistent torque readings result. Machine screw heads should not directly contact the surface of plastic packages types as the screw heads are not sufficiently flat to provide properly distributed force. Without a washer, cracking of the plastic case may occur.

Self–Tapping Screws

Under carefully controlled conditions, sheet metal screws are acceptable. However, during the tapping process with a standard screw, a volcano–like protrusion will develop in the metal being threaded; an unacceptable surface that could increase the thermal resistance may result. When standard sheet metal screws are used, they must be used in a clearance hole to engage a speed nut. If a self–tapping process is desired, the screw type must be used which roll–forms machine screw threads.

Rivets

Rivets are not recommended fasteners for any of the plastic packages. When a rugged metal flange–mount package is being mounted directly to a heatsink, rivets can be used provided press–riveting is used. Crimping force must be applied slowly and evenly. Pop–riveting should never be used because the high crimping force could cause deformation of most semiconductor packages. Aluminum rivets are much preferred over steel because less pressure is required to set the rivet and thermal conductivity is improved.

The hollow rivet, or eyelet, is preferred over solid rivets. An adjustable, regulated pressure press is used such that a gradually increasing pressure is used to pan the eyelet. Use of sharp blows could damage the semiconductor die.

Solder

Until the advent of the surface mount assembly technique, solder was not considered a suitable fastener for power semiconductors. However, user demand has led to the development of new packages for this application. Acceptable soldering methods include conventional belt–furnace, irons, vapor–phase reflow, and infrared reflow. It is important that the semiconductor temperature not exceed the specified maximum (usually 260°C) or the die bond to the case could be damaged. A degraded die bond has excessive thermal resistance which often leads to a failure under power cycling.

Adhesives

Adhesives are available which have coefficients of expansion compatible with copper and aluminum.(5) Highly conductive types are available; a 10 mil layer has approximately 0.3°C/W interface thermal resistance. Different types are offered: high strength types for non–field–serviceable systems or low strength types for field–serviceable systems. Adhesive bonding is attractive when case mounted parts are used in wave soldering assembly because thermal greases are not compatible with the conformal coatings used and the greases foul the solder process.

Plastic Hardware

Most plastic materials will flow, but differ widely in this characteristic. When plastic materials form parts of the fastening system, compression washers are highly valuable to assure that the assembly will not loosen with time and temperature cycling. As previously discussed, loss of contact pressure will increase interface thermal resistance.

Fastening Techniques

Each of the various classes of packages in use requires different fastening techniques. Details pertaining to each type are discussed in following sections. Some general considerations follow.

To prevent galvanic action from occurring when devices are used on aluminum heatsinks in a corrosive atmosphere, many devices are nickel or gold–plated. Consequently, precautions must be taken not to mar the finish.

Another factor to be considered is that when a copper based part is rigidly mounted to an aluminum heatsink, a bimetallic system results which will bend with temperature changes. Not only is the thermal coefficient of expansion different for copper and aluminum, but the temperature gradient through each metal also causes each component to bend. If bending is excessive and the package is mounted by two or more screws the semiconductor chip could be damaged. Bending can be minimized by:

1. Mounting the component parallel to the heatsink fins to provide increased stiffness.
2. Allowing the heatsink holes to be a bit oversized so that some slip between surfaces can occur as temperature changes.
3. Using a highly conductive thermal grease or mounting pad between the heatsink and semiconductor to minimize the temperature gradient and allow for movement.

Flange Mount

Few known mounting difficulties exist with the smaller flange mount packages, such as the TO–204 (TO–3). The rugged base and distance between die and mounting hose combine to make it extremely difficult to cause any warpage unless mounted on a surface which is badly bowed or unless one side is tightened excessively before the other screw is started. It is therefore good practice to alternate tightening of the screws so that pressure is evenly applied. After the screws are finger–tight the hardware should be torqued to its final specification in at least two sequential steps. A typical mounting installation for a popular flange type part is shown in Figure 5–10. Machine screws (preferred), self–tapping screws, islets or rivets may be used to secure the package using guidelines in the previous section, **Fastener and Hardware Characteristics**.

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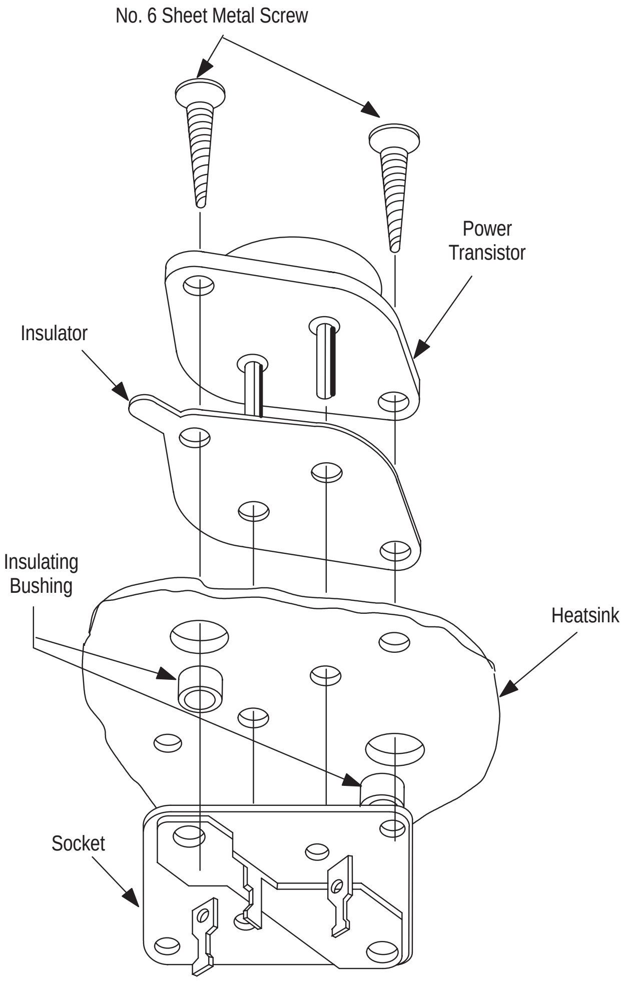
(5) Robert Batson, Elliot Fraunglass and James P. Moran, *Heat Dissipation Through Thermalloy Conductive Adhesives*, EMTAS ’83 Conference, February 1–3, Phoenix, AZ; Society of Manufacturing Engineers, One SME Drive, P.O. Box 930, Dearborn, MI 48128.

Figure 5–10. Hardware Used for a TO–204AA (TO–3) Flange Mount Part



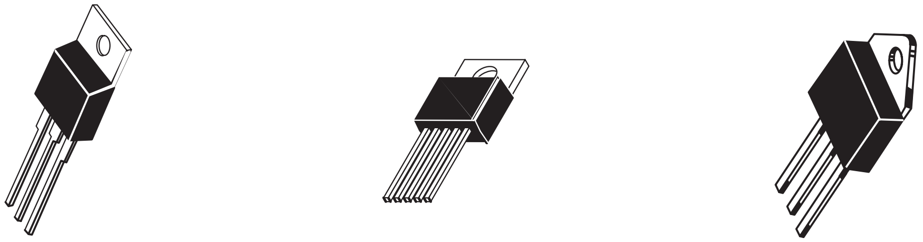
Tab Mount

The tab mount class is composed of a wide array of packages as illustrated in Figure 5–11. Mounting considerations for all varieties are similar to that for the popular TO–220 package, whose suggested mounting arrangements and hardware are shown in Figure 5–12. The rectangular washer shown in Figure 5–12a is used to minimize distortion of the mounting flange; excessive distortion could cause damage to the semiconductor chip. Use of the washer is only important when the size of the mounting hole exceeds 0.140 inch (6–32 clearance). Larger holes are needed to accommodate the lower insulating bushing when the screw is electrically connected to the case; however, the holes should not be larger than necessary to provide hardware clearance and should never exceed a diameter of 0.250 inch. Flange distortion is also possible if excessive torque is used during mounting. A maximum torque of 8 inch–pounds is suggested when using a 6–32 screw.

Care should be exercised to assure that the tool used to drive the mounting screw never comes in contact with the plastic body during the driving operation. Such contact can result in damage to the plastic body and internal device connections. To minimize this problem, Motorola TO–220 packages have a chamfer on one end. TO–220 packages of other manufacturers may need a spacer or combination spacer and isolation bushing to raise the screw head above the top surface of the plastic.

The popular TO–220 package and others of similar construction lift off the mounting surface as pressure is applied to one end. (See Appendix B, Figure B1.) To counter this tendency, at least one hardware manufacturer offers a hard plastic cantilever beam which applies more even pressure on the tab.(6) In addition, it separates the mounting screw from the metal tab. Tab mount parts may also be effectively mounted with clips as shown in Figure 5–14(c). To obtain high pressure without cracking the case, a pressure spreader bar should be used under the clip. Interface thermal resistance with the cantilever beam or clips can be lower than with screw mounting.

Figure 5–11. Several Types of Tab Mounted Parts



CASE 221A (TO–220AB)

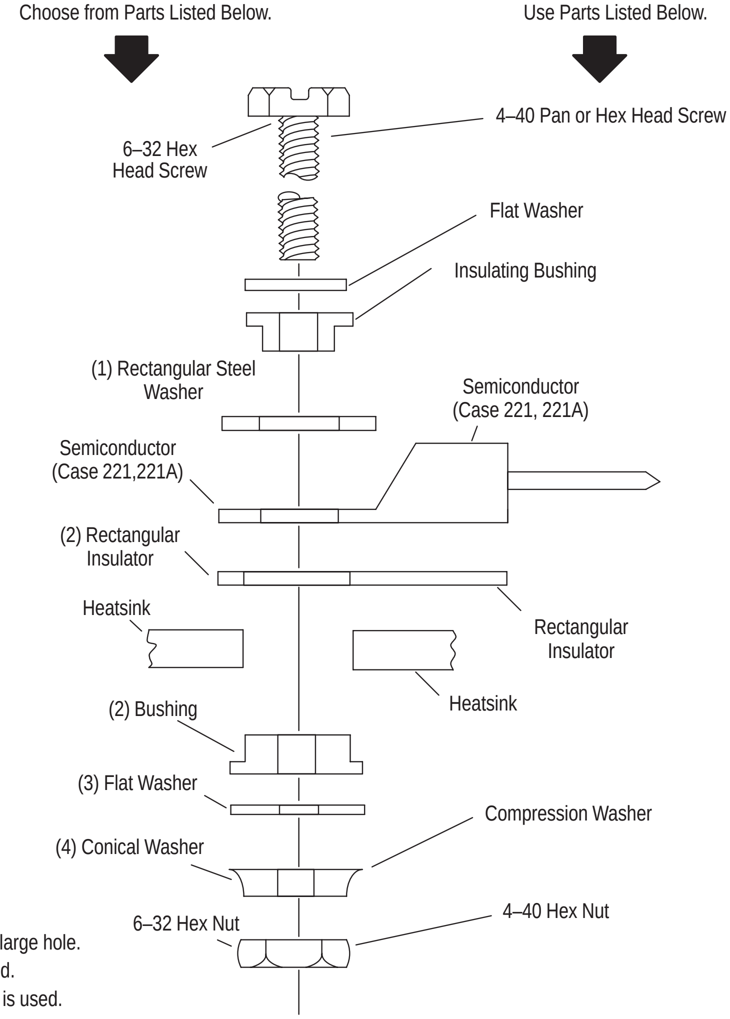
CASE 314D

CASE 340 (TO–218)

Figure 5–12. Mounting Arrangements for Tab Mount TO–220

a) Preferred Arrangement for Isolated or Non–isolated Mounting. Screw is at Semiconductor Case Potential. 6–32 Hardware is Used.

b) Alternate Arrangement for Isolated Mounting when Screw must be at Heatsink Potential. 4–40 Hardware is Used.



(1) Used with thin chassis and/or large hole.
(2) Used when isolation is required.
(3) Required when nylon bushing is used.

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(6) Catalog, Edition 18, Richco Plastic Company, 5825 N. Tripp Ave., Chicago, IL 60546.

Plastic Body Mount

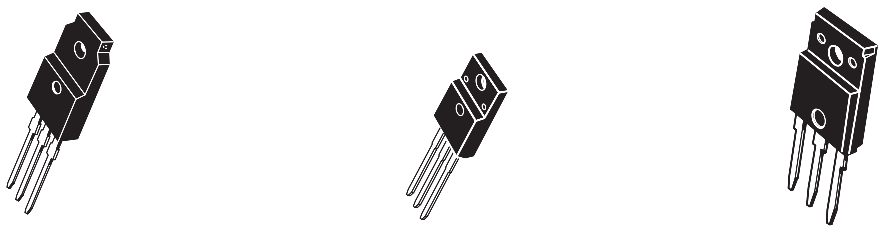
The Full Pak plastic power packages shown in Figure 5–13 are typical of packages in this group. They have been designed to feature minimum size with no compromise in thermal resistance.

The Full Pak (Case 221C) is similar to a TO–220 except that the tab is encased in plastic. Because the mounting force is applied to plastic, the mounting procedure differs from a standard TO–220 and is similar to that of the Thermopad.

Several types of fasteners may be used to secure these packages; machine screws, eyelets, or clips are preferred. With screws or eyelets, a conical washer should be used which applies the proper force to the package over a fairly wide range of deflection and distributes the force over a fairly large surface area. Screws should not be tightened with any type of air–driven torque gun or equipment which may cause high impact. Characteristics of a suitable conical washer is shown in Figure 5–9.

The Full Pak (Case 221C, 221D and 340B) permits the mounting procedure to be greatly simplified over that of a standard TO–220. As shown in Figure 5–14(c), one properly chosen clip, inserted into two slotted holes in the heatsink, is all the hardware needed. Even though clip pressure is much lower than obtained with a screw, the thermal resistance is about the same for either method. This occurs because the clip bears directly on top of the die and holds the package flat while the screw causes the package to lift up somewhat under the die. (See Figure B1 of Appendix B.) The interface should consist of a layer of thermal grease or a highly conductive thermal pad. Of course, screw mounting shown in Figure 5–14(b) may also be used but a conical compression washer should be included. Both methods afford a major reduction in hardware as compared to the conventional mounting method with a TO–220 package which is shown in Figure 5–14(a).

Figure 5–13. Plastic Body Mounted Packages

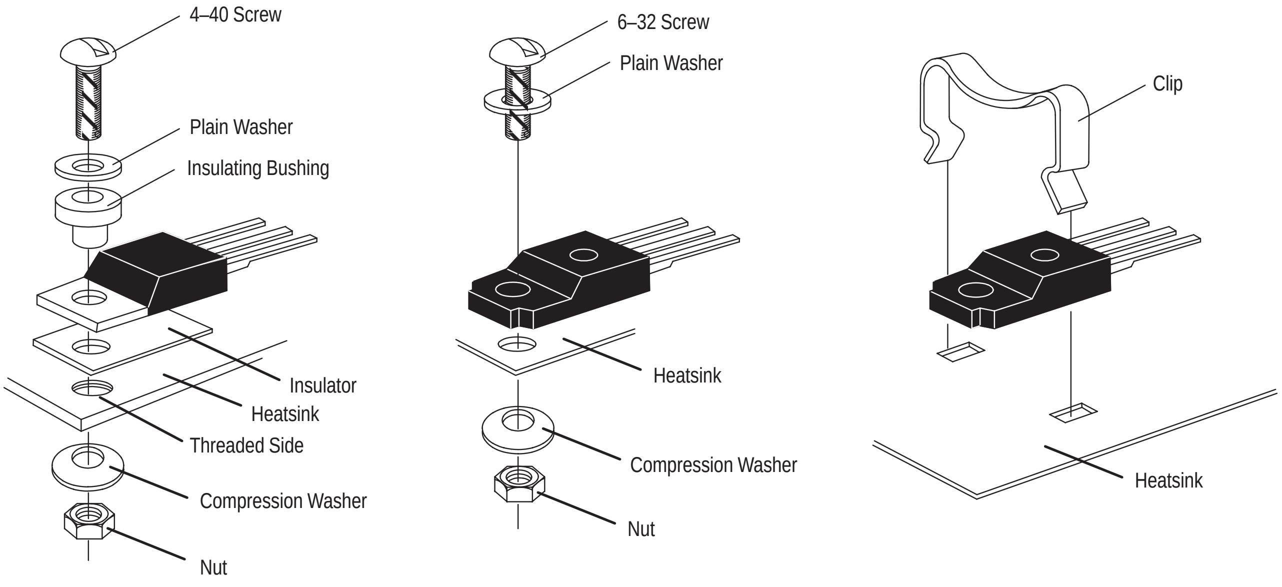


CASE 221C (Full Pak)

CASE 221D (Full Pak)

CASE 340B (Full Pak)

Figure 5–14. Mounting Arrangements for the Full Pak as Compared to a Conventional TO–220



(a) Screw Mounted TO–220

(b) Screw Mounted Full Pak

(c) Clip Mounted Full Pak

Surface Mount

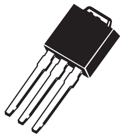
Although many of the tab mount parts have been surface mounted, special small footprint packages for mounting power semiconductors using surface mount assembly techniques have been developed. The DPAK, shown in Figure 5–15, for example, will accommodate a die up to 112 mils × 112 mils, and has a typical thermal resistance around 2°C/W junction to case. The thermal resistance values of the solder interface is well under 1°C/W. The printed circuit board also serves as the heatsink.

Standard glass–epoxy 2 oz. boards do not make very good heatsinks because the thin foil has a high thermal resistance. As Figure 5–16 shows, thermal resistance assymtotes to about 20°C/W at 10 square inches of board area, although a point of diminishing returns occurs at about 3 square inches.

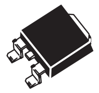
Boards are offered that have thick aluminum or copper substrates. A dielectric coating designed for low thermal resistance is overlayed with one or two ounce copper foil for the preparation of printed conductor traces. Tests run on such a product indicate that case to substrate thermal resistance is in the vicinity of 1°C/W, exact values depending upon board type.(7) The substrate may be an effective heatsink itself, or it can be attached to a conventional finned heatsink for improved performance.

Since DPAK and other surface mount packages are designed to be compatible with surface mount assembly techniques, no special precautions are needed other than to insure that maximum temperature/time profiles are not exceeded.

Figure 5–15. Surface Mounted DPAK Packages

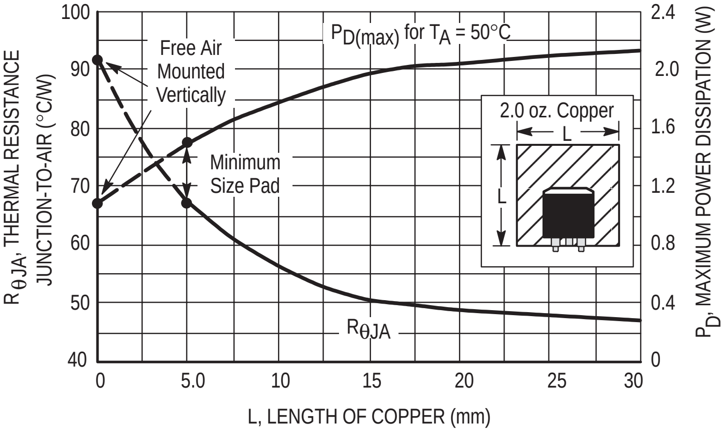


CASE 369



CASE 369A

Figure 5–16. Effect of Footprint Area on Thermal Resistance of DPAK Mounted on a Glass–Epoxy Board



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(7) Herb Fick, *Thermal Management of Surface Mount Power Devices*, Powerconversion and Intelligent Motion, August 1987.

Free Air and Socket Mounting

In applications where average power dissipation is on the order of a watt or so, most power semiconductors may be mounted with little or no heatsinking. The leads of the various metal power packages are not designed to support the packages; their cases must be firmly supported to avoid the possibility of cracked seals around the leads. Many plastic packages may be supported by their leads in applications where high shock and vibration stresses are not encountered and where no heatsink is used. The leads should be as short as possible to increase vibration resistance and reduce thermal resistance. As a general practice however, it is better to support the package. A plastic support for the TO–220 Package and other similar types is offered by heatsink accessory vendors.

In certain situations, in particular where semiconductor testing is required or prototypes are being developed, sockets are desirable. Manufacturers have provided sockets for many of the packages available from Motorola. The user is urged to consult manufacturers' catalogs for specific details. Sockets with Kelvin connections are necessary to obtain accurate voltage readings across semiconductor terminals.

Connecting and Handling Terminals

Pins, leads, and tabs must be handled and connected properly to avoid undue mechanical stress which could cause semiconductor failure. Change in mechanical dimensions as a result of thermal cycling over operating temperature extremes must be considered. Standard metal, plastic, and RF stripline packages each have some special considerations.

Metal Packages

The pins of metal packaged devices using glass to metal seals are not designed to handle any significant bending or stress. If abused, the seals could crack. Wires may be attached using sockets, crimp connectors or solder, provided the data sheet ratings are observed. When wires are attached directly to the pins, flexible or braided leads are recommended in order to provide strain relief.

Plastic Packages

The leads of the plastic packages are somewhat flexible and can be reshaped although this is not a recommended procedure. In many cases, a heatsink can be chosen which makes lead–bending unnecessary. Numerous lead and tab–forming options are available from Motorola on large quantity orders. Preformed leads remove the users risk of device damage caused by bending.

If, however, lead–bending is done by the user, several basic considerations should be observed. When bending the lead, support must be placed between the point of bending and the package. For forming small quantities of units, a pair of pliers may be used to clamp the leads at the case, while bending with the fingers or another pair of pliers. For production quantities, a suitable fixture should be made.

The following rules should be observed to avoid damage to the package.

1. A leadbend radius greater than 1/32 inch for TO–220.
2. No twisting of leads should be done at the case.
3. No axial motion of the lead should be allowed with respect to the case.

The leads of plastic packages are not designed to withstand excessive axial pull. Force in this direction greater than 4 pounds may result in permanent damage to the device. If the mounting arrangement imposes axial stress on the leads, a condition which may be caused by thermal cycling, some method of strain relief should be devised. When wires are used for connections, care should be exercised to assure that movement of the wire does not cause movement of the lead at the lead–to–plastic junctions. Highly flexible or braided wires are good for providing strain relief.

Wire wrapping of the leads is permissible, provided that the lead is restrained between the plastic case and the point of the wrapping. The leads may be soldered; the maximum soldering temperature, however, must not exceed 260°C and must be applied for not more than 5 seconds at a distance greater than 1/8 inch from the plastic case.

Cleaning Circuit Boards

It is important that any solvents or cleaning chemicals used in the process of degreasing or flux removal do not affect the reliability of the devices. Alcohol and unchlorinated freon solvents are generally satisfactory for use with plastic devices, since they do not damage the package. Hydrocarbons such as gasoline and chlorinated freon may cause the encapsulant to swell, possibly damaging the transistor die.

When using an ultrasonic cleaner for cleaning circuit boards, care should be taken with regard to ultrasonic energy and time of application. This is particularly true if any packages are free–standing without support.

Thermal System Evaluation

Assuming that a suitable method of mounting the semiconductor without incurring damage has been achieved, it is important to ascertain whether the junction temperature is within bounds.

In applications where the power dissipated in the semiconductor consists of pulses at a low duty cycle, the instantaneous or peak junction temperature, not average temperature, may be the limiting condition. In this case, use must be made of transient thermal resistance data. For a full explanation of its use, see Motorola Application Note, AN569.

Other applications, notably switches driving highly reactive loads, may create severe current crowding conditions which render the traditional concepts of thermal resistance or transient thermal impedance invalid. In this case, transistor safe operating area, thyristor di/dt limits, or equivalent ratings as applicable, must be observed.

Fortunately, in many applications, a calculation of the average junction temperature is sufficient. It is based on the concept of thermal resistance between the junction and a temperature reference point on the case. (See Appendix A.) A fine wire thermocouple should be used, such as #36 AWG, to determine case temperature. Average operating junction temperature can be computed from the following equation:

$$T_J = T_C + R_{\theta JC} \times P_D$$

where, T_J = junction temperature (°C),
T_C = case temperature (°C),
$R_{\theta JC}$ = thermal resistance junction–to–case as specified on the data sheet (°C/W),
P_D = power dissipated in the device (W).

The difficulty in applying the equation often lies in determining the power dissipation. Two commonly used empirical methods are graphical integration and substitution.

Graphical Integration

Graphical integration may be performed by taking oscilloscope pictures of a complete cycle of the voltage and current waveforms, using a limit device. The pictures should be taken with the temperature stabilized. Corresponding points are then read from each photo at a suitable number of time increments. Each pair of voltage and current values are multiplied together to give instantaneous values of power. The results are plotted on linear graph paper, the number of squares within the curve counted, and the total divided by the number of squares along the time axis. The quotient is the average power dissipation. Oscilloscopes are available to perform these measurements and make the necessary calculations.

Substitution

This method is based upon substituting an easily measurable, smooth dc source for a complex waveform. A switching arrangement is provided which allows operating the load with the device under test, until it stabilizes in temperature. Case temperature is monitored. By throwing the switch to the “test” position, the device under test is connected to a dc power supply, while another pole of the switch supplies the normal power to the load to keep it operating at full power level. The dc supply is adjusted so that the semiconductor case temperature remains approximately constant when the switch is thrown to each position for about 10 seconds. The dc voltage and current values are multiplied together to obtain average power. It is generally necessary that a Kelvin connection be used for the device voltage measurement.

Appendix A
Thermal Resistance Concepts

The basic equation for heat transfer under steady–state conditions is generally written as:

$$q = hA\Delta T \qquad (1)$$

where, q = rate of heat transfer or power dissipation (P_D),

h = heat transfer coefficient,

A = area involved in heat transfer,

ΔT = temperature difference between regions of heat transfer.

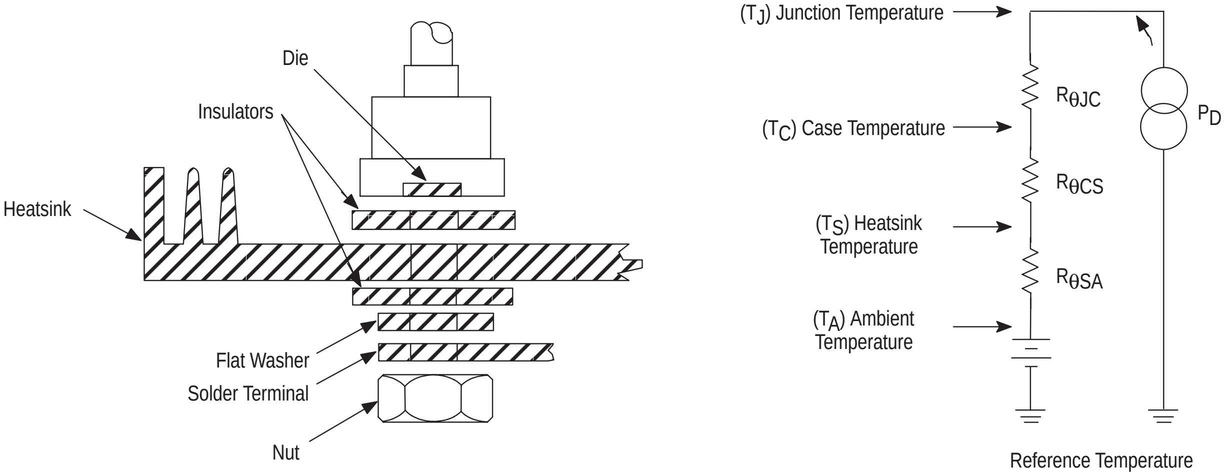
However, electrical engineers generally find it easier to work in terms of thermal resistance, defined as the ratio of temperature to power. From Equation 1, thermal resistance (R_θ) is

$$R_\theta = \Delta T/q = 1/hA \qquad (2)$$

The coefficient (h) depends upon the heat transfer mechanism used and various factors involved in that particular mechanism.

An analogy between Equation 2 and Ohm's Law is often made to form models of heat flow. Note that T could be thought of as a voltage thermal resistance corresponds to electrical resistance (R); and, power (q) is analogous to current (I). This gives rise to a basic thermal resistance model for a semiconductor as indicated by Figure A–1.

Figure A–1. Basic Thermal Resistance Model Showing Thermal to Electrical Analogy for a Semiconductor



The equivalent electrical circuit may be analyzed by using Kirchoff's Law and the following equation results:

$$T_J = P_D(R_{\theta JC} + R_{\theta CS} + R_{\theta SA}) + T_A \qquad (3)$$

where, T_J = junction temperature,

P_D = power dissipation,

$R_{\theta JC}$ = semiconductor thermal resistance (junction–to–case),

$R_{\theta CS}$ = interface thermal resistance (case–to–heatsink),

$R_{\theta SA}$ = heatsink thermal resistance (heatsink–to–ambient),

T_A = ambient temperature.

The thermal resistance junction–to–ambient is the sum of the individual components. Each component must be minimized if the lowest junction temperature is to result.

The value for the interface thermal resistance ($R_{\theta CS}$) may be significant compared to the other thermal resistance terms. A proper mounting procedure can minimize $R_{\theta CS}$.

The thermal resistance of the heatsink is not absolutely constant; its thermal efficiency increases as ambient temperature increases and it is also affected by orientation of the sink. The thermal resistance of the semiconductor is also variable; it is a function of biasing and temperature. Semiconductor thermal resistance specifications are normally at conditions where current density is fairly uniform. In some applications such as in RF power amplifiers and short–pulse applications, current density is not uniform and localized heating in the semiconductor chip will be the controlling factor in determining power handling ability.

Appendix B
Measurement of Interface Thermal Resistance

Measuring the interface thermal resistance $R_{\theta CS}$ appears deceptively simple. All that's apparently needed is a thermocouple on the semiconductor case, a thermocouple on the heatsink, and a means of applying and measuring dc power. However, $R_{\theta CS}$ is proportional to the amount of contact area between the surfaces and consequently is affected by surface flatness and finish and the amount of pressure on the surfaces. The fastening method may also be a factor. In addition, placement of the thermocouples can have a significant influence upon the results. Consequently, values for interface thermal resistance presented by different manufacturers are not in good agreement. Fastening methods and thermocouple locations are considered in this Appendix.

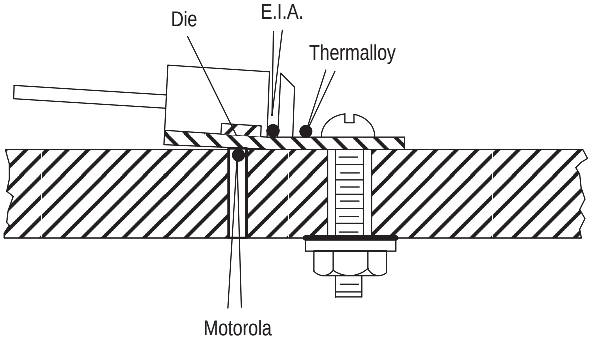
When fastening the test package in place with screws, thermal conduction may take place through the screws, for example, from the flange ear on a TO–204AA package directly to the heatsink. This shunt path yields values which are artificially low for the insulation material and dependent upon screw head contact area and screw material. MIL–I–49456 allows screws to be used in tests for interface thermal resistance probably because it can be argued that this is "application oriented".

Thermalloy takes pains to insulate all possible shunt conduction paths in order to more accurately evaluate insulation materials. The Motorola fixture uses an insulated clamp arrangement to secure the package which also does not provide a conduction path.

As described previously, some packages, such as a TO–220, may be mounted with either a screw through the tab or a clip bearing on the plastic body. These two methods often yield different values for interface thermal resistance. Another discrepancy can occur if the top of the package is exposed to the ambient air where radiation and convection can take place. To avoid this, the package should be covered with insulating foam. It has been estimated that a 15% to 20% error in $R_{\theta CS}$ can be incurred from this source.

Another significant cause for measurement discrepancies is the placement of the thermocouple to measure the semiconductor case temperature. Consider the TO–220 package shown in Figure B–1. The mounting pressure at one end causes the other end — where the die is located — to lift off the mounting surface slightly. To improve contact, Motorola TO–220 Packages are slightly concave. Use of a spreader bar under the screw lessens the lifting, but some is inevitable with a package of this structure.

B–1. JEDEC TO–220 Package Mounted to Heatsink Showing Various Thermocouple Locations and Lifting Caused by Pressure at One End



Three thermocouple locations are shown.

a) The Motorola location is directly under the die reached through a hole in the heatsink. The thermocouple is held in place by a spring which forces the thermocouple into intimate contact with the bottom of the semi's case.

b) The JEDEC location is close to the die on the top surface of the package base reached through a blind hole drilled through the molded body. The thermocouple is swaged in place.

c) The Thermalloy location is on the top portion of the tab between the molded body and the mounting screw. The thermocouple is soldered into position.

Temperatures at the three locations are generally not the same. Consider the situation depicted in Figure B–1. Because the only area of direct contact is around the mounting screw, nearly all the heat travels horizontally along the tab from the die to the contact area. Consequently, the temperature at the JEDEC location is hotter than at the Thermalloy location and the Motorola location is even hotter. Since junction–to–sink thermal resistance must be constant for a given test setup, the calculated junction–to–case thermal resistance values decrease and case–to–sink values increase as the case temperature thermocouple readings become warmer. Thus the choice of reference point for the case temperature is quite important.

There are examples where the relationship between the thermocouple temperatures are different from the previous situation. If a mica washer with grease is installed between the semiconductor package and the heatsink, tightening the screw will not bow the package; instead, the mica will be deformed. The primary heat conduction path is from the die through the mica to the heatsink. In this case, a small temperature drop will exist across the vertical dimension of the package mounting base so that the thermocouple at the EIA location will be the hottest. The thermocouple temperature at the Thermalloy location will be lower but close to the temperature at the EIA location as the lateral heat flow is generally small. The Motorola location will be coolest.

The EIA location is chosen to obtain the highest temperature on the case. It is of significance because power ratings are supposed to be based on this reference point. Unfortunately, the placement of the thermocouple is tedious and leaves the semiconductor in a condition unfit for sale.

The Motorola location is chosen to obtain the highest temperature of the case at a point where, hopefully, the case is making contact to the heatsink. Once the special heatsink to accommodate the thermocouple has been fabricated, this method lends itself to production testing and does not mark the device. However, this location is not easily accessible to the user.

The Thermalloy location is convenient and is often chosen by equipment manufacturers. However, it also blemishes the case and may yield results differing up to 1°C/W for a TO–220 package mounted to a heatsink without thermal grease and no insulator. This error is small when compared to the thermal resistance of heat dissipaters often used with this package, since power dissipation is usually a few watts. When compared to the specified junction–to–case values of some of the higher power semiconductors becoming available, however, the difference becomes significant and it is important that the semiconductor manufacturer and equipment manufacturer use the same reference point.

Another EIA method of establishing reference temperatures utilizes a soft copper washer (thermal grease is used) between the semiconductor package and the heatsink. The washer is flat to within 1.0 mil/inch, has a finish better than 63 µin., and has an imbedded thermocouple near its center. This reference includes the interface resistance under nearly ideal conditions and is therefore application–oriented. It is also easy to use but has not become widely accepted.

A good way to improve confidence in the choice of case reference point is to also test for junction–to–case thermal resistance while testing for interface thermal resistance. If the junction–to–case values remain relatively constant as insulators are changed, torque varied, etc., then the case reference point is satisfactory.

SECTION 6

LINEAR REGULATOR DESIGN EXAMPLE

As an illustration of the use of the material contained in the preceding sections, the following regulator design example is given.

Regulator Performance Requirements:

Output Voltage, $V_O = +10\text{ V} \pm 0.1\text{ V}$
Output Current, $I_O = 1.0\text{ A}$, current limited
Load Regulation, $\leq 0.1\%$ for $I_O = 10\text{ mA}$ to 750 mA
Line Regulation, $\leq 0.1\%$
Output ripple, ≤ 2.0 mVpp
Max Ambient Temperature, $T_A \leq +70°\text{C}$
Supply will have common loads to a negative supply.

1. IC Regulator Selection

Study of the available regulators given in the selection guide reveals that the MC1723C would meet the regulation performance requirements. This regulator must be current boosted to obtain the required 1.0 A output current. A rough cost estimate shows that an MC1723C series pass element combination is the most economical approach.

2. Circuit Configuration

In Section 3, an appropriate circuit configuration is found. This is the MC1723C NPN boost configuration of Figure 3–4A.

3. Determination of Component Values

Using the equations given in Figure 3–4A, the values of C_{ref}, R_1, R_2, R_3 and R_{SC} are determined.

a) C_{ref} is chosen to be 0.1 µF for low noise operation.

b) $R_1 + R_2$ is chosen to be ≈ 10 k.

c) R_2 is then given by: $R_2 \approx \frac{7.0\text{ V}}{V_O}(R_1 + R_2) = 0.7\ (10\text{ k}) = 7.0\text{ k}$

d) Since V_{ref} can vary by as much as ± 5% for the MC1723C, R_2 should be made variable by at least that much, so that V_O can be set to the required value of +10 V ± 0.1 V. R_2 is therefore chosen to consist of a 62 k resistor and a 2.0 k trimpot.

e) $R_1 = 10\text{ k} - R_2 = 10\text{ k} - 7.0\text{ k} = 3.0\text{ k}$

f) $R_{SC} \approx \frac{0.6\text{ V}}{I_{SC}} = \frac{0.6\text{ V}}{1.0\text{ A}} = 0.6\ \Omega$; $0.56\ \Omega$, 1.0 W chosen for R_{SC}.

g) $R_3 = R_1 \,||\, R_2 \cong 2.2\text{ k}$

4. Determination of Input Voltage (V_{in})

There are two basic constraints on the input voltage: 1) the device limits for minimum and maximum V_{in} and, 2) the minimum input–output voltage differential. These limits are found on the device data sheet to be:

$$9.5\text{ V} \le V_{in} \le 40\text{ V and } (V_{in} - V_O) \ge 3.0\text{ V}$$

For the configuration of Figure 3–5A, (V_{in} – V_O) is given by:

$$(V_{in} - V_O) = [V_{in} - (V_O + 2\phi)] \ge 3.0\text{ V, where } \phi = V_{BEon} \approx 0.6\text{ V}$$

Note that (V_{in} – V_O) is defined on the device data sheet to be the differential between the input and output pins. Since the base–emitter junction drops of Q1 and R_{SC} have been added to the circuit, they must be added to the minimum value of (V_{in} – V_O). Therefore,

$$V_{in} \ge V_O + 2\phi + 3.0\text{ V} = 10 + 1.2 + 3$$

$$V_{in} \ge 14.2\text{ V}$$

This condition also satisfies the requirement for a minimum V_{in} of 9.5 V.

In order to simplify the design of the input supply (see Section 8), V_{in} is chosen to be 16 V average with a 3.0 Vpp ripple at full load and up to 25 V at no load. This assures that the input voltage is always above the required minimum value of 14.2 V. Now, the output ripple can be determined. The MC1723C has a typical ripple rejection ratio of –74 db, as given on its data sheet. With an input ripple of 3.0 Vpp, the output ripple would be less than 1.0 mVpp, which meets the regulator output ripple requirements.

5. Selection of the Series Pass Element (Q1)

The transistor type chosen for Q1 must have the following characteristics (see Section 4):

a) $V_{CEO} \ge V_{in(max)}$

b) $I_{C(max)} \ge I_{SC}$

c) $h_{fe} \ge \frac{I_{SC}}{I_O}$ @ $V_{CE} = V_{in} - V_O - \phi$, where $\phi = V_{BEon} \approx 0.6$ V

d) $P_{D(max)} \ge V_{in}, \times I_{SC}$

e) θ_{JC} such to allow practical heatsinking

f) SOA such that it can withstand $V_{CE} = V_{in}$ @ $I_C = I_{SC}$

For this example: $V_{CEO} \ge 25$ V
$I_{C(max)} \ge 1.0$ A
$h_{fe} \ge 25$ @ $V_{CE} = 5.0$ V @ $I_C = 1.0$ A
$P_{D(max)} \ge 16$ W
$\theta_{JC} = 1.52°$C/W
SOA = 1.0 A @ 16 V

A 2N3055 transistor is chosen as a suitable device for Q1 using the selection guide of Section 4 and the transistor data sheets (available from the device manufacturer).

6. Q1 Heatsink Calculation

$$T_J = T_A + P_D\,\theta_{JA} \quad \text{(Equation 15.1 from Section 15)}$$

where, $P_D = V_{in} \times I_{SC}$

$$\theta_{JA} = \theta_{JC} + \theta_{CS} + \theta_{SA} \quad \text{(Equation 6.2)}$$

Solving for θ_{SA}:

$$\theta_{SA} = \left[\frac{T_J - T_A}{P_D}\right] - (\theta_{JC} + \theta_{CS}) \qquad (6.2)$$

From the 2N3055 data sheet, $T_J = 200°C$ and $\theta_{JC} = 1.52°C/W$. The transistor will be mounted with thermal grease directly to the heatsink. Therefore, θ_{CS} is found to be 0.1°C/W from Table 15–1.
Solving for Equation 6.2:

$$\theta_{SA} = \left[\frac{200°C - 70°C}{16\ V \times 1.0\ A}\right] - (1.52 + 0.1)\ °C/W$$

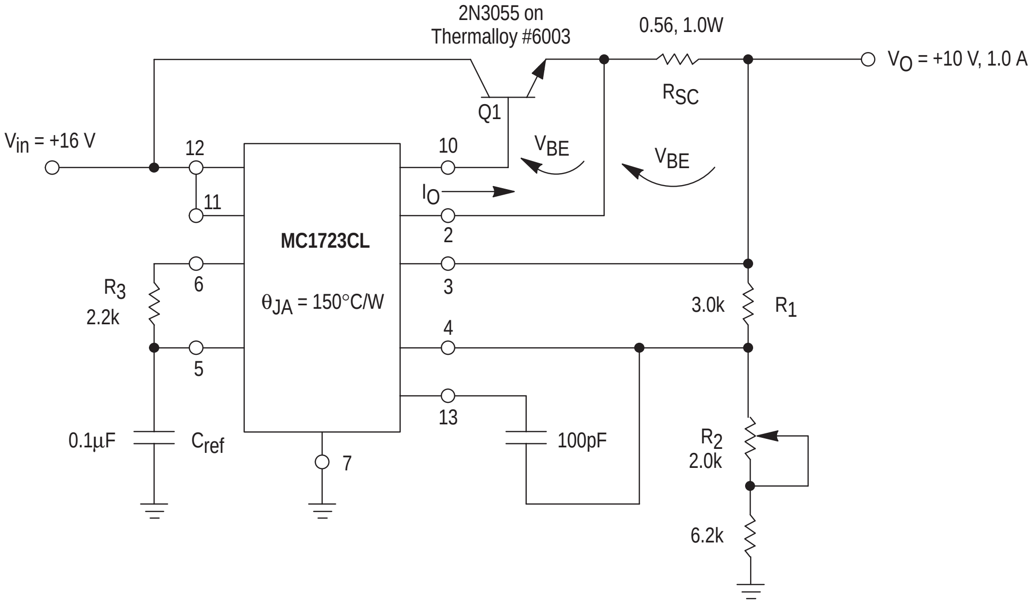
$$\leq 6.6°C/W$$

A commercial heatsink is now chosen from Table 15–2 or one custom designed using the methods given in Section 15. For this example, a Thermalloy #6003 heatsink, having a θ_{CS} of 6.2°C/W, was used.

7. Clamp Diode

Since the regulator can power a load which is also connected to a negative supply, a 1N4001 diode is connected to the output for protection. The complete circuit schematic is shown in Figure 6–1.

Figure 6–1. 10 V, 1.0 A Design Example



8. Construction Input Supply Design

The input supply is now designed using the information contained in Section 8 and the regulator circuit is constructed using the guidelines given in Section 5.

SECTION 7

LINEAR REGULATOR CIRCUIT TROUBLESHOOTING CHECKLIST

Occasionally, the designer's prototype regulator circuit will not operate properly. If problems do occur, the trouble can be traced to a design error in 99.9% of the cases. As a troubleshooting aid to the designer, the following guide is presented.

Of course, it would be difficult, if not impossible, to devise a troubleshooting guide which would cover all possible situations. However, the checklist provided will help the designer pinpoint the problem in the majority of cases. To use the guide, first locate the problem's symptom(s) and then carefully recheck the regulator design in the area indicated using the information contained in the referenced handbook section.

If, after carefully rechecking the circuit, the designer is not successful in resolving the problem, seek assistance from the factory by contacting the nearest Motorola Sales office.

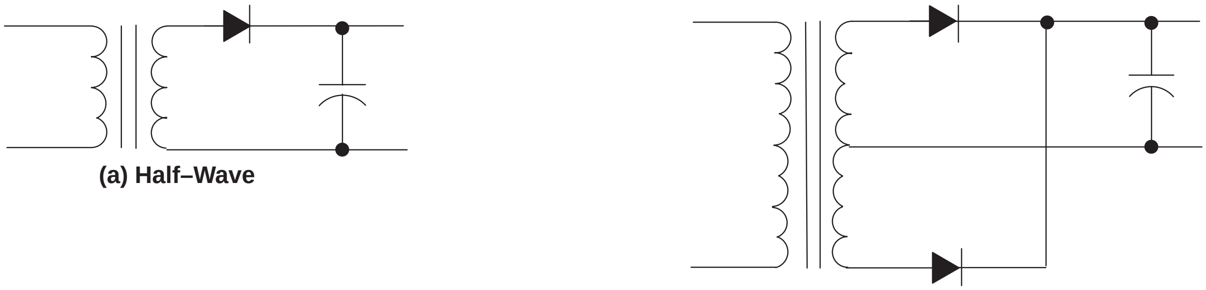
Symptoms	Design Area to Check	Section
Regulator oscillates	1. Layout 2. Compensation capacitor too small 3. Input leads not bypassed 4. External pass element parasitically oscillating	5 3 5 5
Loss of regulation at light loads	1. Emitter–base resistor in "PNP" type boost configuration too large 2. Absence of 1.0 mA ''minimum'' load. (See load regulation test spec on device data sheet) 3. Improper circuit configuration	4 3
Loss of regulation at heavy loads	1. Input voltage too low [$V_{in(min)}$, $\lvert V_{in} - V_O \rvert_{min}$] 2. External pass element gain too low 3. Current limit too low 4. Line resistance between sense points and load 5. Inadequate heatsinking	2, 3 4 3 5 15
IC regulator or pass element fails after warm–up or at high T_A.	1. Inadequate heatsinking 2. Input Voltage Transient $V_{in(max)}$, V_{CEO}	15 2, 4, 5
Pass element fails during short circuit.	1. Insufficient pass element ratings SOA, $I_{C(max)}$ 2. Inadequate heatsinking	4 15
IC regulator fails during short circuit.	1. IC current or SOA capability exceeded 2. Inadequate heatsinking	2
IC regulator fails during power–up	1. Input voltage transient $V_{in(max)}$ 2. IC current or SOA capability exceeded as load (capacitor) is charged up.	2 2
IC regulator fails during power–down.	1. Regulator reverse biased	3
Output voltage does not come up during power–up or after short circuit	1. Out polarity reversal 2. Load has ''latched–up'' in some manner. (Usually seen with op amps, current sources, etc.)	3
Excessive 60 Hz or 120 Hz output ripple	1. Input supply filter capacitor ground loop	5

SECTION 8

DESIGNING THE INPUT SUPPLY

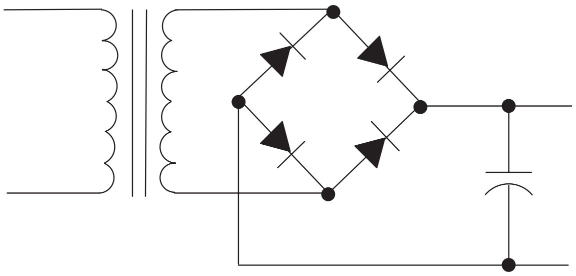
Most input supplies used to power series pass regulator circuits consist of a 60 Hz, single phase step–down transformer followed by a rectifier circuit whose output is smoothed by a choke or capacitor input filter. The type of rectifier circuit used can be either a half–wave, full–wave, or full–wave bridge type, as shown in Figure 8–1. The half–wave circuit is used in low current applications, while the full–wave is preferable in high–current, low output voltage cases. The full–wave bridge is usually used in all other high–current applications.

Figure 8–1. Rectification Schemes



(a) Half–Wave

(b) Full–Wave or Full–Wave Center Tap



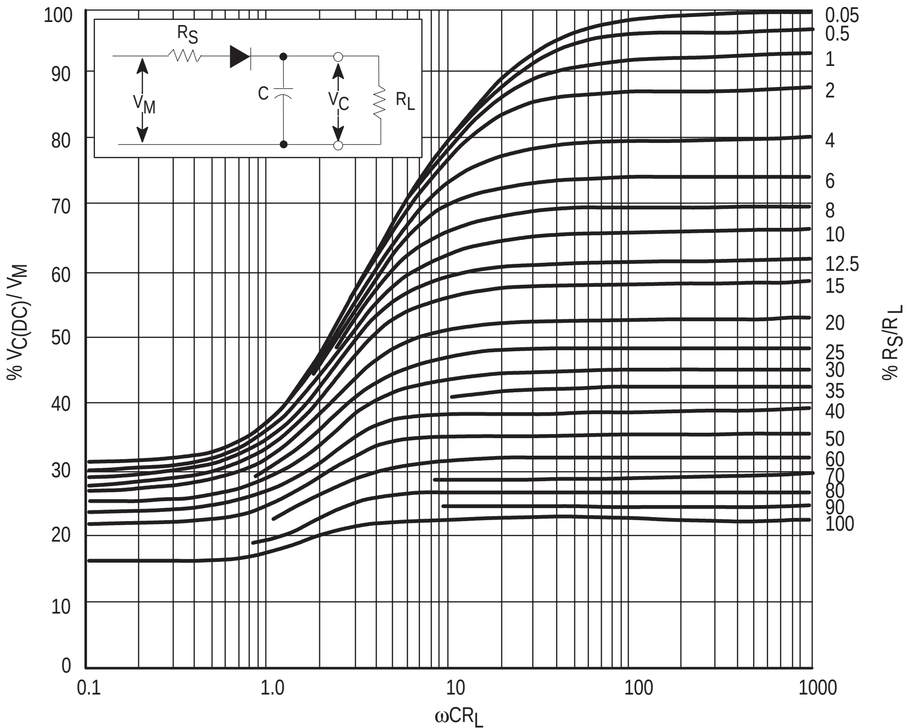
(c) Full–Wave Bridge

In this section, specification of the filter capacitor, rectifier and transformer ratings will be discussed. The specifications for the choke input filter will not be considered since the simpler capacitor input type is more commonly used in series regulated circuits. A detailed description of this type of filter can be found in the reference listed at the end of this section.

1. Design of Capacitor–Input Filters

The best practical procedure for the design of capacitor–input filters still remains based on the graphical data presented by Schade(1) in 1943. The curves shown in Figures 8–2 through 8–5 give all the required design information for half–wave and full–wave rectifier circuits. Whereas Schade originally also gave curves for the impedance of vacuum–tube rectifiers, the equivalent values for semiconductor diodes must be substituted. However, the rectifier forward drop often assumes more significance than the dynamic resistance in low–voltage supply applications, as the dynamic resistance can generally be neglected when compared with the sum of the transformer secondary–winding resistance plus the reflected primary–winding resistance. The forward drop may be of considerable importance, however, since it is about 1.0 V, which clearly cannot be ignored in supplies of 12 V or less.

Figure 8–2. Relation of Applied Alternating Peak Voltage to Direct Output Voltage in Half–Wave Capacitor–Input Circuits



$\omega = 2\pi f$, f = Line Frequency
C in Farads
R_L in Ohms

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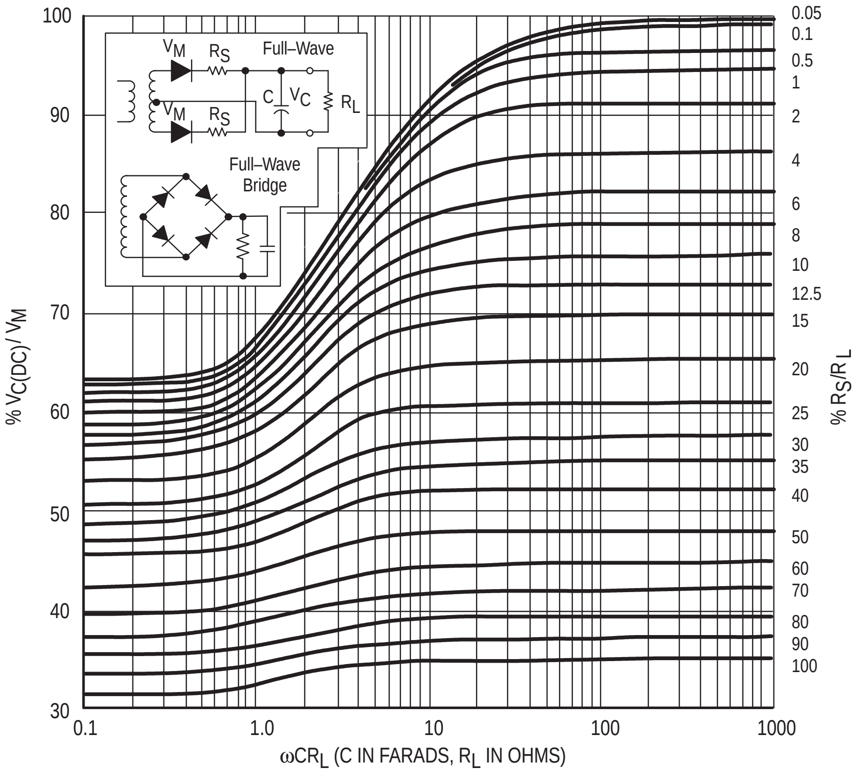
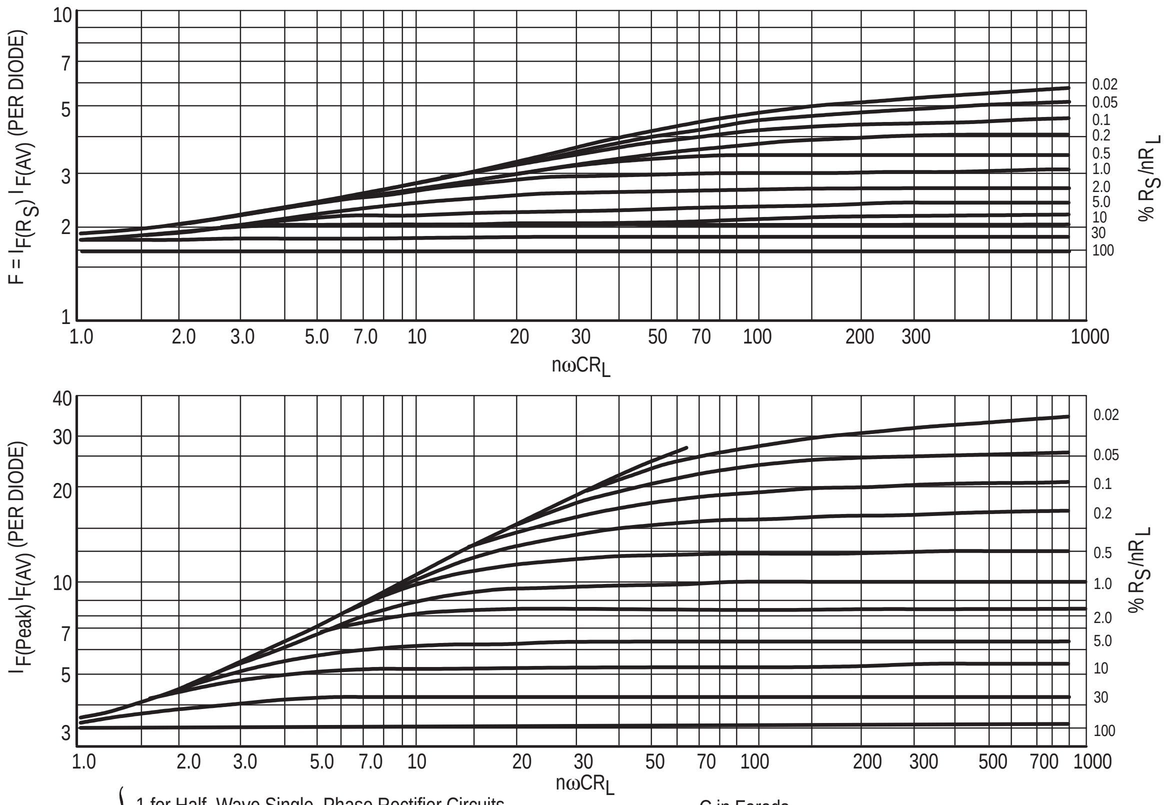
(1)From O. H. Schade, Proc. IRE, Vol. 31, p. 356, 1943.

Figure 8–3. Relation of Applied Alternating Peak Voltage to Direct Output Voltage in Full–Wave Capacitor–Input Circuits



$\omega = 2\pi$ f, f = Line Frequency

Figure 8–4. Relation of RMS and Peak–to–Average Diode Current in Capacitor–Input Circuits

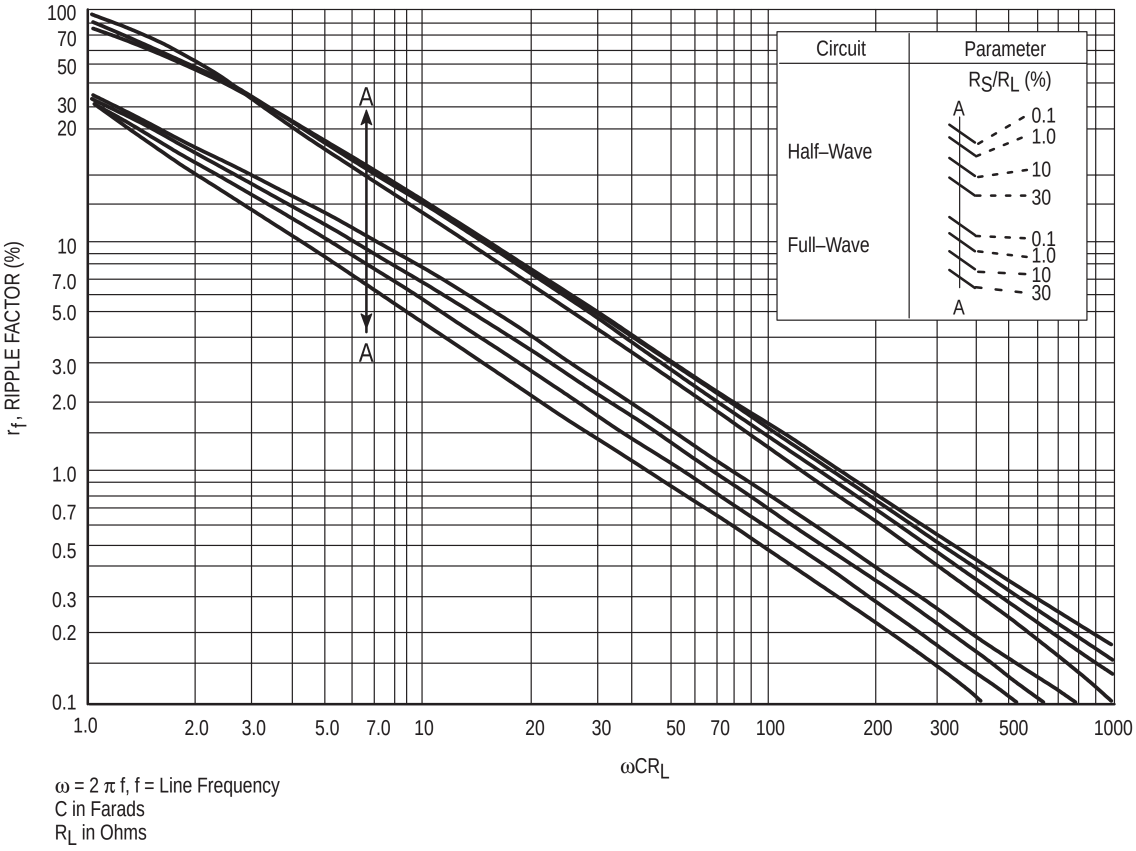


n = { 1 for Half–Wave Single–Phase Rectifier Circuits
2 for Full–Wave Single–Phase Rectifier Circuits

$\omega = 2\pi$ f, where f = Line Frequency

C in Farads
R_L in Ohms
R_S = RMS Equivalent Source Resistance

Figure 8–5. Root–Mean–Square Ripple Voltage for Capacitor–Input Circuits



Returning to the above curves, the full–wave circuit will be considered. Figure 8–3 shows that a circuit must operate with $\omega CR_L \geq 10$ in order to hold the voltage reduction to less than 10% and $\omega CR_L \geq 40$ to obtain less than 2.0% reduction. However, it will also be seen that these voltage reduction figures require R_S/R_L, where R_S is now the total series resistance, to be about 0.1% which, if attainable, causes repetitive peak–to–average current ratios from 10 to 17 respectively, as can be seen from Figure 8–4. These ratios can be satisfied by many diodes; however, they may not be able to tolerate the turn–on surge current generated when the input–filter capacitor is discharged and the transformer primary is energized at the peak of the input waveform. The rectifier is then required to pass a surge current determined by the peak secondary voltage less the rectifier forward drop and limited only by the series resistance R_S. In order to control this turn–on surge, additional resistance must often be provided in series with each rectifier. It becomes evident, then, that a compromise must be made between voltage reduction on the one hand and diode surge rating and hence average current–carrying capacity on the other hand. If small voltage reduction, that is good voltage regulation, is required, a much larger diode is necessary than that demanded by the average current rating.

Surge Current

The capacitor–input filter allows a large surge to develop, because the reactance of the transformer leakage inductance is rather small. The maximum instantaneous surge current is approximately V_M/R_S and the capacitor charges with a time constant $\tau \approx R_S C_1$. As a rough — but conservative — check, the surge will not damage the diode if V_M/R_S is less than the diode I_{FSM} rating and τ is less than 8.3 ms. It is wise to make R_S as large as possible and not pursue tight voltage regulation; therefore, not only will the surge be reduced but rectifier and transformer ratings will more nearly approach the DC power requirements of the supply.

2. Design Procedure

A) From the regulator circuit design (see Section 6), we know:

$V_{C(DC)}$ = the required full load average dc output voltage of the capacitor input filter
$V_{Ripple(pp)}$ = the maximum no load peak–to–peak ripple voltage
V_m = the maximum no load output voltage
I_O = the full–load filter output current
f = the input ac line frequency

B) From Figure 8–5, we can determine a range of minimum capacitor values to obtain sufficient ripple attenuation. First determine r_f:

$$r_f = \frac{V_{Ripple(pp)}}{2\sqrt{2}\,V_{C(DC)}} \times 100\% \qquad (8.1)$$

A range for ωCR_L can now be found from Figure 8–5.

C) Next, determine the range of R_S/R_L from Figure 8–2 or 8–3 using $V_{C(DC)}$ and the values for ωCR_L found in part B. If the range of ωCR_L values initially determined from Figure 8–5 is above $\simeq 10$, R_S/R_L can be found from Figures 8–2 and 8–3 using the lowest ωCR_L value. Otherwise, several iterations between Figures 8–2 or 8–3 and 8–5 may be necessary before an exact solution for R_S/R_L and ωCR_L for a given r_f and $V_{C(DC)}/V_m$ can be found.

D) Once ωCR_L is found, the value of the filter capacitor (C) can be determined from:

$$C = \frac{\omega CR_L}{2\pi f\left(\dfrac{V_{C(DC)}}{I_O}\right)} \qquad (8.2)$$

E) The rectifier requirements may now be determined:

1. Average current per diode;

$I_{F(avg)}$ = I_O for half–wave rectification (8.3)
= $I_O/2$ for full–wave rectification

2. RMS and Peak repetitive rectifier current ratings can be determined from Figure 8–4.
3. The rectifier PIV rating is 2 V_m for the half–wave and full–wave circuits, V_m for the full wave bridge circuit. In addition, a minimum safety margin of 20% to 50% is advisable due to the possibility of line transients.
4. Maximum surge current, $I_{surge} = V_m/(R_S + ESR)$ (8.4)
where, ESR = minimum equivalent series resistance of filter capacitor from its data sheet.

F) Transformer Specification

1. Secondary leg RMS voltage, $V_S = \{V_m + (n)\ 1.0\}/\sqrt{2}$ (8.5)
where; n = 1 for half–wave and full–wave
n = 2 for full–wave bridge
2. Total resistance of secondary and any external resistors to be equal to R_S found from Figures 8–2, 8–3, and 8–4 (see Part C).
3. Secondary RMS current; half–wave = I_{rms}
full–wave = I_{rms} (8.6)
full–wave bridge = $\sqrt{2}\ I_{rms}$
where, I_{rms} = rms rectifier current (from part E.1 and E.2).
4. Transformer VA rating; half–wave = $V_S\ I_{rms}$
full–wave = $2\ V_S\ I_{rms}$ (8.7)
full–wave bridge = $V_S\ I_{rms}(\sqrt{2})$
where, I_{rms} = rms rectifier current (from part E.1 and E.2) and,
V_S = secondary leg RMS voltage.

3. Design Example

A) Find the values for the filter capacitor, transformer rectifier ratings, given Full–Wave Bridge Rectification;

$$\begin{aligned} V_{C(DC)} &= 16\text{ V} \\ V_{Ripple(pp)} &= 3.0\text{ V} \\ V_M &= 25\text{ V} \\ I_O &= 1.0\text{ A} \\ f &= 60\text{ Hz} \end{aligned}$$

B) Using Equation (8.1),

$$r_f = \frac{3}{2\sqrt{2}\,(16)} \times 100\% = 6.6\%$$

from Figure 8.5, $\omega CR_L \simeq 7$ to 15

C) Using $\omega CR_L = 10$, R_S/R_L is found from Figure 8–3 using,

$$\frac{V_{C(DC)}}{V_M} = \frac{16}{25} = 0.64 = 64\%$$

$$R_S/R_L = 20\% \text{ or } R_S = 0.2 \times R_L = 0.2\left(\frac{V_{C(DC)}}{I_O}\right) = 0.2\,(16)$$

$$R_S = 3.2\ \Omega$$

D) From Equation (8.2), the filter capacitor size is found:

$$C = \frac{\omega CR_L}{2\pi f\left(\frac{V_{C(DC)}}{I_O}\right)} = \frac{10}{2\pi f(60)16} = 1658\ \mu\text{F}$$

E) The rectifier ratings are now specified:

1. $I_{F(avg)} = I_O/2 = 0.5$ A from Equation (8.3)
2. $I_{F(rms)} = 2 \times I_{F(AVG)} = 1.0$ A from Figure 8–4
3. $I_{F(Peak)} = 5.2 \times I_{F(AVG)} = 2.6$ A from Figure 8–4
4. PIV = V_M = 25 V (use 50 V for safety margin)
5. $I_{surge} = V_M/(R_S + ESR) \simeq 25/3.2 = 7.8$ A from Equation (8.4), neglecting capacitor ESR.

F) The transformer should have the following ratings:

1. $V_S = \{V_M + n(1.0)\}/\sqrt{2} = (25 + 2)/\sqrt{2} = 19$ VRMS {from Equation (8.5)}
2. Secondary Resistance should be 3.2 Ω
3. Secondary RMS current rating should be 1.4 A, (from Equation (8.6)).
4. From Equation (8.7), the transformer should have a 27 VA rating.

It should be noted that, in order to simplify the procedure, the above design does not allow for line voltage variations or component tolerances. The designer should take these factors into account when designing his input supply. Typical tolerances would be: line voltage = +10% to –15% and filter capacitors = +75% to –10%.

REFERENCES
1. O. H. Schade, Proc. IRE, Vol. 31, 1943.
2. Motorola Silicon Rectifier Manual, 1980.

SECTION 9

AN INTRODUCTION TO SWITCHING POWER SUPPLIES

The Switching Power Supply continues to increase in popularity and is one of the fastest growing markets in the world of power conversion. Its performance and size advantages meet the needs of today's modern and compact electronic equipment and the increasing variety of components directed at these applications makes new designs even more practical.

This guide is intended to provide the designer with an overview of the more popular inverter circuits, their basic theory of operation, and some of the subtle characteristics involved in selecting a circuit and the appropriate components. Also included are valuable design tips on both the major passive and active components needed for a successful design. Finally, a complete set of selector guides to Motorola's Switchmode components is provided which gives a detailed listing of the industry's most comprehensive line of semiconductor products for switching power supplies.

Comparison with Linear Regulators

The primary advantages of a switching power supply are efficiency, size,and weight. It is also a more complex design, cannot meet some of the performance capabilities of linear supplies and generates a considerable amount of electrical noise. However switchers are being accepted in the industry, particularly where size and efficiency are of prime importance. Performance continues to improve and for most applications they are usually cost competitive down to the 20 W power level.

In the past the switcher's advantage versus the linear regulator was in the high power arena where passive components such as transformers and filters were small compared to the linear regulator at the same power level. However, active component count was high and tended to make the switcher less cost effective at low power levels. In recent years, Switchers have been significantly cost reduced because designers have been able to simplify the control circuits with new, cost effective integrated circuits and have found even lower cost alternatives in the passive component area.

A performance comparison chart of switching versus linear supplies is shown in Table 9–1. Switcher efficiencies run from 70% to 80% but occasionally fall to (60% to 65%) when linear post regulators are used for the auxiliary outputs. Some linear power supplies on the other hand, are operated with up to 50% efficiency but these are areas where line variations or hold–up time problems are minimal. Most linears operate with typical efficiencies of only 30%. The overall size reduction of a 20 kHz switcher is about 4:1 and newer designs in the 100 kHz to 200 kHz region end up at about 8:1 (versus a linear). Other characteristics such as static regulation specs are comparable, while ripple and load transient response are usually worse. Output noise specs can be somewhat misleading. Very often a 500 mV switching spike at the output may be attenuated considerably at the load itself due to the series inductance of the connecting cables and the additional filter capacitors found in many logic circuits. In the future, the noise generated at higher switching frequencies (100 kHz to 500 kHz) will probably be easier to filter and the transient response will be faster. Hold–up time is greater for switchers because it is easier to store energy in high voltage capacitors (200 V to 400 V) than in the lower voltage (20 V to 50 V) filter capacitors common to linear power supplies. This is due to the fact that the physical size of a capacitor is dependent on its CV product while energy storage is proportional to CV^2.

Table 9–1. 20 kHz Switcher versus Linear Performance

Parameter	Switcher	Linear
Efficiency	75%	30%
Size	2.0 W/in^3	0.5 W/in^3
Weight	40 W/lb	10 W/lb
Line and Load Regulation	0.1%	0.1%
Output Ripple V_{pp}	50 mV	5.0 mV
Noise V_{pp}	50 mV to 200 mV	—
Transient Response	1.0 ms	20 µs
Hold–Up Time	20 ms to 30 ms	1.0 ms to 2.0 ms

Basic Configurations

A switching power supply is a relatively complex circuit as is shown by the four basic building blocks of Figure 9–1. It is apparent here that the heart of the supply is really the high frequency inverter. It is here that the work of chopping the rectified line at a high frequency (20 kHz to 200 kHz) is done. It is here also that the line voltage is transformed down to the correct output level for use by logic or other electronic circuits. The remaining blocks support this basic function. The 60 Hz input line is rectified and filtered by one block and after the inverter steps this voltage down, the output is again rectified and filtered by another. The task of regulating the output voltage is left to the control circuit which closes the loop from the output to the inverter. Most control circuits generate a fixed frequency internally and utilize pulse width modulation techniques to implement the desired regulation. Basically, the on–time of the square wave drive to the inverter is controlled by the output voltage. As load is removed or input voltage increases,the slight rise in output voltage will signal the control circuit to deliver shorter pulses to the inverter and conversely as the load is increased or input voltage decreases, wider pulses will be fed to the inverter.

The inverter configurations used in today's switchers actually evolved from the buck and boost circuits shown in Figures 9–2a and 9–2b. In each case the regulating means and loop analysis will remain the same but a transformer is added in order to provide electrical isolation between the line and load. The forward converter family which includes the push–pull and half bridge circuits evolved from the buck regulator (Figure 9–2a). And the newest switcher, the flyback converter, actually evolved from the boost regulator. The buck circuit interrupts the line and provides a variable pulse width square wave to a simple averaging LC filter. In this case, the first order approximation of the output voltage is $V_{out} = V_{in} \times$ duty cycle and regulation is accomplished by simply varying the duty cycle. This is satisfactory for most analysis work and only the transformer turns ratio will have to be adjusted slightly to compensate for IR drops, diode drops, and transistor saturation voltages.

Operation of the boost circuit is more subtle in that it first stores energy in a choke and then delivers this energy plus the input line to the load. However, the flyback regulators which evolved from this configuration delivers only the energy stored in the choke to the load. This method of operation is actually based on the buck boost model shown in Figure 9–2c. Here, when the switch is opened, only the stored inductive energy is delivered to the load. The true boost circuit can also regulate by stepping up (or boosting) the input voltage whereas the buck–boost or flyback regulator can step the input voltage up or down. Analysis of the boost regulator begins by dealing with the choke as an energy storage element which delivers a fixed amount of power to the load: $P_O = 1/2\ L\ If_O$ where, I = the peak choke current; $f_O =$ the operating frequency; and, L = the inductance.

Because it delivers a fixed amount of power to the load regardless of load impedance (except for short circuits), the boost regulator is the designer's first choice in photoflash and capacitive–discharge (CD) automotive ignition circuits to recharge the capacitive load. It also makes a good battery charger. For an electronic circuit load, however, the load resistance must be known in order to determine the output voltage:

$$V_O = \sqrt{P_O R_L} = I \sqrt{\frac{L f_O R_L}{2}} \quad \text{where, } R_L = \text{the load resistance.}$$

In this case, the choke current is proportional to the on–time or duty cycle of the switch and regulation for fixed loads simply involves varying the duty cycle as before. However, the output also depends on the load which was not the case with buck regulators and results in a variation of loop gain with load.

Figure 9–1. Functional Block Diagram — Switching Power Supply

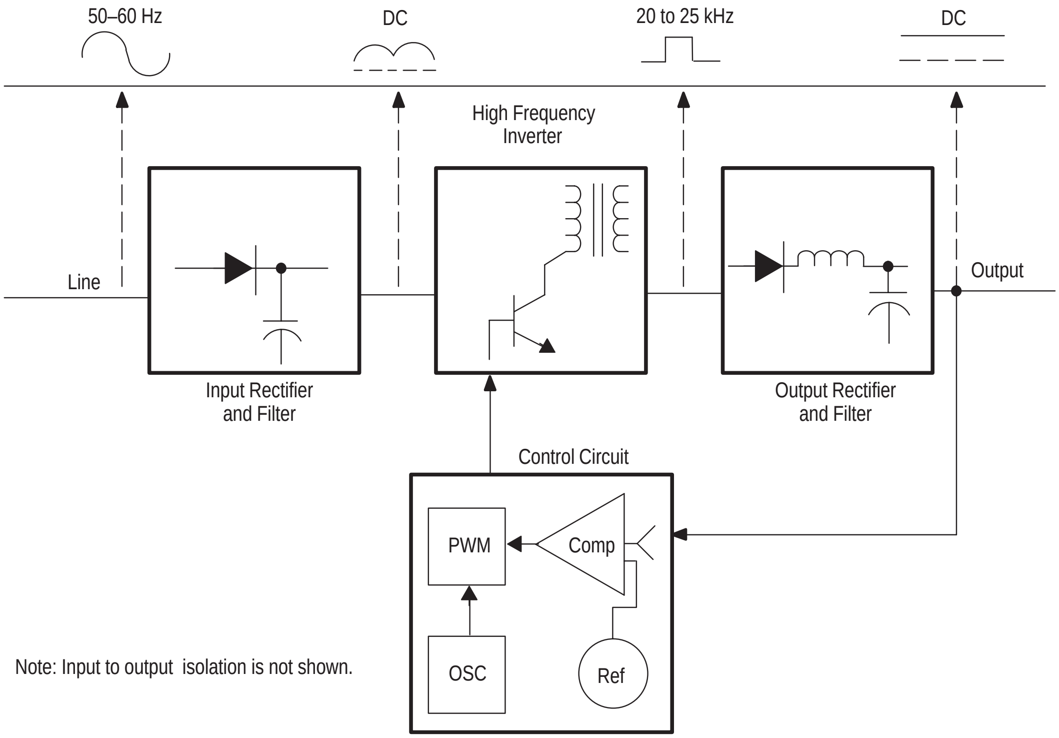
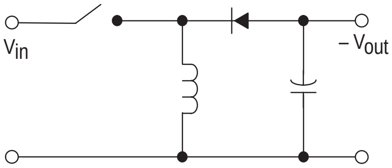


Figure 9–2. Nonisolated DC–DC Converters

(a) Buck (Step–Down)

(b) Boost (Step–Up)



(c) Buck–Boost Regulator
which Resembles the Flyback Regulator
(Step–Up or Down)

For both regulators, transient response or responses to step changes in load are very difficult to analyze. They lead to what is termed a “load dump” problem. This requires that energy already stored in the choke or filter be provided with a place to go when load is abruptly removed. Practical solutions to this problem include limiting the minimum load and using the right amount of filter capacitance to give the regulator time to respond to this change.

The Future

The future offers a lot of growth potential for switchers in general and low power switchers (20 W to 100 W) in particular. The latter are responding to the growth in microprocessor based equipment as well as computer peripherals. Today’s configurations have already been challenged by the sine wave inverter which reduces noise and improves transistor reliability but does effect a cost penalty. Also, a trend to higher switching frequencies to reduce size and cost even further has begun. The latest bipolar designs operate efficiently up to 100 kHz and the FET seems destined to own the 200 kHz to 500 kHz range.

At this time there are a lot of safety and noise specifications. Originally governed only by MIL specs and the VDE in Europe, now both UL and the FCC have released a set of specifications that apply to electronic systems which often include switchers (see Table 9–2). It seems probable, however, that system engineers or power supply designers will be able to add the necessary line filters and EMI shields without evoking a significant cost penalty in the design.

The most optimistic note concerning switchers is in the component area. Switching power supply components have actually evolved from components used in similar applications. And it is very likely that newer and more mature products specifically for switchers will continue to appear over the next several years. The ultimate effect of this evolution will be to further simplify, cost reduce and increase the reliability of these designs.

Table 9–2. SMPS Specifications

Specification	Area
UL 478, VDE 0730, VDE 0806	Safety
VDE 0871, VDE 0875	EMI
MIL–STD–217D	Reliability
MIL–STD–461A	EMI
DOD–STD–1399	Harmonic Content
FCC Class A & B	EMI
CSA C22.2, IEC 380	Safety

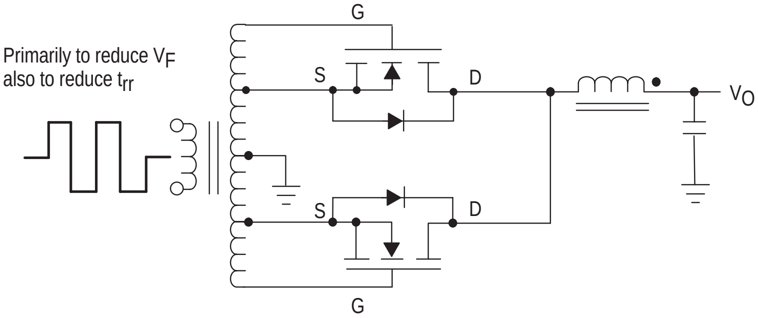
The synchronous rectifier is one example of a new component developed specifically for low voltage switchers. As requirements for 2.0 V and 3.0 V supplies emerge for use by fine geometry VLSI chips, the only way to maintain decent conversion efficiency is to develop lower forward drop rectifiers. The differences in 3.0 V and 5.0 V rectifier requirements are shown in Table 9–3. At this time, Motorola offers low V_F Schottky and area efficient TMOS III FETs for this task and is considering a variety of additional technology options. The direct approach involves using low V_F Schottkys or pinch rectifiers which will feature V_Fs of 0.3 V to 0.4 V. The indirect approach involves using FETs or bipolar transistors and slightly more complex circuitry like that shown in Figure 9–3. Both transistors will feature V_Fs of 0.2 V and, in addition, the bipolar will have high EBOs (30 V) and high gain (100) with a recovery time of 100 ns.

And for designers who are not satisfied with the relatively low frequency limitations of square wave switchers, there is the SRPS. The series resonant power supply topology seems to offer the possibility of working in the 1.0 MHz region. If components like the relatively exotic power transformer can be cost reduced, then it will be possible for this topology to become dominant in the market. The features generally associated with this type of power supply are listed in Table 9–4 and a typical half bridge circuit is shown in Figure 9–4. In a design now being studied in Motorola’s advanced products laboratory, standard FETs, Schottkys and ultrafast rectifiers all appear to work very well at 1.0 MHz.

Table 9–3. Synchronous Rectifier Requirements

Output Voltage	Rectifier Characteristics	
	V_F	V_R
5.0 V	0.5 V–1.0 V	30 V–60 V
3.0 V	0.3 V–0.6 V	20 V–40 V

Figure 9–3. Synchronous Rectifiers for 3.0 V Power Supplies

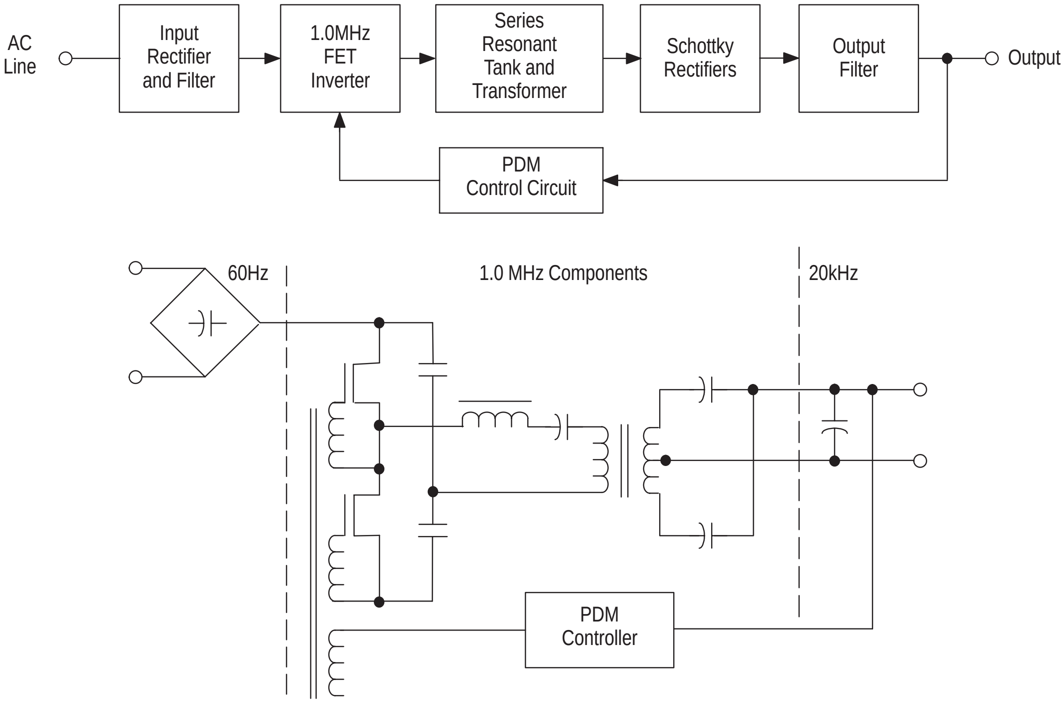


Note: The FET must be operated below V_F of the diode in order to gain the t_{rr} advantage.

Table 9–4. SRPS Features

Feature	Description
High Frequency	Today's line operated designs use sine waves in the 500 kHz to 1.0 MHz range.
Small Size	The ferrite transformer and polypropylene coupling capacitor are smaller than those found in lower frequency square wave designs.
Low Noise	Switching occurs at zero crossings which reduces component stress and lowers EMI.
Efficient	Because switching losses are reduced, efficiency is high (typically 80%).
High Peak to Average Current Ratios	Current ratings of the transistors and rectifiers are twice as high as similar flyback designs.
Special Control Circuit	PDM (density) rather than PWM (width) control is used and requires a control IC with a programmable VCO.
Market	The SRPS is expected to own 15% of the power supply market by 1990.

Figure 9–4. SRPS Block Diagram



SECTION 10

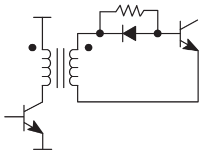
SWITCHING REGULATOR TOPOLOGIES

FET and Bipolar Drive Considerations

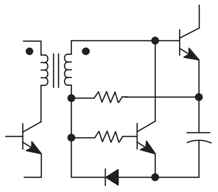
There are probably as many base drive circuits for bipolars as there are designers. Ideally, the transistor would like just enough forward drive (current) to stay in or near saturation and reverse drive that varies with the amount of stored base charge such as a low impedance reverse voltage. Many of today's common drive circuits are shown in Figure 10–1. The fixed drive circuits of Figure 10(a), (b) and (c) tend to emphasize economy, while the Baker clamp and proportional drive circuits of Figure 10(d) and (e) emphasize performance over cost.

FET drive circuits are another alternative. The standard that has evolved at this time is shown in Figure 10–2A. This transformer coupled circuit will produce forward and reverse voltages applied to the FET gate which vary with the duty cycle as shown. For this example, a V_{GS} rating of 20 V would be adequate for the worst case condition of high logic supply (12 V) and minimum duty cycle. And yet, minimum gate drive levels of 10 V are still available with duty cycles up to 50%. If wide variations in duty cycle are anticipated, it might be wise to consider using a semi–regulated logic supply for these situations. Finally, one point that is not obvious when looking at the circuit is that FETs can be directly coupled to many ICs with only 100 mA of sink and source capability and still switch efficiently at 20 kHz. However, to achieve switching efficiently at higher frequencies, 1.0 A to 2.0 A of drive may be required on a pulsed basis in order to quickly charge and discharge the gate capacitances. A simple example will serve to illustrate this point and also show that the Miller effect, produced by C_{DG}, is the predominant speed limitation when switching high voltages (see Figure 10–2B). A FET responds instantaneously to changes in gate voltage and will begin to conduct when the threshold is reached (V_{GS} = 2.0 V to 3.0 V) and be fully on with V_{GS} = 7.0 V to 8.0 V. Gate waveforms will show a porch at a point just above the threshold voltage which varies in duration depending on the amount of drive current available and this determines both the rise and fall times for the drain current.

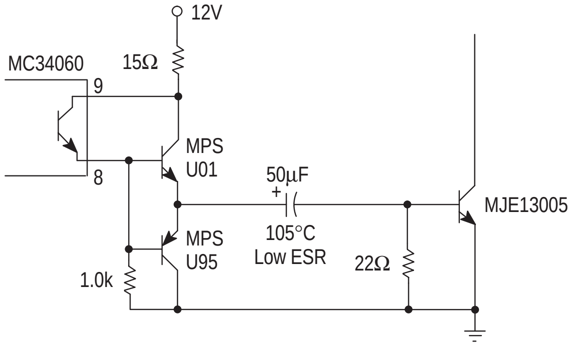
Figure 10–1. Typical Bipolar Base Drive Circuits



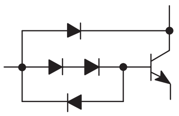
(a) Fixed Drive, Turn–Off Energy Stored in Transformer



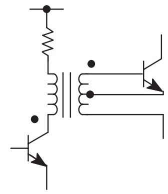
(b) Fixed Drive, Turn–Off Energy Stored in Capacitor



(c) Direct Drive

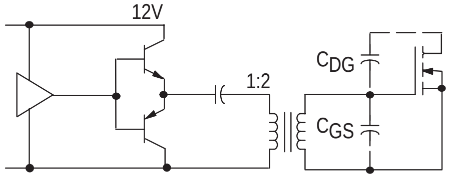


(d) Standard Baker Clamp

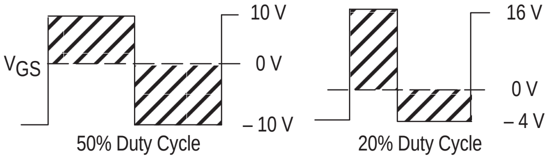


(e) Proportional Base Drive

Figure 10–2A. Typical Transformer Coupled FET Drive

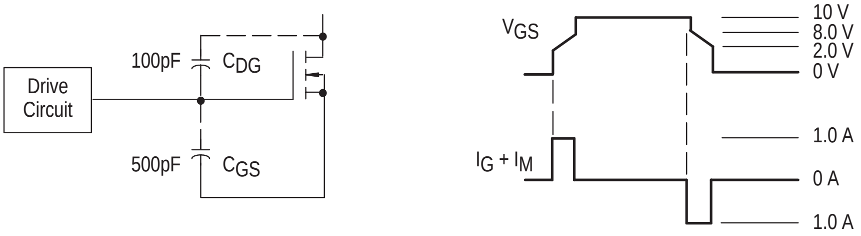


Wave Forms



V_{GS} Wave Forms

Figure 10–2B. FET Drive Current Requirements



1. Miller Current for 30 ns:
$I_M = C_{DG}\ dv/dt$
$= 100\ pF \times \frac{300\ V}{30\ ns} = 1.0\ A$

2. Gate Cap Current for 30 ns:
$I_G = C_{GS}\ dv/dt$
$= 500\ pF \times \frac{6.0\ V}{30\ ns} = 0.1\ A$

To estimate drive current requirements, two simple calculations with gate capacitances can be made:

1. $I_M = C_{DG} dv/dt$ and,
2. $I_G = C_{GS} dv/dt$

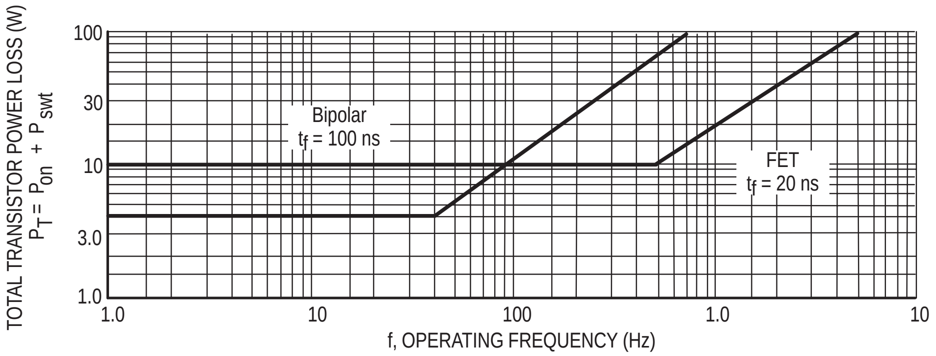
I_M is the current required by the Miller Effect to charge the drain–to–gate capacitance at the rate it is desired to move the drain voltage (and current). And I_G is usually the lesser amount of current required to charge the gate–to–source capacitance through the linear region (2.0 V to 8.0 V). As an example, if 30 ns switching times are desired at 300 V, where C_{DG} = 100 pF and C_{GS} = 500 pF, then:

1. I_M = 100 pF × 300 V/30 ns = 1.0 A and,
2. I_G = 500 pF × 6.0 V/30 ns = 0.1 A

This example shows the direct proportion of drive current capability to speed and also illustrates that for most devices, C_{DG} will have the greatest effect on switching speed and that C_{GS} is important only in estimating turn–on and turn–off delays.

Aside from its unique drive requirements, a FET is very similar to a bipolar transistor. Today’s 400 V FETs compete with bipolar transistors in many switching applications. They are faster and easier to drive, but do cost more and have higher saturation, or more accurately, “on” voltages. The performance or efficiency tradeoffs are analyzed using Figure 10–3, where typical power losses for switching transistors versus frequency are shown. The FET (and bipolar) losses were calculated at 100°C rather than 25°C because on resistance and switching times are highest here and 100°C is typical of many applications. These curves are asymptotes of the actual device performance, but are useful in establishing the “breakpoint” of various devices, which is the point where saturation and switching losses are equal.

Figure 10–3. Typical Switching Losses at 300 V and 5.0 A (T_J = 100°C)



Control Circuits

Over the years, a variety of control ICs for SMPS have been introduced. The voltage mode controllers diagramed in Table 10–1 still dominate this market. The basic regulating function is performed in the pulse width modulator (PWM) section. Here, the dc feedback signal is compared to a fixed frequency sawtooth waveform. The result is a variable duty cycle pulse train which, with suitable buffer or interface circuits, can be used to drive the power switching transistor. Some ICs provide only a single output while others provide a phase splitter or flip–flop to alternately pulse two output channels. Additionally, most ICs provide an error amplifier and reference section shown as a means to process, compare and amplify the feedback signal.

Features required by a control IC vary to some extent because of the particular needs of a designer and on the circuit configuration chosen. However, most of today's current generation ICs have evolved with the following capabilities or features:

- Programmable (to 500 kHz) Fixed Frequency Oscillator
- Linear PWM Section with Duty Cycle from 0% to 100%
- On Board Error Amplifiers
- On Board Reference Regulator
- Adjustable Deadtime
- Under Voltage (low V_{CC}) Inhibit
- Good Output Drive (100 mA to 200 mA)
- Option of Single or Dual Channel Output
- Uncommitted Output Collector and Emitter or Totem Pole Drive Configuration
- Soft–Start
- Digital Current Limiting
- Oscillator Sync Capability

It is primarily the cost differences in these parts that determine whether all or only part of these features will be incorporated. Most of these are evident to the designer who has already started comparing competitive device data sheets.

In addition to the control circuits listed in Table 10–2, Motorola also has two dc converter control chips, the µA78S40 and the MC34063A. These chips feature an on–board 40 V, 2.0 A switching transistor and operate by dropping pulses from a fixed frequency, fixed duty cycle oscillator depending on load demand.

Today there is a demand for simple, low cost, single control ICs. These ICs, like Motorola's MC34060A and MC34063A components, are used to run the low–power flyback type configurations and are usually part of a three chip rather than a single chip system. The differences in these two approaches are illustrated in Figure 10–6.

When it is necessary to drive two or more power transistors, drive transformers are a practical interface element and are driven by the conventional dual channel ICs. In the case of a single transistor converter, however, it is usually more cost effective to directly drive the transistor from the IC. In this situation, an optocoupler is commonly used to couple the feedback signal from the output back to this control IC. And the error amplifier in this case is nothing more than a programmable zener like Motorola's TL431.

Overvoltage Protection

Linear and switching power supplies can be protected from overvoltage with a crowbar circuit. For linear supplies, the pass transistor can fail shorted, allowing high line transformer voltage to the load. For switching power supplies, a loose or disconnected remote sense lead can allow high voltage to the load.

Table 10–1. Basic SM Control ICs

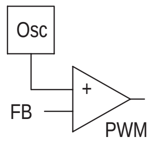
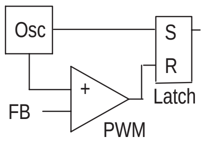
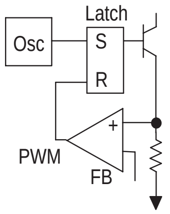
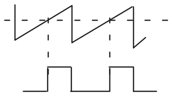
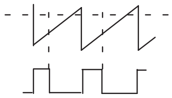
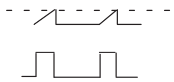
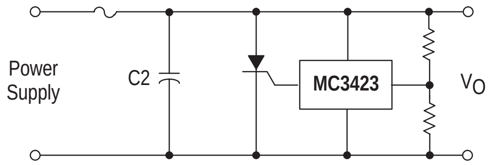
Control Technique	Type A Voltage Mode	Type B Voltage Mode w/Latch	Type C Current Mode
Schematic			
Single Channel Parts	MC34060A	—	UC3842 MC34129
Dual Channel Parts	TL494/594	SG3525A/27A SG3526	—
Features	Low Cost	Digital Current Limiting, Good Noise Immunity	Designed for Flyback, Inherent Feed Forward
PWM Waveforms **Output**			

Table 10–2. Control Circuits

Overvoltage Protection (OVP)		Over/Undervoltage Protection (O/UVP)	Undervoltage Sense MPU/MCU Reset
Standard	**High Performance**		
TL431	MC3423 TL431A	MC3425 MC34161	MC34064–5 MC34164–3 MC34164–5

The list of available circuits is shown in Table 10–2 and a typical 0 V application is shown in Figure 10–4. This crowbar circuit ignores noise spikes but will fire the SCR when a valid overvoltage condition is detected. The SCR will discharge C2 and either blow the fuse or cause the power supply to shut down.

Figure 10–4. Crowbar Circuit



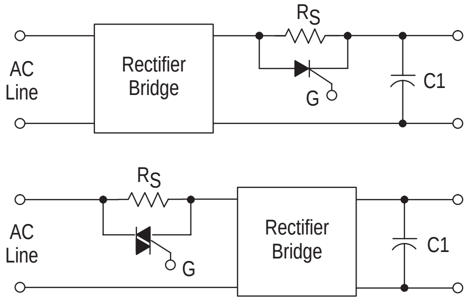
For further information, see the MC3423 data sheet.

Surge Current Protection

Many high current PWM switching supplies operate directly off the ac line. They have very large capacitive input filters with high inrush surge currents. The line circuit breaker and the rectifier bridge must be protected during turn–on.

Surge current limiting can be accomplished by adding R_S and an SCR short after charging C1, as shown in Figure 10–5, or by phase controlling the line voltage with a Triac.

Figure 10–5. Surge Current Limiting for a Switching Power Supply



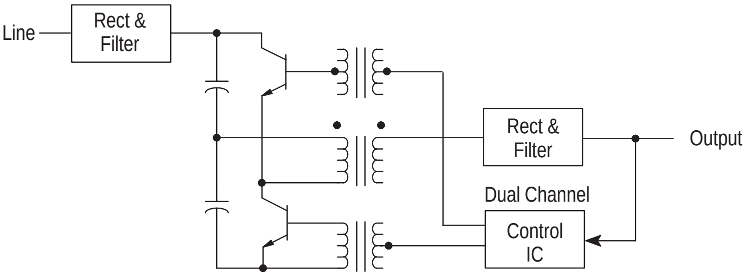
Transformer Design

With respect to transformer design, many of today’s designers would say don’t try it. They’d advise using a consultant or winding house to perform this task and with good reason. It takes quite a bit of time to develop a feel for this craft and be able to use both experience and intuition to find solutions to second and third order problems. Because of these subtle problems, most designers find that after the first paper design is done, as many as four or five lab iterations may be necessary before the transformer meets the design goals. However, there is a considerable design challenge in this area and a great deal of satisfaction can be obtained by mastering it.

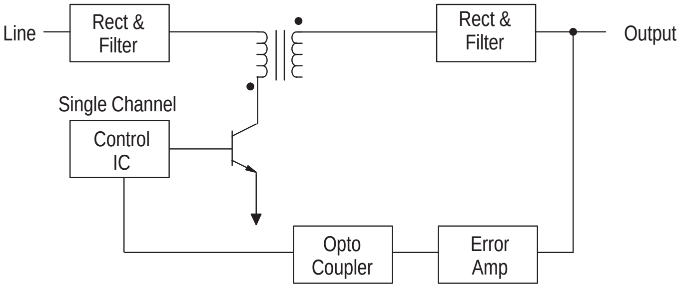
This component design, as do all others, begins by requesting all available literature from the appropriate manufacturers and then following this up with phone calls when specific questions arise. A partial list of companies is shown in Table 10–3. Designs below 20 W generally use pot cores, but for 20 W and above, E cores are preferred. E cores expose the windings to air so that heat is not trapped inside and make it easier to bring out connections for several windings. Remember that flyback designs require lower permeability cores than the others. The classic approach is to consult manufacturers charts like the one shown in Figure 10–8 and then to pick a core with the required power handling ability. Both E and EC (E cores with a round center leg) are popular now and they are available from several manufacturers. EC cores offer a performance advantage (better coupling) but standard E cores cost less and are also used in these applications. Another approach that seems to work equally well is to do a paper design of the estimated windings and turns required. Size the wire for 500 circular mils (CM) per amp and then find a core that has the required window area for this design. Now, before the windings are put on, it is a good idea to modify the turns so that they fit on one layer or an integral number of layers on that bobbin. This involves checking the turns per inch of the wire against the bobbin length. The primary generally goes on first and then the secondaries. If the primary hangs over an extra half layer, try reducing the turns or the wire size. Conversely, if the secondary does not take up a full layer, try bifilar winding (parallel) using wire half the size originally chosen (i.e., 3 wire sizes smaller, like 23 versus 20). This technique ultimately results in the use of foil for the higher current (20 A) low voltage windings. Most windings can be separated with 3 mil mylar (yellow) tape but for good isolation, cloth is recommended between primary and secondary.

Finally, once a mechanical fit has been obtained, it is time for the circuit tests. The isolation voltage rating is strictly a mechanical problem and is one of the reasons why cloth is preferred over tape between the primary and secondary. The inductance and saturating current level of the primary are inherent to the design, and should be checked in the circuit or other suitable test fixture. Such a fixture is shown in Figure 10–7 where the transistor and diode are sized to handle the anticipated currents. The pulse generator is run at a low enough duty cycle to allow the core to reset. Pulse width is increased until the start of saturation is observed (I_{sat}). Inductance is found using $L = E/(di/dt)$.

Figure 10–6. Control Circuit Topologies



(a) Single Chip System — Drive Transformer Isolation



(b) Three Chip System — Opto Coupler Isolation

In forward converters, the transformer generally has no gap in order to minimize the magnetizing current (I_M). For these applications the core should be chosen large enough so that the resulting LI product insures that I_M at operating voltages is less than I_{sat}. For flyback designs, a gap is necessary and the test circuit is useful again to evaluate the effect of the gap. The gap will normally be quite large, Lg > > L_m/u,

where, Lg = gap length
L_m = magnetic path length, and
u = permeability.

Under this stipulation, the gap directly controls the LI parameters and doubling it will decrease L by two and increase I_{sat} by two until fringing effects occur. Gaps of 5 mils to 20 mils are common. Again, the anticipated switching currents must be less than I_{sat} when the core is gapped for the correct inductance.

Table 10–3. Partial List of Core (C) and Transformer (T) Manufacturers

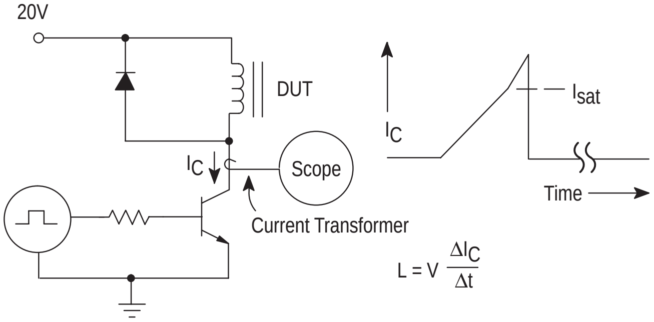
Company	Location	Code
Ferroxcube Inc.	Sauggerties, NY	C
Indiana General	Keasby, NJ	C
Stackpole	St. Marys, PA	C
TDK	El Segundo, CA	C
Pulse Engineering	San Diego, CA	T
Coilcraft	Cary, IL	T

Transformer tests in the actual supply are usually done with a high voltage dc power supply on the primary and with a pulse generator or other manual control for the pulse width (such as using the control IC in the open loop configuration). Here the designer must recheck three areas:

1. Core saturation
2. Correct amount of secondary voltage
3. Transformer heat rise

If problems are detected in any of these areas, the ultimate fix may be to redesign using the next larger core size. However, if problems are minimal, or none exist, it is possible to stay with the same core or even consider using the next smaller size.

Figure 10–7. Simple Coil Tester



Filter Capacitor Considerations

In today’s 20 kHz switchers, aluminum electrolytics still predominate. The good news is that most have been characterized, improved, and cost reduced for this application. The input filter requires a voltage rating that depends on the peak line voltage; i.e., 400 V to 450 V for a 220 V switcher. If voltage is increased beyond this point, the capacitor will begin to act like a zener and be thermally destroyed from high leakage currents if the rating is exceeded for enough time. In doubler circuits, voltage sharing of the two capacitors in series can be a problem. Here extra voltage capability may be needed to make up for the imbalances caused by different values of capacitance and leakage current. A bleeder resistor is normally used here not only for safety but to mask the differences in leakage current. The RMS current rating is also an important consideration for input capacitors and is an example of improvements offered by today’s manufacturers. Earlier “lytics” usually lacked this rating and often overheated. Large capacitors that were not needed for performance were used just to reduce this heating. However, today’s devices offer lower thermal resistance, improved connection to the foil and good RMS ratings. A partial list of manufacturers that supply both high voltage input and the lower voltage output capacitors for switchers is shown in Table 10–4. Most of the companies offer not only the standard 85°C components, but devices with up to 125°C ratings which are required because of the high ambient temperatures (55° to 85°C) that many switchers have to operate in, many times without the benefit of fans.

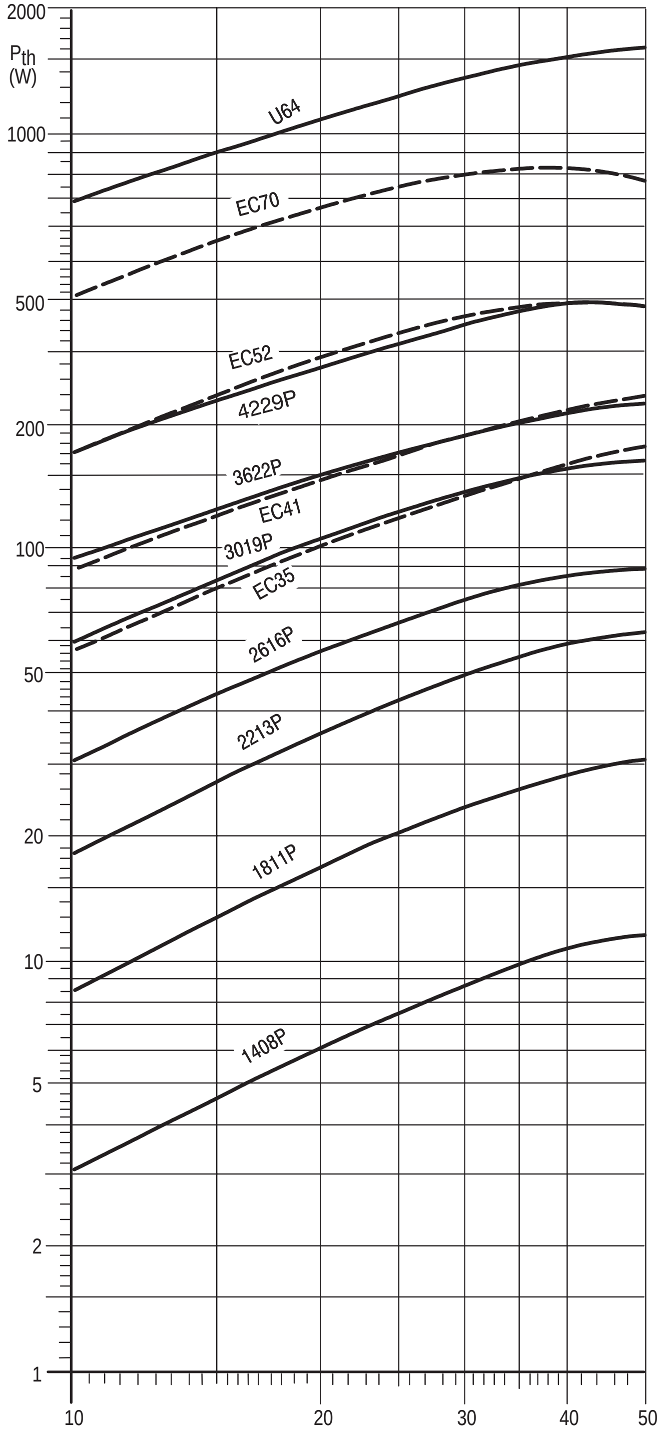
Table 10–4. Partial List of Capacitor Companies

Company (U.S.)	Location
MEPCO/Electra	Columbia, SC
Cornell–Dublier	Sanford, NC
Sangamo	Pickens, SC
Mallory	Indianapolis, IN

For output capacitors the buzz word is low ESR (equivalent series resistance). It turns out that for most capacitors even in the so–called “low ESR” series, the output ripple depends more on this resistance than on the capacitor value itself. Although typical and maximum ESR ratings are now available on most capacitors designed for switchers, the lead inductance generally is not specified except for the ultra–high frequency four terminal capacitors from some vendors. This parameter is responsible for the relatively high switching spikes that appear at the output. However, at this point in time, most designers find it less costly and more effective to add a high frequency noise filter rather than use a relatively expensive capacitor with low equivalent series inductance (ESL).

These LC noise or spike filters are made using small powdered iron toroids (1/2″ to 1″ OD) with distributed windings to minimize interwinding capacitance. And the output is bypassed using a small 0.1 µF ceramic or a 10 µF to 50 µF tantalum or both. Larger powered iron toroids are often used in the main LC output filter although the higher permeability ferrite EC and E cores with relatively large gaps can also be used. Calculations for the size of this component should take into account the minimum load so that the choke will not run “dry” as stated earlier.

Figure 10–8. Core Selection for Bridge Configurations (Reprinted from Ferroxcube Design Manual)



Note: Power handling decreases by a factor of 2 in forward and by 4 in flyback configurations.

SECTION 11

SWITCHING REGULATOR COMPONENT DESIGN TIPS

Transistors

The initial selection of a transistor for a switcher is basically a problem of finding the one with voltage and current capabilities that are compatible with the application. For the final choice performance and cost tradeoffs among devices from the same or several manufacturers have to be weighed. Before these devices can be put in the circuit, both protective and drive circuits will have to be designed.

Motorola's first line of devices for switchers were trademarked “Switchmode” transistors and introduced in the early 70's with data sheets that provided all the information that a designer would need including reverse bias safe operating area (RBSOA) and performance at elevated temperature (100°C). The first series was the 2N6542 through 2N6547, TO–204 (TO–3) and was followed by the MJE13002 through MJE13009 series in a plastic TO–220 package. Finally, high voltage (1.0 kV) requirements were met by the metal MJ8500 thru MJ8505 series and the plastic MJE8500 series. The Switchmode II series is an advanced version of Switchmode I that features faster switching. Switchmode III is a state of the art bipolar with exceptional speed, RBSOA, and up to 1.5 kV blocking capacity. Here, device cost is somewhat higher, but system costs may be lowered because of reduced snubber requirements and higher operating frequencies. A similar argument applies to Motorola TMOS Power FETs. These devices make it possible to switch efficiently at higher frequencies (200 kHz to 500 kHz) but the main selling point is that they are easier to drive. This latter point is the one most often made to show that systems savings are again quite possible even though the initial device cost is higher.

Table 11–1. Motorola High Voltage Switching Transistor Technologies

Family	Typical Device	Typical Fall Time	Approximate Switching Frequency
SWITCHMODE I	2N6545 MJE13005 MJE12007	200 ns to 500 ns	20 k
SWITCHMODE II	MJ13081	100 ns	100 k
SWITCHMODE III	MJ16010	50 ns	200 k
TMOS	MTP5N40	20 ns	500 k

Table 11–2 is a chart of the transistor voltage requirements for the various off–line converter circuits. As illustrated, the most stringent requirement for single transistor circuits (flyback and forward) is the blocking or V_{CEV} rating. Bridge circuits, on the other hand, turn on and off from the dc bus and their most critical voltage is the turn–on or $V_{CEO(sus)}$ rating.

Table 11–2. Power Transistor Voltage Chart

Line Voltage	Circuit			
	Flyback, Forward or Push–Pull		Half or Full–Bridge	
	V_{CEV}	$V_{CEO(sus)}$	$V_{CEO(sus)}$	V_{CEV}
220 120	850 kV to 1.0 kV 450	450 250	450 250	450 250

Most switchmode transistor load lines are inductive during turn–on and turn–off. Turn–on is generally inductive because the short circuit created by output rectifier reverse recovery times is isolated by leakage inductance in the transformer. This inductance effectively snubs most turn–on load lines so that the rectifier recovery (or short circuit) current and the input voltage are not applied simultaneously to the transistor. Sometimes primary interwinding capacitance presents a small current spike but usually turn–on transients are not a problem. Turn–off transients due to this same leakage inductance, however, are almost always a problem. In bridge circuits, clamp diodes can be used to limit these voltage spikes. If the resulting inductive load line exceeds the transistor's reverse bias switching capability (RBSOA) then an RC network may also be added across the primary to absorb some of this transient energy. The time constant of this network should equal the anticipated switching time of the transistor (50 ns to 500 ns). Resistance values of 100 Ω to 1000 Ω in this RC network are generally appropriate. Trial and error will indicate how low the resistor has to be to provide the correct amount of snubbing. For single transistor converters, the circuits shown in Figure 11–1 are generally used.

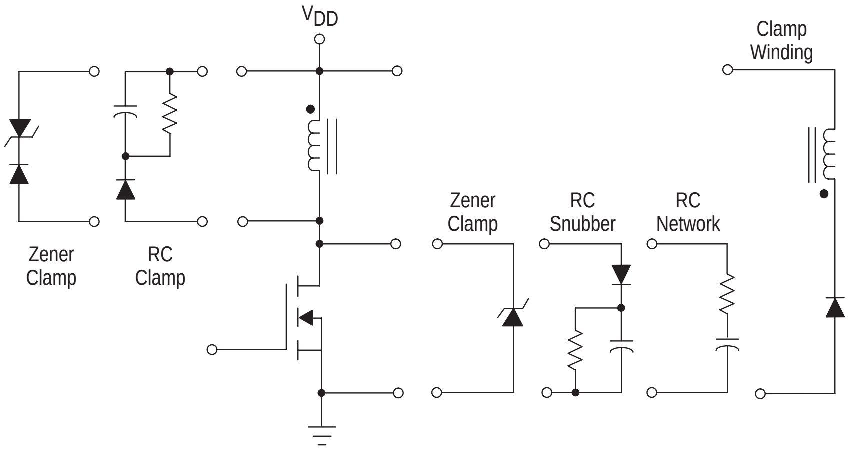
Here slightly different criteria are used to define the R and C snubber values:

$$C = \frac{I\,t_f}{V}$$

where; I = the peak switching current
t_f = the transistor fall time
V = the peak switching voltage (Approximately twice the DC bus)
also, R = t_{on}/C (it is not necessary to completely discharge this capacitor in order to obtain the desired effects of this circuit)
where, t_{on} = the minimum on–time or pulse width
and, $P_R = \dfrac{CV^2f}{2}$
where, P_R = the power rating of the resistor
and, f = the operating frequency.

In most of today's designs snubber elements are small or nonexistent and voltage spikes from energy left in the leakage inductance a more critical problem depending on how good the coupling is between the primary and clamp windings and how fast the clamp diode turns on. FETs often have to be slowed down to prevent self destruction from this spike.

Figure 11–1. Protection Circuits for Switching Transistors



Zener and Mosorb Transient Suppressors

If necessary, protection from voltage spikes may be obtained by adding a zener and rectifier across the primary as shown in Figure 11–1. Here Motorola's 5.0 W zener lines with ratings up to 200 V, and 10 W TO–220 Mosorbs with ratings up to 250 V can provide the clamping or spike limiting function. If the zener must handle most of the power, its size can be estimated using:

$$PZ = \frac{L_L I^2 f}{2}$$

where, P_Z = the zener power rating
and, L_L = the leakage inductance (measured with the clamp winding or secondary shorted)
I = peak collector current
f = operating frequency

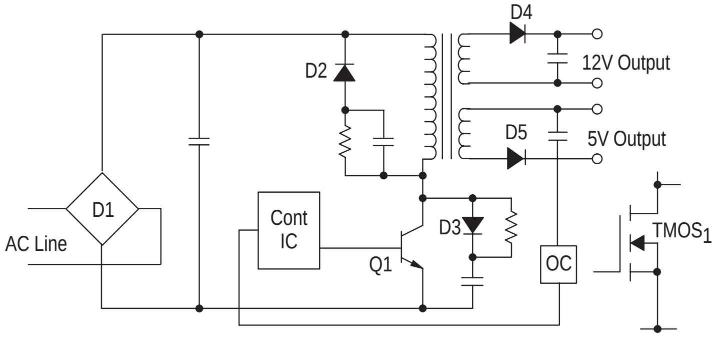
Distinction is sometimes made between devices trademarked Mosorb (by Motorola, Inc.), and standard zener/avalanche diodes used for reference, low–level regulation and low–level protection purposes. It must be emphasized that Mosorb devices are, in fact, zener diodes. The basic semiconductor technology and processing are identical. The primary difference is in the applications for which they are designed. Mosorb devices are intended specifically for transient protection purposes and are designed, therefore, with a large effective junction area that provides high pulse power capability while minimizing the total silicon use. Thus, Mosorb pulse power ratings begin at 600 W — well in excess of low power conventional zener diodes which in many cases do not even include pulse power ratings among their specifications.

MOVs, like Mosorbs, do have the pulse power capabilities for transient suppression. They are metal oxide varistors (not semiconductors) that exhibit bidirectional avalanche characteristics, similar to those of back–to–back connected zeners. The main attributes of such devices are low manufacturing cost, the ability to absorb high energy surges (up to 600 joules) and symmetrical bidirectional "breakdown" characteristics. Major disadvantages are: high clamping factor, an internal wear–out mechanism and an absence of low–end voltage capability. These limitations restrict the use of MOVs primarily to the protection of insensitive electronic components against high energy transients in applications above 20 V, whereas, Mosorbs are best suited for precise protection of sensitive equipment even in the low voltage range the same range covered by conventional zener diodes.

Rectifiers

Once components for the inverter section of a switcher have been chosen, it is time to determine how to get power into and out of this section. This is where the all–important rectifier comes into play. (See Figure 11–2.) The input rectifier is generally a standard recovery bridge that operates off the ac line and into a capacitive filter. For the output section, most designers use Schottkys for efficient rectification of the low voltage, 5.0 V output windings and for the higher voltage, 12 V to 15 V outputs, the more economical fast recovery or ultrafast diodes are used.

Figure 11–2. Switchmode Power Supply Flyback or Boost Design



D1 — Bridge Rectifier — Line Voltage
D2 — Clamp Diode — HV/Fast–Ultrafast
D3 — Snubber Diode — HV/Fast–Ultrafast
D4 — Output Rectifier — Fast/Ultrafast
D5 — Output Rectifier — Schottky

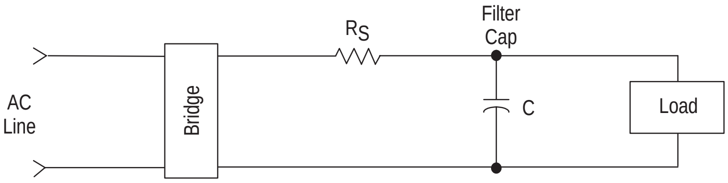
For the process of choosing an input rectifier, it is useful to visualize the circuit shown in Figure 11–3. To reduce cost, most earlier approaches of using choke input filters, soft start relays (Triacs), or SCRs to bypass a large limiting resistor have been abandoned in favor of using small limiting resistors or thermistors and a large bridge. The bridge must be able to withstand the surge currents that exist from repetitive starts at peak line. The procedure for finding the right component and checking its fit is as follows:

1. Choose a rectifier with 2 to 5 times the average I_O required.
2. Estimate the peak surge current (I_P) and time (t) using:

$$I_P = \frac{1.4\ V_{in}}{R_S} \qquad t = R_S C$$

Where V_{in} is the RMS input voltage; R_S is the total series resistance; and C is the filter capacitor size.

Figure 11–3. Choosing Input Rectifiers



3. Compare this current pulse to the sub cycle surge current rating (I_S) of the diode itself. If the curve of I_S versus time is not given on the data sheet, the approximate value for I_S at a particular pulse width (t) may be calculated knowing:
   - I_{FSM} — the single cycle (8.3 ms) surge current rating and using.
   - $I^2 \sqrt{t} = K$, which applies when the diode temperature rise is controlled by its thermal response as well as power (i.e., $T = K'P \sqrt{t}$ for t < 8.0 ms).

   This gives:

$$I_S{}^2 \sqrt{t} = I^2{}_{FSM} \sqrt{8.3\ ms} \quad \text{or,} \quad I_S = I_{FSM} \left(\frac{8.3\ ms}{t}\right)^{1/4} \text{, t is in milliseconds.}$$

4. If $I_S < I_P$, consider either increasing the limiting resistor (R_S) or utilizing a larger diode.

In the output section where high frequency rectifiers are needed, there are several types available to the designer. In addition to the Schottky (SBR) and fast recovery (FR), there is also an ultrafast recovery (UFR). Comparative performance for devices with similar current ratings is shown in Table 11–3. The obvious point here is that lower forward voltage improves efficiency and lower recovery times reduce turn–on losses in the switching transistors, but the tradeoff is higher cost. As stated earlier, Schottkys are generally used for 5.0 V outputs and fast recovery and ultrafast devices for 12 V outputs and greater. The ultrafast is competing both with the Schottky where higher breakdown is needed and with the fast recovery in those applications where performance is more important than cost. Ten years ago Schottkys were very fragile and could fail short from either excessive dv/dt (1.0 V to 5.0 V per nanosecond) or reverse avalanche. Since that time, Motorola has incorporated a “guard ring” or internal zener which minimizes these earlier problems and reduces the need for RC snubbers and other external protective networks.

Table 11–3. Motorola Rectifier Product Portfolio

Parameter	Schottky	Ultrafast	Fast Recovery	Standard Recovery
Forward Voltage (V_F)	0.5 V to 0.6 V	0.9 V to 1.0 V	1.2 V to 1.4 V	1.2 V to 1.4 V
Reverse Recovery Time (t_{rr})	<10 ns	25 ns to 100 ns	150 ns	1.0 μs
t_{rr} Form	Soft	Soft	Soft	Soft
DC Blocking Voltage (V_R)	20 V to 60 V	50 V to 1000 V	50 V to 1000 V	50 V to 1000 V
Cost Ratio	3:1	3:1	2:1	1:1

SECTION 12

BASIC SWITCHING POWER SUPPLY CONFIGURATIONS

The implementation of switching power supplies by the non–specialist is becoming increasingly easy due to the availability of power devices and control ICs especially developed for this purpose by the semiconductor manufacturer.

This section is meant to help in the preliminary selection of the devices required for the implementation of the listed switching power supplies.

Flyback and Forward Converter Switching Power Supplies (50 W to 250 W)

- Input line variation: V_{in} + 10%, – 20%
- Converter efficiency: $\eta = 80\%$
- Output regulation by duty cycle (δ variation: $\delta_{(max)} = 0.4$)
- Maximum Transistor working current:

$$I_W = \frac{2.0\ P_{out}}{\eta \times \delta_{(max)} \times V_{in(min)} \times \sqrt{2}} = \frac{5.5\ P_{out}}{V_{in}} \quad \text{(Flyback)}$$

$$= \frac{P_{out}}{\eta \times \delta_{(max)} \times V_{in(min)} \times \sqrt{2}} = \frac{2.25\ P_{out}}{V_{in}} \quad \text{(Forward)}$$

- Maximum transistor working voltage: $V_W = 2 \times V_{in(max)} \times \sqrt{2}$ + guardband
- Working frequency: f = 20 kHz to 200 kHz

Basic Flyback Configuration

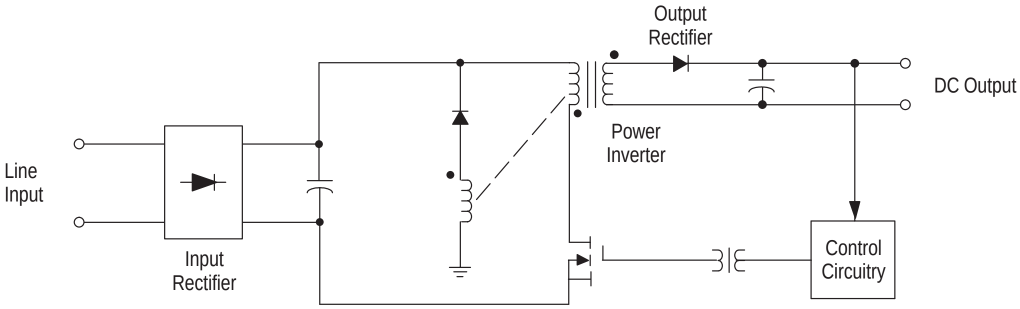


Table 12–1. Flyback and Forward Converter Semiconductor Selection Chart

Output Power	50 W		100 W		175 W		250 W
Input Line Voltage (V_{in})	120 V	220 V 240 V	120 V	220 V 240 V	120 V	220 V 240 V	120 V
MOSFET Requirements:							
Max Working Current (I_W)	2.25 A	1.2 A	4.0 A	2.5 A	8.0 A	4.4 A	11.4 A
Max Working Voltage (V_W)	380 V	750 V	380 V	750 V	380 V	750 V	380 V
Power MOSFETs Recommended:							
Metal (TO–204AA) (TO–3)	MTM4N45	MTM2N90	MTM4N45	MTM2N90	MTM7N45	MTM4N90	MTM15N45
Plastic (TO–220AB)	MTP4N45	MTP2N90	MTP4N45	MTP2N90	—	—	—
Plastic (TO–218AC)	—	—	—	—	MTH7N45	—	—
Input Rectifiers:							
Max Working Current (I_W)	0.4 A	0.25 A	0.4 A	0.5 A	2.35 A	1.25 A	4.6 A
Recommended Types	MDA104A	MDA106A	MDA206	MDA210	MDA970	MDA210	MDA3506
Output Rectifiers: Recommended types for							
Output Voltage of: 5.0 V	MBR3035PT		MBR3035PT		MBR12035CT		MBR20035CT
10 V	MUR3010PT		MUR3010PT		MUR10010CT		MUR10010CT
20 V	MUR1615CT		MUR1615CT		MUR3015PT		MUR10015CT
50 V	MUR1615CT		MUR1615CT		MUR1615CT		MUR3015PT
100 V	MUR 440, MUR840A		MUR840A		MUR840A		MUR840A
Recommended Control Circuits	SG1525A, SG1526, TL494 Inverter Control Circuit MC3423 Overvoltage Detector Error Amplifier: Single TL431; Dual–LM358 Quad MC3403, LM324, LM2902						

Flyback and Forward Converters

To take advantage of the regulating techniques discussed earlier and also provide isolation, a total of seven popular configurations have evolved and are listed below. Each circuit has a practical power range or capability associated with it as follows:

Circuit	Power Range	Parts Cost
DC Converter	5.0 W	$ 4.00
Converter w/30 V Transformer	10 W	7.00
Blocking OSC	20 W	10.00
Flyback	50 W	15.00
Forward	100 W	20.00
Half–Bridge	200 W	30.00
Full–Bridge	500 W	75.00

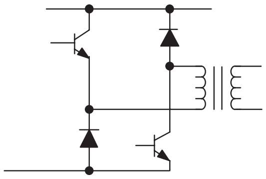
First to be discussed will be the low power (20 W to 200 W) converters which are dominated by the single transistor circuits shown in Figure 12–1. All of these circuits operate the magnetic element in the unipolar rather than bipolar mode. This means that transformer size is sacrificed for circuit simplicity.

The flyback (alternately known as the “ringing choke”) regulator stores energy in the primary winding and dumps it into the secondary windings, see Figure 12–1(a). A clamp winding is usually present to allow energy stored in the leakage reactance to return safely to the line instead of avalanching the switching transistor. The operating model for this circuit is the buck–boost discussed earlier. The flyback is the lowest cost regulator because output filter chokes are not required since the output capacitors feed from a current source rather than a voltage source. It does have higher output ripple than the forward converters because of this. However, it is an excellent choice when multiple output voltages are required and does tend to provide better cross regulation than the other types. In other words changing the load on one winding will have little effect on the output voltage of the others.

Figure 12–1. Low Power Popular (20 to 200 W) Converter Configurations

(a) Flyback (Clamp Winding is Optional)

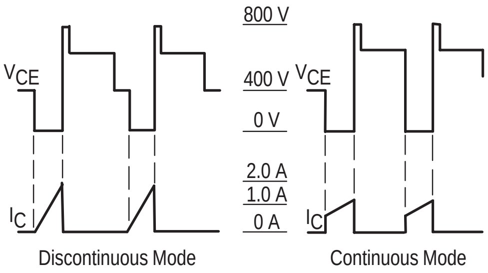
(b) Forward (Clamp Winding is Necessary)



(c) Two Transistor Forward or Flyback
(Clamp Winding is not Needed)

A 120/220 Vac flyback design requires transistors that block twice the peak line plus transients or about 1.0 kV. Motorola’s MJE13000 and 16000A series with ratings of 750 V to 1000 V are normally used here. These bipolar devices are relatively fast (100 ns) and are typically used in the 20 kHz to 50 kHz operating frequency range. The recent availability of 900 V and 1000 V TMOS FETs allows designers to operate in the next higher range (50 kHz to 80 kHz) and some have even gone as high as 300 kHz with square wave designs and FETs. Faster 1.0 kV bipolar transistors are also planned in the future and will provide another design alternative. The two transistor variations of this circuit, Figure 12–1(c), eliminate the clamp winding and add a transistor and diode to effectively clamp peak transistor voltages to the line. With this circuit a designer can use the faster 400 V to 500 V FET transistors and push operating frequencies considerably higher. There is a cost penalty here over the single transistor circuit due to the extra transistor, diodes and gate drive circuitry.

Figure 12–2. Flyback Transistor Waveforms

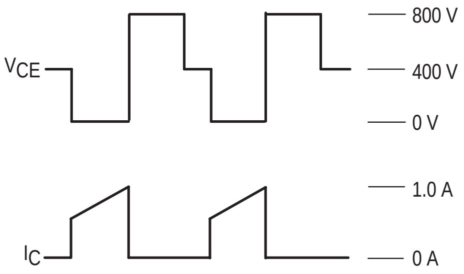


A subtle variation in the method of operation can be applied to the flyback regulator. The difference is referred to as operation in the discontinuous or continuous mode and the waveform diagrams are shown in Figure 12–2. The analysis given in the earlier section on boost regulators dealt strictly with the discontinuous mode where all the energy is dumped from the choke before the transistor turns on again. If the transistor is turned on while energy is still being dumped into the load, the circuit is operating in the continuous mode. This is generally an advantage for the transistor in that it needs to switch only half as much peak current in order to deliver the same power to the load. In many instances, the same transformer transformer may be used with only the gap reduced to provide more inductance. Sometimes the core size will need to be increased to support the higher LI product (2 to 4 times) now required because the inductance must increase by almost 10 times to effectively reduce the peak current by two. In dealing with the continuous mode, it should also be noted that the transistor must now turn on from 500 V to 600 V rather than 400 V level because there no longer is any deadtime to allow the flyback voltage to settle back down in the input voltage level. Generally, it is advisable to have $V_{CEO(sus)}$ ratings comparable to the turn–on requirements except for SMIII where turn–on up to V_{CEV} is permitted.

The flyback converter stands out from the others in its need for a low inductance, high current primary. Conventional E and pot core ferrites are difficult to work with because their permeability is too high even with relatively large gaps (50 to 100 milli–inches). The industry needs something better that will provide permeabilities of 60 to 120 instead of 2000 to 3000 for this application.

The single transistor forward converter is shown in Figure 12–1(b). Although it initially appears very similar to the flyback, it is not. The operating model for this circuit is actually the buck regulator discussed earlier. Instead of storing energy in the transformer and then delivering it to the load, this circuit uses the transformer in the active or forward mode and delivers power to the load while the transistor is on. The additional output rectifier is used as a freewheeling diode for the LC filter and the third winding is actually a reset winding. It generally has the same turns as the primary, (is usually bifilar wound) and does clamp the reset voltage to twice the line. However, its main function is to return energy stored in the magnetizing inductance to the line and thereby reset the core after each cycle of operation. Because it takes the same time to set and reset the core, the duty cycle of this circuit cannot exceed 50%. This also is a very popular low power converter and like the flyback is practically immune from transformer saturation problems. Transistor waveforms shown in Figure 12–3 illustrate that the voltage requirements are identical to the flyback. For the single transistor versions, 400 V turn–on and 1.0 kV blocking devices like the MJE13000 and MJE16000 transistors are required. The two transistor circuit variations shown in Figure 12–1(b) again adds a cost penalty but allows a designer to use the faster 400 V to 500 V devices. With this circuit, operation in the discontinuous mode refers to the time when the load is reduced to a point where the filter choke runs “dry.” This means that choke current starts at and returns to zero during each cycle of operation. Most designers prefer to avoid this type of mode because of higher ripple and noise even though there are no adverse effects on the components themselves. Standard ferrite cores work fine here and in the high power converters as well. In these applications, no gap is used as the high permeability (3000) results in the desirable effect of very low magnetizing current levels. And, zeners or RC clamps may be used to reset the core in lieu of the clamp winding to lower the voltage stress on the switching transistors.

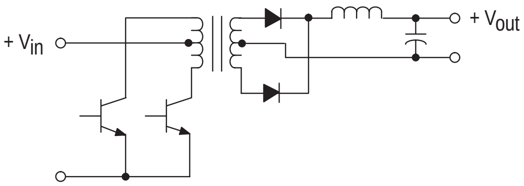
Figure 12–3. Forward Converter Transistor Waveforms



Push–Pull and Bridge Converters

The high power circuits shown in Figures 12–4 to 12–7 all operate the magnetic element in the bipolar or push–pull mode and require 2 to 4 inverter transistors. Because the transformers operate in this mode they tend to be almost half the size of the equivalent single transistor converters and thereby provide a cost advantage over their counterparts at power levels of 200 kW to 1.0 kW.

Figure 12–4. Push–Pull Converter (200 W to 1.0 kW)



The push–pull converter shown in Figure 12–4 is one of the oldest converter circuits around. Its early use was in low voltage inverters such as the 12 Vdc to 120 Vdc power source for recreational vehicles and in dc to dc converters. Because these converters are free running rather than driven and operate from low voltages, transformer saturation problems are minimal. In the high voltage off–line switchers, saturation problems are common and were difficult to solve. The transistors are also subjected to twice the peak line voltage which requires the use of high voltage (1.0 kV) transistors. Both of these drawbacks have tended to discourage designers of off–line switchers from using this configuration until current mode control ICs were introduced. Now these circuits are being looked at with renewed interest.

Push–Pull Switching Power Supplies (100 W to 500 W)

- Input line variation: V_{in} + 10%, – 20%
- Converter efficiency: η = 80%
- Output regulation by duty cycle (δ) variation: $\delta_{(max)} = 0.8$
- Maximum transistor working current:

$$I_W = \frac{P_{out}}{\eta \times \delta_{(max)} \times V_{in(min)} \times \sqrt{2}} = \frac{1.4\ P_{out}}{V_{in}}$$

- Maximum transistor working voltage: $V_W = 2 \times V_{in(max)} \times \sqrt{2}$ + guardband
- Working frequency: f = 20 kHz to 200 kHz

Basic Push–Pull Configuration

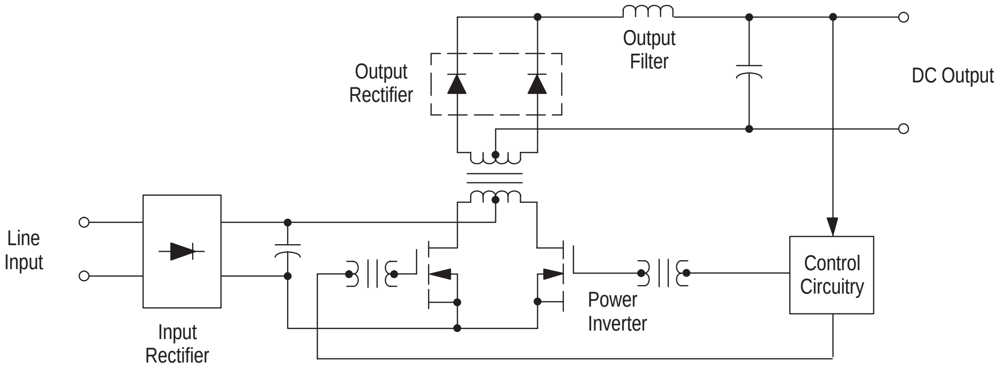


Table 12–2. Push–Pull Semiconductor Selection Chart

Output Power	100 W		250 W		500 W	
Input Line Voltage (V_{in})	120 V	220 V 240 V	120 V	220 V 240 V	120 V	220 V 240 V
MOSFET Requirements: Max Working Current (I_W) Max Working Voltage (V_W)	1.2 A 380 V	0.6 A 750 A	2.9 A 380 V	1.6 A 750 V	5.7 A 380 V	3.1 A 750 V
Power MOSFETs Recommended: Metal (TO–204AA) (TO–3) Plastic (TO–220AB) Plastic (TO–218AC)	MTM2N50 MTP2N45 —	MTM2N90 MTP2N90 —	MTM4N45 MTP4N45 —	MTM2N90 MTP2N94 —	MTM7N45 — MTH7N45	MTM4N90 — —
Input Rectifiers: Max Working Current (I_W) Recommended Types	0.9 A MDA206	0.5 A MDA210	2.35 A MDA970–5	1.25 A MDA210	4.6 A MDA3506	2.5 A MDA3510
Output Rectifiers: Recommended types for output voltages of: 5.0 V 10 V 20 V 50 V 100 V	MBR3035PT MBR3045PT, MUR3010PT MUR1615CT MUR1615CT MUR840A, MUR440		MBR12035CT MUR10010CT MUR3015PT MUR1615CT MUR840A		MBR20035CT MUR10010CT MUR10015CT MUR3015PT MUR840A	
Recommended Control Circuits	SG1525A, SG1526, TL494 Inverter Control Circuit MC3423 Overvoltage Detector Error Amplifier: Single TL431; Dual–LM358 Quad MC3403, LM324, LM2902					

Half–Bridge/Full–Bridge Switching Power Supplies (100 W to 500 W/500 W to 1000 W)

- Input line variation: V_{in} + 10%, – 20%
- Converter efficiency: $\eta = 80\%$
- Output regulation by duty cycle (δ) variation: $\delta_{(max)} = 0.8$
- Maximum working current:

$$I_W = \frac{2\,P_{out}}{\eta \times \delta_{(max)} \times V_{in(min)} \times \sqrt{2}} = \frac{2.8\,P_{out}}{V_{in}} \quad \text{(Half–Bridge)}$$

$$= \frac{P_{out}}{\eta \times \delta_{(max)} \times V_{in(min)} \times \sqrt{2}} = \frac{1.4\,P_{out}}{V_{in}} \quad \text{(Full–Bridge)}$$

- Maximum transistor working voltage: $V_W = V_{in(max)} \times \sqrt{2}$ + guardband
- Working frequency: f = 20 kHz to 200 kHz

Basic Half–Bridge Configuration

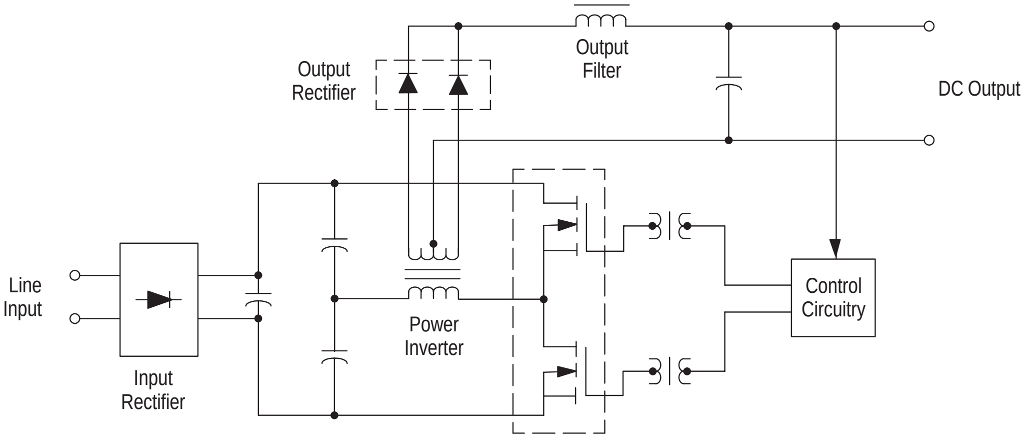


Table 12–3. Half–Bridge Semiconductor Selection Chart

Output Power	100 W		350 W		500 W	
Input Voltage (V_{in})	120 V	220 V 240 V	120 V	220 V 240 V	120 V	220 V 240 V
MOSFET Requirements: Max Working Current (I_W) Max Working Voltage (V_W)	 2.3 A 190 V	 1.25 A 380 V	 5.7 A 190 V	 3.1 A 380 V	 11.5 A 190 V	 6.25 A 380 V
Power MOSFETs Recommended: Metal (TO–204AA) (TO–3) Plastic (TO–220AB) Plastic (TO–218AC)	 MTM5N35 MTP3N40 —	 MTM2N45 MTP2N45 —	 MTM8N40 — MTH8N40	 MTM4N45 MTP4N45 —	 MTM10N25 MTP10N25 —	 MTM7N45 — MTH7N45
Input Rectifiers: Max Working Current (I_W) Recommended Types	 0.9 A MDA206	 0.5 A MDA210	 2.3 A MDA970–5	 1.25 A MDA210	 4.6 A MDA3506	 2.5 A MDA3510
Output Rectifiers: Recommended types for output voltage of: 5.0 V 10 V 20 V 50 V 100 V	 MBR3035PT MBR3045PT, MUR3010PT MUR1615CT MUR1615CT MUR840A, MUR440		 MBR12035CT MUR10010CT MUR3015PT MUR1615CT MUR840A		 MBR20035CT MUR10010CT MUR10015CT MUR3015PT MUR840A	
Recommended Control Circuits	SG1525A, SG1526, TL494 Inverter Control Circuit MC3423 Overvoltage Detector Error Amplifier: Single TL431; Dual–LM358 Quad MC3403, LM324, LM2902					

Half and Full–Bridge

The most popular high power converter is the half–bridge (Figure 12–6). It has two clear advantages over the push–pull and became the favorite rather quickly. First, the transistors never see more than the peak line voltage and the standard 400 V fast switchmode transistors that are readily available may be used. And second, and probably even more important, transformer saturation problems are easily minimized by use of a small coupling capacitor (about 2.0 µF to 5.0 µF) as shown above. Because the primary winding is driven in both directions, a full–wave output filter, rather than half, is now used and the core is actually utilized more effectively. Another more subtle advantage of this circuit is that the input filter capacitors are placed in series across the rectified 220 V line which allows them to be used as the voltage doubler elements on a 120 V line. This still allows the inverter transformer to operate from a nominal 320 V bus when the circuit is connected to either 120 V or 220 V. Finally, this topology allows diode clamps across each transistor to contain destructive switching transients. The designer's dream, of course, is for fast transistors that can handle a clamped inductive load line at rated current. And a few (like the MJE16000 series from Motorola) are beginning to appear on the market. With the improved RBSOA that these transistors feature, less snubbing is required and this improves both the cost and efficiency of these designs.

Figure 12–5. Half–Bridge Converter with Split Windings

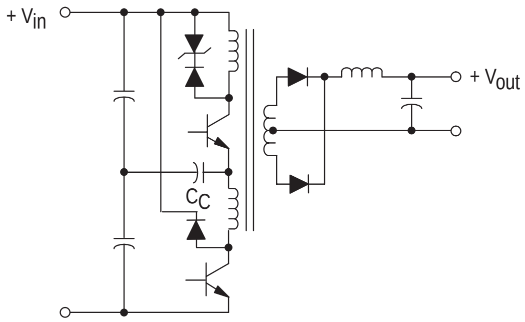
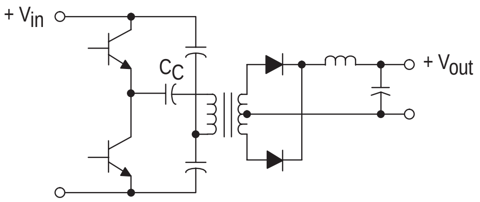


Figure 12–6. Half–Bridge Converter (200 W to 1.0 kW)



Basic Full–Bridge Configuration

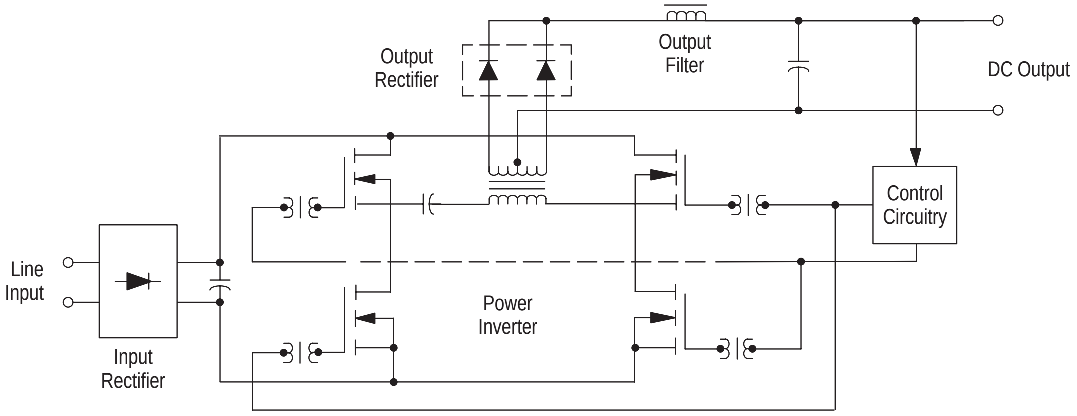


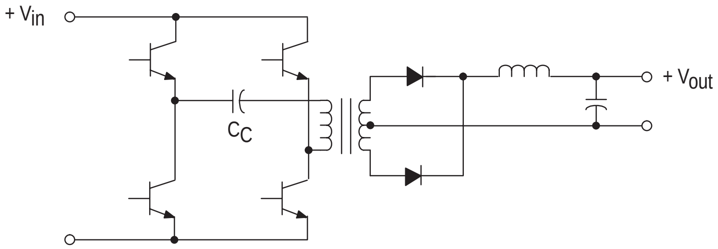
Table 12–4. Full–Bridge Semiconductor Selection Chart

Output Power	500 W		750 W		1000 W	
Input Voltage (V_{in})	120 V	220 V 240 V	120 V	220 V 240 V	120 V	220 V 240 V
MOSFET Requirements: Max Working Curren (I_W) Max Working Voltage (V_W)	 5.7 A 190 V	 3.1 A 380 V	 8.6 A 190 V	 4.7 A 380 V	 11.5 A 190 V	 6.25 A 380 V
Power MOSFETs Recommended: Metal (TO–204AA) (TO–3) Plastic (TO–220AB) Plastic (TO–218AC)	 MTM8N20 MTP8N20 —	 MTM4N45 MTP4N45 —	 MTM10N25 MTP10N25 —	 MTM7N45 MTP4N45 MTH7N45	 MTM15N20 MTP12N20 MTH15N20	 MTM7N45 — MTH7N45
Input Rectifiers: Max Working Current (I_W) Recommended Types	 4.6 A MDA3506	 2.5 A MDA3510	 7.0 A	 3.8 A	 9.25 A	 5.0 A
Output Rectifiers: Recommended types for output voltage of: 5.0 V 10 V 20 V 50 V 100 V	 MBR20035CT MUR10010CT MUR10015CT MUR3015PT MUR804PT		 MBR30035CT MUR10010CT* MUR10015CT MUR3015PT* MUR3040PT		 MBR30035CT* MUR10010CT* MUR10015CT* MUR10015CT MUR3040PT	
Recommended Control Circuits	SG1525A, SG1526, TL494 Inverter Control Circuit MC3423 Overvoltage Detector Error Amplifier: Single TL431; Dual–LM358 Quad MC3403, LM324, LM2902					

*More than one device per leg, matched.

The effective current limit of today's low cost TO–218 discrete transistors (250 mil die) is somewhere in the 10 A to 20 A area. Once this limit is reached, the designer generally changes to the full–bridge configurations shown in Figure 12–7. Because full line rather than half is applied to the primary winding, the power out can be almost double that of the half–bridge with the same switching transistors. Power Darlington transistors are a logical choice for higher power control with current, voltage and speed capabilities allowing very high performance and cost effective designs. Another variation of the half–bridge is the split winding circuit, shown in Figure 12–5. A diode clamp can protect the lower transistor but a snubber or zener clamp must still be used to protect the top transistor from switching transients. Because both emitters are at an ac ground point, expensive drive transformers can now be replaced by lower cost capacitively–coupled drive circuits.

Figure 12–7. Full–Bridge Converter (200 W to 1.0 kW)



SECTION 13

SWITCHING REGULATOR DESIGN EXAMPLES

In addition to the application materials in this data book, Motorola publishes several application notes which contain basic information on the design of power supplies using a variety of Motorola Analog ICs. AN920 describes in detail the principles of operation of the MC34063A and µA78S40 Switching Regulator Subsystems. Several converter design examples and numerous applications circuits with test data are included in this application note. The circuit techniques described in this note are also applicable to the MC34163 and MC34165 Power Switching Regulators.

Operating details of the MC34129 Current Mode Switching Regulator Controller, and examples of its use with Motorola SENSEFET™ products, are provided in AN976. The application note AN983 focuses on a 400 W half-bridge power supply design which uses the TL494 PWM control circuit. The TL594 can be used in this same application.

Essentially all of the data sheets for newer power supply control and supervisory circuits include extensive applications information with test conditions and performance results. Many data sheets also include printed circuit board layouts for some key applications so that the designer can evaluate the integrated circuits in an actual power supply. This data book presents all data sheets in their entirety so that the applications information is readily available for each device.

SECTION 14

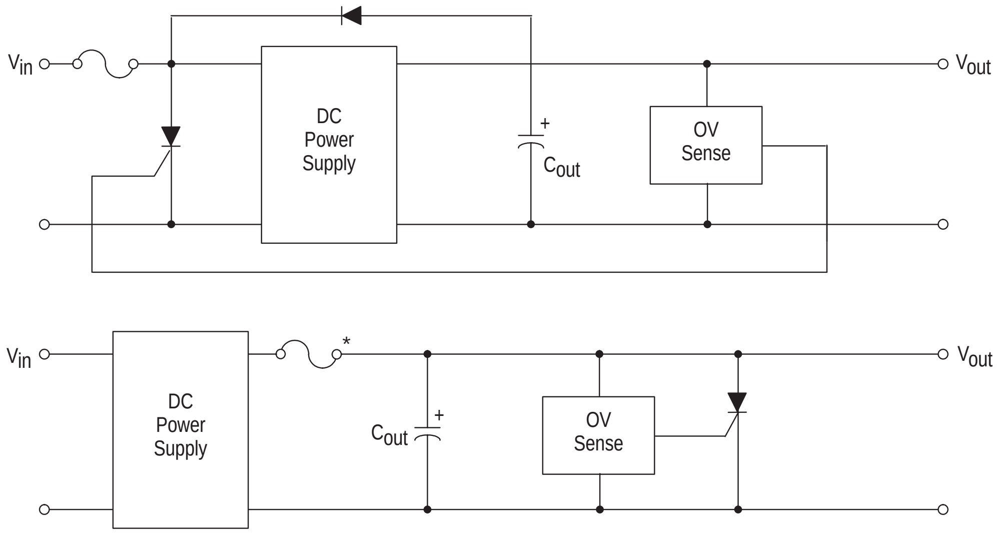
POWER SUPPLY SUPERVISORY AND PROTECTION CONSIDERATIONS

The use of SCR crowbar overvoltage protection (OVP) circuits has been, for many years, a popular method of providing protection from accidental overvoltage stress for the load. In light of the recent advances in LSI circuitry, this technique has taken on added importance. It is not uncommon to have several hundred dollars worth of electronics supplied from a single low voltage supply. If this supply were to fail due to component failure or other accidental shorting of higher voltage supply busses to the low voltage bus, several hundred dollars worth of circuitry could literally go up in smoke. The small additional investment in protection circuitry can easily be justified in such applications.

A. The Crowbar Technique

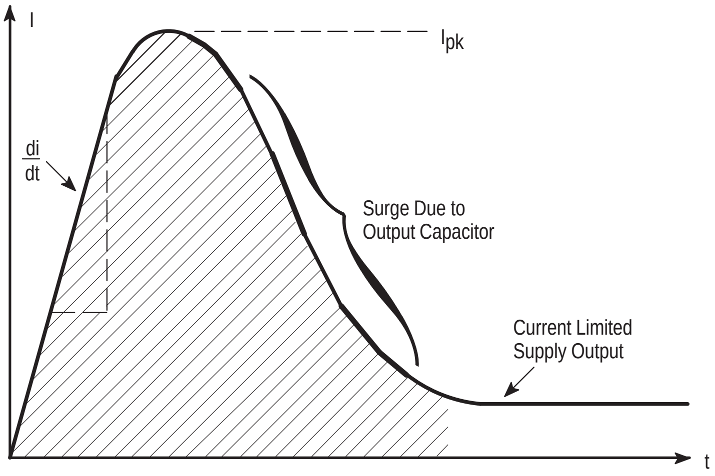
One of the simplest and most effective methods of obtaining overvoltage protection is to use a “crowbar” SCR placed across the equipment’s dc power supply bus. As the name implies, the SCR is used much like a crowbar would be, to short the dc supply when an overvoltage condition is detected. Typical circuit configurations for this circuit are shown on Figure 14–1. This method is very effective in eliminating the destructive overvoltage condition. However, the effectiveness is lost if the OVP circuitry is not reliable.

Figure 14–1. Typical Crowbar OVP Circuit Configurations



*Needed if supply not current–limited.

Figure 14–2. Crowbar SCR Surge Current Waveform



B. SCR Considerations

Referring to Figure 14–1, it can easily be seen that, when activated, the crowbar SCR is subjected to a large current surge from the filter and output capacitors. This large current surge, illustrated in Figure 14–2, can cause SCR failure or degradation by any one of three mechanisms: di/dt, peak surge current, or I2 t. In many instances the designer must empirically determine the SCR and circuit elements which will result in reliable and effective OVP operation. To aid in the selection of devices for this application, Motorola has characterized several devices specifically for crowbar applications. A summary of these specifications and a selection guide for this application is shown in Table 14–1. This significantly reduces the amount of empirical testing that must be done by the designer. A good understanding of the factors that influence the SCR's di/dt and surge current capability will greatly simplify the total circuit design task.

Table 14–1. Crowbar SCRs

Device Type**	Peak Discharge Current*	di/dt*
MCR67	300 A	75 A/µs
MCR68	300 A	75 A/µs
MCR69	750 A	100 A/µs
MCR70	850 A	100 A/µs
MCR71	1700 A	200 A/µs

* tw = 1.0 µs, exponentially decaying

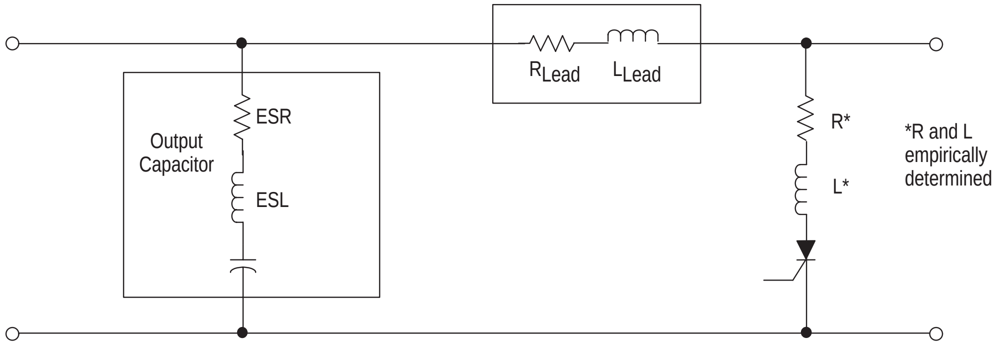
** All devices available with 25, 50, and 100 V ratings

1. di/dt — As the gate region of the SCR is driven on, its area of conduction takes a finite amount of time to grow, starting as a very small region and gradually spreading. Since the anode current flows through this turned–on gate region, very high current densities can occur in the gate region if high anode currents appear quickly (di/dt). This can result in immediate destruction of the SCR or gradual degradation of its forward blocking voltage capabilities, depending upon the severity of the occasion.

The value of di/dt that an SCR can safely handle is influenced by its construction and the characteristics of the gate drive signal. A center–gate–fire SCR has more di/dt capability than a corner–gate–fire type, and heavily overdriving (3 to 5 times I_{GT}) the SCR gate with a fast <1.0 µs rise time signal will maximize its di/dt capability. A typical maximum di/dt in phase control SCRs of less than 50 A rms rating might be 200 A/µs, assuming a gate current of five times IGT and <1.0 µs rise time. If having done this, a di/dt problem still exists, the designer can also decrease the di/dt of the current saveform by adding inductance in series with the SCR, as shown in Figure 14–3. Of course, this reduces the circuit's ability to rapidly reduce the dc bus voltage, and a tradeoff must be made between speedy voltage reduction and di/dt.

2. Surge Current — If the peak current and/or the duration of the surge is excessive, immediate destruction due to device overheating will result. The surge capability of the SCR is directly proportional to its die area. If the surge current cannot be reduced (by adding series resistance, see Figure 14–3) to a safe level which is consistent with the system's requirements for speedy bus voltage reduction, the designer must use a higher current SCR. This may result in the average current capability of the SCR exceeding the steady state current requirements imposed by the dc power supply.

Figure 14–3. Circuit Elements Affecting SCR Surge & di/dt



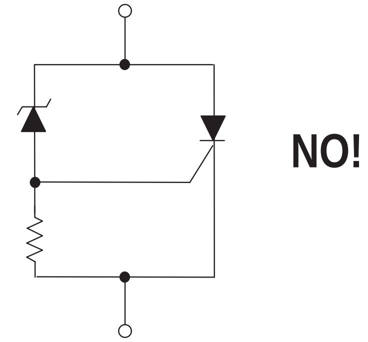
(For additional information on SCRs in crowbar applications refer to *Characterizing the SCR for Crowbar Applications*, Al Pshaenich, Motorola AN789).

C. The Sense and Drive Circuit

In order to maximize the crowbar SCR's di/dt capability, it should receive a fast rise time high–amplitude gate–drive signal. This must be one of the primary factors considered when selecting the sensing and drive circuitry. Also important is the sense circuitry's noise immunity.

Noise immunity can be a major factor in the selection of the sense circuitry employed. If the sensing circuit has low immunity and is operated in a noisy environment, nuisance tripping of the OVP circuit can occur on short localized noise spikes, which would not normally damage the load. This results in excessive system down time. There are several types of sense circuits presently being used in OVP applications. These can be classified into three types: zener, discrete, and “723.”

Figure 14–4. The Zener Sense Circuit



1. The Zener Sense Circuit — Figure 14–4 shows the use of a zener to trigger the crowbar SCR. This method is NOT recommended since it provides very poor gate drive and greatly decreases the SCR's di/dt handling capability, especially since the SCR steals its own very necessary gate drive as it turns on. Additionally, this method does not allow the trip point to be adjusted except by zener replacement.

2. The Discrete Sense Circuit — A technique which can provide adequate gate drive and an adjustable, low temperature coefficient trip point is shown in Figure 14–5. While overcoming the disadvantages of the zener sense circuit, this technique requires many components and is more costly. In addition, this method is not particularly noise immune and often suffers from nuisance tripping.

3. The “723” Sense Circuit — By using an integrated circuit voltage regulator, such as the industry standard “723” type, a considerable reduction in component count can be achieved. This is illustrated in Figure 14–6. Unfortunately, this technique is not noise immune, and suffers an additional disadvantage in that it must be operated at voltages above 9.5 V.

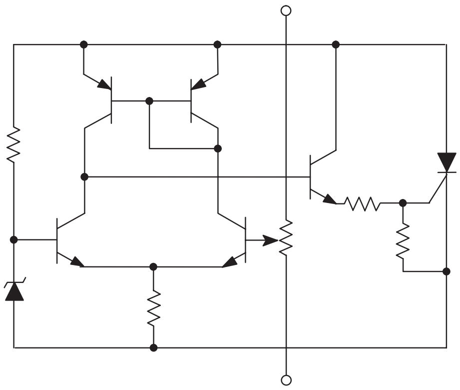


Figure 14–5. The Discrete Sense Circuit

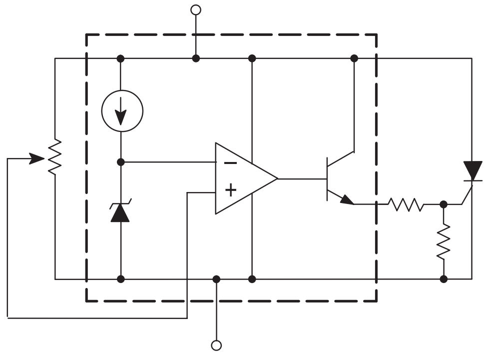


Figure 14–6. The “723” Sense Circuit

4. The MC3423 — To fill the need for a low cost, low complexity method of implementing crowbar overvoltage protection which does not suffer the disadvantages of previous techniques, an IC has been developed for use as an OVP sense and drive circuit, the MC3423.

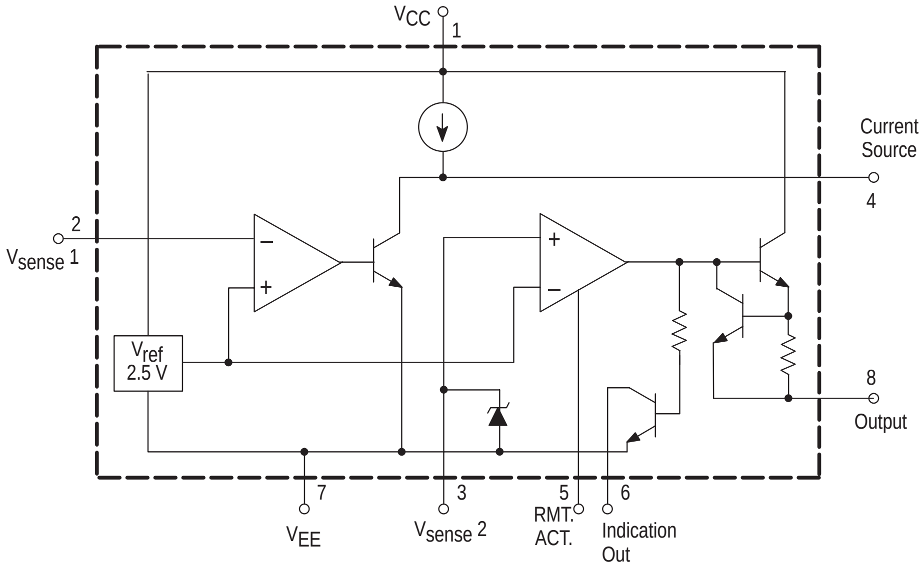
The MC3423 was designed to provide output currents of up to 300 mA with a 400 mA/µs rise time in order to maximize the di/dt capabilities of the crowbar SCR. In addition, its features include:

1. Operation off 4.5 V to 40 V supply voltages.
2. Adjustable low temperature coefficient trip point.
3. Adjustable minimum overvoltage duration before actuation to reduce nuisance tripping in noisy environments.
4. Remote activation input.
5. Indication output.

5. Block Diagram — The block diagram of the MC3423 is shown in Figure 14–7. It consists of a stable 2.6 V reference, two comparators and a high current output. This output, together with the indication output transistor, is activated either by a voltage greater than 2.6 V on Pin 3 or by a TTL/5.0 V CMOS high logic level on the remote activation input, Pin 5.

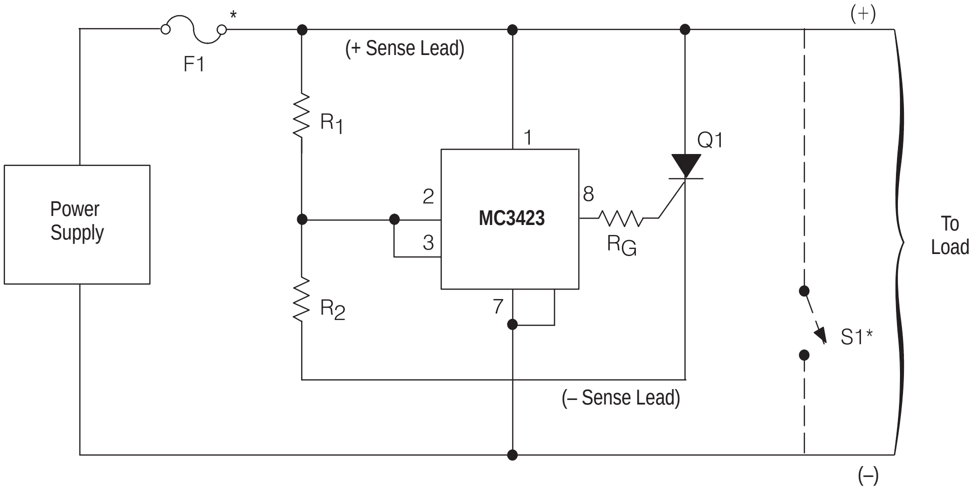
The circuit also has a comparator–controlled current source which can be used in conjunction with and external timing capacitor to set a minimum overvoltage duration (0.5 µs to 1.0 ms) before actuation occurs. This feature allows the OVP circuit to operate in noisy environments without nuisance tripping.

Figure 14–7. MC3423 Block Diagram



6. Basic Circuit Configuration — The basic circuit configuration of the MC3423 OVP is shown in Figure 14–8. In this circuit the voltage sensing inputs of both the internal amplifiers are tied together for sensing the overvoltage condition. The shortest possible propagation delay is thus obtained. The threshold or trip voltage at which the MC3423 will trigger and supply gate drive to the crowbar SCR, Q1, is determined by the selection of R_1 and R_2. Their values can be determined by the equations given in Figure 14–8 or by the graph shown in Figure 14–9. The switch (S1) shown in Figure 14–8 may be used to reset the SCR crowbar. Otherwise, the power supply, across which the SCR is connected, must be shut down to reset the crowbar. If a non current–limited supply is used a fuse or circuit breaker, F1, should be used to protect the SCR and/or the load.

Figure 14–8. MC3423 Basic Circuit Configuration



$$V_{trip} = V_{ref}\left(1 + \frac{R_1}{R_2}\right) \approx 2.6\ V\left(1 + \frac{R_1}{R_2}\right)$$

$R_2 \le 10\ k\Omega$ for minimum drift

*Needed if supply is not current–limited

7. MC3423 Programmable Configuration — In many instances, MC3423 OVP will be used in a noisy environment. To prevent false tripping of the OVP circuit by noise which would not normally harm the load, MC3423 has a programmable delay feature. To implement this feature, the circuit configuration of Figure 14–10 is used.

Here a capacitor is connected from Pin 3 and Pin 4 to V_{EE}. The value of this capacitor determines the minimum duration of the overvoltage condition (t_D) which is necessary to trip the OVP. The value of C_D can be found from Figure 14–11. The circuit operates in the following manner: when V_{CC} rises above the trip point set by R_1 and R_2, the internal current source begins charging the capacitor, C_D, connected to Pins 3 and 4. If the overvoltage condition remains present long enough for the capacitor voltage, V_{CD} to reach V_{ref}, the output is activated. If the overvoltage condition disappears before this occurs, the capacitor is discharged at a rate 10 times faster than the charging rate, resetting the timing feature until the next overvoltage condition occurs.

8. Indication Output — An additional output for use as an indicator of OVP activation is provided by the MC3423. This output (Pin 6) is an open–collector transistor which saturates when the MC3423 OVP is activated. It will remain in a saturated state until the SCR crowbar pulls the supply voltage, V_{CC}, below 4.5 V as in Figure 14–10. This output can be used to clock an edge triggered flip–flop whose output inhibits or shuts down the power supply when the OVP trips. This reduces or eliminates the heatsinking requirements for the crowbar SCR.

Figure 14–9. R_1 versus Trip Voltage for the MC3423 OVP

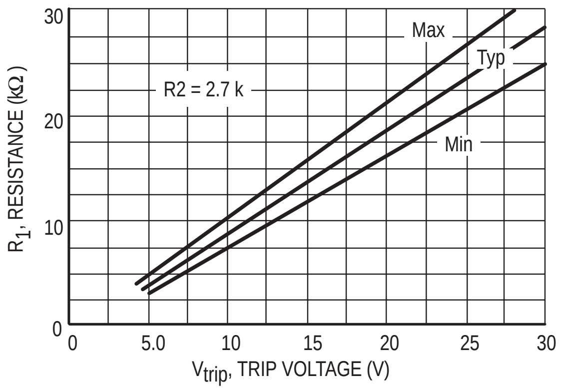
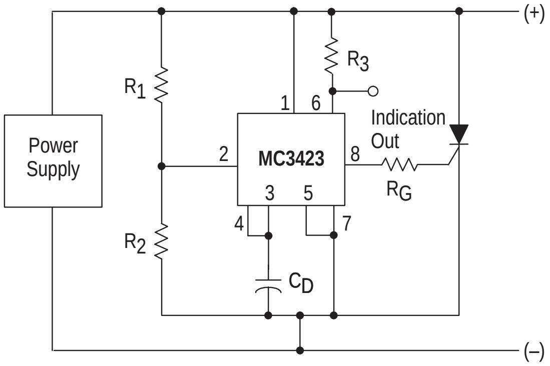


Figure 14–10. MC3423 Configuration for Programmable Minimum Duration of Overvoltage Condition Before Tripping



$$R_3 \geq \frac{V_{trip}}{10\ mA}$$

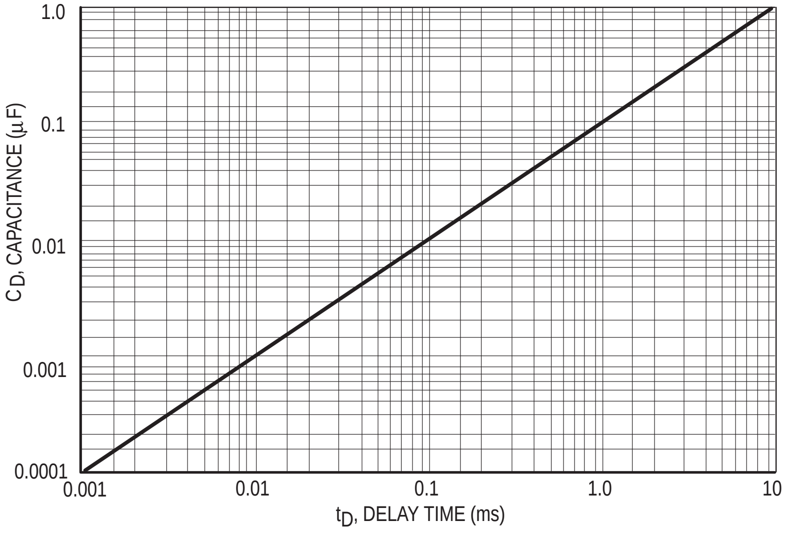
9. Remote Activation Input — Another feature of the MC3423 is its Remote Activation Input, Pin 5. If the voltage on this CMOS/TTL compatible input is held below 0.7 V, the MC3423 operates normally. However, if it is raised to a voltage above 2.0 V, the OVP output is activated independent of whether or not an overvoltage condition is present.

This feature can be used to accomplish an orderly and sequenced shutdown of system power supplies during a system fault condition. In addition, the Indication Output of one MC3423 can be used to activate another MC3423, if a single transistor inverter is used to interface the former's Indication Output to the latter's Remote Activation Input.

D. MC3425 Power Supply Supervisory Circuit

In addition to the MC3423 a second IC, the MC3425 has been developed. Similar in many respects to the MC3423, the MC3425 is a power supply supervisory circuit containing all the necessary functions required to monitor over and undervoltage fault conditions. The block diagram is shown below in Figure 14–12. The Overvoltage (OV) and Undervoltage (UV) Input Comparators are both referenced to an internal 2.5 V regulator. The UV Input Comparator has a feedback activated 12.5 µA current sink (I_H) which is used for programming the input hysteresis voltage (V_H). The source resistance feeding this input (R_H) determines the amount of hysteresis voltage by $V_H = I_H R_H = 12.5 \times 10^{-6}\ R_H$.

Figure 14–11. C_D versus Minimum Overvoltage Duration, t_D for The MC3423 OVP



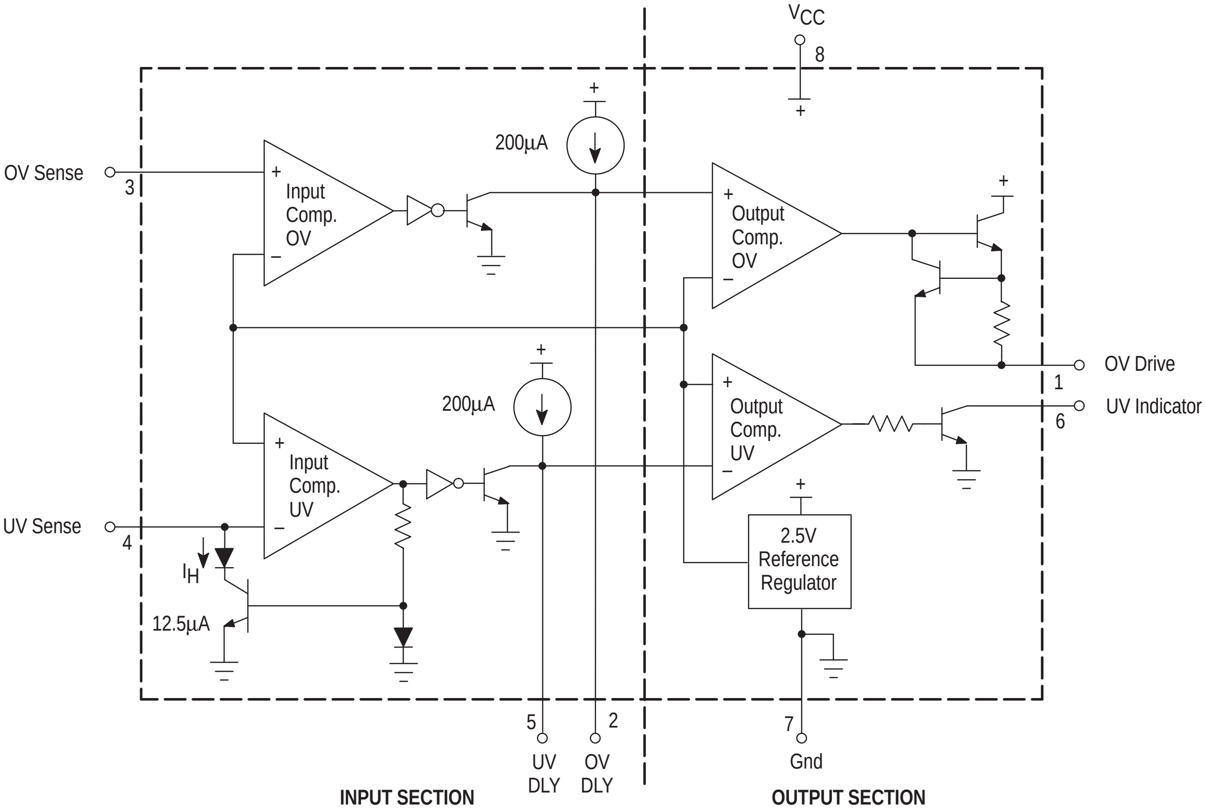
Separate Delay pins (OV DLY, UV DLY) are provided for each channel to independently delay the Drive and Indicator outputs, thus providing greater input noise immunity. The two Delay pins are essentially the outputs of the respective input comparators, and provide a constant current source, $I_{DLY(source)}$, of typically 200 µA when the noninverting input voltage is greater than the inverting input level. A capacitor connected from these Delay pins to ground, will establish a predictable delay time (t_{DLY}) for the Drive and Indicator outputs. The Delay pins are internally connected to the non–inverting inputs of the OV and UV Output Comparators, which are referenced to the internal 2.5 V regulator. Therefore, delay time (t_{DLY}) is based on the constant current source, $I_{DLY(source)}$, charging the external delay capacitor (C_{DLY}) to 2.5 V.

$$t_{DLY} = \frac{V_{ref}\,C_{DLY}}{I_{DLY(source)}} = \frac{2.5\,C_{DLY}}{200\ \mu A} = 12500\,C_{DLY}$$

Figure 14–13 provides C_{DLY} values for a wide range of time delays. The Delay pins are pulled low when the respective input comparator's non–inverting input is less than the inverting input. The sink current $I_{DLY(sink)}$ capability of the Delay pins is ≥1.8 mA and is much greater than the typical 200 µA source current, thus enabling a relatively fast delay capacitor discharge time.

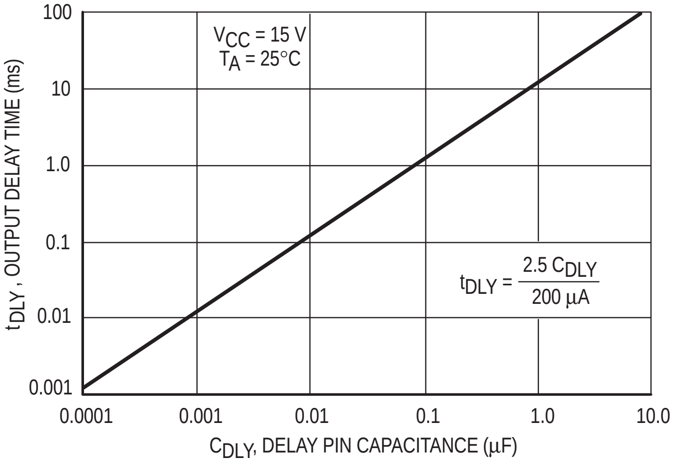
The Overvoltage Drive Output is a current–limited emitter–follower capable of sourcing 300 mA at a turn–on slew rate of 2.0 A/µs, ideal for driving crowbar SCRs. The Undervoltage Indicator Output is an open–collector NPN transistor, capable of sinking 30 mA to provide sufficient drive for LEDs, small relays or shutdown circuitry. These current capabilities apply to both channels operating simultaneously, providing device power dissipation limits are not exceeded. The MC3425 has an internal 2.5 V bandgap reference regulator with an accuracy of ± 4.0% for the basic devices.

Figure 14–12. Block Diagram



Note: All voltages and currents are nominal.

Figure 14–13. Output Delay Time versus Delay Capacitance

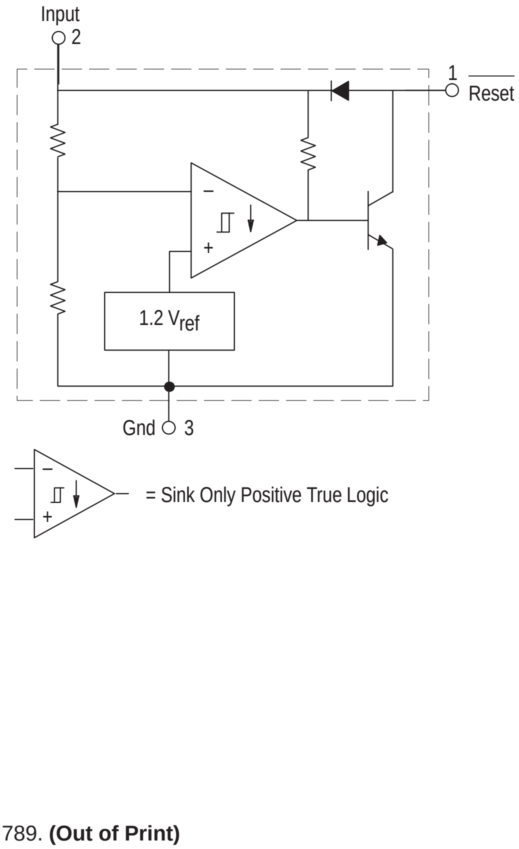


E. MC34064 and MC34164 Series

The MC34064 and MC34164 series are two families of undervoltage sensing circuits specifically designed for use as reset controllers in microprocessor–based systems. They offer the designer an economical solution for low voltage detection with a single external resistor. Both parts feature a trimmed bandgap reference, and a comparator with precise thresholds and built–in hysteresis to prevent erratic reset operation.

The two families of undervoltage sensing circuits, taken together, cover the needs of the most commonly specified power supplies used in MCU/MPU systems. Key parameter specifications of the MC34164 family were chosen to complement the MC34064 series. The table summarizes critical parameters of both families. The MC34064 fulfills the needs of a 5.0 V ± 5% system and features a tighter hysteresis specification. The MC34164 series covers 5.0 V ± 10% and 3.0 V ± 5% power supplies with significantly lower power consumption, making them ideal for applications where extended battery life is required such as consumer products or hand held equipment.

Applications include direct monitoring of the 5.0 V MPU/logic power supply used in appliance, automotive, consumer, and industrial equipment. The MC34164 is specifically designed for battery powered applications where low bias current (1/25th of the MC34064's) is an important characteristic.



REFERENCES
1. *Characterizing the SCR for Crowbar Applications*, Al Pshaenich, Motorola AN789. **(Out of Print)**
2. *Semiconductor Considerations for DC Power Supply SCR Crowbar Circuits*, Henry Wurzburg, Third National Sold–State Power Conversion Conference, June 25, 1976.
3. *Is a Crowbar Enough?* Willis C. Pierce Jr., Hewlett–Packard, Electronic Design 20, Sept. 27, 1974.
4. *Transient Thermal Response — General Data and Its Use*, Bill Roehr and Brice Shiner, Motorola AN569. **(Out of Print)**

SECTION 15

HEATSINKING

A. The Thermal Equation

A necessary and primary requirement for the safe operation of any semiconductor device, whether it be an IC or a transistor, is that its junction temperature be kept below the specified maximum value given on its data sheet. The operating junction temperature is given by:

$$T_J = T_A + P_D\ \theta_{JA} \qquad (15.1)$$

where: T_J = junction temperature (°C)
T_A = ambient air temperature (°C)
P_D = power dissipated by device (W)
θ_{JA} = thermal resistance from junction–to–ambient air (°C/W)

The junction–to–ambient thermal resistance (θ_{JA}) in Equation (15.1), can be expressed as a sum of thermal resistances as shown below:

$$\theta_{JA} = \theta_{JC} + \theta_{CS} + \theta_{SA} \qquad (15.2)$$

where: θ_{JC} = junction–to–case thermal resistance
θ_{CS} = case–to–heatsink thermal resistance
θ_{SA} = heatsink–to–ambient thermal resistance

Equation (15.2) applies only when an external heatsink is used. If no heatsink is used, θ_{JA} is equal to the device package θ_{JA} given on the data sheet.

θ_{JC} depends on the device and its package (case) type, while θ_{SA} is a property of the heatsink and θ_{CS} depends on the type of package/heatsink interface employed. Values for θ_{JC} and θ_{SA} are found on the device and heatsink data sheets, while θ_{CS} is given in Table 15–1.

Table 15–1. θ_{CS} For Various Packages & Mounting Arrangements

	θ_{CS}			
	Metal–to–Metal*		**Using an Insulator***	
Case	**Dry**	**With Heatsink Compound**	**With Heatsink Compound**	**Type**
TO–204	0.5°C/W	0.1°C/W	0.36°C/W 0.28°C/W	3 mil MICA Anodized Aluminum
TO–220	1.2°C/W	1.0°C/W	1.6°C/W	2 mil MICA

*Typical values; heatsink surface should be free of oxidation, paint, and anodization

Examples showing the use of Equations (15.1) and (15.2) in thermal calculations are as follows:

Example 1: Find required heatsink θ_{SA} for an MC7805CT, given:

$$T_{J(max)}\ \text{(desired)} = +125°C$$
$$T_{A(max)} = +70°C$$
$$P_D = 2.0\ W$$

Mounted directly to heatsink with silicon thermal grease at interface:

1. From MC7805CT data sheet, θ_{JC} = 5°C/W
2. From Table 15–1. θ_{CS} = 1.6°C/W
3. Using Equation (15.1) and (15.2), solve for θ_{SA}:

$$\theta_{SA} = \frac{(T_J - T_A)}{P_D} - \theta_{CS} - \theta_{JC}$$

$$\theta_{SA} = \frac{(125 - 70)}{2} - 5.0 - 1.6 \; (\leq 20.9°\text{C/W required})$$

Example 2: Find the maximum allowable T_A for an unheatsinked MC78L15CT, given:

$T_{J(max)}$ (desired) = +125°C
P_D = 0.25 W

1. From MC78L15CT data sheet, θ_{JA} = 200°C/W
2. Using Equation (15.1), find T_A:

$$\begin{aligned} T_A &= T_j - P_D\,\theta_{JA} \\ &= 125 - 0.25\,(200) \\ &= +75°\text{C} \end{aligned}$$

B. Selecting a Heatsink

Usually, the maximum ambient temperature, power being dissipated, the $T_{J(max)}$, and θ_{JC} for the device being used are known. The required θ_{SA} for the heatsink is then determined using Equations (15.1) and (15.2), as in Example 1. The designer may elect to use a commercially available heatsink, or if packaging or economy demands it, design his own.

1. Commercial Heatsinks

As an aid in selecting a heatsink, a representative listing is shown in Table 15–2. This listing is by no means complete and is only included to give the designer an idea of what is available.

Table 15–2. Commercial Heatsink Selection Guide

TO–204AA (TO–3)	
θ_{SA}*(°C/W)	**Manufacturer/Series or Part Number**
0.3–1.0	Thermalloy — 6441, 6443, 6450, 6470, 6560, 6590, 6660, 6690
1.0–3.0	Wakefield — 641 Thermalloy — 6123, 6135, 6169, 6306, 6401, 6403, 6421, 6423, 6427, 6442, 6463, 6500
3.0–5.0	Wakefield — 621, 623 Thermalloy — 6606, 6129, 6141, 6303 IERC — HP Staver — V3–3–2
5.0–7.0	Wakefield — 690 Thermalloy — 6002, 6003, 6004, 6005, 6052, 6053, 6054, 6176, 6301 IERC — LB Staver — V3–5–2
7.0–10	Wakefield — 672 Thermalloy — 6001, 6016, 6051, 6105, 6601 IERC — LA µP Staver — V1–3, V1–5, V3–3, V3–5, V3–7
10–25	Thermalloy — 6013, 6014, 6015, 6103, 6104, 6105, 6117

*All values are typical as given by the manufacturer or as determined from characteristic curves supplied by the manufacturer.

Table 15–2. Commercial Heatsink Selection Guide (continued)

TO–204AA (TO–5)	
θ_{SA}*(°C/W)	**Manufacturer/Series or Part Number**
12 to 20	Wakefield — 260 Thermalloy — 1101, 1103 Staver — V3A–5
20 to 30	Wakefield — 209 Thermalloy — 1116, 1121, 1123, 1130, 1131, 1132, 2227, 3005 IERC — LP Staver — F5–5
30 to 50	Wakefield — 207 Thermalloy — 2212, 2215, 225, 2228, 2259, 2263, 2264 Staver — F5–5, F6–5
	Wakefield — 204, 205, 208 Thermalloy — 1115, 1129, 2205, 2207, 2209, 2210, 2211, 2226, 2230, 2257, 2260, 2262 Staver — F1–5, F5–5

TO–204AB	
θ_{SA}*(°C/W)	**Manufacturer/Series or Part Number**
5.0 to 10	IERC H P3 Series Staver — V3–7–225, V3–7–96
10 to 15	Thermalloy — 6030, 6032, 6034 Staver — V4–3–192, V–5–1
20 to 30	Wakefield — 295 Thermalloy — 6025, 6107
15 to 20	Thermalloy — 6106 Staver — V4–3–128, V6–2

TO–226AA (TO–92)	
θ_{SA}*(°C/W)	**Manufacturer/Series or Part Number**
46	Staver F5–7A, F5–8
50	IERC AUR
57	Staver F5–7D
65	IERC RU
72	Staver F1–8, F2–7
80 to 90	Wakefield 292
85	Thermalloy 2224
DUAL–IN–LINE–PACKAGE ICs	
20	Thermalloy — 6007
30	Thermalloy — 6010
32	Thermalloy — 6011
34	Thermalloy — 6012
45	IERC — LIC
60	Wakefield — 650, 651

*All values are typical as given by the manufacturer or as determined from characteristic curves supplied by the manufacturer.

Staver Co., Inc.: 41–51 N. Saxon Ave., Bay Shore, NY 11706
IERC: 135 W. Magnolia Blvd., Burbank, CA 91502
Thermalloy: P.O. Box 34829, 2021 W. Valley View Ln. Dallas, TX
Wakefield Engin Ind: Wakefield, MA 01880

2. Custom Heatsink Design

Custom heatsinks are usually either forced air cooled or convection cooled. The design of forced air cooled heatsinks is usually done empirically, since it is difficult to obtain accurate air flow measurements. On the other hand, convection cooled heatsinks can be designed with fairly predictable characteristics. It must be emphasized, however, that any custom heatsink design should be thoroughly tested in the actual equipment configuration to be certain of its performance. In the following sections, a design procedure for convection cooled heatsinks is given.

Obviously, the basic goal of any heatsink design is to produce a heatsink with an adequately low thermal resistance, θ_{SA}. Therefore, a means of determining θ_{SA} is necessary in the design. Unfortunately, a precise calculation method for θ_{SA} is beyond the scope of this book.* However, a first order approximation can be calculated for a convection cooled heatsink if the following conditions are met:

1. The heatsink is a flat rectangular or circular plate whose thickness is smaller than its length or width.
2. The heatsink will not be located near other heat radiating surfaces.
3. The aspect ratio of a rectangular heatsink (length:width) is not greater than 2:1.
4. Unrestricted convective air flow.

For the above conditions, the heatsink thermal resistance can be approximated by:

$$\theta_{SA} \simeq \frac{1}{A\eta\,(F_c h_c + \in H_r)} \quad (^\circ C/W) \tag{15.3}$$

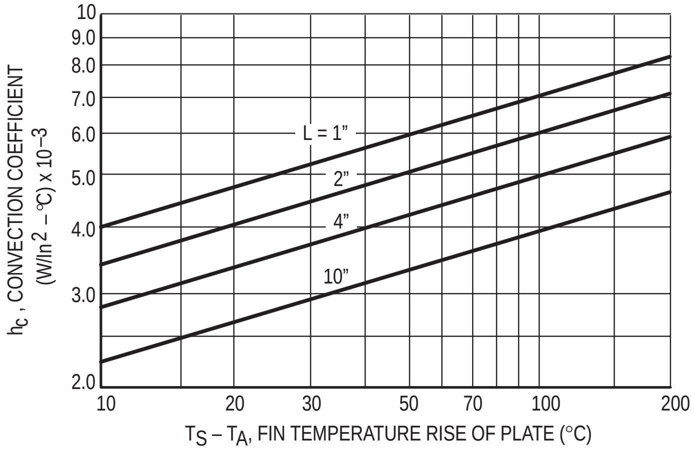
where: A = area of the heatsink surface
η = heatsink effectiveness
F_c = convective correction factor
h_c = convection heat transfer coefficient
$\in$ = emissivity
H_r = normalized radiation heat transfer coefficient

The convective heat transfer coefficient, h_c, can be found from Figure 15–1. Note that it is a function of the heatsink fin temperature rise ($T_S - T_A$) and the heatsink significant dimension (L). The fin temperature rise ($T_S - T_A$) is given by:

$$T_S - T_A = \theta_{SA} P_D \tag{15.4}$$

where: T_S = heatsink temperature
T_A = ambient temperature
θ_{SA} = heatsink–to–ambient thermal resistance
P_D = power dissipated

Figure 15–1. Convection Coefficient (h_c)



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*If greater precision is desired, or more information on heat flow and heatsinking is sought, consult the references list at the end of this section.

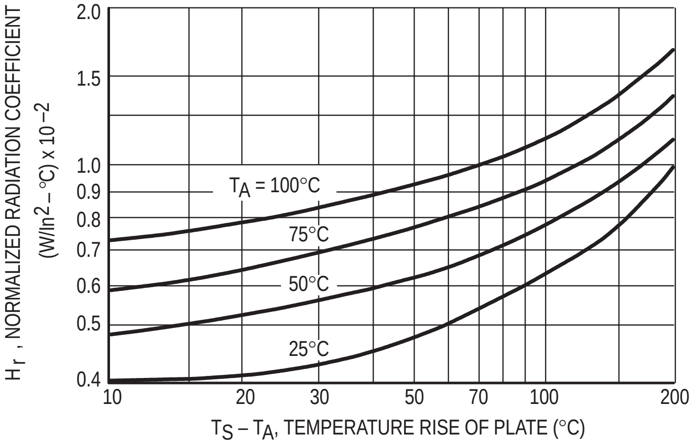
The significant heatsink dimension (L) is dependent on the heatsink shape and mounting place and is given in Table 15–3. The convective correction factor (F_C) is likewise dependent on shape and mounting plane of the heatsink and is also given in Table 15–3.

Table 15–3. Significant Dimension (L) and Correction Factor (F_C) for Convection Thermal Resistance

Surface	Significant Dimension L		Correction Factor F_C	
	Position	**L**	**Position**	**F_C**
Rectangular Plane	Vertical	Height (max 2 ft)	Vertical Plane	1.0
	Horizontal	$\frac{\text{length} \times \text{width}}{\text{length} + \text{width}}$	Horizontal Plane both surfaces exposed	1.35
Circular Plane	Vertical	$\pi / 1 \times$ diameter	Top only exposed	0.9

The normalized radiation heat transfer coefficient (H_r) is dependent on the ambient temperature (T_A) and the heatsink temperature rise ($T_S - T_A$) given by Equation (15.4). H_r can be determined from Figure 15–2.

Figure 15–2. Normalized Radiation Coefficient (H_r)



The emissivity (∈) can be found in Table 15–4 for various heatsink surfaces.

Table 15–4. Typical Emissivities of Common Surfaces

Surface	Emissivity (∈)
Alodine on Aluminum	0.15
Aluminum, Anodized	0.7 to 0.9
Aluminum, Polished	0.05
Copper, Polished	0.07
Copper, Oxidized	0.70
Rolled Sheet Steel	0.66
Air Drying Enamel (any color)	0.85 to 0.91
Oil Paints (any color)	0.92 to 0.96
Varnish	0.89 to 0.93

Finally, the heatsink efficient (η) can be found from the nomograph of Figure 15–3. Use of the nomograph is as follows:

a) Find $h_T = Fchc + \in H_r$ from Figures 15–1, 15–2 and Tables 15–3 and 15–4, and locate this point on the nomograph.

b) Draw a line from h_T through chosen heatsink fin thickness (x) to find α.

c) Determine D for the heatsink shape as given in Figure 15–4 and draw a line from this point through α, which was found in (b), to determine η.

d) If power dissipating element is not located at heatsink's center of symmetry, multiply η by 0.7 (for vertically mounted plates only).

Note that in order to calculate θ_{SA} from Equation (15.3), it is necessary to know the heatsink size. Therefore, in order to arrive at a suitable heatsink design, a trial size is selected, its θ_{SA} evaluated, and the original size reduced or enlarged as necessary. This process is iterated until the smallest heatsink is obtained that has the required θ_{SA}. The following design example is given to illustrate this procedure.

Figure 15–3. Fin Effectiveness Nomogram for Symmetrical Flat, Uniformly Thick Fins

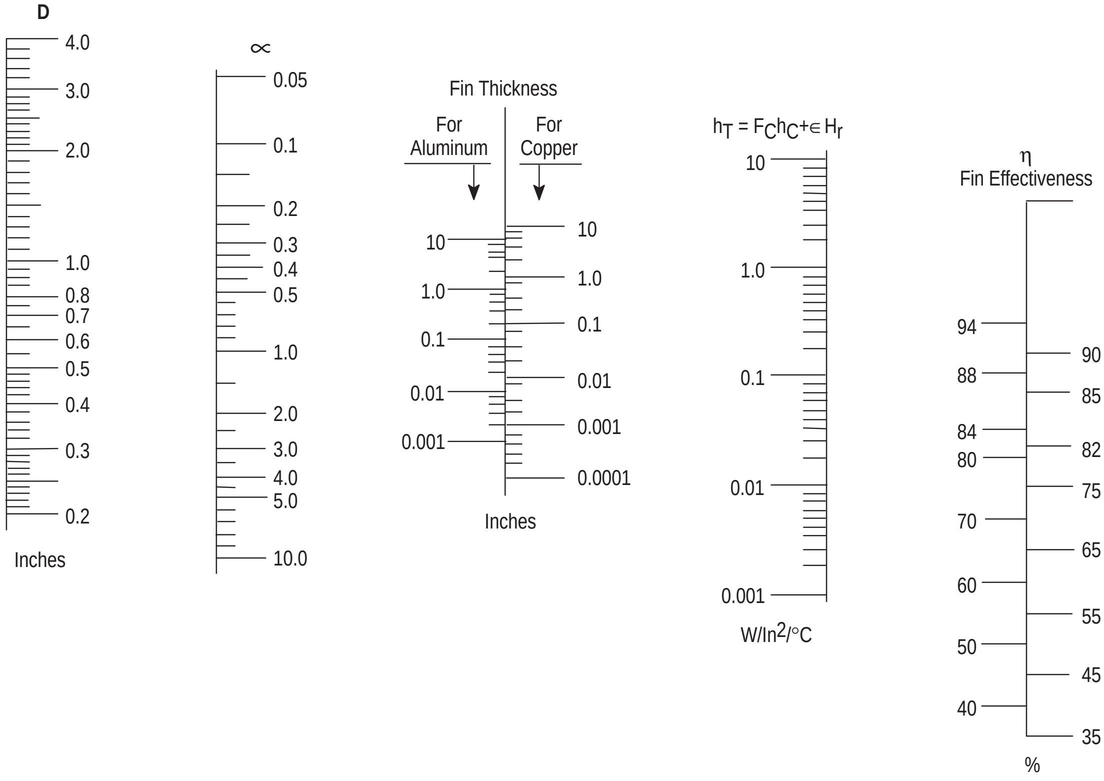


Figure 15–4. Determination of D for Use in η Nomograph of Figure 15–3

$D \cong \sqrt{\frac{ab}{\pi}}$, if $a,b \gg S$ & $b \le 2a$

$D \simeq \frac{d}{2}$, if $d \gg s$

Heatsink Design Example

Design a flat rectangular heatsink for use with a horizontally mounted power device on a PC board, given the following:

1. Heatsink $\theta_{SA} = 25°C/W$
2. Power to be dissipated, $P_D = 2.0$ W
3. Maximum ambient temperature, $T_A = 50°C$
4. Heatsink to be constructed from 1/8″ (0.125″) thick anodized aluminum.
   a) First, a trial heatsink is chosen: 2″ × 3″ (experience will simplify this selection and reduce the number of necessary iterations.)
   b) The factors in Equation (15.3) are evaluated by using the Figures and Tables given:

$$\begin{aligned}
A &= 2'' \times 3'' = 6 \text{ sq. in.}\\
L &= 6/5'' = 1.2 \text{ in. (from Table 15–3)}\\
T_S - T_A &= 50°C \text{ (from Figure 15–4)}\\
h_c &= 5.8 \times 10^{-3} \text{ W/in}^2 - °C \text{ (from Figure 15–1)}\\
F_c &= 0.9 \text{ (from Table 15–3)}\\
H_r &= 6.1 \times 10^{-3} \text{ W/in}^2 - °C \text{ (from Figure 15–2)}\\
\in &= 0.9 \text{ (from Table 15–4)}\\
h_T &= Fchc + H_{r\in} = 10.7 \times 10^{-3} \text{ W/in}^2 - °C\\
\alpha &= 0.13 \text{ (from Figure 15–3)}\\
D &= 1.77 \text{ (from Figure 15–4)}\\
\eta &> 0.94 \simeq 1 \text{ (from Figure 15–3)}
\end{aligned}$$

   c) Using Equation (15.3), find θ_{SA}:

$$\theta_{SA} \simeq \frac{1}{A\eta\ (Fchc + \in H_r)} = 16.66°C/W < 25°C/W$$

   d) Since 2″ × 3″ is too large, try 2″ × 2″. Following the same procedure, θ_{SA} is found to be 25°C/W, which exactly meets the design requirements.

SOIC MINIATURE IC PLASTIC PACKAGE

Thermal Information

The maximum power consumption an integrated circuit can tolerate at a given operating ambient temperature, can be found from the equation:

$$P_{D(T_A)} = \frac{T_{J(max)} - T_A}{R_{\theta JA}\ (typ)}$$

where: $P_{D(T_A)}$ = power dissipation allowable at a given operating ambient temperature,

$T_{J(max)}$ = maximum operating junction temperature as listed in the maximum ratings section,

T_A = desired operating ambient temperature,

$R_{\theta JA}$ (typ) = typical thermal resistance junction–to–ambient.

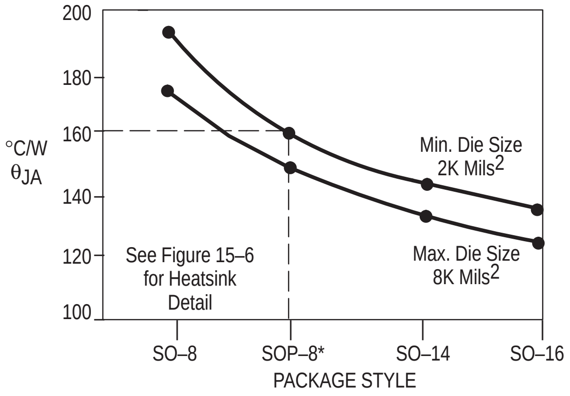
Maximum Ratings

Rating	Symbol	Value	Unit
Operating Ambient Temperature Range	T_A	0 to +70 – 40 to +85	°C
Operating Junction Temperature	T_J	150	°C
Storage Temperature Range	T_{stg}	– 55 to +150	°C

THERMAL CHARACTERISTICS OF SOIC PACKAGES

Measurement specimens are solder mounted on a Philips SO test board #7322–078, 80873 in still air. No auxiliary thermal conduction aids are used. As thermal resistance varies inversely with die area, a given package takes thermal resistance values between the max and min curves shown. These curves represent the smallest (2000 square mils) and largest (8000 square mils) die areas expected to be assembled in the SOIC package.

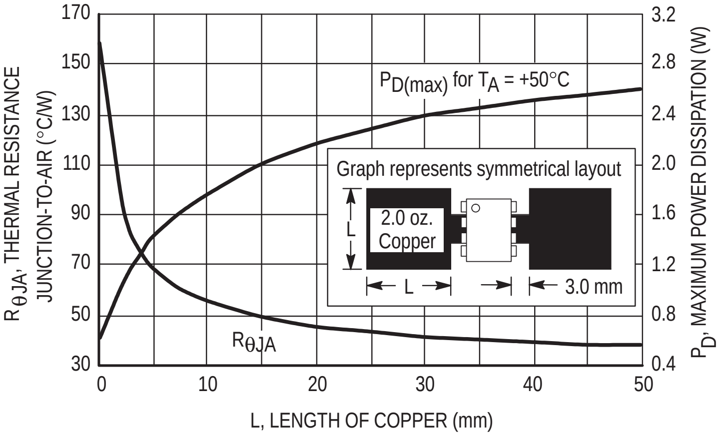
Figure 15–5. Thermal Resistance, Junction–to–Ambient (°C/W)



Data taken using Philips SO test board #7322–078, 80873

*SOP–8 using standard SO–8 footprint — minimum pad size

Figure 15–6. SOP–8 Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length



SOP–8 and SOP–16L Packaged Devices

Several families of voltage regulators and power control ICs have been introduced in surface mounted packages which were developed by the Analog IC Division. The SOP–8 and SOP–16L packages have external dimensions which are identical to the standard SO–8 and SO–16L surface mount devices, but the center four leads of the packages are all connected to the leadframe die flag. This internal modification decreases the package thermal resistance and therefore increases its power dissipation capability. This advantage is fully realized when the package is mounted on a printed circuit board with a single pad for the four center leads. This large area of copper then acts as an external heat spreader, efficiently conducting heat away from the package.

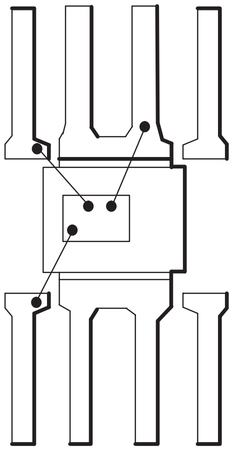
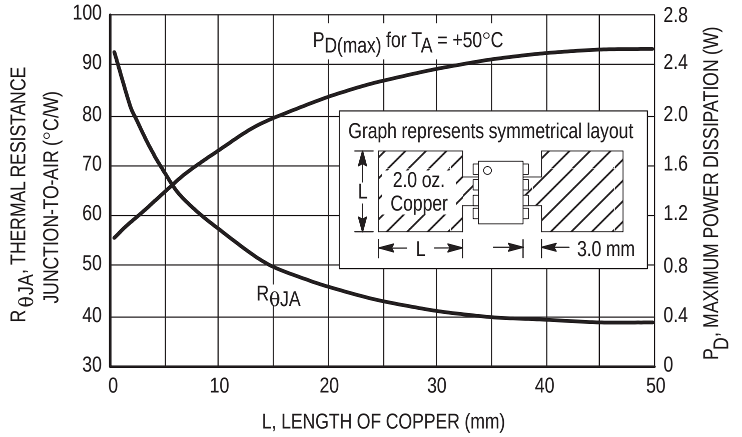


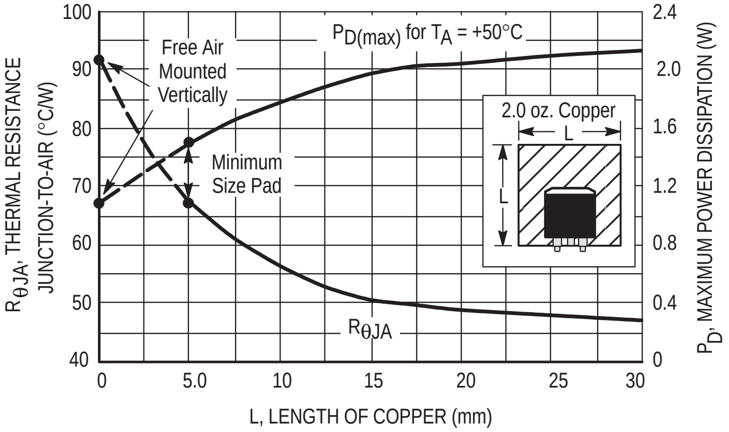
Figure 15–7. SOP–16L Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length



THERMAL CHARACTERISTICS OF DPAK AND D^{2}PAK PACKAGE

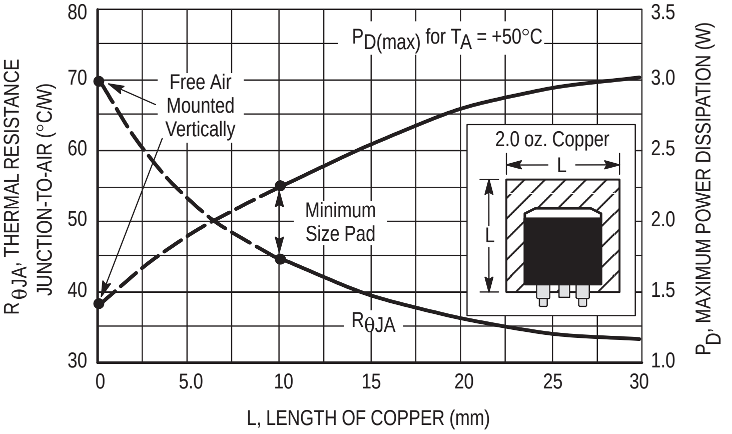
The evaluation was performed using an active device (4900 square mils) mounted on 2.0 ounce copper foil epoxied to a GIO type printed circuit board. Measurements were made in still air and no auxiliary thermal conduction aids were used. The size of a square copper pad was varied, and all measurements were made with the unit mounted as shown in Figure 15–8. The curve shown in Figure 15–8 is a plot of junction–to–air thermal resistance versus the length of the square copper pad in millimeters. This shows that when the DPAK is mounted on a 10 mm × 10 mm square pad of 2.0 ounce copper it has a thermal resistance which is comparable to a TO–220 device mounted vertically without additional heatsinking.

Figure 15–8. DPAK Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length



The thermal characteristics of the D^{2}PAK are shown in Figure 15–9. The device was mounted on 2.0 oz. copper on an FR4–type P.C. board. The maximum power dissipation was measured with a junction temperature of 150°C.

Figure 15–9. 3–Pin and 5–Pin D^{2}PAK Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length



Power/Motor Control Circuits

In Brief . . .

With the expansion of electronics into more and more mechanical systems, there comes an increasing demand for simple but intelligent circuits that can blend these two technologies. In the past, the task of power/motor control was once accomplished with discrete devices. But today this task is being performed by bipolar IC technology due to cost, size, and reliability constraints. Motorola offers integrated circuits designed to anticipate the requirements for both simple and sophisticated control systems, while providing cost effective solutions to meet the needs of the applications.

Power Controllers

An assortment of battery and ac line–operated control ICs for specific applications are shown. They are designed to enhance system performance and reduce complexity in a wide variety of control applications.

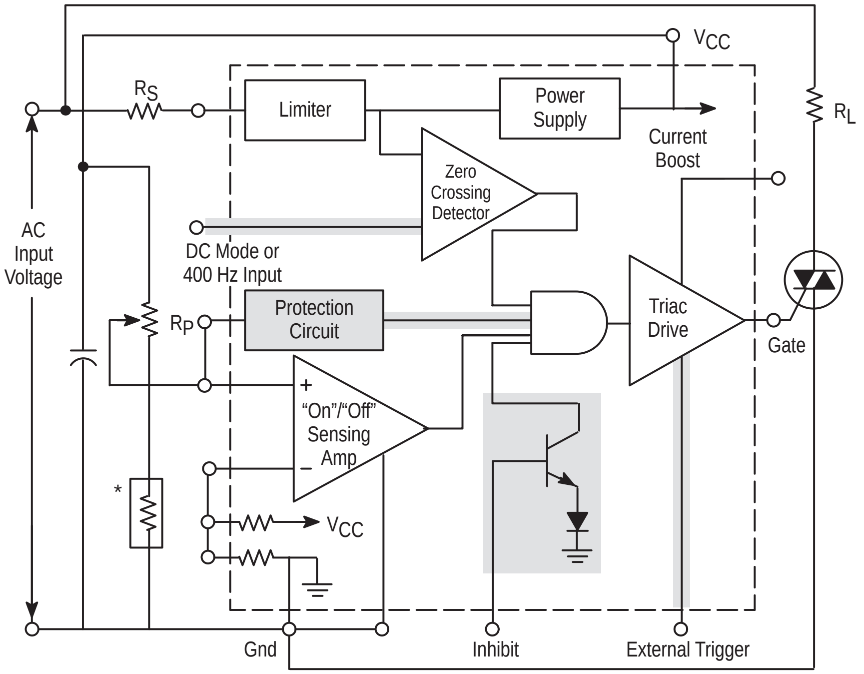
Zero Voltage Switch

CA3059

T_A = –40° to +85°C, Case 646

This device is designed for thyristor control in a variety of ac power switching applications for ac input voltages of 24 V, 120 V, 208/230 V, and 227 V @ 50/60 Hz.

- **Limiter–Power Supply** – Allows operation directly from an ac line.
- **Differential "On"/"Off" Sensing Amplifier** – Tests for condition of external sensors or input command signals. Proportional control capability or hysteresis may be implemented.
- **Zero–Crossing Detector** – Synchronizes the output pulses to the zero voltage point of the ac cycle. Eliminates RFI when used with resistive loads.
- **Triac Drive** – Supplies high current pulses to the external power controlling thyristor.
- **Protection Circuit** (CA3059 only) – A built–in circuit may be actuated, if the sensor opens or shorts, to remove the drive circuit from the external triac.
- **Inhibit Capability** (CA3059 only) – Thyristor firing may be inhibited by the action of an internal diode gate.
- **High Power DC Comparator Operation** (CA3059 only) – Operation in this mode is accomplished by connecting Pin 7 to 12 (thus overriding the action of the zero–crossing detector).



*NTC Sensor
NOTE: Shaded Area Not Included with CA3079.

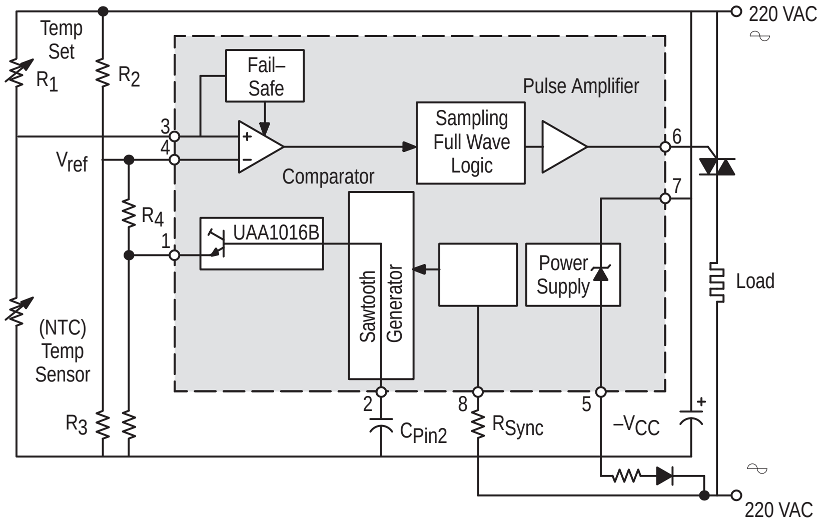
Zero Voltage Controller

UAA1016B

T_A = –20° to +100°C, Case 626

The UAA1016B is designed to drive triacs with the Zero voltage technique which allows RFI free power regulation of resistive loads. It provides the following features:

- Proportional Temperature Control Over an Adjustable Band
- Adjustable Burst Frequency (to Comply with Standards)
- No DC Current Component Through the Main Line (to Comply with Standards)
- Negative Output Current Pulses (Triac Quadrants 2 and 3)
- Direct AC Line Operation
- Low External Components Count



Zero Voltage Controller

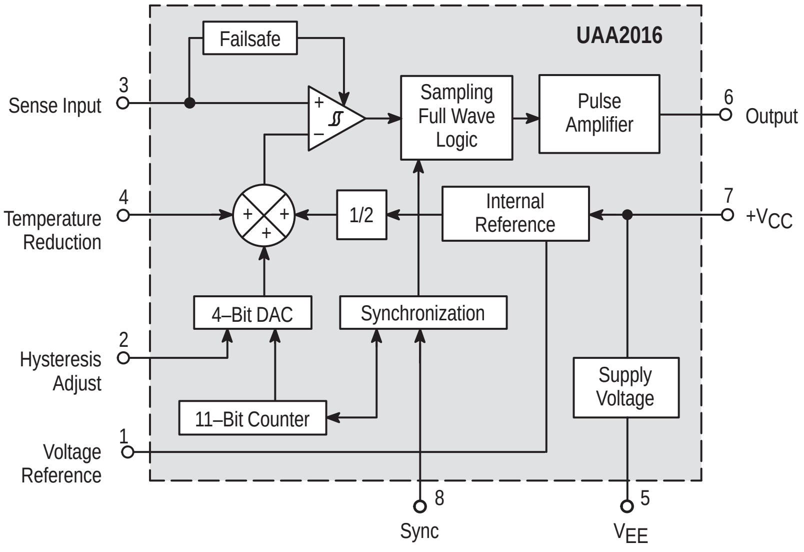
UAA2016P, D

T_A = –20° to +85°C, Case 626, 751

The UAA2016 is designed to drive triacs with the Zero Voltage technique which allows RFI free power regulation of resistive loads. Operating directly on the ac power line, its main application is the precision regulation of electrical heating systems such as panel heaters or irons.

A built–in digital sawtooth waveform permits proportional temperature regulation action over a ±1°C band around the set point. For energy savings there is a programmable temperature reduction function, and for security, a sensor failsafe inhibits output pulses when the sensor connection is broken. Preset temperature (i.e., defrost) application is also possible. In applications where high hysteresis is needed, its value can be adjusted up to 5°C around the set point. All these features are implemented with a very low external component count.

- Zero Voltage Switch for Triacs, up to 2.0 kW (MAC212A8)
- Direct AC Line Operation
- Proportional Regulation of Temperature over a 1°C Band
- Programmable Temperature Reduction
- Preset Temperature (i.e., Defrost)
- Sensor Failsafe
- Adjustable Hysteresis
- Low External Component Count



Power Controllers (continued)

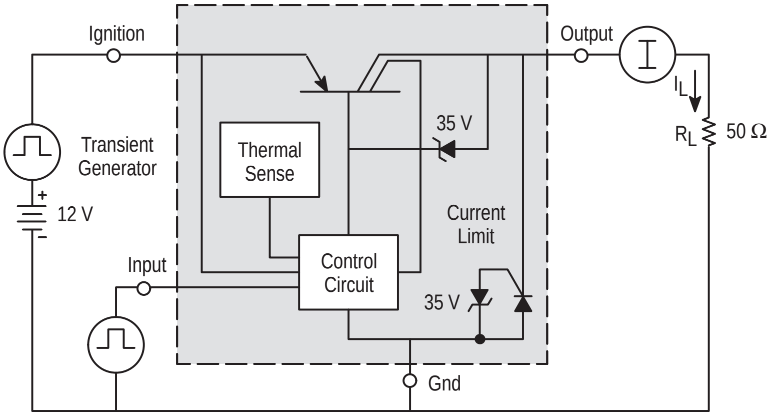
High–Side Driver Switch

MC3399T, DW

T_J = –40° to +150°C, Case 314D, 751G

The MC3399T is a high side driver switch that is designed to drive loads from the positive side of the power supply. The output is controlled by a TTL compatible Enable pin. In the “on” state, the device exhibits very low saturation voltages for load currents in excess of 750 mA. The device also protects the load from positive or negative–going high voltage transients by becoming an open circuit and isolating the transient for its duration from the load.

The MC3399T is fabricated on a Power BiMOS process which combines the best features of Bipolar and MOS technologies. The mixed technology provides higher gain PNP output devices and results in Power Integrated Circuits with reduced quiescent current.



Motor Controllers

This section contains integrated circuits designed for cost effective control of specific motor families. Included are controllers for brushless, dc servo, stepper, and universal type motors.

Brushless DC Motor Controllers

Advances in magnetic materials technology and integrated circuits have contributed to the unprecedented rise in popularity of brushless dc motors. Analog control ICs are making the many features and advantages of brushless motors available at a much more economical price. Motorola offers a family of monolithic integrated brushless dc motor controllers. These ICs provide a choice of control functions which allow many system features to be easily implemented at a fraction of the cost of discrete solutions. The following table summarizes and compares the features of Motorola’s brushless motor controllers.

1Features Summary for Motorola Brushless DC Motor Controllers

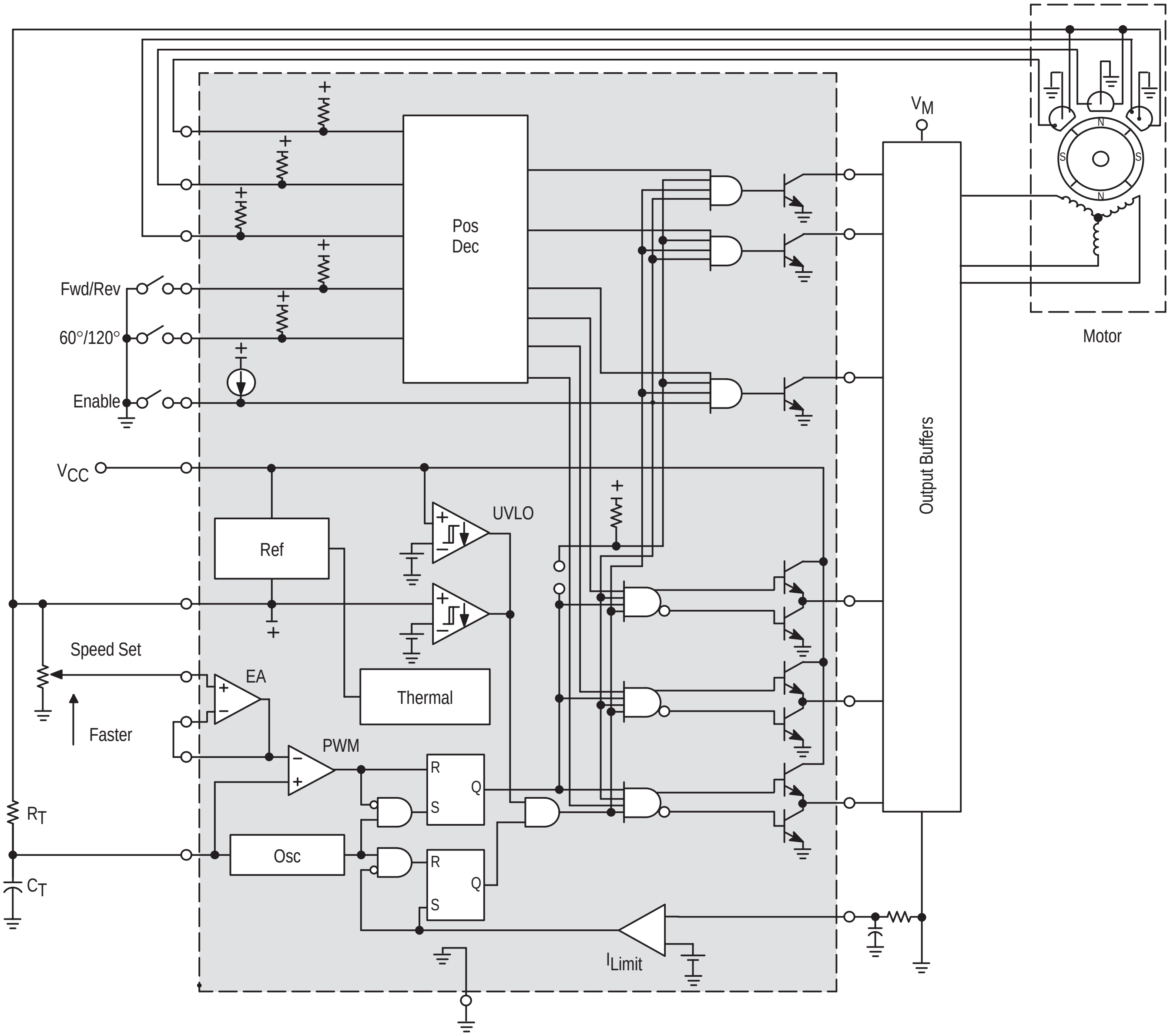
Device	Operating Voltage Range (V)		Undervoltage Lockout	Internal Thermal Shutdown	Fwd/Rev Control	Sensor Electrical Phasing	Output Enable	Output Drivers		6.25 V Reference Output	Current Sense Comparator Input(s)	Error Amplifier	$\overline{\text{FAULT}}$ Output	Separate Drive V_C	Brake Input	Suffix/ Package
	V_{CC}	V_C						Totem Pole (Bottom)	Open Collector (Top)							
MC33033	10–30	–	✓	✓	✓	60°/300° and 120°/240°	✓	✓	✓	✓	Noninv. Only	✓	–	–	–	P/738, DW/751D
MC33035	10–40	10–30	✓	✓	✓		✓	✓	✓	✓	Noninv. and Inv.	✓	✓	✓	✓	P/724, DW/751E

MC33033P, DW

T_A = –40° to +85°C, Case 738, 751D

The MC33033 is a lower cost second generation brushless dc motor controller which has evolved from the full featured MC33034 and MC33035 controllers. The MC33033 contains all of the active functions needed to implement a low cost open loop motor control system. This IC has all of the key control and protection functions of the two full featured devices with the following secondary features deleted: separate drive–circuit supply and ground pins, the brake input, and the fault output signal. Like its MC33035 predecessor, the MC33033 has a control pin which allows the user to select 60°/300° or 120°/240° sensor electrical phasings.

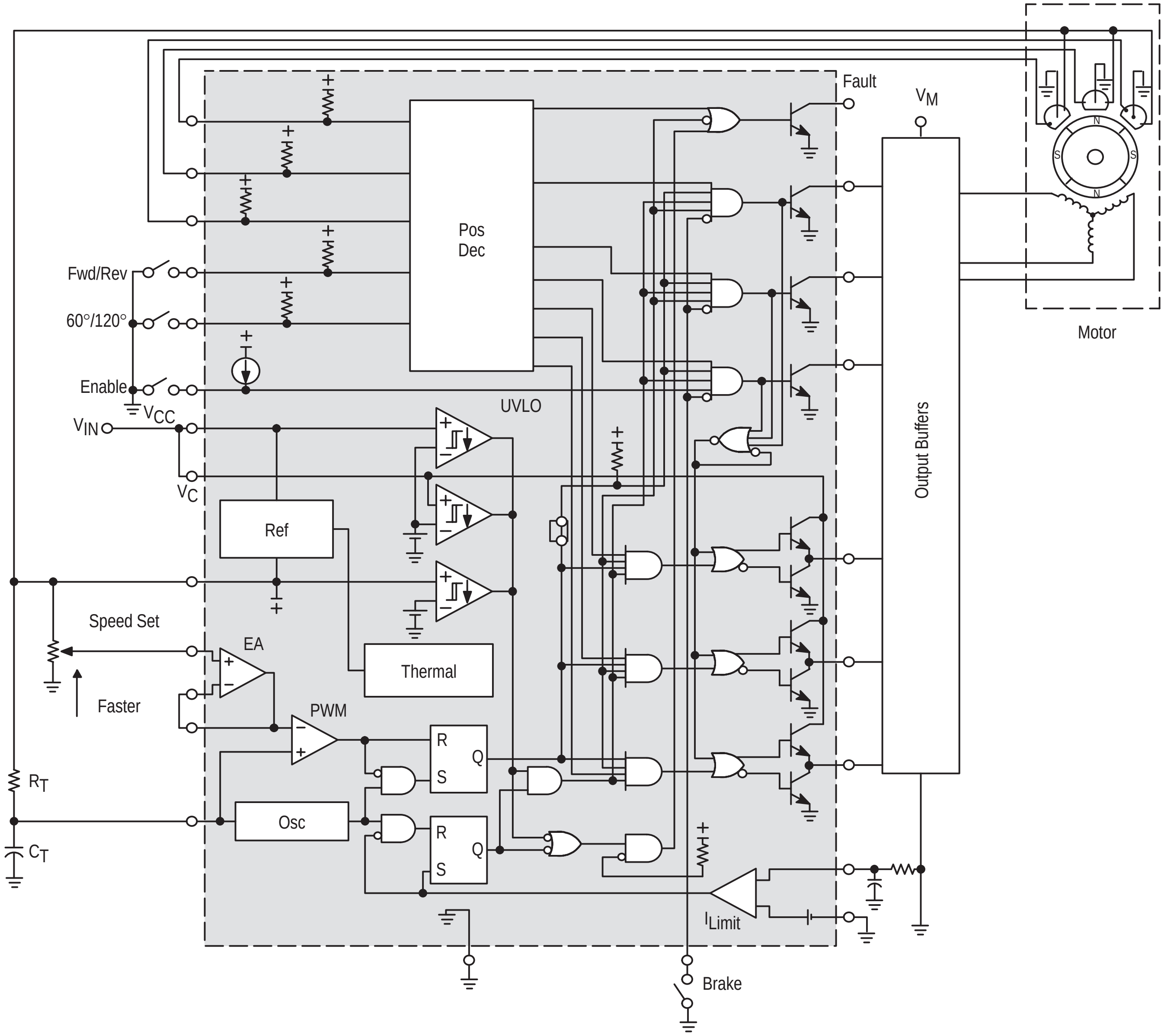
Because of its low cost, the MC33033 can efficiently be used to control brush dc motors as well as brushless. A brush dc motor can be driven using two of the three drive output phases provided in the MC33033, while the Hall sensor input pins are selectively tied to V_{ref} or ground. Other features such as forward/reverse, output enable, speed control, current limiting, undervoltage lockout and internal thermal shutdown will still remain functional.



MC33035P, DW

T_A = –40° to +85°C, Case 724, 751E

The MC33035 is a second generation high performance brushless dc motor controller which contains all of the active functions required to implement a full featured open loop motor control system. While being pin–compatible with its MC33034 predecessor, the MC33035 offers additional features at a lower price. The two additional features provided by the MC33035 are a pin which allows the user to select 60°/300° or 120°/240° sensor electrical phasings, and access to both inverting and noninverting inputs of the current sense comparator. The earlier devices had two part numbers which were needed to support the different sensor phasings, and the inverting input to the current sense comparator was internally grounded. All of the control and protection features of the MC33034 are also provided in the MC33035.

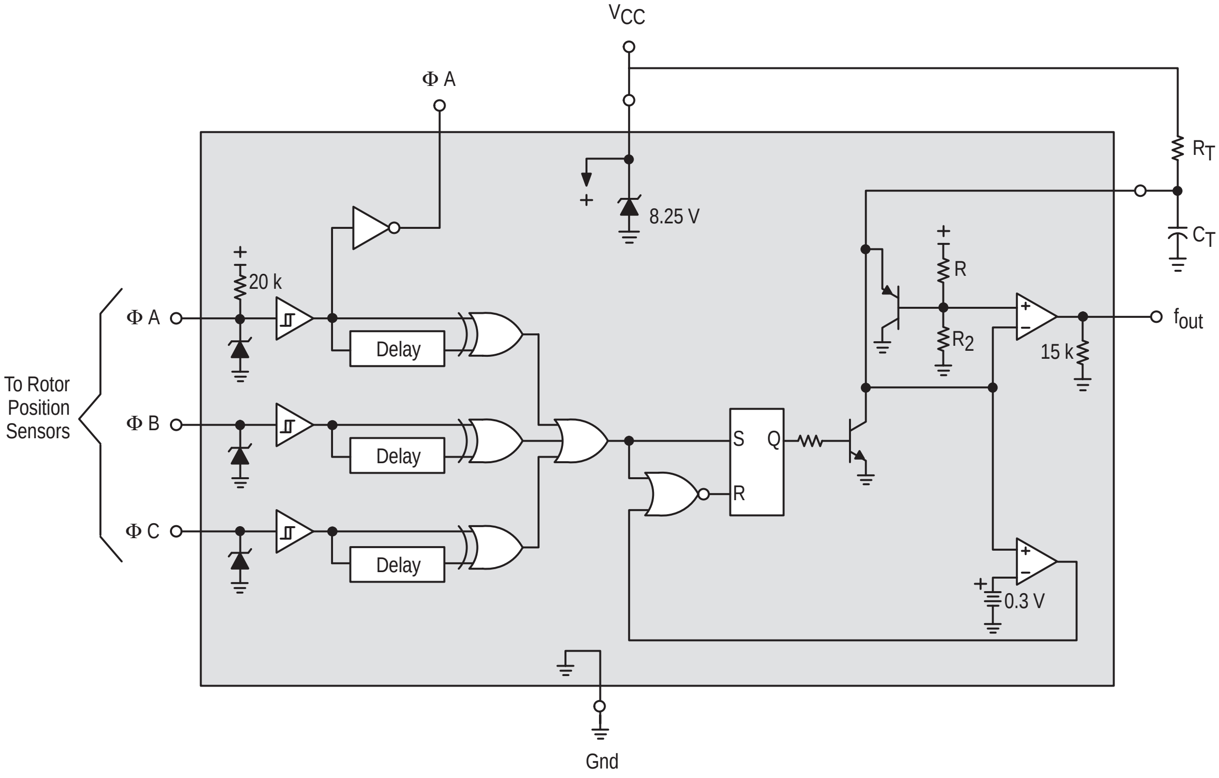


Closed Loop Brushless Motor Adapter

MC33039P, D

T_A = –40° to +85°C, Case 626, 751

The MC33039 is a high performance close loop speed control adapter specifically designed for use in brushless dc motor control systems. Implementation will allow precise speed regulation without the need for a magnetic or optical tachometer. These devices contain three input buffers each with hysteresis for noise immunity, three digital edge detectors, a programmable monostable, and an internal shunt regulator. Also included is an inverter output for use in systems that require conversion of sensor phasing. Although this device is primarily intended for use with the MC33033/35 brushless motor controllers, it can be used cost effectively in many other closed loop speed control applications.

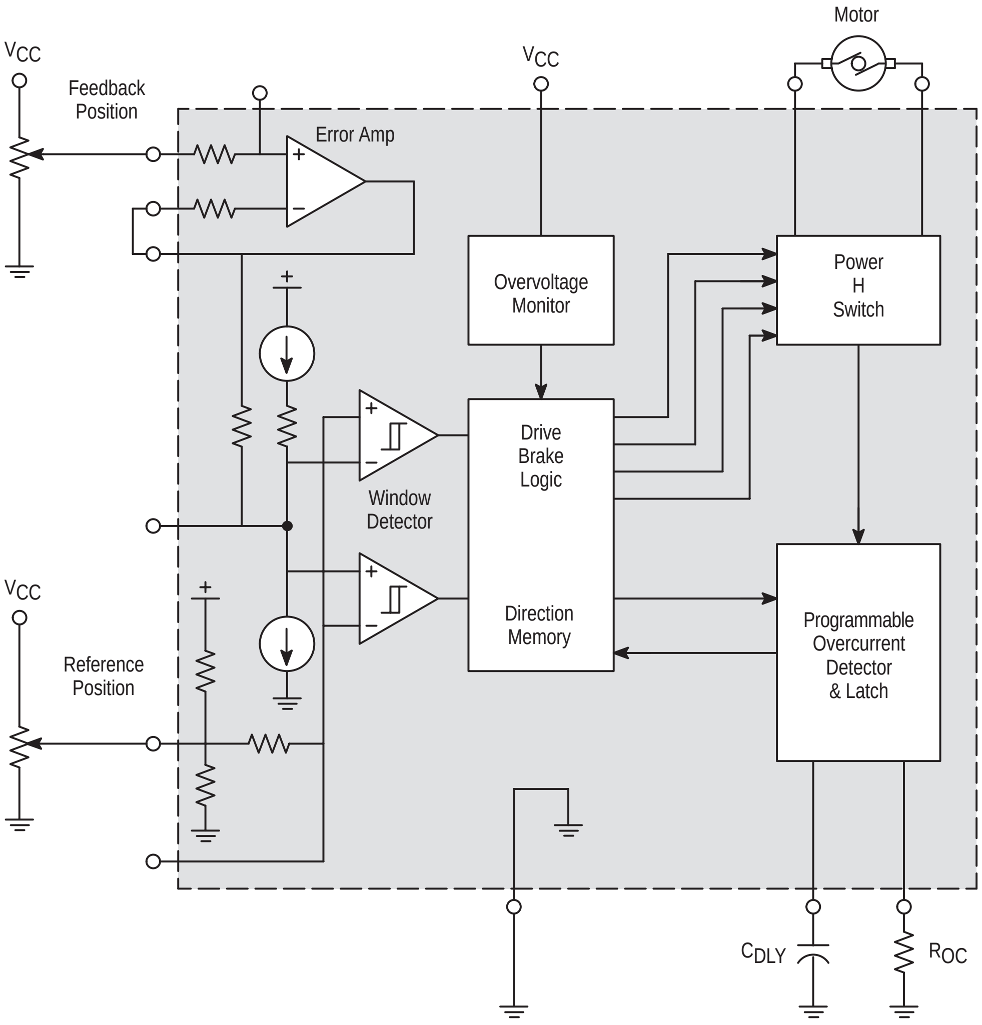


DC Servo Motor Controller/Driver

MC33030P, DW

T_A = –40° to +85°C, Case 648C, 751G

A monolithic dc servo motor controller providing all active functions necessary for a complete closed loop system. This device consists of an on–chip op amp and window comparator with wide input common mode range, drive and brake logic with direction memory, a power H switch driver capable of 1.0 A, independently programmable over current monitor and shutdown delay, and over voltage monitor. This part is ideally suited for almost any servo positioning application that requires sensing of temperature, pressure, light, magnetic flux, or any other means that can be converted to a voltage.



Stepper Motor Driver

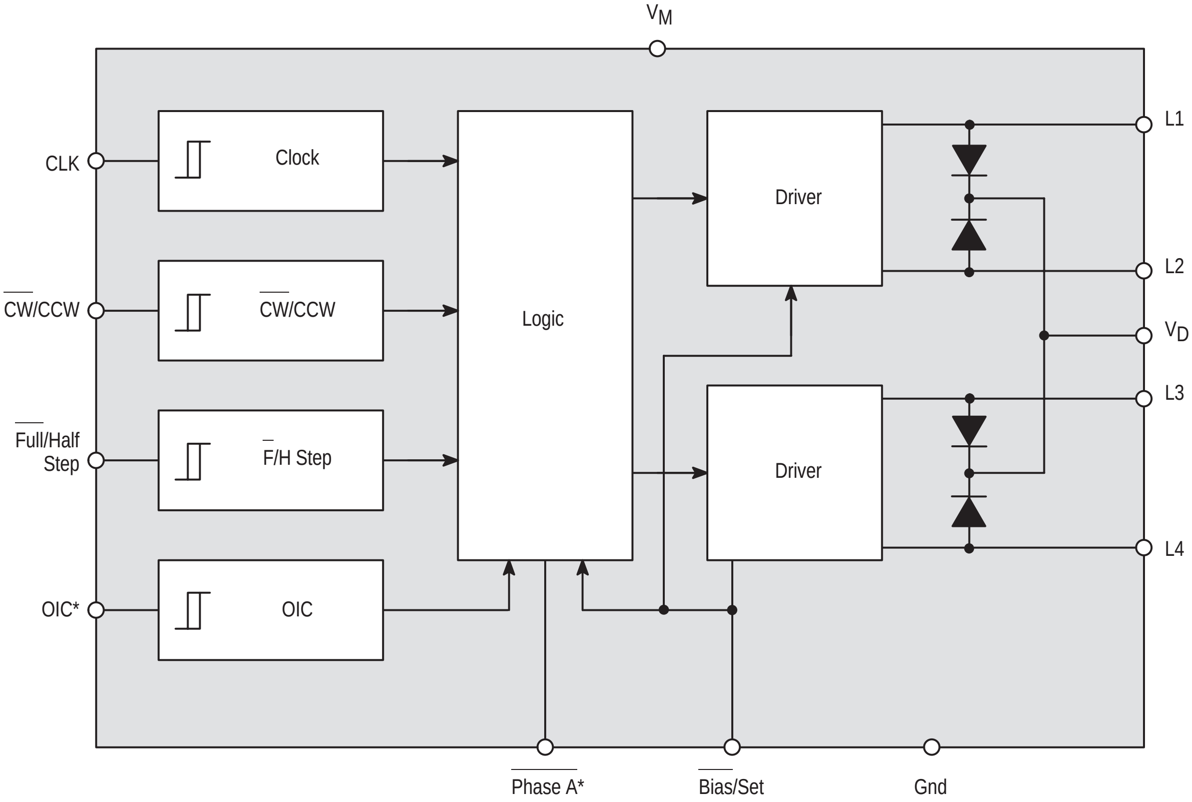
MC3479P, FN

T_A = 0° to +70°C, Case 648C, 775

SAA1042V

T_A = –30° to +125°C, Case 648C

These Stepper Motor Drivers provide up to 500 mA of drive per coil for two phase 6.0 V to 24 V stepper motors. Control logic is provided to accept commands for clockwise, counter clockwise and half or full step operation. The MC3479 has an added Output Impedance Control (OIC) and a Phase A drive state indicator (not available on SAA1042 devices).



* MC3479 Only

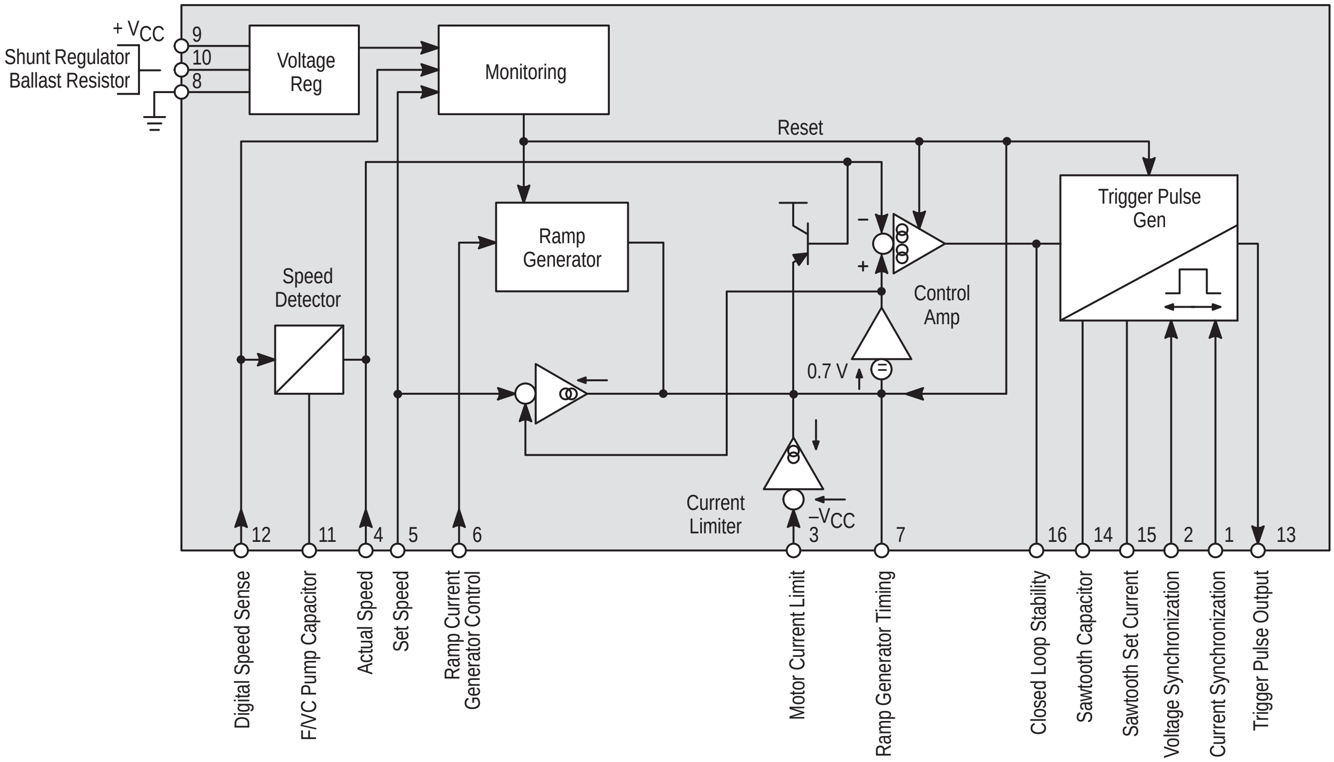
Universal Motor Speed Controller

TDA1085C, CD

T_A = –10° to +120°C, Case 648, 751B

The TDA1085C is a phase angle triac controller having all the necessary functions for universal motor speed control in washing machines. It operates in closed loop configuration and provides two ramp possibilities.

- On-Chip Frequency to Voltage Converter
- On-Chip Ramps Generator
- Soft Start
- Load Current Limitation
- Tachogenerator Circuit Sensing
- Direct Supply from AC Line
- Security Functions Peformed by Monitor



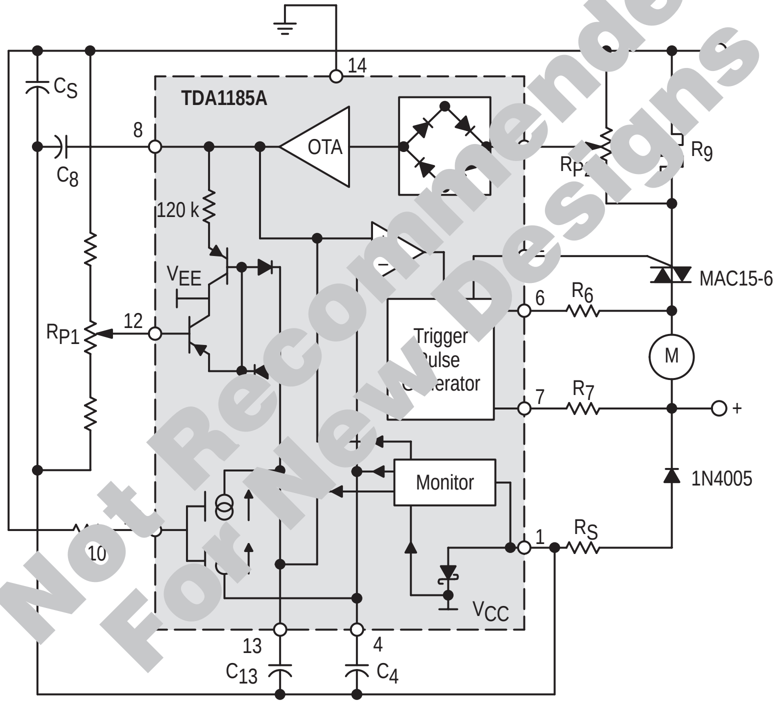
Triac Phase Angle Controller

TDA1185A

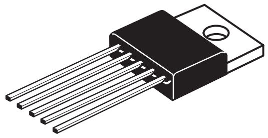
T_A = 0° to +70°C, Case 646

This device generates controlled triac triggering pulses and allows tachless speed stabilization of universal motors by an integrated positive feedback function.

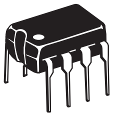
- Low Cost External Components Count
- Optimum Triac Firing (2nd and 3rd Quadrants)
- Repetitive Trigger Pulses when Triac Current is Interrupted by Motor Brush Bounce
- Triac Current Sensed to Allow Inductive Loads
- Soft–Start
- Power Failure Detection and General Circuit Reset
- Low Power Consumption: 1.0 mA



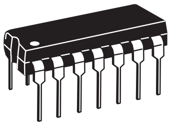
Power/Motor Control Circuits Package Overview



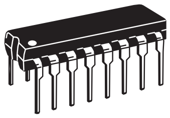
CASE 314D
T SUFFIX



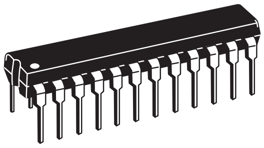
CASE 626
B, P SUFFIX



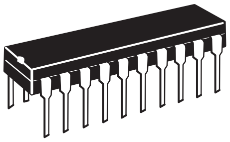
CASE 646



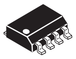
CASE 648, 648C
P, V SUFFIX



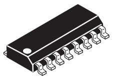
CASE 724
P SUFFIX



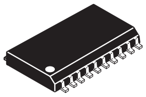
CASE 738
P SUFFIX



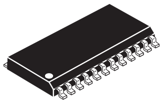
CASE 751
D SUFFIX



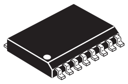
CASE 751B
D SUFFIX



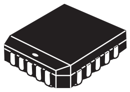
CASE 751D
DW SUFFIX



CASE 751E
DW SUFFIX



CASE 751G
DW SUFFIX



CASE 775
FN SUFFIX

Device Listing

Power Controller

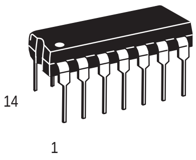
Motor Controllers

NOTE: * Not recommended for new designs.

CA3059

ZERO VOLTAGE SWITCH

SEMICONDUCTOR TECHNICAL DATA



PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

Device	Operating Temperature Range	Package
CA3059	T_A = – 40° to +85°C	Plastic DIP

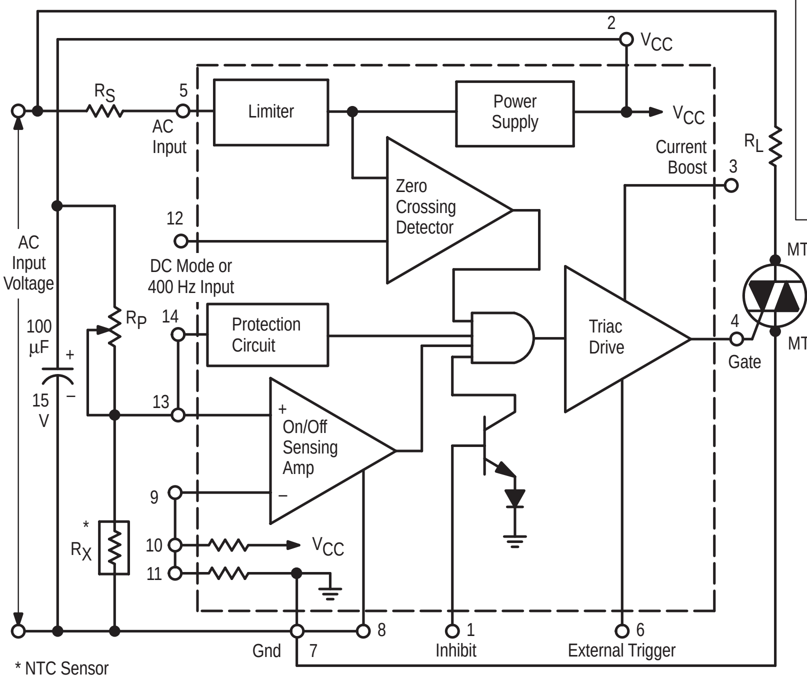
Zero Voltage Switch

This series is designed for thyristor control in a variety of AC power switching applications for AC input voltages of 24 V, 120 V, 208/230 V, and 277 V @ 50/60 Hz.

Applications:

- Relay Control
- Heater Control
- Valve Control
- Lamp Control
- On–Off Motor Switching
- Differential Comparator with Self–Contained Power Supply for Industrial Applications
- Synchronous Switching of Flashing Lights

Figure 1. Representative Block Diagram



AC Input Voltage (50/60 Hz) Vac	Input Series Resistor (R_S) kΩ	Dissipation Rating for R_S W
24	2.0	0.5
120	10	2.0
208/230	20	4.0
277	25	5.0

FUNCTIONAL BLOCK DESCRIPTION

1. **Limiter–Power Supply** — Allows operation of the CA3059 directly from an AC line. Suggested dropping resistor (R_S) values are given in the table below.
2. **Differential On/Off Sensing Amplifier** — Tests for condition of external sensors or input command signals. Proportional control capability or hysteresis may be implemented using this block.
3. **Zero–Crossing Detector** — Synchronizes the output pulses to the zero voltage point of the AC cycle. This synchronization eliminates RFI when used with resistive loads.
4. **Triac Drive** — Supplies high–current pulses to the external power controlling thyristor.
5. **Protection Circuit** — A built–in circuit may be actuated, if the sensor opens or shorts, to remove the drive current from the external triac.
6. **Inhibit Capability** — Thyristor firing may be inhibited by the action of an internal diode gate at Pin 1.
7. **High Power DC Comparator Operation** — Operation in this mode is accomplished by connecting Pin 7 to Pin 12 (thus overriding the action of the zero–crossing detector). When Pin 13 is positive with respect to Pin 9, current to the thyristor is continuous.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
DC Supply Voltage (Between Pins 2 and 7)	V_{CC}	12	Vdc
DC Supply Voltage (Between Pins 2 and 8)	V_{CC}	12	Vdc
Peak Supply Current (Pins 5 and 7)	$I_{5,7}$	± 50	mA
Fail–Safe Input Current (Pin 14)	I_{14}	2.0	mA
Output Pulse Current (Pin 4) (Note 1)	I_{out}	150	mA
Junction Temperature	T_J	150	°C
Operating Temperature Range	T_A	– 40 to + 85	°C
Storage Temperature Range	T_{stg}	– 65 to + 150	°C

ELECTRICAL CHARACTERISTICS (Operation @ 120 Vrms, 50–60 Hz, T_A = 25°C [Note 2])

Characteristic	Figure	Symbol	Min	Typ	Max	Unit
DC Supply Voltage	2	V_S				Vdc
Inhibit Mode						
R_S = 10 k, I_L = 0			6.1	6.5	7.0	
R_S = 5.0 k, I_L = 2.0 mA			—	6.1	—	
Pulse Mode						
R_S = 10 k, I_L = 0			6.0	6.4	7.0	
R_S = 5.0 k, R_L = 2.0 mA			—	6.2	—	
Gate Trigger Current (V_{GT} = 1.0 V, Pins 3 and 2 connected)	3	I_{GT}	—	160	—	mA
Peak Output Current, Pulsed	3	I_{OM}				mA
With Internal Power Supply, V_{GT} = 0						
Pin 3 Open			50	125	—	
Pins 3 and 2 Connected			90	190	—	
With External Power Supply, V_{CC} = 12 V, V_{GT} = 0	4					
Pin 3 Open			—	230	—	
Pins 3 and 2 Connected			—	300	—	
Inhibit Input Ratio (Ratio of Voltage @ Pin 9 to Pin 2)	5	V_9/V_2	0.465	0.485	0.520	—
Total Gate Pulse Duration (C_{Ext} = 0)	6					µs
Positive dv/dt		t_p	70	100	140	
Negative dv/dt		t_n	70	100	140	
Pulse Duration After Zero Crossing (C_{Ext} = 0, R_{Ext} = ∞)	6					µs
Positive dv/dt		t_{p1}	—	50	—	
Negative dv/dt		t_{n1}	—	60	—	
Output Leakage Current Inhibit Mode (Note 3)	3	I_4	—	0.001	10	µA
Input Bias Current	7	I_{IB}	—	0.15	1.0	µA
Common Mode Input Voltage Range (Pins 9 and 13 Connected)	—	V_{CMR}	—	1.4 to 5.0	—	Vdc
Inhibit Input Voltage	8	V_1	—	1.4	1.6	Vdc
External Trigger Voltage	—	$V_6 – V_4$	—	1.4	—	Vdc

NOTES: 1. Care must be taken, especially when using an external power supply, that total package dissipation is not exceeded.
2. The values given in the Electrical Characteristics Table at 120 V also apply for operation at input voltages of 24 V, 208/230 V, and 277 V, except for Pulse Duration test. However, the series resistor (R_S) must have the indicated value, shown in Table A for the specified input voltage.
3. I_4 out of Pin 4, 2.0 V on Pin 1, S_1 position 2.

TEST CIRCUITS

(All resistor values are in ohms)

Figure 2. DC Supply Voltage

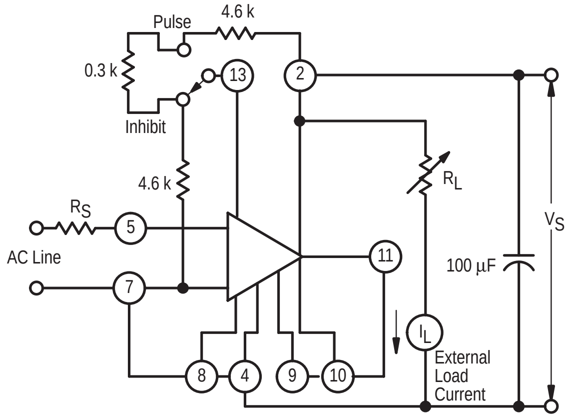


Figure 3. Peak Output (Pulsed) and Gate Trigger Current with Internal Power Supply

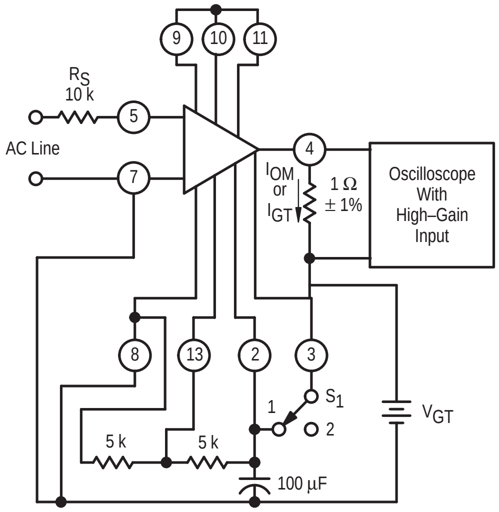


Figure 4. Peak Output Current (Pulsed) with External Power Supply

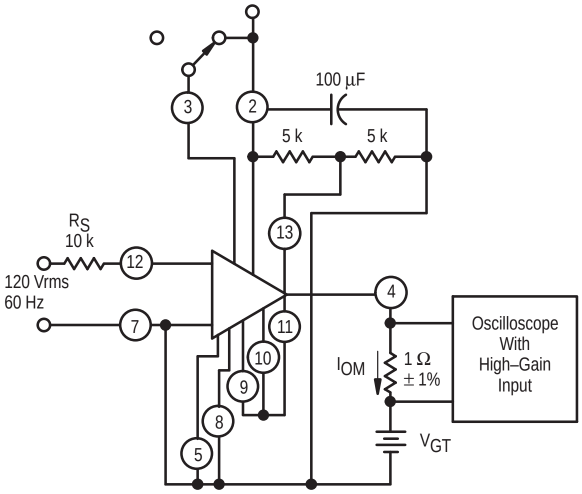


Figure 5. Input Inhibit Ratio

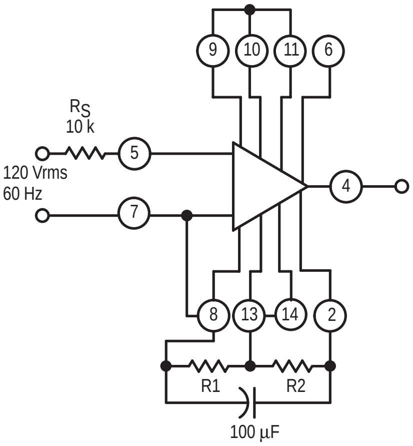


Figure 6. Gate Pulse Duration Test Circuit with Associated Waveform

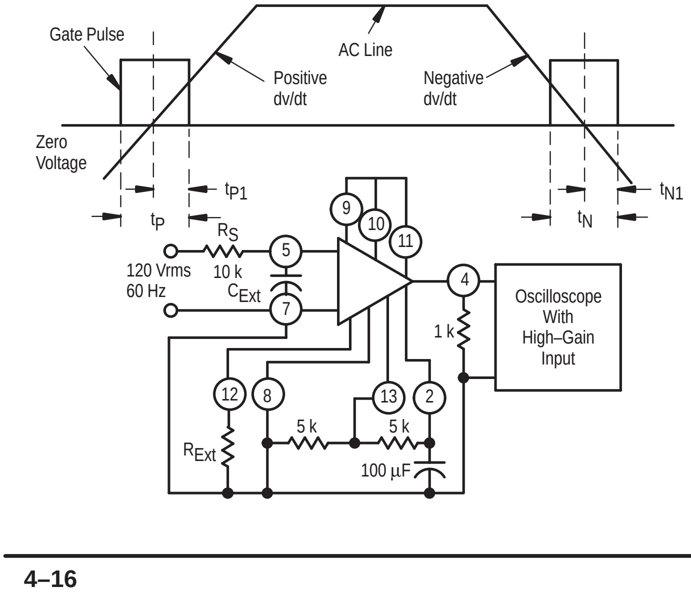
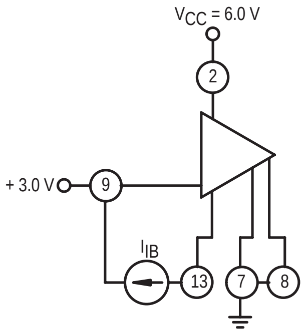


Figure 7. Input Bias Current Test Circuit



TYPICAL CHARACTERISTICS

Figure 8. Inhibit Input Voltage Test

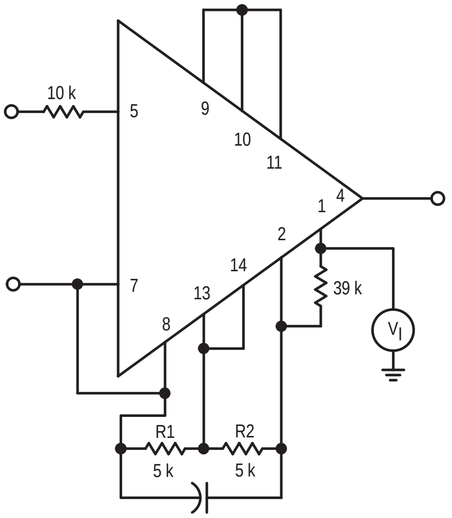


Figure 9. Peak Output Current (Pulsed) versus External Power Supply Voltage

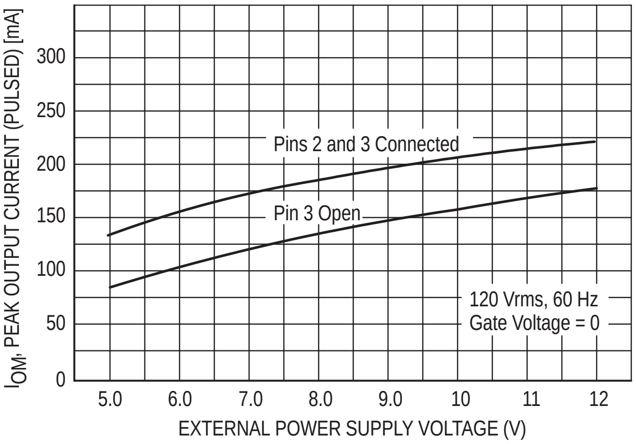


Figure 10. Peak Output Current (Pulsed) versus Ambient Temperature

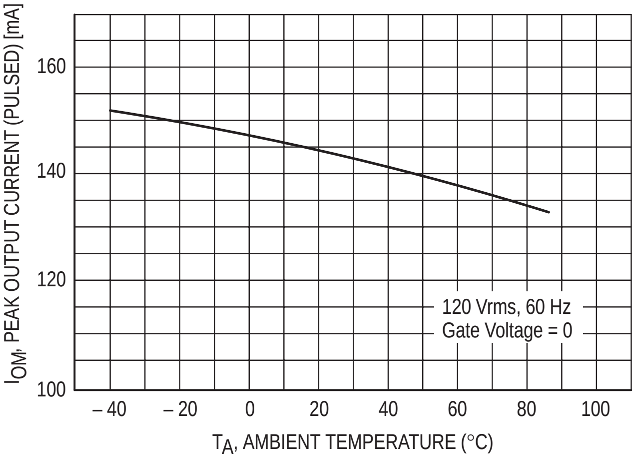


Figure 11. Total Pulse Width versus Ambient Temperature

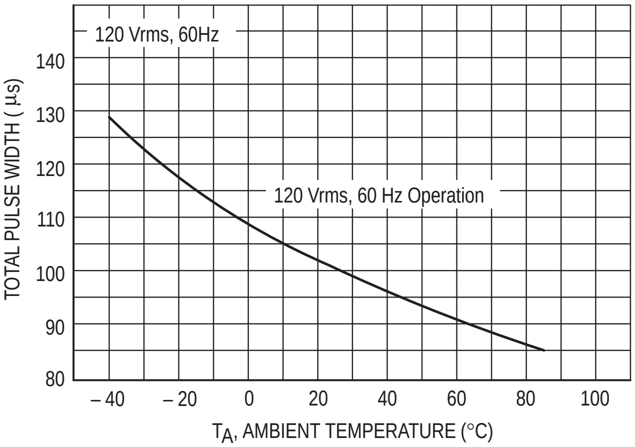


Figure 12. Internal Supply versus Ambient Temperature

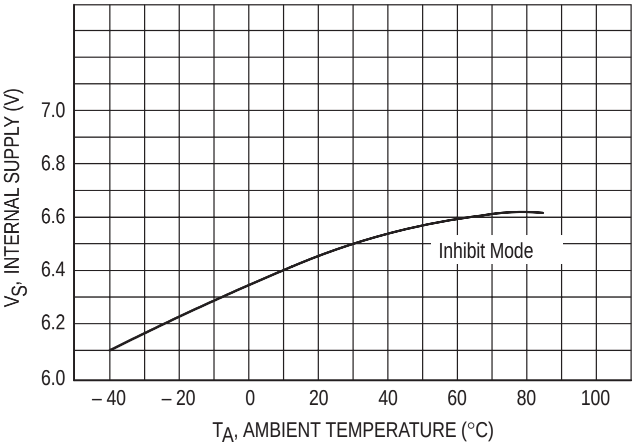


Figure 13. Inhibit Voltage Ratio versus Ambient Temperature

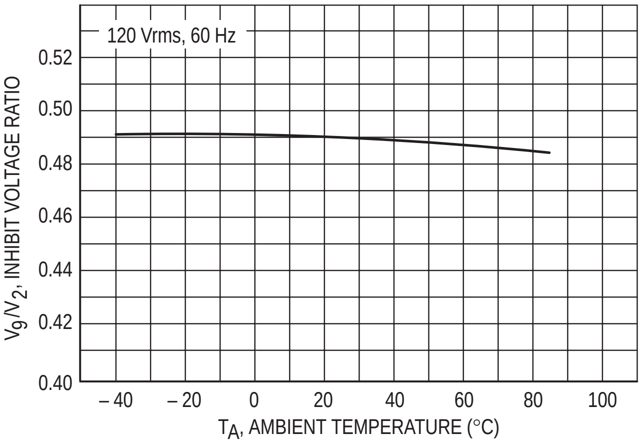
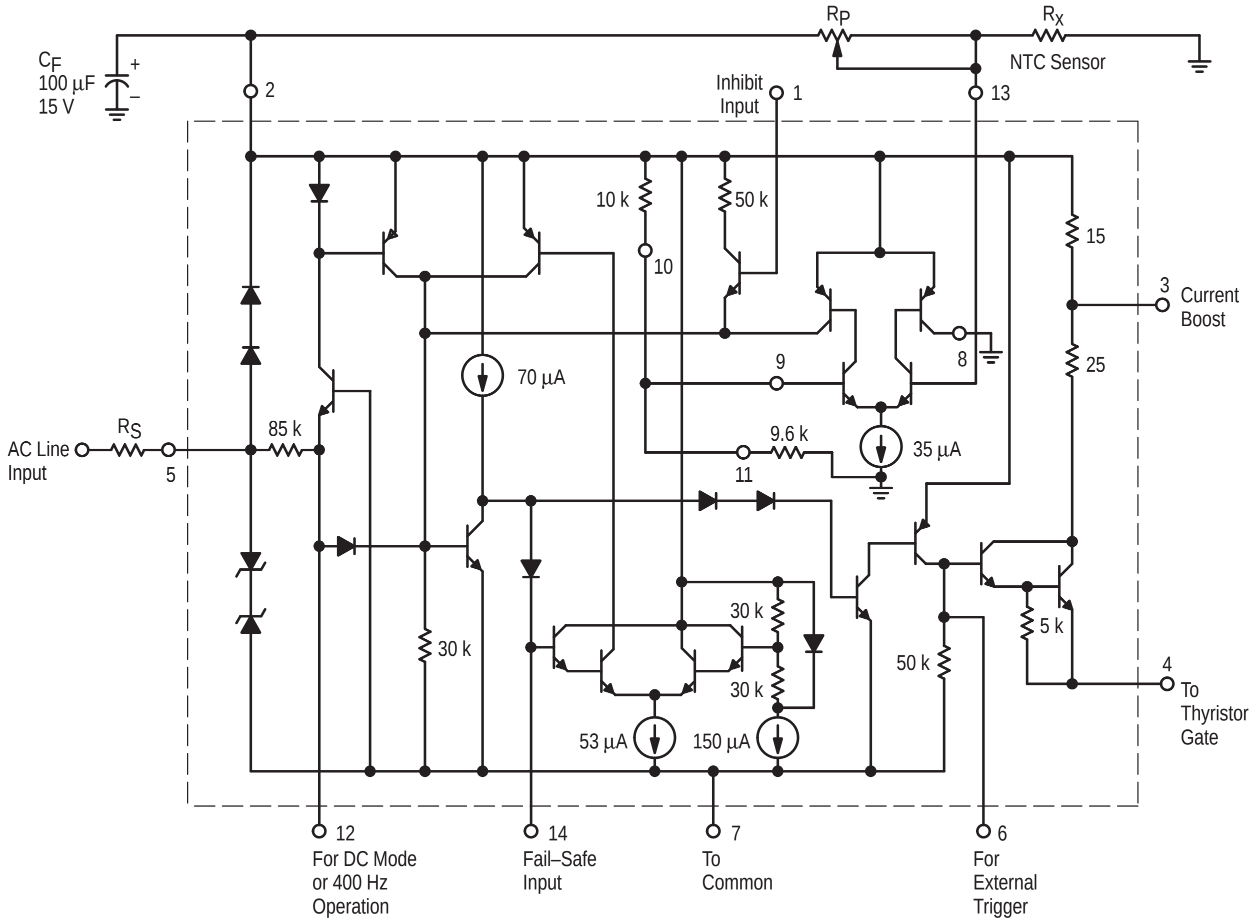


Figure 14. Circuit Schematic



NOTE: Current sources are established by an internal reference.

APPLICATION INFORMATION

Power Supply

The CA3059 is a self–powered circuit, powered from the AC line through an appropriate dropping resistor (see Table A). The internal supply is designed to power the auxiliary power circuits.

In applications where more output current from the internal supply is required, an external power supply of higher voltage should be used. To use an external power supply, connect Pin 5 and Pin 7 together and apply the synchronizing voltage to Pin 12 and the DC supply voltage to Pin 2 as shown in Figure 4.

Operation of Protection Circuit

The protection circuit, when connected, will remove current drive from the triac if an open or shorted sensor is detected. This circuit is activated by connecting Pin 13 to Pin 14 (see Figure 1).

The following conditions should be observed when the protection circuit is utilized:

a. The internal supply should be used and the external load current must be limited to 2 mA with a 5 kΩ dropping resistor.

b. Sensor Resistance (R_X) and R_P values should be between 2 kΩ and 100 kΩ.

c. The relationship $0.33 < R_X/R_P < 3$ must be met over the anticipated temperature range to prevent undesired activation of the circuit. A shunt or series resistor may have to be added.

External Inhibit Function

A priority inhibit command applied to Pin 1 will remove current drive from the thyristor. A command of at least +1.2 V @ 10 µA is required. A DTL or TTL logic 1 applied to Pin 1 will activate the inhibit function.

DC Gate Current Mode

When comparator operation is desired or inductive loads are being switched, Pins 7 and 12 should be connected. This connection disables the zero–crossing detector to permit the flow of gate current from the differential sensing amplifier on demand. Care should be exercised to avoid possible overloading of the internal power supply when operating the device in this mode. A resistor should be inserted between Pin 4 and the thyristor gate in order to limit the current.

MOTOROLA

MC3479

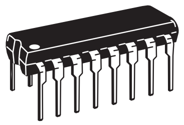
Stepper Motor Driver

STEPPER MOTOR DRIVER

SEMICONDUCTOR TECHNICAL DATA

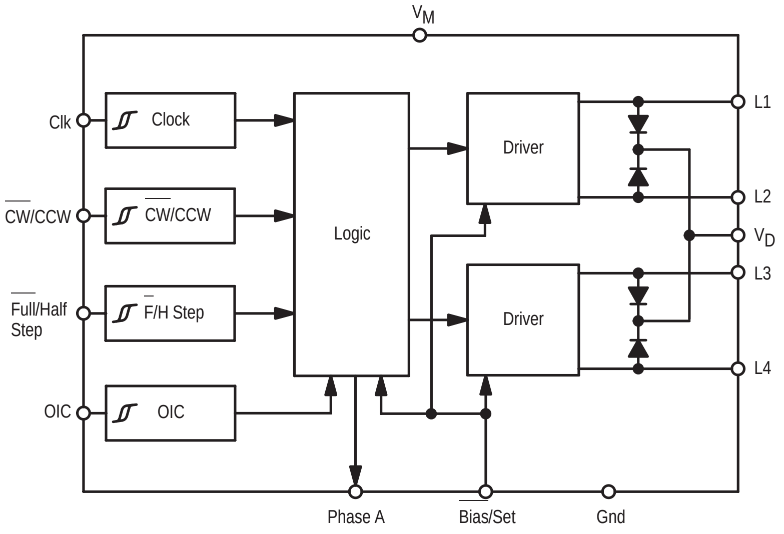
The MC3479 is designed to drive a two–phase stepper motor in the bipolar mode. The circuit consists of four input sections, a logic decoding/sequencing section, two driver–stages for the motor coils, and an output to indicate the Phase A drive state.

- Single Supply Operation: 7.2 to 16.5 V
- 350 mA/Coil Drive Capability
- Clamp Diodes Provided for Back–EMF Suppression
- Selectable CW/CCW and Full/Half Step Operation
- Selectable High/Low Output Impedance (Half Step Mode)
- TTL/CMOS Compatible Inputs
- Input Hysteresis: 400 mV Minimum
- Phase Logic Can Be Initialized to Phase A
- Phase A Output Drive State Indication (Open–Collector)
- Available in Standard DIP and Surface Mount

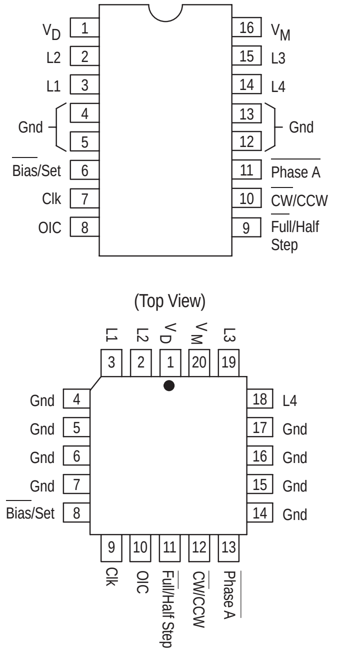


P SUFFIX
PLASTIC PACKAGE
CASE 648C

Figure 1. Representative Block Diagram



PIN CONNECTIONS



ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC3479P	T_A = 0° to +70°C	Plastic

INPUT TRUTH TABLE

	Input Low	Input High
$\overline{\text{CW}}$/CCW	CW	CCW
$\overline{\text{Full}}$/Half Step	Full Step	Half Step
OIC	Hi Z	Low Z
Clk	Positive Edge Triggered	

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_M	+ 18	Vdc
Clamp Diode Cathode Voltage (Pin 1)	V_D	$V_M + 5.0$	Vdc
Driver Output Voltage	V_{OD}	$V_M + 6.0$	Vdc
Drive Output Current/Coil	I_{OD}	± 500	mA
Input Voltage (Logic Controls)	V_{in}	– 0.5 to + 7.0	Vdc
$\overline{\text{Bias}}$/Set Current	I_{BS}	– 10	mA
$\overline{\text{Phase A}}$ Output Voltage	V_{OA}	+ 18	Vdc
$\overline{\text{Phase A}}$ Sink Current	I_{OA}	20	mA
Junction Temperature	T_J	+ 150	°C
Storage Temperature Range	T_{stg}	– 65 to + 150	°C

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Min	Max	Unit
Supply Voltage	V_M	+ 7.2	+ 16.5	Vdc
Clamp Diode Cathode Voltage	V_D	V_M	$V_M + 4.5$	Vdc
Driver Output Current (Per Coil) (Note 1)	I_{OD}	—	350	mA
Input Voltage (Logic Controls)	V_{in}	0	+ 5.5	Vdc
$\overline{\text{Bias}}$/Set Current (Outputs Active)	I_{BS}	– 300	– 75	µA
$\overline{\text{Phase A}}$ Output Voltage	V_{OA}	—	V_M	Vdc
$\overline{\text{Phase A}}$ Sink Current	I_{OA}	0	8.0	mA
Operating Ambient Temperature	T_A	0	+ 70	°C

NOTE: 1. See section on Power Dissipation in Application Information.

DC ELECTRICAL CHARACTERISTICS (Specifications apply over the recommended supply voltage and temperature range, [Notes 2, 3] unless otherwise noted.)

Characteristic	Pins	Symbol	Min	Typ	Max	Unit
INPUT LOGIC LEVELS						
Threshold Voltage (Low–to–High)	7, 8, 9, 10	V_{TLH}	—	—	2.0	Vdc
Threshold Voltage (High–to–Low)		V_{THL}	0.8	—	—	Vdc
Hysteresis		V_{HYS}	0.4	—	—	Vdc
Current: ($V_I = 0.4$ V) ($V_I = 5.5$ V) ($V_I = 2.7$ V)		I_{IL}	– 100 — —	— — —	— + 100 + 20	µA
DRIVER OUTPUT LEVELS						
Output High Voltage ($I_{BS} = -300$ µA): ($I_{OD} = -350$ mA) ($I_{OD} = -0.1$ mA)	2, 3, 14, 15	V_{OHD}	 $V_M - 2.0$ $V_M - 1.2$	 — —	 — —	Vdc
Output Low Voltage ($I_{BS} = -300$ µA, $I_{OD} = 350$ mA)		V_{OLD}	—	—	0.8	Vdc
Differential Mode Output Voltage Difference (Note 4) ($I_{BS} = -300$ µA, $I_{OD} = 350$ mA)		DV_{OD}	—	—	0.15	Vdc
Common Mode Output Voltage Difference (Note 5) ($I_{BS} = -300$ µA, $I_{OD} = -0.1$ mA)		CV_{OD}	—	—	0.15	Vdc
Output Leakage, Hi Z State ($0 \leqslant V_{OD} \leqslant V_M$, $I_{BS} = -5.0$ µA) ($0 \leqslant V_{OD} \leqslant V_M$, $I_{BS} = -300$ µA, F/H = 2.0 V, OIC = 0.8 V)		 I_{OZ1} I_{OZ2}	 – 100 – 100	 — —	 + 100 + 100	µA

NOTES: 2. Algebraic convention rather than absolute values is used to designate limit values.
3. Current into a pin is designated as positive. Current out of a pin is designated as negative.
4. $DV_{OD} = |V_{OD1,2} - V_{OD3,4}|$ where: $V_{OD1,2} = (V_{OHD1} - V_{OLD2})$ or $(V_{OHD2} - V_{OLD1})$, and
$V_{OD3,4} = (V_{OHD3} - V_{OLD4})$ or $(V_{OHD4} - V_{OLD3})$.
5. $CV_{OD} = |V_{OHD1} - V_{OHD2}|$ or $|V_{OHD3} - V_{OHD4}|$.

DC ELECTRICAL CHARACTERISTICS (Specifications apply over the recommended supply voltage and temperature range, [Notes 2, 3] unless otherwise noted.)

Characteristic	Pins	Symbol	Min	Typ	Max	Unit
CLAMP DIODES						
Forward Voltage (I_D = 350 mA)	1, 2, 3, 14, 15	V_{DF}	—	2.5	3.0	Vdc
Leakage Current (Per Diode) (Pin 1 = 21 V; Outputs = 0 V; I_{BS} = 0 µA)		I_{DR}	—	—	100	µA
$\overline{\text{PHASE A}}$ OUTPUT						
Output Low Voltage (I_{OA} = 8.0 mA)	11	V_{OLA}	—	—	0.4	Vdc
Off State Leakage Current (V_{OHA} = 16.5 V)		I_{OHA}	—	—	100	µA
POWER SUPPLY						
Power Supply Current (I_{OD} = 0 µA, I_{BS} = – 300 µA) (L1 = V_{OHD}, L2 = V_{OLD}, L3 = V_{OHD}, L4 = V_{OLD}) (L1 = V_{OHD}, L2 = V_{OLD}, L3 = Hi Z, L4 = Hi Z) (L1 = V_{OHD}, L2 = V_{OLD}, L3 = V_{OHD}, L4 = V_{OHD})	16	 I_{MW} I_{MZ} I_{MN}	 — — —	 — — —	 70 40 75	mA
$\overline{\text{BIAS}}$/SET CURRENT						
To Set $\overline{\text{Phase A}}$	6	I_{BS}	– 5.0	—	—	µA

PACKAGE THERMAL CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit
Thermal Resistance, Junction–to–Ambient (No Heatsink)	$R_{\theta JA}$	—	45	—	°C/W

AC SWITCHING CHARACTERISTICS (T_A = + 25°C, V_M = 12 V) (See Figures 2, 3, 4)

Characteristic	Pins	Symbol	Min	Typ	Max	Unit
Clock Frequency	7	f_{CK}	0	—	50	kHz
Clock Pulse Width (High)	7	PW_{CKH}	10	—	—	µs
Clock Pulse Width (Low)	7	PW_{CKL}	10	—	—	µs
$\overline{\text{Bias}}$/Set Pulse Width	6	PW_{BS}	10	—	—	µs
Setup Time ($\overline{\text{CW}}$/CCW and $\overline{\text{F}}$/HS)	10–7 9–7	t_{su}	5.0	—	—	µs
Hold Time ($\overline{\text{CW}}$/CCW and $\overline{\text{F}}$/HS)	10–7 9–7	t_h	10	—	—	µs
Propagation Delay (Clk–to–Driver Output)		t_{PCD}	—	8.0	—	µs
Propagation Delay ($\overline{\text{Bias}}$/Set–to–Driver Output)		t_{PBSD}	—	1.0	—	µs
Propagation Delay (Clk–to–$\overline{\text{Phase A}}$ Low)	7–11	t_{PHLA}	—	12	—	µs
Propagation Delay (Clk–to–$\overline{\text{Phase A}}$ High)	7–11	t_{PLHA}	—	5.0	—	µs

NOTES: 2. Algebraic convention rather than absolute values is used to designate limit values.
3. Current into a pin is designated as positive. Current out of a pin is designated as negative.

Figure 2. AC Test Circuit

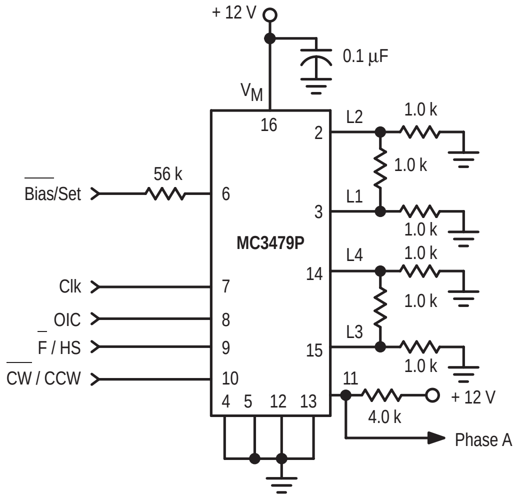
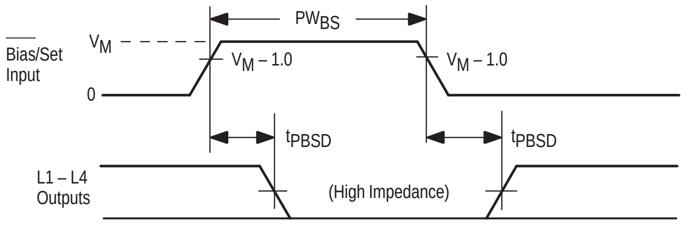


Figure 3. Bias/Set Timing (Refer to Figure 2)



Note: t_r, t_f (10% to 90%) for input signals are ⩽ 25 ns.

PIN FUNCTION DESCRIPTION

Pin No.		Function	Symbol	Description
20–Pin	16–Pin			
20	16	Power Supply	V_M	Power supply pin for both the logic circuit and the motor coil current. Voltage range is + 7.2 to + 16.5 volts.
4, 5, 6, 7, 14, 15, 16, 17	4, 5, 12, 13	Ground	Gnd	Ground pins for the logic circuit and the motor coil current. The physical configuration of the pins aids in dissipating heat from within the IC package.
1	1	Clamp Diode Voltage	V_D	This pin is used to protect the outputs where large voltage spikes may occur as the motor coils are switched. Typically a diode is connected between this pin and Pin 16. See Figure 11.
2, 3, 18, 19	2, 3, 14, 15	Driver Outputs	L1, L2 L3, L4	High current outputs for the motor coils. L1 and L2 are connected to one coil, and L3 and L4 to the other coil.
8	6	Bias/Set	B/S	This pin is typically 0.7 volts below V_M. The current out of this pin (through a resistor to ground) determines the maximum output sink current. If the pin is opened (I_{BS} < 5.0 µA) the outputs assume a high impedance condition, while the internal logic presets to a Phase A condition.
9	7	Clock	Clk	The positive edge of the clock input switches the outputs to the next position. This input has no effect if Pin 6 is open.
11	9	Full/Half Step	F/HS	When low (Logic “0”), each clock input pulse will cause the motor to rotate one full step. When high, each clock pulse will cause the motor to rotate one–half step. See Figure 7 for sequence.
12	10	Clockwise/ Counterclockwise	CW/CCW	This input allows reversing the rotation of the motor. See Figure 7 for sequence.
10	8	Output Impedance Control	OIC	This input is relevant only in the half step mode (Pin 9 > 2.0 V). When low (Logic “0”), the two driver outputs of the non–energized coil will be in a high impedance condition. When high the same driver outputs will be at a low impedance referenced to V_M. See Figure 7.
13	11	Phase A	Ph A	This open–collector output indicates (when low) that the driver outputs are in the Phase A condition (L1 = L3 = V_{OHD}, L2 = L4 = V_{OLD}).

APPLICATION INFORMATION

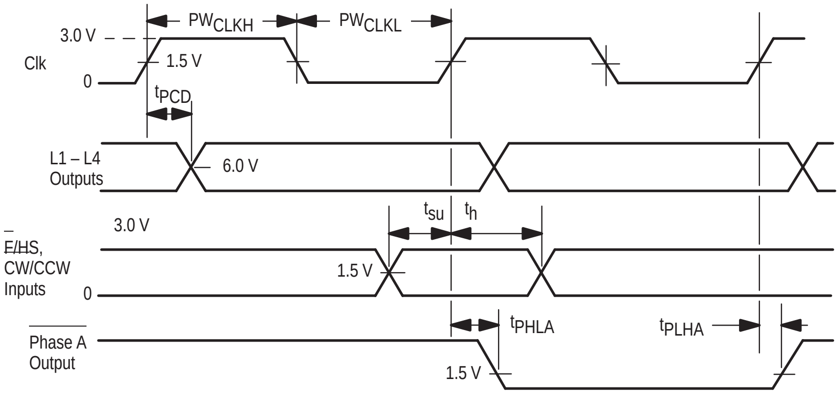
General

The MC3479 integrated circuit is designed to drive a stepper positioning motor in applications such as disk drives and robotics. The outputs can provide up to 350 mA to each of two coils of a two–phase motor. The outputs change state with each low–to–high transition of the clock input, with the new output state depending on the previous state, as well as the input conditions at the logic controls.

Outputs

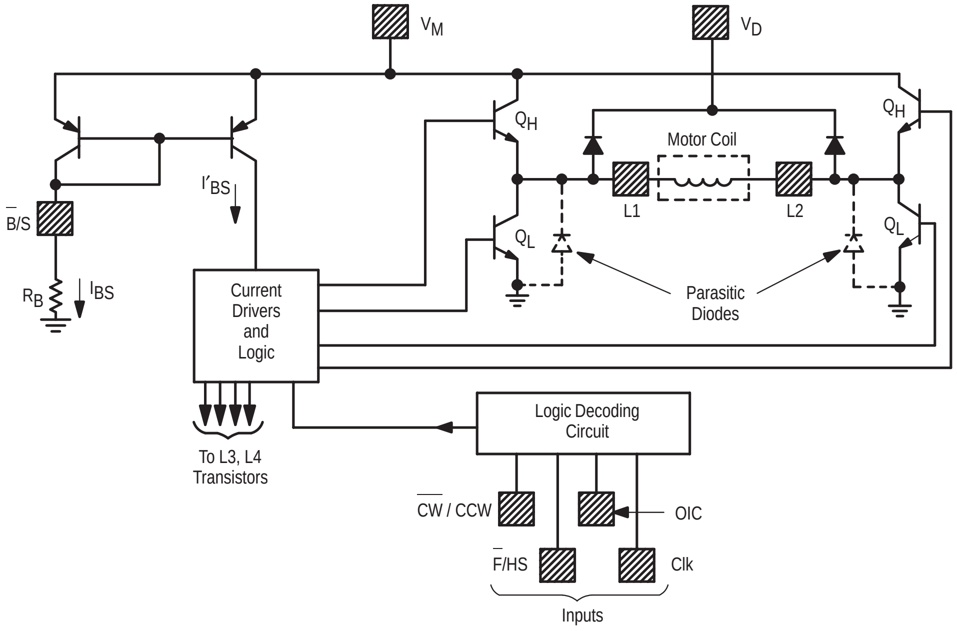
The outputs (L1–L4) are high current outputs (see Figure 5), which when connected to a two–phase motor, provide two full–bridge configurations (L3 and L4 are not shown in Figure 5). The polarities applied to the motor coils depend on which transistor (Q_H or Q_L) of each output is on, which in turn depends on the inputs and the decoding circuitry.

Figure 4. Clock Timing
(Refer to Figure 2)



Note: t_r, t_f (10% to 90%) for input signals are ≤ 10 ns.

Figure 5. Output Stages

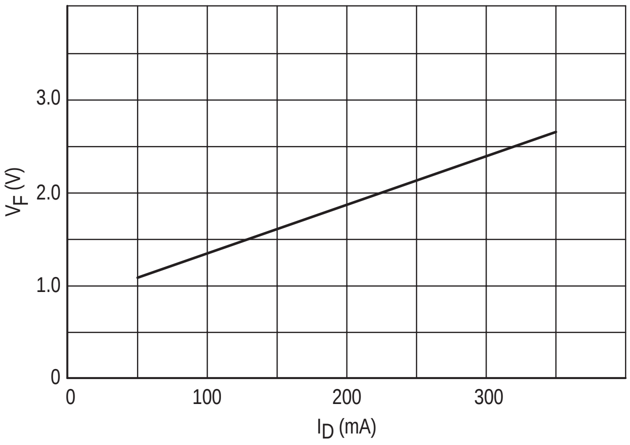


The maximum sink current available at the outputs is a function of the resistor connected between Pin 6 and ground (see section on Bias/Set operation). Whenever the outputs are to be in a high impedance state, both transistors (Q_H and Q_L of Figure 5) of each output are off.

V_D

This pin allows for provision of a current path for the motor coil current during switching, in order to suppress back–EMF voltage spikes. V_D is normally connected to V_M (Pin 16) through a diode (zener or regular), a resistor, or directly. The peaks instantaneous voltage at the outputs must not exceed V_M by more than 6.0 V. The voltage drop across the internal clamping diodes must be included in this portion of the design (see Figure 6). Note the parasitic diodes (Figure 5) across each Q_L of each output provide for a complete circuit path for the switched current.

Figure 6. Clamp Diode Characteristics



$\overline{\text{Full}}$/Half Step

When this input is at a Logic “0” (<0.8 V), the outputs change a full step with each clock cycle, with the sequence direction depending on the CW/CCW input. There are four steps (Phase A, B, C, D) for each complete cycle of the sequencing logic. Current flows through both motor coils during each step, as shown in Figure 7.

When taken to a Logic “1” (>2.0 V), the outputs change a half step with each clock cycle, with the sequence direction depending on the CW/CCW input. Eight steps (Phase A to H) result for each complete cycle of the sequencing logic. Phase A, C, E and G correspond (in polarity) to Phase A, B, C, and D, respectively, of the full step sequence. Phase B, D, F and H provide current to one motor coil, while de–energizing the other coil. The condition of the outputs of the de–energized coil depends on the OIC input, see Figure 7 timing diagram.

OIC

The output impedance control input determines the output impedance to the de–energized coil when operating in the half–step mode. When the outputs are in Phase B, D, F or H (Figure 7) and this input is at a Logic “0” (<0.8 V), the two outputs to the de–energized coil are in a high impedance condition — Q_L and Q_H of both outputs (Figure 5) are off. When this input is at a Logic “1” (>2.0 V), a low impedance output is provided to the de–energized coil as both outputs have Q_H on (Q_L off). To complete the low impedance path requires connecting V_D to V_M as described elsewhere in this data sheet.

$\overline{\text{Bias}}$/Set

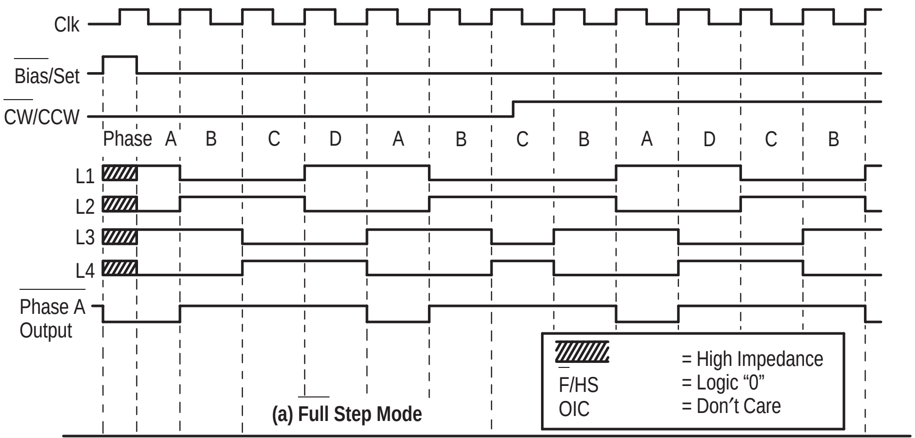
This pin can be used for three functions: a) determining the maximum output sink current; b) setting the internal logic to a known state; and c) reducing power consumption.

a) The maximum output sink current is determined by the base drive current supplied to the lower transistors (Q_Ls of Figure 5) of each output, which in turn, is a function of I_{BS}. The appropriate value of I_{BS} is determined by:

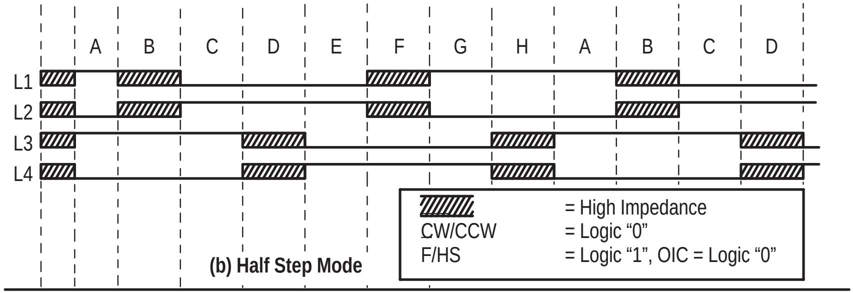
$$I_{BS} = I_{OD} \times 0.86$$

where I_{BS} is in microamps, and I_{OD} is the motor current/coil in milliamps.

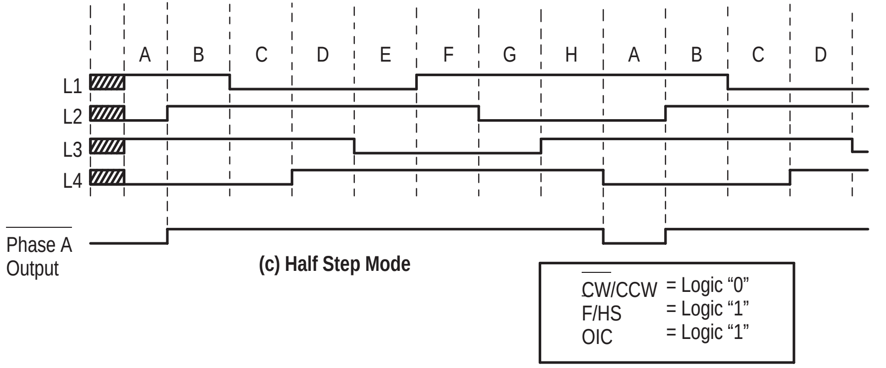
Figure 7. Output Sequence



(a) Full Step Mode



(b) Half Step Mode



(c) Half Step Mode

The value of R_B (between this pin and ground) is then determined by:

$$R_B = \frac{V_M - 0.7\ V}{I_{BS}}$$

b) When this pin is opened (raised to V_M) such that I_{BS} is <5.0 µA, the internal logic is set to the Phase A condition, and the four driver outputs are put into a high impedance state. The Phase A output (Pin 11) goes active (low), and input signals at the controls are ignored during this time. Upon re–establishing I_{BS}, the driver outputs become active, and will be in the Phase A position ($L1 = L3 = V_{OHD}$, $L2 = L4 = V_{OLD}$). The circuit will then respond to the inputs at the controls.

The Set function (opening this pin) can be used as a power–up reset while supply voltages are settling. A CMOS logic gate (powered by V_M) can be used to control this pin as shown in Figure 11.

c) Whenever the motor is not being stepped, power dissipation in the IC and in the motor may be lowered by reducing I_{BS}, so as to reduce the output (motor) current. Setting I_{BS} to 75 µA will reduce the motor current, but will not reset the internal logic as described above. See Figure 12 for a suggested circuit.

Power Dissipation

The power dissipated by the MC3479 must be such that the junction temperature (T_J) does not exceed 150°C. The power dissipated can be expressed as:

$$P = (V_M \times I_M) + (2 \times I_{OD}) [(V_M - V_{OHD}) + V_{OLD}]$$

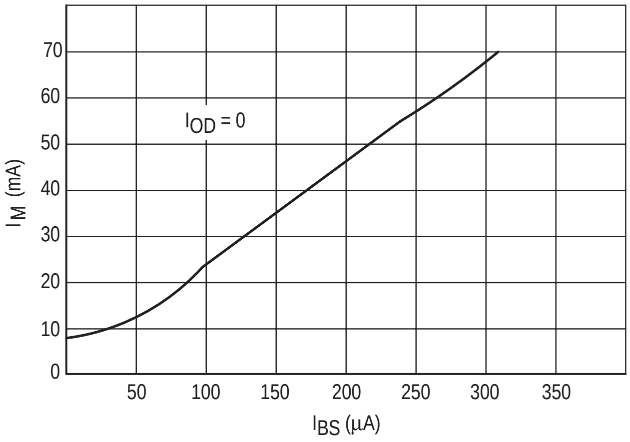
where V_M = Supply voltage;
I_M = Supply current other than I_{OD};
I_{OD} = Output current to each motor coil;
V_{OHD} = Driver output high voltage;
V_{OLD} = Driver output low voltage.

The power supply current (I_M) is obtained from Figure 8. After the power dissipation is calculated, the junction temperature can be calculated using:

$$T_J = (P \times R_{\theta JA}) + T_A$$

where $R_{\theta JA}$ = Junction–to–ambient thermal resistance (52°C/W for the DIP, 72°C/W for the FN Package);
T_A = Ambient Temperature.

Figure 8. Power Supply Current



For example, assume an application where V_M = 12 V, the motor requires 200 mA/coil, operating at room temperature with no heatsink on the IC. I_{BS} is calculated:

$$I_{BS} = 200 \times 0.86$$
$$I_{BS} = 172\ \mu A$$

R_B is calculated:

$$R_B = (12 - 0.7)\ V/172\ \mu A$$
$$R_B = 65.7\ k\Omega$$

From Figure 8, I_M (max) is determined to be 40 mA. From Figure 9, V_{OLD} is 0.46 volts, and from Figure 10, ($V_M - V_{OHD}$) is 1.4 volts.

$$P = (12 \times 0.040) + (2 \times 0.2)(1.4 + 0.46)$$
$$P = 1.22\ W$$
$$T_J = (1.22\ W \times 52°C/W) + 25°C$$
$$T_J = 88°C$$

This temperature is well below the maximum limit. If the calculated T_J had been higher than 150°C, a heatsink such as the Staver Co. V–7 Series, Aavid #5802, or Thermalloy #6012 could be used to reduce $R_{\theta JA}$. In extreme cases, forced air cooling should be considered.

The above calculation, and $R_{\theta JA}$, assumes that a ground plane is provided under the MC3479 (either or both sides of the PC board) to aid in the heat dissipation. Single nominal width traces leading from the four ground pins should be avoided as this will increase T_J, as well as provide potentially disruptive ground noise and IR drops when switching the motor current.

Figure 9. Maximum Saturation Voltage — Driver Output Low

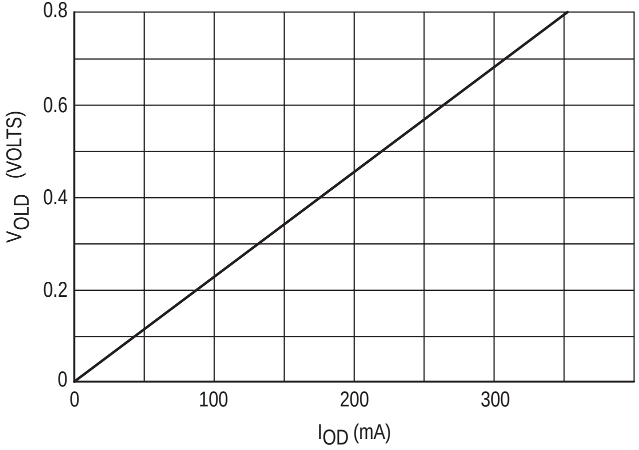


Figure 10. Maximum Saturation Voltage — Driver Output High

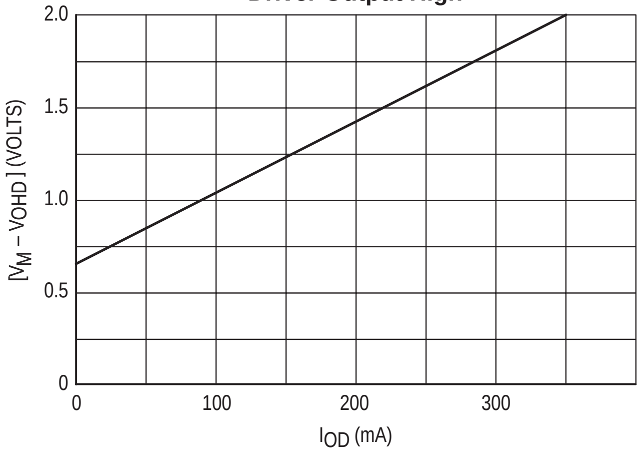


Figure 11. Typical Applications Circuit

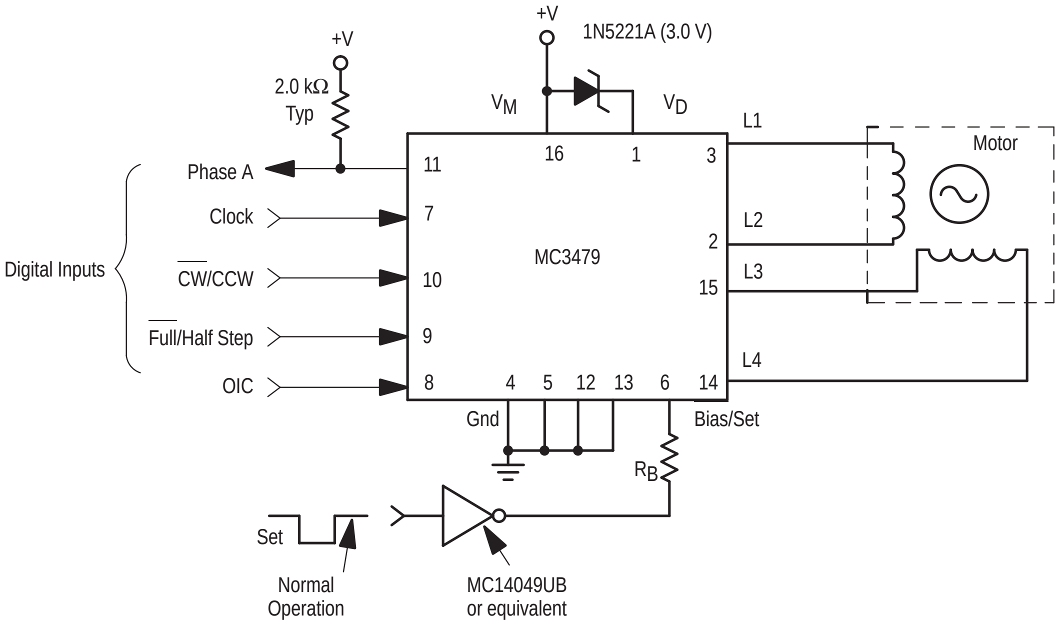
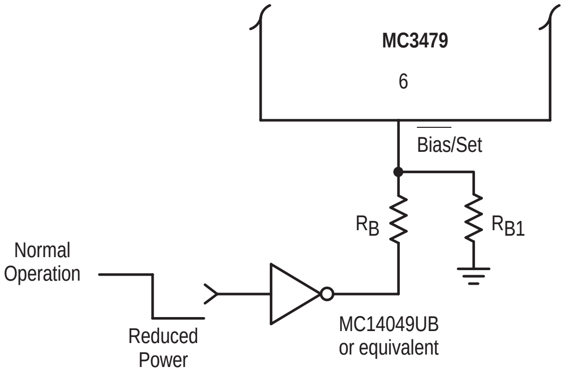


Figure 12. Power Reduction



— Suggested value for R_{B1} (V_M = 12 V) is 150 kΩ.
— R_B calculation (see text) must take into account
the current through R_{B1}.

MOTOROLA

MC33030

DC Servo Motor Controller/Driver

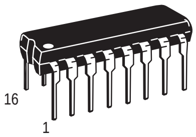
DC SERVO MOTOR CONTROLLER/DRIVER

SEMICONDUCTOR TECHNICAL DATA

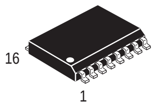
The MC33030 is a monolithic DC servo motor controller providing all active functions necessary for a complete closed loop system. This device consists of an on–chip op amp and window comparator with wide input common–mode range, drive and brake logic with direction memory, Power H–Switch driver capable of 1.0 A, independently programmable over–current monitor and shutdown delay, and over–voltage monitor. This part is ideally suited for almost any servo positioning application that requires sensing of temperature, pressure, light, magnetic flux, or any other means that can be converted to a voltage.

Although this device is primarily intended for servo applications, it can be used as a switchmode motor controller.

- On–Chip Error Amp for Feedback Monitoring
- Window Detector with Deadband and Self Centering Reference Input
- Drive/Brake Logic with Direction Memory
- 1.0 A Power H–Switch
- Programmable Over–Current Detector
- Programmable Over–Current Shutdown Delay
- Over–Voltage Shutdown

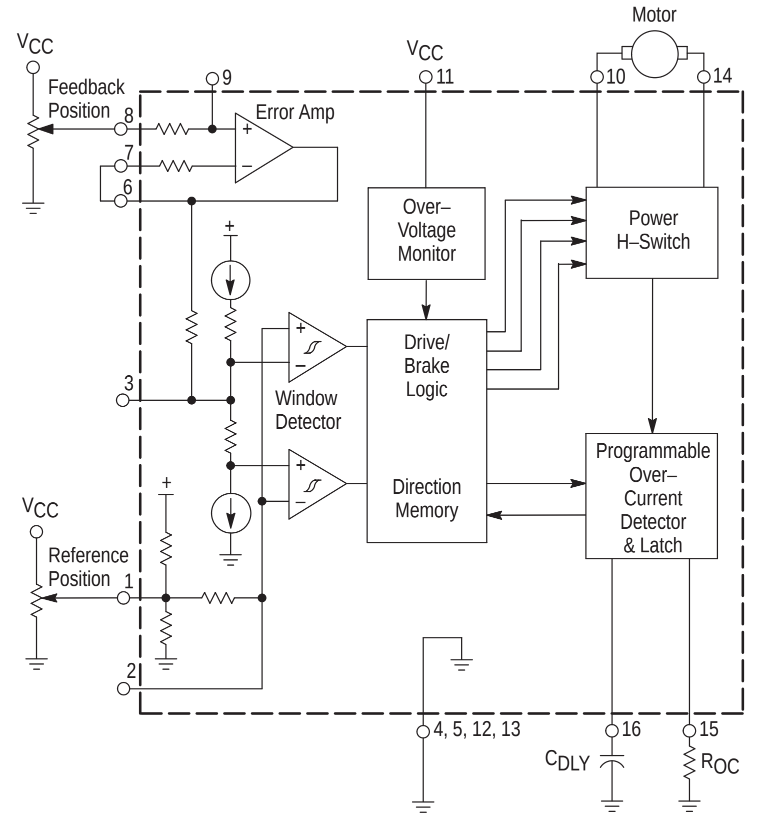


P SUFFIX
PLASTIC PACKAGE
CASE 648C
(DIP–16)



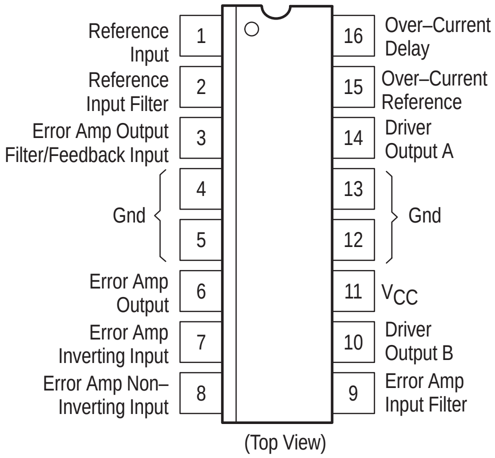
DW SUFFIX
PLASTIC PACKAGE
CASE 751G
(SOP–16L)

Representative Block Diagram



This device contains 119 active transistors.

PIN CONNECTIONS



Pins 4, 5, 12 and 13 are electrical ground and heat sink pins for IC.

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC33030DW	$T_A = -40°$ to $+85°C$	SOP–16L
MC33030P		DIP–16

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	36	V
Input Voltage Range Op Amp, Comparator, Current Limit (Pins 1, 2, 3, 6, 7, 8, 9, 15)	V_{IR}	–0.3 to V_{CC}	V
Input Differential Voltage Range Op Amp, Comparator (Pins 1, 2, 3, 6, 7, 8, 9)	V_{IDR}	–0.3 to V_{CC}	V
Delay Pin Sink Current (Pin 16)	$I_{DLY(sink)}$	20	mA
Output Source Current (Op Amp)	I_{source}	10	mA
Drive Output Voltage Range (Note 1)	V_{DRV}	–0.3 to (V_{CC} + V_F)	V
Drive Output Source Current (Note 2)	$I_{DRV(source)}$	1.0	A
Drive Output Sink Current (Note 2)	$I_{DRV(sink)}$	1.0	A
Brake Diode Forward Current (Note 2)	I_F	1.0	A
Power Dissipation and Thermal Characteristics			°C/W
P Suffix, Dual In Line Case 648C			
Thermal Resistance, Junction–to–Air	$R_{θJA}$	80	
Thermal Resistance, Junction–to–Case (Pins 4, 5, 12, 13)	$R_{θJC}$	15	
DW Suffix, Dual In Line Case 751G			
Thermal Resistance, Junction–to–Air	$R_{θJA}$	94	
Thermal Resistance, Junction–to–Case (Pins 4, 5, 12, 13)	$R_{θJC}$	18	
Operating Junction Temperature	T_J	+150	°C
Operating Ambient Temperature Range	T_A	–40 to +85	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

NOTES: 1. The upper voltage level is clamped by the forward drop, V_F, of the brake diode.
2. These values are for continuous DC current. Maximum package power dissipation limits must be observed.

ELECTRICAL CHARACTERISTICS (V_{CC} = 14 V, T_A = 25°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
ERROR AMP					
Input Offset Voltage (–40°C ≤ T_A ≤ 85°C) $V_{Pin\ 6}$ = 7.0 V, R_L = 100 k	V_{IO}	–	1.5	10	mV
Input Offset Current ($V_{Pin\ 6}$ = 1.0 V, R_L = 100 k)	I_{IO}	–	0.7	–	nA
Input Bias Current ($V_{Pin\ 6}$ = 7.0 V, R_L = 100 k)	I_{IB}	–	7.0	–	nA
Input Common–Mode Voltage Range ΔV_{IO} = 20 mV, R_L = 100 k	V_{ICR}	–	0 to (V_{CC} – 1.2)	–	V
Slew Rate, Open Loop (V_{ID} = 0.5 V, C_L = 15 pF)	SR	–	0.40	–	V/µs
Unity–Gain Crossover Frequency	f_c	–	550	–	kHz
Unity–Gain Phase Margin	ϕm	–	63	–	deg.
Common–Mode Rejection Ratio ($V_{Pin\ 6}$ = 7.0 V, R_L = 100 k)	CMRR	50	82	–	dB
Power Supply Rejection Ratio V_{CC} = 9.0 to 16 V, $V_{Pin\ 6}$ = 7.0 V, R_L = 100 k	PSRR	–	89	–	dB
Output Source Current ($V_{Pin\ 6}$ = 12 V)	$I_{O\,+}$	–	1.8	–	mA
Output Sink Current ($V_{Pin\ 6}$ = 1.0 V)	$I_{O\,–}$	–	250	–	µA
Output Voltage Swing (R_L = 17 k to Ground)	V_{OH}	12.5	13.1	–	V
	V_{OL}	–	0.02	–	V

NOTES: 3. The upper or lower hysteresis will be lost when operating the Input, Pin 3, close to the respective rail. Refer to Figure 4.
4. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient temperature as possible.

ELECTRICAL CHARACTERISTICS (continued) (V_{CC} = 14 V, T_A = 25°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
WINDOW DETECTOR					
Input Hysteresis Voltage ($V_1 – V_4$, $V_2 – V_3$, Figure 18)	V_H	25	35	45	mV
Input Dead Zone Range ($V_2 – V_4$, Figure 18)	V_{IDZ}	166	210	254	mV
Input Offset Voltage ($\lvert [V_2 – V_{Pin\ 2}] – [V_{Pin\ 2} – V_4] \rvert$ Figure 18)	V_{IO}	–	25	–	mV
Input Functional Common–Mode Range (Note 3) Upper Threshold Lower Threshold	 V_{IH} V_{IL}	 – –	 (V_{CC} – 1.05) 0.24	 – –	V
Reference Input Self Centering Voltage Pins 1 and 2 Open	V_{RSC}	–	(1/2 V_{CC})	–	V
Window Detector Propagation Delay Comparator Input, Pin 3, to Drive Outputs V_{ID} = 0.5 V, $R_{L(DRV)}$ = 390 Ω	$t_{p(IN/DRV)}$	–	2.0	–	µs
OVER–CURRENT MONITOR					
Over–Current Reference Resistor Voltage (Pin 15)	R_{OC}	3.9	4.3	4.7	V
Delay Pin Source Current V_{DLY} = 0 V, R_{OC} = 27 k, I_{DRV} = 0 mA	$I_{DLY(source)}$	–	5.5	6.9	µA
Delay Pin Sink Current (R_{OC} = 27 k, I_{DRV} = 0 mA) V_{DLY} = 5.0 V V_{DLY} = 8.3 V V_{DLY} = 14 V	$I_{DLY(sink)}$	 – – –	 0.1 0.7 16.5	 – – –	mA
Delay Pin Voltage, Low State (I_{DLY} = 0 mA)	$V_{OL(DLY)}$	–	0.3	0.4	V
Over–Current Shutdown Threshold V_{CC} = 14 V V_{CC} = 8.0 V	$V_{th(OC)}$	 6.8 5.5	 7.5 6.0	 8.2 6.5	V
Over–Current Shutdown Propagation Delay Delay Capacitor Input, Pin 16, to Drive Outputs, V_{ID} = 0.5 V	$t_{p(DLY/DRV)}$	–	1.8	–	µs
POWER H–SWITCH					
Drive–Output Saturation (– 40°C ≤ T_A ≤ + 85°C, Note 4) High–State (I_{source} = 100 mA) Low–State (I_{sink} = 100 mA)	 $V_{OH(DRV)}$ $V_{OL(DRV)}$	 (V_{CC} – 2) –	 (V_{CC} – 0.85) 0.12	 – 1.0	V
Drive–Output Voltage Switching Time (C_L = 15 pF) Rise Time Fall Time	 t_r t_f	 – –	 200 200	 – –	ns
Brake Diode Forward Voltage Drop (I_F = 200 mA, Note 4)	V_F	–	1.04	2.5	V
TOTAL DEVICE					
Standby Supply Current	I_{CC}	–	14	25	mA
Over–Voltage Shutdown Threshold (– 40°C ≤ T_A ≤ + 85°C)	$V_{th(OV)}$	16.5	18	20.5	V
Over–Voltage Shutdown Hysteresis (Device “off” to “on”)	$V_{H(OV)}$	0.3	0.6	1.0	V
Operating Voltage Lower Threshold (– 40°C ≤ T_A ≤ + 85°C)	V_{CC}	–	7.5	8.0	V

NOTES: 3. The upper or lower hysteresis will be lost when operating the Input, Pin 3, close to the respective rail. Refer to Figure 4.
4. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient temperature as possible.

Figure 1. Error Amp Input Common–Mode Voltage Range versus Temperature

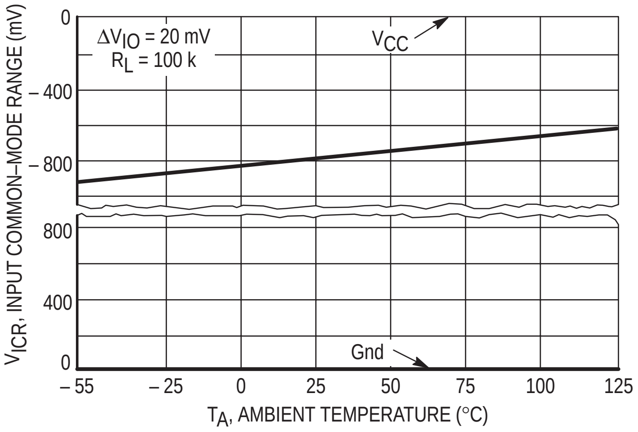


Figure 2. Error Amp Output Saturation versus Load Current

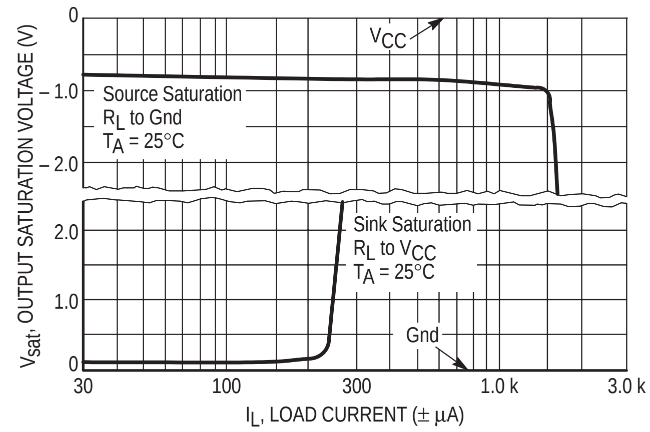


Figure 3. Open Loop Voltage Gain and Phase versus Frequency

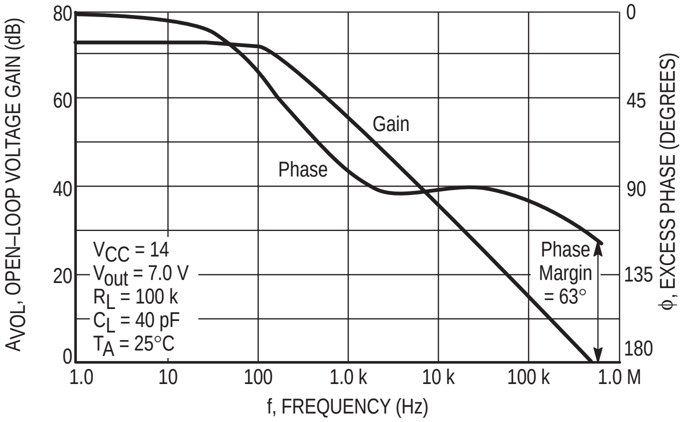


Figure 4. Window Detector Reference–Input Common–Mode Voltage Range versus Temperature

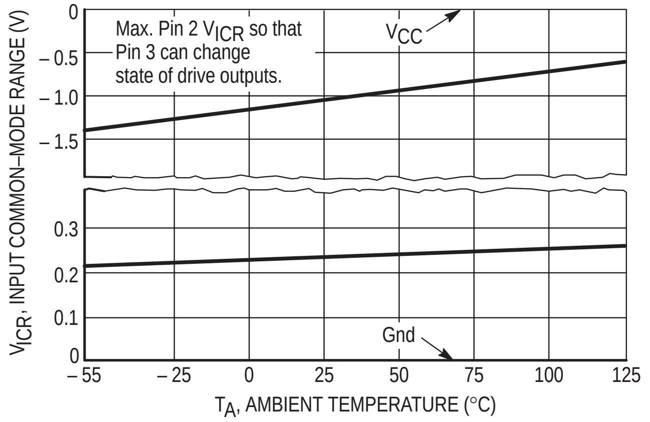


Figure 5. Window Detector Feedback–Input Thresholds versus Temperature

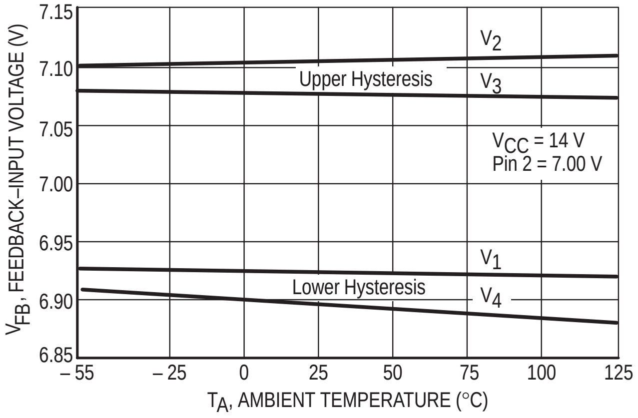


Figure 6. Output Driver Saturation versus Load Current

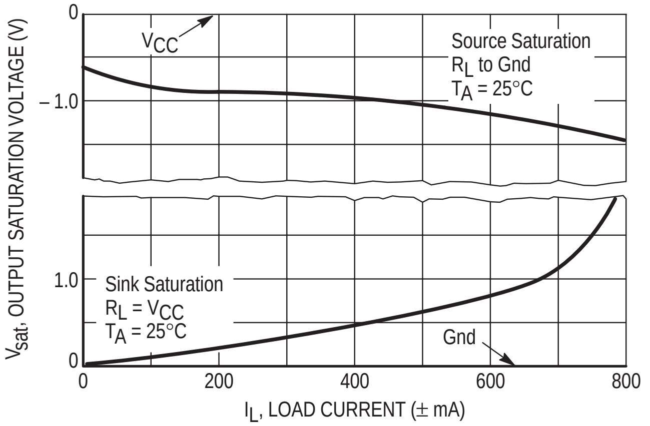


Figure 7. Brake Diode Forward Current versus Forward Voltage

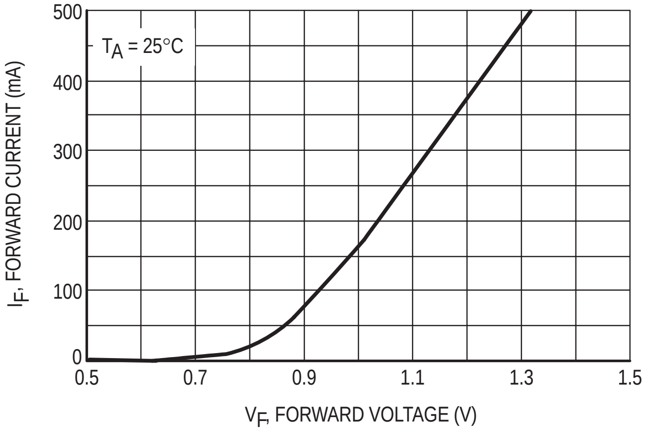


Figure 8. Output Source Current–Limit versus Over–Current Reference Resistance

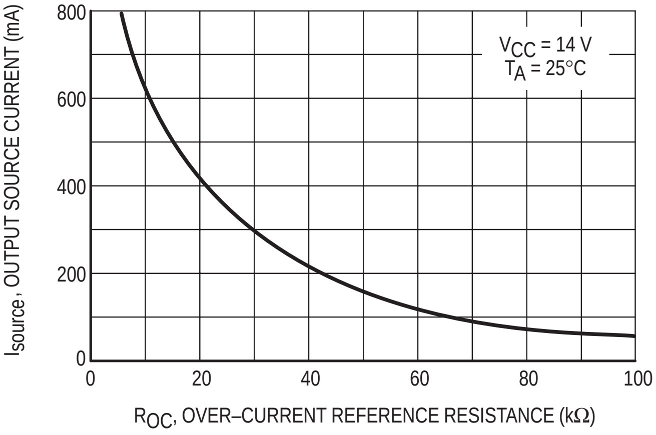


Figure 9. Output Source Current–Limit versus Temperature

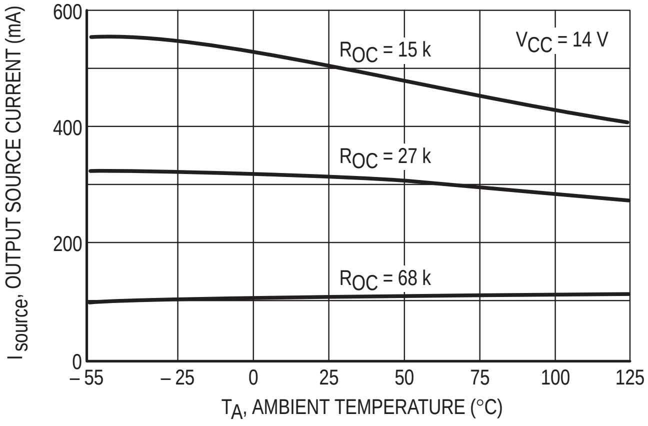


Figure 10. Normalized Delay Pin Source Current versus Temperature

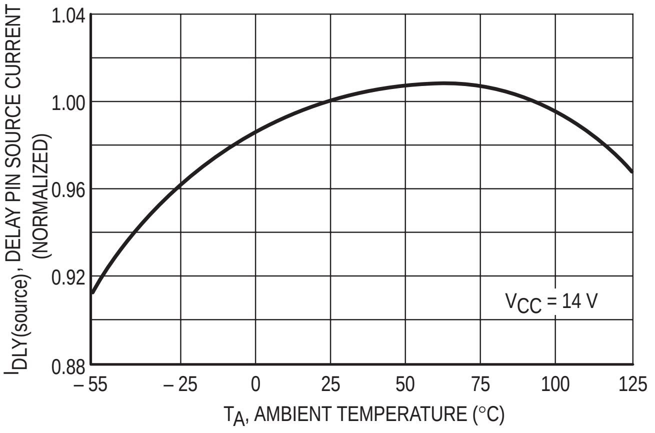


Figure 11. Normalized Over–Current Delay Threshold Voltage versus Temperature

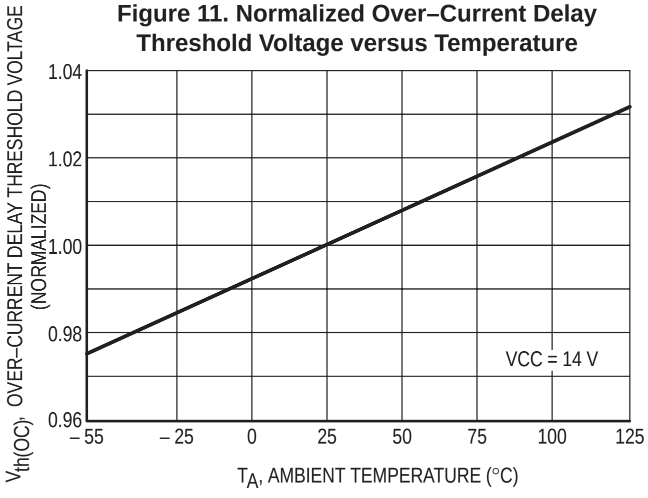


Figure 12. Supply Current versus Supply Voltage

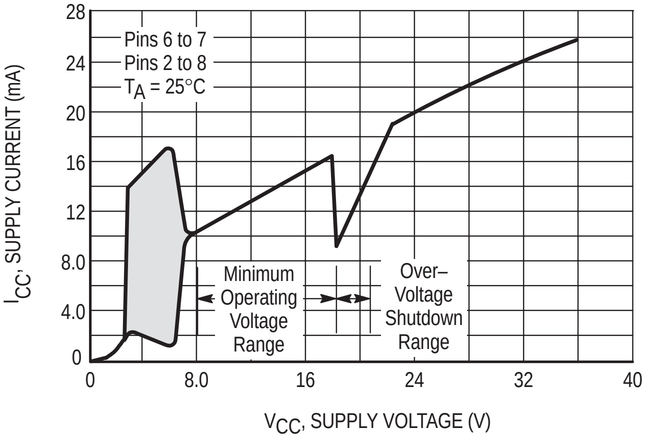


Figure 13. Normalized Over–Voltage Shutdown Threshold versus Temperature

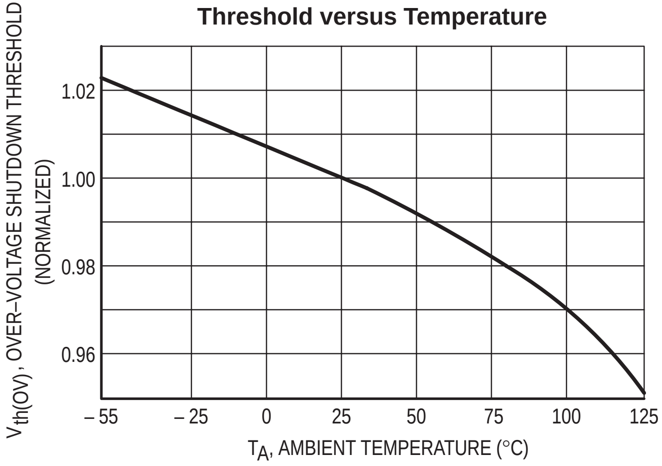


Figure 14. Normalized Over–Voltage Shutdown Hysteresis versus Temperature

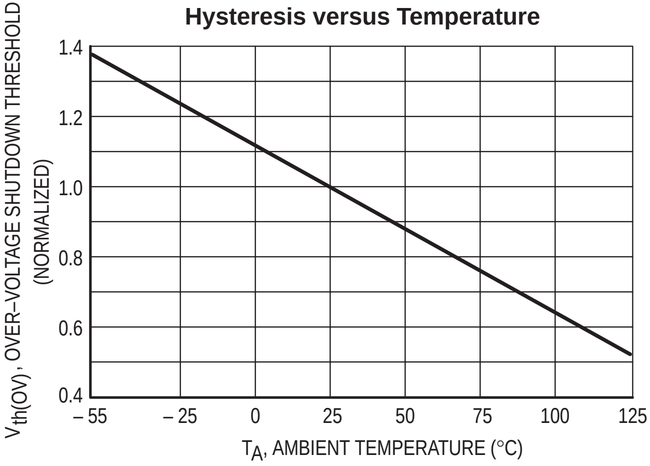


Figure 15. P Suffix (DIP–16) Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length

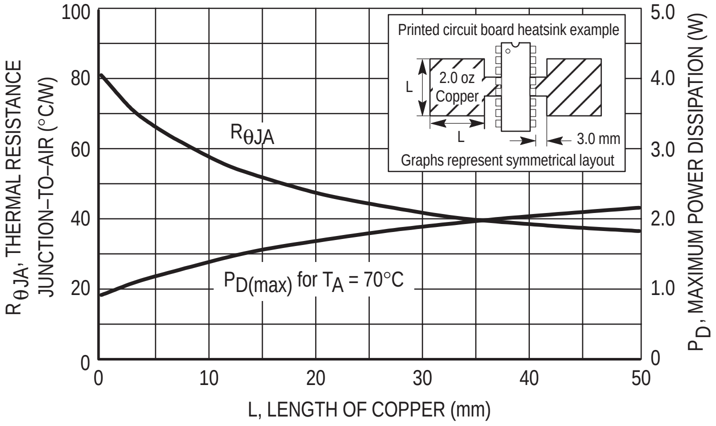
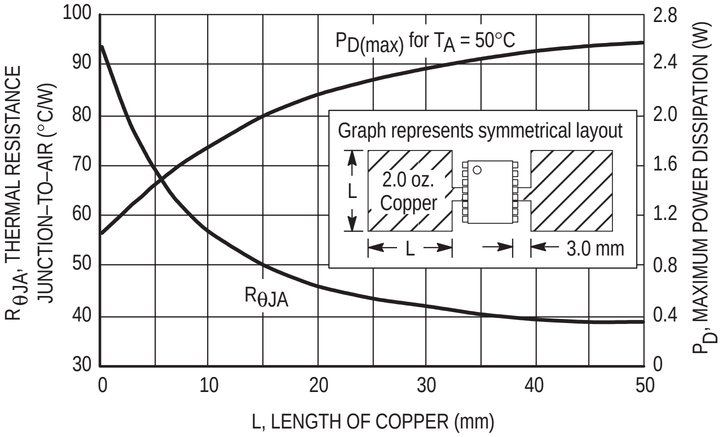


Figure 16. DW Suffix (SOP–16L) Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length



OPERATING DESCRIPTION

The MC33030 was designed to drive fractional horsepower DC motors and sense actuator position by voltage feedback. A typical servo application and representative internal block diagram are shown in Figure 17. The system operates by setting a voltage on the reference input of the Window Dectector (Pin 1) which appears on (Pin 2). A DC motor then drives a position sensor, usually a potentiometer driven by a gear box, in a corrective fashion so that a voltage proportional to position is present at Pin 3. The servo motor will continue to run until the voltage at Pin 3 falls within the dead zone, which is centered about the reference voltage.

The Window Detector is composed of two comparators, A and B, each containing hysteresis. The reference input, common to both comparators, is pre–biased at 1/2 V_{CC} for simple two position servo systems and can easily be overriden by an external voltage divider. The feedback voltage present at Pin 3 is connected to the center of two resistors that are driven by an equal magnitude current source and sink. This generates an offset voltage at the input of each comparator which is centered about Pin 3 that can float virtually from V_{CC} to ground. The sum of the upper and lower offset voltages is defined as the window detector input dead zone range.

To increase system flexibility, an on–chip Error Amp is provided. It can be used to buffer and/or gain–up the actuator position voltage which has the effect of narrowing the dead zone range. A PNP differential input stage is provided so that the input common–mode voltage range will include ground. The main design goal of the error amp output stage was to be able to drive the window detector input. It typically can source 1.8 mA and sink 250 µA. Special design considerations must be made if it is to be used for other applications.

The Power H–Switch provides a direct means for motor drive and braking with a maximum source, sink, and brake current of 1.0 A continuous. Maximum package power dissipation limits must be observed. Refer to Figure 15 for thermal information. For greater drive current requirements, a method for buffering that maintains all the system features is shown in Figure 30.

The Over–Current Monitor is designed to distinguish between motor start–up or locked rotor conditions that can occur when the actuator has reached its travel limit. A fraction of the Power H–Switch source current is internally fed into one of the two inverting inputs of the current comparator, while the non–inverting input is driven by a programmable current reference. This reference level is controlled by the resistance value selected for R_{OC}, and must be greater than the required motor run–current with its mechanical load over temperature; refer to Figure 8. During an over–current condition, the comparator will turn off and allow the current source to charge the delay capacitor, C_{DLY}. When C_{DLY} charges to a level of 7.5 V, the set input of the over–current latch will go high, disabling the drive and brake functions of the Power H–Switch. The programmable time delay is determined by the capacitance value–selected for C_{DLY}.

$$t_{DLY} = \frac{V_{ref}\ C_{DLY}}{I_{DLY(source)}} = \frac{7.5\ C_{DLY}}{5.5\ \mu A} = 1.36\ C_{DLY}\quad \text{in } \mu F$$

This system allows the Power H–Switch to supply motor start–up current for a predetermined amount of time. If the rotor is locked, the system will time–out and shut–down. This feature eliminates the need for servo end–of–travel or limit switches. Care must be taken so as not to select too large of a capacitance value for C_{DLY}. An over–current condition for an excessively long time–out period can cause the integrated circuit to overheat and eventually fail. Again, the maximum package power dissipation limits must be observed. The over–current latch is reset upon power–up or by readjusting $V_{Pin\ 2}$ as to cause $V_{Pin\ 3}$ to enter or pass through the dead zone. This can be achieved by requesting the motor to reverse direction.

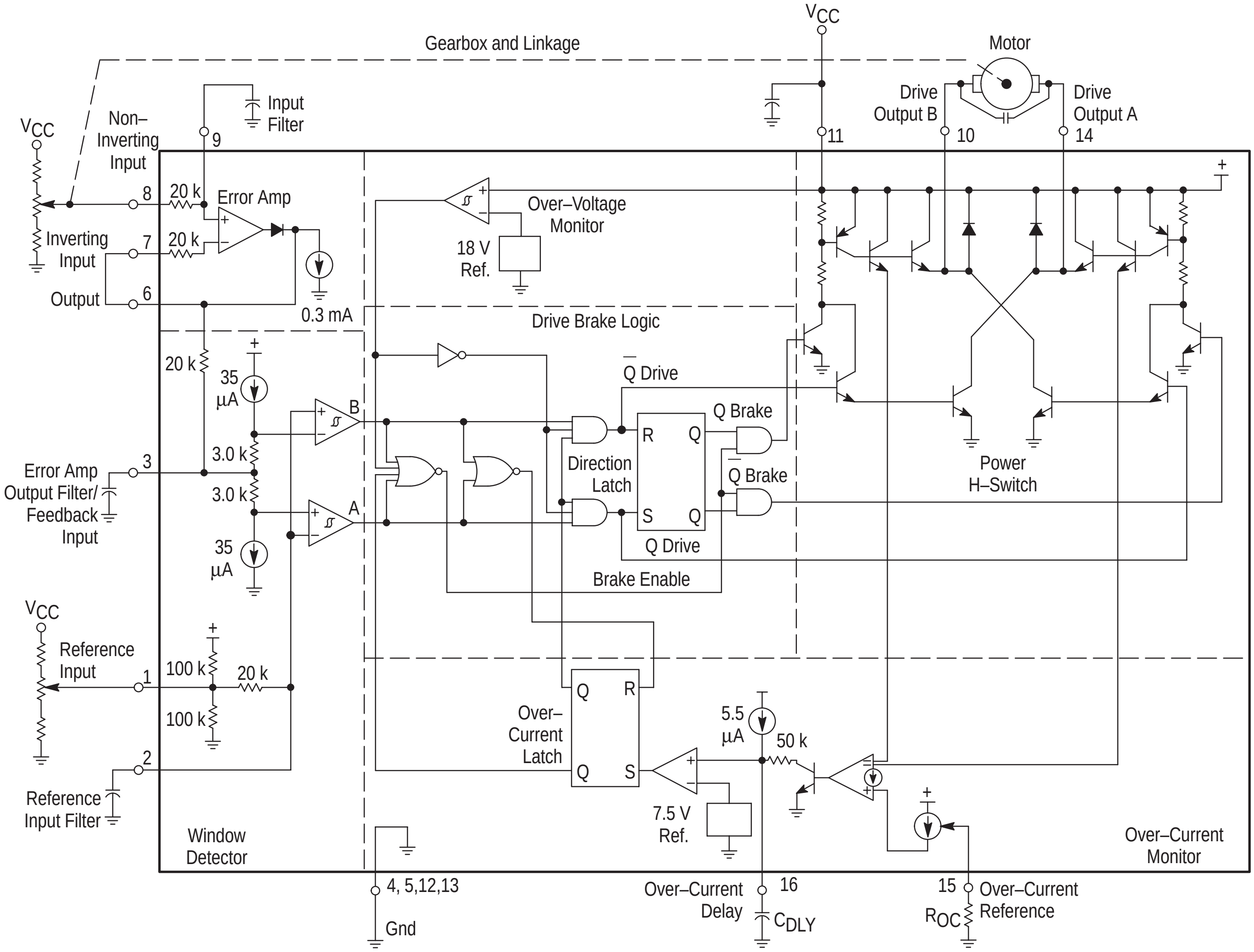
An Over–Voltage Monitor circuit provides protection for the integrated circuit and motor by disabling the Power H–Switch functions if V_{CC} should exceed 18 V. Resumption of normal operation will commence when V_{CC} falls below 17.4 V.

A timing diagram that depicts the operation of the Drive/Brake Logic section is shown in Figure 18. The waveforms grouped in [1] show a reference voltage that was preset, appearing on Pin 2, which corresponds to the desired actuator position. The true actuator position is represented by the voltage on Pin 3. The points V_1 through V_4 represent the input voltage thresholds of comparators A and B that cause a change in their respective output state. They are defined as follows:

V_1 = Comparator B turn–off threshold
V_2 = Comparator A turn–on threshold
V_3 = Comparator A turn–off threshold
V_4 = Comparator B turn–on threshold
V_1–V_4 = Comparator B input hysteresis voltage
V_2–V_3 = Comparator A input hysteresis voltage
V_2–V_4 = Window detector input dead zone range
$|(V_2 - V_{Pin2}) - (V_{Pin2} - V_4)|$ = Window detector input voltage

It must be remembered that points V_1 through V_4 always try to follow and center about the reference voltage setting if it is within the input common–mode voltage range of Pin 3; Figures 4 and 5. Initially consider that the feedback input voltage level is somewhere on the dashed line between V_2 and V_4 in [1]. This is within the dead zone range as defined above and the motor will be off. Now if the reference voltage is raised so that $V_{Pin\ 3}$ is less than V_4, comparator B will turn–on [3] enabling $\overline{Q}$ Drive, causing Drive Output A to sink and B to source motor current [8]. The actuator will move in Direction B until $V_{Pin\ 3}$ becomes greater than V_1. Comparator B will turn–off, activating the brake enable [4] and $\overline{Q}$ Brake [6] causing Drive Output A to go high and B to go into a high impedance state. The inertia of the mechanical system will drive the motor as a generator creating a positive voltage on Pin 10 with respect to Pin 14. The servo system can be stopped quickly, so as not to over–shoot through the dead zone range, by braking. This is accomplished by shorting the motor/generator terminals together. Brake current will flow into the diode at Drive Output B, through the internal V_{CC} rail, and out the emitter of the sourcing transistor at Drive Output A. The end of the solid line and beginning of the dashed for $V_{Pin\ 3}$ [1] indicates the possible resting position of the actuator after braking.

Figure 17. Representative Block Diagram and Typical Servo Application



If $V_{Pin\ 3}$ should continue to rise and become greater than V_2, the actuator will have over shot the dead zone range and cause the motor to run in Direction A until $V_{Pin\ 3}$ is equal to V_3. The Drive/Brake behavior for Direction A is identical to that of B. Overshooting the dead zone range in both directions can cause the servo system to continuously hunt or oscillate. Notice that the last motor run–direction is stored in the direction latch. This information is needed to determine whether Q or Q Brake is to be enabled when $V_{Pin\ 3}$ enters the dead zone range. The dashed lines in [8,9] indicate the resulting waveforms of an over–current condition that has exceeded the programmed time delay. Notice that both Drive Outputs go into a high impedance state until $V_{Pin\ 2}$ is readjusted so that $V_{Pin\ 3}$ enters or crosses through the dead zone [7, 4].

The inputs of the Error Amp and Window Detector can be susceptible to the noise created by the brushes of the DC motor and cause the servo to hunt. Therefore, each of these inputs are provided with an internal series resistor and are pinned out for an external bypass capacitor. It has been found that placing a capacitor with *short leads* directly across the brushes will significantly reduce noise problems. Good quality RF bypass capacitors in the range of 0.001 to 0.1 µF may be required. Many of the more economical motors will generate significant levels of RF energy over a spectrum that extends from DC to beyond 200 MHz. The capacitance value and method of noise filtering must be determined on a system by system basis.

Thus far, the operating description has been limited to servo systems in which the motor mechanically drives a potentiometer for position sensing. Figures 19, 20, 27, and 31 show examples that use light, magnetic flux, temperature, and pressure as a means to drive the feedback element. Figures 21, 22 and 23 are examples of two position, open loop servo systems. In these systems, the motor runs the actuator to each end of its travel limit where the Over–Current Monitor detects a locked rotor condition and shuts down the drive. Figures 32 and 33 show two possible methods of using the MC33030 as a switching motor controller. In each example a fixed reference voltage is applied to Pin 2. This causes $V_{pin\ 3}$ to be less than V_4 and Drive Output A, Pin 14, to be in a low state saturating the TIP42 transistor. In Figure 32, the motor drives a tachometer that generates an ac voltage proportional to RPM. This voltage is rectified, filtered, divided down by the speed set potentiometer, and applied to Pin. 8. The motor will accelerate until $V_{Pin\ 3}$ is equal to V_1 at which time Pin 14 will go to a high state and terminate the motor drive. The motor will now coast until $V_{Pin\ 3}$ is less than V_4 where upon drive is then reapplied. The system operation of Figure 31 is identical to that of 32 except the signal at Pin 3 is an amplified average of the motors drive and back EMF voltages. Both systems exhibit excellent control of RPM with variations of V_{CC}; however, Figure 32 has somewhat better torque characteristics at low RPM.

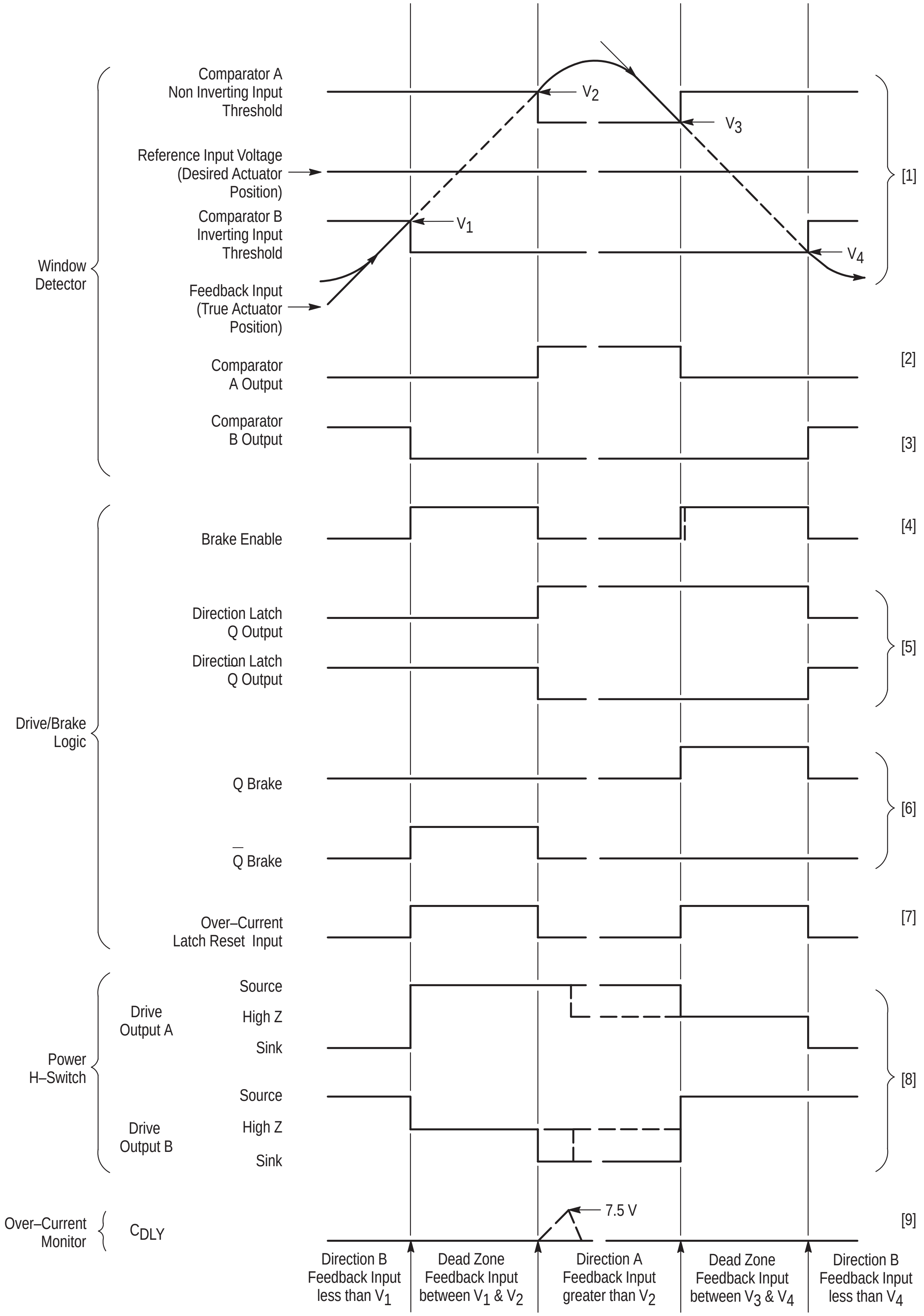
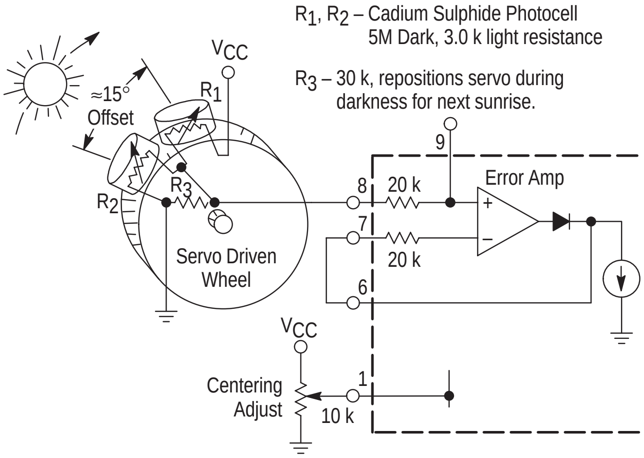


Figure 18. Timing Diagram

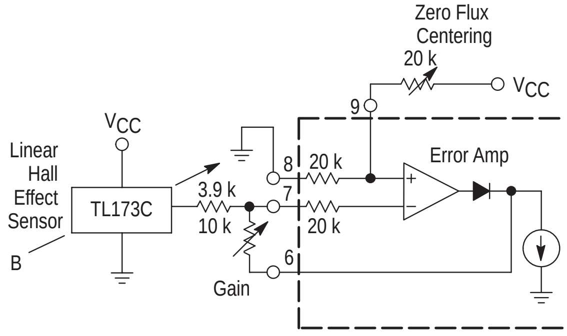
Figure 19. Solar Tracking Servo System



R_1, R_2 – Cadium Sulphide Photocell
5M Dark, 3.0 k light resistance

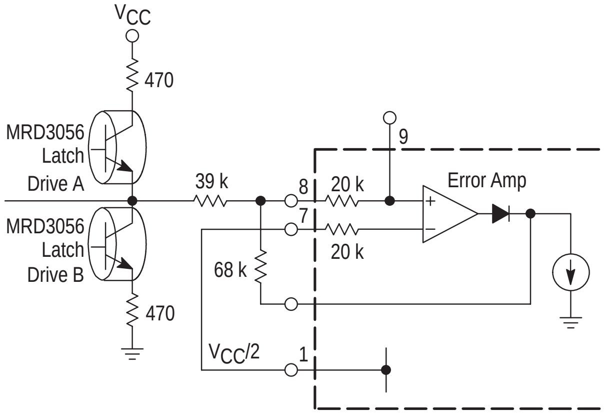
R_3 – 30 k, repositions servo during darkness for next sunrise.

Figure 20. Magnetic Sensing Servo System



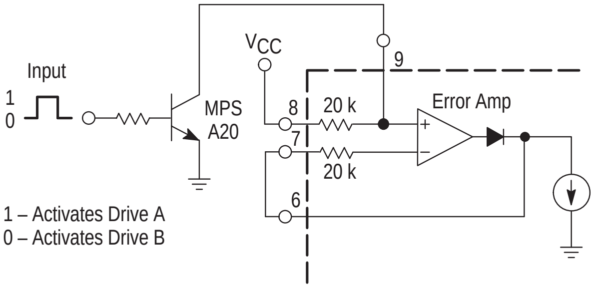
Typical sensitivity with gain set at 3.9 k is 1.5 mV/gauss.
Servo motor controls magnetic field about sensor.

Figure 21. Infrared Latched Two Position Servo System



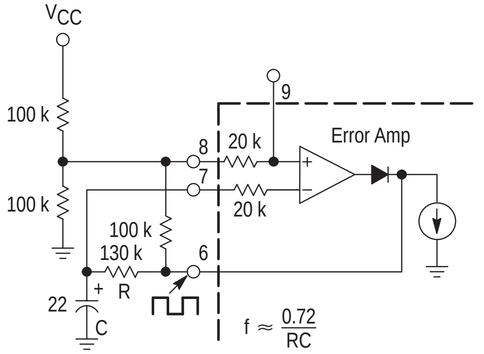
Over–current monitor (not shown) shuts down servo when end stop is reached.

Figure 22. Digital Two Position Servo System



Over–current monitor (not shown) shuts down servo when end stop is reached.

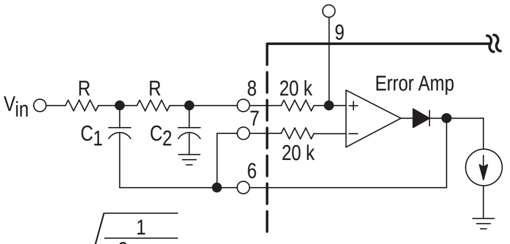
Figure 23. 0.25 Hz Square–Wave Servo Agitator



$$f \approx \frac{0.72}{RC}$$

$$R \geqslant 20\ k$$

Figure 24. Second Order Low–Pass Active Filter

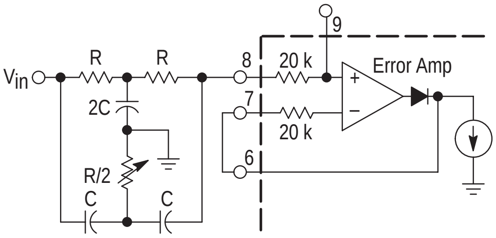


$$f_o = \frac{\sqrt{\frac{1}{R^2 C_1 C_2}}}{2\pi}$$

R = 1.0 M
C_1 = 1000 pF
C_2 = 100 pF

$$Q = \frac{\sqrt{\frac{C_1}{C_2}}}{2}$$

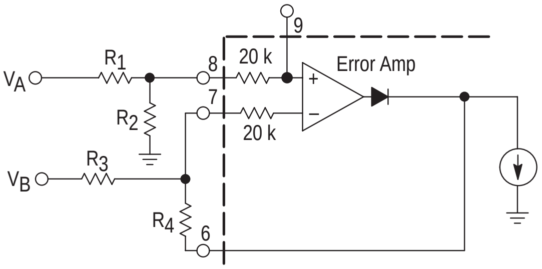
Figure 25. Notch Filter



$$f_{notch} = \frac{1}{2\pi RC}$$

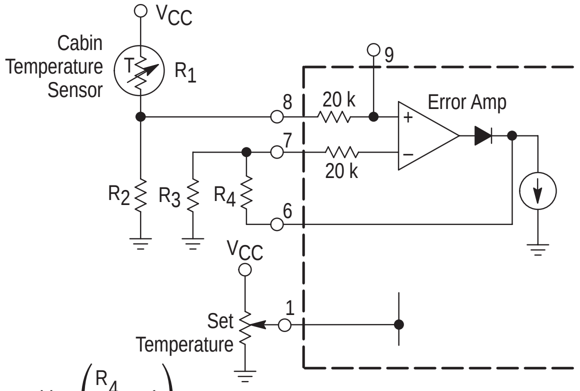
For 60 Hz R = 53.6 k, C = 0.05

Figure 26. Differential Input Amplifier



$$V_{Pin\,6} = V_A\left(\frac{R_3 + R_4}{R_1 + R_2}\right)\frac{R_2}{R_3} - \left(\frac{R_4}{R_3}\,V_B\right)$$

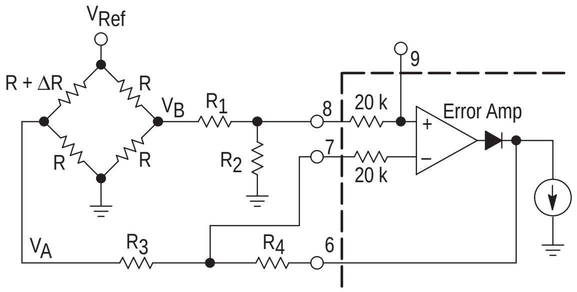
Figure 27. Temperature Sensing Servo System



$$V_{Pin\,6} = \frac{V_{CC}\left(\frac{R_4}{R_3} + 1\right)}{\left(\frac{R_1}{R_2} + 1\right)}$$

In this application the servo motor drives the heat/air conditioner modulator door in a duct system.

Figure 28. Bridge Amplifier

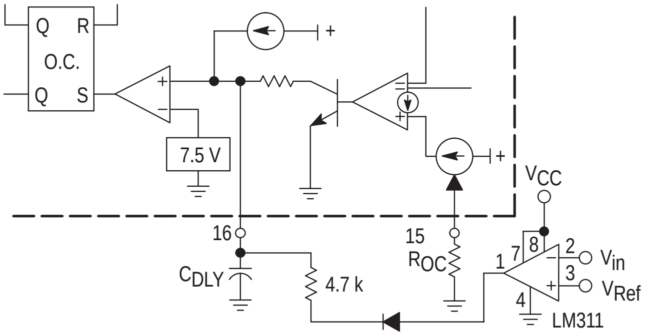


$$V_A - V_B = V_{Ref}\left(\frac{\Delta R}{4R + 2\Delta R}\right)$$

$$R_1 = R_3,\ R_2 = R_4,\ R_1 >> R$$

$$V_{Pin\,6} = \frac{R_4}{R_3}\,(V_A - V_B)$$

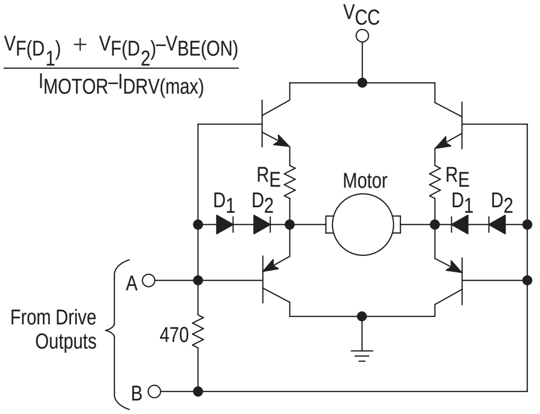
Figure 29. Remote Latched Shutdown



A direction change signal is required at Pins 2 or 3 to reset the over–current latch.

Figure 30. Power H–Switch Buffer

$$R_E \approx \frac{V_{F(D_1)} + V_{F(D_2)} - V_{BE(ON)}}{I_{MOTOR} - I_{DRV(max)}}$$



This circuit maintains the brake and over–current features of the MC33030. Set R_{OC} to 15 k for $I_{DRV(max)} \approx 0.5$ A.

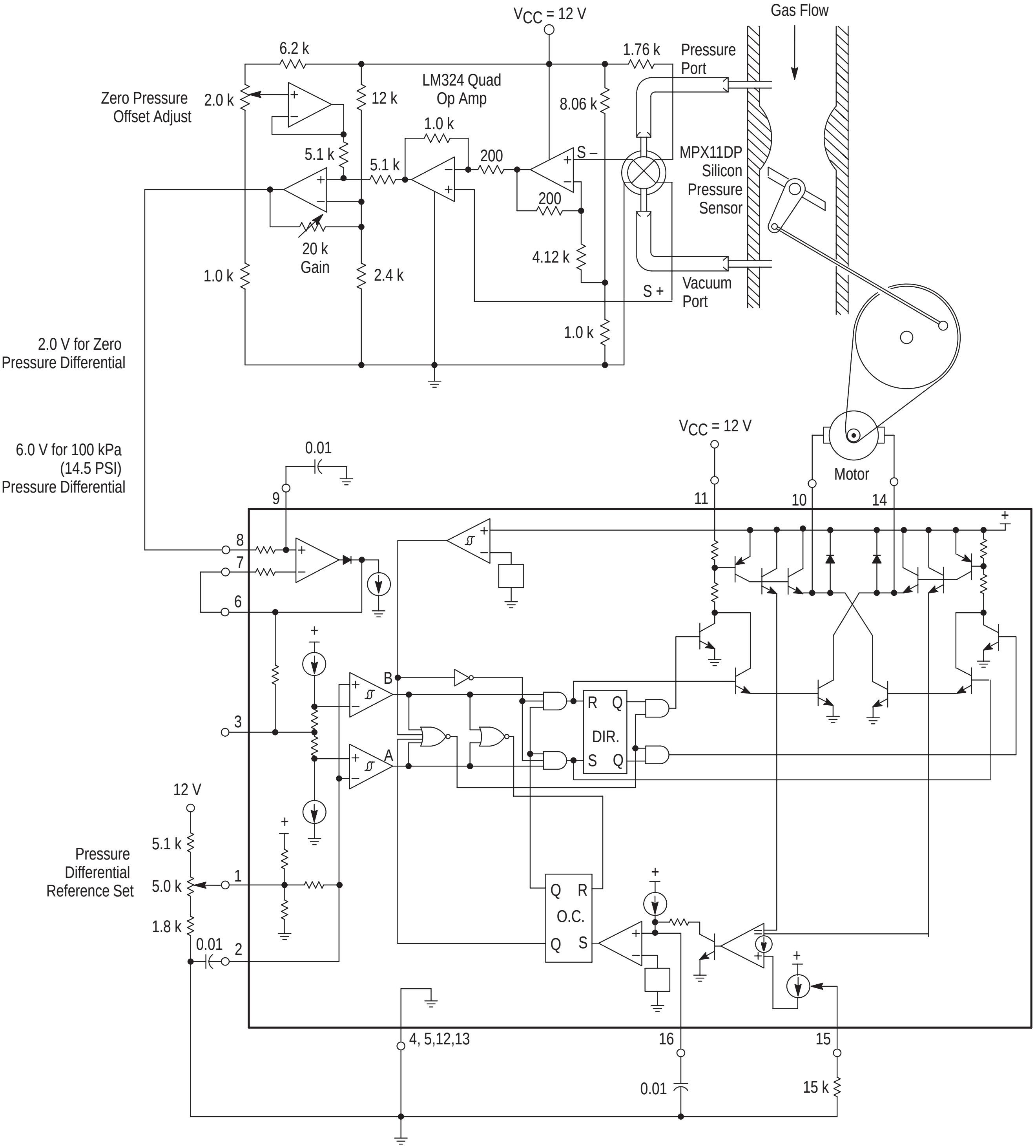


Figure 31. Adjustable Pressure Differential Regulator

Figure 32. Switching Motor Controller With Buffered Output and Tach Feedback

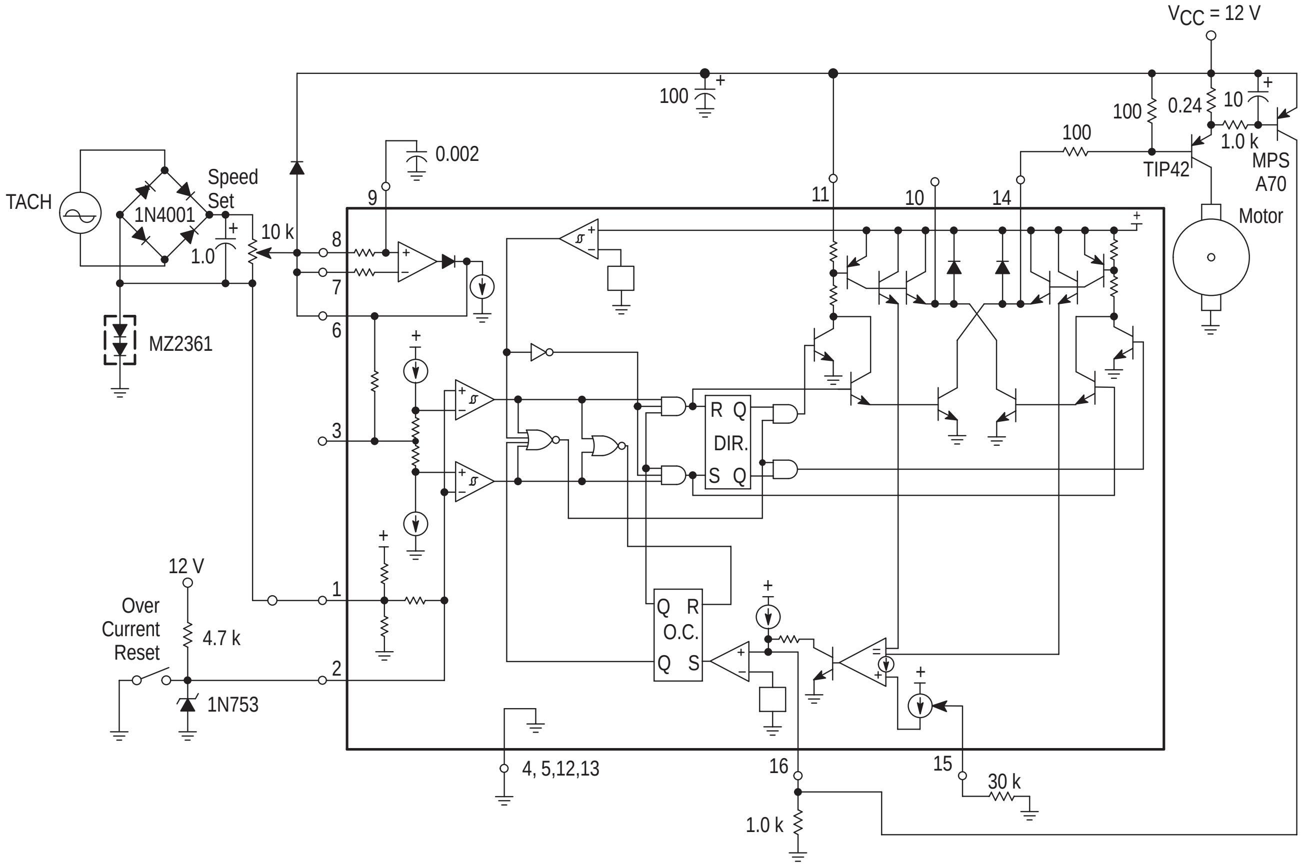
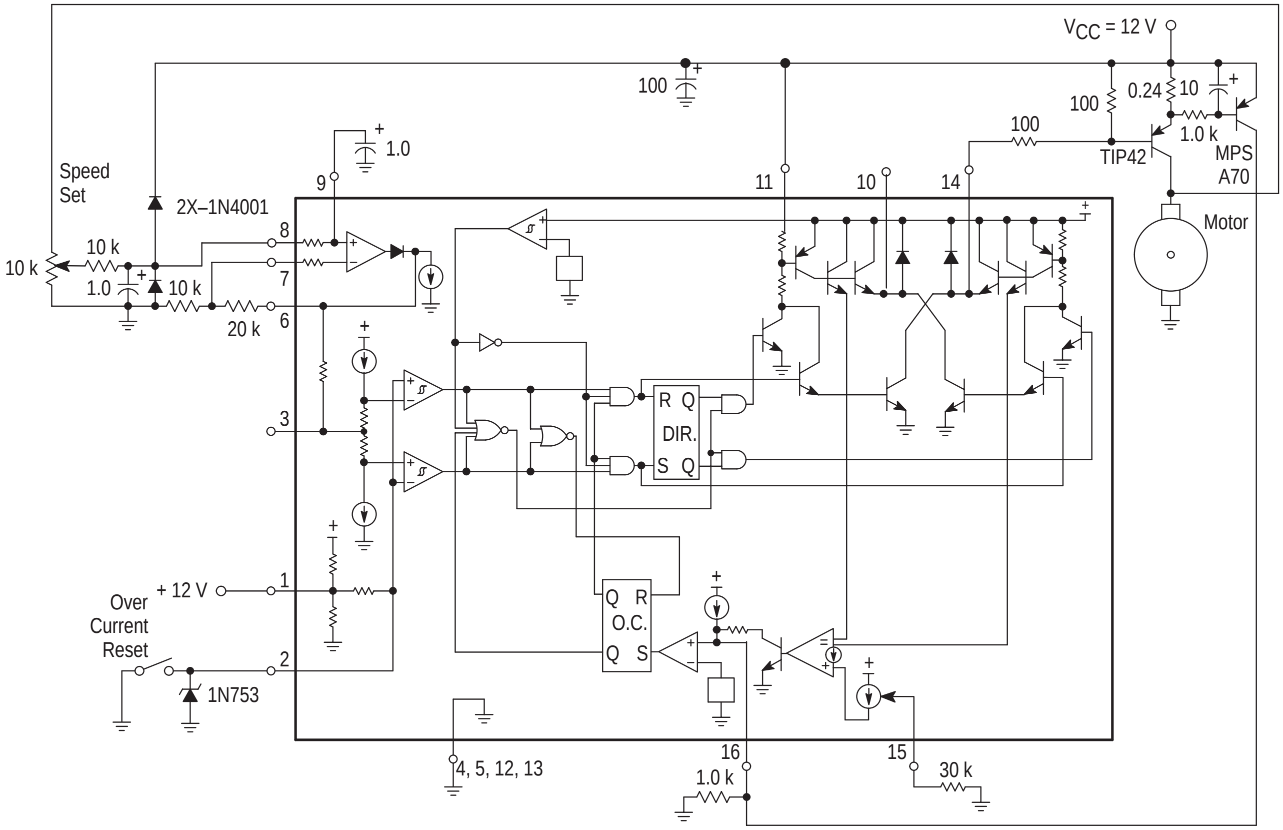


Figure 33. Switching Motor Controller With Buffered Output and Back EMF Sensing



MOTOROLA

MC33033

Brushless DC Motor Controller

The MC33033 is a high performance second generation, limited feature, monolithic brushless dc motor controller which has evolved from Motorola′s full featured MC33034 and MC33035 controllers. It contains all of the active functions required for the implementation of open loop, three or four phase motor control. The device consists of a rotor position decoder for proper commutation sequencing, temperature compensated reference capable of supplying sensor power, frequency programmable sawtooth oscillator, fully accessible error amplifier, pulse width modulator comparator, three open collector top drivers, and three high current totem pole bottom drivers ideally suited for driving power MOSFETs. Unlike its predessors, it does not feature separate drive circuit supply and ground pins, brake input, or fault output signal.

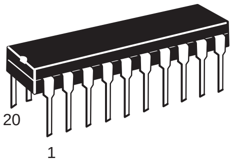
Included in the MC33033 are protective features consisting of undervoltage lockout, cycle–by–cycle current limiting with a selectable time delayed latched shutdown mode, and internal thermal shutdown.

Typical motor control functions include open loop speed, forward or reverse direction, and run enable.The MC33033 is designed to operate brushless motors with electrical sensor phasings of 60°/300° or 120°/240°, and can also efficiently control brush dc motors.

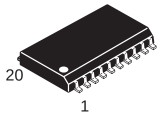
- 10 to 30 V Operation
- Undervoltage Lockout
- 6.25 V Reference Capable of Supplying Sensor Power
- Fully Accessible Error Amplifier for Closed Loop Servo Applications
- High Current Drivers Can Control External 3–Phase MOSFET Bridge
- Cycle–By–Cycle Current Limiting
- Internal Thermal Shutdown
- Selectable 60°/300° or 120°/240° Sensor Phasings
- Also Efficiently Control Brush DC Motors with External MOSFET H–Bridge

BRUSHLESS DC MOTOR CONTROLLER

**SEMICONDUCTOR
TECHNICAL DATA**

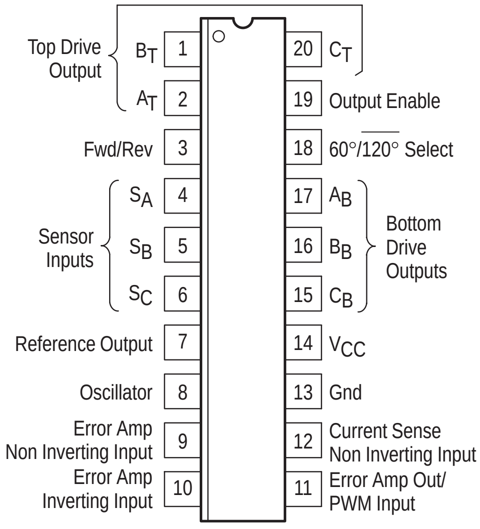


P SUFFIX
PLASTIC PACKAGE
CASE 738



DW SUFFIX
PLASTIC PACKAGE
CASE 751D
(SO–20L)

PIN CONNECTIONS

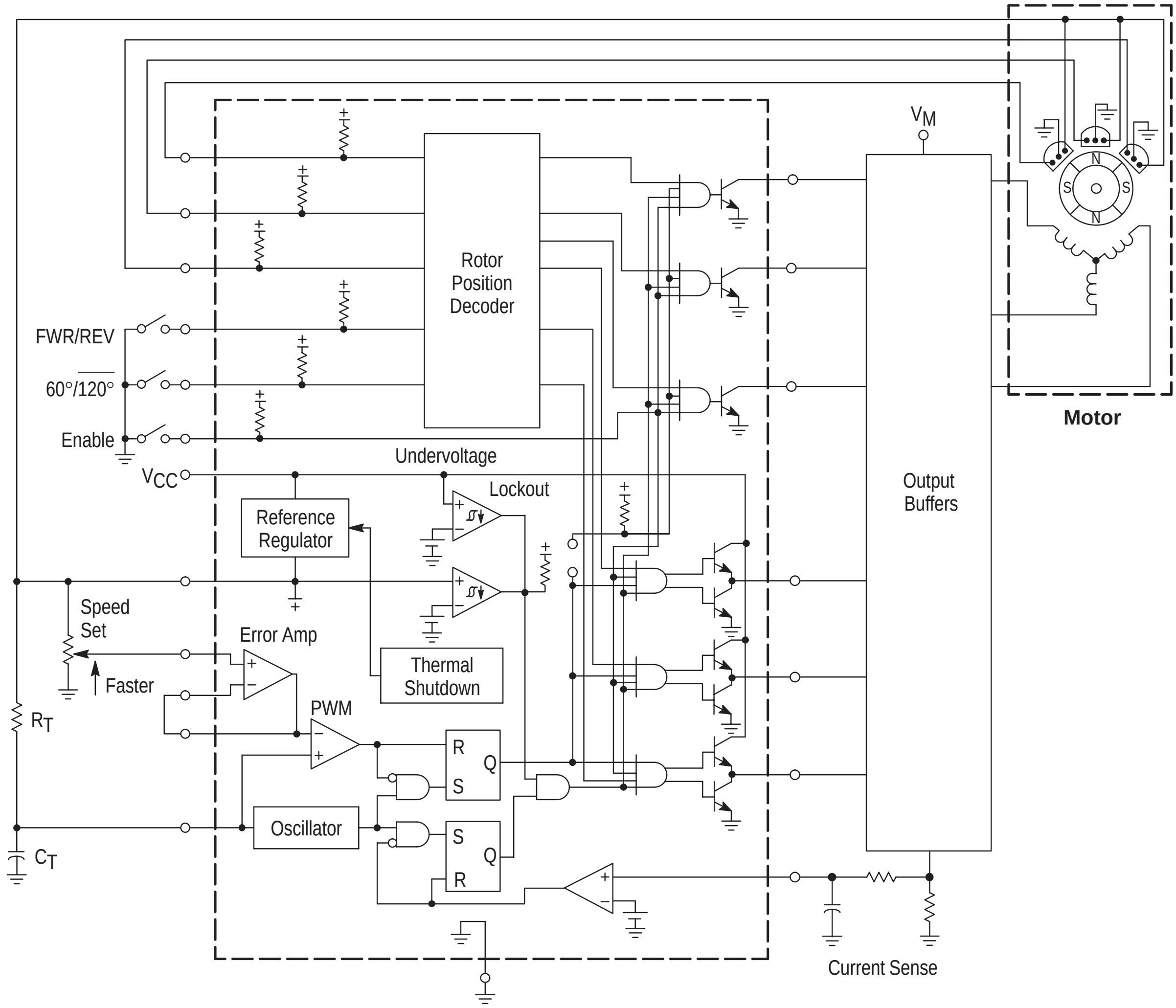


(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC33033DW	$T_A = -40°$ to $+85°C$	SO–20L
MC33033P		Plastic DIP

Representative Schematic Diagram



This device contains 266 active transistors.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	30	V
Digital Inputs (Pins 3, 4, 5, 6, 18, 19)	–	V_{ref}	V
Oscillator Input Current (Source or Sink)	I_{OSC}	30	mA
Error Amp Input Voltage Range (Pins 9, 10, Note 1)	V_{IR}	–0.3 to V_{ref}	V
Error Amp Output Current (Source or Sink, Note 2)	I_{Out}	10	mA
Current Sense Input Voltage Range	V_{Sense}	–0.3 to 5.0	V
Top Drive Voltage (Pins 1, 2, 20)	$V_{CE(top)}$	40	V
Top Drive Sink Current (Pins 1, 2, 20)	$I_{Sink(top)}$	50	mA
Bottom Drive Output Current (Source or Sink, Pins 15,16, 17)	I_{DRV}	100	mA
Power Dissipation and Thermal Characteristics P Suffix, Dual–In–Line, Case 738 Maximum Power Dissipation @ T_A = 85°C Thermal Resistance, Junction–to–Air DW Suffix, Surface Mount, Case 751D Maximum Power Dissipation @ T_A = 85°C Thermal Resistance, Junction–to–Air	 P_D $R_{\theta JA}$ P_D $R_{\theta JA}$	 867 75 619 105	 mW °C/W mW °C/W
Operating Junction Temperature	T_J	150	°C
Operating Ambient Temperature Range	T_A	–40 to +85	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 20 V, R_T = 4.7 k, C_T = 10 nF, T_A = 25°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
REFERENCE SECTION					
Reference Output Voltage (I_{ref} = 1.0 mA) T_A = 25°C T_A = –40° to + 85°C	V_{ref}	 5.9 5.82	 6.24 –	 6.5 6.57	V
Line Regulation (V_{CC} = 10 V to 30 V, I_{ref} = 1.0 mA)	Reg_{line}	–	1.5	30	mV
Load Regulation (I_{ref} = 1.0 mA to 20 mA)	Reg_{load}	–	16	30	mV
Output Short–Circuit Current (Note 3)	I_{SC}	40	75	–	mA
Reference Under Voltage Lockout Threshold	V_{th}	4.0	4.5	5.0	V
ERROR AMPLIFIER					
Input Offset Voltage (T_A = –40° to + 85°C)	V_{IO}	–	0.4	10	mV
Input Offset Current (T_A = –40° to + 85°C)	I_{IO}	–	8.0	500	nA
Input Bias Current (T_A = –40° to + 85°C)	I_{IB}	–	–46	–1000	nA
Input Common Mode Voltage Range	V_{ICR}		(0 V to V_{ref})		V
Open Loop Voltage Gain (V_O = 3.0 V, R_L = 15 k)	A_{VOL}	70	80	–	dB
Input Common Mode Rejection Ratio	CMRR	55	86	–	dB
Power Supply Rejection Ratio (V_{CC} = 10 V to 30 V)	PSRR	65	105	–	dB
Output Voltage Swing High State (R_L = 15 k to Gnd) Low State (R_L = 17 k to V_{ref})	 V_{OH} V_{OL}	 4.6 –	 5.3 0.5	 – 1.0	V

NOTES: 1. The input common mode voltage or input signal voltage should not be allowed to go negative by more than 0.3 V.
2. The compliance voltage must not exceed the range of –0.3 to V_{ref}.
3. Maximum package power dissipation limits must be observed.

ELECTRICAL CHARACTERISTICS (continued) (V_{CC} = 20 V, R_T = 4.7 k, C_T = 10 nF, T_A = 25°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OSCILLATOR SECTION					
Oscillator Frequency	f_{OSC}	22	25	28	kHz
Frequency Change with Voltage (V_{CC} = 10 V to 30 V)	$\Delta f_{OSC}/\Delta V$	–	0.01	5.0	%
Sawtooth Peak Voltage	$V_{OSC(P)}$	–	4.1	4.5	V
Sawtooth Valley Voltage	$V_{OSC(V)}$	1.2	1.5	–	V
LOGIC INPUTS					
Input Threshold Voltage (Pins 3, 4, 5, 6, 18, 19) High State Low State	 V_{IH} V_{IL}	 3.0 –	 2.2 1.7	 – 0.8	V
Sensor Inputs (Pins 4, 5, 6) High State Input Current (V_{IH} = 5.0 V) Low State Input Current (V_{IL} = 0 V)	 I_{IH} I_{IL}	 –150 –600	 –70 –337	 –20 –150	µA
Forward/Reverse, 60°/$\overline{120^\circ}$ Select and Output Enable (Pins 3, 18, 19) High State Input Current (V_{IH} = 5.0 V) Low State Input Current (V_{IL} = 0 V)	 I_{IH} I_{IL}	 –75 –300	 –36 –175	 –10 –75	µA
CURRENT–LIMIT COMPARATOR					
Threshold Voltage	V_{th}	85	101	115	mV
Input Common Mode Voltage Range	V_{ICR}	–	3.0	–	V
Input Bias Current	I_{IB}	–	–0.9	–5.0	µA
OUTPUTS AND POWER SECTIONS					
Top Drive Output Sink Saturation (I_{Sink} = 25 mA)	$V_{CE(sat)}$	–	0.5	1.5	V
Top Drive Output Off–State Leakage (V_{CE} = 30 V)	$I_{DRV(leak)}$	–	0.06	100	µA
Top Drive Output Switching Time (C_L = 47 pF, R_L = 1.0 k) Rise Time Fall Time	 t_r t_f	 – –	 107 26	 300 300	ns
Bottom Drive Output Voltage High State (V_{CC} = 30 V, I_{source} = 50 mA) Low State (V_{CC} = 30 V, I_{sink} = 50 mA)	 V_{OH} V_{OL}	 (V_{CC} – 2.0) –	 (V_{CC} – 1.1) 1.5	 – 2.0	V
Bottom Drive Output Switching Time (C_L = 1000 pF) Rise Time Fall Time	 t_r t_f	 – –	 38 30	 200 200	ns
Under Voltage Lockout Drive Output Enabled (V_{CC} Increasing) Hysteresis	 $V_{th(on)}$ V_H	 8.2 0.1	 8.9 0.2	 10 0.3	V
Power Supply Current	I_{CC}	–	15	22	mA

Figure 1. Oscillator Frequency versus Timing Resistor

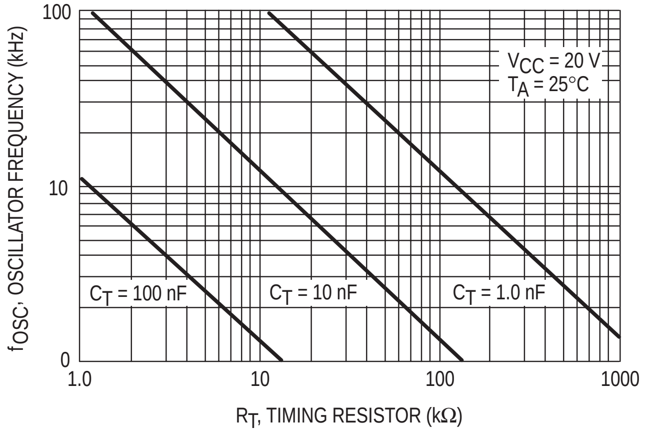


Figure 2. Oscillator Frequency Change versus Temperature

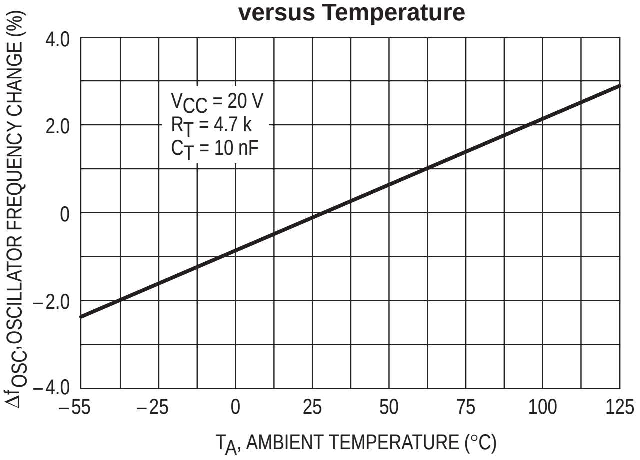


Figure 3. Error Amp Open Loop Gain and Phase versus Frequency

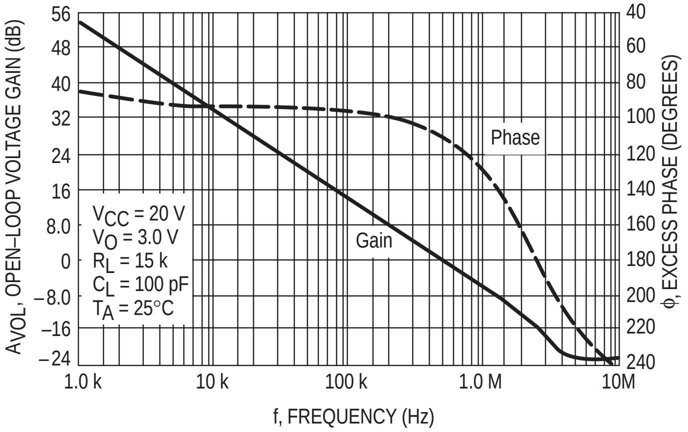


Figure 4. Error Amp Output Saturation Voltage versus Load Current

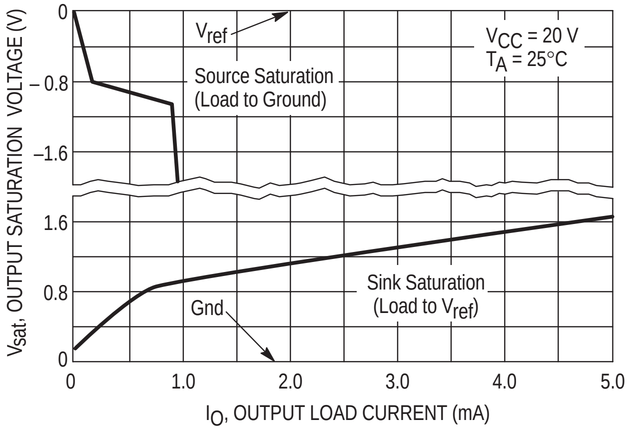


Figure 5. Error Amp Small–Signal Transient Response

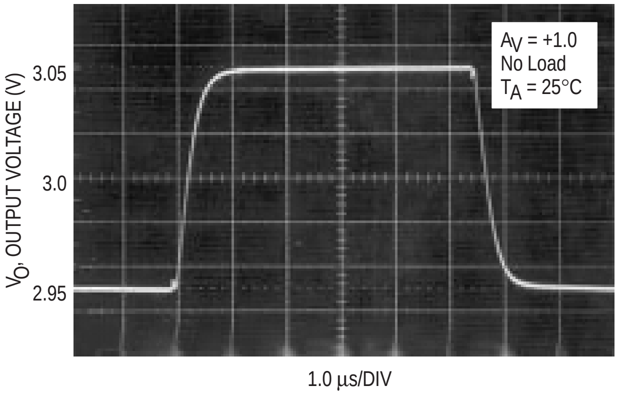


Figure 6. Error Amp Large–Signal Transient Response

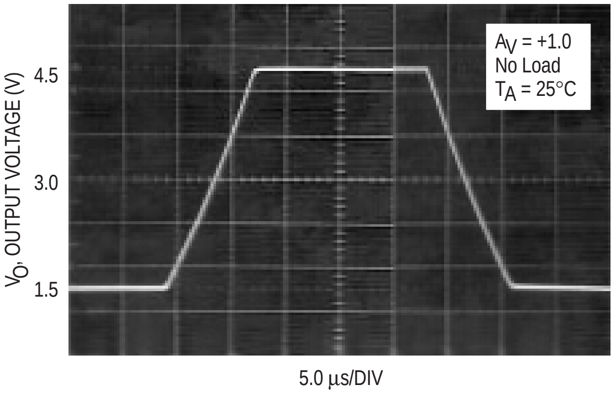


Figure 7. Reference Output Voltage Change versus Output Source Current

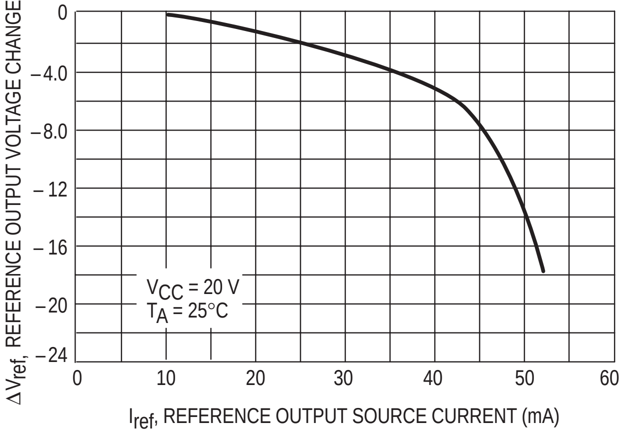


Figure 8. Reference Output Voltage versus Supply Voltage

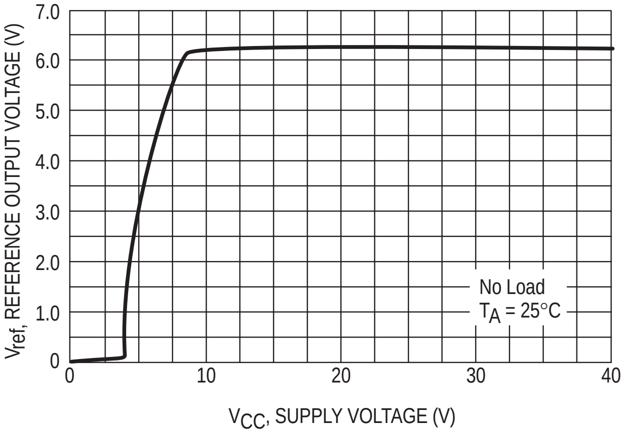


Figure 9. Reference Output Voltage versus Temperature

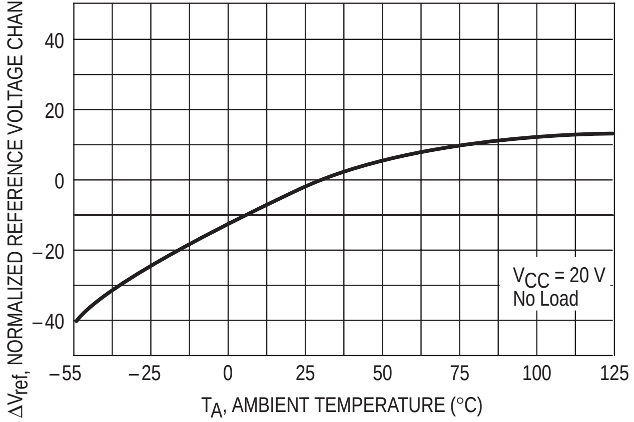


Figure 10. Output Duty Cycle versus PWM Input Voltage

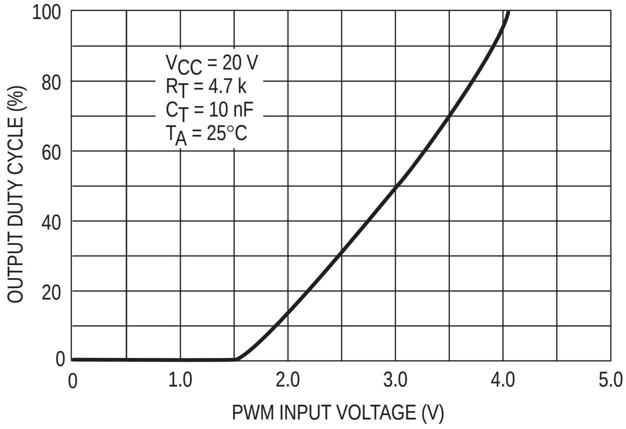


Figure 11. Bottom Drive Response Time versus Current Sense Input Voltage

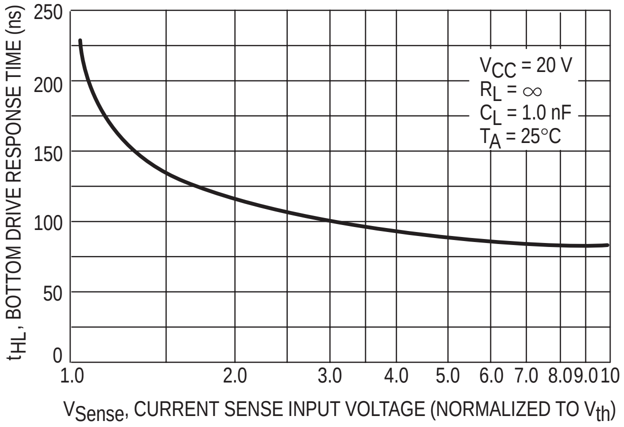


Figure 12. Top Drive Output Saturation Voltage versus Sink Current

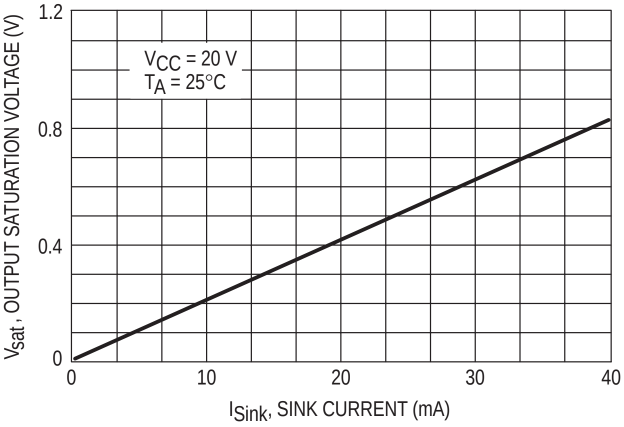


Figure 13. Top Drive Output Waveform

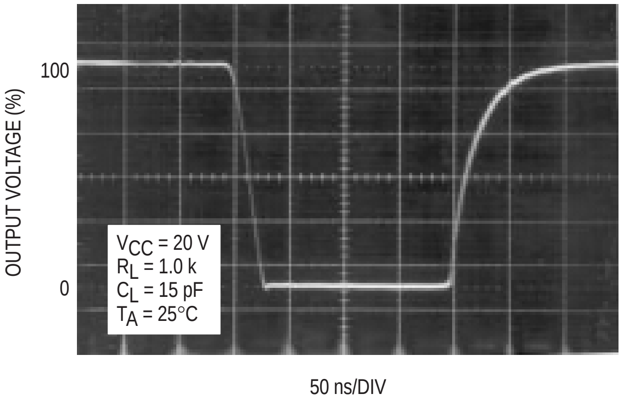


Figure 14. Bottom Drive Output Waveform

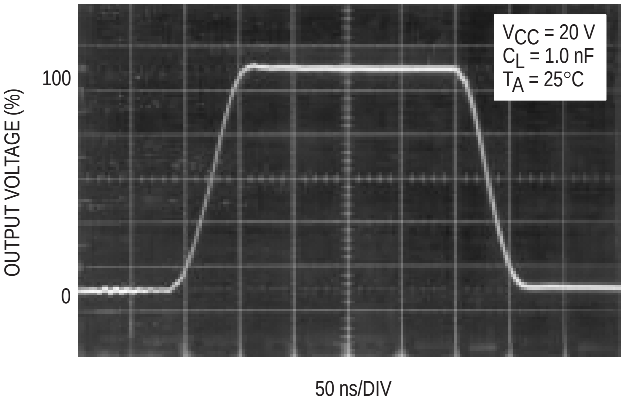


Figure 15. Bottom Drive Output Waveform

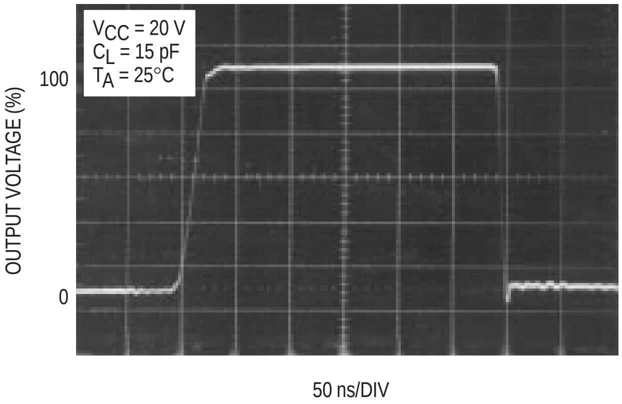


Figure 16. Bottom Drive Output Saturation Voltage versus Load Current

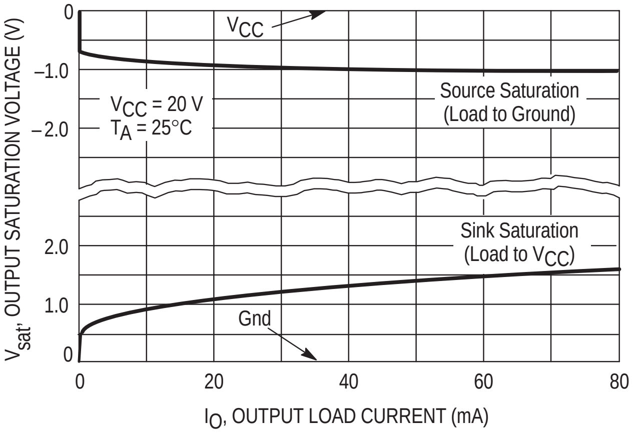
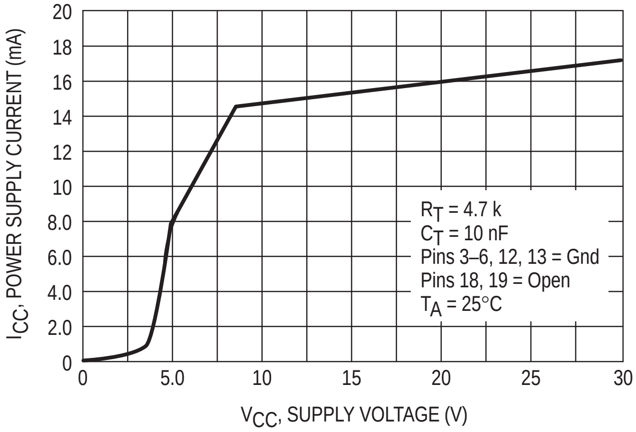


Figure 17. Supply Current versus Voltage



PIN FUNCTION DESCRIPTION

Pin	Symbol	Description
1, 2, 20	B_T, A_T, C_T	These three open collector Top Drive Outputs are designed to drive the external upper power switch transistors.
3	Fwd//Rev	The Forward/Reverse Input is used to change the direction of motor rotation.
4, 5, 6	S_A, S_B, S_C	These three Sensor Inputs control the commutation sequence.
7	Reference Output	This output provides charging current for the oscillator timing capacitor C_T and a reference for the Error Amplifier. It may also serve to furnish sensor power.
8	Oscillator	The Oscillator frequency is programmed by the values selected for the timing components, R_T and C_T.
9	Error Amp Noninverting Input	This input is normally connected to the speed set potentiometer.
10	Error Amp Inverting Input	This input is normally connected to the Error Amp Output in open loop applications.
11	Error Amp Out/PWM Input	This pin is available for compensation in closed loop applications.
12	Current Sense Noninverting Input	A 100 mV signal, with respect to Pin 13, at this input terminates output switch conduction during a given oscillator cycle. This pin normally connects to the top side of the current sense resistor.
13	Gnd	This pin supplies a separate ground return for the control circuit and should be referenced back to the power source ground.
14	V_{CC}	This pin is the positive supply of the control IC. The controller is functional over a V_{CC} range of 10 to 30 V.
15, 16, 17	C_B, B_B, A_B	These three totem pole Bottom Drive Outputs are designed for direct drive of the external bottom power switch transistors.
18	60°/$\overline{120^\circ}$ Select	The electrical state of this pin configures the control circuit operation for either 60° (high state) or 120° (low state) sensor electrical phasing inputs.
19	Output Enable	A logic high at this input causes the motor to run, while a low causes it to coast.

INTRODUCTION

The MC33033 is one of a series of high performance monolithic dc brushless motor controllers produced by Motorola. It contains all of the functions required to implement a limited–feature, open loop, three or four phase motor control system. Constructed with Bipolar Analog technology, it offers a high degree of performance and ruggedness in hostile industrial environments.The MC33033 contains a rotor position decoder for proper commutation sequencing, a temperature compensated reference capable of supplying sensor power, a frequency programmable sawtooth oscillator, a fully accessible error amplifier, a pulse width modulator comparator, three open collector top drive outputs, and three high current totem pole bottom driver outputs ideally suited for driving power MOSFETs.

Included in the MC33033 are protective features consisting of undervoltage lockout, cycle–by–cycle current limiting with a latched shutdown mode, and internal thermal shutdown.

Typical motor control functions include open loop speed control, forward or reverse rotation, and run enable. In addition, the MC33033 has a 60°/120° select pin which configures the rotor position decoder for either 60° or 120° sensor electrical phasing inputs.

FUNCTIONAL DESCRIPTION

A representative internal block diagram is shown in Figure 18, with various applications shown in Figures 34, 36, 37, 41, 43, and 44. A discussion of the features and function of each of the internal blocks given below and referenced to Figures 18 and 36.

Rotor Position Decoder

An internal rotor position decoder monitors the three sensor inputs (Pins 4, 5, 6) to provide the proper sequencing of the top and bottom drive outputs. The Sensor Inputs are designed to interface directly with open collector type Hall Effect switches or opto slotted couplers. Internal pull–up resistors are included to minimize the required number of external components. The inputs are TTL compatible, with their thresholds typically at 2.2 V. The MC33033 series is designed to control three phase motors and operate with four of the most common conventions of sensor phasing. A 60°/120° Select (Pin 18) is conveniently provided which affords the MC33033 to configure itself to control motors having either 60°, 120°, 240° or 300° electrical sensor phasing. With three Sensor Inputs there are eight possible input code combinations, six of which are valid rotor positions. The remaining two codes are invalid and are usually caused by an open or shorted sensor line. With six valid input codes, the decoder can resolve the motor rotor position to within a window of 60 electrical degrees.

The Forward/Reverse input (Pin 3) is used to change the direction of motor rotation by reversing the voltage across the stator winding. When the input changes state, from high to low with a given sensor input code (for example 100), the enabled top and bottom drive outputs with the same alpha designation are exchanged (A_T to A_B, B_T to B_B, C_T to C_B). In effect the commutation sequence is reversed and the motor changes directional rotation.

Motor on/off control is accomplished by the Output Enable (Pin19). When left disconnected, an internal pull–up resistor to a positive source enables sequencing of the top and bottom drive outputs. When grounded, the Top Drive Outputs turn off and the bottom drives are forced low, causing the motor to coast.

The commutation logic truth table is shown in Figure 19. In half wave motor drive applications, the Top Drive Outputs are not required and are typically left disconnected.

Error Amplifier

A high performance, fully compensated Error Amplifier with access to both inputs and output (Pins 9, 10, 11) is provided to facilitate the implementation of closed loop motor speed control. The amplifier features a typical dc voltage gain of 80 dB, 0.6 MHz gain bandwidth, and a wide input common mode voltage range that extends from ground to V_{ref}. In most open loop speed control applications, the amplifier is configured as a unity gain voltage follower with the Noninverting Input connected to the speed set voltage source. Additional configurations are shown in Figures 29 through 33.

Oscillator

The frequency of the internal ramp oscillator is programmed by the values selected for timing components R_T and C_T. Capacitor C_T is charged from the Reference Output (Pin 7) through resistor R_T and discharged by an internal discharge transistor. The ramp peak and valley voltages are typically 4.1 V and 1.5 V respectively. To provide a good compromise between audible noise and output switching efficiency, an oscillator frequency in the range of 20 to 30 kHz is recommended. Refer to Figure 1 for component selection.

Pulse Width Modulator

The use of pulse width modulation provides an energy efficient method of controlling the motor speed by varying the average voltage applied to each stator winding during the commutation sequence. As C_T discharges, the oscillator sets both latches, allowing conduction of the Top and Bottom Drive Outputs. The PWM comparator resets the upper latch, terminating the Bottom Drive Output conduction when the positive–going ramp of C_T becomes greater than the Error Amplifier output. The pulse width modulator timing diagram is shown in Figure 20. Pulse width modulation for speed control appears only at the Bottom Drive Outputs.

Current Limit

Continuous operation of a motor that is severely over–loaded results in overheating and eventual failure. This destructive condition can best be prevented with the use of cycle–by–cycle current limiting. That is, each on–cycle is treated as a separate event. Cycle–by–cycle current limiting is accomplished by monitoring the stator current build–up each time an output switch conducts, and upon sensing an over current condition, immediately turning off the switch and holding it off for the remaining duration of

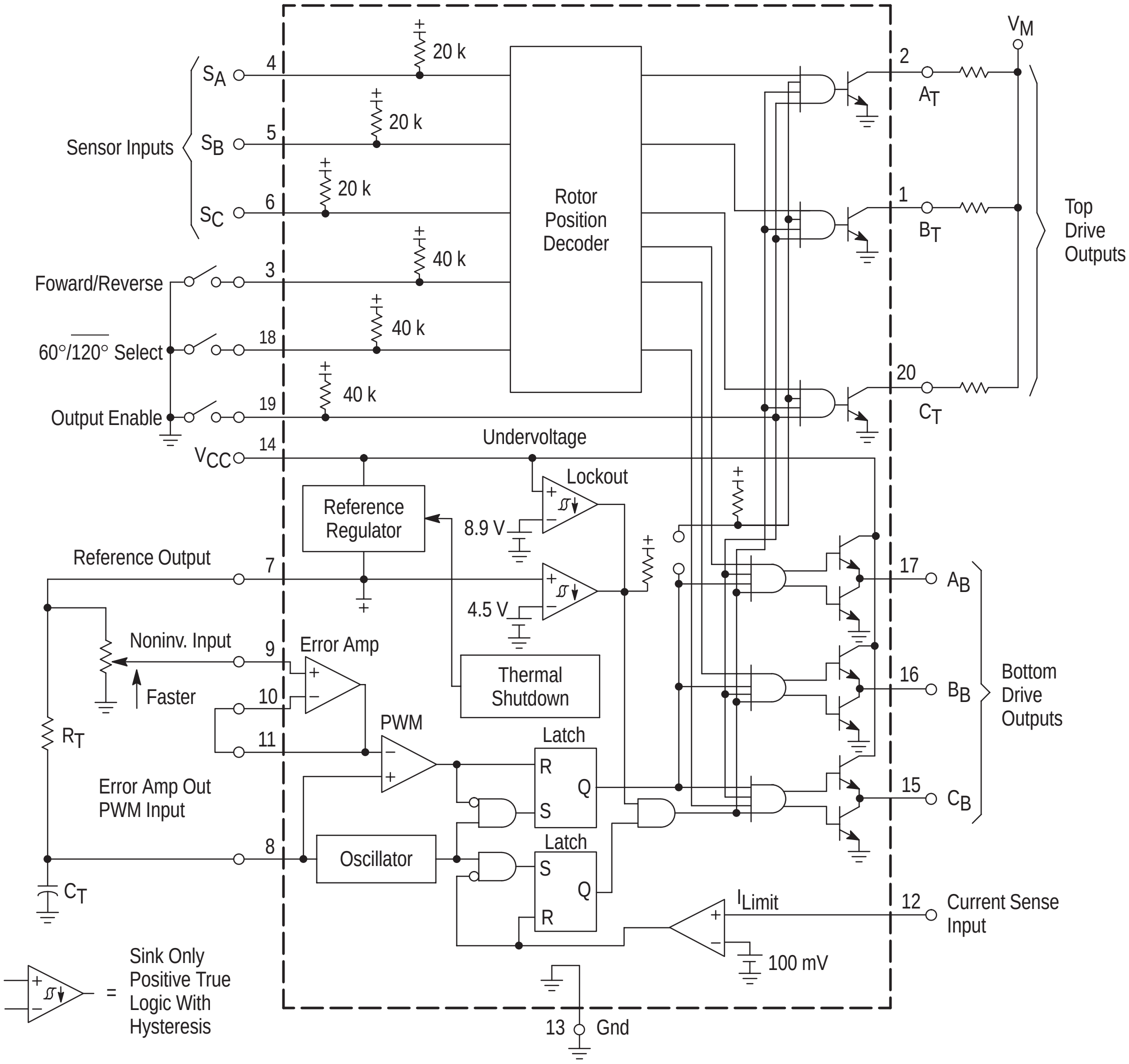


Figure 18. Representative Block Diagram

Figure 19. Three Phase, Six Step Commutation Truth Table (Note 1)

Inputs (Note 2)									Outputs (Note 3)						
Sensor Electrical Phasing (Note 4)									Top Drives			Bottom Drives			
60°			120°												
S_A	S_B	S_C	S_A	S_B	S_C	F/R	Enable	Current Sense	A_T	B_T	C_T	A_B	B_B	C_B	
1	0	0	1	0	0	1	1	0	0	1	1	0	0	1	**(Note 5)** F/R = 1
1	1	0	1	1	0	1	1	0	1	0	1	0	0	1	
1	1	1	0	1	0	1	1	0	1	0	1	1	0	0	
0	1	1	0	1	1	1	1	0	1	1	0	1	0	0	
0	0	1	0	0	1	1	1	0	1	1	0	0	1	0	
0	0	0	1	0	1	1	1	0	0	1	1	0	1	0	
1	0	0	1	0	0	0	1	0	1	1	0	1	0	0	**(Note 5)** F/R = 0
1	1	0	1	1	0	0	1	0	1	1	0	0	1	0	
1	1	1	0	1	0	0	1	0	0	1	1	0	1	0	
0	1	1	0	1	1	0	1	0	0	1	1	0	0	1	
0	0	1	0	0	1	0	1	0	1	0	1	0	0	1	
0	0	0	1	0	1	0	1	0	1	0	1	1	0	0	
1	0	1	1	1	1	X	X	X	1	1	1	0	0	0	**(Note 6)**
0	1	0	0	0	0	X	X	X	1	1	1	0	0	0	
V	V	V	V	V	V	X	0	X	1	1	1	0	0	0	**(Note 7)**
V	V	V	V	V	V	X	1	1	1	1	1	0	0	0	**(Note 8)**

NOTES:
1. V = Any one of six valid sensor or drive combinations.
   X = Don't care.
2. The digital inputs (Pins 3, 4, 5, 6, 18, 19) are all TTL compatible. The current sense input (Pin 12) has a 100 mV threshold with respect to Pin 13. A logic 0 for this input is defined as < 85 mV, and a logic 1 is > 115 mV.
3. The top drive outputs are open collector design and active in the low (0) state.
4. With 60°/120° (Pin 18) in the high (1) state, configuration is for 60° sensor electrical phasing inputs. With Pin 18 in the low (0) state, configuration is for 120° sensor electrical phasing inputs.
5. Valid 60° or 120° sensor combinations for corresponding valid top and bottom drive outputs.
6. Invalid sensor inputs; All top and bottom drives are off.
7. Valid sensor inputs with enable = 0; All top and bottom drives are off.
8. Valid sensor inputs with enable and current sense = 1; All top and bottom drives are off.

oscillator ramp–up period. The stator current is converted to a voltage by inserting a ground–referenced sense resistor R_S (Figure 34) in series with the three bottom switch transistors (Q_4, Q_5, Q_6). The voltage developed across the sense resistor is monitored by the current sense input (Pin 12), and compared to the internal 100 mV reference. If the current sense threshold is exceeded, the comparator resets the lower latch and terminates output switch conduction. The value for the sense resistor is:

$$R_S = \frac{0.1}{I_{stator(max)}}$$

The dual–latch PWM configuration ensures that only one single output conduction pulse occurs during any given oscillator cycle, whether terminated by the output of the Error Amplifier or the current limit comparator.

Reference

The on–chip 6.25 V regulator (Pin 7) provides charging current for the oscillator timing capacitor, a reference for the Error Amplifier, and can supply 20 mA of current suitable for directly powering sensors in low voltage applications. In higher voltage applications it may become necessary to transfer the power dissipated by the regulator off the IC. This is easily accomplished with the addition of an external pass transistor as shown in Figure 21. A 6.25 V reference level was chosen to allow implementation of the simpler NPN circuit, where $V_{ref} – V_{BE}$ exceeds the minimum voltage required by Hall Effect sensors over temperature. With proper transistor selection, and adequate heatsinking, up to one amp of load current can be obtained.

Undervoltage Lockout

A dual Undervoltage Lockout has been incorporated to prevent damage to the IC and the external power switch transistors. Under low power supply conditions, it guarantees that the IC and sensors are fully functional, and that there is sufficient Bottom Drive Output voltage. The positive power supply to the IC (V_{CC}) is monitored to a threshold of 8.9 V. This level ensures sufficient gate drive necessary to attain low $R_{DS(on)}$ when interfacing with standard power MOSFET devices. When directly powering the Hall sensors from the reference, improper sensor operation can result if the reference output voltage should fall below 4.5 V. If one or both of the comparators detects an undervoltage condition, the top drives are turned off and the Bottom Drive Outputs are held in a low state. Each of the comparators contain hysteresis to prevent oscillations when crossing their respective thresholds.

Figure 20. PWM Timing Diagram

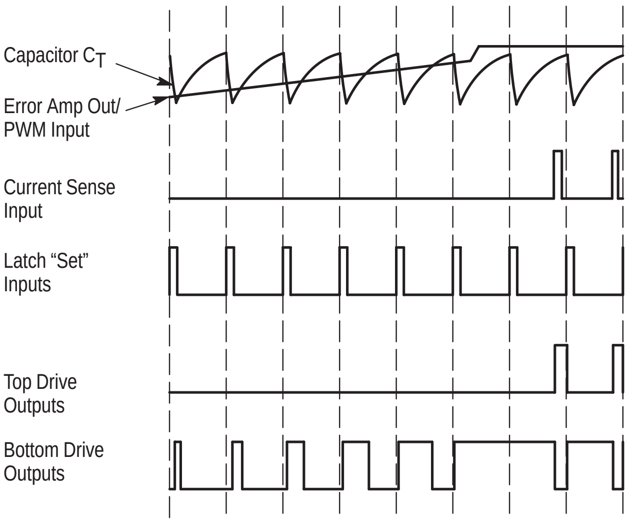
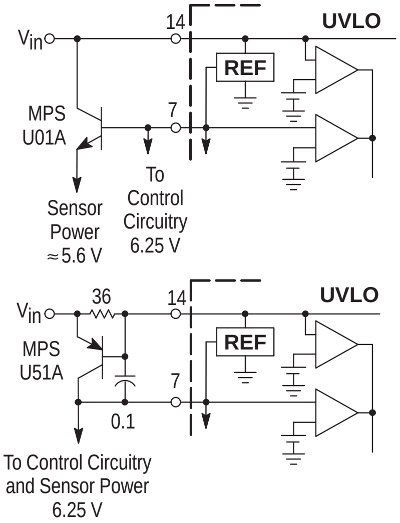
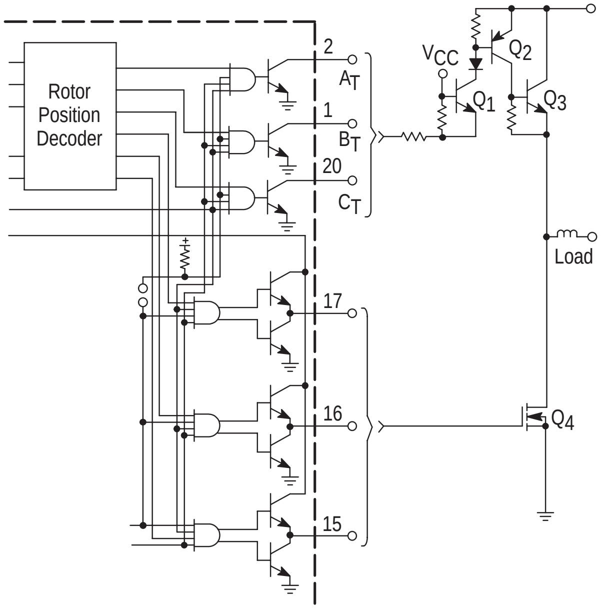


Figure 21. Reference Output Buffers



The NPN circuit is recommended for powering Hall or opto sensors, where the output voltage temperature coefficient is not critical. The PNP circuit is slightly more complex, but also more accurate. Neither circuit has current limiting.

Figure 22. High Voltage Interface with NPN Power Transistors



Transistor Q_1 is a common base stage used to level shift from V_{CC} to the high motor voltage, V_M. The collector diode is required if V_{CC} is present while V_M is low.

Figure 23. High Voltage Interface with N–Channel Power MOSFETs

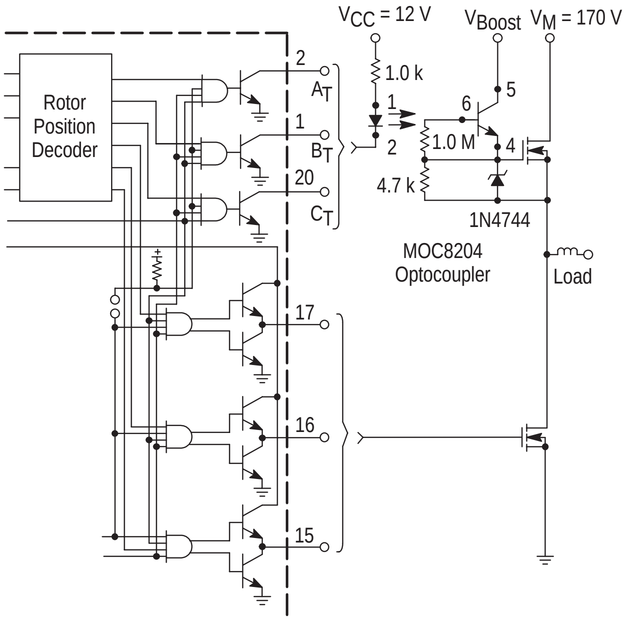
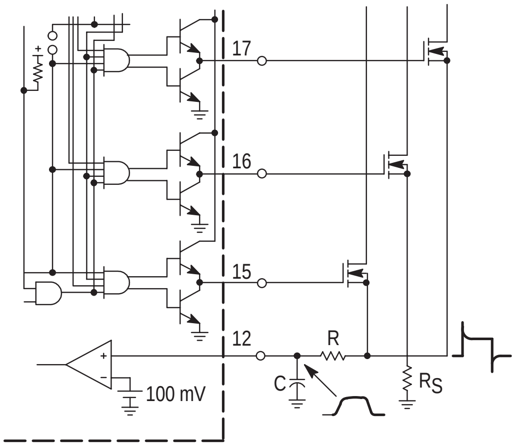
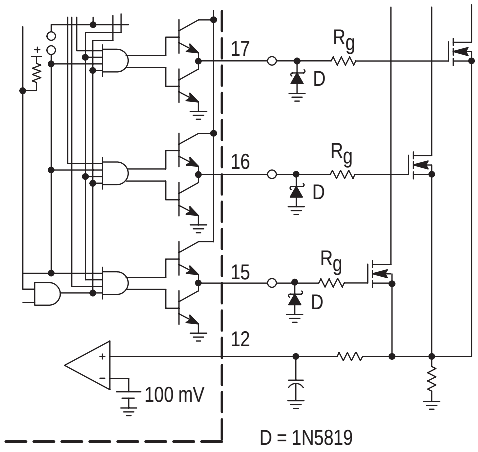


Figure 24. Current Waveform Spike Suppression



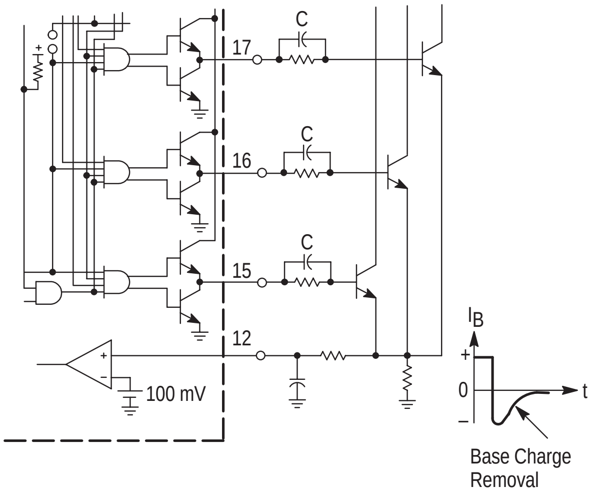
The addition of the RC filter will eliminate current–limit instability caused by the leading edge spike on the current waveform. Resistor R_S should be a low inductance type.

Figure 25. MOSFET Drive Precautions



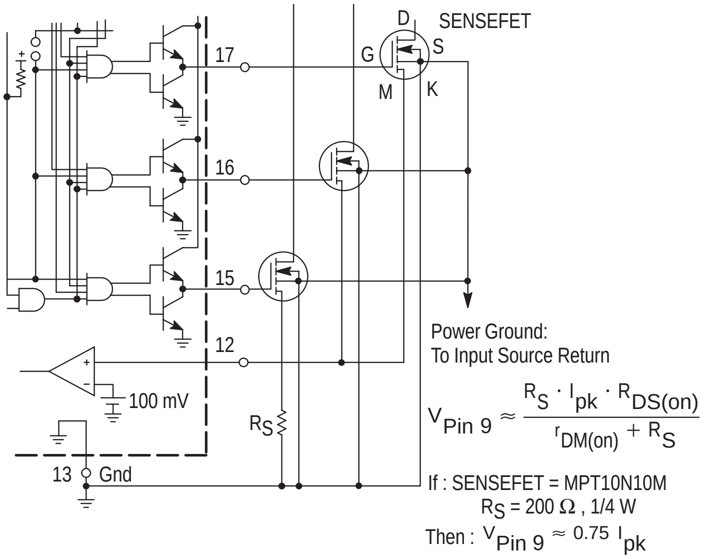
Series gate resistor R_g will damp any high frequency oscillations caused by the MOSFET input capacitance and any series wiring induction in the gate–source circuit. Diode D is required if the negative current into the Bottom Drive Outputs exceeds 50 mA.

Figure 26. Bipolar Transistor Drive



The totem pole output can furnish negative base current for enhanced transistor turn–off, with the addition of capacitor C.

Figure 27. Current Sensing Power MOSFETs

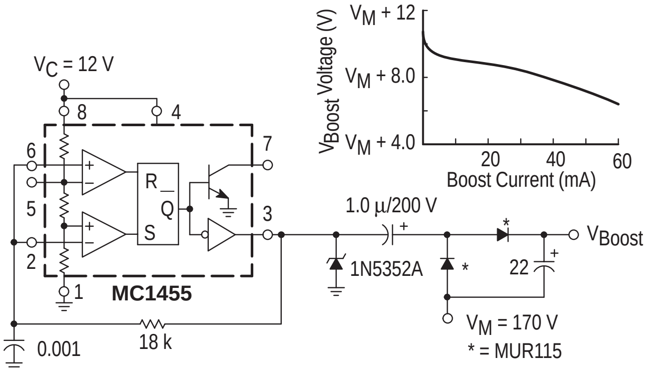


$$V_{Pin\ 9} \approx \frac{R_S \cdot I_{pk} \cdot R_{DS(on)}}{r_{DM(on)} + R_S}$$

If : SENSEFET = MPT10N10M
$R_S = 200\ \Omega$, 1/4 W
Then : $V_{Pin\ 9} \approx 0.75\ I_{pk}$

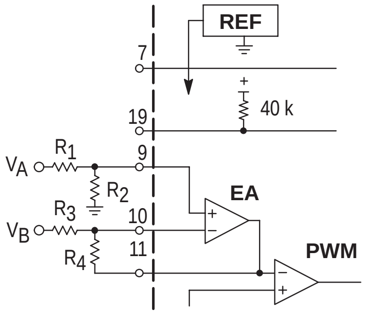
Virtually lossless current sensing can be achieved with the implementation of SENSEFET power switches.

Figure 28. High Voltage Boost Supply



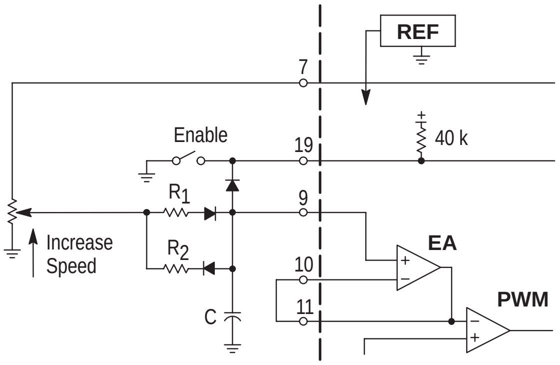
This circuit generates V_{Boost} for Figure 23.

Figure 29. Differential Input Speed Controller



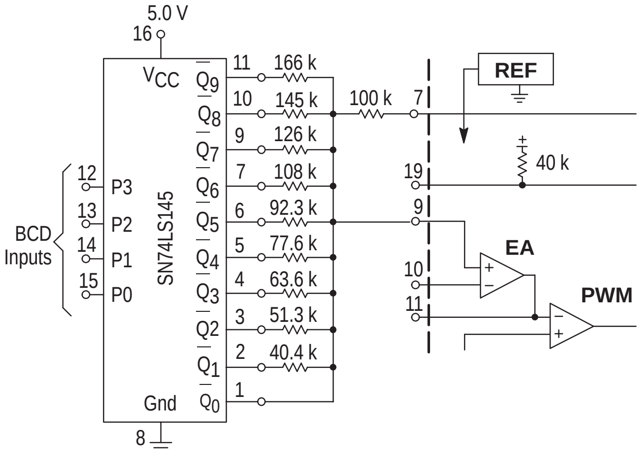
$$V_{Pin\ 11} = V_A \left(\frac{R_3 + R_4}{R_1 + R_2}\right) \frac{R_2}{R_3} - \left(\frac{R_4}{R_3}\ V_B\right)$$

Figure 30. Controlled Acceleration/Deceleration



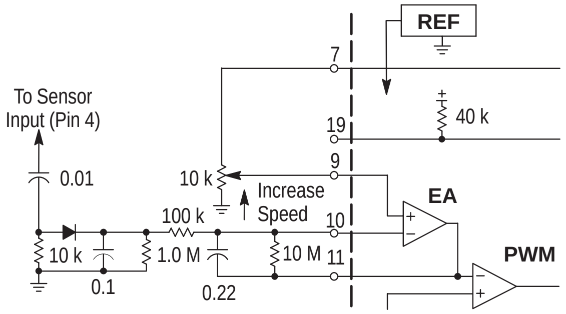
Resistor R_1 with capacitor C sets the acceleration time constant while R_2 controls the deceleration. The values of R_1 and R_2 should be at least ten times greater than the speed set potentiometer to minimize time constant variations with different speed settings.

Figure 31. Digital Speed Controller



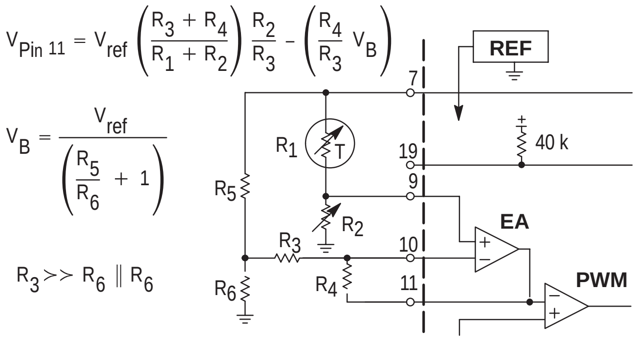
The SN74LS145 is an open collector BCD to One of Ten decoder. When connected as shown, input codes 0000 through 1001 steps the PWM in increments of approximately 10% from 0 to 90% on–time. Input codes 1010 through 1111 will produce 100% on–time or full motor speed.

Figure 32. Closed Loop Speed Control



The rotor position sensors can be used as a tachometer. By differentiating the positive–going edges and then integrating them over time, a voltage proportional to speed can be generated. The error amp compares this voltage to that of the speed set to control the PWM.

Figure 33. Closed Loop Temperature Control



$$V_{Pin\ 11} = V_{ref}\left(\frac{R_3 + R_4}{R_1 + R_2}\right)\frac{R_2}{R_3} - \left(\frac{R_4}{R_3}\,V_B\right)$$

$$V_B = \frac{V_{ref}}{\left(\frac{R_5}{R_6} + 1\right)}$$

$$R_3 >> R_6 \parallel R_6$$

This circuit can control the speed of a cooling fan proportional to the difference between the sensor and set temperatures. The control loop is closed as the forced air cools the NTC thermistor. For controlled heating applications, exchange the positions of R_1 and R_2.

Drive Outputs

The three Top Drive Outputs (Pins 1, 2, 20) are open collector NPN transistors capable of sinking 50 mA with a minimum breakdown of 30 V. Interfacing into higher voltage applications is easily accomplished with the circuits shown in Figures 22 and 23.

The three totem pole Bottom Drive Outputs (Pins 15, 16, 17) are particularly suited for direct drive of N–Channel MOSFETs or NPN bipolar transistors (Figures 24, 25, 26, and 27). Each output is capable of sourcing and sinking up to 100 mA.

Thermal Shutdown

Internal thermal shutdown circuity is provided to protect the IC in the event the maximum junction temperature is exceeded. When activated, typically at 170°C, the IC acts as though the regulator was disabled, in turn shutting down the IC.

SYSTEM APPLICATIONS

Three Phase Motor Commutation

The three phase application shown in Figure 34 is an open loop motor controller with full wave, six step drive. The upper power switch transistors are Darlington PNPs while the lower switches are N–Channel power MOSFETs. Each of these devices contains an internal parasitic catch diode that is used to return the stator inductive energy back to the power supply. The outputs are capable of driving a delta or wye connected stator, and a grounded neutral wye if split supplies are used. At any given rotor position, only one top and one bottom power switch (of different totem poles) is enabled. This configuration switches both ends of the stator winding from supply to ground which causes the current flow to be bidirectional or full wave. A leading edge spike is usually present on the current waveform and can cause a current–limit error. The spike can be eliminated by adding an RC filter in series with the Current Sense Input. Using a low inductance type resistor for R_S will also aid in spike reduction. Figure 35 shows the commutation waveforms over two electrical cycles. The first cycle (0° to 360°) depicts motor operation at full speed while the second cycle (360° to 720°) shows a reduced speed with about 50% pulse width modulation. The current waveforms reflect a constant torque load and are shown synchronous to the commutation frequency for clarity.

Figure 34. Three Phase, Six Step, Full Wave Motor Controller

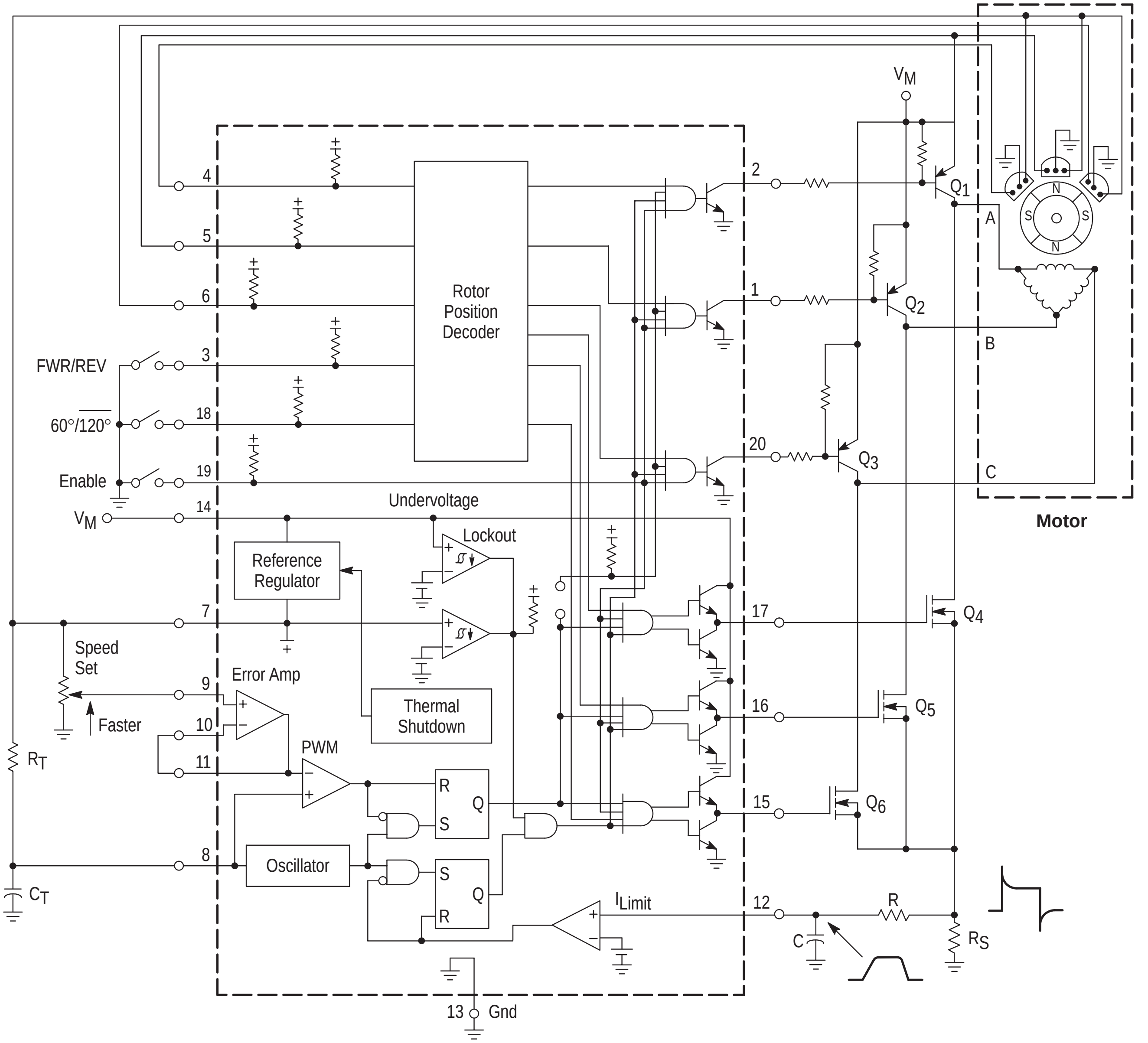


Figure 35. Three Phase, Six Step, Full Wave Commutation Waveforms

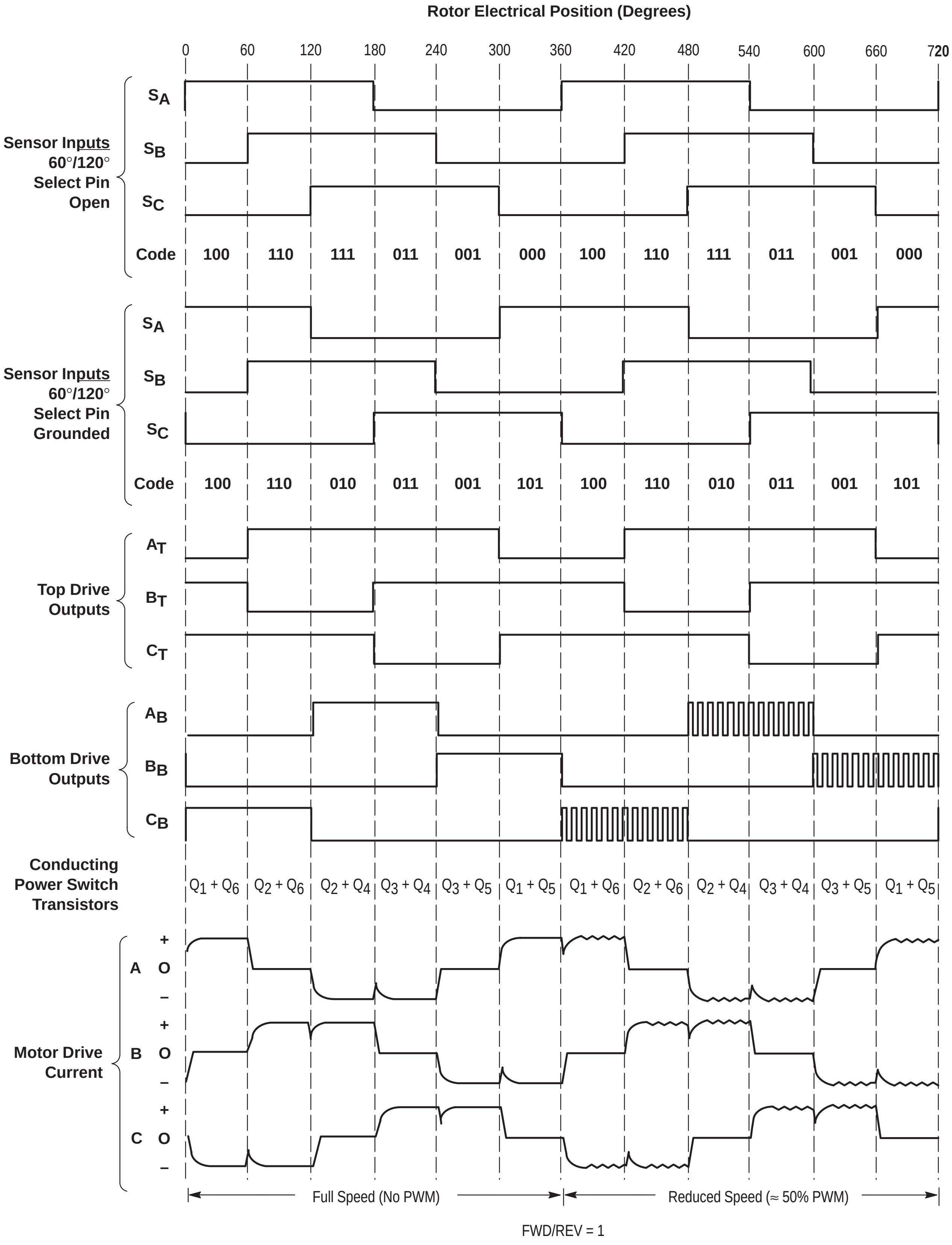
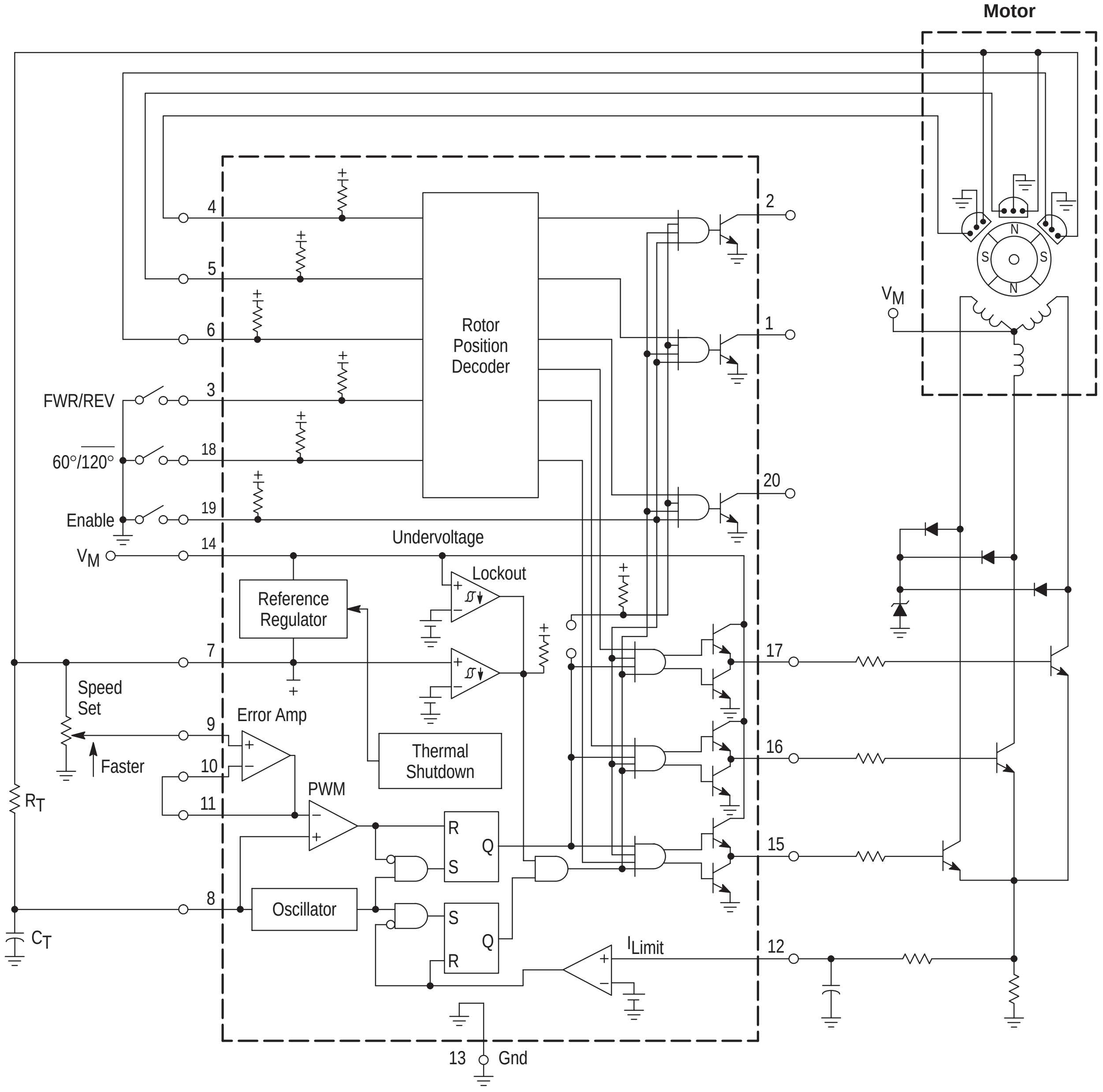


Figure 36 shows a three phase, three step, half wave motor controller. This configuration is ideally suited for automobile and other low voltage applications since there is only one power switch voltage drop in series with a given stator winding. Current flow is unidirectional or half wave because only one end of each winding is switched. The stator flyback voltage is clamped by a single zener and three diodes.

Figure 36. Three Phase, Three Step, Half Wave Motor Controller

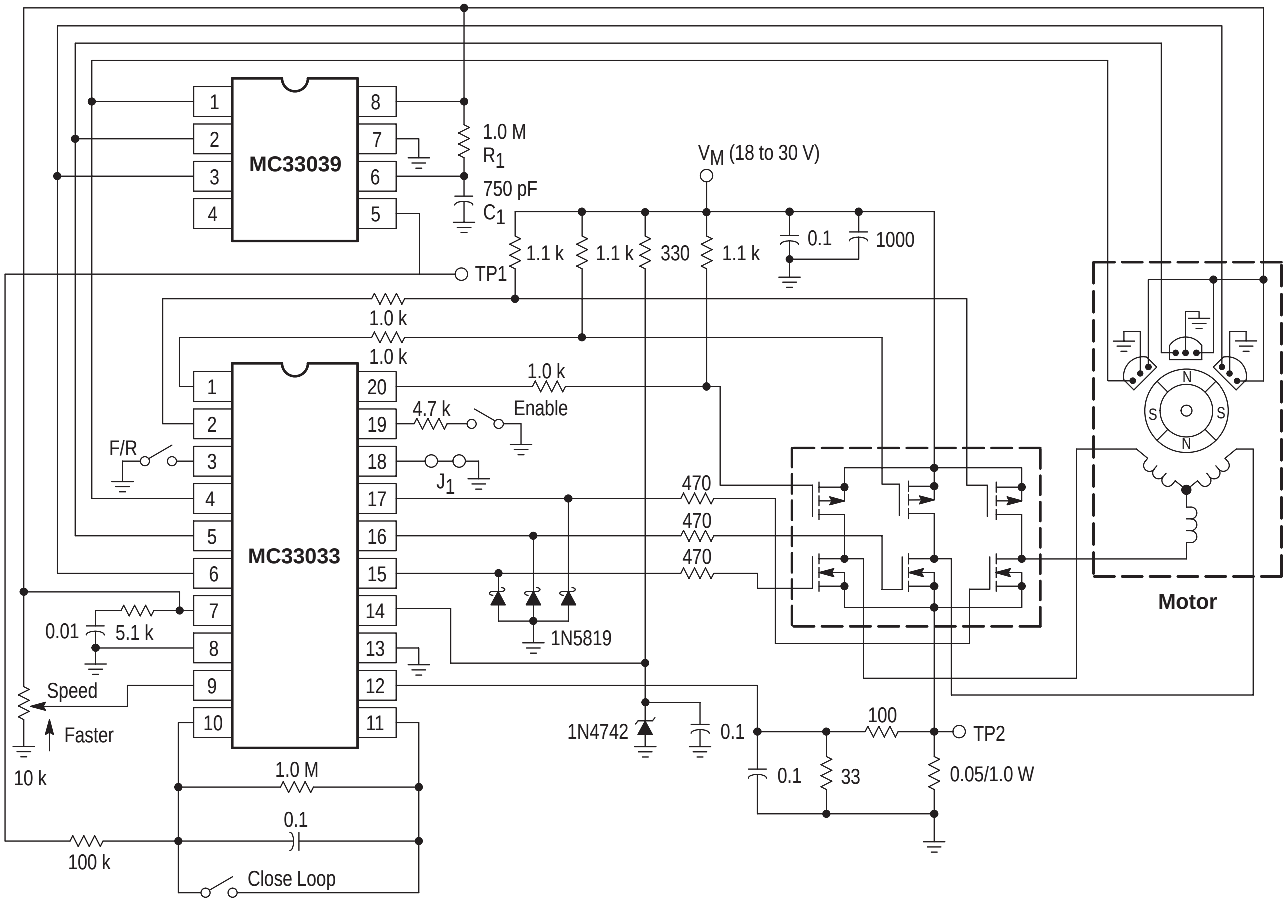


Three Phase Closed Loop Controller

The MC33033, by itself, is capable of open loop motor speed control. For closed loop speed control, the MC33033 requires an input voltage proportional to the motor speed. Traditionally this has been accomplished by means of a tachometer to generate the motor speed feedback voltage. Figure 37 shows an application whereby an MC33039, powered from the 6.25 V reference (Pin 7) of the MC33033, is used to generate the required feedback voltage without the need of a costly tachometer. The same Hall sensor signals used by the MC33033 for rotor position decoding are utilized by the MC33039. Every positive or negative going transition of the Hall sensor signals on any of the sensor lines causes the MC33039 to produce an output pulse of defined amplitude and time duration, as determined by the external resistor R_1 and capacitor C_1. The resulting output train of pulses present at Pin 5 of the MC33039 are integrated by the Error Amplifier of the MC33033 configured as an integrator, to produce a dc voltage level which is proportional to the motor speed. This speed proportional voltage establishes the PWM reference level at Pin 11 of the MC33033 motor controller and completes or closes the feedback loop. The MC33033 ouputs drive a TMOS power MOSFET 3–phase bridge. High current can be expected during conditions of start–up and when changing direction of the motor.

The system shown in Figure 37 is designed for a motor having 120/240 degrees Hall sensor electrical phasing. The system can easily be modified to accommodate 60/300 degree Hall sensor electrical phasing by removing the jumper (J_1) at Pin 18 of the MC33033.

Figure 37. Closed Loop Brushless DC Motor Control With the MC33033 Using the MC33039



Sensor Phasing Comparison

There are four conventions used to establish the relative phasing of the sensor signals in three phase motors. With six step drive, an input signal change must occur every 60 electrical degrees, however, the relative signal phasing is dependent upon the mechanical sensor placement. A comparison of the conventions in electrical degrees is shown in Figure 38. From the sensor phasing table (Figure 39), note that the order of input codes for 60° phasing is the reverse of 300°. This means the MC33033, when the 60°/120° select (Pin 18) and the FWD/REV (Pin 3) both in the high state (open), is configured to operate a 60° sensor phasing motor in the forward direction. Under the same conditions a 300° sensor phasing motor would operate equally well but in the reverse direction. One would simply have to reverse the FWD/REV switch (FWD/REV closed) in order to cause the 300° motor to also operate in the same direction. The same difference exists between the 120° and 240° conventions.

Figure 38. Sensor Phasing Comparison

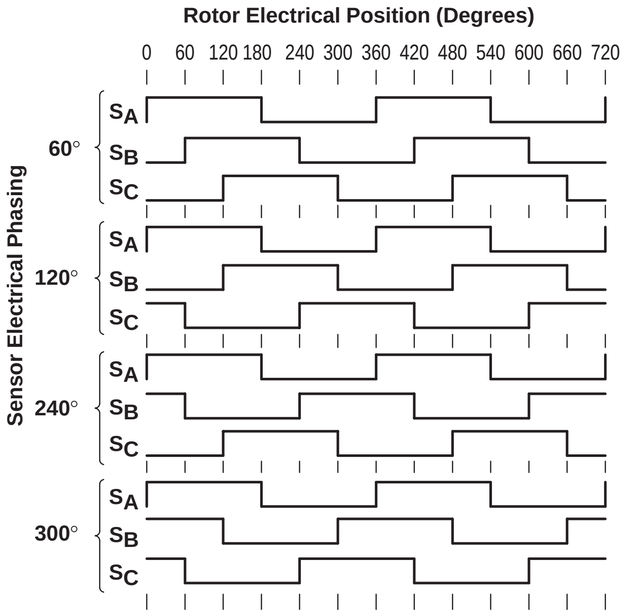


Figure 39. Sensor Phasing Table

Sensor Electrical Phasing (Degrees)											
60°			120°			240°			300°		
S_A	S_B	S_C	S_A	S_B	S_C	S_A	S_B	S_C	S_A	S_B	S_C
1	**0**	**0**	1	0	1	1	1	0	1	**1**	1
1	**1**	0	1	0	0	1	0	0	1	**1**	0
1	**1**	1	1	1	0	1	0	1	**1**	**0**	**0**
0	1	1	0	1	0	0	0	1	0	0	0
0	0	1	0	1	1	0	1	1	0	0	1
0	0	0	0	0	1	0	1	0	0	1	1

In this data sheet, the rotor position has always been given in electrical degrees since the mechanical position is a function of the number of rotating magnetic poles. The relationship between the electrical and mechanical position is:

$$\text{Electrical Degrees} = \text{Mechanical Degrees}\left(\frac{\#\text{Rotor Poles}}{2}\right)$$

An increase in the number of magnetic poles causes more electrical revolutions for a given mechanical revolution. General purpose three phase motors typically contain a four pole rotor which yields two electrical revolutions for one mechanical.

Two and Four Phase Motor Commutation

The MC33033 configured for 60° sensor inputs is capable of providing a four step output that can be used to drive two or four phase motors. The truth table in Figure 40 shows that by connecting sensor inputs S_B and S_C together, it is possible to truncate the number of drive output states from six to four. The output power switches are connected to B_T, C_T, B_B, and C_B. Figure 41 shows a four phase, four step, full wave motor control application. Power switch transistors Q_1 through Q_8 are Darlington type, each with an internal parasitic catch diode. With four step drive, only two rotor position sensors spaced at 90 electrical degrees are required. The commutation waveforms are shown in Figure 42.

Figure 43 shows a four phase, four step, half wave motor controller. It has the same features as the circuit in Figure 36, except for the deletion of speed adjust.

Figure 40. Two and Four Phase, Four Step, Commutation Truth Table

MC33033 (60°/$\overline{120}$° Select Pin Open)						
Inputs			Outputs			
Sensor Electrical Spacing* = 90°			Top Drives		Bottom Drives	
S_A	S_B	F/R	B_T	C_T	B_B	C_B
1	0	1	1	1	0	1
1	1	1	0	1	0	0
0	1	1	1	0	0	0
0	0	1	1	1	1	0
1	0	0	1	0	0	0
1	1	0	1	1	1	0
0	1	0	1	1	0	1
0	0	0	0	1	0	0

*With MC33033 sensor input S_B connected to S_C

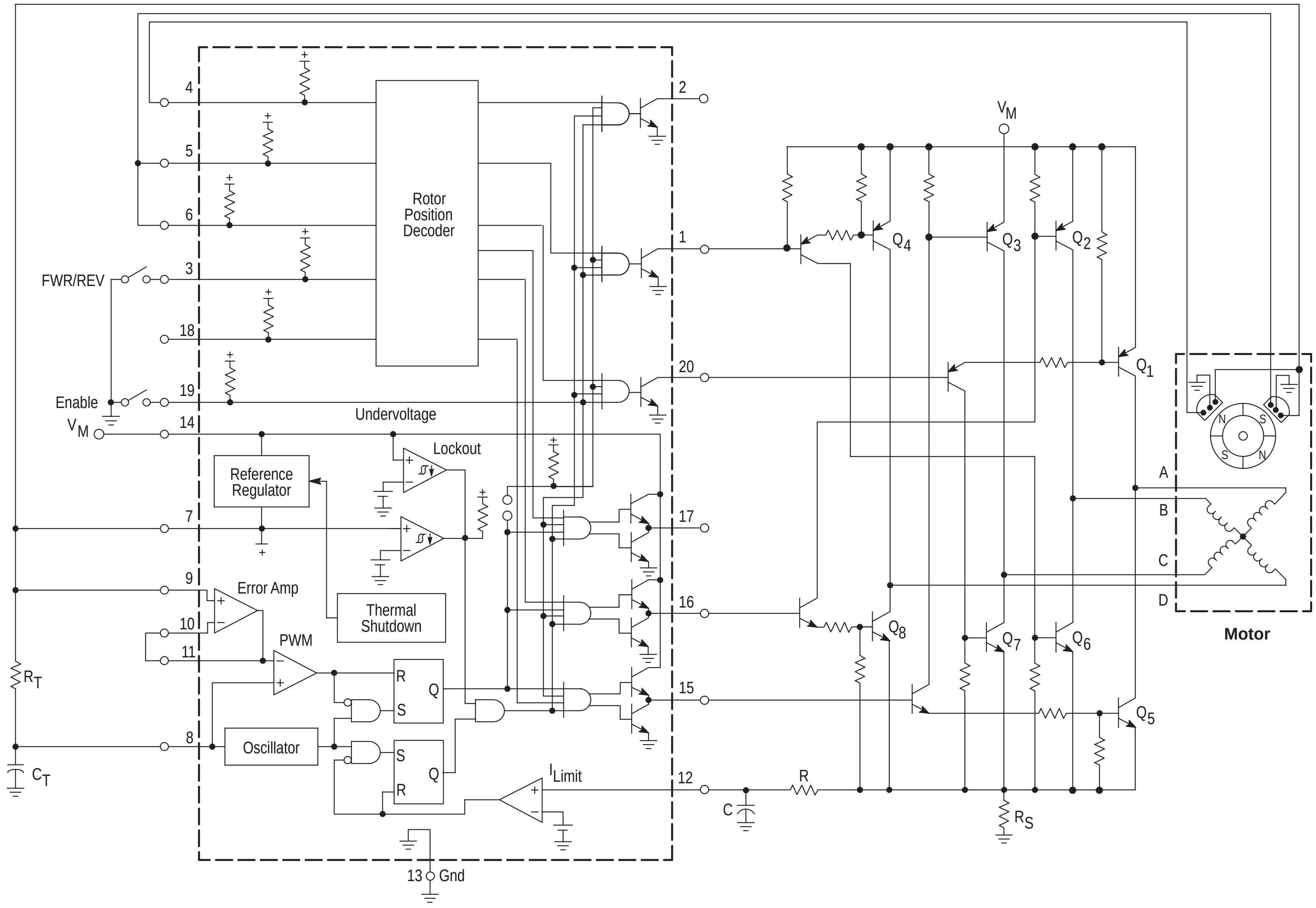


Figure 41. Four Phase, Four Step, Full Wave Controller

Figure 42. Four Phase, Four Step, Full Wave Commutation Waveforms

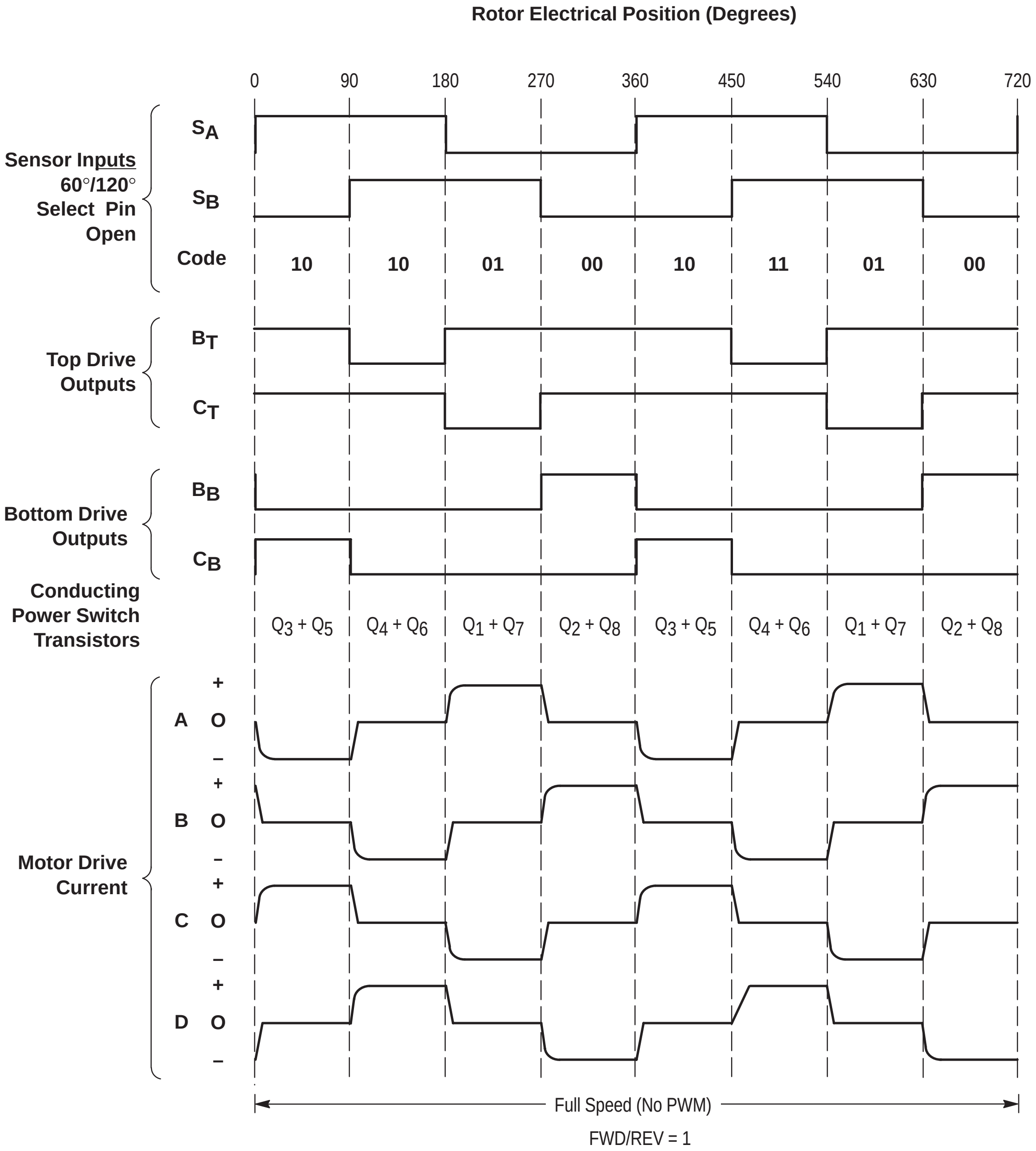
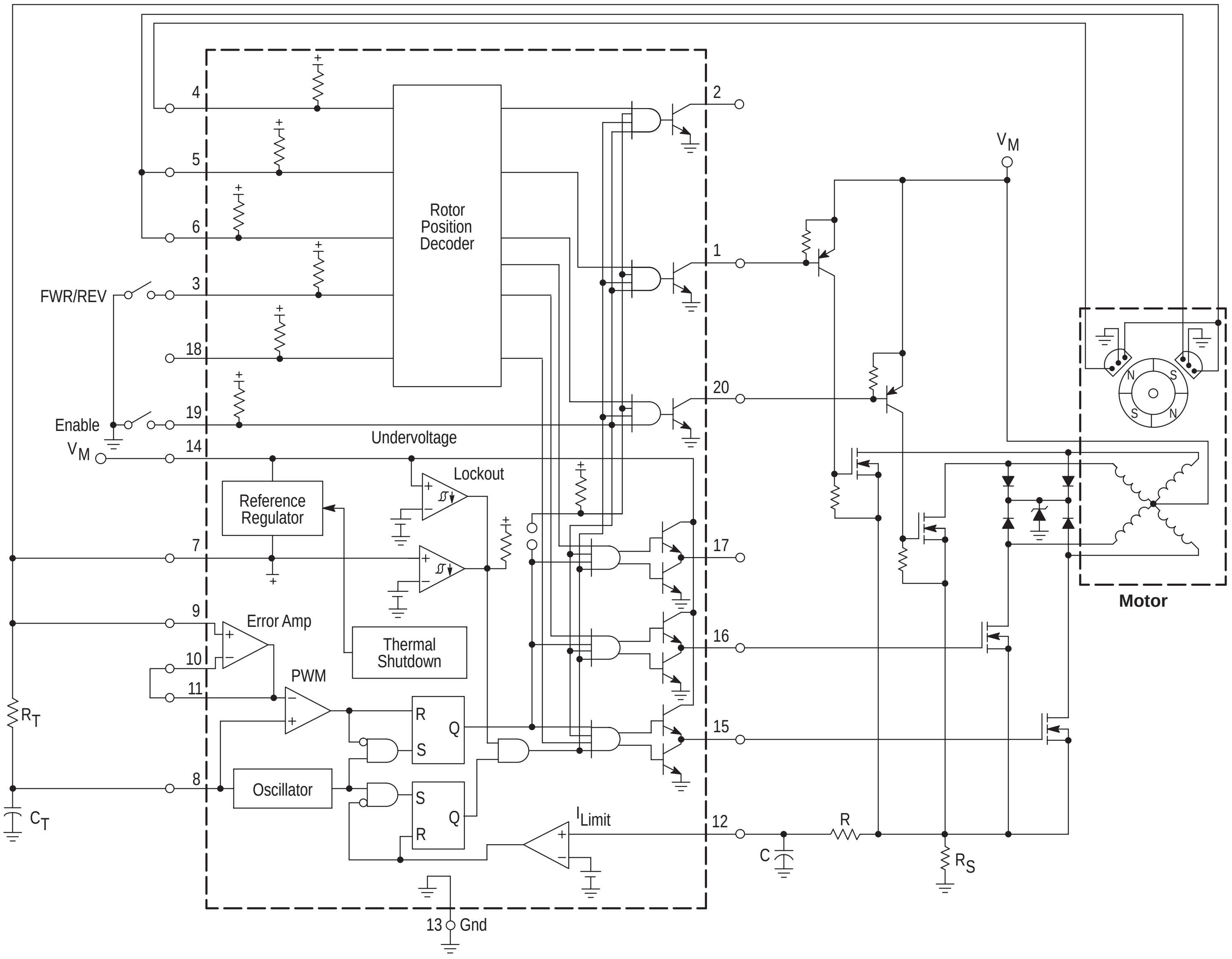


Figure 43. Four Phase, Four Step, Half Wave Motor Controller



Brush Motor Control

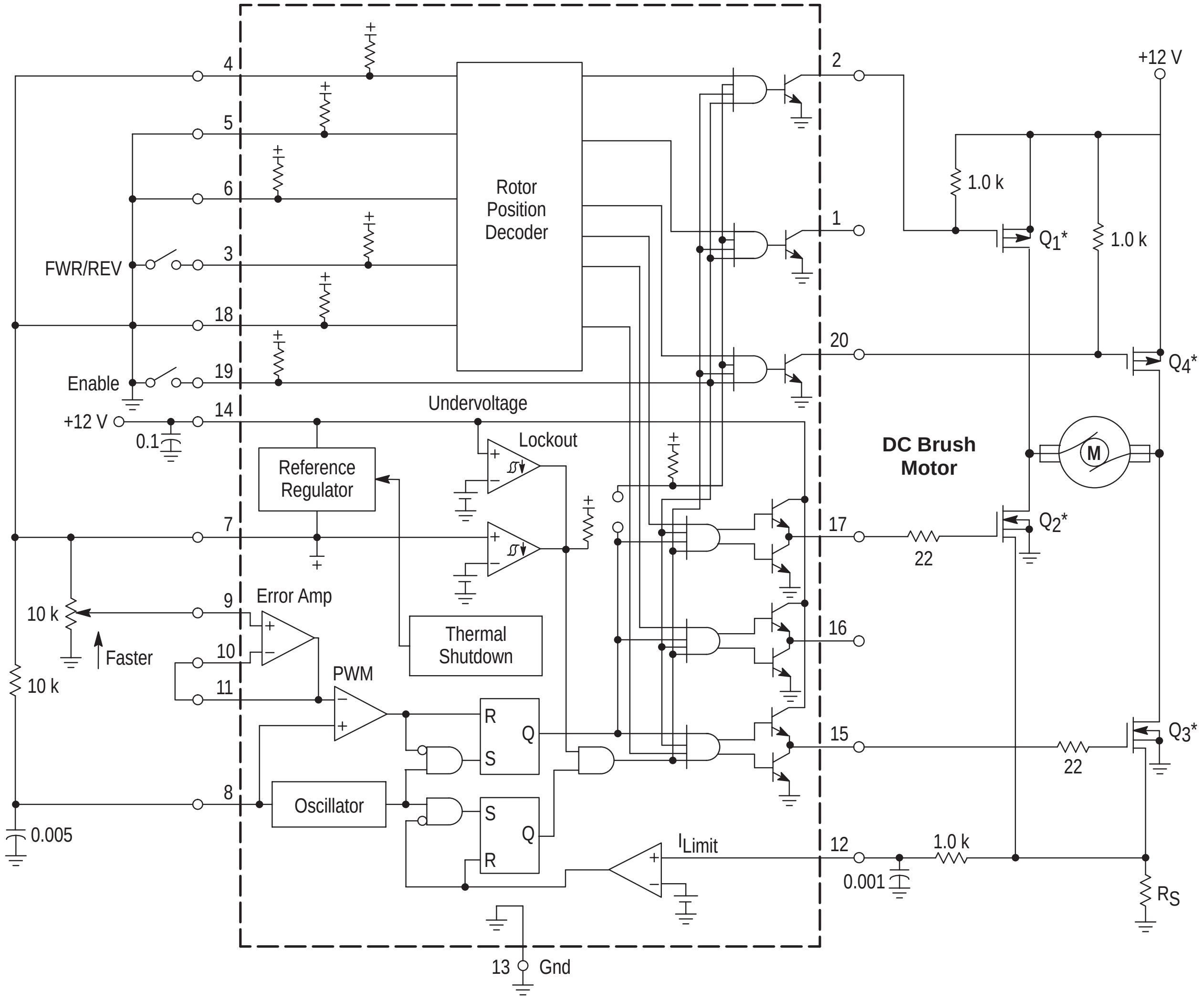
Though the MC33033 was designed to control brushless dc motors, it may also be used to control dc brush–type motors. Figure 44 shows an application of the MC33033 driving a H–bridge affording minimal parts count to operate a brush–type motor. Key to the operation is the input sensor code [100] which produces a top–left (Q_1) and a bottom–right (Q_3) drive when the controller's Forward/Reverse pin is at logic [1]; top–right (Q_4), bottom–left (Q_2) drive is realized when the Forward/Reverse pin is at logic [0]. This code supports the requirements necessary for H–bridge drive accomplishing both direction and speed control.

The controller functions in a normal manner with a pulse width modulated frequency of approximately 25 kHz. Motor speed is controlled by adjusting the voltage presented to the noninverting input of the Error Amplifier establishing the PWM′s slice or reference level. Cycle–by–cycle current limiting of the motor current is accomplished by sensing the voltage (100 mV threshold) across the R_S resistor to ground of the H–bridge motor current. The over current sense circuit makes it possible to reverse the direction of the motor, on the fly, using the normal Forward/Reverse switch, and not have to completely stop before reversing.

LAYOUT CONSIDERATIONS

Do not attempt to construct any of the motor control circuits on wire–wrap or plug–in prototype boards. High frequency printed circuit layout techniques are imperative to prevent pulse jitter. This is usually caused by excessive noise pick–up imposed on the current sense or error amp inputs. The printed circuit layout should contain a ground plane with low current signal and high drive and output buffer grounds returning on separate paths back to the power supply input filter capacitor V_M. Ceramic bypass capacitors (0.01 µF) connected close to the integrated circuit at V_{CC}, V_{ref} and error ampliflier noninverting input may be required depending upon circuit layout. This provides a low impedance path for filtering any high frequency noise. All high current loops should be kept as short as possible using heavy copper runs to minimize radiated EMI.

Figure 44. H–Bridge Brush–Type Controller



MOTOROLA

MC33035

Brushless DC Motor Controller

The MC33035 is a high performance second generation monolithic brushless DC motor controller containing all of the active functions required to implement a full featured open loop, three or four phase motor control system. This device consists of a rotor position decoder for proper commutation sequencing, temperature compensated reference capable of supplying sensor power, frequency programmable sawtooth oscillator, three open collector top drivers, and three high current totem pole bottom drivers ideally suited for driving power MOSFETs.

Also included are protective features consisting of undervoltage lockout, cycle–by–cycle current limiting with a selectable time delayed latched shutdown mode, internal thermal shutdown, and a unique fault output that can be interfaced into microprocessor controlled systems.

Typical motor control functions include open loop speed, forward or reverse direction, run enable, and dynamic braking. The MC33035 is designed to operate with electrical sensor phasings of 60°/300° or 120°/240°, and can also efficiently control brush DC motors.

- 10 to 30 V Operation
- Undervoltage Lockout
- 6.25 V Reference Capable of Supplying Sensor Power
- Fully Accessible Error Amplifier for Closed Loop Servo Applications
- High Current Drivers Can Control External 3–Phase MOSFET Bridge
- Cycle–By–Cycle Current Limiting
- Pinned–Out Current Sense Reference
- Internal Thermal Shutdown
- Selectable 60°/300° or 120°/240° Sensor Phasings
- Can Efficiently Control Brush DC Motors with External MOSFET H–Bridge

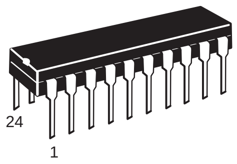
ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC33035DW	$T_A = -40°$ to $+85°C$	SO–24L
MC33035P		Plastic DIP

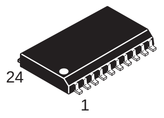
BRUSHLESS DC MOTOR CONTROLLER

SEMICONDUCTOR TECHNICAL DATA

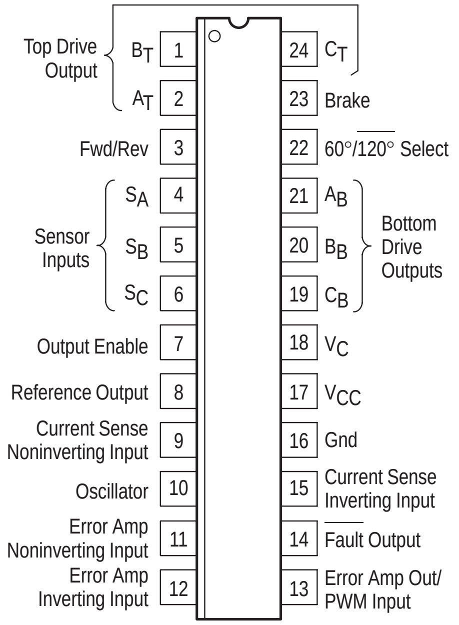
P SUFFIX
PLASTIC PACKAGE
CASE 724



DW SUFFIX
PLASTIC PACKAGE
CASE 751E
(SO–24L)

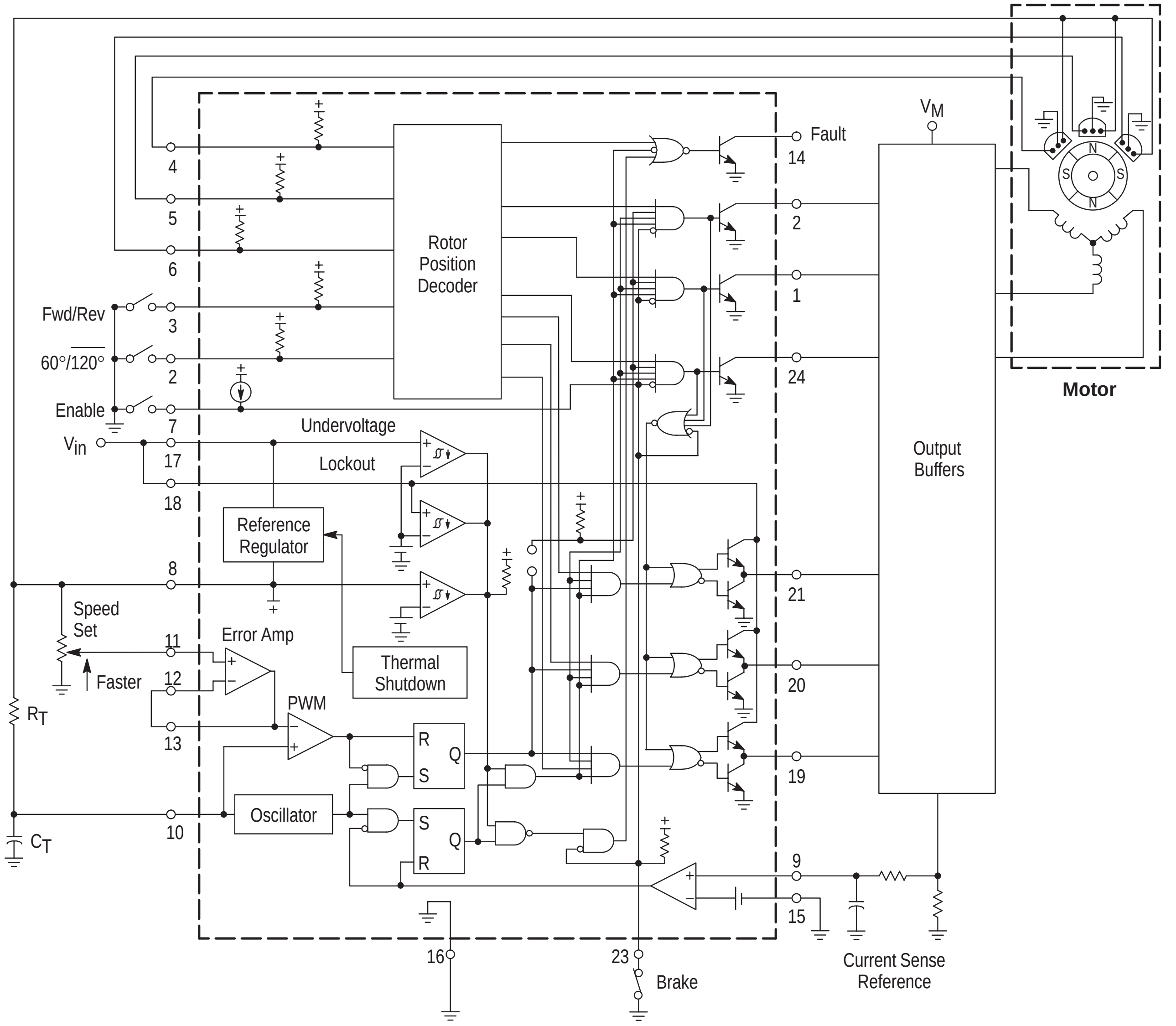


PIN CONNECTIONS



(Top View)

Representative Schematic Diagram



This device contains 285 active transistors.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	40	V
Digital Inputs (Pins 3, 4, 5, 6, 22, 23)	–	V_{ref}	V
Oscillator Input Current (Source or Sink)	I_{OSC}	30	mA
Error Amp Input Voltage Range (Pins 11, 12, Note 1)	V_{IR}	–0.3 to V_{ref}	V
Error Amp Output Current (Source or Sink, Note 2)	I_{Out}	10	mA
Current Sense Input Voltage Range (Pins 9, 15)	V_{Sense}	–0.3 to 5.0	V
$\overline{\text{Fault}}$ Output Voltage	$V_{CE(\overline{Fault})}$	20	V
$\overline{\text{Fault}}$ Output Sink Current	$I_{Sink(\overline{Fault})}$	20	mA
Top Drive Voltage (Pins 1, 2, 24)	$V_{CE(top)}$	40	V
Top Drive Sink Current (Pins 1, 2, 24)	$I_{Sink(top)}$	50	mA
Bottom Drive Supply Voltage (Pin 18)	V_C	30	V
Bottom Drive Output Current (Source or Sink, Pins 19, 20, 21)	I_{DRV}	100	mA
Power Dissipation and Thermal Characteristics P Suffix, Dual In Line, Case 724 Maximum Power Dissipation @ T_A = 85°C Thermal Resistance, Junction–to–Air DW Suffix, Surface Mount, Case 751E Maximum Power Dissipation @ T_A = 85°C Thermal Resistance, Junction–to–Air	 P_D $R_{\theta JA}$ P_D $R_{\theta JA}$	 867 75 650 100	 mW °C/W mW °C/W
Operating Junction Temperature	T_J	150	°C
Operating Ambient Temperature Range	T_A	–40 to +85	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = V_C = 20 V, R_T = 4.7 k, C_T = 10 nF, T_A = 25°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
REFERENCE SECTION					
Reference Output Voltage (I_{ref} = 1.0 mA) T_A = 25°C T_A = –40° to +85°C	V_{ref}	 5.9 5.82	 6.24 –	 6.5 6.57	V
Line Regulation (V_{CC} = 10 to 30 V, I_{ref} = 1.0 mA)	Reg_{line}	–	1.5	30	mV
Load Regulation (I_{ref} = 1.0 to 20 mA)	Reg_{load}	–	16	30	mV
Output Short Circuit Current (Note 3)	I_{SC}	40	75	–	mA
Reference Under Voltage Lockout Threshold	V_{th}	4.0	4.5	5.0	V
ERROR AMPLIFIER					
Input Offset Voltage (T_A = –40° to +85°C)	V_{IO}	–	0.4	10	mV
Input Offset Current (T_A = –40° to +85°C)	I_{IO}	–	8.0	500	nA
Input Bias Current (T_A = –40° to +85°C)	I_{IB}	–	–46	–1000	nA
Input Common Mode Voltage Range	V_{ICR}		(0 V to V_{ref})		V
Open Loop Voltage Gain (V_O = 3.0 V, R_L = 15 k)	A_{VOL}	70	80	–	dB
Input Common Mode Rejection Ratio	CMRR	55	86	–	dB
Power Supply Rejection Ratio (V_{CC} = V_C = 10 to 30 V)	PSRR	65	105	–	dB

NOTES: 1. The input common mode voltage or input signal voltage should not be allowed to go negative by more than 0.3 V.
2. The compliance voltage must not exceed the range of –0.3 to V_{ref}.
3. Maximum package power dissipation limits must be observed.

ELECTRICAL CHARACTERISTICS (continued) (V_{CC} = V_C = 20 V, R_T = 4.7 k, C_T = 10 nF, T_A = 25°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
ERROR AMPLIFIER					
Output Voltage Swing High State (R_L = 15 k to Gnd) Low State (R_L = 15 k to V_{ref})	 V_{OH} V_{OL}	 4.6 –	 5.3 0.5	 – 1.0	V
OSCILLATOR SECTION					
Oscillator Frequency	f_{OSC}	22	25	28	kHz
Frequency Change with Voltage (V_{CC} = 10 to 30 V)	$\Delta f_{OSC}/\Delta V$	–	0.01	5.0	%
Sawtooth Peak Voltage	$V_{OSC(P)}$	–	4.1	4.5	V
Sawtooth Valley Voltage	$V_{OSC(V)}$	1.2	1.5	–	V
LOGIC INPUTS					
Input Threshold Voltage (Pins 3, 4, 5, 6, 7, 22, 23) High State Low State	 V_{IH} V_{IL}	 3.0 –	 2.2 1.7	 – 0.8	V
Sensor Inputs (Pins 4, 5, 6) High State Input Current (V_{IH} = 5.0 V) Low State Input Current (V_{IL} = 0 V)	 I_{IH} I_{IL}	 –150 –600	 –70 –337	 –20 –150	µA
Forward/Reverse, 60°/$\overline{120°}$ Select (Pins 3, 22, 23) High State Input Current (V_{IH} = 5.0 V) Low State Input Current (V_{IL} = 0 V)	 I_{IH} I_{IL}	 –75 –300	 –36 –175	 –10 –75	µA
Output Enable High State Input Current (V_{IH} = 5.0 V) Low State Input Current (V_{IL} = 0 V)	 I_{IH} I_{IL}	 –60 –60	 –29 –29	 –10 –10	µA
CURRENT–LIMIT COMPARATOR					
Threshold Voltage	V_{th}	85	101	115	mV
Input Common Mode Voltage Range	V_{ICR}	–	3.0	–	V
Input Bias Current	I_{IB}	–	–0.9	–5.0	µA
OUTPUTS AND POWER SECTIONS					
Top Drive Output Sink Saturation (I_{sink} = 25 mA)	$V_{CE(sat)}$	–	0.5	1.5	V
Top Drive Output Off–State Leakage (V_{CE} = 30 V)	$I_{DRV(leak)}$	–	0.06	100	µA
Top Drive Output Switching Time (C_L = 47 pF, R_L = 1.0 k) Rise Time Fall Time	 t_r t_f	 – –	 107 26	 300 300	ns
Bottom Drive Output Voltage High State (V_{CC} = 20 V, V_C = 30 V, I_{source} = 50 mA) Low State (V_{CC} = 20 V, V_C = 30 V, I_{sink} = 50 mA)	 V_{OH} V_{OL}	 (V_{CC} –2.0) –	 (V_{CC} –1.1) 1.5	 – 2.0	V
Bottom Drive Output Switching Time (C_L = 1000 pF) Rise Time Fall Time	 t_r t_f	 – –	 38 30	 200 200	ns
$\overline{\text{Fault}}$ Output Sink Saturation (I_{sink} = 16 mA)	$V_{CE(sat)}$	–	225	500	mV
$\overline{\text{Fault}}$ Output Off–State Leakage (V_{CE} = 20 V)	$I_{FLT(leak)}$	–	1.0	100	µA
Under Voltage Lockout Drive Output Enabled (V_{CC} or V_C Increasing) Hysteresis	 $V_{th(on)}$ V_H	 8.2 0.1	 8.9 0.2	 10 0.3	V
Power Supply Current Pin 17 (V_{CC} = V_C = 20 V) Pin 17 (V_{CC} = 20 V, V_C = 30 V) Pin 18 (V_{CC} = V_C = 20 V) Pin 18 (V_{CC} = 20 V, V_C = 30 V)	 I_{CC} I_C 	 – – – –	 12 14 3.5 5.0	 16 20 6.0 10	mA

Figure 1. Oscillator Frequency versus Timing Resistor

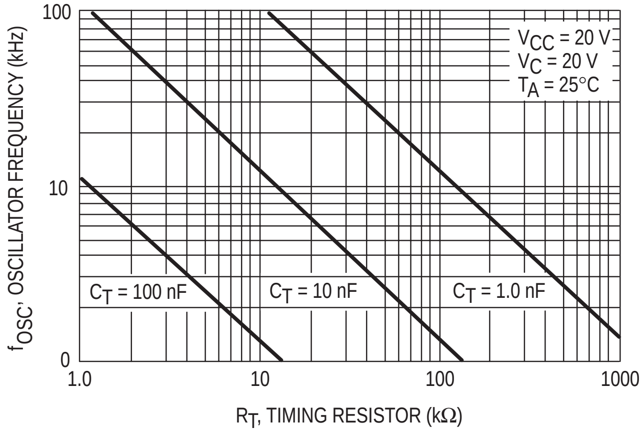


Figure 2. Oscillator Frequency Change versus Temperature

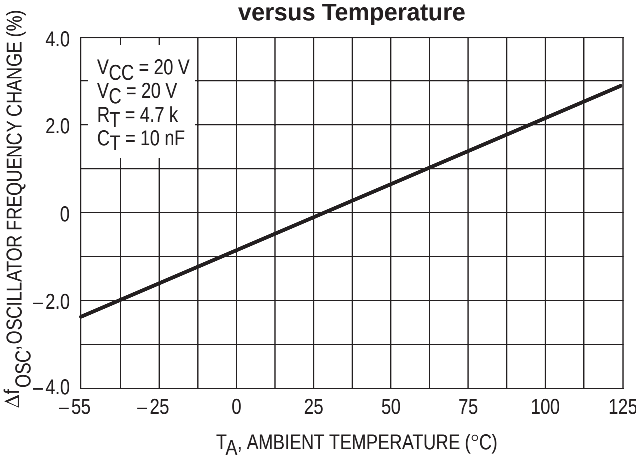


Figure 3. Error Amp Open Loop Gain and Phase versus Frequency

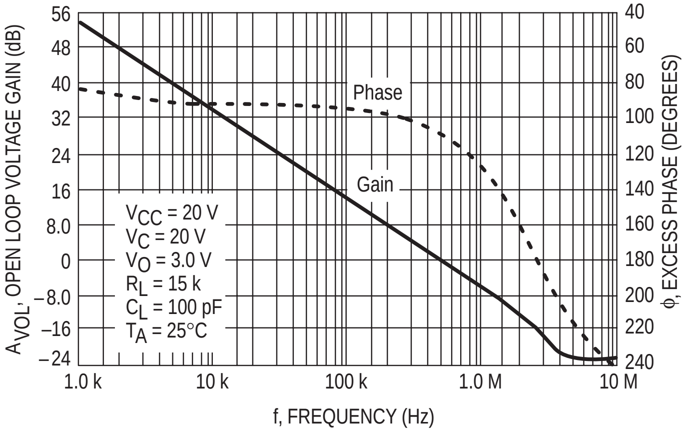


Figure 4. Error Amp Output Saturation Voltage versus Load Current

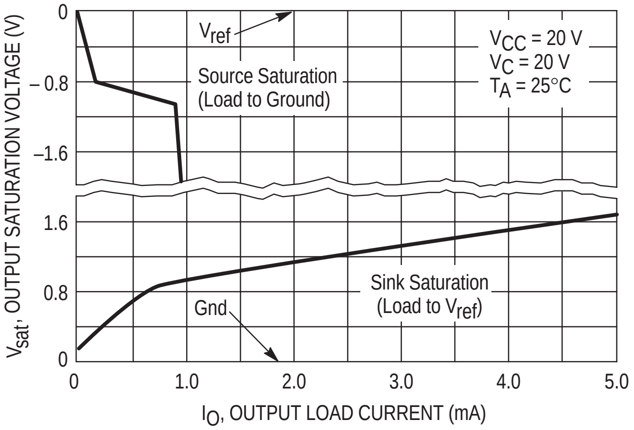


Figure 5. Error Amp Small–Signal Transient Response

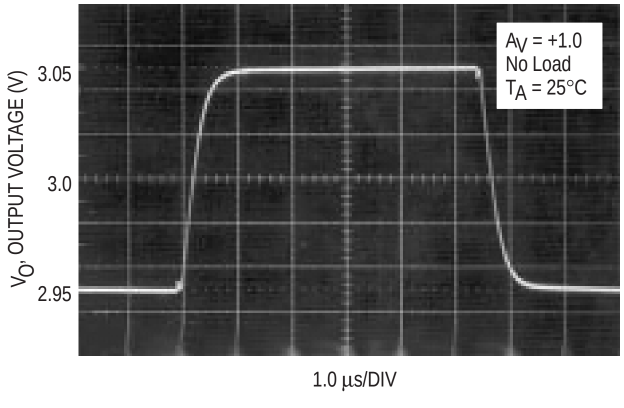


Figure 6. Error Amp Large–Signal Transient Response

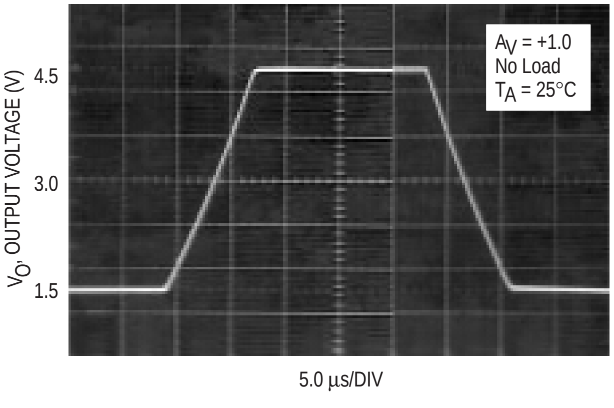


Figure 7. Reference Output Voltage Change versus Output Source Current

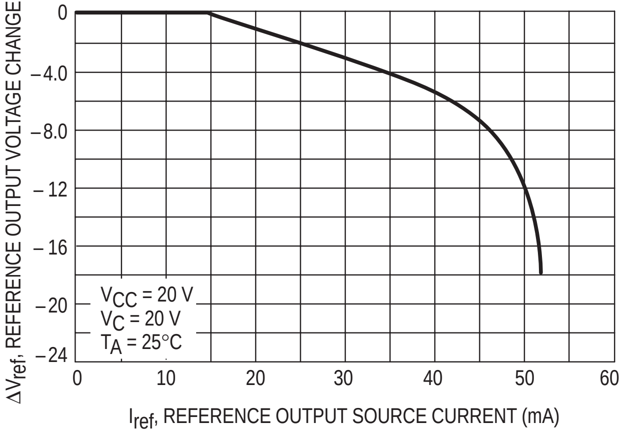


Figure 8. Reference Output Voltage versus Supply Voltage

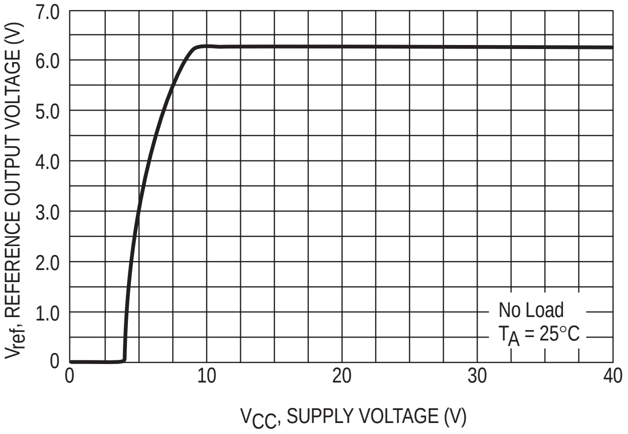


Figure 9. Reference Output Voltage versus Temperature

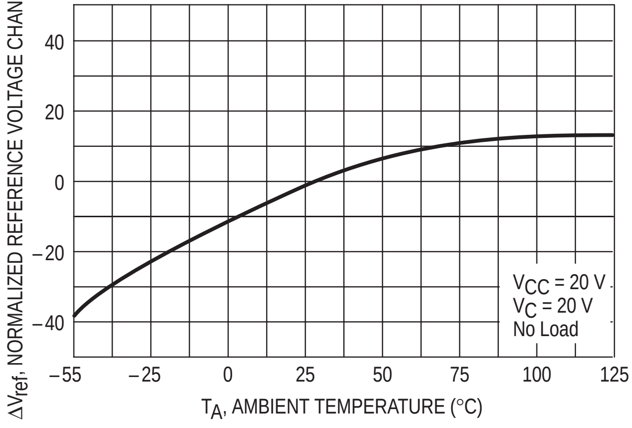


Figure 10. Output Duty Cycle versus PWM Input Voltage

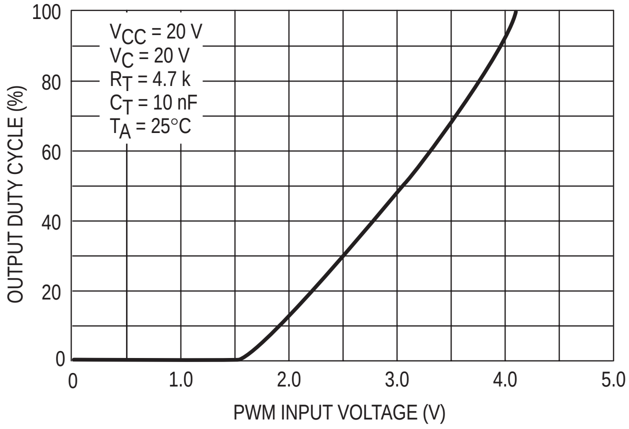


Figure 11. Bottom Drive Response Time versus Current Sense Input Voltage

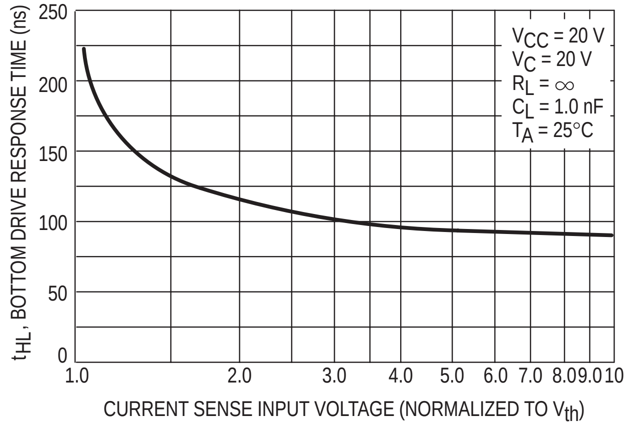


Figure 12. $\overline{\text{Fault}}$ Output Saturation versus Sink Current

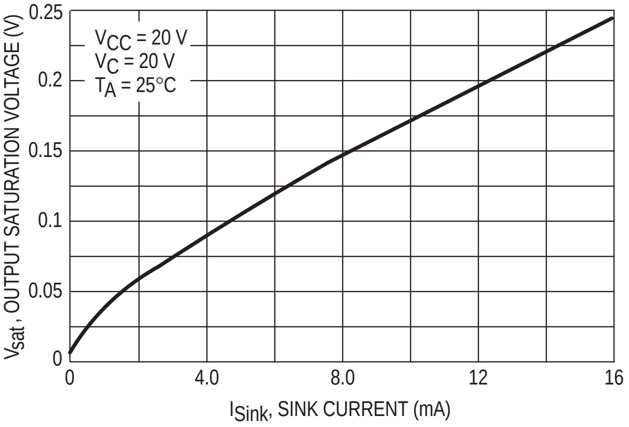


Figure 13. Top Drive Output Saturation Voltage versus Sink Current

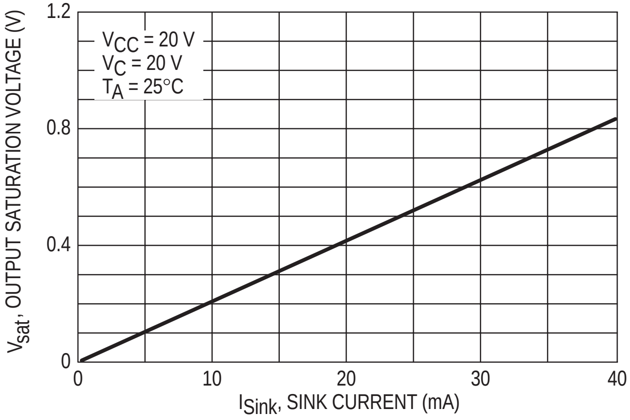


Figure 14. Top Drive Output Waveform

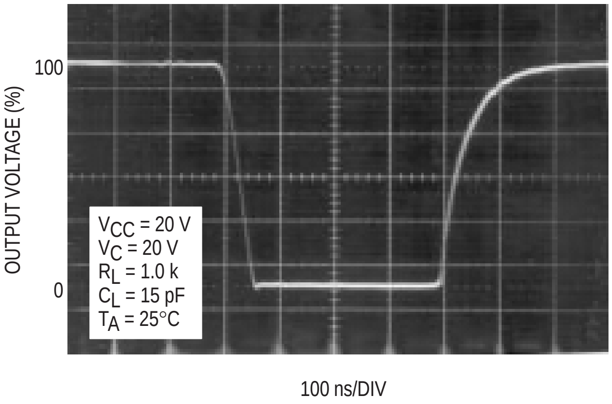


Figure 15. Bottom Drive Output Waveform

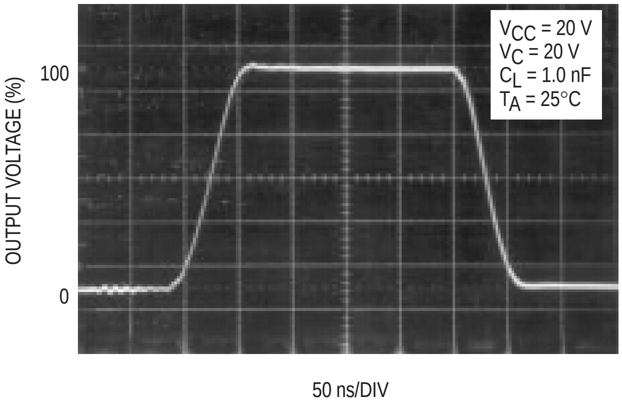


Figure 16. Bottom Drive Output Waveform

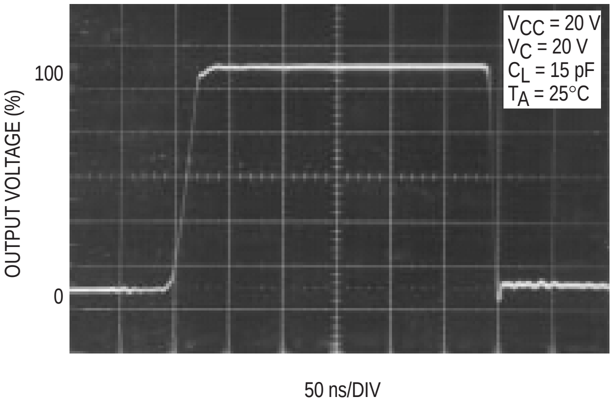


Figure 17. Bottom Drive Output Saturation Voltage versus Load Current

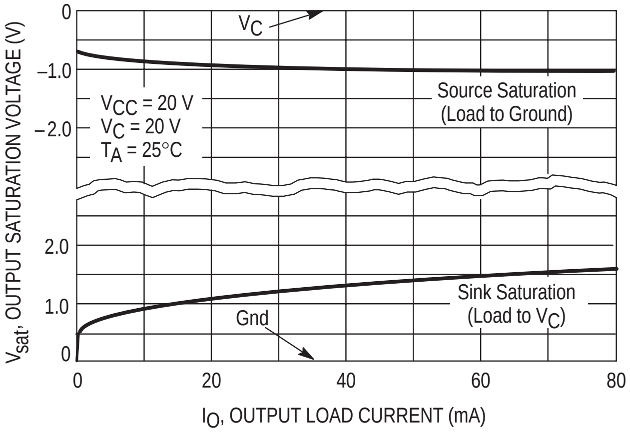
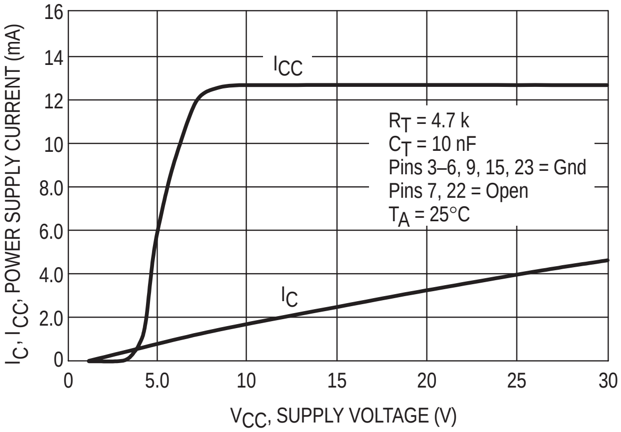


Figure 18. Power and Bottom Drive Supply Current versus Supply Voltage



PIN FUNCTION DESCRIPTION

Pin	Symbol	Description
1, 2, 24	B_T, A_T, C_T	These three open collector Top Drive outputs are designed to drive the external upper power switch transistors.
3	Fwd/Rev	The Forward/Reverse Input is used to change the direction of motor rotation.
4, 5, 6	S_A, S_B, S_C	These three Sensor Inputs control the commutation sequence.
7	Output Enable	A logic high at this input causes the motor to run, while a low causes it to coast.
8	Reference Output	This output provides charging current for the oscillator timing capacitor C_T and a reference for the error amplifier. It may also serve to furnish sensor power.
9	Current Sense Noninverting Input	A 100 mV signal, with respect to Pin 15, at this input terminates output switch conduction during a given oscillator cycle. This pin normally connects to the top side of the current sense resistor.
10	Oscillator	The Oscillator frequency is programmed by the values selected for the timing components, R_T and C_T.
11	Error Amp Noninverting Input	This input is normally connected to the speed set potentiometer.
12	Error Amp Inverting Input	This input is normally connected to the Error Amp Output in open loop applications.
13	Error Amp Out/PWM Input	This pin is available for compensation in closed loop applications.
14	Fault Output	This open collector output is active low during one or more of the following conditions: Invalid Sensor Input code, Enable Input at logic 0, Current Sense Input greater than 100 mV (Pin 9 with respect to Pin 15), Undervoltage Lockout activation, and Thermal Shutdown.
15	Current Sense Inverting Input	Reference pin for internal 100 mV threshold. This pin is normally connected to the bottom side of the current sense resistor.
16	Gnd	This pin supplies a ground for the control circuit and should be referenced back to the power source ground.
17	V_{CC}	This pin is the positive supply of the control IC. The controller is functional over a minimum V_{CC} range of 10 to 30 V.
18	V_C	The high state (V_{OH}) of the Bottom Drive Outputs is set by the voltage applied to this pin. The controller is operational over a minimum V_C range of 10 to 30 V.
19, 20, 21	C_B, B_B, A_B	These three totem pole Bottom Drive Outputs are designed for direct drive of the external bottom power switch transistors.
22	60°/120° Select	The electrical state of this pin configures the control circuit operation for either 60° (high state) or 120° (low state) sensor electrical phasing inputs.
23	Brake	A logic low state at this input allows the motor to run, while a high state does not allow motor operation and if operating causes rapid deceleration.

INTRODUCTION

The MC33035 is one of a series of high performance monolithic DC brushless motor controllers produced by Motorola. It contains all of the functions required to implement a full–featured, open loop, three or four phase motor control system. In addition, the controller can be made to operate DC brush motors. Constructed with Bipolar Analog technology, it offers a high degree of performance and ruggedness in hostile industrial environments. The MC33035 contains a rotor position decoder for proper commutation sequencing, a temperature compensated reference capable of supplying a sensor power, a frequency programmable sawtooth oscillator, a fully accessible error amplifier, a pulse width modulator comparator, three open collector top drive outputs, and three high current totem pole bottom driver outputs ideally suited for driving power MOSFETs.

Included in the MC33035 are protective features consisting of undervoltage lockout, cycle–by–cycle current limiting with a selectable time delayed latched shutdown mode, internal thermal shutdown, and a unique fault output that can easily be interfaced to a microprocessor controller.

Typical motor control functions include open loop speed control, forward or reverse rotation, run enable, and dynamic braking. In addition, the MC33035 has a 60°/120° select pin which configures the rotor position decoder for either 60° or 120° sensor electrical phasing inputs.

FUNCTIONAL DESCRIPTION

A representative internal block diagram is shown in Figure 19 with various applications shown in Figures 36, 38, 39, 43, 45, and 46. A discussion of the features and function of each of the internal blocks given below is referenced to Figures 19 and 36.

Rotor Position Decoder

An internal rotor position decoder monitors the three sensor inputs (Pins 4, 5, 6) to provide the proper sequencing of the top and bottom drive outputs. The sensor inputs are designed to interface directly with open collector type Hall Effect switches or opto slotted couplers. Internal pull–up resistors are included to minimize the required number of external components. The inputs are TTL compatible, with their thresholds typically at 2.2 V. The MC33035 series is designed to control three phase motors and operate with four of the most common conventions of sensor phasing. A 60°/120° Select (Pin 22) is conveniently provided and affords the MC33035 to configure itself to control motors having either 60°, 120°, 240° or 300° electrical sensor phasing. With three sensor inputs there are eight possible input code combinations, six of which are valid rotor positions. The remaining two codes are invalid and are usually caused by an open or shorted sensor line. With six valid input codes, the decoder can resolve the motor rotor position to within a window of 60 electrical degrees.

The Forward/Reverse input (Pin 3) is used to change the direction of motor rotation by reversing the voltage across the stator winding. When the input changes state, from high to low with a given sensor input code (for example 100), the enabled top and bottom drive outputs with the same alpha designation are exchanged (A_T to A_B, B_T to B_B, C_T to C_B). In effect, the commutation sequence is reversed and the motor changes directional rotation.

Motor on/off control is accomplished by the Output Enable (Pin 7). When left disconnected, an internal 25 µA current source enables sequencing of the top and bottom drive outputs. When grounded, the top drive outputs turn off and the bottom drives are forced low, causing the motor to coast and the Fault output to activate.

Dynamic motor braking allows an additional margin of safety to be designed into the final product. Braking is accomplished by placing the Brake Input (Pin 23) in a high state. This causes the top drive outputs to turn off and the bottom drives to turn on, shorting the motor–generated back EMF. The brake input has unconditional priority over all other inputs. The internal 40 kΩ pull–up resistor simplifies interfacing with the system safety–switch by insuring brake activation if opened or disconnected. The commutation logic truth table is shown in Figure 20. A four input NOR gate is used to monitor the brake input and the inputs to the three top drive output transistors. Its purpose is to disable braking until the top drive outputs attain a high state. This helps to prevent simultaneous conduction of the the top and bottom power switches. In half wave motor drive applications, the top drive outputs are not required and are normally left disconnected. Under these conditions braking will still be accomplished since the NOR gate senses the base voltage to the top drive output transistors.

Error Amplifier

A high performance, fully compensated error amplifier with access to both inputs and output (Pins 11, 12, 13) is provided to facilitate the implementation of closed loop motor speed control. The amplifier features a typical DC voltage gain of 80 dB, 0.6 MHz gain bandwidth, and a wide input common mode voltage range that extends from ground to V_{ref}. In most open loop speed control applications, the amplifier is configured as a unity gain voltage follower with the noninverting input connected to the speed set voltage source. Additional configurations are shown in Figures 31 through 35.

Oscillator

The frequency of the internal ramp oscillator is programmed by the values selected for timing components R_T and C_T. Capacitor C_T is charged from the Reference Output (Pin 8) through resistor R_T and discharged by an internal discharge transistor. The ramp peak and valley voltages are typically 4.1 V and 1.5 V respectively. To provide a good compromise between audible noise and output switching efficiency, an oscillator frequency in the range of 20 to 30 kHz is recommended. Refer to Figure 1 for component selection.

Figure 19. Representative Block Diagram

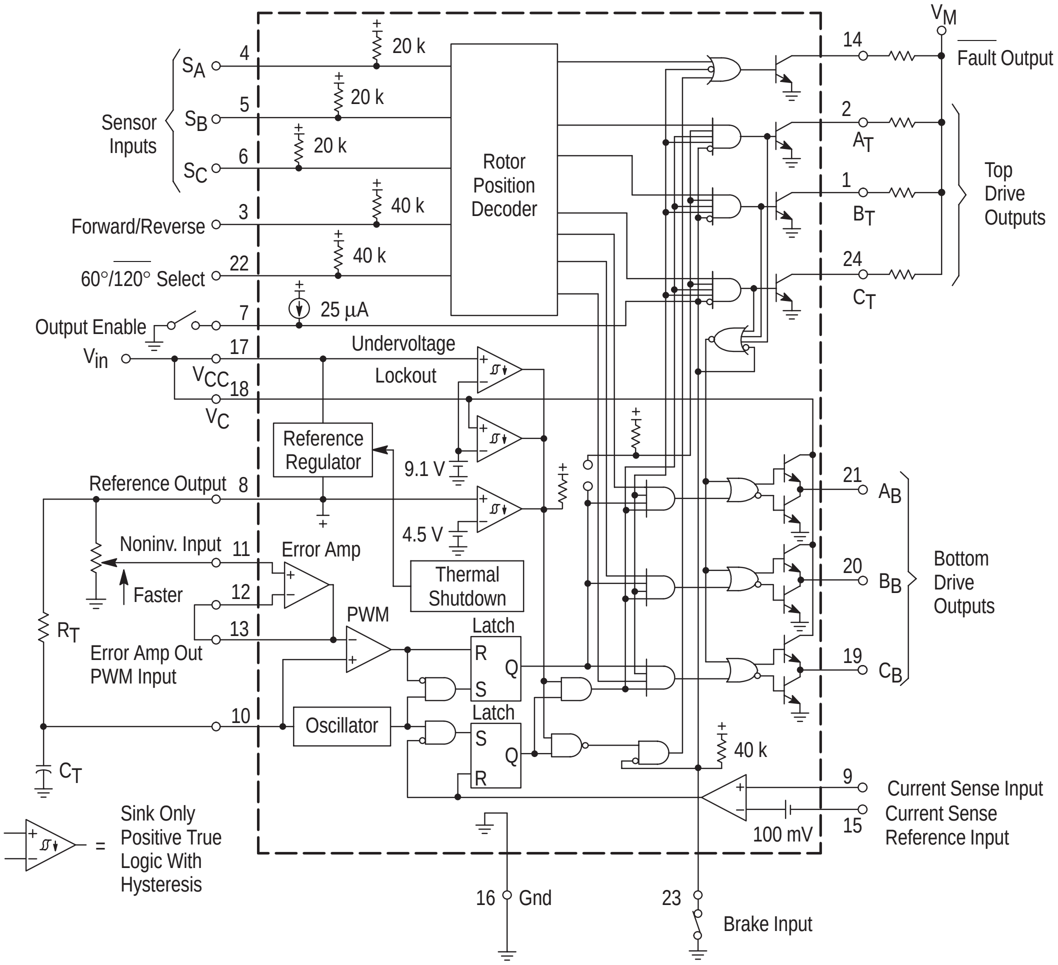


Figure 20. Three Phase, Six Step Commutation Truth Table (Note 1)

Inputs (Note 2)										Outputs (Note 3)							
Sensor Electrical Phasing (Note 4)										Top Drives			Bottom Drives				
60°			120°														
S_A	S_B	S_C	S_A	S_B	S_C	F/R	Enable	Brake	Current Sense	A_T	B_T	C_T	A_B	B_B	C_B	$\overline{\text{Fault}}$	
1	0	0	1	0	0	1	1	0	0	0	1	1	0	0	1	1	**(Note 5)** F/R = 1
1	1	0	1	1	0	1	1	0	0	1	0	1	0	0	1	1	
1	1	1	0	1	0	1	1	0	0	1	0	1	1	0	0	1	
0	1	1	0	1	1	1	1	0	0	1	1	0	1	0	0	1	
0	0	1	0	0	1	1	1	0	0	1	1	0	0	1	0	1	
0	0	0	1	0	1	1	1	0	0	0	1	1	0	1	0	1	
1	0	0	1	0	0	0	1	0	0	1	1	0	1	0	0	1	**(Note 5)** F/R = 0
1	1	0	1	1	0	0	1	0	0	1	1	0	0	1	0	1	
1	1	1	0	1	0	0	1	0	0	0	1	1	0	1	0	1	
0	1	1	0	1	1	0	1	0	0	0	1	1	0	0	1	1	
0	0	1	0	0	1	0	1	0	0	1	0	1	0	0	1	1	
0	0	0	1	0	1	0	1	0	0	1	0	1	1	0	0	1	
1	0	1	1	1	1	X	X	0	X	1	1	1	0	0	0	0	**(Note 6)** Brake = 0
0	1	0	0	0	0	X	X	0	X	1	1	1	0	0	0	0	
1	0	1	1	1	1	X	X	1	X	1	1	1	1	1	1	0	**(Note 7)** Brake = 1
0	1	0	0	0	0	X	X	1	X	1	1	1	1	1	1	0	
V	V	V	V	V	V	X	1	1	X	1	1	1	1	1	1	1	**(Note 8)**
V	V	V	V	V	V	X	0	1	X	1	1	1	1	1	1	0	**(Note 9)**
V	V	V	V	V	V	X	0	0	X	1	1	1	0	0	0	0	**(Note 10)**
V	V	V	V	V	V	X	1	0	1	1	1	1	0	0	0	0	**(Note 11)**

NOTES:
1. V = Any one of six valid sensor or drive combinations X = Don’t care.
2. The digital inputs (Pins 3, 4, 5, 6, 7, 22, 23) are all TTL compatible. The current sense input (Pin 9) has a 100 mV threshold with respect to Pin 15. A logic 0 for this input is defined as < 85 mV, and a logic 1 is > 115 mV.
3. The fault and top drive outputs are open collector design and active in the low (0) state.
4. With 60°/120° select (Pin 22) in the high (1) state, configuration is for 60° sensor electrical phasing inputs. With Pin 22 in low (0) state, configuration is for 120° sensor electrical phasing inputs.
5. Valid 60° or 120° sensor combinations for corresponding valid top and bottom drive outputs.
6. Invalid sensor inputs with brake = 0; All top and bottom drives off, Fault low.
7. Invalid sensor inputs with brake = 1; All top drives off, all bottom drives on, Fault low.
8. Valid 60° or 120° sensor inputs with brake = 1; All top drives off, all bottom drives on, Fault high.
9. Valid sensor inputs with brake = 1 and enable = 0; All top drives off, all bottom drives on, Fault low.
10. Valid sensor inputs with brake = 0 and enable = 0; All top and bottom drives off, Fault low.
11. All bottom drives off, Fault low.

Pulse Width Modulator

The use of pulse width modulation provides an energy efficient method of controlling the motor speed by varying the average voltage applied to each stator winding during the commutation sequence. As C_T discharges, the oscillator sets both latches, allowing conduction of the top and bottom drive outputs. The PWM comparator resets the upper latch, terminating the bottom drive output conduction when the positive–going ramp of C_T becomes greater than the error amplifier output. The pulse width modulator timing diagram is shown in Figure 21. Pulse width modulation for speed control appears only at the bottom drive outputs.

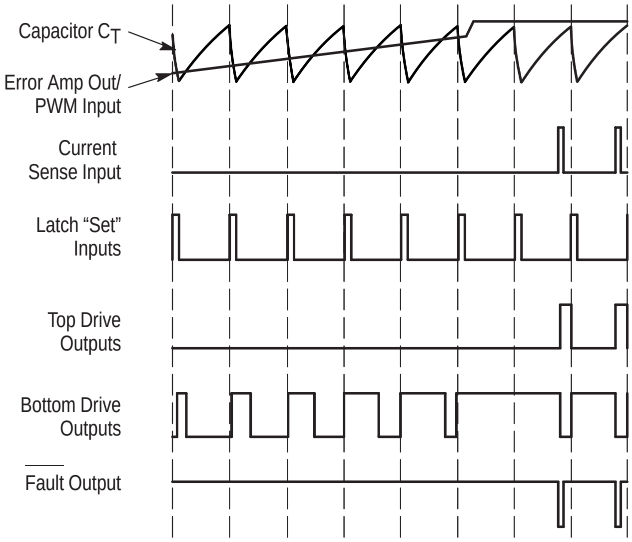
Current Limit

Continuous operation of a motor that is severely over–loaded results in overheating and eventual failure. This destructive condition can best be prevented with the use of cycle–by–cycle current limiting. That is, each on–cycle is treated as a separate event. Cycle–by–cycle current limiting is accomplished by monitoring the stator current build–up each time an output switch conducts, and upon sensing an over current condition, immediately turning off the switch and holding it off for the remaining duration of oscillator ramp–up period. The stator current is converted to a voltage by inserting a ground–referenced sense resistor R_S (Figure 36) in series with the three bottom switch transistors (Q_4, Q_5, Q_6). The voltage developed across the sense resistor is monitored by the Current Sense Input (Pins 9 and 15), and compared to the internal 100 mV reference. The current sense comparator inputs have an input common mode range of approximately 3.0 V. If the 100 mV current sense threshold is exceeded, the comparator resets the lower sense latch and terminates output switch conduction. The value for the current sense resistor is:

$$R_S = \frac{0.1}{I_{stator(max)}}$$

The $\overline{\text{Fault}}$ output activates during an over current condition. The dual–latch PWM configuration ensures that only one single output conduction pulse occurs during any given oscillator cycle, whether terminated by the output of the error amp or the current limit comparator.

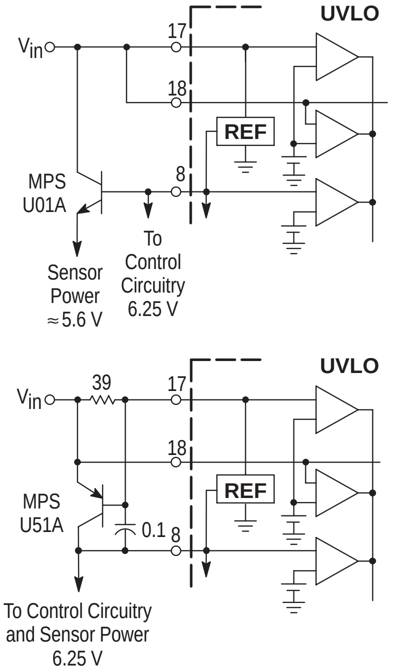
Figure 21. Pulse Width Modulator Timing Diagram



Reference

The on–chip 6.25 V regulator (Pin 8) provides charging current for the oscillator timing capacitor, a reference for the error amplifier, and can supply 20 mA of current suitable for directly powering sensors in low voltage applications. In higher voltage applications, it may become necessary to transfer the power dissipated by the regulator off the IC. This is easily accomplished with the addition of an external pass transistor as shown in Figure 22. A 6.25 V reference level was chosen to allow implementation of the simpler NPN circuit, where $V_{ref} – V_{BE}$ exceeds the minimum voltage required by Hall Effect sensors over temperature. With proper transistor selection and adequate heatsinking, up to one amp of load current can be obtained.

Figure 22. Reference Output Buffers



The NPN circuit is recommended for powering Hall or opto sensors, where the output voltage temperature coefficient is not critical. The PNP circuit is slightly more complex, but is also more accurate over temperature. Neither circuit has current limiting.

Undervoltage Lockout

A triple Undervoltage Lockout has been incorporated to prevent damage to the IC and the external power switch transistors. Under low power supply conditions, it guarantees that the IC and sensors are fully functional, and that there is sufficient bottom drive output voltage. The positive power supplies to the IC (V_{CC}) and the bottom drives (V_C) are each monitored by separate comparators that have their thresholds at 9.1 V. This level ensures sufficient gate drive necessary to attain low $R_{DS(on)}$ when driving standard power MOSFET devices. When directly powering the Hall sensors from the reference, improper sensor operation can result if the reference output voltage falls below 4.5 V. A third comparator is used to detect this condition. If one or more of the comparators detects an undervoltage condition, the Fault Output is activated, the top drives are turned off and the bottom drive outputs are held in a low state. Each of the comparators contain hysteresis to prevent oscillations when crossing their respective thresholds.

Fault Output

The open collector Fault Output (Pin 14) was designed to provide diagnostic information in the event of a system malfunction. It has a sink current capability of 16 mA and can directly drive a light emitting diode for visual indication. Additionally, it is easily interfaced with TTL/CMOS logic for use in a microprocessor controlled system. The Fault Output is active low when one or more of the following conditions occur:

1) Invalid Sensor Input code
2) Output Enable at logic [0]
3) Current Sense Input greater than 100 mV
4) Undervoltage Lockout, activation of one or more of the comparators
5) Thermal Shutdown, maximum junction temperature being exceeded

This unique output can also be used to distinguish between motor start–up or sustained operation in an overloaded condition. With the addition of an RC network between the Fault Output and the enable input, it is possible to create a time–delayed latched shutdown for overcurrent. The added circuitry shown in Figure 23 makes easy starting of motor systems which have high inertial loads by providing additional starting torque, while still preserving overcurrent protection. This task is accomplished by setting the current limit to a higher than nominal value for a predetermined time. During an excessively long overcurrent condition, capacitor C_{DLY} will charge, causing the enable input to cross its threshold to a low state. A latch is then formed by the positive feedback loop from the Fault Output to the Output Enable. Once set, by the Current Sense Input, it can only be reset by shorting C_{DLY} or cycling the power supplies.

Drive Outputs

The three top drive outputs (Pins 1, 2, 24) are open collector NPN transistors capable of sinking 50 mA with a minimum breakdown of 30 V. Interfacing into higher voltage applications is easily accomplished with the circuits shown in Figures 24 and 25.

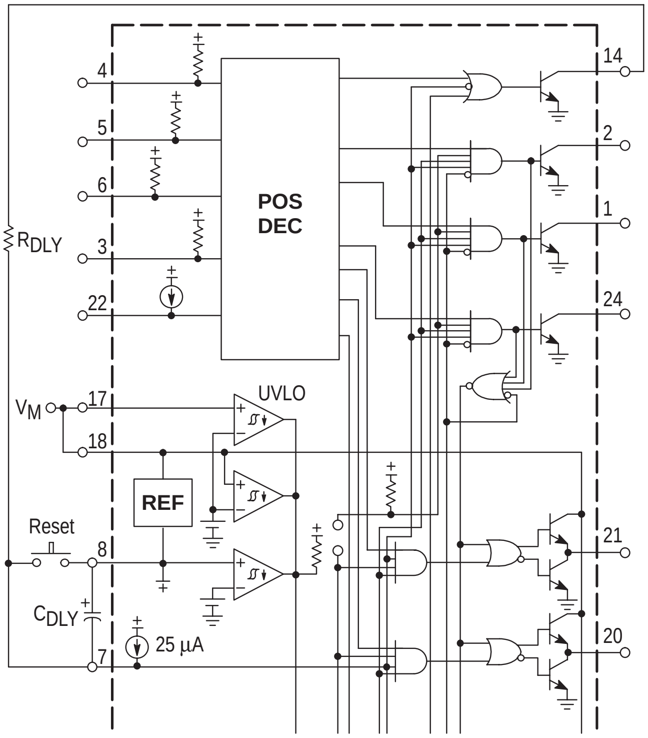
The three totem pole bottom drive outputs (Pins 19, 20, 21) are particularly suited for direct drive of N–Channel MOSFETs or NPN bipolar transistors (Figures 26, 27, 28 and 29). Each output is capable of sourcing and sinking up to 100 mA. Power for the bottom drives is supplied from V_C (Pin 18). This separate supply input allows the designer added flexibility in tailoring the drive voltage, independent of V_{CC}. A zener clamp should be connected to this input when driving power MOSFETs in systems where V_{CC} is greater than 20 V so as to prevent rupture of the MOSFET gates.

The control circuitry ground (Pin 16) and current sense inverting input (Pin 15) must return on separate paths to the central input source ground.

Thermal Shutdown

Internal thermal shutdown circuitry is provided to protect the IC in the event the maximum junction temperature is exceeded. When activated, typically at 170°C, the IC acts as though the Output Enable was grounded.

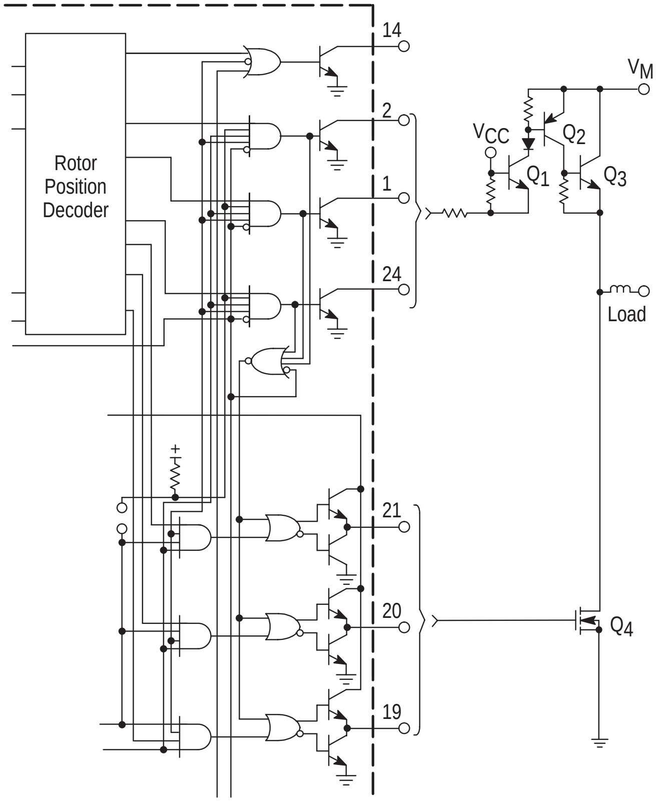
Figure 23. Timed Delayed Latched Over Current Shutdown



$$t_{DLY} \approx R_{DLY}\ C_{DLY}\ \ln\left(\frac{V_{ref} - (I_{IL}\ \text{enable}\ R_{DLY})}{V_{th}\ \text{enable} - (I_{IL}\ \text{enable}\ R_{DLY})}\right)$$

$$\approx R_{DLY}\ C_{DLY}\ \ln\left(\frac{6.25 - (20 \times 10^{-6}\ R_{DLY})}{1.4 - (20 \times 10^{-6}\ R_{DLY})}\right)$$

Figure 24. High Voltage Interface with NPN Power Transistors



Transistor Q_1 is a common base stage used to level shift from V_{CC} to the high motor voltage, V_M. The collector diode is required if V_{CC} is present while V_M is low.

Figure 25. High Voltage Interface with N–Channel Power MOSFETs

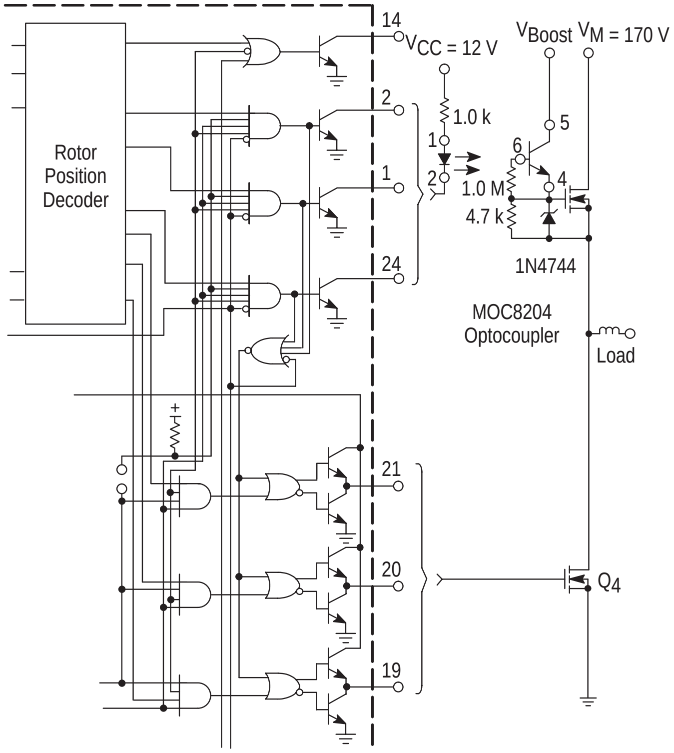
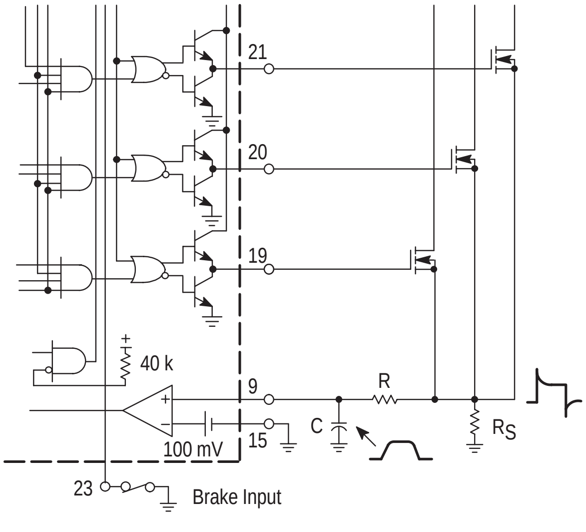
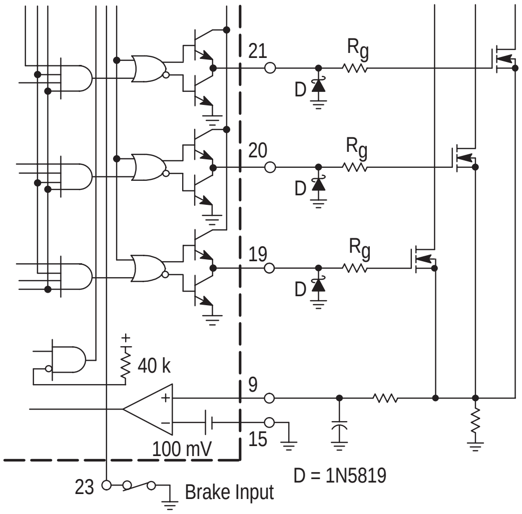


Figure 26. Current Waveform Spike Suppression



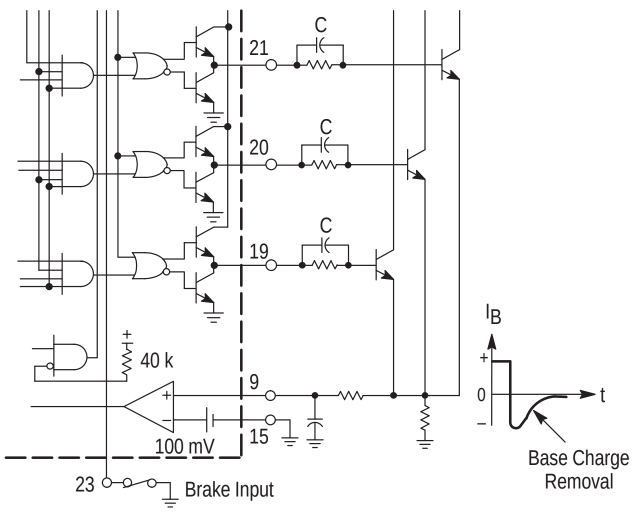
The addition of the RC filter will eliminate current–limit instability caused by the leading edge spike on the current waveform. Resistor R_S should be a low inductance type.

Figure 27. MOSFET Drive Precautions



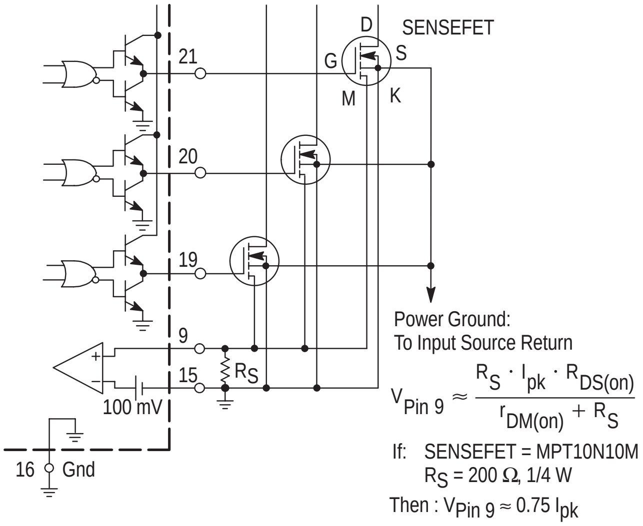
Series gate resistor R_g will dampen any high frequency oscillations caused by the MOSFET input capacitance and any series wiring induction in the gate–source circuit. Diode D is required if the negative current into the Bottom Drive Outputs exceeds 50 mA.

Figure 28. Bipolar Transistor Drive



The totem–pole output can furnish negative base current for enhanced transistor turn–off, with the addition of capacitor C.

Figure 29. Current Sensing Power MOSFETs



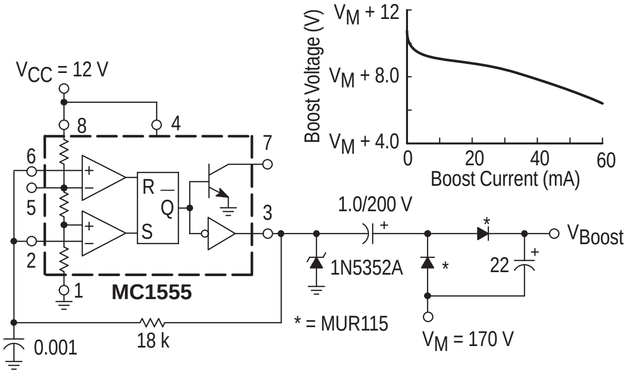
$$V_{Pin\ 9} \approx \frac{R_S \cdot I_{pk} \cdot R_{DS(on)}}{r_{DM(on)} + R_S}$$

If: SENSEFET = MPT10N10M
R_S = 200 Ω, 1/4 W
Then : $V_{Pin\ 9} \approx 0.75\ I_{pk}$

Control Circuitry Ground (Pin 16) and Current Sense Inverting Input (Pin 15) must return on separate paths to the Central Input Source Ground.

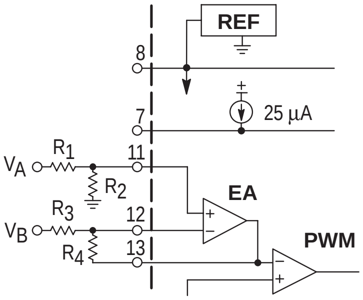
Virtually lossless current sensing can be achieved with the implementation of SENSEFET power switches.

Figure 30. High Voltage Boost Supply



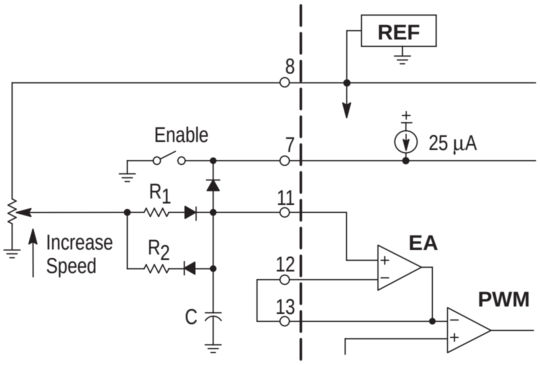
This circuit generates V_{Boost} for Figure 25.

Figure 31. Differential Input Speed Controller



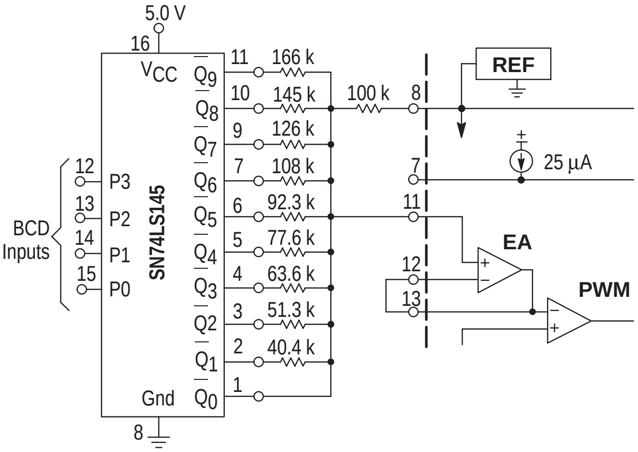
$$V_{Pin\ 13} = V_A \left(\frac{R_3 + R_4}{R_1 + R_2}\right) \frac{R_2}{R_3} - \left(\frac{R_4}{R_3} V_B\right)$$

Figure 32. Controlled Acceleration/Deceleration



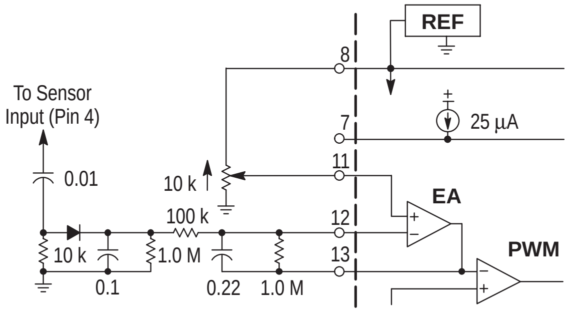
Resistor R_1 with capacitor C sets the acceleration time constant while R_2 controls the deceleration. The values of R_1 and R_2 should be at least ten times greater than the speed set potentiometer to minimize time constant variations with different speed settings.

Figure 33. Digital Speed Controller



The SN74LS145 is an open collector BCD to One of Ten decoder. When connected as shown, input codes 0000 through 1001 steps the PWM in increments of approximately 10% from 0 to 90% on–time. Input codes 1010 through 1111 will produce 100% on–time or full motor speed.

Figure 34. Closed Loop Speed Control



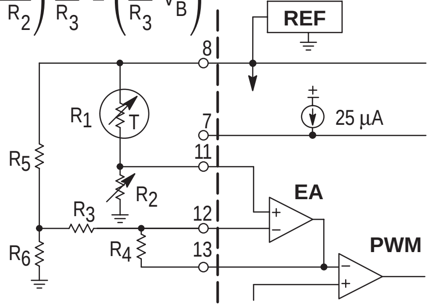
The rotor position sensors can be used as a tachometer. By differentiating the positive–going edges and then integrating them over time, a voltage proportional to speed can be generated. The error amp compares this voltage to that of the speed set to control the PWM.

Figure 35. Closed Loop Temperature Control

$$V_{Pin\ 3} = V_{ref} \left(\frac{R_3 + R_4}{R_1 + R_2}\right) \frac{R_2}{R_3} - \left(\frac{R_4}{R_3} V_B\right)$$

$$V_B = \frac{V_{ref}}{\left(\frac{R_5}{R_6} + 1\right)}$$

$$R_3 >> R_5 \parallel R_6$$



This circuit can control the speed of a cooling fan proportional to the difference between the sensor and set temperatures. The control loop is closed as the forced air cools the NTC thermistor. For controlled heating applications, exchange the positions of R_1 and R_2.

SYSTEM APPLICATIONS

Three Phase Motor Commutation

The three phase application shown in Figure 36 is a full–featured open loop motor controller with full wave, six step drive. The upper power switch transistors are Darlingtons while the lower devices are power MOSFETs. Each of these devices contains an internal parasitic catch diode that is used to return the stator inductive energy back to the power supply. The outputs are capable of driving a delta or wye connected stator, and a grounded neutral wye if split supplies are used. At any given rotor position, only one top and one bottom power switch (of different totem poles) is enabled. This configuration switches both ends of the stator winding from supply to ground which causes the current flow to be bidirectional or full wave. A leading edge spike is usually present on the current waveform and can cause a current–limit instability. The spike can be eliminated by adding an RC filter in series with the Current Sense Input. Using a low inductance type resistor for R_S will also aid in spike reduction. Care must be taken in the selection of the bottom power switch transistors so that the current during braking does not exceed the device rating. During braking, the peak current generated is limited only by the series resistance of the conducting bottom switch and winding.

$$I_{peak} = \frac{V_M + EMF}{R_{switch} + R_{winding}}$$

If the motor is running at maximum speed with no load, the generated back EMF can be as high as the supply voltage, and at the onset of braking, the peak current may approach twice the motor stall current. Figure 37 shows the commutation waveforms over two electrical cycles. The first cycle (0° to 360°) depicts motor operation at full speed while the second cycle (360° to 720°) shows a reduced speed with about 50% pulse width modulation. The current waveforms reflect a constant torque load and are shown synchronous to the commutation frequency for clarity.

Figure 36. Three Phase, Six Step, Full Wave Motor Controller

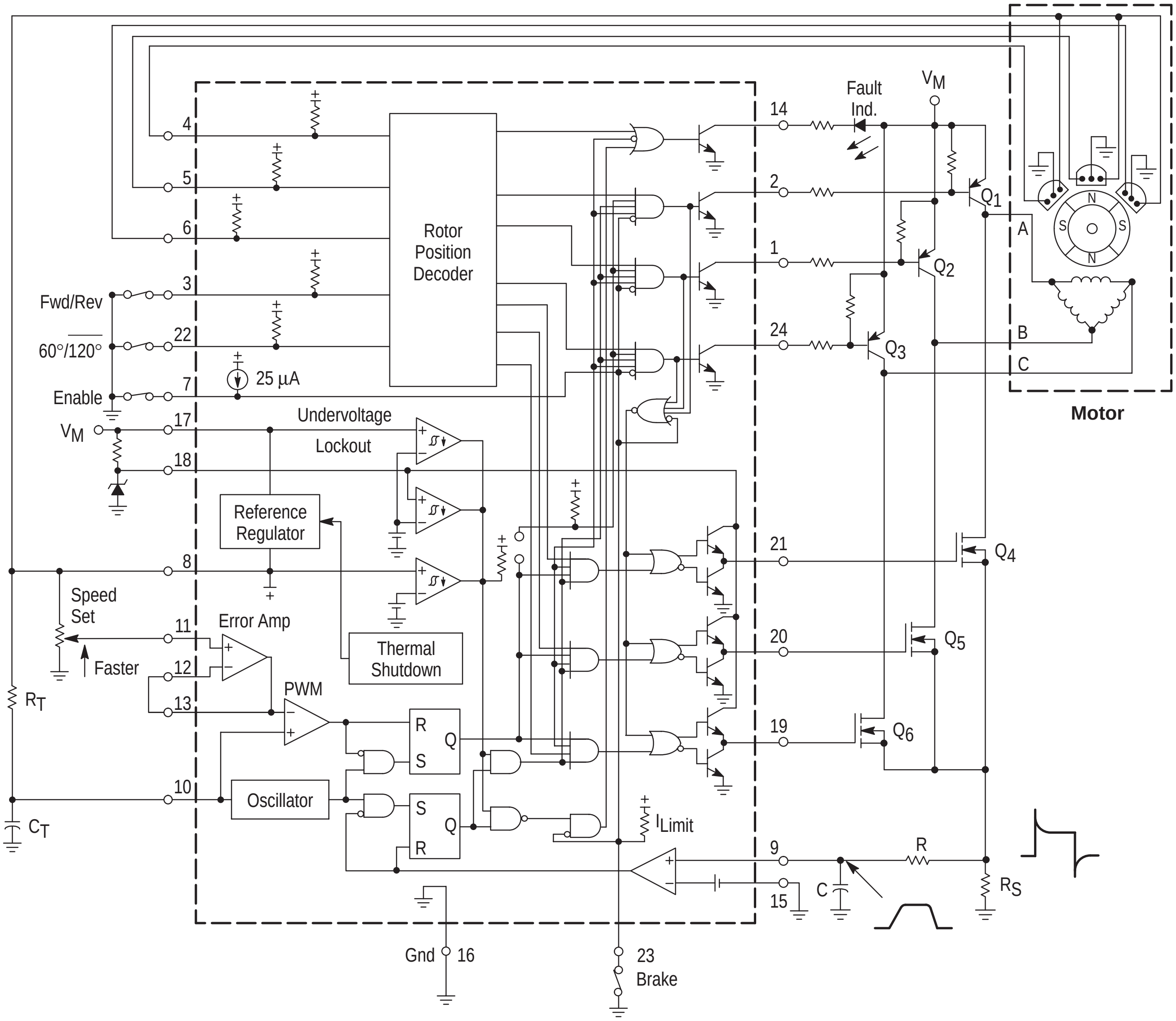


Figure 37. Three Phase, Six Step, Full Wave Commutation Waveforms

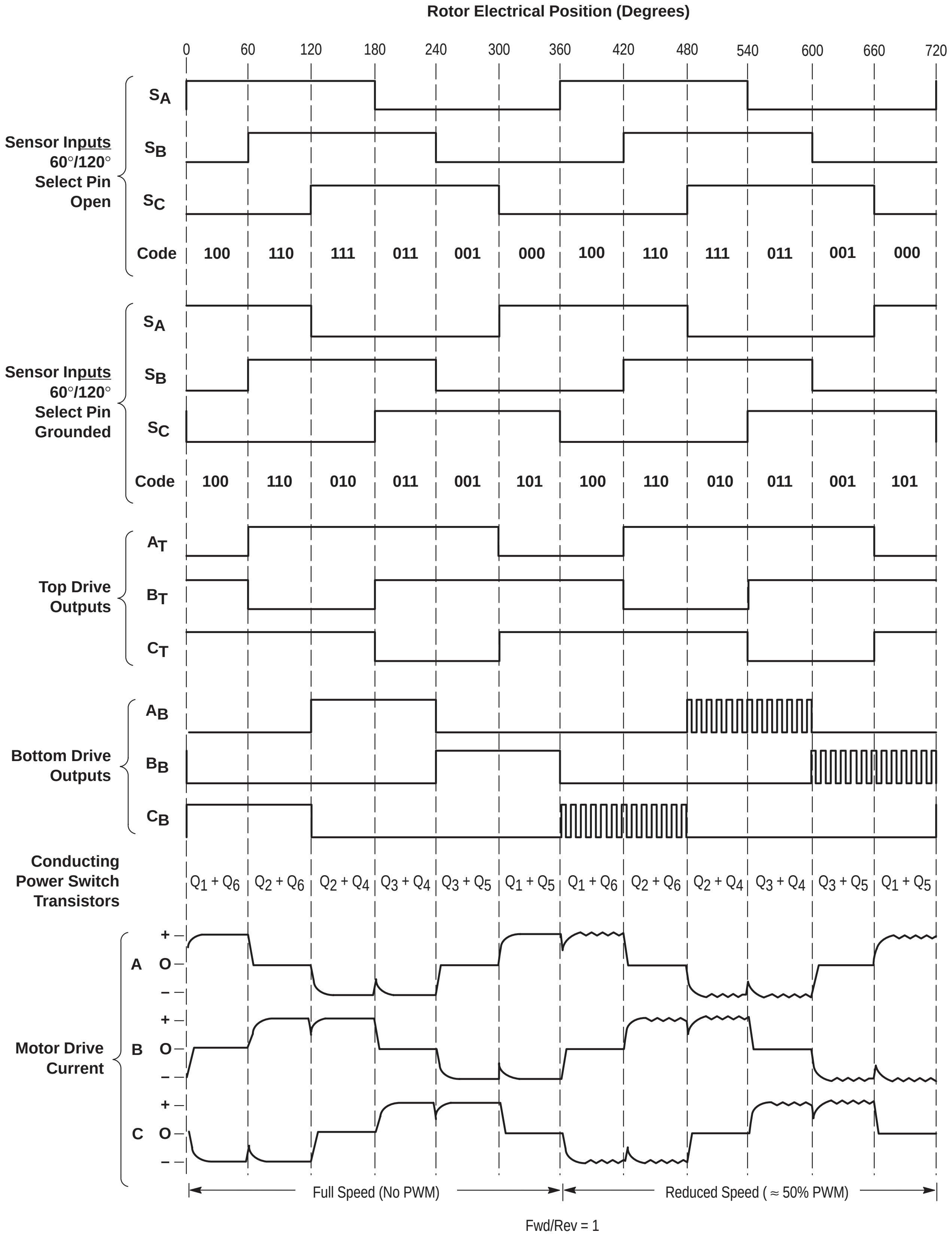
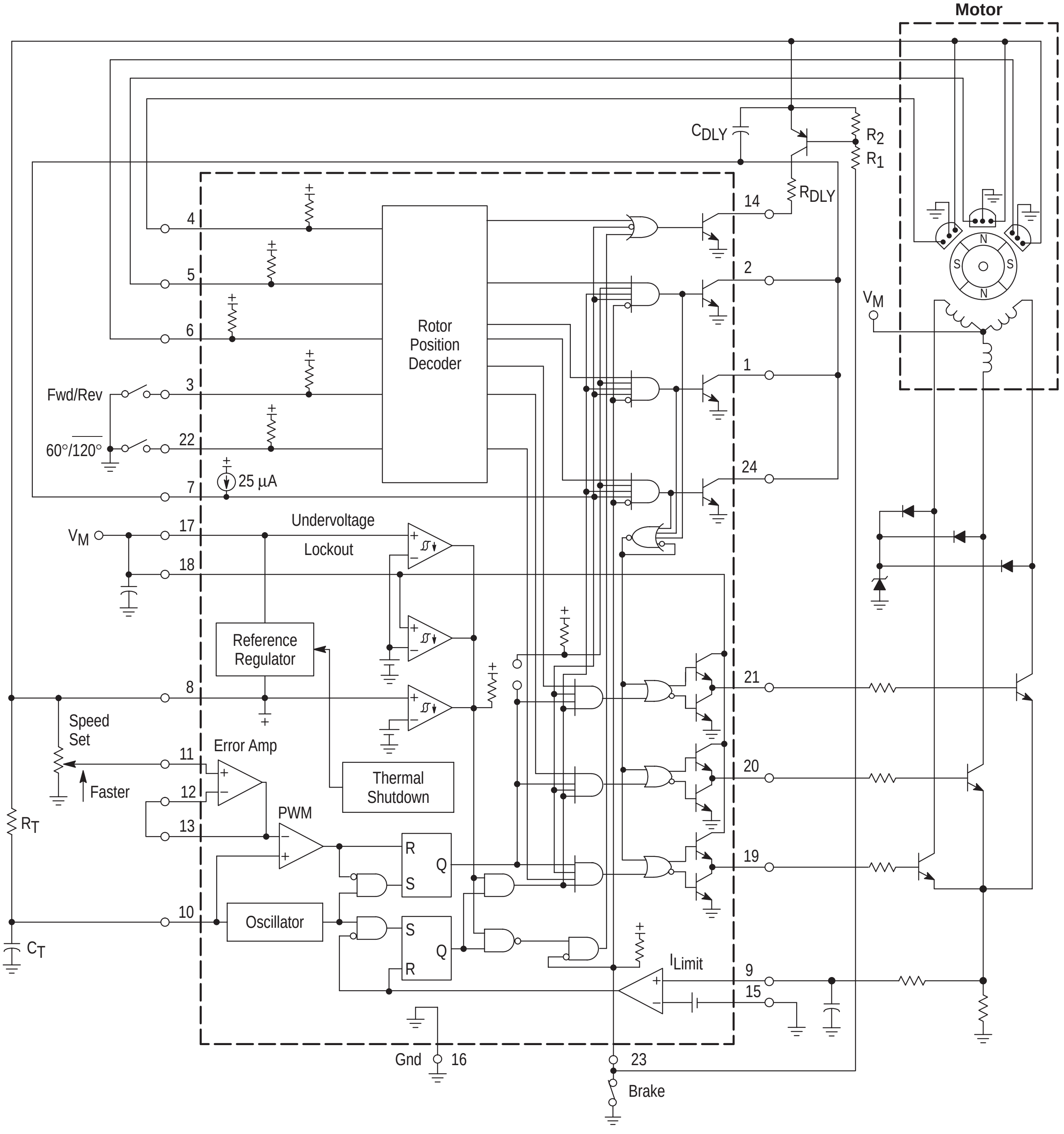


Figure 38 shows a three phase, three step, half wave motor controller. This configuration is ideally suited for automotive and other low voltage applications since there is only one power switch voltage drop in series with a given stator winding. Current flow is unidirectional or half wave because only one end of each winding is switched. Continuous braking with the typical half wave arrangement presents a motor overheating problem since stator current is limited only by the winding resistance. This is due to the lack of upper power switch transistors, as in the full wave circuit, used to disconnect the windings from the supply voltage V_M. A unique solution is to provide braking until the motor stops and then turn off the bottom drives. This can be accomplished by using the Fault Output in conjunction with the Output Enable as an over current timer. Components R_{DLY} and C_{DLY} are selected to give the motor sufficient time to stop before latching the Output Enable and the top drive AND gates low. When enabling the motor, the brake switch is closed and the PNP transistor (along with resistors R_1 and R_{DLY}) are used to reset the latch by discharging C_{DLY}. The stator flyback voltage is clamped by a single zener and three diodes.

Figure 38. Three Phase, Three Step, Half Wave Motor Controller

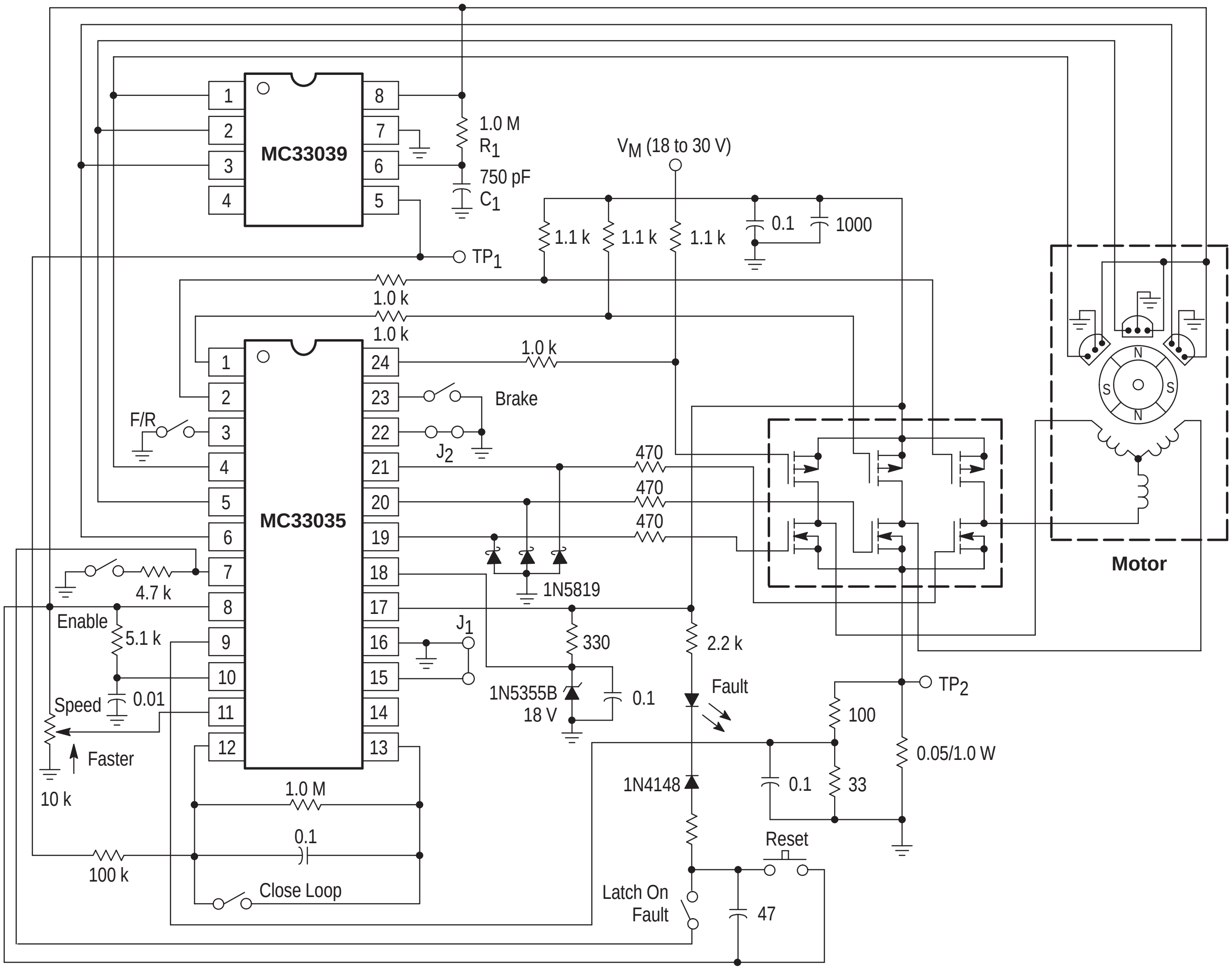


Three Phase Closed Loop Controller

The MC33035, by itself, is only capable of open loop motor speed control. For closed loop motor speed control, the MC33035 requires an input voltage proportional to the motor speed. Traditionally, this has been accomplished by means of a tachometer to generate the motor speed feedback voltage. Figure 39 shows an application whereby an MC33039, powered from the 6.25 V reference (Pin 8) of the MC33035, is used to generate the required feedback voltage without the need of a costly tachometer. The same Hall sensor signals used by the MC33035 for rotor position decoding are utilized by the MC33039. Every positive or negative going transition of the Hall sensor signals on any of the sensor lines causes the MC33039 to produce an output pulse of defined amplitude and time duration, as determined by the external resistor R_1 and capacitor C_1. The output train of pulses at Pin 5 of the MC33039 are integrated by the error amplifier of the MC33035 configured as an integrator to produce a DC voltage level which is proportional to the motor speed. This speed proportional voltage establishes the PWM reference level at Pin 13 of the MC33035 motor controller and closes the feedback loop. The MC33035 outputs drive a TMOS power MOSFET 3–phase bridge. High currents can be expected during conditions of start–up, breaking, and change of direction of the motor.

The system shown in Figure 39 is designed for a motor having 120/240 degrees Hall sensor electrical phasing. The system can easily be modified to accommodate 60/300 degree Hall sensor electrical phasing by removing the jumper (J_2) at Pin 22 of the MC33035.

Figure 39. Closed Loop Brushless DC Motor Control Using The MC33035 and MC33039



Sensor Phasing Comparison

There are four conventions used to establish the relative phasing of the sensor signals in three phase motors. With six step drive, an input signal change must occur every 60 electrical degrees; however, the relative signal phasing is dependent upon the mechanical sensor placement. A comparison of the conventions in electrical degrees is shown in Figure 40. From the sensor phasing table in Figure 41, note that the order of input codes for 60° phasing is the reverse of 300°. This means the MC33035, when configured for 60° sensor electrical phasing, will operate a motor with either 60° or 300° sensor electrical phasing, but resulting in opposite directions of rotation. The same is true for the part when it is configured for 120° sensor electrical phasing; the motor will operate equally, but will result in opposite directions of rotation for 120° for 240° conventions.

Figure 40. Sensor Phasing Comparison

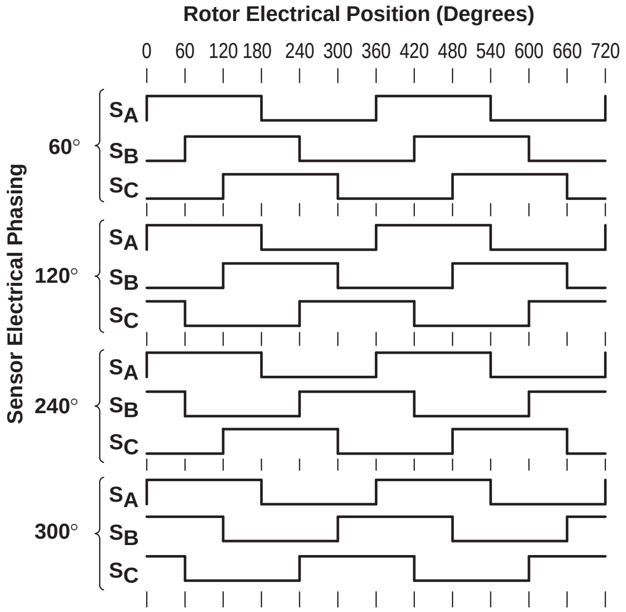


Figure 41. Sensor Phasing Table

Sensor Electrical Phasing (Degrees)											
60°			120°			240°			300°		
S_A	S_B	S_C	S_A	S_B	S_C	S_A	S_B	S_C	S_A	S_B	S_C
1	**0**	**0**	1	0	1	1	1	0	1	**1**	1
1	**1**	0	1	0	0	1	0	0	1	**1**	0
1	**1**	1	1	1	0	1	0	1	**1**	**0**	**0**
0	1	1	0	1	0	0	0	1	0	0	0
0	0	1	0	1	1	0	1	1	0	0	1
0	0	0	0	0	1	0	1	0	0	1	1

In this data sheet, the rotor position is always given in electrical degrees since the mechanical position is a function of the number of rotating magnetic poles. The relationship between the electrical and mechanical position is:

$$\text{Electrical Degrees} = \text{Mechanical Degrees}\left(\frac{\text{\#Rotor Poles}}{2}\right)$$

An increase in the number of magnetic poles causes more electrical revolutions for a given mechanical revolution. General purpose three phase motors typically contain a four pole rotor which yields two electrical revolutions for one mechanical.

Two and Four Phase Motor Commutation

The MC33035 is also capable of providing a four step output that can be used to drive two or four phase motors. The truth table in Figure 42 shows that by connecting sensor inputs S_B and S_C together, it is possible to truncate the number of drive output states from six to four. The output power switches are connected to B_T, C_T, B_B, and C_B. Figure 43 shows a four phase, four step, full wave motor control application. Power switch transistors Q_1 through Q_8 are Darlington type, each with an internal parasitic catch diode. With four step drive, only two rotor position sensors spaced at 90 electrical degrees are required. The commutation waveforms are shown in Figure 44.

Figure 45 shows a four phase, four step, half wave motor controller. It has the same features as the circuit in Figure 38, except for the deletion of speed control and braking.

Figure 42. Two and Four Phase, Four Step, Commutation Truth Table

MC33035 (60°/$\overline{120^\circ}$ Select Pin Open)						
Inputs			Outputs			
Sensor Electrical Spacing* = 90°			Top Drives		Bottom Drives	
S_A	S_B	F/R	B_T	C_T	B_B	C_B
1	0	1	1	1	0	1
1	1	1	0	1	0	0
0	1	1	1	0	0	0
0	0	1	1	1	1	0
1	0	0	1	0	0	0
1	1	0	1	1	1	0
0	1	0	1	1	0	1
0	0	0	0	1	0	0

*With MC33035 sensor input S_B connected to S_C.

Figure 43. Four Phase, Four Step, Full Wave Motor Controller

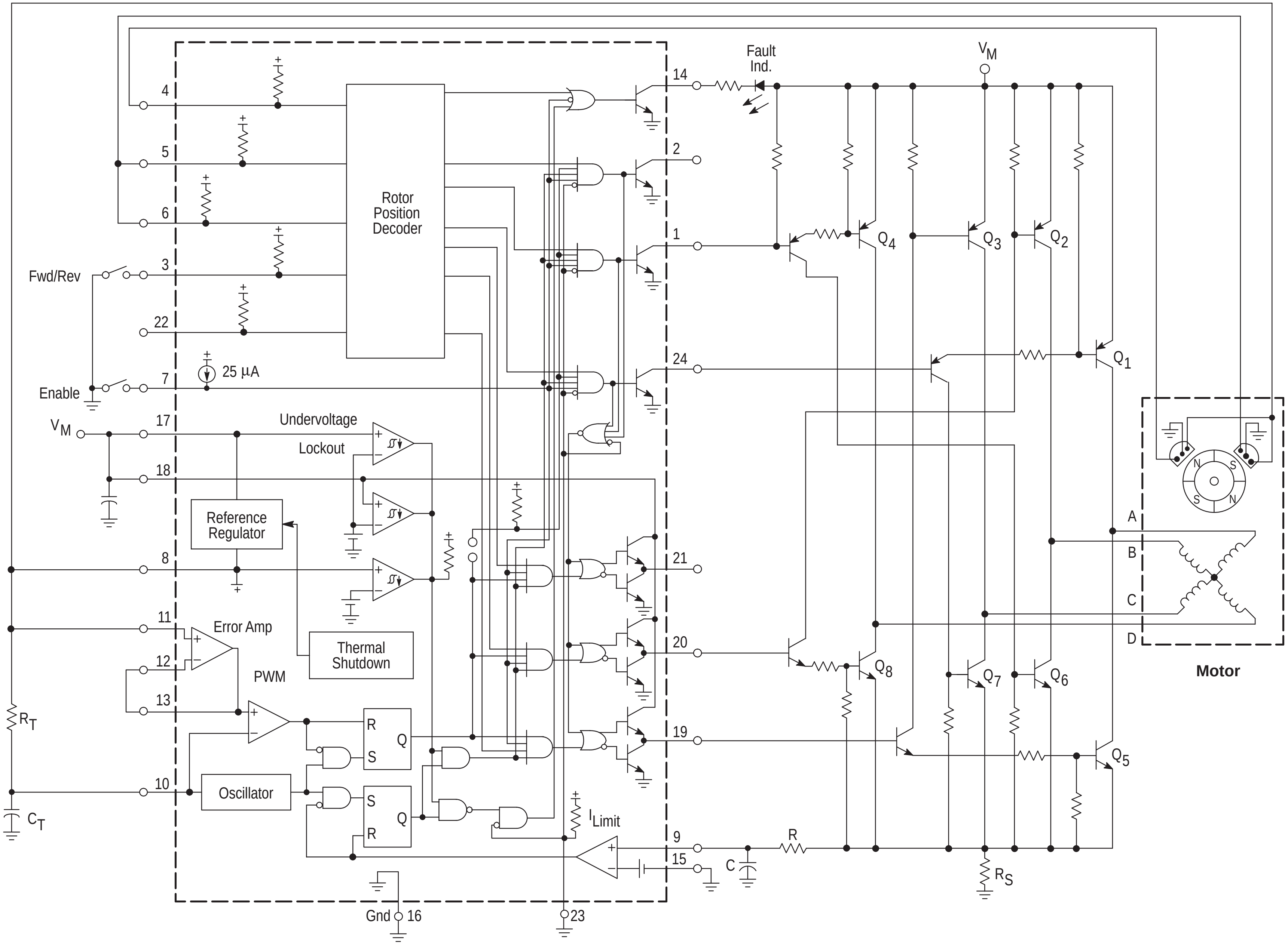


Figure 44. Four Phase, Four Step, Full Wave Motor Controller

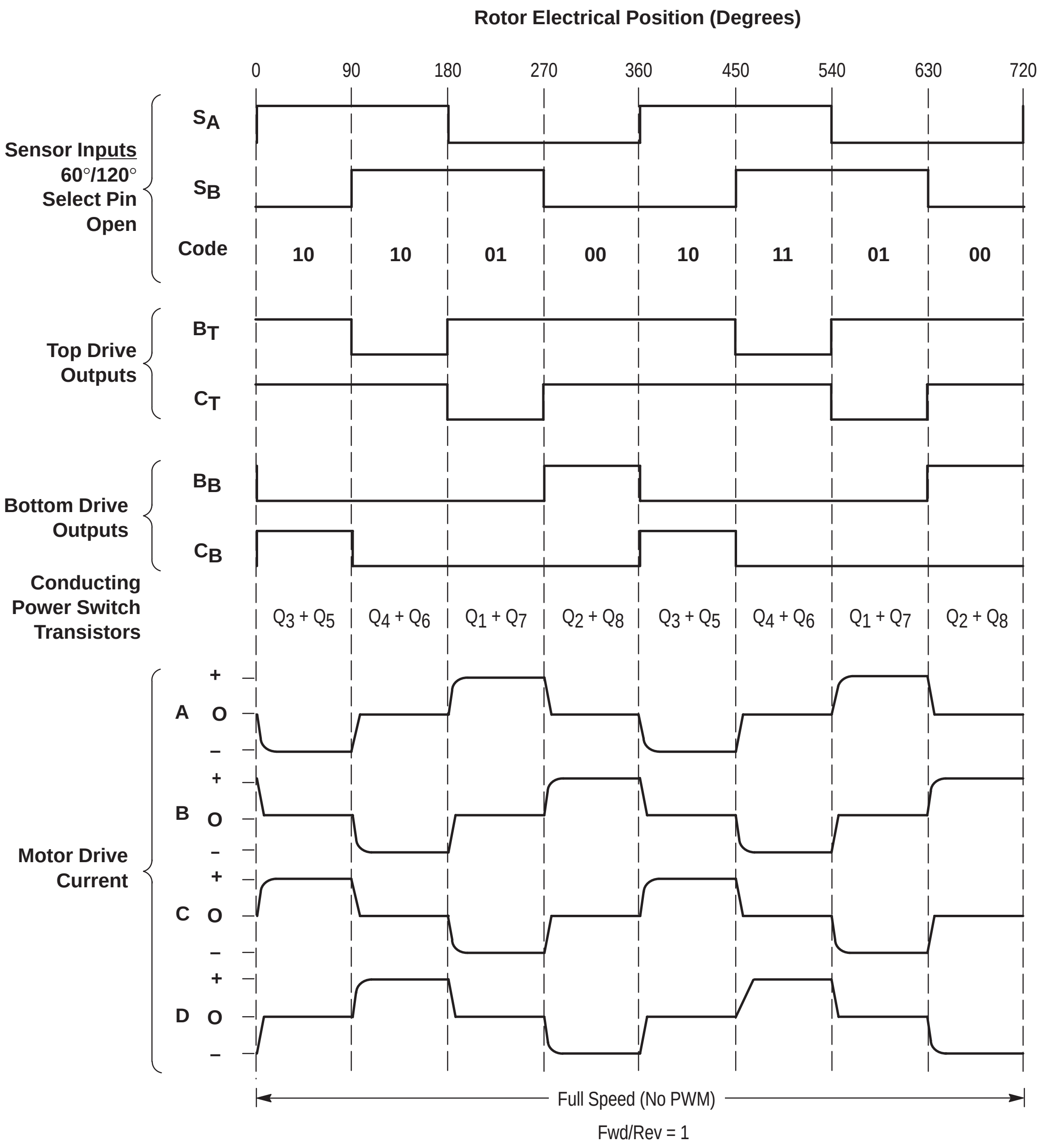
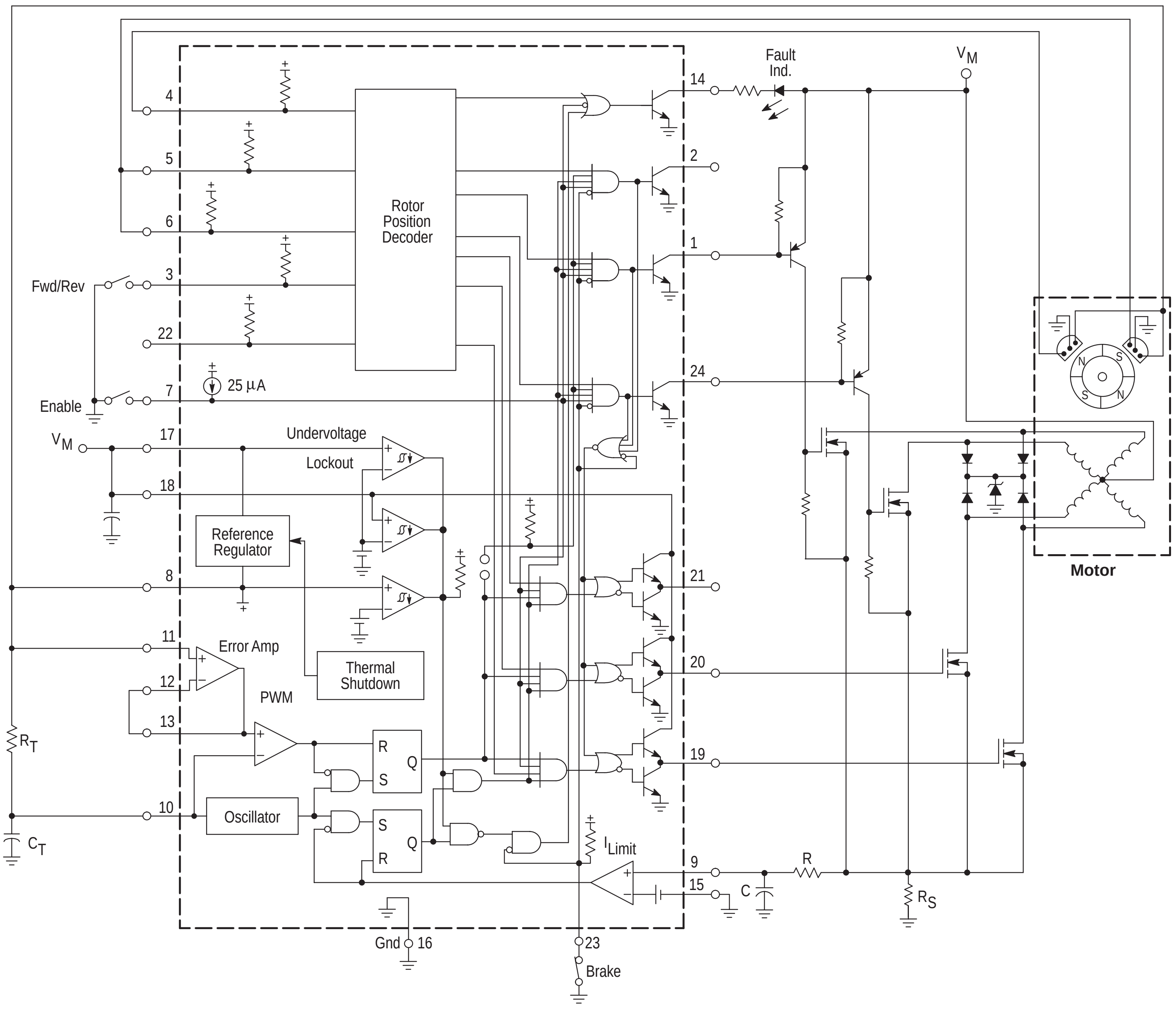


Figure 45. Four Phase, Four Step, Half Wave Motor Controller



Brush Motor Control

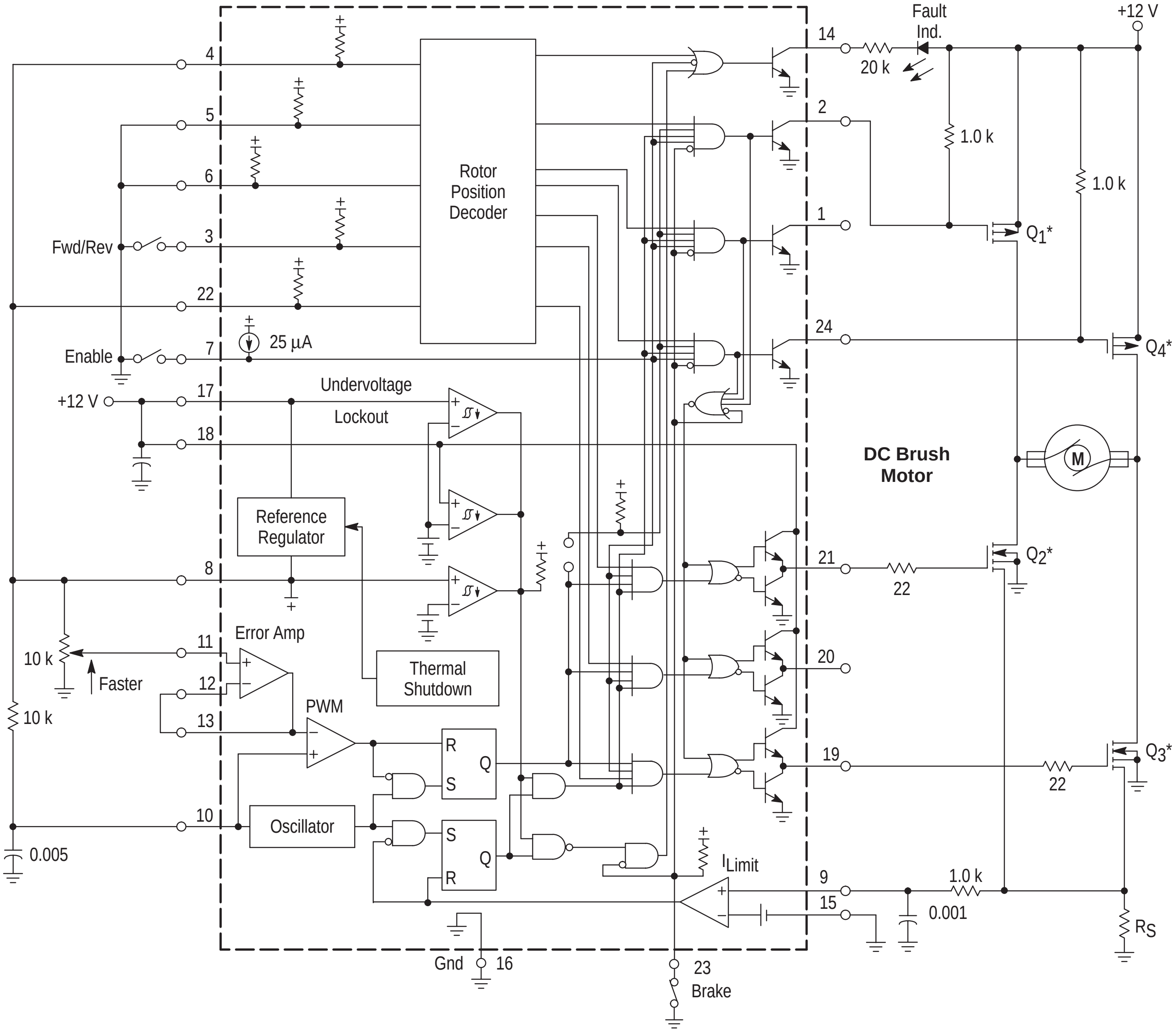
Though the MC33035 was designed to control brushless DC motors, it may also be used to control DC brush type motors. Figure 46 shows an application of the MC33035 driving a MOSFET H–bridge affording minimal parts count to operate a brush–type motor. Key to the operation is the input sensor code [100] which produces a top–left (Q_1) and a bottom–right (Q_3) drive when the controller's forward/reverse pin is at logic [1]; top–right (Q_4), bottom–left (Q_2) drive is realized when the Forward/Reverse pin is at logic [0]. This code supports the requirements necessary for H–bridge drive accomplishing both direction and speed control.

The controller functions in a normal manner with a pulse width modulated frequency of approximately 25 kHz. Motor speed is controlled by adjusting the voltage presented to the noninverting input of the error amplifier establishing the PWM's slice or reference level. Cycle–by–cycle current limiting of the motor current is accomplished by sensing the voltage (100 mV) across the R_S resistor to ground of the H–bridge motor current. The over current sense circuit makes it possible to reverse the direction of the motor, using the normal forward/reverse switch, on the fly and not have to completely stop before reversing.

LAYOUT CONSIDERATIONS

Do not attempt to construct any of the brushless motor control circuits on wire–wrap or plug–in prototype boards. High frequency printed circuit layout techniques are imperative to prevent pulse jitter. This is usually caused by excessive noise pick–up imposed on the current sense or error amp inputs. The printed circuit layout should contain a ground plane with low current signal and high drive and output buffer grounds returning on separate paths back to the power supply input filter capacitor V_M. Ceramic bypass capacitors (0.1 µF) connected close to the integrated circuit at V_{CC}, V_C, V_{ref} and the error amp noninverting input may be required depending upon circuit layout. This provides a low impedance path for filtering any high frequency noise. All high current loops should be kept as short as possible using heavy copper runs to minimize radiated EMI.

Figure 46. H–Bridge Brush–Type Controller



MOTOROLA

MC33039

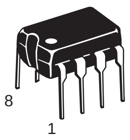
Closed Loop Brushless Motor Adapter

The MC33039 is a high performance closed–loop speed control adapter specifically designed for use in brushless DC motor control systems. Implementation will allow precise speed regulation without the need for a magnetic or optical tachometer. This device contains three input buffers each with hysteresis for noise immunity, three digital edge detectors, a programmable monostable, and an internal shunt regulator. Also included is an inverter output for use in systems that require conversion of sensor phasing. Although this device is primarily intended for use with the MC33035 brushless motor controller, it can be used cost effectively in many other closed–loop speed control applications.

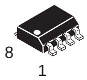
- Digital Detection of Each Input Transition for Improved Low Speed Motor Operation
- TTL Compatible Inputs With Hysteresis
- Operation Down to 5.5 V for Direct Powering from MC33035 Reference
- Internal Shunt Regulator Allows Operation from a Non–Regulated Voltage Source
- Inverter Output for Easy Conversion between 60°/300° and 120°/240° Sensor Phasing Conventions

CLOSED LOOP BRUSHLESS MOTOR ADAPTER

SEMICONDUCTOR TECHNICAL DATA

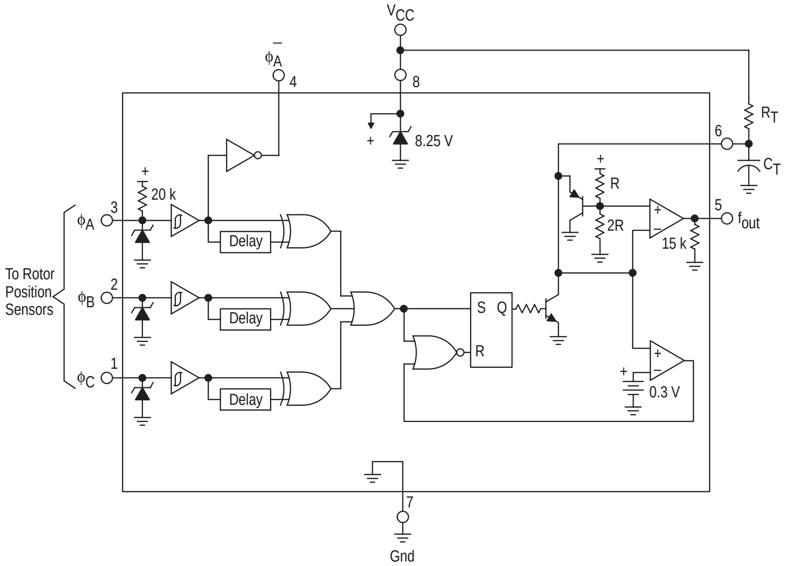


P SUFFIX
PLASTIC PACKAGE
CASE 626

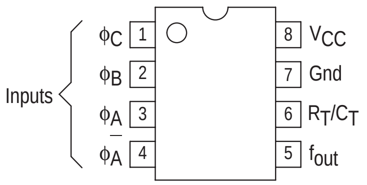


D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

Representative Block Diagram



PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC33039D	T_A = – 40° to +85°C	SO–8
MC33039P		Plastic DIP

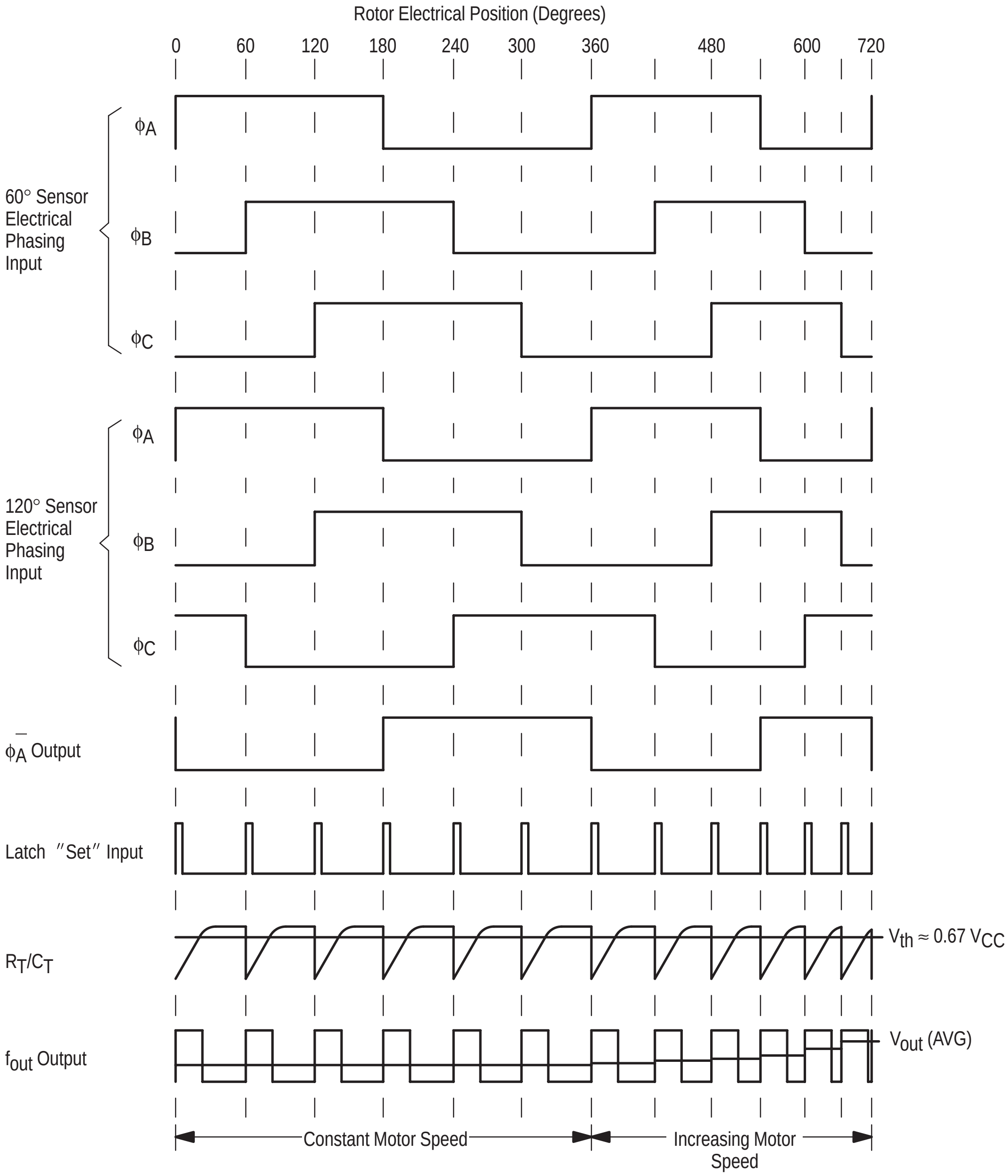
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
V_{CC} Zener Current	$I_{Z(V_{CC})}$	30	mA
Logic Input Current (Pins 1, 2, 3)	I_{IH}	5.0	mA
Output Current (Pins 4, 5), Sink or Source	I_{DRV}	20	mA
Power Dissipation and Thermal Characteristics Maximum Power Dissipation @ T_A = + 85°C Thermal Resistance, Junction–to–Air	 P_D $R_{\theta JA}$	 650 100	 mW °C/W
Operating Junction Temperature	T_J	+ 150	°C
Operating Ambient Temperature Range	T_A	– 40 to + 85	°C
Storage Temperature Range	T_{stg}	– 65 to + 150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 6.25 V, R_T = 10 k, C_T = 22 nF, T_A = 25°C, unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
LOGIC INPUTS					
Input Threshold Voltage High State Low State Hysteresis	 V_{IH} V_{IL} V_H	 2.4 — 0.4	 2.1 1.4 0.7	 — 1.0 0.9	V
Input Current High State (V_{IH} = 5.0 V) ϕA ϕB, ϕC Low State (V_{IL} = 0 V) ϕA ϕB, ϕC	 I_{IH} I_{IL} 	 – 40 — – 190 —	 – 60 – 0.3 – 300 – 0.3	 – 80 – 5.0 – 380 – 5.0	µA
MONOSTABLE AND OUTPUT SECTIONS					
Output Voltage High State $f_{\overline{out}}$ (I_{source} = 5.0 mA) ϕA (I_{source} = 2.0 mA) Low State $f_{\overline{out}}$ (I_{sink} = 10 mA) ϕA (I_{sink} = 10 mA)	 V_{OH} V_{OL} 	 3.60 4.20 — —	 3.95 4.75 0.25 0.25	 4.20 — 0.50 0.50	V
Capacitor C_T Discharge Current	I_{dischg}	20	35	60	mA
Output Pulse Width (Pin 5)	t_{PW}	205	225	245	µs
POWER SUPPLY SECTION					
Power Supply Operating Voltage Range (T_A = – 40° to + 85°C)	V_{CC}	5.5	—	V_Z	V
Power Supply Current	I_{CC}	1.8	3.9	5.0	mA
Zener Voltage (I_Z = 10 mA)	V_Z	7.5	8.25	9.0	V
Zener Dynamic Impedance (ΔI_Z = 10 mA to 20 mA, f $\leqslant$ 1.0 kHz)	$\lvert Z_{ka} \rvert$	—	2.0	5.0	Ω

Figure 1. Typical Three Phase, Six Step Motor Application



OPERATING DESCRIPTION

The MC33039 provides an economical method of implementing closed–loop speed control of brushless DC motors by eliminating the need for a magnetic or optical tachometer. Shown in the timing diagram of Figure 1, the three inputs (Pins 1, 2, 3) monitor the brushless motor rotor position sensors. Each sensor signal transition is digitally detected, OR′ed at the Latch ′Set′ Input, and causes C_T to discharge. A corresponding output pulse is generated at f_{out} (Pin 5) of a defined amplitude, and programmable width determined by the values selected for R_T and C_T (Pin 6). The average voltage of the output pulse train increases with motor speed. When fed through a low pass filter or integrator, a DC voltage proportional to speed is generated. Figure 2 shows the proper connections for a typical closed loop application using the MC33035 brushless motor controller. Constant speed operation down to 100 RPM is possible with economical three phase four pole motors.

The $\overline{\phi_A}$ inverter output (Pin 4) is used in systems where the controller and motor sensor phasing conventions are not compatible. A method of converting from either convention to the other is shown in Figure 3. For a more detailed explanation of this subject, refer to the text above Figure 39 on the MC33035 data sheet.

The output pulse amplitude V_{OH} is constant with temperature and controlled by the supply voltage on V_{CC} (Pin 8). Operation down to 5.5 V is guaranteed over temperature. For systems without a regulated power supply, an internal 8.25 V shunt regulator is provided.

Figure 2. Typical Closed Loop Speed Control Application

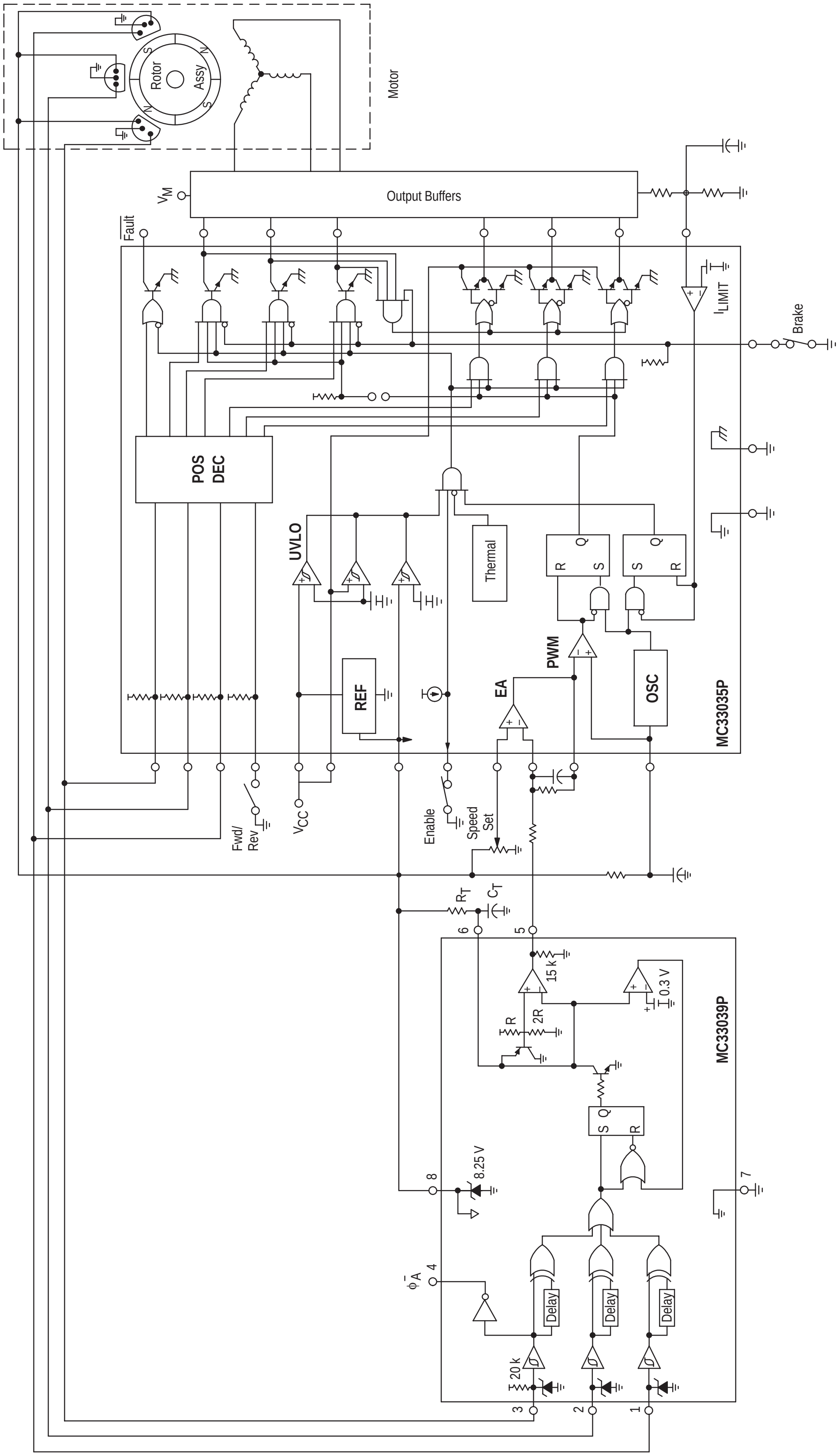


Figure 3. f_{out}, Pulse Width versus Timing Resistor

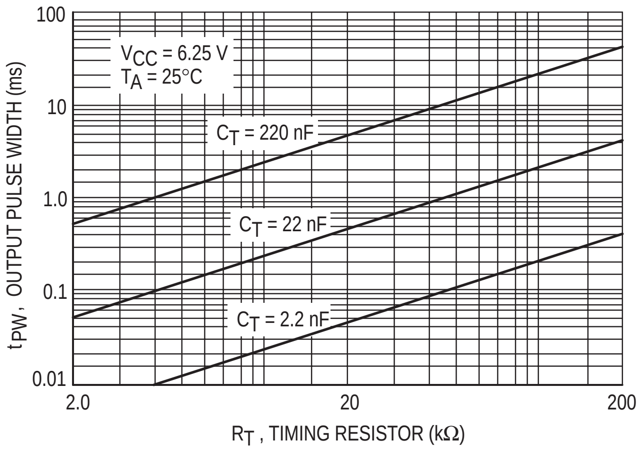


Figure 4. f_{out}, Pulse Width Change versus Temperature

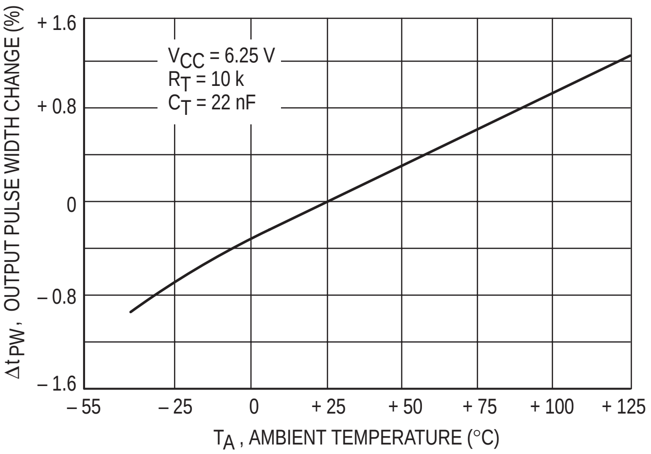


Figure 5. f_{out}, Pulse Width Change versus Supply Voltage

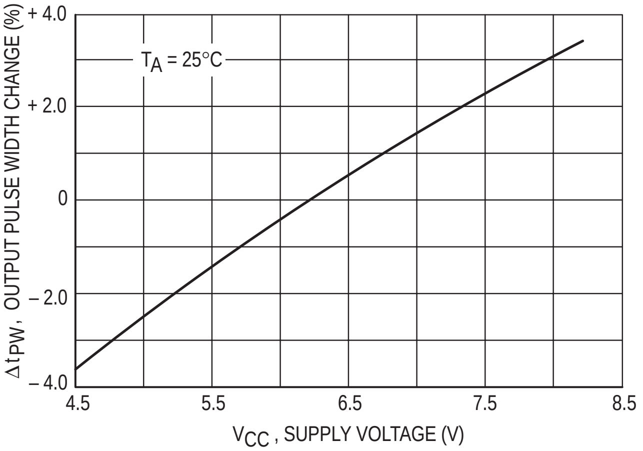


Figure 6. Supply Current versus Supply Voltage

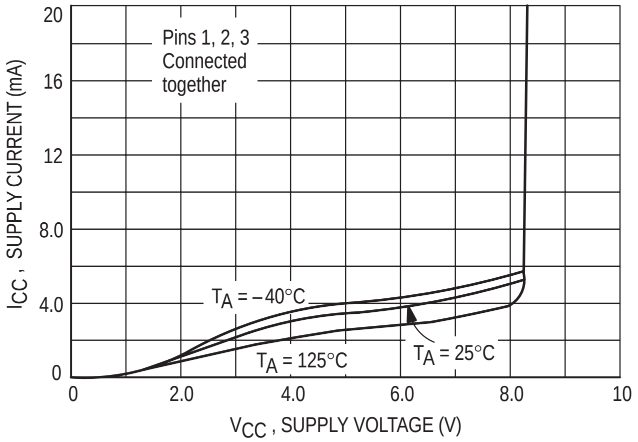


Figure 7. f_{out}, Saturation versus Load Current

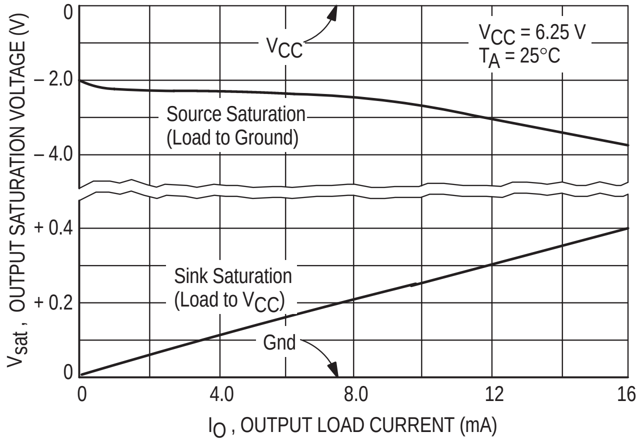
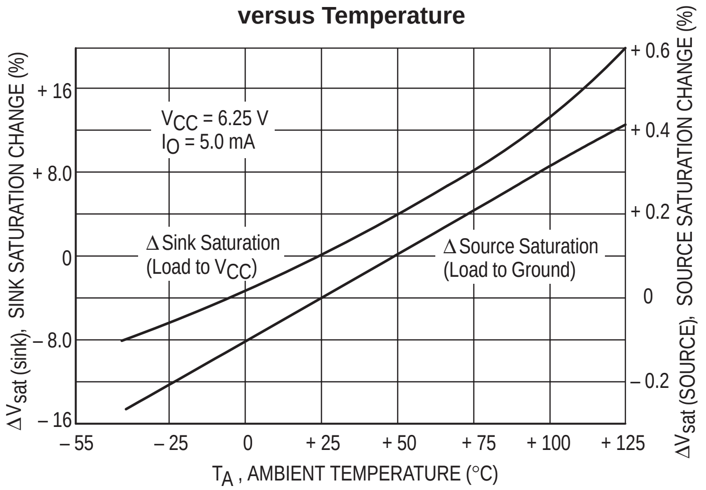


Figure 8. f_{out}, Saturation Change versus Temperature



MOTOROLA

SAA1042

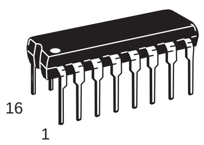
Stepper Motor Driver

The SAA1042 drives a two–phase stepper motor in the bipolar mode. The device contains three input stages, a logic section and two output stages. The IC is contained in a 16 pin dual–in–line heat tab plastic package for improved heatsinking capability. The center four ground pins are connected to the copper alloy heat tab and improve thermal conduction from the die to the circuit board.

- Drive Stages Designed for Motors: 6.0 V and 12 V: SAA1042V
- 500 mA/Coil Drive Capability
- Built–In Clamp Diodes for Overvoltage Suppression
- Wide Logic Supply Voltage Range
- Accepts Commands for CW/CCW and Half/Full Step Operation
- Inputs Compatible with Popular Logic Families: MOS, TTL, DTL
- Set Input Defined Output State
- Drive Stage Bias Adaptable to Motor Power Dissipation for Optimum Efficiency

STEPPER MOTOR DRIVER

SEMICONDUCTOR TECHNICAL DATA



V SUFFIX
PLASTIC PACKAGE
CASE 648C

PIN CONNECTIONS

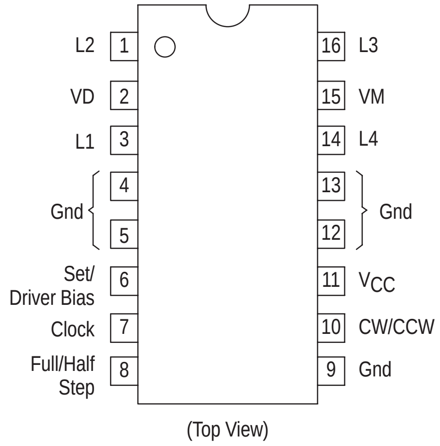
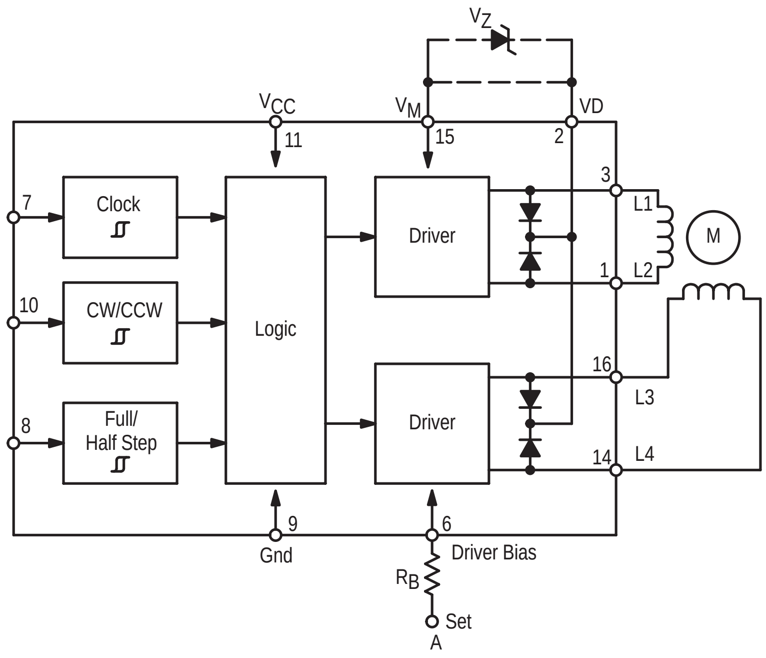


Figure 1. Representative Block Diagram



ORDERING INFORMATION

Device	Operating Temperature Range	Package
SAA1042V	T_J = – 30° to +125°C	Plastic DIP

MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted.)

Rating	Symbol	SAA1042V	Unit
Clamping Voltage (Pins 1, 3, 14, 16)	V_{clamp}	20	V
Over Voltage ($V_{OV} = V_{clamp} – V_M$)	V_{OV}	6.0	V
Supply Voltage	V_{CC}	20	V
Switching or Motor Current/Coil	I_M	500	mA
Input Voltage (Pins 7, 8, 10)	V_{in} clock V_{in} Full/Half V_{in} CW/CCW	V_{CC}	V
Power Dissipation (Note 1) Thermal Resistance, Junction–to–Air Thermal Resistance, Junction–to–Case	P_D θJA θJC	2.0 80 15	W °C/W
Operating Junction Temperature Range	T_J	–30 to +125	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

NOTE: 1. The power dissipation (P_D) of the circuit is given by the supply voltage (V_M and V_{CC}) and the motor current (I_M), and can be determined from Figures 3 and 5. $P_D = P_{drive} – P_{logic}$.

ELECTRICAL CHARACTERISTICS (T_A = 25°C, unless otherwise noted.)

Characteristics	Pin(s)	Symbol	V_{CC}	Min	Typ	Max	Unit
Supply Current	11	I_{CC}	5.0 V 20 V	— —	— —	3.5 8.5	mA
Motor Supply Current ($I_{Pin\ 6}$ = –400 µA, Pins 1, 3, 14, 16 Open) V_M = 6.0 V V_M = 12 V V_M = 24 V	15	I_M	5.0 V 5.0 V 5.0 V	— — —	25 30 40	— — —	mA
Input Voltage, High State	7, 8, 10	V_{IH}	5.0 V 10 V 15 V 20 V	2.0 7.0 10 14	— — — —	— — — —	V
Input Voltage, Low State		V_{IL}	5.0 V 10 V 15 V 20 V	— — — —	— — — —	0.8 1.5 2.5 3.5	
Input Reverse Current, High State ($V_{in} = V_{CC}$)	7, 8, 10	I_{IR}	5.0 V 10 V 15 V 20 V	— — — —	— — — —	2.0 2.0 3.0 5.0	µA
Input Forward Current, Low State (V_{in} = Gnd)		I_{IF}	5.0 V 10 V 15 V 20 V	–10 –25 –40 –50	— — — —	— — — —	
Output Voltage, High State (V_M = 12 V) I_{out} = –500 mA I_{out} = –50 mA	1, 3, 14, 16	V_{OH}	5.0 – 20 V	— —	V_M – 2.0 V_M – 1.2	— —	V
Output Voltage, Low State I_{out} = 500 mA I_{out} = 50 mA		V_{OL}	5.0 – 20 V	— —	0.7 0.2	— —	
Output Leakage Current, Pin 6 = Open ($V_M = V_D = V_{clamp\ max}$)	1, 3, 14, 16	I_{DR}	5.0 – 20 V	–100	—	—	µA
Clamp Diode Forward Voltage (Drop at I_M = 500 mA)	2	V_F	—	—	2.5	3.5	V
Clock Frequency	7	f_c	5.0 – 20 V	0	—	50	kHz
Clock Pulse Width	7	t_w	5.0 – 20 V	10	—	—	µs
Set Pulse Width	6	t_s	—	10	—	—	µs
Set Control Voltage, High State Low State	6	—	—	V_M —	— —	— 0.5	V

INPUT/OUTPUT FUNCTIONS

Clock — (Pin 7) This input is active on the positive edge of the clock pulse and accepts Logic ‘1’ input levels dependent on the supply voltage and includes hysteresis for noise immunity.

CW/CCW — (Pin 10) This input determines the motor’s rotational direction. When the input is held low, (OV, see the electrical characteristics) the motor’s direction is nominally clockwise (CW). When the input is in the high state, Logic ‘1’, the motor direction is nominally counter clockwise (CCW), depending on the motor connections.

Full/Half Step — (Pin 8) This input determines the angular rotation of the motor for each clock pulse. In the low state, the motor will make a full step for each applied clock pulse, while in the high state, the motor will make half a step.

V_D — (Pin 2) This pin is used to protect the outputs (1, 3,14, 16) where large positive spikes occur due to switching the motor coils. The maximum allowable voltage on these pins is the clamp voltage (V_{clamp}). Motor performance is improved if a zener diode is connected between Pin 2 and 15, as shown in Figure 1.

The following conditions have to be considered when selecting the zener diode:

$$V_{clamp} = V_M + 6.0\text{ V}$$
$$V_Z = V_{clamp} - V_M - V_F$$

where: V_F = clamp diodes forward voltage drop (see Figure 4)

V_{clamp}: ≤ 20 V for SAA1042V ≤ 30 V for SAA1042AV

Pins 2 and 15 can be linked, in this case $V_Z = 0$ V.

Set/Bias Input — (Pin 6) This input has two functions:

1) The resistor R_B adapts the drivers to the motor current.
2) A pulse via the resistor R_B sets the outputs (1, 3, 14, 16) to a defined state.

The resistor R_B can be determined from the graph of Figure 2 according to the motor current and voltage. Smaller values of R_B will increase the power dissipation of the circuit and larger values of R_B may increase the saturation voltage of the driver transistors.

When the “set” function is not used, terminal A of the resistor R_B must be grounded. When the set function is used, terminal A has to be connected to an open–collector (buffer) circuit. Figure 7 shows this configuration. The buffer circuit (off–state) has to sustain the motor voltage (V_M). When a pulse is applied via the buffer and the bias resistor (R_B), the motor driver transistors are turned off during the pulse and after the pulse has ended, the outputs will be in defined states. Figure 6 shows the Timing Diagram.

Figure 7 illustrates a typical application in which the SAA1042 drives a 12 V stepper motor with a current consumption of 200 mA/coil. A bias resistor (R_B) of 56 kΩ is chosen according to Figure 2.

The maximum voltage permitted at the output pin is V_M + 6.0 V (see Maximum Ratings table), in this application V_M = 12 V, therefore the maximum voltage is 18 V. The outputs are protected by the internal diodes and an external zener connected between Pins 2 and 15.

From Figure 4, it can be seen that the voltage drop across the internal diodes is about 1.7 V at 200 mA. This results in a zener voltage between Pins 2 and 15 of:

$$V_Z = 6.0\text{ V} - 1.7\text{ V} = 4.3\text{ V.}$$

To allow for production tolerances and a safety margin, a 3.9 V zener has been chosen for this example.

The clock is derived from the line frequency which is phase–locked by the MC14046B and the MC14024. The voltage on the clock input is normally low (Logic ‘0’). The motor steps on the positive going transition of the clock pulse.

The Logic ‘0’ applied to the Full/Half input (Pin 8) operates the motor in Full Step mode. A Logic ‘1’ at this input will result in Half Step mode. The logic level state on the CW/CCW input (Pin 10), and the connection of the motor coils to the outputs determines the rotational direction of the motor.

These two inputs should be biased to a Logic ‘0’ or ‘1’ and not left floating. In the event of non–use, they should be tied to ground or the logic supply line, V_{CC}.

The output drivers can be set to a fixed operating point by use of the Set input and a bias resistor, R_B. A positive pulse to this input turns the drivers off and sets the logic state of the outputs.

After the negative going transition of the Set pulse, and until the first positive going transition of the clock, the outputs will be:

L1 = L3 = high and L2 = L4 = low, (see Figure 6).

The Set input can be driven by a MC14007B or a transistor whose collector resistor is R_B. **If the input is not used, the bottom of R_B must be grounded.**

The total power dissipation of the circuit can be determined from Figures 3 and 5:

$$P_D = 0.9\text{ W} + 0.08\text{ W} = 0.98\text{ W.}$$

The junction temperature can then be computed using Figure 8.

Figure 2. Bias Resistor R_B versus Motor Current

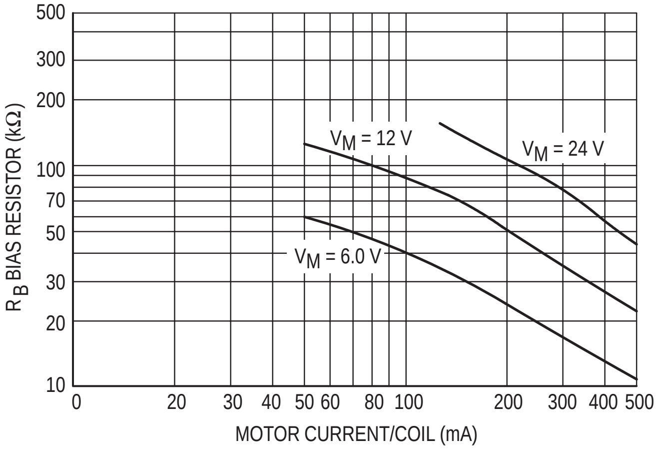


Figure 3. Drive Stage Power Dissipation

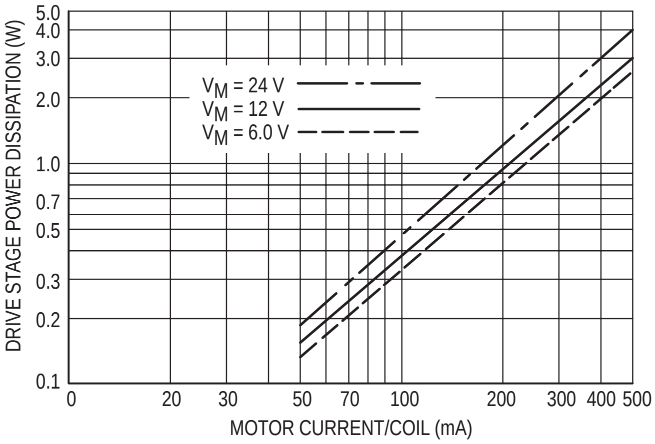


Figure 4. Clamp Diode Forward Current versus Forward Voltage

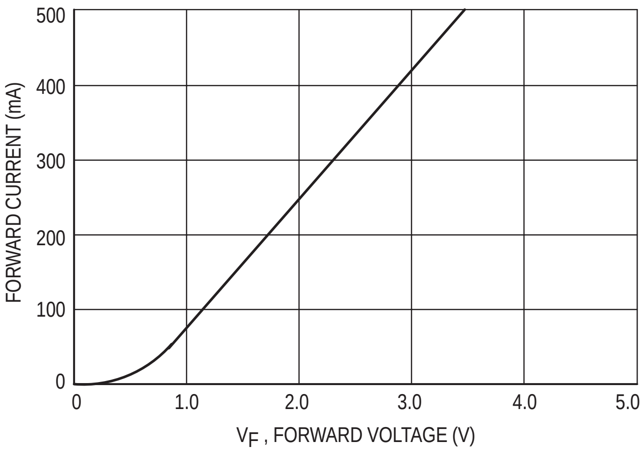


Figure 5. Power Dissipation versus Logic Supply Voltage

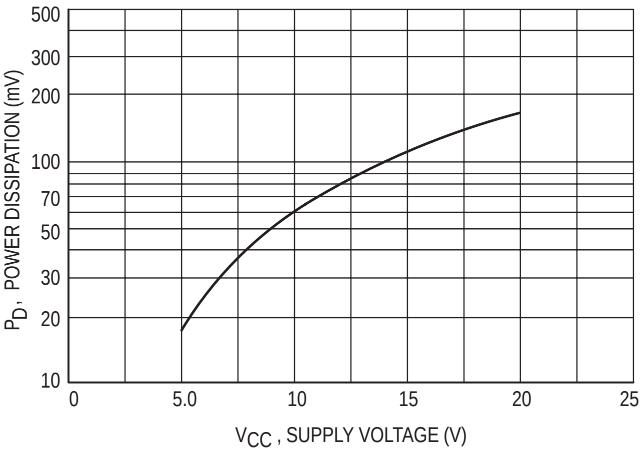


Figure 6. Timing Diagram

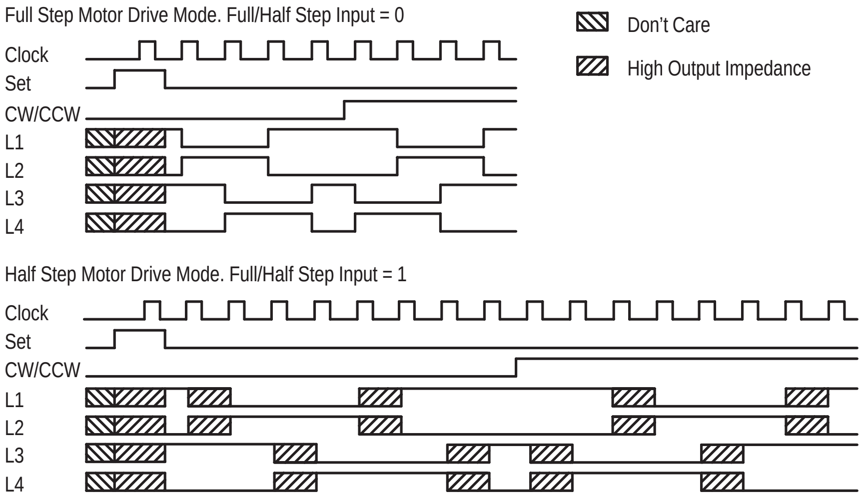


Figure 7. Typical Application
Selectable Step Rates with the Time Base Derived from the Line Frequency

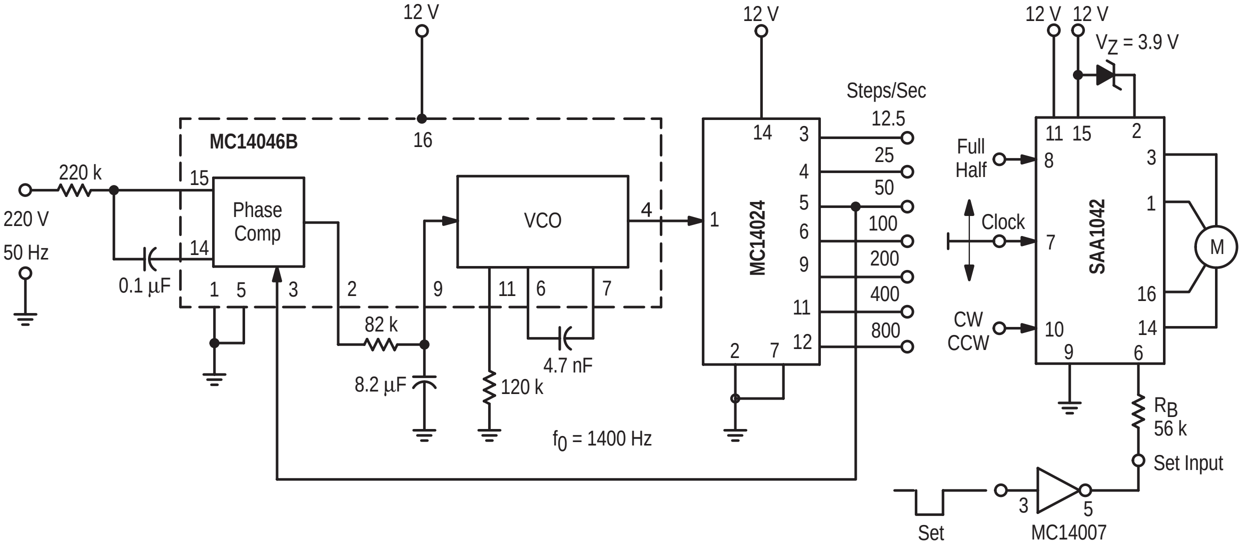
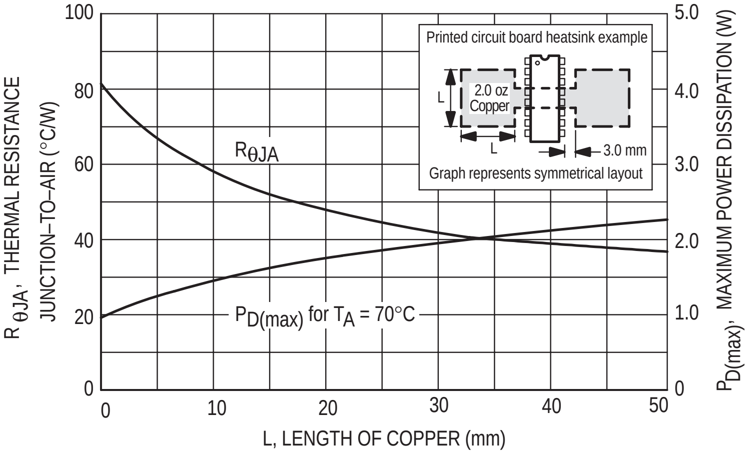


Figure 8. Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length



TDA1085C

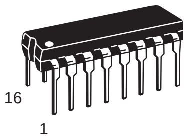
Universal Motor Speed Controller

The TDA1085C is a phase angle triac controller having all the necessary functions for universal motor speed control in washing machines. It operates in closed loop configuration and provides two ramp possibilities.

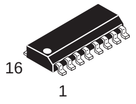
- On–Chip Frequency to Voltage Converter
- On–Chip Ramps Generator
- Soft–Start
- Load Current Limitation
- Tachogenerator Circuit Sensing
- Direct Supply from AC Line
- Security Functions Peformed by Monitor

UNIVERSAL MOTOR SPEED CONTROLLER

SEMICONDUCTOR TECHNICAL DATA



PLASTIC PACKAGE
CASE 648

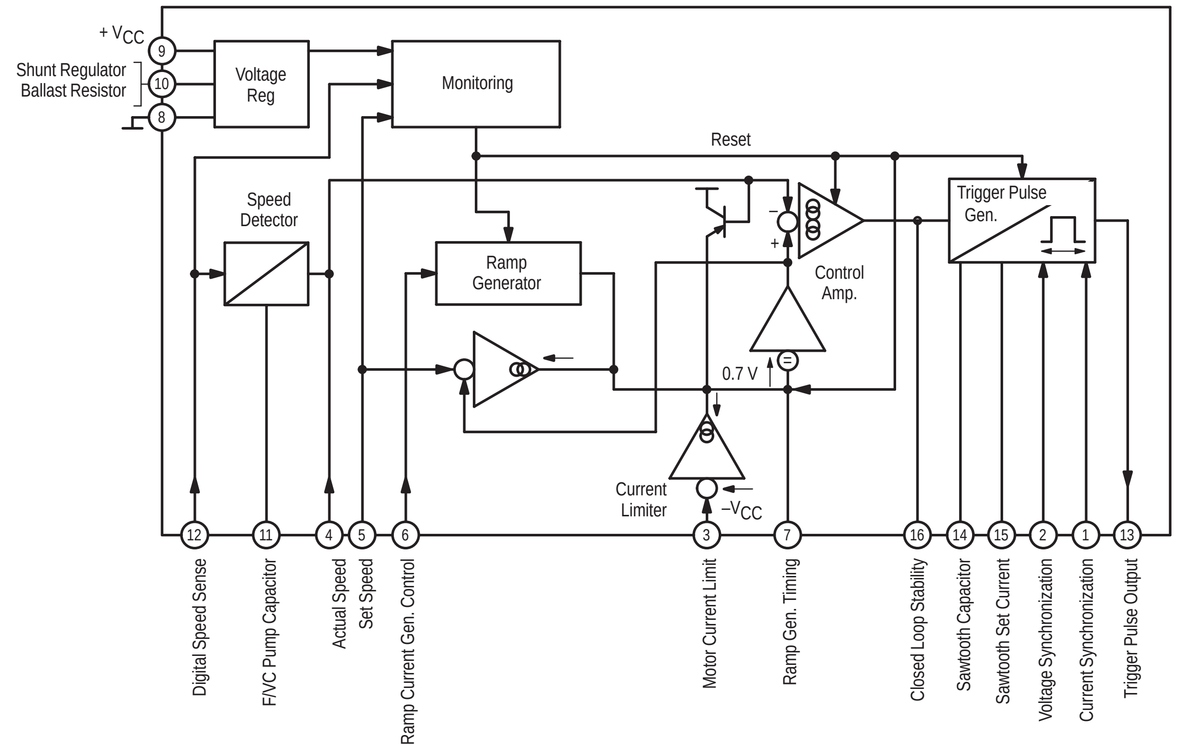


D SUFFIX
PLASTIC PACKAGE
CASE 751B
(SO–16)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
TDA1085CD	T_J = – 10° to +120°C	SO–16
TDA1085C		Plastic DIP

Figure 1. Representative Block Diagram and Pin Connections



MAXIMUM RATINGS (T_A = 25°C, voltages are referenced to Pin 8, ground)

Rating	Symbol	Value	Unit
Power Supply, when externally regulated, $V_{Pin\ 9}$	V_{CC}	15	V
Maximum Voltage per listed pin Pin 3 Pin 4–5–6–7–13–14–16 Pin 10	V_{Pin}	 + 5.0 0 to + V_{CC} 0 to + 17	V
Maximum Current per listed pin Pin 1 and 2 Pin 3 Pin 9 (V_{CC}) Pin 10 shunt regulator Pin 12 Pin 13	I_{Pin}	 – 3.0 to + 3.0 – 1.0 to + 0 15 35 – 1.0 to + 1.0 – 200	mA
Maximum Power Dissipation	P_D	1.0	W
Thermal Resistance, Junction–to–Air	$R_{\theta JA}$	65	°C/W
Operating Junction Temperature	T_J	– 10 to + 120	°C
Storage Temperature Range	T_{stg}	– 55 to + 150	°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C)

Characteristic	Symbol	Min	Typ	Max	Unit
VOLTAGE REGULATOR					
Internally Regulated Voltage ($V_{Pin\ 9}$) ($I_{Pin\ 7}$ = 0, $I_{Pin\ 9}$ + $I_{Pin\ 10}$ = 15 mA, $I_{Pin\ 13}$ = 0)	V_{CC}	15	15.3	15.6	V
V_{CC} Temperature Factor	TF	—	– 100	—	ppm/°C
Current Consumption ($I_{Pin\ 9}$) (V_9 = 15 V, V_{12} = V_8 = 0, I_1 = I_2 = 100 µA, all other pins not connected)	I_{CC}	—	4.5	6.0	mA
V_{CC} Monitoring Enable Level Disable Level	V_{CC} EN V_{CC} DIS	— —	V_{CC} – 0.4 V_{CC} – 1.0	— —	V
RAMP GENERATOR					
Reference Speed Input Voltage Range	$V_{Pin\ 5}$	0.08	—	13.5	V
Reference Input Bias Current	– $I_{Pin\ 5}$	0	0.8	1.0	µA
Ramp Selection Input Bias Current	– $I_{Pin\ 6}$	0	—	1.0	µA
Distribution Starting Level Range	V_{DS}	0	—	2.0	V
Distribution Final Level $V_{Pin\ 6}$ = 0.75 V	V_{DF}/V_{DS}	2.0	2.09	2.2	
High Acceleration Charging Current $V_{Pin\ 7}$ = 0 V $V_{Pin\ 7}$ = 10 V	– $I_{Pin\ 7}$	 1.0 1.0	 — 1.2	 1.7 1.4	mA
Distribution Charging Current $V_{Pin\ 7}$ = 2.0 V	– $I_{Pin\ 7}$	4.0	5.0	6.0	µA

ELECTRICAL CHARACTERISTICS (continued)

Characteristic	Symbol	Min	Typ	Max	Unit
CURRENT LIMITER					
Limiter Current Gain — $I_{Pin\ 7}/I_{Pin\ 3}$ (I_{Pin3} = – 300 µA)	C_g	130	180	250	
Detection Threshold Voltage $I_{Pin\ 3}$ = – 10 µA	$V_{Pin\ 3\ TH}$	50	65	80	mV
FREQUENCY TO VOLTAGE CONVERTER					
Input Signal “Low Voltage”	$V_{12\ L}$	–100	—	—	mV
Input Signal “High Voltage”	$V_{12\ H}$	+100	—	—	mV
Monitoring Reset Voltage	$V_{12\ R}$	5.0	—	—	V
Negative Clamping Voltage $I_{Pin\ 12}$ = – 200 µA	– $V_{12\ CL}$	—	0.6	—	V
Input Bias Current	– I_{Pin12}	—	25	—	µA
Internal Current Source Gain $G = \frac{I_{Pin\ 4}}{I_{Pin\ 11}}, V_{Pin\ 4} = V_{Pin\ 11} = 0$	G.0	9.5	—	11	
Gain Linearity versus Voltage on Pin 4 ($G_{8.6}$ = Gain for $V_{Pin\ 4}$ = 8.6 V)	$G/G_{8.6}$				
V_4 = 0 V		1.04	1.05	1.06	
V_4 = 4.3 V		1.015	1.025	1.035	
V_4 = 12 V		0.965	0.975	0.985	
Gain Temperature Effect ($V_{Pin\ 4}$ = 0)	TF	—	350	—	ppm/°C
Output Leakage Current ($I_{Pin\ 11}$ = 0)	– $I_{Pin\ 4}$	0	—	100	nA
CONTROL AMPLIFIER					
Actual Speed Input Voltage Range	$V_{Pin\ 4}$	0	—	13.5	V
Input Offset Voltage $V_{Pin\ 5} – V_{Pin\ 4}$ ($I_{Pin\ 16}$ = 0, $V_{Pin\ 16}$ = 3.0 and 8.0 V)	V_{off}	0	—	50	mV
Amplifier Transconductance ($I_{Pin\ 16}/\Delta\ (V_5 – V_4)$) ($I_{Pin\ 16}$ = + and – 50 µA, $V_{Pin\ 16}$ = 3.0 V)	T	270	340	400	µA/V
Output Current Swing Capability	$I_{Pin\ 16}$				µA
Source		– 200	– 100	– 50	
Sink		50	100	200	
Output Saturation Voltage	$V_{16\ sat}$	—	—	0.8	V
TRIGGER PULSE GENERATOR					
Synchronization Level Currents					µA
Voltage Line Sensing	$I_{Pin\ 2}$	—	± 50	± 100	
Triac Sensing	$I_{Pin\ 1}$	—	± 50	± 100	
Trigger Pulse Duration ($C_{Pin\ 14}$ = 47 nF, $R_{Pin\ 15}$ = 270 kΩ)	T_p	—	55	—	µs
Trigger Pulse Repetition Period, conditions as a.m.	T_R	—	220	—	µs
Output Pulse Current $V_{Pin\ 13} = V_{CC}$ – 4.0 V	– $I_{Pin\ 13}$	180	192	—	mA
Output Leakage Current $V_{Pin\ 13}$ = – 3.0 V	$I_{13\ L}$	—	—	30	µA
Full Angle Conduction Input Voltage	V_{14}	—	11.7	—	V
Saw Tooth “High” Level Voltage	$V_{14\ H}$	12	—	12.7	V
Saw Tooth Discharge Current, I_{Pin15} = 100 µA	$I_{Pin\ 14}$	95	—	105	µA

GENERAL DESCRIPTION

The TDA 1085C triggers a triac accordingly to the speed regulation requirements. Motor speed is digitally sensed by a tachogenerator and then converted into an analog voltage.

The speed set is externally fixed and is applied to the internal linear regulation input after having been submitted to programmable acceleration ramps. The overall result consists in a full motor speed range with two acceleration ramps which allow efficient washing machine control (Distribute function).

Additionally, the TDA 1085C protects the whole system against AC line stop or variations, overcurrent in the motor and tachogenerator failure.

INPUT/OUTPUT FUNCTIONS
(Refer to Figures 1 and 8)

Voltage Regulator – (Pins 9 and 10) This is a parallel type regulator able to sink a large amount of current and offering good characteristics. Current flow is provided from AC line by external dropping resistors R1, R2, and rectifier: This half wave current is used to feed a smoothering capacitor, the voltage of which is checked by the IC.

When V_{CC} is reached, the excess of current is derived by another dropping resistor R10 and by Pin 10. These three resistors must be determined in order:

- To let 1.0 mA flow through Pin 10 when AC line is minimum and V_{CC} consumption is maximum (fast ramps and pulses present).
- To let V_{10} reach 3.0 V when AC line provides maximum current and V_{CC} consumption is minimum (no ramps and no pulses).
- All along the main line cycle, the Pin 10 dynamic range must not be exceeded unless loss of regulation.

An AC line supply failure would cause shut down.

The double capacitive filter built with R1 and R2 gives an efficient V_{CC} smoothing and helps to remove noise from set speeds.

Speed Sensing – (Pins 4, 11, 12) The IC is compatible with an external analog speed sensing: its output must be applied to Pin 4, and Pin 12 connected to Pin 8.

In most of the applications it is more convenient to use a digital speed sensing with an unexpensive tachogenerator which doesn′t need any tuning. During every positive cycle at Pin 12, the capacitor $C_{Pin\ 11}$ is charged to almost V_{CC} and during this time, Pin 4 delivers a current which is 10 times the one charging $C_{Pin\ 11}$. The current source gain is called G and is tightly specified, but nevertheless requires an adjustment on $R_{Pin\ 4}$. The current into this resistor is proportional to $C_{Pin\ 11}$ and to the motor speed; being filtered by a capacitor, $V_{Pin\ 4}$ becomes smothered and represents the “true actual motor speed”.

To maintain linearity into the high speed range, it is important to verify that $C_{Pin\ 11}$ is fully charged: the internal source on Pin 11 has 100 KΩ impedance. Nevertheless $C_{Pin\ 11}$ has to be as high as possible as it has a large influence on FV/C temperature factor. A 470 KΩ resistor between Pins 11 and 9 reduces leakage currents and temperature factor as well, down to neglectable effects.

Pin 12 also has a monitoring function: when its voltage is above 5.0 V, the trigger pulses are inhibited and the IC is reset. It also senses the tachogenerator continuity, and in case of any circuit aperture, it inhibits pulse, avoiding the motor to run out of control. In the TDA 1085C, Pin 12 is negatively clamped by an internal diode which removes the necessity of the external one used in the former circuit.

Ramp Generator – (Pins 5, 6, 7) The true Set Speed value taken in consideration by the regulation is the output of the ramp generator (Pin 7). With a given value of speed set input (Pin 5), the ramp generator charges an external capacitor $C_{Pin\ 7}$ up to the moment $V_{Pin\ 5}$ (set speed) equals $V_{Pin\ 4}$ (true speed), see Figure 2. The IC has an internal charging current source of 1.2mA and delivers it from 0 to 12 V at Pin 7. It is the high acceleration ramp (5.0 s typical) which allows rapid motor speed changes without excessive strains on the mechanics. In addition, the TDA 1085C offers the possibility to break this high acceleration with the introduction of a low acceleration ramp (called Distribution) by reducing the Pin 7 source current down to 5.0 µA under Pin 6 full control, as shown by following conditions:

- Presence of high acceleration ramp $V_{Pin\ 5} > V_{Pin\ 4}$
- Distribution occurs in the $V_{Pin\ 4}$ range (true motor speed) defined by $V_{Pin\ 6} \leqq V_{Pin\ 4} \leqq 2.0\ V_{Pin\ 6}$

For two fixed values of $V_{Pin\ 5}$ and $V_{Pin\ 6}$, the motor speed will have high acceleration, excluding the time for $V_{Pin\ 4}$ to go from $V_{Pin\ 6}$ to two times this value, high acceleration again, up to the moment the motor has reached the set speed value, at which it will stay, see Figure 3.

Should a reset happen (whatever the cause would be), the above mentioned successive ramps will be fully reprocessed from 0 to the maximum speed. If $V_{Pin\ 6} = 0$, only the high acceleration ramp occurs.

To get a real zero speed position, Pin 5 has been designed in such a way that its voltage from 0 to 80 mV is interpreted as a true zero. As a consequence, when changing the speed set position, the designer must be sure that any transient zero would not occur: if any, the entire circuit will be reset.

As the voltages applied by Pins 5 and 6 are derived from the internal voltage regulator supply and Pin 4 voltage is also derived from the same source, motor speed (which is determined by the ratios between above mentioned voltages) is totally independent from V_{CC} variations and temperature factor.

Control Amplifier – (Pin 16) It amplifies the difference between true speed (Pin 4) and set speed (Pin 5), through the ramp generator. Its output available at Pin 16 is a double sense current source with a maximum capability of ± 100 µA and a specified transconductance (340 µA/V typical). Pin 16 drives directly the trigger pulse generator, and must be loaded by an electrical network which compensates the mechanical characteristics of the motor and its load, in order to provide stability in any condition and shortest transient response; see Figure 4.

This network must be adjusted experimentally.

In case of a periodic torque variations, Pin 16 directly provides the phase angle oscillations.

Trigger Pulse Generator – **(Pins 1, 2, 5, 13, 14, 15)**
This circuit performs four functions:

- The conversion of the control amplifier DC output level to a proportional firing angle at every main line half cycle.
- The calibration of pulse duration.
- The repetition of the pulse if the triac fails to latch on if the current has been interrupted by brush bounce.
- The delay of firing pulse until the current crosses zero at wide firing angles and inductive loads.

$R_{Pin\ 15}$ programs the Pin 14 discharging current. Saw tooth signal is then fully determined by R15 and C14 (usually 47 nF). Firing pulse duration and repetition period are in inverse ratio to the saw tooth slope. Pin 13 is the pulse output and an external limiting resistor is mandatory. Maximum current capability is 200 mA.

Current Limiter – (Pin 3) Safe operation of the motor and triac under all conditions is ensured by limiting the peak current. The motor current develops an alternative voltage in the shunt resistor (0.05 Ω in Figure 4). The negative half waves are transferred to Pin 3 which is positively preset at a voltage determined by resistors R3 and R4. As motor current increases, the dynamical voltage range of Pin 3 increases and when Pin 3 becomes slightly negative in respect to Pin 8, a current starts to circulate in it. This current, amplified typically 180 times, is then used to discharge Pin 7 capacitor and, as a result, reduces firing angle down to a value where an equilibrium is reached. The choice of resistors R3, R4 and shunt determines the magnitude of the discharge current signals on $C_{Pin\ 7}$.

Notice that the current limiter acts only on peak triac current.

APPLICATION NOTES
(Refer to Figure 4)

Printed Circuit Layout Rules
In the common applications, where TDA 1085C is used, there is on the same board, presence of high voltage, high currents as well as low voltage signals where millivolts count. It is of first magnitude importance to separate them from each other and to respect the following rules:

- Capacitor decoupling pins, which are the inputs of the same comparator, must be physically close to the IC, close to each other and grounded in the same point.
- Ground connection for tachogenerator must be directly connected to Pin 8 and should ground only the tacho. In effect, the latter is a first magnitude noise generator due to its proximity to the motor which induces high dϕ/dt signals.
- The ground pattern must be in the “star style” in order to fully eliminate power currents flowing in the ground network devoted to capacitors decoupling sensitive Pins: 4, 5, 7, 11, 12, 14, 16.

As an example, Figure 5 presents a PC board pattern which concerns the group of sensitive Pins and their associated capacitors into which the a.m. rules have been implemented. Notice the full separation of “Signal World” from “Power”, one by line AB and their communication by a unique strip.

These rules will lead to much satisfactory volume production in the sense that speed adjustment will stay valid in the entire speed range.

Power Supply
As dropping resistor dissipates noticeable power, it is necessary to reduce the I_{CC} needs down to a minimum. Triggering pulses, if a certain number of repetitions are kept in reserve to cope with motor brush wearing at the end of its life, are the largest I_{CC} user. Classical worst case configuration has to be considered to select dropping resistor. In addition, the parallel regulator must be always into its dynamic range, i.e., $I_{Pin\ 10}$ over 1.0 mA and $V_{Pin\ 10}$ over 3.0 V in any extreme configuration. The double filtering cell is mandatory.

Tachogenerator Circuit
The tacho signal voltage is proportional to the motor speed. Stablility considerations, in addition, require an RC filter, the pole of which must be looked at. The combination of both elements yield a constant amplitude signal on Pin 12 in most of the speed range. It is recommended to verify this maximum amplitude to be within 1.0 V peak in order to have the largest signal/noise ratio without resetting the integrated circuit (which occurs if $V_{Pin\ 12}$ reaches 5.5 V). It must be also verified that the Pin 12 signal is approximately balanced between “high” (over 300 mV) and “low”. An 8–poles tacho is a minimum for low speed stability and a 16–poles is even better.

The RC pole of the tacho circuit should be chosen within 30 Hz in order to be as far as possible from the 150 Hz which corresponds to the AC line 3rd harmonic generated by the motor during starting procedure. In addition, a high value resistor coming from V_{CC} introduces a positive offset at Pin 12, removes noise to be interpreted as a tacho signal. This offset should be designed in order to let Pin 12 reach at least – 200 mV (negative voltage) at the lowest motor speed. We remember the necessity of an individual tacho ground connection.

Frequency to Voltage Converter – F V/C
$C_{Pin\ 11}$ has a recommended value of 820 pF for 8–poles tachos and maximum motor rpm of 15000, and $R_{Pin\ 11}$ must be always 470 K.

$R_{Pin\ 4}$ should be choosen to deliver within 12 V at maximum motor speed in order to maximize signal/noise ratio. As the FV/C ratio as well as the $C_{Pin\ 11}$ value are dispersed, $R_{Pin\ 4}$ must be adjustable and should be made of a fixed resistor in serice with a trimmer representing 25% of the total. Adjustment would become easier.

Once adjusted, for instance at maximum motor speed, the FV/C presents a residual non linearity; the conversion factor (mV per RPM) increases by within 7.7% as speed draws to zero. The guaranteed dispersion of the latter being very narrow, a maximum 1% speed error is guaranteed if during Pin 5 network design the small set values are modified, once forever, according this increase.

The following formulas give $V_{Pin\ 4}$:

$$V_{Pin\ 4} = G.0 \cdot (V_{CC} – V_a) \cdot C_{Pin\ 11} \cdot R_4 \cdot f \cdot \frac{1}{\left(1 + \frac{120k}{R_{Pin11}}\right)} \text{ In volts.}$$

$G.0 \cdot (V_{CC} – V_a) \simeq 140$
$V_a = 2.0\ V_{BE}$
$120\ k = R_{int}$, on Pin 11

Speed Set – (Pin 5) Upon designer choice, a set of external resistors apply a series of various voltages corresponding to the various motor speeds. When switching external resistors, verify that no voltage below 80 mV is ever applied to Pin 5. If so, a full circuit reset will occur.

Ramps Generator – (Pin 6) If only a high acceleration ramp is needed, connect Pin 6 to ground.

When a Distribute ramp should occur, preset a voltage on Pin 6 which corresponds to the motor speed starting ramp point. Distribution (or low ramp) will continue up to the moment the motor speed would have reached twice the starting value.

The ratio of two is imposed by the IC. Nevertheless, it could be externally changed downwards (Figure 6) or upwards (Figure 7).

The distribution ramp can be shortened by an external resistor from V_{CC} charging $C_{Pin\ 7}$, adding its current to the internal 5.0 µA generator.

Power Circuits
Triac Triggering pulse amplitude must be determined by Pin 13 resistor according to the needs in Quadrant IV. Trigger pulse duration can be disturbed by noise signals generated by the triac itself, which interfere within Pins 14 and 16, precisely those which determine it. While easily visible, this effect is harmless.

The triac must be protected from high AC line dV/dt during external disturbances by 100 nF x 100 Ω network.

Shunt resistor must be as non–inductive as possible. It can be made locally by using constantan alloy wire.

When the load is a DC fed universal motor through a rectifier bridge, the triac must be protected from commutating dV/dt by a 1.0 to 2.0 mH coil in series with MT_2.

Synchronization functions are performed by resistors sensing AC line and triac conduction. 820 k values are normal but could be reduced down to 330 k in order to detect the “zeros” with accuracy and to reduce the residual DC line component below 20 mA.

Current Limitation
The current limiter starts to discharge Pin 7 capacitor (reference speed) as the motor current reaches the designed threshold level. The loop gain is determined by the resistor connecting Pin 3 to the series shunt. Experience has shown that its optimal value for a 10 Arms limitation is within 2.0 kΩ. Pin 3 input has a sensitivity in current which is limited to reasonable values and should not react to spikes.

If not used, Pin 3 must be connected to a maximum positive voltage of 5.0 V rather than be left open.

Loop Stability
The Pin 16 network is predominant and must be adjusted experimentally during module development. The values indicated in Figure 4 are typical for washing machine applications but accept large modifications from one model to another. R16 (the sole restriction) should not go below 33 k, otherwise slew rate limitation will cause large transient errors for load steps.

Figure 2. Acceleration Ramp

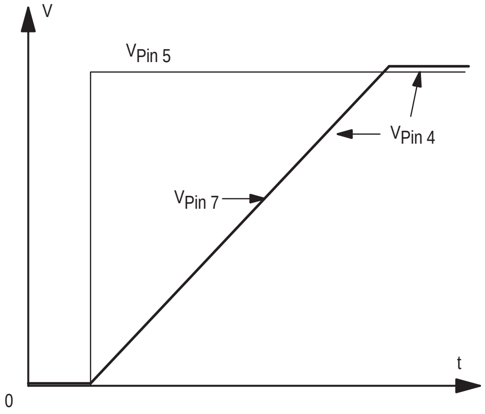


Figure 3. Programmable Double Acceleration Ramp

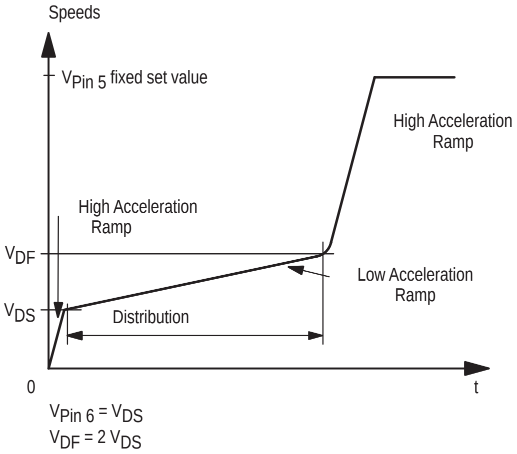
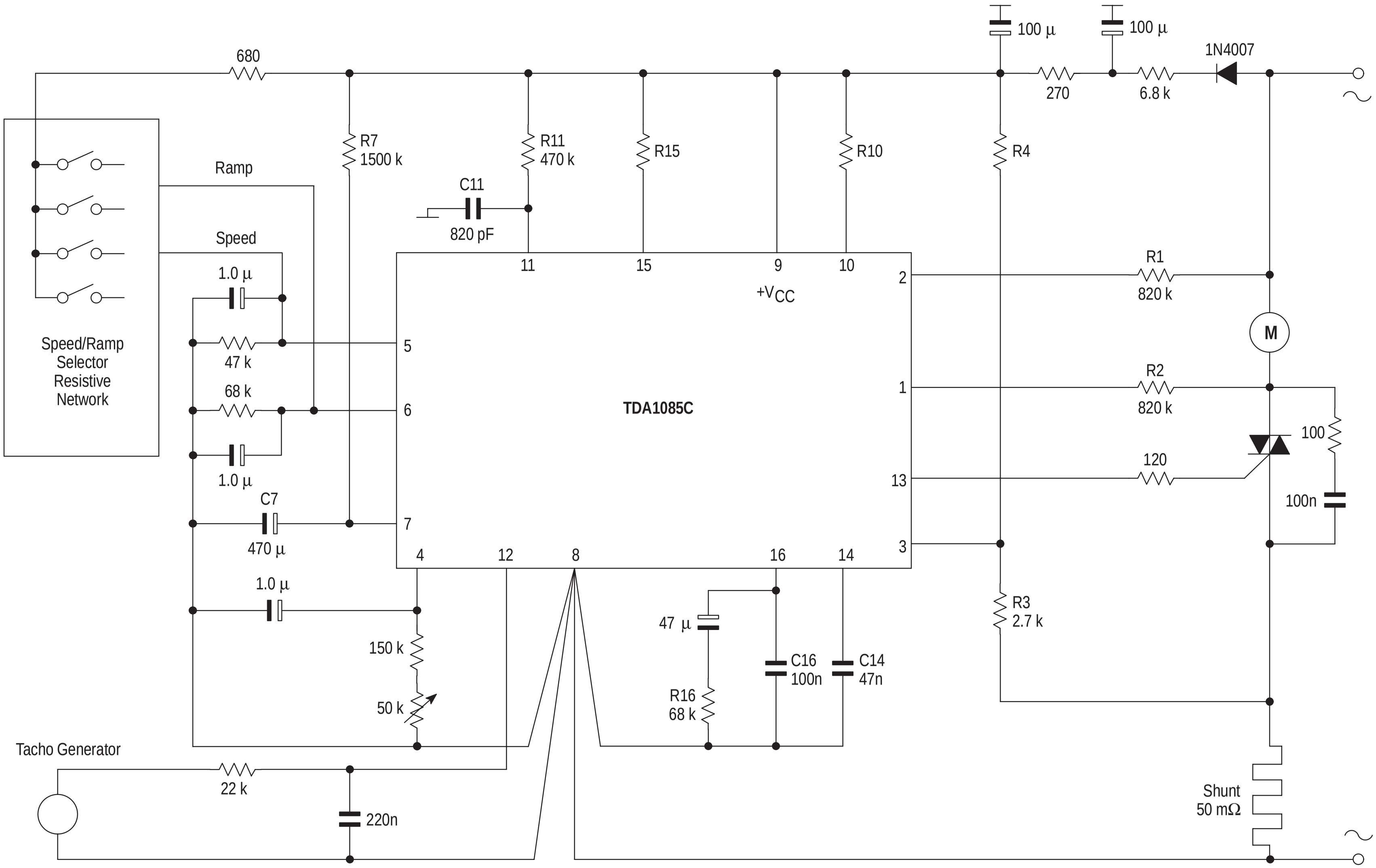


Figure 4. Basic Application Circuit



Current limitation: 10 A adjusted by R4 experimentally

Ramps High acceleration: 3200 rpm per second

Distribution ramp: 10 s from 850 to 1300 rpm

Speeds:	**Pin 5 Voltage Set:**	
Wash 800 rpm	609 mV	Including nonlinearity corrections
Distribution 1300	996 mV	Including nonlinearity corrections
Spin 1: 7500	5,912 V	Including nonlinearity corrections
Spin 2: 15,000	12,000 V	Adjustment point

Motor Speed Range: 0 to 15,000 rpm

Tachogenerator 8 poles delivering 30 V peak to peak at 6000 rpm, in open circuit

FV/C Factor: 8 mV per rpm (12 V full speed) $C_{Pin\ 11} = 680$ pF $V_{CC} = 15.3$ V

Triac MAX15A–8 15 A 600 V

Igt min = 90 mA to cover Quad IV at –10°C

Figure 5. PC Board Layout

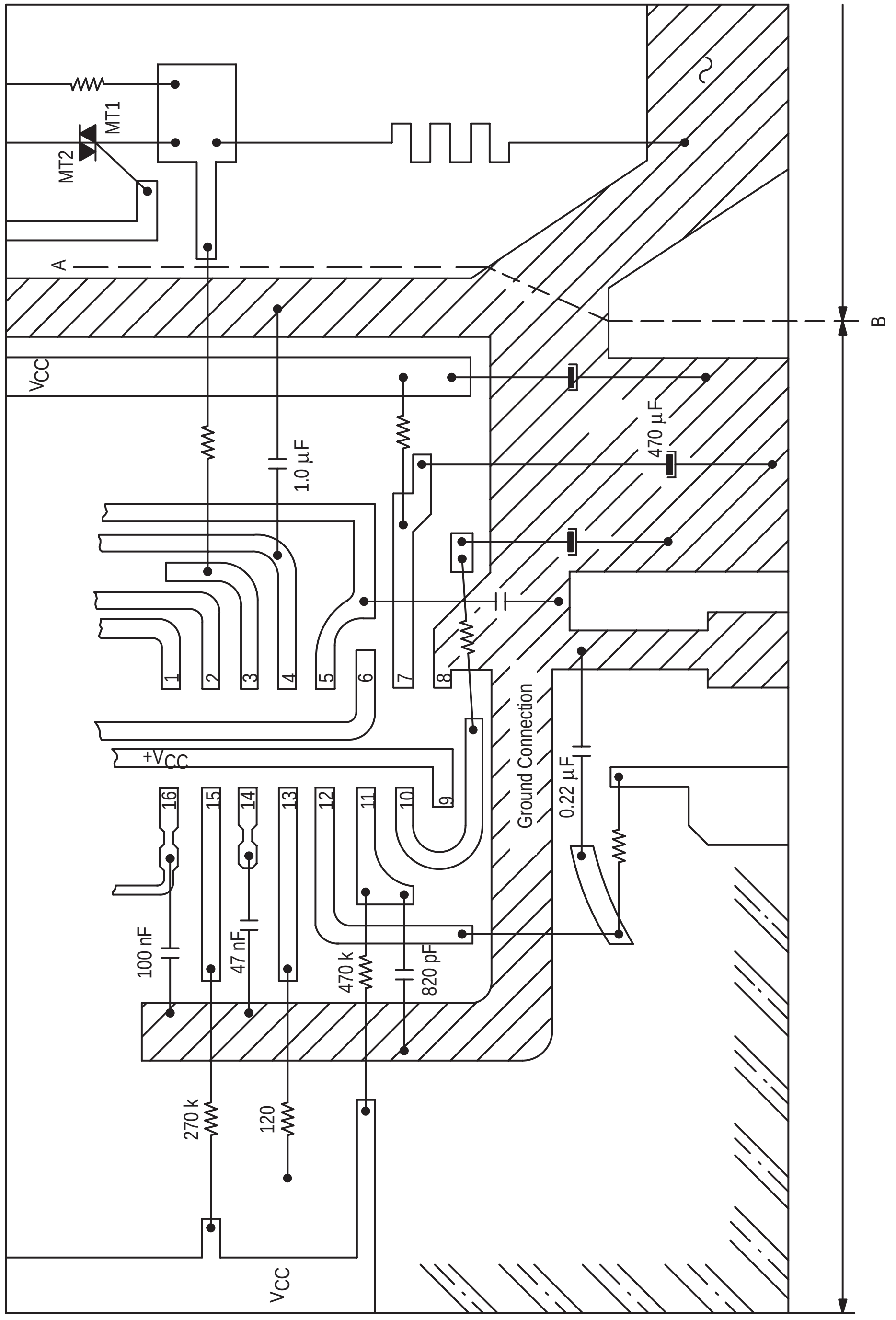


Figure 6. Distribution Speed k < 2

For k = 1.6, $R_3 = 0.6\ (R1 + R2)$,
R_3 C within 4 seconds

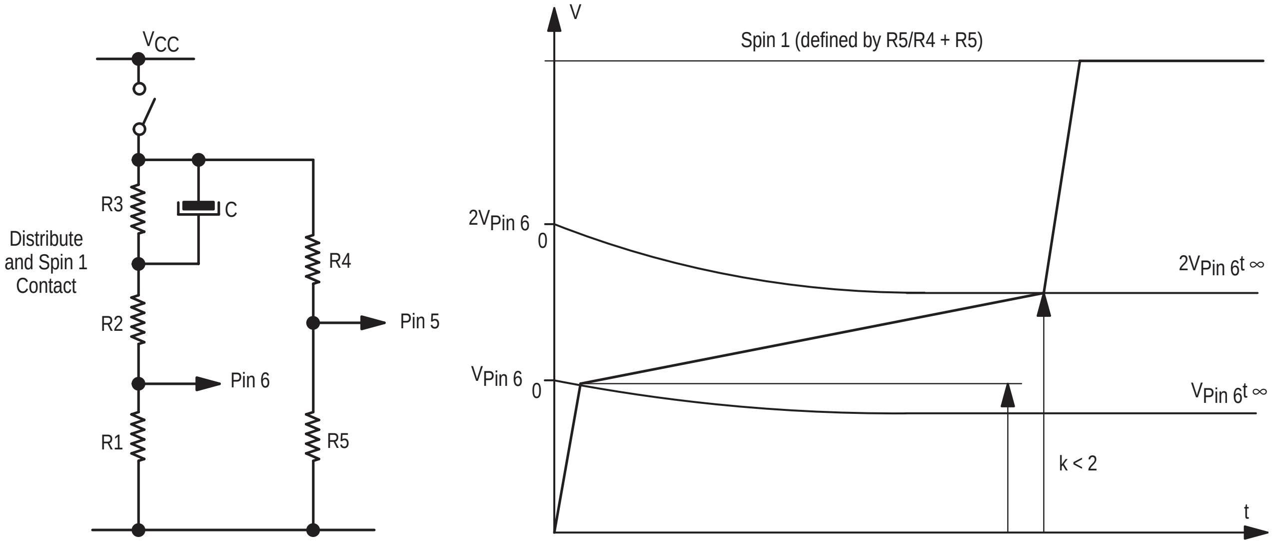


Figure 7. Distribution Speed k > 2

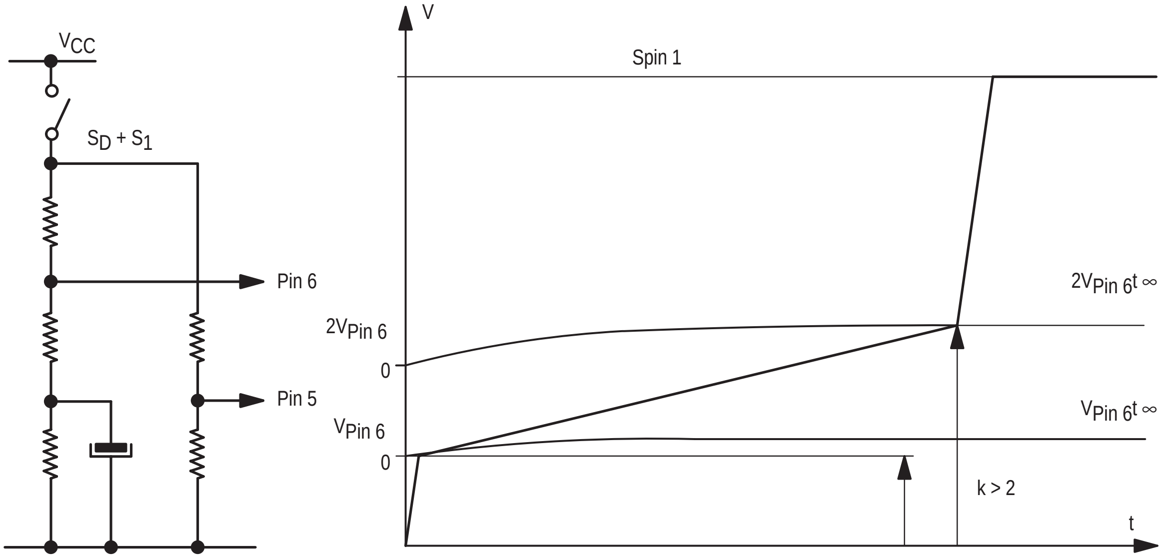
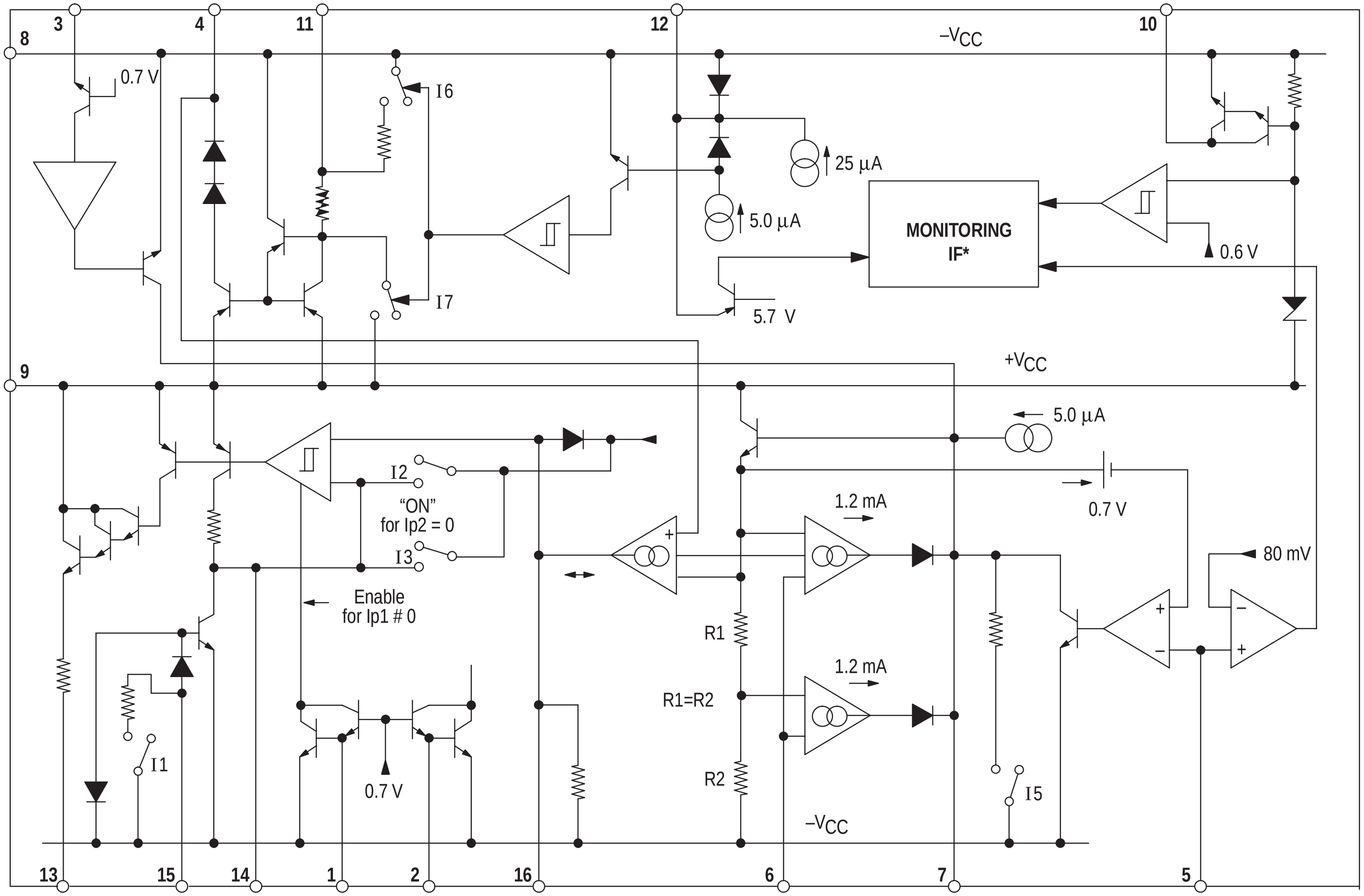


Figure 8. Simplified Schematic



*(P12 connected) and (V_{CC}OK) and (VP5>80 mV)
Then
(I1 OFF),(I2 OFF), (I4 OFF) and (I5 OFF)

MOTOROLA

TDA1185A

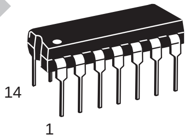
Triac Phase Angle Controller

TRIAC PHASE ANGLE CONTROLLER

SEMICONDUCTOR TECHNICAL DATA

The TDA1185A generates controlled triac triggering pulses and allows tachless speed stabilization of universal motors by an integrated positive feedback function. Typical applications are power hand tools, vacuum cleaners, mixers, light dimmer and other small appliances.

- Supply Power Obtained from AC Line
- Can be used with 220 V/50 Hz or 110 V/60 Hz
- Low Count/Cost External Components
- Optimum Triac Firing (2nd and 3rd Quadrants)
- Repetitive Trigger Pulses when Triac Current is Interrupted by Motor Brush Bounce
- Triac Current Sensing to Allow Inductive Loads
- Programmable Soft–Start
- Power Failure Detection and General Circuit Reset
- Low Power Consumption: 6.0 mA



PLASTIC PACKAGE
CASE 646

PIN CONNECTIONS

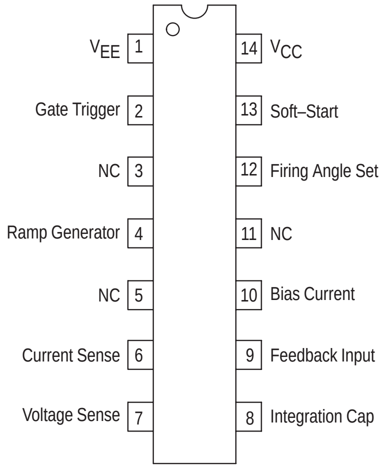
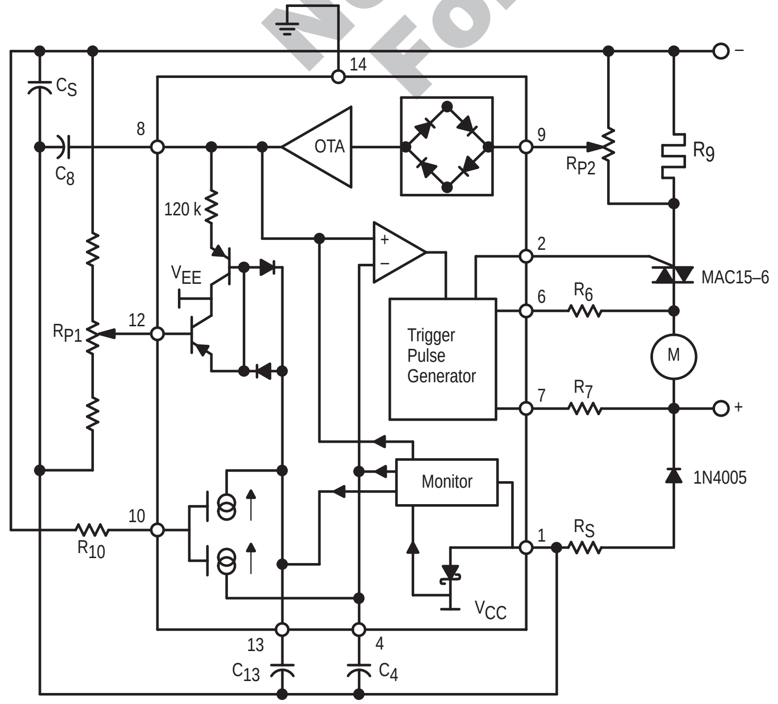


Figure 1. Representative Block Diagram



ORDERING INFORMATION

Device	Operating Temperature Range	Package
TDA1185A	T_A = 0° to +70°C	Plastic DIP

MAXIMUM RATINGS (Voltages are referenced to Pin 14, ground)

Rating	Symbol	Value	Unit
Maximum Voltage Range per Listed Pin	V_{Pin}		V
Pins 3, 5, 11 (not connected)		– 20 to + 20	
Pins 4, 8, 13		– V_{CC} to 0	
Pin 2		– 3.0 to + 3.0	
Maximum Positive Voltage (No minimum value	$V_{Pin\ 12}$	0	
allowed; see current ratings)	$V_{Pin\ 1}$	0.5	
Maximum Current per Listed Pin	I_{Pin}		
Pin 1		± 20	mA
Pins 6 and 7		± 2.0	mA
Pin 9		± 0.5	mA
Pin 10		± 300	µA
Pin 12		– 500	µA
Maximum Power Dissipation (@ T_A = 25°C)	P_D	250	mW
Maximum Thermal Resistance, Junction–to–Ambient	$R_{\theta JA}$	100	°C/W
Operating Ambient Temperature Range	T_A	0 to + 70	°C
Storage Temperature Range	T_{stg}	– 55 to + 125	°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C, voltages are referenced to Pin 14 [ground] unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Power Supply					
Zener Regulated Voltage, ($V_{Pin\ 1}$) $I_{Pin\ 1}$ = 2.0 mA	– V_{CC}	– 9.6	– 8.6	– 7.6	V
Circuit Current Consumption, $I_{Pin\ 1}$ $V_{Pin\ 1}$ = – 6.0 V, $I_{Pin\ 2}$ = 0 A	– I_{CC}	– 2.0	– 1.0	—	mA
Monitoring Enable Supply Voltage (V_{EN})	$V_{Pin\ 1EN}$	V_{CC} + 0.2	—	V_{CC} + 0.5	V
Monitoring Disable Supply Voltage (V_{DIS})	$V_{Pin\ 1DIS}$	V_{EN} + 0.12	—	V_{EN} + 0.3	
Phase Set					
Control Voltage Static Offset $V_{Pin\ 8}$ – $V_{Pin\ 12}$	V_{off}	1.2	—	2.0	V
Pin 12 Input Bias Current	$I_{Pin\ 12}$	– 200	—	0	nA
$V_{Pin\ 4}$ – $V_{Pin\ 12}$ Residual Offset		—	180	—	mV
Soft–Start Capacitor Charging Current $R_{Pin\ 10}$ = 100 kΩ, $V_{Pin\ 13}$ from – V_{CC} to – 3.0 V	$I_{Pin\ 13}$	– 17	– 14	– 11	µA
Sawtooth Generator					
Sawtooth Capacitor Discharge Current R_{10} = 100 kΩ $V_{Pin\ 4}$ from – 2.0 to – 6.0 V	$I_{Pin\ 4}$	67	70	73	µA
Capacitor Charging Current	$I_{Pin\ 4}$	– 10	—	– 1.5	mA
Sawtooth “High” Voltage ($V_{Pin\ 4}$)	V_{HTH}	– 2.5	– 1.6	– 1.0	V
Sawtooth Minimum “Low” Voltage ($V_{Pin\ 4}$)	V_{LTH}	—	– 7.1	—	V
Positive Feedback					
Pin 9 Input Bias Current, $V_{Pin\ 9}$ = 0	$I_{Pin\ 9}$	—	2 x $I_{Pin\ 10}$	—	
Programming Pin Voltage Related to Pin 1	$V_{Pin\ 10}$	1.0	1.25	1.5	V
Transfer Function Gain $\Delta V_{Pin\ 8}/\Delta V_{Pin\ 9}$					
R_{10} = 100 kΩ , $\Delta V_{Pin\ 9}$ = 50 mV	A	—	75	—	
R_{10} = 270 kΩ , $\Delta V_{Pin\ 9}$ = 50 mV	A	—	36	—	
Pin 8 Output Internal Impedance	$Z_{Pin\ 8}$	—	120	—	kΩ
Trigger Pulse Generator					
Output Current (Sink) $V_{Pin\ 2}$ = 0 V	$I_{Pin\ 2}$	60	—	80	mA
Output Leakage Current $V_{Pin\ 2}$ = + 2.0 V		—	—	4.0	µA
Output Pulse Width	t_P				
C_4 = 47 nF R_{10} = 270 kΩ		—	55	—	µs
Output Pulse Repetition Period	t				
C_4 = 47 nF R_{10} = 270 kΩ		—	420	—	µs
Current Synchronization Threshold Levels $I_{Pin\ 6}$, $I_{Pin\ 7}$	I_{sync}	– 40	—	+ 40	µA

PIN FUNCTION DESCRIPTION

Pin No.	Function	Description
1	V_{EE}	This pin is the negative supply for the chip and is clamped at – 8.6 V by an internal zener.
2	Gate Trigger Pulse	This pin supplies – 1.0 V triac trigger pulse at twice the line frequency.
3	NC	Not connected.
4	Ramp Generator	The value of the capacitor at this pin determines the slope of the ramp.
5	NC	Not connected.
6	Current Sense	This pin senses if the triac is on, and if so, will disable the gate trigger pulse.
7	Voltage Sense	The internal timing of the chip is set by the frequency of the voltage at this pin.
8	Integration Capacitor	This pin is the output of the feedback and the variation in voltage is averaged out by the capacitor.
9	Feedback Input	The change in load current is detected by the change in voltage across R9.
10	Current Program	The bias current for the circuit is determined by the resistor value at this pin.
11	NC	Not connected.
12	Phase Angle Set	The voltage at this pin sets the no–load firing angle.
13	Soft–Start	The firing angle is slowly increased from 180° to the set value of Pin 12.
14	V_{CC}	Ground

Introduction

The Motorola TDA1185A generates trigger pulses (Pin 2) for triac control of power into an AC load. The triac trigger pulse is determined by generating a ramp voltage (Pin 4) synchronized to twice the AC line frequency and compared to an external set voltage (Pin 12) representing the conduction angle. Gate pulses are negative (sink current) and thus the triac is driven into its most effective quadrants (Q2 to Q3).

If the load is a Universal motor (the speed of which decreases as torque increases), the TDA1185A allows to increase the conduction angle proportionally to the motor current, sensed (Pin 9) by a low value resistor in series with the load.

FUNCTIONAL DESCRIPTION

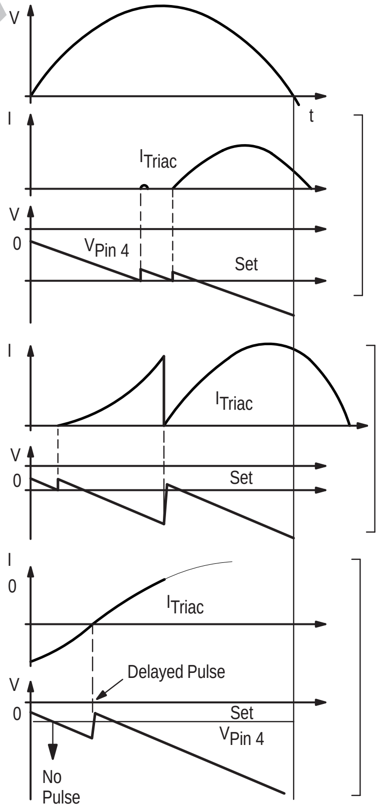
DC Power Supply

DC power is directly derived from the AC line through a 2.0 W resistor, half–wave rectifier and filtering capacitor circuit. The V_{EE} voltage is internally regulated by an integrated zener. Referenced to ground (Pin 14), the power supply voltage is – 8.6 V. The TDA1185A internal consumption is 6.0 mA.

Trigger Pulse Generator

It delivers a 60 mA minimum sink current pulse (Pin 2) through an internally short circuit protected output. Pulse width is roughly proportional to R_{10} x C_4 and is repeated every 420 µs if triac fails to latch or is switched off by brush bounce. With inductive loads, the current lags in respect to the voltage. Pin 6 delays the triggering pulse up to the moment the triac is off, in order to prevent erratic power control (see Figure 2).

Figure 2. Multipulse Generation Delayed Pulse



The triac failed to latch at the first pulse. Successive pulses are generated up to the moment latching occurs.

The triac turned off due to brush bounce, a new pulse is immediately delivered.

Approaching full conduc–tion, a pulse would occur when the triac still carries current; the pulse is delaye until the triac turns off.

Ramp Generator

A constant current sink discharges capacitor C_4 producing a negative voltage ramp synchronized with the main line. Pin 4 voltage is reset to – 1.6 V at every AC line zero crossing (see Figure 3) and ramps down to – 7.1 V. The constant current sink is externally programmable by R_{10} using the equation below.

$$I_4 = I_{10} \pm 5\%$$

$$I_{10} = \frac{|V_{EE} + 1.25|}{R_{10}}$$

Main Comparator

Its role is to determine the trigger pulse which occurs when the ramp voltage equals the phase angle set voltage at Pin 12. Fixed phase angle set voltage values lead to a constant TRIAC conduction angle unless positive current feedback (Pin 9) is connected or the Soft–Start capacitor (Pin 13) is not charged.

Soft–Start

The TDA1185A allows the user to avoid any abrupt inrush of current into the load. This provides protection for fragile loads, light bulbs or tubes. Another advantage is that the AC line disturbance is minimized.

The conduction angle is established from zero to the set value at Pin 12 according to a voltage ramp generated by a constant current delivered to C_{13}. The value of current I_{13} can be expressed by the following equation:

$$I_{13} = 0.2 \times I_{10} \pm 10\%$$

The voltage ramp lasts as long as V_{13} is lower than the set voltage V_{12}. Upon reset, V_{13} is forced to V_{EE} as shown in Figure 4. If the load is a universal motor, it will not turn until a minimum conduction angle is achieved to overcome friction. The time the voltage ramp requires to reach its threshold value is considered deadtime, and can be eliminated by an appropriate series resistor at Pin 13. The voltage drop developed by I_{13} thru the resistor causes the conduction angle to immediately reach the threshold value and have the Soft–Start function without dead time (see Figure 5).

Figure 3. Triggering Pulse Timing

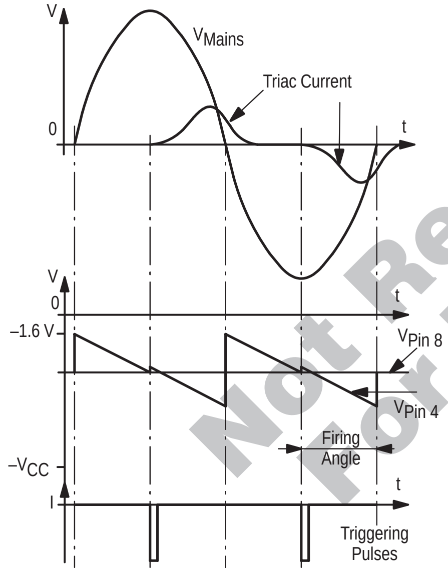


Figure 4. Soft–Start

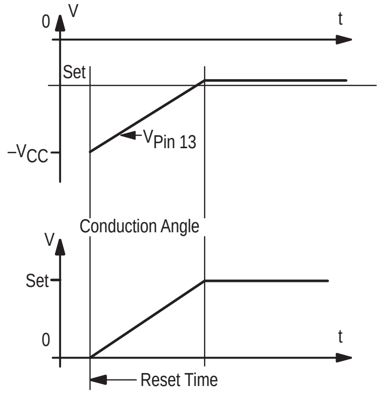


Figure 5. Soft–Start without Deadtime

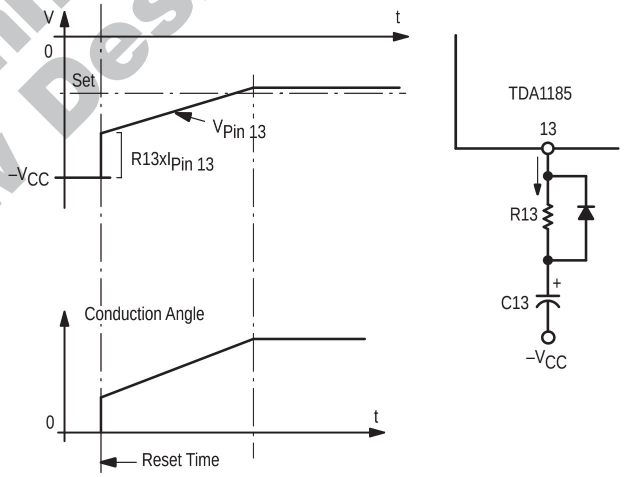
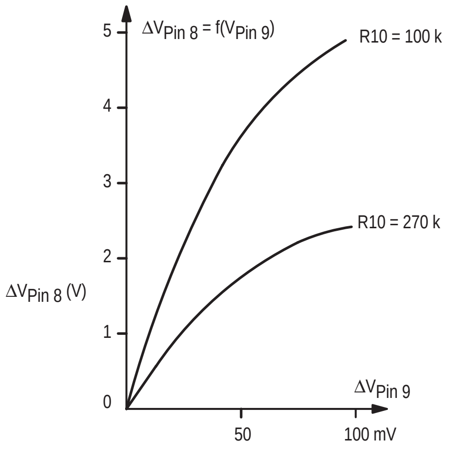


Figure 6. Transfer Function



Positive Current Feedback

The Universal motor speed drops as load increases. To maintain the speed, the triac conduction angle must be increased. For this purpose, Pin 9 senses the motor current as a **voltage** developed in a low value resistor, R_9, amplifies, rectifies and adds it internally to the set voltage at Pin 12. Any voltage variation at the output of the feedback, Pin 8, is smoothed out by capacitor C_8. The transfer function, $\Delta V_8 = f(\Delta V_9)$, is shown in Figure 6.

The gain in the linear region is dependent on R_{10}. The voltage transferred to Pin 8 is proportional to the current RMS value, as motor current is not far from a sine wave. This averaging effect is shown in Figure 7.

With large amplitude signals at Pin 9, the change in voltage at Pin 8 reaches a maximum value. This saturation effect limits the maximum conduction angle increase. This effect is illustrated in Figure 8 where the total Pin 8 voltage can be written as follows:

$$V_8 = V_{12} + f(|V_9|, R_{10}) + 1.25$$

The effect of the feedback is illustrated in Figure 9.

Monitoring

A central logic block performs the ENABLE/DISABLE function of the IC with respect to power supply voltage. Under DISABLE conditions, Pin 4, 8, 12 and 13 are forced to appropriate voltages to prepare for the next reset. Refer to the block diagram in Figure 10.

APPLICATION CONSIDERATIONS

Component Selection

To regulate the speed of a universal motor, it is necessary to determine how much gain in the feedback is needed. A change in motor current (due to load increase) causes the conduction angle to change by the appropriate amount to keep the speed constant. This entails, through trial and error, choosing an appropriate resistor value for R_{10}, since the gain of the feedback is determined by value of R_{10} as shown in Figure 8.

Figure 7. Averaging Effect of Transfer Function

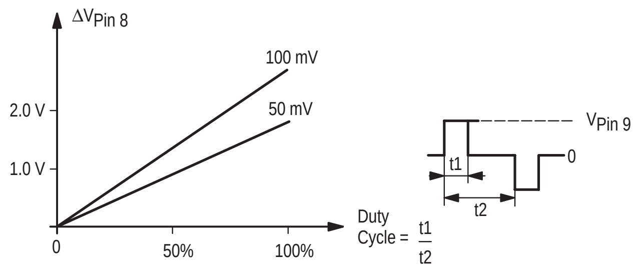
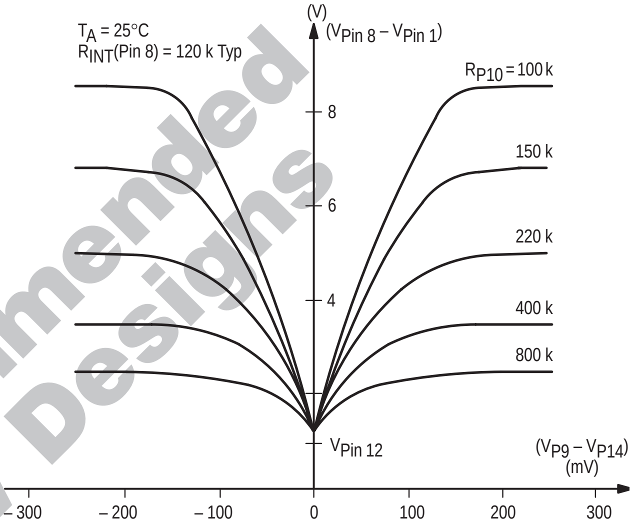


Figure 8. Transfer Function (Pin 8/Pin 9)



Once R_{10} is picked, C_4 can be calculated from the following equation:

$$C_4 \approx \frac{.672}{f_{line} \times R_{10}}$$

where f_{line} is the line frequency.

Figure 9. Positive Feedback Effect (Offset voltages have been neglected)

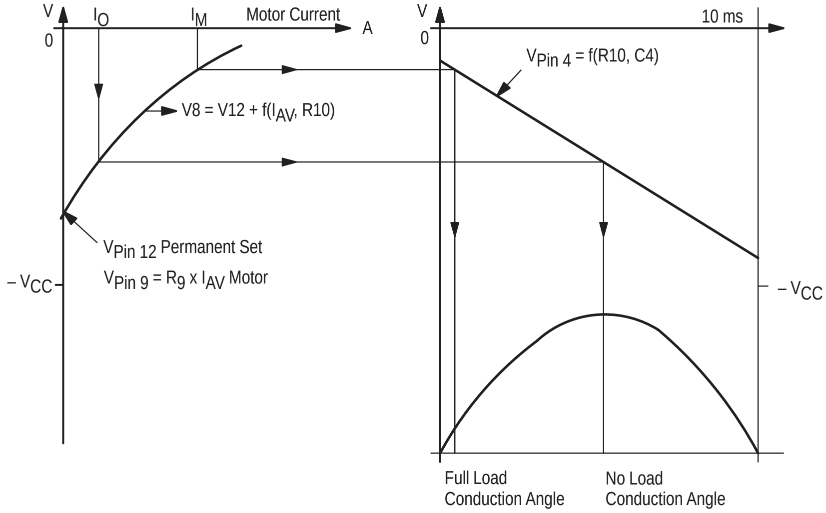
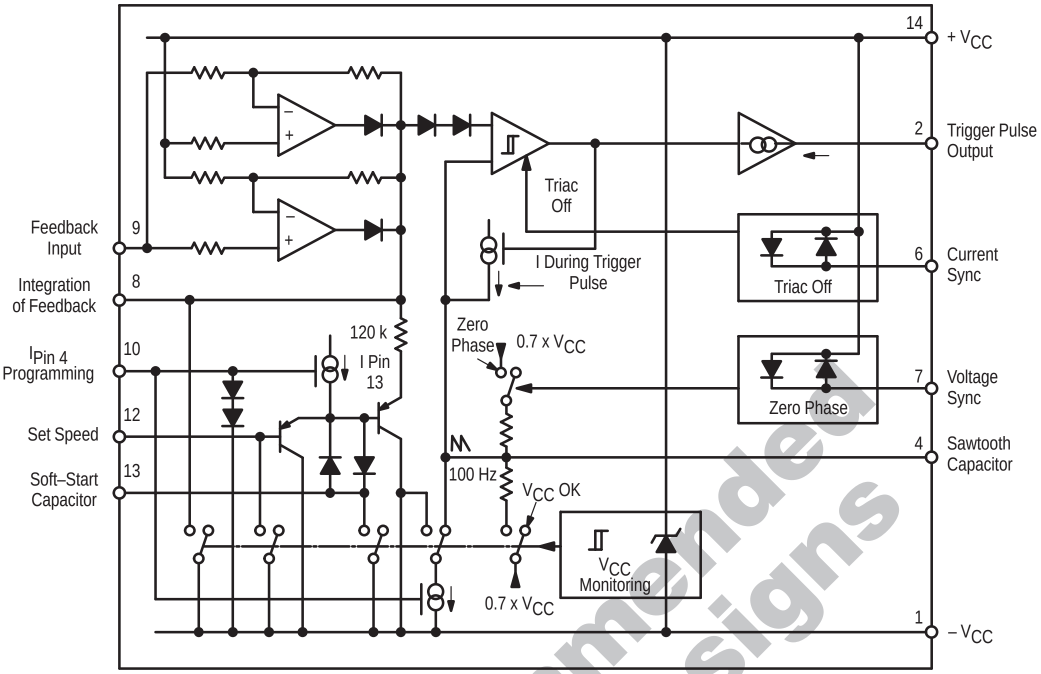


Figure 10. Internal Block Diagram



Capacitor C_8 is an integration cap used to smooth out the voltage at Pin 8. The value should be large enough to accomplish this task yet not too large to slow the response of the system.

Capacitor C_{13} determines how fast the conduction angle reaches the set value programmed at Pin 12. To achieve a desired delay, the value for C_{13} can be calculated by the following equation:

$$C_{13} \approx \frac{8 \times t_d}{|8.6 - V_{12}| \times R_{10}}$$

The remaining component values have experimentally been determined and are constant, regardless of application. The following table lists typical values for 110 V application.

Component	Value	Units
R_S	10/2.0 W	kΩ
R_{P1}	100	kΩ
R_{P2}	100	Ω
R_6	330/0.5 W	kΩ
R_7	330/0.5 W	kΩ
R_9	0.05/5.0 W	Ω
R_{10}	100	kΩ
C_4	0.1	µF
C_8	0.22	µF
C_{13}	10	µF

Using an oscilloscope, it should be verified that the ramp generator is ramping down from – 1.6 to – 7.1 V. The slope of the ramp can be changed by C_4 and the DC level of the waveform can be adjusted by R_7.

Pin 9 has a low internal impedance and requires R_{P2} to adjust the feedback level. Pin 8 must always be connected to V_{EE} through a filtering capacitor. For values of R_{10} less than 100 kΩ, the circuit becomes sensitive and could become unstable. Figures 11 and 12 show typical waveforms. As shown, the increase in motor current has resulted in the firing angle to decrease. This translates to an increase in the average power delivered to the load.

Figure 11. No Load Applied

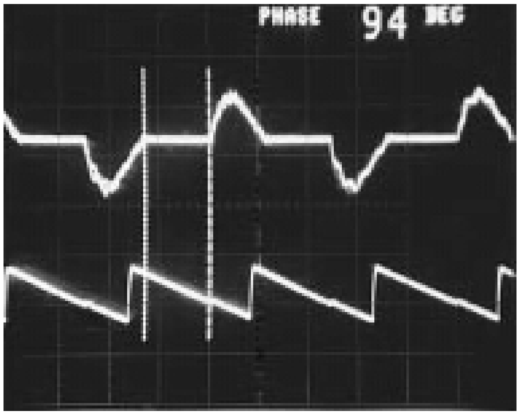


Figure 12. Load Applied

Temperature Effects

The TDA1185A has a very efficient internal temperature compensation. If the current feedback is not connected, the RMS power delivered to the load is stabilized within ± 0.2% over a temperature range of 20 to 70°C. The feedback introduces, in the same temperature range, a drift of 250 mV on the voltage of Pin 8; this slight increase in conduction angle may be successfully used to compensate a motor ohmic resistance increase with temperature.

Main Line Voltage Compensation

As the conduction angle is independent of main line voltage, any change in the latter induces a power variation to the load. A resistor connected to the rectifier anode and to Pin 12 with a capacitor to V_{EE} will introduce a decrease in voltage at Pin 12 as the line voltage is increasing. The values of the RC network can experimentally be determined.

Firing Angle Dynamics

With purely resistive loads, the effective RMS applied voltage to the load is directly proportional to the firing angle (Figure 13). With inductive loads, since the current lags with respect to voltage, 100% power corresponds to a firing angle which is less than 180°.

APPLICATION IDEAS

Soft–Start

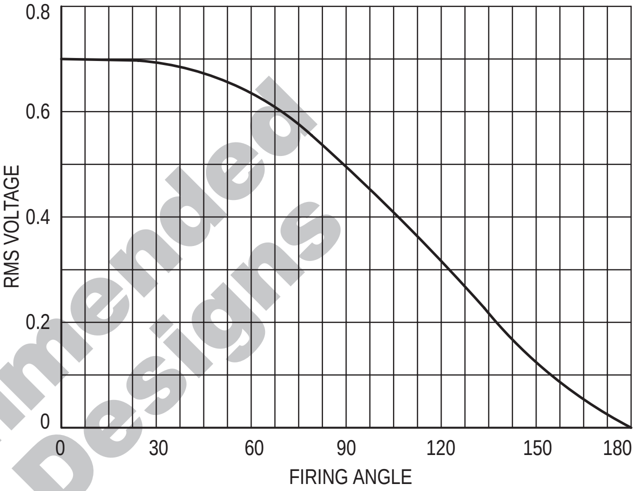
The Soft–Start feature of the TDA1185A in itself opens the door to a lot of interesting applications. For example, the TDA1185A can be used to bring up fragile loads slowly. Expensive and sensitive tubes can be turned on slowly, thus eliminating the inrush of current that could lead to burn out. In this application, R_{P1} is replaced with a resistor divider such that the voltage at Pin 12 results in a conduction angle of 180°. Pin 9 should be grounded, since the feedback portion of the TDA1185A is not necessary (see Figure 14). The time to achieve full conduction is found by the equation below:

$$\Delta t \approx 8.71 \times R_{10} \times C_{13}$$

Light Dimmer

With practically no modification the TDA1185A can be used in a light dimmer application. All that is required is to ground the input to the feedback Pin 9. By grounding Pin 9, we have disconnected the feedback loop and the conduction angle is controlled solely by R_{P1}. Further, since the feedback is disconnected, R_9 and R_{P2} are no longer necessary. The Soft–Start feature can still be used to protect the bulb from an inrush of current. This setup can be used in any application that requires manual control of the power delivered to the load (see Figure 15).

Figure 13. RMS Voltage versus Firing Angle



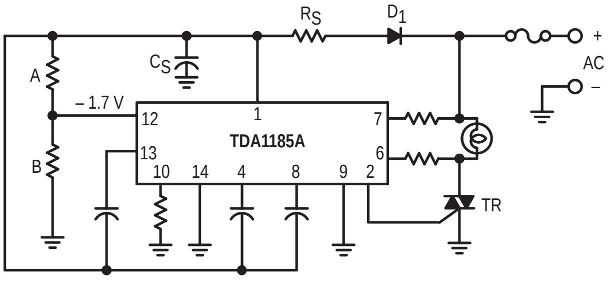
Soft Shut–Off

Once again with little modification, the TDA1185A can be used to turnoff the load slowly. An example of this is in automatic garage lighting. Typically, lights that are on a timer go off without a warning, usually in the most inopportune time (like when you're about to step over the dog). With a soft shut–off, the light dims out slowly, alerting you that it is about to go off. As in the previous case, the feedback is disconnected and R_{P1} is replaced with capacitor C_{12} and a switch (see Figure 16). The turn–off time can be calculated by the following equation:

$$\Delta t \approx R_{12} \times C_{12}$$

R_{12} is the sum of the two resistors on both sides of C_{12}.

Figure 14. Soft–Start Circuit



R_S = 10 kΩ 2 W
R_6 = 470 kΩ. 1/2 W
R_7 = 470 kΩ 1/2 W
R_{10} = 200 kΩ
R_{12A} = 4 x R_{12B}

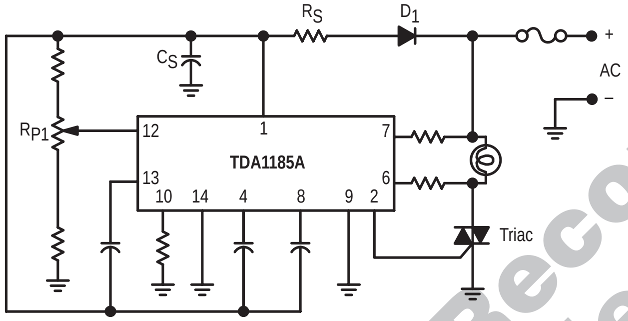
C_4 = 44 nF
C_{13} = 10 µF
C_S = 100 µF
Turn–off time = 8.71 x R_{10} x C_{13}

PC Board

The printed circuit board in Figure 17 is included for the designer's convenience to evaluate the TDA1185A. The size of the board is intentionally small to show the compactness that can be achieved. Figure 18 shows the component layout for the PC board. R_{P1} has one of the outer leads connected to V_{EE} and the other to R_{12}. The center lead of R_{P1} is connected to Pin 12.

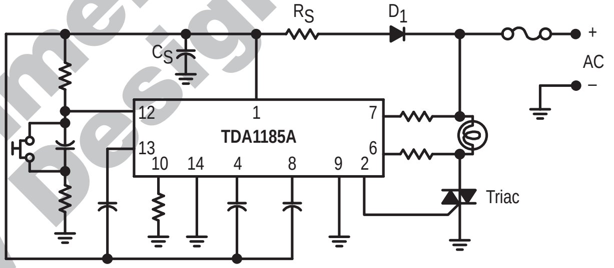
Warning Shock Hazard: It is highly recommended that an isolation transformer be used. Remove the chassis ground for all test equipment.

Figure 15. Light Dimmer Circuit



R_P = 100 k
R_S = 10 k 2 W
R_6 = 470 k 1/2 W
R_7 = 470 k 1/2 W
R_{10} = 200 k
C_4 = 44 nF
C_8 = 0.22 µF
C_{13} = 4.7 µF
C_S = 100 µF 16 V

Figure 16. Soft Shut–Off Circuit



R_S = 10 k 2 W
R_6 = 470 k 1/2 W
R_7 = 470 k 1/2 W
R_{12} = Designer's Choice
R_{10} = 200 k
C_4 = 44 nF
C_{12} = Designer's Choice
C_{13} = 0.47 µF
C_S = 100 µF
Turn–off time = R_{12} x C_{12}

Figure 17. Evaluation Board
(Component Side)

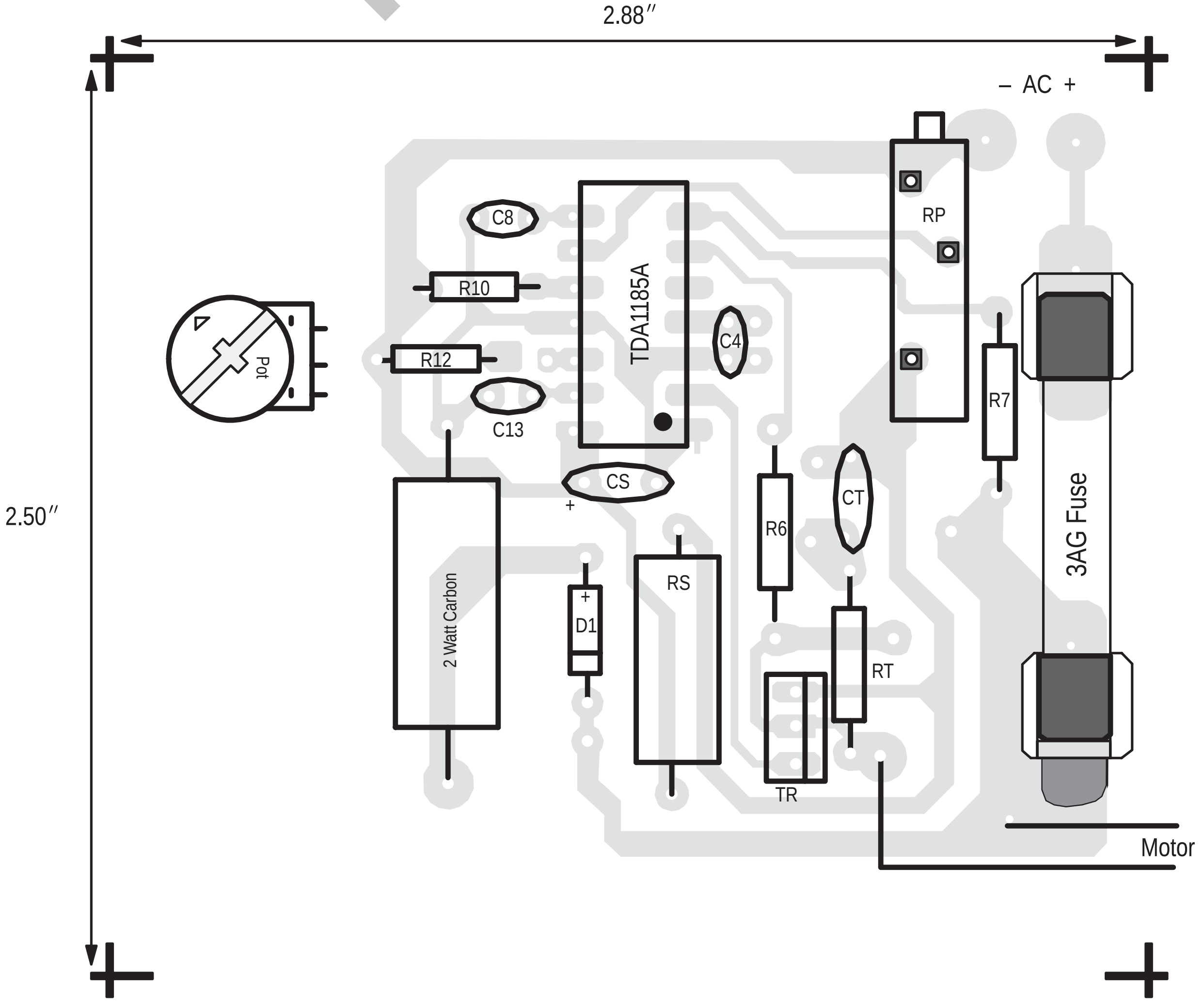
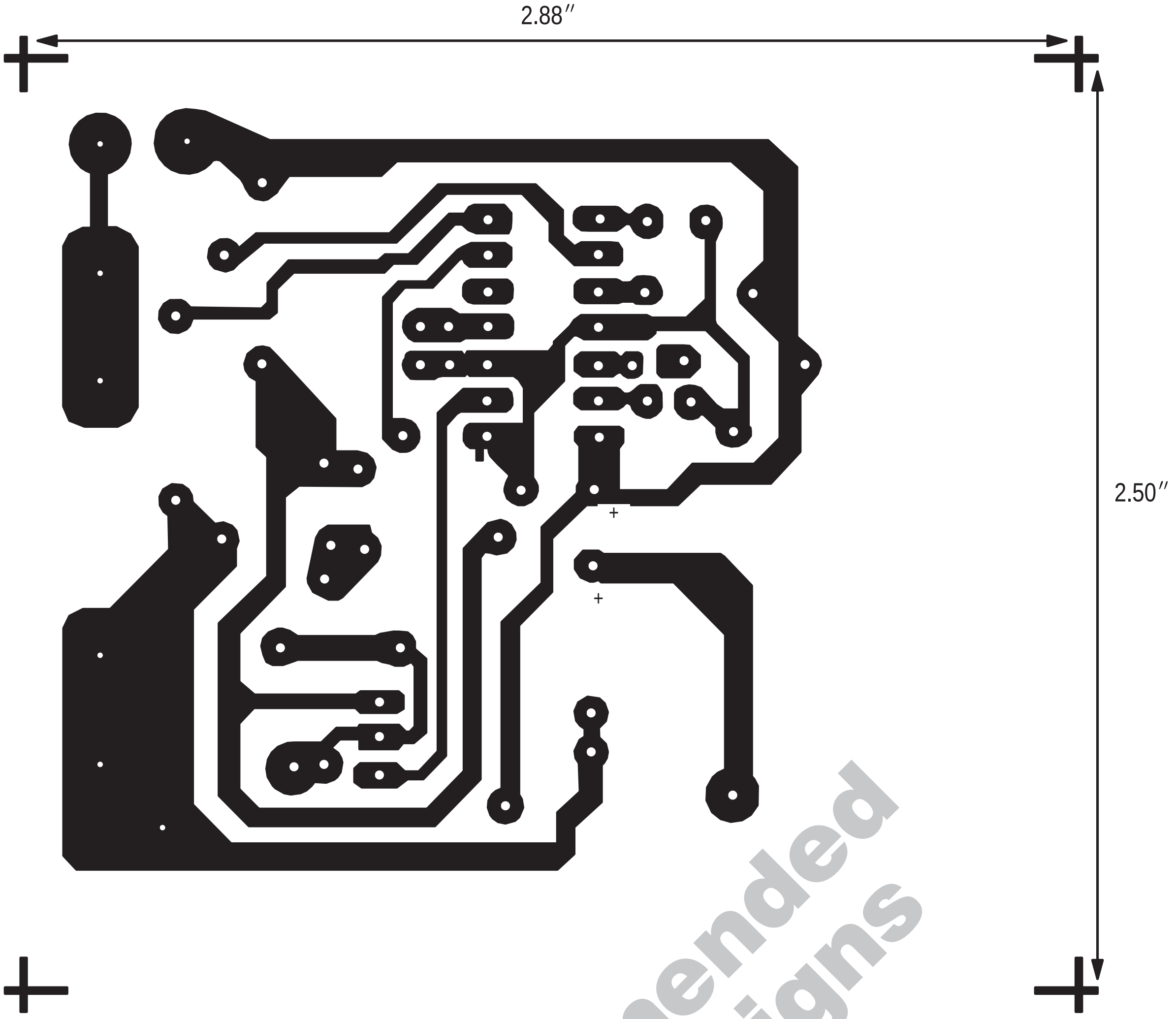


Figure 18. Evaluation Board
(Copper Side)



MOTOROLA

UAA1016B

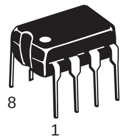
Zero Voltage Controller

The UAA1016B is designed to drive triacs with the Zero Voltage technique which allows RFI free power regulation of resistive loads. It provides the following features:

- Proportional Temperature Control Over an Adjustable Band
- Adjustable Burst Frequency (to Comply with Standards)
- No DC Current Component Through the Main Line (to Comply with Standards)
- Negative Output Current Pulses (Triac Quadrants 2 and 3)
- Direct AC Line Operation
- Low External Components Count

ZERO VOLTAGE SWITCH PROPORTIONAL BAND TEMPERATURE CONTROLLER

SEMICONDUCTOR TECHNICAL DATA

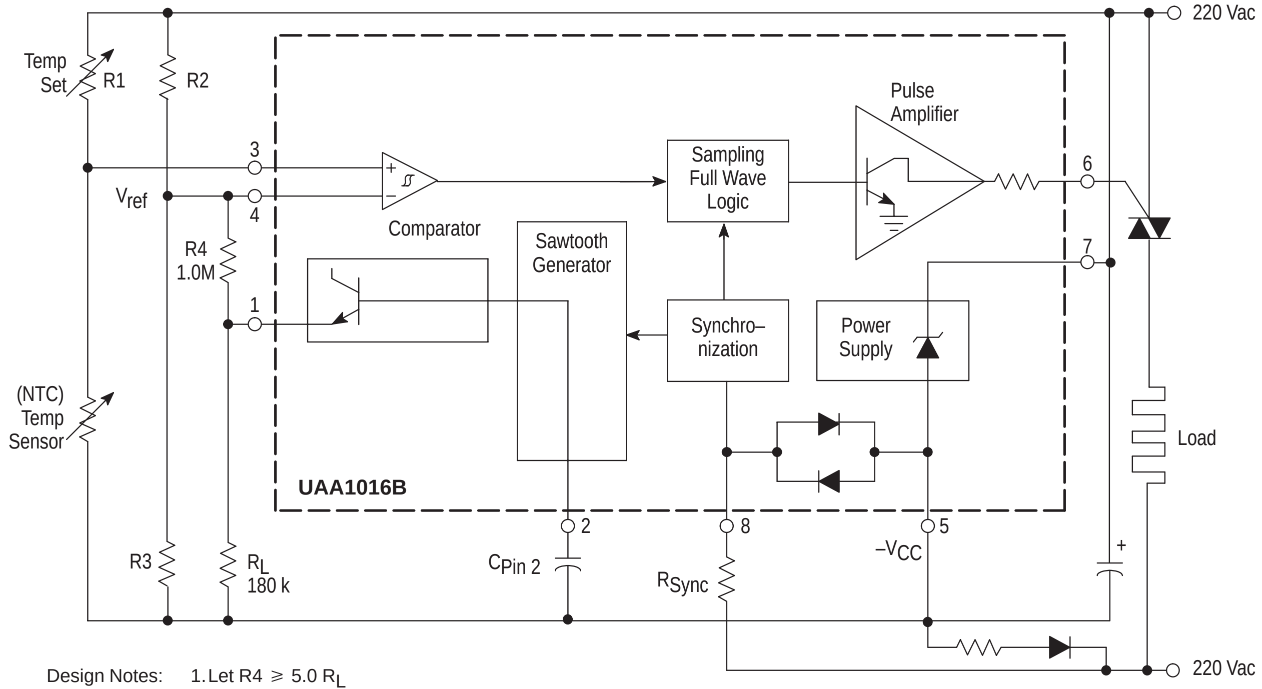


PLASTIC PACKAGE
CASE 626

ORDERING INFORMATION

Device	Operating Temperature Range	Package
UAA1016B	T_A = –20° to +100°C	Plastic DIP

Representative Block Diagram and Pin Connections



Design Notes:
1. Let R4 ⩾ 5.0 R_L
2. Select $\frac{R2}{R3}$ Ratio for a symmetrical reference deviation centered about Pin 1 output swing, R2 will be slightly greater than R3.
3. Select R2 and R3 values for the desired reference deviation where $\Delta V_{ref} = \dfrac{\Delta V_{Pin1}}{\dfrac{R4}{R2\,||\,R3} + 1}$

This device contains 30 active transistors.

MAXIMUM RATINGS (Voltages Referred to Pin 7)

Parameter	Symbol	Max. Rating	Unit
Supply Current ($I_{Pin\ 5}$)	I_{CC}	15	mA
Nonrepetitive Supply Current ($I_{Pin\ 5}$)	I_{CCP}	200	mA
AC Synchronization Current (Pin 8)	I_{syn}	3.0	mArms
Maximum Pin Voltages	$V_{Pin\ 1}$ $V_{Pin\ 2}$ $V_{Pin\ 3}$ $V_{Pin\ 4}$ $V_{Pin\ 6}$	0; – V_{CC} 0; – V_{CC} 0; – V_{CC} 0; – V_{CC} 2.0; – V_{CC}	V
Maximum Current Drain	$I_{Pin\ 1}$	1.0	mA
Power Dissipation $T_A = 25°C$	P_D	625	mW
Maximum Thermal Resistance	$R_{\theta JA}$	100	°C/W
Operating Temperature Range	T_A	–20 to +100	°C

NOTE: ESD data available upon request.

ELECTRICAL CHARACTERISTICS (T_A = 25°C, Voltages Referred to Pin 7, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Current Consumption (Pins 6 and 8 not connected)	I_{CC}	–	0.8	1.5	mA
Stabilized Supply Voltage ($V_{Pin\ 5}$) I_{CC} = 2.0 mA max	$–V_{CC}$	–9.6	–8.6	–7.6	V
Output Pulse Current ($V_{Pin\ 6}$ from –1.0 to +1.0 V)	I_{out}	60	90	120	mA
Output Pulse Width $R_{Pin\ 8}$ = 220 kΩ , V_{mains} = 220 Vac/50 Hz, (Figures 3 and 4)	t_{p1} t_{p2}	58 160	60 220	120 320	µs
Comparator Input Offset Voltage ($V_{Pin\ 3} – V_{Pin\ 4}$)	V_{off}	–10	–	10	mV
Comparator Common Mode Voltage Range	V_{CM}	$–V_{CC} + 1$	–	–1.5	V
Input Bias Current (Pins 3 and 4)	I_{IB}	–	–	1.0	µA
Output Leakage Current ($I_{Pin\ 6}$) $V_{Pin\ 6}$ = +2.0 V	I_{outL}	–	–	10	µA
Capacitor Charging Current (Source)	$I_{Pin\ 2}$	–20	–16	–12	µA
Capacitor Discharge Current (Sink)	$I'_{Pin\ 2}$	–	6.4	–	mA
Sawtooth Pulse Length ($C_{Pin\ 2}$ = 1.0 µF)	t_{saw}	–	0.85	–	S
Output Threshold Sawtooth Levels ($V_{Pin\ 2}$)	V_{TH1} V_{TH2}	– –	–1.0 $–V_{CC} + 1.25$	– –	V
Output Voltage Pin 1	$V_{Pin\ 1}$	–	$V_{Pin\ 2} – 0.75$	–	V

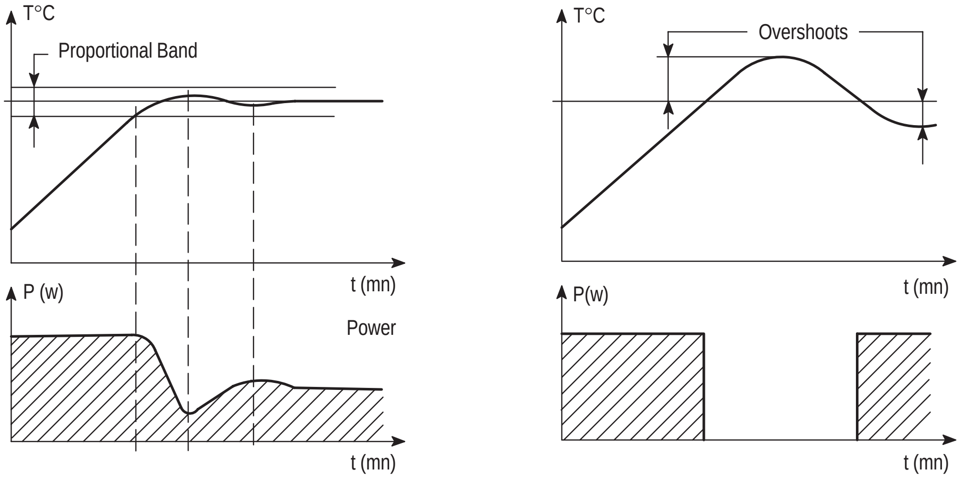
CIRCUIT DESCRIPTION

The circuit delivers current pulses to the triac at zero crossings of the main line sensed by Pin 8 through R_{sync}. An internal full wave logic allows the triac to latch during full wave periods in order to avoid any dc component in the main line, in compliance with European regulations. Trigger pulses are generated when the comparator detects $V_{Pin\ 3}$ is above $V_{Pin\ 4}$ (or $V_{reference}$) as sensed temperature through the NTC is then lower than the set value (V_{ref} corresponding to the external Wheatstone bridge equilibrium).

In order to comply with norms limiting the frequency at which a kW sized load, or above, may be connected to the main line (fluorescent tubes “flickering”), the UAA1016B has an internal time base providing (power is delivered by bursts to the load) a proportional temperature band control. In fact, most of the heating regulation systems require low temperature overshoot for more precision and stability which cannot be accomplished by direct on/off regulation (see Figure 1). An internal low frequency sawtooth generator whose output is available at Pin 1, allows the designer to introduce a periodic linear change of V_{ref}. This deviation defines the temperature band allowing proportional power control (see Figure 2).

The IC is directly powered from the mains by a dropping resistor, a diode and a filter capacitor.

Figure 1. Proportional Temperature Control versus On/Off Control



(PROPORTIONAL TEMPERATURE CONTROL)

Reduced Overshoot
Stability

(ON/OFF CONTROL)

Large Overshoot
Marginal Stability

KEY CIRCUIT FUNCTIONS DESCRIPTION

Power Supply

The rectified supply current is Zener regulated to 8.6 V. Current consumption of the UAA1016B is typically less than 1.0 mA. The major part of the current fed by the dropping resistor is used for the sensor bridge and triac gate pulses. Any excess of supply current is excess power dissipation into the integrated Zener. Current consumption of the triac pulses may be derived from Figure 3 and 4 (Igt maximum and pulse duration). Usually an 18 kΩ, 2.0 W dropping resistor is convenient to feed the UAA1016.

Comparator

When $V_{Pin\ 3}$ is higher than $V_{Pin\ 4}$ (V_{ref}), the comparator allows the triggering logic to deliver pulses to the triac (Figure 2). The offset hysteresis input voltage has been designed to be as low as possible (±10 mV maximum) in order to minimize the uncontrollable temperature band (proportional to the hysteresis) as per Figure 5. Noise rejection is performed by a synchronous sampling of the comparator output during very short times (typical less than 100 ns).

Sawtooth Generator

A sawtooth voltage signal is generated by a constant current source (typical 7.5 µA), charging an external capacitor $C_{Pin\ 2}$ between two threshold levels, V_{TH1} and V_{TH2}, which are respectively:

$V_{TH1} = –1.0\ V$
$V_{TH2} = –V_{CC} + 1.25\ V$

Charging and discharging currents occur only with negative halfcycles of the line. In the UAA1016B, the sawtooth signal is available at Pin 1 as a voltage source $V_{Pin\ 1} = V_{Pin\ 2} – 0.75\ V$. Maximum source current is 1.0 mA, but to keep good linearity of sawtooth signal, a source current of 40 µA is recommended (see Figure 6).

Sampling Full Wave Logic

Two consecutive zero–crossing trigger pulses are generated at every positive mains half–cycle of the line to minimize generation of noise (as per Figure 7). Within every zero–crossing the pulses are positioned as per Figure 3. Pulse length is also adjustable by R_{sync} on Pin 8 to allow positive triggering of the triac at this critical moment (firing with low voltage between main terminals requires long pulses).

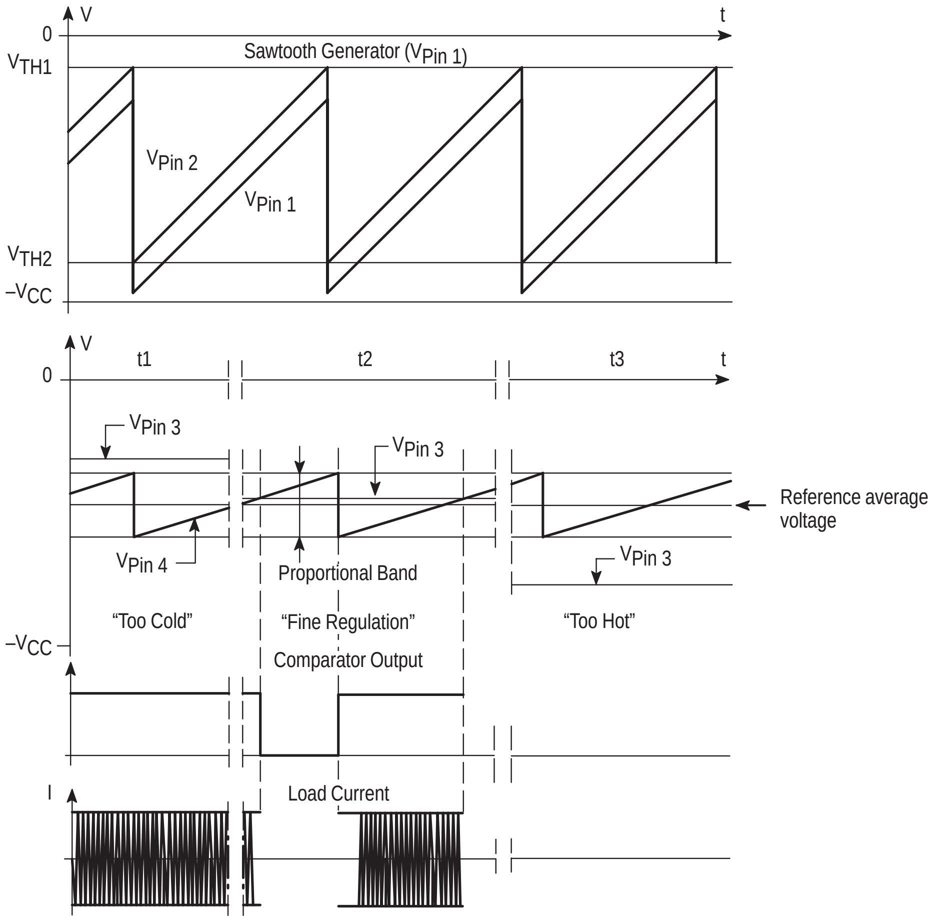
Pulse Amplifier

The pulse amplifier circuit delivers minimum current pulses of 60 mA (sink). The triac is triggered in quadrants II and III.

Synchronization Circuit

This circuit detects mains zero–crossings through R_{sync} and the value selected determines the trigger pulse length. A zero crossing current detector is employed with typical thresholds of ± 27 µA to ± 98 µA (see Figures 3 and 4).

Figure 2. Sawtooth Generator and Proportional Band



COMMENTS TO FIGURE 2

Referring to Figure 1, the average value of V_{ref} is set by R2 and R3. R4 defines the amplitude of the sawtooth signal superimposed on V_{ref}, defining the Proportional Band.

Figure 2 shows three conditions:

1) During time t1 we always have $V_{Pin\ 3} > V_{ref}$, and as a result, the comparator is always "on" and the triac fired (100% maximum power)

2) During time t2, $V_{Pin\ 3}$ is in the proportional band, and the average power delivered to the load is a fraction of maximum power.

3) During time t3, $V_{Pin\ 3} < V_{ref}$, and the triac is always "off."

When the sensor temperature is above the set value and is slowly decreasing as no heating occurs, $V_{Pin\ 3} – V_{Pin\ 4}$ must exceed half the hysteresis value before power is applied again (1). A similar effect occurs in the opposite direction when temperature sensor is below the set value and can remain stable as position (2). This defines the "uncontrollable temperature band" which will be very small if hysteresis is also very small.

SUGGESTIONS FOR USE

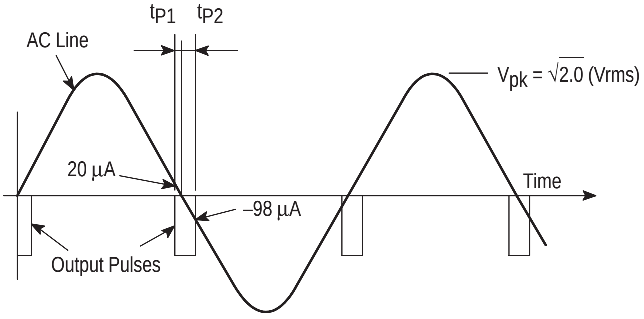
The temperature sensor circuit is a Wheatstone bridge including the sensor element. Comparator inputs may be free from power line noise only if the sensor element is purely resistive (NTC resistor). Usage of any P–N junction sensor would drastically reduce noise rejection.

Fixed phase sensing of the internal comparator output eliminates parasitic signals.

Some loads, even designed to be resistive, have in fact a slight inductive component. A phase shift at Pin 8 can be achieved with external capacitor C3 connected to Pin 8 network (see Figure 8).

Suggested maximum source current at Pin 1 is 40 µA, in order to have acceptable sawtooth signal linearity.

Figure 3. Output Pulse Width Definitions



$$t_{P2} = \frac{\sin^{-1}\left(\frac{98\times10^{-6}}{Vrms \cdot \sqrt{2.0}}\right)}{360f_{AC}} \qquad t_{P1} = \frac{\sin^{-1}\left(\frac{27\times10^{-6}}{Vrms \cdot \sqrt{2.0}}\right)}{360f_{AC}}$$

Figure 4. Typical Output Pulse Length versus Synchronization Resistor

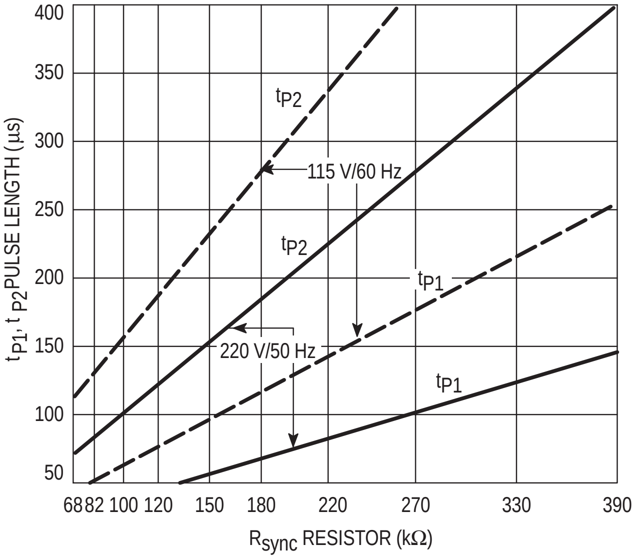


Figure 5. Effects of Inputs Comparator Hysteresis

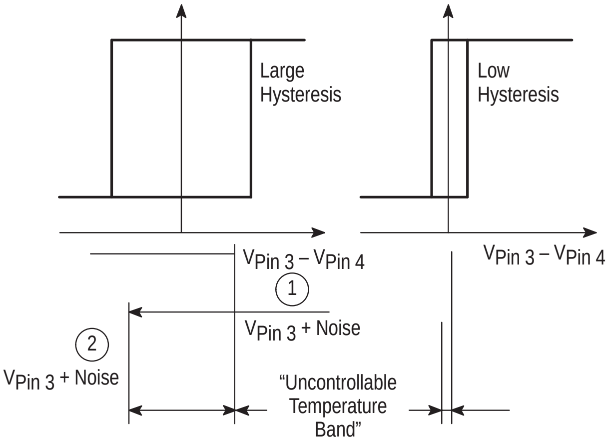


Figure 6. Pin 1 Internal Network

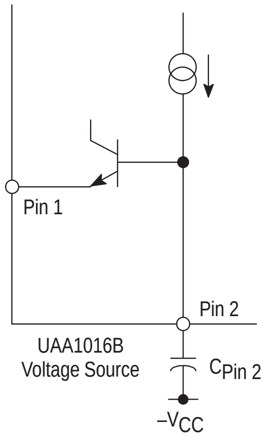
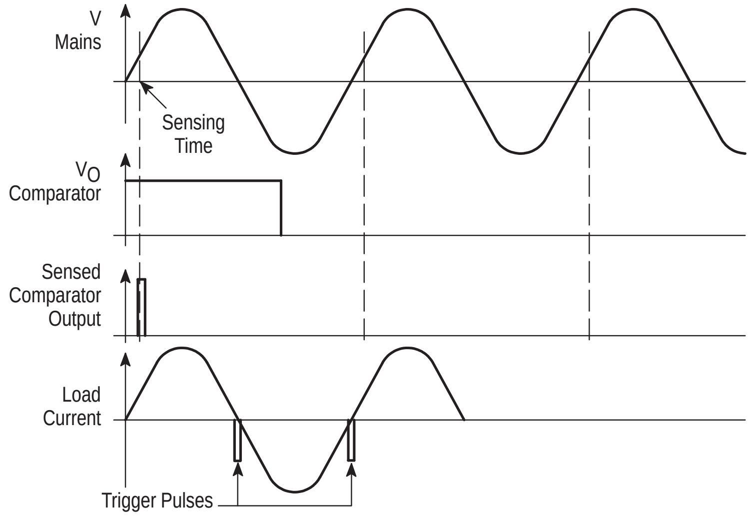


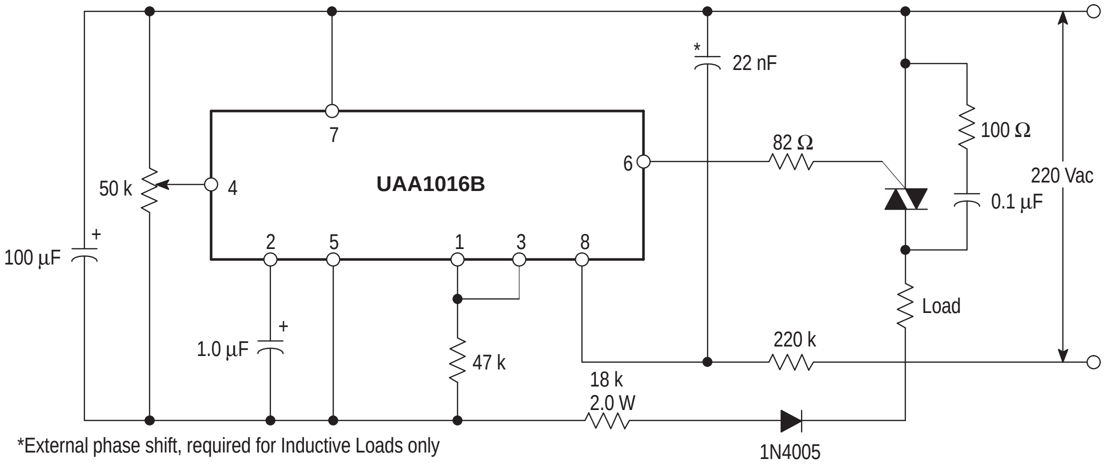
Figure 7. Trigger Pulse Generation



APPLICATION CIRCUITS

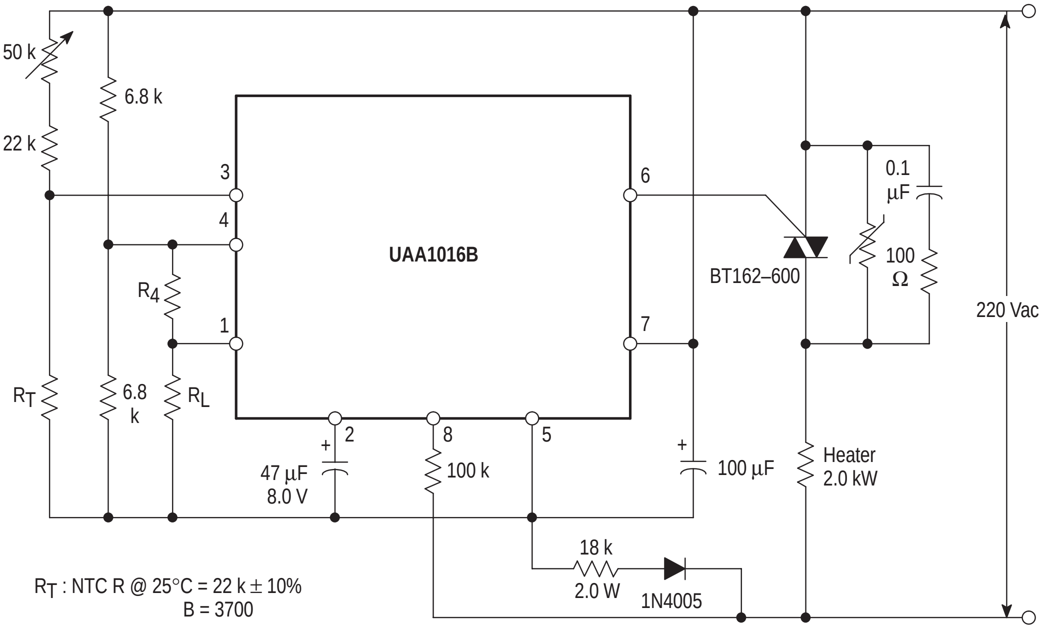
Figure 8 shows a very simple application of the UAA1016B as an electronic rheostat having 100% efficiency. C3 is required only if load has an inductive component. Figure 9 shows a typical application as a panel heater thermostat with a proportional temperature band of 1.0°C at 25°C.

Figure 8. Electronic Rheostat



*External phase shift, required for Inductive Loads only

Figure 9. Application Circuit–Electric Radiator with Proportional Band Thermostat
(Proportional Band 1°C at 25°C)



R_T : NTC R @ 25°C = 22 k ± 10%
B = 3700

MOTOROLA

UAA2016

Product Preview

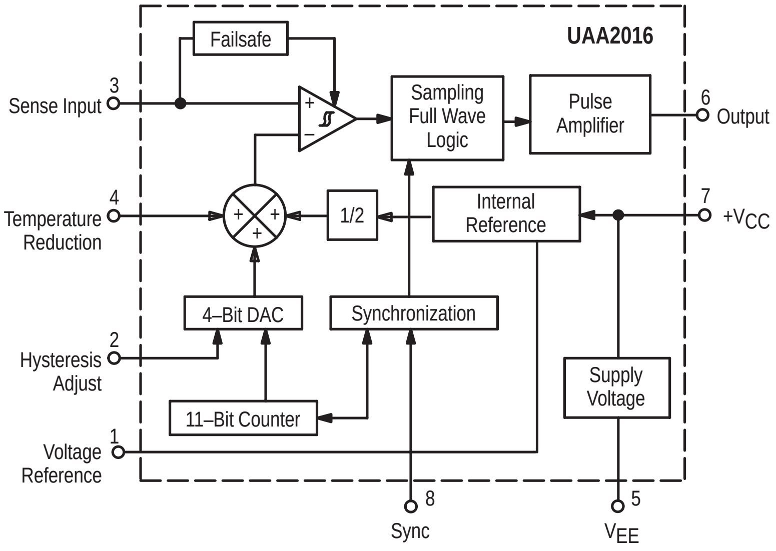
Zero Voltage Switch Power Controller

The UAA2016 is designed to drive triacs with the Zero Voltage technique which allows RFI–free power regulation of resistive loads. Operating directly on the AC power line, its main application is the precision regulation of electrical heating systems such as panel heaters or irons.

A built–in digital sawtooth waveform permits proportional temperature regulation action over a ±1°C band around the set point. For energy savings there is a programmable temperature reduction function, and for security a sensor failsafe inhibits output pulses when the sensor connection is broken. Preset temperature (i.e. defrost) application is also possible. In applications where high hysteresis is needed, its value can be adjusted up to 5°C around the set point. All these features are implemented with a very low external component count.

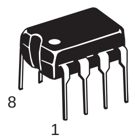
- Zero Voltage Switch for Triacs, up to 2.0 kW (MAC212A8)
- Direct AC Line Operation
- Proportional Regulation of Temperature over a 1°C Band
- Programmable Temperature Reduction
- Preset Temperature (i.e. Defrost)
- Sensor Failsafe
- Adjustable Hysteresis
- Low External Component Count

Representative Block Diagram

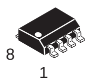


ZERO VOLTAGE SWITCH POWER CONTROLLER

SEMICONDUCTOR TECHNICAL DATA

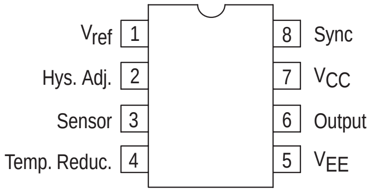


P SUFFIX
PLASTIC PACKAGE
CASE 626



D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
UAA2016D	T_A = – 20° to +85°C	SO–8
UAA2016P		Plastic DIP

MAXIMUM RATINGS (Voltages referenced to Pin 7)

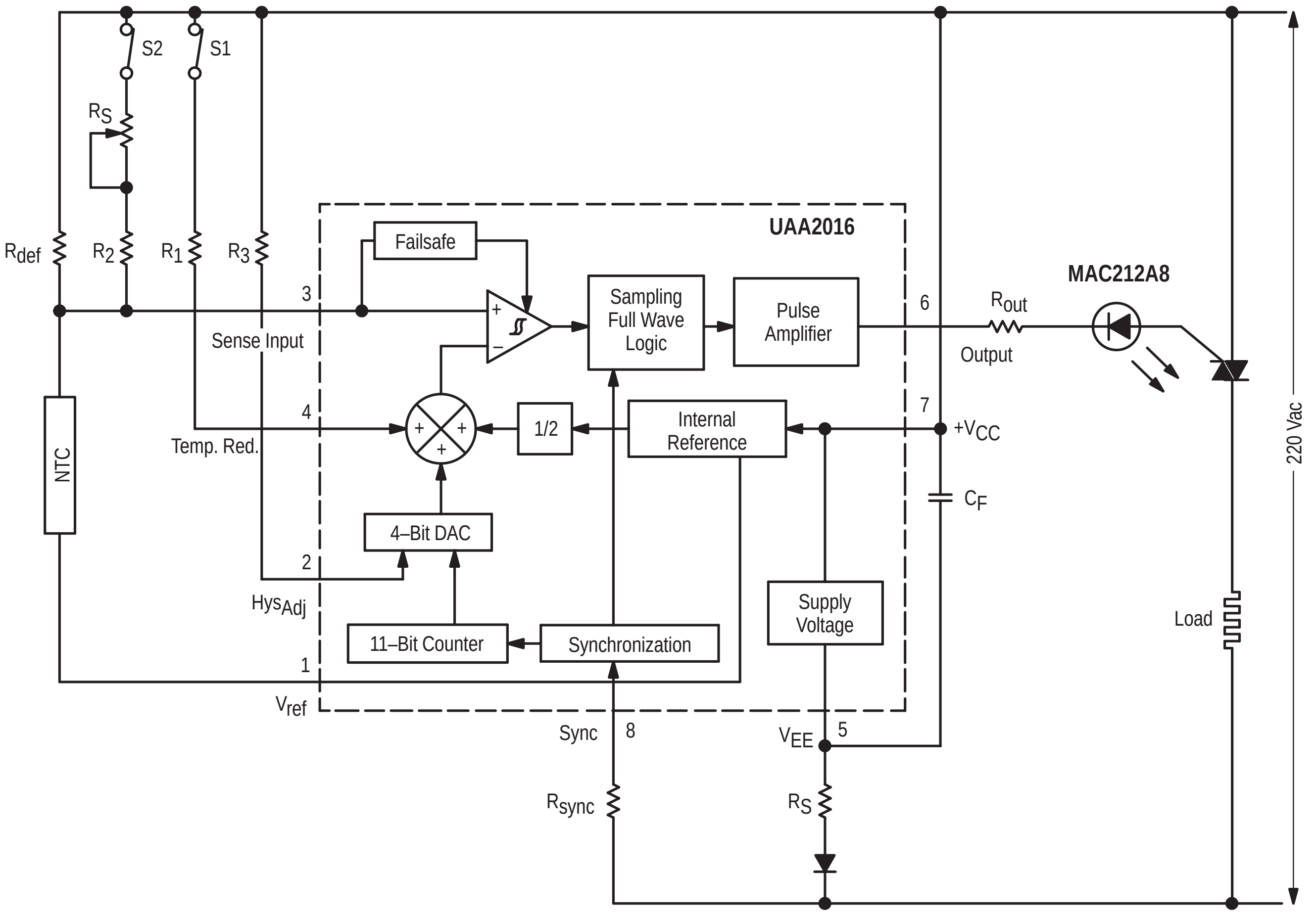
Rating	Symbol	Value	Unit
Supply Current ($I_{Pin\ 5}$)	I_{CC}	15	mA
Non–Repetitive Supply Current (Pulse Width = 1.0 µs)	I_{CCP}	200	mA
AC Synchronization Current	I_{sync}	3.0	mA
Pin Voltages	$V_{Pin\ 2}$ $V_{Pin\ 3}$ $V_{Pin\ 4}$ $V_{Pin\ 6}$	0; V_{ref} 0; V_{ref} 0; V_{ref} 0; V_{EE}	V
V_{ref} Current Sink	$I_{Pin\ 1}$	1.0	mA
Output Current (Pin 6) (Pulse Width < 400 µs)	I_O	150	mA
Power Dissipation	P_D	625	mW
Thermal Resistance, Junction–to–Air	$R_{\theta JA}$	100	°C/W
Operating Temperature Range	T_A	– 20 to + 85	°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{EE} = –7.0 V, voltages referred to Pin 7, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Supply Current (Pins 6, 8 not connected) (T_A = – 20° to + 85°C)	I_{CC}	—	0.9	1.5	mA
Stabilized Supply Voltage (Pin 5) (I_{CC} = 2.0 mA)	V_{EE}	–10	– 9.0	– 8.0	V
Reference Voltage (Pin 1)	V_{ref}	– 6.5	– 5.5	– 4.5	V
Output Pulse Current (T_A = – 20° to + 85°C) (R_{out} = 60 W, V_{EE} = – 8.0 V)	I_O	90	100	130	mA
Output Leakage Current (V_{out} = 0 V)	I_{OL}	—	—	10	µA
Output Pulse Width (T_A = – 20° to + 85°C) (Note 1) (Mains = 220 Vrms, R_{sync} = 220 kΩ)	T_P	50	—	100	µs
Comparator Offset (Note 5)	V_{off}	–10	—	+10	mV
Sensor Input Bias Current	I_{IB}	—	—	0.1	µA
Sawtooth Period (Note 2)	T_S	—	40.96	—	sec
Sawtooth Amplitude (Note 6)	A_S	50	70	90	mV
Temperature Reduction Voltage (Note 3) (Pin 4 Connected to V_{CC})	V_{TR}	280	350	420	mV
Internal Hysteresis Voltage (Pin 2 Not Connected)	V_{IH}	—	10	—	mV
Additional Hysteresis (Note 4) (Pin 2 Connected to V_{CC})	V_H	280	350	420	mV
Failsafe Threshold (T_A = – 20° to + 85°C) (Note 7)	V_{FSth}	180	—	300	mV

NOTES:
1. Output pulses are centered with respect to zero crossing point. Pulse width is adjusted by the value of R_{sync}. Refer to application curves.
2. The actual sawtooth period depends on the AC power line frequency. It is exactly 2048 times the corresponding period. For the 50 Hz case it is 40.96 sec. For the 60 Hz case it is 34.13 sec. This is to comply with the European standard, namely that 2.0 kW loads cannot be connected or removed from the line more than once every 30 sec.
3. 350 mV corresponds to 5°C temperature reduction. This is tested at probe using internal test pad. Smaller temperature reduction can be obtained by adding an external resistor between Pin 4 and V_{CC}. Refer to application curves.
4. 350 mV corresponds to a hysteresis of 5°C. This is tested at probe using internal test pad. Smaller additional hysteresis can be obtained by adding an external resistor between Pin 2 and V_{CC}. Refer to application curves.
5. Parameter guaranteed but not tested. Worst case 10 mV corresponds to 0.15°C shift on set point.
6. Measured at probe by internal test pad. 70 mV corresponds to 1°C. Note that the proportional band is independent of the NTC value.
7. At very low temperature the NTC resistor increases quickly. This can cause the sensor input voltage to reach the failsafe threshold, thus inhibiting output pulses; refer to application schematics. The corresponding temperature is the limit at which the circuit works in the typical application. By setting this threshold at 0.05 V_{ref}, the NTC value can increase up to 20 times its nominal value, thus the application works below – 20°C.

Figure 1. Application Schematic



APPLICATION INFORMATION

(For simplicity, the LED in series with R_{out} is omitted in the following calculations.)

Triac Choice and R_{out} Determination

Depending on the power in the load, choose the triac that has the lowest peak gate trigger current. This will limit the output current of the UAA2016 and thus its power consumption. Use Figure 4 to determine R_{out} according to the triac maximum gate current (I_{GT}) and the application low temperature limit. For a 2.0 kW load at 220 Vrms, a good triac choice is the Motorola MAC212A8. Its maximum peak gate trigger current at 25°C is 50 mA.

For an application to work down to – 20°C, R_{out} should be 60 Ω. It is assumed that: $I_{GT}(T) = I_{GT}(25°C) \times \exp(–T/125)$ with T in °C, which applies to the MAC212A8.

Output Pulse Width, R_{sync}

The pulse with T_P is determined by the triac's I_{Hold}, I_{Latch} together with the load value and working conditions (frequency and voltage):

Given the RMS AC voltage and the load power, the load value is:

$$R_L = V^2\text{rms/POWER}$$

The load current is then:

$$I_{Load} = (\text{Vrms} \times \sqrt{2} \times \sin(2\pi ft) – V_{TM})/R_L$$

where V_{TM} is the maximum on state voltage of the triac, f is the line frequency.

Set $I_{Load} = I_{Latch}$ for $t = T_P/2$ to calculate T_P.

Figures 6 and 7 give the value of T_P which corresponds to the higher of the values of I_{Hold} and I_{Latch}, assuming that V_{TM} = 1.6 V. Figure 8 gives the R_{sync} that produces the corresponding T_P.

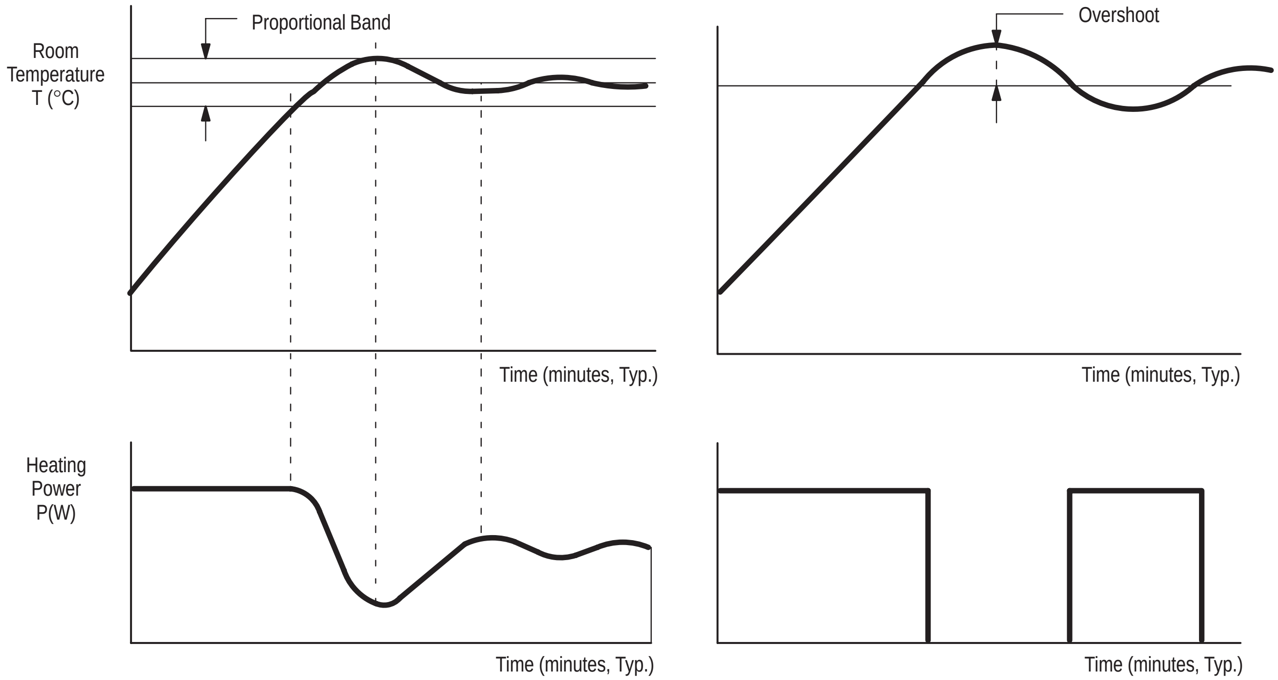
R_{Supply} and Filter Capacitor

With the output current and the pulse width determined as above, use Figures 9 and 10 to determine R_{Supply}, assuming that the sinking current at V_{ref} pin (including NTC bridge current) is less than 0.5 mA. Then use Figure 11 and 12 to determine the filter capacitor (C_F) according to the ripple desired on supply voltage. The maximum ripple allowed is 1.0 V.

Temperature Reduction Determined by R_1

(Refer to Figures 13 and 14.)

Figure 2. Comparison Between Proportional Control and ON/OFF Control



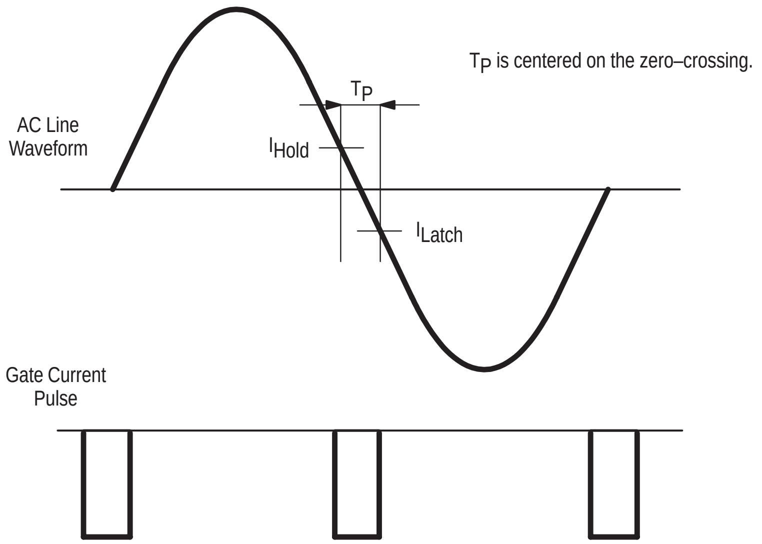
Proportional Temperature Control

- Reduced Overshoot
- Good Stability

ON/OFF Temperature Control

- Large Overshoot
- Marginal Stability

Figure 3. Zero Voltage Technique



T_P is centered on the zero–crossing.

$$T_P = \frac{14 \times R_{sync} + 7 \times 10^5}{Vrms \times \sqrt{2} \times \pi f} (\mu s)$$

f = AC Line Frequency (Hz)
Vrms = AC Line RMS Voltage (V)
R_{sync} = Synchronization Resistor (Ω)

CIRCUIT FUNCTIONAL DESCRIPTION

Power Supply (Pin 5 and Pin 7)

The application uses a current source supplied by a single high voltage rectifier in series with a power dropping resistor. An integrated shunt regulator delivers a V_{EE} voltage of – 8.6 V with respect to Pin 7. The current used by the total regulating system can be shared in four functional blocks: IC supply, sensing bridge, triac gate firing pulses and zener current. The integrated zener, as in any shunt regulator, absorbs the excess supply current. The 50 Hz pulsed supply current is smoothed by the large value capacitor connected between Pins 5 and 7.

Temperature Sensing (Pin 3)

The actual temperature is sensed by a negative temperature coefficient element connected in a resistor divider fashion. This two element network is connected between the ground terminal Pin 5 and the reference voltage – 5.5 V available on Pin 1. The resulting voltage, a function of the measured temperature, is applied to Pin 3 and internally compared to a control voltage whose value depends on several elements: Sawtooth, Temperature Reduction and Hysteresis Adjust. (Refer to Application Information.)

Temperature Reduction

For energy saving, a remotely programmable temperature reduction is available on Pin 4. The choice of resistor R_1 connected between Pin 4 and V_{CC} sets the temperature reduction level.

Comparator

When the positive input (Pin 3) receives a voltage greater than the internal reference value, the comparator allows the triggering logic to deliver pulses to the triac gate. To improve the noise immunity, the comparator has an adjustable hysteresis. The external resistor R_3 connected to Pin 2 sets the hysteresis level. Setting Pin 2 open makes a 10 mV hysteresis level, corresponding to 0.15°C. Maximum hysteresis is obtained by connecting Pin 2 to V_{CC}. In that case the level is set at 5°C. This configuration can be useful for low temperature inertia systems.

Sawtooth Generator

In order to comply with European norms, the ON/OFF period on the load must exceed 30 seconds. This is achieved by an internal digital sawtooth which performs the proportional regulation without any additional component. The sawtooth signal is added to the reference applied to the comparator negative input. Figure 2 shows the regulation improvement using the proportional band action.

Noise Immunity

The noisy environment requires good immunity. Both the voltage reference and the comparator hysteresis minimize the noise effect on the comparator input. In addition the effective triac triggering is enabled every 1/3 sec.

Failsafe

Output pulses are inhibited by the “failsafe” circuit if the comparator input voltage exceeds the specified threshold voltage. This would occur if the temperature sensor circuit is open.

Sampling Full Wave Logic

Two consecutive zero–crossing trigger pulses are generated at every positive mains half–cycle. This ensures that the number of delivered pulses is even in every case. The pulse length is selectable by R_{sync} connected on Pin 8. The pulse is centered on the zero–crossing mains waveform.

Pulse Amplifier

The pulse amplifier circuit sinks current pulses from Pin 6 to V_{EE}. The minimum amplitude is 70 mA. The triac is then triggered in quadrants II and III. The effective output current amplitude is given by the external resistor R_{out}. Eventually, an LED can be inserted in series with the Triac gate (see Figure 1).

Figure 4. Output Resistor versus Triac Gate Current

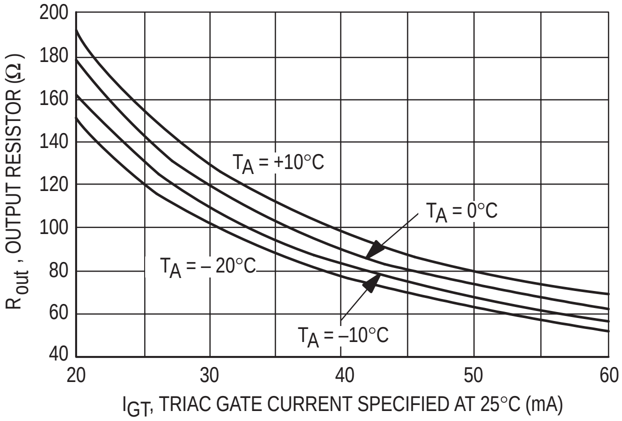


Figure 5. Minimum Output Current versus Output Resistor

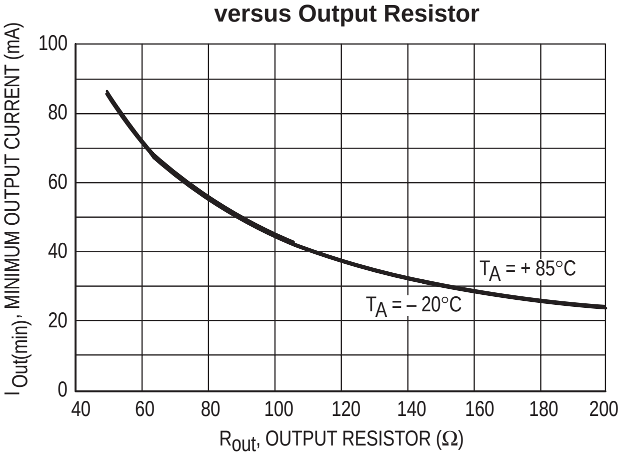


Figure 6. Output Pulse Width versus Maximum Triac Latch Current

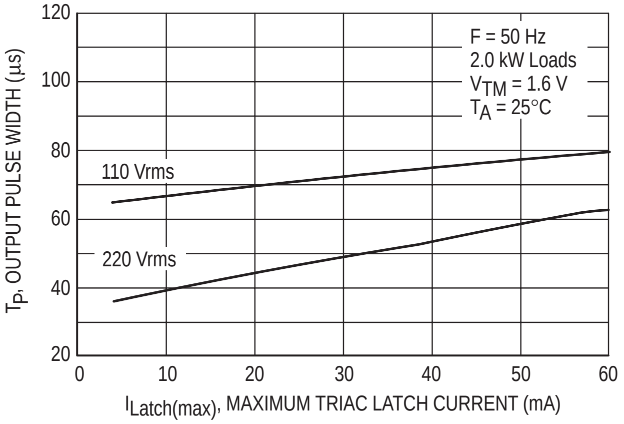


Figure 7. Output Pulse Width versus Maximum Triac Latch Current

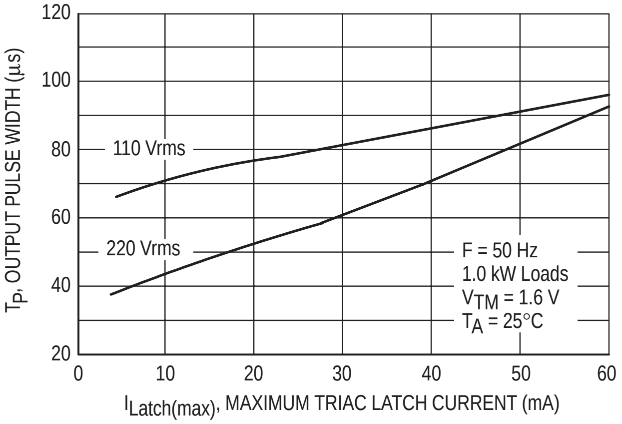


Figure 8. Synchronization Resistor versus Output Pulse Width

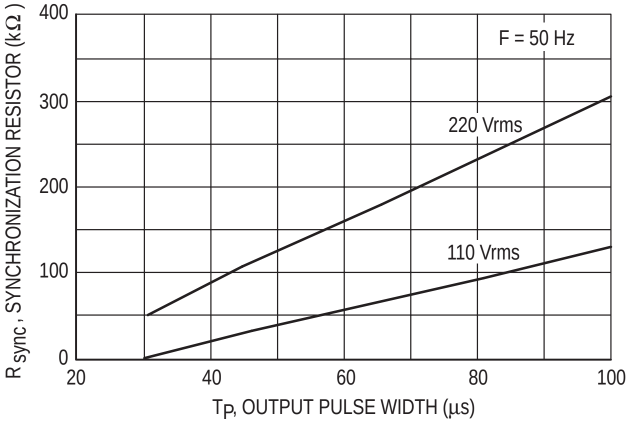


Figure 9. Maximum Supply Resistor versus Output Current

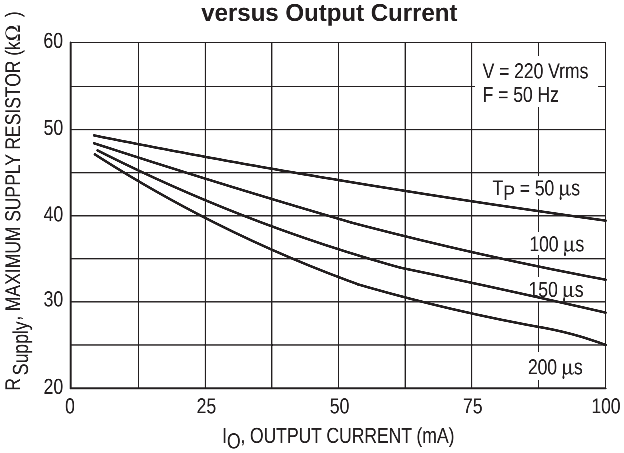


Figure 10. Maximum Supply Resistor versus Output Current

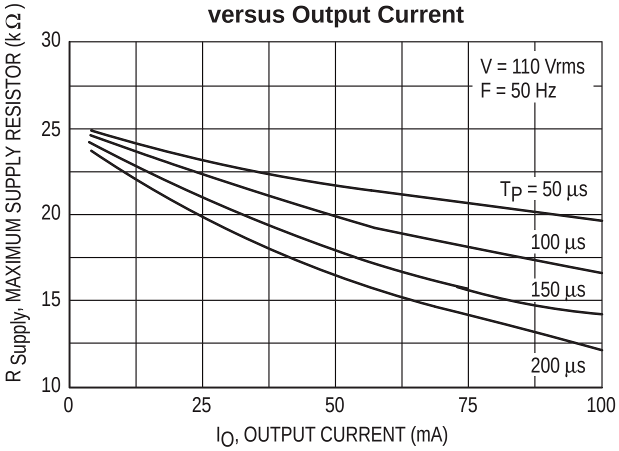


Figure 11. Minimum Filter Capacitor versus Output Current

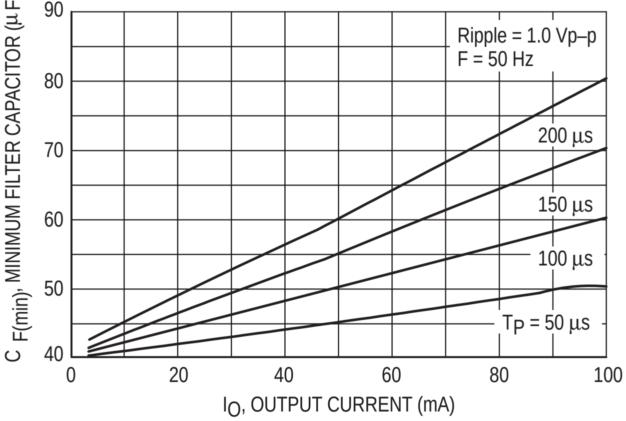


Figure 12. Minimum Filter Capacitor versus Output Current

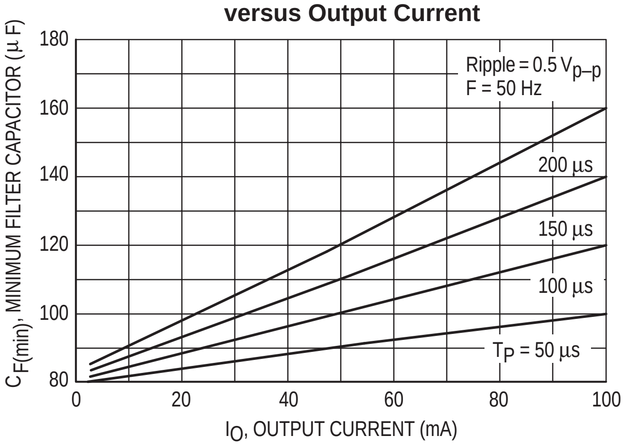


Figure 13. Temperature Reduction versus R_1

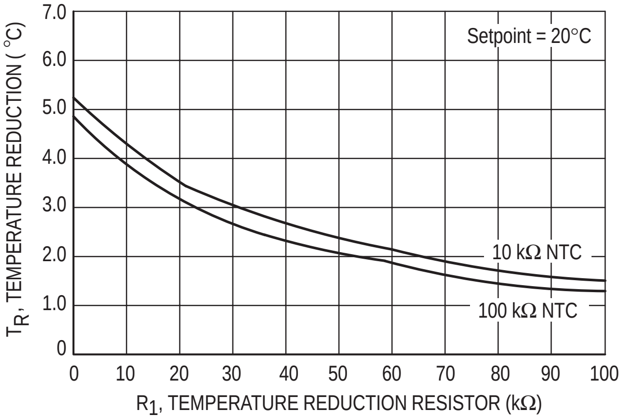


Figure 14. Temperature Reduction versus Temperature Setpoint

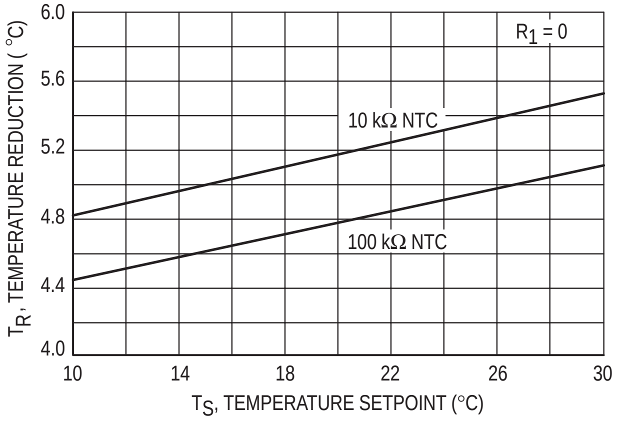


Figure 15. R_{DEF} versus Preset Temperature

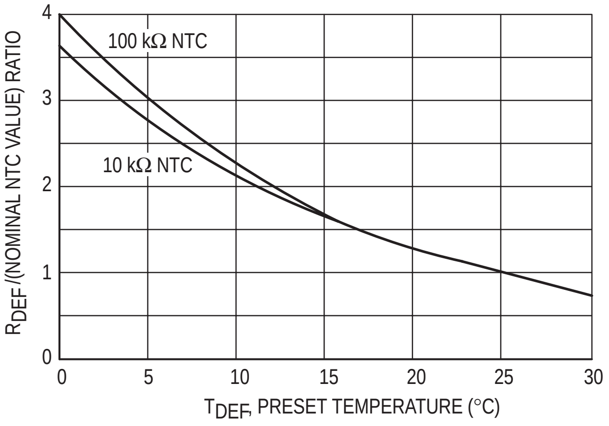


Figure 16. $R_S + R_2$ versus Preset Setpoint

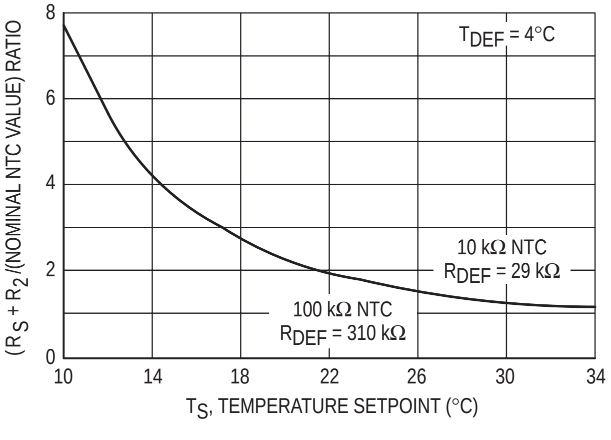
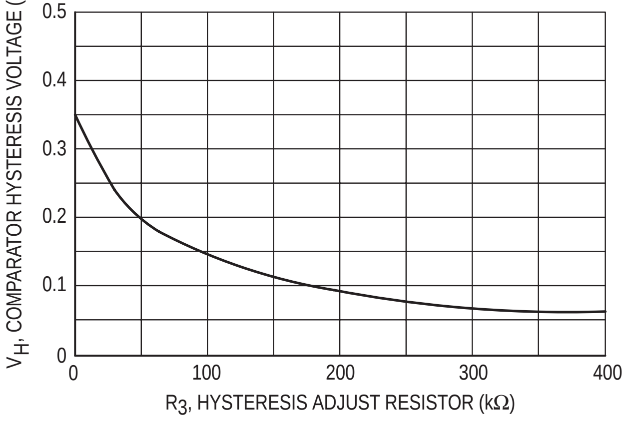


Figure 17. Comparator Hysteresis versus R_3



Voltage References

In Brief . . .

Motorola's line of precision voltage references is designed for applications requiring high initial accuracy, low temperature drift, and long term stability. Initial accuracies of ±1.0%, and ±2.0% mean production line adjustments can be eliminated. Temperature coefficients of 25 ppm/°C max (typically 10 ppm/°C) provide excellent stability. Uses for the references include D/A converters, A/D converters, precision power supplies, voltmeter systems, temperature monitors, and many others.

Precision Low Voltage References

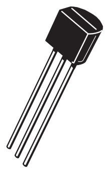
A family of precision low voltage bandgap reference devices designed for applications requiring low temperature drift.

1Precision Low Voltage References

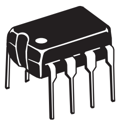
V_{out} (V) Typ	I_O (mA) Max	V_{out}/T ppm/°C Max	Device		Reg_{line} (mV) Max	Reg_{load} (mV) Max	Package
			0° to +70°C	**–40° to +85°C**			
1.235 ± 12 mV 1.235 ± 25 mV	20	80 Typ	LM385BZ–1.2 LM385Z–1.2	LM285Z–1.2	(Note 1)	1.0 (Note 2)	Z, D
2.5 ± 38 mV 2.5 ± 75 mV			LM385BZ–2.5 LM385Z–2.5	LM285Z–2.5		2.0 (Note 3)	
2.5 ± 25 mV	10	25	MC1403A	–	3.0/4.5 (Note 4)	10 (Note 5)	D
		40	MC1403				
5.0 ± 50 mV		40	MC1404P5	–	6.0 (Note 6)		P
6.25 ± 60 mV		40	MC1404P6	–			
10 ± 100 mV		40	MC1404P10	–			
2.5 to 37	100	50 Typ	TL431C, AC, BC	TL431I, AI, BI	Shunt Reference Dynamic Impedance (z) ≤ 0.5 Ω		LP, P, D, DM

Notes:
1. Micropower Reference Diode Dynamic Impedance (z) ≤ 1.0 Ω at I_R = 100 µA.
2. 10 µA ≤ I_R ≤ 1.0 mA.
3. 20 µA ≤ I_R ≤ 1.0 mA.
4. 4.5 V ≤ V_{in} ≤ 15 V/15 V ≤ V_{in} ≤ 40 V.
5. 0 mA ≤ I_L ≤ 10 mA.
6. (V_{out} + 2.5 V) ≤ V_{in} ≤ 40 V.

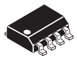
Voltage References Package Overview



CASE 29
LP, Z SUFFIX



CASE 626
P SUFFIX



CASE 751
D SUFFIX

CASE 846A
DM SUFFIX

Device Listing

Voltage References

MOTOROLA

LM285
LM385, B

Micropower Voltage Reference Diodes

MICROPOWER VOLTAGE REFERENCE DIODES

SEMICONDUCTOR TECHNICAL DATA

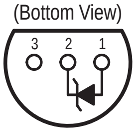
The LM285/LM385 series are micropower two–terminal bandgap voltage regulator diodes. Designed to operate over a wide current range of 10 µA to 20 mA, these devices feature exceptionally low dynamic impedance, low noise and stable operation over time and temperature. Tight voltage tolerances are achieved by on–chip trimming. The large dynamic operating range enables these devices to be used in applications with widely varying supplies with excellent regulation. Extremely low operating current make these devices ideal for micropower circuitry like portable instrumentation, regulators and other analog circuitry where extended battery life is required.

The LM285/LM385 series are packaged in a low cost TO–226AA plastic case and are available in two voltage versions of 1.235 and 2.500 V as denoted by the device suffix (see Ordering Information table). The LM285 is specified over a –40°C to +85°C temperature range while the LM385 is rated from 0°C to +70°C.

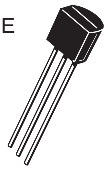
The LM385 is also available in a surface mount plastic package in voltages of 1.235 and 2.500 V.

- Operating Current from 10 µA to 20 mA
- 1.0%, 1.5%, 2.0% and 3.0% Initial Tolerance Grades
- Low Temperature Coefficient
- 1.0 Ω Dynamic Impedance
- Surface Mount Package Available

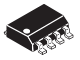
Z SUFFIX
PLASTIC PACKAGE
CASE 29

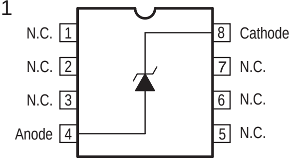


N.C.
Cathode
Anode

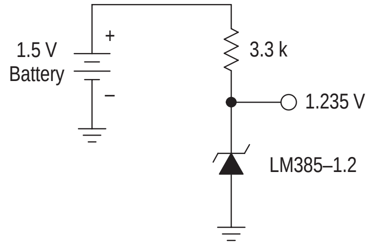


D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)





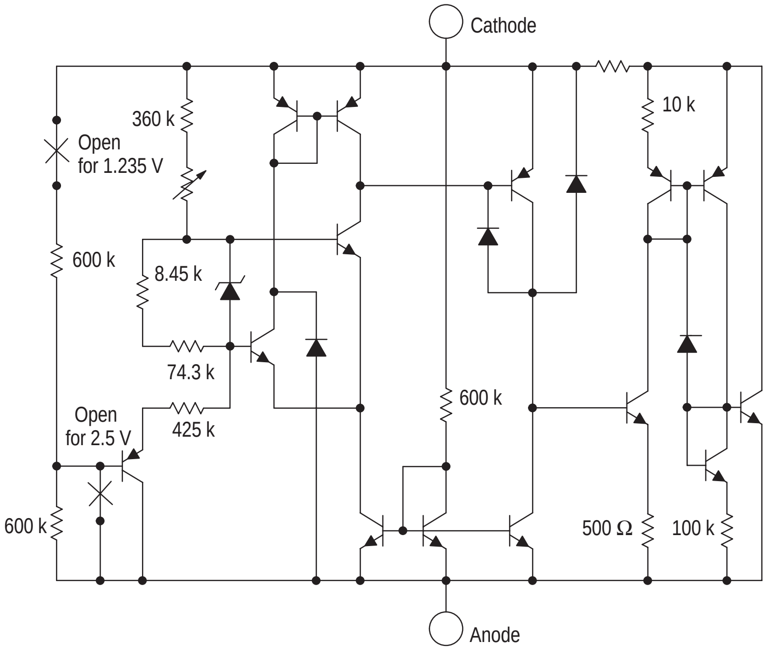
Standard Application



ORDERING INFORMATION

Device	Operating Temperature Range	Reverse Break–down Voltage	Tolerance
LM285D–1.2 LM285Z–1.2	T_A = –40° to +85°C	1.235 V	±1.0%
LM285D–2.5 LM285Z–2.5		2.500 V	±1.5%
LM385BD–1.2 LM385BZ–1.2	T_A = 0° to +70°C	1.235 V	±1.0%
LM385D–1.2 LM385Z–1.2		1.235 V	±2.0%
LM385BD–2.5 LM385BZ–2.5		2.500 V	±1.5%
LM385D–2.5 LM385Z–2.5		2.500 V	±3.0%

Representative Schematic Diagram



MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted)

Rating	Symbol	Value	Unit
Reverse Current	I_R	30	mA
Forward Current	I_F	10	mA
Operating Ambient Temperature Range LM285 LM385	T_A	 – 40 to + 85 0 to +70	°C
Operating Junction Temperature	T_J	+ 150	°C
Storage Temperature Range	T_{stg}	– 65 to + 150	°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C, unless otherwise noted)

Characteristic	Symbol	LM285–1.2			LM385–1.2/LM385B–1.2			Unit
		Min	Typ	Max	Min	Typ	Max	
Reverse Breakdown Voltage (I_{Rmin} ⩽ I_R ⩽ 20 mA) LM285–1.2/LM385B–1.2 $T_A = T_{low}$ to T_{high} (Note 1) LM385–1.2 $T_A = T_{low}$ to T_{high} (Note 1)	$V_{(BR)R}$	 1.223 1.200 – –	 1.235 – – –	 1.247 1.270 – –	 1.223 1.210 1.205 1.192	 1.235 – 1.235 –	 1.247 1.260 1.260 1.273	V
Minimum Operating Current T_A = 25°C $T_A = T_{low}$ to T_{high} (Note 1)	I_{Rmin}	 – –	 8.0 –	 10 20	 – –	 8.0 –	 15 20	µA
Reverse Breakdown Voltage Change with Current I_{Rmin} ⩽ I_R ⩽ 1.0 mA, T_A = +25°C $T_A = T_{low}$ to T_{high} (Note 1) 1.0 mA ⩽ I_R ⩽ 20 mA, T_A = +25°C $T_A = T_{low}$ to T_{high} (Note 1)	$\Delta V_{(BR)R}$	 – – – –	 – – – –	 1.0 1.5 10 20	 – – – –	 – – – –	 1.0 1.5 20 25	mV
Reverse Dynamic Impedance I_R = 100 µA, T_A = +25°C	Z		0.6	–	–	0.6	–	W
Average Temperature Coefficient 10 µA ⩽ I_R ⩽ 20 mA, $T_A = T_{low}$ to T_{high} (Note 1)	$\Delta V_{(BR)}/\Delta T$	–	80	–	–	80	–	ppm/°C
Wideband Noise (RMS) I_R = 100 µA, 10 Hz ⩽ f ⩽ 10 kHz	n	–	60	–	–	60	–	µV
Long Term Stability I_R = 100 µA, T_A = +25°C ± 0.1°C	S	–	20	–	–	20	–	ppm/ kHR

ELECTRICAL CHARACTERISTICS (T_A = 25°C, unless otherwise noted)

Characteristic	Symbol	LM285–2.5			LM385–2.5/LM385B–2.5			Unit
		Min	Typ	Max	Min	Typ	Max	
Reverse Breakdown Voltage ($I_{Rmin} \leqslant I_R \leqslant$ 20 mA)	$V_{(BR)R}$							V
LM285–2.5/LM385B–2.5		2.462	2.5	2.538	2.462	2.5	2.538	
$T_A = T_{low}$ to T_{high} (Note 1)		2.415	–	2.585	2.436	–	2.564	
LM385–2.5		–	–	–	2.425	2.5	2.575	
$T_A = T_{low}$ to T_{high} (Note 1)		–	–	–	2.400	–	2.600	
Minimum Operating Current	I_{Rmin}							µA
T_A = 25°C		–	13	20	–	13	20	
$T_A = T_{low}$ to T_{high} (Note 1)		–	–	30	–	–	30	
Reverse Breakdown Voltage Change with Current	$\Delta V_{(BR)R}$							mV
$I_{Rmin} \leqslant I_R \leqslant$ 1.0 mA, T_A = +25°C		–	–	1.0	–	–	2.0	
$T_A = T_{low}$ to T_{high} (Note 1)		–	–	1.5	–	–	2.5	
1.0 mA $\leqslant I_R \leqslant$ 20 mA, T_A = +25°C		–	–	10	–	–	20	
$T_A = T_{low}$ to T_{high} (Note 1)		–	–	20	–	–	25	
Reverse Dynamic Impedance I_R = 100 µA, T_A = +25°C	Z		0.6	–	–	0.6	–	W
Average Temperature Coefficient 20 µA $\leqslant I_R \leqslant$ 20 mA, $T_A = T_{low}$ to T_{high} (Note 1)	$\Delta V_{(BR)}/\Delta T$	–	80	–	–	80	–	ppm/°C
Wideband Noise (RMS) I_R = 100 µA, 10 Hz $\leqslant$ f $\leqslant$ 10 kHz	n	–	120	–	–	120	–	µV
Long Term Stability I_R = 100 µA, T_A = +25°C ± 0.1°C	S	–	20	–	–	20	–	ppm/ kHR

NOTES: 1. T_{low} = – 40°C for LM285–1.2, LM285–2.5
= 0°C for LM385–1.2, LM385B–1.2, LM385–2.5, LM385B–2.5

T_{high} = +85°C for LM285–1.2, LM285–2.5
= +70°C for LM385–1.2, LM385B–1.2, LM385–2.5, LM385B–2.5

TYPICAL PERFORMANCE CURVES FOR LM285–1.2/385–1.2/385B–1.2

Figure 1. Reverse Characteristics

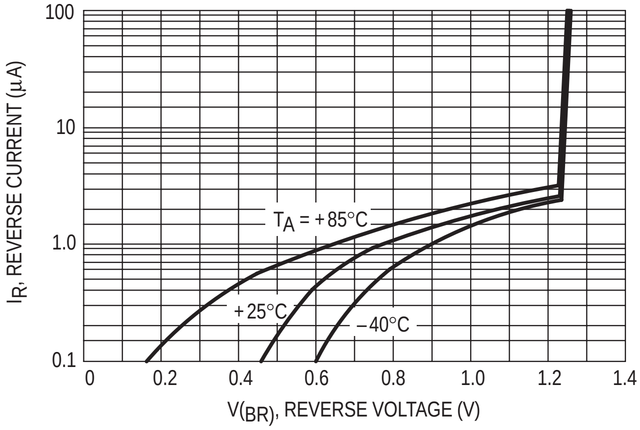


Figure 2. Reverse Characteristics

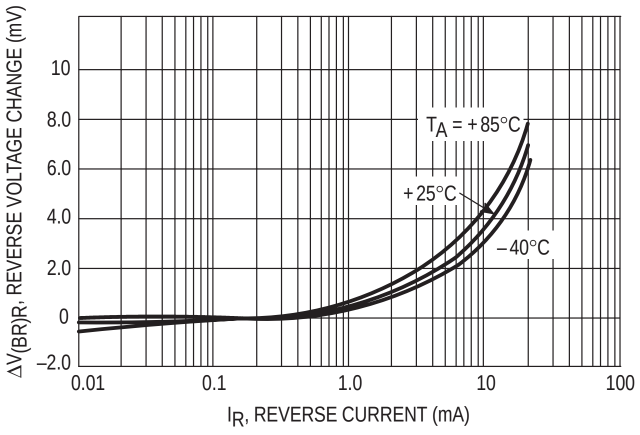


Figure 3. Forward Characteristics

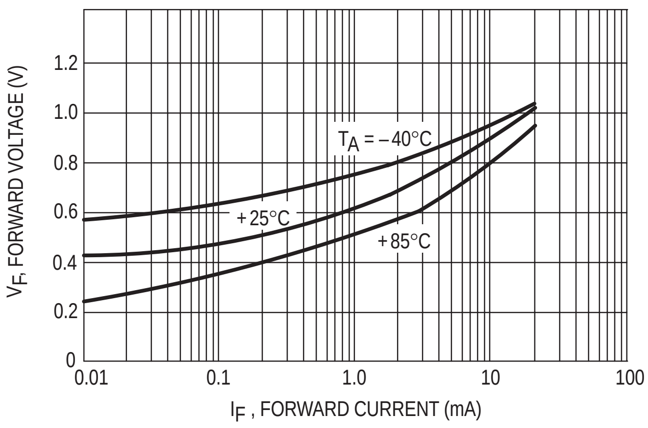


Figure 4. Temperature Drift

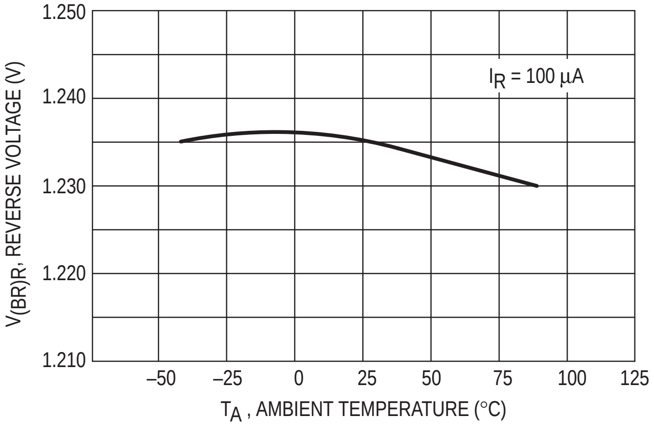


Figure 5. Noise Voltage

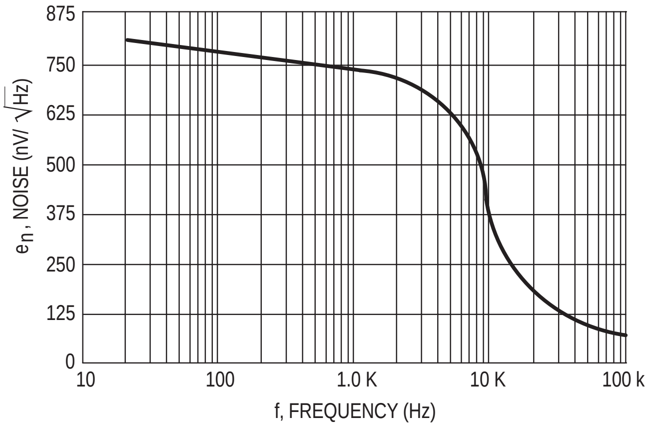
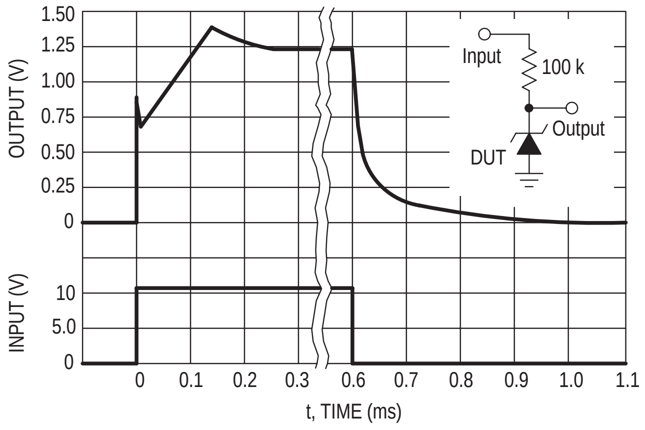


Figure 6. Response Time



TYPICAL PERFORMANCE CURVES FOR LM285–2.5/385–2.5/385B–2.5

Figure 7. Reverse Characteristics

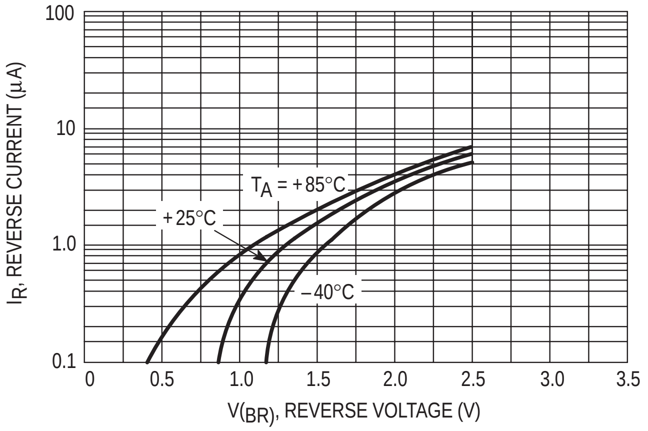


Figure 8. Reverse Characteristics

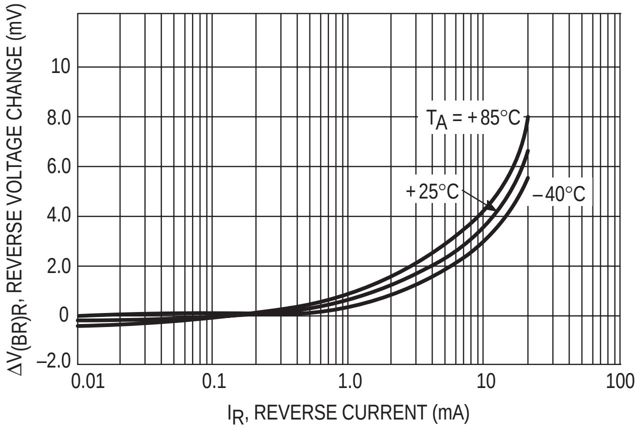


Figure 9. Forward Characteristics

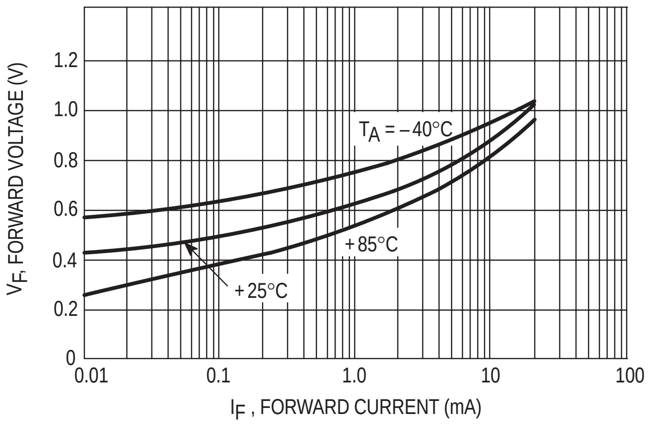


Figure 10. Temperature Drift

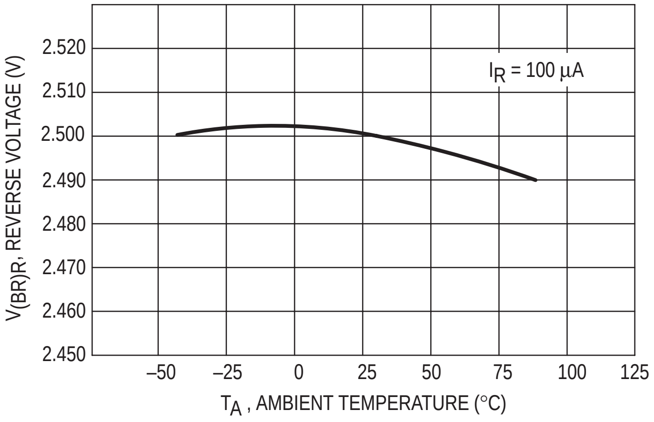


Figure 11. Noise Voltage

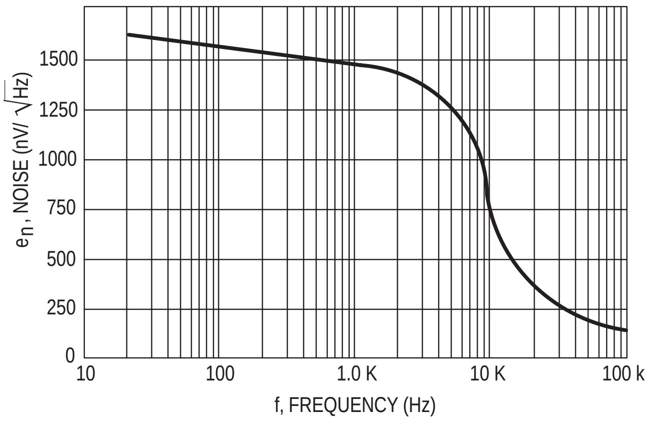
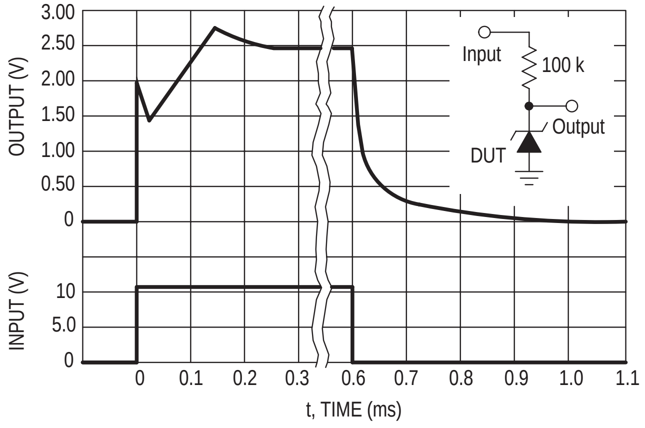


Figure 12. Response Time



MOTOROLA

MC1403, B

Low Voltage Reference

A precision band–gap voltage reference designed for critical instrumentation and D/A converter applications. This unit is designed to work with D/A converters, up to 12 bits in accuracy, or as a reference for power supply applications.

- Output Voltage: 2.5 V ± 25 mV
- Input Voltage Range: 4.5 V to 40 V
- Quiescent Current: 1.2 mA Typical
- Output Current: 10 mA
- Temperature Coefficient: 10 ppm/°C Typical
- Guaranteed Temperature Drift Specification
- Equivalent to AD580
- Standard 8–Pin DIP, and 8–Pin SOIC Package

Typical Applications

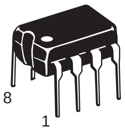
- Voltage Reference for 8 to 12 Bit D/A Converters
- Low T_C Zener Replacement
- High Stability Current Reference
- Voltmeter System Reference

MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted.)

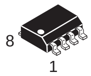
Rating	Symbol	Value	Unit
Input Voltage	V_I	40	V
Storage Temperature	T_{stg}	–65 to 150	°C
Junction Temperature	T_J	+175	°C
Operating Ambient Temperature Range MC1403B MC1403	T_A	–40 to +85 0 to +70	°C °C

PRECISION LOW VOLTAGE REFERENCE

SEMICONDUCTOR TECHNICAL DATA

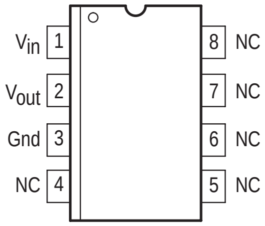


P1 SUFFIX
PLASTIC PACKAGE
CASE 626



D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

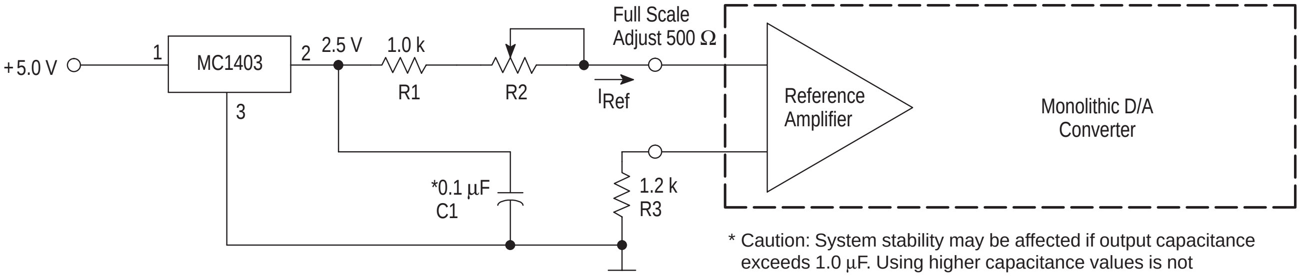
PIN CONNECTIONS



ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC1403D	T_A = 0° to +70°C	SO–8
MC1403P1		Plastic DIP
MC1403BD	T_A = –40° to +85°C	SO–8
MC1403BP1		Plastic DIP

Figure 1. A Reference for Monolithic D/A Converters



* Caution: System stability may be affected if output capacitance exceeds 1.0 µF. Using higher capacitance values is not recommended and should be carefully considered.

Providing the Reference Current for Motorola Monolithic D/A Converters

The MC1403 makes an ideal reference for many monolithic D/A converters, requiring a stable current reference of nominally 2.0 mA. This can be easily obtained from the MC1403 with the addition of a series resistor, R1. A variable resistor, R2, is recommended to provide means for full–scale adjust on the D/A converter.

The resistor R3 improves temperature performance by matching the impedance on both inputs of the D/A reference amplifier. The capacitor decouples any noise present on the reference line. It is essential if the D/A converter is located any appreciable distance from the reference.

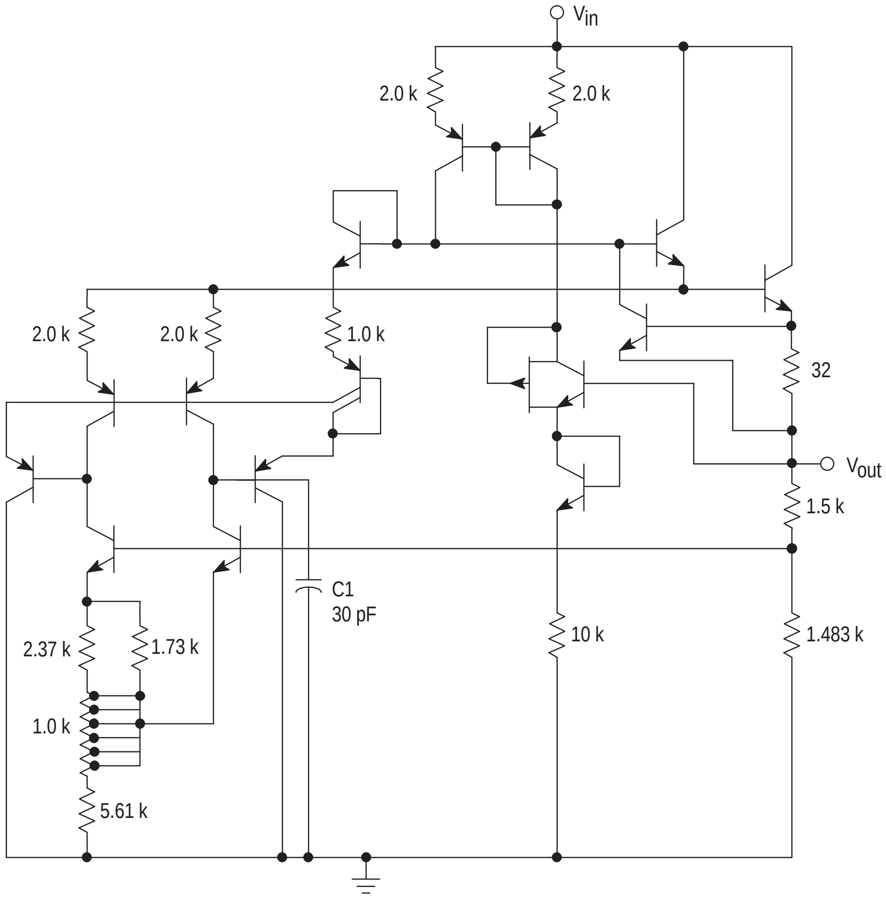
A single MC1403 reference can provide the required current input for up to five of the monolithic D/A converters.

ELECTRICAL CHARACTERISTICS (V_{in} = 15 V, T_A = 25°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (I_O = 0 mA)	V_{out}	2.475	2.5	2.525	V
Temperature Coefficient of Output Voltage* MC1403	$\Delta V_O/\Delta T$	–	10	40	ppm/°C
Output Voltage Change* (Over specified temperature range)	ΔV_O				mV
MC1403 0 to +70°C		–	–	7.0	
MC1403B –40 to +85°C		–	–	12.5	
Line Regulation (I_O = 0 mA)	Reg_{line}				mV
($15\ V \leqslant V_I \leqslant 40\ V$)		–	1.2	4.5	
($4.5\ V \leqslant V_I \leqslant 15\ V$)		–	0.6	3.0	
Load Regulation (0 mA < I_O < 10 mA)	Reg_{load}	–	–	10	mV
Quiescent Current (I_O = 0 mA)	I_Q	–	1.2	1.5	mA

* This test is not applicable to the MC1403D or MC1403BD surface mount devices.

Figure 2. MC1403, B Schematic



This device contains 15 active transistors.

Figure 3. Typical Change in V_{out} versus V_{in}

(Normalized to V_{in} = 15 V @ T_C = 25°C)

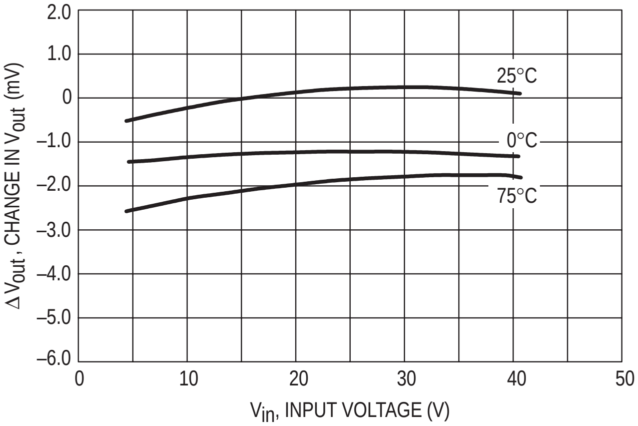


Figure 4. Change in Output Voltage versus Load Current

(Normalized to V_{out} @ V_{in} = 15 V, I_{out} = 0 mA)

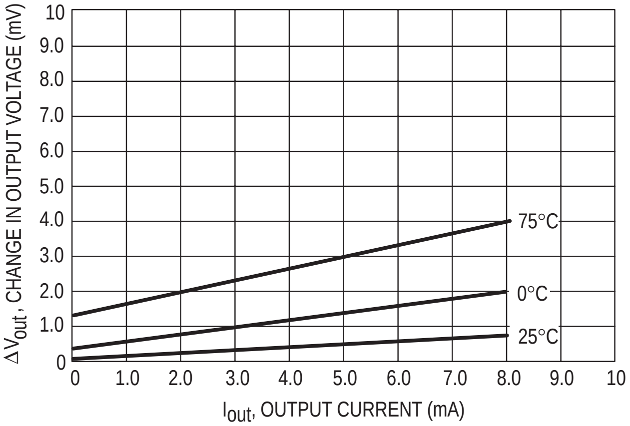


Figure 5. Quiescent Current versus Temperature

(V_{in} = 15 V, I_{out} = 0 mA)

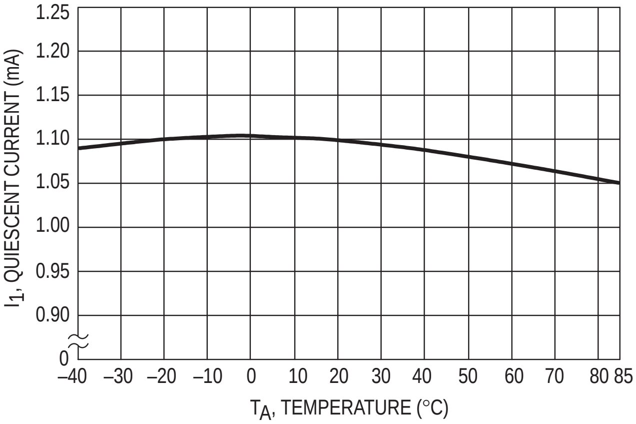


Figure 6. Change in V_{out} versus Temperature

(Normalized to V_{out} @ V_{in} = 15 V)

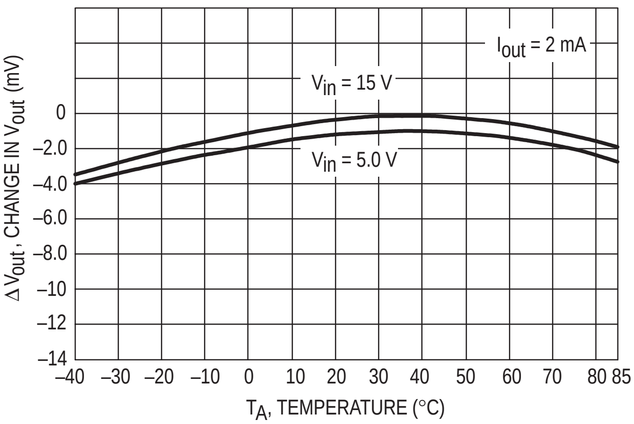
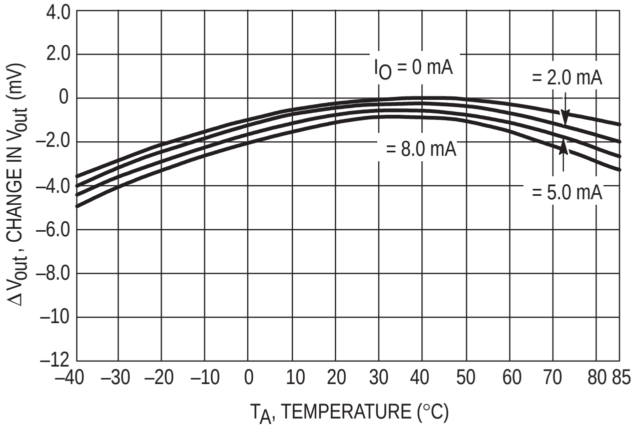


Figure 7. Change in V_{out} versus Temperature

(Normalized to T_A = 25°C, V_{in} = 15 V, I_{out} = 0 mA)



3–1/2–Digit Voltmeter – Common Anode Displays, Flashing Overrange

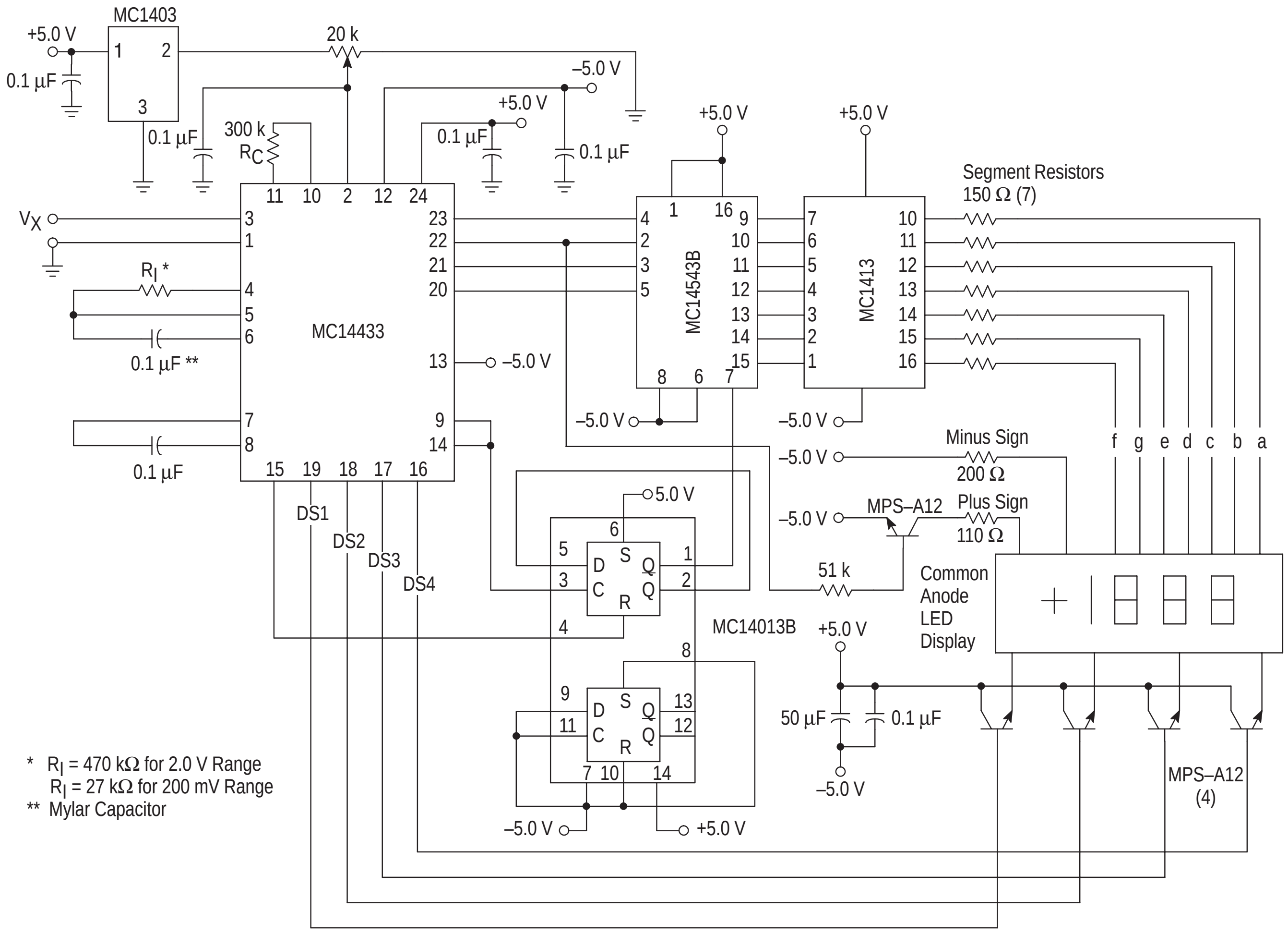
An example of a 3–1/2–digit voltmeter using the MC14433 is shown in the circuit diagram of Figure 8. The reference voltage for the system uses an MC1403 2.5 V reference IC. The full scale potentiometer can calibrate for a full scale of 199.9 mV or 1.999 V. When switching from 2.0 V to 200 mV operation, R_I is also changed, as shown on the diagram.

When using R_C equal to 300 kΩ, the clock frequency for the system is about 66 kHz. The resulting conversion time is approximately 250 ms.

When the input is overrange, the display flashes on and off. The flashing rate is one–half the conversion rate. This is done by dividing the EOC pulse rate by 2 with 1/2 MC14013B flip–flop and blanking the display using the blanking input of the MC14543B.

The display uses an LED display with common anode digit lines driven with an MC14543B decoder and an MC1413 LED driver. The MC1413 contains 7 Darlington transistor drivers and resistors to drive the segments of the display. The digit drive is provided by four MPS–A12 Darlington transistors operating in an emitter–follower configuration. The MC14543B, MC14013B and LED displays are referenced to V_{EE} via Pin 13 of the MC14433. This places the full power supply voltage across the display. The current for the display may be adjusted by the value of the segment resistors shown as 150 Ω in Figure 8.

Figure 8. 3–1/2–Digit Voltmeter



MOTOROLA

MC1404

Voltage Reference Family

The MC1404 of ICs is a family of temperature–compensated voltage references for precision data conversion applications, such as A/D, D/A, V/F, and F/V. Advances in laser–trimming and ion–implanted devices, as well as monolithic fabrication techniques, make these devices stable and accurate to 12 bits over both military and commercial temperature ranges. In addition to excellent temperature stability, these parts offer excellent long–term stability and low noise.

- Output Voltages: Standard, 5.0 V, 6.25 V, 10 V
- Trimmable Output: > ± 6%
- Wide Input Voltage Range: V_{ref} + 2.5 V to 40 V
- Low Quiescent Current: 1.25 mA Typical
- Temperature Coefficient: 10 ppm/°C Typical
- Low Output Noise: 12 µV p–p Typical
- Excellent Ripple Rejection: > 80 dB Typical

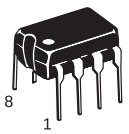
Typical Applications

- Voltage Reference for 8 to 12 Bit D/A Converters
- Low T_C Zener Replacement
- High Stability Current Reference
- MPU D/A and A/D Applications

PRECISION LOW DRIFT VOLTAGE REFERENCES

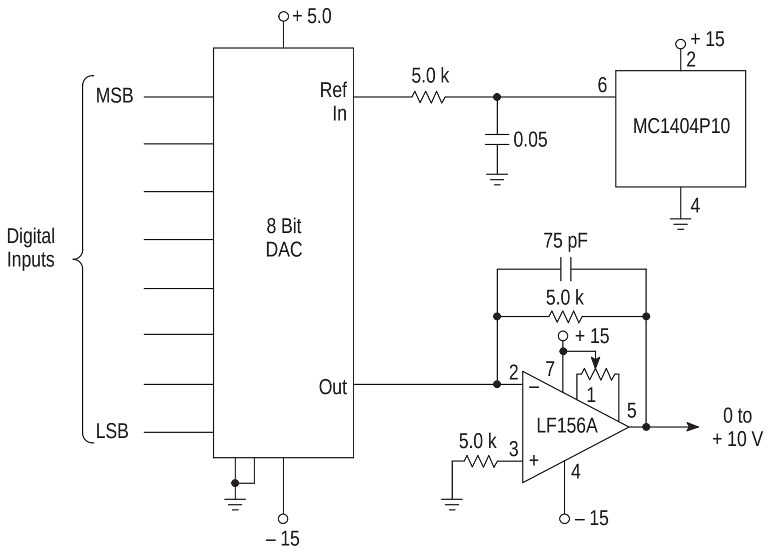
5.0, 6.25, and 10–VOLT OUTPUT VOLTAGES

SEMICONDUCTOR TECHNICAL DATA

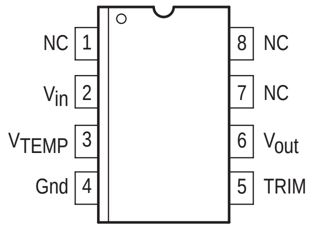


P SUFFIX
PLASTIC PACKAGE
CASE 626

Figure 1. Voltage Output 8–Bit DAC Using MC1404P10



PIN CONNECTIONS



ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC1404P5	T_A = 0° to +70°C	Plastic DIP
MC1404P6		Plastic DIP
MC1404P10		Plastic DIP

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage	V_{in}	40	V
Storage Temperature	T_{stg}	– 65 to + 150	°C
Junction Temperature	T_J	+ 175	°C
Operating Ambient Temperature Range	T_A	0 to + 70	°C

ELECTRICAL CHARACTERISTICS (V_{in} = 15 V, T_A = 25°C, and Trim Terminal not connected, unless otherwise noted.)

Characteristic		Symbol	Min	Typ	Max	Unit
Output Voltage		V_O				V
(I_O = 0 mA)	MC1404P5		4.95	5.0	5.05	
	MC1404P6		6.19	6.25	6.31	
	MC1404P10		9.9	10	10.1	
Output Voltage Tolerance		–	–	± 0.1	± 1.0	%
Output Trim Range (Figure 10) (R_P = 100 kΩ)		ΔV_{TRIM}	± 6.0	–	–	%
Output Voltage Temperature Coefficient, Over Full Temperature Range		$\Delta V_O/\Delta T$	–	10	40	ppm/°C
Maximum Output Voltage Change		ΔV_O				mV
Over Temperature Range	MC1404P5		–	–	14	
	MC1404P6		–	–	17.5	
	MC1404P10		–	–	28	
Line Regulation (Note 1) ($V_{in} = V_{out}$ + 2.5 V to 40 V, I_{out} = 0 mA)		Reg_{line}	–	2.0	6.0	mV
Load Regulation (Note 1) ($0 \leqslant I_O \leqslant 10$ mA)		Reg_{load}	–	–	10	mV
Quiescent Current (I_O = 0 mA)		I_Q	–	1.2	1.5	mA
Short Circuit Current		I_{sc}	–	20	45	mA
Long Term Stability		–	–	25	–	ppm/1000 hrs

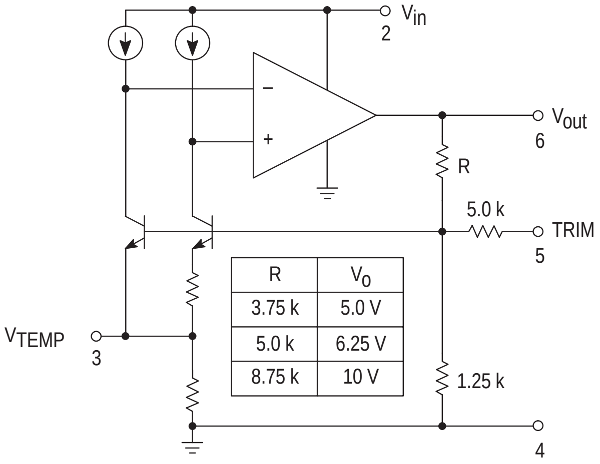
NOTE: 1. Includes thermal effects.

DYNAMIC CHARACTERISTICS (V_{in} = 15 V, T_A = 25°C, all voltage ranges, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Turn–On Settling Time (to ± 0.01%)	t_S	–	50	–	µs
Output Noise Voltage – P to P (Bandwidth 0.1 to 10 Hz)	V_n	–	12	–	µV
Small–Signal Output Impedance	r_o				Ω
120 Hz		–	0.15	–	
500 Hz		–	0.2	–	
Power Supply Rejection Ratio	PSRR	70	80	–	dB

TYPICAL CHARACTERISTICS

Figure 2. Simplified Device Diagram



R	V_O
3.75 k	5.0 V
5.0 k	6.25 V
8.75 k	10 V

Figure 3. Line Regulation versus Temperature

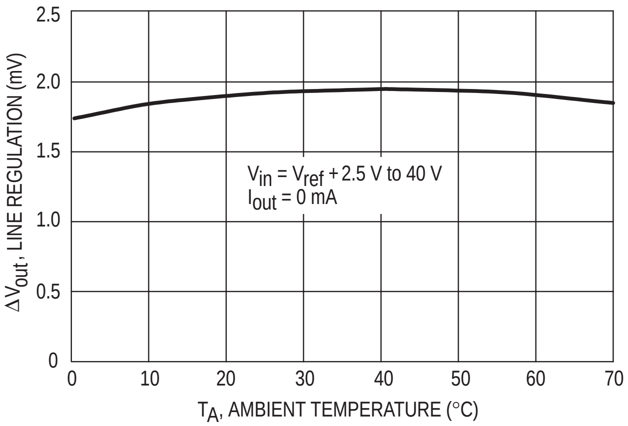


Figure 4. Output Voltage versus Temperature MC1404P10

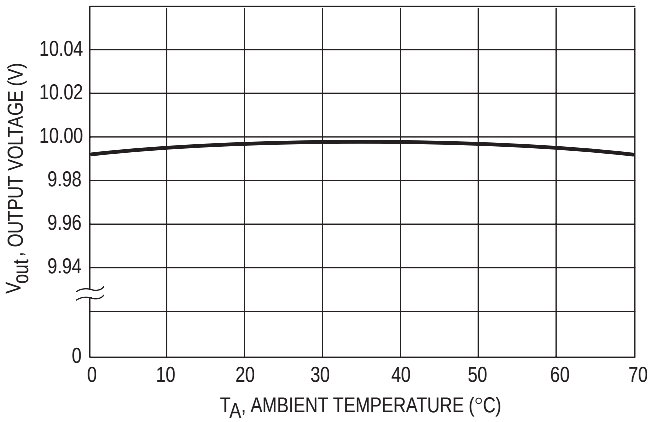


Figure 5. Load Regulation versus Temperature

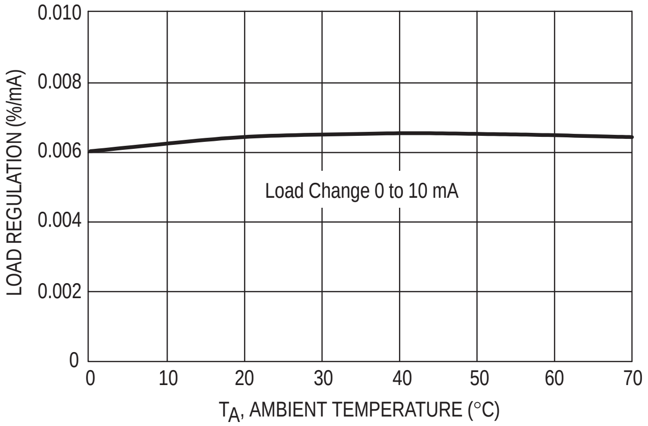


Figure 6. Power Supply Rejection Ratio versus Frequency

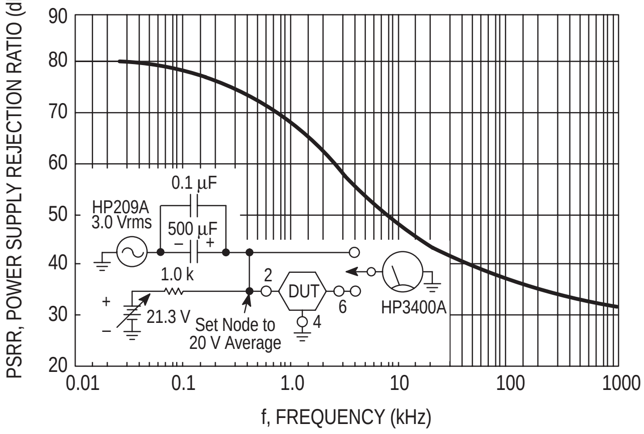


Figure 7. Quiescent Current versus Temperature

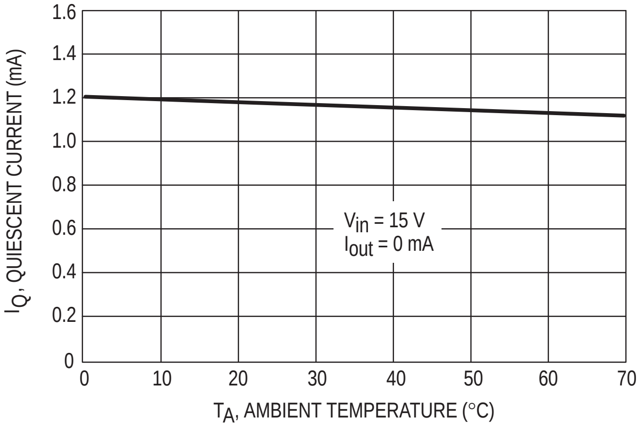


Figure 8. Short Circuit Current versus Temperature

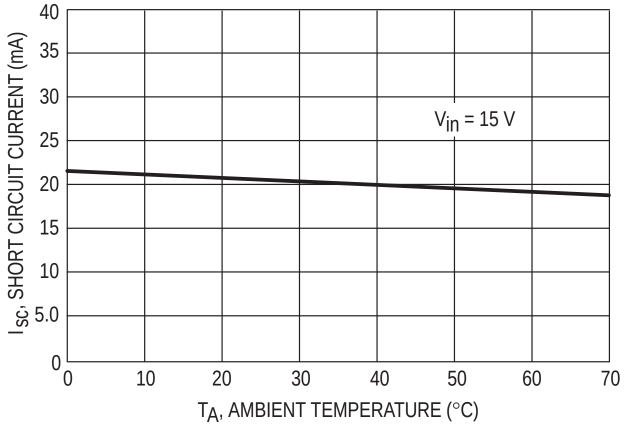


Figure 9. V_{TEMP} Output versus Temperature

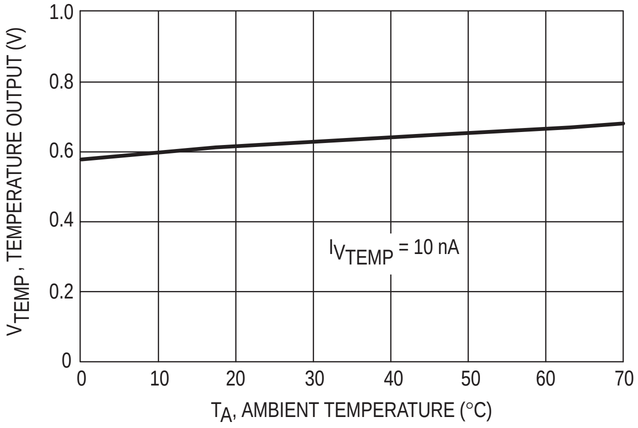
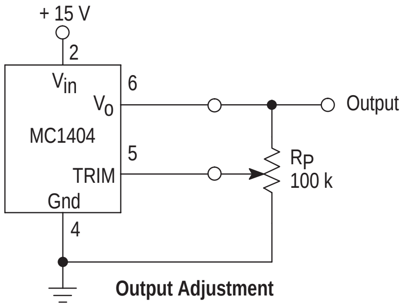


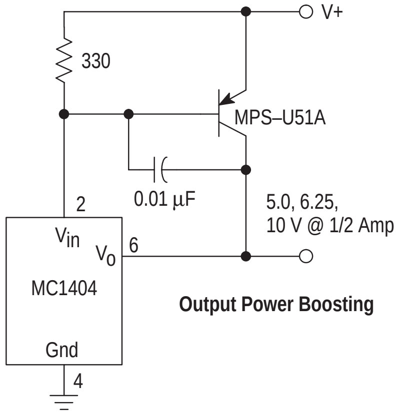
Figure 10. Output Trim Configuration



The MC1404 trim terminal can be used to adjust the output voltage over a ± 6.0% range. For example, the output can be set to 10.000 V or to 10.240 V for binary applications. For trimming, Bourns type 3059, 100 kΩ or 200 kΩ trimpot is recommended.

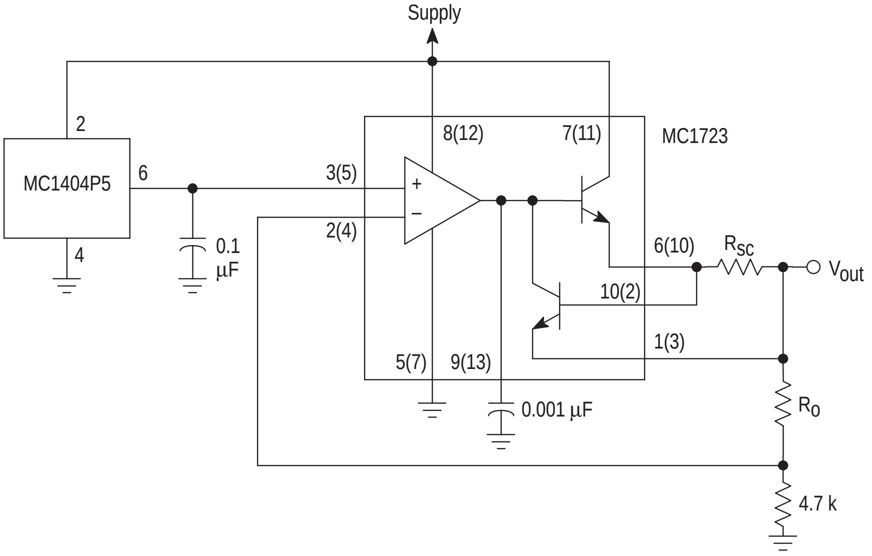
Although Figure 10 illustrates a wide trim range, temperature coefficients may become unpredictable for trim > ± 6.0%.

Figure 11. Precision Supply Using MC1404



The addition of a power transistor, a resistor, and a capacitor converts the MC1404 into a precision supply with one ampere current capability. At V+ = 15 V, the MC1404 can carry in excess of 14 mA of load current with good regulation. If the power transistor current gain exceeds 75, a one ampere supply can be realized.

Figure 12. Ultra Stable Reference for MC1723 Voltage Regulator



$$V_{out} = 5.0\ V\left(\frac{R_O + 4.7\ k}{4.7\ k}\right)$$

$$I_{omax} \approx \frac{0.6\ V}{R_{SC}}$$

Figure 13. 5.0 V, 6.0 Amp, 25 kHz Switching Regulator with Separate Ultra–Stable Reference

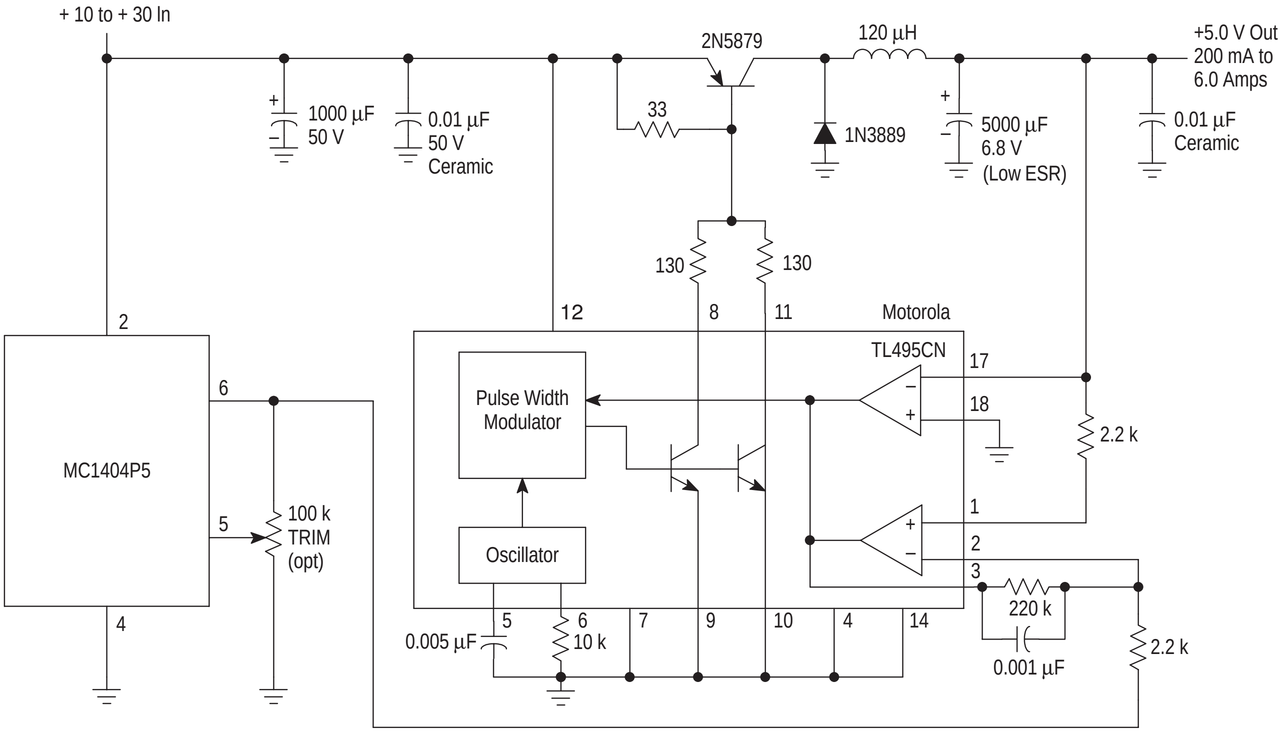
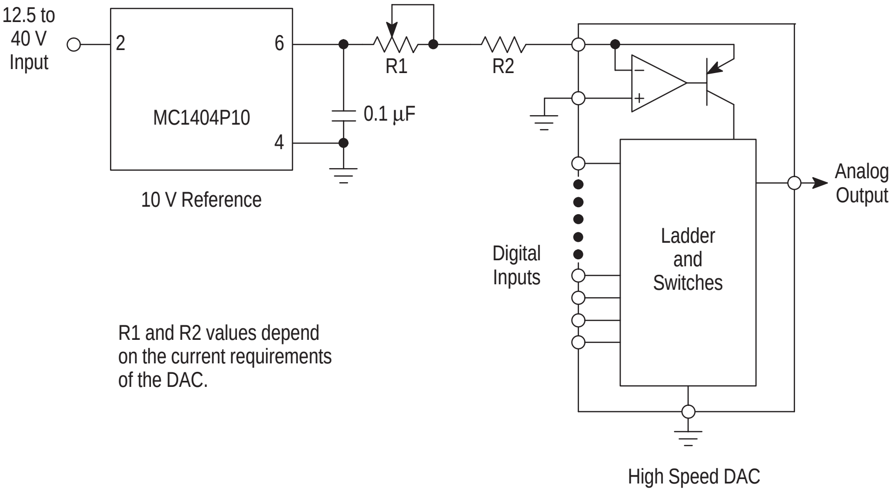


Figure 14. Reference for a High Speed DAC



R1 and R2 values depend on the current requirements of the DAC.

MOTOROLA

TL431, A, B
Series

Programmable Precision References

The TL431, A, B integrated circuits are three–terminal programmable shunt regulator diodes. These monolithic IC voltage references operate as a low temperature coefficient zener which is programmable from V_{ref} to 36 V with two external resistors. These devices exhibit a wide operating current range of 1.0 mA to 100 mA with a typical dynamic impedance of 0.22 Ω. The characteristics of these references make them excellent replacements for zener diodes in many applications such as digital voltmeters, power supplies, and op amp circuitry. The 2.5 V reference makes it convenient to obtain a stable reference from 5.0 V logic supplies, and since the TL431, A, B operates as a shunt regulator, it can be used as either a positive or negative voltage reference.

- Programmable Output Voltage to 36 V
- Voltage Reference Tolerance: ±0.4%, Typ @ 25°C (TL431B)
- Low Dynamic Output Impedance, 0.22 Ω Typical
- Sink Current Capability of 1.0 mA to 100 mA
- Equivalent Full–Range Temperature Coefficient of 50 ppm/°C Typical
- Temperature Compensated for Operation over Full Rated Operating Temperature Range
- Low Output Noise Voltage

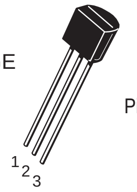
ORDERING INFORMATION

Device	Operating Temperature Range	Package
TL431CLP, ACLP, BCLP	T_A = 0° to +70°C	TO–92
TL431CP, ACP, BCP		Plastic
TL431CDM, ACDM, BCDM		Micro–8
TL431CD, ACD, BCD		SOP–8
TL431ILP, AILP, BILP	T_A = –40° to +85°C	TO–92
TL431IP, AIP, BIP		Plastic
TL431IDM, AIDM, BIDM		Micro–8
TL431ID, AID, BID		SOP–8

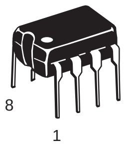
PROGRAMMABLE PRECISION REFERENCES

SEMICONDUCTOR TECHNICAL DATA

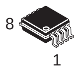
Z, LP SUFFIX
PLASTIC PACKAGE
CASE 29
(TO–92)



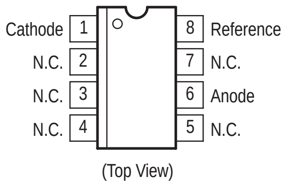
Pin 1. Reference
2. Anode
3. Cathode



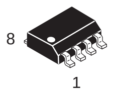
P SUFFIX
PLASTIC PACKAGE
CASE 626

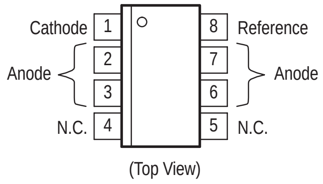


DM SUFFIX
PLASTIC PACKAGE
CASE 846A
(Micro–8)



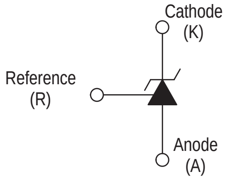
D SUFFIX
PLASTIC PACKAGE
CASE 751
(SOP–8)



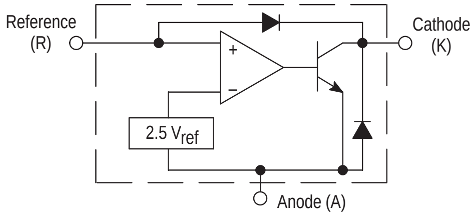


SOP–8 is an internally modified SO–8 package. Pins 2, 3, 6 and 7 are electrically common to the die attach flag. This internal lead frame modification decreases power dissipation capability when appropriately mounted on a printed circuit board. SOP–8 conforms to all external dimensions of the standard SO–8 package.

Symbol

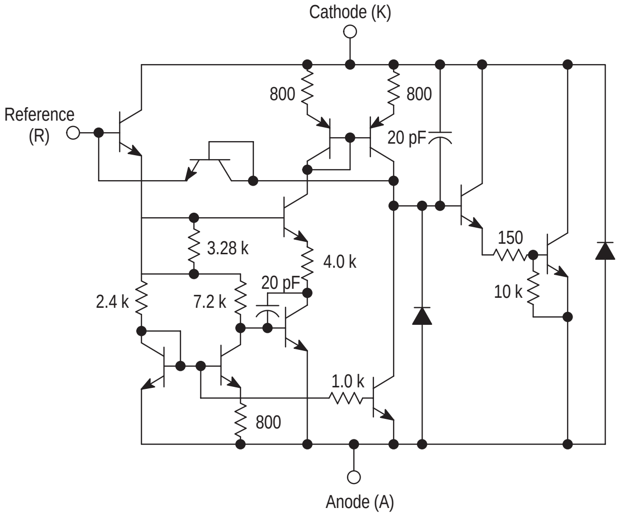


Representative Block Diagram



Representative Schematic Diagram

Component values are nominal



This device contains 12 active transistors.

MAXIMUM RATINGS (Full operating ambient temperature range applies, unless otherwise noted.)

Rating	Symbol	Value	Unit
Cathode to Anode Voltage	V_{KA}	37	V
Cathode Current Range, Continuous	I_K	–100 to +150	mA
Reference Input Current Range, Continuous	I_{ref}	–0.05 to +10	mA
Operating Junction Temperature	T_J	150	°C
Operating Ambient Temperature Range TL431I, TL431AI, TL431BI TL431C, TL431AC, TL431BC	T_A	 –40 to +85 0 to +70	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Total Power Dissipation @ T_A = 25°C Derate above 25°C Ambient Temperature D, LP Suffix Plastic Package P Suffix Plastic Package DM Suffix Plastic Package	P_D	 0.70 1.10 0.52	W
Total Power Dissipation @ T_C = 25°C Derate above 25°C Case Temperature D, LP Suffix Plastic Package P Suffix Plastic Package	P_D	 1.5 3.0	W

NOTE: ESD data available upon request.

RECOMMENDED OPERATING CONDITIONS

Condition	Symbol	Min	Max	Unit
Cathode to Anode Voltage	V_{KA}	V_{ref}	36	V
Cathode Current	I_K	1.0	100	mA

THERMAL CHARACTERISTICS

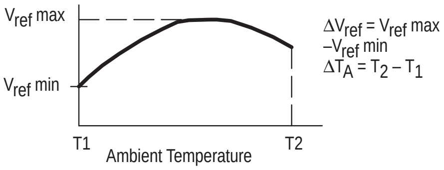
Characteristic	Symbol	D, LP Suffix Package	P Suffix Package	DM Suffix Package	Unit
Thermal Resistance, Junction–to–Ambient	$R_{\theta JA}$	178	114	240	°C/W
Thermal Resistance, Junction–to–Case	$R_{\theta JC}$	83	41	–	°C/W

ELECTRICAL CHARACTERISTICS (T_A = 25°C, unless otherwise noted.)

Characteristic	Symbol	TL431I			TL431C			Unit
		Min	Typ	Max	Min	Typ	Max	
Reference Input Voltage (Figure 1)	V_{ref}							V
$V_{KA} = V_{ref}$, I_K = 10 mA								
T_A = 25°C		2.44	2.495	2.55	2.44	2.495	2.55	
$T_A = T_{low}$ to T_{high} (Note 1)		2.41	–	2.58	2.423	–	2.567	
Reference Input Voltage Deviation Over Temperature Range (Figure 1, Notes 1, 2, 4) $V_{KA} = V_{ref}$, I_K = 10 mA	ΔV_{ref}	–	7.0	30	–	3.0	17	mV
Ratio of Change in Reference Input Voltage to Change in Cathode to Anode Voltage	$\frac{\Delta V_{ref}}{\Delta V_{KA}}$							mV/V
I_K = 10 mA (Figure 2), ΔV_{KA} = 10 V to V_{ref}		–	–1.4	–2.7	–	–1.4	–2.7	
ΔV_{KA} = 36 V to 10 V		–	–1.0	–2.0	–	–1.0	–2.0	
Reference Input Current (Figure 2)	I_{ref}							µA
I_K = 10 mA, R1 = 10 k, R2 = ∞								
T_A = 25°C		–	1.8	4.0	–	1.8	4.0	
$T_A = T_{low}$ to T_{high} (Note 1)		–	–	6.5	–	–	5.2	
Reference Input Current Deviation Over Temperature Range (Figure 2, Note 1, 4) I_K = 10 mA, R1 = 10 k, R2 = ∞	ΔI_{ref}	–	0.8	2.5	–	0.4	1.2	µA
Minimum Cathode Current For Regulation $V_{KA} = V_{ref}$ (Figure 1)	I_{min}	–	0.5	1.0	–	0.5	1.0	mA
Off–State Cathode Current (Figure 3) V_{KA} = 36 V, V_{ref} = 0 V	I_{off}	–	2.6	1000	–	2.6	1000	nA
Dynamic Impedance (Figure 1, Note 3) $V_{KA} = V_{ref}$, ΔI_K = 1.0 mA to 100 mA f ≤ 1.0 kHz	$\lvert Z_{KA}\rvert$	–	0.22	0.5	–	0.22	0.5	Ω

NOTE 1: T_{low} = –40°C for TL431AIP TL431AILP, TL431IP, TL431ILP, TL431BID, TL431BIP, TL431BILP, TL431AIDM, TL431IDM, TL431BIDM
= 0°C for TL431ACP, TL431ACLP, TL431CP, TL431CLP, TL431CD, TL431ACD, TL431BCD, TL431BCP, TL431BCLP, TL431CDM, TL431ACDM, TL431BCDM
T_{high} = +85°C for TL431AIP, TL431AILP, TL431IP, TL431ILP, TL431BID, TL431BIP, TL431BILP, TL431IDM, TL431AIDM, TL431BIDM
= +70°C for TL431ACP, TL431ACLP, TL431CP, TL431ACD, TL431BCD, TL431BCP, TL431BCLP, TL431CDM, TL431ACDM, TL431BCDM

NOTE 2: The deviation parameter ΔV_{ref} is defined as the difference between the maximum and minimum values obtained over the full operating ambient temperature range that applies.



The average temperature coefficient of the reference input voltage, αV_{ref} is defined as:

$$V_{ref}\,\frac{ppm}{°C} = \frac{\left(\frac{\Delta V_{ref}}{V_{ref}\ @\ 25°C}\right) X\ 10^6}{\Delta T_A} = \frac{\Delta V_{ref} \times 10^6}{\Delta T_A (V_{ref}\ @\ 25°C)}$$

αV_{ref} can be positive or negative depending on whether V_{ref} Min or V_{ref} Max occurs at the lower ambient temperature. (Refer to Figure 6.)

Example : ΔV_{ref} = 8.0 mV and slope is positive,

V_{ref} @ 25°C = 2.495 V, ΔT_A = 70°C $\qquad \alpha V_{ref} = \frac{0.008 \times 10^6}{70\ (2.495)} = 45.8$ ppm/°C

NOTE 3 : The dynamic impedance Z_{KA} is defined as $\lvert Z_{KA}\rvert = \frac{\Delta V_{KA}}{\Delta I_K}$

When the device is programmed with two external resistors, R1 and R2, (refer to Figure 2) the total dynamic impedance of the circuit is defined as:

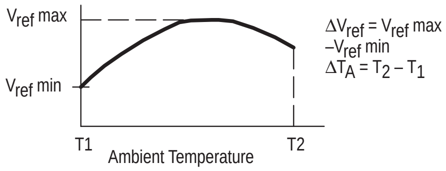
$$\lvert Z_{KA}'\rvert \approx \lvert Z_{KA}\rvert \left(1 + \frac{R1}{R2}\right)$$

ELECTRICAL CHARACTERISTICS (T_A = 25°C, unless otherwise noted.)

Characteristic	Symbol	TL431AI			TL431AC			TL431B			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Reference Input Voltage (Figure 1) $V_{KA} = V_{ref}$, I_K = 10 mA	V_{ref}										V
T_A = 25°C		2.47	2.495	2.52	2.47	2.495	2.52	2.483	2.495	2.507	
$T_A = T_{low}$ to T_{high}		2.44	–	2.55	2.453	–	2.537	2.475	2.495	2.515	
Reference Input Voltage Deviation Over Temperature Range (Figure 1, Notes 1, 2, 4) $V_{KA} = V_{ref}$, I_K = 10 mA	ΔV_{ref}	–	7.0	30	–	3.0	17	–	3	17	mV
Ratio of Change in Reference Input Voltage to Change in Cathode to Anode Voltage	$\frac{\Delta V_{ref}}{\Delta V_{KA}}$										mV/V
I_K = 10 mA (Figure 2), ΔV_{KA} = 10 V to V_{ref}		–	–1.4	–2.7	–	–1.4	–2.7	–	–1.4	–2.7	
ΔV_{KA} = 36 V to 10 V		–	–1.0	–2.0	–	–1.0	–2.0	–	–1.0	–2.0	
Reference Input Current (Figure 2) I_K = 10 mA, R1 = 10 k, R2 = ∞	ΔI_{ref}										µA
T_A = 25°C		–	1.8	4.0	–	1.8	4.0	–	1.6	3.0	
$T_A = T_{low}$ to T_{high} (Note 1)		–	–	6.5	–	–	5.2	–	–	4.0	
Reference Input Current Deviation Over Temperature Range (Figure 2, Note 1) I_K = 10 mA, R1 = 10 k, R2 = ∞	ΔI_{ref}	–	0.8	2.5	–	0.4	1.2	–	0.4	1.2	µA
Minimum Cathode Current For Regulation $V_{KA} = V_{ref}$ (Figure 1)	I_{min}	–	0.5	1.0	–	0.5	1.0	–	0.5	1.0	mA
Off–State Cathode Current (Figure 3) V_{KA} = 36 V, V_{ref} = 0 V	I_{off}	–	260	1000	–	260	1000	–	230	500	nA
Dynamic Impedance (Figure 1, Note 3) $V_{KA} = V_{ref}$, ΔI_K = 1.0 mA to 100 mA f ≤ 1.0 kHz	$\|Z_{KA}\|$	–	0.22	0.5	–	0.22	0.5	–	0.14	0.3	Ω

NOTE 1: T_{low} = –40°C for TL431AIP TL431AILP, TL431IP, TL431ILP, TL431BID, TL431BIP, TL431BILP, TL431AIDM, TL431IDM, TL431BIDM
= 0°C for TL431ACP, TL431ACLP, TL431CP, TL431CLP, TL431CD, TL431ACD, TL431BCD, TL431BCP, TL431BCLP, TL431CDM, TL431ACDM, TL431BCDM
T_{high} = +85°C for TL431AIP, TL431AILP, TL431IP, TL431ILP, TL431BID, TL431BIP, TL431BILP, TL431IDM, TL431AIDM, TL431BIDM
= +70°C for TL431ACP, TL431ACLP, TL431CP, TL431ACD, TL431BCD, TL431BCP, TL431BCLP, TL431CDM, TL431ACDM, TL431BCDM

NOTE 2: The deviation parameter ΔV_{ref} is defined as the difference between the maximum and minimum values obtained over the full operating ambient temperature range that applies.



The average temperature coefficient of the reference input voltage, αV_{ref} is defined as:

$$V_{ref}\ \frac{ppm}{°C} = \frac{\left(\dfrac{\Delta V_{ref}}{V_{ref}\ @\ 25°C}\right) \times 10^6}{\Delta T_A} = \frac{\Delta V_{ref} \times 10^6}{\Delta T_A\ (V_{ref}\ @\ 25°C)}$$

αV_{ref} can be positive or negative depending on whether V_{ref} Min or V_{ref} Max occurs at the lower ambient temperature. (Refer to Figure 6.)

Example : ΔV_{ref} = 8.0 mV and slope is positive,

V_{ref} @ 25°C = 2.495 V, ΔT_A = 70°C $\qquad \alpha V_{ref} = \frac{0.008 \times 10^6}{70\ (2.495)} = 45.8$ ppm/°C

NOTE 3 : The dynamic impedance Z_{KA} is defined as $|Z_{KA}| = \frac{\Delta V_{KA}}{\Delta I_K}$

When the device is programmed with two external resistors, R1 and R2, (refer to Figure 2) the total dynamic impedance of the circuit is defined as:

$$|Z_{KA}'| \approx |Z_{KA}| \left(1 + \frac{R1}{R2}\right)$$

NOTE 4: This test is not applicable to surface mount (D and DM suffix) devices.

Figure 1. Test Circuit for $V_{KA} = V_{ref}$

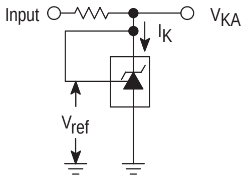
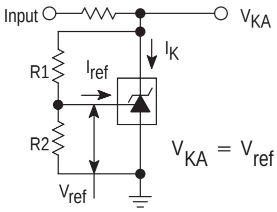


Figure 2. Test Circuit for $V_{KA} > V_{ref}$



$$V_{KA} = V_{ref}\left(1 + \frac{R1}{R2}\right) + I_{ref} \cdot R1$$

Figure 3. Test Circuit for I_{of}

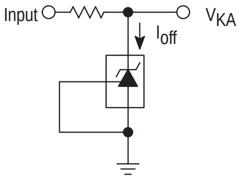


Figure 4. Cathode Current versus Cathode Voltage

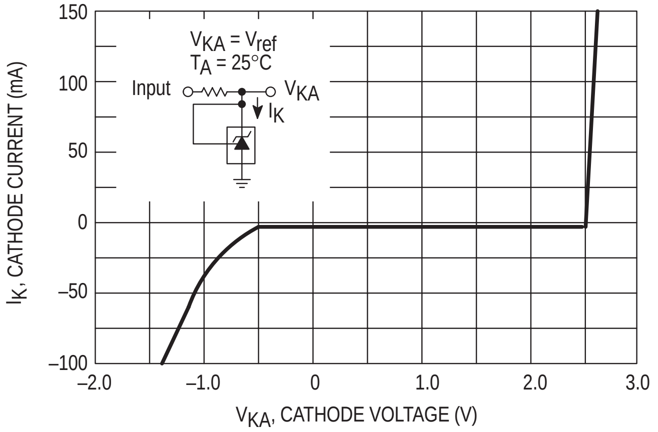


Figure 5. Cathode Current versus Cathode Voltage

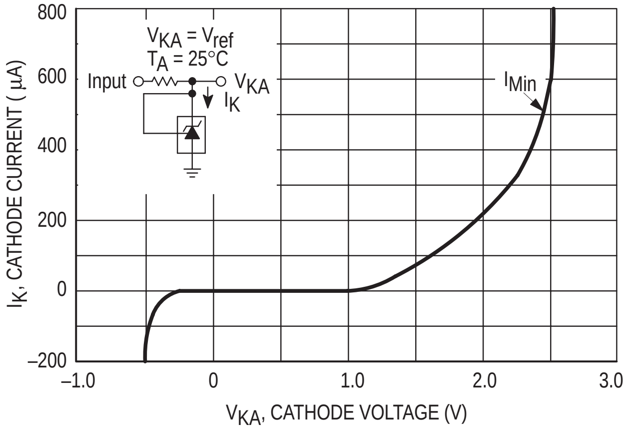


Figure 6. Reference Input Voltage versus Ambient Temperature

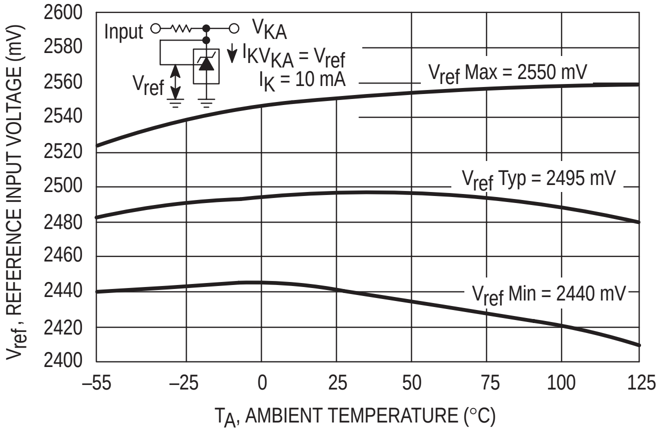


Figure 7. Reference Input Current versus Ambient Temperature

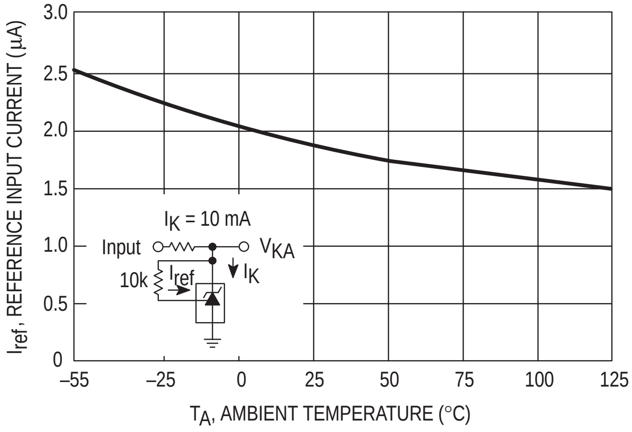


Figure 8. Change in Reference Input Voltage versus Cathode Voltage

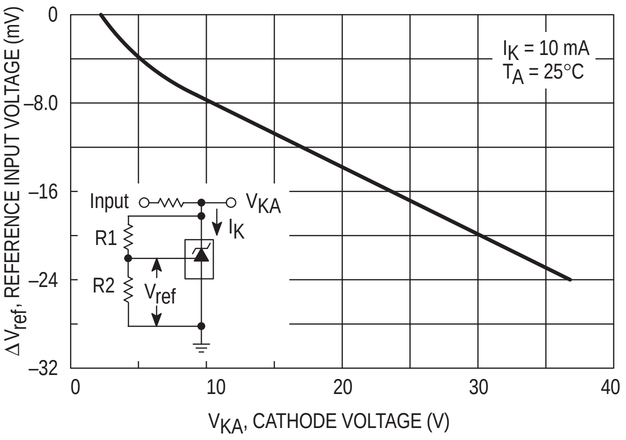


Figure 9. Off–State Cathode Current versus Ambient Temperature

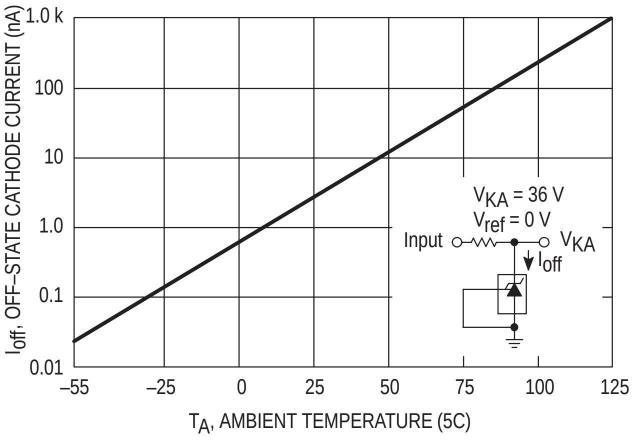


Figure 10. Dynamic Impedance versus Frequency

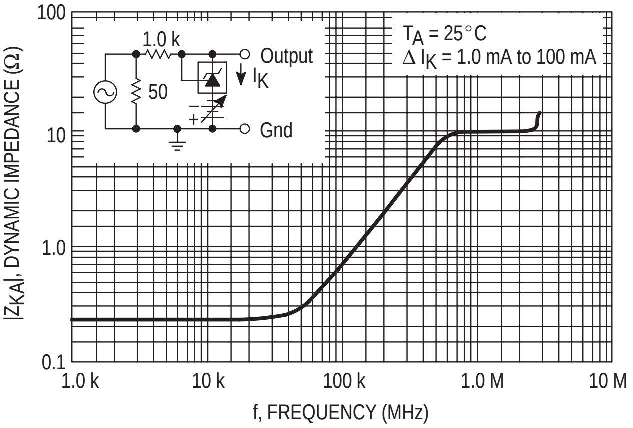


Figure 11. Dynamic Impedance versus Ambient Temperature

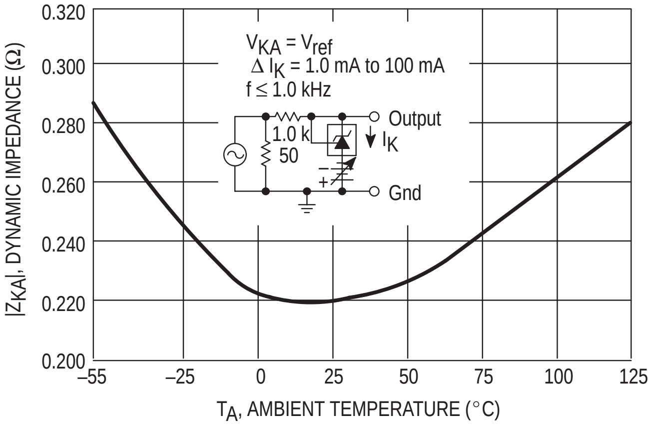


Figure 12. Open–Loop Voltage Gain versus Frequency

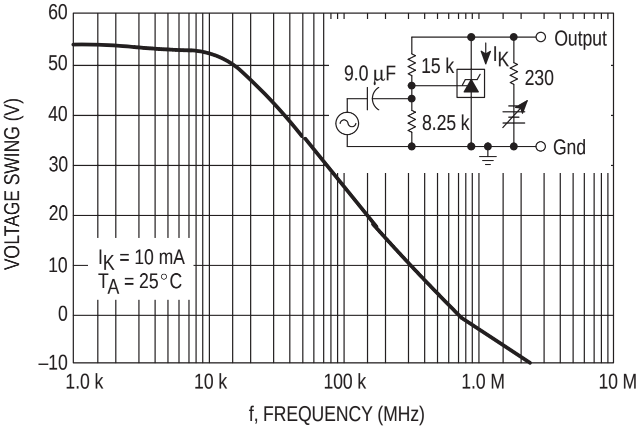
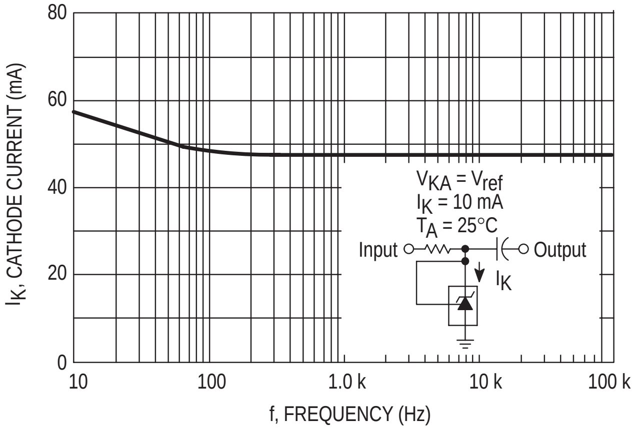


Figure 13. Spectral Noise Density



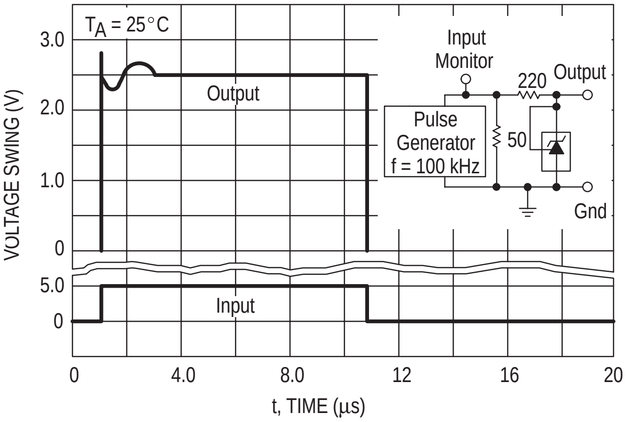


Figure 14. Pulse Response

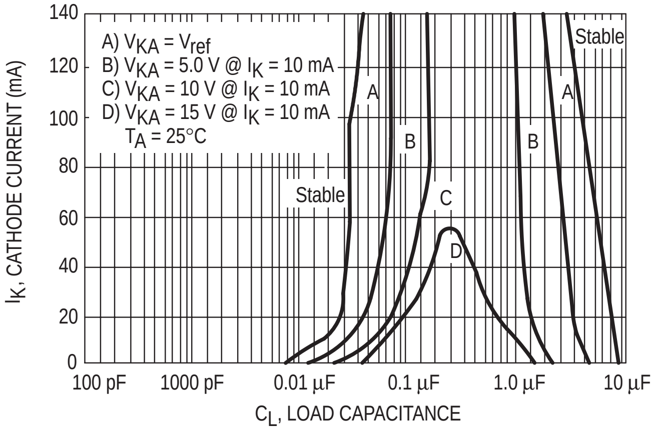


Figure 15. Stability Boundary Conditions

Figure 16. Test Circuit For Curve A of Stability Boundary Conditions

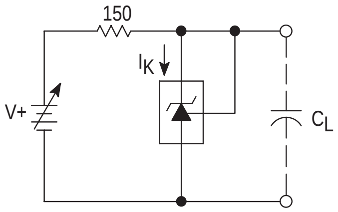
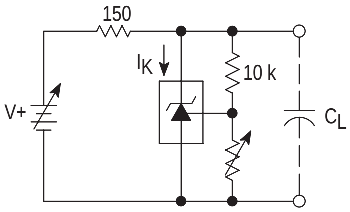
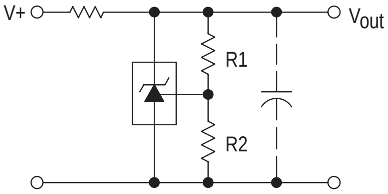


Figure 17. Test Circuit For Curves B, C, And D of Stability Boundary Conditions



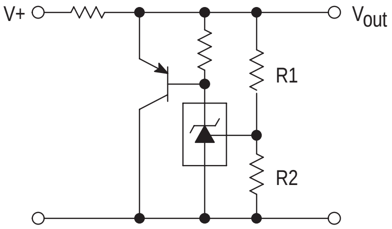
TYPICAL APPLICATIONS

Figure 18. Shunt Regulator



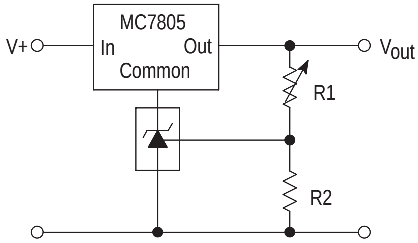
$$V_{out} = \left(1 + \frac{R1}{R2}\right) V_{ref}$$

Figure 19. High Current Shunt Regulator



$$V_{out} = \left(1 + \frac{R1}{R2}\right) V_{ref}$$

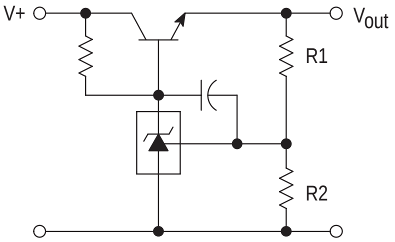
Figure 20. Output Control for a Three–Terminal Fixed Regulator



$$V_{out} = \left(1 + \frac{R1}{R2}\right) V_{ref}$$

$$V_{out}\ \mathrm{min} = V_{ref} + 5.0V$$

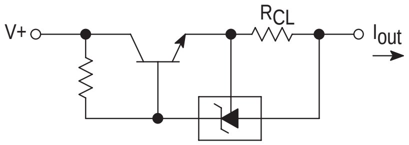
Figure 21. Series Pass Regulator



$$V_{out} = \left(1 + \frac{R1}{R2}\right) V_{ref}$$

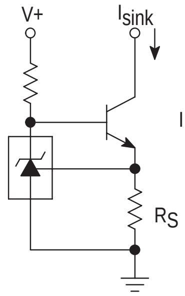
$$V_{out}\ \mathrm{min} = V_{ref} + V_{be}$$

Figure 22. Constant Current Source



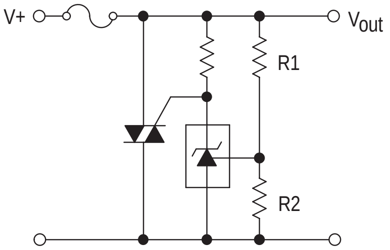
$$I_{out} = \frac{V_{ref}}{R_{CL}}$$

Figure 23. Constant Current Sink



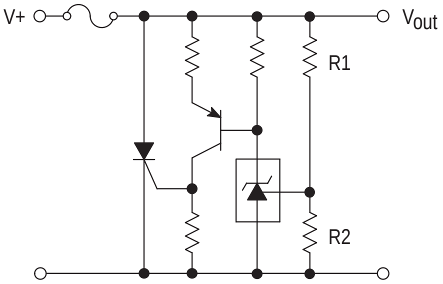
$$I_{Sink} = \frac{V_{ref}}{R_S}$$

Figure 24. TRIAC Crowbar

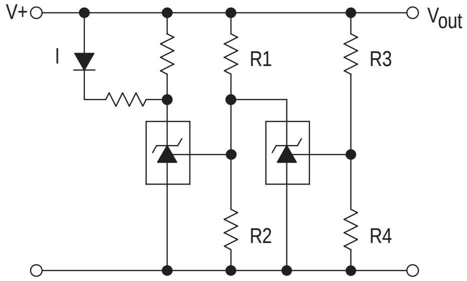


$$V_{out(trip)} = \left(1 + \frac{R1}{R2}\right) V_{ref}$$

Figure 25. SRC Crowbar



$$V_{out(trip)} = \left(1 + \frac{R1}{R2}\right) V_{ref}$$

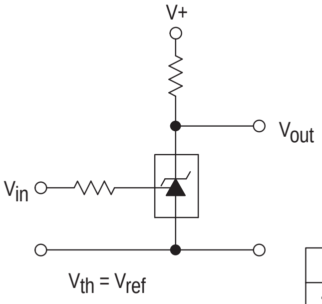


L.E.D. indicator is ‘on’ when V+ is between the upper and lower limits.

$$\text{Lower Limit} = \left(1 + \frac{R1}{R2}\right) V_{ref}$$

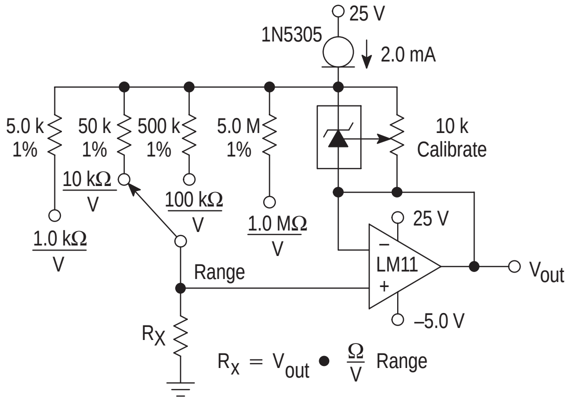
$$\text{Upper Limit} = \left(1 + \frac{R3}{R4}\right) V_{ref}$$

Figure 26. Voltage Monitor



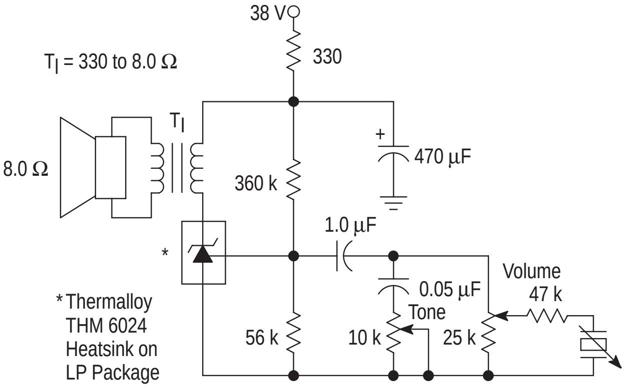
V_{in}	V_{out}
< V_{ref}	V+
> V_{ref}	≈ 2.0 V

Figure 27. Single–Supply Comparator with Temperature–Compensated Threshold



$$R_X = V_{out} \bullet \frac{\Omega}{V} \text{ Range}$$

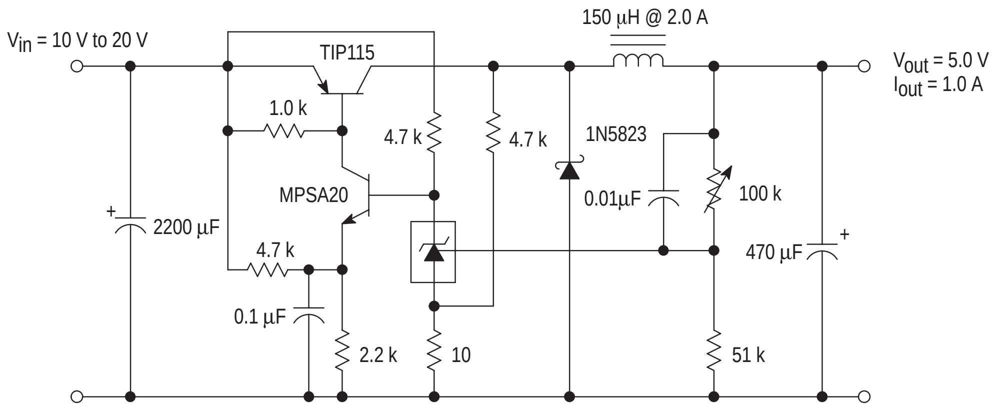
Figure 28. Linear Ohmmeter



*Thermalloy THM 6024 Heatsink on LP Package

Figure 29. Simple 400 mW Phono Amplifier

Figure 30. High Efficiency Step–Down Switching Converter



Test	Conditions	Results
Line Regulation	V_{in} = 10 V to 20 V, I_O = 1.0 A	53 mV (1.1%)
Load Regulation	V_{in} = 15 V, I_O = 0 A to 1.0 A	25 mV (0.5%)
Output Ripple	V_{in} = 10 V, I_O = 1.0 A	50 mVpp P.A.R.D.
Output Ripple	V_{in} = 20 V, I_O = 1.0 A	100 mVpp P.A.R.D.
Efficiency	V_{in} = 15 V, I_O = 1.0 A	82%

Data Conversion

In Brief . . .

Motorola's line of digital–to–analog and analog–to–digital converters include several varieties to suit a number of applications.

The A/D converters include an 8–bit flash converter suitable for NTSC and PAL systems. CMOS devices include 8 to 10–bit converters, as well as other high speed digitizers.

The D/A converters have 6 and 8–bit devices, and video speed (for NTSC and PAL) devices.

Data Conversion

The line of data conversion products which Motorola offers spans a wide spectrum of speed and resolution/accuracy. Features, including bus compatibility, minimize external parts count and provide easy interface to microprocessor systems. Various technologies, such as Bipolar and CMOS, are utilized to achieve functional capability, accuracy and production repeatability. Bipolar technology generally results in higher speed, while CMOS devices offer greatly reduced power consumption.

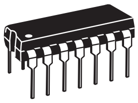
Table 1. A–D Converters

Resolution (Bits)	Device	Nonlinearity Max	Conversion Time/Rate	Input Voltage Range	Supplies (V)	Temperature Range (°C)	Suffix/ Package	Comments
CMOS								
8	MC145040	±1/2 LSB	10 µs	0 to V_{DD}	+5.0 ±10%	–40 to +125	P/738, DW/751D	Requires External Clock, 11–Ch MUX
	MC145041		20 µs					Includes Internal Clock, 11–Ch MUX
	MC14549B/ MC14559B	Successive Approximation Registers			+3.0 to +18	–40 to +85	P/648	Compatible with MC1408 S.A.R. 8–bit D–A Converter
Triple 8–Bit	MC44251	1 LSB	18 MHz	1.6 to 4.6 V	+5.0 ±10%	–40 to +85	FN/777	3 Separate Video Channels
10	MC145050	±1 LSB	21 µs	0 to V_{DD}	+5.0 ±10%	–40 to +125	P/738, DW/751D	Requires External Clock, 11–Ch MUX
	MC145051		44 µs					Includes Internal Clock, 11–Ch MUX
	MC145053						P/646, D/751A	Includes Internal Clock, 5–Ch MUX
8–10	MC14443/ MC14447	±0.5% Full Scale	300 µs	Variable w/Supply	+5.0 to +18	–40 to +85	P/648, DW/751G	µP Compatible, Single Slope, 6–Ch MUX
3–1/2 Digit	MC14433	±0.05% ±1 Count	40 ms	±2.0 V ±200 mV	+5.0 to +8.0 –2.8 to –8.0		P/709, DW/751E	Dual Slope
Bipolar								
8	MC10319	±1 LSB	25 MHz	0 to 2.0 Vpp Max	+5.0 and –3.0 to –6.0	0 to +70	P/709, DW/751F Die Form	Video Speed Flash Converter, Internal Gray Code TTL Outputs
Sigma–Delta								
16	MC145073	±1 LSB	48 kHz	1.9 Vpp	4.5 to 5.5	–40 to +85	DW/751E	Dual Channel, Sigma–Delta architecture

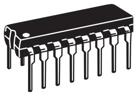
Table 2. D–A Converters

Resolution (Bits)	Device	Accuracy @ 25°C Max	Max Settling Time (± 1/2 LSB)	Supplies (V)	Temperature Range (°C)	Suffix/ Package	Comments
CMOS							
6	MC144110	–	–	+5.0 to +15	0 to +85	P/707, DW/751D	Serial input, Hex DAC, 6 outputs
	MC144111	–	–			P/646, DW/751G	Serial input, Quad DAC, 4 outputs
	MC144112	–	–	+2.5 to +5.5	–40 to +85	P/646, D/751A	Serial input, Quad DAC, 4 outputs
Triple 8–Bit	MC44200	±1/2 LSB	30 ns	+5.0 ±10%	–40 to +85	FU/824A	Triple Video DAC, 55 MHz, TTL
Sigma–Delta							
16, 18, 20	MC145074	See data sheet	6.0 ns	4.5 to 5.5	–40 to +85	D/751B	Dual Channel, Sigma–Delta architecture, MC145076 FIR Filter available
–	MC145076	See data sheet	–	+5.0	–40 to +85	D/751B	Dual Channel Bit Stream, 144 tap FIR Filter

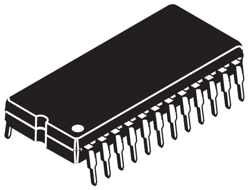
Data Conversion Package Overview



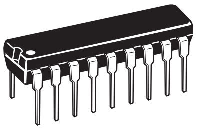
CASE 646
P SUFFIX



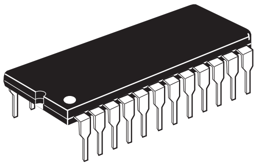
CASE 648
P SUFFIX



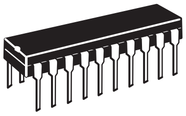
CASE 649
P SUFFIX



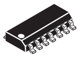
CASE 707
P SUFFIX



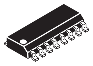
CASE 709
P SUFFIX



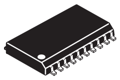
CASE 738
P SUFFIX



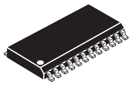
CASE 751A
D SUFFIX



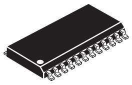
CASE 751B
D SUFFIX



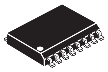
CASE 751D
DW SUFFIX



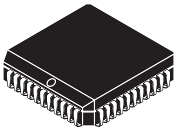
CASE 751E
DW SUFFIX



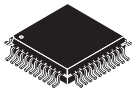
CASE 751F
DW SUFFIX



CASE 751G
DW SUFFIX



CASE 777
FN SUFFIX



CASE 824A
FU SUFFIX

Device Listing and Related Literature

A–D Converters

Device	Function	Page
MC10319	High Speed 8–Bit Analog–to–Digital Flash Converter	6–6

RELATED APPLICATION NOTES

App Note	Title	Related Device
AN702	High Speed Digital–to–Analog and Analog–to–Digital Techniques	**General Information**
AN926	Techniques for Improving the Settling Time of a DAC and Op Amp Combination	**Various**

MOTOROLA

MC10319

High Speed 8-Bit Analog-to-Digital Converter

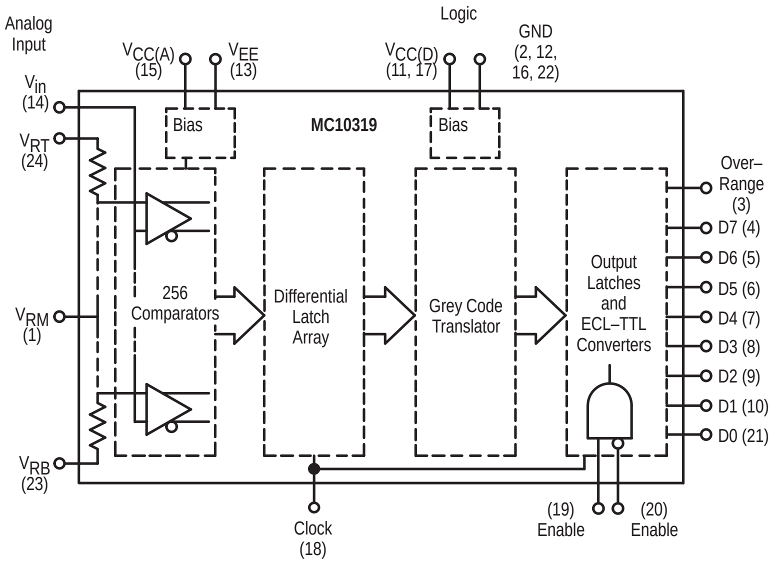
The MC10319 is an 8–bit high speed parallel flash A/D converter. The device employs an internal Grey Code structure to eliminate large output errors on fast slewing input signals. It is fully TTL compatible, requiring a + 5.0 V supply and a wide tolerance negative supply of – 3.0 to – 6.0 V. Three–state TTL outputs allow direct drive of a data bus or common I/O memory.

The MC10319 contains 256 parallel comparators across a precision input reference network. The comparator outputs are fed to latches and then to an encoder network, to produce an 8–bit data byte plus an overrange bit. The data is latched and converted to 3–state LS–TTL outputs. The overrange bit is always active to allow for either sensing of the overrange condition or ease of interconnecting a pair of devices to produce a 9–bit A/D converter.

Applications include video display and radar processing, high speed instrumentation and TV broadcast encoding.

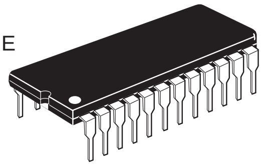
- Internal Grey Code for Speed and Accuracy, Binary Outputs
- 8–Bit Resolution/9–Bit Typical Accuracy
- Easily Interconnected for 9–Bit Conversion
- 3–State LS–TTL Outputs with True/Complement Enable Inputs
- 25 MHz Sampling Rate
- Wide Input Range: 1.0 to 2.0 V_{pp}, between ± 2.0 V
- Low Input Capacitance: 50 pF
- Low Power Dissipation: 618 mW
- No Sample/Hold Required for Video Bandwidth Signals
- Single Clock Cycle Conversion

Representative Block Diagram

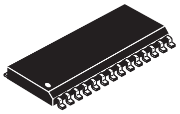


HIGH SPEED
8–BIT ANALOG–TO–DIGITAL
FLASH CONVERTER

SEMICONDUCTOR
TECHNICAL DATA

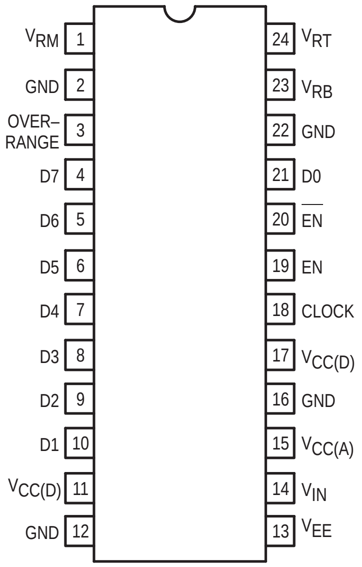


P SUFFIX
PLASTIC PACKAGE
CASE 709



DW SUFFIX
PLASTIC PACKAGE
CASE 751F
(SO–28L)

PIN CONNECTIONS
(P only)



ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC10319DW	T_A = 0° to +70°C	SO–28L
MC10319P		Plastic

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	$V_{CC(A),(D)}$ V_{EE}	+ 7.0 – 7.0	Vdc
Positive Supply Voltage Differential	$V_{CC(D)}$ – $V_{CC(A)}$	– 0.3 to + 0.3	Vdc
Digital Input Voltage (Pins 18 to 20)	$V_{I(D)}$	– 0.5 to + 7.0	Vdc
Analog Input Voltage (Pins 1, 14, 23, 24)	$V_{I(A)}$	– 2.5 to + 2.5	Vdc
Reference Voltage Span (Pin 24 to Pin 23)	–	2.3	Vdc
Applied Output Voltage (Pins 4 to 10, 21 in 3–State)	–	– 0.3 to + 7.0	Vdc
Junction Temperature	T_J	+ 150	°C
Storage Temperature	T_{stg}	– 65 to + 150	°C

Devices should not be operated at these values. The “Recommended Operating Limits” table provides guidelines for actual device operation.

RECOMMENDED OPERATING LIMITS

Characteristic	Symbol	Min	Typ	Max	Unit
Power Supply Voltage (Pin 15) (Pins 11, 17)	$V_{CC(A)}$ $V_{CC(D)}$	+ 4.5	+ 5.0	+ 5.5	Vdc
$V_{CC(D)} - V_{CC(A)}$	ΔV_{CC}	– 0.1	0	+ 0.1	Vdc
Power Supply Voltage (Pin 13)	V_{EE}	– 6.0	– 5.0	– 3.0	Vdc
Digital Input Voltages (Pins 18 to 20)	$V_{I(D)}$	0	–	+ 5.0	Vdc
Analog Input (Pin 14)	$V_{I(A)}$	– 2.1	–	+ 2.1	Vdc
Voltage @ V_{RT} (Pin 24)	V_{RT}	– 1.0	–	+ 2.1	Vdc
Voltage @ V_{RB} (Pin 23)	V_{RB}	– 2.1	–	+ 1.0	Vdc
$V_{RT} - V_{RB}$	ΔV_R	+ 1.0	–	+ 2.1	Vdc
$V_{RB} - V_{EE}$	–	1.3	–	–	Vdc
Applied Output Voltage (Pins 4 to 10, 21 in 3–State)	V_o	0	–	5.5	Vdc
Clock Pulse Width – High Low	t_{CKH} t_{CKL}	5.0 15	20 20	– –	ns
Clock Frequency	f_{CLK}	0	–	25	MHz
Operating Ambient Temperature	T_A	0	–	+ 70	°C

ELECTRICAL CHARACTERISTICS (0° $<$ T_A $<$ 70°C, V_{CC} = 5.0 V, V_{EE} = – 5.2 V, V_{RT} = +1.0 V, V_{RB} = – 1.0 V, unless noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
TRANSFER CHARACTERISTICS (f_{CKL} = 25 MHz)					
Resolution	N	–	–	8.0	Bits
Monotonicity	MON	Guaranteed			Bits
Integral Nonlinearity	INL	–	± 1/4	± 1.0	LSB
Differential Nonlinearity	DNL	–	–	± 1.0	LSB
Differential Phase (See Figure 16)	DP	–	1	–	Deg.
Differential Gain (See Figure 16)	DG	–	1	–	%
Power Supply Rejection Ratio (4.5 V $<$ V_{CC} $<$ 5.5 V, V_{EE} = – 5.2 V) (– 6.0 V $<$ V_{EE} $<$ – 3.0 V, V_{CC} = + 5.0 V)	PSRR	 – –	 0.1 0	 – –	LSB/V

ELECTRICAL CHARACTERISTICS – continued

($0° < T_A < 70°C$, V_{CC} = 5.0 V, V_{EE} = – 5.2 V, V_{RT} = +1.0 V, V_{RB} = – 1.0 V, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
ANALOG INPUTS (Pin 14)					
Input Current @ $V_{in} = V_{RB}$ (See Figure 5)	I_{INL}	– 100	0	–	µA
Input Current @ $V_{in} = V_{RT}$ (See Figure 5)	I_{INH}	–	60	150	µA
Input Capacitance ($V_{RT} – V_{RB}$ = 2.0 V, See Figure 4)	C_{in}	–	36	–	pF
Input Capacitance ($V_{RT} – V_{RB}$ = 1.0 V, See Figure 4)	C_{in}	–	55	–	pF
Bipolar Offset Error	V_{OS}	–	0.1	–	LSB
REFERENCE					
Ladder Resistance (V_{RT} to V_{RB}, T_A = 25°C)	R_{ref}	104	130	156	Ω
Temperature Coefficient	T_C	–	+ 0.29	–	%/°C
Ladder Capacitance (Pin 1 open)	C_{ref}	–	25	–	pF
ENABLE INPUTS (V_{CC} = 5.5 V) (See Figure 6)					
Input Voltage – High (Pins 19 to 20)	V_{IHE}	2.0	–	–	V
Input Voltage – Low (Pins 19 to 20)	V_{ILE}	–	–	0.8	V
Input Current @ 2.7 V	I_{IHE}	–	0	20	µA
Input Current @ 0.4 V @ $\overline{EN}$ (0 < EN < 5.0 V)	I_{IL1}	– 400	– 100	–	µA
Input Current @ 0.4 V @ EN ($\overline{EN}$ = 0 V)	I_{IL2}	– 400	– 100	–	µA
Input Current @ 0.4 V @ EN ($\overline{EN}$ = 2.0 V)	I_{IL3}	– 20	– 2.0	–	µA
Input Clamp Voltage (I_{IK} = – 18 mA)	V_{IKE}	– 1.5	– 1.3	–	V
CLOCK INPUTS (V_{CC} = 5.5 V)					
Input Voltage High	V_{IHC}	2.0	–	–	Vdc
Input Voltage Low	V_{ILC}	–	–	0.8	Vdc
Input Current @ 0.4 V (See Figure 7)	I_{ILC}	– 400	– 80	–	µA
Input Current @ 2.7 V (See Figure 7)	I_{IHC}	– 100	– 20	–	µA
Input Clamp Voltage (I_{IK} = – 18 mA)	V_{IKC}	– 1.5	– 1.3	–	Vdc
DIGITAL OUTPUTS					
High Output Voltage (I_{OH} = – 400 µA, V_{CC} = 4.5 V, See Figure 8)	V_{OH}	2.4	3.0	–	V
Low Output Voltage (I_{OL} = 4.0 mA, See Figure 9)	V_{OL}	–	0.35	0.4	V
Output Short Circuit Current* (V_{CC} = 5.5 V)	I_{SC}	–	35	–	mA
Output Leakage Current (0.4 < V_O < 2.4 V, See Figure 3, V_{CC} = 5.5 V, D0 to D7 in 3–State Mode)	I_{LK}	– 50	–	+ 50	µA
Output Capacitance (D0 to D7 in 3–State Mode)	C_{out}	–	9.0	–	pF

*Only one output is to be shorted at a time, not to exceed 1 second.

Characteristic	Symbol	Min	Typ	Max	Unit
POWER SUPPLIES					
$V_{CC(A)}$ Current (4.5 V < $V_{CC(A)}$ < 5.5 V) (Outputs unloaded)	$I_{CC(A)}$	10	17	25	mA
$V_{CC(D)}$ Current (4.5 V < $V_{CC(D)}$ < 5.5 V) (Outputs unloaded)	$I_{CC(D)}$	50	90	133	mA
V_{EE} Current (– 6.0 < V_{EE} < – 3.0 V)	I_{EE}	– 14	– 10	– 6.0	mA
Power Dissipation ($V_{RT} – V_{RB}$ = 2.0 V) (Outputs unloaded)	P_D	–	618	995	mW

TIMING CHARACTERISTICS (T_A = 25°C, V_{CC} = + 5.0 V, V_{EE} = – 5.2 V, V_{RT} = + 1.0 V, V_{RB} = – 1.0 V, see System Timing Diagram, Figure 1.)

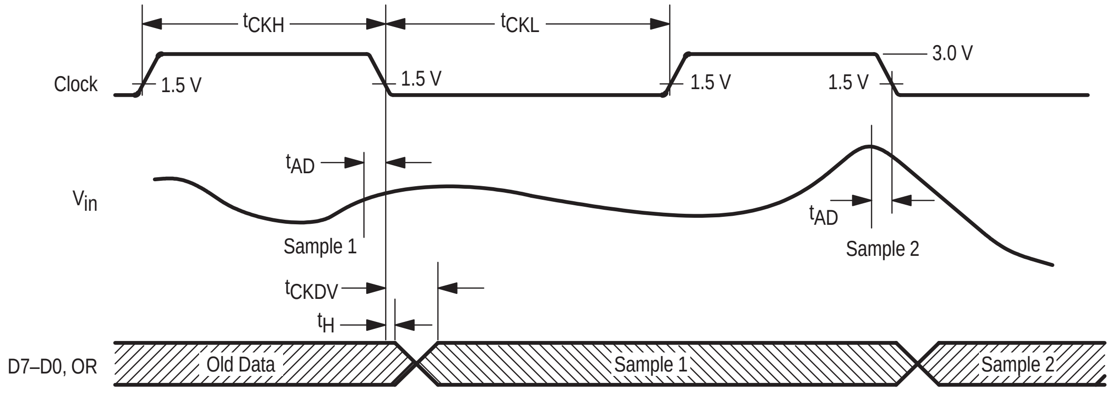
Characteristic	Symbol	Min	Typ	Max	Unit
INPUTS					
Min Clock Pulse Width – High	t_{CKH}	–	5.0	–	ns
Min Clock Pulse Width – Low	t_{CKL}	–	15	–	ns
Max Clock Rise, Fall Time	$t_{R,F}$	–	100	–	ns
Clock Frequency	f_{CLK}	0	30	25	MHz
OUTPUTS					
New Data Valid from Clock Low	t_{CKDV}	–	19	–	ns
Aperture Delay	t_{AD}	–	4.0	–	ns
Hold Time	t_H	–	6.0	–	ns
Data High to 3–State from Enable Low*	t_{EHZ}	–	27	–	ns
Data Low to 3–State from Enable Low*	t_{ELZ}	–	18	–	ns
Data High to 3–State from $\overline{\text{Enable}}$ High*	$t_{\overline{E}HZ}$	–	32	–	ns
Data Low to 3–State from $\overline{\text{Enable}}$ High*	$t_{\overline{E}LZ}$	–	18	–	ns
Valid Data from Enable High (Pin 20 = 0 V)*	t_{EDV}	–	15	–	ns
Valid Data from $\overline{\text{Enable}}$ Low (Pin 19 = 5.0 V)*	$t_{\overline{E}DV}$	–	16	–	ns
Output Transition Time* (10% to 90%)	t_{tr}	–	8.0	–	ns

*See Figure 2 for output loading.

PIN FUNCTION DESCRIPTION

Function	Pin		Description
	P Suffix	DW Suffix	
V_{RM}	1	1	The midpoint of the reference resistor ladder. Bypassing can be done at this point to improve performance at high frequencies.
GND	2, 12 16, 22	2, 13, 17 18, 25, 26	Digital ground. The pins should be connected directly together, and through a low impedance path to the power supply.
OVR	3	3	Overrange output. Indicates V_{in} is more positive than V_{RT} 1/2 LSB. This output does not have 3–state capability.
D7–D0	4 to 10, 21	4 to 10, 24	Digital Outputs. D7 (Pin 4) is the MSB. D0 (Pin 21 or 24) is the LSB. LS–TTL compatible with 3–state capability.
$V_{CC(D)}$	11, 17	11, 12 19, 20	Power supply for the digital section. +5.0 V, ±10% required. Reference to digital ground.
V_{EE}	13	14	Negative power supply. Nominally – 5.2 V, it can range from – 3.0 to – 6.0 V, and must be more negative than V_{RB} by $>$ 1.3 V. Reference to analog ground.
V_{in}	14	15	Signal voltage input. This voltage is compared to the reference to generate a digital equivalent. Input impedance is nominally 16 to 33K in parallel with 36 pF.
$V_{CC(A)}$	15	16	Power supply for the analog section. +5.0 V, ±10% required. Reference to analog ground.
CLK	18	21	Clock input. TTL compatible.
EN	19	22	Enable input. TTL compatible, a logic 1 (and $\overline{\text{EN}}$ at a logic 0) enables the data outputs. A logic 0 puts the outputs in a 3–state mode.
EN	20	23	$\overline{\text{Enable}}$ input. TTL compatible, a logic 0 (and EN at a logic 1) enables the data outputs. A logic 1 puts the outputs in a 3–state mode.
V_{RB}	23	27	The bottom (most negative point) of the internal reference resistor ladder.
V_{RT}	24	28	The top (most positive point) of the internal reference resistor ladder.

Figure 1. System Timing Diagram



t_{CKDV} and t_H measured at output levels of 0.8 and 2.4 V.

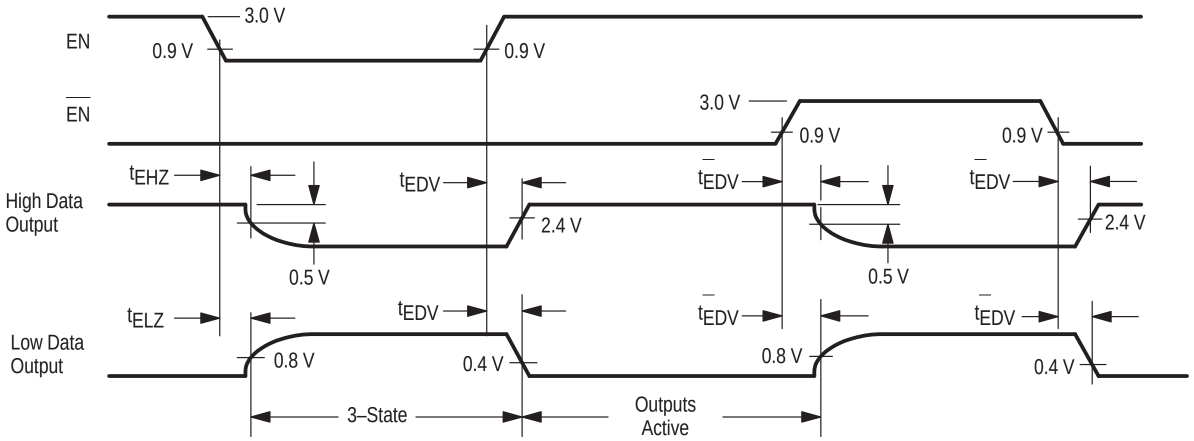
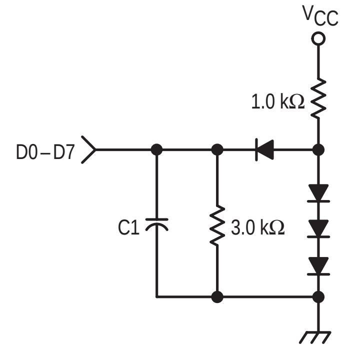


Figure 2. Data Output Test Circuit



Diodes = 1N914 or equivalent, C1 ≈ 15 pF

Figure 3. Output 3–State Leakage Current

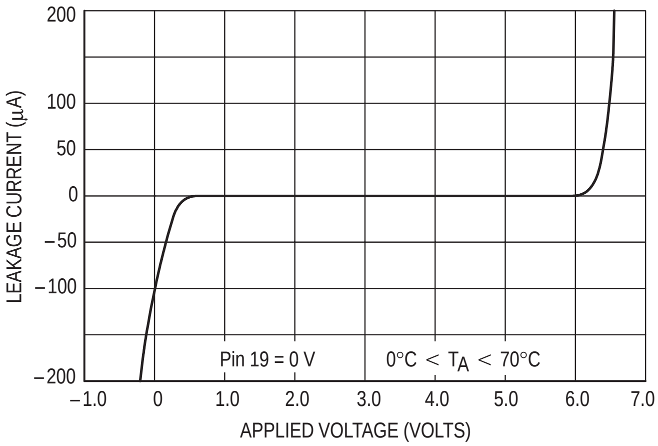


Figure 4. Input Capacitance @ V_{in} (Pin 14)

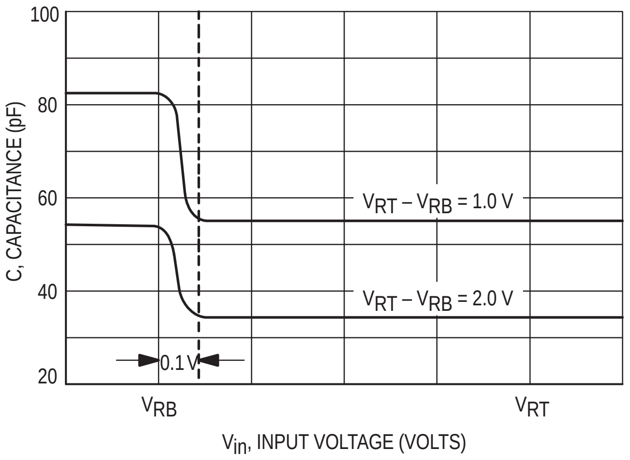


Figure 5. Input Current @ V_{in} (Pin 14)

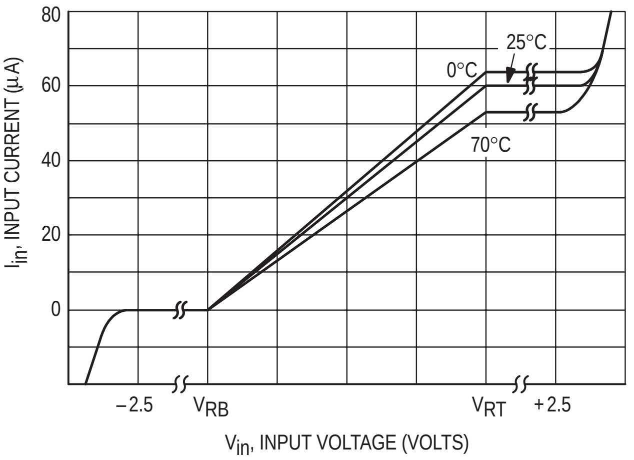


Figure 6. Input Current @ Enable, $\overline{\text{Enable}}$

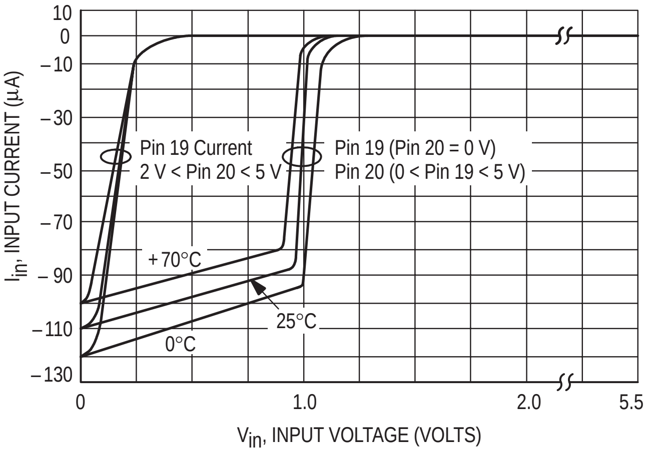


Figure 7. Clock Input Current

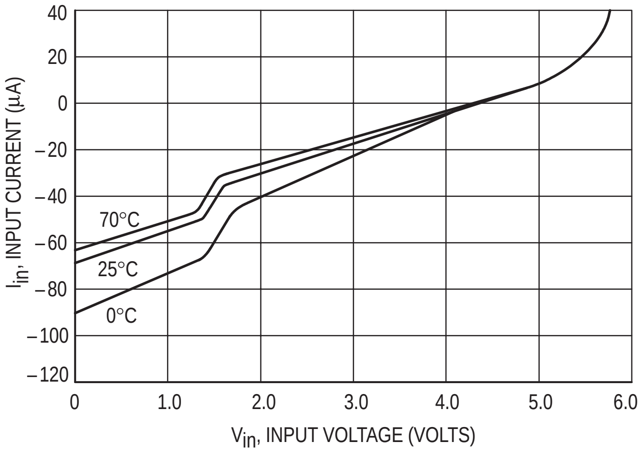


Figure 8. Output Voltage versus Output Current

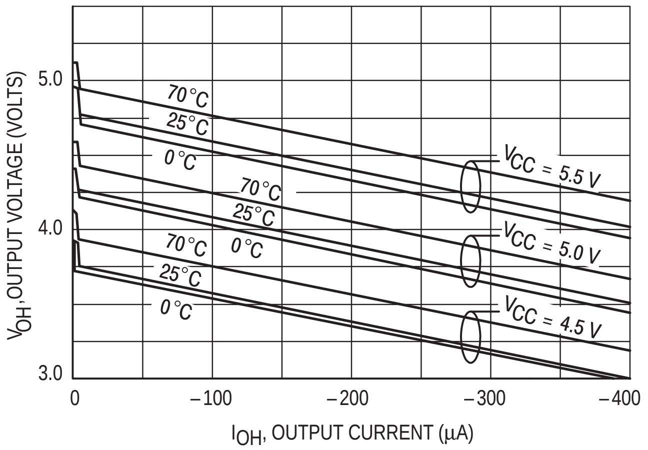


Figure 9. Output Voltage versus Output Current

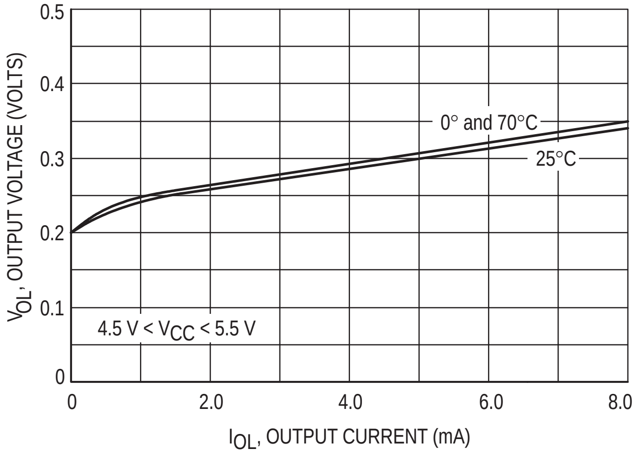


Figure 10. Supply Current versus Temperature

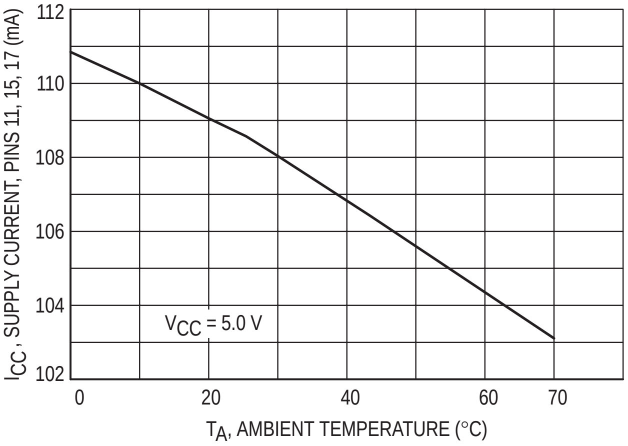


Figure 11. Supply Current versus Temperature

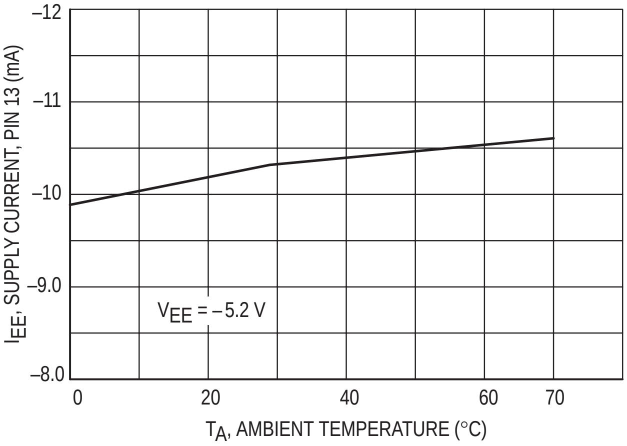


Figure 12. Differential Linearity Error

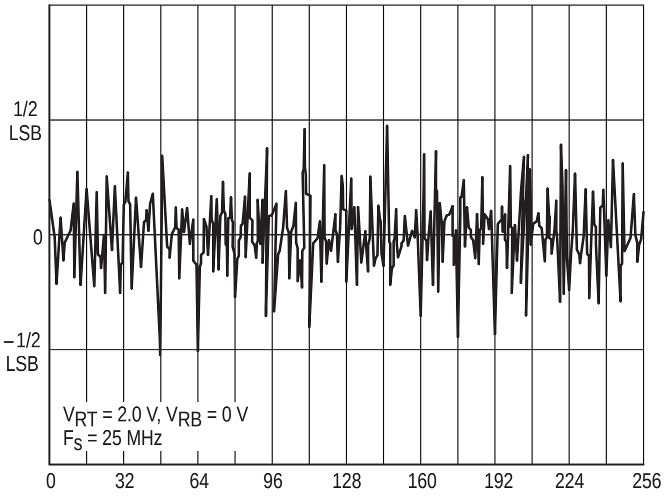


Figure 13. Integral Linearity Error

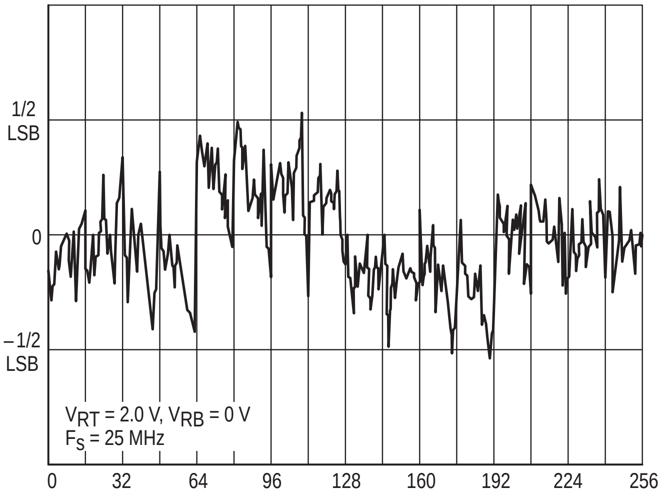


Figure 14. Differential Linearity Error

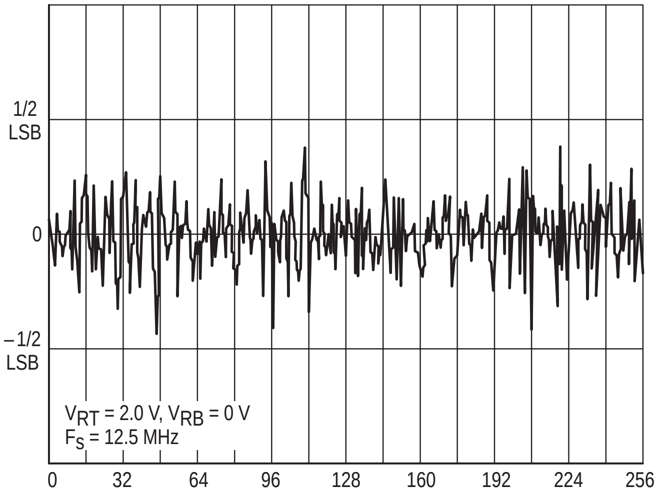
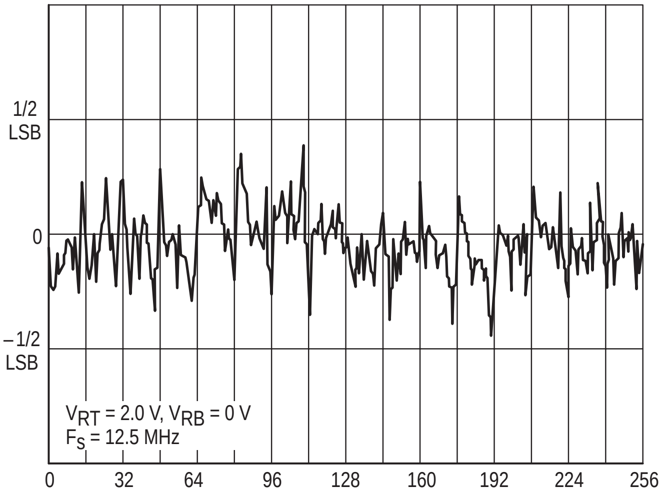


Figure 15. Integral Linearity Error



DESIGN GUIDELINES

Introduction

The MC10319 is a high speed, 8–bit, parallel (“flash”) type analog–to–digital converter containing 256 comparators at the front end. See Figure 17 for a block diagram. The comparators are arranged such that one input of each is referenced to evenly spaced voltages, derived from the reference resistor ladder. The other input of the comparators is connected to the input signal (V_{in}). Some of the comparator′s differential outputs will be “true,” while other comparators will have “not true” outputs, depending on their relative position. Their outputs are then latched, and converted to an 8–bit Grey code by the Differential Latch Array. The Grey code ensures that any input errors due to cross talk, feed–thru, or timing disparities result in glitches at the output of only a few LSBs, rather than the more traditional 1/2 scale and 1/4 scale glitches.

The Grey code is then translated to an 8–bit binary code, and the differential levels are translated to TTL levels before being applied to the output latches. Enable inputs at this final stage permit the TTL outputs (except overrange) to be put into a high impedance (3–state) condition.

ANALOG SECTION

Signal Input

The signal voltage to be digitized (V_{in}) is applied simultaneously to one input of each of the 256 comparators through Pin 14. The other inputs of the comparators are connected to 256 evenly spaced voltages derived from the reference ladder. The output code depends on the relative position of the input signal and the reference voltages. The comparators have a bandwidth of > 50 MHz, which is more than sufficient for the allowable (Nyquist Theorem) input frequency of 12.5 MHz.

The current into Pin 14 varies linearly from 0 (when $V_{in} = V_{RB}$) to ≈60 µA (when $V_{in} = V_{RT}$). If V_{in} is taken below V_{RB} or above V_{RT}, the input current will remain at the value corresponding to V_{RB} and V_{RT} respectively (see Figure 5). However, V_{in} must be maintained within the absolute range of ±2.5 V (with respect to ground) – otherwise excessive currents will result at Pin 14, due to internal clamps.

The input capacitance at Pin 14 is typically 36 pF if $[V_{RT} – V_{RB}]$ is 2.0 V, and increases to 55 pF if $[V_{RT} – V_{RB}]$ is reduced to 1.0 V (see Figure 4). The capacitance is constant as V_{in} varies from V_{RT} down to ≈0.1 V above V_{RB}. Taking V_{in} to V_{RB} will show an increase in the capacitance of ≈50%. If V_{in} is taken above V_{RT}, or below V_{RB}, the capacitance will stay at the values corresponding to V_{RT} and V_{RB}, respectively.

The source impedance of the signal voltage should be maintained below 100 Ω (at the frequencies of interest) in order to avoid sampling errors.

Reference

The reference resistor ladder is composed of a string of equal value resistors to provide 256 equally spaced voltages for the comparators (see Figure 17 for the actual configuration). The voltage difference between adjacent comparators corresponds to 1 LSB of the input range. The first comparator (closest to V_{RB}) is referenced 1/2 LSB above V_{RB}, and 256th comparator (for the overrange) is referenced 1/2 LSB below V_{RT}. The total resistance of the ladder is nominally 130 Ω, ±20%, requiring 15.4 mA @ 2.0 V, and 7.7 mA @ 1.0 V. There is a nominal warm–up change of ≈ +9.0% in the ladder resistance due to the +0.29%/°C temperature coefficient.

The minimum recommended span $[V_{RT} – V_{RB}]$ is 1.0 V. A lower span will allow offsets and nonlinearities to become significant. The maximum recommended span is 2.1 V due to power limitations of the resistor ladder. The span may be anywhere within the range of – 2.1 to + 2.1 V with respect to ground, and V_{RB} must be at least 1.3 V more positive than V_{EE}. The reference voltages must be stable and free of noise and spikes, since the accuracy of a conversion is directly related to the quality of the reference.

In most applications, the reference voltages will remain fixed. In applications involving a varying reference for modulation or signal scrambling, the modulating signal may be applied to V_{RT}, or V_{RB}, or both. The output will vary inversly with the reference signal, introducing a nonlinearity into the transfer function. The addition of the modulating signal and the dc level applied to the reference must be such that the absolute voltage at V_{RT} and V_{RB} is maintained within the values listed in the Recommended Operating Limits. The RMS value of the span must be maintained ≤ 2.1 V.

V_{RM} (Pin 1) is the midpoint of the resistor ladder, excluding the Overrange comparator. The voltage at V_{RM} is:

$$\frac{V_{RT} + V_{RB}}{2.0} - 1/2 \text{ LSB}$$

In most applications, bypassing this pin to ground (0.1 µF) is sufficient to maintain accuracy. In applications involving very high frequencies, and where linearity is critical, it may be necessary to trim the voltage at the midpoint. A means for accomplishing this is indicated in Figure 18.

Power Supplies

$V_{CC(A)}$ is the positive power supply for the comparators, and $V_{CC(D)}$ is the positive power supply for the digital portion. Both are to be +5.0 V, ±10%, and the two are to be within 100 mV of each other. There is indirect internal coupling between $V_{CC(D)}$ and $V_{CC(A)}$. If they are powered separately, and one supply fails, there will be current flow through the MC10319 to the failed supply.

$I_{CC(A)}$ is nominally 17 mA, and does not vary with clock frequency or with V_{in}. It does vary linearly with $V_{CC(A)}$. $I_{CC(D)}$ is nominally 90 mA, and is independent of clock frequency. It does vary, however, by 6 to 7 mA as V_{in} is changed, with the lowest current occurring when V_{in} = V_{RT}. It varies linearly with $V_{CC(D)}$.

V_{EE} is the negative power supply for the comparators, and is to be within the range – 3.0 to – 6.0 V. Additionally, V_{EE} must be at least 1.3 V more negative than V_{RB}. I_{EE} is a nominal – 10 mA, and is independent of clock frequency, V_{in}, and V_{EE}.

For proper operation, the supplies **must** be bypassed **at the IC**. A 10 μF tantalum, in parallel with a 0.1 μF ceramic is recommended for each supply to ground.

DIGITAL SECTION

Clock

The Clock input is TTL compatible with a typical frequency range of 0 to 30 MHz. There is no duty cycle limitations, but the minimum low and high times must be adhered to. See Figure 7 for the input current requirements.

The conversion sequence is shown in Figure 19, and is as follows:

- On the rising edge, the data output latches are latched with old data, and the comparator output latches are released to follow the input signal (V_{in}).
- During the high time, the comparators track the input signal. The data output latches retain the old data.
- On the falling edge, the comparator outputs are latched with the data immediately prior to this edge. The conversion to digital occurs within the device, and the data output latches are released to indicate the new data within 20 ns.
- During the clock low time, the comparator outputs remain latched, and the data output latches remain transparent.

A summary of the sequence is that data present at V_{in} just prior to the Clock falling edge is digitized and available at the data outputs immediately after that same falling edge.

The comparator output latches provide the circuit with an effective sample–and–hold function, eliminating the need for an external sample–and–hold.

Enable Inputs

The two Enable inputs are TTL compatible, and are used to change the data outputs (D7–D0) from active to 3–state. This capability allows cascading two MC10319s into a 9–bit configuration, flip–flopping two MC10319s into a 50 MHz configuration, connecting the outputs directly to a data bus, multiplexing multiple converters, etc. See the Applications Information section for more details. For the outputs to be active, Pin 19 must be a Logic “1”, and Pin 20 must be a Logic “0”. Changing either input will put the outputs into the high impedance mode. The Enable inputs affect **only** the state of the outputs – they do not inhibit a conversion. The input current into Pins 19 and 20 is shown in Figure 6, and the input/output timing is shown in Figure 1 and 20. Leaving either pin open is equivalent to a Logic “1”, although good design practice dictates that an input should never be left open.

The Overrange output (Pin 3) is not affected by the Enable inputs as it does not have 3–state capability.

Outputs

The Data outputs are TTL level outputs with high impedance capability. Pin 4 is the MSB (D7), and Pin 21 is the LSB (D0). The eight outputs are active as long as the Enable inputs are true (Pin 19 = high, Pin 20 = low). The timing of the outputs relative to the Clock input and the Enable inputs is shown in Figures 1 and 20. Figures 8 and 9 indicate the output voltage versus load current, while Figure 3 indicates the leakage current when in the high impedance mode.

The output code is natural binary, depicted in the table below.

The Overrange output (Pin 3) goes high when the input, V_{in}, is more positive than V_{RT} – 1/2 LSB. This output is always active – it does not have high impedance capability. Besides being used to indicate an input overrange, it is additionally used for cascading two MC10319s to form a 9–bit A/D converter (see Figure 27).

Table 1. Output Code

Input	V_{RT}, V_{RB} (V)			Output Code	Overrange
	2.048 V, 0 V	+ 1.0 V, – 1.0 V	+ 1.0 V, 0 V		
$> V_{RT}$ – 1/2 LSB	> 2.044V	> 0.9961 V	> 0.9980 V	FF_H	1
V_{RT} – 1/2 LSB	2.044 V	0.9961 V	0.9980 V	FF_H	0 ↔ 1
V_{RT} – 1 LSB	2.040 V	0.992 V	0.9961 V	FF_H	0
V_{RT} – 1–1/2 LSB	2.036 V	0.988 V	0.9941 V	FE_H ↔ FF_H	0
Midpoint	1.024 V	0.000 V	0.5000 V	80_H	0
V_{RB} + 1/2 LSB	4.0 mV	– 0.9961 V	1.95 mV	00_H ↔ 01_H	0
$< V_{RB}$	< 0 V	< – 1.0 V	< 0 V	00_H	0

APPLICATIONS INFORMATION

Power Supplies, Grounding

The PC board layout, and the quality of the power supplies and the ground system **at the IC** are very important in order to obtain proper operation. Noise, from any source, coming into the device on V_{CC}, V_{EE}, or ground can cause an incorrect output code due to interaction with the analog portion of the circuit. At the same time, noise generated within the MC10319 can cause incorrect operation if that noise does not have a clear path to ac ground.

Both the V_{CC} and V_{EE} power supplies must be decoupled to ground **at the IC** (within 1″ max) with a 10 µF tantalum and a 0.1 µF ceramic. Tantalum capacitors are recommended since electrolytic capacitors simply have too much inductance at the frequencies of interest. The quality of the V_{CC} and V_{EE} supplies should then be checked at the IC with a high frequency scope. Noise spikes (always present when digital circuits are present) can easily exceed 400 mV peak, and if they get into the analog portion of the IC, the operation can be disrupted. Noise can be reduced by inserting resistors and/or inductors between the supplies and the IC.

If switching power supplies are used, there will usually be spikes of 0.5 V or greater at frequencies of 50 to 200 kHz. These spikes are generally more difficult to reduce because of their greater energy content. In extreme cases, 3–terminal regulators (MC78L05ACP, MC7905.2CT), with appropriate high frequency filtering, should be used and dedicated to the MC10319.

The ripple content of the supplies should not allow their magnitude to exceed the values in the Recommended Operating Limits table.

The PC board tracks supplying V_{CC} and V_{EE} to the MC10319 should preferably not be at the tail end of the bus distribution, after passing through a maze of digital circuitry. The MC10319 should be close to the power supply, or the connector where the supply voltages enter the board. If the V_{CC} and V_{EE} lines are supplying considerable current to other parts of the boards, then it is preferable to have dedicated lines from the supply or connector directly to the MC10319.

The four ground pins (2, 12, 16, and 22) must be connected directly together. Any long path between them can cause stability problems due to the inductance (at 25 MHz) of the PC tracks. The ground return for the signal source must be noise free.

Reference Voltage Circuits

Since the accuracy of the conversion is directly related to the quality of the references, it is imperative that accurate and stable voltages be provided to V_{RT} and V_{RB}. If the reference span is 2.0 V, then 1/2 LSB is only 3.9 mV, and it is desireable that V_{RT} and V_{RB} be accurate to within this amount, and furthermore, that they do not drift more than this amount once set. Over the temperature range of 0° to 70°C, a maximum temperature coefficient of 28 ppm/°C is required.

The voltage supplies used for digital circuits should preferably **not** be used as a source for generating V_{RT} and V_{RB}, due to the noise spikes (50 to 400 mV) present on the supplies and on their ground lines. Generally ±15 V, or ±12 V, are available for analog circuits, and are usually clean compared to supplies used for digital circuits, although ripple may be present in varying amounts. Ripple is easier to filter out than spikes, however, and so these supplies are preferred.

Figure 21 depicts a circuit which can provide an extremely stable voltage to V_{RT} **at the current required** (the maximum reference current is 19.2 mA @ 2.0 V). The MC1403 series of reference sources has very low temperature coefficients, good noise rejection, and a high initial accuracy, allowing the circuit to be built without an adjustment pot if the V_{RT} voltage is to remain fixed at one value. Using 0.1% wirewound resistors for the divider provides sufficient accuracy and stability in many cases. Alternately, resistor networks provide high ratio accuracies, and close temperature tracking. If the application requires V_{RT} to be changed periodically, the two resistors can be replaced with a 20 turn, cermet potentiometer. Wirewound potentiometers should not be used for this type of application since the pot's slider jumps from winding to winding, and an exact setting can be difficult to obtain. Cermet pots allow for a smooth continuous adjustment.

In Figure 21, R1 reduces the power dissipation in the transistor, and can be carbon composition. The 0.1 µF capacitor in the feedback path provides stability in the unity gain configuration. Recommended op amps are: LM358, MC34001 series, LM308A, LM324, and LM11C. Offset drift is the key parameter to consider in choosing an op amp, and the LM308A has the lowest drift of those mentioned. Bypass capacitors are not shown in Figure 21, but should always be provided at the input to the 2.5 V reference, and at the power supply pins of the op amp.

Figure 22 shows a simpler and more economical circuit, using the LM317LZ regulator, but with lower initial accuracy and temperature stability. The op amp/current booster is not needed since the LM317LZ can supply the current directly. In a well controlled environment, this circuit will suffice for many applications. Because of the lower initial accuracy, an adjustment pot is a necessity.

Figure 23 shows two circuits for providing the voltage to V_{RB}. The circuits are similar to those of Figures 21 and 22, and have similar accuracy and stability. The output transistor is a PNP in this case since the circuit must sink the reference current.

VIDEO APPLICATIONS

The MC10319 is suitable for digitizing video signals directly without signal conditioning, although the standard 1.0 V_{pp} video signal can be amplified to a 2.0 V_{pp} signal for slightly better accuracy. Figure 24 shows the input (top trace) and reconstructed output of a standard NTSC test signal, sampled at 25 MSPS, consisting of a sync pulse, 3.58 MHz color burst, a 3.58 MHz signal in a Sin^2x envelope, a pulse, a white level signal, and a black level signal. Figure 25 shows a Sin^2x pulse that has been digitized and reconstructed at 25 MSPS. The width of the pulse is ≈450 ns at the base. Figure 26 shows an application circuit for digitizing video.

9–Bit A/D Converter

Figure 27 shows how two MC10319s can be connected to form a 9–bit converter. In this configuration, the outputs (D7 to D0) of the two 8–bit converters are paralleled. The outputs of one device are active, while the outputs of the other are in the 3–state mode. The selection is made by the Overrange output of the lower MC10319, which controls Enable inputs on the two devices. Additionally, this output provides the 9th bit.

The reference ladders are connected in series, providing the 512 steps required for 9 bits. The input voltage range is determined by V_{RT} of the upper MC10319, and V_{RB} of the lower device. A minimum of 1.0 volt is required across each converter. The 500 Ω pot (20 turn cermet) allows for adjustment of the midpoint since the reference resistors of the two MC10319s may not be identical in value. Without the adjustment, a non–equal voltage division would occur, resulting in a nonlinear conversion. If the references are to be symmetrical about ground (e.g., ± 1.0 V), the adjustment can be eliminated, and the midpoint connected to ground. The use of latches on the outputs is optional, depending on the application.

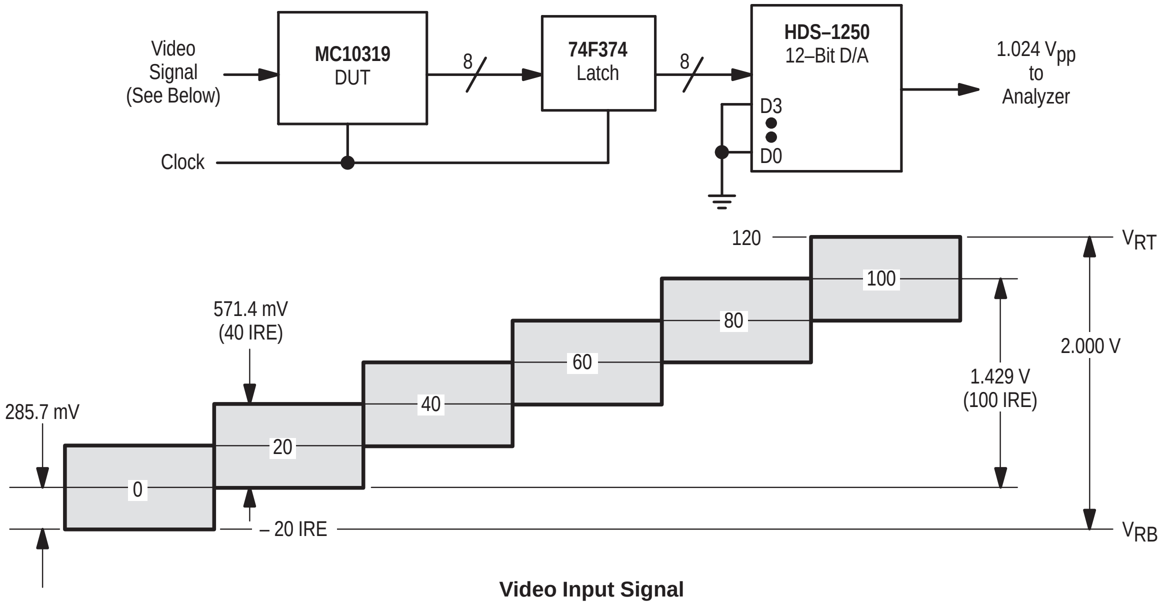
50 MHz, 8–Bit A/D Converter

Figure 28 shows how two MC10319s can be connected together in a flip–flop arrangement in order to have an effective conversion speed of 50 MHz. The 74F74 D–type flip–flop provides a 25 MHz clock to each converter, and at the same time, controls the Enables so as to alternately enable and disable the outputs. The Overranges do not have 3–state capability, and so cannot be paralleled. Instead they are OR'd together. The use of latches is optional, and depends on the application. Data should be latched, or written to RAM (in a DMA operation), on the high–to–low transition of the 50 MHz clock.

Negative Voltage Regulator

In the cases where a negative power supply is not available (neither the – 3.0 to – 6.0 V, nor a higher negative voltage from which to derive it), the circuit of Figure 29 can be used to generate – 5.0 V from the + 5.0 V supply. The PC board space required is small (≈ 2.0 in^2), and it can be located physically close to the MC10319. The MC34063A is a switching regulator, and in Figure 29 is configured in an inverting mode of operation. The regulator operating specifications are also given.

Figure 16. Differential Phase and Gain Test



Video Input Signal

1. Input waveform: 571.4 mV_{pp}, sine wave @ 3.579545 MHz, dc levels as shown above.
2. MC10319 clock at 14.31818 MHz (4x) asynchronous to input.
3. Differential gain: peak–to–peak output @ each IRE level compared to that at 0 IRE.
4. Differential phase: Phase @ each IRE level compared to that @ 0 IRE.

Figure 17. Representative Block Diagram

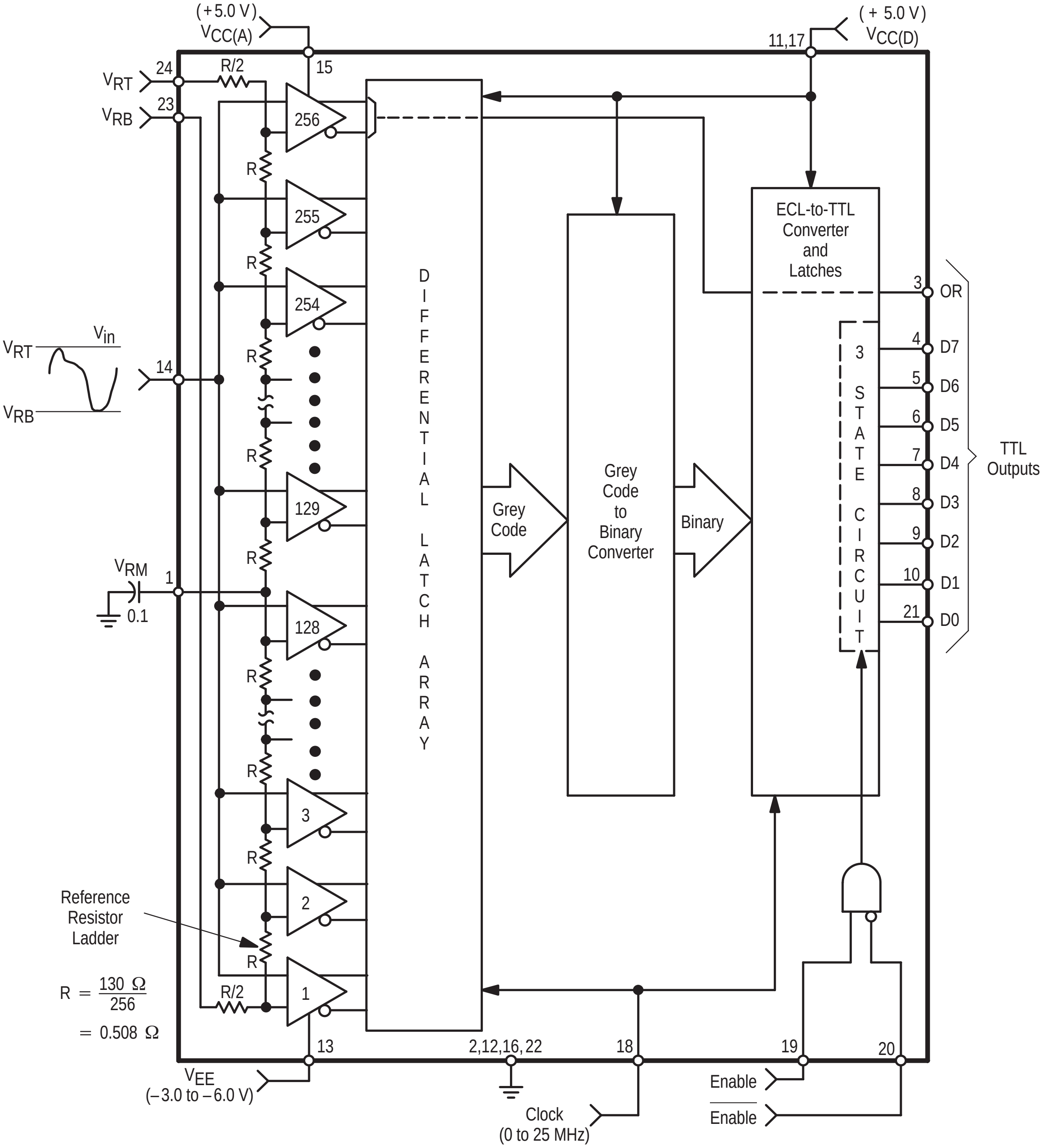


Figure 18. Adjusting V_{RM} for Improved Linearity

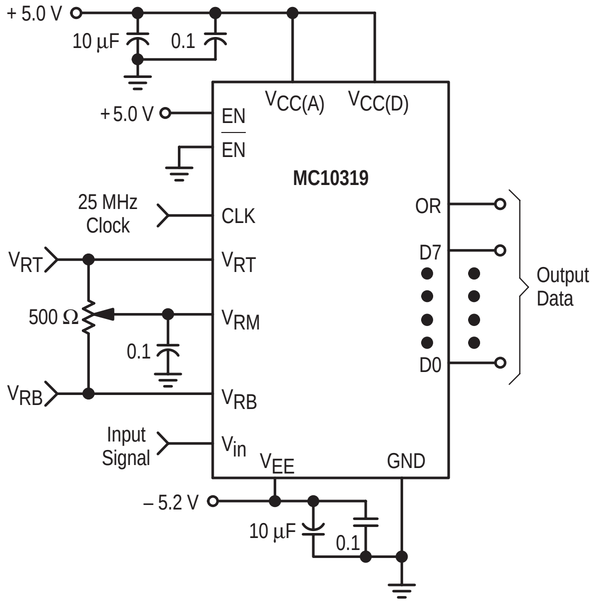


Figure 19. Conversion Sequence

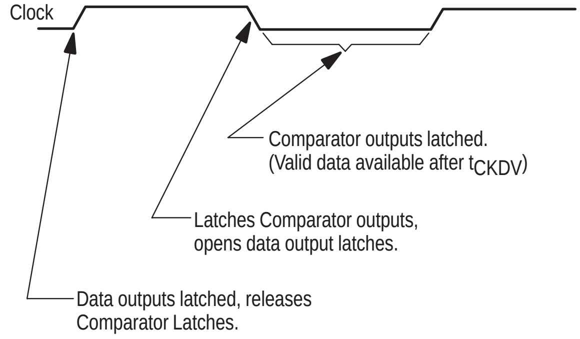
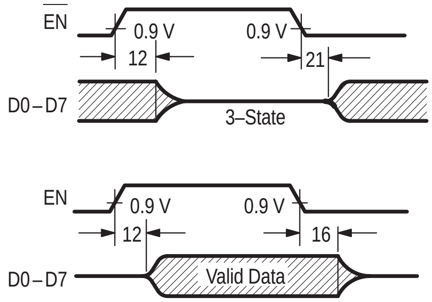
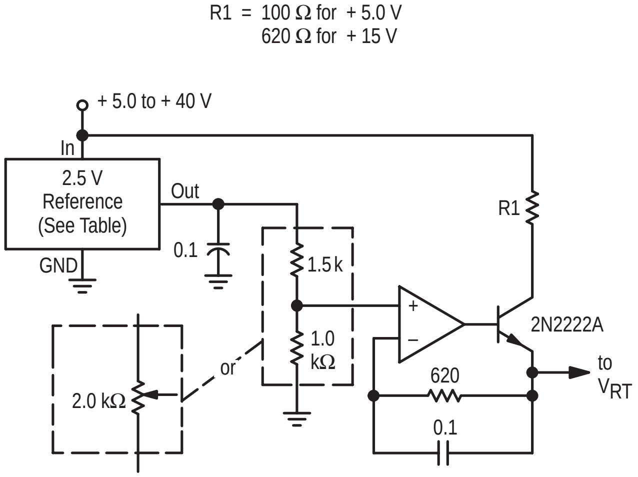


Figure 20. Enable to Output Critical Timing



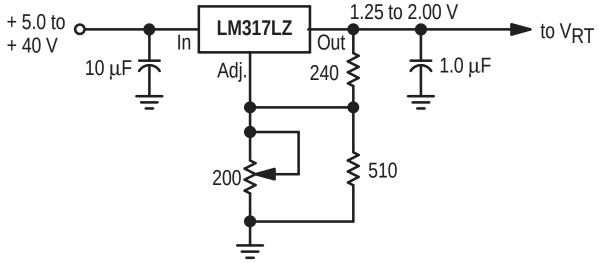
Timing @ D7 to D0 measured where waveform starts to change.
Indicated time values are typical @ 25°C, and are in ns.

Figure 21. Precision V_{RT} Voltage Source



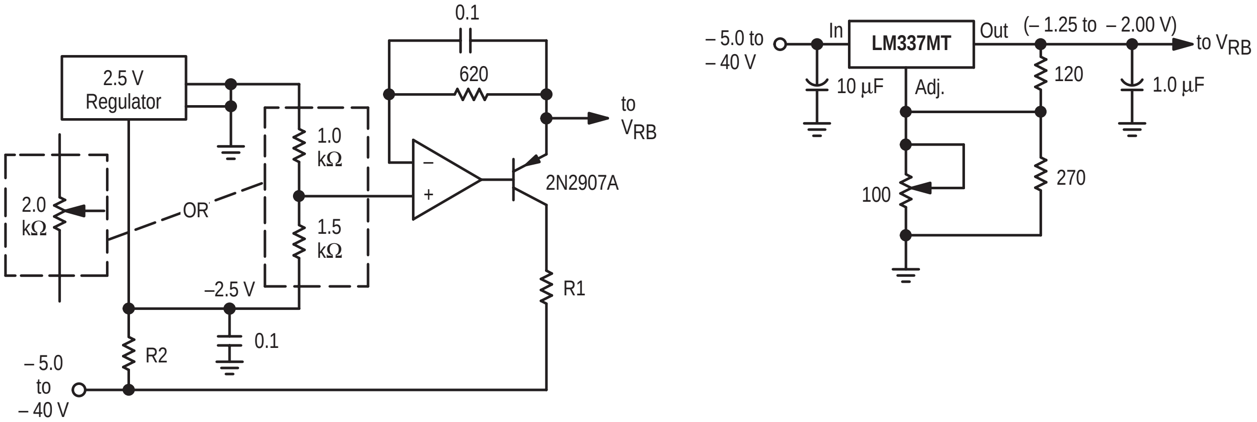
2.5 V References	MC1403	MC1403A
Line Regulation	0.5 mV	0.5 mV
T_C (ppm/°C) max	40	25
ΔV_{out} for 0 to +70°C	7.0 mV	4.4 mV
Initial Accuracy	± 1%	± 1%

Figure 22. Voltage Source for V_{RT} Pin



LM317LZ	
Line Regulation	1.0 mV
T_C (ppm/°C) max	60
ΔV_{out} for 0 to +70°C	8.4 mV
Initial Accuracy	± 4%

Figure 23. Voltage Sources for V_{RB} Pin



R1 = 100 Ω for –5.0 V
   = 620 Ω for –15 V

R2 = 620 Ω for –5.0 V
   = 3.0 kΩ for –15 V

2.5 V Reference	LM337MT
Line Regulation	1.0 mV
T_C (ppm/°C) max	48
ΔV_{out} for 0 to +70°C	6.7 mV
Initial Accuracy	±4%

Figure 24. Composite Video Waveform

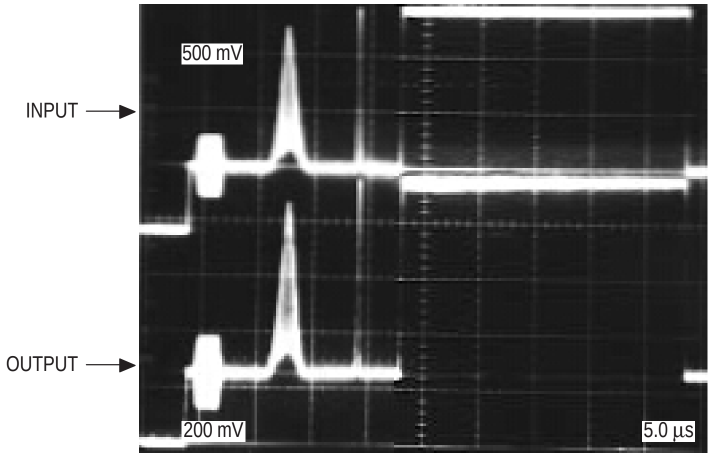


Figure 25. SIN^2 x Waveform

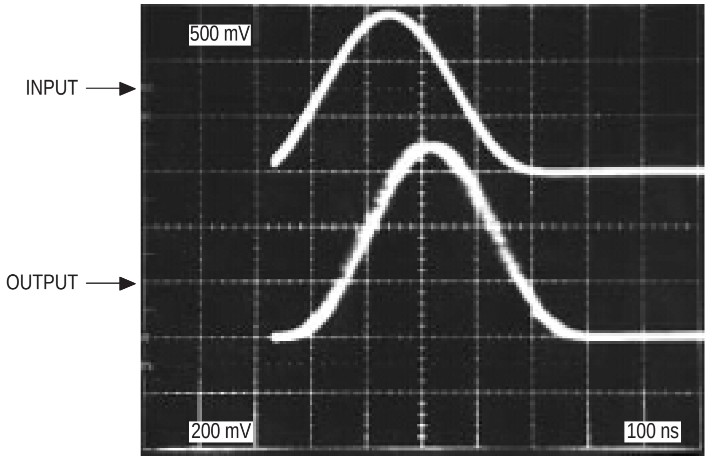
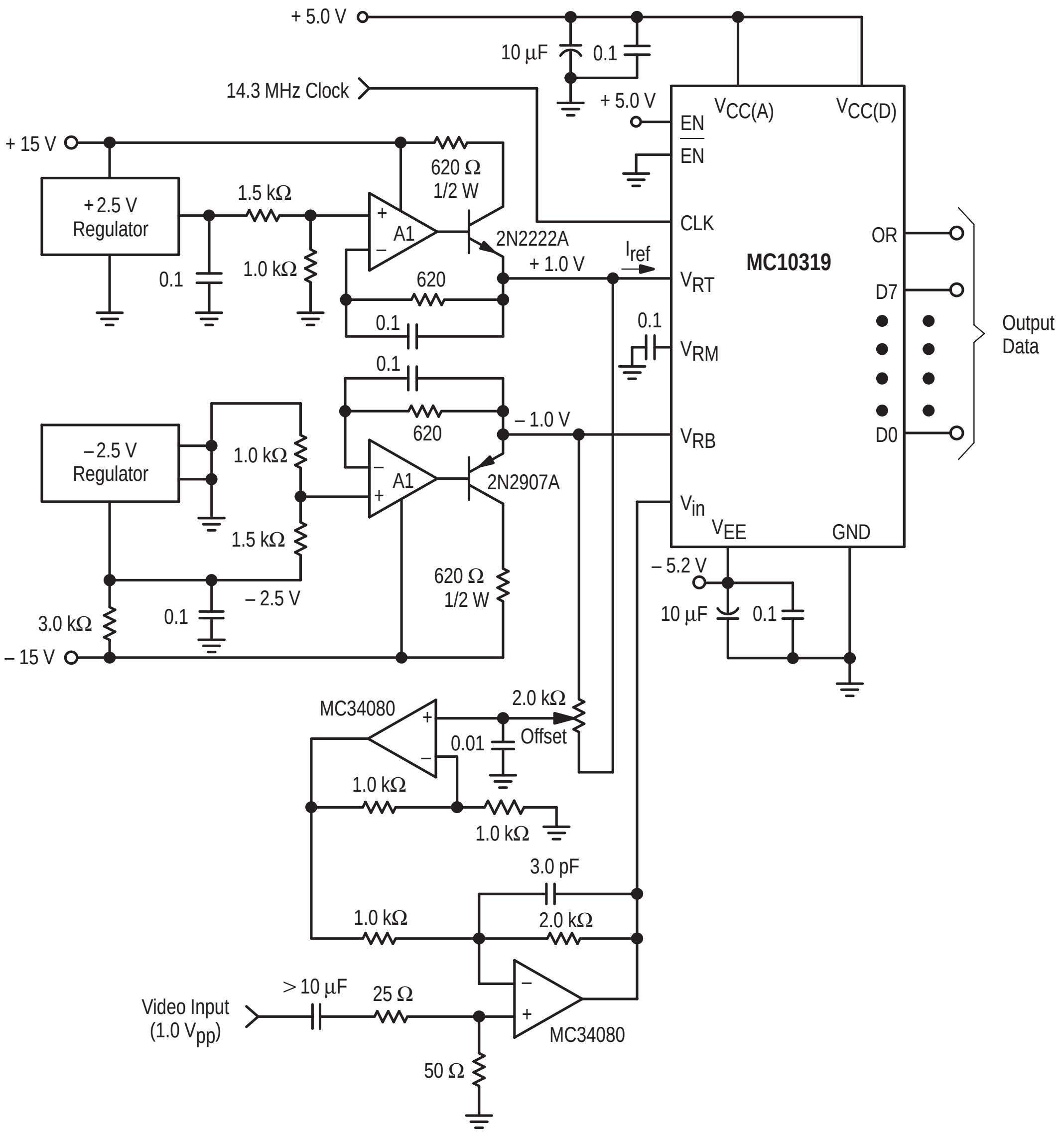


Figure 26. Application Circuit for Digitizing Video



NOTES: 1) MC34080′s powered from ± 15 V supplies. MC34083 (Dual) may be used.
2) Bypass capacitors required at power supply pins of **all** ICs.
3) Ground plane required over all parts of circuit board.
4) Care in layout around MC34080′s necessary for good frequency response.
5) A1 = MC34002.

Figure 27. 9–Bit A/D Converter

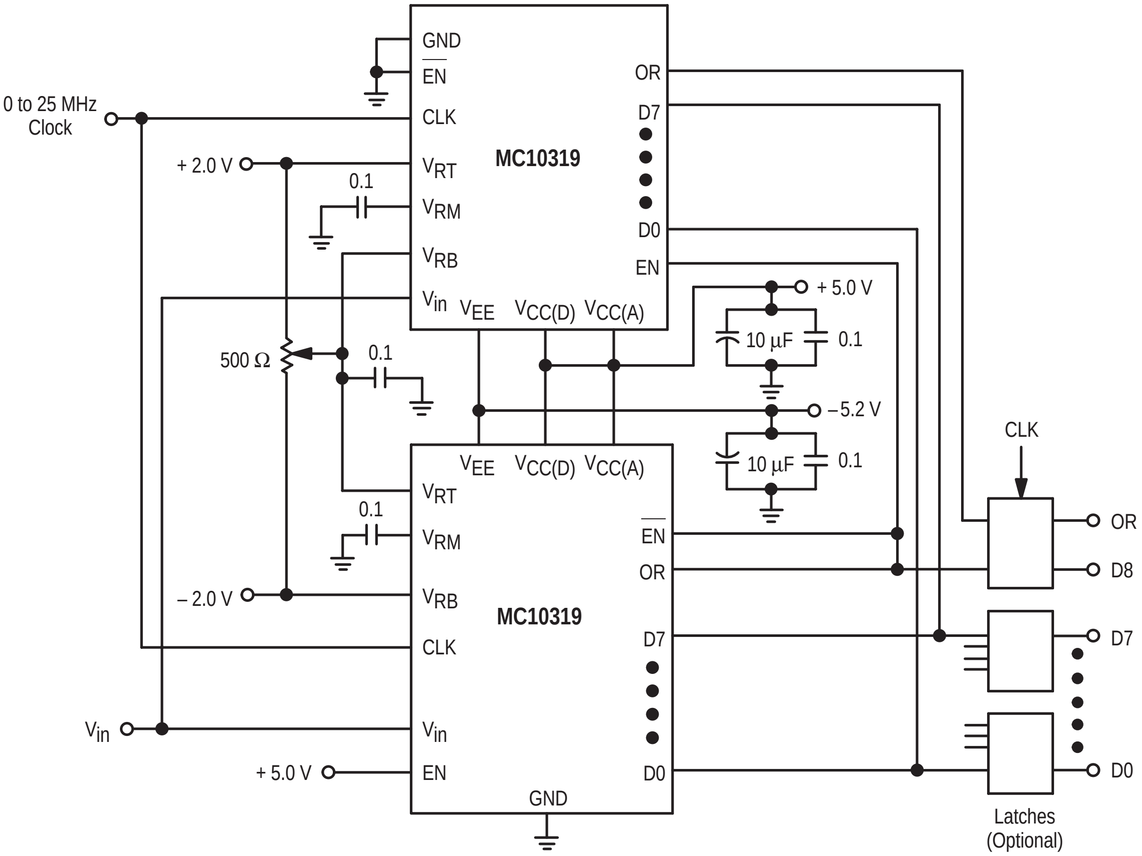


Figure 28. 50 MHz 8–Bit A/D Converter

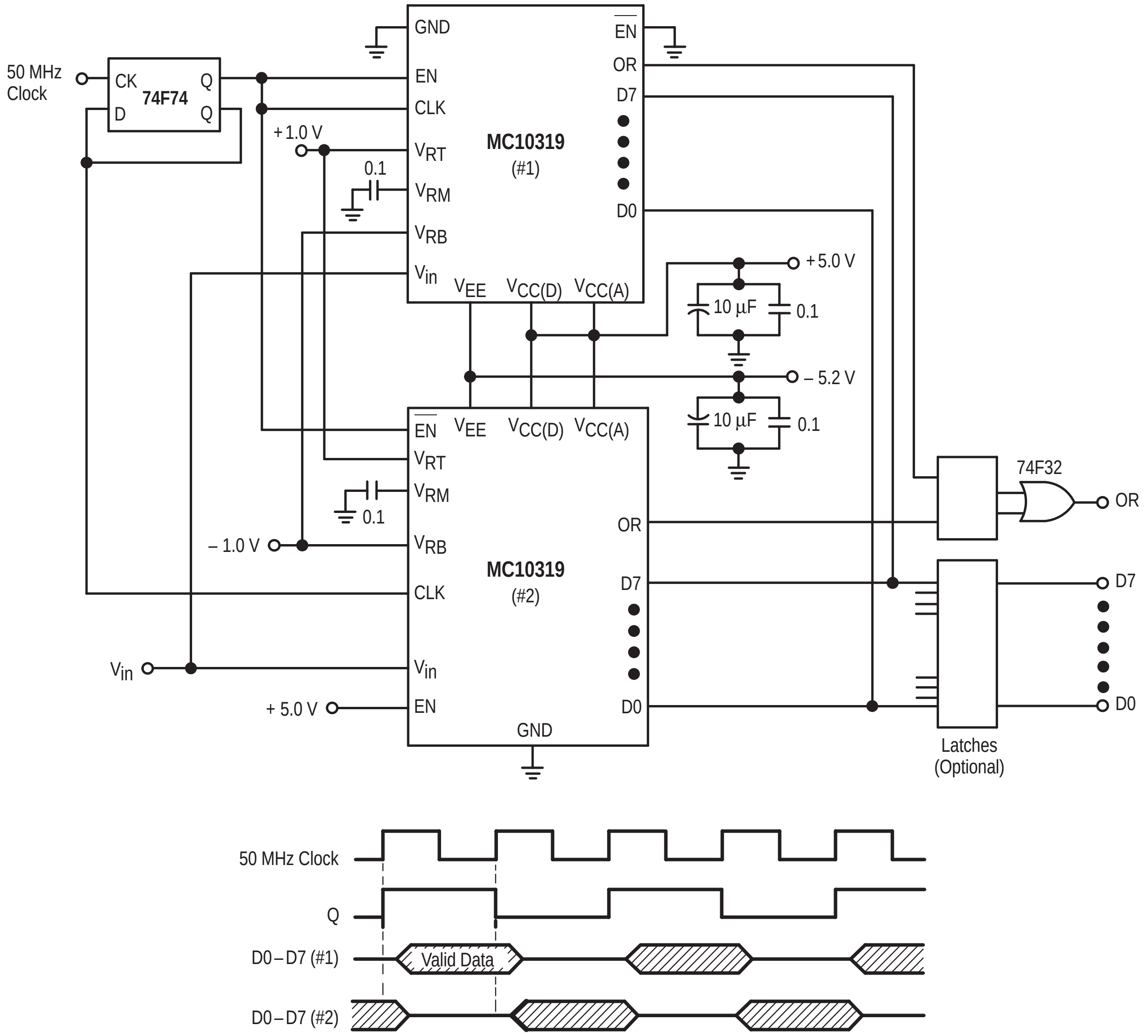
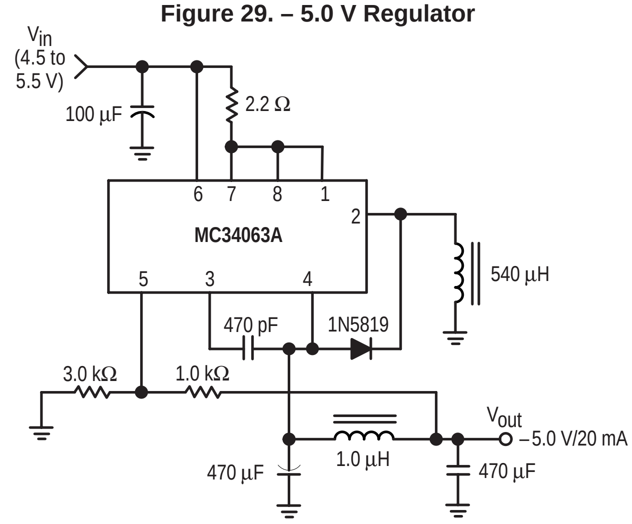


Figure 29. – 5.0 V Regulator



Test	Conditions	Results
Line Regulation	4.5 V $<$ V_{in} $<$ 5.5 V, I_{out} = 10 mA	0.16%
Load Regulation	V_{in} = 5.0 V, 8.0 mA $<$ I_{out} $<$ 20 mA	0.4%
Output Ripple	V_{in} = 5.0 V, I_{out} = 20 mA	2.0 mV_{pp}
Short Circuit I_{out}	V_{in} = 5.0 V, R1 = 0.1 Ω	140 mA
Efficiency	V_{in} = 5.0 V, I_{out} = 50 mA	52%

GLOSSARY

Aperture Delay – The time difference between the sampling signal (typically a clock edge) and the actual analog signal converted. The actual signal converted may occur before or after the sampling signal, depending on the internal configuration of the converter.

Bipolar Input – A mode of operation whereby the analog input (of an A/D), or output (of a DAC), includes both negative and positive values. Examples are – 1.0 to + 1.0 V, – 5.0 to + 5.0 V, – 2.0 to + 8.0 V, etc.

Bipolar Offset Error – The difference between the actual and ideal locations of the 00_H to 01_H transition, where the ideal location is 1/2 LSB above the most negative reference voltage.

Bipolar Zero Error – The error (usually expressed in LSBs) of the input voltage location (of an A/D) of the 80_H to 81_H transition. The ideal location is 1/2 LSB above zero volts in the case of an A/D setup for a symmetrical bipolar input (e.g., – 1.0 to + 1.0 V).

Differential Nonlinearity – The maximum deviation in the actual step size (one transition level to another) from the ideal step size. The ideal step size is defined as the Full Scale Range divided by 2^n (n = number of bits). This error must be within ± 1 LSB for proper operation.

ECL – Emitter coupled logic.

Full Scale Range (Actual) – The difference between the actual minimum and maximum end points of the analog input (of an A/D).

Full Scale Range (Ideal) – The difference between the actual minimum and maximum end points of the analog input (of an A/D), plus one LSB.

Gain Error – The difference between the actual and expected gain (end point to end point), with respect to the reference, of a data converter. The gain error is usually expressed in LSBs.

Grey Code – Also known as *reflected binary code*, it is a digital code such that each code differs from adjacent codes by only one bit. Since more than one bit is never changed at each transition, race condition errors are eliminated.

Integral Nonlinearity – The maximum error of an A/D, or DAC, transfer function from the ideal straight line connecting the analog end points. This parameter is sensitive to dynamics, and test conditions must be specified in order to be meaningful. This parameter is the best overall indicator of the device′s performance.

Line Regulation – The ability of a voltage regulator to maintain a certain output voltage as the input to the regulator is varied. The error is typically expressed as a percent of the nominal output voltage.

Load Regulation – The ability of a voltage regulator to maintain a certain output voltage as the load current is varied. The error is typically expressed as a percent of the nominal output voltage.

LSB – Least Significant Bit. It is the lowest order bit of a binary code.

Monotonicity – The characteristic of the transfer function whereby increasing the input code (of a DAC), or the input signal (of an A/D), results in the output never decreasing.

MSB – Most Significant Bit. It is the highest order bit of a binary code.

Natural Binary Code – A binary code defined by:

$$N = A_n 2^n + \ldots + A_3 2^3 + A_2 2^2 + A_1 2^1 + A_0 2^0$$

where each “A” coefficient has a value of 1 or 0. Typically, all zeroes correspond to a zero input voltage of an A/D, and all ones correspond to the most positive input voltage.

Nyquist Theorem – See Sampling Theorem.

Offset Binary Code – Applicable only to bipolar input (or output) data converters, it is the same as Natural Binary, except that all zeros correspond to the most negative input voltage (of an A/D), while all ones correspond to the most positive input.

Power Supply Sensitivity – The change in a data converter′s performance with changes in the power supply voltage(s). This parameter is usually expressed in percent of full scale versus ΔV.

Quantitization Error – Also known as *digitization error* or uncertainty. It is the inherent error involved in digitizing an analog signal due to the finite number of steps at the digital output versus the infinite number of values at the analog input. This error is a minimum of ± 1/2 LSB.

Resolution – The smallest change which can be discerned by an A/D converter, or produced by a DAC. It is usually expressed as the number of bits (n), where the converter has 2^n possible states.

Sampling Theorem – Also known as the *Nyquist Theorem.* It states that the sampling frequency of an A/D must be no less that 2x the highest frequency (of interest) of the analog signal to be digitized in order to preserve the information of that analog signal.

Unipolar Input – A mode of operation whereby the analog input range (of an A/D), or output range (of a DAC), includes values of a signal polarity. Examples are 0 to + 2.0 V, 0 to – 5.0 V, 2.0 to 8.0 V, etc.

Unipolar Offset Error – The difference between the actual and ideal locations of the 00_H to 01_H transition, where the ideal location is 1/2 LSB above the most negative input voltage.

Interface Circuits

In Brief . . .

Described in this section is Motorola's line of interface circuits, which provide the means for interfacing with microprocessor or digital systems and the external world, or to other systems.

Also included are devices which allow a microprocessor to communicate with its own array of memory and peripheral I/O circuits.

The line drivers, receivers, and transceivers permit communication between systems over cables of several thousand feet in length, and at data rates of up to several megahertz. The common EIA data transmission standards, several European standards, and IEEE–488 are addressed by these devices.

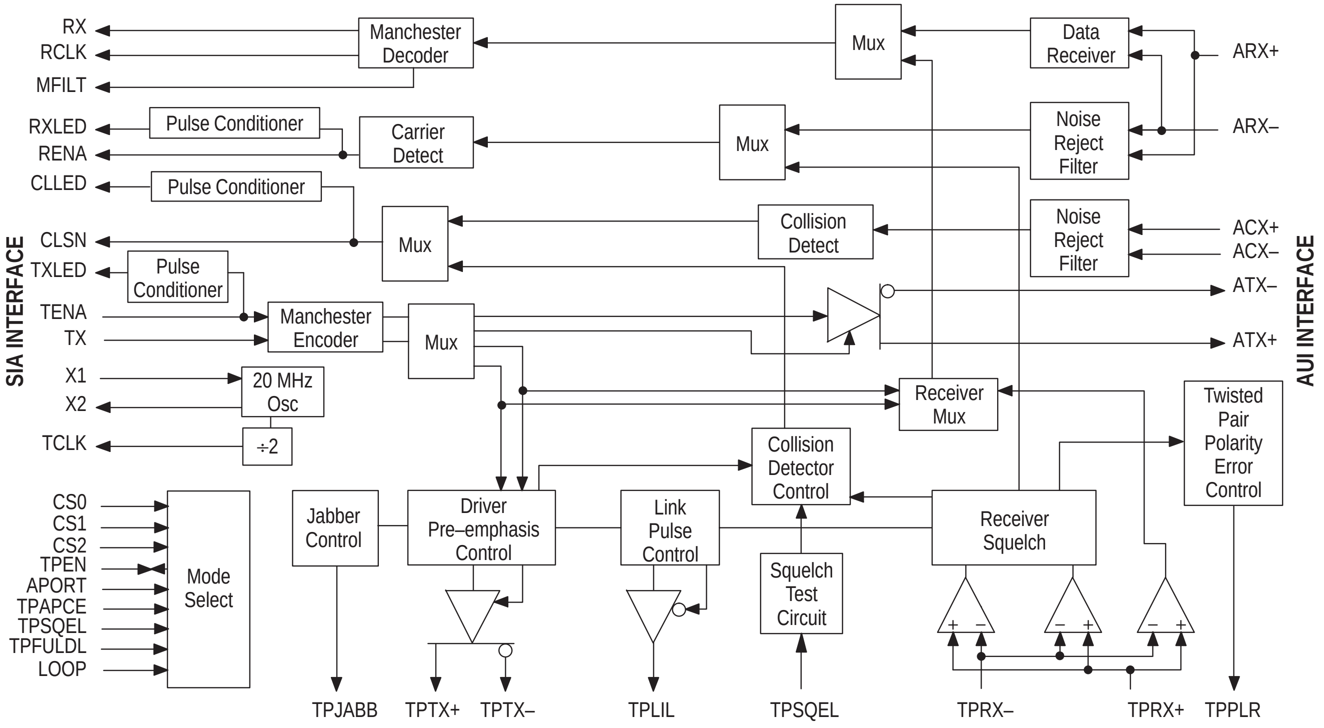
The peripheral drivers are designed to handle high current loads such as relay coils, lamps, stepper motors, and others. Input levels to these drivers can be TTL, CMOS, high voltage MOS, or other user defined levels. The display drivers are designed for LCD or LED displays, and provide various forms of decoding.

Enhanced Ethernet Transceiver

MC68160FB

T_A = 0° to +70°C, Case 848D

The MC68160 Enhanced Ethernet Interface Circuit is a BiCMOS device which supports both IEEE 802.3 Access Unit Interface (AUI) and 10BASE–T Twisted Pair (TP) Interface media connections through external isolation transformers. It encodes NRZ data to Manchester data and supplies the signals which are required for data communication via 10BASE–T or AUI interfaces. The MC68160 gluelessly interfaces to the Ethernet controller contained in the MC68360 Quad Integrated Communications Controller (QUICC) device. The MC68160 also interfaces easily to most other industry–standard IEEE 802.3 LAN controllers. Prior to twisted pair data reception, Smart Squelch circuitry qualifies input signals for correct amplitude, pulse width, and sequence requirements.

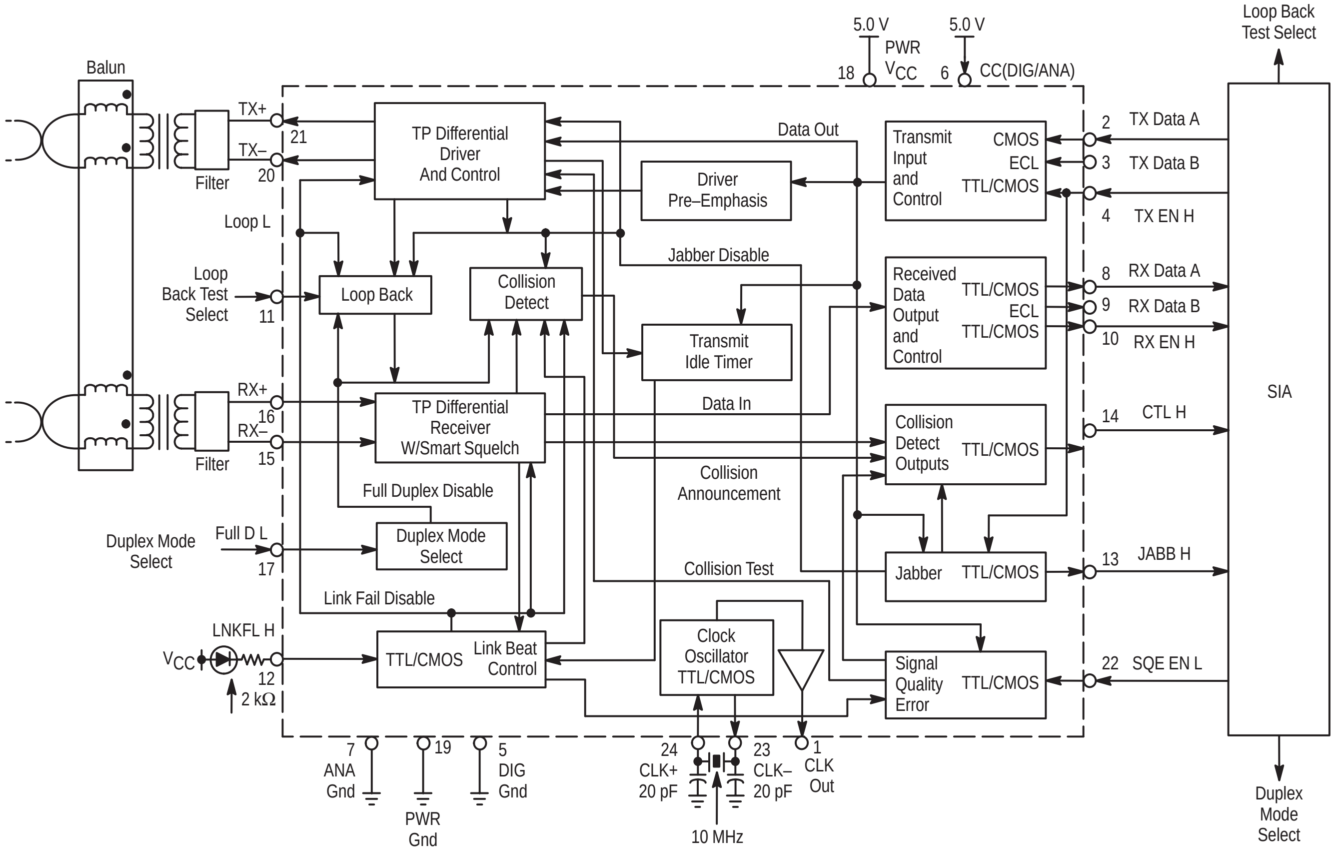


ISO 8802–3[IEEE 802.3] 10BASE–T Transceiver

MC34055DW

T_A = 0° to +70°C, Case 751E

The Motorola 10BASE–T transceiver, designed to comply with the ISO 8802–3[IEEE 802.3] 10BASE–T specification, will support a Medium Dependent Interface (MDI) in an embedded Media Attachment Unit (MAU). The interface supporting the Data Terminal Equipment (DTE) is TTL, CMOS, and raised ECL compatible, and the interface to the Twisted Pair (TP) media is supported through standard 10BASE–T filters and transformers. Differential data intended for the TP media is provided a 50 ns pre–emphasis and data at the TP receiver, is screened by Smart Squelch circuitry for specific threshold, pulse width, and sequence requirements.



Hex EIA–485 Transceiver with Three–State Outputs

MC34058/59FTA

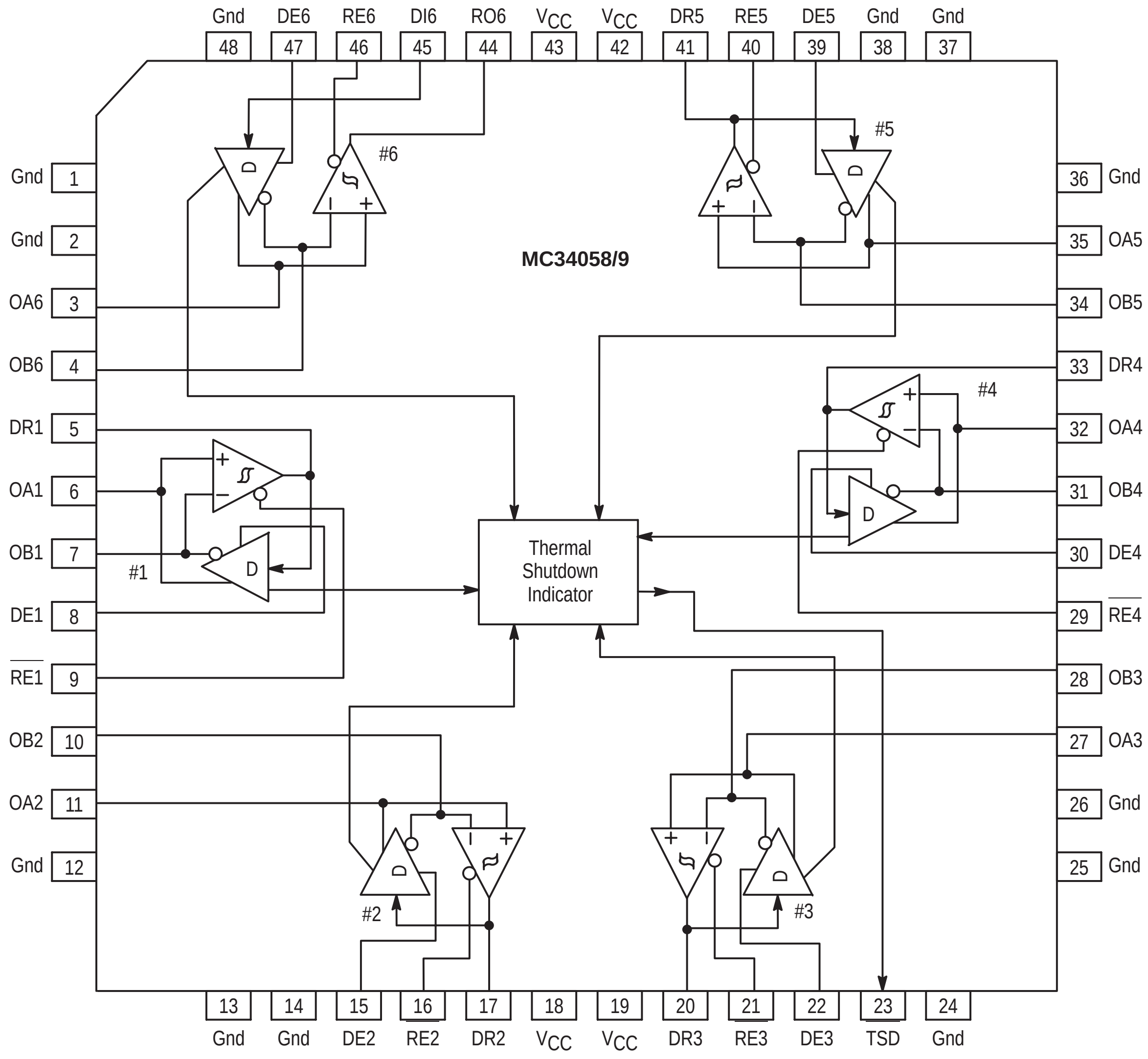
T_A = 0° to +70°C, Case 932

The Motorola MC34058/9 Hex Transceiver is composed of six driver/receiver combinations designed to comply with the EIA–485 standard. Features include three–state outputs, thermal shutdown for each driver, and current limiting in both directions. This device also complies with EIA–422 and CCITT Recommendations V.11 and X.27.

The devices are optimized for balanced multipoint bus transmission at rates to 20 MBPS (MC34059). The driver outputs/receiver inputs feature a wide common mode voltage range, allowing for their use in noisy environments. The current limit and thermal shutdown features protect the devices from line fault conditions.

The MC34058/9 is available in a space saving 7.0 mm 48 lead surface mount quad package designed for optimal heat dissipation.

- Meets EIA–485 Standard for Party Line Operation
- Meets EIA–422A and CCITT Recommendations V.11 and X.27
- Operating Ambient Temperature: 0°C to +70°C
- Common Mode Driver Output/Receiver Input Range: –7.0 to +12 V
- Positive and Negative Current Limiting
- Transmission Rates to 14 MBPS (MC34058) and 20 MBPS (MC34059)
- Driver Thermal Shutdown at 150°C Junction Temperature
- Thermal Shutdown Active Low Output
- Single +5.0 V Supply, ±10%
- Low Supply Current
- Compact 7.0 mm 48 Lead TQFP Plastic Package
- Skew Specified for MC34059



5.0 V, 200 M–Bit/Sec PR–IV Hard Disk Drive Read Channel

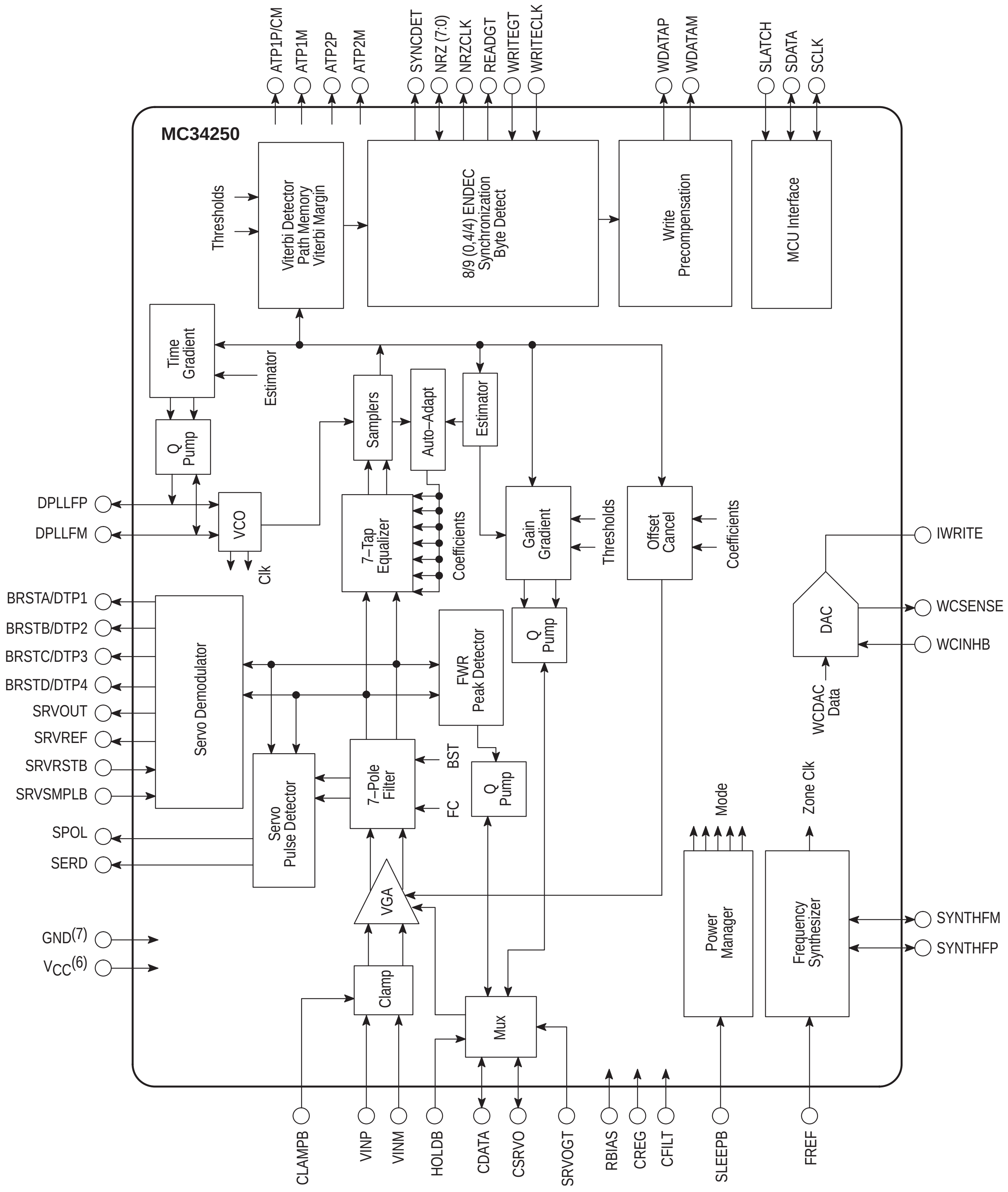
MC34250FTA

T_A = 0° to +70°C, Case 840F

The Motorola MC34250 is a fully integrated partial response maximum likelihood disk drive read/write channel for use in zoned recording applications. This device integrates the AGC, active filter, 7 tap equalizer, Viterbi detector, frequency synthesizer, servo demodulator, 8/9 rate (0,4/4) Encoder/Decoder with write precompensation and power management in a single 64 pin 10 mm x 10 mm TQFP package.

FEATURES:

- 50 to 200 MBPS Programmable Data Rate
- 800 mW at 200 MBPS and 5.0 V
- Channel Monitor Output
- Programmable AGC Charge Pump Currents with Different Values for Data and Servo Envelope Modes and Gain Gradient Mode
- Programmable AGC Peak Detector Droop Currents with Different Values for Data and Servo Envelope Modes
- Separate AGC Charge Pump Outputs for Data and Servo Modes
- Programmable Dual Threshold Qualifier or Hysteresis Comparator Type Pulse Detector for Servo Data Detection.
- ERD and Polarity Outputs for Servo Timing and Raw Encoded Data
- Integrated 7 pole 0.05° Equiripple Linear Phase Filter with Programmable Bandwidth from 5.0 MHz to 80 MHz and Different Values for Both Data and Servo Modes
- Programmable Symmetrical Boost from 0 to 10 dB and Different Values for Data and Servo Modes
- Programmable Asymmetrical Boost of Up to ±40% of Nominal Filter Group Delay in Both Data and Servo Modes
- 7 Tap Continuous Time Transversal Equalizer with 8 Bit Programmable Tap Weights and Integrated Decision Directed Sign–Sign Least Mean Squared Adaptation
- Internal Offset Cancellation Loops
- Fast Acquisition Data Phase Locked Loop with Zero Phase Restart
- Programmable Data Phase Locked Loop Charge Pump Current
- Integrated Soft Decision Viterbi Detectors with Programmable Merge References
- Integrated 8/9 Rate (0,4/4) Encoder and Decoder with Code Scrambler and Descrambler
- Programmable 2/4/8 Bit NRZ Data Interface
- Programmable Write Precompensation Delays Locked to the Frequency Synthesizer
- Differential PECL Write Data Outputs
- External Write Data Path for DC Erase or Other Non–Encoded Data
- Integrated Write Current DAC
- Programmable Power Management
- Bi–Directional Serial Microprocessor Interface
- Various Test Modes Controlled Via the Serial Microprocessor Interface


ATP1P/CM
ATP1M
ATP2P
ATP2M
SYNCDET
NRZ (7:0)
NRZCLK
READGT
WRITEGT
WRITECLK
WDATAP
WDATAM
SLATCH
SDATA
SCLK
MC34250
Thresholds
Viterbi Detector
Path Memory
Viterbi Margin
8/9 (0,4/4) ENDEC
Synchronization
Byte Detect
Write
Precompensation
MCU Interface
Time
Gradient
Estimator
Samplers
Auto–Adapt
Estimator
Q
Pump
DPLLFP
DPLLFM
VCO
Clk
7–Tap
Equalizer
Coefficients
Gain
Gradient
Thresholds
Offset
Cancel
Coefficients
IWRITE
BRSTA/DTP1
BRSTB/DTP2
BRSTC/DTP3
BRSTD/DTP4
SRVOUT
SRVREF
SRVRSTB
SRVSMPLB
Servo Demodulator
FWR
Peak Detector
Q
Pump
DAC
WCSENSE
WCINHB
WCDAC
Data
Servo
Pulse Detector
7–Pole
Filter
BST
FC
Q
Pump
Mode
Zone Clk
SPOL
SERD
VGA
Power
Manager
Frequency
Synthesizer
SYNTHFM
SYNTHFP
GND(7)
VCC(6)
Clamp
Mux
CLAMPB
VINP
VINM
HOLDB
CDATA
CSRVO
SRVOGT
RBIAS
CREG
CFILT
SLEEPB
FREF

Microprocessor Bus Interface

Motorola offers a spectrum of line drivers and receivers which provide interfaces to many industry standard specifications. Many of the devices add key operational features, such as hysteresis, short circuit protection, clamp diode protection, or special control functions.

Table 1. Magnetic Read/Write

Device	Comments	T_A (°C)	Suffix/ Package
MC3467*	Magnetic Tape Sense Amplifier. Trace independent preamplifiers with individual gain control. Optimized for use with 9–track magnetic tape memory systems.	0 to + 70	P/707

* Not recommended for new designs.

Single–Ended Bus Transceivers

Table 2. For Instrumentation Bus, Meets GPIB/IEEE Standard 488

Driver Characteristics		Receiver Characteristics				
Output Current (mA)	Propagation Delay Max (ns)	Propagation Delay Max (ns)	Transceivers Per Package	Device	Suffix/ Package	Comments
48	17	25	4	MC3448A*	P/648, D/751B	Input hysteresis, open collector, 3–state outputs with terminations

*Not recommended for new designs.

Table 3. For High Current Party–Line Bus for Industrial and Data Communications

Driver Characteristics		Receiver Characteristics				
Output Current (mA)	Propagation Delay Max (ns)	Propagation Delay Max (ns)	Transceivers Per Package	Device	Suffix/ Package	Comments
100	15	15	4	MC26S10*	P/648, D/751B	Open collector outputs, common enable

*Not recommended for new designs.

Line Receivers

Table 4. General Purpose

S = Single Ended D = Differential	Type of Output	t_{prop} Delay Time Max (ns)	Party Line Opera–tion	Strobe or Enable	Power Supplies (V)	Device	Suffix/ Package	Receivers Per Package	Companion Drivers	Comments
D	TP OC(1)	25	✓	✓	± 5.0	MC3450*	P/648	4	MC3453	Quad

(1) OC = Open Collector, TP = Totem–pole output.
* Note recommended for new designs.

Table 5. EIA Standard

S = Single Ended D = Differential	Type of Output	t_{prop} Delay Time Max (ns)	Party Line Opera–tion	Strobe or Enable	Power Supplies (V)	Device	Suffix/ Package	Receivers Per Package	Companion Drivers	Comments
S	TP	4000	–	–	+5.0	MC14C89B, AB	P/646, D/751A	4	MC1488 MC14C88B	EIA–232–D/ EIA–562
	R(1)	85	–	–		MC1489 MC1489A				EIA–232–D
S, D	TP	30	✓	✓		AM26LS32*	PC/648		AM26LS31*	EIA–422/423
		35				SN75175	N/648, D/751B		MC75174B	EIA–422/423/ 485

(1) R = Resistor Pull–up, TP = Totem–pole output.
* Not recommended for new designs.

Line Drivers

Table 6. EIA Standard

Output Current Capa–bility (mA)	t_{prop} Delay Time Max (ns)	S = Single Ended D = Differ-ential	Party Line Opera–tion	Strobe or Enable	Power Supplies (V)	Device	Suffix/ Package	Drivers Per Package	Companion Receivers	Comments
85	35	D	✓	✓	+5.0	MC75174B MC75172B	P/648	4	SN75175	EIA–485
48	20					AM26LS31*	PC/648		MC3486 AM26LS32*	EIA–422 with 3–state outputs
						MC26LS31	D/751B			
15	3500	S	–		±7.0 to ±12	MC14C88B	P/646, D/751A		MC14C89B MC14C89AB	EIA–232–D/ EIA–562
10	350				±9.0 to ±12	MC1488			MC1489 MC1489A	EIA–232–D
60	300	S/D		EIA–422 ✓ EIA–423 –	±5.0	AM26LS30	PC/648	2 (422) 4 (423)	AM26LS32*	EIA–422 or EIA–423 Switchable
						MC26LS30	D/751B			

* Not recommended for new designs.

Table 7. Line Transceivers

Driver Prop Delay (Max ns)	Receiver Prop Delay Max (ns)	DE = Driver Enable RE = Receiver Enable	Party Line Operation	Power Supplies (V)	Device	Suffix/ Package	Drivers Per Package	Receivers Per Package	EIA Standard
23	23	DE, RE	✓	+5.0	MC34058	FTA/932	6	6	EIA–485 to 14 MBPS
					MC34059	FTA/932	6	6	EIA–485 to 20 MBPS

Table 8. EIA–232–E/V.28 CMOS Drivers/Receivers

Device	Suffix/ Package	Pins	Drivers	Receivers	Power Supplies (V)	Features
MC145403	P/738, DW/751D	20	3	5	±5.0 to ±12	
MC145404			4	4		
MC145405			5	3		
MC145406	P/648, DW/751G, SD/940B	16	3			
MC145407	P/738, DW/751D	20			+5.0	Charge Pump
MC145408	P/724, DW/751E, SD/940B	24	5	5	±5.0 to ±12	
MC145583	DW/751F, VF/940J	28	3	5	+3.3 to +5.0	On–board ring monitor circuit; charge pump, power down
MC145705	P/738, DW/751D	20	2	3	+5.0	Charge Pump, Power Down
MC145706			3	2		
MC145707	P/724, DW/751E	24		3		

Table 9. Peripheral Drivers

Output Current Capability (mA)	Input Capability	Propagation Delay Time Max (μs)	Output Clamp Diode	Off State Voltage Max (V)	Device	Drivers Per Package	Suffix/ Package	Logic Function
500	TTL, CMOS	1.0	✓	50	ULN2803	8	A/707	Invert
	6.0 V to 15 V MOS				ULN2804			
	TTL, 5.0 V CMOS				MC1413, B (ULN2003A)	7	P/648, D/751B P/648, D/751B	
	8.0 V to 18 V MOS				MC1416, B (ULN2004A)			
1500	TTL, 5.0 V CMOS	1.0	✓	50	ULN2068*	4	B/648C	Invert

* Not recommended for new designs.

Table 10. IEEE 802.3 Transceivers

Device	Power Supply	10 BaseT	NRZ	IEEE	Comments	Suffix/ Package
MC34055	+5.0 Vdc	Transmit and Receive over 4 Pins	Raised ECL, CMOS	802.3 Type 10BaseT	Transceiver with non–return to zero (NRZ) interface. Intended for but not restricted to concentrators and repeator applications.	DW/751E
MC68160			TTL, CMOS	802.3 Type 10BaseT/ AUI/NRZ	Interfaces gluelessly to Motorola’s MC68360 communications controller.	FB/848D

Read/Write Channel

Table 11. Hard Disk Drive Read Channel

Device	Power Supply	Comments	T_A (°C)	Suffix/ Package
MC34250	5.0 V	200 Mbps fully integrated partial response maximum likelihood hard disk drive read/write channel which equalizes to a PR–IV shape and uses 8/9 rate (0, 4/4) coding.	0 to +70	FTA/840F

Inkjet Drivers

Table 12. 28–Channel Inkjet Driver

Device	Power Supply	Comments	T_A (°C)	Suffix/ Package
MC34156	5.0 V	A 4 to 14 line decoder determines the selected output driver in each of two 14 driver banks. Two independent output enable lines permit 1 or 2 of 28 outputs. Outputs are open collector 30 V Darlington drivers capable of sinking 500 mA.	0 to +70	FN/777

CMOS Display Drivers

These CMOS devices include digit as well as matrix drivers for LEDs, LCDs, and VFDs. They find applications over a wide range of end equipment such as instruments, automotive dashboards, home computers, appliances, radios and clocks.

Table 13. Display Drivers

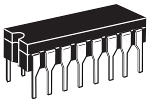
Display Type	Input Format	Drive Capability Per Package	On–Chip Latch	Display Control	Segment Drive Current	Device
LCD (Direct Drive)	Parallel BCD	7 Segments	✓	Blank	≈ 1.0 mA	MC14543B
				Blank, Ripple Blank		MC14544B
	Serial Binary [Compatible with the Serial Peripheral Interface (SPI) on CMOS MCUs]	33 Segments or Dots			20 µA	MC145453
Muxed LCD (1/4 Mux)		48 Segments or Dots			≈ 200 µA	MC145000
		44 Segments or Dots				MC145001
LED, Incandescent, Fluorescent(1)	Parallel BCD	7 Segments		Blank, Lamp Test	25 mA	MC14511B
				Blank, Ripple Blank, Lamp Test		MC14513B
			–	Blank	65 mA	MC14547B
Muxed LED (1/4 Mux)	Serial Binary [Compatible with the Serial Peripheral Interface (SPI) on CMOS MCUs]	4 Digits + Decimals	✓	Oscillator (Scanner)	50 mA (Peak)	MC14499
Muxed LED (1/5 Mux)		5 Characters + Decimals or 25 Lamps		Oscillator (Scanner), Low Power Mode, Dimming	0 to 35 mA (Peak) Adjustable	MC14489
LED (Direct Drive)	Parallel Hex	7 Segments + A thru F Indicator			10 mA(2)	MC14495–1
(Interfaces to Display Drivers)	Parallel BCD	7 Segments	–	Ripple Blank, Enable	–	MC14558B

(1) Absolute maximum working voltage = 18 V.
(2) On–chip current–limiting resistor.

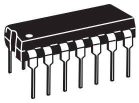
Table 14. Functions

Device	Function	Package
MC14489	Multi–Character LED Display/Lamp Driver	738, 751D
MC14495–1	Hexadecimal–to–7 Segment Latch/Decoder ROM/Driver	648, 751G
MC14499	4–Digit 7–Segment LED Display Decoder/Driver with Serial Interface	707, 751D
MC14511B	BCD–to–7–Segment Latch/Decoder/Driver	648, 751G
MC14513B	BCD–to–7–Segment Latch/Decoder/Driver with Ripple Blanking	726, 707
MC14543B	BCD–to–7–Segment Latch/Decoder/Driver for Liquid Crystals	620, 648
MC14544B	BCD–to–7–Segment Latch/Decoder/Driver with Ripple Blanking	726, 707
MC14547B	High–Current BCD–to–7–Segment Decoder/Driver	620, 648
MC14558B	BCD–to–7–Segment Decoder	620, 648
MC145000	48–Segment Serial Input Multiplexed LCD Driver (Master)	709, 776
MC145001	44–Segment Serial Input Multiplexed LCD Driver (Slave)	707, 776
MC145453	33–Segment, Non–Multiplexed LCD Driver with Serial Interface	711, 777

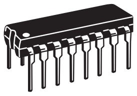
Interface Circuits Package Overview



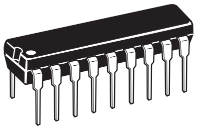
CASE 620



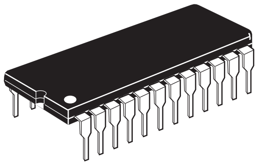
CASE 646
P SUFFIX



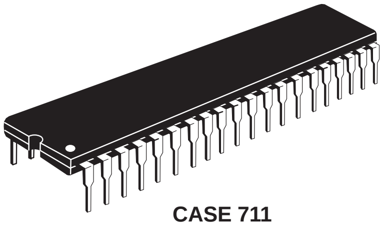
CASE 648
N, P, PC SUFFIX



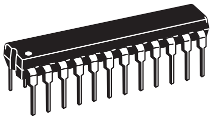
CASE 707
A SUFFIX



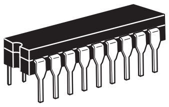
CASE 709
P SUFFIX



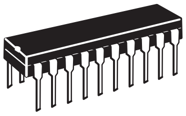
CASE 711
P SUFFIX



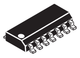
CASE 724
P SUFFIX



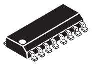
CASE 726



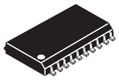
CASE 738
P SUFFIX



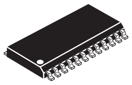
CASE 751A
D SUFFIX



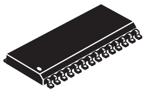
CASE 751B
D SUFFIX



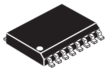
CASE 751D
DW SUFFIX



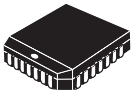
CASE 751E
DW SUFFIX



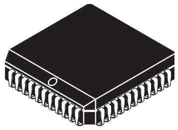
CASE 751F
DW SUFFIX



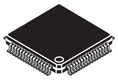
CASE 751G
DW SUFFIX



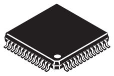
CASE 776
FN SUFFIX



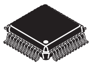
CASE 777
FN SUFFIX



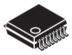
CASE 840F
FTA SUFFIX



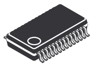
CASE 848D
FB SUFFIX



CASE 932
FTA SUFFIX



CASE 940B
SD SUFFIX



CASE 940J
VF SUFFIX

Device Listing

Interface Circuits

NOTE: * Not recommended for new designs.

MOTOROLA

AM26LS30

Dual Differential (EIA-422-A)/ Quad Single-Ended (EIA-423-A) Line Drivers

The AM26LS30 is a low power Schottky set of line drivers which can be configured as two differential drivers which comply with EIA–422–A standards, or as four single–ended drivers which comply with EIA–423–A standards. A mode select pin and appropriate choice of power supplies determine the mode. Each driver can source and sink currents in excess of 50 mA.

In the differential mode (EIA–422–A), the drivers can be used up to 10 Mbaud. A disable pin for each driver permits setting the outputs into a high impedance mode within a ±10 V common mode range.

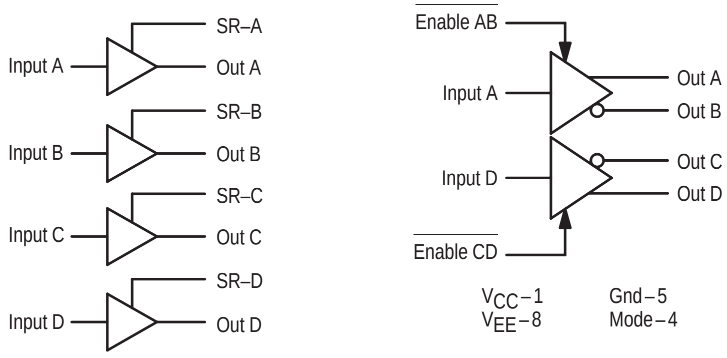
In the single–ended mode (EIA–423–A), each driver has a slew rate control pin which permits setting the slew rate of the output signal so as to comply with EIA–423–A and FCC requirements and to reduce crosstalk. When operated from symmetrical supplies (±5.0 V), the outputs exhibit zero imbalance.

The AM26LS30 is available in a 16–pin plastic DIP and surface mount package. Operating temperature range is –40° to +85°C.

- Operates as Two Differential EIA–422–A Drivers, or Four Single–Ended EIA–423–A Drivers
- High Impedance Outputs in Differential Mode
- Short Circuit Current Limit In Both Source and Sink Modes
- ± 10 V Common Mode Range on High Impedance Outputs
- ± 15 V Range on Inputs
- Low Current PNP Inputs Compatible with TTL, CMOS, and MOS Outputs
- Individual Output Slew Rate Control in Single–Ended Mode
- Replacement for the AMD AM25LS30 and National Semiconductor DS3691

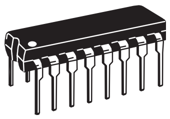
Representative Block Diagrams

Single–Ended Mode EIA–423–A **Differential Mode EIA–422–A**

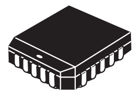


DUAL DIFFERENTIAL/ QUAD SINGLE–ENDED LINE DRIVERS

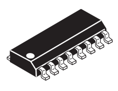
SEMICONDUCTOR TECHNICAL DATA



PC SUFFIX
PLASTIC PACKAGE
CASE 648

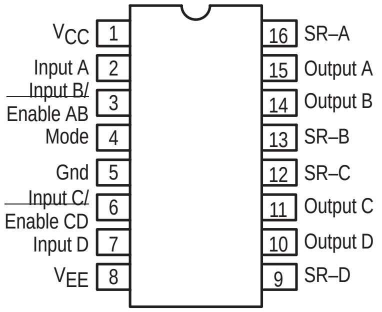


FN SUFFIX
PLASTIC PACKAGE
CASE 775

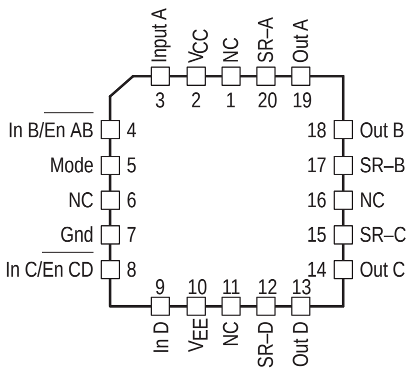


D SUFFIX
PLASTIC PACKAGE
CASE 751B
(SO–16)

PIN CONNECTIONS



(Top View)



ORDERING INFORMATION

Device	Operating Temperature Range	Package
AM26LS30PC	T_A = – 40° to +85°C	Plastic DIP
MC26LS30D		SO–16
AM26LS30FN		PLCC–20

MAXIMUM OPERATING CONDITIONS (Pin numbers refer to DIP and SO–16 packages only.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC} V_{EE}	–0.5, +7.0 –7.0, +0.5	Vdc
Input Voltage (All Inputs)	V_{in}	–0.5, +20	Vdc
Applied Output Voltage when in High Impedance Mode (V_{CC} = 5.0 V, Pin 4 = Logic 0, Pins 3, 6 = Logic 1)	V_{za}	±15	Vdc
Output Voltage with V_{CC}, V_{EE} = 0 V	V_{zb}	±15	
Output Current	I_O	Self limiting	–
Junction Temperature	T_J	–65, +150	°C

Devices should not be operated at these limits. The “Recommended Operating Conditions” table provides conditions for actual device operation.

RECOMMENDED OPERATING CONDITIONS

Rating	Symbol	Min	Typ	Max	Unit
Power Supply Voltage (Differential Mode)	V_{CC} V_{EE}	+4.75 –0.5	5.0 0	+5.25 +0.3	Vdc
Power Supply Voltage (Single–Ended Mode)	V_{CC} V_{EE}	+4.75 –5.25	+5.0 –5.0	+5.25 –4.75	
Input Voltage (All Inputs)	V_{in}	0	–	+15	Vdc
Applied Output Voltage (when in High Impedance Mode)	V_{za}	–10	–	+10	
Applied Output Voltage, V_{CC} = 0	V_{zb}	–10	–	+10	
Output Current	I_O	–65	–	+65	mA
Operating Ambient Temperature (See text)	T_A	–40	–	+85	°C

All limits are not necessarily functional concurrently.

ELECTRICAL CHARACTERISTICS (EIA–422–A differential mode, Pin 4 $\leqslant$ 0.8 V, –40°C $< T_A <$ 85°C, 4.75 V $\leqslant V_{CC} \leqslant$ 5.25 V, V_{EE} = Gnd, unless otherwise noted. Pin numbers refer to DIP and SO–16 packages only.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (see Figure 1)					
Differential, $R_L = \infty$, V_{CC} = 5.25 V	$\lvert V_{OD1}\rvert$	–	4.2	6.0	Vdc
Differential, R_L = 100 Ω, V_{CC} = 4.75 V	$\lvert V_{OD2}\rvert$	2.0	2.6	–	Vdc
Change in Differential Voltage, R_L = 100 Ω (Note 4)	$\lvert \Delta V_{OD2}\rvert$	–	10	400	mVdc
Offset Voltage, R_L = 100 Ω	V_{OS}	–	2.5	3.0	Vdc
Change in Offset Voltage*, R_L = 100 Ω	$\lvert \Delta V_{OS}\rvert$	–	10	400	mVdc
Output Current (each output)					
Power Off Leakage, V_{CC} = 0, –10 V $\leqslant V_O \leqslant$ +10 V	I_{OLK}	–100	0	+100	µA
High Impedance Mode, V_{CC} = 5.25 V, –10 V $\leqslant V_O \leqslant$ +10 V	I_{OZ}	–100	0	+100	
Short Circuit Current (Note 2)					
High Output Shorted to Pin 5 (T_A = 25°C)	I_{SC-}	–150	–95	–60	mA
High Output Shorted to Pin 5 (–40°C $< T_A <$ +85°C)	I_{SC-}	–150	–	–50	
Low Output Shorted to +6.0 V (T_A = 25°C)	I_{SC+}	60	75	150	
Low Output Shorted to +6.0 V (–40°C $< T_A <$ +85°C)	I_{SC+}	50	–	150	
Inputs					
Low Level Voltage	V_{IL}	–	–	0.8	Vdc
High Level Voltage	V_{IH}	2.0	–	–	Vdc
Current @ V_{in} = 2.4 V	I_{IH}	–	0	40	µA
Current @ V_{in} = 15 V	I_{IHH}	–	0	100	
Current @ V_{in} = 0.4 V	I_{IL}	–200	–8.0	–	
Current, 0 $\leqslant V_{in} \leqslant$ 15 V, V_{CC} = 0	I_{IX}	–	0	–	
Clamp Voltage (I_{in} = –12 mA)	V_{IK}	–1.5	–	–	Vdc
Power Supply Current (V_{CC} = +5.25 V, Outputs Open) (0 $\leqslant$ Enable $\leqslant V_{CC}$)	I_{CC}	–	16	30	mA

NOTES:
1. All voltages measured with respect to Pin 5.
2. Only one output shorted at a time, for not more than 1 second.
3. Typical values established at +25°C, V_{CC} = +5.0 V, V_{EE} = –5.0 V.
4. V_{in} switched from 0.8 to 2.0 V.
5. Imbalance is the difference between $\lvert V_{O2}\rvert$ with $V_{in} <$ 0.8 V and $\lvert V_{O2}\rvert$ with $V_{in} >$ 2.0 V.

TIMING CHARACTERISTICS (EIA–422–A differential mode, Pin 4 $\leqslant$ 0.8 V, T_A = 25°C, V_{CC} = 5.0 V, V_{EE} = Gnd, (Notes 1 and 3) unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Differential Output Rise Time (Figure 3)	t_r	–	70	200	ns
Differential Output Fall Time (Figure 3)	t_f	–	70	200	ns
Propagation Delay Time – Input to Differential Output					ns
Input Low to High (Figure 3)	t_{PDH}	–	90	200	
Input High to Low (Figure 3)	t_{PDL}	–	90	200	
Skew Timing (Figure 3)					ns
$\lvert t_{PDH} \text{ to } t_{PDL} \rvert$ for Each Driver	t_{SK1}	–	9.0	–	
Max to Min t_{PDH} Within a Package	t_{SK2}	–	2.0	–	
Max to Min t_{PDL} Within a Package	t_{SK3}	–	2.0	–	
Enable Timing (Figure 4)					ns
Enable to Active High Differential Output	t_{PZH}	–	150	300	
Enable to Active Low Differential Output	t_{PZL}	–	190	350	
Enable to 3–State Output From Active High	t_{PHZ}	–	80	350	
Enable to 3–State Output From Active Low	t_{PLZ}	–	110	300	

ELECTRICAL CHARACTERISTICS (EIA–423–A single–ended mode, Pin 4 $\geqslant$ 2.0 V, –40°C $<$ T_A $<$ 85°C, 4.75 V $\leqslant$ $\lvert V_{CC} \rvert$, $\lvert V_{EE} \rvert$ $\leqslant$ 5.25 V, (Notes 1 and 3) unless otherwise noted).

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (V_{CC} = $\lvert V_{EE} \rvert$ = 4.75 V)					Vdc
Single–Ended Voltage, $R_L = \infty$ (Figure 2)	$\lvert V_{O1} \rvert$	4.0	4.2	6.0	
Single–Ended Voltage, R_L = 450 Ω, (Figure 2)	$\lvert V_{O2} \rvert$	3.6	3.95	6.0	
Voltage Imbalance (Note 5), R_L = 450 Ω	$\lvert \Delta V_{O2} \rvert$	–	0.05	0.4	
Slew Control Current (Pins 16, 13, 12, 9)	I_{SLEW}	–	±120	–	µA
Output Current (Each Output)					
Power Off Leakage, V_{CC} = V_{EE} = 0, –6.0 V $\leqslant$ V_O $\leqslant$ +6.0 V	I_{OLK}	–100	0	+100	µA
Short Circuit Current (Output Short to Ground, Note 2)					
V_{in} $\leqslant$ 0.8 V (T_A = 25°C)	I_{SC+}	60	80	150	mA
V_{in} $\leqslant$ 0.8 V (–40°C $<$ T_A $<$ +85°C)	I_{SC+}	50	–	150	
V_{in} $\geqslant$ 2.0 V (T_A = 25°C)	I_{SC-}	–150	–95	–60	
V_{in} $\geqslant$ 2.0 V (–40°C $<$ T_A $<$ +85°C)	I_{SC-}	–150	–	–50	
Inputs					
Low Level Voltage	V_{IL}	–	–	0.8	Vdc
High Level Voltage	V_{IH}	2.0	–	–	Vdc
Current @ V_{in} = 2.4 V	I_{IH}	–	0	40	µA
Current @ V_{in} = 15 V	I_{IHH}	–	0	100	
Current @ V_{in} = 0.4 V	I_{IL}	–200	–8.0	–	
Current, 0 $\leqslant$ V_{in} $\leqslant$ 15 V, V_{CC} = 0	I_{IX}	–	0	–	
Clamp Voltage (I_{in} = –12 mA)	V_{IK}	–1.5	–	–	Vdc
Power Supply Current (Outputs Open)	I_{CC}	–	17	30	mA
V_{CC} = +5.25 V, V_{EE} = –5.25 V, V_{in} = 0.4 V	I_{EE}	–22	–8.0	–	

TIMING CHARACTERISTICS (EIA–423–A single–ended mode, Pin 4 $\geqslant$ 2.0 V, T_A = 25°C, V_{CC} = 5.0 V, V_{EE} = –5.0 V, (Notes 1 and 3) unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Timing (Figure 5)					
Output Rise Time, C_C = 0	t_r	–	65	300	ns
Output Fall Time, C_C = 0	t_f	–	65	300	
Output Rise Time, C_C = 50 pF	t_r	–	3.0	–	µs
Output Fall Time, C_C = 50 pF	t_f	–	3.0	–	
Rise Time Coefficient (Figure 16)	C_{rt}	–	0.06	–	µs/pF
Propagation Delay Time, Input to Single Ended Output (Figure 5)					ns
Input Low to High, C_C = 0	t_{PDH}	–	100	300	
Input High to Low, C_C = 0	t_{PDL}	–	100	300	
Skew Timing, C_C = 0 (Figure 5)					ns
$\lvert t_{PDH} \text{ to } t_{PDL} \rvert$ for Each Driver	t_{SK4}	–	15	–	
Max to Min t_{PDH} Within a Package	t_{SK5}	–	2.0	–	
Max to Min t_{PDL} Within a Package	t_{SK6}	–	5.0	–	

Table 1

Operation	V_{CC}	V_{EE}	Inputs					Outputs			
			Mode	A	B	C	D	A	B	C	D
Differential (EIA–422–A)	+5.0	Gnd	0	0	0	0	0	0	1	1	0
			0	1	0	0	1	1	0	0	1
			0	X	1	0	1	Z	Z	0	1
			0	1	0	0	0	1	0	1	0
			0	0	0	0	1	0	1	0	1
			0	1	0	1	X	1	0	Z	Z
Single–Ended (EIA–423–A)	+5.0	–5.0	1	0	0	0	0	0	0	0	0
			1	1	0	0	0	1	0	0	0
			1	0	1	0	0	0	1	0	0
			1	0	0	1	0	0	0	1	0
			1	0	0	0	1	0	0	0	1
X	0	X	X	X	X	X	X	Z	Z	Z	Z

X = Don’t Care
Z = High Impedance (Off)

Figure 1. Differential Output Test

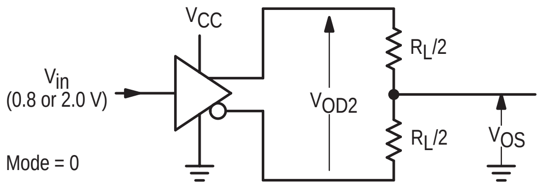


Figure 2. Single–Ended Output Test

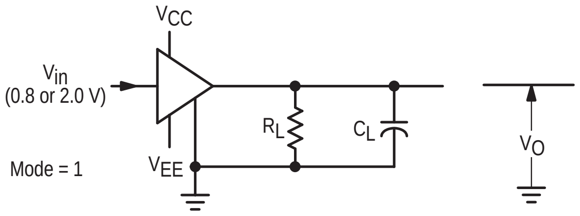
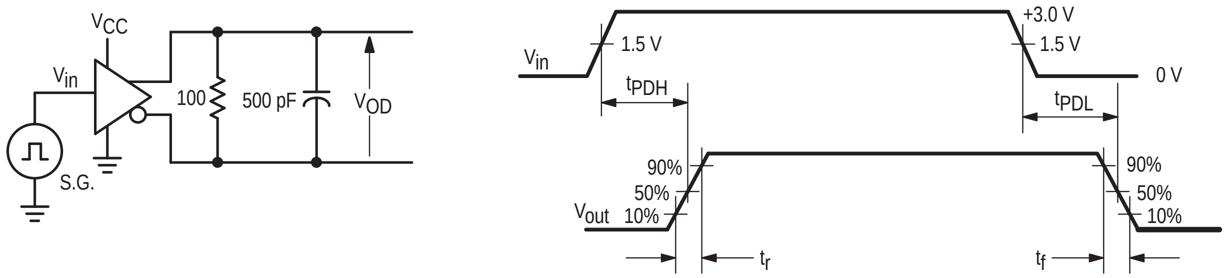
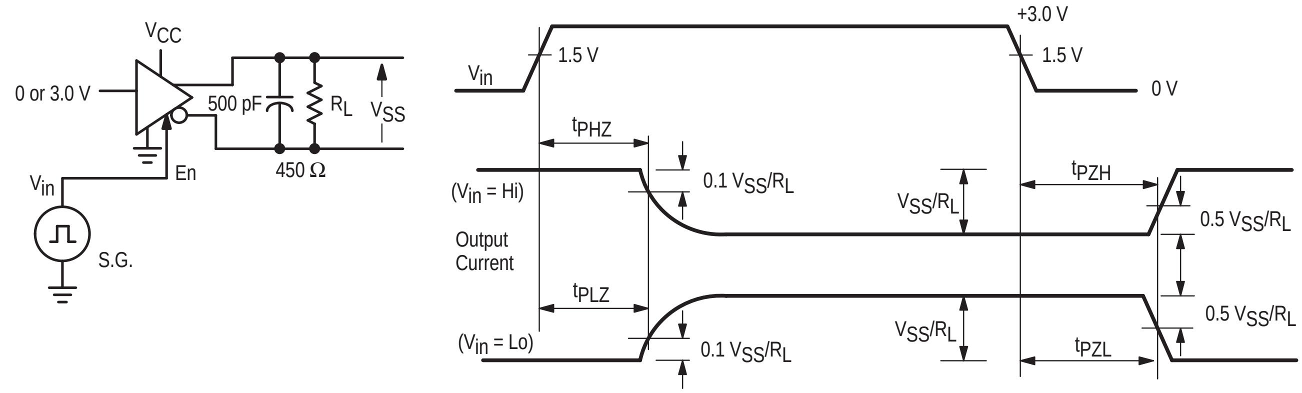


Figure 3. Differential Mode Rise/Fall Time and Data Propagation Delay



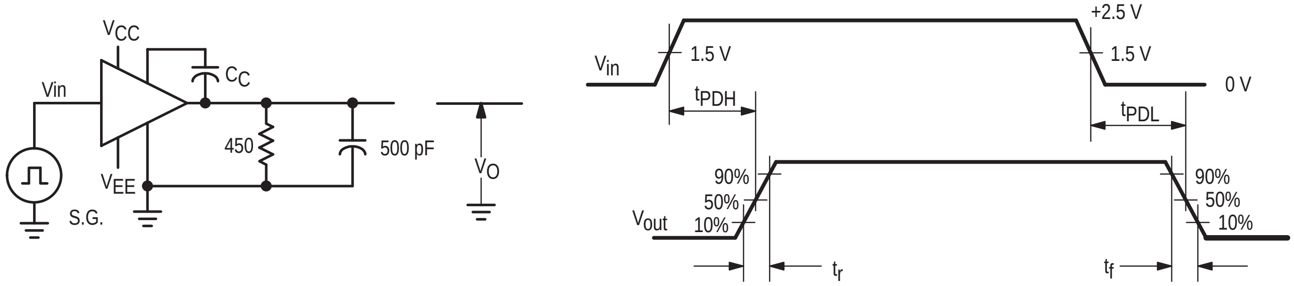
NOTES: 1. S.G. set to: $f \leqslant 1.0$ MHz; duty cycle = 50%; t_r, t_f, $\leqslant 10$ ns.
2. $t_{SK1} = |t_{PDH} – t_{PDL}|$ for each driver.
3. t_{SK2} computed by subtracting the shortest t_{PDH} from the longest t_{PDH} of the 2 drivers within a package.
4. t_{SK3} computed by subtracting the shortest t_{PDL} from the longest t_{PDL} of the 2 drivers within a package.

Figure 4. Differential Mode Enable Timing



NOTES: 1. S.G. set to: f ≤ 1.0 MHz; duty cycle = 50%; t_r, t_f, ≤ 10 ns.
2. Above tests conducted by monitoring output current levels.

Figure 5. Single–Ended Mode Rise/Fall Time and Data Propagation Delay



NOTES: 1. S.G. set to: f ≤ 100 kHz; duty cycle = 50%; t_r, t_f, ≤ 10 ns.
2. $t_{SK4} = |t_{PDH} – t_{PDL}|$ for each driver.
3. t_{SK5} computed by subtracting the shortest t_{PDH} from the longest t_{PDH} of the 4 drivers within a package.
4. t_{SK6} computed by subtracting the shortest t_{PDL} from the longest t_{PDL} of the 4 drivers within a package.

Figure 6. Differential Output Voltage versus Load Current

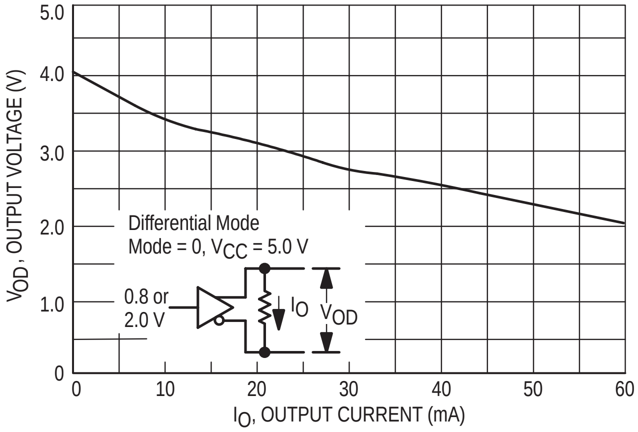


Figure 7. Internal Bias Current versus Load Current

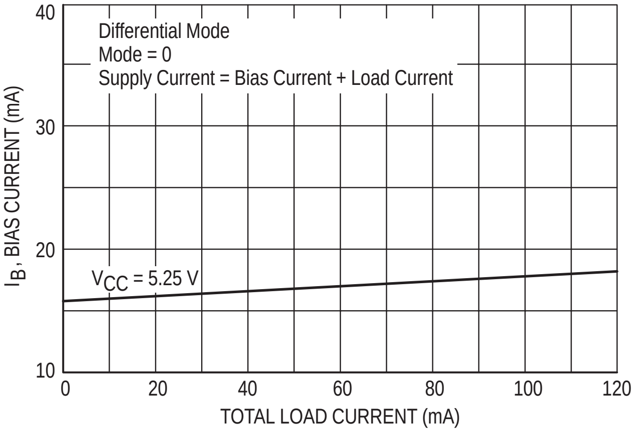


Figure 8. Short Circuit Current versus Output Voltage

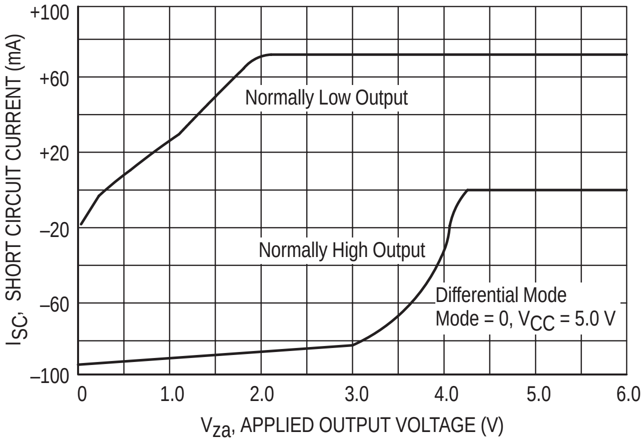


Figure 9. Input Current versus Input Voltage
(Pin numbers refer to DIP and SO–16 packages only.)

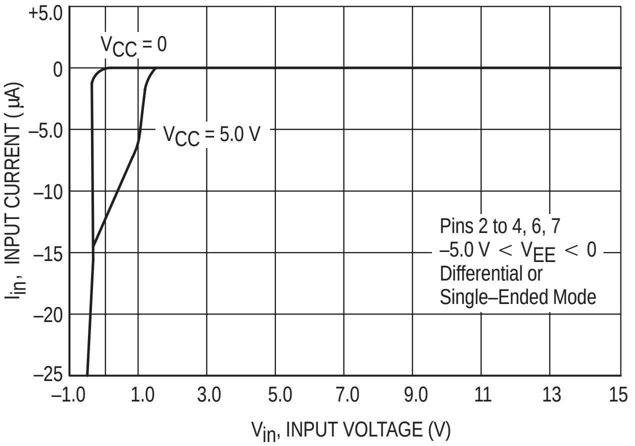


Figure 10. Output Voltage versus Output Source Current

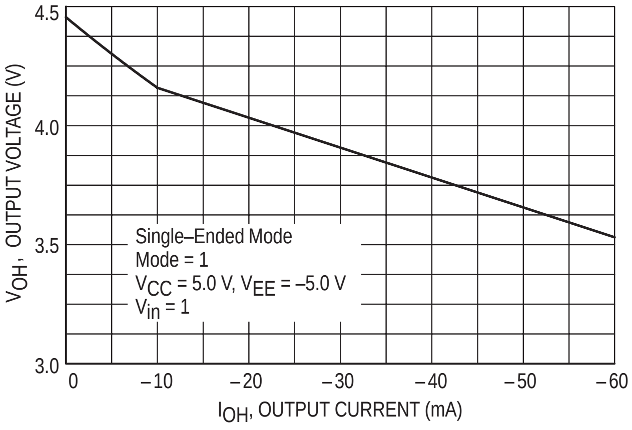


Figure 11. Output Voltage versus Output Sink Current

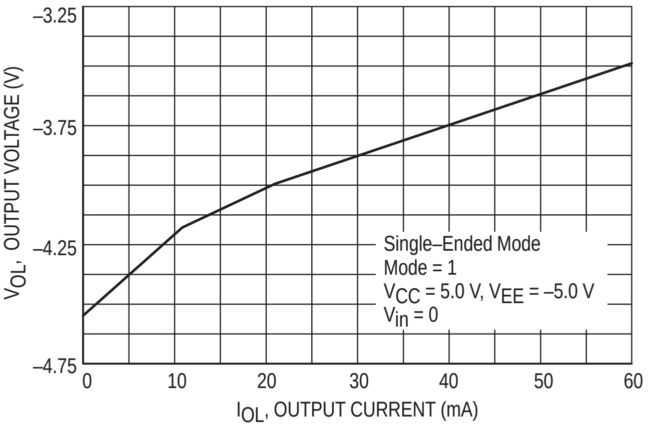


Figure 12. Internal Positive Bias Current versus Load Current

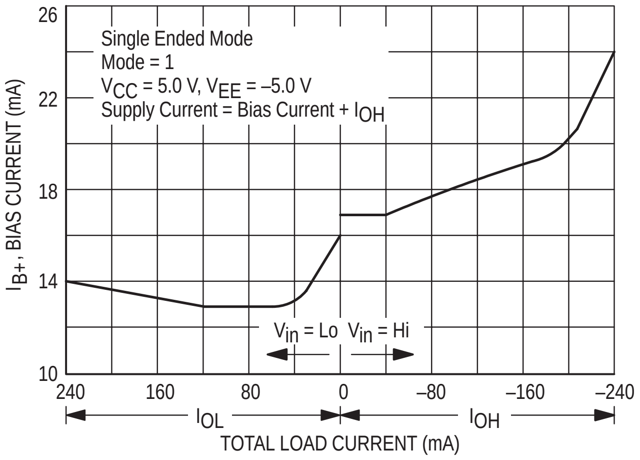


Figure 13. Internal Negative Bias Current versus Load Current

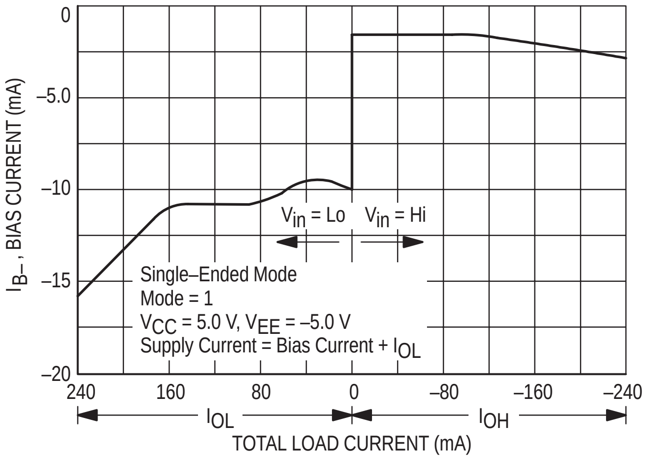


Figure 14. Short Circuit Current versus Output Voltage

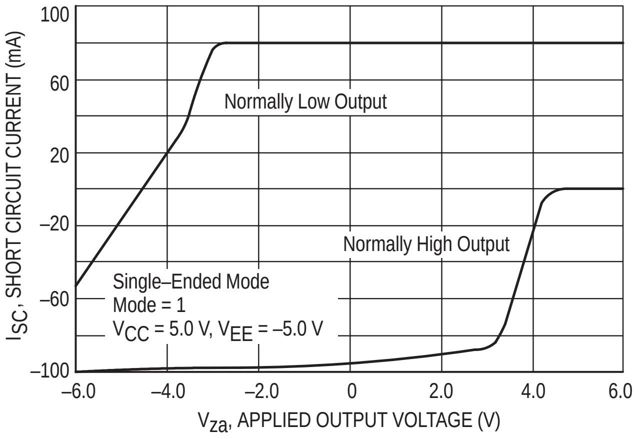


Figure 15. Short Circuit Current versus Temperature

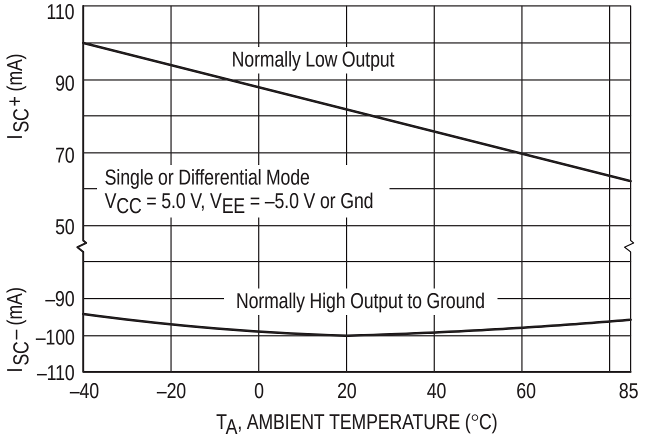
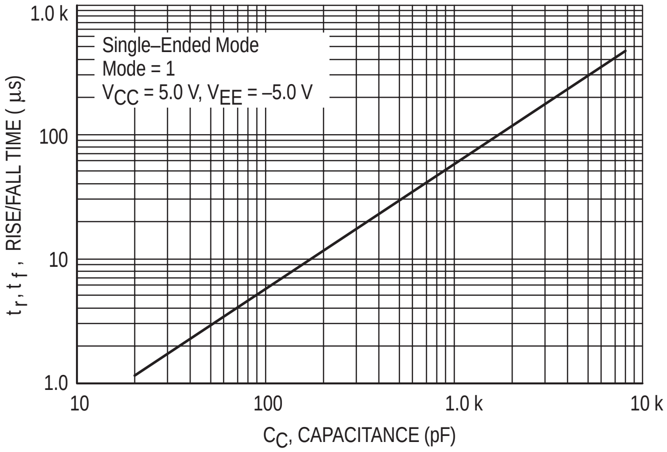


Figure 16. Rise/Fall Time versus Capacitance



APPLICATIONS INFORMATION

(Pin numbers refer to DIP and SO–16 packages only.)

Description

The AM26LS30 is a dual function line driver – it can be configured as two differential output drivers which comply with EIA–422–A Standard, or as four single–ended drivers which comply with EIA–423–A Standard. The mode of operation is selected with the Mode pin (Pin 4) and appropriate power supplies (see Table 1). Each of the four outputs is capable of sourcing and sinking 60 to 70 mA while providing sufficient voltage to ensure proper data transmission.

As differential drivers, data rates to 10 Mbaud can be transmitted over a twisted pair for a distance determined by the cable characteristics. EIA–422–A Standard provides guidelines for cable length versus data rate. The advantage of a differential (balanced) system over a single–ended system is greater noise immunity, common mode rejection, and higher data rates.

Where extraneous noise sources are not a problem, the AM26LS30 may be configured as four single–ended drivers transmitting data rates to 100 Kbaud. Crosstalk among wires within a cable is controlled by the use of the slew rate control pins on the AM26LS30.

Mode Selection

(Differential Mode)

In this mode (Pins 4 and 8 at ground), only a +5.0 V supply ±5% is required at V_{CC}. Pins 2 and 7 are the driver inputs, while Pins 10, 11, 14 and 15 are the outputs (see Block Diagram on page 1). The two outputs of a driver are always complementary and the differential voltage available at each pair of outputs is shown in Figure 6 for V_{CC} = 5.0 V. The differential output voltage will vary directly with V_{CC}. A “high” output can only source current, while a “low” output can only sink current (except for short circuit current – see Figure 8).

The two outputs will be in a high impedance mode when the respective Enable input (Pin 3 or 6) is high, or if $V_{CC} \leqslant$ 1.1 V. Output leakage current over a common mode range of ± 10 V is typically less than 1.0 µA.

The outputs have short circuit current limiting, typically, less than 100 mA over a voltage range of 0 to +6.0 V (see Figure 8). Short circuits should not be allowed to last indefinitely as the IC may be damaged.

Pins 9, 12, 13 and 16 are not normally used when in this mode, and should be left open.

(Single–Ended Mode)

In this mode (Pin 4 ≥ 2.0 V) V_{CC} requires +5.0 V, and V_{EE} requires –5.0 V, both ±5.0%. Pins 2, 3, 6, and 7 are inputs for the four drivers, and Pins 15, 14, 11, and 10 (respectively) are the outputs. The four drivers are independent of each other, and each output will be at a positive or a negative voltage depending on its input state, the load current, and the supply voltage. Figures 10 & 11 indicate the high and low output voltages for V_{CC} = 5.0 V, and V_{EE} = –5.0 V. The graph of Figure 10 will vary directly with V_{CC}, and the graph of Figure 11 will vary directly with V_{EE}. A “high” output can only source current, while a “low” output can only sink current (except short circuit current – see Figure 14).

The outputs will be in a high impedance mode only if $V_{CC} \leqslant$ 1.1 V. Changing V_{EE} to 0 V does not set the outputs to a high impedance mode. Leakage current over a common mode range of ±10 V is typically less than 1.0 µA.

The outputs have short circuit current limiting, typically less than 100 mA over a voltage range of ±6.0 V (see Figure 14). Short circuits should not be allowed to last indefinitely as the IC may be damaged.

Capacitors connected between Pins 9, 12, 13, and 16 and their respective outputs will provide slew rate limiting of the output transition. Figure 16 indicates the required capacitor value to obtain a desired rise or fall time (measured between the 10% and 90% points). The positive and negative transition times will be within ≈ ±5% of each other. Each output may be set to a different slew rate if desired.

Inputs

The five inputs determine the state of the outputs in accordance with Table 1. All inputs (regardless of the operating mode) have a nominal threshold of +1.3 V, and their voltage must be kept within a range of 0 V to +15 V for proper operation. If an input is taken more than 0.3 V below ground, excessive currents will flow, and the proper operation of the drivers will be affected. An open pin is equivalent to a logic high, but good design practices dictate that inputs should never be left open. Unused inputs should be connected to ground. The characteristics of the inputs are shown in Figure 9.

Power Supplies

V_{CC} requires +5.0 V, ±5%, regardless of the mode of operation. The supply current is determined by the IC’s internal bias requirements and the total load current. The internally required current is a function of the load current and is shown in Figure 7 for the differential mode.

In the single–ended mode, V_{EE} must be –5.0 V, ±5% in order to comply with EIA–423–A standards. Figures 12 and 13 indicate the internally required bias currents as a function of total load current (the sum of the four output loads). The discontinuity at 0 load current exists due to a change in bias current when the inputs are switched. The supply currents vary ≈ ± 2.0 mA as V_{CC} and V_{EE} are varied from $|4.75\ V|$ to $|5.25\ V|$.

Sequencing of the supplies during power–up/power–down is not required.

Bypass capacitors (0.1 µF minimum on each supply pin) are recommended to ensure proper operation. Capacitors reduce noise induced onto the supply lines by the switching action of the drivers, particularly where long P.C. board tracks are involved. Additionally, the capacitors help absorb transients induced onto the drivers’ outputs from the external cable (from ESD, motor noise, nearby computers, etc.).

Operating Temperature Range

The maximum ambient operating temperature, listed as +85°C, is actually a function of the system use (i.e., specifically how many drivers within a package are used) and at what current levels they are operating. The maximum power which may be dissipated within the package is determined by:

$$P_{Dmax} = \frac{T_{Jmax} - T_A}{R_{\theta JA}}$$

where $R_{\theta JA}$ = package thermal resistance which is typically:
67°C/W for the DIP (PC) package,
120°C/W for the SOIC (D) package,
T_{Jmax} = max. allowable junction temperature (150°C)
T_A = ambient air temperature near the IC package.

1) Differential Mode Power Dissipation

For the differential mode, the power dissipated within the package is calculated from:

$P_D = [(V_{CC} - V_{OD}) \times I_O]$ (each driver) + $(V_{CC} \times I_B)$

where: V_{CC} = the supply voltage
V_{OD} = is taken from Figure 6 for the known value of I_O
I_B = the internal bias current (Figure 7)

As indicated in the equation, the first term (in brackets) must be calculated and summed for each of the two drivers, while the last term is common to the entire package. Note that the term $(V_{CC} - V_{OD})$ is constant for a given value of I_O and does not vary with V_{CC}. For an application involving the following conditions:

T_A = +85°C, I_O = –60 mA (each driver), V_{CC} = 5.25 V, the suitability of the package types is calculated as follows.

The power dissipated is:

P_D = [3.0 V × 60 mA × 2] + (5.25 V × 18 mA)
P_D = 454 mW

The junction temperature calculates to:

T_J = 85°C + (0.454 W × 67°C/W) = 115°C for the DIP package,
T_J = 85°C + (0.454 W × 120°C/W) = 139°C for the
T_J = SOIC package.

Since the maximum allowable junction temperature is not exceeded in any of the above cases, either package can be used in this application.

2) Single–Ended Mode Power Dissipation

For the single–ended mode, the power dissipated within the package is calculated from:

$$P_D = (I_{B+} \times V_{CC}) + (I_{B-} \times V_{EE}) + [(I_O \times (V_{CC} - V_{OH})]\text{(each driver)}$$

The above equation assumes I_O has the same magnitude for both output states, and makes use of the fact that the absolute value of the graphs of Figures 10 and 11 are nearly identical. I_B+ and I_B– are obtained from the right half of Figures 12 and 13, and $(V_{CC} - V_{OH})$ can be obtained from Figure 10. Note that the term $(V_{CC} - V_{OH})$ is constant for a given value of I_O and does not vary with V_{CC}. For an application involving the following conditions:

T_A = +85°C, I_O = –60 mA (each driver), V_{CC} = 5.25 V, V_{EE} = –5.25 V, the suitability of the package types is calculated as follows.

The power dissipated is:

P_D = (24 mA × 5.25 V) + (–3.0 mA × –5.25 V) + [60 mA × 1.45 V × 4.0]
P_D = 490 mW

The junction temperature calculates to:

T_J = 85°C + (0.490 W × 67°C/W) = 118°C for the DIP package,
T_J = 85°C + (0.490 W × 120°C/W) = 144°C for the SOIC package.

Since the maximum allowable junction temperature is not exceeded in any of the above cases, either package can be used in this application.

SYSTEM EXAMPLES

(Pin numbers refer to DIP and SO–16 packages only.)

Differential System

An example of a typical EIA–422–A system is shown in Figure 17. Although EIA–422–A does not specifically address multiple driver situations, the AM26LS30 can be used in this manner since the outputs can be put into a high impedance mode. It is, however, the system designer's responsibility to ensure the Enable pins are properly controlled so as to prevent two drivers on the same cable from being "on" at the same time.

The limit on the number of receivers and drivers which may be connected on one system is determined by the input current of each receiver, the maximum leakage current of each "off" driver, and the DC current through each terminating resistor. The sum of these currents must not exceed the capability of the "on" driver (≈60 mA). If the cable is of any significant length, with receivers at various points along its length, the common mode voltage may vary along its length, and this parameter must be considered when calculating the maximum driver current.

The cable requirements are defined not only by the AC characteristics and the data rate, but also by the DC resistance. The maximum resistance must be such that the minimum voltage across any receiver inputs is never less than 200 mV.

The ground terminals of each driver and receiver in Figure 17 must be connected together by a dedicated wire (or the shield) in the cable to provide a common reference. Chassis grounds or power line grounds should not be relied on for this common connection as they may generate significant common mode differences. Additionally, they usually do not provide a sufficiently low impedance at the frequencies of interest.

Single–Ended System

An example of a typical EIA–423–A system is shown in Figure 18. Multiple drivers on a single data line are not possible since the drivers cannot be put into a high impedance mode. Although each driver is shown connected to a single receiver, multiple receivers can be driven from a single driver as long as the total load current of the receivers and the terminating resistor does not exceed the capability of the driver (≈60 mA). If the cable is of any significant length, with receivers at various points along its length, the common mode voltage may vary along its length, and this parameter must be considered when calculating the maximum driver current.

The cable requirements are defined not only by the AC characteristics and the data rate, but also by the DC resistance. The maximum resistance must be such that the minimum voltage across any receiver inputs is never less than 200 mV.

The ground terminals of each driver and receiver in Figure 18 must be connected together by a dedicated wire (or the shield) in the cable so as to provide a common reference. Chassis grounds or power line grounds should not be relied on for this common connection as they may generate significant common mode differences. Additionally, they usually do not provide a sufficiently low impedance at the frequencies of interest.

Additional Modes of Operation

If compliance with EIA–422–A or EIA–423–A Standard is not required in a particular application, the AM26LS30 can be operated in two other modes.

1) The device may be operated in the differential mode (Pin 4 = 0) with V_{EE} connected to any voltage between ground and –5.25 V. Outputs in the low state will be referenced to V_{EE}, resulting in a differential output voltage greater than that shown in Figure 6. The Enable pins will operate the same as previously described.

2) The device may be operated in the single–ended mode (Pin 4 = 1) with V_{EE} connected to any voltage between ground and –5.25 V. Outputs in the high state will be at a voltage as shown in Figure 10, while outputs in a low state will be referenced to V_{EE}.

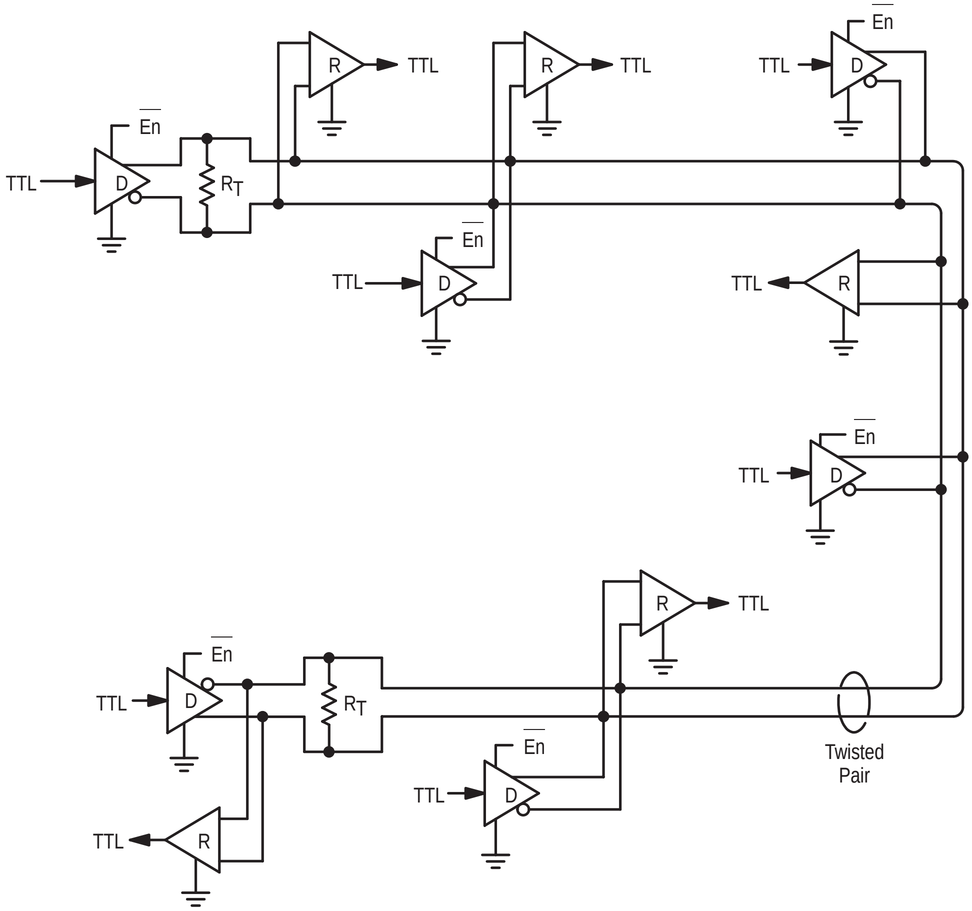
Termination Resistors

Transmission line theory states that, in order to preserve the shape and integrity of a waveform traveling along a cable, the cable must be terminated in an impedance equal to its characteristic impedance. In a system such as that depicted in Figure 17, in which data can travel in both directions, both physical ends of the cable must be terminated. Stubs leading to each receiver and driver should be as short as possible.

In a system such as that depicted in Figure 18, in which data normally travels in one direction only, a terminator is theoretically required only at the receiving end of the cable. However, if the cable is in a location where noise spikes of several volts can be induced onto it, then a terminator (preferably a series resistor) should be placed at the driver end to prevent damage to the driver.

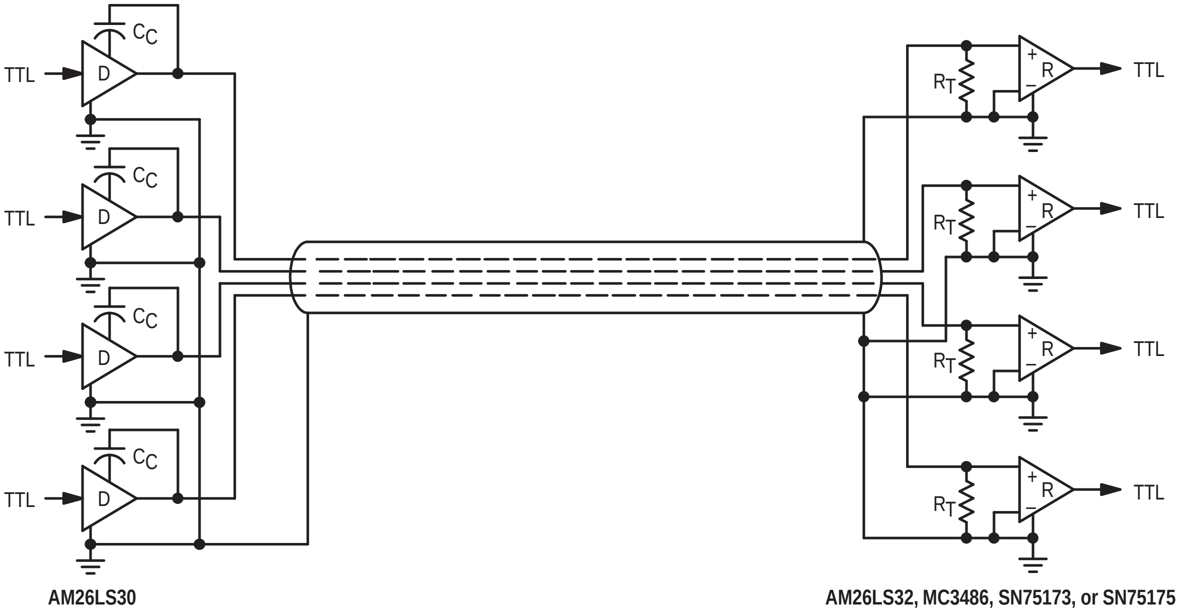
Leaving off the terminations will generally result in reflections which can have amplitudes of several volts above V_{CC} or several volts below ground or V_{EE}. These overshoots/undershoots can disrupt the driver and/or receiver, create false data, and in some cases, damage components on the bus.

Figure 17. EIA–422–A Example



NOTES: 1. Terminating resistors R_T should be located at the physical ends of the cable.
2. Stubs should be as short as possible.
3. Receivers = AM26LS32, MC3486, SN75173 or SN75175.
4. Circuit grounds must be connected together through a dedicated wire.

Figure 18. EIA–423–A Example



MOTOROLA

AM26LS31

Quad Line Driver with NAND Enabled Three-State Outputs

QUAD EIA–422 LINE DRIVER WITH THREE–STATE OUTPUTS

SEMICONDUCTOR TECHNICAL DATA

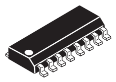
The Motorola AM26LS31 is a quad differential line driver intended for digital data transmission over balanced lines. It meets all the requirements of EIA–422 Standard and Federal Standard 1020.

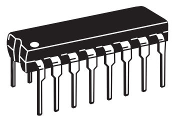
The AM26LS31 provides an enable/disable function common to all four drivers as opposed to the split enables on the MC3487 EIA–422 driver.

The high impedance output state is assured during power down.

- Full EIA–422 Standard Compliance
- Single +5.0 V Supply
- Meets Full $V_O = 6.0$ V, $V_{CC} = 0$ V, $I_O < 100\ \mu A$ Requirement
- Output Short Circuit Protection
- Complementary Outputs for Balanced Line Operation
- High Output Drive Capability
- Advanced LS Processing
- PNP Inputs for MOS Compatibility

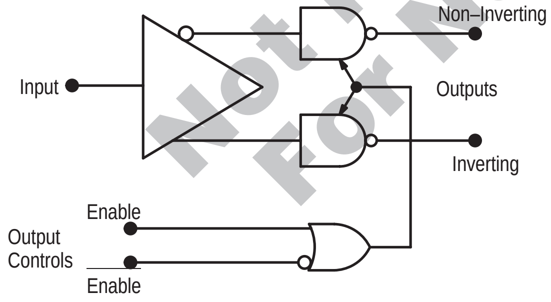
D SUFFIX
PLASTIC PACKAGE
CASE 751B
(SO–16)



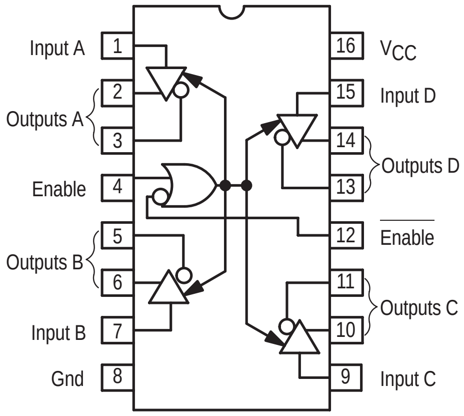


PC SUFFIX
PLASTIC PACKAGE
CASE 648

Representative Block Diagrams



PIN CONNECTIONS



TRUTH TABLE			
Input	**Control Inputs (E/$\overline{E}$)**	**Non–Inverting Output**	**Inverting Output**
H	H/L	H	L
L	H/L	L	H
X	L/H	Z	Z

L = Low Logic State
H = High Logic State
X = Irrelevant
Z = Third–State (High Impedance)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
AM26LS31PC	T_A = 0 to +70°C	Plastic DIP
MC26LS31D*		SO–16

* Note that the surface mount MC26LS31D device uses the same die as in the plastic DIP AM26LS31DC device, but with an MC prefix to prevent confusion with the package suffix.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	8.0	Vdc
Input Voltage	V_I	5.5	Vdc
Operating Ambient Temperature Range	T_A	0 to + 70	°C
Operating Junction Temperature Range	T_J	150	°C
Storage Temperature Range	T_{stg}	– 65 to + 150	°C

ELECTRICAL CHARACTERISTICS (Unless otherwise noted, specifications apply 4.75 V $\leqslant V_{CC} \leqslant$ 5.25 V and 0°C $\leqslant T_A \leqslant$ 70°C. Typical values measured at V_{CC} = 5.0 V, and T_A = 25°C.)

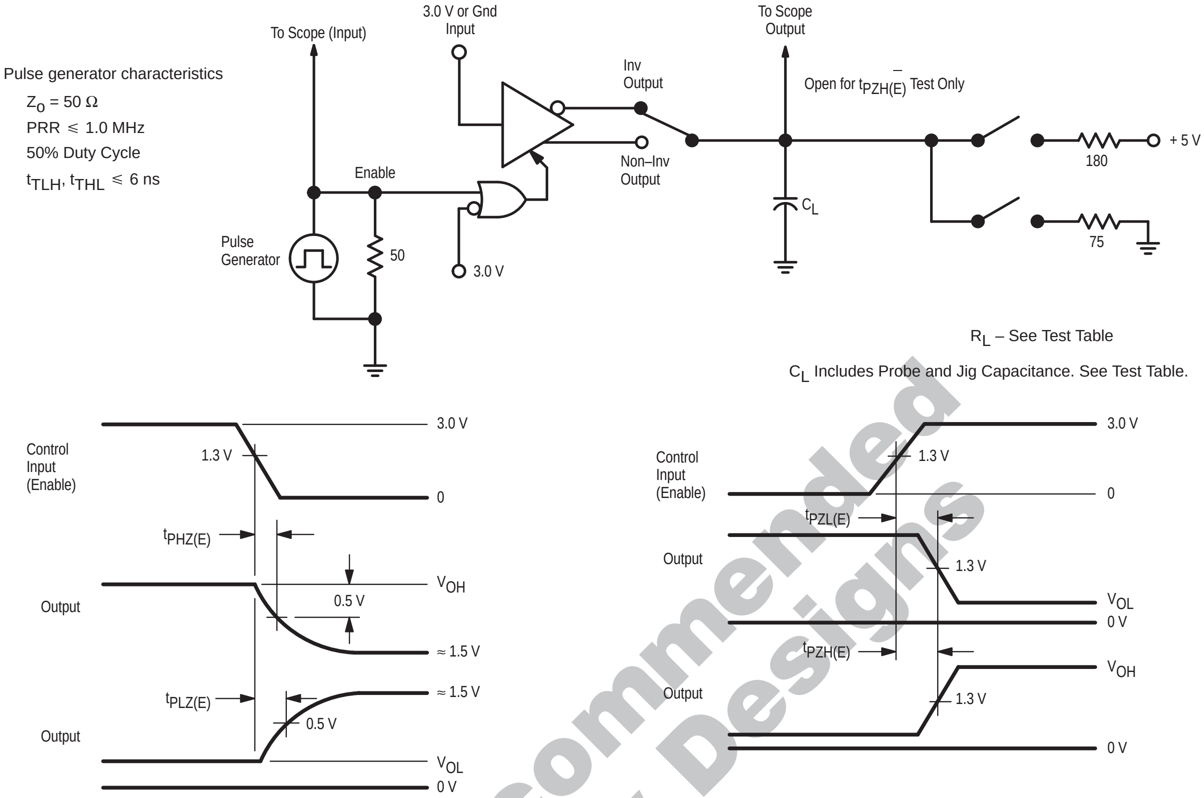
Characteristic	Symbol	Min	Typ	Max	Unit
Input Voltage – Low Logic State	V_{IL}	–	–	0.8	Vdc
Input Voltage – High Logic State	V_{IH}	2.0	–	–	Vdc
Input Current – Low Logic State (V_{IL} = 0.4 V)	I_{IL}	–	–	– 360	µA
Input Current – High Logic State (V_{IH} = 2.7 V) (V_{IH} = 7.0 V)	I_{IH}	 – –	 – –	 + 20 + 100	µA
Input Clamp Voltage (I_{IK} = – 18 mA)	V_{IK}	–	–	– 1.5	V
Output Voltage – Low Logic State (I_{OL} = 20 mA)	V_{OL}	–	–	0.5	V
Output Voltage – High Logic State (I_{OH} = –20 mA)	V_{OH}	2.5	–	–	V
Output Short Circuit Current (V_{IH} = 2.0 V) Note 1	I_{OS}	– 30	–	– 150	mA
Output Leakage Current – Hi–Z State (V_{OL} = 0.5 V, $V_{IL(E)}$ = 0.8 V, $V_{IH(\overline{E})}$ = 2.0 V) (V_{OH} = 2.5 V, $V_{IL(E)}$ = 0.8 V, $V_{IH(E)}$ = 2.0 V)	$I_{O(Z)}$	 – –	 – –	 – 20 + 20	µA
Output Leakage Current – Power OFF (V_{OH} = 6.0 V, V_{CC} = 0 V) (V_{OL} = – 0.25 V, V_{CC} = 0 V)	$I_{O(off)}$	 – –	 – –	 + 100 – 100	µA
Output Offset Voltage Difference, Note 2	$V_{OS} - \overline{V_{OS}}$	–	–	± 0.4	V
Output Differential Voltage, Note 2	V_{OD}	2.0	–	–	V
Output Differential Voltage Difference, Note 2	$\lvert\Delta V_{OD}\rvert$	–	–	± 0.4	V
Power Supply Current (Output Disabled) Note 3	I_{CCX}	–	60	80	mA

NOTES: 1. Only one output may be shorted at a time.
2. See EIA Specification EIA–422 for exact test conditions.
3. Circuit in three–state condition.

SWITCHING CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Propagation Delay Times High to Low Output Low to High Output	 t_{PHL} t_{PLH}	 – –	 – –	 20 20	ns
Output Skew		–	–	6.0	ns
Propagation Delay – Control to Output (C_L = 10 pF, R_L = 75 Ω to Gnd) (C_L = 10 pF, R_L = 180 Ω to V_{CC}) (C_L = 30 pF, R_L = 75 Ω to Gnd) (C_L = 30 pF, R_L = 180 Ω to V_{CC})	 $t_{PHZ(E)}$ $t_{PLZ(E)}$ $t_{PZH(E)}$ $t_{PZL(E)}$	 – – – –	 – – – –	 30 35 40 45	ns

Figure 1. Three–State Enable Test Circuit and Waveforms

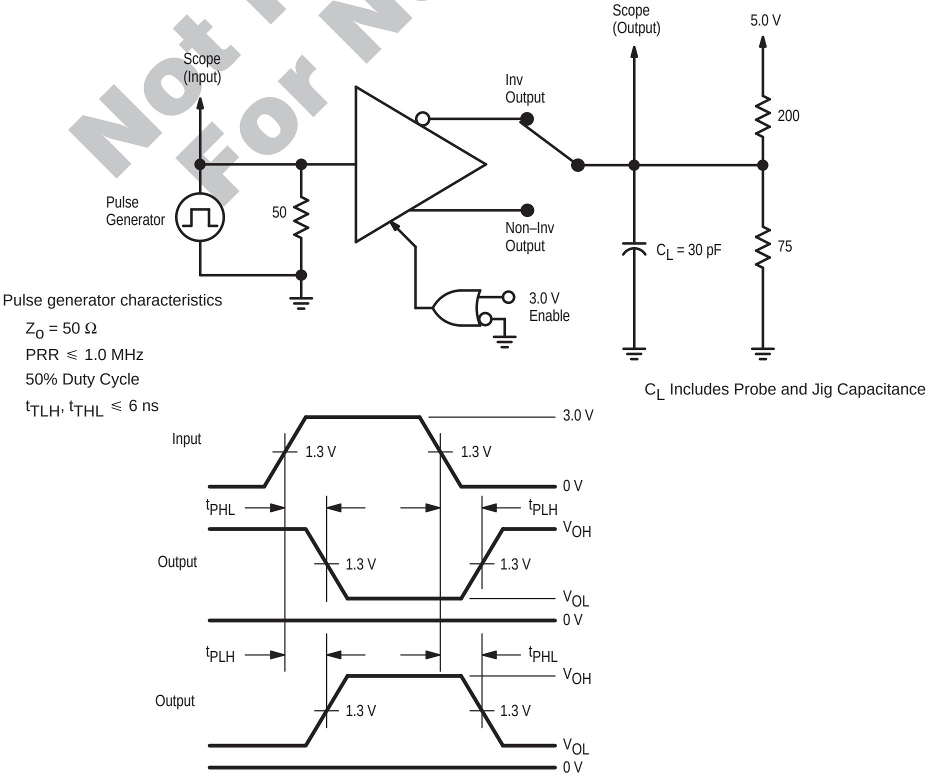


Pulse generator characteristics
$Z_o = 50\ \Omega$
PRR ≤ 1.0 MHz
50% Duty Cycle
t_{TLH}, t_{THL} ≤ 6 ns

R_L – See Test Table

C_L Includes Probe and Jig Capacitance. See Test Table.

Figure 2. Propagation Delay Times Input to Output Waveforms and Test Circuit



Pulse generator characteristics
$Z_o = 50\ \Omega$
PRR ≤ 1.0 MHz
50% Duty Cycle
t_{TLH}, t_{THL} ≤ 6 ns

C_L Includes Probe and Jig Capacitance

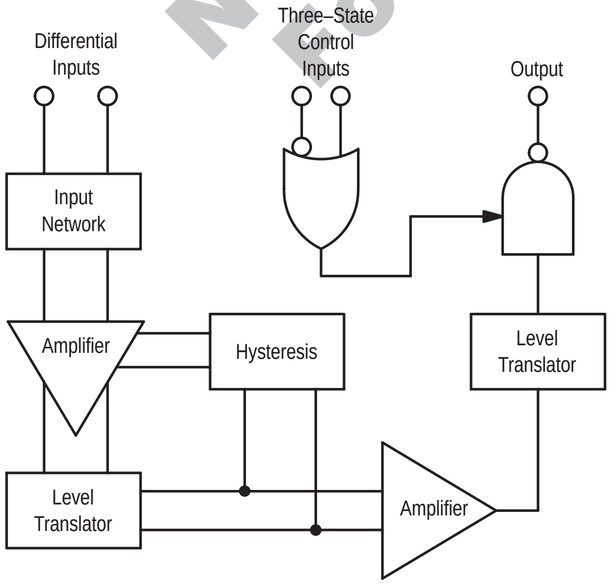
MOTOROLA

QUAD EIA-422/423 Line Receiver with Three-State Outputs

Motorola's Quad EIA–422/3 Receiver features four independent receiver chains which comply with EIA Standards for the Electrical Characteristics of Balanced/Unbalanced Voltage Digital Interface Circuits. Receiver outputs are 74LS compatible, three–state structures which are forced to a high impedance state when Pin 4 is a Logic "0" and Pin 12 is a Logic "1." A PNP device buffers each output control pin to assure minimum loading for either Logic "1" or Logic "0" inputs. In addition, each receiver chain has internal hysteresis circuitry to improve noise margin and discourage output instability for slowly changing input waveforms. A summary of AM26LS32 features include:

- Four Independent Receiver Chains
- Three–State Outputs
- High Impedance Output Control Inputs (PIA Compatible)
- Internal Hysteresis – 30 mV (Typical) @ Zero Volts Common Mode
- Fast Propagation Times – 25 ns (Typical)
- TTL Compatible
- Single 5.0 V Supply Voltage
- Fail–Safe Input–Output Relationship. Output Always High When Inputs Are Open, Terminated or Shorted
- 6.0 k Minimum Input Impedance

Representative Block Diagram



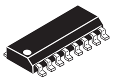
* Note that the surface mount MC26LS32D device uses the same die as in the plastic DIP AM26LS32DC device, but with an MC prefix to prevent confusion with the package suffix.

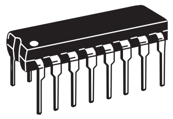
AM26LS32

QUAD EIA–422/3 LINE RECEIVER WITH THREE–STATE OUTPUTS

SEMICONDUCTOR TECHNICAL DATA

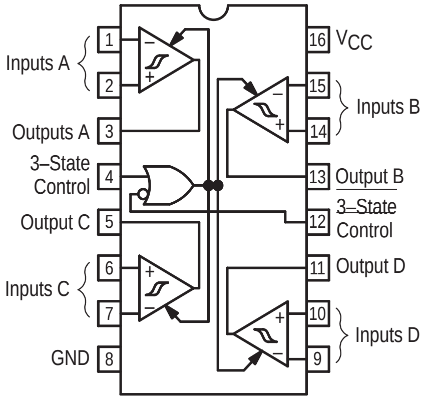
D SUFFIX
PLASTIC PACKAGE
CASE 751B
(SO–16)





PC SUFFIX
PLASTIC PACKAGE
CASE 648

PIN CONNECTIONS



ORDERING INFORMATION

Device	Operating Temperature Range	Package
AM26LS32PC	T_A = 0 to 70°C	Plastic DIP
MC26LS32D*		SO–16

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	7.0	Vdc
Input Common Mode Voltage	V_{ICM}	± 25	Vdc
Input Differential Voltage	V_{ID}	± 25	Vdc
Three–State Control Input Voltage	V_I	7.0	Vdc
Output Sink Current	I_O	50	mA
Storage Temperature	T_{stg}	– 65 to + 150	°C
Operating Junction Temperature	T_J	+ 150	°C

RECOMMENDED OPERATING CONDITIONS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	4.75 to 5.25	Vdc
Operating Ambient Temperature	T_A	0 to + 70	°C
Input Common Mode Voltage Range	V_{ICR}	– 7.0 to + 7.0	Vdc
Input Differential Voltage Range	V_{IDR}	6.0	Vdc

ELECTRICAL CHARACTERISTICS (Unless otherwise noted, minimum and maximum limits apply over recommended temperature and power supply voltage ranges. Typical values are for T_A = 25°C, V_{CC} = 5.0 V and V_{IC} = 0 V. See Note 1.)

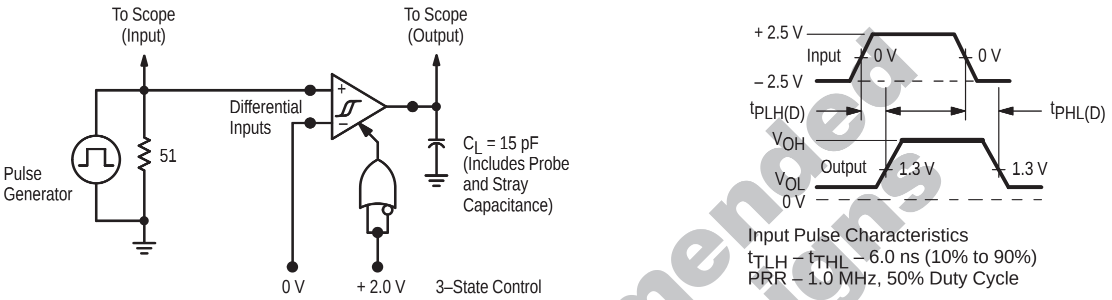
Characteristic	Symbol	Min	Typ	Max	Unit
Input Voltage – High Logic State (Three–State Control)	V_{IH}	2.0	–	–	V
Input Voltage – Low Logic State (Three–State Control)	V_{IL}	–	–	0.8	V
Differential Input Threshold Voltage (Note 2) (–7.0 V ≤ V_{IC} ≤ 7.0 V, V_{IH} = 2.0 V) (I_O = –0.4 mA, V_{OH} ≥ 2.7 V) (I_O = 8.0 mA, V_{OL} ≤ 0.45 V)	$V_{TH(D)}$	– –	– –	0.2 –0.2	V
Input Bias Current (V_{CC} = 0 V or 5.25) (Other Inputs at –15 V ≤ V_{in} ≤ +15 V) V_{in} = +15 V V_{in} = –15 V	$I_{IB(D)}$	– –	– –	2.3 –2.8	mA
Input Resistance (–15 V ≤ V_{in} ≤ +15 V)	R_{in}	6.0 K	–	–	Ohms
Input Balance and Output Level (–7.0 V ≤ V_{IC} ≤ 7.0 V, V_{IH} = 2.0 V, See Note 3) (I_O = –0.4 mA, V_{ID} = 0.4 V) (I_O = 8.0 mA, V_{ID} = –0.4 V)	V_{OH} V_{OL}	2.7 –	– –	– 0.45	V
Output Third State Leakage Current ($V_{I(D)}$ = + 3.0 V, V_{IL} = 0.8 V, V_O = 0.4 V) ($V_{I(D)}$ = – 3.0 V, V_{IL} = 0.8 V, V_O = 2.4 V)	I_{OZ}	– –	– –	–20 20	µA
Output Short Circuit Current ($V_{I(D)}$ = 3.0 V, V_{IH} = 2.0 V, V_O = 0 V, See Note 4)	I_{OS}	–15	–	–85	mA
Input Current – Low Logic State (Three–State Control) (V_{IL} = 0.4 V)	I_{IL}	–	–	–360	µA
Input Current – High Logic State (Three–State Control) (V_{IH} = 2.7 V) (V_{IH} = 5.5 V)	I_{IH}	– –	– –	20 100	µA
Input Clamp Diode Voltage (Three–State Control) (I_{IC} = –18 mA)	V_{IK}	–	–	–1.5	V
Power Supply Current (V_{IL} = 0 V) (All Inputs Grounded)	I_{CC}	–	–	70	mA

NOTES: 1. All currents into device pins are shown as positive, out of device pins are negative. All voltages referenced to ground unless otherwise noted.
2. Differential input threshold voltage and guaranteed output levels are done simultaneously for worst case.
3. Refer to EIA–422/3 for exact conditions. Input balance and guaranteed output levels are done simultaneously for worst case.
4. Only one output at a time should be shorted.

SWITCHING CHARACTERISTICS (V_{CC} = 5.0 V and T_A = 25°C, unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Propagation Delay Time – DIfferential Inputs to Output					ns
(Output High to Low)	$t_{PHL(D)}$	–	–	30	
(Output Low to High)	$t_{PLH(D)}$	–	–	30	
Propagation Delay Time – Three–State Control to Output					ns
(Output Low to Third State)	t_{PLZ}	–	–	35	
(Output High to Third State)	t_{PHZ}	–	–	35	
(Output Third State to High)	t_{PZH}	–	–	30	
(Output Third State to Low)	t_{PZL}	–	–	30	

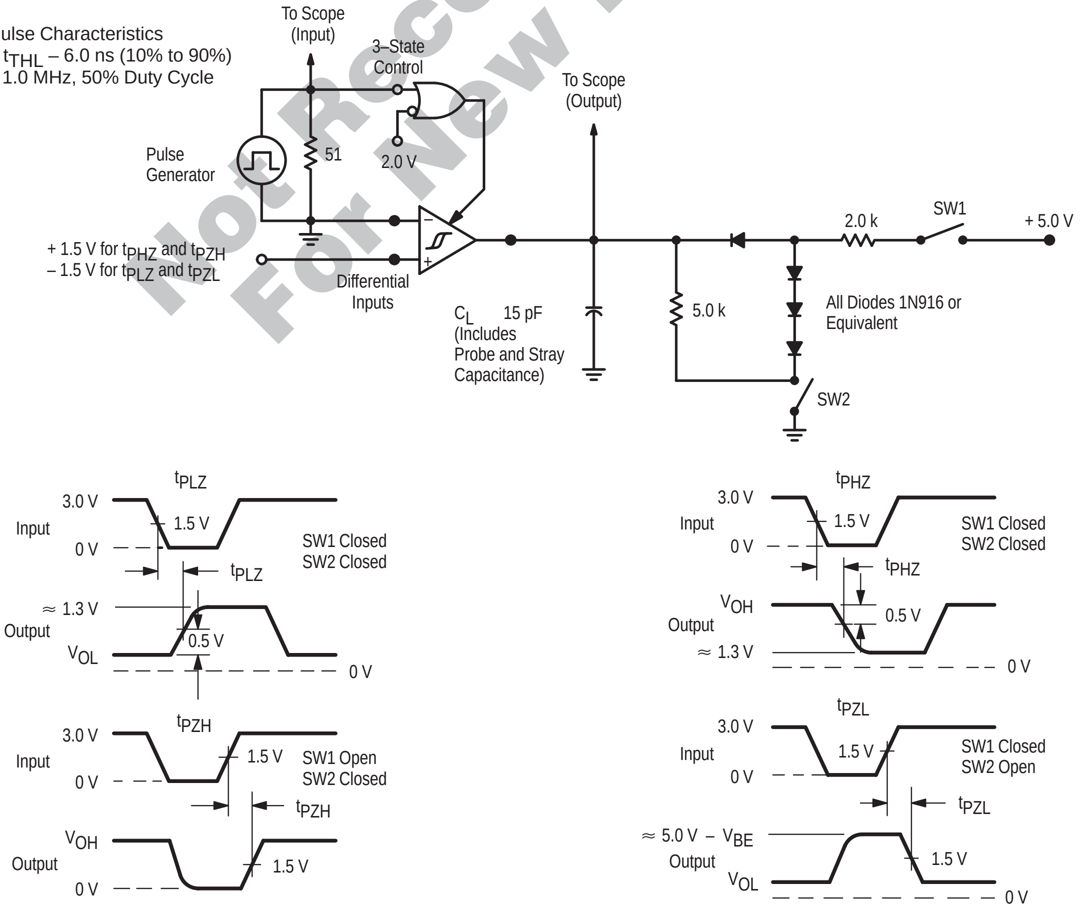
Figure 1. Switching Test Circuit and Wave for Propagation Delay Differential Input to Output



Input Pulse Characteristics
t_{TLH} – t_{THL} – 6.0 ns (10% to 90%)
PRR – 1.0 MHz, 50% Duty Cycle

Figure 2. Propagation Delay Three–State Control Input to Output

Input Pulse Characteristics
t_{TLH} – t_{THL} – 6.0 ns (10% to 90%)
PRR – 1.0 MHz, 50% Duty Cycle



MOTOROLA

MC1413, B
MC1416, B

High Voltage, High Current Darlington Transistor Arrays

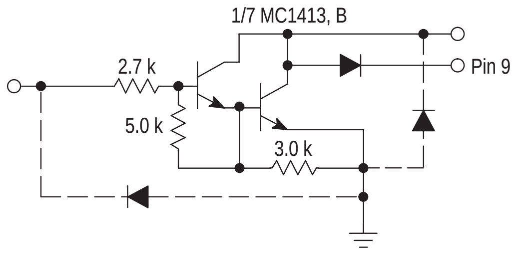
The seven NPN Darlington connected transistors in these arrays are well suited for driving lamps, relays, or printer hammers in a variety of industrial and consumer applications. Their high breakdown voltage and internal suppression diodes insure freedom from problems associated with inductive loads. Peak inrush currents to 500 mA permit them to drive incandescent lamps.

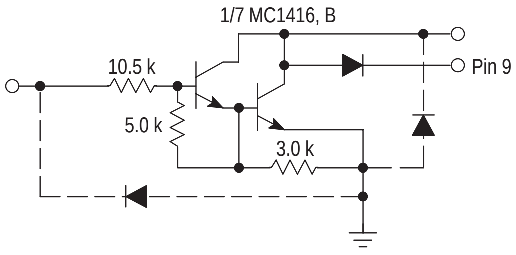
The MC1413, B with a 2.7 kΩ series input resistor is well suited for systems utilizing a 5.0 V TTL or CMOS Logic. The MC1416, B uses a series 10.5 kΩ resistor and is useful in 8.0 to 18 V MOS systems.

ORDERING INFORMATION

Plastic DIP	SOIC	Operating Temperature Range
MC1413P (ULN2003A) MC1416P (ULN2004A)	MC1413D MC1416D	T_A = –20° to +85°C
MC1413BP MC1416BP	MC1413BD MC1416BD	T_A = –40° to +85°C

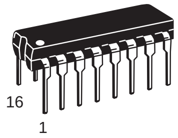
Representative Schematic Diagrams



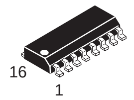


PERIPHERAL DRIVER ARRAYS

SEMICONDUCTOR TECHNICAL DATA

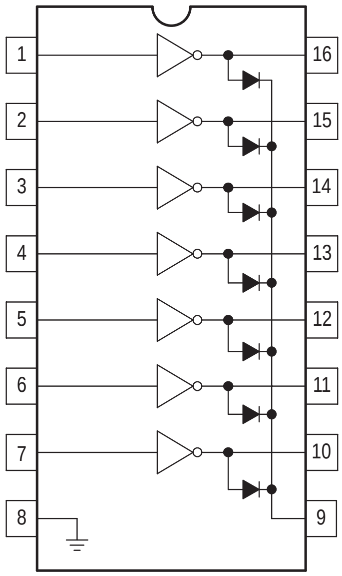


P SUFFIX
PLASTIC PACKAGE
CASE 648



D SUFFIX
PLASTIC PACKAGE
CASE 751B
(SO–16)

PIN CONNECTIONS



(Top View)

MAXIMUM RATINGS (T_A = 25°C, and rating apply to any one device in the package, unless otherwise noted.)

Rating	Symbol	Value	Unit
Output Voltage	V_O	50	V
Input Voltage	V_I	30	V
Collector Current – Continuous	I_C	500	mA
Base Current – Continuous	I_B	25	mA
Operating Ambient Temperature Range MC1413–16 MC1413B–16B	T_A	 –20 to +85 –40 to +85	°C
Storage Temperature Range	T_{stg}	–55 to +150	°C
Junction Temperature	T_J	150	°C
Thermal Resistance, Junction–to–Ambient Case 648, P Suffix Case 751B, D Suffix	θ_{JA}	 67 100	°C/W

NOTE: ESD data available upon request.

ELECTRICAL CHARACTERISTICS (T_A = 25°C, unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Output Leakage Current (V_O = 50 V, T_A = +85°C) (V_O = 50 V, T_A = +25°C) (V_O = 50 V, T_A = +85°C, V_I = 1.0 V)	 All Types All Types MC1416, B	I_{CEX}	 – – –	 – – –	 100 50 500	µA
Collector–Emitter Saturation Voltage (I_C = 350 mA, I_B = 500 µA) (I_C = 200 mA, I_B = 350 µA) (I_C = 100 mA, I_B = 250 µA)	 All Types All Types All Types	$V_{CE(sat)}$	 – – –	 1.1 0.95 0.85	 1.6 1.3 1.1	V
Input Current – On Condition (V_I = 3.85 V) (V_I = 5.0 V) (V_I = 12 V)	 MC1413, B MC1416, B MC1416, B	$I_{I(on)}$	 – – –	 0.93 0.35 1.0	 1.35 0.5 1.45	mA
Input Voltage – On Condition (V_{CE} = 2.0 V, I_C = 200 mA) (V_{CE} = 2.0 V, I_C = 250 mA) (V_{CE} = 2.0 V, I_C = 300 mA) (V_{CE} = 2.0 V, I_C = 125 mA) (V_{CE} = 2.0 V, I_C = 200 mA) (V_{CE} = 2.0 V, I_C = 275 mA) (V_{CE} = 2.0 V, I_C = 350 mA)	 MC1413, B MC1413, B MC1413, B MC1416, B MC1416, B MC1416, B MC1416, B	$V_{I(on)}$	 – – – – – – –	 – – – – – – –	 2.4 2.7 3.0 5.0 6.0 7.0 8.0	V
Input Current – Off Condition (I_C = 500 µA, T_A = 85°C)	All Types	$I_{I(off)}$	50	100	–	µA
DC Current Gain (V_{CE} = 2.0 V, I_C = 350 mA)		h_{FE}	1000	–	–	–
Input Capacitance		C_I	–	15	30	pF
Turn–On Delay Time (50% E_I to 50% E_O)		t_{on}	–	0.25	1.0	µs
Turn–Off Delay Time (50% E_I to 50% E_O)		t_{off}	–	0.25	1.0	µs
Clamp Diode Leakage Current (V_R = 50 V)	T_A = +25°C T_A = +85°C	I_R	– –	– –	50 100	µA
Clamp Diode Forward Voltage (I_F = 350 mA)		V_F	–	1.5	2.0	V

TYPICAL PERFORMANCE CURVES – $T_A = 25°C$

Figure 1. Output Current versus Input Voltage

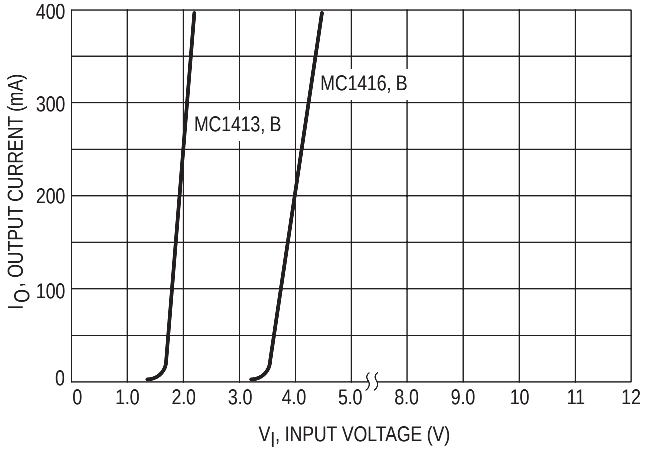


Figure 2. Output Current versus Input Current

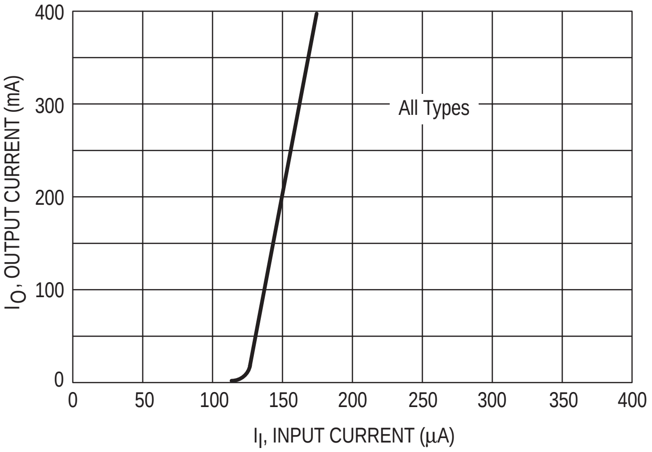


Figure 3. Typical Output Characteristics

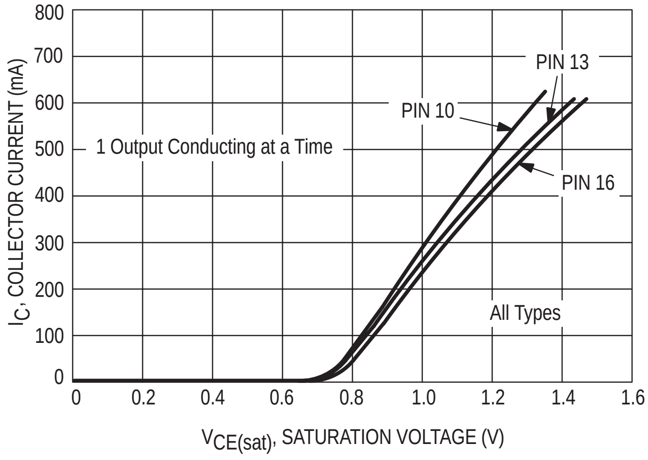


Figure 4. Input Characteristics – MC1413, B

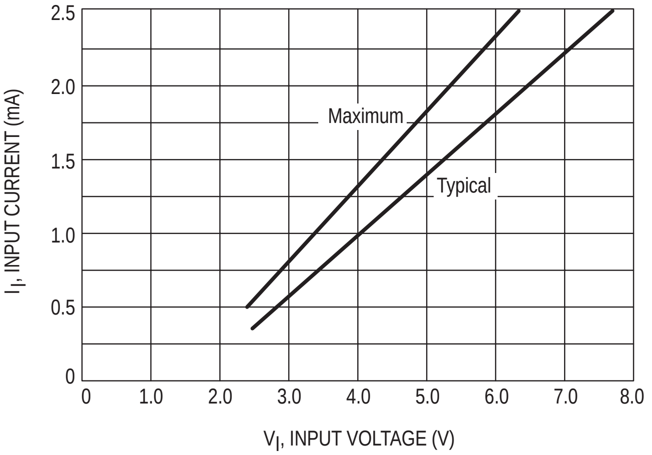


Figure 5. Input Characteristics – MC1416, B

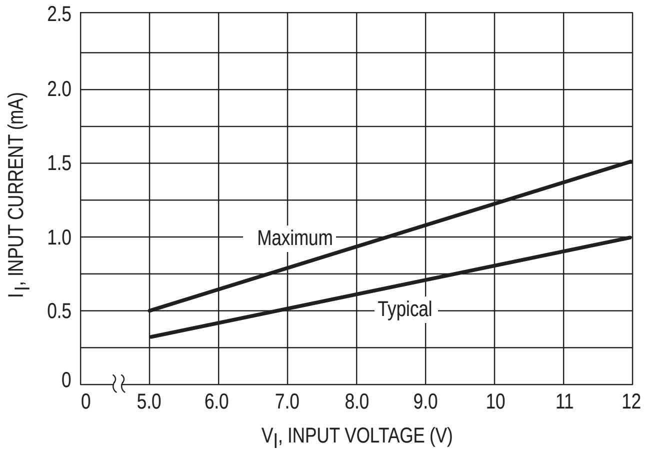
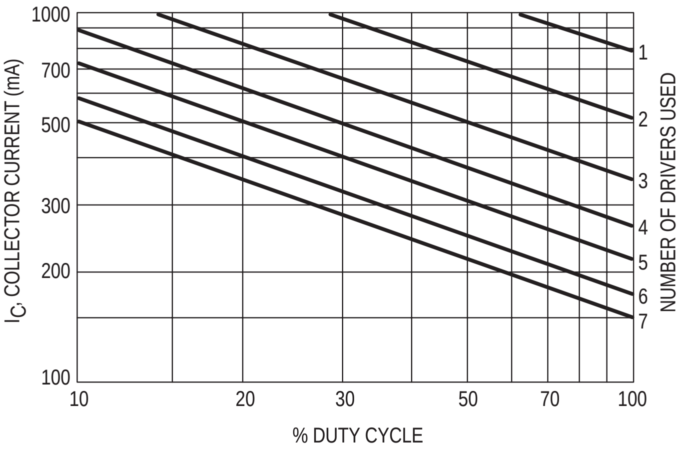


Figure 6. Maximum Collector Current versus Duty Cycle (and Number of Drivers in Use)



MOTOROLA

MC1488

Quad Line Driver

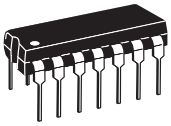
The MC1488 is a monolithic quad line driver designed to interface data terminal equipment with data communications equipment in conformance with the specifications of EIA Standard No. EIA–232D.

Features:

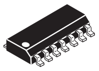
- Current Limited Output
  ±10 mA typical
- Power–Off Source Impedance
  300 Ω mininum
- Simple Slew Rate Control with External Capacitor
- Flexible Operating Supply Range
- Compatible with All Motorola MDTL and MTTL Logic Families

QUAD MDTL LINE DRIVER
EIA–232D

SEMICONDUCTOR
TECHNICAL DATA



P SUFFIX
PLASTIC PACKAGE
CASE 646

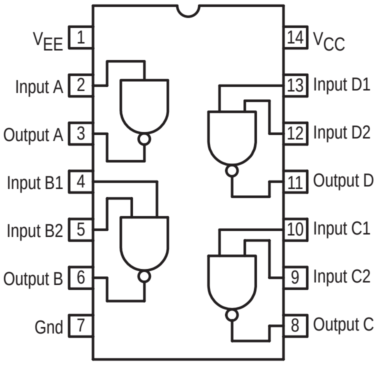


D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO–14)

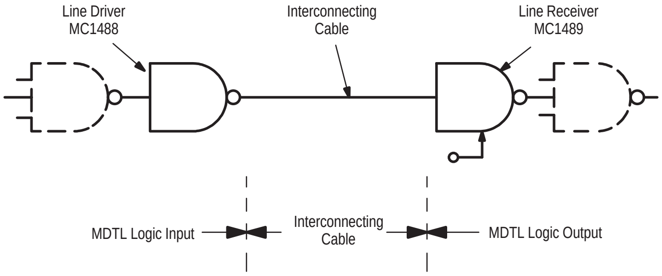
ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC1488P	T_A = 0 to + 75°C	Plastic
MC1488D		SO–14

PIN CONNECTIONS

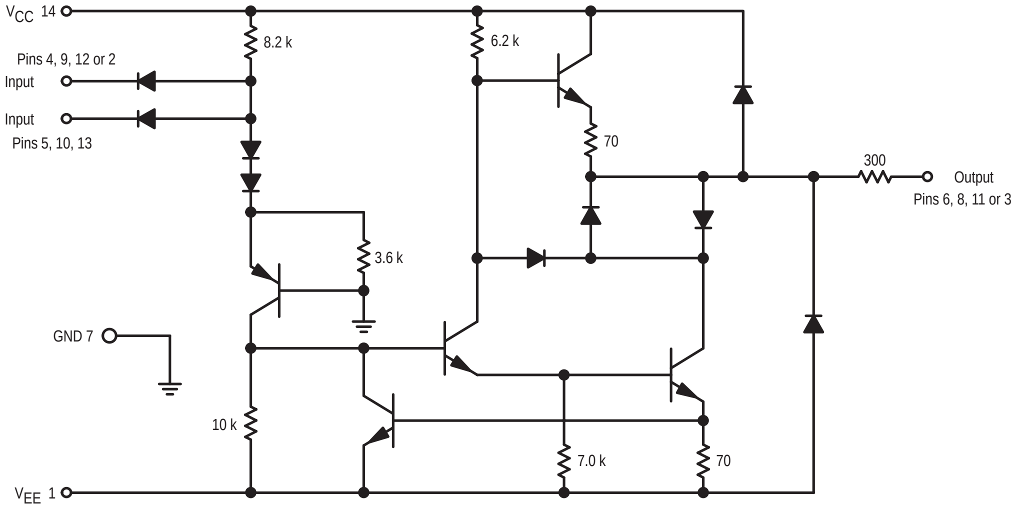


Simplified Application



Circuit Schematic

(1/4 of Circuit Shown)



MAXIMUM RATINGS (T_A = + 25°C, unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC} V_{EE}	+ 15 – 15	Vdc
Input Voltage Range	V_{IR}	$-15 \leq V_{IR} \leq 7.0$	Vdc
Output Signal Voltage	V_O	±15	Vdc
Power Derating (Package Limitation, SO–14 and Plastic Dual–In–Line Package) Derate above T_A = + 25°C	P_D $1/R_{\theta JA}$	1000 6.7	mW mW/°C
Operating Ambient Temperature Range	T_A	0 to + 75	°C
Storage Temperature Range	T_{stg}	– 65 to + 175	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = + 9.0 ± 1% Vdc, V_{EE} = – 9.0 ± 1% Vdc, T_A = 0 to 75°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Current – Low Logic State (V_{IL} = 0)	I_{IL}	–	1.0	1.6	mA
Input Current – High Logic State (V_{IH} = 5.0 V)	I_{IH}	–	–	10	µA
Output Voltage – High Logic State	V_{OH}				Vdc
(V_{IL} = 0.8 Vdc, R_L = 3.0 kΩ, V_{CC} = + 9.0 Vdc, V_{EE} = – 9.0 Vdc)		+ 6.0	+ 7.0	–	
(V_{IL} = 0.8 Vdc, R_L = 3.0 kΩ, V_{CC} = + 13.2 Vdc, V_{EE} = – 13.2 Vdc)		+ 9.0	+ 10.5	–	
Output Voltage – Low Logic State	V_{OL}				Vdc
(V_{IH} = 1.9 Vdc, R_L = 3.0 kΩ, V_{CC} = + 9.0 Vdc, V_{EE} = – 9.0 Vdc)		– 6.0	– 7.0	–	
(V_{IH} = 1.9 Vdc, R_L = 3.0 kΩ, V_{CC} = + 13.2 Vdc, V_{EE} = – 13.2 Vdc)		– 9.0	– 10.5	–	
Positive Output Short–Circuit Current, Note 1	I_{OS+}	+ 6.0	+ 10	+ 12	mA
Negative Output Short–Circuit Current, Note 1	I_{OS-}	– 6.0	– 10	– 12	mA
Output Resistance (V_{CC} = V_{EE} = 0, $\lvert V_O \rvert$ = ± 2.0 V)	r_o	300	–	–	Ohms
Positive Supply Current (R_I = ∞)	I_{CC}				mA
(V_{IH} = 1.9 Vdc, V_{CC} = + 9.0 Vdc)		–	+ 15	+ 20	
(V_{IL} = 0.8 Vdc, V_{CC} = + 9.0 Vdc)		–	+ 4.5	+ 6.0	
(V_{IH} = 1.9 Vdc, V_{CC} = + 12 Vdc)		–	+ 19	+ 25	
(V_{IL} = 0.8 Vdc, V_{CC} = + 12 Vdc)		–	+ 5.5	+ 7.0	
(V_{IH} = 1.9 Vdc, V_{CC} = + 15 Vdc)		–	–	+ 34	
(V_{IL} = 0.8 Vdc, V_{CC} = + 15 Vdc)		–	–	+ 12	
Negative Supply Current (R_L = ∞)	I_{EE}				
(V_{IH} = 1.9 Vdc, V_{EE} = – 9.0 Vdc)		–	– 13	– 17	mA
(V_{IL} = 0.8 Vdc, V_{EE} = – 9.0 Vdc)		–	–	– 500	µA
(V_{IH} = 1.9 Vdc, V_{EE} = – 12 Vdc)		–	– 18	– 23	mA
(V_{IL} = 0.8 Vdc, V_{EE} = – 12 Vdc)		–	–	– 500	µA
(V_{IH} = 1.9 Vdc, V_{EE} = – 15 Vdc)		–	–	– 34	mA
(V_{IL} = 0.8 Vdc, V_{EE} = – 15 Vdc)		–	–	– 2.5	mA
Power Consumption	P_C				mW
(V_{CC} = 9.0 Vdc, V_{EE} = – 9.0 Vdc)		–	–	333	
(V_{CC} = 12 Vdc, V_{EE} = – 12 Vdc)		–	–	576	

SWITCHING CHARACTERISTICS (V_{CC} = + 9.0 ± 1% Vdc, V_{EE} = – 9.0 ± 1% Vdc, T_A = + 25°C.)

Propagation Delay Time	(z_I = 3.0 k and 15 pF)	t_{PLH}	–	275	350	ns
Fall Time	(z_I = 3.0 k and 15 pF)	t_{THL}	–	45	75	ns
Propagation Delay Time	(z_I = 3.0 k and 15 pF)	t_{PHL}	–	110	175	ns
Rise Time	(z_I = 3.0 k and 15 pF)	t_{TLH}	–	55	100	ns

NOTE: 1. Maximum Package Power Dissipation may be exceeded if all outputs are shorted simultaneously.

CHARACTERISTIC DEFINITIONS

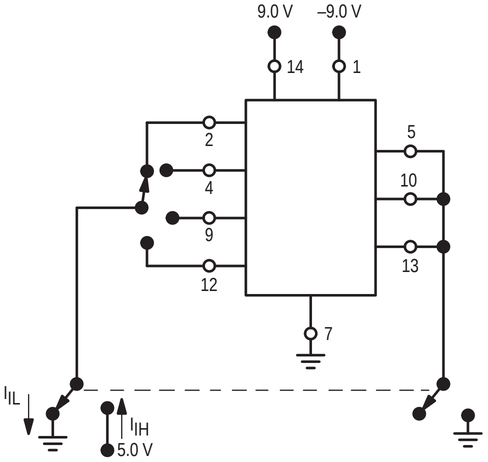


Figure 1. Input Current

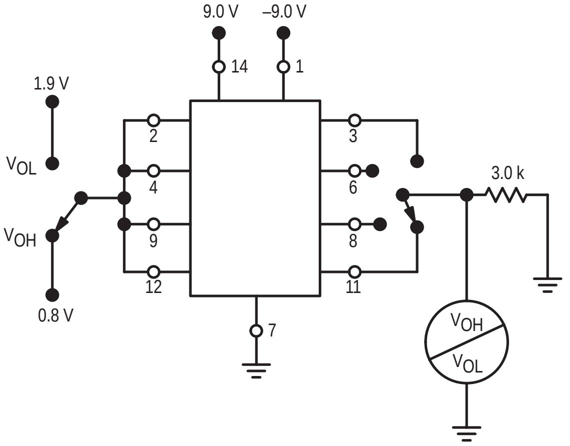


Figure 2. Output Voltage

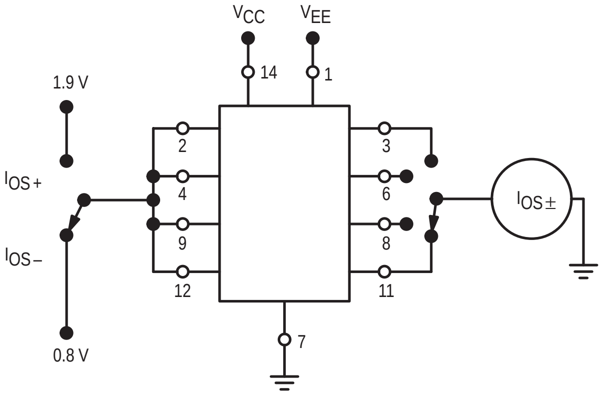


Figure 3. Output Short–Circuit Current

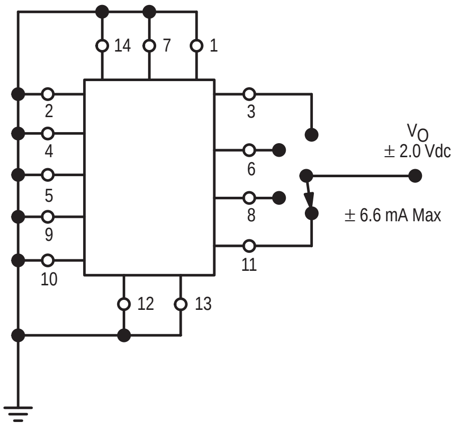


Figure 4. Output Resistance (Power Off)

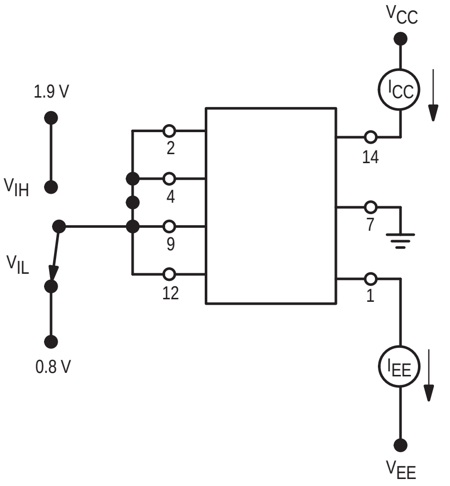


Figure 5. Power Supply Currents

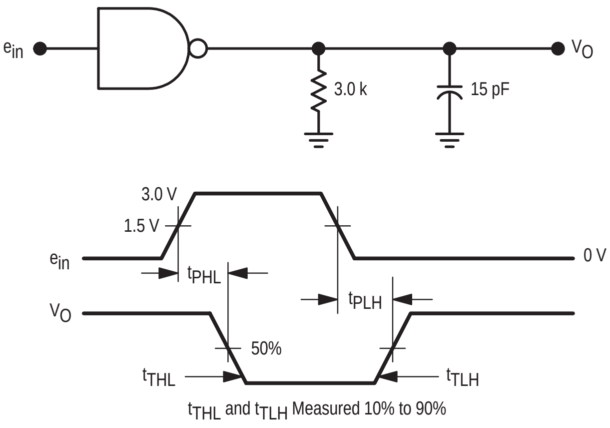


Figure 6. Switching Response

TYPICAL CHARACTERISTICS

(T_A = +25°C, unless otherwise noted.)

Figure 7. Transfer Characteristics versus Power Supply Voltage

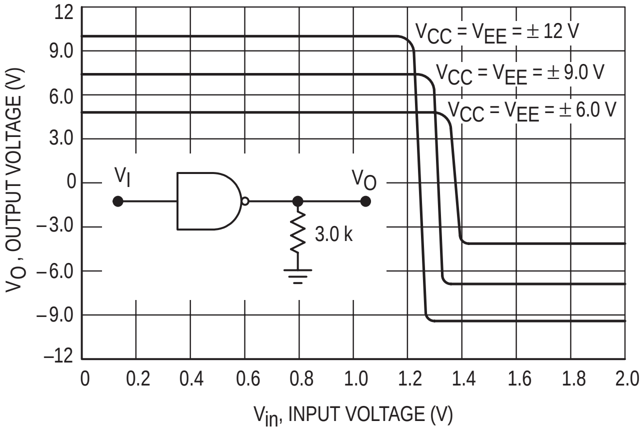


Figure 8. Short Circuit Output Current versus Temperature

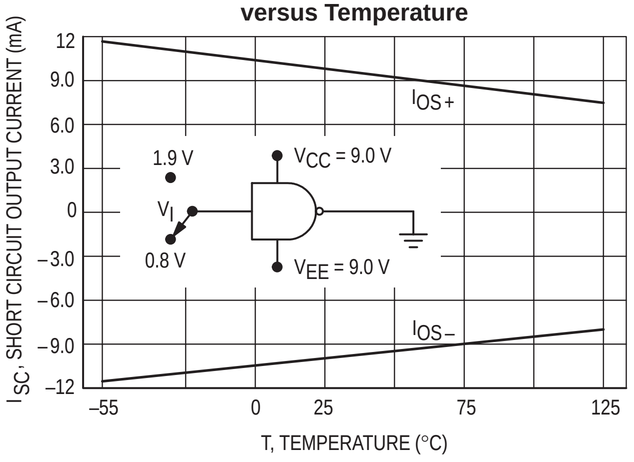


Figure 9. Output Slew Rate versus Load Capacitance

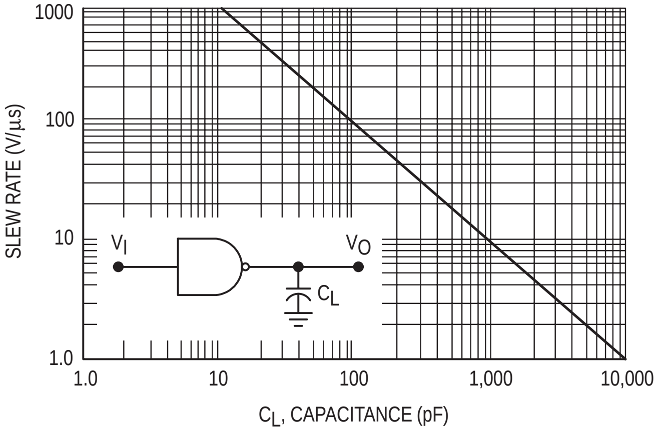


Figure 10. Output Voltage and Current–Limiting Characteristics

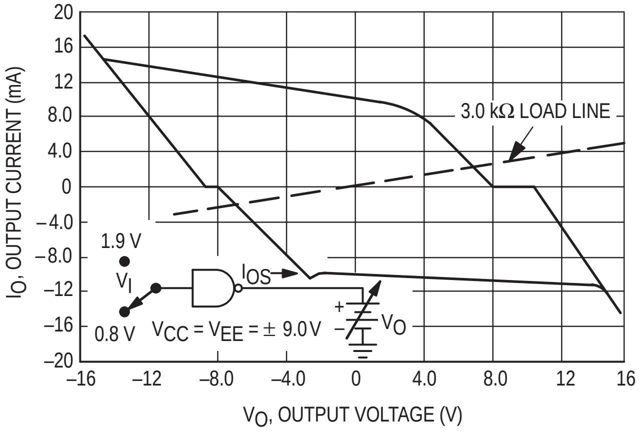
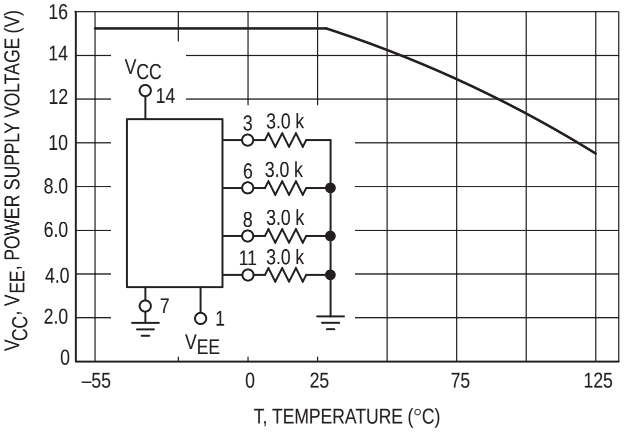


Figure 11. Maximum Operating Temperature versus Power Supply Voltage



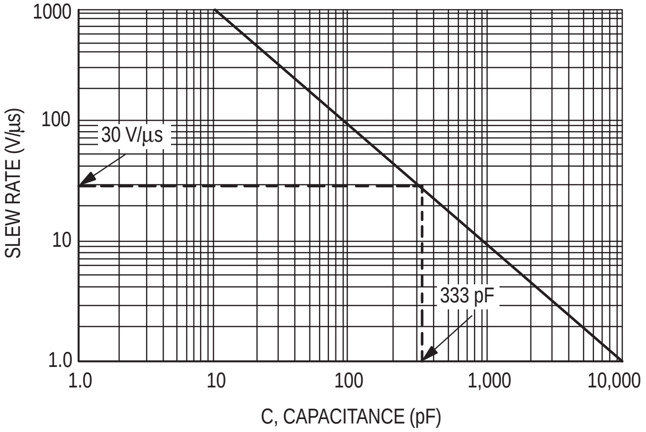
APPLICATIONS INFORMATION

The Electronic Industries Association EIA–232D specification details the requirements for the interface between data processing equipment and data communications equipment. This standard specifies not only the number and type of interface leads, but also the voltage levels to be used. The MC1488 quad driver and its companion circuit, the MC1489 quad receiver, provide a complete interface system between DTL or TTL logic levels and the EIA–232D defined levels. The EIA–232D requirements as applied to drivers are discussed herein.

The required driver voltages are defined as between 5.0 and 15 V in magnitude and are positive for a Logic “0” and negative for a Logic “1.” These voltages are so defined when the drivers are terminated with a 3000 to 7000 Ω resistor. The MC1488 meets this voltage requirement by converting a DTL/TTL logic level into EIA–232D levels with one stage of inversion.

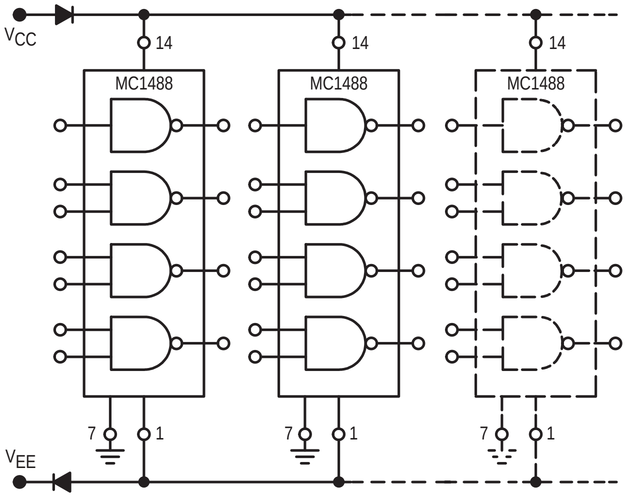
The EIA–232D specification further requires that during transitions, the driver output slew rate must not exceed 30 V per microsecond. The inherent slew rate of the MC1488 is much too fast for this requirement. The current limited output of the device can be used to control this slew rate by connecting a capacitor to each driver output. The required capacitor can be easily determined by using the relationship $C = I_{OS} \times \Delta T/\Delta V$ from which Figure 12 is derived. Accordingly, a 330 pF capacitor on each output will guarantee a worst case slew rate of 30 V per microsecond.

Figure 12. Slew Rate versus Capacitance for I_{SC} = 10 mA



The interface driver is also required to withstand an accidental short to any other conductor in an interconnecting cable. The worst possible signal on any conductor would be another driver using a plus or minus 15 V, 500 mA source. The MC1488 is designed to indefinitely withstand such a short to all four outputs in a package as long as the power supply voltages are greater than 9.0 V (i.e., $V_{CC} \geqslant 9.0$ V; $V_{EE} \leqslant -9.0$ V). In some power supply designs, a loss of system power causes a low impedance on the power supply outputs. When this occurs, a low impedance to ground would exist at the power inputs to the MC1488 effectively shorting the 300 Ω output resistors to ground. If all four outputs were then shorted to plus or minus 15 V, the power dissipation in these resistors would be excessive. Therefore, if the system is designed to permit low impedances to ground at the power supplies of the drivers, a diode should be placed in each power supply lead to prevent overheating in this fault condition. These two diodes, as shown in Figure 13, could be used to decouple all the driver packages in a system. (These same diodes will allow the MC1488 to withstand momentary shorts to the ± 25 V limits specified in the earlier Standard EIA–232B.) The addition of the diodes also permits the MC1488 to withstand faults with power supplies of less than the 9.0 V stated above.

Figure 13. Power Supply Protection to Meet Power Off Fault Conditions



The maximum short circuit current allowable under fault conditions is more than guaranteed by the previously mentioned 10 mA output current limiting.

Other Applications

The MC1488 is an extremely versatile line driver with a myriad of possible applications. Several features of the drivers enhance this versatility:

1. Output Current Limiting – this enables the circuit designer to define the output voltage levels independent of power supplies and can be accomplished by diode clamping of the output pins. Figure 14 shows the MC1488 used as a DTL to MOS translator where the high level voltage output is clamped one diode above ground. The resistor divider shown is used to reduce the output voltage below the 300 mV above ground MOS input level limit.

2. Power Supply Range – as can be seen from the schematic drawing of the drivers, the positive and negative driving elements of the device are essentially independent and do not require matching power supplies. In fact, the positive supply can vary from a minimum 7.0 V (required for driving the negative pulldown section) to the maximum specified 15 V. The negative supply can vary from approximately – 2.5 V to the minimum specified – 15 V. The MC1488 will drive the output to within 2.0 V of the positive or negative supplies as long as the current output limits are not exceeded. The combination of the current limiting and supply voltage features allow a wide combination of possible outputs within the same quad package. Thus if only a portion of the four drivers are used for driving EIA–232D lines, the remainder could be used for DTL to MOS or even DTL to DTL translation. Figure 15 shows one such combination.

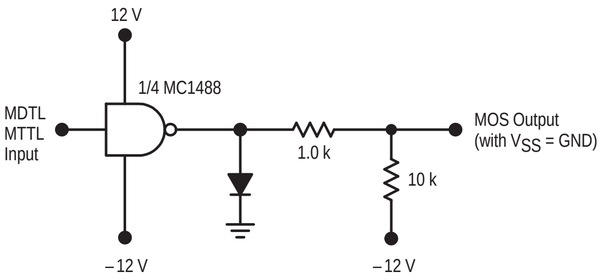


Figure 14. MDTL/MTTL–to–MOS Translator

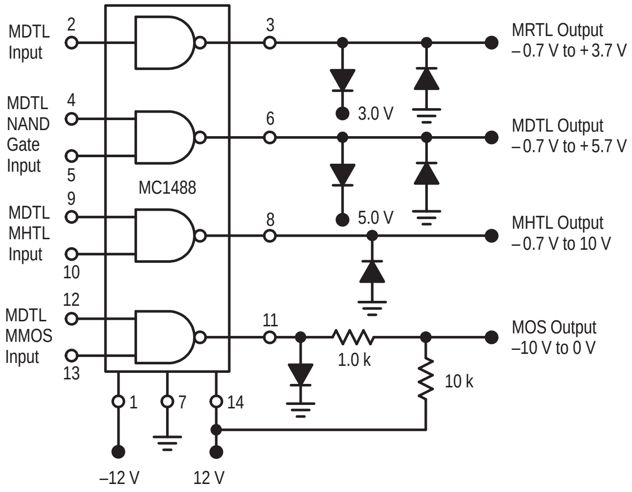


Figure 15. Logic Translator Applications

MOTOROLA

MC1489, A

Quad Line Receivers

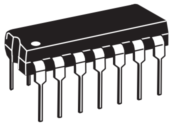
The MC1489 monolithic quad line receivers are designed to interface data terminal equipment with data communications equipment in conformance with the specifications of EIA Standard No. EIA–232D.

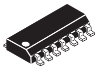
- Input Resistance – 3.0 k to 7.0 kΩ
- Input Signal Range – ± 30 V
- Input Threshold Hysteresis Built In
- Response Control
  - a) Logic Threshold Shifting
  - b) Input Noise Filtering

QUAD MDTL
LINE RECEIVERS
EIA–232D

SEMICONDUCTOR
TECHNICAL DATA

P SUFFIX
PLASTIC PACKAGE
CASE 646



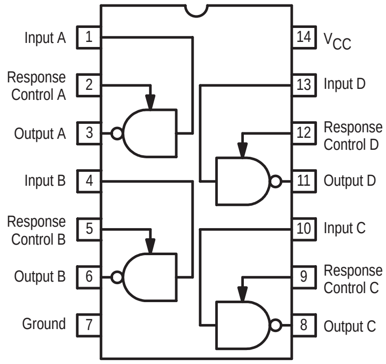


D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO–14)

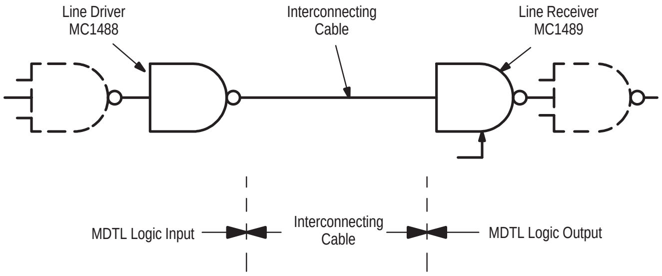
ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC1489P, AP	T_A = 0 to + 75°C	Plastic
MC1489D, AD		SO–14

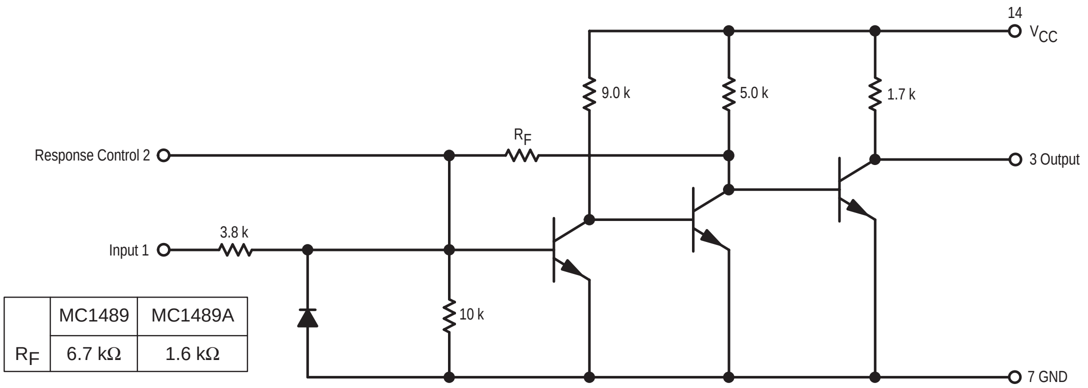
PIN CONNECTIONS



Simplified Application



Representative Schematic Diagram
(1/4 of Circuit Shown)



	MC1489	MC1489A
R_F	6.7 kΩ	1.6 kΩ

MAXIMUM RATINGS (T_A = + 25°C, unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	10	Vdc
Input Voltage Range	V_{IR}	± 30	Vdc
Output Load Current	I_L	20	mA
Power Dissipation (Package Limitation, SO–14 and Plastic Dual In–Line Package) Derate above T_A = + 25°C	P_D $1/\theta_{JA}$	1000 6.7	mW mW/°C
Operating Ambient Temperature Range	T_A	0 to + 75	°C
Storage Temperature Range	T_{stg}	– 65 to + 175	°C

ELECTRICAL CHARACTERISTICS (Response control pin is open.) (V_{CC} = + 5.0 Vdc ± 10%, T_A = 0 to + 75°C, unless otherwise noted)

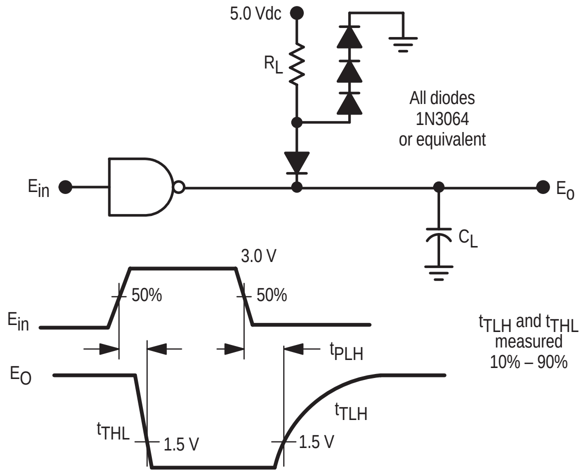
Characteristics		Symbol	Min	Typ	Max	Unit
Positive Input Current	(V_{IH} = + 25 Vdc) (V_{IH} = + 3.0 Vdc)	I_{IH}	3.6 0.43	– –	8.3 –	mA
Negative Input Current	(V_{IH} = – 25 Vdc) (V_{IH} = – 3.0 Vdc)	I_{IL}	– 3.6 – 0.43	– –	– 8.3 –	mA
Input Turn–On Threshold Voltage (T_A = + 25°C, $V_{OL} \leqslant$ 0.45 V)	MC1489 MC1489A	V_{IH}	1.0 1.75	– 1.95	1.5 2.25	Vdc
Input Turn–Off Threshold Voltage (T_A = + 25°C, $V_{OH} \geqslant$ 2.5 V, I_L = – 0.5 mA)	MC1489 MC1489A	V_{IL}	0.75 0.75	– 0.8	1.25 1.25	Vdc
Output Voltage High	(V_{IH} = 0.75 V, I_L = – 0.5 mA) (Input Open Circuit, I_L = – 0.5 mA)	V_{OH}	2.5 2.5	4.0 4.0	5.0 5.0	Vdc
Output Voltage Low	(V_{IL} = 3.0 V, I_L = 10 mA)	V_{OL}	–	0.2	0.45	Vdc
Output Short–Circuit Current		I_{OS}	–	– 3.0	– 4.0	mA
Power Supply Current (All Gates “on,” I_{out} = 0 mA, V_{IH} = + 5.0 Vdc)		I_{CC}	–	16	26	mA
Power Consumption	(V_{IH} = + 5.0 Vdc)	P_C	–	80	130	mW

SWITCHING CHARACTERISTICS (V_{CC} = 5.0 Vdc ± 1%, T_A = + 25°C, See Figure 1.)

Propagation Delay Time	(R_L = 3.9 kΩ)	t_{PLH}	–	25	85	ns
Rise Time	(R_L = 3.9 kΩ)	t_{TLH}	–	120	175	ns
Propagation Delay Time	(R_L = 390 kΩ)	t_{PHL}	–	25	50	ns
Fall Time	(R_L = 390 kΩ)	t_{THL}	–	10	20	ns

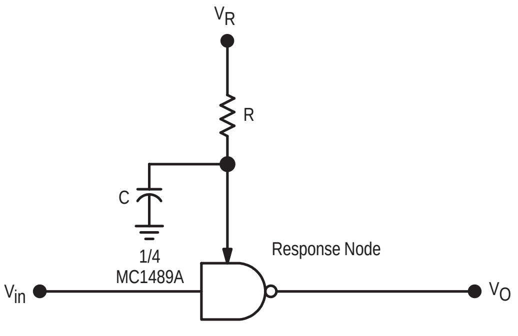
TEST CIRCUITS

Figure 1. Switching Response



C_L = 15 pF = total parasitic capacitance which includes probe and wiring capacitances

Figure 2. Response Control Node



C, capacitor is for noise filtering.
R, resistor is for threshold shifting.

TYPICAL CHARACTERISTICS

(V_{CC} = 5.0 Vdc, T_A = +25°C, unless otherwise noted)

Figure 3. Input Current

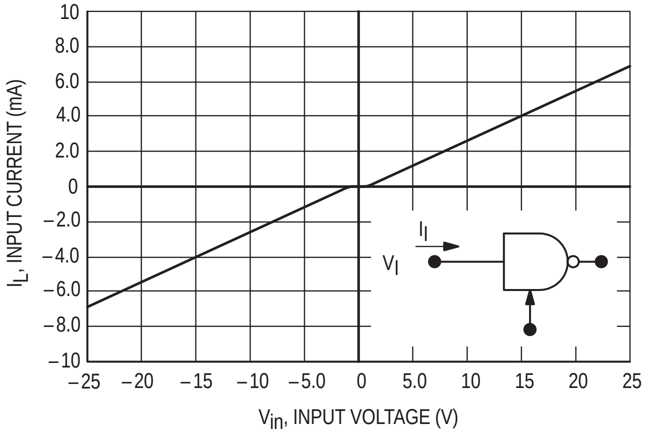


Figure 4. MC1489 Input Threshold Voltage Adjustment

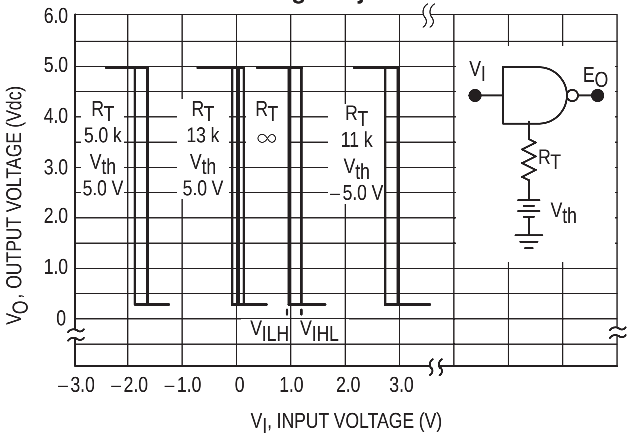


Figure 5. MC1489A Input Threshold Voltage Adjustment

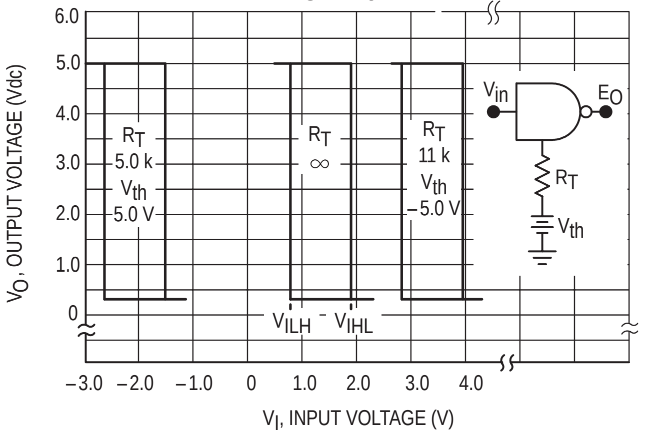


Figure 6. Input Threshold Voltage versus Temperature

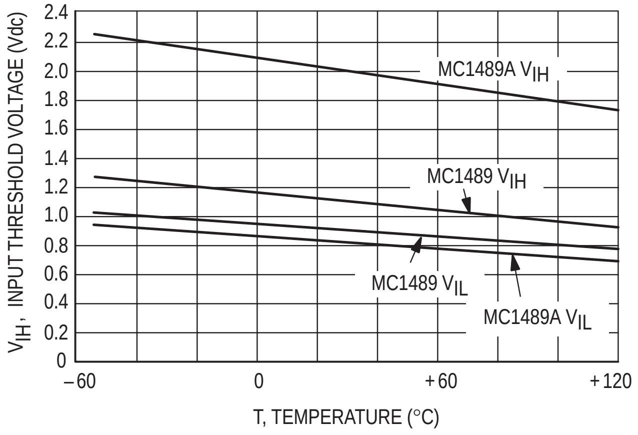
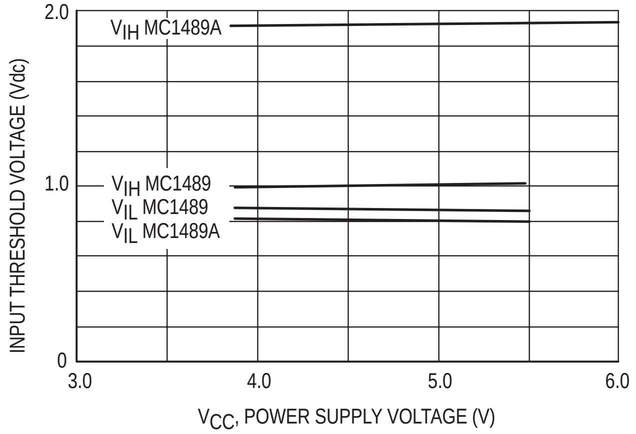


Figure 7. Input Threshold versus Power Supply Voltage



APPLICATIONS INFORMATION

General Information

The Electronic Industries Association (EIA) has released the EIA–232D specification detailing the requirements for the interface between data processing equipment and data communications equipment. This standard specifies not only the number and type of interface leads, but also the voltage levels to be used. The MC1488 quad driver and its companion circuit, the MC1489 quad receiver, provide a complete interface system between DTL or TTL logic levels and the EIA–232D defined levels. The EIA–232D requirements as applied to receivers are discussed herein.

The required input impedance is defined as between 3000 Ω and 7000 Ω for input voltages between 3.0 and 25 V in magnitude; and any voltage on the receiver input in an open circuit condition must be less than 2.0 V in magnitude. The MC1489 circuits meet these requirements with a maximum open circuit voltage of one V_{BE}.

The receiver shall detect a voltage between – 3.0 and – 25 V as a Logic “1” and inputs between 3.0 and 25 V as a Logic “0.” On some interchange leads, an open circuit of power “OFF” condition (300 Ω or more to ground) shall be decoded as an “OFF” condition or Logic “1.” For this reason, the input hysteresis thresholds of the MC1489 circuits are all above ground. Thus an open or grounded input will cause the same output as a negative or Logic “1” input.

Device Characteristics

The MC1489 interface receivers have internal feedback from the second stage to the input stage providing input hysteresis for noise rejection. The MC1489 input has typical turn–on voltage of 1.25 V and turn–off of 1.0 V for a typical hysteresis of 250 mV. The MC1489A has typical turn–on of 1.95 V and turn–off of 0.8 V for typically 1.15 V of hysteresis.

Each receiver section has an external response control node in addition to the input and output pins, thereby allowing the designer to vary the input threshold voltage levels. A resistor can be connected between this node and an external power supply. Figures 2, 4 and 5 illustrate the input threshold voltage shift possible through this technique.

This response node can also be used for the filtering of high frequency, high energy noise pulses. Figures 8 and 9 show typical noise pulse rejection for external capacitors of various sizes.

These two operations on the response node can be combined or used individually for many combinations of interfacing applications. The MC1489 circuits are particularly useful for interfacing between MOS circuits and MDTL/MTTL logic systems. In this application, the input threshold voltages are adjusted (with the appropriate supply and resistor values) to fall in the center of the MOS voltage logic levels (see Figure 10).

The response node may also be used as the receiver input as long as the designer realizes that he may not drive this node with a low impedance source to a voltage greater than one diode above ground or less than one diode below ground. This feature is demonstrated in Figure 11 where two receivers are slaved to the same line that must still meet the EIA–232D impedance requirement.

Figure 8. Typical Turn On Threshold versus Capacitance from Response Control Pin to GND

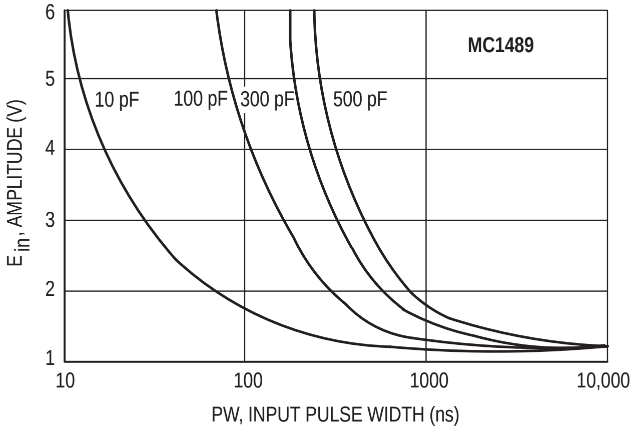


Figure 9. Typical Turn On Threshold versus Capacitance from Response Control Pin to GND

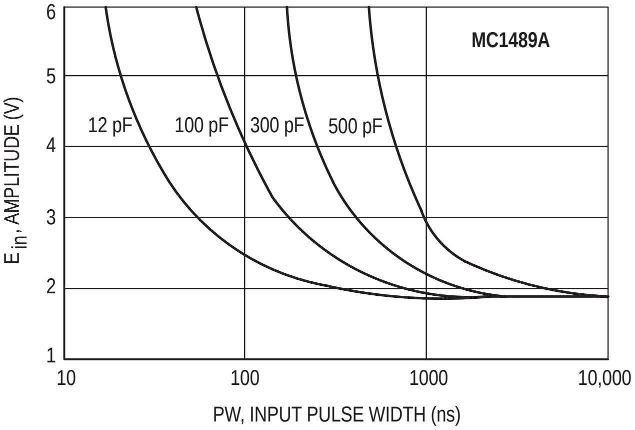


Figure 10. Typical Translator Application – MOS to DTL or TTL

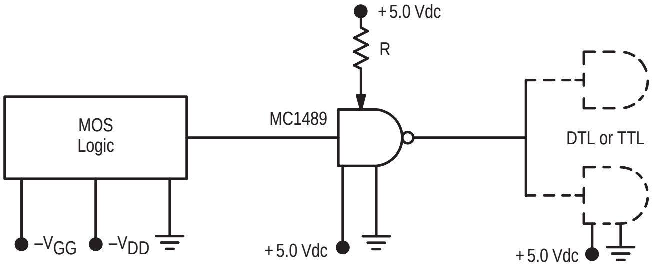
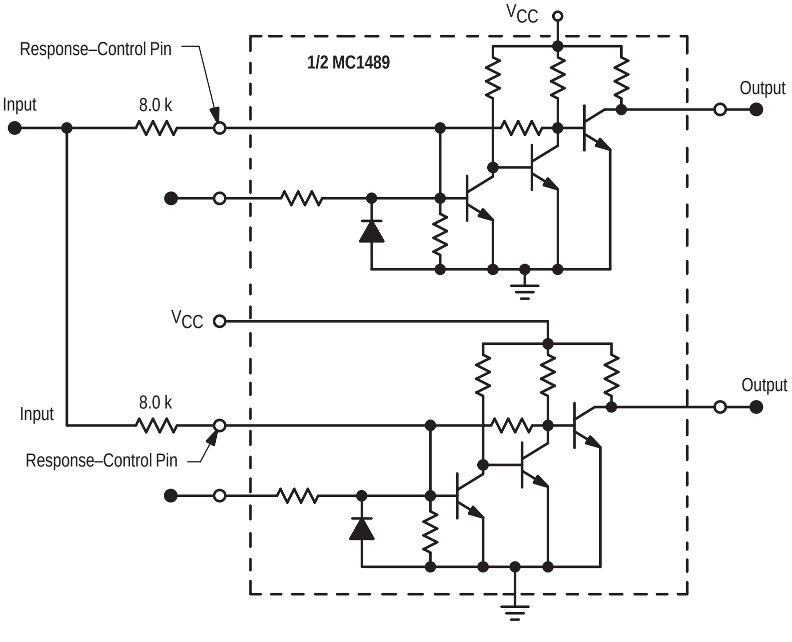


Figure 11. Typical Paralleling of Two MC1489, A Receivers to Meet EIA–232D



MOTOROLA

MC14C88B

Quad Low Power Line Driver

The MC14C88B is a low power monolithic quad line driver, using BiMOS technology, which conforms to EIA–232–D, EIA–562, and CCITT V.28. The inputs feature TTL and CMOS compatibility with minimal loading. The outputs feature internally controlled slew rate limiting, eliminating the need for external capacitors. Power off output impedance exceeds 300 Ω, and current limiting protects the outputs in the event of short circuits.

Power supply current is less than 160 μA over the supply voltage range of ±4.5 to ±15 V. EIA–232–D performance is guaranteed with a minimum supply voltage of ±6.5 V.

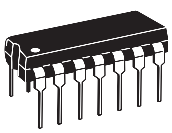
The MC14C88B is pin compatible with the MC1488, SN75188, SN75C188, DS1488, and DS14C88. This device is available in 14 pin plastic DIP, and surface mount packaging.

Features:

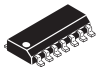
- BiMOS Technology for Low Power Operation (< 5.0 mW)
- Meets Requirements of EIA–232–D, EIA–562, and CCITT V.28
- Quiescent Current Less Than 160 μA
- TTL/CMOS Compatible Inputs
- Minimum 300 Ω Output Impedance when Powered Off
- Supply Voltage Range: ±4.5 to ±15 V
- Pin Equivalent to MC1488
- Current Limited Output: 10 mA Minimum
- Operating Ambient Temperature: –40° to 85°C

QUAD LOW POWER LINE DRIVER

SEMICONDUCTOR TECHNICAL DATA

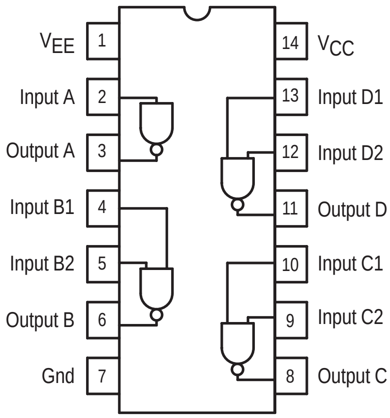


P SUFFIX
PLASTIC PACKAGE
CASE 646



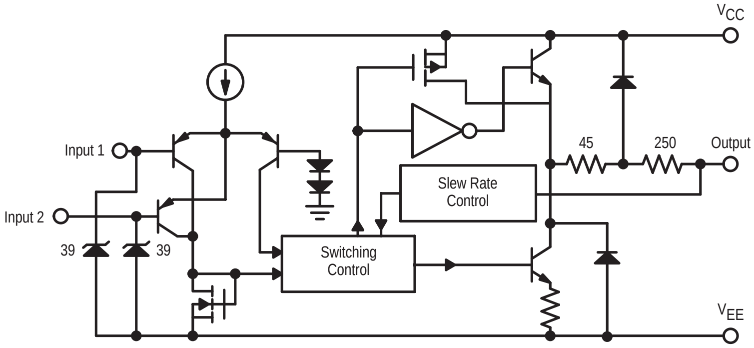
D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO–14)

PIN CONNECTIONS



(Top View)

Representative Block Diagram
(Each Driver)



ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC14C88BP	T_A = – 40° to +85°C	Plastic DIP
MC14C88BD		SO–14

MAXIMUM RATINGS (T_A = +25°C, unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage $V_{CC(max)}$ $V_{EE(min)}$ $(V_{CC} - V_{EE})_{max}$	 V_{CC} V_{EE} $V_{CC} - V_{EE}$	 +17 –17 34	Vdc
Input Voltage (All Inputs)	V_{in}	V_{EE}–0.3, V_{EE}+39	Vdc
Applied Output Voltage, when $V_{CC}=V_{EE} \neq 0$ V Applied Output Voltage, when $V_{CC}=V_{EE} = 0$ V	V_X	V_{EE}–6.0 V, V_{CC}+6.0 V ±15	Vdc
Output Current	I_O	Self Limiting	mA
Operating Junction Temperature	T_J	– 65, + 150	°C

Devices should not be operated at these limits. The “Recommended Operating Conditions” table provides for actual device operation.

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Min	Typ	Max	Unit
Power Supply Voltage	V_{CC} V_{EE}	+4.5 –15	– –	+15 –4.5	Vdc
Input Voltage (All Inputs)	V_{in}	0	–	V_{CC}	Vdc
Applied Output Voltage ($V_{CC}=V_{EE}=0$ V)	V_O	–2.0	0	+2.0	Vdc
Output DC Load	R_L	3.0	–	7.0	kΩ
Operating Ambient Temperature Range	T_A	–40	–	+85	°C

All limits are not necessarily functional concurrently.

ELECTRICAL CHARACTERISTICS (–40°C $\leq T_A \leq$ +85°C, unless otherwise noted.)*

Characteristic	Symbol	Min	Typ	Max	Unit
Supply Current (I_{out} = 0, see Figure 2)					μA
I_{CC} @ 4.75 V $\leq V_{CC}, -V_{EE} \leq$ 15 V					
Outputs High	$I_{CC\ (OH)}$	–	–	160	
Outputs Low	$I_{CC\ (OL)}$	–	–	160	
I_{EE}					
Outputs High	$I_{EE\ (OH)}$	–160	–	–	
Outputs Low	$I_{EE\ (OL)}$	–160	–	–	
Output Voltage – High, $V_{in} \leq 0.8$ V (R_L = 3.0 kΩ , see Figure 3)	V_{OH}				Vdc
V_{CC} = +4.75 V, V_{EE} = –4.75 V		3.7	3.8	–	
V_{CC} = +5.0 V, V_{EE} = –5.0 V		4.0	4.3	–	
V_{CC} = +6.5 V, V_{EE} = –6.5 V		5.0	6.1	–	
V_{CC} = +12 V, V_{EE} = –12 V		10	10.5	–	
V_{CC} = +13.2 V, V_{EE} = –13.2 V ($R_L = \infty$)		–	13.2	13.2	
Output Voltage – Low, $V_{in} \geq 2.0$ V	V_{OL}				
V_{CC} = +4.75 V, V_{EE} = –4.75 V		–	–3.8	–3.7	
V_{CC} = +5.0 V, V_{EE} = –5.0 V		–	–4.2	–4.0	
V_{CC} = +6.5 V, V_{EE} = –6.5 V		–	–6.0	–5.0	
V_{CC} = +12 V, V_{EE} = –12 V		–	–10.5	–10	
V_{CC} = +13.2 V, V_{EE} = –13.2 V ($R_L = \infty$)		–13.2	–13.2	–	
Output Short Circuit Current** (see Figure 4) ($V_{CC} = \lvert V_{EE} \rvert$ = 15 V)	I_{OS}				mA
Normally High Output, shorted to ground		–35	–	–10	
Normally Low Output, shorted to ground		+10	–	+35	
Output Source Resistance ($V_{CC} = V_{EE}$ = 0 V, –2.0 V $\leq V_{out} \leq$ +2.0 V)	R_O	300	–	–	Ω
Input Voltage					
Low Level	V_{IL}	0	–	0.8	Vdc
High Level	V_{IH}	2.0	–	V_{CC}	

* Typicals reflect performance @ T_A = 25°C

** Only one output shorted at a time, for not more than 1 second.

ELECTRICAL CHARACTERISTICS (continued) ($-40°C \leqslant T_A \leqslant +85°C$, unless otherwise noted.)*

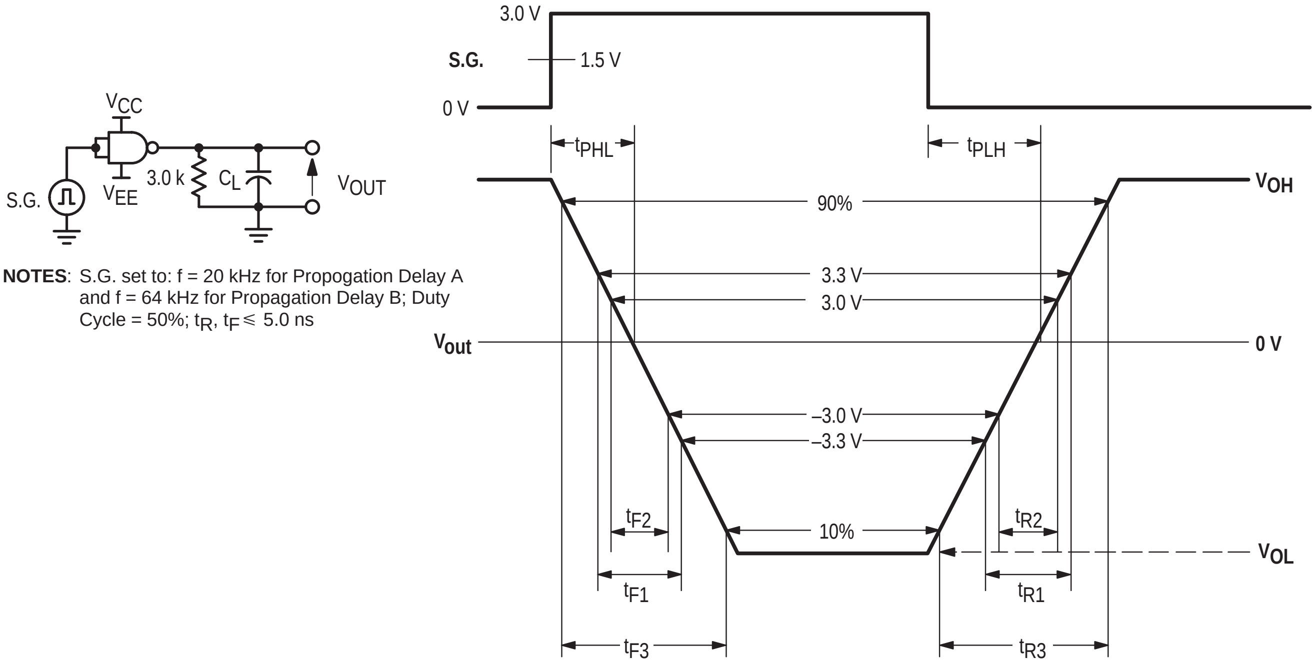
Characteristic	Symbol	Min	Typ	Max	Unit
Input Current	I_{in}				µA
V_{in} = 0 V, $V_{CC} = \lvert V_{EE} \rvert$ = 4.75 V		–10	–0.1	0	
V_{in} = 0 V, $V_{CC} = \lvert V_{EE} \rvert$ = 15 V		–10	–0.1	0	
V_{in} = 4.5 V, $V_{CC} = \lvert V_{EE} \rvert$ = 4.75 V		0	+0.1	+10	
V_{in} = 4.5 V, $V_{CC} = \lvert V_{EE} \rvert$ = 15 V		0	+0.1	+10	

TIMING CHARACTERISTICS ($-40°C \leqslant T_A \leqslant +85°C$, unless otherwise noted.)*

Characteristic	Symbol	Min	Typ	Max	Unit
Output Rise Time					µs
V_{CC} = 4.75 V, V_{EE} = –4.75 V					
$-3.3\ V \leqslant V_O \leqslant 3.3\ V$	t_{R1}				
C_L = 15 pF		0.22	0.66	2.1	
C_L = 1000 pF		0.22	1.52	2.1	
$-3.0\ V \leqslant V_O \leqslant 3.0\ V$	t_{R2}				
C_L = 15 pF		0.20	0.51	1.5	
C_L = 1000 pF		0.20	1.16	1.5	
V_{CC} = 12.0 V, V_{EE} = –12.0 V					
$-3.0\ V \leqslant V_O \leqslant 3.0\ V$					
C_L = 15 pF		0.20	0.62	1.5	
C_L = 2500 pF		0.20	0.82	1.5	
$10\% \leqslant V_O \leqslant 90\%$	t_{R3}				
C_L = 15 pF		0.53	1.41	3.2	
Output Fall Time					µs
V_{CC} = 4.75 V, V_{EE} = –4.75 V					
$3.3\ V \leqslant V_O \leqslant -3.3\ V$	t_{F1}				
C_L = 15 pF		0.22	0.93	2.1	
C_L = 1000 pF		0.22	1.28	2.1	
$3.0\ V \leqslant V_O \leqslant -3.0\ V$	t_{F2}				
C_L = 15 pF		0.20	0.72	1.5	
C_L = 1000 pF		0.20	1.01	1.5	
V_{CC} = 12.0 V, V_{EE} = –12.0 V					
$3.0\ V \leqslant V_O \leqslant -3.0\ V$					
C_L = 15 pF		0.20	0.70	1.5	
C_L = 2500 pF		0.20	0.94	1.5	
$90\% \leqslant V_O \leqslant 10\%$	t_{F3}				
C_L = 15 pF		0.53	1.71	3.2	
Output Slew Rate, 3.0 kΩ $< R_L <$ 7.0 kΩ , 15 pF $< C_L <$ 2500 pF	S_R	4.0	–	30	V/µs
Propagation Delay A (C_L = 15 pF, see Figure 1)					µs
V_{CC} = 12.0 V, V_{EE} = –12.0 V					
Input to Output – Low to High	t_{PLH}	–	0.9	3.0	
Input to Output – High to Low	t_{PHL}	–	2.3	3.5	
Propagation Delay B (C_L = 15 pF, see Figure 1)					
V_{CC} = 4.75 V, V_{EE} = –4.75 V					
Input to Output – Low to High	t_{PLH}	–	0.4	2.0	
Input to Output – High to Low	t_{PHL}	–	1.5	2.5	

* Typicals reflect performance @ $T_A = 25^{\circ}C$

Figure 1. Timing Diagram



NOTES: S.G. set to: f = 20 kHz for Propogation Delay A and f = 64 kHz for Propagation Delay B; Duty Cycle = 50%; t_R, $t_F \leqslant$ 5.0 ns

STANDARDS COMPLIANCE

The MC14C88 is designed to comply with EIA–232–D (formerly RS–232), the newer EIA–562 (which is a higher speed version of the EIA–232), and CCITT's V.28. EIA–562 was written around modern integrated circuit technology, whereas EIA–232 retains many of the specs written around the electro–mechanical circuitry in use at the time of its creation. Yet the user will find enough similarities to allow a certain amount of compatibility among equipment built to the two standards. Following is a summary of the key specifications relating to the systems and the drivers.

Parameter	EIA–232–D	EIA–562
Maximum Data Rate	20 kbaud	38.4 kbaud Asynchronous 64 kbaud Synchronous
Maximum Cable Length	50 feet	Based on cable capacitance/data rate
Maximum Slew Rate	⩽ 30 V/µs anywhere on the waveform	⩽ 30 V/µs anywhere on the waveform ⩾ 4.0 V/µs between +3.0 and –3.0 V
Transition Region	–3.0 to +3.0 V	–3.3 to +3.3 V
Transition Time	For UI ⩾ 25 ms, t_R ⩽1.0 ms For 25 ms > UI > 125 µs, t_R ⩽ 4% UI For UI < 125 µs, t_R ⩽ 5.0 µs	For UI ⩾ 50 µs, 220 ns < t_R ⩽ 3.1 µs For UI < 50 µs, 220 ns < t_R ⩽ 2.1 µs (within the transition region)
MARK (one, off)	More negative than –3.0 V	More negative than –3.3 V
Space (zero, on)	More positive than +3.0 V	More positive than +3.3 V
Short Circuit Proof ?	Yes, to any system voltage	Yes, to ground
Short Circuit Current	⩽ 500 mA to any system voltage	⩽ 60 mA to ground
Open Circuit Voltage	$\lvert V_{OC} \rvert$ ⩽ 25 V	$\lvert V_{OC} \rvert$ < 13.2 V
Loaded Output Voltage	5.0 V ⩽ $\lvert V_O \rvert$ ⩽15 V for loads between 3.0 kΩ and 7.0 kΩ	$\lvert V_O \rvert$ ⩾ 3.7 V for a load of 3.0 kΩ
Power Off Input Source Impedance	⩾ 300 Ω for $\lvert V_O \rvert$ ⩽ 2.0 V	⩾ 300 Ω for $\lvert V_O \rvert$ ⩽ 2.0 V

NOTE: UI = Unit Interval, or bit time.
V.28 standard has the same specifications as EIA–232, with the exception of transition time which is listed as "less than 1.0 ms, or 3% of the UI, whichever is less".

Figure 2. Typical Supply Current versus Supply Voltage

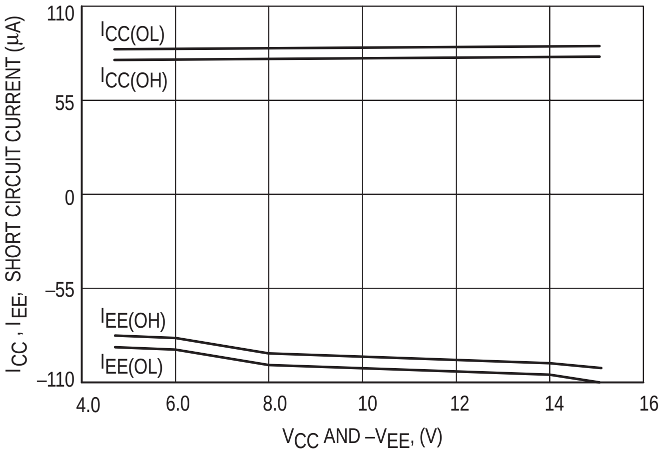


Figure 3. Typical Output Voltage versus Supply Voltage

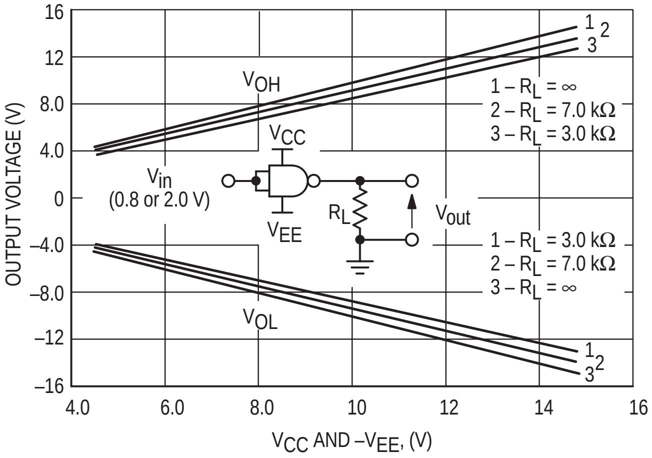


Figure 4. Typical Short Circuit Current versus Supply Voltage

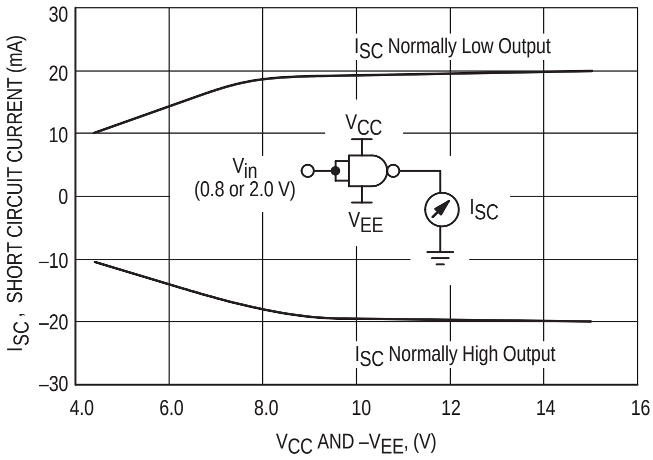
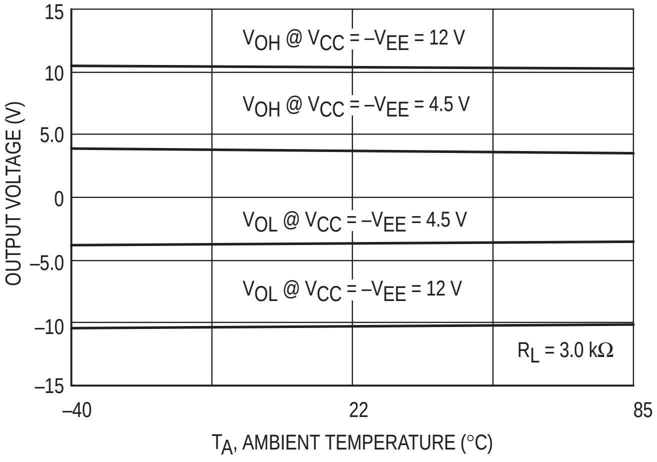


Figure 5. Typical Output Voltage versus Temperature



APPLICATIONS INFORMATION

Description

The MC14C88 was designed to be a direct replacement for the MC1488 in that it meets all EIA–232 specifications. However, use is extended as the MC14C88 also meets the faster EIA–562 and CCITT V.28 specifications. Slew rate limited outputs conform to the mentioned specifications and eliminate the need for external output capacitors. Low power consumption is made possible by BiMOS technology. Power supply current is limited to less than 160 μA, plus load currents over the supply voltage range of ±4.5 V to ±15 V (see Figure 2).

Outputs

The output low or high voltage depends on the state of the inputs, the load current, and the supply voltage (see Table 1 and Figure 3). The graphs apply to each driver regardless of how many other drivers within the package are supplying load current.

Table 1. Function Tables

Driver 1

Input A	Output A
H	L
L	H

Drivers 2 through 4

Input *1	Input *2	Output*
H	H	L
L	X	H
X	L	H

H = High level, L = Low level, X = Don't care.

Driver Inputs

The driver inputs determine the state of the outputs in accordance with Table 1. The nominal threshold voltage for the inputs is 1.4 Vdc, and for proper operation, the input voltages should be restricted to the range Gnd to V_{CC}. Should the input voltage drop below V_{EE} by more than 0.3 V or rise above V_{EE} by more than 39 V, excessive currents will flow at the input pin. Open input pins are equivalent to logic high, but good design practices dictate that inputs should never be left open.

Operating Temperature Range

The ambient operating temperature range is listed at –40° to +85°C and meets EIA–232–D, EIA–562 and CCITT V.28 specifications over this temperature range. The maximum ambient temperature is listed as +85°C. However, a lower ambient may be required depending on system use, i.e. specifically how many drivers within a package are used, and at what current levels they are operating. The maximum power which may be dissipated within the package is determined by:

$$P_{Dmax} = \frac{T_{Jmax} - T_A}{R_{\theta JA}}$$

where: $R_{\theta JA}$ = the package thermal resistance (typically, 100°C/W for the DIP package, 125°C/W for the SOIC package);
T_{Jmax} = the maximum operating junction temperature (150°C); and
T_A = the ambient temperature.

$$P_D = \{ [(V_{CC} - V_{OH}) \times |I_{OH}|] \text{ or } [(V_{OL} - V_{EE}) \times |I_{OL}|] \}_{\text{each driver}} + (V_{CC} \times I_{CC}) + (V_{EE} \times I_{EE})$$

where: V_{CC} and V_{EE} are the positive and negative supply voltages;
V_{OH} and V_{OL} are measured or estimated from Figure 3;
I_{CC} and I_{EE} are the quiescent supply currents measured or estimated from Figure 2.

As indicated, the first term (in brackets) must be calculated and summed for each of the four drivers, while the last terms are common to the entire package.

MC14C89B, AB

Quad Low Power Line Receivers

The MC14C89B and MC14C89AB are low monolithic quad line receivers using bipolar technology, which conform to the EIA–232–E, EIA–562 and CCITT V.28 Recommendations. The outputs feature LSTTL and CMOS compatibility for easy interface to +5.0 V digital systems. Internal time–domain filtering eliminates the need for external filter capacitors in most cases.

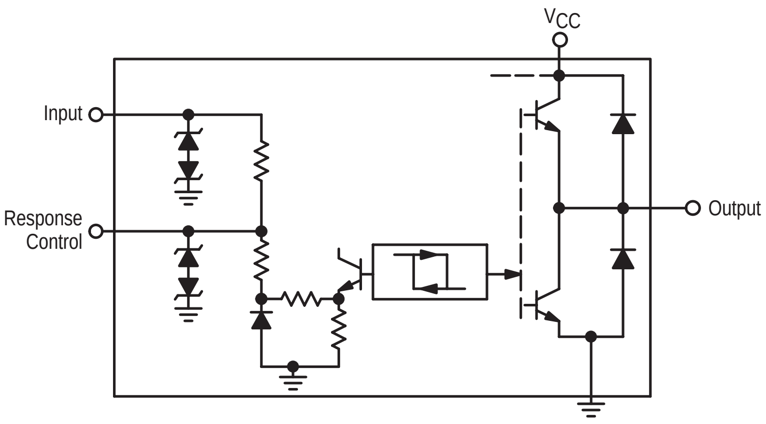
The MC14C89B has an input hysteresis of 0.35 V, while the MC14C89AB hysteresis is 0.95 V. The response control pins allow adjustment of the threshold level if desired. Additionally, an external capacitor may be added for additional noise filtering.

The MC14C89B and MC14C89AB are available in both a 14 pin dual–in–line plastic DIP and SOIC package.

Features:

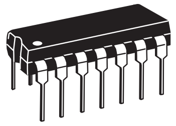
- Low Power Consumption
- Meets EIA–232–E, EIA–562, and CCITT V.28 Recommendations
- TTL/CMOS Compatible Outputs
- Standard Power Supply: + 5.0 V ±10%
- Pin Equivalent to MC1489, MC1489A, TI’s SN75C189/A, SN75189/A and National Semiconductor’s DS14C89/A
- External Filtering Not Required in Most Cases
- Threshold Level Externally Adjustable
- Hysteresis: 0.35 V for MC14C89B, 0.95 V for MC14C89AB
- Available in Plastic DIP, and Surface Mount Packaging
- Operating Ambient Temperature: –40° to +85°C

Representative Block Diagram (Each Receiver)

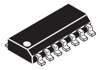


QUAD LOW POWER LINE RECEIVERS

SEMICONDUCTOR TECHNICAL DATA

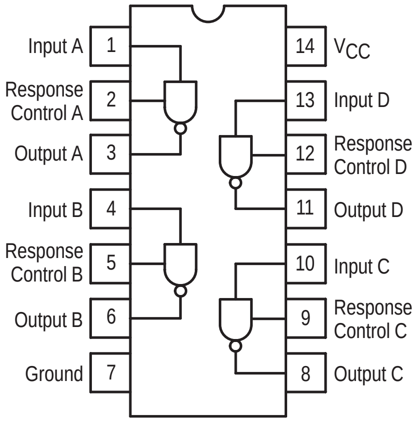


P SUFFIX
PLASTIC PACKAGE
CASE 646



D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO–14)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC14C89BP	T_A = – 40° to +85°C	Plastic DIP
MC14C89ABP		Plastic DIP
MC14C89ABD		SO–14

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage $V_{CC(max)}$ $V_{CC(min)}$	V_{CC}	 + 7.0 – 0.5	Vdc
Input Voltage	V_{in}	± 30	Vdc
Output Load Current	I_O	Self–Limiting	–
Junction Temperature	T_J	–65, +150	°C

Devices should not be operated at these limits. The “Recommended Operating Conditions” table provides for actual device operation.

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Min	Typ	Max	Unit
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	Vdc
Input Voltage	V_{in}	–25	–	25	Vdc
Output Current Capability	I_O	–7.5	–	6.0	mA
Operating Ambient Temperature	T_A	–40	–	85	°C

All limits are not necessarily functional concurrently.

ELECTRICAL CHARACTERISTICS (–40°C $\leq T_A \leq$ +85°C, unless otherwise noted.)*

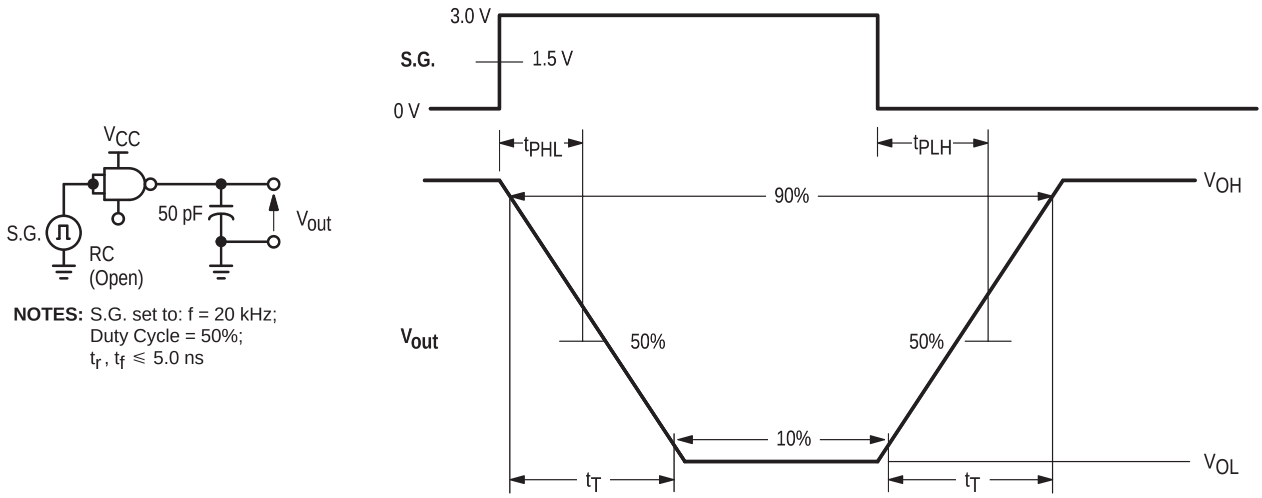
Characteristic	Symbol	Min	Typ	Max	Unit
Supply Current ($I_{out} = 0$) I_{CC} @ +4.5 V $\leq V_{CC} \leq$ +5.5 V	I_{CC}	 –	 330	 700	µA
Output Voltage – High, $V_{in} \leq$ 0.4 V (See Figures 2 and 3)	V_{OH}				Vdc
I_{out} = –20 µA V_{CC} = 4.5 V		3.5	3.8	–	
V_{CC} = 5.5 V		3.5	4.8	–	
I_{out} = –3.2 mA V_{CC} = 4.5 V		2.5	3.7	–	
V_{CC} = 5.5 V		2.5	4.7	–	
Output Voltage – Low, $V_{in} \geq$ 2.4 V	V_{OL}				
I_{out} = 3.2 mA V_{CC} = 4.5 V		–	0.1	0.4	
V_{CC} = 5.5 V		–	0.1	0.4	
Output Short Circuit Current** (V_{CC} = 5.5 V, see Figure 4)	I_{OS}				mA
Normally High Output shorted to ground		–35	–13.9	–	
Normally Low Output shorted to V_{CC}		–	+10.3	35	
Input Threshold Voltage (V_{CC} = 5.0 V)					
(MC14C89AB, see Figure 5) Low Level	V_{IL}	0.75	0.95	1.25	Vdc
High Level	V_{IH}	1.6	1.90	2.25	
(MC14C89B, see Figure 6)	V_{IL}	0.75	0.95	1.25	
Low Level	V_{IH}	1.0	1.3	1.5	
High Level					
Input Impedance (+4.5 V $< V_{CC} <$ +5.5 V –25 V $< V_{in} <$ +25 V)		3.0	5.5	7.0	kΩ

* Typicals reflect performance @ T_A = 25°C
**Only one output shorted at a time, for not more than 1.0 seconds.

TIMING CHARACTERISTICS (T_A = +25°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Transition Time (10% to 90%) 4.5 V $\leq V_{CC} \leq$ 5.5 V	t_T	 –	 0.08	 0.30	 µs
Propagation Delay Time 4.5 V $\leq V_{CC} \leq$ 5.5 V					
Output Low–to–High	t_{PLH}	–	3.35	6.0	µs
Output High–to–Low	t_{PHL}	–	2.55	6.0	
Input Noise Rejection (see Figure 9)		1.0	1.5	–	µs

Figure 1. Timing Diagram



NOTES: S.G. set to: f = 20 kHz;
Duty Cycle = 50%;
t_r, $t_f \leqslant 5.0$ ns

STANDARDS COMPLIANCE

The MC14C89B and MC14C89AB are designed to comply with EIA–232–E (formerly RS–232), the newer EIA–562 (which is a higher speed version of the EIA–232), and CCITT V.28 Recommendations. EIA–562 was written around modern integrated circuit technology, whereas EIA–232 retains many of the specifications written around the electro–mechanical circuitry in use at the time of its creation. Yet the user will find enough similarities to allow a certain amount of compatibility among equipment built to the two standards. Following is a summary of the key specifications relating to the systems and the receivers.

Parameter	EIA–232–E	EIA–562
Max Data Rate	20 kBaud	38.4 kBaud Asynchronous 64 kBaud Synchronous
Max Cable Length	50 feet	Based on cable capacitance/data rate
Transition Region	–3.0 V to +3.0 V	–3.0 V to +3.0 V
MARK (one, off)	More negative than –3.0 V	More negative than –3.3 V
SPACE (zero, on)	More positive than +3.0 V	More positive than +3.3 V
Fail Safe	Output = Binary 1	Output = Binary 1
Open Circuit Input Voltage	$< \lvert 2.0 \rvert$ V	Not Specified
Slew Rate (at the driver)	$\leqslant$30 V/µs anywhere on the waveform	$\leqslant$30 V/µs anywhere on the waveform, $\geqslant$4.0 V/µs between +3.0 V and –3.0 V
Loaded Output Voltage (at the driver)	5.0 V $\leqslant \lvert V_O \rvert \leqslant$ 15 V for loads between 3.0 kΩ and 7.0 kΩ	$\lvert V_O \rvert \geqslant$ 3.7 V for a load of 3.0 kΩ

Figure 2. Typical Output versus Supply Voltage

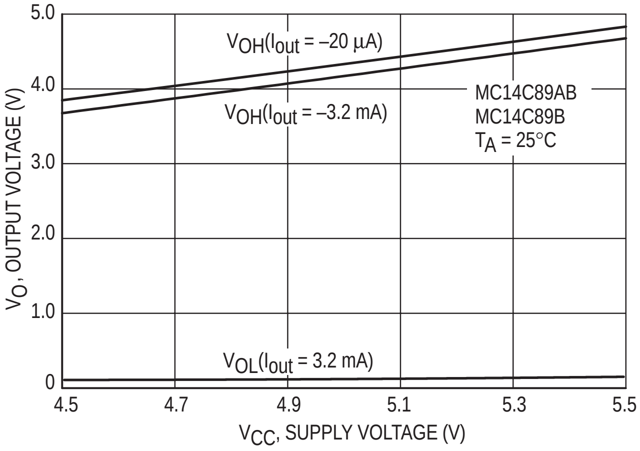


Figure 3. Typical Output Voltage versus Temperature

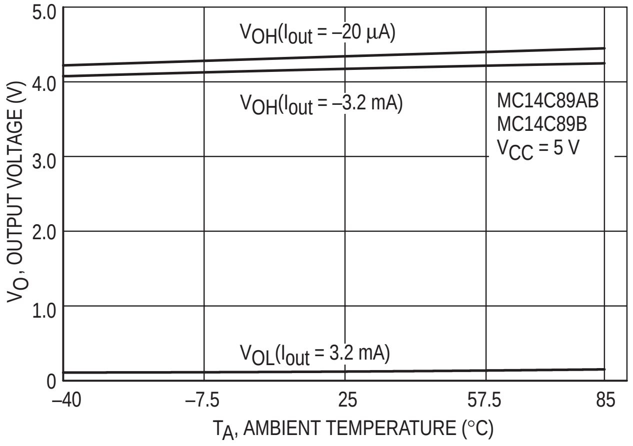


Figure 4. Typical Short Circuit Current versus Temperature

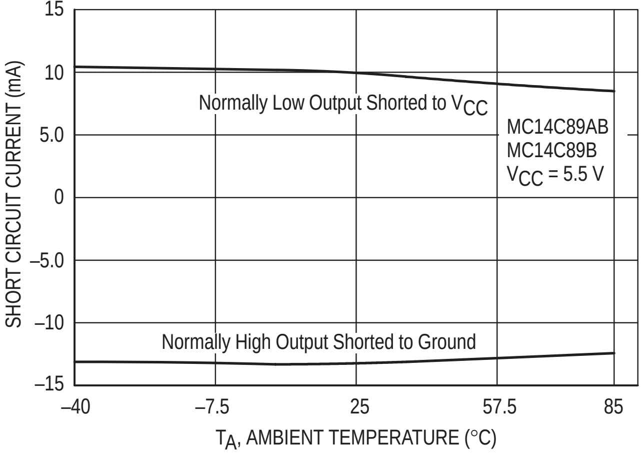


Figure 5. Typical Threshold Voltage versus Temperature

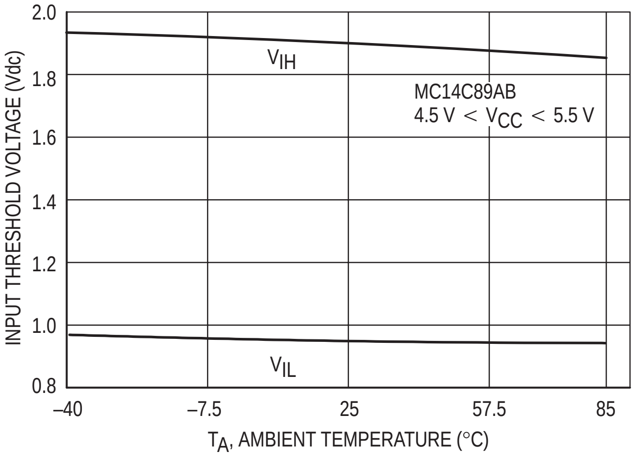


Figure 6. Typical Threshold Voltage versus Temperature

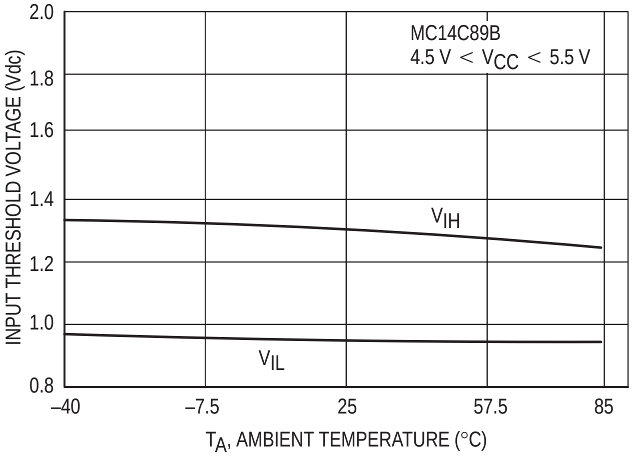


Figure 7. Typical Effect of Response Control Pin Bias

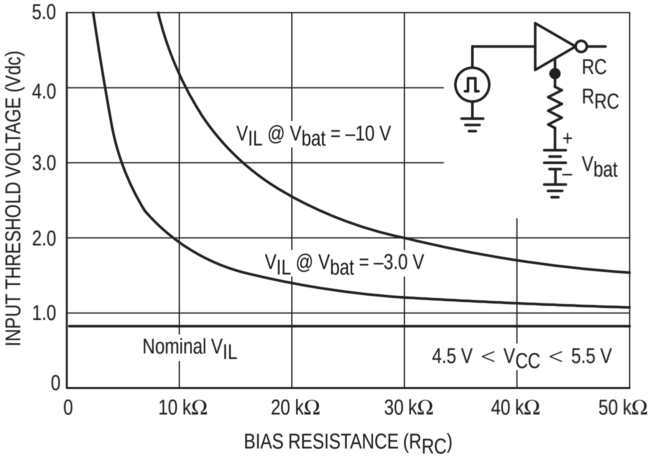
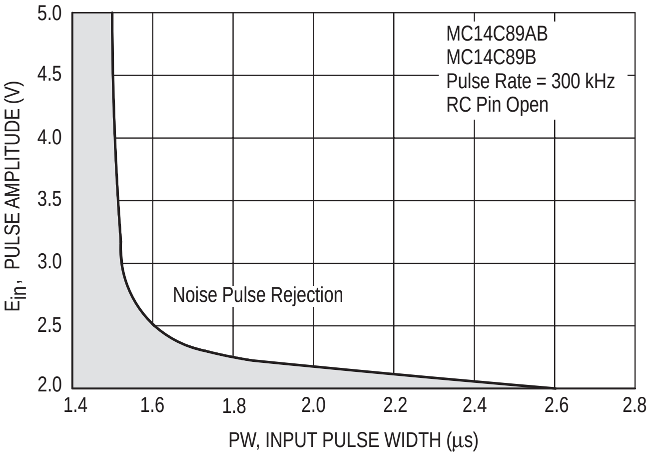


Figure 8. Typical Noise Pulse Rejection



APPLICATIONS INFORMATION

Description

The MC14C89AB and MC14C89B are designed to be direct replacements for the MC1489A and MC1489. Both devices meet all EIA–232 specifications and also the faster EIA–562 and CCITT V.28 specifications. Noise pulse rejection circuitry eliminates the need for most response control filter capacitors but does not exclude the possibility as filtering is still possible at the Response Control (RC) pins. Also, the Response Control pins allow for a user defined selection of the threshold voltages. The MC14C89AB and MC14C89B are manufactured with a bipolar technology using low power techniques and consume at most 700 µA, plus load currents with a +5.0 V supply.

Outputs

The output low or high voltage depends on the state of the inputs, the load current, the bias of the Response Control pins, and the supply voltage. Table 1 applies to each receiver, regardless of how many other receivers within the package are supplying load current.

Table 1. Function Table

Receivers

Input*	Output*
H	L
L	H

*The asterisk denotes A, B, C, or D.

Receiver Inputs and Response Control

The receiver inputs determine the state of the outputs in accordance with Table 1. The nominal V_{IL} and V_{IH} thresholds are 0.95 V and 1.90 V respectively for the MC14C89AB. For the MC14C89B, the nominal V_{IL} and V_{IH} thresholds are 0.95 and 1.30, respectively. The inputs are able to withstand ±30 V referenced to ground. Should the input voltage exceed ground by more than ±30 V, excessive currents will flow at the input pin. Open input pins will generate a logic high output, but good design practices dictate that inputs should never be left open.

The Response Control (RC) pins are coupled to the inputs through a resistor string. The RC pins provide for adjustment of the threshold voltages of the IC while preserving the amount of hysteresis. Figure 10 shows a typical application to adjust the threshold voltages. The RC pins also provide access to an internal resistor string which permits low pass filtering of the input signal within the IC. Like the input pins, the RC pins should not be taken above or below ground by more than ±30 V or excessive currents will flow at these pins. The dependence of the low level threshold voltage (V_{IL}) upon R_{RC} and V_{bat} can be described by the following equation:

$$V_{IL} \simeq \left\{ V_{0.09} - V_{bat}\left[\frac{505\ \Omega}{R_{RC}\ (1.6)\ +\ 2.02\ k\Omega}\right]\right\}\left(\frac{5.32\ k\Omega + \dfrac{6.67 \times 10^{6}\ \Omega^{2}}{R_{RC}}}{505\ \Omega}\right) \qquad (1)$$

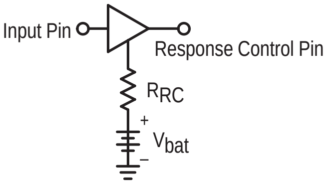
V_{IH} can be found by calculating for V_{IL} using equation (1) then adding the hysteresis for each device (0.35 for the MC14C89B or 0.95 V for the MC14C89AB). Figure 7 plots equation (1) for two values of V_{bat} and a range of R_{RC}.

If an RC pin is to be used for low pass filtering, the capacitor chosen can be calculated by the equation,

$$C_{RC} \simeq \frac{1}{2.02\ k\Omega\ 2\pi\ f_{-3dB}} \qquad (2)$$

where $f_{-3\,dB}$ represents the desired –3 dB role–off frequency of the low pass filter.

Figure 9. Application to Adjust Thresholds



Another feature of the MC14C89AB and MC14C89B is input noise rejection. The inputs have the ability to ignore pulses which exceed the V_{IH} and V_{IL} thresholds but are less than 1.0 µs in duration. As the duration of the pulse exceeds 1.0 µs, the noise pulse may still be ignored depending on its amplitude. Figure 8 is a graph showing typical input noise rejection as a function of pulse amplitude and pulse duration. Figure 8 reflects data taken for an input with an unconnected RC pin and applied to the MC14C89AB and MC14C89B.

Operating Temperature Range

The ambient operating temperature range is listed as –40°C to +85°C, and the devices are designed to meet the EIA–232–E, EIA–562 and CCITT V.28 specifications over this temperature range. The timing characteristics are guaranteed to meet the specifications at +25°C. The maximum ambient operating temperature is listed as +85°C. However, a lower ambient may be required depending on system use (i.e., specifically how many receivers within a package are used), and at what current levels they are operating. The maximum power which may be dissipated within the package is determined by:

$$P_{D(max)} = \frac{T_{J(max)} - T_{A}}{R_{\theta JA}}$$

where: $R_{\theta JA}$ = thermal resistance (typ., 100°C/W for the DIP and 125°C/W for the SOIC packages);
$T_{J(max)}$ = maximum operating junction temperature (150°C); and
T_{A} = ambient temperature.
$P_{D} = \{[(V_{CC} - V_{OH}) \times |I_{OH}|]$ or $[(V_{OL}) \times |I_{OL}|]\}_{\text{each receiver}} + (V_{CC} \times I_{CC})$

where: V_{CC} = positive supply voltage;
V_{OH}, V_{OL} = measured or estimated from Figure 2 and 3;
I_{CC} = measured quiescent supply current.

As indicated, the first term (in brackets) must be calculated and summed for each of the four receivers, while the last term is common to the entire package.

MOTOROLA

Quad Open-Collector Bus Transceiver

This quad transceiver is designed to mate Schottky TTL or NMOS logic to a low impedance bus. The Enable and Driver inputs are PNP buffered to ensure low input loading. The Driver (Bus) output is open–collector and can sink up to 100 mA at 0.8 V, thus the bus can drive impedances as low as 100 Ω. The receiver output is active pull–up and can drive ten Schottky TTL loads.

An active–low $\overline{\text{Enable}}$ controls all four drivers allowing the outputs of different device drivers to be connected together for party–line operation. The line can be terminated at both ends and still give considerable noise margin at the receiver. Typical receiver threshold is 2.0 V.

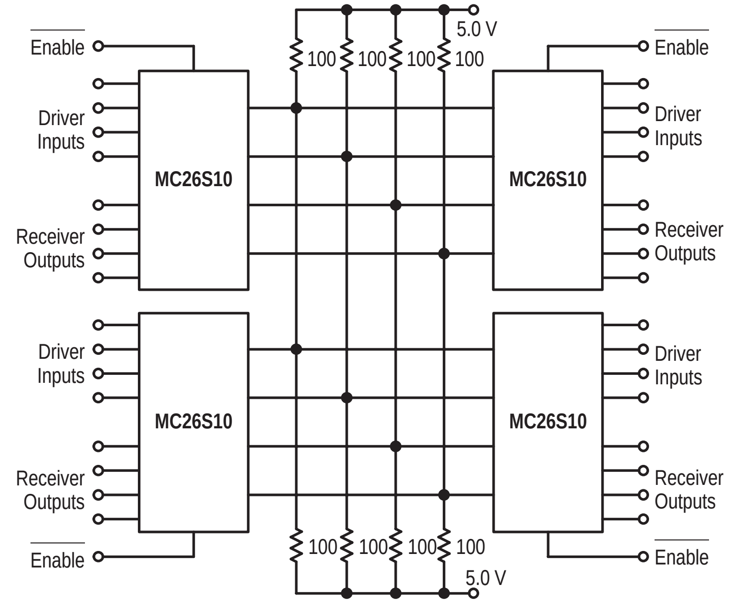
Advanced Schottky processing is utilized to assure fast propagation delay times. Two ground pins are provided to improve ground current handling and allow close decoupling between V_{CC} and ground at the package. Both ground pins should be tied to the ground bus external to the package.

- Driver Can Sink 100 mA at 0.8 V (Maximum)
- PNP Inputs for Low–Logic Loading
- Typical Driver Delay = 10 ns
- Typical Receiver Delay = 10 ns
- Schottky Processing for High Speed
- Inverting Driver

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC26S10P	T_A = 0 to +70°C	Plastic DIP
MC26S10D		SO–16

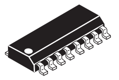
Simplified Application



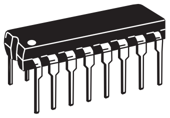
MC26S10

QUAD OPEN–COLLECTOR BUS TRANSCEIVER

SEMICONDUCTOR TECHNICAL DATA

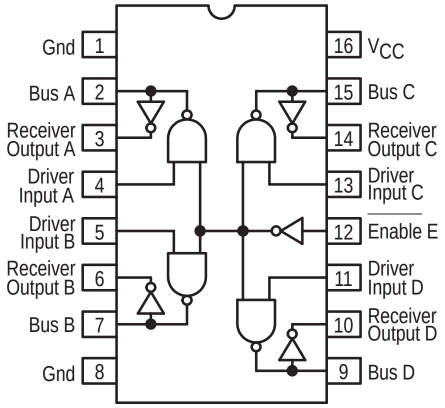


D SUFFIX
PLASTIC PACKAGE
CASE 751B
(SO–16)



P SUFFIX
PLASTIC PACKAGE
CASE 648

PIN CONNECTIONS



TRUTH TABLE

$\overline{\text{Enable}}$	Driver Input	Bus	Receiver Output
L	L	H	L
L	H	L	H
H	X	Y	Y

L = Low Logic State
H = High Logic State
X = Irrelevant
Y = Assumes condition controlled by other elements on the bus

MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	–0.5 to +7.0	Vdc
Input Voltage	V_I	–0.5 to +5.5	Vdc
Input Current	I_I	–3.0 to +5.0	mA
Output Voltage – High Impedance State	$V_{o\ (Hi–z)}$	–0.5 to V_{CC}	V
Output Current – Bus	$I_{o(B)}$	200	mA
Output Current – Receiver	$I_{o(R)}$	30	mA
Operating Ambient Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	–65 to +150	°C
Junction Temperature	T_J	150	°C

ELECTRICAL CHARACTERISTICS (Unless otherwise noted V_{CC} = 4.75 to 5.25 V and T_A = 0 to +70°C. Typical values measured at V_{CC} = 5.0 V and T_A = 25°C.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Voltage – Low Logic State (Driver and $\overline{\text{Enable}}$ Inputs)	V_{IL}	–	–	0.8	V
Input voltage – High Logic State (Driver and $\overline{\text{Enable}}$ Inputs)	V_{IH}	2.0	–	–	V
Input Clamp Voltage (Driver and Enable Inputs) (I_{IK} = –18 mA)	V_{IK}	–	–	–1.2	V
Input Current – Low Logic State (V_{IL} = 0.4 V) (Enable Input) (Driver Inputs)	I_{IL}	 – –	 – –	 –0.36 –0.54	mA
Input Current – High Logic State (V_{IH} = 2.7 V) (Enable Input) (Driver Inputs)	I_{IH}	 – –	 – –	 20 30	µA
Input Current – Maximum Voltage (V_{IH1} = 5.5 V) (Enable or Driver Inputs)	I_{IH1}	–	–	100	µA
Driver Output Voltage – Low Logic State (I_{OL} = 40 mA) (I_{OL} = 70 mA) (I_{OL} = 100 mA)	$V_{OL(D)}$	 – – –	 0.33 0.42 0.51	 0.5 0.7 0.8	V
Driver (Bus) Leakage Current (V_{OH} = 4.5 V) (V_{OL} = 0.8 V)	$I_{O(D)}$	 – –	 – –	 100 –50	µA
Driver (Bus) Leakage Current (V_{CC} = 0 V, V_{OH} = 4.5 V)	$I_{O1(D)}$	–	–	100	µA
Receiver Input High Threshold ($V_{IH(\overline{E})}$ = 2.4 V)	$V_{TH(R)}$	2.25	2.0	–	V
Receiver Input Low Threshold ($V_{IH(\overline{E})}$ = 2.4 V)	$V_{TL(R)}$	–	2.0	1.75	V
Receiver Output Voltage – Low Logic State (I_{OL} = 20 mA)	$V_{OL(R)}$	–	–	0.5	V
Receiver Output Voltage – High Logic State (I_{OH} = –1.0 mA)	$V_{OH(R)}$	2.7	3.4	–	V
Receiver Output Short–Circuit Current (Note1)	$I_{OS(R)}$	–18	–	–60	mA
Power Supply Current – Output Low State ($V_{IL(\overline{E})}$ = 0 V)	I_{CC}	–	45	70	mA

NOTE: 1. One output shorted at a time. Duration not to exceed 1.0 second.

SWITCHING CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Propagation Delay Time Driver Input to Output	$t_{PLH(D)}$ $t_{PHL(D)}$	– –	10 10	15 15	ns
Propagation Delay Time Enable Input to Output	$t_{PLH(\overline{E})}$ $t_{PHL(\overline{E})}$	– –	14 13	18 18	ns
Propagation Delay Time Bus to Receiver Output	$t_{PLH(R)}$ $t_{PHL(R)}$	– –	10 10	15 15	ns
Rise and Fall Time of Driver Output	$t_{TLH(D)}$ $t_{THL(D)}$	4.0 2.0	10 4.0	– –	ns

SWITCHING WAVEFORMS AND CIRCUITS

Figure 1. Data Input to Bus Output (Driver)

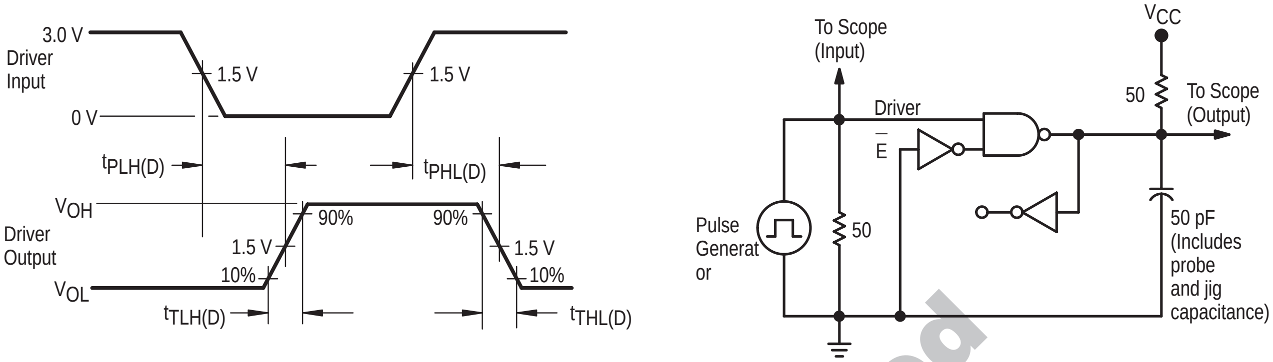


Figure 2. Enable Input to Bus Output (Driver)

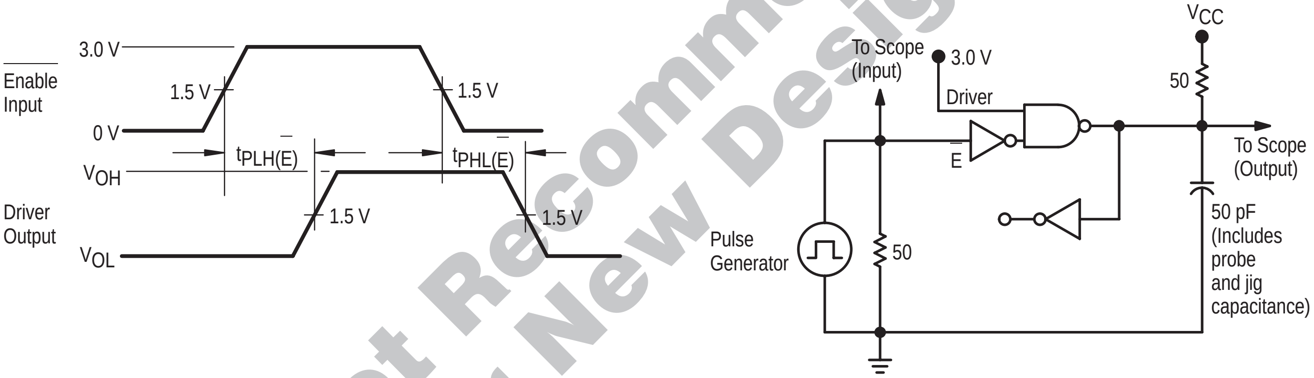
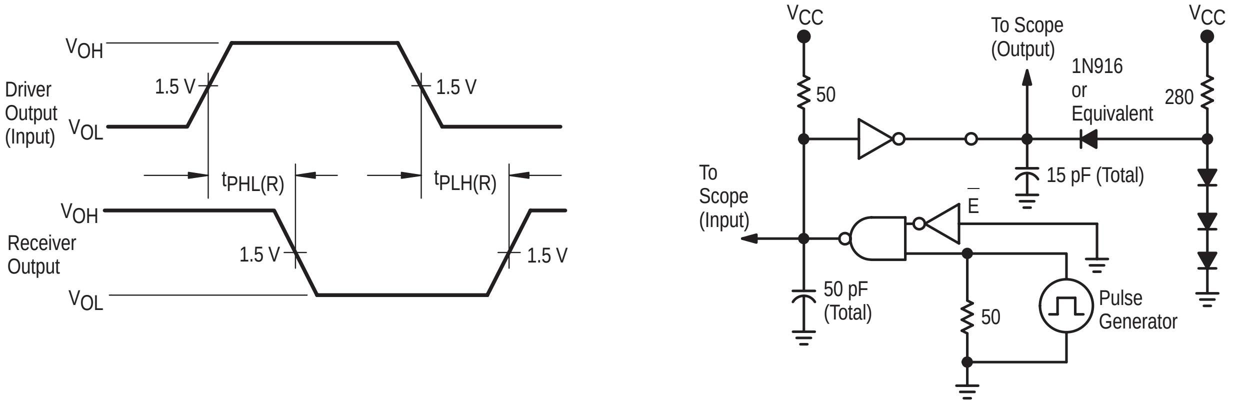


Figure 3. Bus Input to Receiver Output



MOTOROLA

MC3448A

Quad Bidirectional Instrumentation Bus (GPIB) Transceiver

This bidirectional bus transceiver is intended as the interface between TTL or MOS logic and the IEEE Standard Instrumentation Bus (488–1978, often referred to as GPIB). The required bus termination is internally provided.

Each driver/receiver pair forms the complete interface between the bus and an instrument. Either the driver or the receiver of each channel is enabled by its corresponding Send/Receive input with the disabled output of the pair forced to a high impedance state. An additional option allows the driver outputs to be operated in an open collector* or active pull–up configuration. The receivers have input hysteresis to improve noise margin, and their input loading follows the bus standard specifications.

- Four Independent Driver/Receiver Pairs
- Three–State Outputs
- High Impedance Inputs
- Receiver Hysteresis – 600 mV (Typical)
- Fast Propagation Times – 15 to 20 ns (Typical)
- TTL Compatible Receiver Outputs
- Single 5.0 V Supply
- Open Collector Driver Output Option*
- Power Up/Power Down Protection (No Invalid Information Transmitted to Bus)
- No Bus Loading When Power Is Removed From Device
- Terminations Provided: Termination Removed When Device is Unpowered

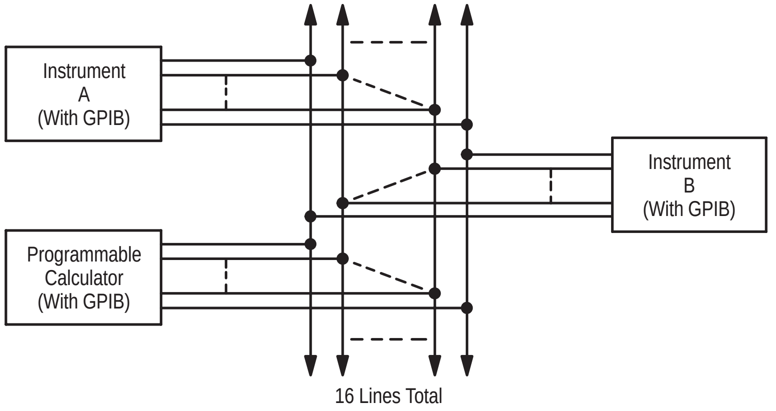
* Selection of the “Open Collector” configuration, in fact, selects an open collector device with a passive pull–up load/termination which conforms to Figure 7, IEEE 488–1978 Bus Standard.

TRUTH TABLE

Send/Rec.	Enable	Info. Flow	Comments
0	X	Bus → Data	–
1	1	Data → Bus	Active Pull–Up
1	0	Data → Bus	Open Col.

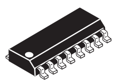
X = Don′t Care

Typical Measurement System Application

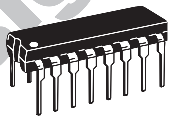


QUAD THREE–STATE BUS TRANSCEIVER WITH TERMINATION NETWORKS

SEMICONDUCTOR TECHNICAL DATA

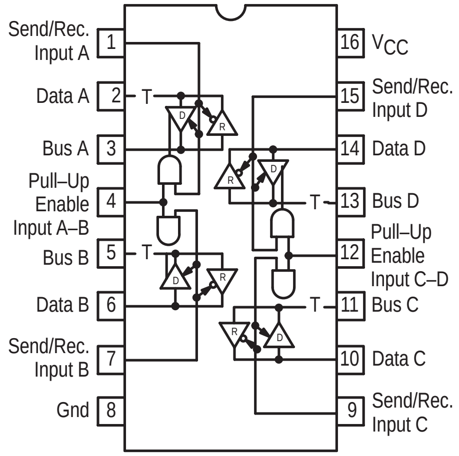


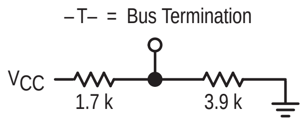
D SUFFIX
PLASTIC PACKAGE
CASE 751B
(SO–16)



P SUFFIX
PLASTIC PACKAGE
CASE 648

PIN CONNECTIONS





ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC3448AP	T_A = 0 to +70°C	Plastic DIP
MC3448AD		SO–16

MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	7.0	Vdc
Input Voltage	V_I	5.5	Vdc
Driver Output Current	$I_{O(D)}$	150	mA
Junction Temperature	T_J	150	°C
Operating Ambient Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	– 65 to +150	°C

ELECTRICAL CHARACTERISTICS (Unless otherwise noted, 4.75 V $\leqslant V_{CC} \leqslant$ 5.25 V and 0 $\leqslant T_A \leqslant$ 70°C; typical values are at T_A = 25°C, V_{CC} = 5.0 V)

Characteristic	Symbol	Min	Typ	Max	Unit
Bus Voltage (Bus Pin Open) ($V_{I(S/R)}$ = 0.8 V) ($I_{(BUS)}$ = –12 mA)	 $V_{(BUS)}$ $V_{IC(BUS)}$	 2.75 –	 – –	 3.7 – 1.5	V
Bus Current (5.0 V $\leqslant V_{(BUS)} \leqslant$ 5.5 V) ($V_{(BUS)}$ = 0.5 V) (V_{CC} = 0 V, 0 V $\leqslant V_{(BUS)} \leqslant$ 2.75 V)	$I_{(BUS)}$	 0.7 –1.3 –	 – – –	 2.5 – 3.2 +0.04	mA
Receiver Input Hysteresis ($V_{I(S/R)}$ = 0.8 V)	–	400	600	–	mV
Receiver Input Threshold ($V_{I(S/R)}$ = 0.8 V, Low to High) ($V_{I(S/R)}$ = 0.8 V, High to Low)	 $V_{ILH(R)}$ $V_{IHL(R)}$	 – 0.8	 1.6 1.0	 1.8 –	V
Receiver Output Voltage – High Logic State ($V_{I(S/R)}$ = 0.8 V, $I_{OH(R)}$ = –800 µA, $V_{(BUS)}$ = 2.0 V)	$V_{OH(R)}$	2.7	–	–	V
Receiver Output Voltage – Low Logic State ($V_{I(S/R)}$ = 0.8 V, $I_{OL(R)}$ = 16 mA, $V_{(BUS)}$ = 0.8 V)	$V_{OL(R)}$	–	–	0.5	V
Receiver Output Short Circuit Current ($V_{I(S/R)}$ = 0.8 V, $V_{(Bus)}$ = 2.0 V)	$I_{OS(R)}$	– 15	–	–75	mA
Driver Input Voltage – High Logic State ($V_{I(S/R)}$ = 2.0 V)	$V_{IH(D)}$	2.0	–	–	V
Driver Input Voltage – Low Logic State ($V_{I(S/R)}$ = 2.0 V)	$V_{IL(D)}$	–	–	0.8	V
Driver Input Current – Data Pins ($V_{I(S/R)} = V_{I(E)}$ = 2.0 V) (0.5 $\leqslant V_{I(D)} \leqslant$ 2.7 V) ($V_{I(D)}$ = 5.5 V)	 $I_{I(D)}$ $I_{IB(D)}$	 –200 –	 – –	 40 200	µA
Input Current – Send / Receive (0.5 $\leqslant V_{I(S/R)} \leqslant$ 2.7 V) ($V_{I(S/R)}$ = 5.5 V)	 $I_{I(S/R)}$ $I_{IB(S/R)}$	 –100 –	 – –	 20 100	µA
Input Current – Enable (0.5 $\leqslant V_{I(E)} \leqslant$ 2.7 V) ($V_{I(E)}$ = 5.5 V)	 $I_{I(E)}$ $I_{IB(E)}$	 –200 –	 – –	 20 100	µA
Driver Input Clamp Voltage ($V_{I(S/R)}$ = 2.0 V, $I_{IC(D)}$ = –18 mA)	$V_{IC(D)}$	–	–	–1.5	V
Driver Output Voltage – High Logic State ($V_{I(S/R)}$ = 2.0 V, $V_{IH(D)}$ = 2.0 V, $V_{IH(E)}$ = 2.0 V, I_{OH} = – 5.2 mA)	$V_{OH(D)}$	2.5	–	–	V
Driver Output Voltage – Low Logic State (Note 1) ($V_{I(S/R)}$ = 2.0 V, $I_{OL(D)}$ = 48 mA)	$V_{OL(D)}$	–	–	0.5	V
Output Short Circuit Current ($V_{I(S/R)}$ = 2.0 V, $V_{IH(D)}$ = 2.0 V, $V_{IH(E)}$ = 2.0 V)	$I_{OS(D)}$	–30	–	–120	mA
Power Supply Current (Listening Mode – All Receivers On) (Talking Mode – All Drivers On)	 I_{CCL} I_{CCH}	 – –	 63 106	 85 125	mA

SWITCHING CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C, unless otherwise noted)

Propagation Delay of Driver (Output Low to High) (Output High to Low)	 $t_{PLH(D)}$ $t_{PHL(D)}$	 – –	 – –	 15 17	ns
Propagation Delay of Receiver (Output Low to High) (Output High to Low)	 $t_{PLH(R)}$ $t_{PHL(R)}$	 – –	 – –	 25 23	ns

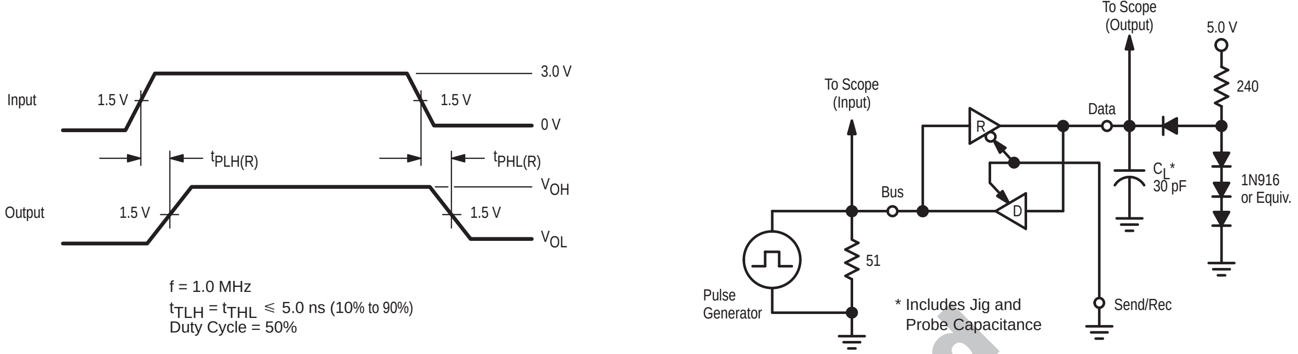
NOTE: 1. A modification of the IEEE 488–1978 Bus Standard changes $V_{OL(D)}$ from 0.4 to 0.5 V maximum to permit the use of Schottky technology.

SWITCHING CHARACTERISTICS (continued) (V_{CC} = 5.0 V, T_A = 25°C, unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Propagation Delay Time – Send/Receive to Data Logic High to Third State Third State to Logic High Logic Low to Third State Third State to Logic Low	 $t_{PHZ(R)}$ $t_{PZH(R)}$ $t_{PLZ(R)}$ $t_{PZL(R)}$	 – – – –	 – – – –	 30 30 30 30	ns
Propagation Delay Time – Send/Receive to Bus Logic High to Third State Third State to Logic High Logic Low to Third State Third State to Logic Low	 $t_{PHZ(D)}$ $t_{PZH(D)}$ $t_{PLZ(D)}$ $t_{PZL(D)}$	 – – – –	 – – – –	 30 30 30 30	ns
Turn–On Time – Enable to Bus Pull–Up Enable to Open Collector Open Collector to Pull–Up Enable	 $t_{POFF(E)}$ $t_{PON(E)}$	 – –	 – –	 30 20	ns

PROPAGATION DELAY TEST CIRCUITS AND WAVEFORMS

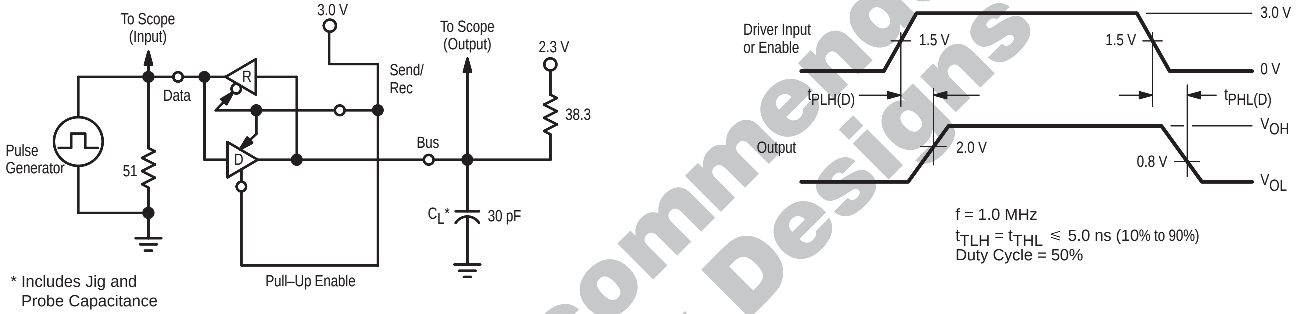
Figure 1. Bus Input to Data Output (Receiver)



f = 1.0 MHz
$t_{TLH} = t_{THL} \leqslant 5.0$ ns (10% to 90%)
Duty Cycle = 50%

* Includes Jig and Probe Capacitance

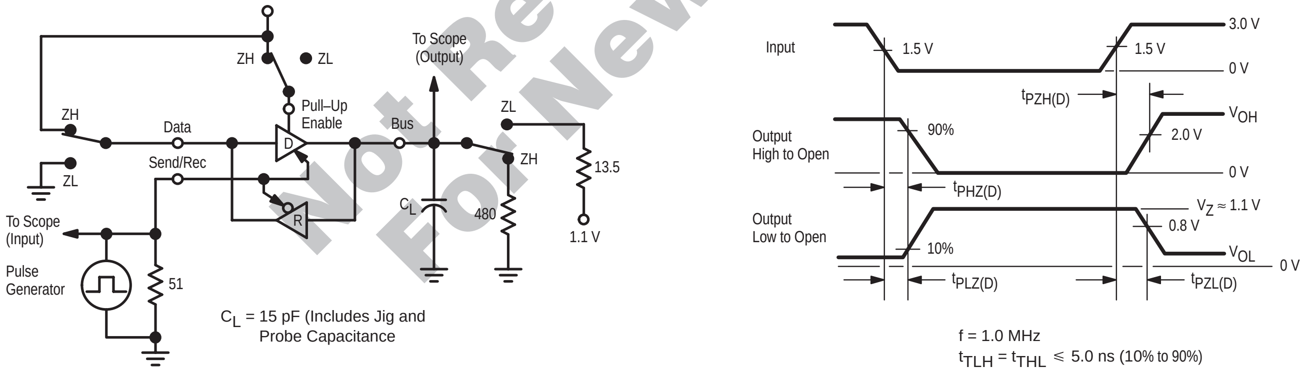
Figure 2. Data Input to Bus Output (Driver)



* Includes Jig and Probe Capacitance

f = 1.0 MHz
$t_{TLH} = t_{THL} \leqslant 5.0$ ns (10% to 90%)
Duty Cycle = 50%

Figure 3. Send/Receive Input to Bus Output (Driver)



C_L = 15 pF (Includes Jig and Probe Capacitance

f = 1.0 MHz
$t_{TLH} = t_{THL} \leqslant 5.0$ ns (10% to 90%)
Duty Cycle = 50%

Figure 4. Send/Receive Input to Data Output (Receiver)

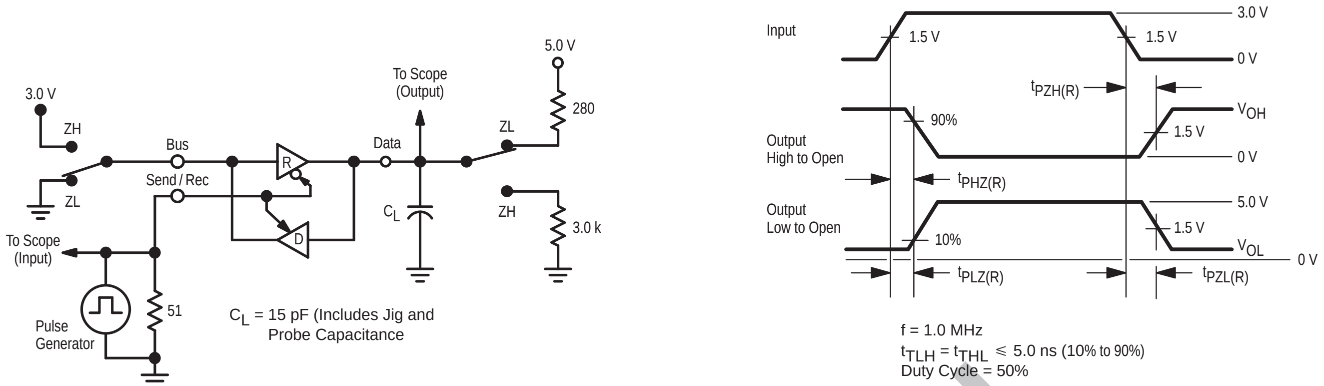


Figure 5. Enable Input to Bus Output (Driver)

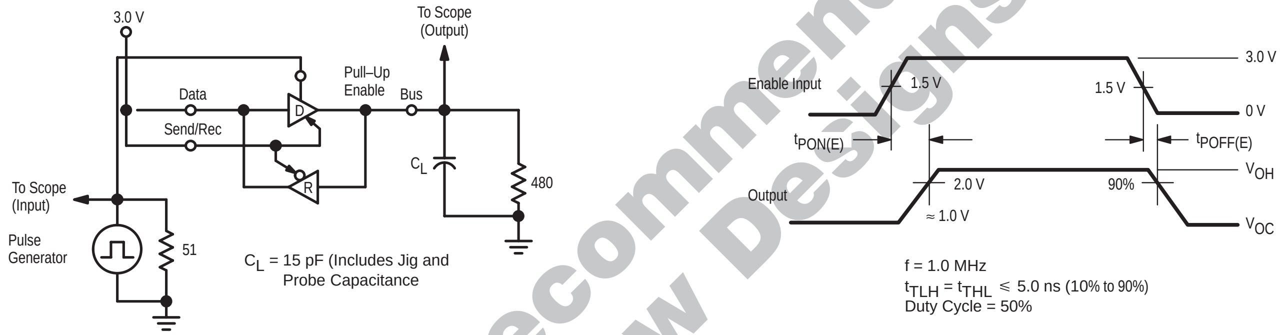


Figure 6. Typical Receiver Hysteresis Characteristics

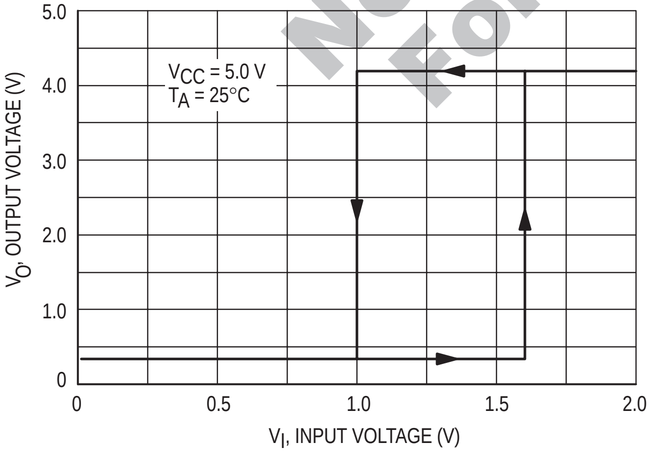


Figure 7. Typical Bus Load Line

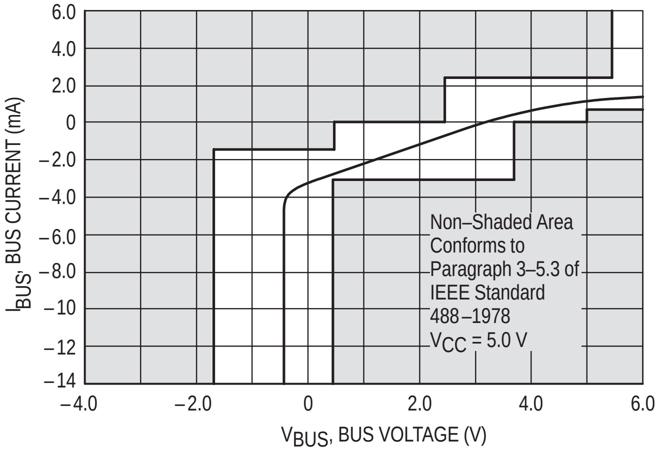
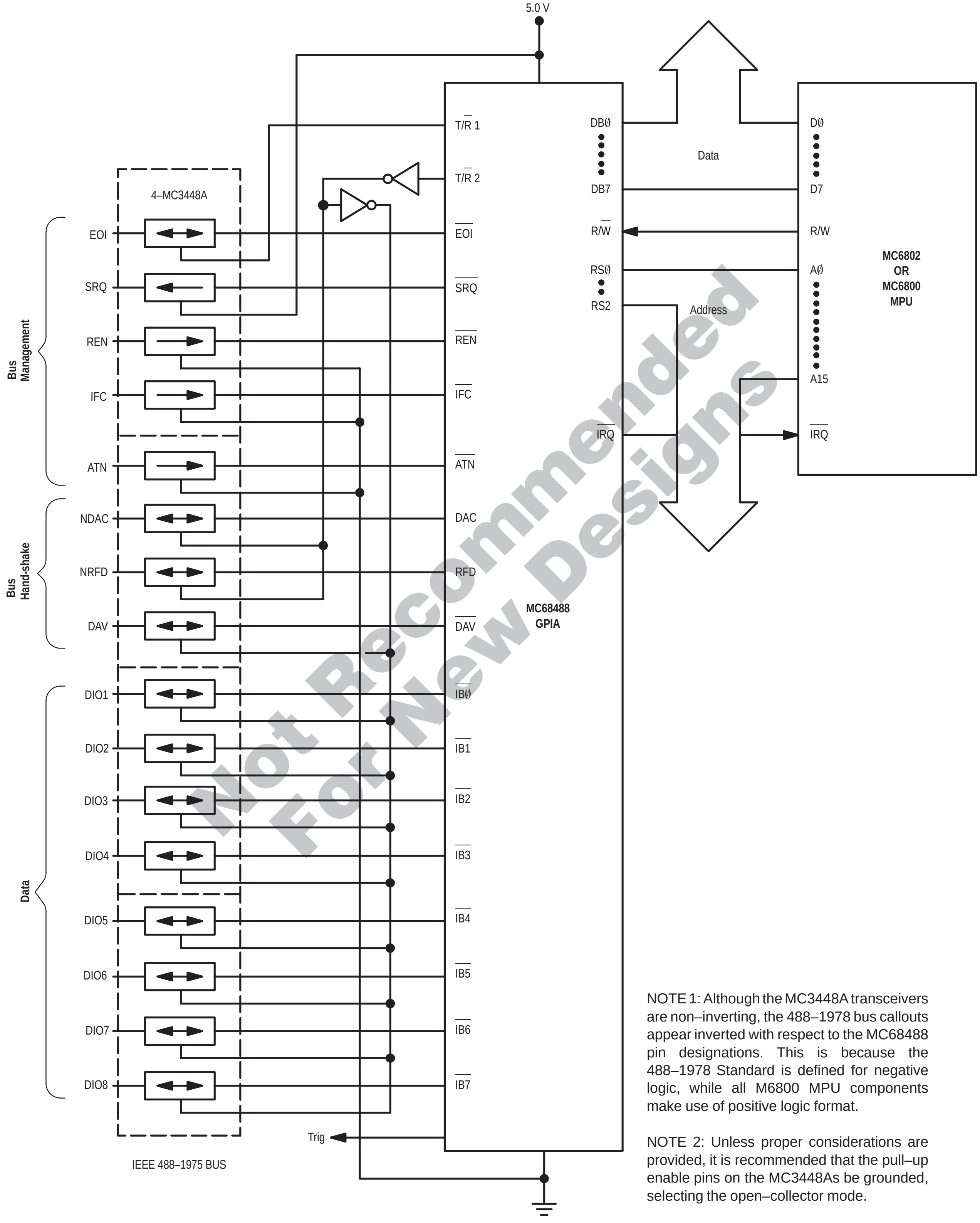


Figure 8. Simple System Configuration



NOTE 1: Although the MC3448A transceivers are non–inverting, the 488–1978 bus callouts appear inverted with respect to the MC68488 pin designations. This is because the 488–1978 Standard is defined for negative logic, while all M6800 MPU components make use of positive logic format.

NOTE 2: Unless proper considerations are provided, it is recommended that the pull–up enable pins on the MC3448As be grounded, selecting the open–collector mode.

MOTOROLA

Quad MTTL Compatible Line Receivers

MC3450

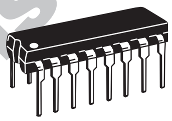
QUAD LINE RECEIVERS WITH COMMON THREE–STATE STROBE INPUT

SEMICONDUCTOR TECHNICAL DATA

The MC3450 features four MC75107 type active pullup line receivers with the addition of a common three–state strobe input. When the strobe input is at a logic zero, each receiver output state is determined by the differential voltage across its respective inputs. With the strobe high, the receiver outputs are in the high impedance state.

The strobe input on both devices is buffered to present a strobe loading factor of only one for all four receivers and inverted to provide best compatability with standard decoder devices.

- Receiver Performance Identical to the Popular MC75107/MC75108 Series
- Four Independent Receivers with Common Strobe Input
- Implied “AND” Capability with Open Collector Outputs
- Useful as a Quad 1103 type Memory Sense Amplifier



P SUFFIX
PLASTIC PACKAGE
CASE 648

TRUTH TABLE

Input	Strobe	Output MC3450
$V_{ID} \geq$ + 25 mV	L	H
	H	Z
– 25 mV $\leq V_{ID} \leq$ + 25 mV	L	I
	H	Z
$V_{ID} \leq$ – 25 mV	L	L
	H	Z

L = Low Logic State
H = High Logic State
Z = Third (High Impedance) State
I = Indeterminate State

PIN CONNECTIONS

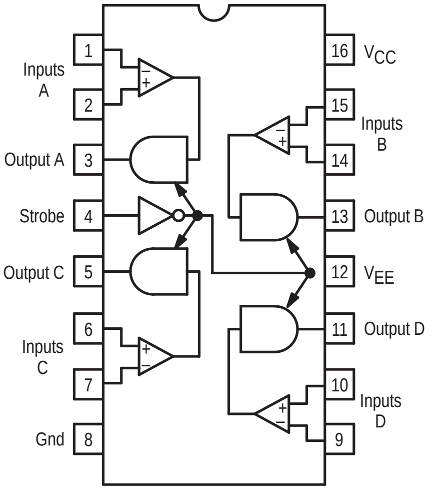
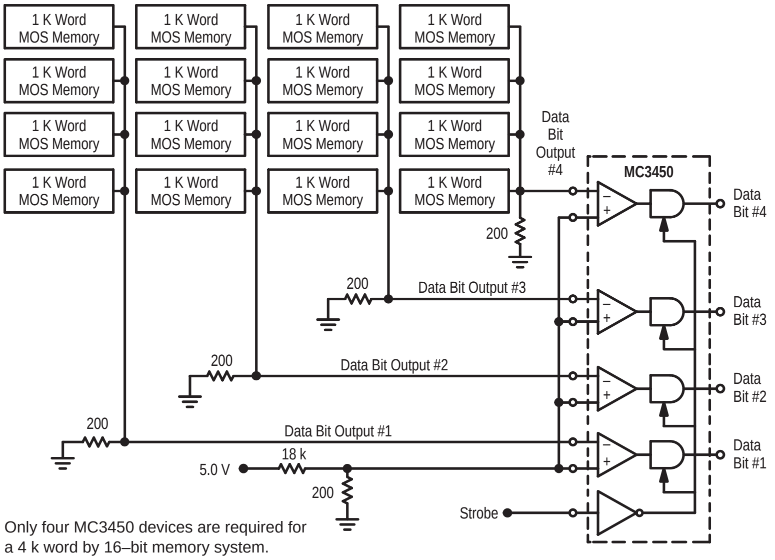


Figure 1. A Typical MOS Memory Sensing Application for a 4 k Word by 4–Bit Memory Arrangement Employing 1103 Type Memory Devices



Only four MC3450 devices are required for a 4 k word by 16–bit memory system.

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC3450P	T_A = 0 to +70°C	Plastic DIP

MAXIMUM RATINGS (T_A = 0 to +70°C, unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltages	V_{CC}, V_{EE}	±7.0	Vdc
Differential Mode Input Signal Voltage Range	V_{IDR}	±6.0	Vdc
Common Mode Input Voltage Range	V_{ICR}	±5.0	Vdc
Strobe Input Voltage	$V_{I(S)}$	5.5	Vdc
Power Dissipation (Package Limitation)	P_D		
Ceramic Dual In–Line Package		1000	mW
Derate above T_A = 25°C		6.6	mW/°C
Plastic Dual In–Line Package		1000	mW
Derate above T_A = 25°C		6.6	mW/°C
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Power Supply Voltages	V_{CC} V_{EE}	+4.75 –4.75	+5.0 –5.0	+5.25 –5.25	Vdc
Output Load Current	I_{OL}	–	–	16	mA
Differential Mode Input Voltage Range	V_{IDR}	–5.0	–	+5.0	Vdc
Common Mode Input Voltage Range	V_{ICR}	–3.0	–	+3.0	Vdc
Input Voltage Range (any input to Ground)	V_{IR}	–5.0	–	+3.0	Vdc

ELECTRICAL CHARACTERISTICS (V_{CC} = +5.0 Vdc, V_{EE} = –5.0 Vdc, T_A = 0 to +70°C, unless otherwise noted.)

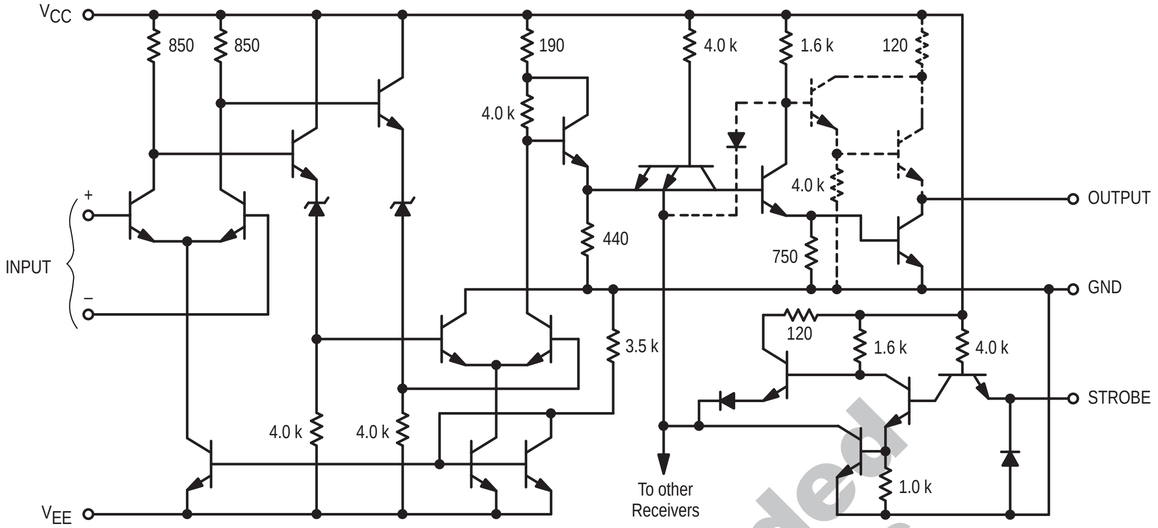
Characteristic	Symbol	MC3450			Unit
		Min	Typ	Max	
High Level Input Current to Receiver Input	$I_{IH(I)}$	–	–	75	µA
Low Level Input Current to Receiver Input	$I_{IL(I)}$	–	–	–10	µA
High Level Input Current to Strobe Input	$I_{IH(S)}$				
$V_{IH(S)}$ = 2.4 V		–	–	40	µA
$V_{IH(S)}$ = 5.25 V		–	–	1.0	mA
Low Level Input Current to Strobe Input $V_{IL(S)}$ = 0.4 V	$I_{IL(S)}$	–	–	–1.6	mA
High Level Output Voltage	V_{OH}	2.4	–	–	Vdc
High Level Output Leakage Current	I_{CEX}	–	–	–	µA
Low Level Output Voltage	V_{OL}	–	–	0.5	Vdc
Short–Circuit Output Current	I_{OS}	–18	–	–70	mA
Output Disable Leakage Current	I_{off}	–	–	40	µA
High Logic Level Supply Current from V_{CC}	I_{CCH}	–	45	60	mA
High Logic Level Supply Current from V_{EE}	I_{EEH}	–	–17	–30	mA

SWITCHING CHARACTERISTICS (V_{CC} = +5.0 Vdc, V_{EE} = –5.0 Vdc, T_A = +25°C, unless otherwise noted.)

Characteristic	Symbol	MC3450			Unit
		Min	Typ	Max	
High to Low Logic Level Propagation Delay Time (Differential Inputs)	$t_{PHL(D)}$	–	–	25	ns
Low to High Logic Level Propagation Delay Time (Differential Inputs)	$t_{PLH(D)}$	–	–	25	ns
Open State to High Logic Level Propagation Delay Time (Strobe)	$t_{PZH(S)}$	–	–	21	ns
High Logic Level to Open State Propagation Delay Time (Strobe)	$t_{PHZ(S)}$	–	–	18	ns
Open State to Low Logic Level Propagation Delay Time (Strobe)	$t_{PZL(S)}$	–	–	27	ns
Low Logic Level to Open State Propagation Delay Time (Strobe)	$t_{PLZ(S)}$	–	–	29	ns
High Logic to Low Logic Level Propagation Delay Time (Strobe)	$t_{PHL(S)}$	–	–	–	ns
Low Logic to High Logic Level Propagation Delay Time (Strobe)	$t_{PLH(S)}$	–	–	–	ns

Figure 2. Circuit Schematic

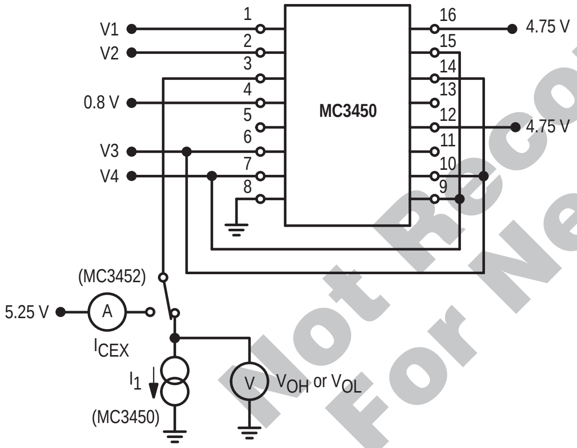
(1/4 Circuit Shown)



Dashed components apply to the MC3450 circuit only.

TEST CIRCUITS

Figure 3. I_{CEX}, V_{OH}, and V_{OL}



TEST TABLE

	V1	V2	V3	V4	
	MC3450	**MC3450**	**MC3450**	**MC3450**	**I1**
V_{OH}	2.975 V	3.0 V	3.0 V	GND	0.4 mA
	–3.0 V	–2.975 V	GND	–3.0 V	
I_{CEX}		–	–	–	–
		–	–	–	–
V_{OL}	3.0 V	2.975 V	GND	3.0 V	–16 mA
	–2.975 V	–3.0V	–3.0 V	GND	

Channel A shown under test. Other channels are tested similarly.

Figure 4. I_{CCH} and I_{EEH}

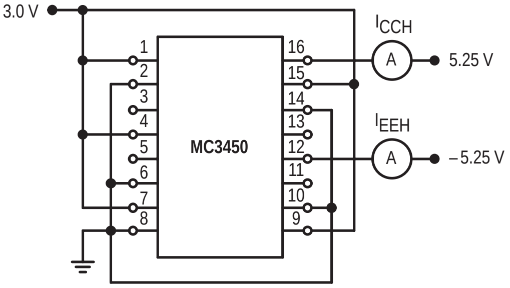
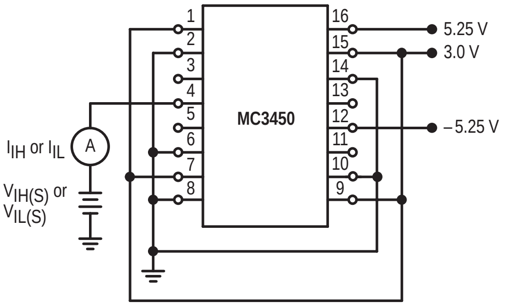
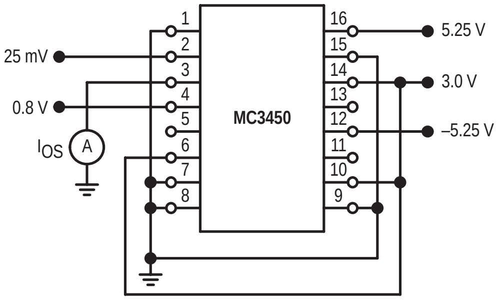


Figure 5. $I_{IH(S)}$ and $I_{IL(S)}$



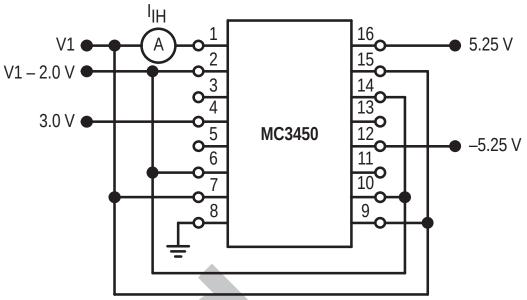
TEST CIRCUITS (continued)

Figure 6. I_{OS}



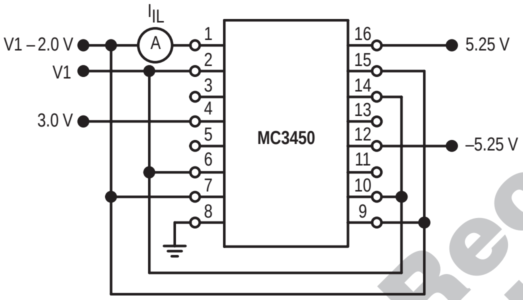
Channel A shown under test, other channels are tested similarly.
Only one output shorted at a time.

Figure 7. I_{IH}



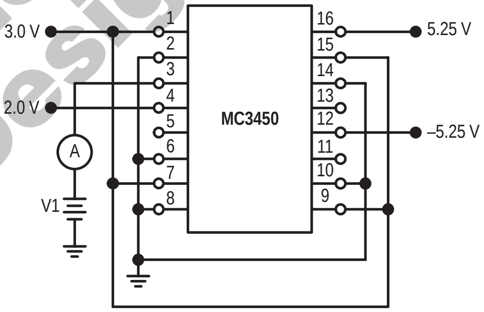
Channel A(–) shown under test, other channels are tested similarly. Devices are tested with V1 from 3.0 V to – 3.0 V.

Figure 8. I_{IL}



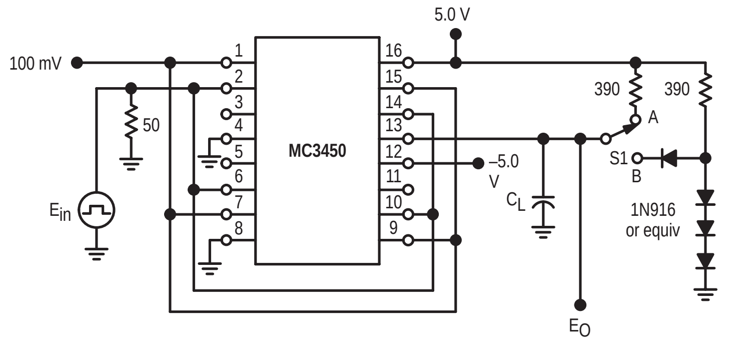
Channel A(–) shown under test, other channels are tested similarly. Devices are tested with V1 from 3.0 V to – 3.0 V.

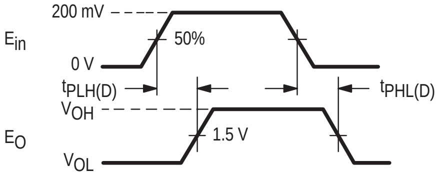
Figure 9. I_{off}



Output of Channel A shown under test, other outputs are tested similarly for V1 = 0.4 V and 2.4 V.

Figure 10. Receiver Propagation Delay $t_{PLH(D)}$ and $t_{PHL(D)}$



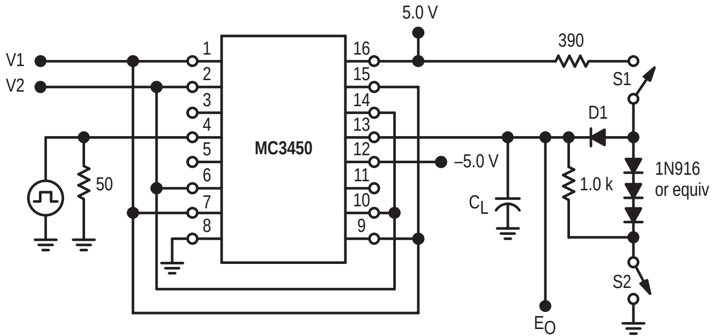


Output of Channel B shown under test, other channels are tested similarly.
S1 at “A” for MC3452
S1 at “B” for MC3450
C_L = 15 pF total for MC3452
C_L = 50 pF total for MC3450

E_{in} waveform characteristics:
t_{TLH} and t_{THL} ≤ 10 ns measured 10% to 90%
PRR = 1.0 MHz
Duty Cycle = 500 ns

TEST CIRCUITS (continued)

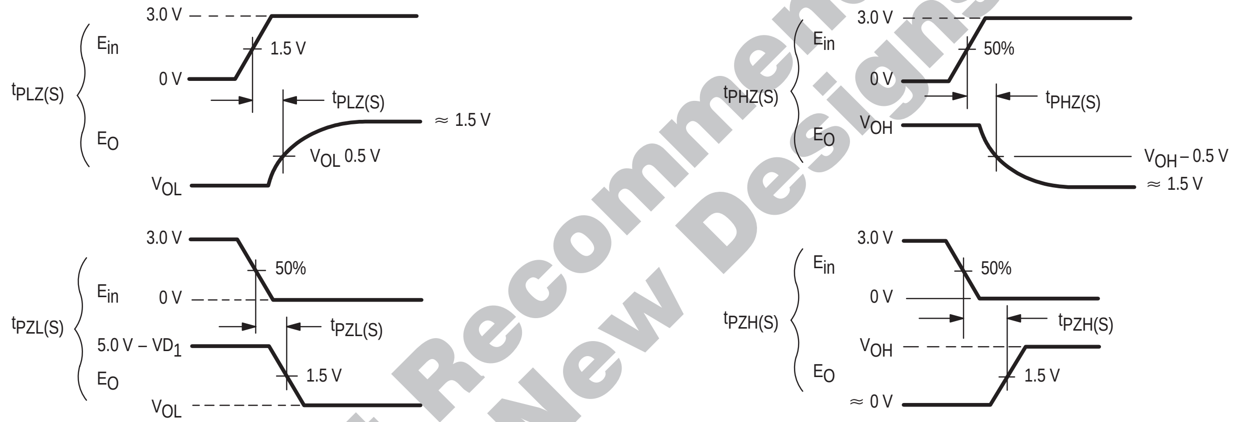
Figure 11. Strobe Propagation Delay Times $t_{PLZ(S)}$ $t_{PZL(S)}$ $t_{PHZ(S)}$ and $t_{PZH(S)}$



Output of Channel B shown under test, other channels are tested similarly.

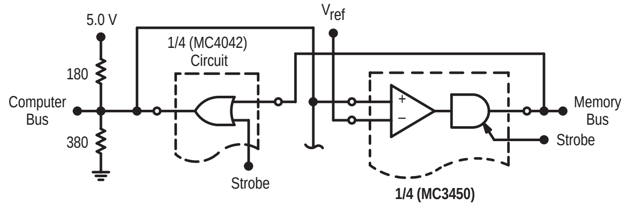
	V1	V2	S1	S2	C_L
$t_{PLZ(S)}$	100 mV	GND	Closed	Closed	15 pF
$t_{PZL(S)}$	100 mV	GND	Closed	Open	50 pF
$t_{PHZ(S)}$	GND	100 mV	Closed	Closed	15 pF
$t_{PZH(S)}$	GND	100 mV	Open	Closed	50 pF

C_L includes jig and probe capacitance.
E_{in} waveform characteristics:
t_{TLH} and t_{THL} ≤ 10 ns measured 10% to 90%.
PRR = 1.0 MHz
Duty Cycle = 50%



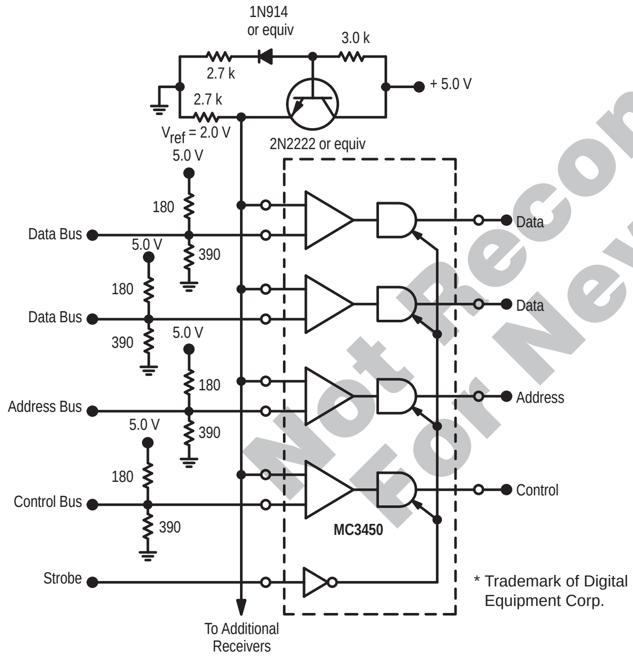
APPLICATIONS INFORMATION

Figure 12. Bidirectional Data Transmission



The three–state capability of the MC3450 permits bidirectional data transmission as illustrated.

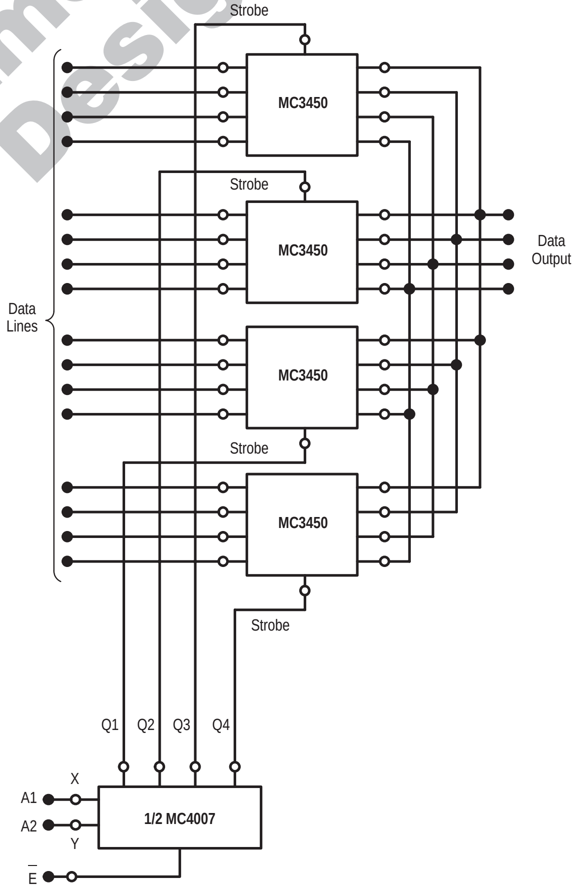
Figure 13. Single–Ended Uni–Bus™ Line Receiver Application for Minicomputer



* Trademark of Digital Equipment Corp.

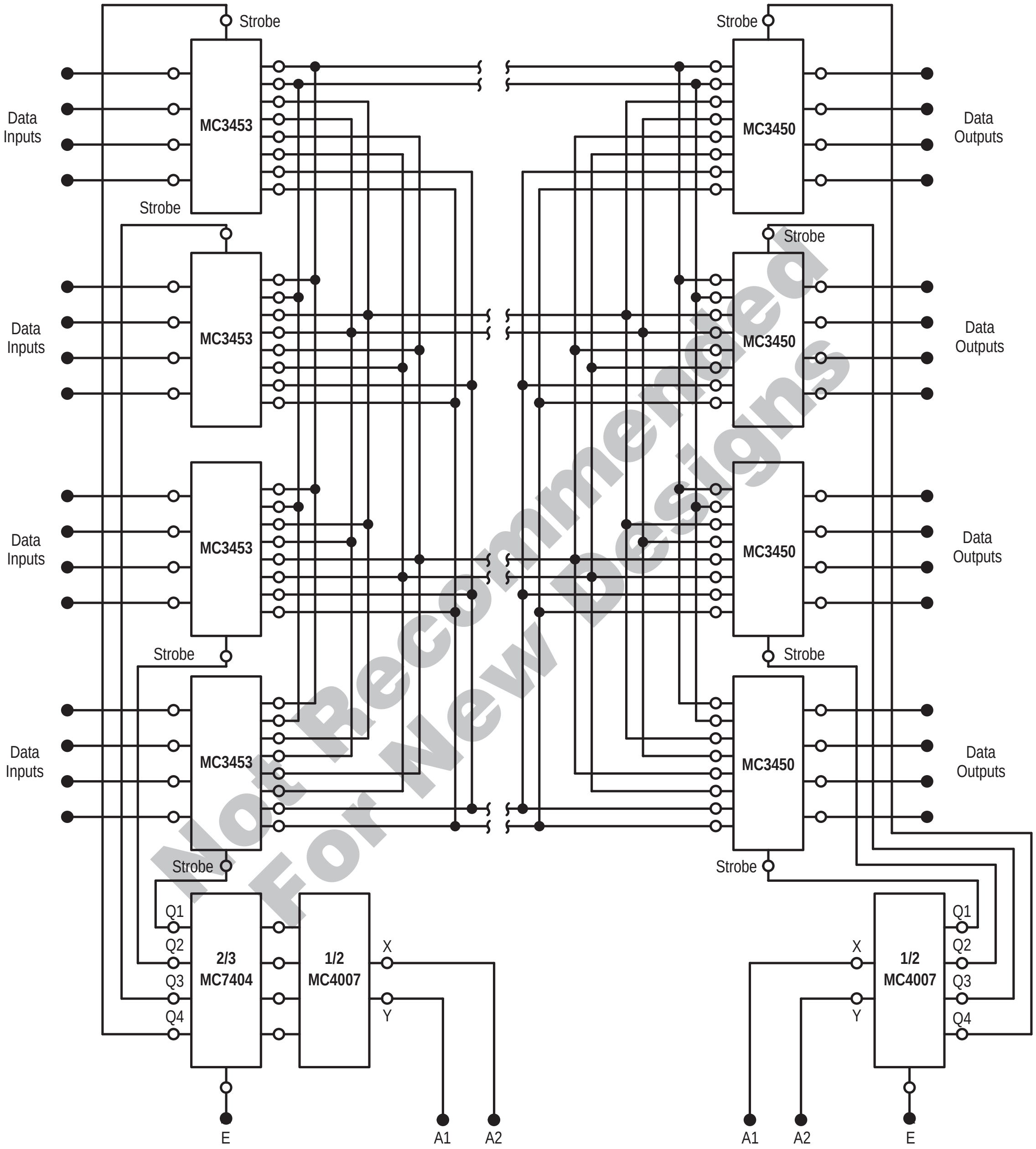
The MC3450 can be used for single–ended as well as differential line receiving. For single–ended line receiver applications, such as are encountered in minicomputers, the configuration shown in Figure 15 can be used. The voltage source, which generates V_{ref}, should be designed so that the V_{ref} voltage is halfway between V_{OH}(min) and V_{OL}(max). The maximum input overdrive required to guarantee a given logic state is extremely small, 25 mV maximum. This low–input overdrive enhances differential noise immunity. Also the high–input impedance of the line receiver permits many receivers to be placed on a single line with minimum load effects.

Figure 14. Wired “OR” Data Selection Using Three–State Logic



APPLICATIONS INFORMATION (continued)

Figure 15. Party–Line Data Transmission System with Multiplex Decoding



MOTOROLA

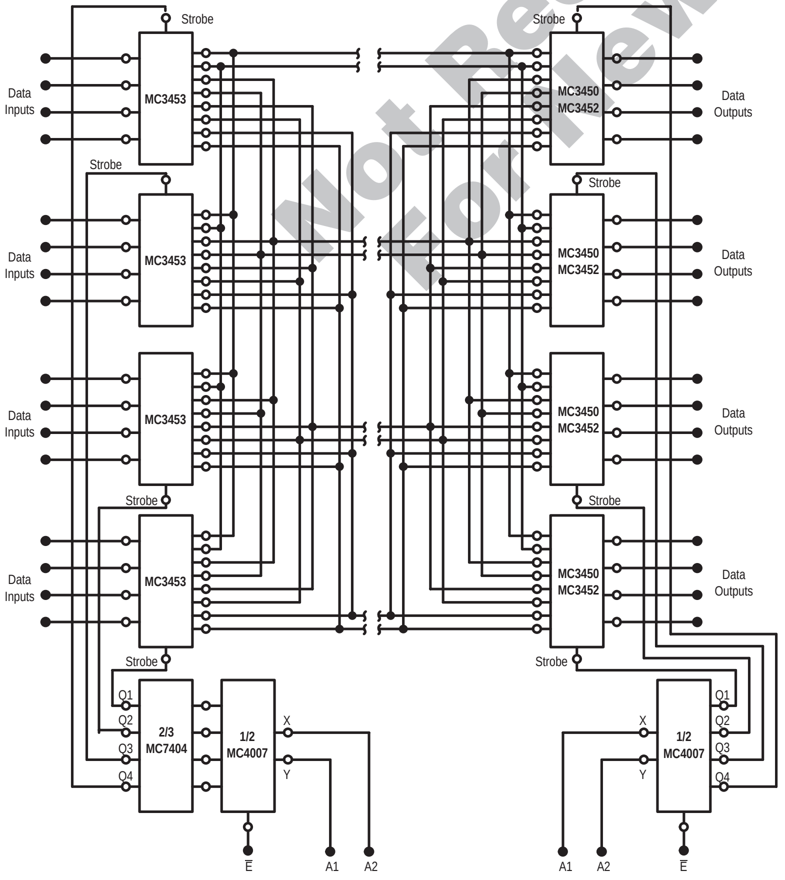
MC3453

MTTL Compatible Quad Line Driver

The MC3453 features four SN75110 type line drivers with a common inhibit input. When the inhibit input is high, a constant output current is switched between each pair of output terminals in response to the logic level at that channel′s input. When the inhibit is low, all channel outputs are nonconductive (transistors biased to cut–off). This minimizes loading in party–line systems where a large number of drivers share the same line.

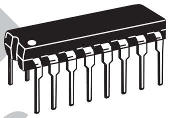
- Four Independent Drivers with Common Inhibit Input
- – 3.0 V Output Common–Mode Voltage Over Entire Operating Range
- Improved Driver Design Exceeds Performance of Popular SN75110

Figure 1. Party–Line Data Transmission System with Multiplex Decoding



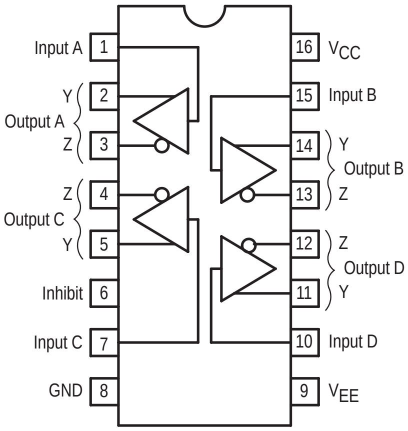
QUAD LINE DRIVER WITH COMMON INHIBIT INPUT

SEMICONDUCTOR TECHNICAL DATA



P SUFFIX
PLASTIC PACKAGE
CASE 648

PIN CONNECTIONS



TRUTH TABLE (positive logic)

Logic Input	Inhibit Input	Output Current	
		Z	Y
H	H	On	Off
L	H	Off	On
H	L	Off	Off
L	L	Off	Off

L = Low Logic Level
H = High Logic Level

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC3453P	T_A = 0 to +70°C	Plastic DIP

MAXIMUM RATINGS (T_A = 0 to +70°C, unless otherwise noted.)

	Symbol	Value	Unit
Power Supply Voltage Logic and Inhibitor Input Voltages	V_{CC} V_{EE} V_{in}	+7.0 –7.0 5.5	V V
Common–Mode Output Voltage Range	V_{OCR}	–5.0 to +12	V
Power Dissipation (Package Limitation) Plastic Dual In–Line Package Derate above T_A = 25°C	P_D	 1000 6.6	 mW mW/°C
Operating Ambient Temperature Range	T_A	0 to +70	°C
Storage Temperature Range Plastic and Ceramic Dual In–Line Packages	T_{stg}	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS (See Notes 1 and 2.)

Characteristic	Symbol	Min	Nom	Max	Unit
Power Supply Voltages	V_{CC} V_{EE}	+4.75 –4.75	+5.0 –5.0	+5.25 –5.25	V
Common–Mode Output Voltage Range Positive Negative	V_{OCR}	 0 0	 – –	 +10 –3.0	V

NOTES: 1. These voltage values are in respect to the ground terminal.
2. When not using all four channels, unused outputs **must** be grounded.

DEFINITIONS OF INPUT LOGIC LEVELS*

Characteristic	Symbol	Min	Max	Unit
High–Level Input Voltage (at any input)	V_{IH}	2.0	5.5	V
Low–Level Input Voltage (at any input)	V_{IL}	0	0.8	V

* The algebraic convention, where the most positive limit is designated maximum, is used with Logic Level Input Voltage Levels only.

ELECTRICAL CHARACTERISTICS (T_A = 0 to +70°C, unless otherwise noted.)

Characteristic##	Symbol	Min	Typ#	Max	Unit
High–Level Input Current (Logic Inputs) (V_{CC} = Max, V_{EE} = Max, V_{IH_L} = 2.4 V) (V_{CC} = Max, V_{EE} = Max, V_{IH_L} = V_{CC} Max)	I_{IH_L}	 – –	 – –	 40 1.0	 µA mA
Low–Level Input Current (Logic Inputs) (V_{CC} = Max, V_{EE} = Max, V_{IL_L} = 0.4 V)	I_{IL_L}	–	–	–1.6	mA
High–Level Input Current (Inhibit Input) (V_{CC} = Max, V_{EE} = Max, V_{IH_I} = 2.4 V) (V_{CC} = Max, V_{EE} = Max, V_{IH_I} = V_{CC} Max)	I_{IH_I}	 –	 –	 40	 µA
Low–Level Input Current (Inhibit Input) (V_{CC} = Max, V_{EE} = Max, V_{IL_I} = 0.4 V)	I_{IL_I}	–	–	–1.6	mA
Output Current (“ON” state) (V_{CC} = Max, V_{EE} = Max) (V_{CC} = Min, V_{EE} = Min)	$I_{O(on)}$	 – 6.5	 11 11	 15 –	mA
Output Current (“OFF” state) (V_{CC} = Min, V_{EE} = Min)	$I_{O(off)}$	–	5.0	100	µA
Supply Current from V_{CC} (with driver enabled) (V_{IL_L} = 0.4 V, V_{IH_I} = 2.0 V)	$I_{CC(on)}$	–	35	50	mA

#All typical values are at V_{CC} = 5.0 V, V_{EE} = –5.0 V, T_A = 25°C.
##For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable device type. Ground unused inputs and outputs.

ELECTRICAL CHARACTERISTICS (T_A = 0 to +70°C, unless otherwise noted.)

Characteristic##	Symbol	Min	Typ#	Max	Unit
Supply Current from V_{EE} (with driver enabled) (V_{IL_L} = 0.4 V, V_{IH_I} = 2.0 V)	$I_{EE(on)}$	–	65	90	mA
Supply Current from V_{CC} (with driver inhibited) (V_{IL_L} = 0.4 V, V_{IL_I} = 0.4 V)	$I_{CC(off)}$	–	35	50	mA
Supply Current from V_{EE} (with driver inhibited) (V_{IL_L} = 0.4 V, V_{IL_I} = 0.4 V)	$I_{EE(off)}$	–	25	40	mA

#All typical values are at V_{CC} = 5.0 V, V_{EE} = –5.0 V, T_A = 25°C.
##For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable device type. Ground unused inputs and outputs.

SWITCHING CHARACTERISTICS (V_{CC} = 5.0 V, V_{EE} = –5.0 V, T_A = 25°C.)

Characteristic	Symbol	Min	Typ	Max	Unit
Propagation Delay Time from Logic Input to Output Y or Z (R_L = 50 ohms, C_L = 40 pF)	t_{PLH_L} t_{PHL_L}	– –	9.0 9.0	17 17	ns
Propagation Delay time from Inhibit Input to Output Y or Z (R_L = 50 ohms, C_L = 40 pF)	t_{PLH_I} t_{PHL_I}	– –	20 16	25 25	ns

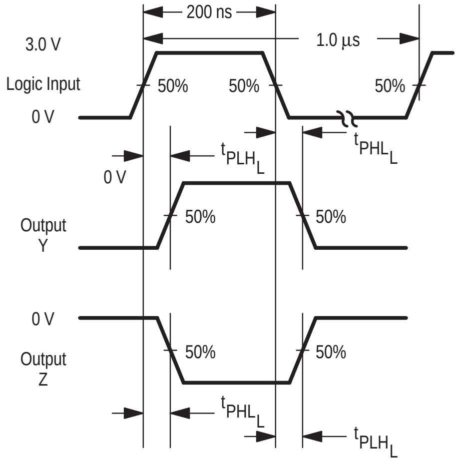


Figure 2. Logic Input to Outputs Propagation Delay Time Waveforms

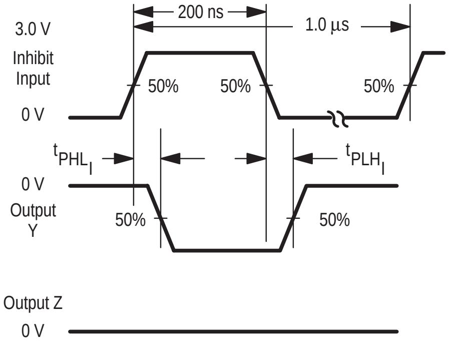


Figure 3. Inhibit Input to Outputs Propagation Delay Time Waveforms

TEST CIRCUITS

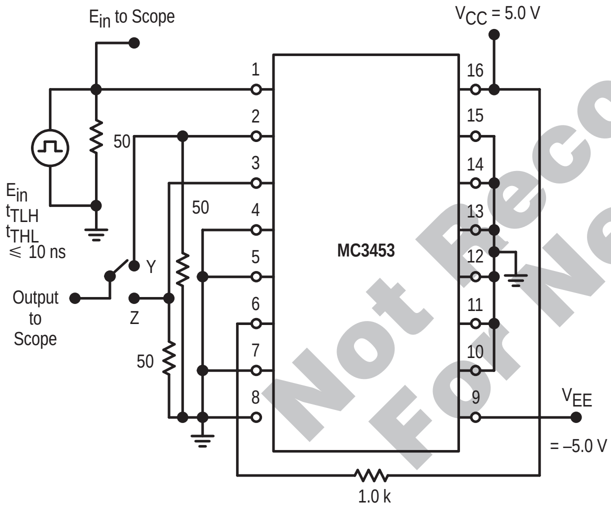


Figure 4. Logic Input to Output Propagation Delay Time Test Circuit

Channel A shown under test, the other channels are tested similarly.

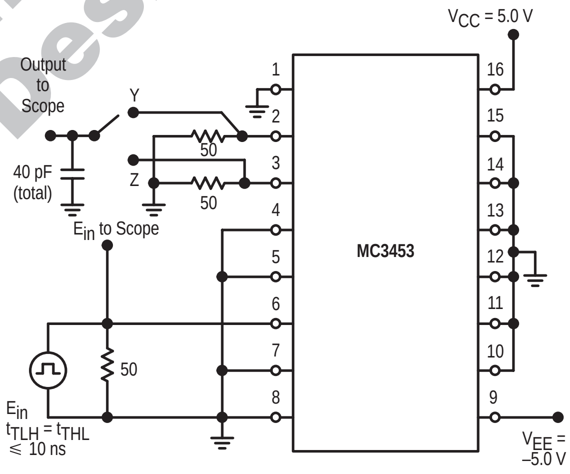
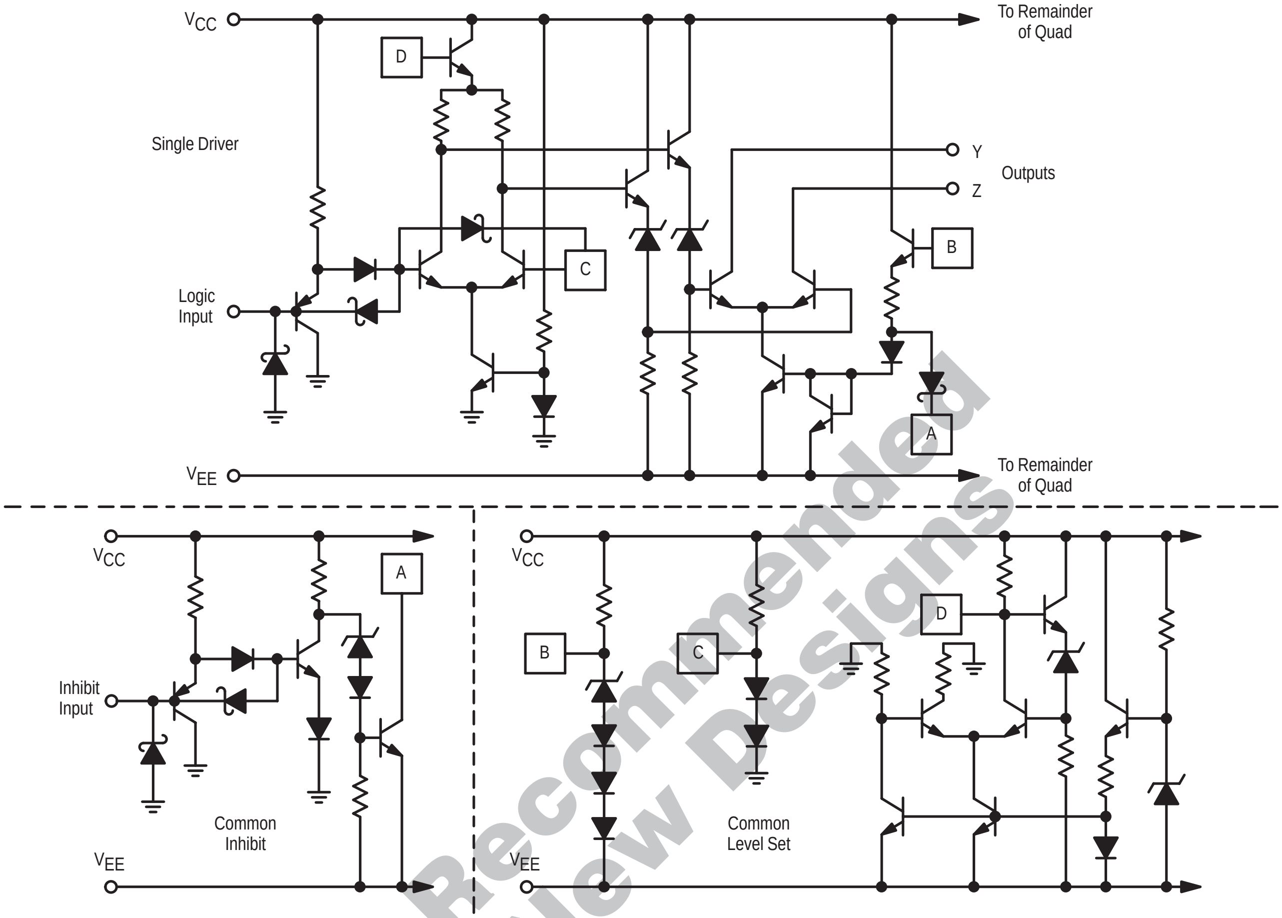


Figure 5. Inhibit Input to Output Propagation Delay time Test Circuit

Channel A shown under test, the other channels are tested similarly.

Figure 6. Circuit Schematic
(1/4 Circuit Shown)



MC3467

Triple Wideband Preamplifier with Electronic Gain Control (EGC)

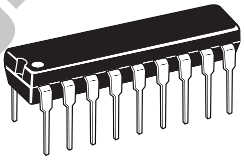
TRIPLE MAGNETIC TAPE MEMORY PREAMPLIFIER

SEMICONDUCTOR TECHNICAL DATA

The MC3467 provides three independent preamplifiers with individual electronic gain control in a single 18–pin package. Each preamplifier has differential inputs and outputs allowing operation in completely balanced systems. The device is optimized for use in 9–track magnetic tape memory systems where low noise and low distortion are paramount objectives.

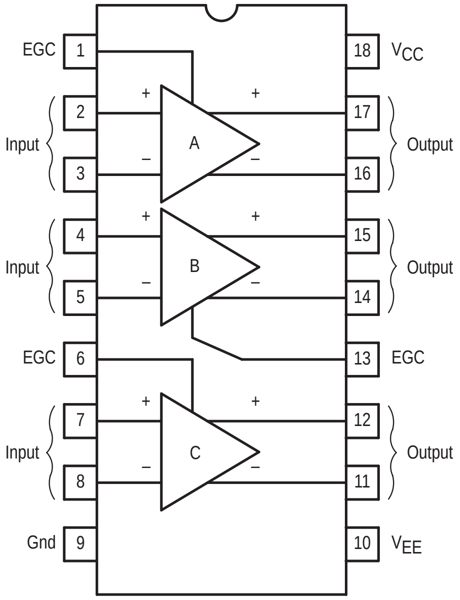
The electronic gain control allows each amplifier′s gain to be set anywhere from essentially zero to a maximum of approximately 100 V/V.

- Wide Bandwidth – 15 MHz (Typical)
- Individual Electronic Gain Control
- Differential Input/Output

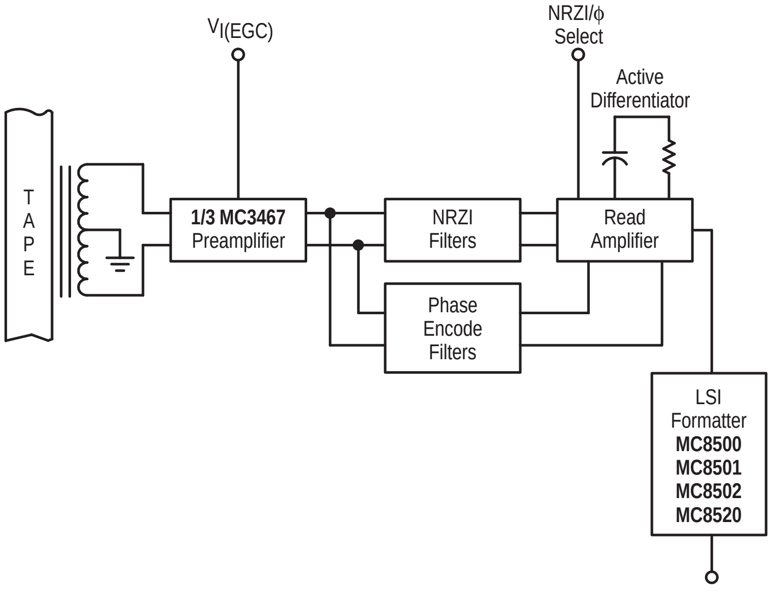


P SUFFIX
PLASTIC PACKAGE
CASE 707

PIN CONNECTIONS



Simplified Application
High Performance 9–Track Open Reel Tape System



ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC3467P	T_A = 0 to +70°C	Plastic DIP

MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltages			V
Positive Supply Voltage	V_{CC}	6.0	
Negative Supply Voltage	V_{EE}	–9.0	
EGC Voltages (Pins 1, 6 and 13)	$V_{I(EGC)}$	–5.0 to V_{CC}	V
Input Differential Voltage	V_{ID}	± 5.0	V
Input Common–Mode Voltage	V_{IC}	± 5.0	V
Amplifier Output Short Circuit Duration (to Ground)	t_{sc}	10	s
Operating Ambient Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	– 65 to +150	°C
Junction Temperature	T_J	+150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, V_{EE} = –6.0 V, f =100 kHz, T_A = 0 to +70°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Power Supply Voltage Range					V
Positive Supply Voltage	V_{CCR}	4.75	5.0	5.25	
Negative Supply Voltage	V_{EER}	–5.5	–6.0	–7.0	
Operating EGC Voltage	$V_{I(EGC)}$	0	–	V_{CC}	
Differential Voltage Gain (Balanced) ($V_{I(EGC)}$ = 0, e_i = 25 mVpp) (See Figure 1)	A_{VD}	85	100	120	V/V
Differential Voltage Gain ($V_{I(EGC)}$ = V_{CC})	A_{VD}	–	0.5	2.0	V/V
Maximum Input Differential Voltage (Balanced) (T_A = 25°C)	V_{IDR}	0.2	–	–	V_{pp}
Output Voltage Swing (Balanced) (Figure 1) (e_i = 200 mVpp)	V_{OR}	6.0	8.0	–	V_{pp}
Input Common–Mode Range	V_{ICR}	± 1.5	± 2.0	–	V
Differential Output Offset Voltage (T_A = 25°C)	V_{OOD}	–	500	–	mV
Common–Mode Output Offset Voltage (T_A = 25°C)	V_{OOC}	–	500	–	mV
Common–Mode Rejection Ratio (Figure 2) $V_{I(EGC)}$ = 0, V_{CM} = 1.0 V pp	CMRR				dB
(f = 100 kHz)		60	100	–	
(f = 1.0 MHz)		40	100	–	
Small–Signal Bandwidth (Figure 1) (–3.0 dB, e_i = 1.0 mVpp, T_A = 25°C)	BW	10	15	–	MHz
Input Bias Current	I_{IB}	–	5.0	15	µA
Output Sink Current (Figure 5)	I_{OS}	1.0	1.4	–	mA
Differential Noise Voltage Referred to Input (Figure 3) ($V_{I(EGC)}$ = 0, R_S = 50 Ω, BW = 10 Hz to 1.0 MHz, T_A = 25°C)	e_n	–	3.5	–	μV_{RMS}
Positive Power Supply Current (Figure 4)	I_{CC}	–	30	40	mA
Negative Power Supply Current (Figure 4)	I_{EE}	–	–30	–40	mA
Input Resistance (T_A = 25°C)	r_i	12	25	–	kΩ
Input Capacitance (T_A = 25°C)	C_i	–	2.0	–	pF
Output Resistance (Unbalanced) (T_A = 25°C)	r_o	–	30	–	Ohms

Figure 1. Differential Voltage Gain, Bandwidth and Output Voltage Swing Test Circuit

(Channel A under test, other channels tested similarly)

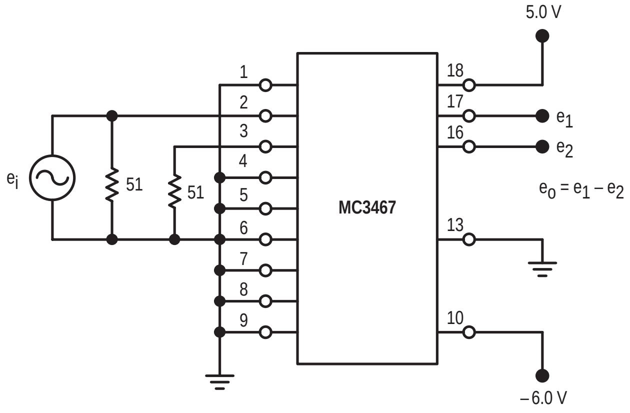


Figure 2. Common–Mode Rejection Ratio

(Channel A under test, other amplifiers tested similarly)

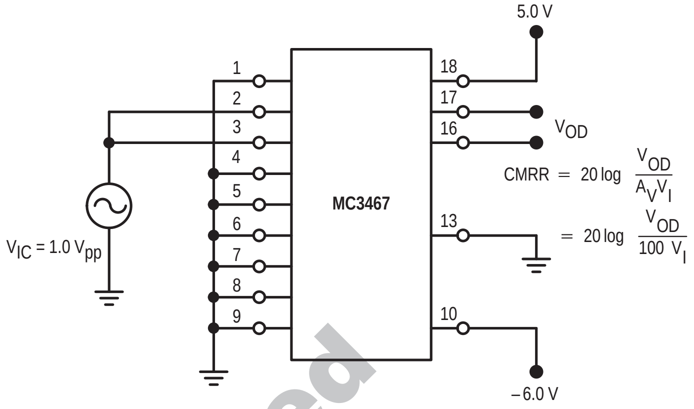
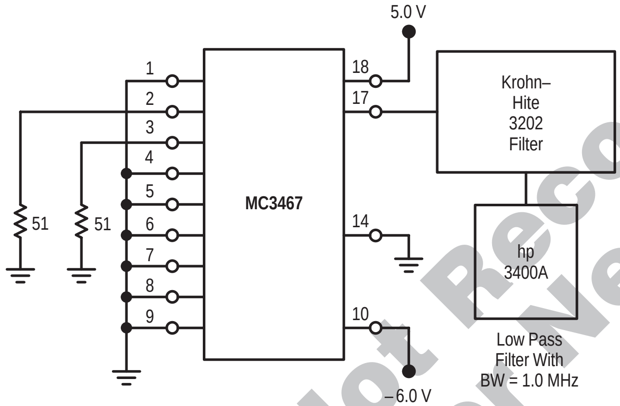


Figure 3. Differential Noise Voltage Referred to the Input



Assume Uncorrelated Noise Sources

e_n (Differential Noise at Input) $= e_o \sqrt{2} / 100$

Figure 4. Power Supply Current Test Circuit

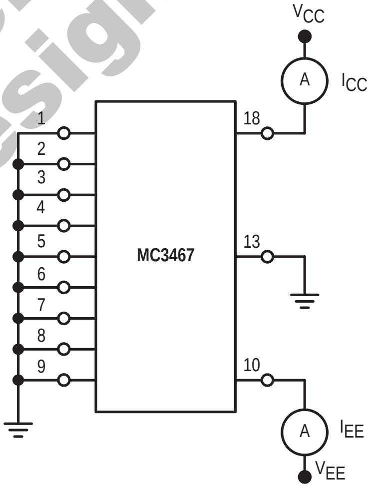


Figure 5. Output Sink Current Test Circuit

(Channel A under test, other channels tested similarly)

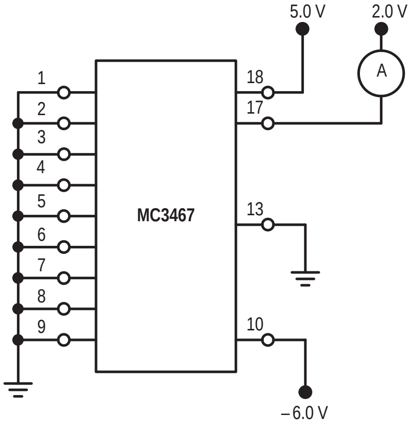
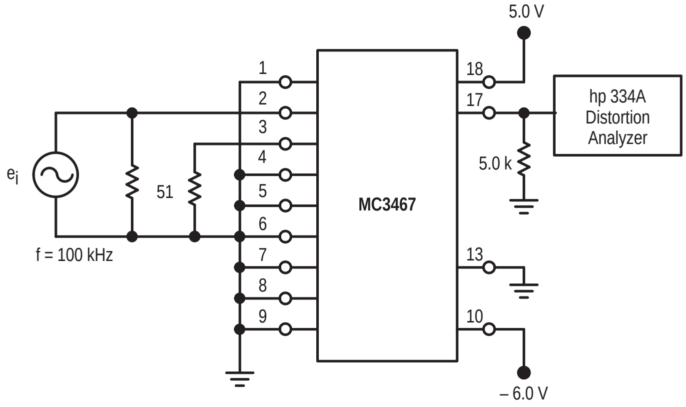


Figure 6. Total Harmonic Distortion Test Circuit

(Channel A under test, other channels tested similarly)



TYPICAL CHARACTERISTICS
(V_{CC} = 5.0 V, V_{EE} = –6.0V, T_A = 25° unless otherwise noted)

Figure 7. Total Harmonic Distortion (THD) versus Input Voltage

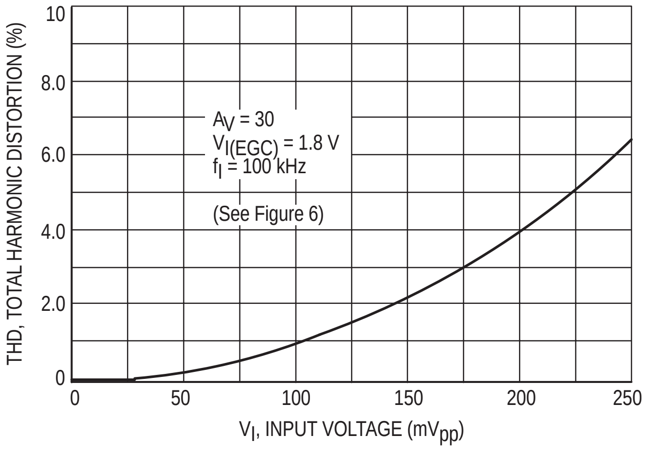


Figure 8. Normalized Voltage Gain versus Frequency

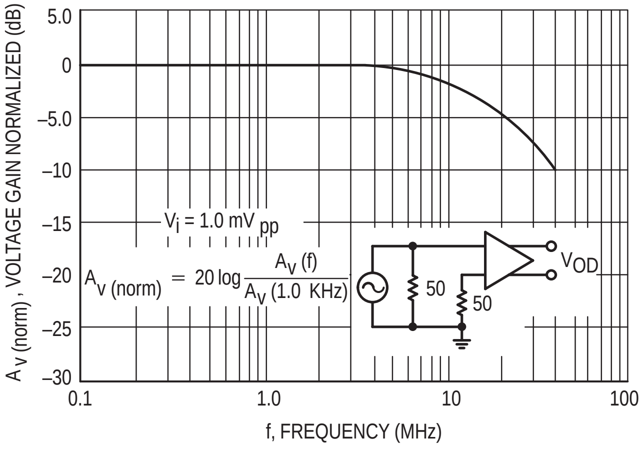


Figure 9. Normalized Voltage Gain versus Ambient Temperature

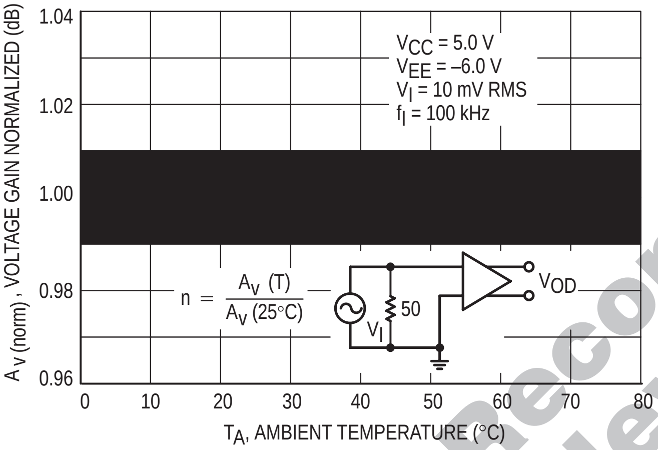


Figure 10. Normalized Positive Power Supply Current versus Positive Power Supply Voltage

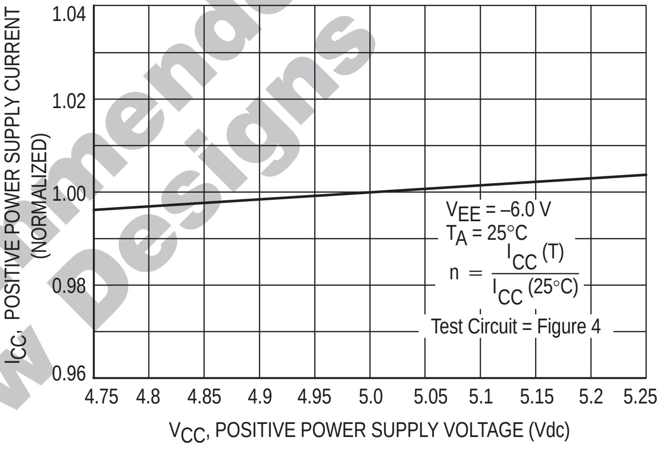


Figure 11. Normalized Negative Power Supply Current versus Negative Power Supply Voltage

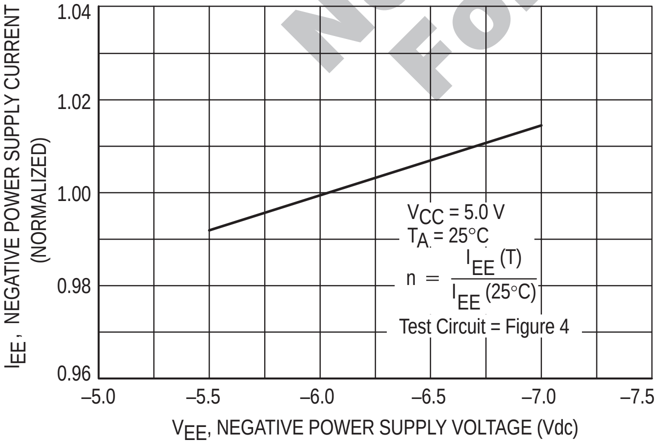


Figure 12. Normalized Power Supply Currents versus Ambient Temperature

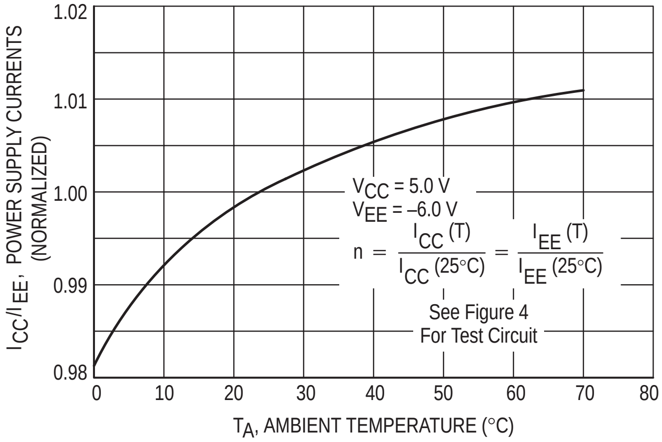


Figure 13. Differential Voltage Gain versus Electronic Gain Control Voltage ($V_{I(EGC)}$)

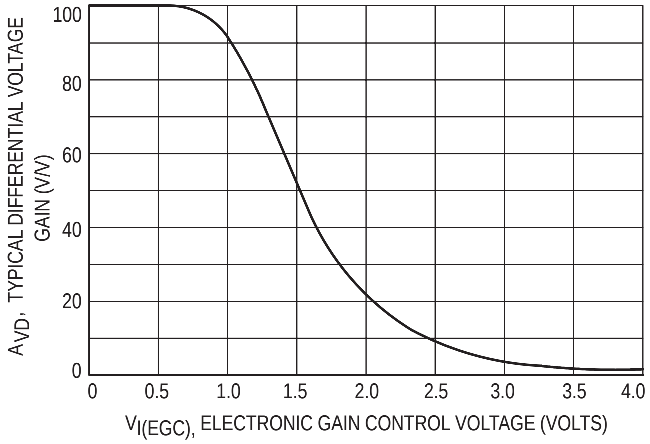


Figure 14. Common–Mode Rejection Ratio (CMRR) versus Frequency

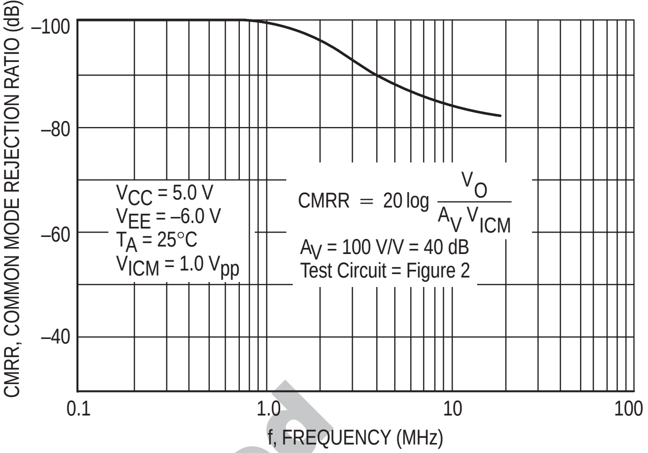


Figure 15. Phase Shift versus Frequency

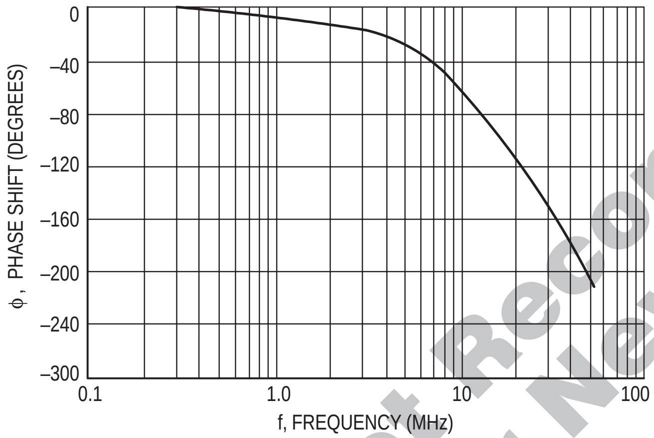
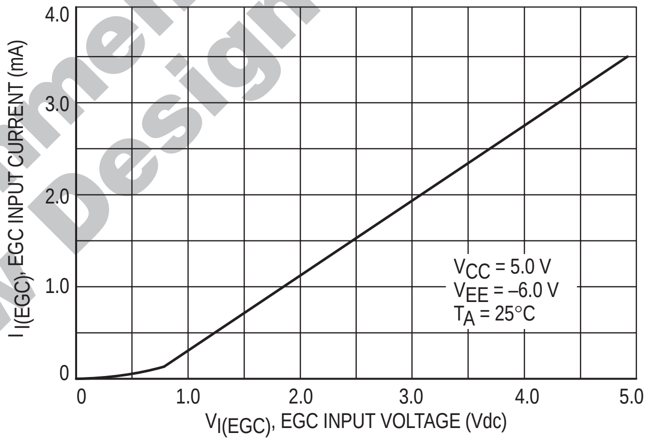
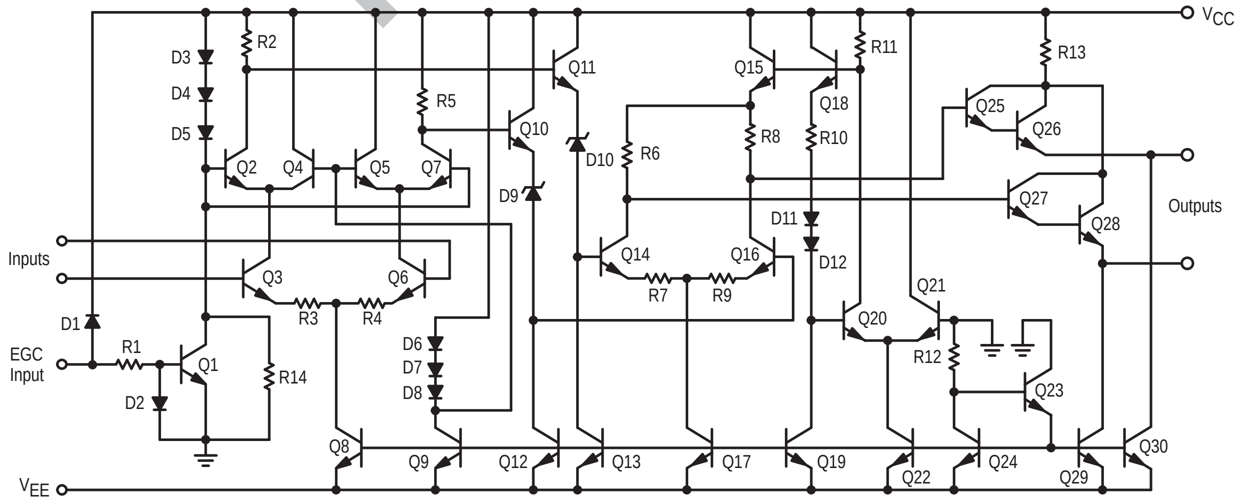


Figure 16. Typical EGC Input Current versus EGC Input Voltage



Representative Schematic Diagram

1/3 MC3467



MOTOROLA

MC3481
MC3485

Quad Single-Ended Line Drivers

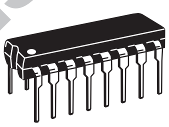
IBM 360/370 QUAD LINE DRIVERS

SEMICONDUCTOR TECHNICAL DATA

The MC3481 and MC3485 are quad single–ended line drivers specifically designed to meet the IBM 360/370 I/O specification (GA22–6974–3).

Output levels are guaranteed over the full range of output load and fault conditions. Compliance with the IBM requirements for fault protection, flagging, and power up/power down protection for the bus make this an ideal line driver for party line operations.

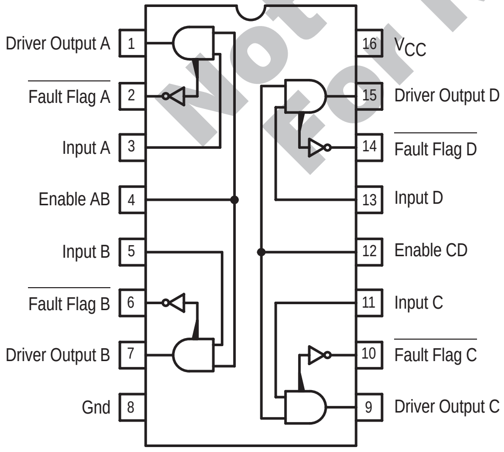
- Separate Enable and Fault Flags – MC3481
- Common Enable and Fault Flag – MC3485
- Power Up/Down Does Not Disturb Bus
- Schottky Circuitry for High–Speed – PNP Inputs
- Internal Bootstraps for Faster Rise Times
- Driver Output Current Foldback Protection
- MC3485 has LS Totem Pole Driver Output



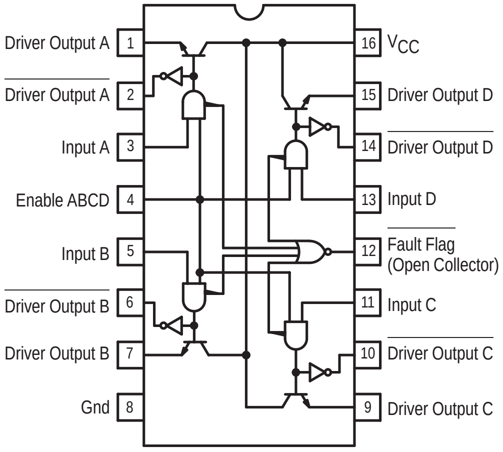
P SUFFIX
PLASTIC PACKAGE
CASE 648

PIN CONNECTIONS

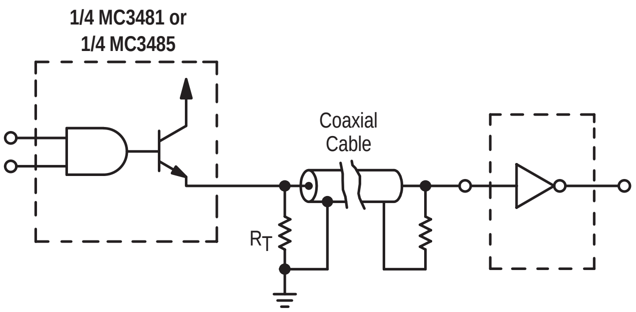
MC3481: Dual Enable Individual Fault Flag



MC3485: Common Enable Common Fault Flag



Simplified Application



ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC3481P	T_A = 0 to +70°C	Plastic DIP
MC3485P		

MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	+ 7.0	V
Input Voltage	V_I	10	V
Driver Output Voltage	V_O	5.5	V
Power Dissipation (Package Limitation) Derate Above T_A = 25°C	P_D $1/R_{\theta JA}$	962 7.7	mW mW°C
Operating Ambient Temperature Range	T_A	0 to + 70	°C
Junction Temperature	T_J	+ 150	°C
Storage Temperature Range	T_{stg}	65 to + 150	°C

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Min	Typ	Max	Unit
Power Supply Voltage	V_{CC}	4.5	5.0	5.95	Vdc
High Level Output Current	I_{OH}	–	–	59.3	mA
Operating Ambient Temperature Range	T_A	0	–	+ 70	°C

SWITCHING CHARACTERISTICS (See Note 1. Unless otherwise noted, these specifications apply over recommended temperature range. I/O Driver characteristics are guaranteed for V_{CC} = 5.0 V ± 10 % and Select–Out Driver characteristics are guaranteed for V_{CC} = 5.25 to 5.95 V. Typical values measured at T_A = 25 °C and V_{CC} = 5.0 V. See Tables 1 and 2, Figures 1 and 2 for load conditions.)

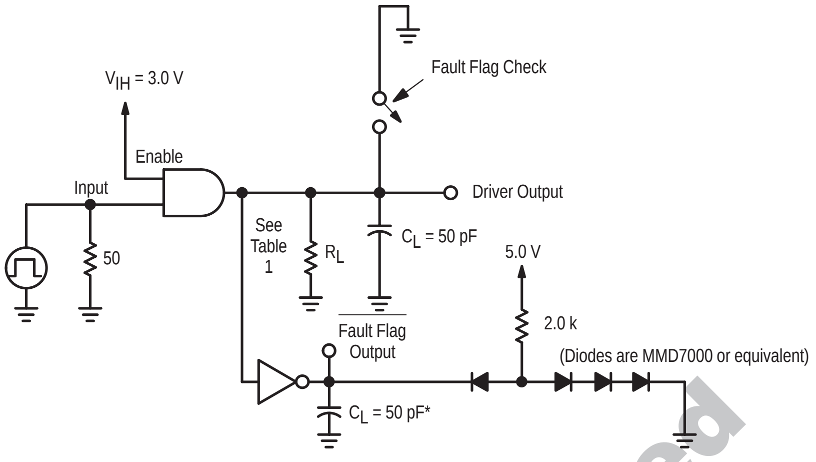
Characteristics	Symbol	Min	Typ	Max	Unit
Propagation Delay Time					ns
High–to–Low–Level, Driver Output					
As I/O Driver	$t_{PHL(D)}$	–	18	–	
As Select–Out Driver	$t_{PHL(DS)}$	–	19	–	
Low–to–High–Level, Driver Output					
As I/O Driver	$t_{PLH(\overline{D})}$	–	20	–	
As Select–Out Driver	$t_{PLH(\overline{D}S)}$	–	21	–	
High–to–Low–Level, Driver Output					
As I/O Driver	$t_{PHL(\overline{D})}$	–	25	–	
As Select–Out Driver	$t_{PHL(\overline{D}S)}$	–	26	–	
Low–to–High–Level, Driver Output					
As I/O Driver	$t_{PLH(\overline{D})}$	–	25	–	
As Select–Out Driver	$t_{PLH(\overline{D}S)}$	–	26	–	
High–to–Low–Level, Fault Flag – MC3481					
As I/O Driver	$t_{PHL(\overline{F})}$	–	45	–	
As Select–Out Driver	$t_{PHL(\overline{F}S)}$	–	47	–	
Low–to–High–Level, Fault Flag – MC3481					
As I/O Driver	$t_{PLH(\overline{F})}$	–	40	–	
As Select–Out Driver	$t_{PLH(\overline{F}S)}$	–	42	–	
Ratio of Propagation Delay Times As I/O Driver	$\frac{t_{PLH(D)}}{t_{PHL(D)}}$	–	1.0	–	

NOTES: 1. Reference IBM specification GA22–6974–3 for test terminology.
2. The fault protection circuitry of the MC3481 and MC3485 requires relatively clean input voltage waveforms for current operation. Noise pulses which enter the threshold region (0.8 to 2.0 V) may cause the output to enter the fault protect mode. To exit the protect mode, it is necessary to gate an input of the effected driver to the low logic state.

ELECTRICAL CHARACTERISTICS (Unless otherwise noted, these specifications apply over recommended power supply and temperature ratings. Typical values measured at T_A = 25°C and V_{CC} = +5.0 V)

Characteristic	Symbol	MC3481			MC3485			Unit
		Min	Typ	Max	Min	Typ	Max	
High–Level Input Voltage Note 2	V_{IH}	2.0	–	–	2.0	–	–	V
Low–Level Input Voltage Note 2	V_{IL}	–	–	0.8	–	–	0.8	V
High–Level Input Current	I_{IH}							µA
(V_{CC} = 4.5 V, V_{IH} = 2.7 V) – Input		–	–	20	–	–	20	
Enable		–	–	40	–	–	80	
(V_{CC} = 4.5 V, V_{IH} = 5.5 V) – Input		–	–	100	–	–	100	
Enable		–	–	200	–	–	400	
Low–Level Input Current	I_{IL}							µA
(V_{CC} = 5.95 V, V_{IL} = 0.4 V) – Input		–	–	–250	–	–	– 250	
Enable		–	–	–500	–	–	– 1000	
Input Clamp Voltage	V_{IC}							V
(I_{IC} = –18 mA)		–	–	–1.5	–	–	– 1.5	
High–Level Driver Output Voltage								V
(V_{CC} = 4.5 V, V_{IH} = 2.0 V, I_{OH} = – 59.3 mA)	$V_{OH(D)}$	3.11	3.6	–	3.11	3.6	–	
(V_{CC} = 5.25 V, V_{IH} = 2.0 V, I_{OH} = –41 mA)	$V_{OH(DS)}$	3.9	–	–	3.9	–	–	
Low–Level Driver Output Voltage								V
(V_{CC} = 5.5 V, V_{IL} = 0.8 V, I_{OL} = –240 µA)	$V_{OL(D)}$	–	–	+ 0.15	–	–	+ 0.15	
(V_{CC} = 5.95 V, V_{IL} = 0.8 V, I_{OL} = –1.0 mA)	$V_{OL(DS)}$	–	–	+ 0.15	–	–	+ 0.15	
Driver Output Short Circuit Current								mA
(V_{CC} = 5.5 V, V_{IH} = 2.0 V, V_{OS} = 0 V)	$I_{OS(D)}$	–	–	–5.0	–	–	– 5.0	
(V_{CC} = 5.95 V, V_{IH} = 2.0 V, V_{OS} = 0 V)	$I_{OS(DS)}$	–	–	–5.0	–	–	– 5.0	
Driver Output Reverse Leakage Current								µA
(V_{CC} = 4.5 V, V_{IL} = 0 V, V_O = 3.11 V)	I_{OR1}	–	–	+100	–	–	+ 100	
(V_{CC} = 0 V, V_{IL} = 0 V, V_O = 3.11 V)	I_{OR2}	–	–	+200	–	–	+ 200	
High–Level $\overline{\text{Driver Output}}$ Voltage (V_{CC} = 4.5 V, V_{IL} = 0.8 V, I_{OH} = –400 µA)	$V_{OH(\overline{D})}$	–	–	–	2.5	3.0	–	V
Low–Level $\overline{\text{Driver Output}}$ Voltage (V_{CC} = 4.5 V, V_{IH} = 2.0 V, I_{OL} = 8.0 mA)	$V_{OL(\overline{D})}$	–	–	–	–	–	0.5	V
$\overline{\text{Driver Output}}$ Short Circuit Current								mA
(V_{CC} = 5.5 V, V_{OS} =0 V, only one output shorted at a time)	$I_{OS(\overline{D})}$	–	–	–	–15	– 60	–100 –110	
(V_{CC} = 5.95 V, V_{OS} =0 V, only one ouput shorted at a time)	$I_{OS(\overline{DS})}$	–	–	–	–15	–		
High–Level $\overline{\text{Fault Flag}}$ Output Voltage (V_{CC} = 4.5 V, I_{OH} = –400 µA)	$V_{OH(\overline{F})}$	2 5	3.0	–	–	–	–	V
Low–Level $\overline{\text{Fault Flag}}$ Output Voltage (V_{CC} = 4.5 V, V_{IH} = 2.0 V, I_{OL} = 8.0 mA, Driver Output shorted to Ground	$V_{OL(\overline{F})}$	–	–	0.5	–	–	0.5	V
$\overline{\text{Fault Flag}}$ Output Short Circuit Current								mA
(V_{CC} = 5.5 V, V_{OS} =0 V, only one output shorted at a time)	$I_{OS(\overline{F})}$	– 15	–	–100	–	–	–	
(V_{CC} = 5.95 V, V_{OS} =0 V, only one output shorted at a time)	$I_{OS(\overline{FS})}$	– 15	–	–110	–	–	–	
High–Level $\overline{\text{Fault Flag}}$ Output Current (V_{CC} = 5.95 V, V_{OH} = 5.95 V)	$I_{OH(\overline{F})}$	–	–	–	–	–	+100	µA
High–Level Power Supply Current								mA
(V_{CC} = 5.5 V, V_{IH} = 2.0 V, no output loading)	I_{CCH}	–	50	70	–	55	75	
(V_{CC} = 5.95 V, V_{IH} = 2.0 V, no output loading)	I_{CCHS}	–	–	80	–	–	85	
Low–Level Power Supply Current								mA
(V_{CC} = 5.5 V, V_{IL} = 0.8 V, no output loading)	I_{CCL}	–	35	55	–	35	55	
(V_{CC} = 5.95 V, V_{IL} = 0.8 V, no output loading)	I_{CCLS}	–	–	70	–	–	70	

Figure 1. MC3481 AC Test Circuit and Waveforms



* Load Capacitance shown includes
Fixture and Probe Capacitance

Table	Driver Application	
1	I/O	Select–Out
V_{OH}	3.11 V	3.9 V
Input Frequency	5 MHz	1 MHz
Input Pulse Width	100 ns	500 ns
Input Amplitude	0 V to 4 V	0 V to 4 V
Input t_{TLH}	⩽6 ns	⩽6 ns
Input t_{THL}	⩽6 ns	⩽6 ns
Load Resistance (R_L)	50	90

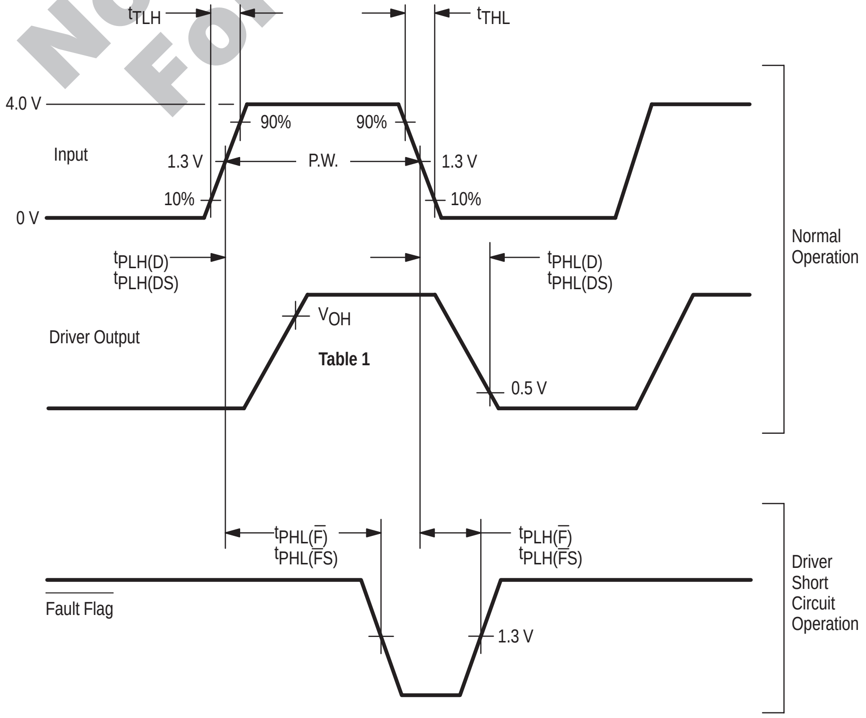
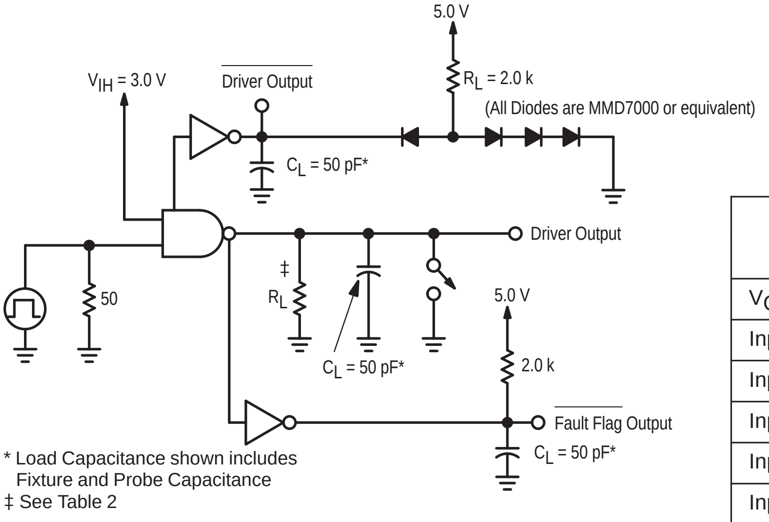
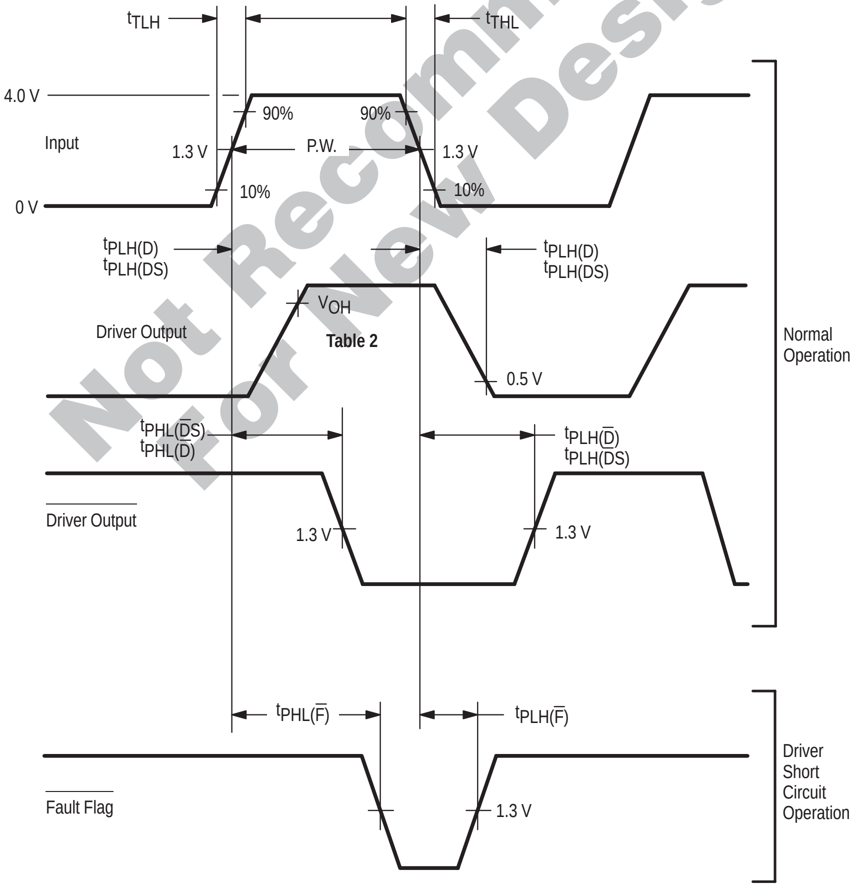


Figure 2. MC3485 AC Test Circuit and Waveforms



* Load Capacitance shown includes Fixture and Probe Capacitance
‡ See Table 2

Table 2	Driver Application	
	I/O	Select–Out
V_{OH}	3.11 V	3.9 V
Input Frequency	5 MHz	1 MHz
Input Pulse Width	100 ns	500 ns
Input Amplitude	0 V to 4 V	0 V to 4 V
Input t_{TLH}	≤6 ns	≤6 ns
Input t_{THL}	≤6 ns	≤6 ns
Load Resistance (R_L)	50	90



MOTOROLA

MC3488A

Dual EIA-423/EIA-232D Line Driver

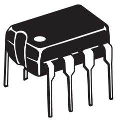
The MC3488A dual is single–ended line driver has been designed to satisfy the requirements of EIA standards EIA–423 and EIA–232D, as well as CCITT X.26, X.28 and Federal Standard FIDS1030. It is suitable for use where signal wave shaping is desired and the output load resistance is greater than 450 ohms. Output slew rates are adjustable from 1.0 µs to 100 µs by a single external resistor. Output level and slew rate are insensitive to power supply variations. Input undershoot diodes limit transients below ground and output current limiting is provided in both output states.

The MC3488A has a standard 1.5 V input logic threshold for TTL or NMOS compatibility.

- PNP Buffered Inputs to Minimize Input Loading
- Short Circuit Protection
- Adjustable Slew Rate Limiting
- MC3488A Equivalent to 9636A
- Output Levels and Slew Rates are Insensitive to Power Supply Voltages
- No External Blocking Diode Required for V_{EE} Supply
- Second Source µA9636A

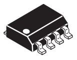
DUAL EIA–423/EIA–232D DRIVER

SEMICONDUCTOR TECHNICAL DATA

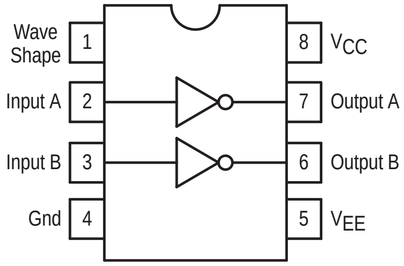


P1 SUFFIX
PLASTIC PACKAGE
CASE 626

D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)



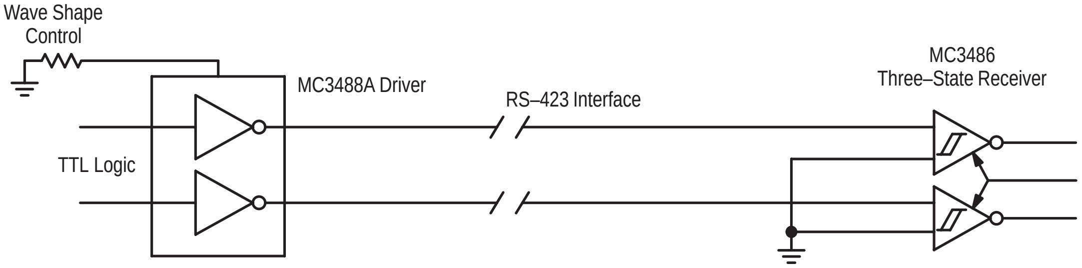
PIN CONNECTIONS



ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC3488AP1	T_A = 0 to +70°C	Plastic DIP
MC3488AD		SO–8

Simplified Application



MAXIMUM RATINGS (Note 1)

Rating	Symbol	Value	Unit
Power Supply Voltages	V_{CC} V_{EE}	+ 15 – 15	V
Output Current Source Sink	 I_{O} + I_{O} –	 + 150 – 150	mA
Operating Ambient Temperature	T_A	0 to + 70	°C
Junction Temperature Range	T_J	150	°C
Storage Temperature Range	T_{stg}	– 65 to + 150	°C

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Min	Typ	Max	Unit
Power Supply Voltages	V_{CC} V_{EE}	10.8 – 13.2	12 – 12	13.2 – 10.8	V
Operating Temperature Range	T_A	0	25	70	°C
Wave Shaping Resistor	R_{WS}	10	–	1000	kΩ

TARGET ELECTRICAL CHARACTERISTICS (Unless otherwise noted, specifications apply over recommended operating conditions)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Voltage – Low Logic State	V_{IL}	–	–	0.8	V
Input Voltage – High Logic State	V_{IH}	2.0	–	–	V
Input Current – Low Logic State (V_{IL} = 0.4 V)	I_{IL}	– 80	–	–	µA
Input Current – High Logic State (V_{IH} = 2.4 V) (V_{IH} = 5.5 V)	 I_{IH1} I_{IH2}	 – –	 – –	 10 100	µA
Input Clamp Diode Voltage (I_{IK} = – 15 mA)	V_{IK}	– 1.5	–	–	V
Output Voltage – Low Logic State ($R_L = \infty$) EIA–423 (R_L= 3.0 kΩ) EIA–232D (R_L= 450 Ω) EIA–423	V_{OL}	 – 6.0 – 6.0 – 6.0	 – – –	 – 5.0 – 5.0 – 4.0	V
Output Voltage – High Logic State ($R_L = \infty$) EIA–423 (R_L.= 3.0 kΩ) EIA–232D (R_L = 450 Ω) EIA–423	V_{OH}	 5.0 5.0 4.0	 – – –	 6.0 6.0 6.0	V
Output Resistance ($R_L \geqslant$ 450 Ω)	R_O	–	25	50	Ω
Output Short–Circuit Current (Note 2) (V_{in} = V_{out} = 0 V) (V_{in} = $V_{IH(Min)}$, V_{out} = 0 V)	 I_{OSH} I_{OSL}	 – 150 + 15	 – –	 – 15 + 150	mA
Output Leakage Current (Note 3) (V_{CC} = V_{EE} = 0 V, – 6.0 V $\leqslant V_o \leqslant$ 6.0 V)	I_{ox}	– 100	–	100	µA
Power Supply Currents (R_W = 100 kΩ, $R_L = \infty$, $V_{IL} \leqslant V_{in} \leqslant V_{IH}$)	I_{CC} I_{EE}	– – 18	– –	+ 18 –	mA

NOTES: 1. Devices should not be operated at these values. The ″Electrical Characteristics″ provide conditions for actual device operation.
2. One output shorted at a time.
3. No V_{EE} diode required.

TRANSITION TIMES (Unless otherwise noted, C_L = 30 pF, f = 1.0 kHz, V_{CC} = – V_{EE} = 12.0 V ± 10%, T_A = 25°C, R_L = 450 Ω. Transition times measured 10% to 90% and 90% to 10%)

Characteristic	Symbol	Min	Typ	Max	Unit
Transition Time, Low–to–High State Output	t_{TLH}				µs
(R_W = 10 kΩ)		0.8	–	1.4	
(R_W = 100 kΩ)		8.0	–	14	
(R_W = 500 kΩ)		40	–	70	
(R_W = 1000 kΩ)		80	–	140	
Transition Time, High–to–Low State Output	t_{THL}				µs
(R_W = 10 kΩ)		0.8	–	1.4	
(R_W = 100 kΩ)		8.0	–	14	
(R_W = 500 kΩ)		40	–	70	
(R_W = 1000 kΩ)		80	–	140	

Figure 1. Test Circuit and Waveforms for Transition Times

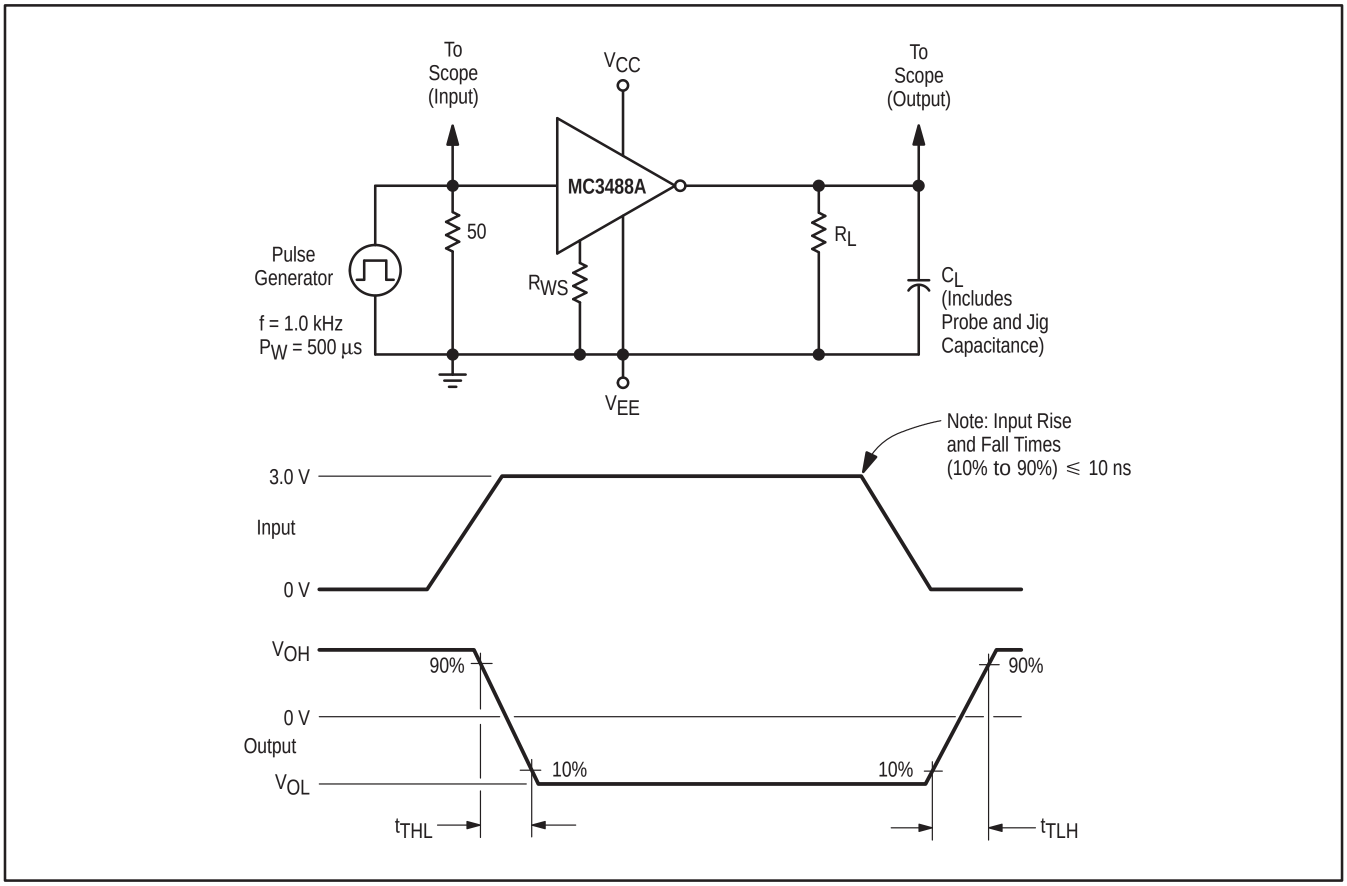


Figure 2. Output Transition Times versus Wave Shape Resistor Value

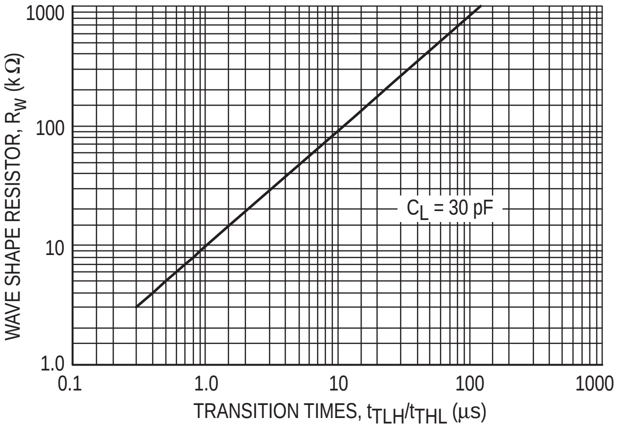


Figure 3. Input/Output Characteristics versus Temperature

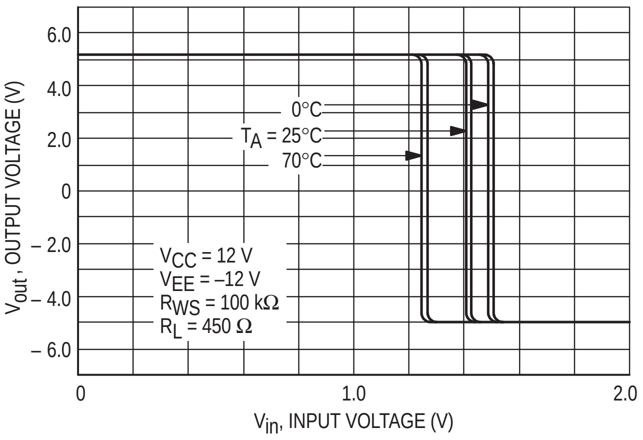
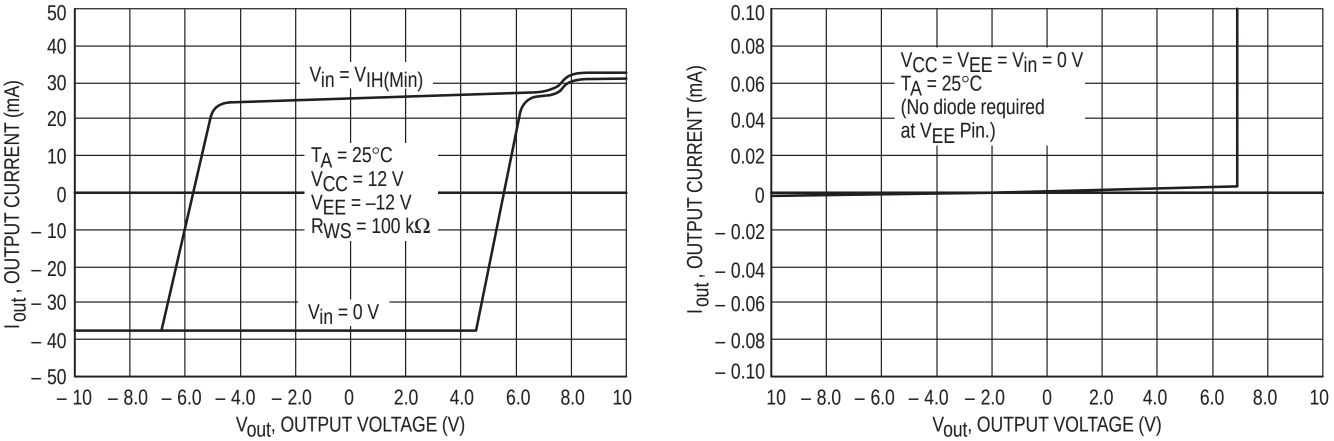


Figure 4. Output Current versus Output Voltage


Power–On

Power–Off

Figure 5. Supply Current versus Temperature

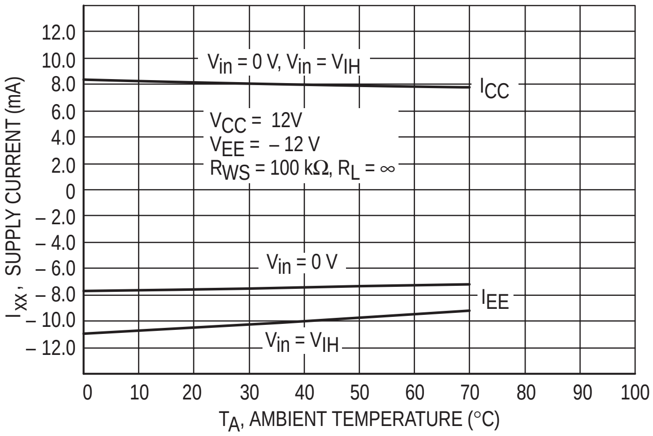
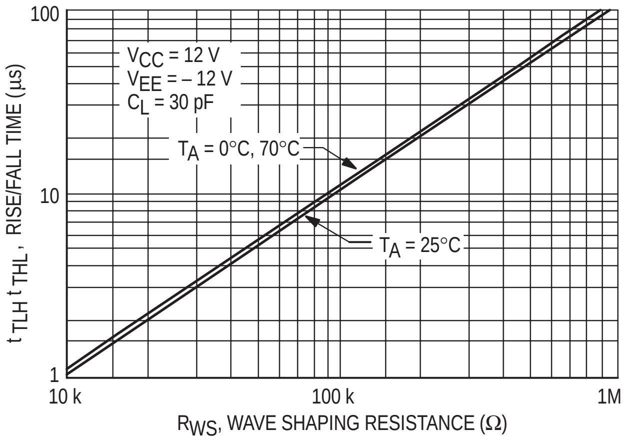


Figure 6. Rise/Fall Time versus R_{WS}



MOTOROLA

IEEE 802.3 10BASE-T Transceiver

The Motorola 10BASE–T transceiver, designed to comply with the ISO 8802–3 [IEEE 802.3] 10BASE–T specification, will support a Medium Dependent Interface (MDI) in an embedded Media Attachment Unit (MAU)*. The interface supporting the Data Terminal Equipment (DTE) is TTL, CMOS, and raised ECL compatible, and the interface to the Twisted Pair (TP) media is supported through standard 10BASE–T filters and transformers. Differential data intended for the TP media is provided a 50 ns pre–emphasis and data at the TP receiver is screened by Smart Squelch circuitry for specific threshold, pulse width, and sequence requirements.

Other features of the MC34055 include: Collision and Jabber detection status outputs, select mode pins for forcing Loop Back and Full–Duplex operation, a Signal Quality Error pin for testing the collision detect circuitry without affecting the TP output, and a LED driver for Link Integrity status. An on–chip oscillator, capable of receiving a clock input or operating under crystal control, is also provided for internal timing and driving a buffered clock output.

The MC34055 is manufactured on a BiCMOS process and is packaged in a 24 pin SOIC.

- BiCMOS Technology for Low Power Operation
- Standard 5.0 V, ± 5% Voltage Supply
- Smart Squelch Enforcement of Threshold, Pulse Width, and Sequence Requirements
- Driver Pre–Emphasis for Output Data
- TTL, CMOS and Raised ECL Compatible
- Interfaces to TP Media with Standard 10BASE–T Filters and Transformers
- LED Capable Status Outputs for Collision, Jabber Detection, and Link Integrity
- Directly Driven or Crystal Controlled Clock Oscillator
- Selectable Full–Duplex Operation
- Signal Quality Error Test Pin
- Selectable Loop Back

MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted.)

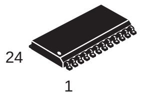
Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to 7.0	Vdc
Differential Voltage at RX+/RX–	V_{ID}	– 5.25 to 5.25	Vdc
Voltage Applied to Logic and Mode/Test Select Inputs		– 0.5 to 5.5	Vdc
Voltage Applied to Logic Outputs and Output Status Pins		– 0.5 to 7.0	Vdc
Ambient Operating Temperature Range	T_A	0 to 70	°C
Junction Temperature	T_J	– 65 to 150	°C

NOTE: Devices should not be operated at these limits. The “Recommended Operating Conditions” table provides for actual device operation.

MC34055

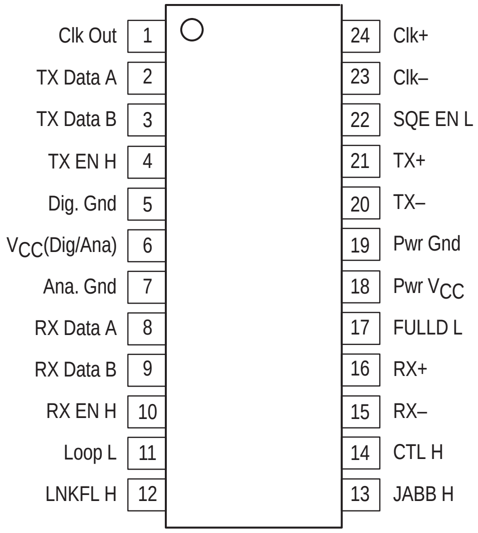
10BASE–T TRANSCEIVER

SEMICONDUCTOR
TECHNICAL DATA



DW SUFFIX
PLASTIC PACKAGE
CASE 751E
(SO–24L)

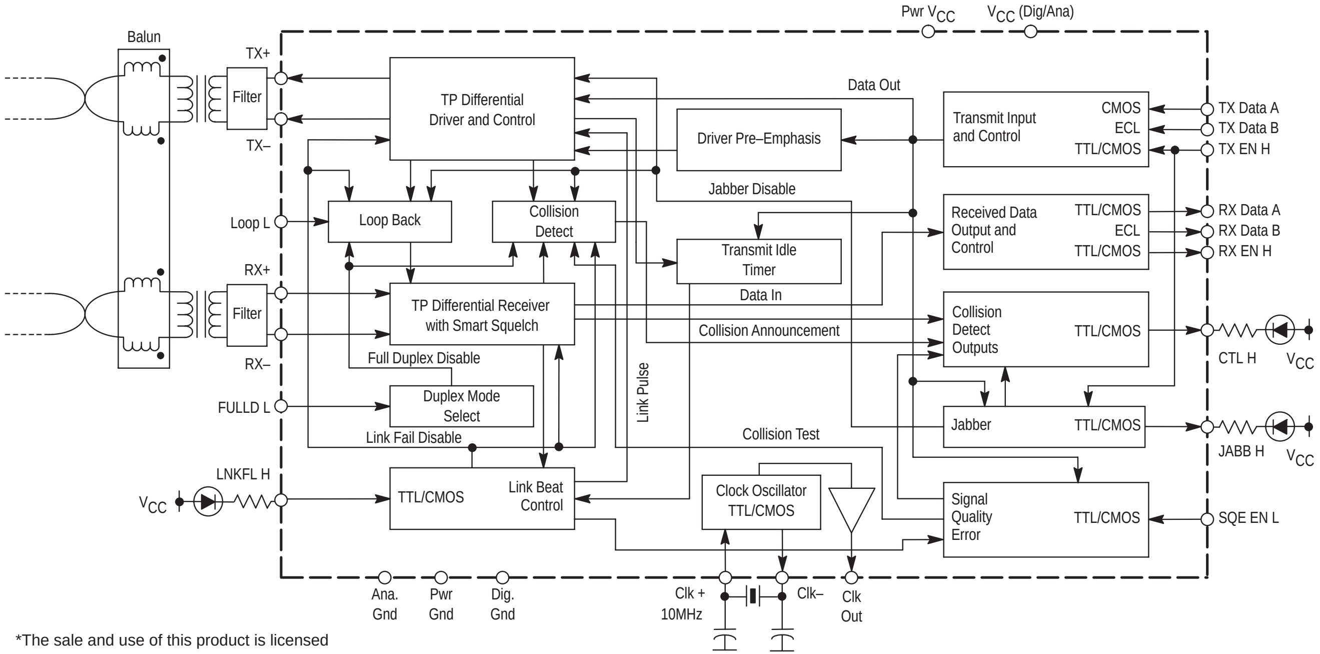
PIN CONNECTIONS



ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC34055DW	T_A = 0° to +70°C	SO–24L

Simplified Block Diagram



*The sale and use of this product is licensed under technology covered by one or more Digital Equipment Corporation patents.

This device contains 9,875 active transistors.

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Min	Typ	Max	Unit
Power Supply Voltage	V_{CC}	4.75	5.0	5.25	Vdc
Voltage Applied to Logic Inputs and Status Pins	–	0	–	5.25	Vdc
Differential Input Voltage	–	0.59	–	2.8	Vpp
Operating Ambient Temperature	T_A	0	–	70	°C

NOTE: All limits are not necessarily functional concurrently.

ELECTRICAL CHARACTERISTICS (0°C ≤ T_A ≤ 70°C, V_{CC} = 5.0 V, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Supply Current (4.75 V ≤ V_{CC} ≤ 5.25 V)	I_{CC}	–	60	180	mA
Reset Circuit Threshold	–	4.0	–	4.4	Vdc

TWISTED PAIR TRANSMITTER

Output Differential Voltage (See Load Circuits: Differential Load Circuit)	V_O				Vpp
Output Differential Voltage with Pre–Emphasis		2.2	2.53	2.8	
Output Differential Voltage		1.56	1.72	1.98	
Common Mode Driver Impedance	Z_{OCM}	6.0	8.5	14	Ω
Transmitter Differential Output Impedance	Z_{OD}	8.0	15.5	29	Ω

TX DATA A

Input High Voltage (I_{IH} = + 20 µA)	V_{IH}	3.15	–	5.25	Vdc
Input Low Voltage (I_{IL} = –150 µA)	V_{IL}	0	–	0.8	

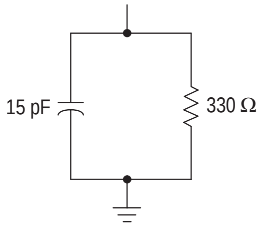
TX DATA B

Input Voltage (See Load Circuits: ECL Load Circuit)				Vdc
High: @ 0°C	V_{IH}	0.984 V_{CC} – 0.923	0.984 V_{CC} – 0.763	
@ 25°C		0.984 V_{CC} – 0.877	0.984 V_{CC} – 0.727	
@ 70°C		0.984 V_{CC} – 0.825	0.984 V_{CC} – 0.644	
Low: @ 0°C	V_{IL}	0.750 V_{CC} – 0.568	0.750 V_{CC} – 0.361	
@ 25°C		0.750 V_{CC} – 0.550	0.750 V_{CC} – 0.350	
@ 70°C		0.750 V_{CC} – 0.531	0.750 V_{CC} – 0.324	

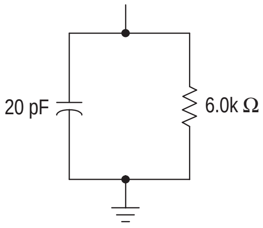
ELECTRICAL CHARACTERISTICS (0°C ≤ T_A ≤ 70°C, V_{CC} = 5.0 V, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
TX EN H					
Input High Voltage (I_{IH} = 200 μA)	V_{IH}	2.0	–	5.0	Vdc
Input Low Voltage (I_{IL} = – 20 μA)	V_{IL}	0	–	0.8	
RX DATA A/RX EN H/JABB H/CTL H					
Output Voltage (See Load Circuits: CMOS Load Circuit)					Vdc
High (I_{OH} = –12 mA)	V_{OH}	3.7	–	–	
Low (I_{OL} = +16 mA)	V_{OL}	–	–	0.5	
RX DATA B					
Output Voltage (See Load Circuits: ECL Load Circuit)					Vdc
High: @ 0°C	V_{OH}	0.984 V_{CC} – 0.923		0.984 V_{CC} – 0.763	
@ 25°C		0.984 V_{CC} – 0.877		0.984 V_{CC} – 0.727	
@ 70°C		0.984 V_{CC} – 0.825		0.984 V_{CC} – 0.644	
Low: @ 0°C	V_{OL}	0.750 V_{CC} – 0.568		0.750 V_{CC} – 0.361	
@ 25°C		0.750 V_{CC} – 0.550		0.750 V_{CC} – 0.350	
@ 70°C		0.750 V_{CC} – 0.531		0.750 V_{CC} – 0.324	
SIGNAL QUALITY ERROR TEST ENABLE CONTROL (SQE EN L)					
Test Control Voltage					Vdc
Test Disabled (Input High Voltage)(I_{IH} = + 20 μA Max.)	V_{IH}	2.0	–	5.0	
Test Enabled (Input Low Voltage)(– 50 μA < I_{IL} < –150 μA)	V_{IL}	0	–	0.8	
FULL DUPLEX MODE SELECT (FULLD L)					
Mode Select Control Voltage					Vdc
Normal Operation (Input High)(I_{IH} = + 20 μA)	V_{IH}	2.0	–	5.0	
Full Duplex (Input Low)(– 50 μA < I_{IH} < –150 μA)	V_{IL}	0	–	0.8	
LOOPBACK TEST MODE FUNCTION (LOOP L)					
Test Control Voltage					Vdc
Test Disabled (Input High)(I_{IH} = + 20 μA)	V_{IH}	2.0	–	5.0	
Test Enabled (Input Low)(I_{IL} = – 200 μA)	V_{IL}	0	–	0.8	
LINK FAIL STATUS (LINKFL H)					
Status Output Voltage (See Load Circuits: CMOS Load Circuit)					
Maximum Voltage for Output Low Condition (I_{OL} = 20 mA)	V_{OH}	–	–	0.5	Vdc
Output Low Sink Current	V_{OL}	–	–	20	mA
CLOCK OSCILLATOR					
Clk+ Input Logic Threshold					
High Level Input Voltage (I_{IH} = +100 μA Max.)	V_{IH}	2.0	–	5.0	Vdc
Logic Low Input Voltage (I_{IL} = –100 μA Max.)	V_{IL}	–	–	0.8	μA
Clk Out Output Voltage (See Load Circuits: CMOS Load Circuit)					Vdc
Logic High (I_{OH} = –12 mA)	V_{OH}	3.7	3.9	–	
Logic Low (I_{out} = +16 μA)	V_{OL}	–	0.25	0.5	

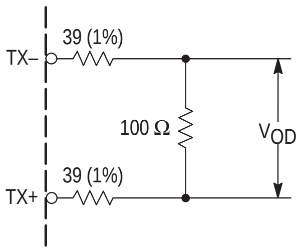
Output Load Circuits



ECL Load Circuit



TTL/CMOS Load Circuit



Differential Load Circuit

TIMING CHARACTERISTICS ($0°C \le T_A \le 70°C$)

Characteristic	Symbol	Min	Typ	Max	Unit
TRANSMIT START TIMING					
TX EN H to TX+/TX– Enable Time	t_{TXEN}	–	–	75	ns
TX Data A/B to TX+/TX– Enable Time	t_{FDXD}	–	–	75	ns
Steady State Propagation Delay of TX Data A/B to TX+/TX– Output	t_{TXSS}	–	–	75	ns
Pre–Emphasis Pulse Width	t_{PRCM}	45	–	55	ns
Transmitter Caused Edge Skew Between TX+ and TX–	$t_{Skew\ T}$	–	–	2.0	ns
Transmitter Added Edge Jitter to TX+/TX– from TX Data A/B	$t_{Jitter\ T}$	–	–	4.0	ns
Steady–State Delay between the TX Data A/B Input to the RX Data A/B Outputs for Normal Operation	t_{TXRX}	–	–	50	ns
TX EN H Assert to RX EN H Assert Under Normal Operation	t_{DREL}	–	–	50	ns
TRANSMIT STOP TIMING					
Delay between TX EN H Low and TX+/TX– High	t_{TXDH}	–	–	75	ns
TX EN H Assert/De–assert Delay from TX EN H to RX EN H Assert/De–assert	t_{XTRE}	–	–	400	ns
End of Packet Hold Time from Last TX Data A/B Edge or TX EN H De–assert	t_{TDDC}	250	–	–	ns
LINK BEAT PULSES					
Output Link Test Pulse Width	t_{LKPW}	80	–	120	ns
Minimum Link Beat Pulse Duration on RX+/RX–	t_{LDCY_A}	80	–	192	ns
LOOP BACK MODE TIMING					
Delay from Loop L Deassertion to RX EN H Driven from TX EN H Status	t_{LTRA}	–	–	30	ns
TX EN H Assert/De–assert to RX EN H, Assert/De–assert when in Loop–Back Mode and Receiver Inactive	t_{LTRX}	–	–	50	ns
Steady–State TX Data A/B to RX Data A/B when in Loop–Back Mode	t_{LTRD}	–	–	50	ns
SMART SQUELCH					
Interval Unit Squelch Deactivation	t_{SQ}	–	–	5.0	Bit Times
RECEIVE START TIMING					
Receiver–Added Edge Skew to RX Data A/B Signal	$t_{Skew\ R}$	–	–	1.5	ns
Receiver–Added Edge Jitter to RX Data A/B Signal	$t_{Jitter\ R}$	–	–	1.5	ns
Start–Up Delay from RX+/RX– to RX Data A/B	t_{RXNE}	–	–	50	ns
Delay from RX EN H Assertion Until RX Data A/B Valid	t_{RARE}	–10	–	+10	ns
Steady–State Propagation Delay from RX+/RX– Data A/B	t_{RXSS}	–	–	50	ns
RECEIVE SHUTDOWN TIMING					
Last received Data Edge until the RX EN H Output forces low	t_{RXDE}	155	–	250	ns

Figure 1. Start Up and Steady State Transmit Timing

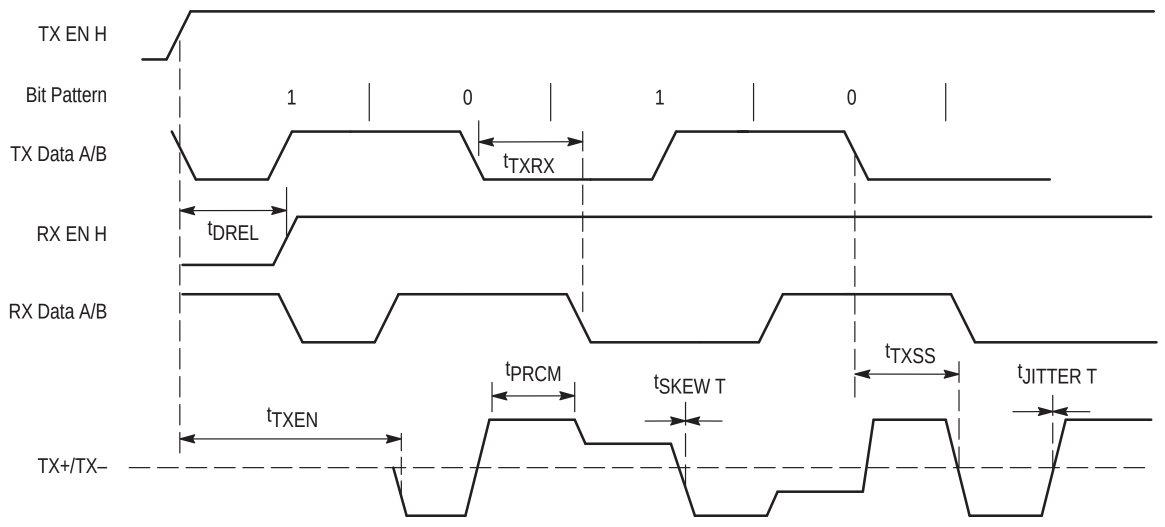


Figure 2. Driver Shutdown Timing

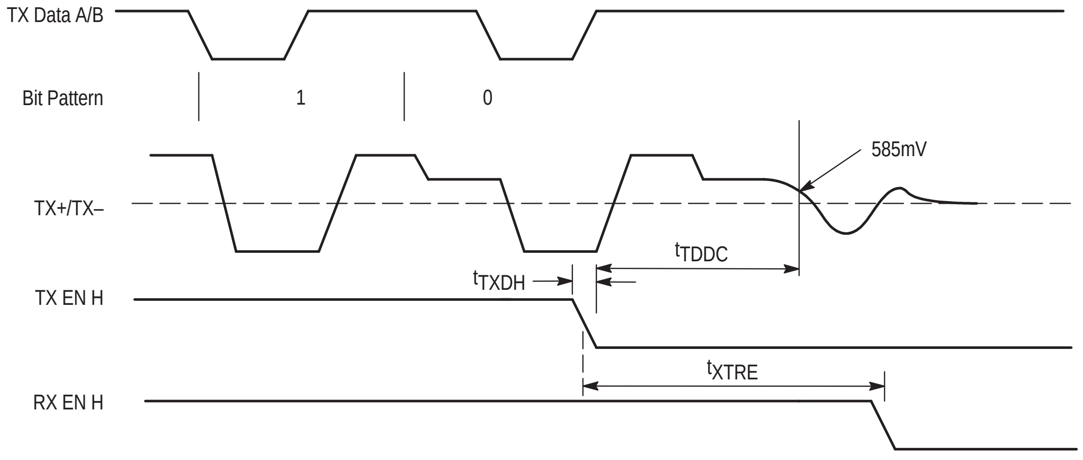


Figure 3. Link Pulse Timing

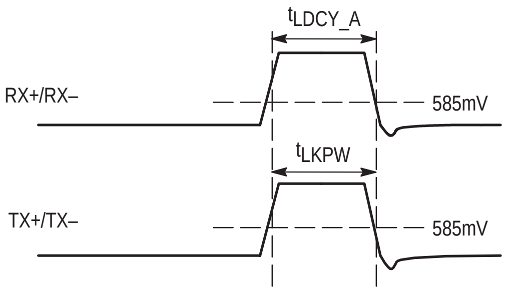


Figure 4. Loop Back Timing

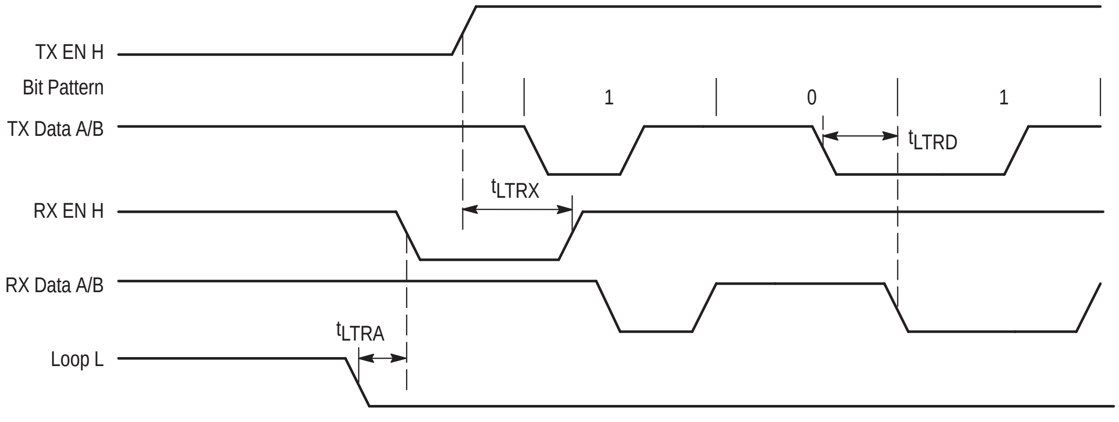


Figure 5. Receive Startup Timing

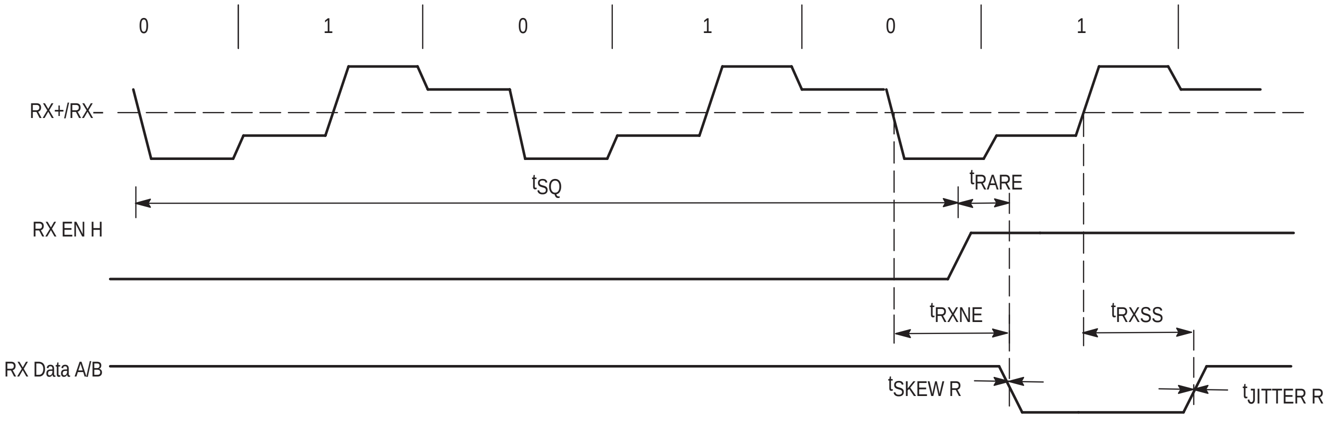
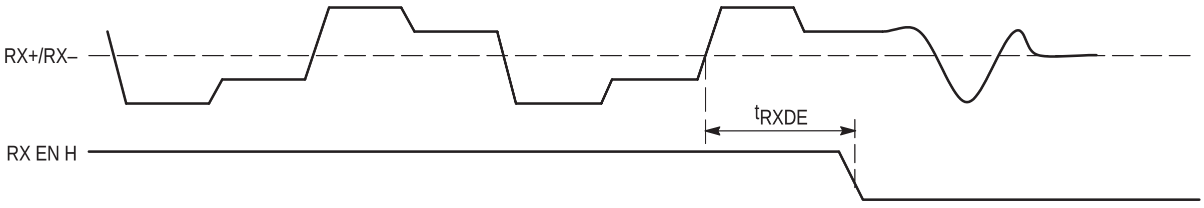


Figure 6. Receive Shutdown Timing



PIN FUNCTION DESCRIPTION

Pin	Symbol	Description
1	Clk Out	TTL/CMOS buffered 10 MHz clock output. This pin will source 400 µA and sink 16 mA.
2	TX Data A	CMOS transmit input pin. Data input at this pin is output to the TP media. The input will source less than 175 µA and sink less than 20 µA.
3	TX Data B	Raised ECL transmit input pin. Data input at this pin is output to the TP media. The input can source 40 µA for a high level input or 70 µA for a low level input.
4	TX EN H	TTL/CMOS transmit enable pin. Transmit is enabled when asserted high. The input will source less than 175 µA and sink less than 20 µA.
5	Dig. Gnd	Digital ground
6	V_{CC}(Dig/Ana)	Digital and analog V_{CC}. With the current consumed at this pin and Pin 18, the device will consume less than 180 mA at 5.0 Vdc.
7	Ana. Gnd	Analog ground
8	RX Data A	TTL/CMOS received data output pin. Data from the TP media is output at this pin. The output will source 12 mA and sink 16 mA.
9	RX Data B	Raised ECL received data output pin. Data from the TP media is output at this pin.
10	RX EN H	TTL/CMOS received data output enable pin. This pin is asserted after the Smart Squelch circuitry determines that there is valid data at the TP input pins and also when internal loop–back is occurring. The output will source 12 mA and sink 16 mA. The receive data outputs are forced high when this pin is low.
11	Loop L	TTL/CMOS Loopback test select. Asserting this pin causes the transmit data to be looped to the receive circuit while the TP transmit driver sends a link pulse. The input will source less than 175 µA and sink less than 20 µA.
12	LNKFL H	This pin is driven high to indicate a link fail state. When low, the pin will sink 20 mA to light an LED. An usquelched condition due to valid data on the receive circuit will cause the pin to transition high and low in 100 ms intervals.
13	JABB H	TTL/CMOS Jabber status pin. This pin is asserted when a Jabber condition is detected and will source 12 mA and sink 16 mA.
14	CTL H	TTL/CMOS status pin. This pin pulled high when Jabber or Collision conditions are detected. Also high for a time interval when a Signal Quality Error test is being performed. The pin will source 12 mA and sink 16 mA.
15	RX–	The inverting terminal of the TP differential receiver.
16	RX+	The noninverting terminal of the TP differential receiver.
17	FULLD L	TTL/CMOS duplex mode select. When low, this pin forces the device to operate in full–duplex mode. The input will source less than 175 µA and sink less than 20 µA.
18	Pwr V_{CC}	Power supply pin. With the current consumed at this pin and Pin 6, the device will consume less than 180 mA at 5.0 Vdc.
19	Pwr Gnd	Power ground pin.
20	TX–	The inverting terminal of the TP differential driver.
21	TX+	The noninverting terminal of the TP differential driver.
22	SQE EN L	TTL/CMOS Signal Quality Error test enable pin. Pulling this pin low allows test of the collision detect circuitry without affecting the twisted pair channel. The input will source less than 175 µA and sink less than 20 µA.
23	Clk–	TTL/CMOS clock oscillator pin. See Pin 24.
24	Clk+	TTL/CMOS clock oscillator pin. This pin is used with Pin 23 if the internal oscillator is to be free run with a crystal. The oscillator can also be directly driven with a TTL/CMOS clock signal at this pin. The oscillator frequency should be 10 MHz with a duty cycle of 50 ± 20%.

FUNCTIONAL DESCRIPTION

Introduction

The Motorola 10BASE–T transceiver, designed to comply with the ISO 8802–3[IEEE 802.3] 10BASE–T specification, will support one Medium Dependent Interface (MDI) through standard 10BASE–T filters and transformers. Although the device is capable of being used in embedded or external Medium Attachment Units (MAU), it was primarily designed for use in repeater or hub applications. For this reason a digital interface is provided rather than an AUI interface. This interface is TTL, CMOS, and raised ECL compatible and allows for easy connection in hub applications.

Other features of the MC34055 include: select mode pins of forcing Loop–Back and Full–Duplex operation; a Signal Quality Error pin for testing the collision detect circuitry without affecting the twisted pair output; and LED drivers for Link Integrity status; Collision detection; and Jabber detection. An on chip oscillator, capable of receiving a clock input or operating under crystal control, is also provided for internal timing and driving a buffered clock output.

Data Transmission

For data intended for the twisted pair, the MC34055 has two data inputs, TX Data A and TX Data B. TX Data A is CMOS compatible and TX Data B is raised ECL compatible. The inputs were not intended to be used simultaneously in a single application and are internally logically combined. The unused input should be disabled by connection to V_{CC}.

When data transmission is intended, the MC34055 detects the first falling edge of the Manchester encoded frame at the input being used, synchronizes the on chip oscillator (Pins 23 and 24) and asserts the twisted pair driver output to full differential amplitude within 25 ns if the driver enable pin (TX EN H) is previously asserted. Also, since twisted pair attenuates a 10 MHz signal more than a 5.0 MHz signal the 10BASE–T standard requires that data applied to the twisted pair receive pre–equalization. To fulfill this requirement the MC34055 provides an additional 730 mV for approximately 50 ns to output data. This is accomplished over the single pair of differential driver pins. TX+ and TX–, and effectively equalizes the power of all data components at the receiver. Figure 7A shows a 10 MHz waveform. Figure 7B shows the effect of pre–emphasis on a 5.0 MHz waveform. Manchester encoded data with the pattern shown in Figure 7A would represent a repeating pattern of zeros (000000...). Figure 7B would represent an alternating pattern of ones and zeros (0101010...).

Figure 7A. 10 MHz Waveform on Differential Outputs

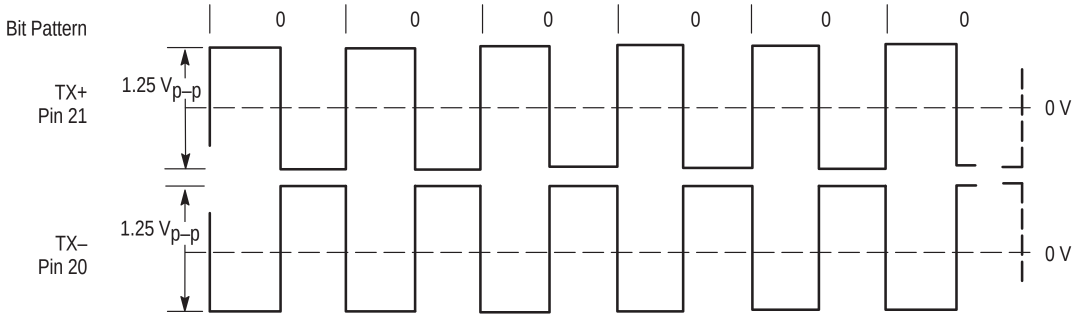
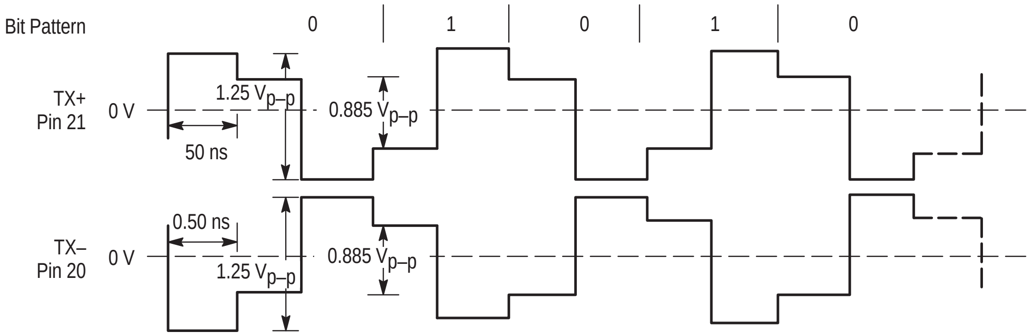


Figure 7B. 5.0 MHz Waveform on Differential Outputs



The figures show the voltage waveforms on the differential driver output pins. To actually meet the 10BASE–T specification requires bandpass filtering and a pulse transformer.

The output voltage waveform specifications of the IEEE 802.3 standard require that voltages impressed on the twisted pair meet a voltage template. The MC34055 can meet the voltage template for all the 10BASE–T applications by choosing the appropriate low pass filter and external components in the driver output circuitry. When the differential transmit driver output pins are configured to drive the bandpass filters and pulse transformer as shown in Figure 8, the resultant waveform is capable of meeting the voltage template.

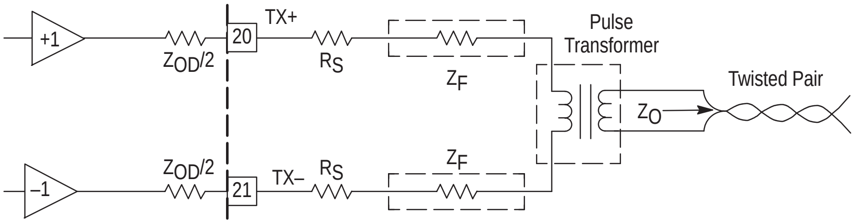
Following the end–of–frame activity, an internal pull–up resistor pulls TX Data A/B high and causes the differential driver to maintain full differential output voltage for approximately 250 ns. The differential driver interprets the lack of transition activity as an end of frame and starts an idle timer. Should another frame intended for the twisted pair arrive before the idle timer expires(~250 ns), the idle timer will be reset, if not, the transmit driver function will begin the decay to idle process. During idle periods the differential driver must force the media to a minimal differential voltage unless a link beat is being produced. The transition to minimal voltage is subject to performance requirements in the IEEE specification and is met by the MC34055 when the appropriate filters and transformers are used to interface to the media.

The MC34055 differential driver generates link pulses (beats) during idle periods. The link pulses produced are singular positive (TX+ positive with respect to TX–) pulses applied to the media at 16 ms intervals and last approximately 100 ns. The link pulses allow the receiver at the other end of the link to verify the validity of the segment. There is the possibility, due to the two asynchronous sources, that one of the two input pins (TX Data A or TX Data B) will receive frame activity immediately after a link pulse is initiated. In this event, the transmit differential driver will remain active for the entire frame interval and the link pulse will not affect more than one bit interval.

The MC34055 also has Jabber circuitry to detect and disable the twisted pair driver in the event that a serial controller fails constantly transmitting. Should any data source try to transmit longer than 20 ms minimum, the Jabber function will disable the differential driver outputs, the collision presence detector and the internal loopback function. Also, two status indicator pins, CTL H and JABB H are asserted. The MC34055 will remain in the jabber state until the TX EN H pin is pulled low or the jabbering input ceases to toggle for a minimum of 500 ms. The status indicator pins, CTL H and JABB H will also sink up to 20 mA and can therefore support external LEDs.

The driver also works with the receiver to provide loop–back. Under normal operating conditions (Loop L= “1”), the data applied to the TX Data A/B pins is looped back internally to the RX Data A/B pins. This function is disabled when there is a collision condition or FULLD L is low.

Figure 8. Differential Driver Media Interface Circuitry

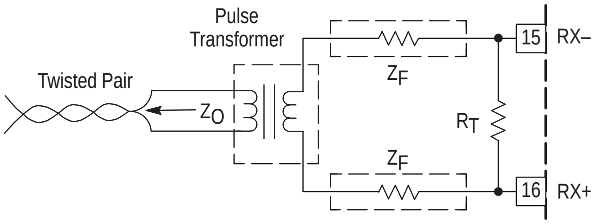


Where: Z_{OD} is the transmitters differential output impedance (~20 Ω),
R_S is a 1% series resistor,
Z_F is the filters impedance, and Z_O is the characteristic impedance of the twisted pair (100 Ω).

Data Reception

Data intended for the DTE proceeds from the twisted pair to the isolation transformer and bandpass filters before reaching the differential receiver terminals. Figure 9 shows the configuration of the external media receive circuitry. Once transitions at the receiver terminals (RX+ and RX–) are detected, the on–chip oscillator is synchronized and the received data is screened by smart squelch circuitry for validity. This qualification requires incoming data to meet amplitude and sequence requirements. If the data meets the Smart Squelch requirements, the receiver enters the unsquelch state and the data is forwarded to the RX Data A/B output pins provided Loop L is not low. Two data outputs are provided to increase design flexibility, RX Data A and RX Data B. RX Data A is CMOS/TTL compatible and RX Data B is raised ECL compatible.

Figure 9. Differential Receiver Media Interface Circuitry



Where: R_T is a terminating resistor (100 Ω), Z_F is the filters impedance, and Z_O is the characteristic impedance of the twisted pair (100 Ω).

The MC34055 powers up in a squelched and “link OK” state, after which minimum and maximum link test and maximum link fail timers are started. If valid data or a link pulse is received after the link test minimum timer but before the link fail maximum timer times out, the timers are reset and begin counting again. In the event of missing or incorrect link pulses, the MC34055 enters the link fail state whereby the LNKFL H status pin is asserted until valid data or link pulse activity appears at the receiver terminals.

Powering up in the squelched state assures that the data path to the data output pin (RX Data A/B) is disabled, and prevents noise at the receiver terminals (RX+/RX–), from being interpreted as valid input data. Once transitions appear at the receiver terminals, the smart squelch circuitry checks for the smart squelch requirements to unsquelch; an alternating sequence (1010... or 0101...) of pulses with amplitude of at least 525 mV. This requirement is met by the preamble of an IEEE 802.3 frame with good signal to noise ratio.

After a pulse is received and checked for proper polarity and amplitude, the pulse width is checked for proper duration. If the duration is to short or too long the smart squelch circuitry resets and begins to look again for a proper sequence. By requiring the differential pulses to meet amplitude and sequence requirements, it is unlikely that pulses due to crosstalk from coresident twisted pairs are capable of causing the receiver to unsquelch. If a positive pulse is received first and the differential driver is not transmitting, the receiver should unsquelch after three alternating pulses. If a negative pulse is received first, one additional pulse is required before unsquelch. If the differential driver is transmitting, three additional pulses are required to unsquelch.

After meeting the smart squelch requirements, the MC34055 will pull high the RX EN H pin and enable the path to the receive data pin (RX Data A/B) provided the MC34055 is not in the loop back test mode (Loop L low). If the receiver unsquelches, the receive enable pin remains high and the data path to the receive data pin remains enabled until transitions cease to exist at the receiver terminals. Valid data reception is also indicated by high/low transitions of the LNKFL H pin at 100 ms intervals. When transitions at the differential terminals cease, marking the end of frame activity, the receiver re–enters the squelch state, pulls low on the RX EN H pin, and begins accepting valid link pulses until the start of the next 802.3 frame.

If the MC34055 is requested to begin transmitting (TX EN H is asserted), and the receiver unsquelches simultaneously, there is a collision. Also, if the MC34055 driver enable pin is previously asserted and the receiver detects valid transition activity, the receiver Smart Squelch circuitry verifies the possibility of collision by requiring three extra transitions at the differential receiver before the unsquelch condition is reached. If unsquelch occurs, a collision condition exists. During all collision conditions the MC34055 asserts the CTL H status pin for the duration of the condition and for a time after the end of collision.

During a collision condition the receive and transmit paths are still both enabled allowing transparency to the media. Either the presence of simultaneous transmit and receive activity or the condition of the CTL H status pin can be used by the communications controller to acknowledge and react to the collision. In applications where a 10 MHz collision signal is required by an SIA, the combination of this status pin and the clock oscillator output can be logically combined to provide a 10 MHz output. If the DTE reacts to the collision and ceases transmitting, the MC34055 will decay to idle until a re–transmit is attempted.

Crystal Oscillator

The MC34055 has an on–chip clock oscillator used to provide a reliable and accurate time reference to all the internal timers. The oscillator can be run with a crystal or driven at Pin 24 from an external clock source. Also provided is a buffered clock output which is useful if the MC34055 is to be used in a repeater or concentrator application.

Table 1. The crystal used in the oscillator is subject to the following specifications.

Crystal Operating Mode	Fundamental
Crystal Cut Type	AT
Crystal External Shunt Capacitance	7.0 pF Max
Crystal Resonant Mode	Series
Crystal Accuracy	± 0.01% @ 25°C
Crystal Temperature Variance	0.005% from 0° to 70°C
Crystal Series Resistance	25 Ω Max, 17 Ω Typical
Crystal Operating Temperature Range	0° to 70°C

LOOP L Test Mode

If the Loop L pin is low, the MC34055 is in a test mode whereby the data at the input pin (TX Data A/B) is being looped back internally to the receive data pin(RX Data A/B). In this mode the data path from the differential receiver terminals to the receive data output pins (RX Data A/B) is disconnected while the Smart Squelch functionality of the differential receiver is still operational. This test mode allows the DTE to test the MC34055 internal loop back circuitry since the data is looped back to the receive circuitry as close to the twisted pair interface as possible.

Signal Quality Error Test

The MC34055 also provides the ability to test the collision detect circuitry without disabling either of the data paths. By pulling the SQE EN L pin low, a collision test is provided to the collision detect circuitry immediately following the last edge of a transmitted 802.3 frame. The test verifies the operability of the collision detect circuitry, operability is announced by the assertion of the CTL H pin for a period following a valid data transmission.

Jabber Detection

The transmit circuitry of the MC34055 has the ability to monitor and shut down the differential driver in the event of a jabber condition. If transmission activity ever exceeds 20 ms minimum, the differential driver, the collision detect, and internal loop back circuits are disabled. To announce the presence of a jabber condition, both the CTL H and the JABB H status output pins are asserted. In order to end the jabber condition, the TX Data A/B input must stop toggling, or the TX EN H pin must be pulled low for a minimum of 500 ms. The status output pins have the ability to drive an external led and were added to facilitize network manageability. The jabber status outputs will not assert during power up or power down.

Full Duplex Mode

The MC34055 can be operated in a full–duplex mode if required. When the FULLD L pin is pulled low the device will enter the full duplex mode. This mode allows the transmitter and driver to operate independently. Collision will not be announced and the internal loop back operation is disabled. The Signal Quality Error test, however, is still operational if enabled.

Status Pins

The MC34055 has three status indicator pins capable of sourcing or sinking enough current to support an external LED. Status pin levels (“1” or “0”) report the condition of the transceiver. Table 2 shows the combinations and significance.

Table 2

Status Pin			Condition
JABB H	**CTL H**	**LNKFL H**	
“0”	“1”	X	Collision condition or Signal Quality Error test.
“1”	“1”	X	Jabber condition
X	X	“0”	Link Failure. Incorrect or nonexistent link pulses, or lack of data at the receiver terminals.
X	X	“1”	Link “OK”. Receiving link pulses.
X	X	“0101…”	Link “OK”. Receiving valid data.

Test Select Pins

The MC34055 has three operation mode test select pins, Loop L, SQE EN L and FULLD L. The level of the pin determines the mode of operation. Table 3 shows the levels and corresponding conditions of the status pins.

Table 3

Pin	Status	Condition
Loop L	“1”	Normal operating mode. Loop back occurs when the transmitter initiates and the receiver is receiving link pulses. The RX EN H pin follows the TX EN H pin and the transmit data appears on the RX Data A/B output pin being used.
	“0”	Loop back test mode. The transmit circuit is looped back internally as close to the differential receive circuit as possible. In this mode the RX EN H pin follows the TX EN H pin and the transmit data appears on the RX Data A/B output pin being used. Any received data other than link pulses are ignored and the receiver will not unsquelch or announce collision.
SQE EN L	“0”	Normal operating mode. Concurrent transmit and receive activity results in a collision condition.
	“1”	Test enabled. An internal test is run on the collision circuitry and the CTL H pin is asserted for a time window following the last positive packet edge. Data transmission and reception is undisturbed.
FULLD L	“1”	Normal operating mode. Internal loop–back is operable and collision is announced.
	“0”	Internal loop–back is disabled and collision will not be announced. Signal Quality Error test is still operable.

APPLICATIONS INFORMATION

The MC34055 implements the physical layer of a 10BASE–T application of IEEE 802.3. It provides the physical connection to the media (twisted pair) and the services required by the MAC sublayer of the Data Link Layer. Two interfaces are defined in the IEEE 802.3 specification of the physical layer; one is the MDI providing connection to the twisted pair; and the other is the AUI providing connection to the encoder/decoder function of the Data Link Layer. While the MC34055 provides the connection to the twisted pair, a CMOS and raised ECL interface is provided instead of an AUI.

The MC34055 implements the twisted pair interface of the physical layer in a 802.3 10BASE–T application but circuitry must be added if an AUI is desired, (see Figure 10 for suggested schematic). For example, an external MAU application requires the AUI and a twisted pair interface. A chip capable of realizing the AUI interface is the Texas Instruments SN75ALS085. This IC has an AUI interface and another interface which is compatible with the MC34055. The differential input of the 75ALS085 can be used for the TX+/TX– terminals of the AUI. The differential drivers of the 75ASL085 can be used as the RX+/RX– and the COL+/COL– terminals of the AUI. The other interface of the 75ALS085 then will interface to the MC34055 by three paths shown in the application suggestion. The application accounts for all the inputs/outputs of an external MAU.

Embedded applications do not require a full AUI and a MC10116 can be used to interface between the raised ECL interfaces of the MC34055 and the AUI of existing encoder/decoder chips. The MC10116 is a MECL 10k Triple Line Receiver with typical propagation delay and rise and fall times (20% to 80%) of 2.0 ns. Figure 11 shows the use of the MC10116 with the MC34055 and the AMD 7992 SIA.

In a multi–port repeater, or hub, a port is required for each DTE connected to the IEEE 802.3 network. This port consists of two connections, one for the TX+/TX– pair and another for the RX+/RX– pair. The repeater unit then multiplexes these lines so that all of the stations are capable of transmitting to or receiving from all the other stations on the network. This establishes the need for a transceiver without an AUI interface. If an AUI is present with each 10BASE–T transceiver, chip count is increased because there is a requirement to convert from balanced to unbalanced lines before multiplexing.

An application suggestion for the use of the MC34055 used in a multiport repeater is shown in Figure 6. Here the receive and transmit lines for the 10BASE–T transceivers are multiplexed by the hub hardware.

Figure 10. External MAU Application

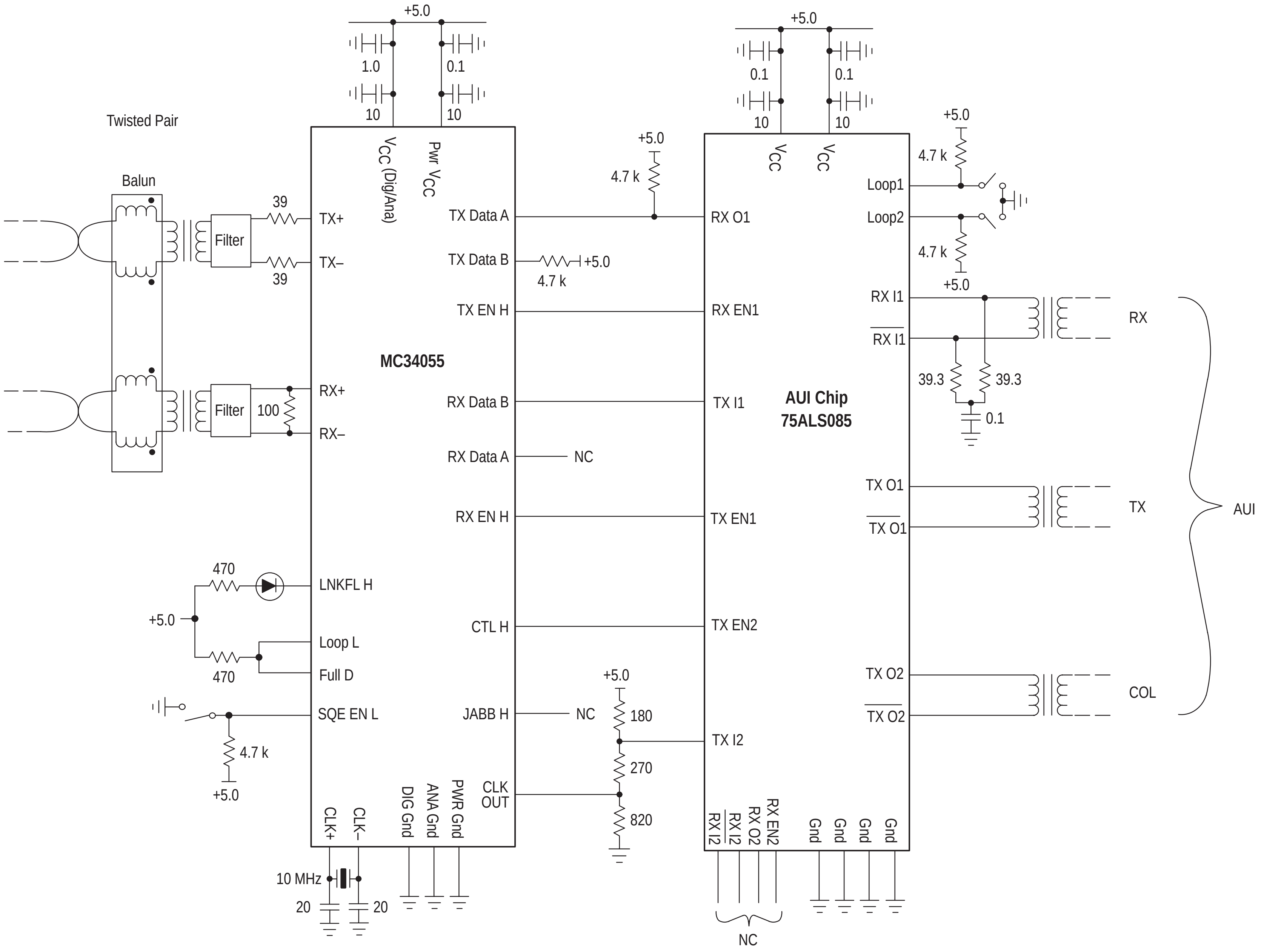


Figure 11. Internal MAU Application

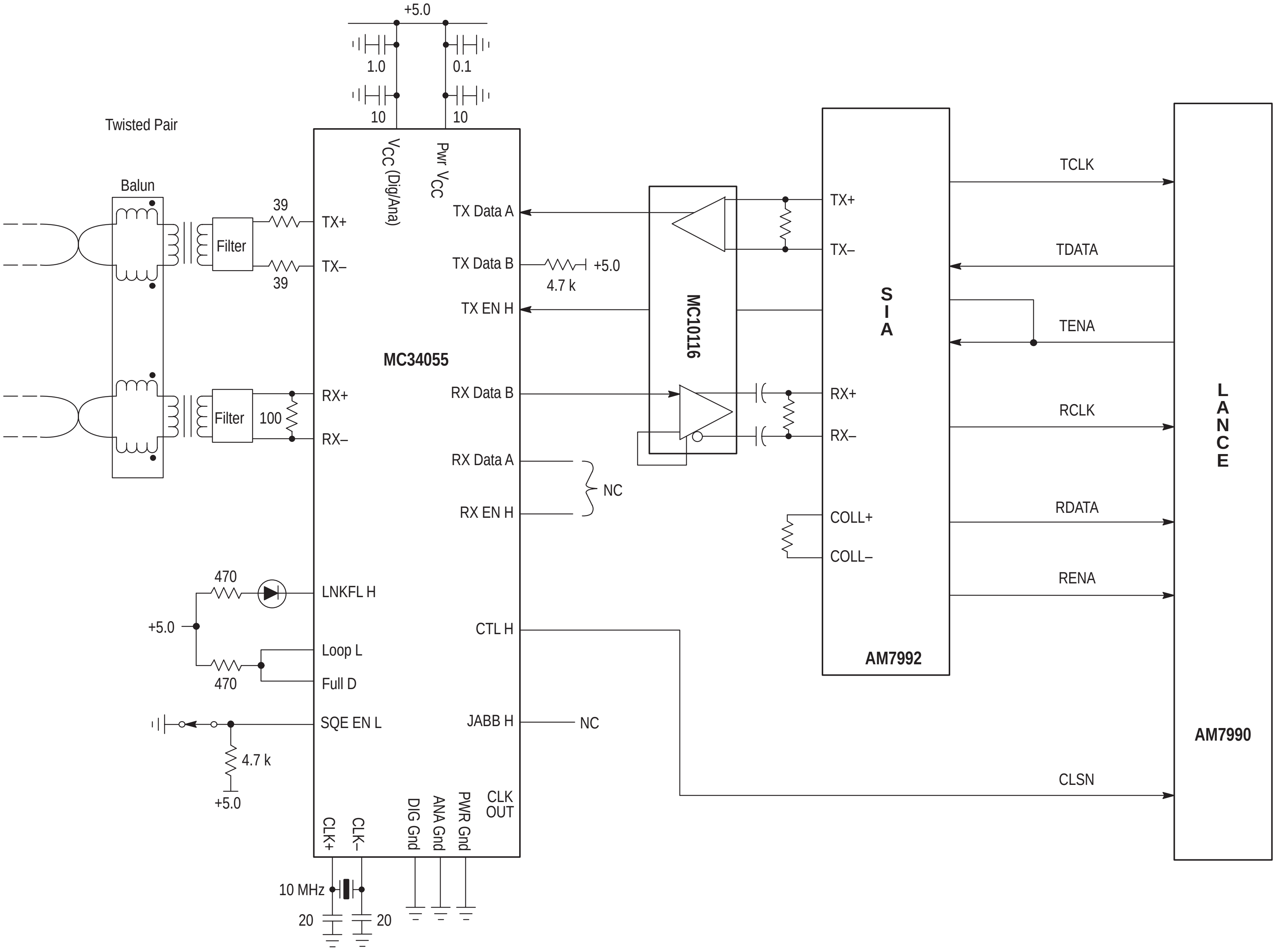
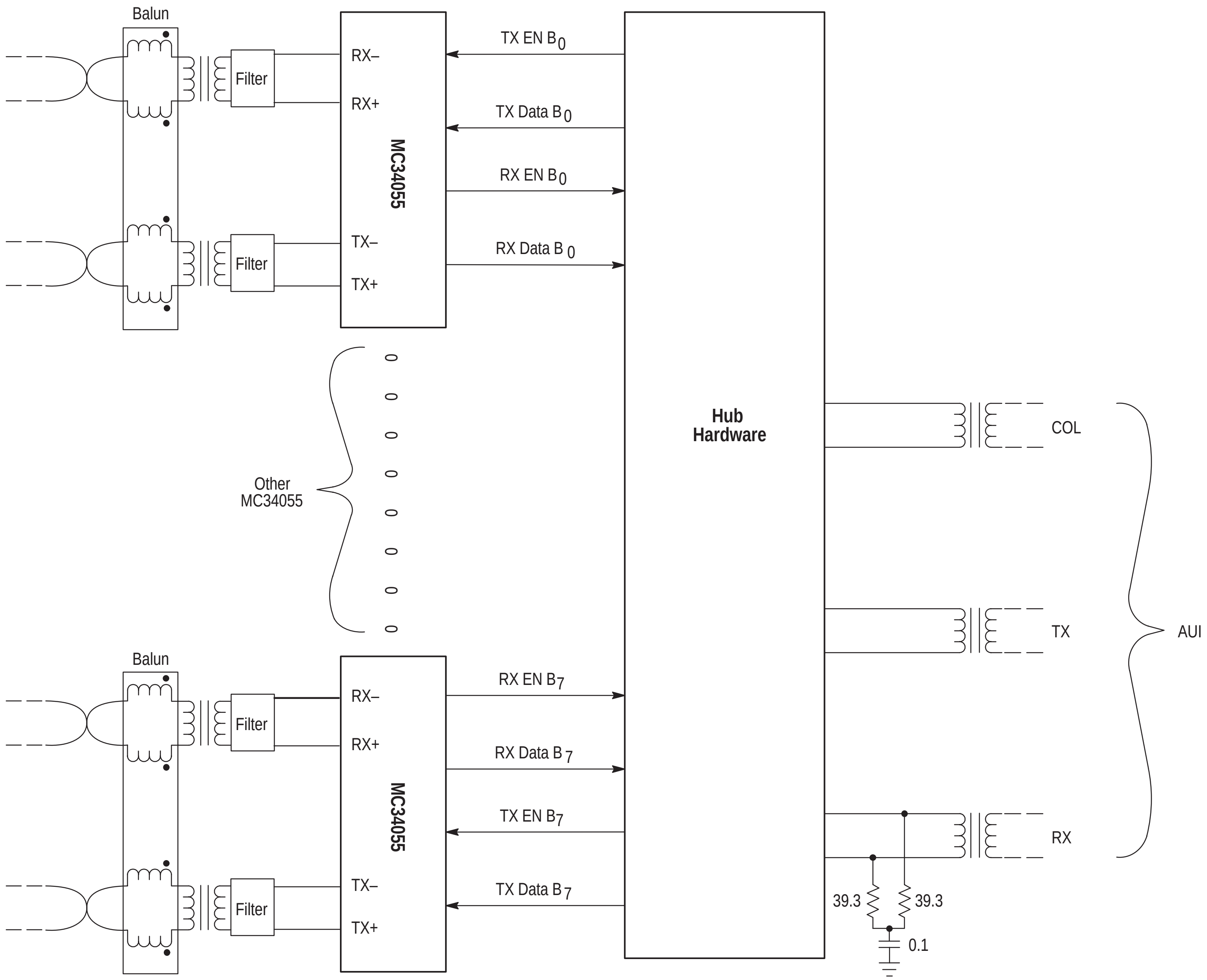


Figure 12. 10BASE–T Connecentrator Application



MOTOROLA

MC34058
MC34059

Hex EIA-485 Transceiver with Three-State Outputs

HEX EIA–485 TRANSCEIVER with THREE–STATE OUTPUTS

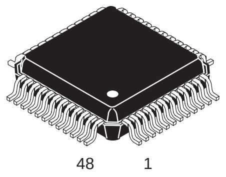
SEMICONDUCTOR TECHNICAL DATA

The Motorola MC34058/9 Hex Transceiver is composed of six driver/receiver combinations designed to comply with the EIA–485 standard. Features include three–state outputs, thermal shutdown for each driver, and current limiting in both directions. This device also complies with EIA–422 and CCITT Recommendations V.11 and X.27.

The devices are optimized for balanced multipoint bus transmission at rates to 20 MBPS (MC34059). The driver outputs/receiver inputs feature a wide common mode voltage range, allowing for their use in noisy environments. The current limit and thermal shutdown features protect the devices from line fault conditions.

The MC34058/9 is available in a space saving 7.0 mm 48 lead surface mount quad package designed for optimal heat dissipation.

- Meets EIA–485 Standard for Party Line Operation
- Meets EIA–422A and CCITT Recommendations V.11 and X.27
- Operating Ambient Temperature: 0°C to +70°C
- Common Mode Driver Output/Receiver Input Range: –7.0 to +12 V
- Positive and Negative Current Limiting
- Transmission Rates to 14 MBPS (MC34058) and 20 MBPS (MC34059)
- Driver Thermal Shutdown at 150°C Junction Temperature
- Thermal Shutdown Active Low Output
- Single +5.0 V Supply, ±10%
- Low Supply Current
- Compact 7.0 mm 48 Lead TQFP Plastic Package

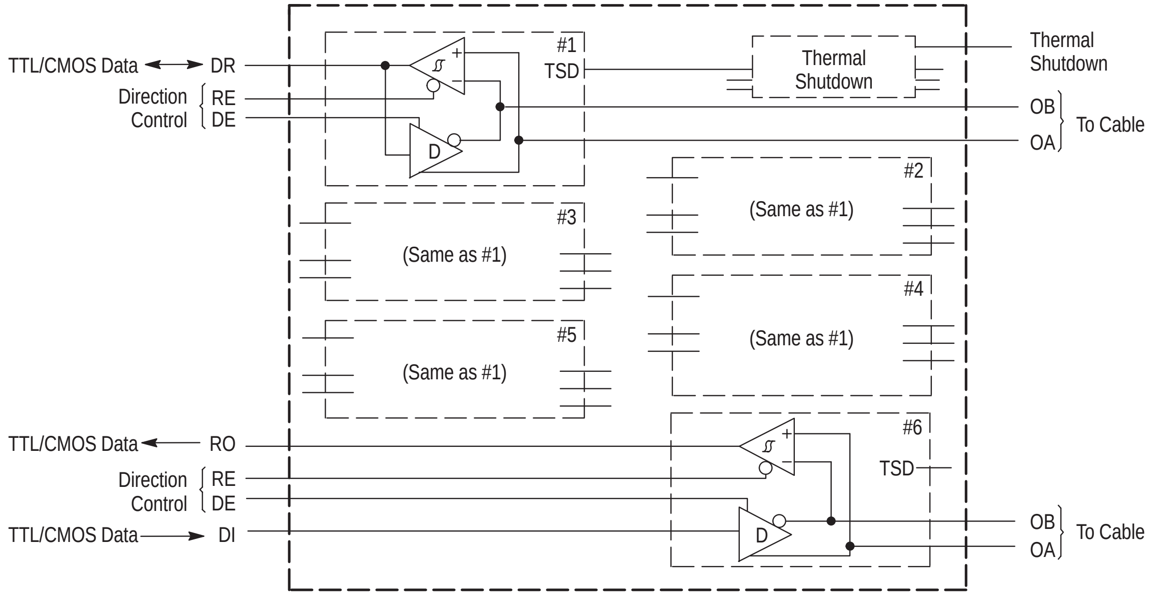


FTA SUFFIX
PLASTIC PACKAGE
CASE 932
(Thin QFP)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC34058FTA	T_A = 0° to +70°C	TQFP–48
MC34059FTA		

Representative Block Diagram



This device contains 1,399 active transistors.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	–0.5, 7.0	Vdc
Input Voltage (Driver Data, Enables)	V_{in}	7.0	Vdc
Applied Driver Output Voltage When in Three–State Condition (V_{CC} = 5.0 V)	V_Z	–10, 14	Vdc
Applied Driver Output Voltage When V_{CC} = 0 V	V_X	±14	Vdc
Output Current	I_O	Self Limiting	–
Storage Temperature	T_{stg}	–65, 150	°C

NOTE: Devices should not be operated at these limits. The “Recommended Operating Conditions” provides for actual device operation.

RECOMMENDED OPERATING CONDITIONS (All limits are not necessarily functional concurrently.)

Characteristic	Symbol	Min	Typ	Max	Unit
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	Vdc
Input Voltage (All Inputs Except Receiver Inputs)	V_{in}	0	–	V_{CC}	Vdc
Driver Output Voltage in Three–State Condition, Receiver Inputs, or When V_{CC} = 0 V	V_{CM}	–7.0	–	12	Vdc
Driver Output Current (Normal Data Transmission)	I_O	–60	–	60	mA
Operating Ambient Temperature	T_A	0	–	70	°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0 V ± 10%)

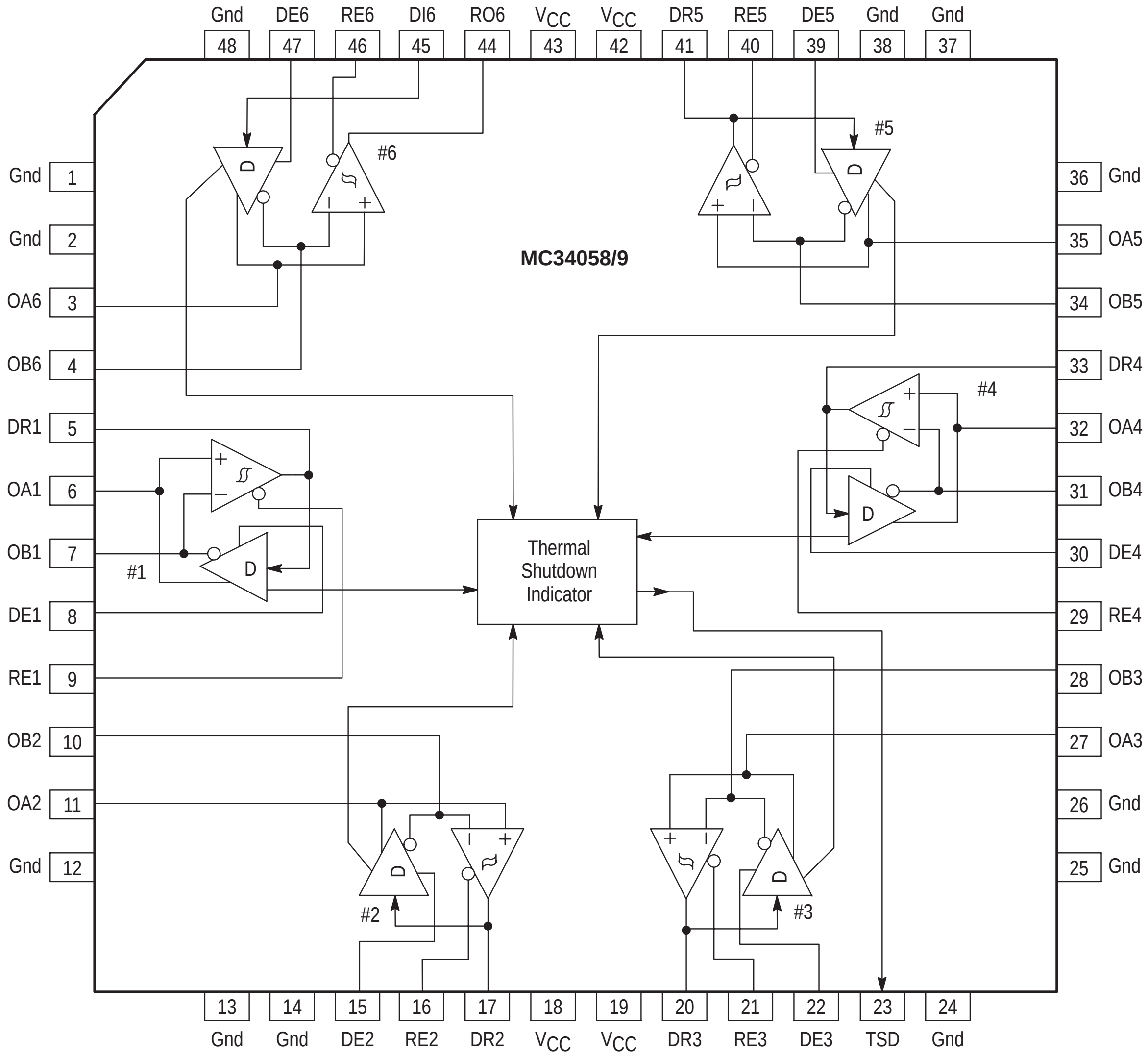
Characteristic	Symbol	Min	Typ	Max	Unit
DRIVER CHARACTERISTICS					
Output Voltage					
Single Ended, I_O = 0	V_O	0	–	V_{CC}	Vdc
Differential, Open Circuit (I_O = 0)	$\lvert V_{OD1} \rvert$	1.5	–	–	Vdc
Differential, R_L = 54 Ω	$\lvert V_{OD2} \rvert$	1.5	–	–	Vdc
Change in Differential Voltage (Note 1), R_L = 54 Ω	$\lvert \Delta V_{OD2} \rvert$	–	–	200	mVdc
Differential, R_L = 100 Ω	$\lvert \Delta V_{OD2A} \rvert$	2.0	–	–	Vdc
Change in Differential Voltage (Note 1), R_L = 100 Ω	$\lvert V_{OD2A} \rvert$	–	–	200	mVdc
Common Mode Voltage, R_L = 54 Ω	V_{OCM}	–	–	3.0	Vdc
Common Mode Voltage Change, R_L = 54 Ω	$\lvert \Delta V_{OCM} \rvert$	–	–	200	mVdc
Output Current (Each Output)					mA
Short Circuit Current, –7.0 V ≤ V_O ≤ 12 V	I_{OS}	–250	–	250	
Driver Data Inputs					Vdc
Low Level Voltage	V_{ILD}	–	–	0.8	
High Level Voltage	V_{IHD}	2.0	–	–	
Clamp Voltage (I_{in} = –18 mA)	V_{IKD}	–1.5	–	–	
Thermal Shutdown Junction Temperature	T_{JTS}	–	150	–	°C
RECEIVER CHARACTERISTICS					
Input Threshold R_O = High	V_{th}	–	–	200	mVdc
R_O = Low		–200	–	–	
Input Loading (Driver Disabled)		–	0.36	1.0	U.L.
Hysteresis	V_H	–	100	–	mV
Output Voltage High (I_{OH} = –400 µA)	V_{OHR}	2.4	–	–	Vdc
Low (I_{OL} = 4.0 mA)	V_{OLR}	–	–	0.4	
Output Short Circuit Current	I_{OSR}	–	45	85	mA
Output Leakage Current When in Three–State Mode	I_{OLKR}	–	–	20	µA

NOTE: 1. Input switched from low to high.

ELECTRICAL CHARACTERISTICS (continued) (T_A = 25°C, V_{CC} = 5.0 V ± 10%)

Characteristic	Symbol	Min	Typ	Max	Unit
MISCELLANEOUS					
Enable Inputs					Vdc
Low Level Voltage	V_{ILE}	0	–	0.8	
High Level Voltage	V_{IHE}	2.0	–	V_{CC}	
Clamp Voltage (I_{in} = –18 mA)	V_{IKE}	–1.5	–	–	
Power Supply Current (Total Package, All Outputs Open, Enabled or Disabled)	I_{CC}	–	18	28	mA
Thermal Shutdown Output Voltage					Vdc
High	V_{OHT}	2.4	–	–	
Low	V_{OLT}	0	–	0.8	
TIMING CHARACTERISTICS – DRIVER					
Propagation Delay – Input to Single Ended Output					ns
Input to Output – Low–to–High	t_{PLH}	–	10	20	
Input to Output – High–to–Low	t_{PHD}	–	11	20	
Propagation Delay – Input to Differential Output					ns
Input Low–to–High	t_{PLHD}	–	15	23	
Input High–to–Low	t_{PHLD}	–	15	23	
Differential Output Transition Time	t_{DR}, t_{DF}	–	9.0	10.7	ns
Skew Timing MC34058					ns
$\lvert t_{PLHD} - t_{PHLD} \rvert$ for Each Driver	t_{SK1}	0	0.1	–	
Maximum – Minimum t_{PLHD} Within a Package	t_{SK2}	0	–	8.0	
Maximum – Minimum t_{PHLD} Within a Package	t_{SK3}	0	–	6.0	
Skew Timing MC34059					ns
$\lvert t_{PLHD} - t_{PHLD} \rvert$ for Each Driver	t_{SK7}	0	0.1	–	
Propagation Delay Difference Between Any Two Drivers (Same Package or Different Packages at Same V_{CC} and T_A)	t_{SK8}	–	<4.0	–	
Enable Timing					ns
Single Ended Outputs					
Enable to Active High Output	t_{PZH}	–	15	40	
Enable to Active Low Output	t_{PZL}	–	25	40	
Active High to Disable	t_{PHZ}	–	12	25	
Active Low to Disable	t_{PLZ}	–	10	25	
Differential Outputs					
Enable to Active Output	t_{PZD}	–	–	40	
Enable to Three–State Output	t_{PDZ}	–	–	25	
TIMING CHARACTERISTICS – RECEIVER					
Propagation Delay					ns
Input to Output – Low–to–High	t_{PLHR}	–	16	23	
Input to Output – High–to–Low	t_{PHLR}	–	16	23	
Skew Timing					ns
$\lvert t_{PLHR} - t_{PHLR} \rvert$ for Each Receiver	t_{SK4}	0	1.0	–	
Maximum – Minimum t_{PLHR} Within a Package	t_{SK5}	0	–	3.0	
Maximum – Minimum t_{PHLR} Within a Package	t_{SK6}	0	–	3.0	
Skew Timing Propagation Delay Difference Between Any Two Receivers in Different Packages at Same V_{CC} and T_A (MC34059 Only)	t_{SK9}	–	<5.0	–	ns
Enable Timing					ns
Single Ended Outputs					
Enable to Active High Output	t_{PZHR}	–	15	22	
Enable to Active Low Output	t_{PZLR}	–	25	30	
Active High to Disable	t_{PHZR}	–	12	25	
Active Low to Disable	t_{PLZR}	–	10	25	

Block Diagram and Pinout



PINOUT SUMMARY

OA	NonInverting Output/Input	DE	Driver Enable, Active High (TTL)
OB	Inverting Output/Input	$\overline{\text{RE}}$	Receiver Enable, Active Low (TTL)
DR	Driver Input/Receiver Output (TTL)	$\overline{\text{TSD}}$	Thermal Shutdown Indicator
DI6	#6 Driver Input (TTL)	V_{CC}	Connect 4 Pins to 5.0 V, ±10%
RO6	#6 Receiver Output (TTL)	Gnd	Connect 12 Pins to Circuit Ground

Figure 1. V_{OD} and V_{OS} Test Circuit

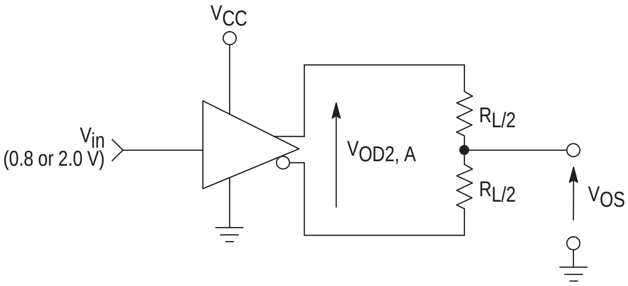


Figure 2. V_{OD} and V_{CM} Test Circuit

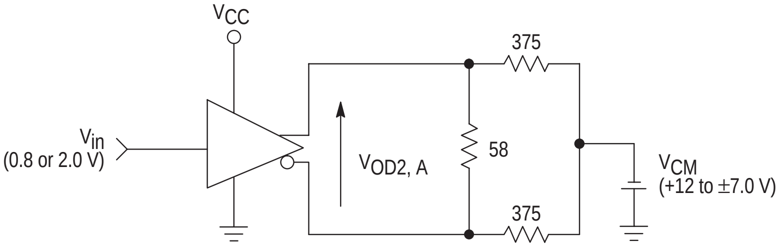


Figure 3. V_{OD} AC Test Conditions

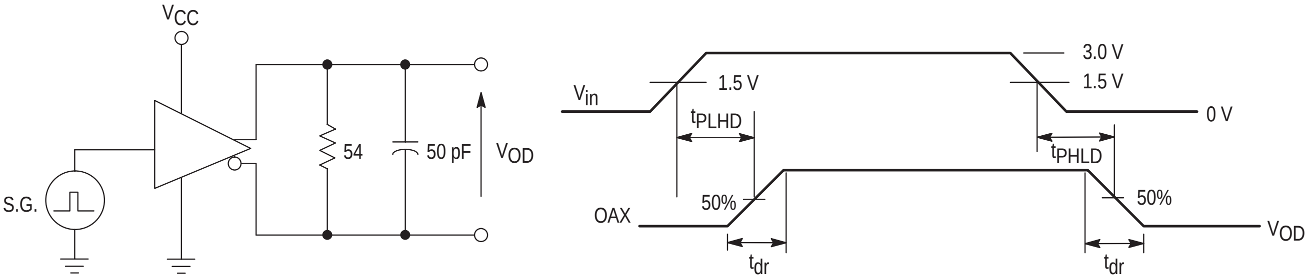


Figure 4. V_{OH} and V_{OL} AC Test Conditions

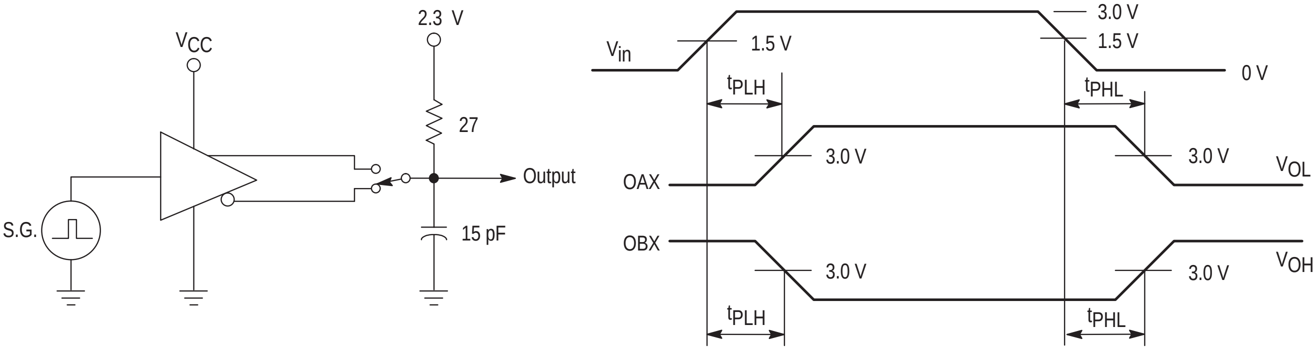


Figure 5. V_{OH} versus I_{OH}

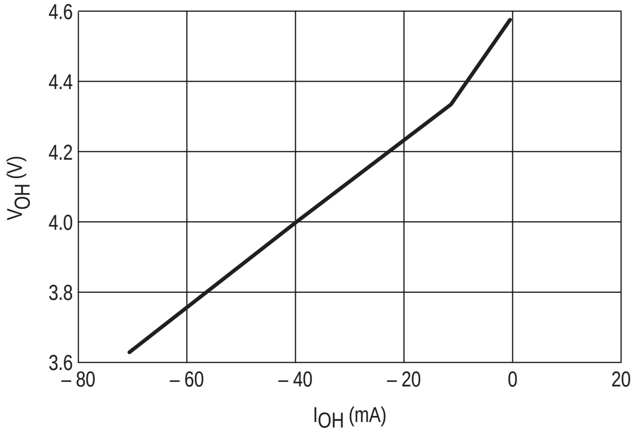


Figure 6. V_{OL} versus I_{OL}

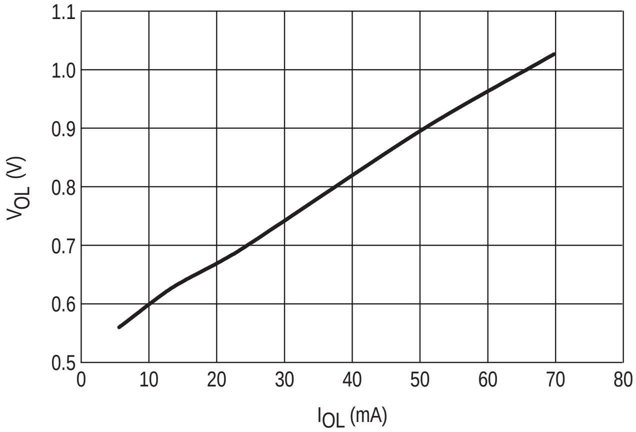


Figure 7. V_{OD} versus I_{OL}

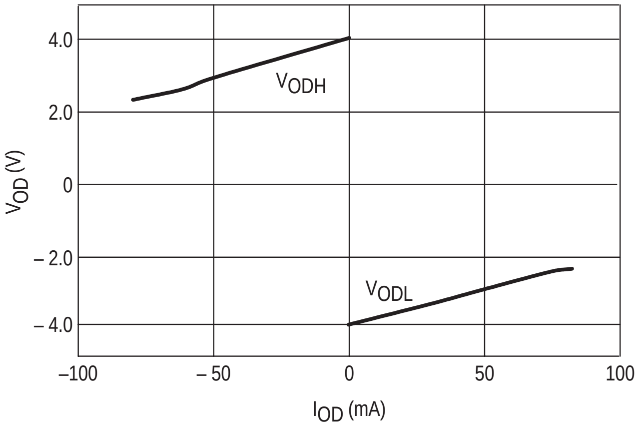
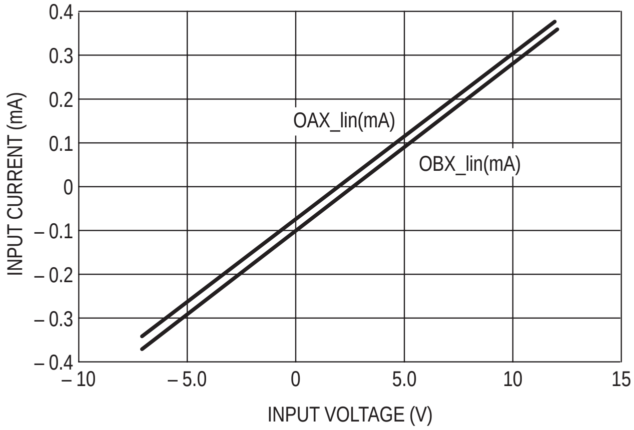


Figure 8. Input Characteristics of OAX and OAB



Description

The MC34058/9 is a differential line driver designed to comply with EIA–485 Standard for use in balanced digital multipoint systems containing multiple drivers. The drivers also comply with EIA–422–A and CCITT Recommendations V.11 and X.27. Positive and negative current limiting of the drivers meet the EIA–485 requirement for protection from damage in the event that two or more drivers try to transmit simultaneously on the same cable. Data rates in excess of 10 MBPS are possible, depending on the cable length and cable characteristics. Only a single power supply, 5.0 V ±10% is required.

Driver Inputs

The driver inputs and enable logic determine the state of the outputs in accordance with Table 1. The driver inputs have a nominal threshold of 1.2 V, and the voltage must be kept within the range of 0 V to V_{CC} for proper operation. If the voltage is taken more than 0.5 V below ground or above V_{CC}, excessive currents will flow and proper operation of the drivers will be affected. An open Pin is equivalent to a logic high, but good design practices dictate that inputs should never be left open. The inputs are TTL type and their characteristics are unchanged by the state of the enable pins.

Driver Outputs

Each output (when active) will be a low or a high voltage, depending on the input state and the load current (see Tables 1, 2 and Figures 2 and 3). The graphs apply to each driver, regardless of how many other drivers within the package are supplying load current.

Table 1. Driver Truth Table

Driver Data Inputs	Enables		Outputs	
	DEX	**REX**	**OAX**	**OBX**
H	H	H	H	L
L	H	H	L	H
X	L	H	Z	Z
X	H	L	Not Defined	Not Defined

The outputs will be in a high impedance state when:
a) The Enable inputs are set according to Table 1;
b) The junction temperature exceeds the trip point of the thermal shutdown circuit. When in this condition, the output's source and sink capability are shut off, and a leakage current of less than 20 µA will flow. Disabled outputs may be taken to any voltage between –7.0 V and 12 V without damage to internal circuitry.

The drivers are protected from short circuits by two methods:
a) Current limiting is provided at each output, in both the source and sink direction, for shorts to any voltage within the 12 V to –7.0 V range, with respect to circuit ground. The short circuit current will flow until the fault is removed, or until the thermal shutdown activates. The current limiting circuit has a negative temperature coefficient and requires no resetting upon removal of the fault condition.
b) A thermal shutdown circuit disables the outputs when the junction temperature reaches +150°C, ± 20°C. The thermal shutdown circuit has a hysteresis of ~ 12°C to prevent oscillations. When this circuit activates, the output stage of each driver is put into the high impedance mode, thereby shutting off the output currents. However, the remainder of the internal circuitry remains biased and the outputs will become active once again as the IC cools down.

Receiver Inputs

The receiver inputs and enable logic determine the state of the receiver outputs in accordance with Table 2. Each receiver input pair has a nominal differential threshold of at most 200 mV (Pin OAX with respect to OBX) and a common mode voltage range of –7.0 V and 12 V must be maintained for proper operation. A nominal hysteresis of 100 mV is typical. The receiver input characteristics are shown in Figure 8. When the inputs are in the high impedance state, they remain capable of the common mode voltage range of –7.0 V to 12 V.

Receiver Outputs

The receiver outputs are TTL type outputs and act in accordance with Table 2.

Enable Logic

Each driver output is active when the Driver Enable input is true according to Table 1. Each receiver output is active when the Receiver Enable input is true according to Table 2.

The Enable inputs have a nominal threshold of 1.2 V and their voltage must be kept within the range of 0 V and V_{CC} for proper operation. If the voltage is taken more than 0.5 V below ground or above V_{CC}, excessive currents will flow and proper operation of the drivers will be affected. An open pin is equivalent to a logic high, but good design practices dictate that inputs should never be left open. The enable inputs are TTL compatible. Since the same pins are used for driver input and receiver output, care must be taken to make sure that DEX and $\overline{\text{REX}}$ are not both enabled. This may result in corruption of both the transmitted and received data.

Table 2. Receiver Truth Table

Receiver Data Inputs	Enables		Outputs
OAX–OBX	**DEX**	**$\overline{\text{REX}}$**	**DRX**
≥ +200 mV	L	L	H
≤ –200 mV	L	L	L
X	L	H	Z
X	H	L	Not Defined

APPLICATIONS

The MC34058/9 was designed to meet EIA/TIA–422 and EIA/TIA–485 standards. EIA/TIA–422 specifies balanced point–to–point transmission with the provision for multiple receivers on the line. EIA/TIA–485 specifies balanced point–to–point transmission and allows for multiple drivers and receivers on the line. Refer to EIA/TIA documents for more details. Figure 9 shows a typical EIA/TIA–422 example. Figure 10 shows a typical EIA/TIA–485 example.

Figure 9. Typical EIA/TIA–422 Application

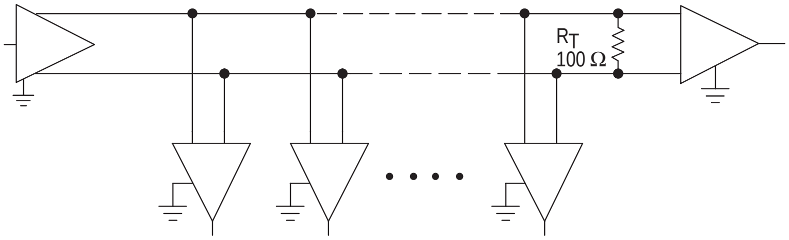
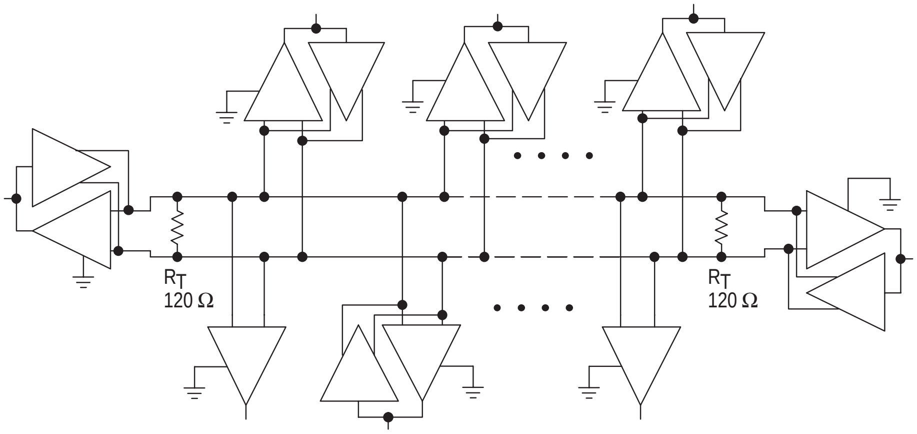
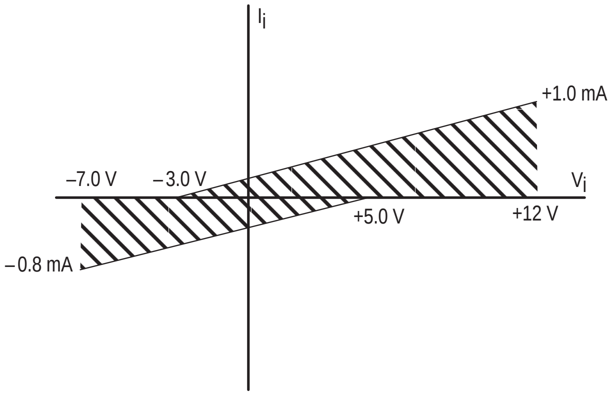


Figure 10. Typical EIA/TIA–485 Application



EIA/TIA–422 specifications require the ability to drive at least 10 receivers of input impedance of greater than or equal to 4.0 KΩ plus the 100 Ω termination resistor. This protocol was intended for unidirectional transmission. EIA/TIA–485 is capable of bidirectional transmission by allowing multiple drivers and receivers on the same twisted pair segment. The loading of the twisted pair segment can be up to 32 Unit Loads (U.L.) plus the two 120 Ω terminating resistors. The U.L. definition is shown in Figure 11.

Figure 11. TIA/EIA–485 Unit Load Definition



Calculating Power Dissipation for the MC34058/9 Hex–Transceiver.

The operational temperature range is listed as 0°C to 70°C to satisfy both EIA/TIA–485 and EIA/TIA–422 specifications. However, a lower ambient temperature may be required depending on the specific board layout and/or application.

Using a first order approximation for heat transfer, the maximum power which may be dissipated by the package is determined by (see Appendix A for more details);

$$P_{Dmax} = \frac{T_{Jmax} - T_A}{\theta ja} \qquad [1]$$

where:

θja = package thermal resistance (see Appendix A)

T_{Jmax} = Maximum Junction Temperature. Since the thermal shutdown feature has a trip point of 150°C ± 20°, T_{Jmax} is selected to be +130°C.

T_A = Ambient Operating Temperature.

The power generated within the package is then;

$$PD = \left\{\left[\left(V_{CC} - V_{OH_1}\right) \cdot I_{OH_1}\right] + V_{OL_1} \cdot I_{OL_1}\right\} + ..$$

$$\text{(each\_driver)..} + \left\{\left[\left(V_{CC} - V_{OH_6}\right) \cdot I_{OH_6}\right] + \right.$$

$$\left. V_{OL_6} \cdot I_{OL_6}\right\} + V_{CC} \cdot I_{CCQ} \qquad [2]$$

As indicated in the equation, the part of Equation 2 consisting of I_{OH}, V_{OH}, I_{OL} and V_{OL} must be calculated for each of the drivers and summed for the total power dissipation estimate. The last term can be considered the quiescent power required to keep the IC operational and is measured with the drivers idle and unloaded. The V_{OH} and V_{OL} terms can be determined from the output current versus output voltage curves which provide driver output characteristics.

Example 1 estimates thermal performance based on current requirements.

Example 1. Balanced and Unbalanced Operation

I_{OL} = 50 mA and I_{OH} = ±50 mA for each driver. V_{CC} = 5.0 V.
How many drivers can be used? (Typical power supply current I_{CCQ} = 18 mA.)

Solution:

I_{CCQ} = 0.018 A
The quiescent power is given by: $PQ = I_{CCQ} \cdot V_{CC}$, and is equal to $PQ = 0.09$ W.

Balanced Operation:

To determine the amount of power dissipated by each output stage we need to know the differential output voltage for the output current required. Figure 7 shows that for I_{OH} and I_{OL} differential of 50 mA, V_{ODH} and V_{ODL} are:

$$V_{OD} = |3.0|, \text{ and } I_{OL} = |I_{OH}| = I_{Out} = 0.050 \text{ A.}$$

And the power dissipated by each driver is given by;

$$P_{DrvB} = I_{Out} \cdot \left(V_{CC} - V_{OD}\right) \text{ and equal to}$$

$$P_{DrvB} = 0.10 \text{ W.}$$

Unbalanced Operation:

To determine the amount of power dissipated by each output stage we need to know the single–ended output voltage for the output current required. Figures 5 and 6 shows that for an I_{OH} and I_{OL} of ±50 mA,

$$V_{OH} = 3.9 \text{ V} \quad V_{OL} = 0.895 \text{ V}$$

And the power dissipated by each driver is calculated by;

$$P_{DrvU} = \left(V_{CC} - V_{OH}\right) \cdot |I_{OH}| + V_{OL} \cdot I_{OL}$$

and equal to

$$P_{DrvU} = 0.10 \text{ W.}$$

(For this example, balanced operation is assumed.)

Summing the quiescent and driver power for 6 transceivers operating in a package produces;

$$P_{DTotal} = PQ + 6 \cdot P_{DrvB}, \text{ and equal to } P_{DTotal} = 0.69 \text{ W.}$$

For the MC34058/9, the thermal resistance is capable of a wide range. The ability of the package to dissipate power depends on board type and temperature, layout and ambient temperature (see Appendix A). For the purposes of this example the thermal resistance can range from 40°C/W to 100°C/W;

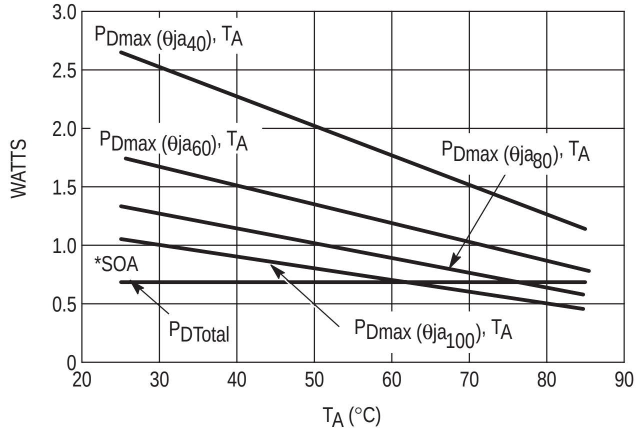
$$\theta ja = j, \ j = 40, 60, .. 100°C/W.$$

Varying the ambient operating temperature T_A = 25, 30, .. 85°C; specifying a maximum junction temperature to avoid thermal shutdown T_{Jmax} = 130°C; and using the first order approximation for maximum power dissipation;

$$P_{Dmax\left(\theta ja\right)}, \ T_A = \frac{T_{Jmax} - T_A}{\theta ja}$$

produces a set curves that can be used to determine a Safe Operating Area for the specific application. P_{DTotal} is graphed with P_{Dmax} to provide a reference.

Graph of Maximum Power Dissipation Possible for a Particular θja and Ambient Temperature

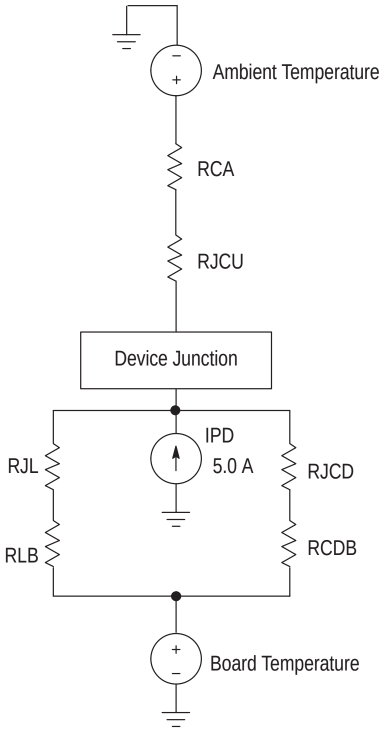


* Safe Operating Area (SOA), is an operating power, P_{DTotal}, less than P_{Dmax}.

So all the drivers in the package can be used if the thermal resistance and/or the ambient temperature is low enough.

Appendix A. Optimizing the Thermal Performance of the MC34058/9

Figure 12. Electrical Model of Package Heat Transfer



An equivalent electrical circuit for the thermal model for the MC34058/9 package is shown in Figure 12. It is a simplified model that shows the dominant means of heat transfer from the thermally enhanced 48–ld package used for the MC34058/9. The model is a first order approximation and is intended to emphasize the need to consider thermal issues when designing the IC into any system. It is however customary to use similar models and Equation 1 to estimate device junction temperatures.

Equation 1 is the common means of using the thermal resistance of a package to estimate junction temperature in a particular system.

$$T_J = \left(P_D \cdot \theta jx\right) + T_A \qquad [1]$$

The term θjx in Equation 1 is usually quoted as a øja value in °C/Watt. However, since the 48–ld package for the MC34058/9 has been thermally enhanced to take advantage of other heat sinking potentials, it must be modified. θjx must actually be considered a composite of all the heat transfer paths from the chip. That is, the three dominant and parallel paths shown in Figure 12. Of those three paths, potentially the most effective is the corner package leads. This is because these corner leads have been attached to the flag on which the silicon die is situated. These pins can be connected to circuit board ground to provide a more efficient conduction path for internal package heat. This path is modeled as the Rjl (junction–to–leads) and Rlb (leads–to–board) combination in Figure 12. This path provides the most effective way of removing heat from the device provided that there is a viable temperature potential (i.e. heat sinking source) to conduct towards. However, if it is not properly considered in the system design, the other paths, (Rjcd + Rcdb) and (Rjcu + Rca) attain greater importance and must be more carefully considered.

So Equation 1, modified to reflect a more complete heat transfer model becomes;

$$T_J = T_A \cdot \frac{\left(\dfrac{1}{\dfrac{1}{Rjcd} + \dfrac{1}{Rjlb}}\right)}{\left(\dfrac{1}{\dfrac{1}{Rjcd} + \dfrac{1}{Rjlb}}\right) + Rjca} + \ldots \qquad [2]$$

$$\ldots\ T_B \cdot \frac{Rjca}{\left(\dfrac{1}{\dfrac{1}{Rjcd} + \dfrac{1}{Rjlb}}\right) + Rjca} + PDISS \cdot \theta ja$$

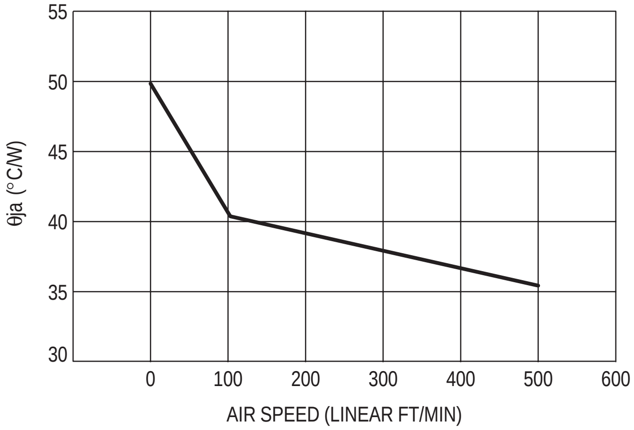
where;

T_J= Junction Temperature
T_A = Ambient Temperature
T_B = Board Temperature
P_{DISS} = Device Power
and θja = Total Thermal Resistance and is composed the parallel combination of all the heat transfer paths from the package.

While Equation 2 is still only a first order approximation of the heat transfer paths of the MC34058/9, at least now it includes consideration for the most effective heat transfer path for the MC34058/9; the board to which the device is soldered. The modified equation also better serves to explain how external variables, namely the board and ambient temperatures, affect the thermal performance of the MC34058/9.

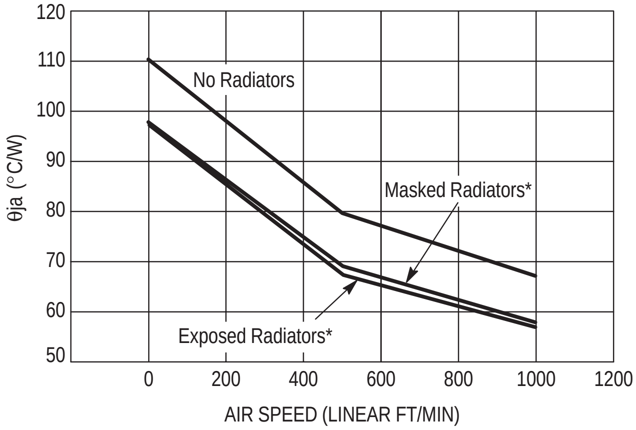
Methods of removing heat via the flag connected pins can be classified into two means; conduction and convection. Radiation is omitted as the contribution is small compared to the other means. Conduction is by far the best method to draw heat away from the MC34058/9 package. This is best accomplished by using a multilayer board with generous ground plane. In this case, the flag connected pins can be connected directly to the ground plane to maximize the heat transfer from the package. Figure 13 shows the results of thermal measurements of a board with an external ground plane (the actual ground area was approximately 6 1/4 in^2). The thermal leads are connected to the board ground plane per the recommended strategy.

Figure 13. Thermal Resistance (θja) for Board with Large External Ground Plane



θjc for the package on this board is 25 ± 20% depending on the location of the package on the board.

Figure 14A. Thermal Resistance (θja) for Board Without Ground Plane



* Masked radiators were covered by a solder mask. Exposed radiators were bare copper.

Figure 14B. Layout Used for Thermal Resistance Measurements in Figure 14A

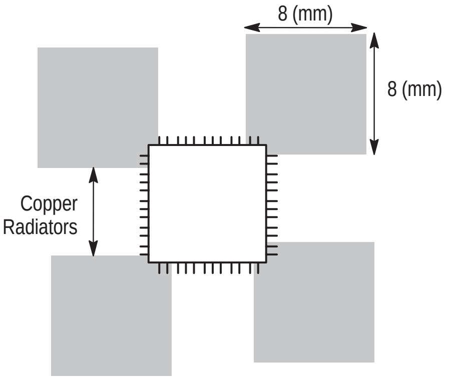


Figure 15. Placement of Thermal Vias to Enhance Heat Transfer to Ground Plane

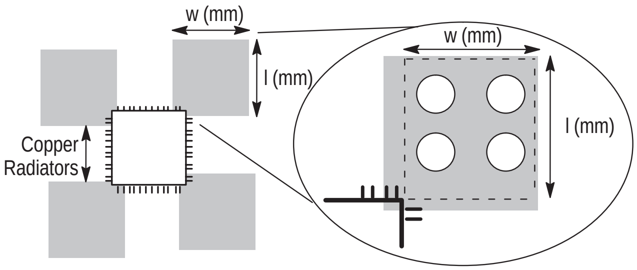


Figure 14A on the other hand shows the result of a single layer board without an internal ground plane. The graphs show that even though there are radiators of substantial area surrounding the package, substantial degredation of thermal performance is evident (Figure 14B shows the layout used for the measurements in Figure 14A). Comparing Figures 13 and 14A shows almost a 2:1 improvement for the strategy involving the external ground plane.

It is clear from Figures 13, 14A and Example 1, that if an application is to use all the device drivers, preparations to assure adequate thermal performance of the system must be taken.

If an extensive external ground plane is unavailable, and only an internal ground plane is available, the thermal performance of the device can still be improved by providing thermal vias to connect the radiators to the internal ground plane. Figure 15 shows a proposed scheme for thermal vias (contact board manufactures for specifics about the thermal performance of their products and possible enhancements).

The thermal resistance for this structure on 1.0 oz. Copper connecting each of the four radiators to an internal ground plane and provide an estimated thermal resistance of approximately 5.0°C/W. The vias used in the estimate had 80 mil diameters, on 100 mil centers and a 1.0 mil copper thickness.

MOTOROLA

MC34156

Product Preview

28-Channel Inkjet Driver

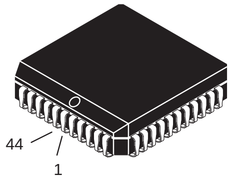
28–CHANNEL INKJET DRIVER
(SMARTMOS™ Technology)

SEMICONDUCTOR TECHNICAL DATA

The MC34156 is a 28–Channel Decoder/Driver intended to be used in inkjet printer applications. By using sophisticated SMARTMOS™ technology, it has been possible to combine low power CMOS inputs and logic and high current, high voltage bipolar outputs capable of sustaining a maximum of 30 V.

A 4–to–14 line decoder determines the selected output driver (n) in each 14–driver bank. Two independent output enable inputs (active low) then provide the final decoding to activate 1– or 2–of–28 outputs (OUT_{An} and/or OUT_{Bn}). The ac electrical characteristics of the drivers are tightly controlled and thereby the energy of the device delivers to the inkjet print head. A Chip Enable function is provided to lock out the drivers during system power up. The 28 bipolar power outputs are open collector 30 V Darlington drivers capable of sinking 500 mA at ambient temperatures up to 70°C. All driver outputs are capable of withstanding a contact discharge of ±8.0 kV with the IC biased.

- ESD Output Protection with Clamping Diodes
- Addressable Data Entry
- Tightly Controlled AC and Electrical Characteristics for Inkjet Printers
- CMOS, TTL Compatible Inputs
- Low Power CMOS Logic

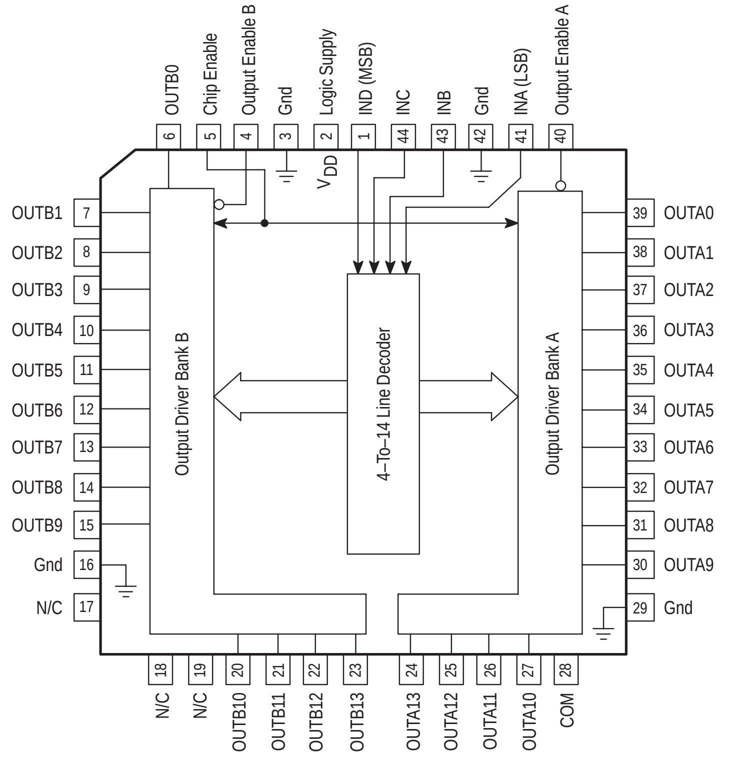


FN SUFFIX
PLASTIC PACKAGE
CASE 777

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC34156FN	T_A = 0° to +70°C	Plastic Package

Simplified Block Diagram



PIN ASSIGNMENTS

Pin No.	Pin Name	Pin Description
1	IND	4th Decoder Input
2	V_{DD}	Power Supply
3	Gnd	Ground
4	ENB	Enable Pin for B Set Drivers
5	Chip Enable	Chip Enable
6	OUTB0	B Set 1st Driver
7	OUTB1	B Set 2nd Driver
8	OUTB2	B Set 3rd Driver
9	OUTB3	B Set 4th Driver
10	OUTB4	B Set 5th Driver
11	OUTB5	B Set 6th Driver
12	OUTB6	B Set 7th Driver
13	OUTB7	B Set 8th Driver
14	OUTB8	B Set 9th Driver
15	OUTB9	B Set 10th Driver
16	Gnd	Ground
17	N/C	Not Connected
18	N/C	Not Connected
19	N/C	Not Connected
20	OUTB10	B Set 11th Driver
21	OUTB11	B Set 12th Driver
22	OUTB12	B Set 13th Driver
23	OUTB13	B Set 14th Driver
24	OUTA13	A Set 14th Driver
25	OUTA12	A Set 13th Driver
26	OUTA11	A Set 12th Driver
27	OUTA10	A Set 11th Driver
28	COM	Common
29	Gnd	Ground
30	OUTA9	A Set 10th Driver
31	OUTA8	A Set 9th Driver
32	OUTA7	A Set 8th Driver
33	OUTA6	A Set 7th Driver
34	OUTA5	A Set 6th Driver
35	OUTA4	A Set 5th Driver
36	OUTA3	A Set 4th Driver
37	OUTA2	A Set 3rd Driver
38	OUTA1	A Set 2nd Driver
39	OUTA0	A Set 1st Driver
40	ENA	Enable Pin for A Set Drivers
41	INA	1st Decoder Input
42	Gnd	Ground
43	INB	2nd Decoder Input
44	INC	3rd Decoder Input

Figure 1. Functional Block Diagram

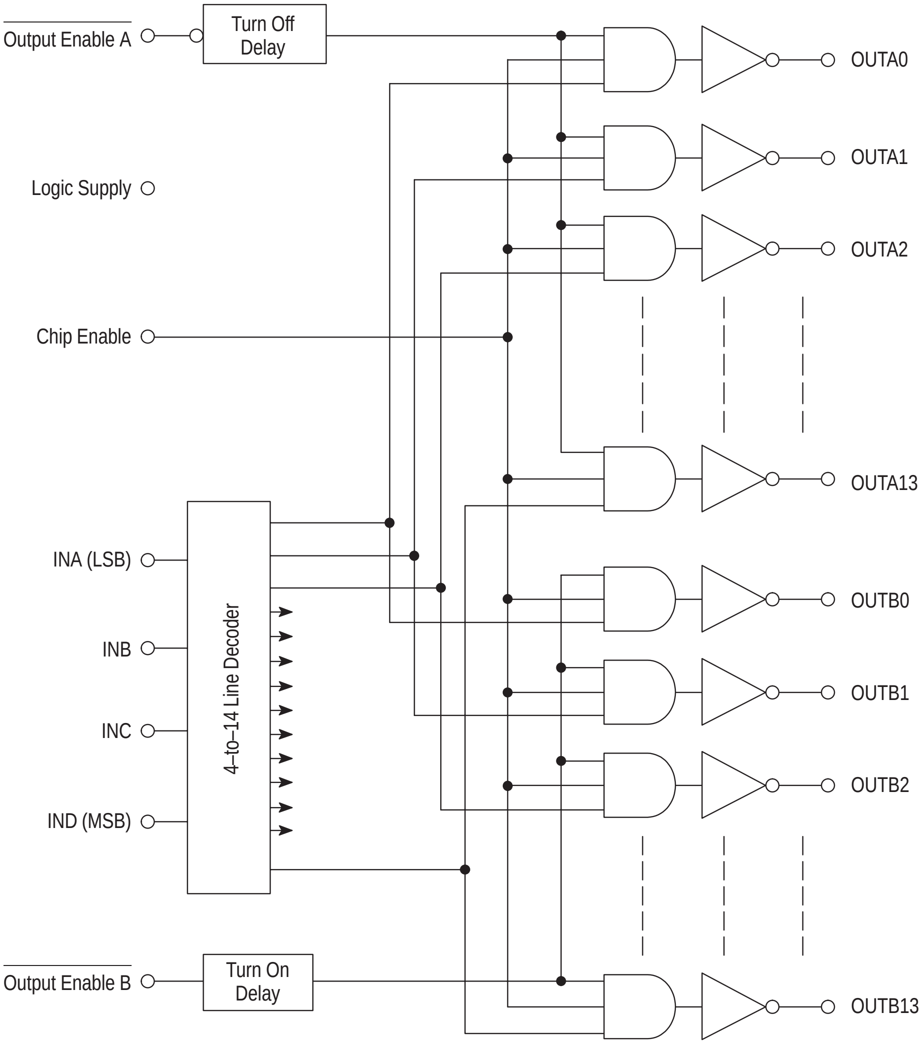


Figure 2. Output Driver Configuration

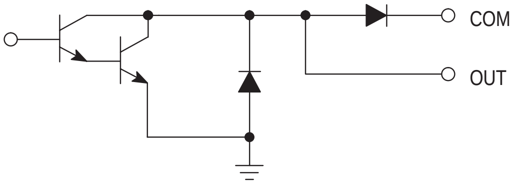
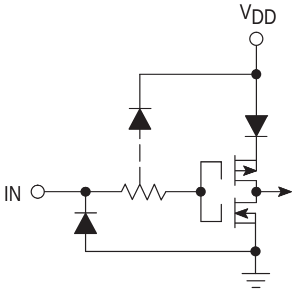


Figure 3. Typical Input Circuit



MOTOROLA

MC34250

Product Preview

5.0 V, 200 M-Bit/Sec PR-IV Hard Disk Drive Read Channel

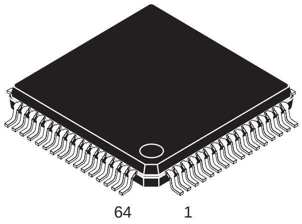
The Motorola MC34250 is a fully integrated partial response maximum likelihood disk drive read/write channel for use in zoned recording applications. This device integrates the AGC, active filter, 7 tap equalizer, Viterbi detector, frequency synthesizer, servo demodulator, 8/9 rate (0,4/4) Encoder/Decoder with write precompensation and power management in a single 64 pin 10 mm x 10 mm TQFP package.

FEATURES:

- 50 to 200 MBPS Programmable Data Rate
- 800 mW at 200 MBPS and 5.0 V
- Channel Monitor Output
- Programmable AGC Charge Pump Currents with Different Values for Data and Servo Envelope Modes and Gain Gradient Mode
- Programmable AGC Peak Detector Droop Currents with Different Values for Data and Servo Envelope Modes
- Separate AGC Charge Pump Outputs for Data and Servo Modes
- Programmable Dual Threshold Qualifier or Hysteresis Comparator Type Pulse Detector for Servo Data Detection.
- ERD and Polarity Outputs for Servo Timing and Raw Encoded Data
- Integrated 7 pole 0.05° Equiripple Linear Phase Filter with Programmable Bandwidth from 5.0 MHz to 80 MHz and Different Values for Both Data and Servo Modes
- Programmable Symmetrical Boost from 0 to 10 dB and Different Values for Data and Servo Modes
- Programmable Asymmetrical Boost of Up to ±40% of Nominal Filter Group Delay in Both Data and Servo Modes
- 7 Tap Continuous Time Transversal Equalizer with 8 Bit Programmable Tap Weights and Integrated Decision Directed Sign–Sign Least Mean Squared Adaptation
- Internal Offset Cancellation Loops
- Fast Acquisition Data Phase Locked Loop with Zero Phase Restart
- Programmable Data Phase Locked Loop Charge Pump Current
- Integrated Soft Decision Viterbi Detectors with Programmable Merge References
- Integrated 8/9 Rate (0,4/4) Encoder and Decoder with Code Scrambler and Descrambler
- Programmable 2/4/8 Bit NRZ Data Interface
- Programmable Write Precompensation Delays Locked to the Frequency Synthesizer
- Differential PECL Write Data Outputs
- External Write Data Path for DC Erase or Other Non–Encoded Data
- Integrated Write Current DAC
- Programmable Power Management
- Bi–Directional Serial Microprocessor Interface
- Various Test Modes Controlled Via the Serial Microprocessor Interface

HARD DISK DRIVE READ CHANNEL

SEMICONDUCTOR TECHNICAL DATA

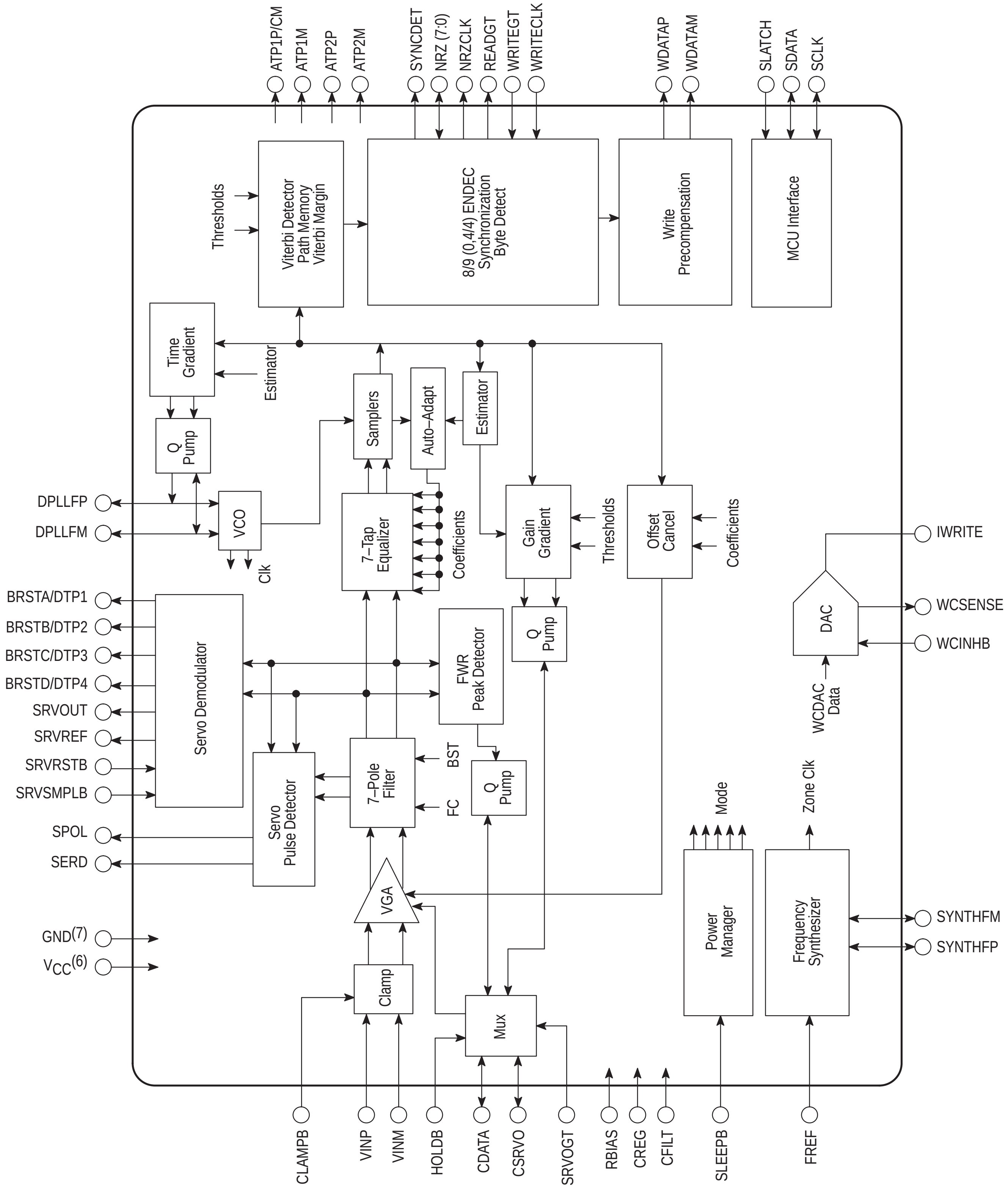


FTA SUFFIX
PLASTIC PACKAGE
CASE 840F
(Thin QFP)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC34250FTA	T_A = 0° to +70°C	TQFP–64

Simplified Block Diagram



This device contains 80,000 active transistors.

MC68160

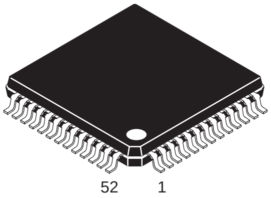
Enhanced Ethernet Transceiver

ENHANCED ETHERNET INTERFACE TRANSCEIVER

SEMICONDUCTOR TECHNICAL DATA

The MC68160 Enhanced Ethernet Interface Circuit is a BiCMOS device which supports both IEEE 802.3 Access Unit Interface (AUI) and 10BASE–T Twisted Pair (TP) Interface media connections through external isolation transformers. It encodes NRZ data to Manchester data and supplies the signals which are required for data communication via 10BASE–T or AUI interfaces. The MC68160 gluelessly interfaces to the Ethernet controller contained in the MC68360 Quad Integrated Communications Controller (QUICC) device. The MC68160 also interfaces easily to most other industry–standard IEEE 802.3 LAN controllers. Prior to twisted pair data reception, Smart Squelch circuitry qualifies input signals for correct amplitude, pulse width, and sequence requirements.

- Interfaces with AMD, National, Intel and Fujitsu IEEE 802.3 LAN Controllers
- Automatic Twisted Pair Wiring Polarity Fault Detection and Correction Option
- Automatic Port Selection Option with Status Output
- Driver Pre–emphasis for Twisted Pair Output Data
- Crystal Controlled Clock Oscillator or External Clock Generator Option
- Digital Phase–Locked–Loop (DPLL) Timing Recovery and Data Decoding
- Standby Mode with Reduced Power Consumption
- Twisted Pair Signal Quality Error (Heartbeat) Test Option
- Diagnostic Local Loop Back Option
- Transmit, Receive and Collision Detection Status Output
- Full–Duplex Operation Option on Twisted Pair Port
- Twisted Pair Jabber Detection and Status Output
- Link Integrity Testing and Status Output

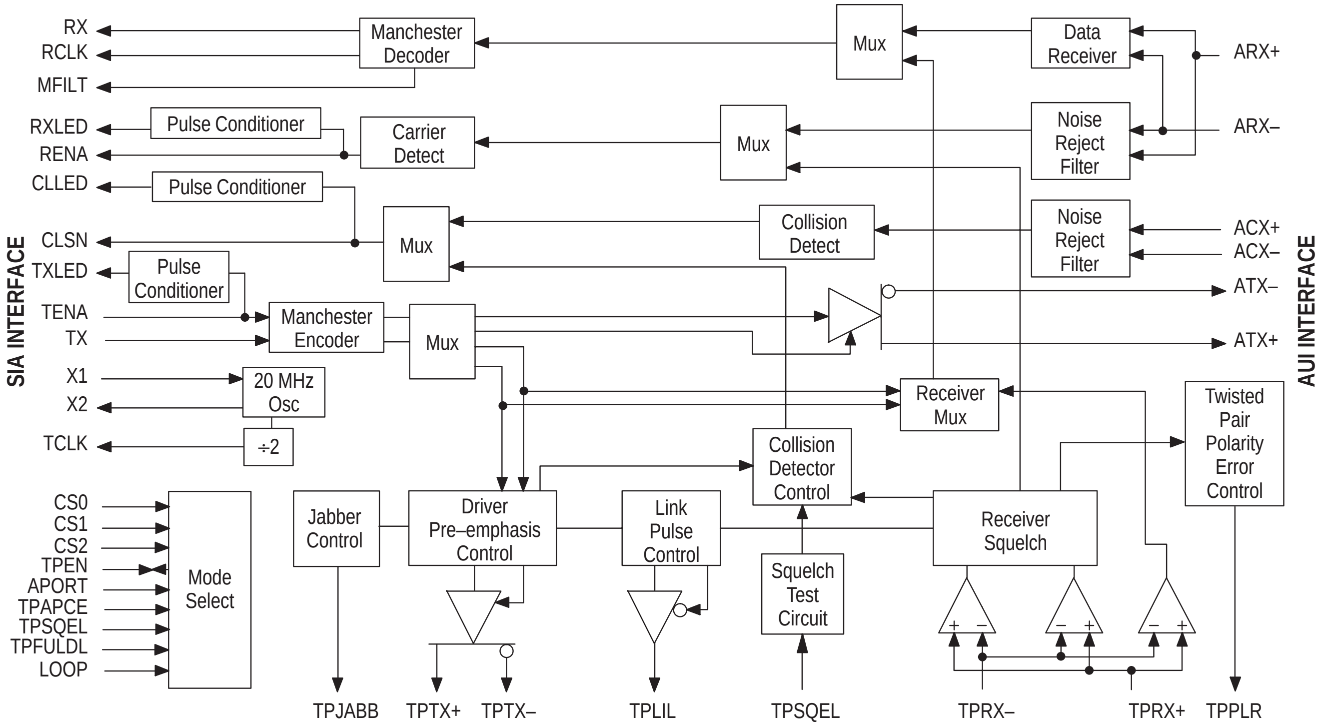


FB SUFFIX
PLASTIC PACKAGE
CASE 848D
(Thin QFP)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC68160FB	T_A = 0° to + 70°C	TQFP–52

Figure 1. 10Base–T Interface Block Diagram



This device contains 20,000 active transistors.

MC68160

Enhanced Ethernet Serial Transceiver

Table 1. Pin Function Description

Pin(s)	Symbol	Type	Name/Function
CONTROLLER INTERFACE			
1	RENA	O TTL/CMO	**Receive Enable Output:** Indication of the presence of network activity, synchronous to RCLK. In the standby mode, RENA is driven to the high impedance state.
2	RX	O TTL/CMOS	**Receive Data Output:** Recovered data, synchronous to RCLK. Following a reset operation, 100 ms should be allowed before attempting to read data processed by the MC68160. This delay is needed to insure that the receive phase locked loop is properly synchronized with incoming data. In the standby mode, RX is driven to the high impedance state.
48	TCLK	O TTL/CMOS	**Transmit Clock Output CMOS/TTL Output:** TCLK provides a symmetrical clock signal at 10 MHz for reference timing of data to be encoded. In the standby mode, TCLK is driven to the high impedance state.
49	TENA	I TTL	**Transmit Enable Input:** Input signal synchronous to TCLK which enables data transmission on the active port. An internal pull–down resistor is provided so that the input is low under no connect conditions. (This resistor is removed in the standby mode). If TENA is asserted at the conclusion of a reset operation, it must first be deasserted and then reasserted before data transmission can occur. In the standby mode, TENA is driven to the high impedance state.
50	RCLK	O TTL/CMOS	**Receive Clock Output:** Recovered clock. In the standby mode, RCLK is driven to the high impedance state.
51	CLSN	O TTL/CMOS	**Collision Output:** In the AUI mode, indicates the presence of signals at the ACX+ and ACX– terminals which meet threshold and pulse width requirements. In the TP mode, indicates simultaneous transmit and receive activity, a heartbeat (SQE Test) signal was generated, or the jabber timer has expired. In the standby mode, CLSN is driven to the high impedance state.
52	TX	I TTL	**Transmit Data Input:** Input signal synchronous to TCLK which provides NRZ serial data to be Manchester encoded. In the standby mode, TX is driven to the high impedance state.
AUI INTERFACE			
21 22	ACX– ACX+	I	**AUI Differential Collision Inputs:** These inputs are connected to a pair of internally biased line receivers consisting of a carrier detect receiver with offset threshold and noise filtering to detect the line activity. Signals at ACX+/– have no effect on data path functions.
23 24	ARX– ARX+	I	**AUI Differential Receiver Inputs:** These inputs are connected to a pair of internally biased line receivers consisting of a carrier detect receiver with offset threshold and noise filtering to detect the line activity, and a data receiver with no offset for Manchester Data reception.
25 26	ATX– ATX+	O	**AUI Differential Transmit Outputs :** This line pair is intended to operate into terminated transmission lines. For TX signals meeting setup and hold time to TCLK when TENA is previously asserted, Manchester encoded data is outputted at ATX+/–. When operating into a 78 Ω terminated transmission line, signaling meets the required output levels and skew for IEEE–802.3 drop cables. When the 10BASE–T port is automatically or manually selected, the AUI outputs are driven to a low power standby state in which the outputs deliver a balanced high state voltage.
TWISTED PAIR INTERFACE			
31 32	TPRX– TPRX+	I	**Twisted Pair Differential Receiver Inputs:** These inputs are connected to a receiver with Smart Squelch capability which only allows differential receive data to pass as long as the input amplitude is greater than a minimum signal threshold level and a specific pulse sequence is received. This assures a good signal to noise ratio while the signal pair is active by preventing crosstalk and impulse noise conditions from activating the receive function.
36 37	TPTX– TPTX+	O	**Twisted Pair Differential Transmitter Outputs:** These lines have pre–distortion drive capability and are intended to drive terminated twisted pair transmission lines. When the AUI port is manually selected, the 10BASE–T outputs are driven to a low power standby state in which the outputs deliver a balanced high state voltage. However, when the AUI port is automatically selected, the 10BASE–T outputs remain active.

NOTE: The sense of the controller interface pins will change, depending on the controller selected.

Table 1. Pin Function Description (continued)

Pin(s)	Symbol	Type	Name/Function
OSCILLATOR AND FREQUENCY MULTIPLIER			
12	MFILT	C	**Frequency Multiplier Filter Connection Point:** An external resistor capacitor filter must be attached to this pin.
16	X1	I/C CMOS	**Oscillator Inverter Input and Crystal Connection Point:** When connected for crystal oscillator operation, the frequency of the clock which appears at TCLK is half that of the crystal oscillator. As an option, instead of connecting to a crystal, X1 may be driven from an external 20 MHz CMOS compatible clock generator.
17	X2	O/C CMOS	**Oscillator Inverter Output and Crystal Connection Point:** This pin is used only for the connection of an external crystal and capacitor. It must be left unconnected if X1 is driven by an external CMOS Clock generator.
MODE SELECT			
3 4 5	CS0 CS1 CS2	I TTL	**Mode Select:** The logic states applied to these pins select the appropriate interface for the desired IEEE–802.3 controller or enable the standby mode. When the standby mode is selected, the MC68160 power supply current is greatly reduced. Additionally, in the standby mode, all of the controller inputs and outputs are driven to the high impedance state.
6	LOOP	I TTL	**Diagnostic Loopback:** Asserting this function causes serial NRZ data at the TX input to be Manchester encoded and then looped back through the Manchester decoder, appearing at the RX output. This diagnostic loopback function operates independent of Twisted Pair (TP) or Access Unit Interface (AUI) port connectivity or activity. Neither the TP port nor the AUI port transmits data from the controller while diagnostic loopback is selected. Likewise, the controller interface receives data neither from the TP nor the AUI receivers while in this mode. The polarity fault detection and link integrity functions are not inhibited by the diagnostic loopback mode. If otherwise enabled, they continue to function. If the twisted pair port is selected, and TPSQEL is driven to the low logic state, a collision detect pulse is delivered following each transmission to simulate the twisted pair SQE test.
9	APORT	I TTL	**Automatic Port Selection Enable:** When high, MC68160 will automatically select the TP or AUI port based on the presence or absence of valid link beats or frames at the TP receive input. If the AUI port is automatically selected, the MC68160 will continue to produce link pulses for the TP port. Changing ports requires approximately 1.0 ms to allow the circuitry for the new port to resume normal operation. The power consumption is minimized in the circuitry associated with the unselected port.
27	TPSQEL	I TTL	**Twisted Pair Signal Quality Error Test Enable:** Forcing this pin low enables testing of the internal TP collision detect circuitry after each transmit operation to the TP media. This function provides a simulated collision to as much of the MC68160 collision detect circuitry as possible without affecting the attached twisted pair channel. A normal SQE test results in a high logic state at the CLSN controller interface pin which begins 6 to 16–bit times after the last transition of a transmitted signal and continues for 5 to 15–bit times. (When the AUI port is selected, SQE test signals are generated by the coaxial cable transceiver and delivered to the controller via the MC68160 ACX+/– receive inputs)
28	TPFULDL	I TTL	**Twisted Pair Full Duplex Mode Select:** Forcing this pin low allows simultaneous transmit and receive operation on the twisted pair port without an indicated collision. This pin is not to be asserted with LOOP as a test mode is enabled that disrupts normal operation.
29	TPAPCE	I TTL	**Twisted Pair Automatic Polarity Correction Enable:** When TPAPCE is high, automatic polarity correction is enabled, and MC68160 will internally correct for a polarity fault on the receive circuit. Additionally, when TPAPCE is high, the presence of a polarity fault is indicated on TPPLR.
46	TPEN	I/O TTL (TTL/CMOS)	**Twisted Pair Port Enable:** If APORT is low, TPEN is an input which determines whether the AUI port (TPEN low) or TP port (TPEN high) will be manually selected. If the AUI port is manually selected, the MC68160 will not produce link pulses for the TP port. If APORT is high, TPEN is an output which will indicate which port has been automatically selected by driving TPEN low (for AUI) or high (for TP). In its output mode TPEN can sink 10 mA in the low output state and source 10 mA in the high output state. (See Pin 9 Description.) Changing ports requires approximately 1.0 ms to allow the circuitry for the new port to resume normal operation. The power consumption is minimized in the circuitry associated with the unselected port. In the standby mode, this pin is driven to the high impedance state.

Table 1. Pin Function Description (continued)

Pin(s)	Symbol	Type	Name/Function
STATUS INDICATOR			
40	TXLED	O TTL/CMOS	**Transmit Status LED Driver Output:** This pin indicates the transmit status of the currently selected TP or AUI port. When there is no transmit activity detected, an internal pull–up takes this pin to its normal off (high) state. When transmit activity is detected, the LED driver turns on. In its on state, TXLED flashes the LED by driving low at approximately 10 Hz at a 50% duty cycle. In the standby mode, this output is driven to the high impedance state.
41	RXLED	O TTL/CMOS	**Receive Status LED Driver Output:** This pin indicates the receive status of the currently selected TP or AUI port. When there is no receive activity detected, an internal pull–up takes this pin to its normal off (high) state. When receive activity is detected, the LED driver turns on. In its on state, RXLED flashes the LED by driving low at approximately 10 Hz at a 50% duty cycle. In the standby mode, this output is driven to the high impedance state.
42	CLLED	O TTL/CMOS	**Collision Status LED Driver Output:** This pin indicates the collision status of the currently selected TP or AUI port. When there is no collision activity detected, an internal pull–up takes this pin to its normal off (high) state. When collision activity is detected, the LED driver turns on. In its on state, CLLED flashes the LED by driving low at approximately 10 Hz at a 50% duty cycle. In the standby mode, this output is driven to the high impedance state.
43	TPLIL	O TTL/CMOS	**Twisted Pair Link Integrity Output:** This output is driven to the low output state to indicate good link integrity on the TP port during TP mode. It is deasserted (high) when link integrity fails in TP mode. The TPLIL output is driven to the high impedance state when the AUI port is selected. In the standby mode, this output is also driven to the high impedance state.
44	TPPLR	O TTL/CMOS	**Twisted Pair Polarity Error Output:** If TPAPCE is high and the wires connected to the Twisted Pair Receiver Inputs (TPRX+, TPRX–) are reversed, TPPLR will be driven to the low logic state to indicate the fault. TPPLR remains low when the MC68160 has automatically corrected for the reversed wires. If the twisted pair link integrity tests fail, this output will be driven to the high logic state. When the AUI mode is selected this output is driven to the high impedance state. In the standby mode, this output is also driven to the high impedance state.
45	TPJABB	O TTL/CMOS	**Twisted Pair Jabber Output:** This pin is driven high to indicate a jabber condition at the TPTX+/– outputs. (Jabber condition also causes CLLED to be driven alternately to the high and low output levels). TPJABB is driven to the low output state when no jabber condition is present. When the AUI mode is selected this output is driven to the high impedance state. In the standby mode, this output is also driven to the high impedance state.
POWER SUPPLY AND GROUND			
10	VDDDIV		**Frequency Divider Supply Pin**
11 13	VDDFM GNDFM		**Frequency Multiplier Supply and Ground Pins**
14 15	GNDVCO VDDVCO		**Voltage Controlled Oscillator Ground and Supply Pins**
20	GNDSUB		**Substrate Ground Pin**
7 8 18 19	VDDDIG GNDDIG VDDDIG GNDDIG		**Digital Supply and Ground Pins**
30 33	VDDANA GNDANA		**Analog Supply and Ground Pins**
34 35 38 39	GNDPWR VDDPWR VDDPWR GNDPWR		**Power Supply and Ground Pins**
47	GNDCTL		**Controller Interface Ground Pin**

NOTE: Power and ground pins are not connected internally. Failure to connect externally may cause malfunction or damage to the IC.

Table 2. Controller Interface Selection

Motorola Transceiver MC68160 (EEST™)	Motorola Controller[2] MC68360 (QUICC™)		Intel Controllers 82586, 82590, 82593, 82596		Fujitsu Controllers 86950 (Etherstar™) 86960 (NICE™)		National Controllers 8390, 83C690, 83932B (SONIC™)	
CS0 CS1 CS2	1 1 0		0 1 0		1 0 0		0 0 0	
Pin	**Pin**	**Sense**	**Pin**	**Sense**	**Pin**	**Sense**	**Pin**	**Sense**
TCLK	TCLK	High	$\overline{\text{TXC}}$	Low	TCKN	Low	TXC	High
TX	TX	High	TXD	High	TXD	High	TXD	High
TENA	TENA	High	$\overline{\text{RTS}}$	Low	TEN	High	TXE	High
RCLK	RCLK	High	$\overline{\text{RXC}}$	Low	RCN	Low	RXC	High
RX	RX	High	RXD	High	RXD	High	RXD	High
RENA	RENA	High	$\overline{\text{CRS}}$	Low	XCD	High	CRS	High
CLSN	CLSN	High	$\overline{\text{CDT}}$	Low	XCOL	Low	COL	High
LOOP[1]	N.A.	High	$\overline{\text{LPBK}}$	Low	LBC	High	LPBK	High

NOTES: 1. Although LOOP input is not ordinarily classifed as a controller pin, it is included in this table because its sense varies according to the controller used.
2. The Motorola controller interface contained in the MC68360 (QUICC™) is compatible with the AMD 7990 (LANCE™) and 79C900 (ILACC™) controllers.
3. The pin sense is shown from the perspective of the identified controller pin.

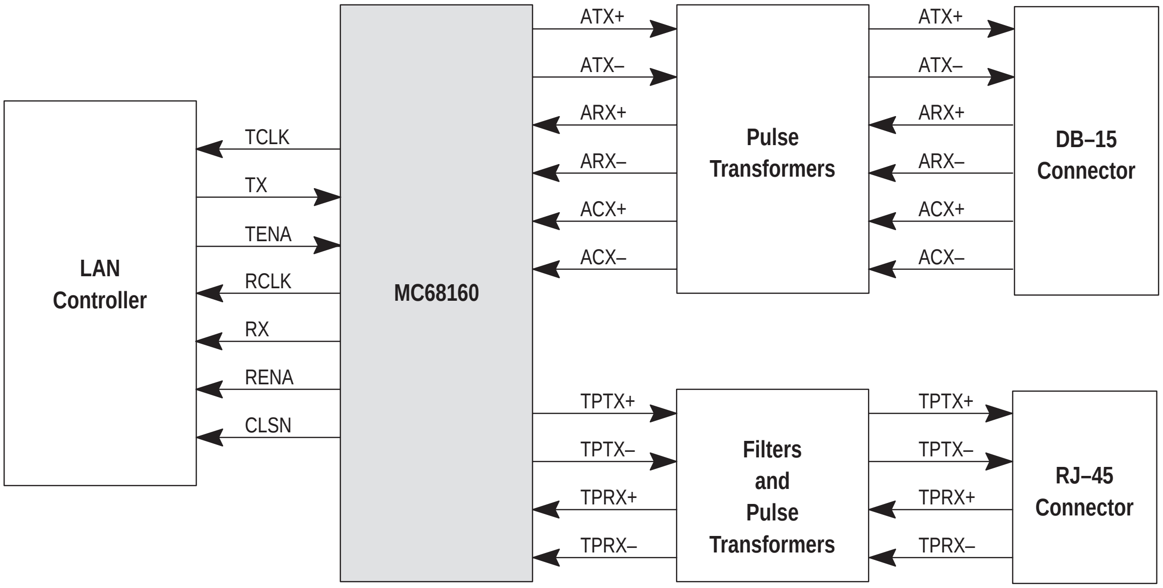
Table 3. Controller Independent Mode Selection

Pin	Standby Mode	Reserved	Reserved	Reserved
CS0 CS1 CS2	1 1 1	0 1 1	1 0 1	0 0 1

NOTE: In standby mode, the MC68160 consumes less power supply current than in any other mode. Additionally, in the standby mode, all of the controller inputs and outputs are driven to the high impedance state. When the standby mode is deasserted, an internal reset pulse of approximately 6.0 µs duration is generated.

Following a period of operation in the standby mode, the time required to insure stable data reception is approximately 100 ms.

Figure 2. Applications Block Diagram



ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS

Characteristic	Symbol	Min	Max	Unit
Storage Temperature Range	T_{stg}	–65	150	°C
Power Supply Voltage Range Analog Digital	 V_{DDA} V_{DDD}	 – –	 7.0 7.0	V
Voltage on any TTL compatible input pin with respect to Ground Voltage on TPRX, ARX, or ACX input pins with respect to Ground	V	–0.5 –0.5	V_{DD} + 0.5 6.0	V
Differential Voltage on TPRX, ARX, or ACX Input Pins	V_{DIFF}	–6.0	6.0	V

NOTE: Stresses in excess of the Absolute Maximum Ratings can cause permanent damage to the device. Functional operation of the device is not implied at these or any other conditions in excess of those indicated in the operation sections of this data sheet. Exposure to Absolute Maximum Ratings conditions for extended periods can adversely affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Min	Max	Unit
Power Supply Voltage Range	V_{DD}	4.75	5.25	V
Power Supply Ripple (20 kHz to 100 kHz)	–	–	50	mV
Power Supply Impulse Noise (Either Polarity)	–	–	100	mV
Ambient Operating Temperature Range	T_A	0	70	°C
ARX/ACX Input Differential Rise and Fall Time (see Figure 39)	t_{260}	2.0	10	ns
ARX Pair Idle Time after Transmission (see Figure 39)	t_{265}	8.0	–	µs

ESD

Although protection circuitry has been designed into this device, proper precautions should be taken to avoid exposure to electrostatic discharge (ESD) during handling and mounting. Motorola employs a Human Body Model (HBM) and a Charged Device Model (CDM) for ESD–susceptibility testing and protection design evaluation. ESD has been adopted for the CDM, however, a standard HBM (resistance = 1500 Ω capacitance – 100 pF) is widely used and, therefore, can be used for comparison purposes. The HBM ESD threshold presented here was obtained by using the circuit parameters contained in this specification. ESD threshold voltage is designed to 1.0 kV Human Body Model.

DC ELECTRICAL CHARACTERISTICS (Unless otherwise noted, minimum and maximum limits apply over the recommended ambient operating temperature and power supply voltage ranges.)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
POWER SUPPLY						
Undervoltage Shutdown Threshold	–	–	–	–	4.4	V
Power Supply Current	I_{DD}	– Standby Mode	– –	145 –	200 5.0	mA

DC ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0 V ± 5%. Unless otherwise noted, minimum and maximum limits apply over the recommended ambient operating temperature and power supply voltage ranges.)

Characteristic	Symbol	Test Conditions	Min	Max	Unit
TTL COMPATIBLE INPUTS					
TTL Compatible Input Voltage		–			V
Low State	V_{IL}(TTL)		–	0.8	
High State	V_{IH}(TTL)		2.0	–	
Input Current TTL Compatible Input Pins (Note 1)		0 V < V_I < V_{DD}	–	±10	μA
Input Current TENA TTL Compatible Input Pin: with Pull–Down Resistor					
I_{IH}	I_{IH}		–	+200	
I_{IL}	I_{IL}		–	–20	
with Pull–Down Resistor removed in Standby Mode	I_{IH} & I_{IL}		–	±10	
CMOS COMPATIBLE INPUTS					
CMOS Compatible Input Voltage		–			V
Low State	V_{IL}(CMOS)		–	1.0	
High State	V_{IH}(CMOS)		3.0	–	
Input Current (Pin X1)	I_{IH} & I_{IL}	0 V < V_I < V_{DD}	–	±100	μA
TTL/CMOS COMPATIBLE OUTPUTS					
TTL/CMOS Compatible Output Voltage	V_{OL}				V
Low State (Note 2)		I_{OL} = 4.0 mA	–	0.45	
Low State (Note 3)		I_{OL} = 10 mA	–	0.45	
TTL/CMOS Compatible Output Voltage	V_{OH}				V
High State (Note 4)		I_{OH} = –500 μA	3.9	–	
High State (Note 5)		I_{OH} = –10 mA	3.9	–	
High State (Note 2)		I_{OH} = –4.0 mA	2.4	–	
Three State Output Leakage Current	I_{OZ}	0 V ≤ V_{OZ} ≤ V_{DD}	–	±10	μA

Characteristic	Symbol	Test Conditions	Min	Max	Unit
TWISTED PAIR RECEIVER INPUTS					
Input Voltage Range (DC + AC)	V_{ITP}	–	1.5	4.3	V
Differential Input Squelch Threshold Voltage	V_{ITPSQ}	Note 10	270	390	mV
Common Mode Bias Generator Voltage	V_{BCMTP}	Note 9	1.8	3.2	V
Common Mode Input Resistance	R_{CMTP}	–	1000	–	Ω
Differential Input Resistance	R_{DIFFTP}	–	2.5	–	kΩ
TWISTED PAIR TRANSMITTER OUTPUTS					
Differential Output Voltage		Note 7			V
Pre–Emphasis Level	V_{ODFTPP}		±2.2	±2.8	
Signal Level	V_{ODFTPS}		±1.56	±1.98	
Common Mode Output Voltage Range	V_{OCMTP}	Note 6	0	4.0	V
Common Mode Output Voltage in Standby Mode	$V_{OCMTPSB}$	I_{OH} = –100 μA	V_{DD} – 1.0	V_{DD}	V
Differential Output Voltage					
IDLE Mode	V_{ODFTPI}	Note 6	–	±50	mV
Open Circuit	V_{ODFTPO}	Note 8	–	5.25	V
Differential Output Impedance		Note 8			Ω
TRANSMISSION Mode	R_{ODFTPT}		12	28	
IDLE Mode	R_{ODFTPI}		8.0	29	

NOTES:
1. APORT, TPAPCE, CS0, CS1, CS2, TX, LOOP, TPFULDL, TPSQEL and TPEN (In Input Mode).
2. TCLK, RX, RCLK, RENA and CLSN.
3. TPPLR, TPLIL, TPJABB, TXLED, RXLED, CLLED and TPEN (In Output Mode).
4. TPPLR, TPLIL, CLLED, TXLED and RXLED.
5. TPJABB and TPEN (In Output Mode).
6. Measured with Test Load B1 (shown in Figure 3), applied directly to the TPTX+/– pins of the device.
7. Measured differentially with Test Load B2 (shown in Figure 4), applied directly to the TPTX+/– pins of the device.
8. Measured directly on the TPTX+/– pins of the device.
9. Measured with Test Load B3 (shown in Figure 5), applied directly to the TPRX+/– pins of the device.
10. The Common Mode Input Voltage is between 1.8 V and 3.2 V.

Characteristic	Symbol	Test Conditions	Min	Max	Unit
TWISTED PAIR TRANSMITTER OUTPUTS					
Common Mode Output Impedance TRANSMISSION Mode IDLE Mode	 R_{OCMTPT} R_{OCMTPI}	Note 8	 3.0 1.0	 7.0 10	 Ω kΩ

NOTES:
1. APORT, TPAPCE, CS0, CS1, CS2, TX, LOOP, TPFULDL, TPSQEL and TPEN (In Input Mode).
2. TCLK, RX, RCLK, RENA and CLSN.
3. TPPLR, TPLIL, TPJABB, TXLED, RXLED, CLLED and TPEN (In Output Mode).
4. TPPLR, TPLIL, CLLED, TXLED and RXLED.
5. TPJABB and TPEN (In Output Mode).
6. Measured with Test Load B1 (shown in Figure 3), applied directly to the TPTX+/– pins of the device.
7. Measured differentially with Test Load B2 (shown in Figure 4), applied directly to the TPTX+/– pins of the device.
8. Measured directly on the TPTX+/– pins of the device.
9. Measured with Test Load B3 (shown in Figure 5), applied directly to the TPRX+/– pins of the device.
10. The Common Mode Input Voltage is between 1.8 V and 3.2 V.

DC ELECTRICAL CHARACTERISTICS (Unless otherwise noted, minimum and maximum limits apply over the recommended ambient operating temperature and power supply voltage ranges.)

Characteristic	Symbol	Test Conditions	Min	Max	Unit
AUI RECEIVER INPUTS					
Input Voltage Range (DC + AC)	V_{IA}	–	1.0	4.2	V
Differential Mode Input Voltage Range	V_{IDFA}	–	±318	±1315	mV
Differential Input Squelch Threshold Voltage	V_{IASQ}	–	–275	–175	mV
Common Mode Input Resistance	R_{ICMA}	$1.0\ V < V_{ICMA} < 4.2\ V$	1.5	–	kΩ
Differential Input Resistance (ARX, ACX Inputs)	R_{IDFA}	$1.0\ V < V_{ICMA} < 4.2\ V$ $318\ mV < V_{IDMA} < 1315\ mV$	5.0	–	kΩ
AUI TRANSMITTER OUTPUTS					
Common Mode Output Voltage IDLE Mode ACTIVE Mode STANDBY Mode	 V_{OCMIA} V_{OCMAA} V_{OCMSA}	Figure 6 $I_O = –100\ \mu A$	 1.0 1.0 $V_{DD} – 2.0$	 4.2 4.2 $V_{DD} – 1.2$	V
Differential Output Voltage IDLE Mode ACTIVE Mode	 V_{ODFIA} V_{ODFAA}	Figure 6	 – ±600	 ±40 ±1315	mV
Differential Output Load Current IDLE Mode	I_{ODFIA}	Figure 7	 –	 ±4.0	mA
Output Short Circuit Current	I_{ODSA}	Output Short Circuited to V_{DD} or GND	–	±150	mA

Figure 3. Test Load B1

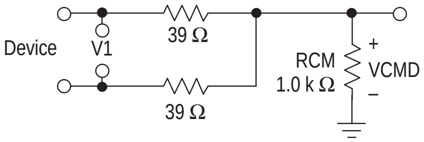


Figure 4. Test Load B2

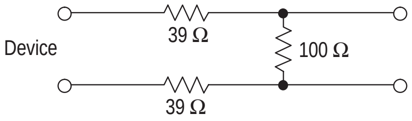
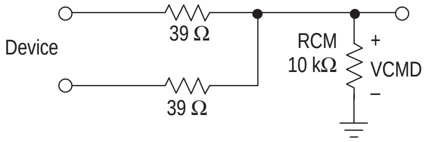


Figure 5. Test Load B3



NOTE: A total of 50 Ω per driver output is required for proper series line termination. This is realized with the 39 Ω external resistors shown in Figures 3, 4 and 5, together with the internal driver output resistance.

Figure 6. AUI Common Mode Termination

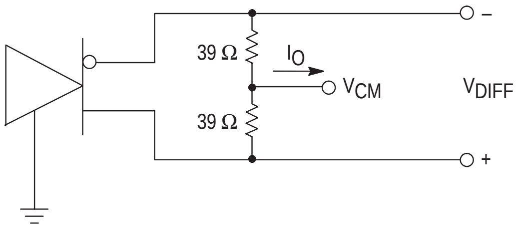
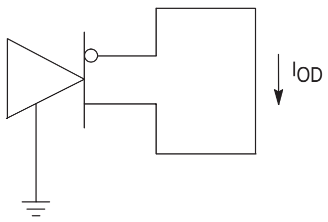


Figure 7. AUI Differential Output Short Circuit Current



AC ELECTRICAL CHARACTERISTICS (Unless otherwise noted, minimum and maximum limits apply over the recommended temperature and power supply voltage ranges.)

Characteristic	Symbol	Min	Max	Unit
EXTERNAL CLOCK INPUT (X1)				
Cycle Time (Note 1) (See Figure 8)	t_1	49.995	50.005	ns
Fall Time	t_2	–	5.0	
Rise Time	t_3	–	5.0	
Low Time	t_4	20	30	
High Time	t_5	20	30	
RECEIVE PHASE–LOCKED–LOOP SWITCHING				
Stabilization Time	t_7	–	100	ms
CONTROLLER TRANSMIT SWITCHING (MOTOROLA MODE)				
TCLK Cycle Time	t_{10}	99	101	ns
TCLK High Time	t_{11}	45	55	
TCLK Low Time	t_{12}	45	55	
TCLK Rise and Fall Time	t_{13}	–	8.0	
TX Setup Time to TCLK ↑	t_{14}	20	–	ns
TX Hold Time to TCLK ↑	t_{15}	0	–	
TENA Setup Time to TCLK ↑	t_{16}	20	–	ns
TENA Hold Time to TCLK ↑	t_{17}	0	–	
CONTROLLER RECEIVE SWITCHING				
RCLK Cycle Time	t_{20}	90	–	ns
RCLK High Time	t_{21}	42	–	
RCLK Low Time	t_{22}	47	55	
RCLK Rise and Fall Time	t_{23}	–	8.0	
RX Hold Time from RCLK ↑	t_{24}	10	–	ns
RX Set–Up Time to RCLK ↑	$t_{24.1}$	70	–	
RCLK Delay from RENA ↑	t_{25}	–	650	ns
RX Delay from RENA ↑	t_{26}	–	600	
RENA Deassertion Delay from RCLK ↑ (See Figure 12)	t_{27}	10	30	ns

NOTES: 1. To meet IEEE–802.3 specifications.
2. Load on specified output is 20 pF to ground, unless otherwise noted.
3. ↑ = Rising Edge

Figure 8. X1 Input Voltage Levels for Timing Measurements

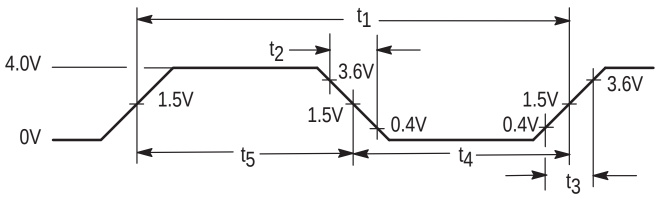
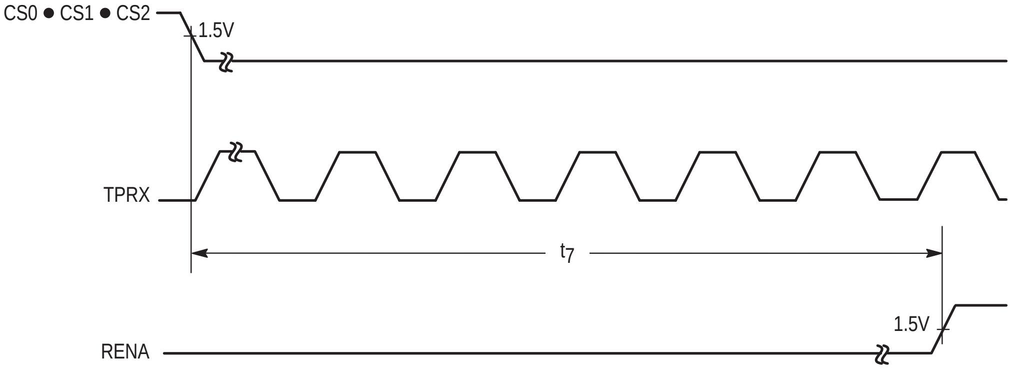


Figure 9. Receive Phase–Locked–Loop Switching



NOTE: CS0 • CS1 • CS2 is the logical AND operation and refers to the pins not at Logic 1.

Figure 10. Transmit Timing (Motorola Mode)

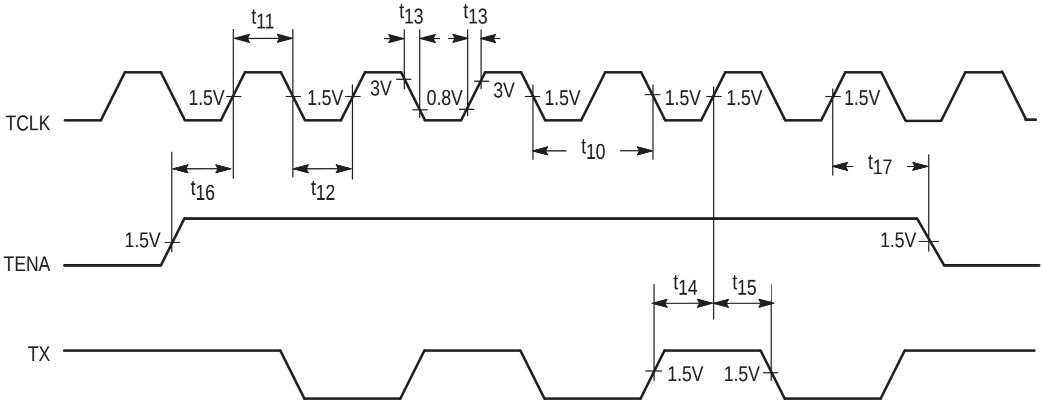


Figure 11. Receive Timing (Motorola Start of Frame)

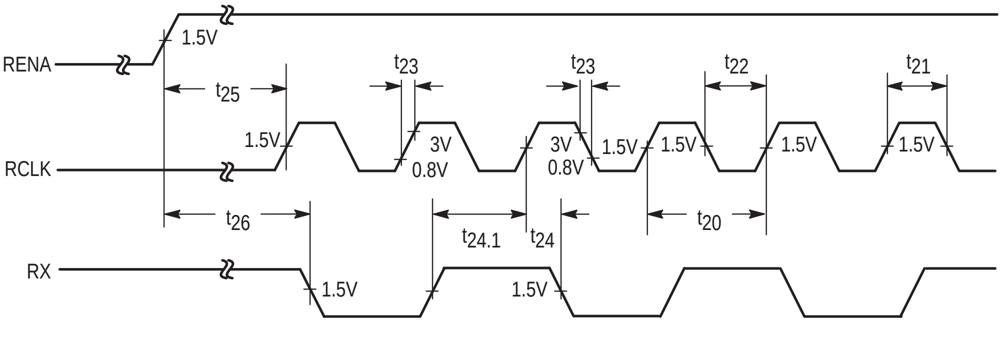
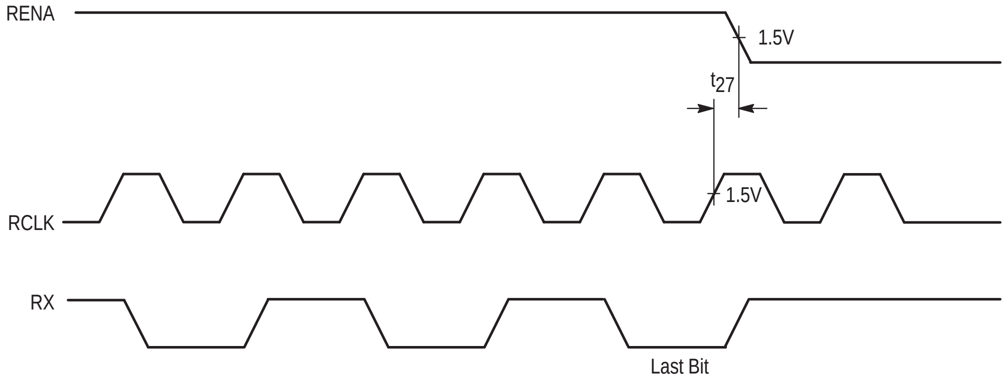


Figure 12. Receive Timing (Motorola End of Frame)



CONTROLLER TRANSMIT SWITCHING (Intel Mode)

Characteristic	Symbol	Min	Max	Unit
TXC Cycle Time	t_{40}	99	101	ns
TXC High and Low Time	t_{41}	40	–	
TXC Rise and Fall Time	t_{42}	–	5.0	
TXD Setup Time to TXC ↓	t_{43}	20	–	ns
TXD Hold Time to TXC ↓	t_{44}	0	–	
RTS Setup Time to TXC ↓	t_{45}	20	–	ns
RTS Hold Time to TXC ↓	t_{46}	0	–	

CONTROLLER RECEIVE SWITCHING

Characteristic	Symbol	Min	Max	Unit
RXC Cycle Time	t_{80}	90	–	ns
RXC High Time	t_{81}	45	55	
RXC Low Time	t_{82}	40	–	
RXC Rise and Fall Time	t_{83}	–	5.0	
RXD Hold Time from RXC ↓	t_{85}	50	–	ns
RXD Set–Up Time to RXC ↓	$t_{85.1}$	35	–	
CRS Delay from RXC ↑	t_{86}	12	30	

NOTE: Load on specified output is 20 pF to ground, unless otherwise noted.
↑ = Rising Edge
↓ = Falling Edge

Figure 13. Transmit Timing (Intel)

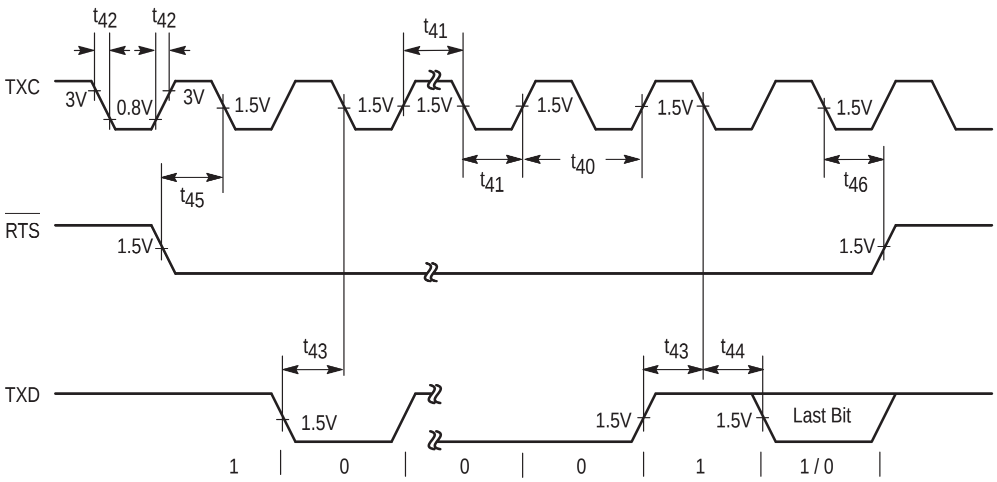
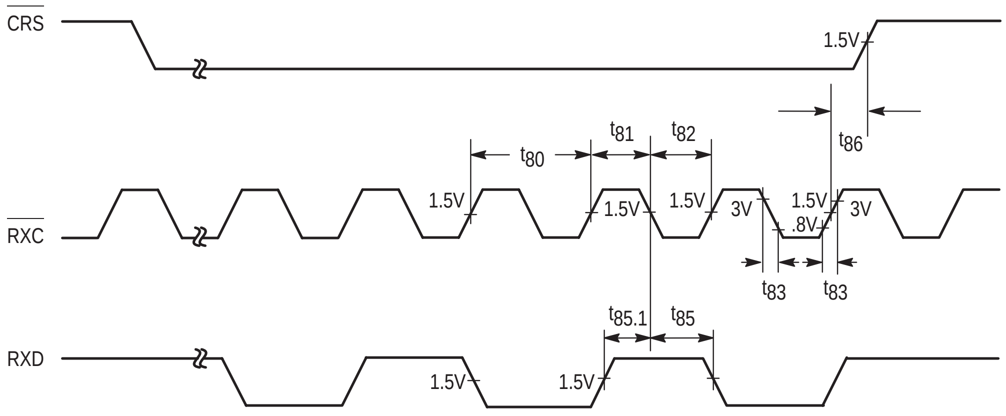


Figure 14. Receive Timing (Intel)



CONTROLLER TRANSMIT SWITCHING (Fujitsu Mode)

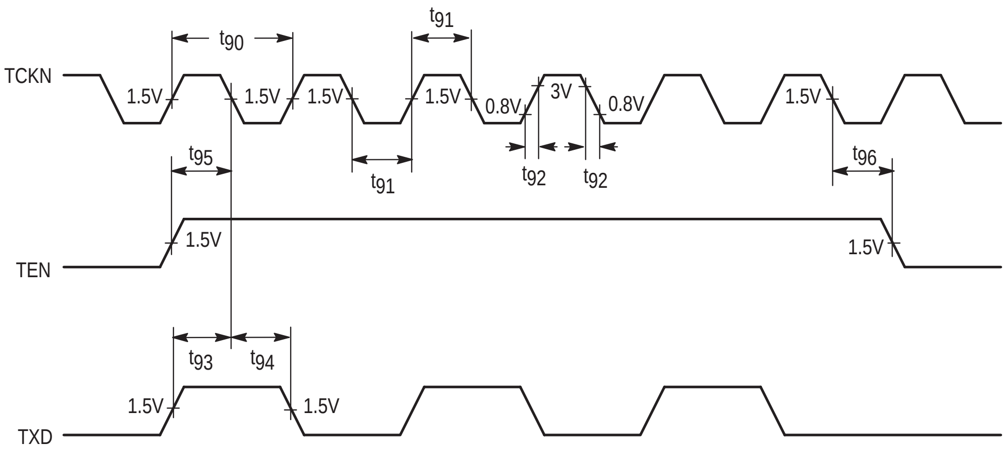
Characteristic	Symbol	Min	Max	Unit
TCKN Cycle Time TCKN High and Low Time TCKN Rise and Fall Time	t_{90} t_{91} t_{92}	99 45 –	101 55 8.0	ns
TXD Setup Time to TCKN ↓ TXD Hold Time to TCKN ↓	t_{93} t_{94}	20 0	– –	ns
TEN Setup Time to TCKN ↓ TEN Hold Time to TCKN ↓	t_{95} t_{96}	20 0	– –	ns

CONTROLLER RECEIVE SWITCHING

Characteristic	Symbol	Min	Max	Unit
RCKN Cycle Time RCKN High Time RCKN Low Time RCKN Rise and Fall Time	t_{100} t_{101} t_{102} t_{103}	90 40 45 –	– – 55 8.0	ns
RXD Hold Time from RCKN ↓ RXD Set–Up Time RCLK ↓ RCKN Delay from XCD ↑	t_{104} $t_{104.1}$ t_{105}	50 35 –	– – 600	ns
XCD Deassertion Delay from RCKN ↑ (See Figure 17)	t_{106}	0	–	ns

NOTE: Load on specified output is 20 pF to ground, unless otherwise noted.
↑ = Rising Edge
↓ = Falling Edge

Figure 15. Transmit Timing (Fujitsu)



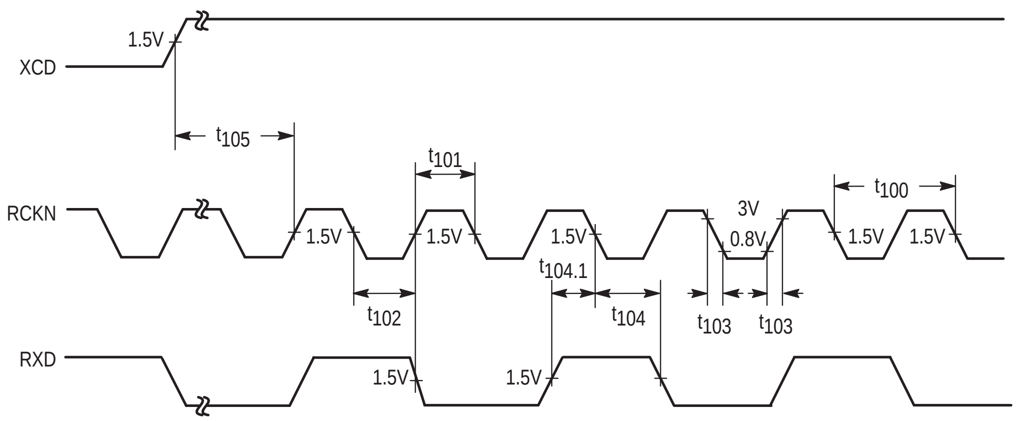


Figure 16. Receive Timing (Fujitsu Start of Frame)

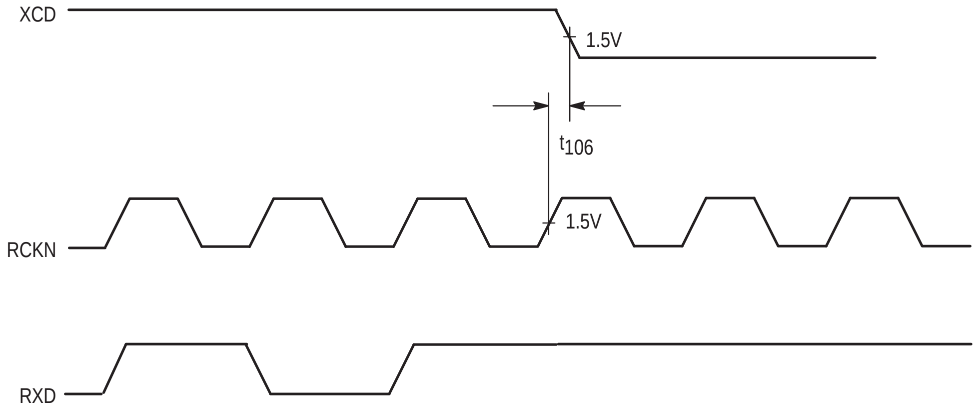


Figure 17. Receive Timing (Fujitsu End of Frame)

CONTROLLER TRANSMIT SWITCHING (National Mode)

Characteristic	Symbol	Min	Max	Unit
TXC Cycle Time TXC High and Low Time TXC Rise and Fall Time	t_{110} t_{111} t_{112}	99 45 –	101 55 8.0	ns
TXD Setup Time to TXC ↑ TXD Hold Time to TXC ↑	t_{113} t_{114}	20 0	– –	ns
TXE Setup Time to TXC ↑ TXE Hold Time to TXC ↑	t_{115} t_{116}	20 0	– –	ns

CONTROLLER RECEIVE SWITCHING

Characteristic	Symbol	Min	Max	Unit
RXC Cycle Time RXC Low Time RXC High Time RXC Rise and Fall Time	t_{120} t_{121} t_{122} t_{123}	90 40 40 –	– – 60 8.0	ns
RXD Hold Time from RXC ↑ RXD Set–Up Time from RXC ↑ RXC Delay from CRS ↑	t_{124} $t_{124.1}$ t_{125}	50 35 –	– – 600	ns
CRS Deassertion Delay from RXC ↓	t_{126}	0	15	ns
RXC continuing beyond CRS ↓	t_{127}	5.0	–	cycles

NOTE: Load on specified output is 20 pF to ground, unless otherwise noted.
↑ = Rising Edge
↓ = Falling Edge

Figure 18. Transmit Timing (National)

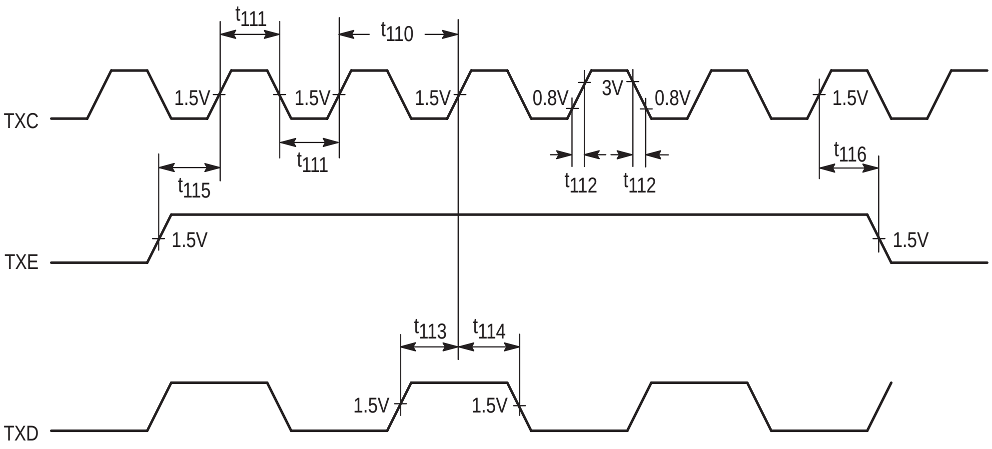
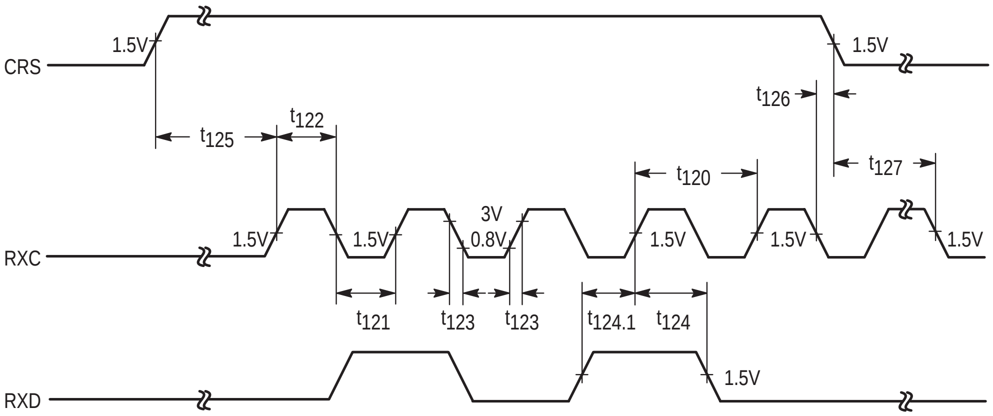


Figure 19. Receive Timing (National)



TP TRANSMIT SWITCHING

Characteristic	Symbol	Min	Typ	Max	Unit
TPTX Common Mode AC Output Voltage (Note 3)	V_{OCMTP}	–	–	50	mVrms
TX to TPTX Steady State Propagation Delay (Note 2) (See Figure 24)	t_{130}	–	–	200	ns
Bit Duration Center–to–Center	t_{131}	98	–	102	
Half–Bit Cell Duration Center–to–Boundary	t_{132}	48	–	52	
TENA Assert to RENA Assert Delay (Note 7) (See Figure 24)	t_{133}	–	–	400	ns
Internal Loopback Delay from TX to RX (Note 7) (See Figure 24)	t_{134}	–	–	450	ns
TPTX End of Packet Hold Time from last positive TPTX Signal Edge to +585 mV Differential Output Level (Note 5) (See Figure 25)	t_{135}	250	–	400	ns
TPTX Precompensation Pulse Width (Notes 2 and 6) (See Figure 25)	t_{136}	–	45–58	–	ns
RENA Deassert Delay from TENA Deassert when Receiver is inactive					ns
Motorola Mode	t_{137}	250	–	450	
Fujitsu Mode					
National Mode					
Intel Mode (Note 4) (See Figure 26)	t_{138}	250	–	450	
TPTX Data–to–Link Test Pulse (Note 2) (See Figure 27)	t_{139}	8.0	–	24	ms
TPTX Link Test Pulse Width (Note 2)	t_{140}	80	–	240	ns
TPTX Link Test Pulse Decay–to–Idle Condition (Note 1)	t_{141}	80	–	240	ns
TPTX Link Test Pulse to next Link Test Pulse (Note 2)	t_{142}	8.0	–	24	ms

NOTES:
1. Measured differentially across the output of Test Load A which is connected directly to the TPTX+/– pins of the device.
2. Measured differentially across the output of Test Load D shown in Figure 23 which is connected directly to the TPTX+/– pins of the device.
3. Measured across the output of Test Load C which is connected directly to the TPTX+/– pins of the device.
4. Same as t_{137} except the logic states for TENA and RENA are inverted.
5. Measured across the output of Test Load B shown in Figure 21.
6. Measured at the +/–90% points of the precompensation voltage feature of the waveform. (The 0% reference is 0 V differential.)
7. Load on specified output is 20 pF to ground.

Figure 20. Test Load A

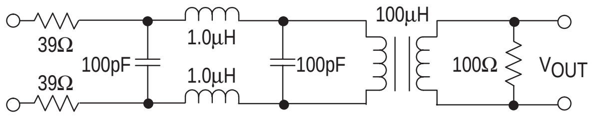


Figure 21. Test Load B

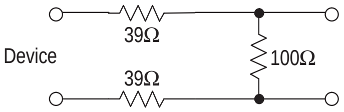


Figure 22. Test Load C

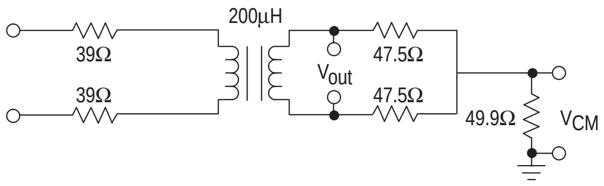
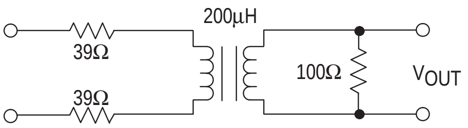


Figure 23. Test Load D



NOTE: A total of 50 Ω per driver output is required for proper series line termination. This is realized with the 39 Ω external resistors shown in Figures 20 to 23, together with the internal driver output resistance.

Figure 24. TPTX Transmit Timing (Start of Frame) Switching

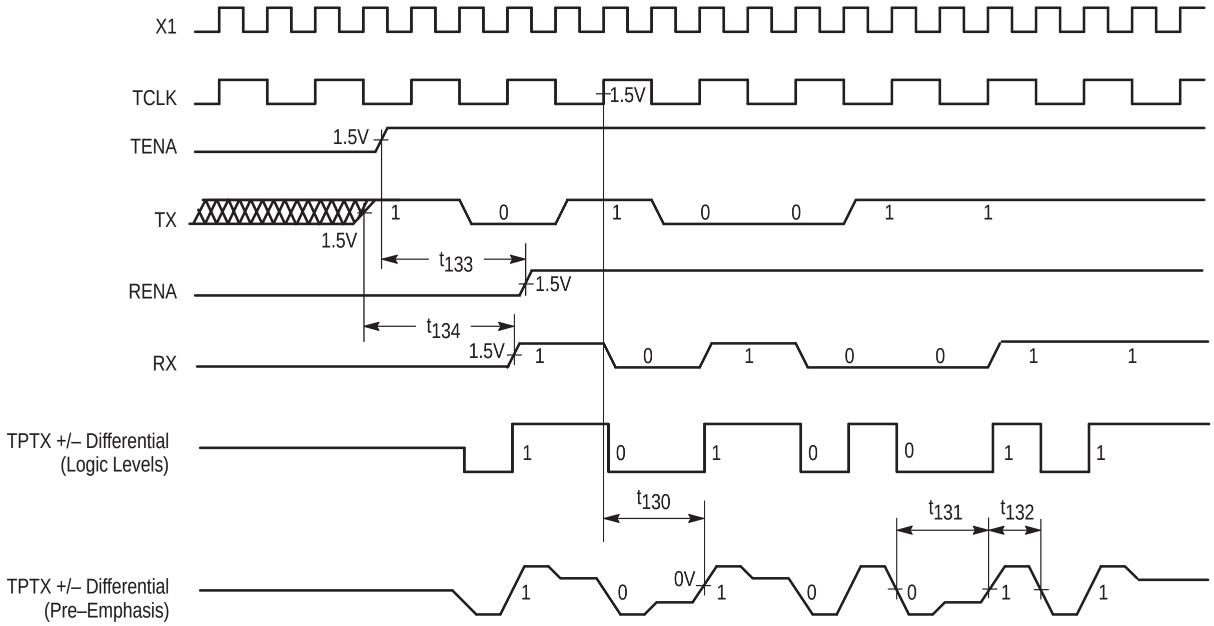


Figure 25. TPTX Transmit Timing (End of Frame) Switching

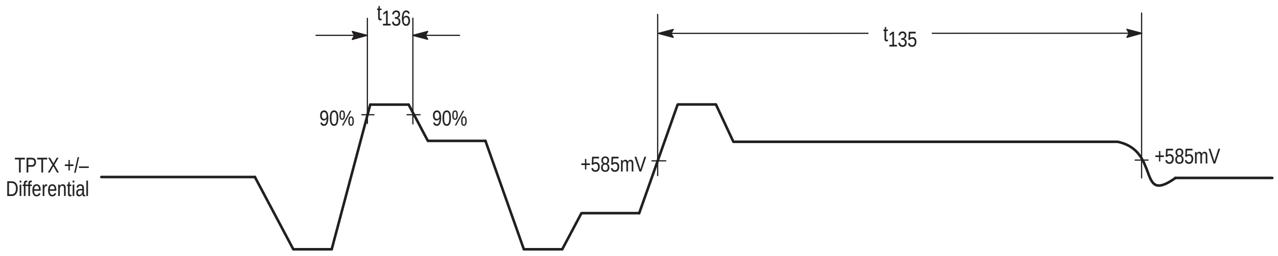


Figure 26. RENA Deassert Delay from TENA

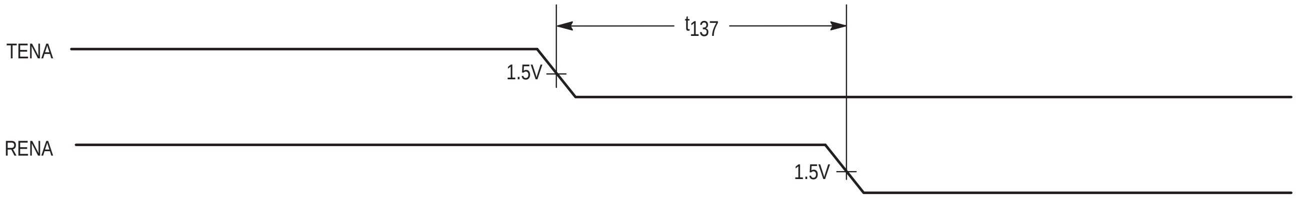
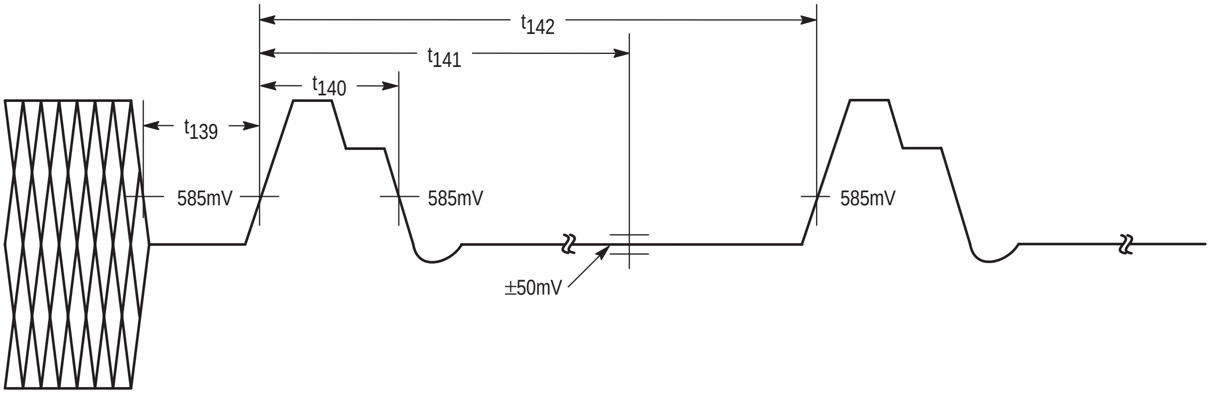


Figure 27. TPTX+/– Link Pulse Timing



TP TRANSMIT JABBER SWITCHING

Characteristic	Symbol	Min	Max	Unit
Max Length of Transmission before Assertion of TPJABB to indicate Jabber Condition CLSN to indicate Jabber Condition	 t_{160} t_{161}	 20 20	 60 60	ms
Time from End of Jabber Condition to Deassertion: of TPJABB of CLSN	 t_{162} t_{163}	 500 500	 750 750	ms

TP TRANSMIT SIGNAL QUALITY ERROR TEST SWITCHING

CLSN (Signal Quality Error Test) (See Figure 29) Assertion from last positive TPTX edge Deassertion from last positive TPTX edge Pulse Width	 t_{170} t_{171} t_{172}	 0.6 – 0.5	 1.6 3.1 1.5	µs
TPSQEL Disable Delay Time (See Figure 29)	t_{173}	–	40	ns

NOTE: The load attached to the specified output is a 20 pF capacitor connected to ground, unless otherwise noted.

Figure 28. TPJABB Switching

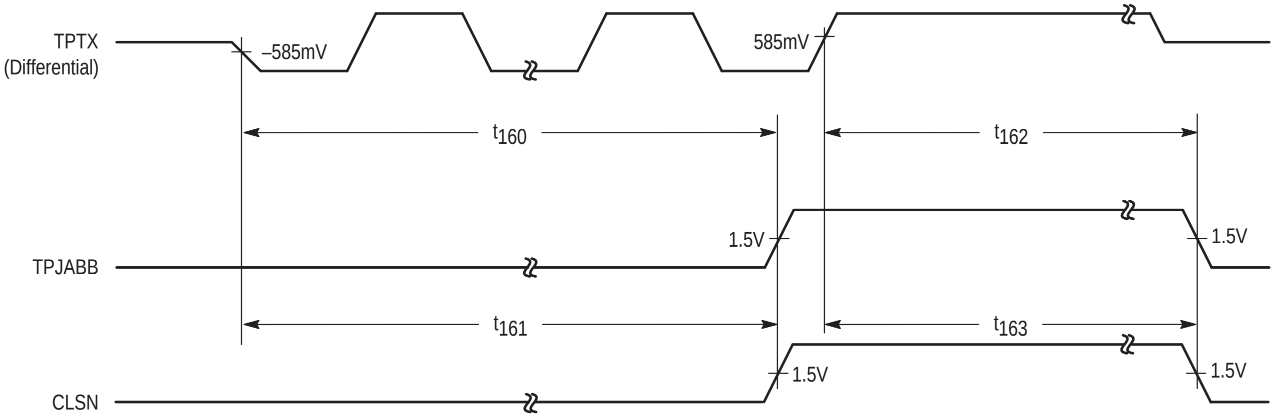
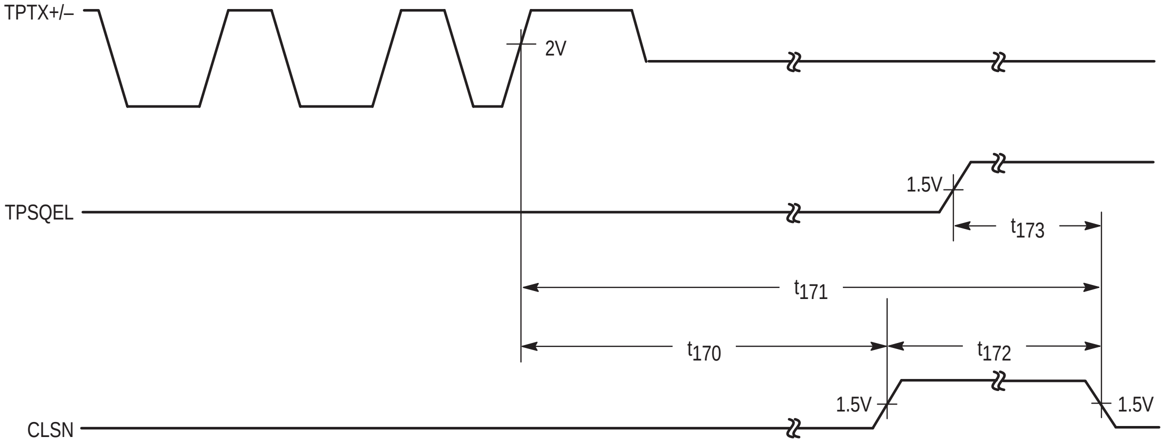


Figure 29. TPTX SQE (CLSN) Timing (End of Frame)



TP RECEIVE SWITCHING

Characteristic	Symbol	Min	Max	Unit
Differential Input Voltage Range Unconditional Squelch (Note 1) (1.8 V < Input Common Mode Voltage < 3.2 V)	V_{IDFSTP}	0	|264|	mV
Positive or Negative Differential Input Pulse Width for Conditional Receive Unsquelch (See Figure 31)	t_{180}	20	30	ns
TPRX to RCLK Bit Loss at start of packet (See Figure 32)	t_{181}	–	10	Bits
TPRX to RCLK Steady State Propagation Delay (See Figure 32)	t_{182}	–	400	ns
TPRX to RX Start Up Delay (See Figure 32)	t_{183}	–	1.5	µs
TPRX held high from last valid positive transition (See Figure 33)	t_{186}	230	–	ns
RENA Deassertion Delay from last valid positive transition of TPRX Pair (See Figure 33)	t_{187}	–	350	ns

TP RECEIVE LINK INTEGRITY SWITCHING

Characteristic	Symbol	Min	Max	Unit
Required Pulse Width Range to be recognized as a Link Pulse (Note 2)	t_{200}	50	200	ns
Last TPRX activity to high state TPLIL Output (Receive Link Loss Timeout Interval)	t_{201}	100	150	ms
Receive Link Beat Separation				ms
Minimum Range (Note 3)	t_{202}	3.0	7.0	
Maximum Range (Note 4)	t_{203}	100	150	

NOTES: 1. Measured with Test Load H attached to the receive pins.
2. Measured at the receive pins.
3. Link beats closer in time to this range of values are considered noise, and are rejected.
4. Link beats further apart in time than this range of values are not considered consecutive, and are rejected.

Figure 30. Test Load H

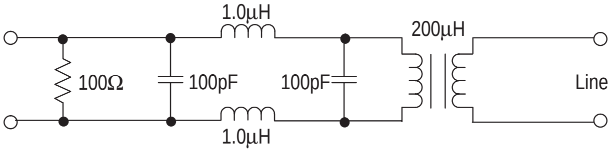


Figure 31. TPRX Input Switching

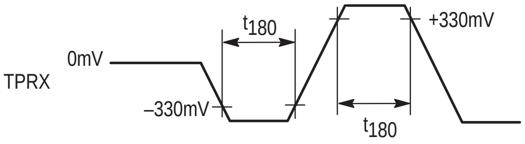


Figure 32. TPRX Receive Timing (Start of Frame)

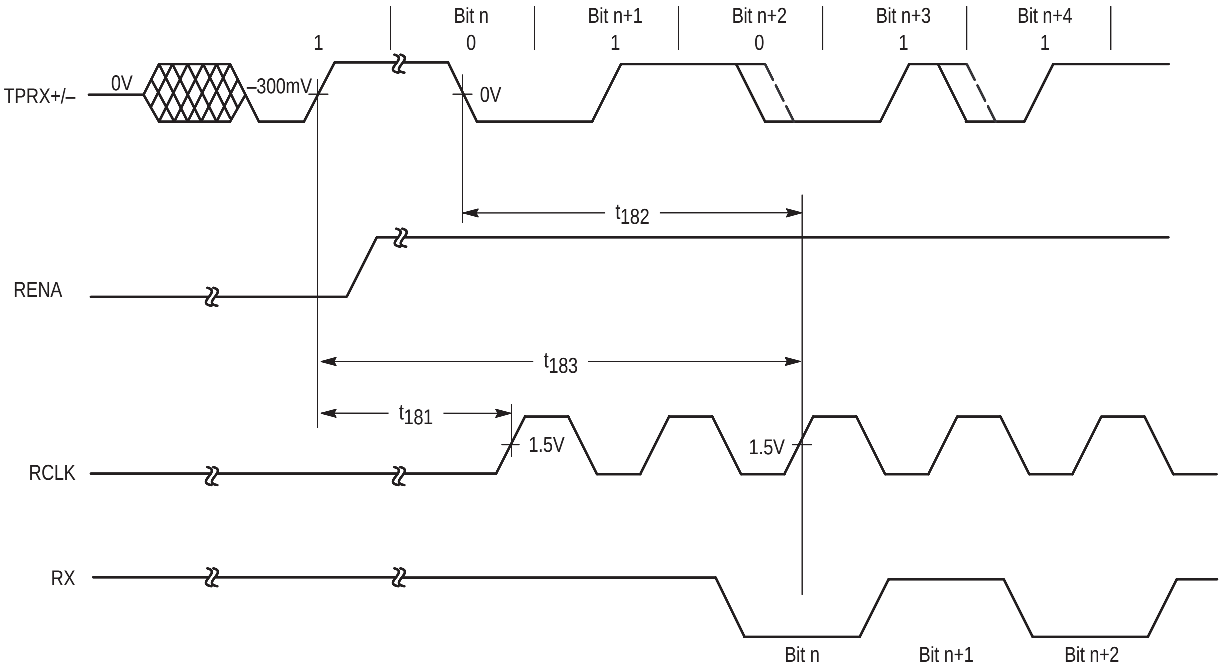


Figure 33. RENA Deassertion Delay from Last Valid Positive Transition of TPRX Pair

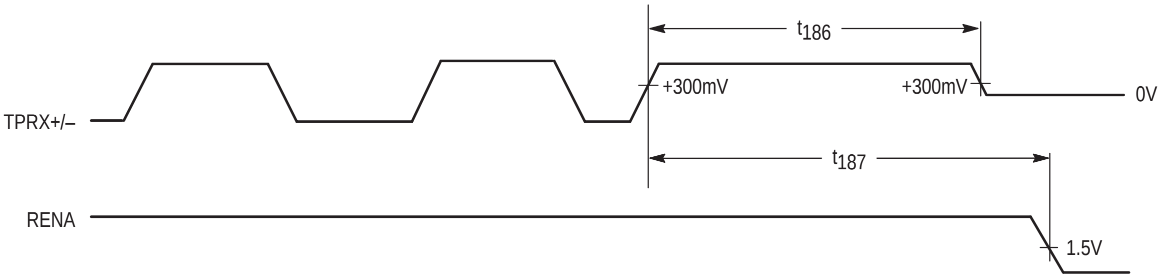
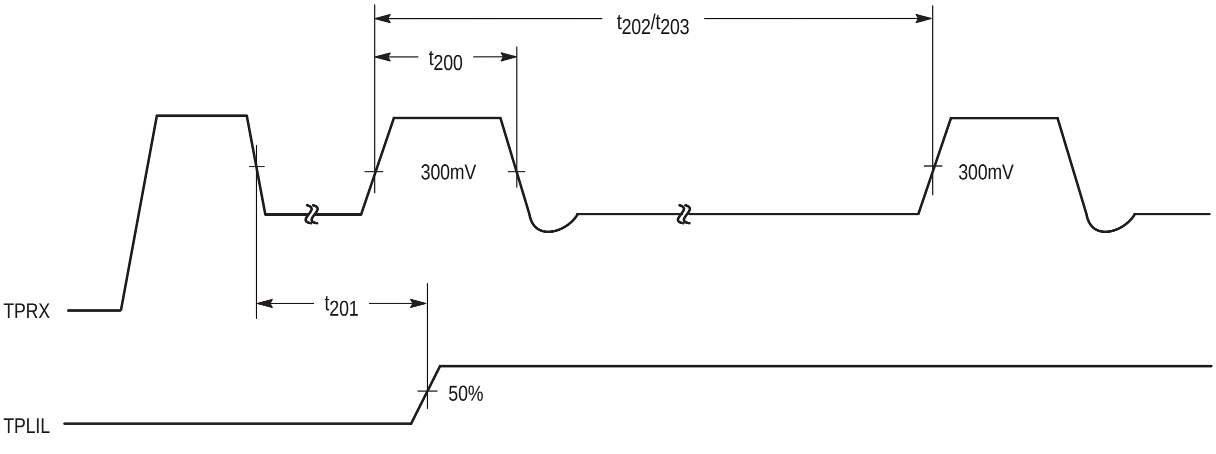


Figure 34. TP Receive Link Integrity Switching



TP COLLISION SWITCHING

Characteristic	Symbol	Min	Max	Unit
Time from collision (TPRX activity caused assertion of RENA followed by assertion of TENA) to assertion of CLSN	t_{210}	–	300	ns
Time from end of collision (Deassertion of TENA with uninterrupted TPRX pair activity) to deassertion of CLSN	t_{211}	350	900	

TP FULL DUPLEX SWITCHING

Characteristic	Symbol	Min	Max	Unit
TPFULDL assert to collision detect disable (See Figure 36)	t_{220}	–	50	ns
TPFULDL deassert to collision detect enable	t_{221}	–	50	
TPFULDL assert to data loop back disable (See Figure 37)	t_{222}	–	350	ns
TPFULDL deassert to data loop back enable	t_{223}	–	150	

NOTE: Load on specified output is 20 pF to ground, unless otherwise noted.

Figure 35. TPTX Collision Timing

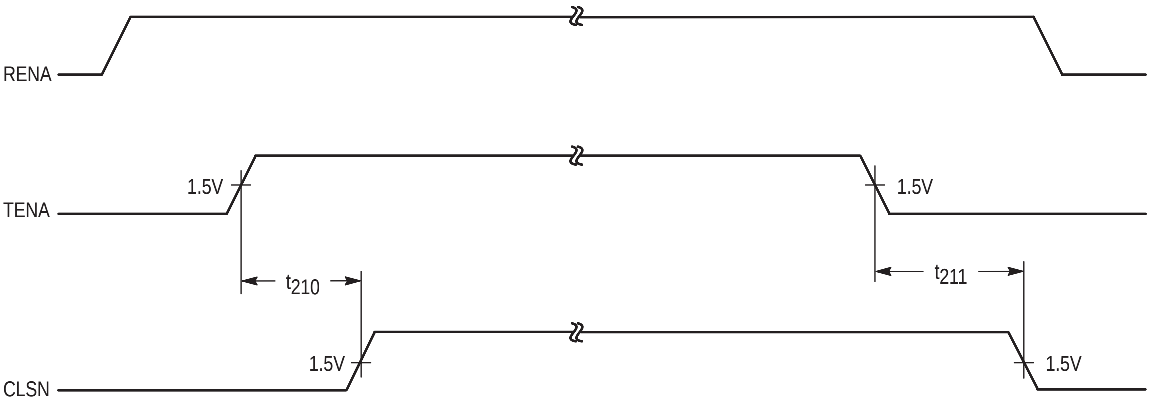


Figure 36. TPTX Full Duplex Timing

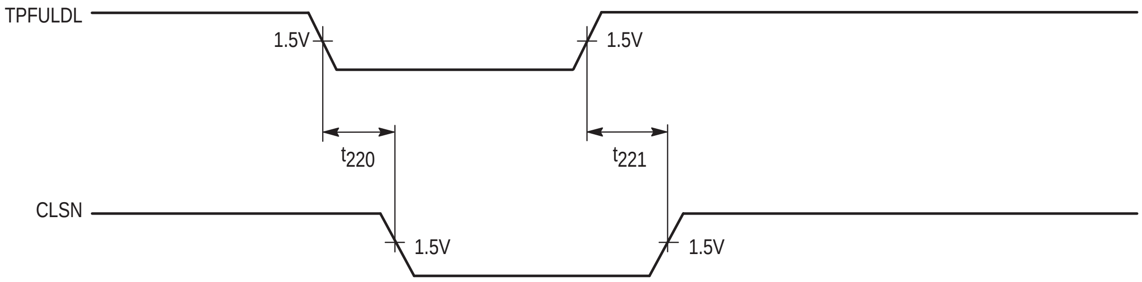
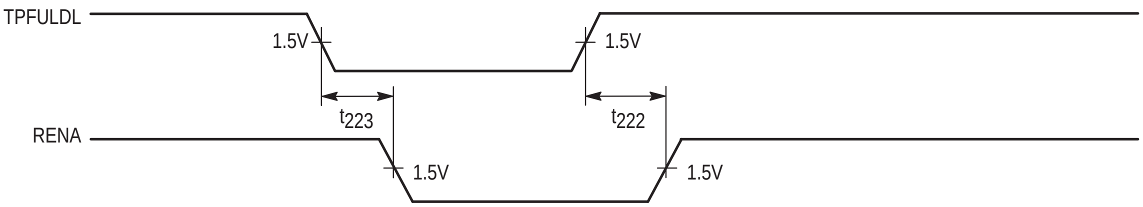


Figure 37. TPTX Full Duplex Timing

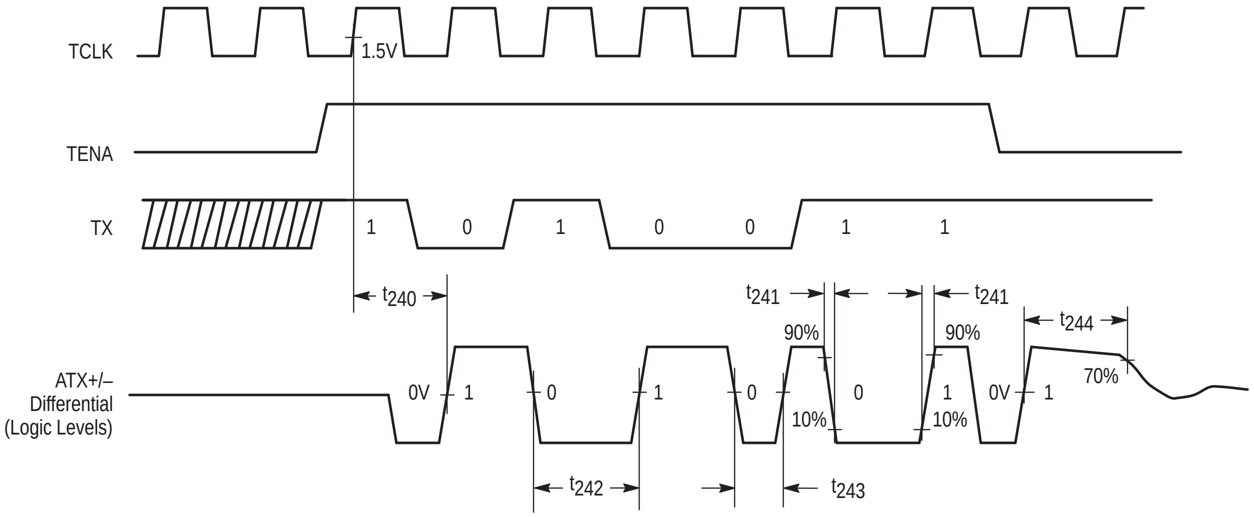


AUI TRANSMIT SWITCHING

Characteristic	Symbol	Min	Typ	Max	Unit
TCLK to ATX Pair Steady State Propagation Delay	t_{240}	–	–	100	ns
Output Differential Rise and Fall Times (Measured directly at device pins)	t_{241}	1.0	–	5.0	ns
ATX Bit Cell Duration center–to–center (Measured directly at device pins)	t_{242}	–	99.5–100.5	–	ns
ATX Half–Bit Cell Duration center–to–boundary (Measured directly at device pins)	t_{243}	–	49.5–50.5	–	ns
ATX Pair Held at Positive Differential at start of Idle (Measured through transformer)	t_{244}	200	–	–	ns

NOTE: Load on specified output is a shunt 27 μH inductor and 83 Ω resistor.

Figure 38. ATX Transmit Timings



AUI RECEIVE SWITCHING

Characteristic	Symbol	Min	Max	Unit
ARX/ACX Differential Input Voltage Range	–	±318	±1315	mV
ARX/ACX Differential Input Pulse Width to: Initiate Data Reception Inhibit Data Reception	 t_{261} t_{262}	 30 –	 – 18	ns
RENA Assertion Delay RENA Deassertion Delay	t_{266} t_{267}	– –	100 450	ns

Squelching Characteristics

The receive data pairs and the collision pairs should have the following squelch characteristics:

1. The squelch circuits are on at idle (with input voltage at approximately 0 V differential).
2. If an input is in squelch, pulse is rejected if the peak differential voltage is more positive than –175 mV, regardless of pulse width.
3. A pulse is considered valid if its peak differential voltage is more negative than –300 mV and its width, measured at –285 mV, is > 25 ns.
4. The squelch circuits are disabled by the first valid negative differential pulse on either the AUI receive data or collision pair.
5. If a positive differential pulse occurs on either the AUI receive data or collision pair > 175 ns, end of frame is assumed and squelch circuitry is turned on.

Figure 39. ARX/ACX Timing

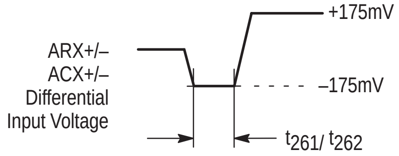
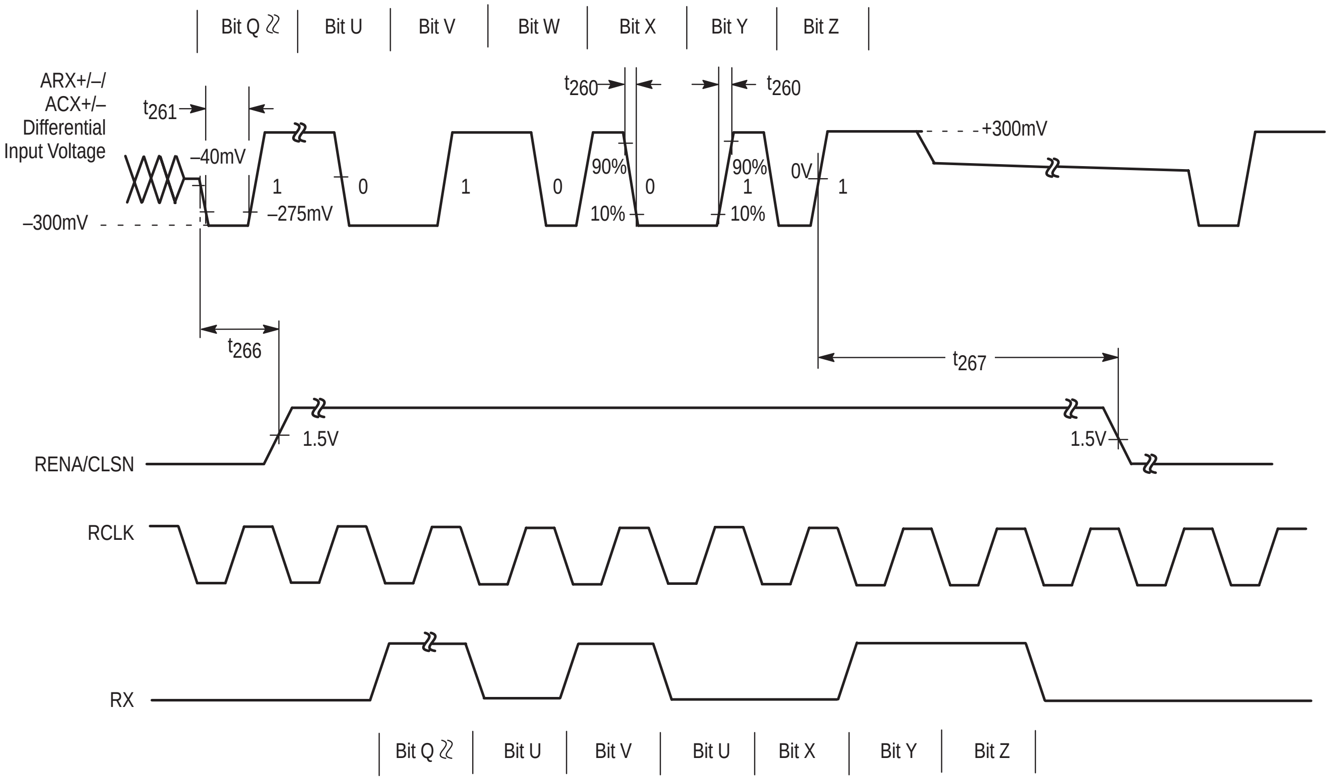


Figure 40. ARX/ACX Timing



FUNCTIONAL DESCRIPTION

Introduction

The MC68160(EEST) was designed to perform the physical connection to the Ethernet media. This is done through two separate media dependent interfaces and a SIA interface. The media dependent interfaces are the Attachment Unit Interface(AUI) and the 10BASE–T Twisted Pair(TP) port. The SIA interface is compatible with most industry controllers and selected by three mode control pins. Chip status is indicated by the condition of 6 status indicator pins. All but one are open collector outputs.

If the EEST isn't receiving data, the controller may initiate transmission. NRZ data from the communications controller SIA interface is encoded by the MC68160 into Manchester Code in preparation for transmission on the media. The data is then applied to either the AUI or TP port. If the data was transmitted using the 10BASE–T port, this data is also looped back to the receive data interface SIA pins connected to the controller. This allows detection of a collision condition in the event that another station on the media attempted transmission at the same time. After the entire data frame has been transmitted, the EEST must force the media idle signal. The idle signal frees the media for other stations that have deferred transmission. If no other transmissions are required the link enters an idle state. During this idle state the 10BASE–T transmitter issues idle pulses which communicates to the receiver connected to the other side that the link is valid. If the transmitter connected at the other end begins transmission, the EEST will assert a receive enable signal, and forward the received data to the controller.

Upon reception of data at the 10BASE–T port, the data is screened for proper sequence and pulse width requirements. If the preamble of the received frame meets the requirements, the PLL locks onto the 64–bit preamble and begins to decode the Manchester Code to NRZ code. This code is then presented to the communications controller at the receive data pins at the SIA interface. If data is received at the AUI port, it is sent directly to the communications controller via the SIA interface.

Data Transmission

To have properly encoded transmit data, the communications controller must be synchronized to TCLK. Transmission to the 10BASE–T or AUI media occurs when TENA is asserted and data is applied to the TX pin. Finally, to signify transmission, the TXLED in will cycle on and off at a 100 ms period. Data transmission for EEST is accomplished either over the 10BASE–T port or the AUI port. Both connections to the media are made with industry standard media interface components. The 10BASE–T interface requires a filter and transformer, the AUI interface requires only a transformer. The filter for the 10BASE–T transmit circuit will have to be chosen for each application.

If after approximately 40 ms after a TP or AUI transmission has begun, the EEST is still transmitting, the TPJABB pin will assert to signify a jabber condition. Also, the CLLED pin will transition high and low alternately with a 100 ms period. The transmit circuitry is, however, unaffected by the jabber condition, so the communications controller has the responsibility of monitoring and stopping transmission.

When transmission is complete, the transmit circuitry will begin the end of transmit and decay to idle responses necessary to meet requirements of the 802.3 standard for the TP and AUI port.

Data Reception

Other than the case of being in Loop Back mode, data reception to the RX pin of the EEST is initiated by signaling at the RX+/– or AUI ARX+/– pins. If at the TP port, the data is screened for validity by checking for sequence and pulse width requirements, then passed to the decode and receive circuitry. The RENA pin asserts and the data and corresponding clock is passed to the communications controller. After the frame has been transmitted, the MC68160 detects the ending transmission and negates RENA. If at the AUI port, the data is checked for proper pulse width requirements before being passed to the decode circuitry. If the data pulses are longer than at least 20 ns, RENA gets asserted and the frame is decoded to RX with and accompanying RCLK output.

Collision

Collision is the occurrence of simultaneous transmit activity by two or more stations on the network. In the event of collision, the data transfer paths are unaffected. If the MC68160 is in the twisted pair mode, collision is detect by simultaneous receive and transmit activity. If in the AUI mode, collision is detected by activity on the ACX+/– pins. In either case, if collision is detected, the CLSN pin will assert to notify the communications controller.

Jabber

The EEST has a jabber timer to detect the jabber condition. In the event that the transmitting station continues to transmit beyond the allowable transmit time, a jabber timer (40 ms) will expire and assert the TPJABB pin to alert the communications controller of the situation. The TPJABB pin can source or sink up to 10 mA, and so, is capable of driving a status LED. In the AUI mode, the pin is driven to high impedance since the transceiver connected to the AUI port must alert the communications controller of the jabber condition.

Full Duplex

A feature unique to the MC68160 is the Full Duplex mode. In this mode the EEST is capable of transmitting and receiving simultaneously. Collision conditions are not announced and internal loop back is disabled. The remainder of the EEST functionality remains unchanged from the non–Full Duplex mode. Full Duplex mode is enabled by asserting the TPFULDL pin.

Auto Port Selection

If the APORT pin is asserted, the MC68160 will automatically select the TP or AUI port depending on the presence of valid link beats or frames at the TP RX+/– pins. If the AUI port is automatically selected by another transmitting station or by setting TPEN low, the TP transmit port of the EEST continues to transmit link beats to keep the link active.

Auto Polarity Selection

If the RX+ and the RX– wires happen to get reversed, the MC68160 has the ability to automatically reverse the pins internally so that the received data is valid. In addition, an open collector status pin (TPPLR) is driven low to indicate the fault. In the AUI or reset mode this pin presents a high impedance.

Loop Back Mode

To test the transmit and receive circuitry without disturbing the connected network, the EEST has a Loop Back mode. Loop Back mode routes transmit data and clock to the receive data and clock pins using as much of the transmit and receive circuitry as possible. This gives a test of the MC68160 Manchester encode and decode function.

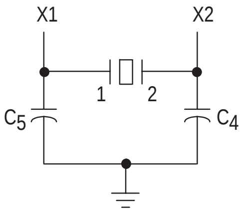
APPLICATIONS INFORMATION

Selection of Crystal and External Components

Accuracy of frequency and stability over temperature are the main determinants of crystal choice. Specifications for a suitable crystal are tabulated below.

Frequency	20.000 MHz
Mode	Fundamental
Tolerance	± 100 ppm
Stability	± 100 ppm
Aging	± 5 ppm/yr
Shunt Capacitance	7.0 pF
Load Capacitance	18–20 pF
Series Fundamental Resistance (ESR)	25 Ω
Drive Level	500 μW

A suitable crystal is the MTRON HC49 MP–1, 20.000 MHz crystal. 20 pF for C4 and C5 have been shown to work reliably.



PLL Filter Components

The filter components at Pin 12 were chosen to assure adequate pull–range but with a emphasis on stability. It is not foreseeable that a design would need to change the components, but for the sake of completeness, relevant values are provided here.

$$\text{VCO Gain} = 24 \left(\frac{\text{MHz}}{\text{Volt} \bullet \text{sec}}\right) \text{ and,}$$

$$\text{Phase Detector Gain} = \frac{100}{\pi/2} \left(\frac{\mu\text{A}}{\text{rad}}\right) \text{ and the}$$

filter impedance function is;

$$Z(j\omega) \approx \frac{(j\omega + 1/C6)}{j\omega \bullet C5 \bullet (j\omega + 1/C5)} \quad (\text{for } C6 >> C5)$$

10BASE–T Filter and Transformer Choice

The MC68160 differential outputs are low impedance voltage sources. Therefore, external series resistors must be used in order to match the characteristic impedance of twisted pair. Since the output resistance of each leg of the transmitter is about 10 Ω, a 39 Ω resistor is used in series as shown in the applications schematic. So the impedance presented from the source to the isolation transformer is then very nearly 100 Ω. The following is a list of some 10BASE–T filter module vendors and their products.

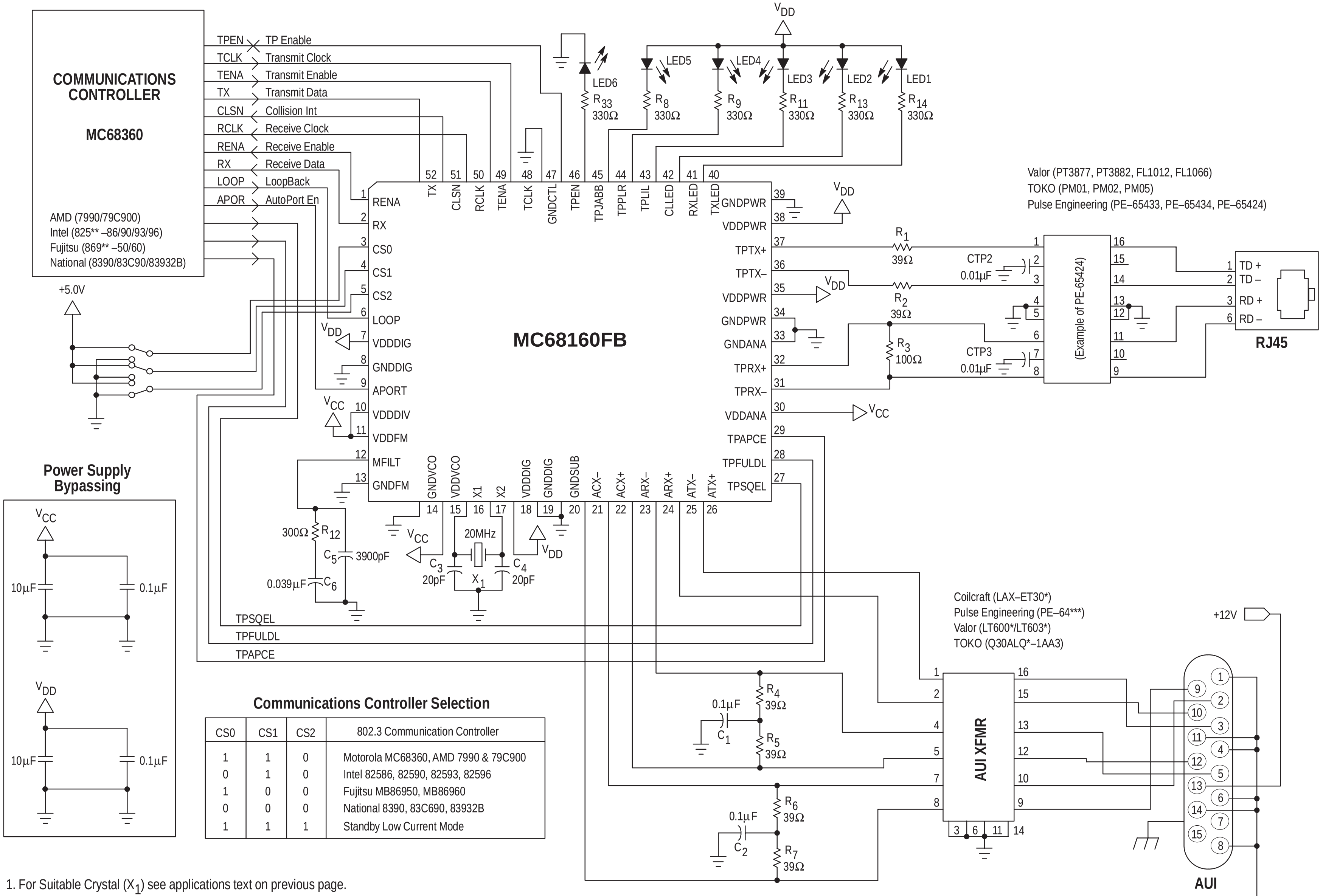
Vendor	**Part #**
FEE Fil–Mag	78Z1120B–01, 78Z1122B/D–01, 78Z1122 F–01
Valor Electronics	PT3877, FL1012, FL1066
Pulse Engineering	PE–65434, PE65424, PE65433
TOKO	PM01–00, PM02–00, PM05–00

AUI Transformer Choice

Like the 10BASE–T outputs, the AUI differential outputs are low impedance sources and capable of meeting the IEEE 802.3 waveform requirements when a coupling transformer is used. Some AUI transformer vendors and their products are provided below.

Vendor	**Part #**
Coilcraft	LAX–ET304
FEE Fil–Mag	23Z90, 23Z91/ 23Z92
Valor Electronics	LT6032, LT6033
Pulse Engineering	PE64502, PE6103
TOKO	Q30ALQ8–1AA3, Q30ALQ9–1AA3

Figure 41. Typical Application Diagram



Communications Controller Selection

CS0	CS1	CS2	802.3 Communication Controller
1	1	0	Motorola MC68360, AMD 7990 & 79C900
0	1	0	Intel 82586, 82590, 82593, 82596
1	0	0	Fujitsu MB86950, MB86960
0	0	0	National 8390, 83C690, 83932B
1	1	1	Standby Low Current Mode

1. For Suitable Crystal (X_1) see applications text on previous page.
2. Decoupling capacitors should be placed as close to supply pins as possible.

MOTOROLA

MC75172B
MC75174B

Quad EIA-485 Line Drivers with Three-State Outputs

QUAD EIA–485 LINE DRIVERS

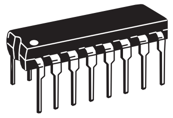
SEMICONDUCTOR TECHNICAL DATA

The Motorola MC75172B/174B Quad Line drivers are differential high speed drivers designed to comply with the EIA–485 Standard. Features include three–state outputs, thermal shutdown, and output current limiting in both directions. These devices also comply with EIA–422–A, and CCITT Recommendations V.11 and X.27.

The MC75172B/174B are optimized for balanced multipoint bus transmission at rates in excess of 10 MBPS. The outputs feature wide common mode voltage range, making them suitable for party line applications in noisy environments. The current limit and thermal shutdown features protect the devices from line fault conditions. These devices offer optimum performance when used with the MC75173 and MC75175 line receivers.

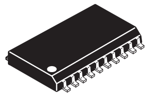
Both devices are available in 16–pin plastic DIP and 20–pin wide body surface mount packages.

- Meets EIA–485 Standard for Party Line Operation
- Meets EIA–422–A and CCITT Recommendations V.11 and X.27
- Operating Ambient Temperature: –40°C to +85°C
- High Impedance Outputs
- Common Mode Output Voltage Range: –7 to 12 V
- Positive and Negative Current Limiting
- Transmission Rates in Excess of 10 MBPS
- Thermal Shutdown at 150°C Junction Temperature, (±20°C)
- Single 5.0 V Supply
- Pin Compatible with TI SN75172/4 and NS µA96172/4
- Interchangeable with MC3487 and AM26LS31 for EIA–422–A Applications



P SUFFIX
PLASTIC PACKAGE
CASE 648

DW SUFFIX
PLASTIC PACKAGE
CASE 751D
(SO–20L)

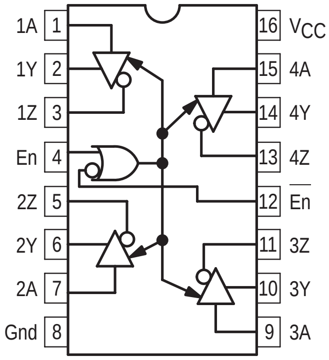


ORDERING INFORMATION

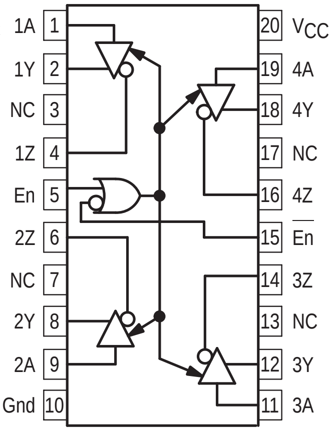
Device	Operating Temperature Range	Package
MC75172BDW	T_A = –40° to +85°C	SO–20L
MC75174BDW		SO–20L
MC75174BP		Plastic DIP

PIN CONNECTIONS

MC75172B

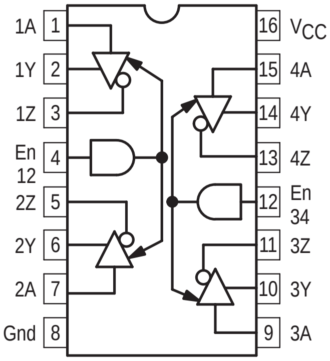


P Package

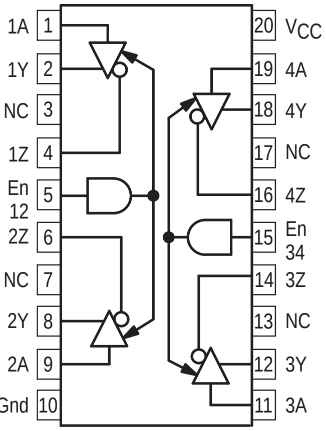


DW Package

MC75174B



P Package



DW Package

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	–0.5, +7.0	Vdc
Input Voltage (Data, Enable)	V_{in}	+7.0	Vdc
Input Current (Data, Enable)	I_{in}	–24	mA
Applied Output Voltage, when in 3–State Condition (V_{CC} = 5.0 V)	V_{za}	–10, +14	Vdc
Applied Output Voltage, when V_{CC} = 0 V	V_{zb}	±14	
Output Current	I_O	Self–Limiting	–
Storage Temperature	T_{stg}	–65, +150	°C

Devices should not be operated at these limits. The “Recommended Operating Conditions” table provides for actual device operation.

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Min	Typ	Max	Unit
Power Supply Voltage	V_{CC}	+4.75	+5.0	+5.25	Vdc
Input Voltage (All Inputs)	V_{in}	0	–	V_{CC}	Vdc
Output Voltage in 3–State Condition, or when V_{CC} = 0 V	V_{cm}	–7.0	–	+12	Vdc
Output Current (Normal data transmission)	I_O	–65	–	+65	mA
Operating Ambient Temperature (see text)	T_A				°C
EIA–485		–40	–	+85	
EIA–422		0	–	+85	

All limits are not necessarily functional concurrently.

ELECTRICAL CHARACTERISTICS (–40°C $\leqslant T_A \leqslant$ 85°C, 4.75 V $\leqslant V_{CC} \leqslant$ 5.25 V, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage					
Single–Ended Voltage					Vdc
I_O = 0	V_O	0	–	6.0	
High @ I_O = –33 mA	V_{OH}	–	4.0	–	
Low @ I_O = +33 mA	V_{OL}	–	1.6	–	
Differential Voltage					
Open Circuit (I_O = 0)	$\lvert V_{OD1} \rvert$	1.5	3.4	6.0	
R_L = 54 Ω (Figure 1)	$\lvert V_{OD2} \rvert$	1.5	2.3	5.0	
Change in Differential*, R_L = 54 Ω (Figure 1)	$\lvert \Delta V_{OD2} \rvert$	–	5.0	200	mVdc
Differential Voltage, R_L = 100 Ω (Figure 1)	$\lvert V_{OD2A} \rvert$	–	2.2	–	Vdc
Change in Differential*, R_L = 100 Ω (Figure 1)	$\lvert \Delta V_{OD2A} \rvert$	–	5.0	200	mVdc
Differential Voltage, –7.0 V $\leqslant V_{cm} \leqslant$ 12 V (Figure 2)	$\lvert V_{OD3} \rvert$	1.5	–	5.0	Vdc
Change in Differential*, –7.0 V $\leqslant V_{cm} \leqslant$ 12 V (Figure 2)	$\lvert \Delta V_{OD3} \rvert$	–	5.0	200	mVdc
Offset Voltage, R_L = 54 Ω (Figure 1)	V_{OS}	–	2.9	–	Vdc
Change in Offset*, R_L = 54 Ω (Figure 1)	$\lvert \Delta V_{OS} \rvert$	–	5.0	200	mVdc
Output Current (Each Output)					
Power Off Leakage, V_{CC} = 0, –7.0 V $\leqslant V_O \leqslant$ 12 V	$I_{O(off)}$	–50	0	+50	µA
Leakage in 3–State Mode, –7.0 V $\leqslant V_O \leqslant$ 12 V	I_{OZ}	–50	0	+50	
Short Circuit Current to Ground	I_{OSR}	–150	–	+150	mA
Short Circuit Current, –7.0 V $\leqslant V_O \leqslant$ 12 V	I_{OS}	–250	–	+250	

*V_{in} switched from 0.8 to 2.0 V.
Typical values determined at 25°C ambient and 5.0 V supply.

ELECTRICAL CHARACTERISTICS (–40°C $\leqslant T_A \leqslant$ 85°C, 4.75 V $\leqslant V_{CC} \leqslant$ 5.25 V, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Inputs					Vdc
Low Level Voltage (Pins 4 & 12, MC75174B only)	$V_{IL(A)}$	0	–	0.7	
Low Level Voltage (All Other Pins)	$V_{IL(B)}$	0	–	0.8	
High Level Voltage (All Inputs)	V_{IH}	2.0	–	V_{CC}	
Current @ V_{in} = 2.7 V (All Inputs)	I_{IH}	–	0.2	20	µA
Current @ V_{in} = 0.5 V (All Inputs)	I_{IL}	–100	–15	–	
Clamp Voltage (All Inputs, I_{in} = –18 mA)	V_{IK}	–1.5	–	–	Vdc
Thermal Shutdown Junction Temperature	T_{jts}	–	+150	–	°C
Power Supply Current (Outputs Open, V_{CC} = 5.25 V)	I_{CC}				mA
Outputs Enable		–	60	70	
Outputs Disabled		–	30	40	

TIMING CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0 V)

Characteristics	Symbol	Min	Typ	Max	Unit
Propagation Delay – Input to Single–ended Output (Figure 3)					ns
Output Low–to–High	t_{PLH}	–	23	30	
Output High–to–Low	t_{PHL}	–	18	30	
Propagation Delay – Input to Differential Output (Figure 4)					ns
Input Low–to–High	$t_{PLH(D)}$	–	15	25	
Input High–to–Low	$t_{PHL(D)}$	–	17	25	
Differential Output Transition Time (Figure 4)	t_{dr}, t_{df}	–	19	25	ns
Skew Timing					ns
$\lvert t_{PLHD} - t_{PHLD} \rvert$ for Each Driver	t_{SK1}	–	0.2	–	
Max – Min t_{PLHD} Within a Package	t_{SK2}	–	1.5	–	
Max – Min t_{PHLD} Within a Package	t_{SK3}	–	1.5	–	
Enable Timing					ns
Single–ended Outputs (Figure 5)					
Enable to Active High Output	$t_{PZH(E)}$	–	48	60	
Enable to Active Low Output	$t_{PZL(E)}$	–	20	30	
Active High to Disable (using Enable)	$t_{PHZ(E)}$	–	35	45	
Active Low to Disable (using Enable)	$t_{PLZ(E)}$	–	30	50	
Enable to Active High Output (MC75172B only)	$t_{PZH(E)}$	–	58	70	
Enable to Active Low Output (MC75172B only)	$t_{PZL(E)}$	–	28	35	
Active High to Disable (using Enable, MC75172B only)	$t_{PHZ(E)}$	–	38	50	
Active Low to Disable (using Enable, MC75172B only)	$t_{PLZ(E)}$	–	36	50	
Differential Outputs (Figure 6)					ns
Enable to Active Output	$t_{PZD(E)}$	–	47	–	
Enable to Active Output (MC75172B only)	$t_{PZD(E)}$	–	56	–	
Enable to 3–State Output	$t_{PDZ(E)}$	–	32	–	
Enable to 3–State Output (MC75172B only)	$t_{PDZ(E)}$	–	40	–	

Figure 1. V_{DD} Measurement

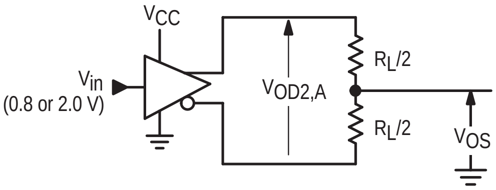


Figure 2. Common Mode Test

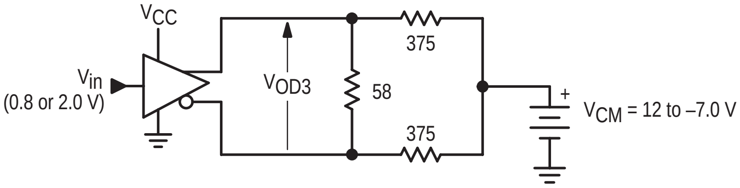


Figure 3. Propagation Delay, Single–Ended Outputs

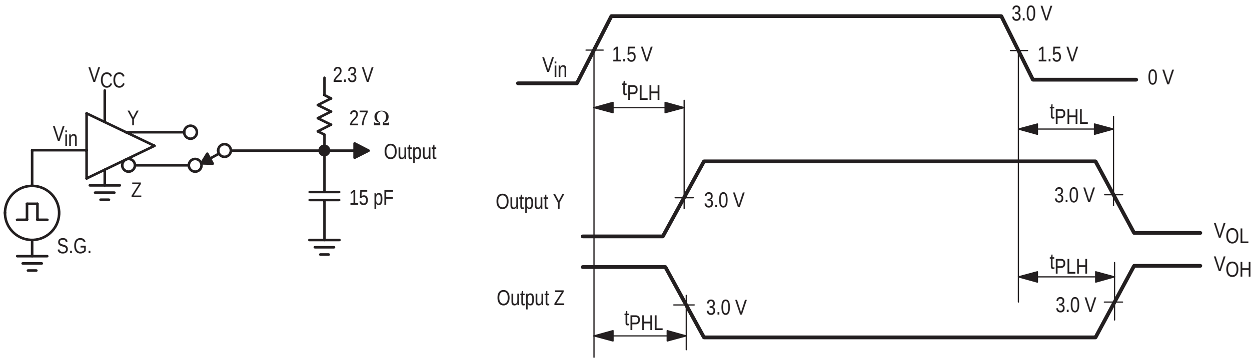
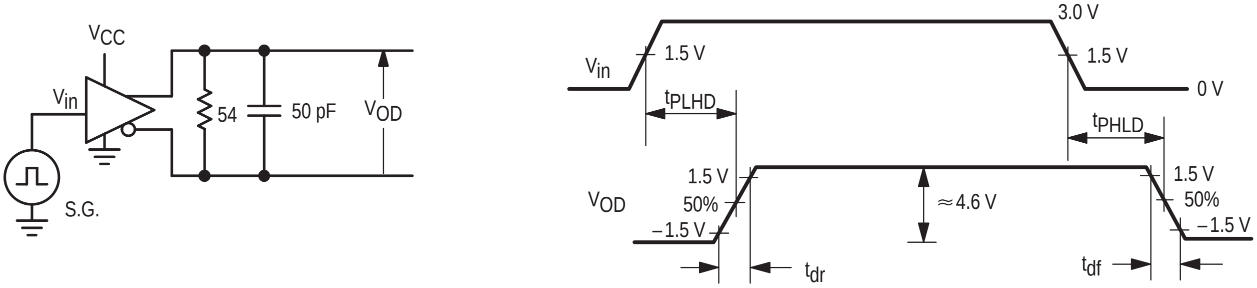


Figure 4. Propagation Delay, Differential Outputs



NOTES: 1. S.G. set to: f ⩽ 1.0 MHz; duty cycle = 50%; t_r, t_f, ⩽ 5.0 ns.
2. $t_{SK1} = |t_{PLHD} - t_{PHLD}|$ for each driver.
3. t_{SK2} computed by subtracting the shortest t_{PLHD} from the longest t_{PLHD} of the 4 drivers within a package.
4. t_{SK3} computed by subtracting the shortest t_{PHLD} from the longest t_{PHLD} of the 4 drivers within a package.

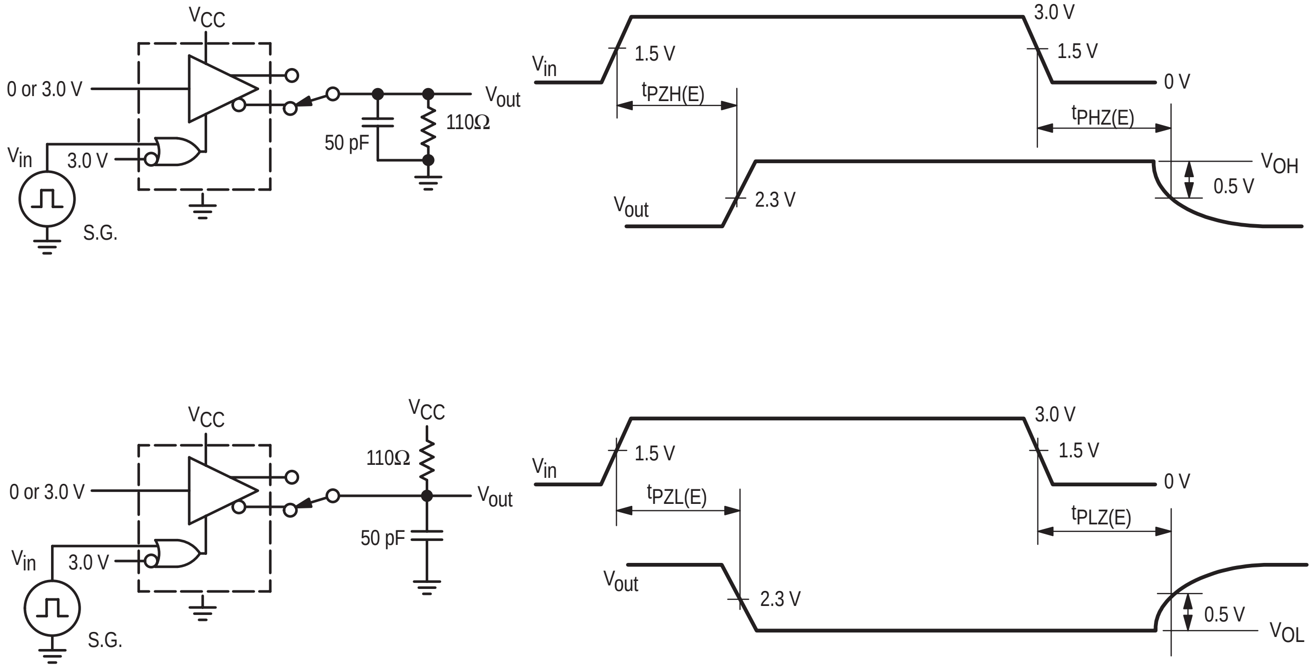


Figure 5. Enable Timing, Single–Ended Outputs

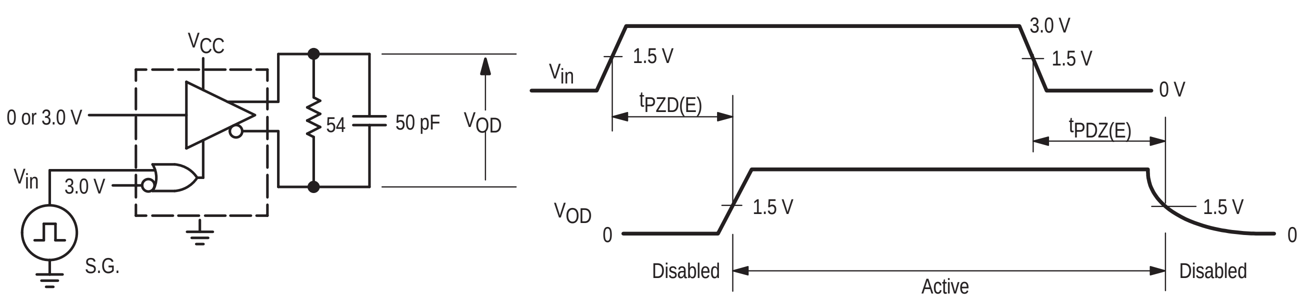


Figure 6. Enable Timing, Differential Outputs

NOTES: 1. S.G. set to: f ≤ 1.0 MHz; duty cycle = 50%; t_f, t_f, ≤ 5.0 ns.
2. V_{in} is inverted for Enable measurements.

Figure 7. Single–Ended Output Voltage versus Output Sink Current

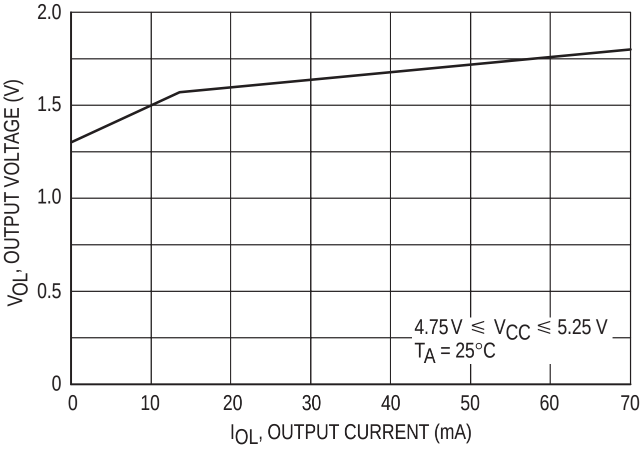


Figure 8. Single–Ended Output Voltage versus Temperature

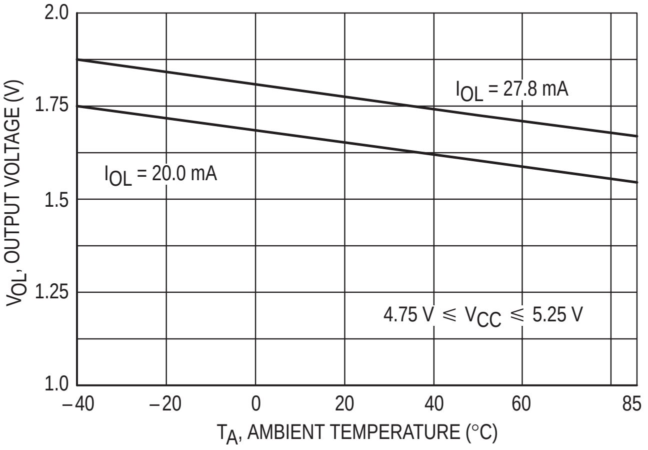


Figure 9. Single–Ended Output Voltage versus Output Source Current

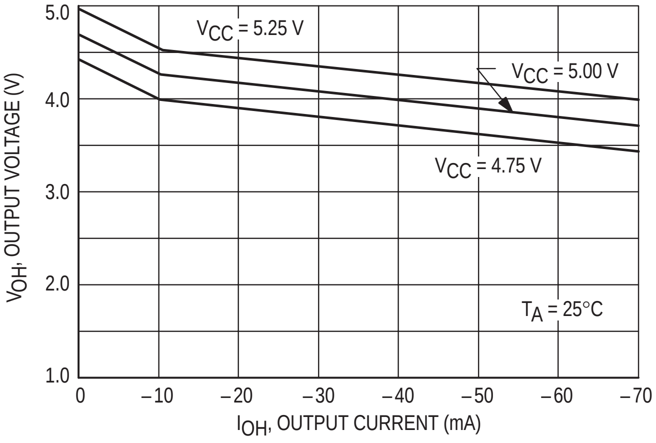


Figure 10. Single–Ended Output Voltage versus Temperature

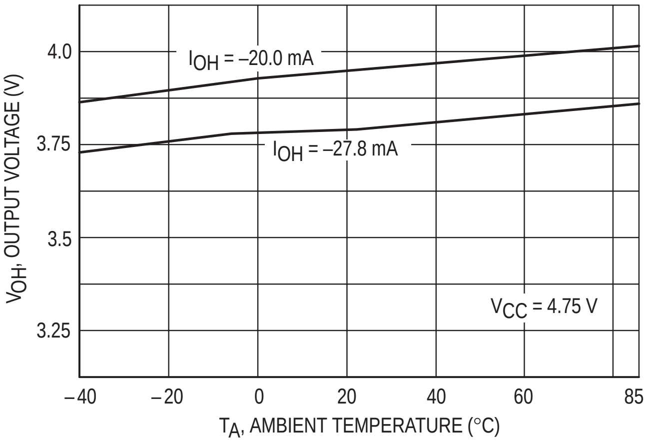


Figure 11. Output Differential Voltage versus Load Current

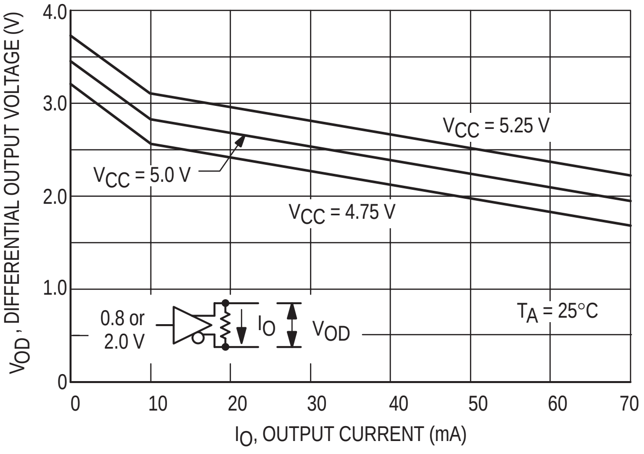


Figure 12. Output Differential Voltage versus Temperature

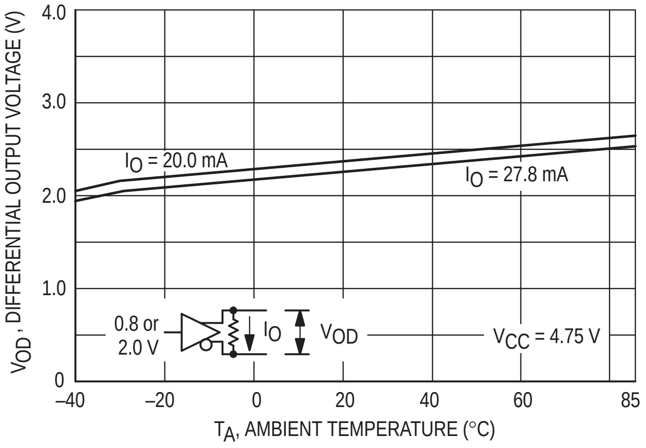


Figure 13. Output Leakage Current versus Output Voltage

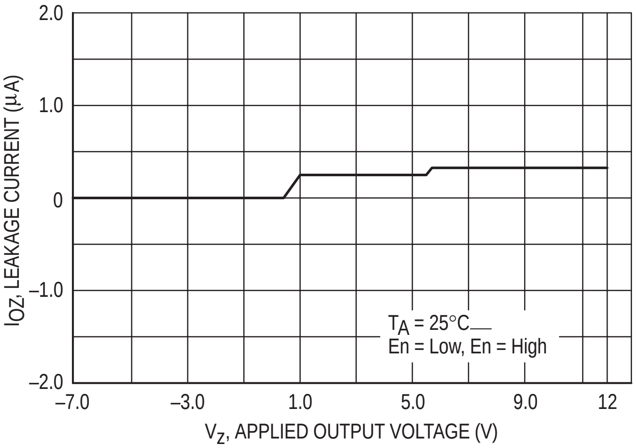


Figure 14. Output Leakage Current versus Temperature

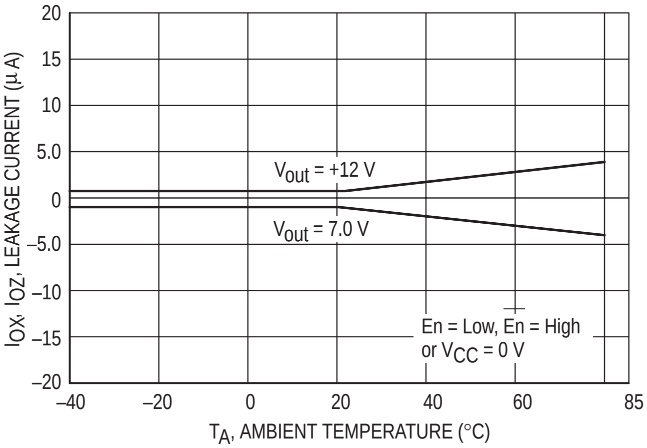


Figure 15. Input Current versus Input Voltage

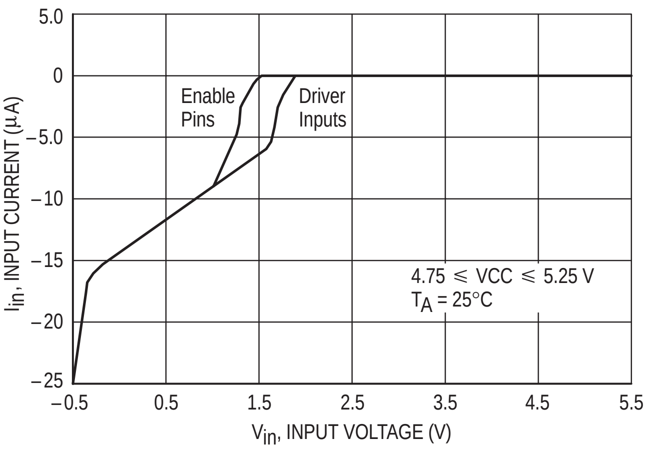
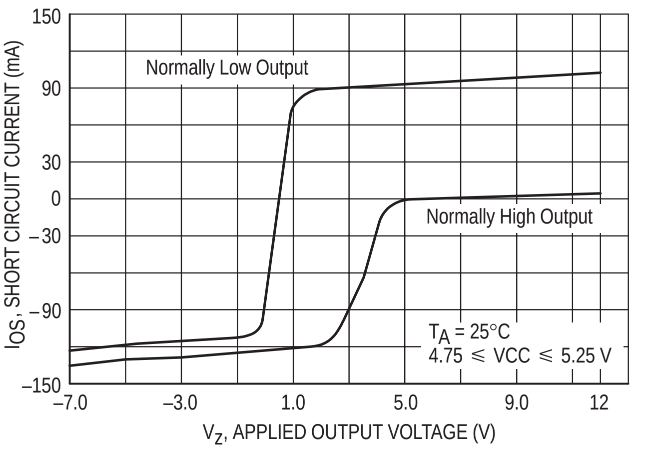


Figure 16. Short Circuit Current versus Common Mode Voltage



APPLICATIONS INFORMATION

Description

The MC75172B and MC75174B are differential line drivers designed to comply with EIA–485 Standard (April 1983) for use in balanced digital multipoint systems containing multiple drivers. The drivers also comply with EIA–422–A and CCITT Recommendations V.11 and X.27. The drivers meet the EIA–485 requirement for protection from damage in the event that two or more drivers attempt to transmit data simultaneoulsy on the same cable. Data rates in excess of 10 MBPS are possible, depending on the cable length and cable characteristics. A single power supply, 5.0 V, ±5%, is required at a nominal current of 60 mA, plus load currents.

Outputs

Each output (when active) will be a low or a high voltage, which depends on the input state and the load current (see Table 1, 2 and Figures 7 to 10). The graphs apply to each driver, regardless of how many other drivers within the package are supplying load current.

Table 1. MC75172B Truth Table

Data Input	Enables		Outputs	
	EN	EN	Y	Z
H	H	X	H	L
L	H	X	L	H
H	X	L	H	L
L	X	L	L	H
X	L	H	Z	Z

Table 2. MC75174B Truth Table

Data Input	Enable	Outputs	
		Y	Z
H	H	H	L
L	H	L	H
X	L	Z	Z

H = Logic high, L = Logic low, X = Irrelevant, Z = High impedance

The two outputs of a driver are always complementary. A “high” output can only source current out, while a “low” output can only sink current (except for short circuit current – see Figure 16).

The outputs will be in the high impedance mode when:

a) the Enable inputs are set according to Table 1 or 2;

b) V_{CC} is less than 1.5 V;

c) the junction temperature exceeds the trip point of the thermal shutdown circuit (see below). When in this condition, the output’s source and sink capability are shut off, and only leakage currents will flow (see Figures 13, 14). Disabled outputs may be taken to any voltage between –7.0 V and 12 V without damage.

The drivers are protected from short circuits by two methods:

a) Current limiting is provided at each output, in both the source and sink direction, for shorts to any voltage within the range of 12 V to –7.0 V, with respect to circuit ground (see Figure 16). The short circuit current will flow until the fault is removed, or until the thermal shutdown circuit activates (see below). The current limiting circuit has a negative temperature coefficient and requires no resetting upon removal of the fault condition.

b) A thermal shutdown circuit disables the outputs when the junction temperature reaches 150°C, ±20°C. The thermal shutdown circuit has a hysteresis of ≈ 12°C to prevent oscillations. When this circuit activates, the output stage of each driver is put into the high impedance mode, thereby shutting off the output currents. The remainder of the internal circuitry remains biased. The outputs will become active once again as the IC cools down.

Driver Inputs

The driver inputs determine the state of the outputs in accordance with Tables 1 and 2. The driver inputs have a nominal threshold of 1.2 V, and their voltage must be kept within the range of 0 V to V_{CC} for proper operation. If the voltage is taken more than 0.5 V below ground, excessive currents will flow, and proper operation of the drivers will be affected. An open pin is equivalent to a logic high, but good design practices dictate that inputs should never be left open. The characteristics of the driver inputs are shown in Figure 15. This graph is not affected by the state of the Enable pins.

Enable Logic

Each driver’s outputs are active when the Enable inputs (Pins 4 and 12) are true according to Tables 1 and 2.

The Enable inputs have a nominal threshold of 1.2 V and their voltage must be kept within the range of 0 V to V_{CC} for proper operation. If the voltage is taken more than 0.5 V below ground, excessive currents will flow, and proper operation of the drivers will be affected. An open pin is equivalent to a logic high, but good design practices dictate that inputs should never be left open. The Enable input characteristics are shown in Figure 15.

Operating Temperature Range

The minimum ambient operating temperature is listed as –40°C to meet EIA–485 specifications, and 0°C to meet EIA–422–A specifications. The higher V_{OD} required by EIA–422–A is the reason for the narrower temperature range.

The maximum ambient operating temperature (applicable to both EIA–485 and EIA–422–A) is listed as 85°C. However, a lower ambient may be required depending on system use (i.e. specifically how many drivers within a package are used) and at what current levels they are operating. The maximum power which may be dissipated within the package is determined by:

$$PD_{max} = \frac{T_{Jmax} - T_A}{R_{\theta JA}}$$

where: $R_{\theta JA}$ = package thermal resistance (typical 70°C/W for the DIP package, 85°C/W for SOIC package);
T_{Jmax} = max. operating junction temperature, and
T_A = ambient temperature.

Since the thermal shutdown feature has a trip point of 150°C, ±20°C, T_{Jmax} is selected to be 130°C. The power dissipated within the package is calculated from:

$$PD = \{[(V_{CC} - V_{OH}) \bullet I_{OH}] + V_{OL} \bullet I_{OL})\} \text{ each driver } + (V_{CC} \bullet I_{CC})$$

where: V_{CC} = the supply voltage;
V_{OH}, V_{OL} are measured or estimated from Figures 7 to 10;
I_{CC} = the quiescent power supply current (typical 60 mA).

As indicated in the equation, the first term (in brackets) must be calculated and summed for each of the four drivers, while the last term is common to the entire package.

Example 1: T_A = 25°C, $I_{OL} = I_{OH}$ = 55 mA for each driver, V_{CC} = 5.0 V, DIP package. How many drivers per package can be used?

Maximum allowable power dissipation is:

$$PD_{max} = \frac{130°C - 25°C}{70°C/W} = 1.5 \text{ W}$$

Since the power supply current of 60 mA dissipates 300 mW, that leaves 1.2 W (1.5 W – 0.3 W) for the drivers. From Figures 7 and 9, $V_{OL} \approx 1.75$ V, and $V_{OH} \approx 3.85$ V. The power dissipated in each driver is:

$$\{(5.0 - 3.85) \bullet 0.055\} + (1.75 \bullet 0.055) = 160 \text{ mW}.$$

Since each driver dissipates 160 mW, the four drivers per package could be used in this application

Example 2: T_A = 85°C, I_{OL} = 27.8 mA, I_{OH} = 20 mA for each driver, V_{CC} = 5.0 V, SOIC package. How many drivers per package can be used?

Maximum allowable power dissipation is:

$$PD_{max} = \frac{130°C - 85°C}{85°C/W} = 0.53 \text{ W}$$

Since the power supply current of 60 mA dissipates 300 mW, that leaves 230 mW (530 mW – 300 mW) for the drivers. From Figures 8 and 10 (adjusted for V_{CC} = 5.0 V), $V_{OL} \approx 1.38$ V, and $V_{OH} \approx 4.27$ V. The power dissipated in each driver is:

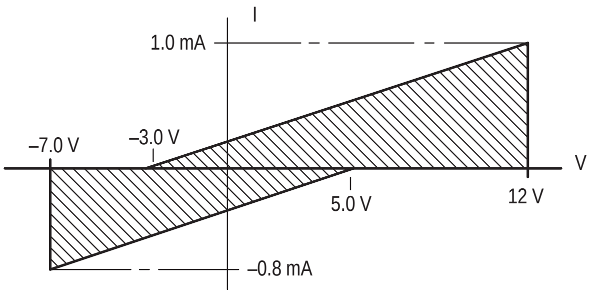
$$\{(5.0 - 4.27) \bullet 0.020\} + (1.38 \bullet 0.0278) = 53 \text{ mW}$$

Since each driver dissipates 53 mW, the use of all four drivers in a package would be marginal. Options include reducing the load current, reducing the ambient temperature, and/or providing a heat sink.

System Requirements

EIA–485 requires each driver to be capable of transmitting data differentially to at least 32 unit loads, plus an equivalent DC termination resistance of 60Ω, over a common mode voltage of –7.0 to 12 V. A unit load (U.L.), as defined by EIA–485, is shown in Figure 17.

Figure 17. Unit Load Definition



Reprinted from EIA–485, Electronic Industries Association, Washington,DC.

A load current within the shaded regions represents an impedance of less than one U.L., while a load current of a magnitude outside the shaded area is greater than one U.L. A system's total load is the sum of the unit load equivalents of each receiver's input current, and each disabled driver's output leakage current. The 60Ω termination resistance mentioned above allows for two 120Ω terminating resistors.

Using the EIA–485 requirements (worst case limits), and the graphs of Figures 7 and 9, it can be determined that the maximum current an MC75172B or MC75174B driver will source or sink is ≈65 mA.

System Example

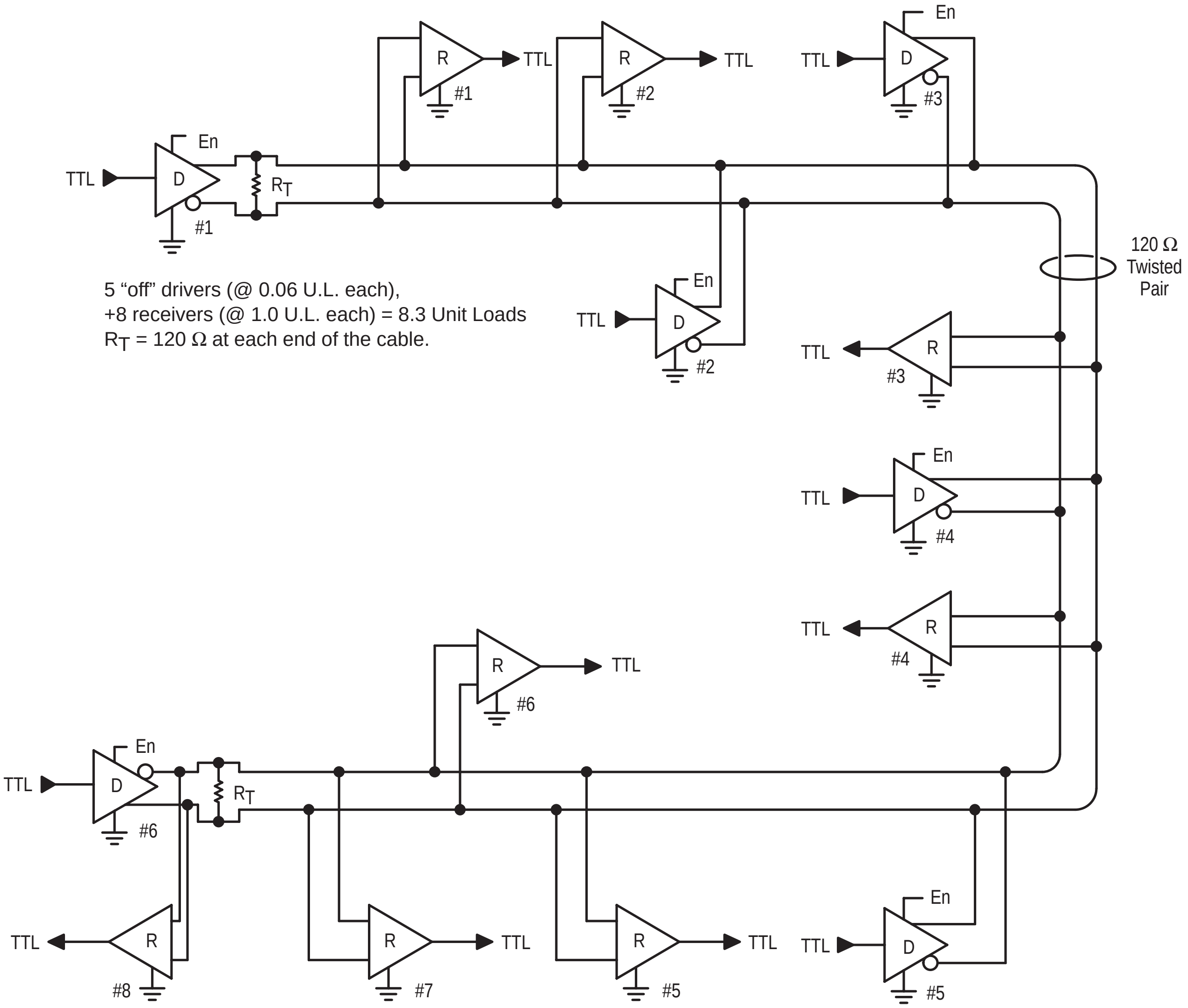
An example of a typical EIA–485 system is shown in Figure 18. In this example, it is assumed each receiver's input characteristics correspond to 1.0 U.L. as defined in Figure 17. Each "off" driver, with a maximum leakage of ±50 µA over the common mode range, presents a load of ≈0.06 U.L. The total load for the active driver is therefore 8.3 unit loads, plus the parallel combination of the two terminating resistors (60Ω). It is up to the system software to control the driver Enable pins to ensure that only one driver is active at any time.

Termination Resistors

Transmission line theory states that, in order to preserve the shape and integrity of a waveform traveling along a cable, the cable must be terminated in an impedance equal to its characteristic impedance. In a system such as that depicted in Figure 18, in which data can travel in both directions, both physical ends of the cable must be terminated. Stubs, leading to each receiver and driver, should be as short as possible.

Leaving off the terminations will generally result in reflections which can have amplitudes of several volts above V_{CC} or below ground. These overshoots and undershoots can disrupt the driver and/or receiver operation, create false data, and in some cases damage components on the bus.

Figure 18. Typical EIA–485 System



5 “off” drivers (@ 0.06 U.L. each),
+8 receivers (@ 1.0 U.L. each) = 8.3 Unit Loads
R_T = 120 Ω at each end of the cable.

NOTES: 1. Terminating resistors R_T must be located at the physical ends of the cable.
2. Stubs should be as short as possible.
3. Circuit ground of all drivers and receivers must be connected via a dedicated wire within the cable. Do not rely on chassis ground or power line ground.

Comparing System Requirements

Characteristic	Symbol	EIA–485	EIA–422–A	V.11 and X.27
GENERATOR (DRIVER)				
Output Impedance (Note 1)	Z_{out}	Not Specified	< 100 Ω	50 10 100 Ω
Open Circuit Voltage				
Differential	V_{OCD}	1.5 to 6.0 V	≤ 6.0 V	≤ 6.0 V, w/3.9 kΩ, Load
Single–Ended	V_{OCS}	< 6.0 V	≤ 6.0 V	≤ 6.0 V, w/3.9 kΩ, Load
Loaded Differential Voltage	V_{OD}	1.5 to 5.0 V, w/54 Ω load	≥ 2.0 V or ≥ 0.5 V_{OCD}, w/100 Ω load	≥ 2.0 V or ≥ 0.5 V_{OCD}, w/100 Ω load
Differential Voltage Balance	ΔV_{OD}	< 200 mV	≤ 400 mV	< 400 mV
Output Common Mode Range	V_{CM}	–7.0 to +12 V	Not Specified	Not Specified
Offset Voltage	V_{OS}	$-1.0 < V_{OS} < 3.0$ V	≤ 3.0 V	≤ 3.0 V
Offset Voltage Balance	ΔV_{OS}	< 200 mV	≤ 400 mV	< 400 mV
Short Circuit Current	I_{OS}	≤ 250 mA for –7.0 to 12 V	≤ 150 mA to ground	≤ 150 mA to ground
Leakage Current (V_{CC} = 0)	I_{OLK}	Not Specified	≤ 100 µA to –0.25 V thru 6.0 V	≤ 100 µA to ± 0.25 V
Output Rise/Fall Time (Note 2)	t_r, t_f	≤ 0.3 T_B, w/54 Ω/1150 pF load	≤ 0.1 T_B or ≤ 20 ns, w/100 Ω load	≤ 0.1 T_B or ≤ 20 ns, w/100 Ω load
RECEIVER				
Input Sensitivity	V_{th}	± 200 mV	± 200 mV	± 300 mV
Input Bias Voltage	V_{bias}	≤ 3.0 V	≤ 3.0 V	≤ 3.0 V
Input Common Mode Range	V_{cm}	–7.0 to 12 V	–7.0 to 7.0 V	–7.0 to 7.0 V
Dynamic Input Impedance	R_{in}	Spec number of U.L.	≥ 4 kΩ	≥ 4 kΩ

NOTES: 1. Compliance with V.11 and X.27 (Blue book) output impedance requires external resistors in series with the outputs of the MC75172B and MC75174B.
2. T_B = Bit time.

Additional Information

Copies of the EIA Recommendations (EIA–485 and EIA–422–A) can be obtained from the Electronics Industries Association, Washington, D.C. (202–457–4966). Copies of the CCITT Recommendations (V.11 and X.27) can be obtained from the United States Department of Commerce, Springfield, VA (703–487–4600).

MOTOROLA

SN75175

Quad EIA-485 Line Receiver

The Motorola SN75175 is a monolithic quad differential line receiver with three–state outputs. It is designed specifically to meet the requirements of EIA–485, EIA–422A/23A Standards and CCITT recommendations.

The device is optimized for balanced multipoint bus transmission at rates up to 10 megabits per second. It also features high input impedance, input hysteresis for increased noise immunity, and input sensitivity of ±200 mV over a common mode input voltage range of –12 V to 12 V. The SN75175 is designed for optimum performance when used with the SN75172 or SN75174 quad differential line drivers.

- Meets EIA Standards EIA–422A and EIA–423A, EIA–485
- Meets CCITT Recommendations V.10, V.11, X.26, and X.27
- Designed for Multipoint Transmission on Long Bus Lines in Noisy Environments
- 3–State Outputs
- Common–Mode Input Voltage Range . . . –12 V to 12 V
- Input Sensitivity . . . ±200 mV
- Input Hysteresis . . . 50 mV Typ
- High Input Impedance . . . 1 EIA–485 Unit Load
- Operates from Single 5.0 V Supply
- Lower Power Requirements
- Plug–In Replacement for MC3486

This device contains 174 active transistors.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	7.0	Vdc
Input Common Mode Voltage	V_{ICM}	±25	Vdc
Input Differential Voltage	V_{ID}	±25	Vdc
Three–State Control Input Voltage	V_I	7.0	Vdc
Output Sink Current	I_O	50	mA
Storage Temperature	T_{stg}	–65 to +150	°C
Operating Junction Temperature	T_J	+150	°C

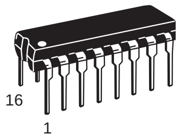
NOTE: ESD data available upon request.

RECOMMENDED OPERATING CONDITIONS

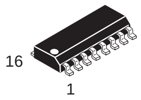
Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	4.75 to 5.25	Vdc
Operating Ambient Temperature	T_A	0 to +70	°C
Input Common Mode Voltage Range	V_{ICM}	–12 to +12	Vdc
Input Differential Voltage Range	V_{IDR}	–12 to +12	Vdc

QUAD EIA–485
LINE RECEIVER WITH
THREE–STATE OUTPUTS

SEMICONDUCTOR
TECHNICAL DATA

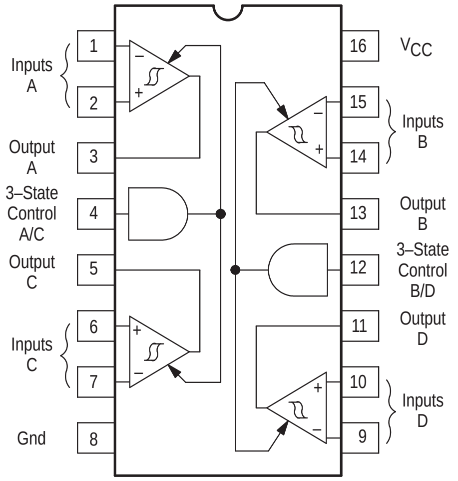


N SUFFIX
PLASTIC PACKAGE
CASE 648



D SUFFIX
PLASTIC PACKAGE
CASE 751B
(SO–16)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
SN75175N	T_A = 0 to +70°C	Plastic DIP
SN75175D		SO–16

ELECTRICAL CHARACTERISTICS (Unless otherwise noted, minimum and maximum limits apply over recommended temperature and power supply voltage ranges. Typical values are for T_A = 25°C, V_{CC} = 5.0 V, and V_{ICM} = 0 V, Note 1.)

Characteristic	Symbol	Min	Typ	Max	Unit
Differential Input Threshold Voltage (Note 2)	$V_{TH(D)}$				V
(–12 V $\leq V_{ICM} \leq$ 12 V, V_{IH} = 2.0 V)					
(I_O = –0.4 mA, $V_{OH} \geq$ 2.7 V)		–	–	0.2	
(I_O = 16 mA, $V_{OL} \leq$ 0.5 V)		–	–	–0.2	
Input Hysteresis	$V_{T+} – V_{T–}$	–	50	–	mV
Input Line Current (Differential Inputs)	I_I				mA
(Unmeasured Input at 0 V, Note 3)					
(V_I = 12 V)		–	–	1.0	
(V_I = –7.0 V)		–	–	–0.8	
Input Resistance (Note 4)	r_i	1 Unit Load	–	–	
Input Balance and Output Level (Note 3)					V
(–12 V $\leq V_{ICM} \leq$ 12 V, V_{IH} = 2.0 V)					
(I_O = –0.4 mA, V_{ID} = 0.2 V)	V_{OH}	2.7	–	–	
(I_O = 8.0 mA, V_{ID} = –0.2 V)	V_{OL}	–	–	0.45	
(I_O = 16 mA, V_{ID} = –0.2 V)	V_{OL}	–	–	0.5	
Input Voltage – High Logic State (Three–State Control)	V_{IH}	2.0	–	–	V
Input Voltage – Low Logic State (Three–State Control)	V_{IL}	–	–	0.8	V
Input Current – High Logic State (Three–State Control)	I_{IH}				µA
(V_{IH} = 2.7 V)		–	–	20	
(V_{IH} = 5.5 V)		–	–	100	
Input Current – Low Logic State (Three–State Control) (V_{IL} = 0.4 V)	I_{IL}	–	–	–100	µA
Input Clamp Diode Voltage (Three–State Control) (I_{IK} = –18 mA)	V_{IK}	–	–	–1.5	V
Output Third State Leakage Current	I_{OZ}				µA
($V_{I(D)}$ = 3.0 V, V_{IL} = 0.8 V, V_O = 0.4 V)		–	–	–20	
($V_{I(D)}$ = –3.0 V, V_{IL} = 0.8 V, V_O = 2.4 V)		–	–	20	
Output Short–Circuit Current (Note 5) ($V_{I(D)}$ = 3.0 V, V_{IH} = 2.0 V, V_O = 0 V)	I_{OS}	–15	–	–85	mA
Power Supply Current (V_{IL} = 0 V) (All Inputs Grounded)	I_{CC}	–	–	70	mA

NOTES: 1. All currents into device pins are shown as positive, out of device pins are negative. All voltages referenced to ground unless otherwise noted.
2. Differential input threshold voltage and guaranteed output levels are done simultaneously for worst case.
3. Refer to EIA–485 for exact conditions. Input balance and guaranteed output levels are done simultaneously for worst case.
4. Input resistance should be derived from input line current specifications and is shown for reference only. See EIA–485 and input line current specifications for more specific input resistance information.
5. Only one output at a time should be shorted.

SWITCHING CHARACTERISTICS (Unless otherwise noted, V_{CC} = 5.0 V and T_A = 25°C.)

Characteristic	Symbol	Min	Typ	Max	Unit
Propagation Delay Time – Differential Inputs to Output					ns
Output High to Low	$t_{PHL(D)}$	–	25	35	
Output Low to High	$t_{PLH(D)}$	–	25	35	
Propagation Delay Time – Three–State Control to Output					ns
Output Low to Third State	t_{PLZ}	–	16	35	
Output High to Third State	t_{PHZ}	–	19	35	
Output Third State to High	t_{PZH}	–	11	30	
Output Third State to Low	t_{PZL}	–	11	30	

FUNCTION TABLE (EACH RECEIVER)

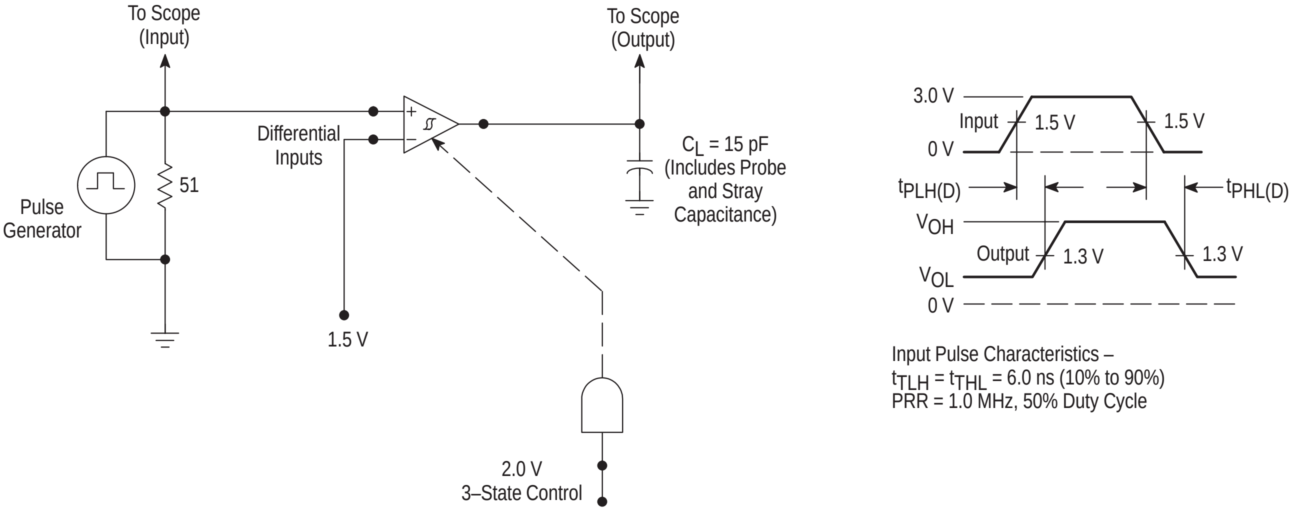
Differential Inputs	3–State Control	Output Y
$V_{ID} \geqslant 2.0$ V	H	H
-0.2 V $< V_{ID} < 0.2$ V	H	?
$V_{ID} \leqslant -0.2$ V	H	L
X	L	Z

H = high level
L = low level
X = irrelevant

? = indeterminate
Z = high–impedance (off)

SWITCHING TEST CIRCUIT AND WAVEFORMS

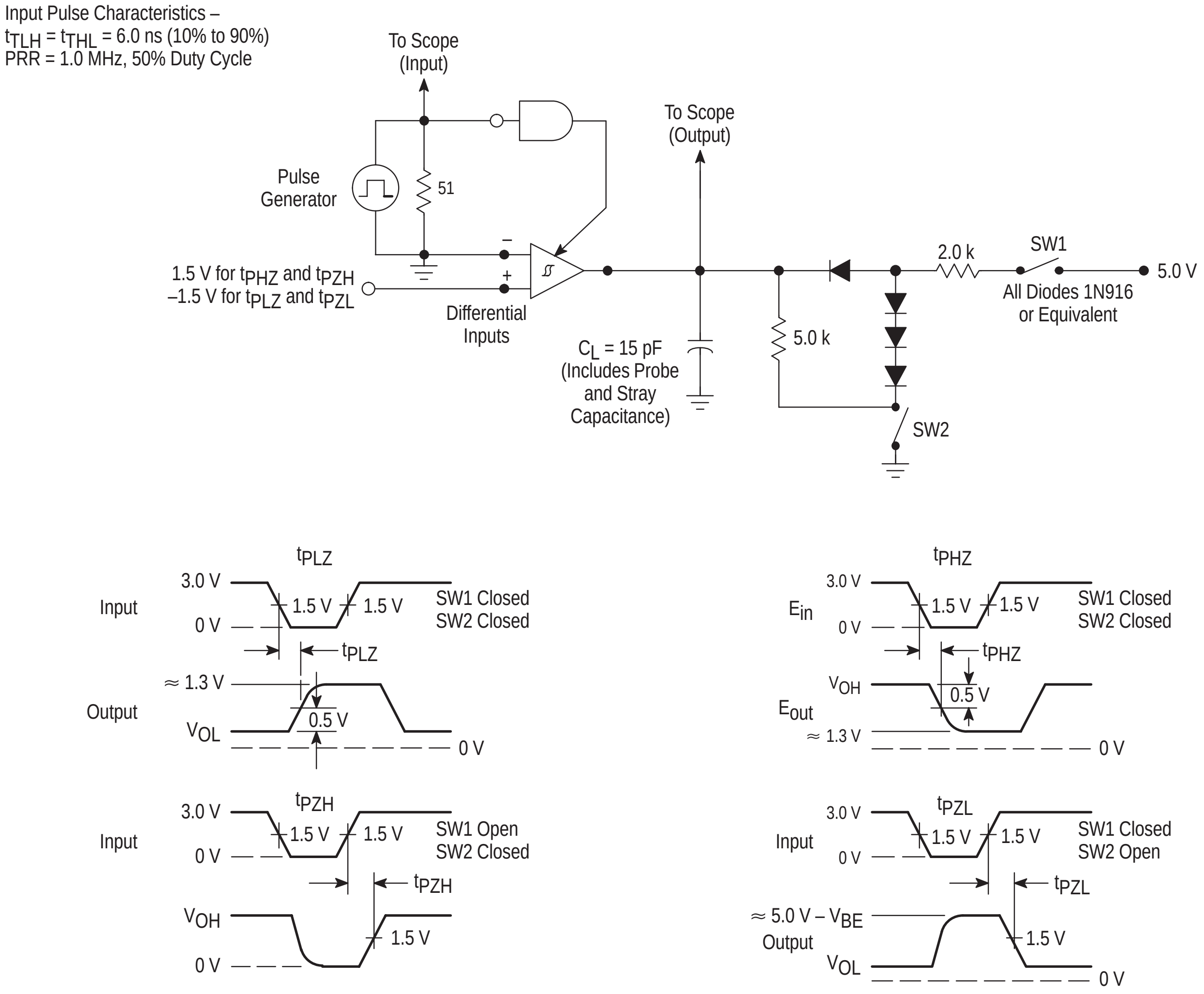
Figure 1. Propagation Delay, Differential Input to Output



Input Pulse Characteristics –
$t_{TLH} = t_{THL}$ = 6.0 ns (10% to 90%)
PRR = 1.0 MHz, 50% Duty Cycle

SWITCHING TEST CIRCUIT AND WAVEFORMS (continued)

Figure 2. Propagation Delay, Three–State Control Input to Output



TYPICAL CHARACTERISTICS

Figure 3. Output Voltage versus Differential Input Voltage

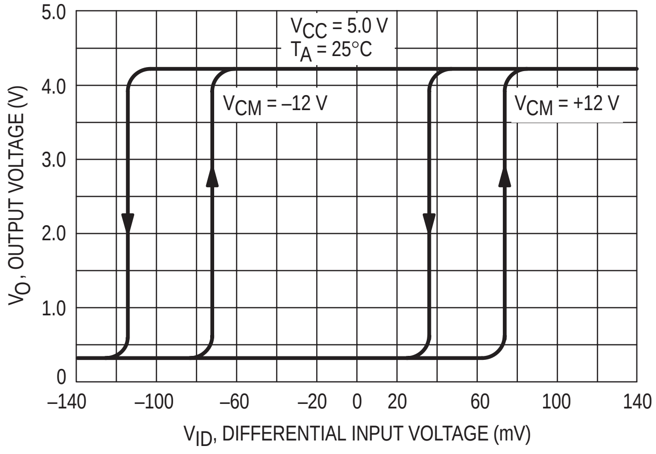


Figure 4. Output Voltage versus 3–State Control Voltage

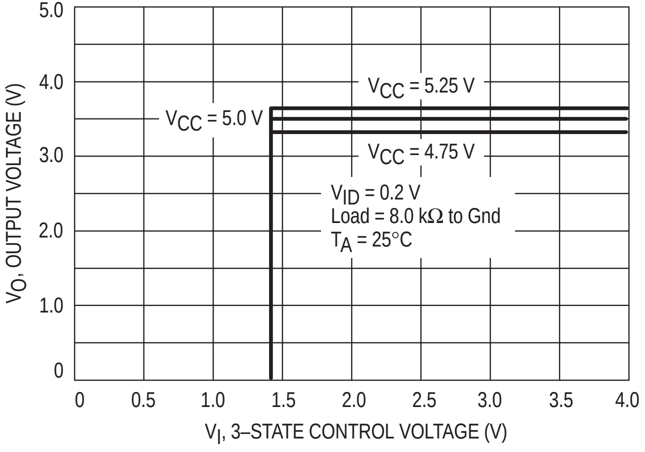


Figure 5. High Level Output Voltage versus Output Current

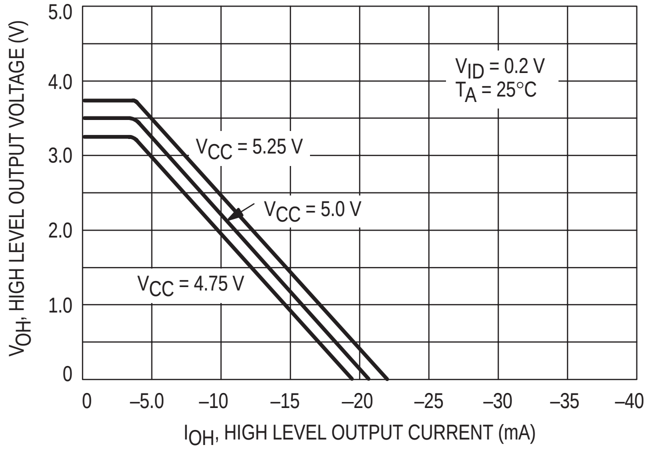


Figure 6. Low Level Output Voltage versus Output Current

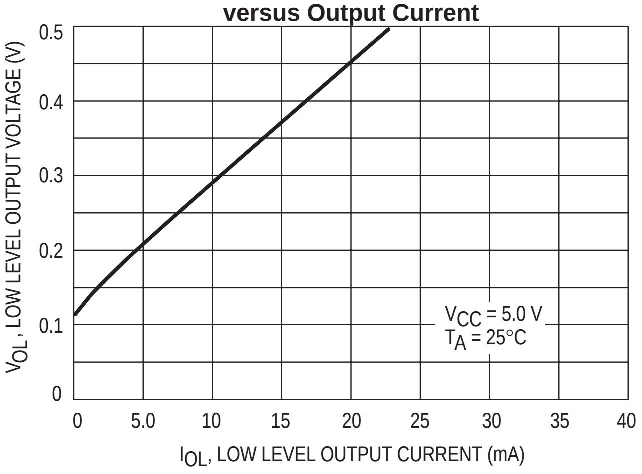


Figure 7. High Level Output Voltage versus Temperature

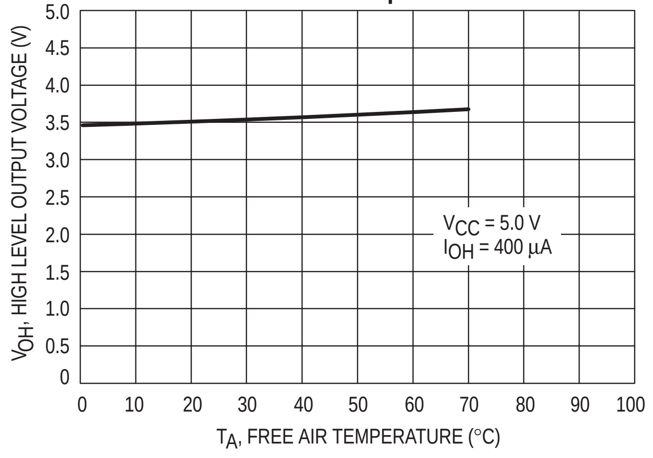
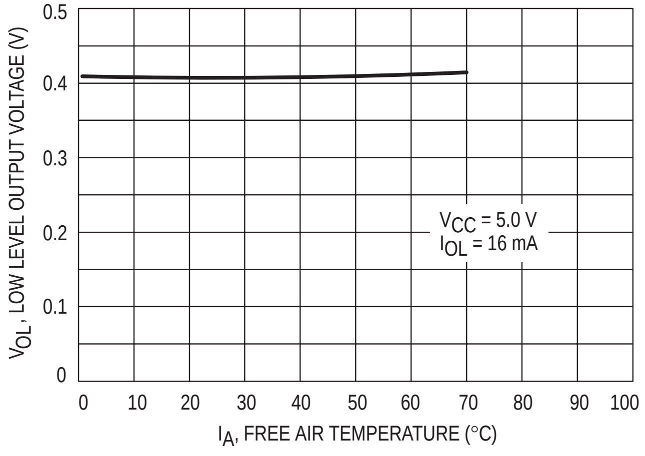


Figure 8. Low Level Output Voltage versus Temperature



MOTOROLA

ULN2068

Quad 1.5 A Sinking High Current Switch

The ULN2068 is a high–voltage, high–current quad Darlington switch array designed for high current loads, both resistive and reactive, up to 300 W.

It is intended for interfacing between low level (TTL, DTL, LS and 5.0 V CMOS) logic families and peripheral loads such as relays, solenoids, dc and stepping motors, multiplexer LED and incandescent displays, heaters, or other high voltage, high current loads.

The Motorola ULN2068 is specified with minimum guaranteed breakdown of 50 V and is 100% tested for safe area using an inductive load. It includes integral transient suppression diodes. Use of a predriver stage reduces input current while still allowing the device to switch 1.5 Amps.

It is supplied in an improved 16–Pin plastic DIP package with heat sink contact tabs (Pins 4, 5, 12 and 13). A copper alloy lead frame allows maximum power dissipation using standard cooling techniques. The use of the contact tab lead frame facilitates attachment of a DIP heat sink while permitting the use of standard layout and mounting practices.

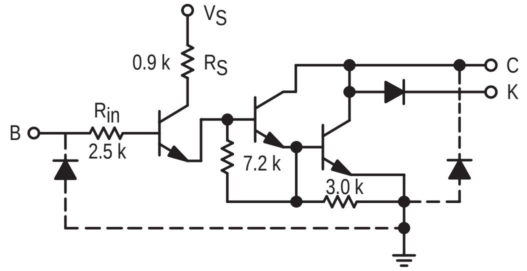
- TTL, DTL, LS, CMOS Compatible Inputs
- 1.5 A Maximum Output Current
- Low Input Current
- Internal Freewheeling Clamp Diodes
- 100% Inductive Load Tested
- Heat Tab Copper Alloy Lead Frame for Increased Dissipation

MAXIMUM RATINGS (T_A = 25°C and ratings apply to any one device in the package, unless otherwise noted)

Rating	Symbol	Value	Unit
Output Voltage	V_O	50	V
Input Voltage (Note 1)	V_I	15	V
Supply Voltage	V_S	10	V
Collector Current (Note 2)	I_C	1.75	A
Input Current (Note 3)	I_I	25	mA
Operating Ambient Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	–55 to +150	°C
Junction Temperature	T_J	150	°C

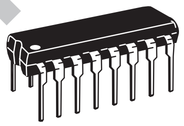
NOTES: 1. Input voltage referenced to ground.
2. Allowable output conditions shown in Figures 11 and 12.
3. May be limited by max input voltage.

Partial Schematic



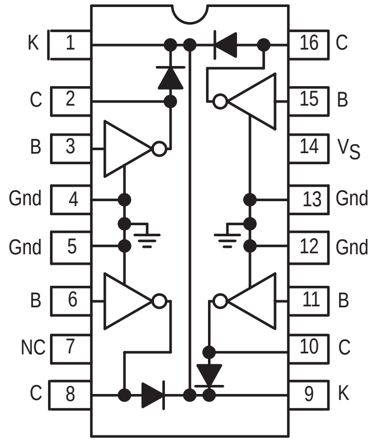
QUAD 1.5 A DARLINGTON SWITCH

SEMICONDUCTOR TECHNICAL DATA



B SUFFIX
PLASTIC PACKAGE
CASE 648C

PIN CONNECTIONS



ORDERING INFORMATION*

Device	Operating Temperature Range	Package
ULN2068B	T_A = 0 to +70°C	Plastic DIP

*Other options of this ULN2060/2070 series are available for volume applications. Contact your local Motorola Sales Representative.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Leakage Current (Figure 1) (V_{CE} = 50 V) (V_{CE} = 50 V, T_A = 70°C)	I_{CEX}	 – –	 – –	 100 500	µA
Collector–Emitter Saturation Voltage (Figure 2) (I_C = 500 mA (I_C = 750 mA } V_{in} = 2.4 V) (I_C = 1.0 A (I_C = 1.25 A	$V_{CE(sat)}$	 – – – –	 – – – –	 1.13 1.25 1.40 1.60	V
Input Current – On Condition (Figure 4) (V_I = 2.4 V) (V_I = 3.75 V)	$I_{I(on)}$	 – –	 – –	 0.25 1.0	mA
Input Voltage – On Condition (Figure 5) (V_{CE} = 2.0 V, I_C = 1.5 A)	$V_{I(on)}$	 –	 –	 2.4	V
Inductive Load Test (Figure 3) (V_S = 5.5 V, V_{CC} = 24.5 V, t_{PW} = 4.0 ms)	ΔV_{out}	 –	 –	 100	mV
Supply Current (Figure 8) (I_C = 500 mA, V_{in} = 2.4 V, V_S = 5.5 V)	I_S	 –	 –	 6.0	mA
Turn–On Delay Time (50% E_I to 50% E_O)	t_{PHL}	 –	 –	 1.0	µs
Turn–Off Delay Time (50% E_I to 50% E_O)	t_{PLH}	 –	 –	 4.0	µs
Clamp Diode Leakage Current (Figure 6) (V_R = 50 V) (V_R = 50 V, T_A = 70°C)	I_R	 – –	 – –	 50 100	µA
Clamp Diode Forward Voltage (Figure 7) (I_F = 1.0 A) (I_F = 1.5 A)	V_F	 – –	 – –	 1.75 2.0	V

TEST FIGURES

Figure 1.

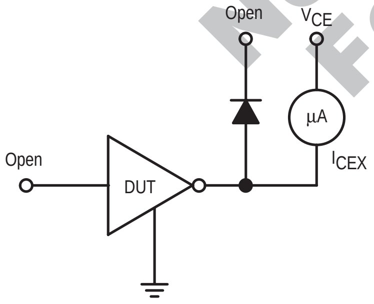


Figure 2.

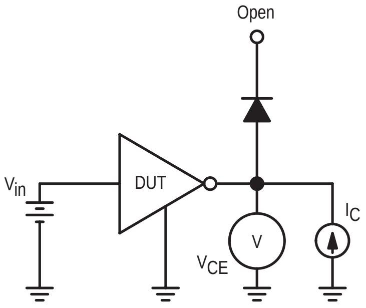


Figure 3.

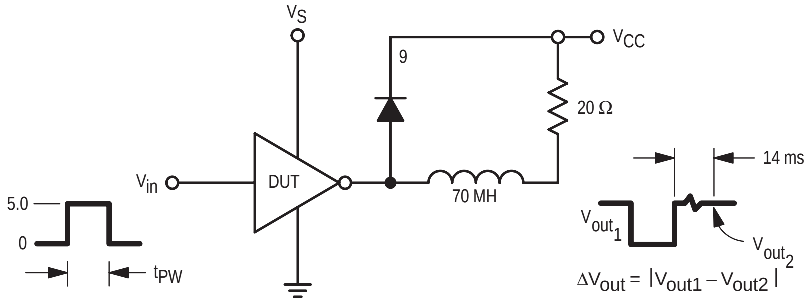
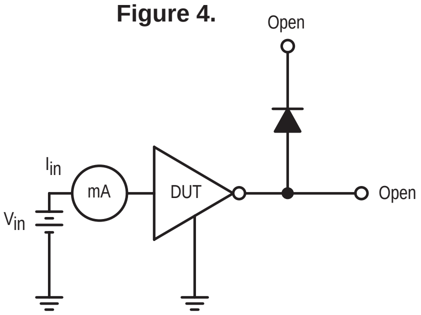


Figure 4.



TEST FIGURES (continued)

Figure 5.

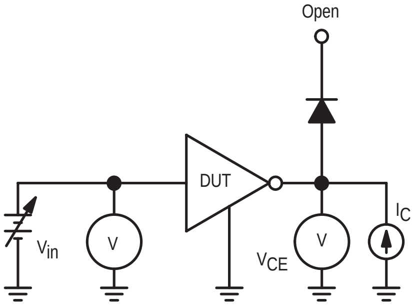


Figure 6.

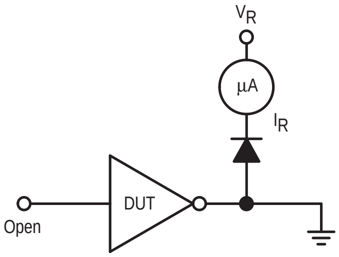


Figure 7.

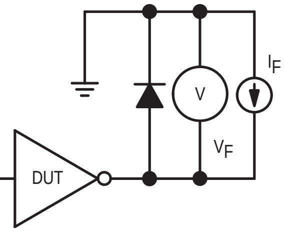
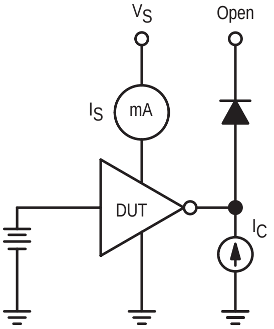


Figure 8.



TYPICAL CHARACTERISTIC CURVES – $T_A = 25°C$

Figure 9. Input Current versus Input Voltage

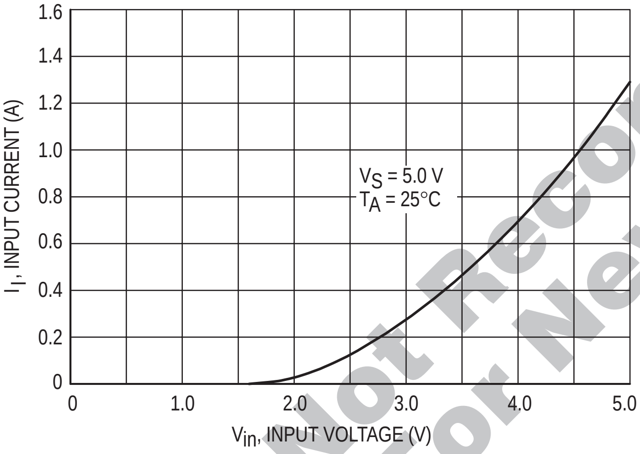


Figure 10. Collector Current versus Input Current

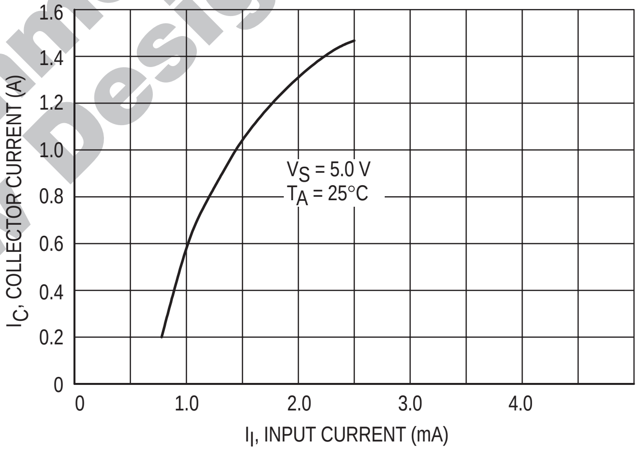


Figure 11. T_A = 70°C w/o Heat Sink

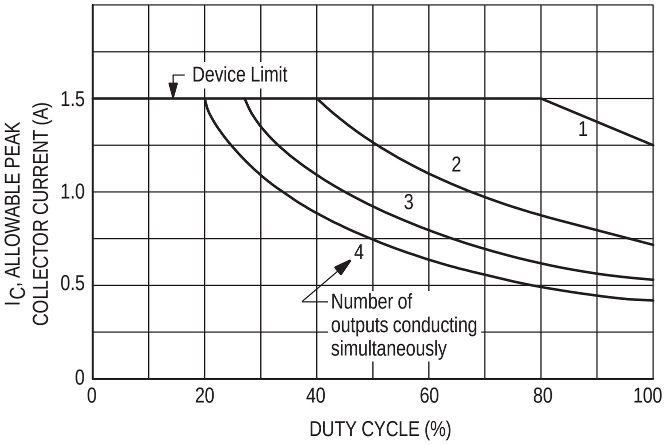


Figure 12. T_A = 70°C w/Staver V–8 Heat Sink (37.5°C/W)

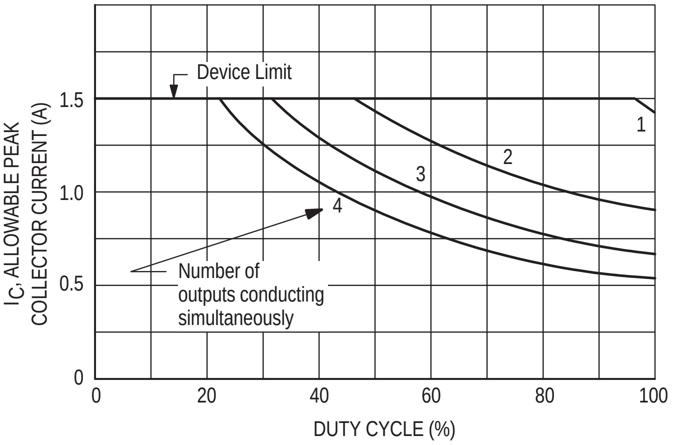


Figure 13. T_A = 70°C w/Staver V–7 Heat Sink (27.5°C/W)

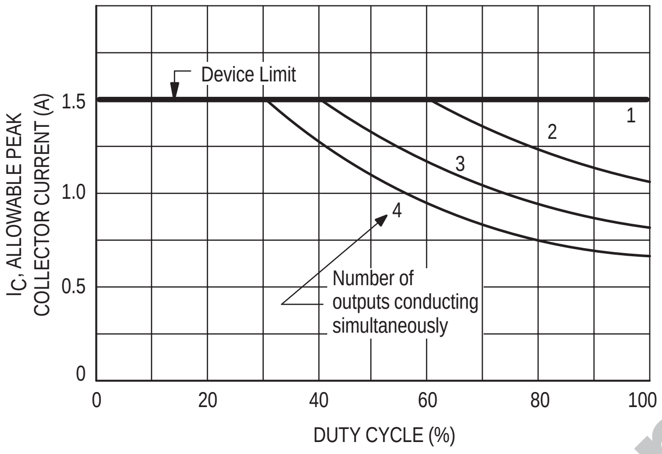


Figure 14. T_A = 50°C w/o Heat Sink

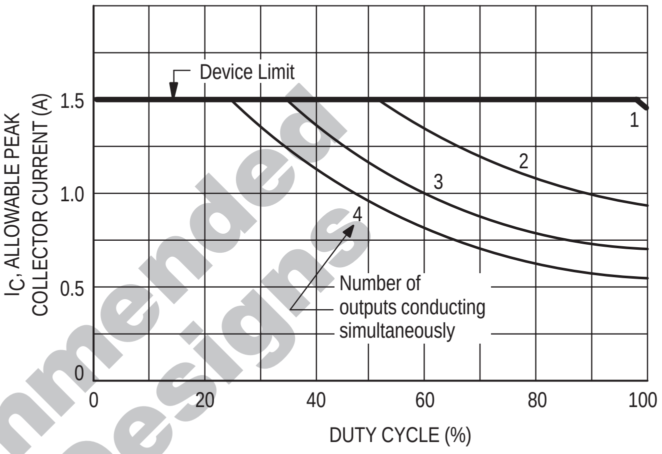


Figure 15. T_A = 50°C w/Staver V–8 Heat Sink (37.5°C/W)

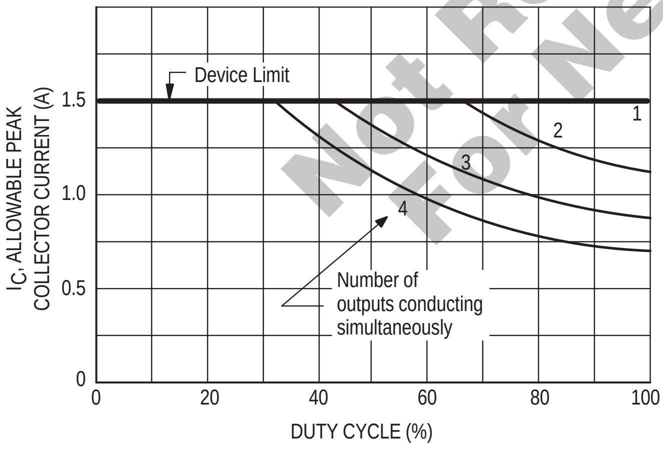
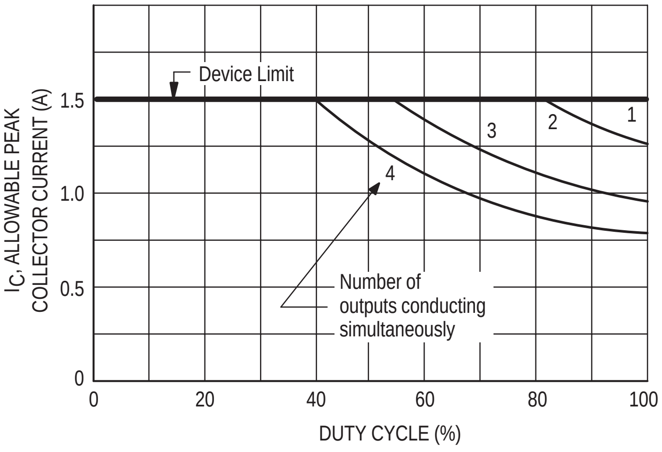


Figure 16. T_A = 50°C w/Staver V–7 Heat Sink (27.5°C/W)



ULN2803
ULN2804

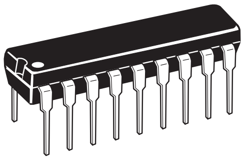
Octal High Voltage, High Current Darlington Transistor Arrays

The eight NPN Darlington connected transistors in this family of arrays are ideally suited for interfacing between low logic level digital circuitry (such as TTL, CMOS or PMOS/NMOS) and the higher current/voltage requirements of lamps, relays, printer hammers or other similar loads for a broad range of computer, industrial, and consumer applications. All devices feature open–collector outputs and free wheeling clamp diodes for transient suppression.

The ULN2803 is designed to be compatible with standard TTL families while the ULN2804 is optimized for 6 to 15 volt high level CMOS or PMOS.

OCTAL PERIPHERAL DRIVER ARRAYS

SEMICONDUCTOR TECHNICAL DATA



A SUFFIX
PLASTIC PACKAGE
CASE 707

MAXIMUM RATINGS (T_A = 25°C and rating apply to any one device in the package, unless otherwise noted.)

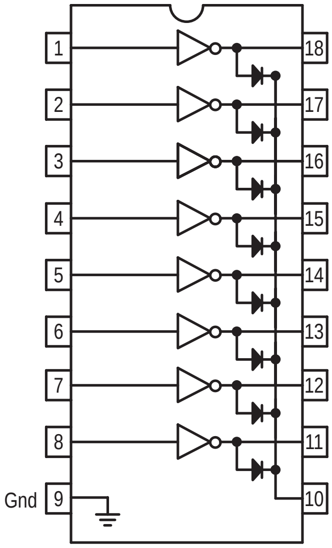
Rating	Symbol	Value	Unit
Output Voltage	V_O	50	V
Input Voltage (Except ULN2801)	V_I	30	V
Collector Current – Continuous	I_C	500	mA
Base Current – Continuous	I_B	25	mA
Operating Ambient Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	–55 to +150	°C
Junction Temperature	T_J	125	°C

$R_{\theta JA}$ = 55°C/W
Do not exceed maximum current limit per driver.

ORDERING INFORMATION

Device	Characteristics		
	Input Compatibility	V_{CE}(Max)/I_C(Max)	Operating Temperature Range
ULN2803A ULN2804A	TTL, 5.0 V CMOS 6 to 15 V CMOS, PMOS	50 V/500 mA	T_A = 0 to + 70°C

PIN CONNECTIONS



ELECTRICAL CHARACTERISTICS (T_A = 25°C, unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Output Leakage Current (Figure 1)		I_{CEX}				µA
(V_O = 50 V, T_A = +70°C)	All Types		–	–	100	
(V_O = 50 V, T_A = +25°C)	All Types		–	–	50	
(V_O = 50 V, T_A = +70°C, V_I = 6.0 V)	ULN2802		–	–	500	
(V_O = 50 V, T_A = +70°C, V_I = 1.0 V)	ULN2804		–	–	500	
Collector–Emitter Saturation Voltage (Figure 2)		$V_{CE(sat)}$				V
(I_C = 350 mA, I_B = 500 µA)	All Types		–	1.1	1.6	
(I_C = 200 mA, I_B = 350 µA)	All Types		–	0.95	1.3	
(I_C = 100 mA, I_B = 250 µA)	All Types		–	0.85	1.1	
Input Current – On Condition (Figure 4)		$I_{I(on)}$				mA
(V_I = 17 V)	ULN2802		–	0.82	1.25	
(V_I = 3.85 V)	ULN2803		–	0.93	1.35	
(V_I = 5.0 V)	ULN2804		–	0.35	0.5	
(V_I = 12 V)	ULN2804		–	1.0	1.45	
Input Voltage – On Condition (Figure 5)		$V_{I(on)}$				V
(V_{CE} = 2.0 V, I_C = 300 mA)	ULN2802		–	–	13	
(V_{CE} = 2.0 V, I_C = 200 mA)	ULN2803		–	–	2.4	
(V_{CE} = 2.0 V, I_C = 250 mA)	ULN2803		–	–	2.7	
(V_{CE} = 2.0 V, I_C = 300 mA)	ULN2803		–	–	3.0	
(V_{CE} = 2.0 V, I_C = 125 mA)	ULN2804		–	–	5.0	
(V_{CE} = 2.0 V, I_C = 200 mA)	ULN2804		–	–	6.0	
(V_{CE} = 2.0 V, I_C = 275 mA)	ULN2804		–	–	7.0	
(V_{CE} = 2.0 V, I_C = 350 mA)	ULN2804		–	–	8.0	
Input Current – Off Condition (Figure 3) (I_C = 500 µA, T_A = +70°C)	All Types	$I_{I(off)}$	50	100	–	µA
DC Current Gain (Figure 2) (V_{CE} = 2.0 V, I_C = 350 mA)	ULN2801	h_{FE}	1000	–	–	–
Input Capacitance		C_I	–	15	25	pF
Turn–On Delay Time (50% E_I to 50% E_O)		t_{on}	–	0.25	1.0	µs
Turn–Off Delay Time (50% E_I to 50% E_O)		t_{off}	–	0.25	1.0	µs
Clamp Diode Leakage Current (Figure 6)	T_A = +25°C	I_R	–	–	50	µA
(V_R = 50 V)	T_A = +70°C				100	
Clamp Diode Forward Voltage (Figure 7) (I_F = 350 mA)		V_F	–	1.5	2.0	V

TEST FIGURES

(See Figure Numbers in Electrical Characteristics Table)

Figure 1.

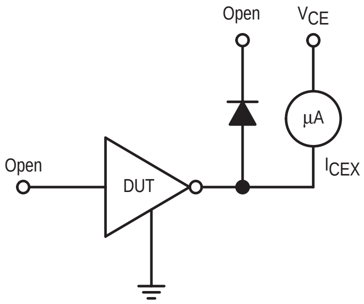


Figure 2.

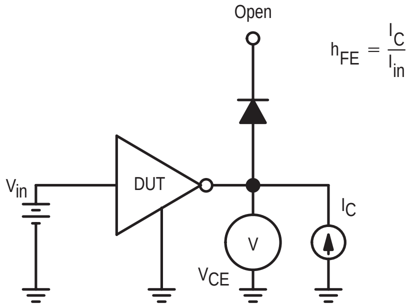


Figure 3.

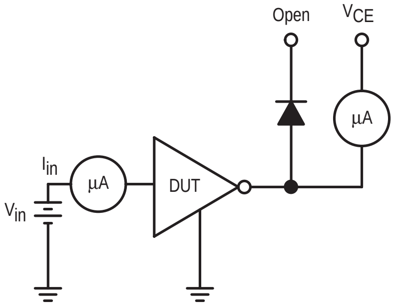


Figure 4.

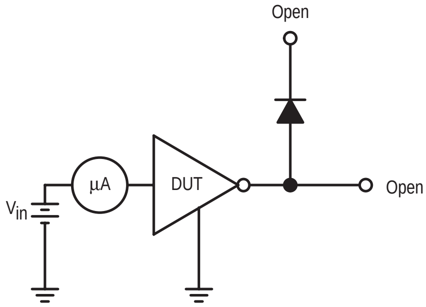


Figure 5.

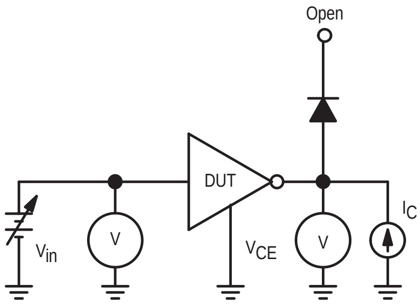


Figure 6.

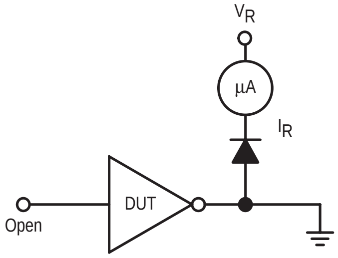
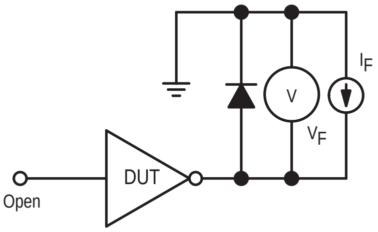


Figure 7.



TYPICAL CHARACTERISTIC CURVES – T_A = 25°C, unless otherwise noted

Output Characteristics

Figure 8. Output Current versus Saturation Voltage

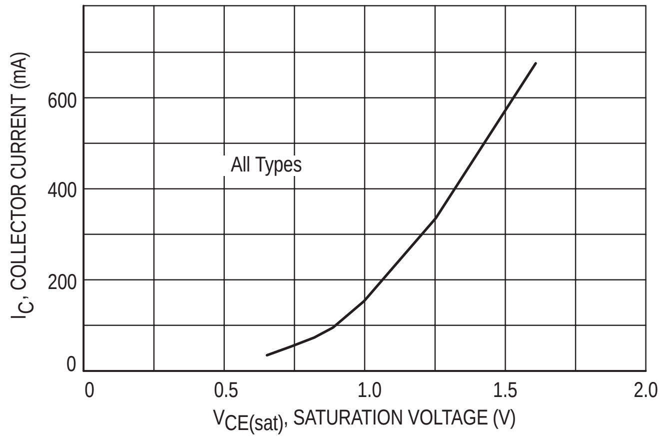
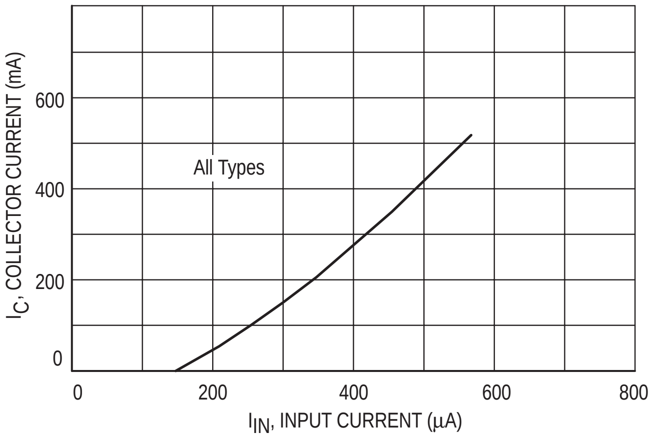


Figure 9. Output Current versus Input Current



Input Characteristics

Figure 10. ULN2803 Input Current versus Input Voltage

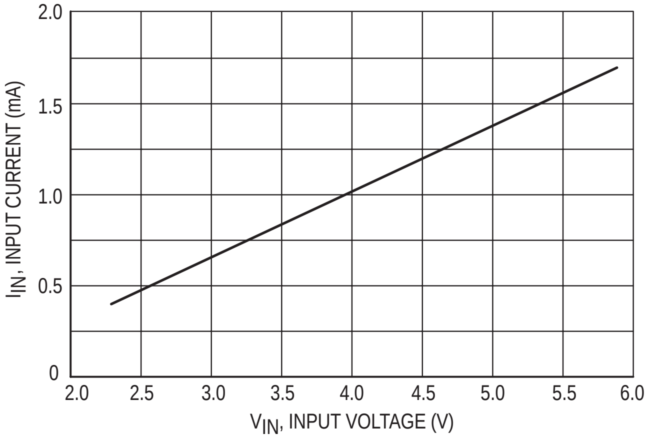


Figure 11. ULN2804 Input Current versus Input Voltage

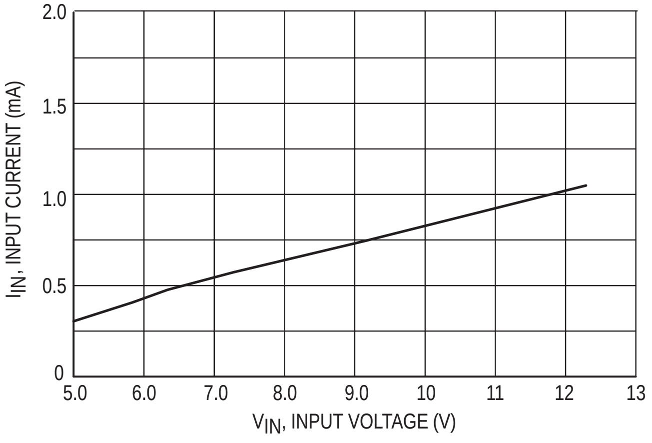
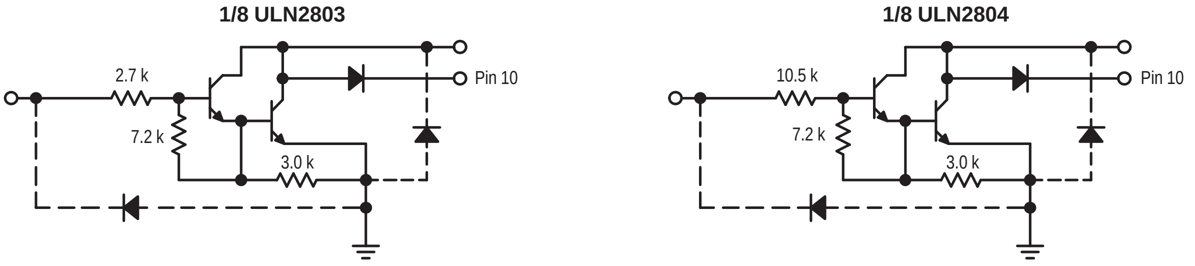


Figure 12. Representative Schematic Diagrams



Communication Circuits

In Brief . . .

RF

Radio communication has greatly expanded its scope in the past several years. Once dominated by public safety radio, the 30 to 1000 MHz spectrum is now packed with personal and low cost business radio systems. The vast majority of this equipment uses FM or FSK modulation and is targeted at short range applications. From mobile phones and VHF marine radios to garage door openers and radio controlled toys, these new systems have become a part of our lifestyle. Motorola Analog has focused on this technology, adding a wide array of new products including complete receivers processed in our exclusive 3.0 GHz MOSAIC® 1.5 process. New surface mount packages for high density assembly are available for all of these products, as well as a growing family of supporting application notes and development kits.

Telephone & Voice/Data

Traditionally, an office environment has utilized two distinctly separate wired communications systems: telecommunications and data communications. Each had its individual hardware components complement, and each required its own independent transmission line system: twisted wire pairs for Telecom and relatively high priced coaxial cable for Datacom. But times have changed. Today, Telecom and Datacom coexist comfortably on inexpensive twisted wire pairs and use a significant number of components in common. This has led to the development and enhancement of PBX (Private Branch Exchanges) to the point where the long heralded "office of the future," with simultaneous voice and data communications capability at each station, is no longer of the future at all. The capability is here today!

Motorola Semiconductor serves a wide range of requirements for the voice/data marketplace. We offer both CMOS and Analog technologies, each to its best advantage, to upgrade the conventional analog voice systems and establish new capabilities in digital communications. Early products, such as the solid–state single–chip crosspoint switch, the more recent monolithic Subscriber–Loop–Interface Circuit (SLIC), a single–chip Codec/Filter (Mono–Circuit), the Universal Digital Loop Transceivers (UDLT), basic rate ISDN (Integrated Services Digital Network), and single–chip telephone circuits are just a few examples of Motorola leadership in the voice/data area.

Page

RF Communications

Table 1. RF Front End ICs

Device	Low Noise Amplifier				Mixer				Voltage Cont Osc	V_{CC} (V)	I_{CC} (mA)	Suffix/ Package
	Gain (dB)	Noise Figure (dB)	IIP3 (dBm)	P1dB (dBm)	Gain (dB)	Noise Figure (dB)	IIP3 (dBm)	P1dB (dBm)				
MC13141	17	1.8	–5	–15	7	16	–3 to +15	–10	–	2.7 to 6.5	7.7	D1/751, D/751A, FTB/976
MC13142	17	1.8	–5	–15	±3	12	–3 to +21	3	Yes	2.7 to 6.5	13	D/751B, FTB/976
MC13143	–	–	–	–	±3	12	–3 to +21	3	–	1.8 to 6.5	1	D/751
MC13144	13 to 19	1.4	–1	–7	–	–	–	–	–	1.8 to 6.5	2 to 9	D/751

NOTES: All devices operate over a wide range of RF input and IF frequencies, from dc to 2.0 GHz.
Typical performance shown at 900 MHz.

Table 2. Wideband (FM/FSK) IFs

Device	V_{CC}	I_{CC}	Sensitivity (Typ)	IF	Mute	RSSI	Max Data Rate	Notes	Suffix/ Package
MC13055	3–12 V	25 mA	20 µV	40 MHz	✓	✓	2.0 Mb	Wideband Data IF, includes data shaper	P/648, D/751B
MC13155	3–6 V	7.0 mA	100 µV	250 MHz	–		10 Mb	Video Speed FM IF	D/751B

Table 3. Wideband Single Conversion Receivers – VHF

Device	V_{CC}	I_{CC}	Sensitivity (Typ)	RF Input	IF	Mute	RSSI	Max Data Rate	Notes	Suffix/ Package
MC3356	3–9 V	25 mA	30 µV	200 MHz	10.7 MHz	✓	✓	500 kb	Includes front end mixer/L.O.	P/738, DW/751D
MC13156	2–6 V	5.0 mA	2.0 µV	500 MHz	21.4 MHz	–			CT–2 FM/Demodulator	DW/751E, FB/873
MC13158	2–6 V	6.0 mA						>1.2 Mb	FM IF/Demodulator with split IF for DECT	FTB/873
MC13159	2.7–5 V	5.5 mA		600 MHz				500 kb	FM IF for PHS	DTB/948F

Table 4. Narrowband Single Conversion Receivers – VHF

Device	V_{CC}	I_{CC}	12 dB SINAD Sensitivity (Typ)	RF Input	IF	Mute	RSSI	Max Data Rate	Notes	Suffix/ Package
MC3357	4–8 V	5.0 mA	5.0 µV	45 MHz	455 kHz	✓	–	> 4.8 kb	Ceramic Quad Detector/Resonator	P/648, D/751B
MC3359	4–9 V	7.0 mA	2.0 µV						Scan output option	P/707, DW/751D
MC3371	2–8 V	6.0 mA		60 MHz			✓	> 4.8 kb	RSSI	P/648, D/751B, DTB/948F
MC3372									RSSI, Ceramic Quad Detector/Resonator	
MC13150	3–6 V	1.8 mA	1.0 µV	500 MHz			✓ 110 dB	>9.6 kb	Coilless Detector with Adjustable Bandwidth	FTB/873, FTA/977

RF Communications (continued)

Table 5. Narrowband Dual Conversion Receivers – FM/FSK – VHF

Device	V_{CC}	I_{CC}	12 dB SINAD Sensitivity (Typ)	RF Input	IF1	IF2 (Limiter In)	Mute	RSSI	Data Rate	Notes	Suffix/ Package
MC3362	2–7 V	3.0 mA	0.7 µV	180 MHz	10.7 MHz	455 kHz	–	✓	> 4.8 kb	Includes buffered VCO output	P/724, DW/751E
MC3363		4.0 mA	0.4 µV				✓			Includes RF amp/mute	DW/751F
MC3335			0.7 µV							Low cost version	DW/751D, P/738
MC13135			1.0 µV				–			Voltage buffered RSSI, LC Quad Detector	DW/751E, P/724
MC13136										Voltage Buffered RSSI, Ceramic Quad Detector	

Table 6. Universal Cordless Phone Subsystem ICs

Device	V_{CC}	I_{CC}	Dual Conversion Receiver	Universal Dual PLL	Compander and Audio Interface	Voice Scrambler	Low Battery Detect	Programmable R_X, T_X Trim Gain and LBD Voltage Reference	Suffix/ Package
MC13109	2.0–5.5 V	Active Mode 6.7 mA Inactive Mode 40 µA	✓	✓	✓	–	1	–	FB/848B, FTA/932
MC13110	2.7–5.5 V	Active Mode 8.2 mA Inactive Mode 60 µA	✓	✓	✓	✓	2	✓	FB/848B
MC13111	2.7–5.5 V	Active Mode 8.2 mA Inactive Mode 60 µA	✓	✓	✓	–	2	✓	FB/848B

Table 7. Transmitters – AM/FM/FSK

Device	V_{CC}	I_{CC}	P_{out}	Max RF Freq Out	Max Mod Freq	Notes	Suffix/ Package
MC2833	3–8 V	10 mA	–30 dBm to +10 dBm	150 MHz	50 kHz	FM transmitter. Includes two frequency multiplier/amplifier transistors	P/648, D/751B
MC13175	2–5 V	40 mA	8.0 dBm	500 MHz	5.0 MHz	AM/FM transmitter. Single frequency PLL $f_{out} = 8 \times f_{ref}$, includes power down function	D/751B
MC13176				1.0 GHz		$f_{out} = 32 \times f_{ref}$, includes power down function	

Table 8. Balanced Modulator/Demodulator

Device	V_{CC}	I_{CC}	Function	Suffix/ Package
MC1496	3–5 V	10 mA	General purpose balanced modulator/demodulator for AM, SSB, FM detection with Carrier Balance >50 dB	P/646, D/751A

Table 9. Infrared Transceiver

Device	V_{CC}	I_{CC}	12 dB SINAD Sensitivity (Typ)	Max IF Freq	Carr Det	RSSI	Data Rate	Notes	Suffix/ Package
MC13173	3–5 V	6.5 mA	5.0 µV	10.7 MHz	✓	✓	200 kb	Includes Single Frequency PLL for T_X Carrier and R_X L_O	FTB/873

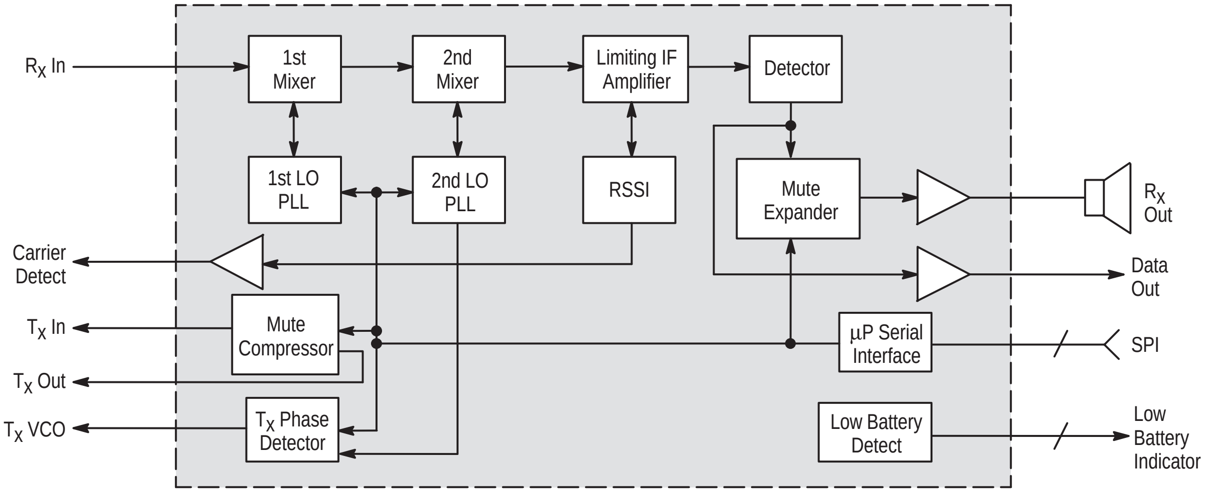
Universal Cordless Telephone Subsystem IC

MC13109FB, FTA

T_A = –20° to +85°C, Case 848B, 932

The MC13109 integrates several of the functions required for a cordless telephone into a single integrated circuit. This significantly reduces component count, board space requirements, and external adjustments. It is designed for use in both the handset and the base.

- Dual Conversion FM Receiver
  - Complete Dual Conversion Receiver – Antenna Input to Audio Output 80 MHz Maximum Carrier Frequency
  - RSSI Output
  - Carrier Detect Output with Programmable Threshold
  - Comparator for Data Recovery
  - Operates with Either a Quad Coil or Ceramic Discriminator
- Compander
  - Expandor Includes Mute, Digital Volume Control and Speaker Driver
  - Compressor Includes Mute, ALC and Limiter
- Dual Universal Programmable PLL
  - Supports New 25 Channel U.S. Standard with No External Switches
  - Universal Design for Domestic and Foreign CT–1 Standards
  - Digitally Controlled Via a Serial Interface Port
  - Receive Side Includes 1st LO VCO, Phase Detector, and 14–Bit Programmable Counter and 2nd LO with 12–Bit Counter
  - Transmit Section Contains Phase Detector and 14–Bit Counter
  - MPU Clock Output Eliminates Need for MPU Crystal
- Supply Voltage Monitor
  - Externally Adjustable Trip Point
- 2.0 to 5.5 V Operation with One–Third the Power Consumption of Competing Devices



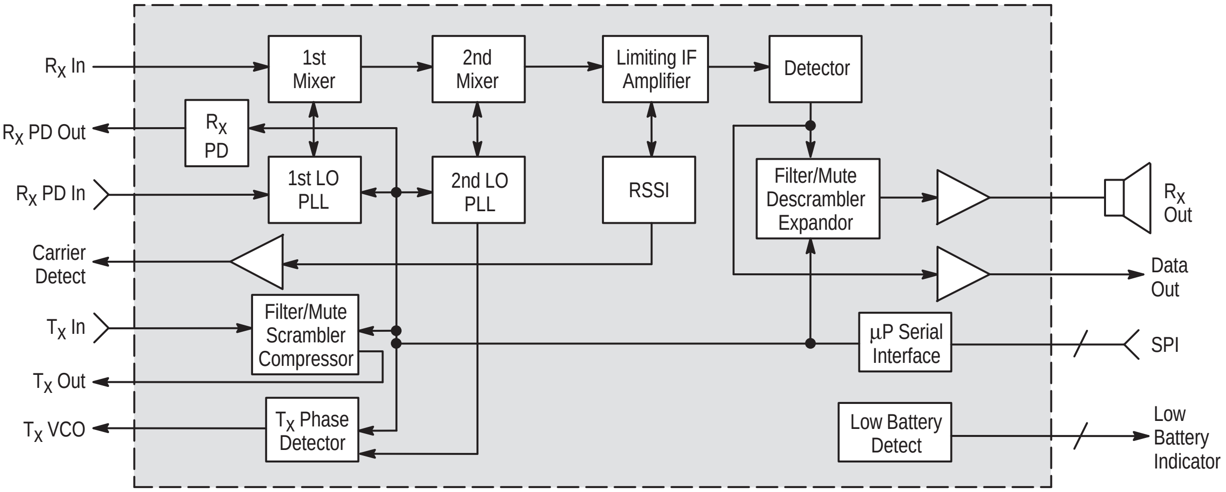
Universal Cordless Telephone Subsystem IC with Scrambler

MC13110FB

T_A = –40° to +85°C, Case 848B

The MC13110 integrates several of the functions required for a cordless telephone into a single integrated circuit. This significantly reduces component count, board space requirements, and external adjustments. It is designed for use in both the handset and the base.

- Dual Conversion FM Receiver
  - Complete Dual Conversion Receiver – Antenna In to Audio Out 80 MHz Maximum Carrier Frequency
  - RSSI Output
  - Carrier Detect Output with Programmable Threshold
  - Comparator for Data Recovery
  - Operates with Either a Quad Coil or Ceramic Discriminator
- Compander
  - Expandor Includes Mute, Digital Volume Control, Speaker Driver, 3.5 kHz Low Pass Filter, and Programmable Gain Block
  - Compressor Includes Mute, 3.5 kHz Low Pass Filter, Limiter, and Programmable Gain Block
- Dual Universal Programmable PLL
  - Supports New 25 Channel U.S. Standard with New External Switches
  - Universal Design for Domestic and Foreign CT–1 Standards
  - Digitally Controlled Via a Serial Interface Port
  - Receive Side Includes 1st LO VCO, Phase Detector, and 14–Bit Programmable Counter and 2nd LO with 12–Bit Counter
  - Transmit Section Contains Phase Detector and 14–Bit Counter
  - MPU Clock Outputs Eliminates Need for MPU Crystal
- Supply Voltage Monitor
  - Provides Two Levels of Monitoring with Separate Outputs
  - Separate, Adjustable Trip Points
- Frequency Inversion Scrambler/Descrambler
  - Can Be Enabled/Disabled Via MPU Interface
  - Programmable Carrier Modulation Frequency
- 2.7 to 5.5 V Operation with One–Third the Power Consumption of Competing Devices



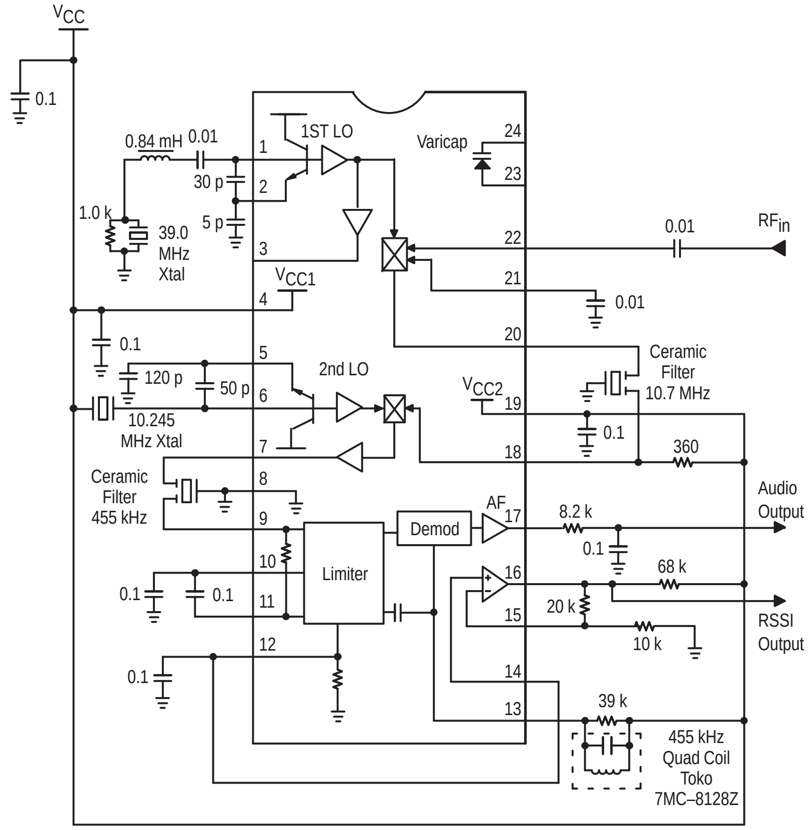
Narrowband FM Receiver

MC13135/136P, DW

T_A = –40° to +85°C, Case 724, 751E

The MC13135 is a full dual conversion receiver with oscillators, mixers, Limiting IF Amplifier, Quadrature Discriminator, and RSSI circuitry. It is designed for use in security systems, cordless phones, and VHF mobile and portable radios. Its wide operating supply voltage range and low current make it ideal for battery applications. The Received Signal Strength Indicator (RSSI) has 65 dB of dynamic range with a voltage output, and an operational amplifier is included for a dc buffered output. Also, an improved mixer third order intercept enables the MC13135 to accommodate larger input signal levels.

- Complete Dual Conversion Circuitry
- Low Voltage: 2.0 to 6.0 Vdc
- RSSI with Op Amp: 65 dB Range
- Low Drain Current: 3.5 mA Typical
- Improved First and Second Mixer 3rd Order Intercept
- Detector Output Impedance: 25 Ω Typically



Narrowband FM Coilless Detector IF Subsystem

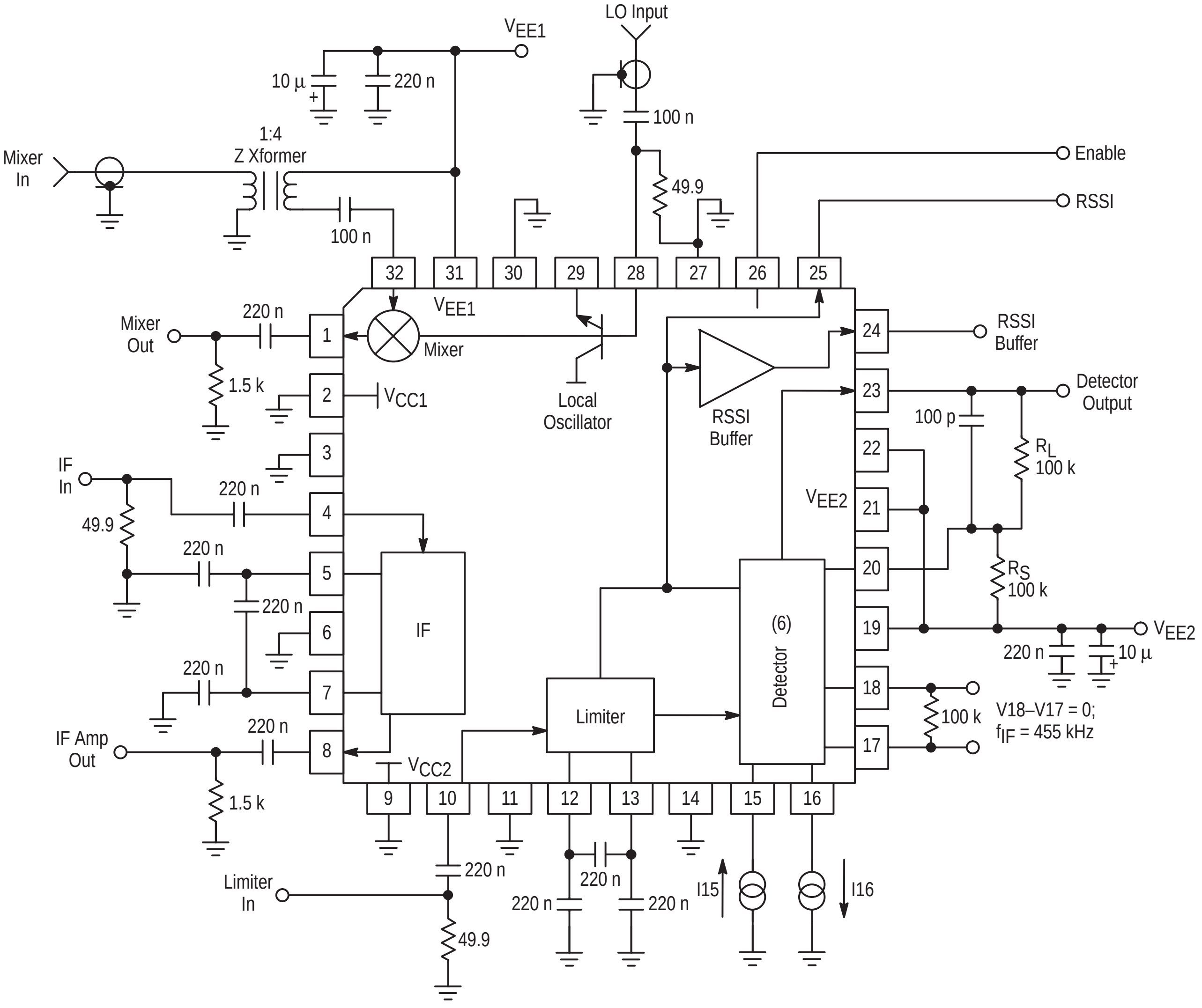
MC13150FTA, FTB

T_A = –40° to +85°C, Case 977, 873

The MC13150 is a narrowband FM IF subsystem targeted at cellular and other analog applications. Excellent high frequency performance is achieved, with low cost, through use of Motorola's MOSAIC 1.5™ RF bipolar process. The MC13150 has an onboard Colpitts VCO for Crystal controlled second LO in dual conversion receivers. The mixer is a double balanced configuration with excellent third order intercept. It is useful to beyond 200 MHz. The IF amplifier is split to accommodate two low cost cascaded filters. RSSI output is derived by summing the output of both IF sections. The quadrature detector is a unique design eliminating the conventional tunable quadrature coil.

Applications for the MC13150 include cellular, CT–1 900 MHz cordless telephone, data links and other radio systems utilizing narrowband FM modulation.

- Linear Coilless Detector
- Adjustable Demodulator Bandwidth
- 2.5 to 6.0 Vdc Operation
- Low Drain Current: < 2.0 mA
- Typical Sensitivity of 2.0 µV for 12 dB SINAD
- IIP3, Input Third Order Intercept Point of 0 dBm
- RSSI Range of Greater Than 100 dB
- Internal 1.4 kΩ Terminations for 455 kHz Filters
- Split IF for Improved Filtering and Extended RSSI Range



Wideband FM IF System

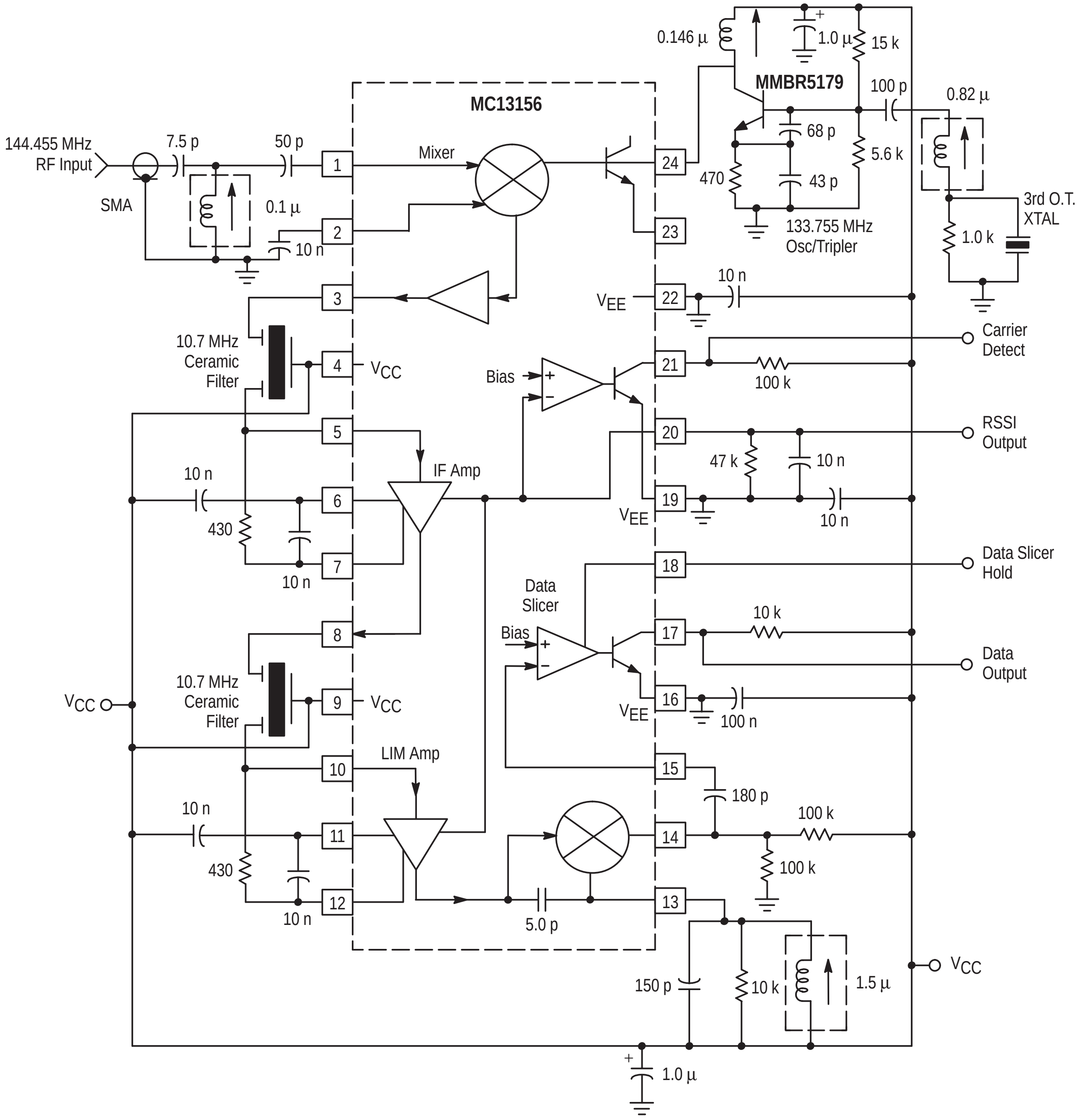
MC13156DW, FB

$T_A = –40°$ to $+85°C$, Case 751E, 873

The MC13156 is a wideband FM IF subsystem targeted at high performance data and analog applications. Excellent high frequency performance is achieved, with low cost, through use of Motorola's MOSAIC 1.5™ RF bipolar process. The MC13156 has an onboard Colpitts VCO for PLL controlled multichannel operation. The mixer is useful to beyond 200 MHz and may be used in a differential, balanced, or single–ended configuration. The IF amplifier is split to accommodate two low cost cascaded filters. RSSI output is derived by summing the output of both IF sections. A precision data shaper has a hold function to preset the shaper for fast recovery of new data.

Applications for the MC13156 include CT–2, wideband data links, and other radio systems utilizing GMSK, FSK or FM modulation.

- 2.0 to 6.0 Vdc Operation
- Typical Sensitivity of 6.0 µV for 12 dB SINAD
- RSSI Dynamic Range Typically 80 dB
- High Performance Data Shaper for Enhanced CT–2 Operation
- Internal 300 Ω and 1.4 kΩ Terminations for 10.7 MHz and 455 kHz Filters
- Split IF for Improved Filtering and Extended RSSI Range



Wideband FM IF Subsystem

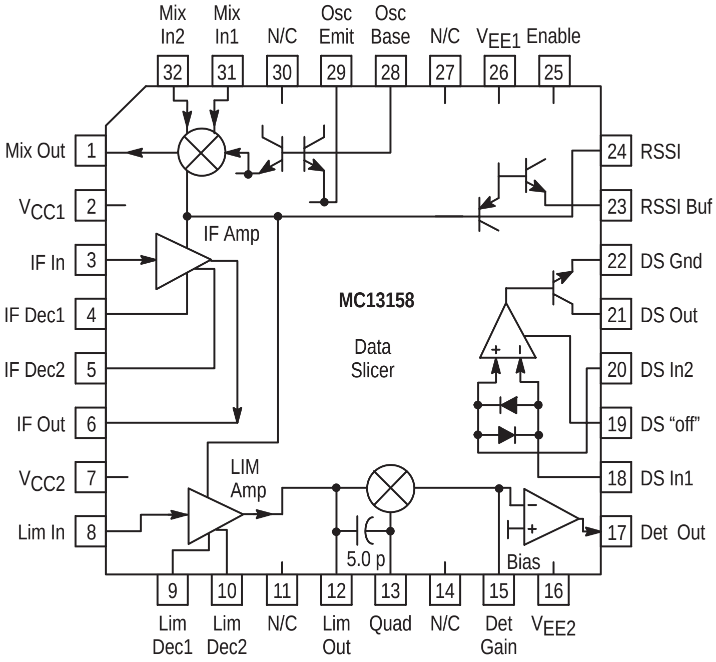
MC13158FTB

T_A = –40° to +85°C, Case 873

The MC13158 is a wideband IF subsystem that is designed for high performance data and analog applications. Excellent high frequency performance is achieved, with low cost, through the use of Motorola's MOSAIC 1.5™ RF bipolar process. The MC13158 has an on–board grounded collector VCO transistor that may be used with a fundamental or overtone crystal in single channel operation or with a PLL in multi–channel operation. The mixer is useful to 500 MHz and may be used in a balanced differential or single ended configuration. The IF amplifier is split to accommodate two low cost cascaded filters. RSSI output is derived by summing the output of both IF sections. A precision data shaper has an Off function to shut the output "off" to save current. An enable control is provided to power down the IC for power management in battery operated applications.

Applications include DECT, wideband wireless data links for personal and portable laptop computers and other battery operated radio systems which utilize GFSK, FSK or FM modulation.

- Designed for DECT Applications
- 1.8 to 6.0 Vdc Operating Voltage
- Low Power Consumption in Active and Standby Mode
- Greater than 600 kHz Detector Bandwidth
- Data Slicer with Special Off Function
- Enable Function for Power Down of Battery Operated Systems
- RSSI Dynamic Range of 80 dB Minimum
- Low External Component Count



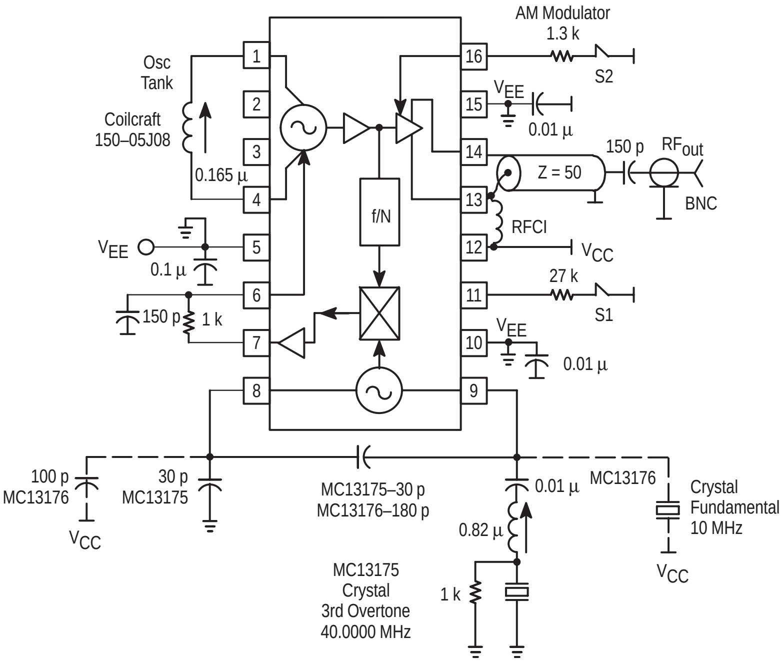
UHF, FM/AM Transmitter

MC13175/176D

T_A = 0° to +70°C, Case 751B

The MC13175 and MC13176 are one chip FM/AM transmitter subsystems designed for AM/FM communication systems operating in the 260 to 470 MHz band covered by FCC Title 47; Part 15. They include a Colpitts crystal reference oscillator, UHF oscillator, ÷8 (MC13175) or ÷32 (MC13176) prescaler, and phase detector forming a versatile PLL system. Another application is as a local oscillator in a UHF or 900 MHz receiver. MC13175/176 offer the following features:

- UHF Current Controlled Oscillator
- Use Easily Available 3rd Overtone or Fundamental Crystals for Reference
- Low Number of External Parts Required
- Low Operating Supply Voltage (1.8 – 5 Vdc)
- Low Supply Drain Currents
- Power Output Adjustable (Up to +10 dBm)
- Differential Output for Loop Antenna or Balun Transformer Networks
- Power Down Feature
- ASK Modulated by Switching Output “On”/“Off”
- MC13175 – $f_o = 8 \times f_{ref}$
- MC13176 – $f_o = 32 \times f_{ref}$



Telecommunications

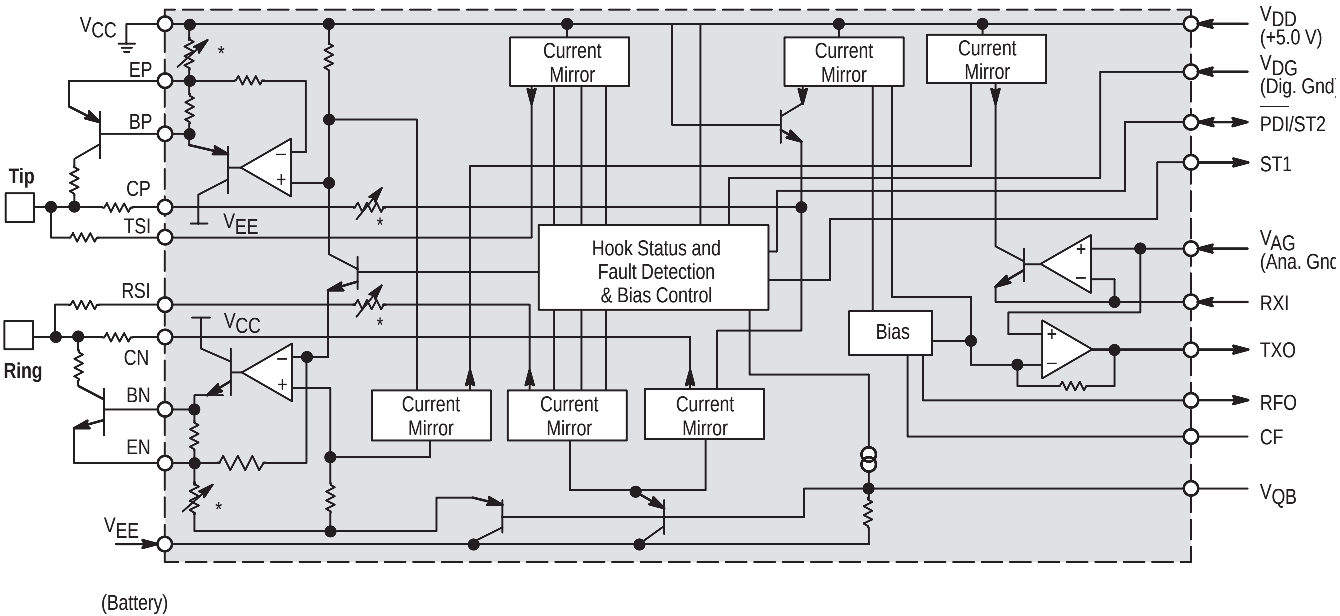
Subscriber Loop Interface Circuit (SLIC)

MC33120/1P, FN

T_A = –40° to +85°C, Case 738, 776

With a guaranteed minimum longitudinal balance of 58 dB, the MC33120/1 is ideally suited for Central Office applications, as well as PBXs, and other related equipment. Protection and sensing components on the two–wire side can be non–precision while achieving required system performance. Most BORSHT functions are provided while maintaining low power consumption, and a cost effective design. Size and weight reduction over conventional transformer designs permit a higher density system.

- All Key Parameters Externally Programmable with Resistors:
  - Transmit and Receive Gains
  - Transhybrid Loss
  - Return Loss
  - DC Loop Current Limit and Battery Feed Resistance
  - Longitudinal Impedance
- Single and Double Fault Sensing and Protection
- Minimum 58 dB Longitudinal Balance (2–wire and 4–wire) Guaranteed
- Digital Hook Status and Fault Outputs
- Power Down Input
- Loop Start or Ground Start Operation
- Size & Weight Reduction Over Conventional Approaches
- Available in 20 Pin DIP and 28 Pin PLCC Packages
- Battery Voltage: –42 to –58 V (for MC33120),
  –21.6 to –42 V (for MC33121)



* Indicates Trimmed Resistor

PBX Architecture (Analog Transmission)

PCM Mono–Circuits Codec–Filters (CMOS LSI)

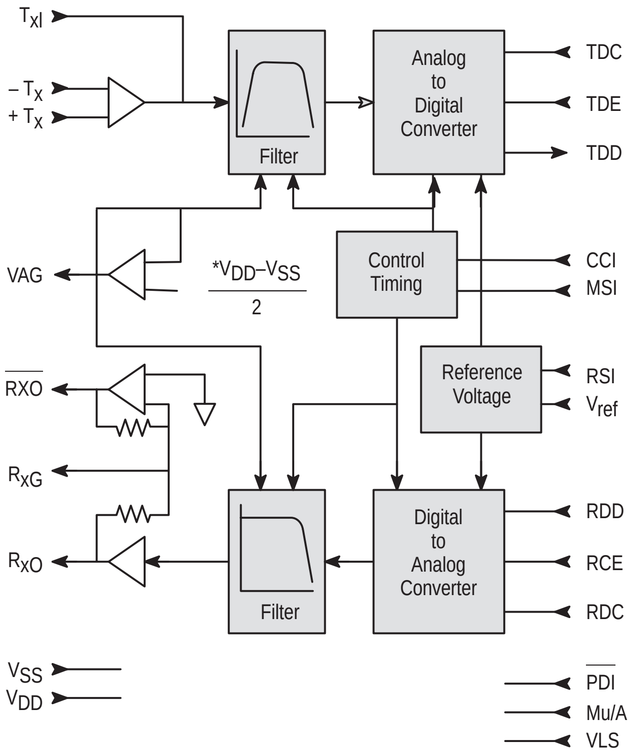
MC145500 Series

Case 648, 708, 751G, 776

The Mono–circuits perform the digitizing and restoration of the analog signals. In addition to these important functions, Motorola's family of pulse–code modulation mono–circuits also provides the band–limiting filter functions – all on a single monolithic CMOS chip with extremely low power dissipation.

The Mono–circuits require no external components. They incorporate the bandpass filter required for antialiasing and 60 Hz rejection, the A/D–D/A conversion functions for either U.S. Mu–Law or European A–Law companding formats, the low–pass filter required for reconstruction smoothing, an on–board precision voltage reference, and a variety of options that lend flexibility to circuit implementations. Unique features of Motorola's Mono–circuit family include wide power supply range (6.0 to 13 V), selectable on–board voltage reference (2.5, 3.1, or 3.8 V), and TTL or CMOS I/O interface.

Motorola supplies three versions in this series. The MC145503 and MC145505 are general–purpose devices in 16 pin packages designed to operate in digital telephone or line card applications. The MC145502 is the full–feature device that presents all of the options available on the chip. This device is packaged in a 22 pin DIP and 28 pin chip carrier package.



MC145554/57/64/67

Case 648, 751D, 751G, 738

These per channel PCM Codec–Filters perform the voice digitization and reconstruction as well as the band limiting and smoothing required for PCM systems. They are designed to operate in both synchronous and asynchronous applications and contain an on–chip precision voltage reference. The MC145554 (Mu–Law) and MC145557 (A–Law) are general purpose devices that are offered in 16 pin packages. The MC145564 (Mu–Law) and MC145567 (A–Law), offered in 20 pin packages, add the capability of analog loop–back and push–pull power amplifiers with adjustable gain.

All four devices include the transmit bandpass and receive lowpass filters on–chip, as well as active RC pre–filtering and post–filtering. Fully differential analog circuit design assures lowest noise. Performance is specified over the extended temperature range of –40° to +85°C.

These PCM Codec–Filters accept both industry standard clock formats. They also maintain compatibility with Motorola's family of MC3419/MC33120 SLIC products.

MC14LC5480P, DW, SD

Case 738, 751D, 940C–02

This 5.0 V, general purpose per channel PCM Codec–Filter offers selectable Mu–Law or A–Law companding in 20 pin DIP, SOG and SSOP packages. It performs the voice digitization and reconstruction as well as the band limiting and smoothing required for PCM systems. It is designed to operate in both synchronous and asynchronous applications and contains an on–chip precision reference voltage (1.575 V).

The transmit bandpass and receive lowpass filters, and the active RC pre–filtering and post–filtering are incorporated, as well as fully differential analog circuit design for lowest noise. Push–pull 300 Ω power drivers with external gain adjust are also included.

The MC14LC5480 PCM Codec–Filter accepts a variety of clock formats, including short–frame sync, long–frame sync, IDL, and GCI timing environments. This device also maintains compatibility with Motorola's family of Telecom products, including the MC145472 U–Interface Transceiver, MC145474/75 S/T–Interface Transceiver, MC145532 ADPCM Transcoder, MC145422/26 UDLT–I, MC145421/25 UDLT–II, and MC3419/MC33120 SLIC.

Replaces the MC145480P, DW, SD.

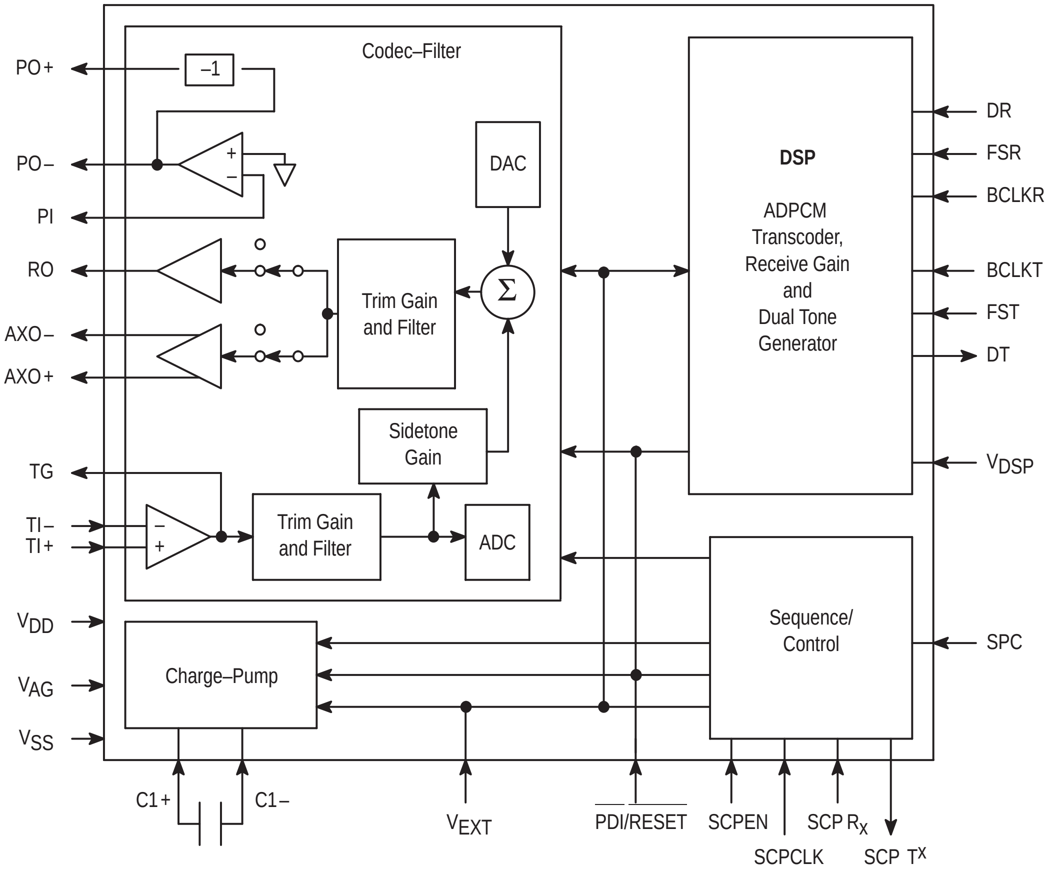
MC14LC5540P, DW, FU

Case 710, 751F, 873

The MC14LC5540 ADPCM Codec is a single chip implementation of a PCM Codec–Filter and an ADPCM encoder/decoder, and therefore provides an efficient solution for applications requiring the digitization and compression of voiceband signals. This device is designed to operate over a wide voltage range, 2.7 V to 5.25 V, and as such is ideal for battery powered as well as ac powered applications. The MC14LC5540 ADPCM Codec also includes a serial control port and internal control and status registers that permit a microcomputer to exercise many built–in features.

The ADPCM Codec is designed to meet the 32 kbps ADPCM conformance requirements of CCITT Recommendation G.721 (1988) and ANSI T1.301 (1987). It also meets ANSI T1.303 and CCITT Recommendation G.723 for 24 kbps ADPCM operation, and the 16 kbps ADPCM standard, CCITT Recommendation G.726. This device also meets the PCM conformance specification of the CCITT G.714 Recommendation.

Figure 1. MC14LC5540 ADPCM Codec Block Diagram



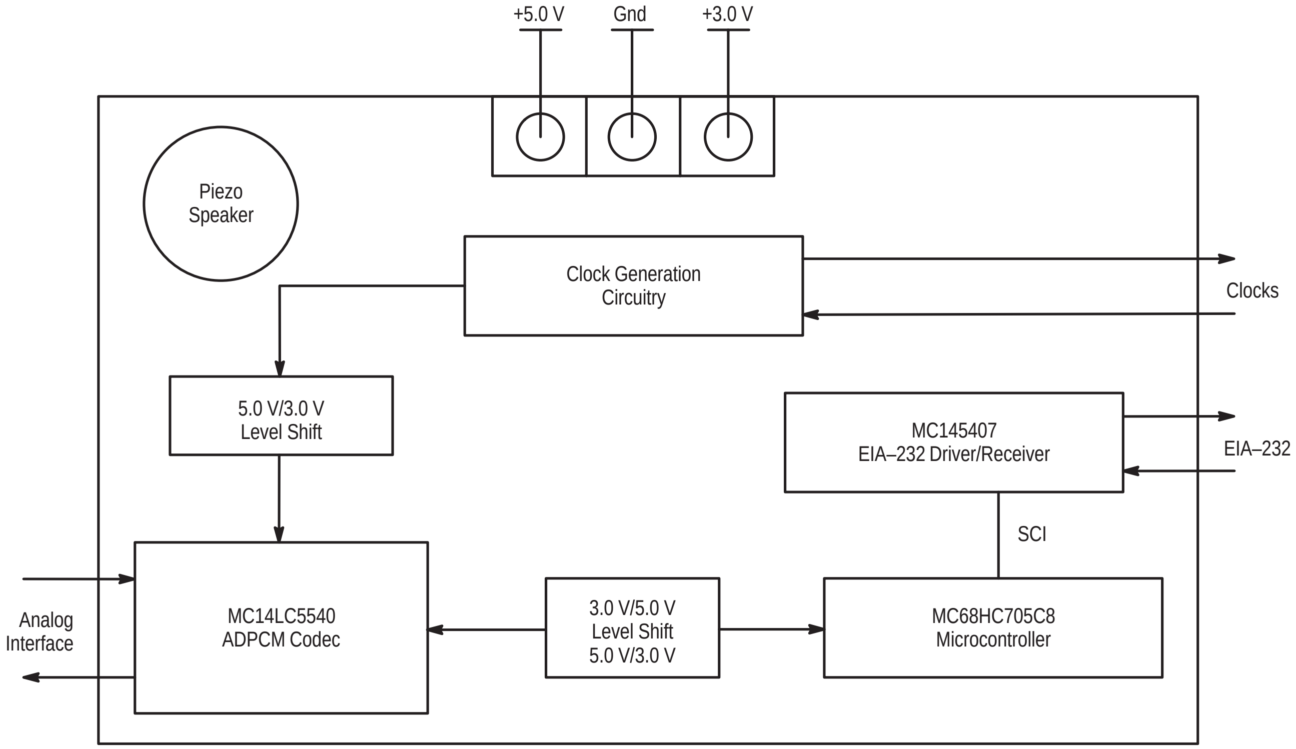
MC145537EVK

ADPCM Codec Evaluation Kit

The MC145537EVK is the primary tool for evaluation and demonstration of the MC14LC5540 ADPCM Codec. It provides the necessary hardware and software interface to access the many features and operational modes of the MC14LC5540 ADPCM Codec.

- Provides Stand Alone Evaluation on Single Board
- The kit provides Analog–to–Analog, Analog–to–Digital or Digital–to–Analog Connections – with Digital Connections being 64 kbps PCM, 32 or 24 kbps ADPCM, or 16 kbps CCITT G.726 or Motorola Proprietary ADPCM
- +5.0 V Only Power Supply, or 5.0 V Plus 2.7 to 5.25 V Supply
- Easily Interfaced to Test Equipment, Customer System, Second MC145537EVK or MC145536EVK (5.0 V Only) for Full Duplex Operation
- Convenient Access to Key Signals
- Piezo Loudspeaker
- EIA–232 Serial Computer Terminal Interface for Control of the MC14LC5540 ADPCM Codec Features
- Compatible Handset Provided
- Schematics, Data Sheets, and User’s Manual Included

Figure 2. MC145537EVK Block Diagram

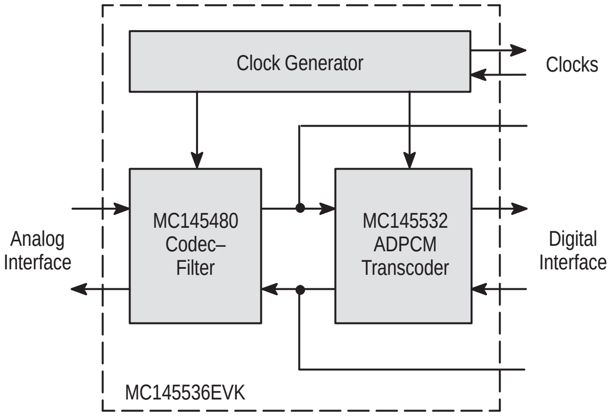


MC145536EVK

Codec–Filter/ADPCM Transcoder Evaluation Kit

The MC145536EVK is the primary tool for evaluation and demonstration of the MC14LC5480 Single +5.0 V supply PCM Codec–Filter and the MC145532 ADPCM Transcoder (see ‘‘Telephone Accessory Circuits’’). The MC145536EVK provides the necessary hardware needed to evaluate the many separate operating modes under which the MC14LC5480 and MC145532 are intended to operate.

- Provides Stand Alone Evaluation on a Single Board
- Easily Interfaced to Test Equipment, Customer System, or Second MC145536EVK
- Convenient Access to Key Signals
- Generous Wire–Wrap Area for Application Development
- The kit provides Analog–to–Analog, Analog–to–Digital, or Digital–to–Analog Connections – with Digital Connections Being 64 kbps PCM; 32, 24, or 16 kbps Motorola Proprietary ADPCM
- Compatible Handset Included
- Schematics, Data Sheets, and User’s Manual included



Dual Tone Multiple Frequency Receiver

MC145436AP, DW

Case 646, 751G

This device contains the filter and decoder for detection of a pair of tones conforming to the DTMF standard with outputs in hexadecimal. Switched capacitor filter technology is used together with digital circuitry for the timing control and output circuits. The MC145436A provides excellent power–line noise and dial tone rejection.

Replaces MC145436P, DW.

ISDN Voice/Data Circuits

Integrated Services Digital Network

ISDN is the revolutionary concept of converting the present analog telephone networks to an end–to–end global digital network. ISDN standards make possible a wide variety of services and capabilities that are revolutionizing communications in virtually every industry.

Motorola’s ISDN product family includes the MC14LC5472 and MC145572 U–Interface Transceivers, the MC145474/75 and MC145574 S/T–Interface Transceivers, MC145488 Dual Data Link Controller, and the MC68302 Integrated Multi–Protocol Processor. These are supported by a host of related devices including the MC14LC5480 +5.0 V PCM Codec–Filter, MC145532 ADPCM Transcoder, MC14LC5540 ADPCM Codec, MC145500 family of single–chip codec/filters, MC145436A DTMF Decoder, MC33120 Subscriber Loop Interface Circuit, MC34129 Switching Power Supply Controller, and the MC145406/07 CMOS EIA 232–E Driver/ Receiver family.

Motorola’s key ISDN devices fit into four ISDN network applications: a digital subscriber line card, an NT1 network termination, an ISDN terminal adapter, and an ISDN terminal. Digital subscriber line cards are used in central offices, remote concentrators, channel banks, T1 multiplexers, and other switching equipment. The NT1 network termination block illustrates the simplicity of remote U– to S/T–interface conversion. The ISDN terminal adapter and ISDN terminal block show how Motorola ICs are used to combine voice and data in PC compatible boards, digital telephones, and other terminal equipment. Expanded applications such as a PBX may include these and other Motorola ISDN circuits. Many “non–ISDN” uses, such as pairgain applications, are appropriate for Motorola’s ISDN devices as well.

Second Generation U–Interface Transceivers

MC145572PB

Case 842D

MC145572FN

Case 777

The MC145572 fully conforms to ANSI T1.601–1992, the North American standard for ISDN Basic Access on a single twisted–wire pair. The transceiver achieves a remarkable 10^{-7} bit error rate performance on all ANSI specified test loops with worst–case impairments present. The state–of–the–art 0.65 micron single–chip solution uses advanced design techniques to combine precision analog signal processing elements with three digital signal coprocessors to build an adaptively equalized echo cancelling receiver.

Two modes of handling U–interface maintenance functions are provided on the MC145572. In the automatic maintenance mode the U–interface transceiver handles all ANSI specified maintenance and channel procedures internally to minimize your software development effort. Automatic procedures include generating and monitoring the cyclic redundancy check, reporting and counting far end block errors (near end block errors too), handling the ACT and DEA bits, as well as monitoring and appropriately responding to embedded operations channel messages.

The MC145572 has 275 mW maximum power dissipation. It also has an enhanced TDM interface that supports an on–chip timeslot assigner, GCI and IDL modes of operation.

The optional manual maintenance mode lets you choose an inexpensive microcontroller, such as a member of Motorola's MC68HC05 family, to control and augment the standard maintenance channel functions. This flexible feature also allows for easy implementation of proprietary maintenance functions.

Second Generation S/T–Interface Transceivers

MC145574PB

Case 873A

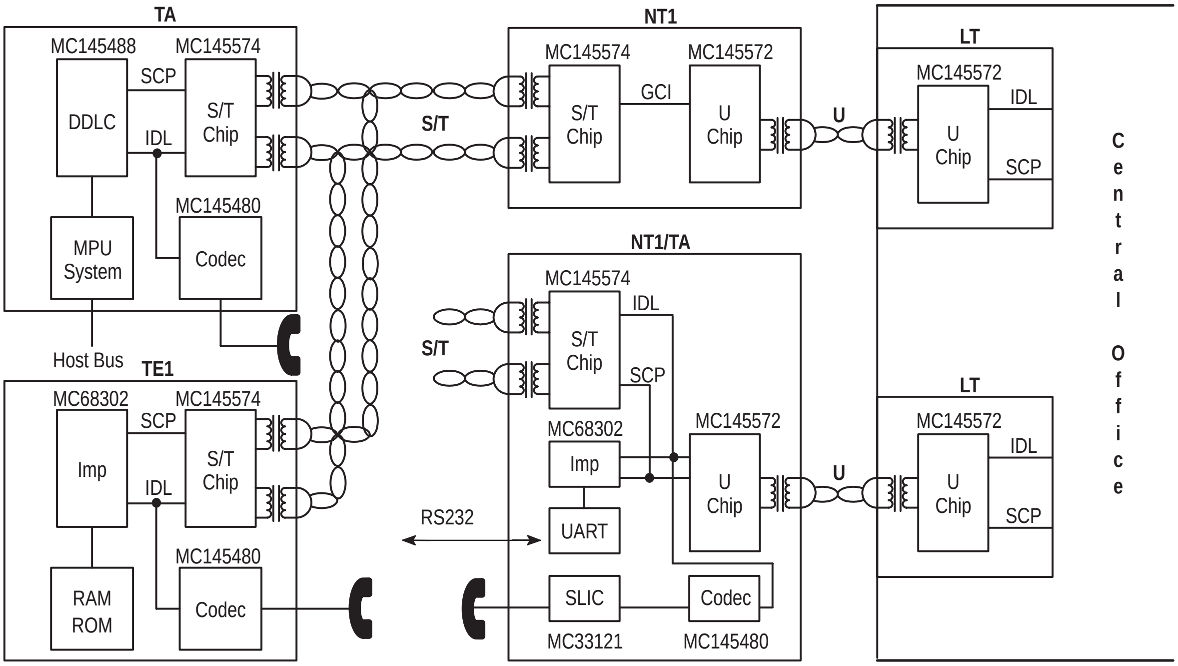
MC145574DW

Case 751F

The MC145574 S/T–Interface Transceivers provide a CCITT I.430 compatible interface for use in line card, network termination, and ISDN terminal equipment applications. Manufactured with Motorola's advanced 0.65 micron CMOS mixed analog and digital process technology, the MC145574 is a physical layer device capable of operating in point–to–point or point–to–multipoint passive bus arrangements. In addition, the MC145574 implements the optional NT1 Star topology, NT terminal mode and TE slave mode.

This device features outstanding transmission performance. It reliably transmits over 1 kilometer in a point–to–point application. Comparable performance is achieved in all other topologies as well. Other features include pin selectable terminal or network operating modes, industry standard microprocessor serial control port, full support of the multiframing S and Q channels, a full range of loopbacks, and low power CMOS operation, with a maximum power consumption of 90 mW.

The MC145574 has an enhanced TDM interface that supports GCI, IDL and an on–chip timeslot assigner.



Dual Data Link Controller

MC145488FN
Case 779

The MC145488 features two full–duplex serial HDLC channels with an on–chip Direct Memory Access (DMA) controller. The DMA controller minimizes the number of microprocessor interrupts from the communications channels, freeing the microprocessor’s resources for other tasks. The DMA controller can access up to 64 kbytes of memory, and transfers either 8–bit bytes or 16–bit words to or from memory. The MC145488 DDLC is compatible with Motorola’s MC68000 and other microprocessors.

In a typical ISDN terminal application, one DDLC communications channel supports the D–channel (LAPD) while the other supports the B–channel (LAPB). While the DDLC is ideally suited for ISDN applications, it can support many other HDLC protocol applications as well.

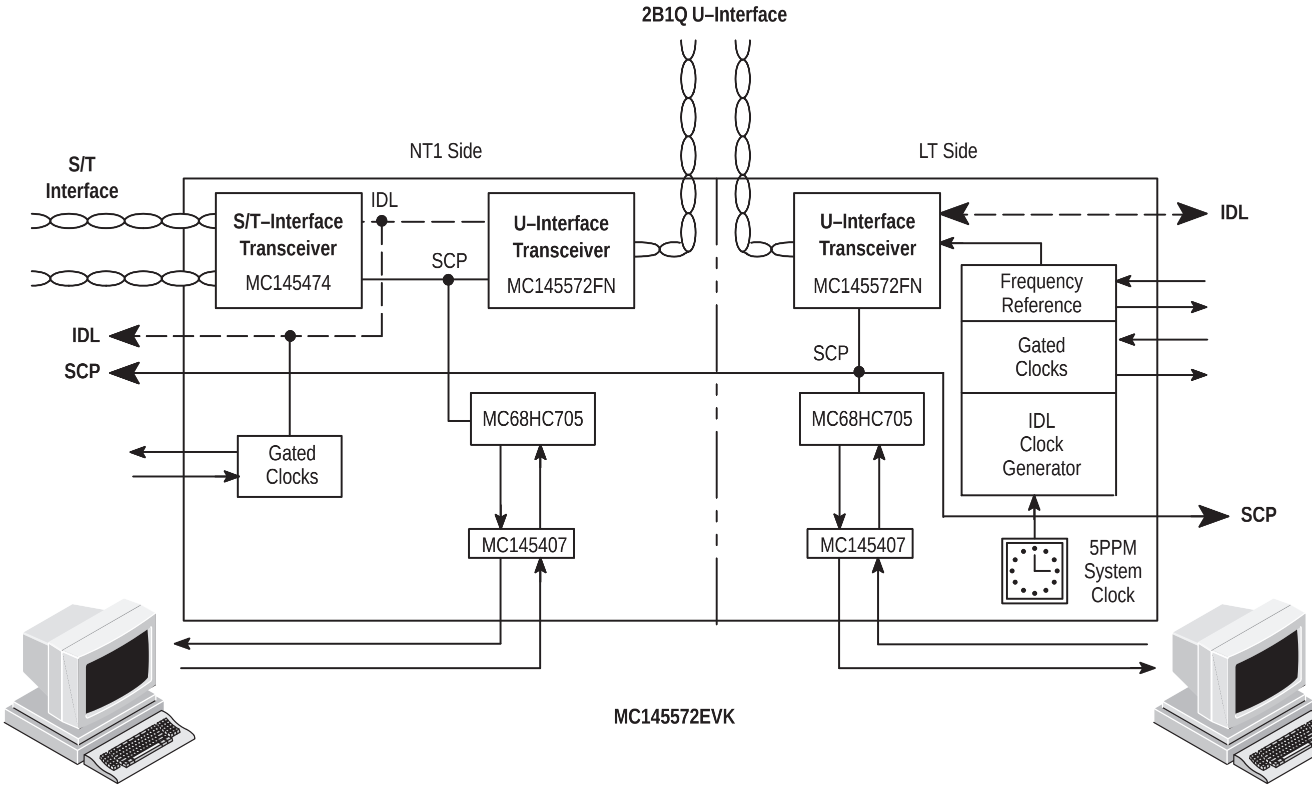
Some of the powerful extras found on the DDLC include automatic abort and retransmit of D–channel collisions in S/T–interface applications, address recognition, automatic recovery mechanisms for faulty frame correction, and several system test modes. Address recognition provides a reduction in the host microprocessor load by filtering data frames not addressed to the host. The DDLC can compare either SAPI or TEI fields of LAPD frames. For LAPD (Q.921) applications, both A and B addresses may be checked.

MC14LC5494EVK
U–Interface Transceiver Evaluation Kit discontinued

MC145572EVK
U–Interface Transceiver Evaluation Kit

This kit provides the hardware and software to evaluate the many configurations under which the MC145572EVK is able to operate. Used as a whole, it operates as both ends of the two–wire U interface that extends from the customer premises (NT1) to the switch line card (LT). The two halves of the board can be physically and functionally separated, providing independent NT1 and LT evaluation capability.

The kit provides the ability to interactively manipulate status registers in the MC145572EVK U–Interface transceiver or in the MC145474/75 S/T–Interface transceiver with the aid of an external terminal. The device can also be controlled using the MC68302 Integrated Multiprotocol Processor application development system to complete a total Basic Rate ISDN evaluation solution.



Voice/Data Communication (Digital Transmission)

2–Wire Universal Digital Loop Transceiver (UDLT)

MC145422P, DW Master Station

Case 708, 751E

MC145426P, DW Slave Station

Case 708, 751E

The UDLT family of transceivers allows the use of existing twisted–pair telephone lines (between conventional telephones and a PBX) for the transmission of digital data. With the UDLT, every voice–only telephone station in a PBX system can be upgraded to a digital telephone station that handles the complex voice/data communications with no increase in cabling costs.

In implementing a UDLT–based system the A/D to D/A conversion function associated with each telset is relocated from the PBX directly to the telset. The SLIC (or its equivalent circuit) is eliminated since its signaling information is transmitted digitally between two UDLTs.

The UDLT master–slave system incorporates the modulation/demodulation functions that permit data communications over a distance up to 2 kilometers. It also provides the sequence control that governs the exchange of information between master and slave. Specifically, the master resides on the PBX line card where it transmits and receives data over the wire pair to the telset. The slave is located in the telset and interfaces the mono–circuit to the wire pair. Data transfer occurs in 10–bit bursts (8 bits of data and 2 signaling bits), with the master transmitting first, and the slave responding in a synchronized half–duplex transmission format.

UDLTs utilize a 256 kilobaud Modified Differential Phase Shift Keyed (MDPSK) burst modulation technique for transmission to minimize radio frequency, electromagnetic, and crosstalk interference. Implementation through CMOS technology takes advantage of low–power operation, increased reliability, and the proven capabilities to perform complex telecommunications functions.

Functional Features

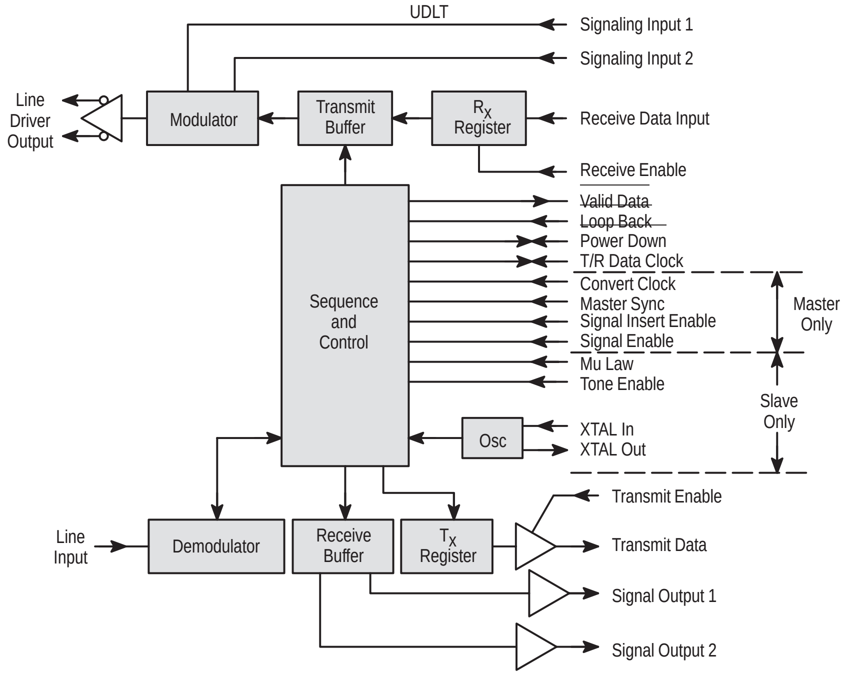
- Provides Synchronous Duplex 64 kbits/Second Voice/Data Channel and Two 8 kbits/Second Signaling Data Channels Over One 26 AWG Wire Pair Up to 2 km.
- Compatible with Existing and Evolving Telephone Switch Architectures and Call Signaling Schemes
- Automatic Detection Threshold Adjustment for Optimum Performance Over Varying Signal Attenuations
- Protocol Independent
- Single 5.0 V to 8.0 V Power Supply

MC145422 Master UDLT

- 2.048 MHz Master Clock
- Pin Controlled Power–Down and Loop–Back Features
- Variable Data Clock – 64 kHz to 2.56 MHz
- Pin Controlled Insertion/Extraction of 8 kbits/Seconds Channel into LSB of 64 kbits/Second Channel for Simultaneous Routing of Voice and Data Through PCM Voice Path of Telephone Switch

MC145426 Slave UDLT

- Compatible with MC145500 Series and Later PCM Mono–Circuits
- Automatic Power–Up/Down Feature
- On–Chip Data Clock Recovery and Generation
- Pin Controlled 500 Hz D3 or CCITT Format PCM Tone Generator for Audible Feedback Applications



2–Wire ISDN Universal Digital Loop Transceiver II (UDLT II)

MC145421P, DW Master

Case 709, 751E

MC145425P, DW Slave

Case 709, 751E

Similar to the MC145422/26 UDLT, but provide synchronous full duplex 160 kbps voice and data communication in a 2B + 2D format for ISDN compatibility on a single twisted pair up to 1 km. Single 5.0 V power supply, protocol independent.

Electronic Telephone

The Complete Electronic Telephone Circuit

MC34010P, FN

T_A = –20° to +60°C, Case 711, 777

The conventional transformer–driven telephone handset is undergoing major innovations. The bulky transformer is disappearing. So are many of its discrete components, including the familiar telephone bell. They are being replaced with integrated circuits that perform all the major handset functions simply, reliably and inexpensively . . . functions such as 2–to–4 wire conversion, DTMF dialing, tone ringing, and a variety of related activities.

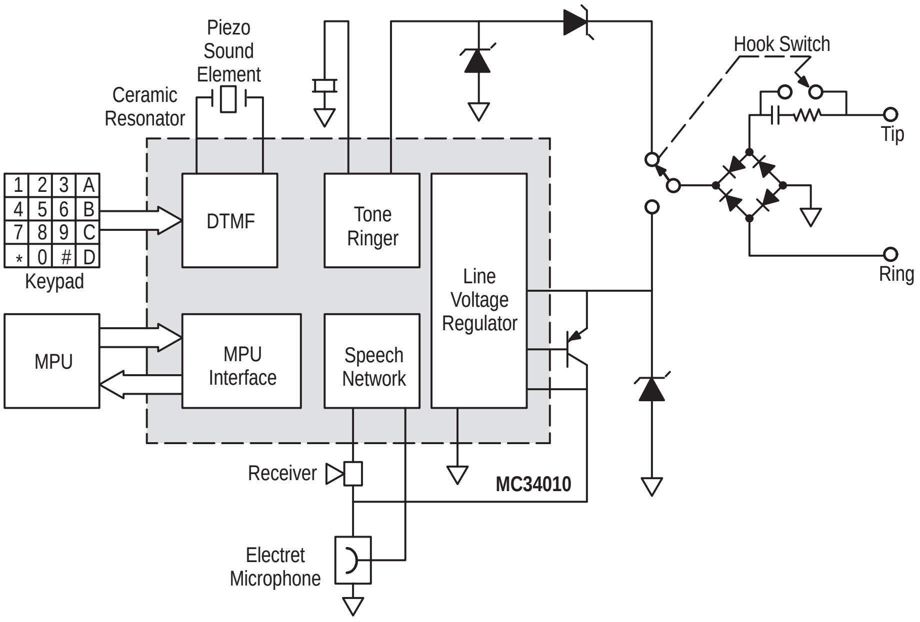
The culmination of these capabilities is the Electronic Telephone Circuit, the MC34010. These ICs place all of the above mentioned functions on a single monolithic chip.

These telephone circuits utilize advanced bipolar analog (I^2L) technology and provide all the necessary elements of a modern tone–dialing telephone. The MC34010 even incorporates an MPU interface circuit for the inclusion of automatic dialing in the final system.

- Provides all basic telephone functions, including DTMF dialer, tone ringer, speech network and line voltage regulator
- DTMF generator uses low cost ceramic resonator with accurate frequency synthesis technique
- Tone ringer drives piezoelectric transducer and satisfies EIA–470 requirements
- Speech network provides 2–to–4 wire conversion with adjustable sidetone utilizing an electret transmitter
- On–chip regulator insures stable operation over wide range of loop lengths
- I^2L technology provides low 1.4 V operation and high static discharge immunity
- Microprocessor interface port for automatic dialing features

Also Available

A broad line of additional telephone components for customizing systems design.



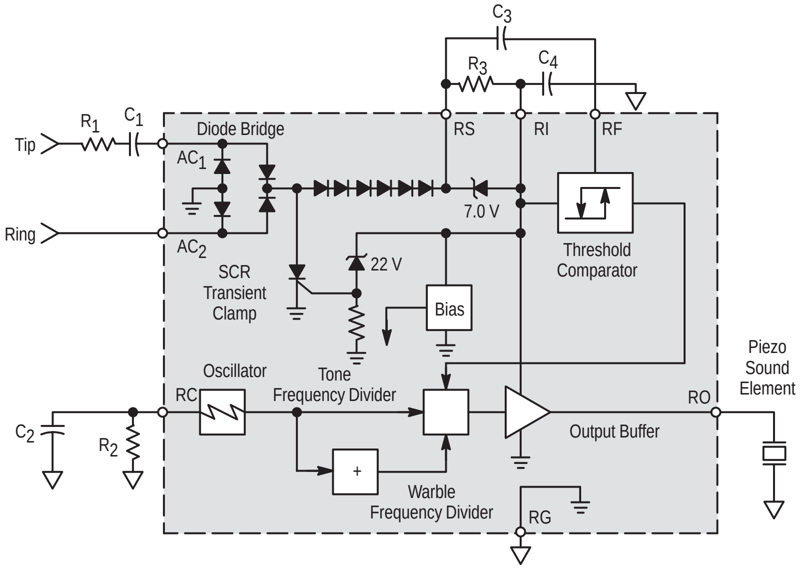
Tone Ringers

The MC34012, MC34017, and MC34117 Tone Ringers are designed to replace the bulky bell assembly of a telephone, while providing the same function and performance under a variety of conditions. The operational requirements spelled out by the FCC and EIA–470, simply stated, are that a ringer circuit MUST function when a ringing signal is provided, and MUST NOT ring when other signals (speech, dialing, noise) are on the line. The tone ringers described below were designed to meet those requirements with a minimum of external components.

MC34012P, D

T_A = –20° to +60°C, Case 626, 751

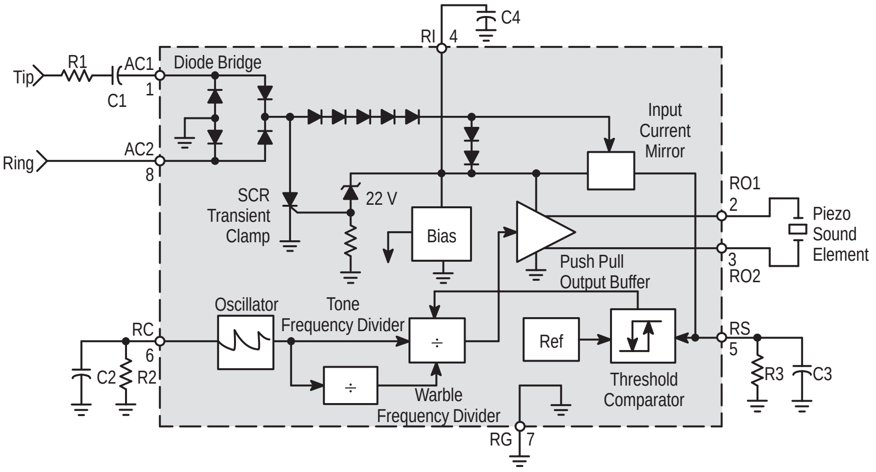
- Complete Telephone Bell Replacement
- On–Chip Diode Bridge and Transient Protection
- Single–Ended Output to Piezo Transducer
- Input Impedance Signature Meets Bell and EIA Standards
- Rejects Rotary Dial and Hook Switch Transients
- Adjustable Base Frequencies
- Output Frequency to Warble Ratio –
    - MC34012–1:80
    - MC34012–2:160
    - MC34012–3:40



MC34017P, D

T_A = –20° to +60°C, Case 626, 751

- Complete Telephone Bell Replacement Circuit with Minimum External Components
- On–Chip Diode Bridge and Transient Protection
- Direct Drive for Piezoelectric Transducers
- Push Pull Output Stage for Greater Output Power Capability
- Base Frequency Options
    - – MC34017–1: 1.0 kHz
    - – MC34017–2: 2.0 kHz
    - – MC34017–3: 500 Hz
- Input Impedance Signature Meets Bell and EIA Standards
- Rejects Rotary Dial Transients

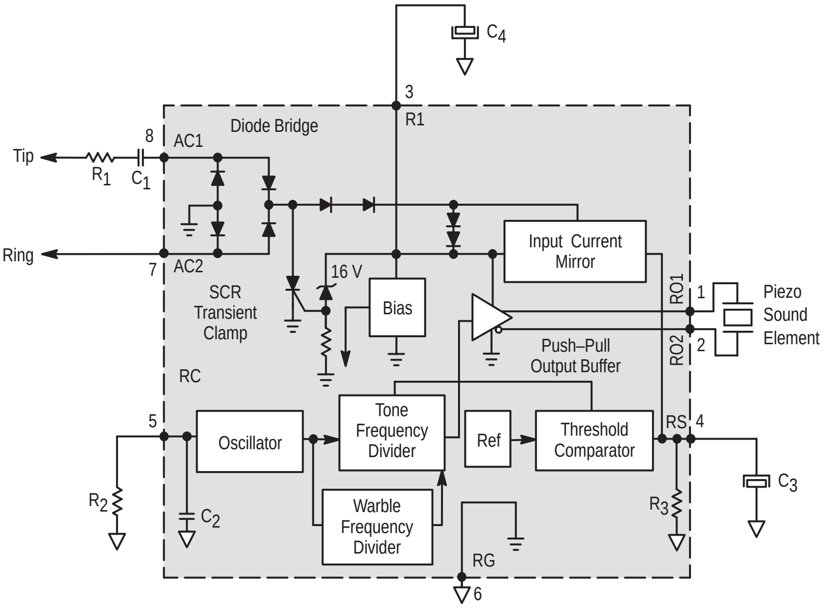


Tone Ringers **(continued)**

MC34217P, D

T_A = –20° to +60°C, Case 626, 751

- Complete Telephone Bell Replacement
- On–Chip Diode Bridge
- Internal Transient Protection
- Differential Output to Piezo Transducer for Louder Sound
- Input Impedance Signature Meets Bell and EIA Standards
- Rejects Rotary Dial and Hook Switch Transients
- Base Frequency and Warble Frequencies are Independently Adjustable
- Adjustable Base Frequency
- Reduced Number of Externals



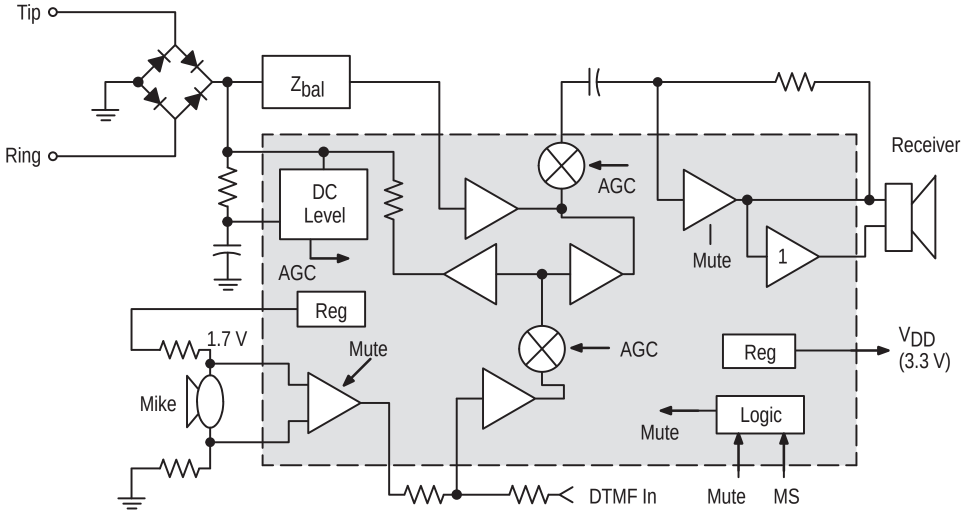
Speech Networks

Telephone Speech Network with Dialer Interface

MC34114P, DW

T_A = –20° to +70°C, Case 707, 751D

- Operation Down to 1.2 V
- Adjustable Transmit, Receive, and Sidetone Gains by External Resistors
- Differential Microphone Amplifier Input Minimizes RFI
- Transmit, Receive, and Sidetone Equalization on both Voice and DTMF Signals
- Regulated 1.7 V Output for Biasing Microphone
- Regulated 3.3 V Output for Powering External Dialer
- Microphone and Receive Amplifiers Muted During Dialing
- Differential Receive Amplifier Output Eliminates Coupling Capacitor
- Operates with Receiver Impedances of 150 Ω and Higher



Cordless Universal Telephone Interface

MC34016DW, P

T_A = –20° to +70°C, Case 751D, 738

The MC34016 is a telephone line interface meant for use in cordless telephone base stations for CT0, CT1, CT2 and DECT. The circuit forms the interface towards the telephone line and performs all speech and line interface functions like dc and ac line termination, 2–4 wire conversion, automatic gain control and hookswitch control. Adjustment of transmission parameters is accomplished by two 8 bit registers accessible via the integrated serial bus interface and by external components.

- DC Masks for Voltage and Current Regulation
- Supports Passive or Active AC Set Impedance Applications
- Double Wheatstone Bridge Sidetone Architecture
- Symmetrical Inputs and Outputs with Large Signal Swing Capability
- Gain Setting and Mute Function for T_X and R_X Amplifiers
- Very Low Noise Performance
- Serial Bus Interface SPI Compatible
- Operation from 3.0 to 5.5 V

FEATURES

Line Driver Architecture

- Two DC Masks for Voltage Regulation
- Two DC Masks for Current Regulation
- Passive or Active Set Impedance Adjustment
- Double Wheatstone Bridge Architecture
- Automatic Gain Control Function

Transmit Channel

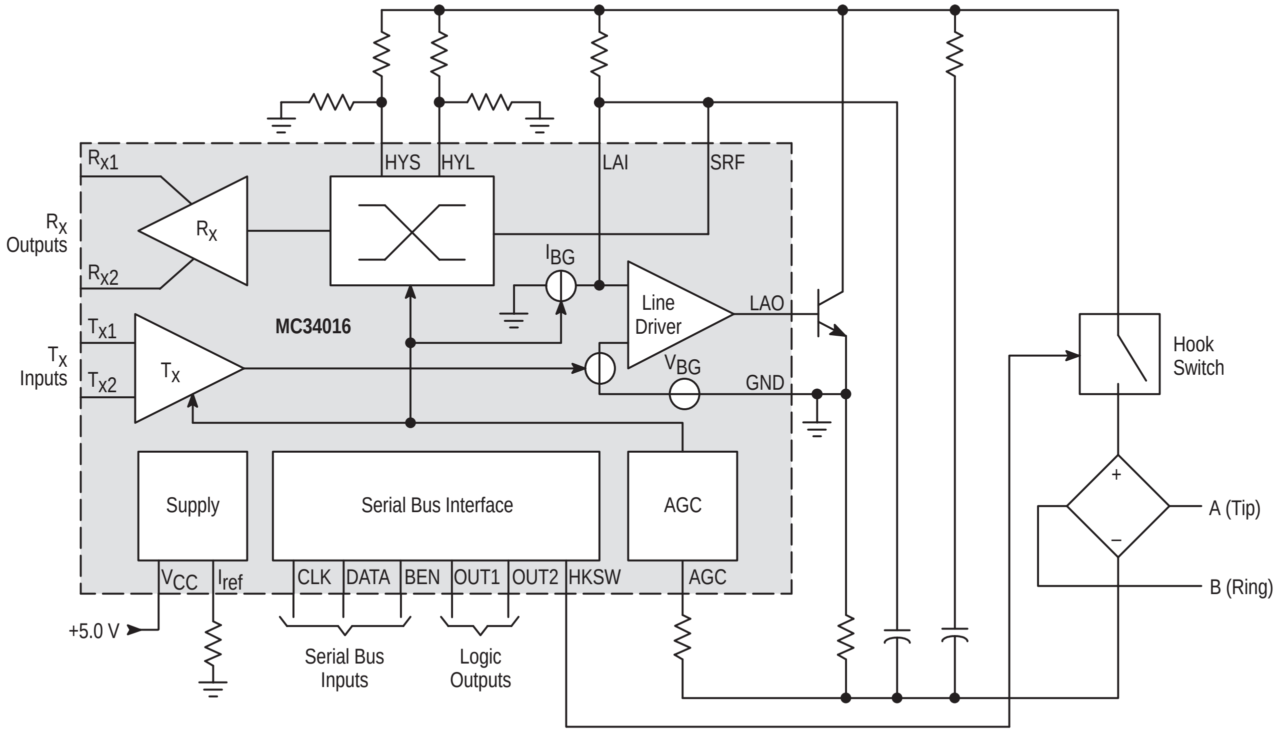
- Symmetrical Inputs Capable of Handling Large Voltage Swing
- Gain Select Option via Serial Bus Interface
- Transmit Mute Function, Programmable via Bus
- Large Voltage Swing Capability at the Telephone Line

Receive Channel

- Double Sidetone Architecture for Optimum Line Matching
- Symmetrical Outputs Capable of Producing High Voltage Swing
- Gain Select Option via Serial Bus Interface
- Receive Mute Function, Programmable via Serial Bus

Serial Bus Interface

- 3–Wire Connection to Microcontroller
- One Programmable Output Meant for Driving a Hookswitch
- Two Programmable Outputs Capable of Driving Low Ohmic Loads
- Two 8–Bit Registers for Parameter Adjustment



Programmable Telephone Line Interface Circuit with Loudspeaker Amplifier

MC34216DW

T_A = 0° to +70°C, Case 751F

The MC34216 is developed for use in telephone applications where besides the standard telephone functions also the group listening–in feature is required. In cooperation with a microcontroller, the circuit performs all basic telephone functions including DTMF generation and pulse–dialing. The listening–in part includes a loudspeaker amplifier, an anti–howling circuit and a strong supply. In combination with the TCA3385, the ringing is performed via the loudspeaker.

FEATURES

Line Driver and Supply

- DC and AC Termination of the Line
- Selectable Masks: France, U.K., Low Voltage
- Current Protection
- Adjustable Set Impedance for Resistive and Complex Termination
- Efficient Supply Point for Loudspeaker Amplifier and Peripherals

Handset Operation

- Transmit and Receive Amplifiers
- Adjustable Sidetone Network
- Line Length AGC
- Microphone and Earpiece Mute
- Earpiece Gain Increase Switch
- Microphone Squelch Function
- Transmit Amplifier Soft Clipping

Dialing and Ringing

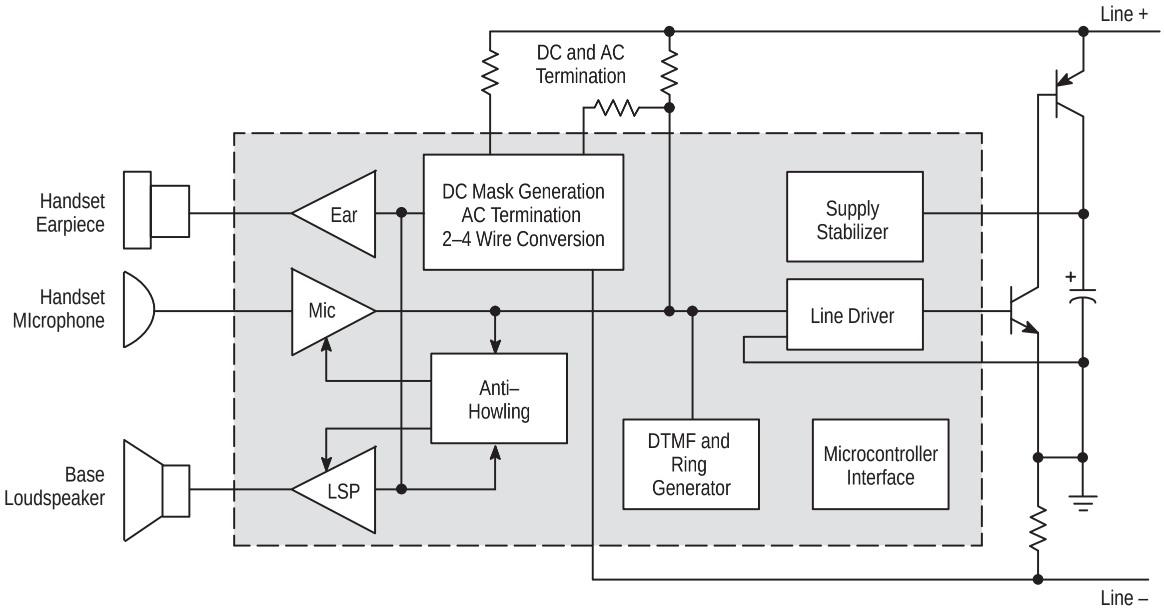
- Generates DTMF, Pilot Tones and Ring Signal
- Interrupter Driver for Pulse–Dialing
- Low Current While Pulse–Dialing
- Optimized for Ringing via Loudspeaker
- Programmable Ring Melodies
- Uses Inexpensive 500 kHz Resonator

Loudspeaking Facility

- Integrated Loudspeaker Amplifier
- Peak–to–Peak Limiter Prevents Distortion
- Programmable Volume
- Anti–Howling Circuitry for Group Listening–In
- Interfacing for Handsfree Conversation

Application Areas

- Corded Telephony with Group Listening–In
- Cordless Telephony Base Station with Group Listening–In
- Telephones with Answering Machines
- Fax, Intercom, Modem



Telephone Line Interface

TCA3388DP, FP

T_A = 0° to +70°C, Case 738, 751D

The TCA3388 is a telephone line interface circuit which performs the basic functions of a telephone set in combination with a microcontroller and a ringer. It includes dc and ac line termination, the hybrid function with 2 adjustable sidetone networks, handset connections and an efficient supply point.

FEATURES

Line Driver and Supply

- DC and AC Termination of the Telephone Line
- Selectable DC Mask: France, U.K., Low Voltage
- Current Protection
- Adjustable Set Impedance for Resistive and Complex Termination
- Efficient Supply Point for Peripherals
- Hook Status Detection

Handset Operation

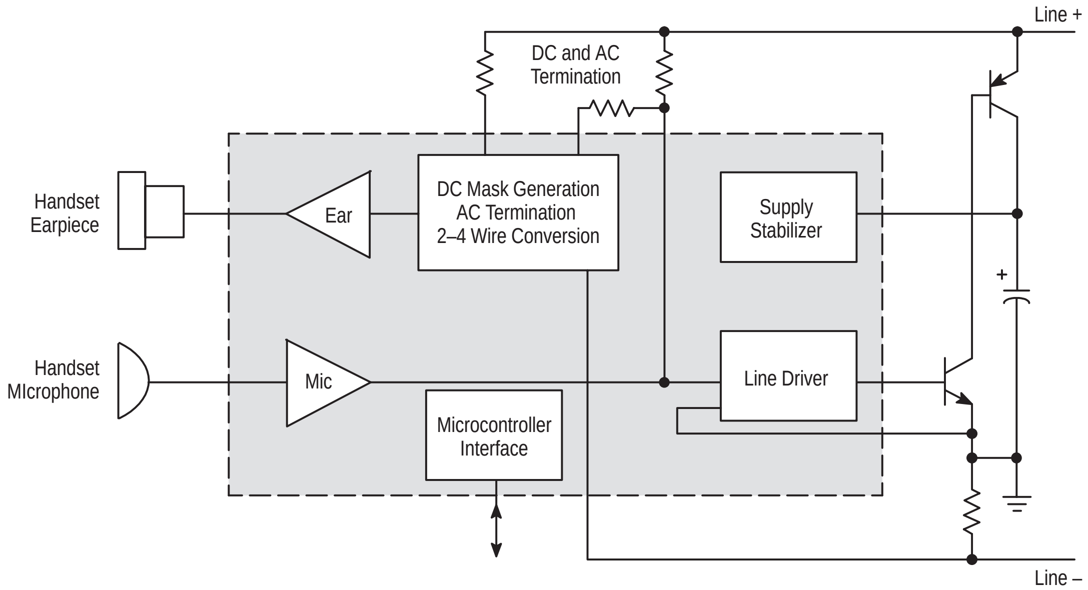
- Transmit and Receive Amplifiers
- Double Anti–Sidetone Network
- Line Length AGC
- Microphone and Earpiece Mute
- Transmit Amplifier Soft Clipping

Dialing and Ringing

- Interrupter Driver for Pulse–Dialing
- Reduced Current Consumption During Pulse–Dialing
- DTMF Interfacing
- Ringing via External Ringer

Application Areas

- Corded Telephony
- Cordless Telephony Base Station
- Answering Machines
- Fax
- Intercom
- Modem



Speakerphones

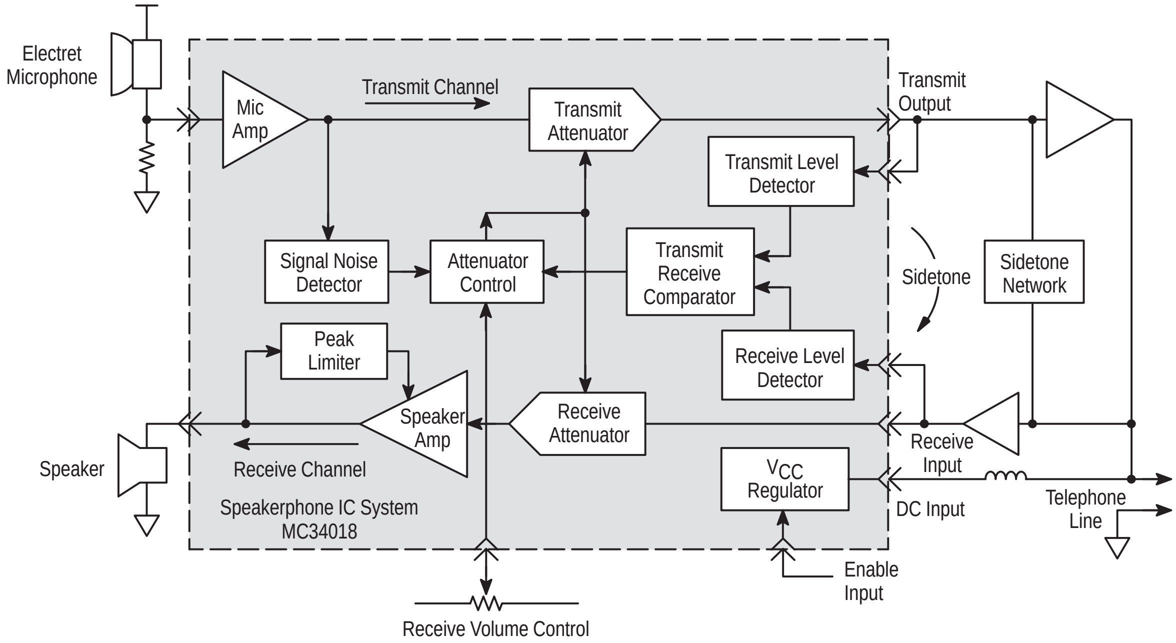
Voice Switched Speakerphone Circuit

MC34018P, DW

T_A = –20° to +60°C, Case 710, 751F

The MC34018 Speakerphone integrated circuit incorporates the necessary amplifiers, attenuators, and control functions to produce a high quality hands–free speakerphone system. Included are a microphone amplifier, a power audio amplifier for the speaker, transmit and receive attenuators, a monitoring system for background sound level, and an attenuation control system which responds to the relative transmit and receive levels as well as the background level. Also included are all necessary regulated voltages for both internal and external circuitry, allowing line–powered operation (no additional power supplies required). A Chip Select pin allows the chip to be powered down when not in use. A volume control function may be implemented with an external potentiometer. MC34018 applications include speakerphones for household and business uses, intercom systems, automotive telephones, and others.

- All Necessary Level Detection and Attenuation Controls for a Hands–Free Telephone in a Single Integrated Circuit
- Background Noise Level Monitoring with Long Time Constant
- Wide Operating Dynamic Range Through Signal Compression
- On–Chip Supply and Reference Voltage Regulation
- Typical 100 mW Output Power (into 25 Ω) with Peak Limiting to Minimize Distortion
- Chip Select Pin for Active/Standby Operation
- Linear Volume Control Function



Voice Switched Speakerphone Circuit

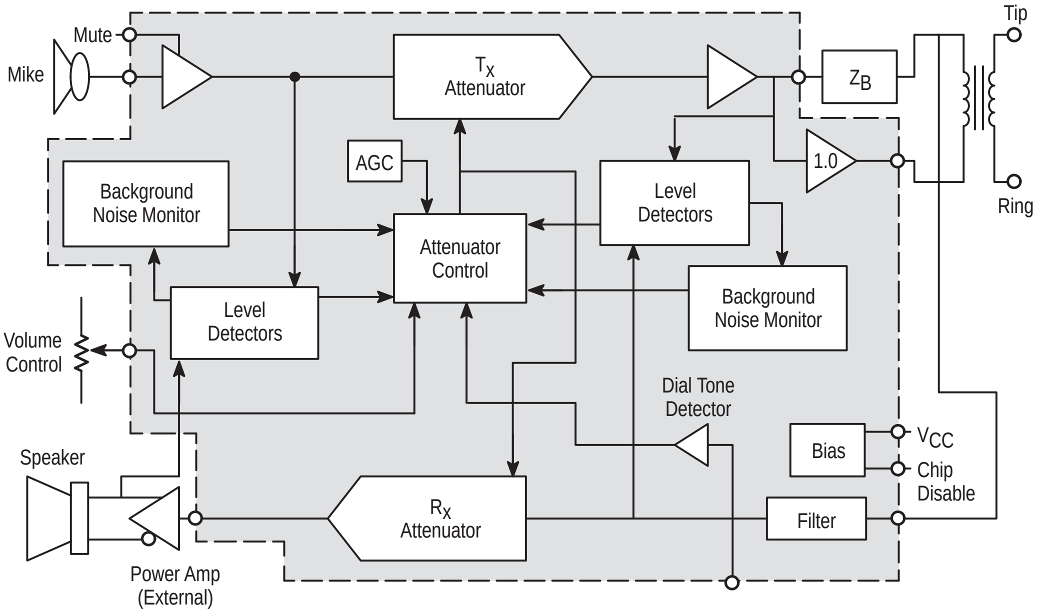
MC34118P, DW

T_A = –20° to +60°C, Case 710, 751F

The MC34118 Voice Switched Speakerphone circuit incorporates the necessary amplifiers, attenuators, level detectors, and control algorithm to form the heart of a high quality hands–free speakerphone system. Included are a microphone amplifier with adjustable gain and mute control, Transmit and Receive attenuators which operate in a complementary manner, level detectors at input and output of both attenuators,and background noise monitors for both the transmit and receive channels. A dial tone detector prevents the dial tone from being attenuated by the Receive background noise monitor circuit. Also included are two line driver amplifiers which can be used to form a hybrid network in conjunction with an external coupling transformer. A high–pass filter can be used to filter out 60 Hz noise in the receive channel, or for other filtering functions. A Chip Disable pin permits powering down the entire circuit to conserve power on long loops where loop current is at a minimum.

The MC34118 may be operated from a power supply, or it can be powered from the telephone line, requiring typically 5.0 mA. The MC34118 can be interfaced directly to Tip and Ring (through a coupling transformer) for stand–alone operation, or it can be used in conjunction with a handset speech network and/or other features of a featurephone.

- Improved Attenuator Gain Range: 52 dB Between Transmit and Receive
- Low Voltage Operation for Line–Powered Applications (3.0 to 6.5 V)
- 4–Point Signal Sensing for Improved Sensitivity
- Background Noise Monitors for Both Transmit and Receive Paths
- Microphone Amplifier Gain Set by External Resistors – Mute Function Included
- Chip Disable for Active/Standby Operation
- On Board Filter Pinned–Out for User Defined Function
- Dial Tone Detector Inhibits Receive Idle Mode During Dial Tone Presence
- Compatible with MC34119 Speaker Amplifier



Voice Switched Speakerphone with µProcessor Interface

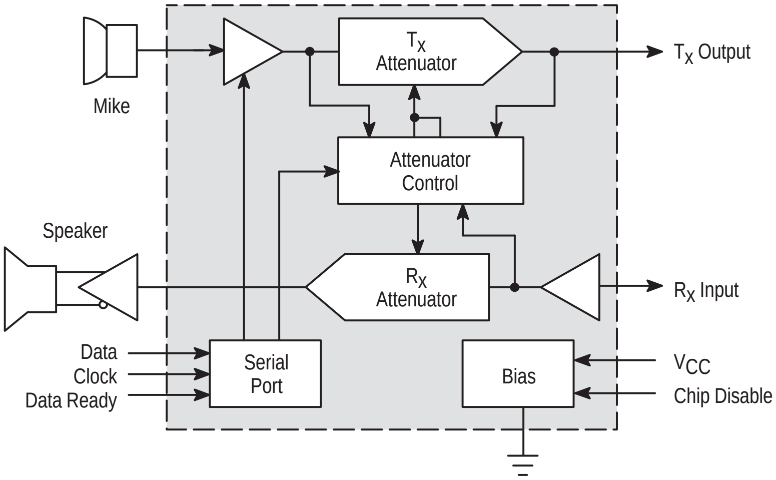
MC33218AP, DW

T_A = –40° to +85°C, Case 724, 751E

The MC33218A, Voice Switched Speakerphone circuit incorporates the necessary amplifiers, attenuators, level detectors, and control algorithm to form the heart of a high quality hands–free speakerphone system. Included are a microphone amplifier with adjustable gain, and mute control, transmit and receive attenuators which operate in a complementary manner, and level detectors and background noise monitors for both paths. A dial tone detector prevents dial tone from being attenuated by the receive background noise monitor. A Chip Disable pin permits powering down the entire circuit to conserve power.

Also included is an 8–bit serial µprocessor port for controlling the receive volume, microphone mute, attenuator gain, and operation mode (force to transmit, force to receive, etc.). Data rate can be up to 1.0 MHz. The MC33218A can be operated from a power supply, or from the telephone line, requiring typically 3.8 mA. It can also be used in intercoms and other voice–activated applications.

- Low Voltage Operation: 2.5 to 6.0 V
- 2–Point Sensing, Background Noise Monitor in Each Path
- Chip Disable Pin for Active/Standby Operation
- Microphone Amplifier Gain Set by External Resistors – Mute Function Included
- Dial Tone Detector to Inhibit Receive Idle Mode During Dial Tone Presence
- Microprocessor port for controlling:
  - Receive Volume Level (16 Steps)
  - Attenuator Range (26 or 52 dB, Selectable)
  - Microphone Mute
  - Force to Transmit, Receive, Idle or Normal Voice Switched Operation
- Compatible with MC34119 Speaker Amplifier



Voice Switched Speakerphone Circuit

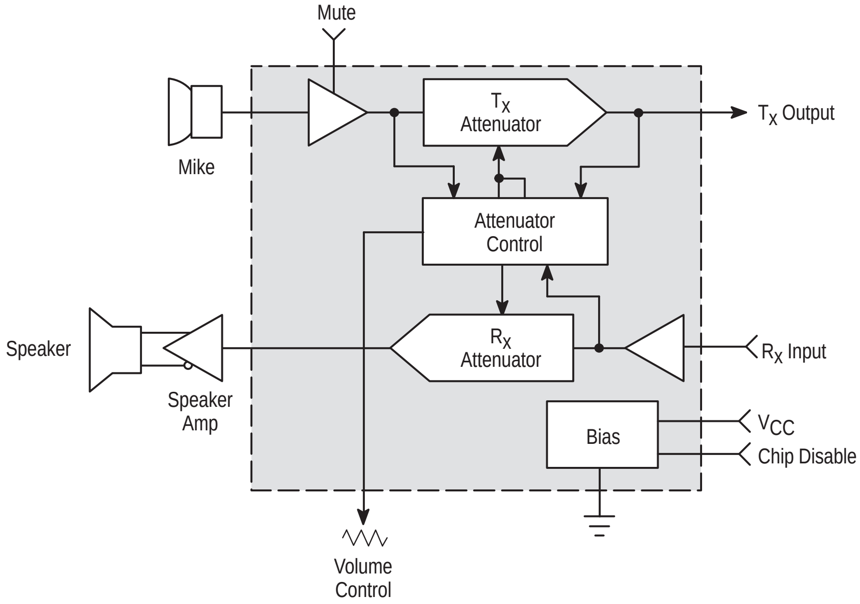
MC33219AP, ADW

T_A = –40° to +85°C, Case 724, 751E

The MC33219A Voice Switched Speakerphone Circuit incorporates the necessary amplifiers, attenuators, level detectors, and control algorithm to form the heart of a high quality hands–free speakerphone system. Included are a microphone amplifier with adjustable gain, and mute control, transmit and receive attenuators which operate in a complementary manner, and level detectors and background noise monitors. A dial tone detector prevents dial tone from being attenuated by the receive background noise monitor. A Chip Disable pin permits powering down the entire circuit to conserve power.

The MC33219A may be operated from a power supply, or it can be powered from the telephone line requiring typically 4.0 mA. The MC33219A can be interfaced directly to Tip and Ring (through a coupling transformer for stand–alone operation, or it can be used in conjuction with a handset speech network and/or other features of a featurephone.

- Low Voltage Operation: 2.7 to 6.0 V
- 2–Point Sensing, Background Noise Monitor in Each Path
- Chip Disable Pin for Active/Standby Operation
- Microphone Amplifier Gain Set by External Resistors – Mute Function Included
- Dial Tone Detector to Inhibit Receive Idle Mode During Dial Tone Presence
- Volume Control Range: 34 dB
- Compatible with MC34119 Speaker Amplifier



Telephone Line Interface and Speakerphone Circuit

MC33215B, FB

T_A = 0° to +70°C, Case 858, 848B

The MC33215 is a combination speech network/ speakerphone developed for use in fully electronic telephone sets with a speakerphone function. The circuit performs the ac and dc line terminations, 2–4 wire conversion, line length AGC and DTMF transmission. The speakerphone part includes a half duplex controller with signal and noise monitoring, base microphone and loudspeaker amplifiers, and an efficient supply. The circuit is designed to operate at low line currents down to 4.0 mA enabling parallel operation with a classical telephone set.

FEATURES

Line Driver and Supply

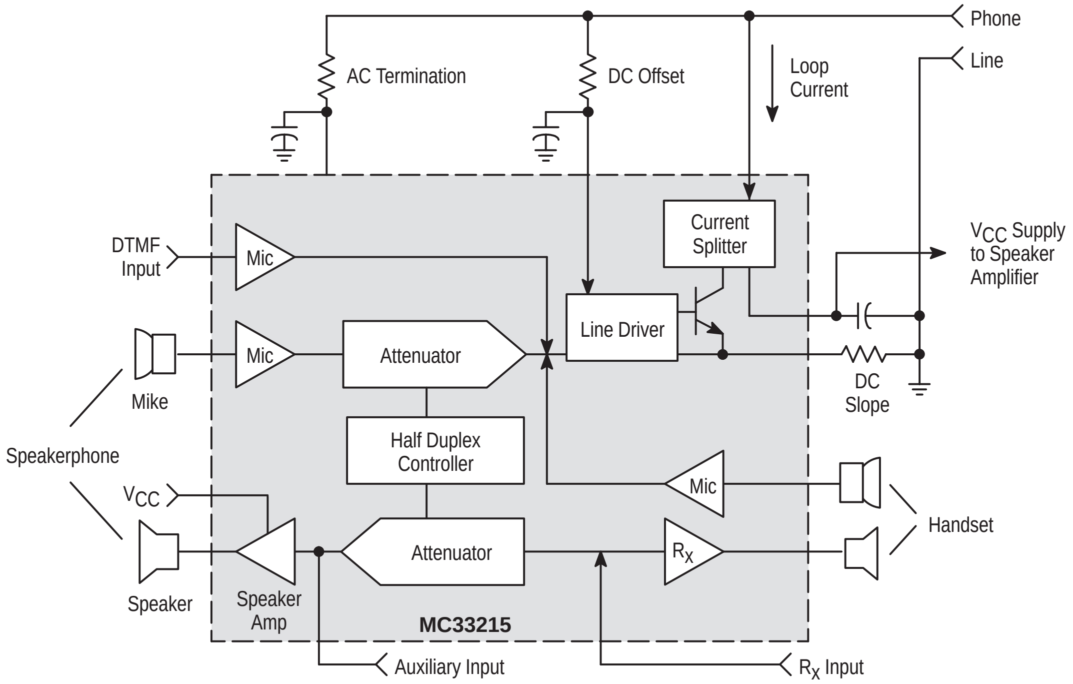
- AC and DC Termination of Telephone Line
- Adjustable Set Impedance for Real and Complex Termination
- Efficient Supply for Speaker Amplifier and Peripherals
- Two Supplies for Handset and Base Microphones
- Separate Supply Arrangement for Handset and Speakerphone Operation

Handset Operation

- Transmit and Receive Amplifiers
- Differential Microphone Inputs
- Sidetone Cancellation Network
- Line Length AGC
- Microphone and Earpiece Mute
- Separate Input for DTMF and Auxiliary Signals
- Parallel Operation Down to 4.0 mA of Line Current

Speakerphone Operation

- Integrated Microphone and Loudspeaker Amplifiers
- Differential Microphone Inputs
- Loudspeaker Amplifier can be Powered and Used Separately from the Rest of the Circuit
- Integrated Switches for Smooth Switch Over from Handset to Speakerphone Mode
- Signal and Background Noise Monitoring in Both Channels
- Adjustable Switching Depth for Handsfree Operation
- Adjustable Switch Over and Idle Mode Timing
- Dial Tone Detector in the Receive Channel
- Handsfree Operation via Loudspeaker and Base Microphone



Speakerphones (continued)

Table 10. The Motorola Family of Speakerphone Integrated Circuits

MC34018	MC34118	MC33218A	MC33219A
Two point sensing with slow idle, background noise monitor in T_X path only	Four point sensing with both fast and slow idle modes, background noise monitors in both R_X and T_X paths	Two point sensing with slow idle, background noise monitors in both R_X and T_X paths	Two point sensing with slow idle, background noise monitors in both R_X and T_X paths
No dial tone detector in receive path	Receive path has dial tone detector	Receive path has dial tone detector	Receive path has dial tone detector
Attenuator Characteristics: • Range: 44 dB • Tolerance: ±4.0 dB • Gain tracking not specified • White noise is constant	Attenuator Characteristics: • Range: 52 dB • Tolerance: ±2.0 dB • Gain Tracking: <1.0 dB • White noise reduces with volume	Attenuator Characteristics: • Range: 52 or 26 dB (selectable) • Tolerance: ±3.0 dB • Gain Tracking: <1.0 dB • White noise reduces with volume	Attenuator Characteristics: • Range: 52 dB • Tolerance: ±3.0 dB • Gain Tracking: <1.0 dB • White noise reduces with volume
External hybrid required	Hybrid amplifiers on board	External hybrid required	External hybrid required
Speaker amplifier is on board (34 dB, 100 mW)	External speaker amplifier required (MC34119)	External speaker amplifier required (MC34119)	External speaker amplifier required (MC34119)
Filtering is external	Configurable filter on board	Filtering is external	Filtering is external
Microphone amplifier has fixed gain and no muting	Microphone amplifier has adjustable gain and mute input	Microphone amplifier has adjustable gain, and can be muted through µP port	Microphone amplifier has adjustable gain and a mute input
Supply Voltage: 4.0 V to 11 V	Supply Voltage: 2.8 V to 6.5 V	Supply Voltage: 2.5 V to 6.5 V	Supply Voltage: 2.7 V to 6.5 V
Supply Current: 6.5 mA typ., 9.0 mA max	Supply Current: 5.5 mA typ., 8.0 mA max	Supply Current: 4.0 mA typ., 5.0 mA max	Supply Current: 3.0 mA typ., 5.0 mA max
Speaker amplifier reduces gain to prevent clipping	Receive gain is reduced as supply voltage falls to prevent clipping	Receive gain is reduced as supply voltage falls to prevent clipping	Receive gain is reduced as supply voltage falls to prevent clipping
Volume control is linear. Cannot override voice switched operation except through additional circuitry. Attenuator gain is fixed at 44 dB (slightly variable). No microphone mute.	Volume control is linear, and microphone mute has separate pin. Cannot override voice switched operation except through additional circuitry. Attenuator gain is fixed at 52 dB.	8–bit µP serial port controls: • Volume control (16 steps) • Microphone mute • Range selection (26 dB or 52 dB) • Force to transmit, idle, receive, or normal voice switched operation	Volume control is linear, and microphone mute has separate pin. Attenuator range fixed at 52 dB. Cannot override voice switched operation except through additional circuitry.
28 Pin DIP and SOIC packages	28 Pin DIP and SOIC packages	24 Pin narrow DIP and SOIC packages	24 Pin narrow DIP and SOIC packages
External Required: • 12 Resistors • 11 Capacitors (≤1.0 µF) • 8 Capacitors (>1.0 µF)	External Required: • 14 Resistors • 12 Capacitors (≤1.0 µF) • 9 Capacitors (>1.0 µF)	External Required: • 12 Resistors • 11 Capacitors (≤1.0 µF) • 4 Capacitors (>1.0 µF)	External Required: • 12 Resistors • 11 Capacitors (≤1.0 µF) • 4 Capacitors (>1.0 µF)
Temperature Range: –20° to +60°C	Temperature Range: –20° to +60°C	Temperature Range: –40° to +85°C	Temperature Range: –40° to +85°C

Telephone Accessory Circuits

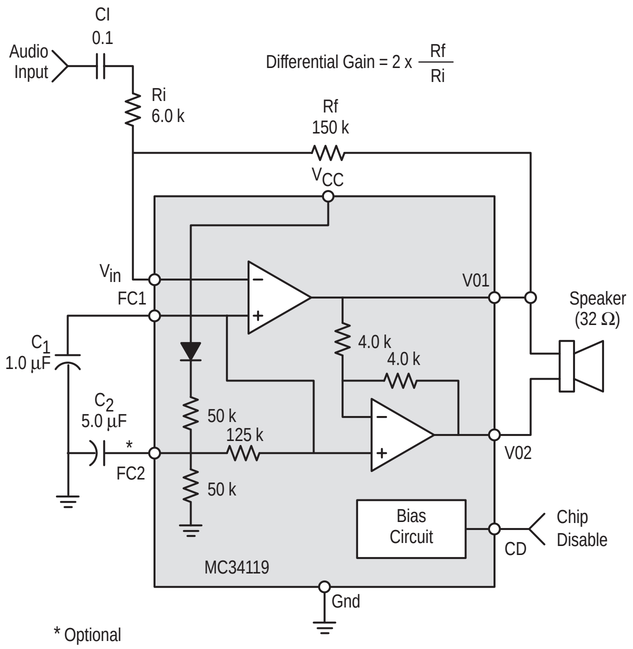
Audio Amplifier

MC34119P, D

T_A = 0° to +70°C, Case 626, 751

A low power audio amplifier circuit intended (primarily) for telephone applications, such as speakerphones. Provides differential speaker outputs to maximize output swing at low supply voltages (2.0 V min.). Coupling capacitors to the speaker, and snubbers, are not required. Overall gain is externally adjustable from 0 to 46 dB. A Chip Disable pin permits powering–down to mute the audio signal and reduce power consumption.

- Drives a Wide Range of Speaker Loads (16 to 100 Ω)
- Output Power Exceeds 250 mW with 32 Ω Speaker
- Low Distortion (THD = 0.4% Typical)
- Wide Operating Supply Voltage (2.0 V to 16 V) – Allows Telephone Line Powered Applications.
- Low Quiescent Supply Current (2.5 mA Typical)
- Low Power–Down Quiescent Current (60 µA Typical)



Current Mode Switching Regulator

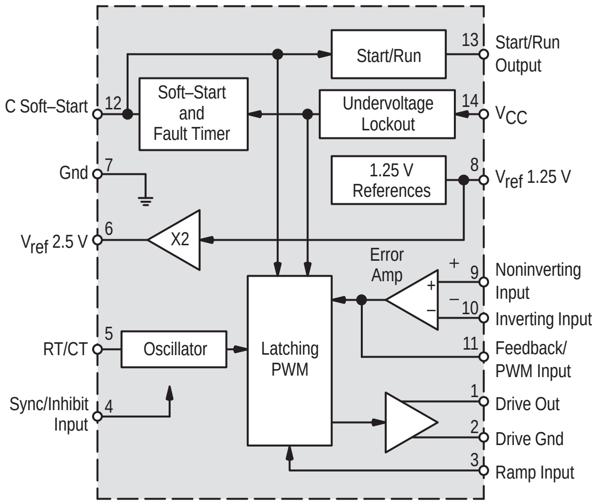
MC34129P, D

T_A = 0° to +70°C, Case 646, 751A

High performance current mode switching regulator for low–power digital telephones. Unique internal fault timer provides automatic restart for overload recovery. A start/run comparator is included to implement bootstrapped operation of V_{CC}.

Although primarily intended for digital telephone systems, these devices can be used cost effectively in many other applications. On–chip functions and features include:

- Current Mode Operation to 300 kHz
- Automatic Feed Forward Compensation
- Latching PWM for Cycle–By–Cycle Current Limiting
- Latched–Off or Continuous Retry after Fault Timeout
- Soft–Start with Maximum Peak Switch Current Clamp
- Internally Trimmed 2% Bandgap Reference
- Input Undervoltage Lockout



300 Baud FSK Modems

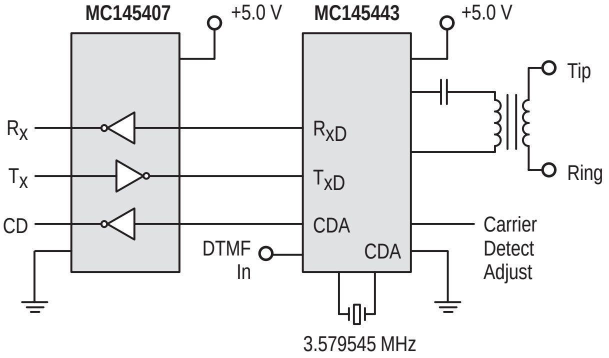
MC145442P, DW Modem – CCITT V.21
Case 738, 751D

MC145443P, DW Modem – Bell 103
Case 738, 751D

This powerful modem combines a complete FSK modulator/demodulator and an accompanying transmit/receive filter system on a single silicon chip. Designed for bidirectional transmission over the telephone network, the modem operates at 300 baud and can be obtained for compatibility with CCITT V.21 and Bell 103 specifications.

The modem contains an on–board carrier–detect circuit that allows direct operation on a telephone line (through a simple transformer), providing simplex, half–duplex, and full–duplex data communications. A built–in power amplifier is capable of driving –9.0 dBm onto a 600 Ω line in the transmit mode.

CMOS processing keeps power dissipation to a very low 45 mW, with a power–down dissipation of only 1.0 mW . . . from a single 5.0 V power supply. Available in a 20 pin dual–in–line P suffix, and a wide body surface mount DW suffix.



MC145444H, DW – CCITT V.21
Case 804, 751D

MC145446AFW – CCITT V.21
Case 751M

This device includes the DTMF generator and call progress tone detector (CPTD) as well as the other circuitry needed for full–duplex, half–duplex, or simplex 300 baud data communication over a pair of telephone lines. It is intended for use with telemeter system or remote control system applications.

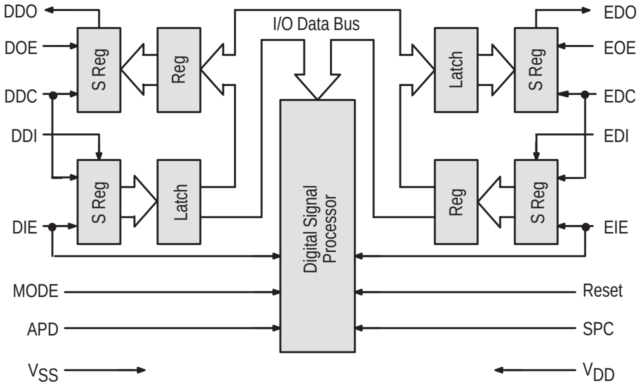
The differential line driver is capable of driving 0 dBm into a 600 Ω load. The transmit attenuator is programmable in 1.0 dB steps.

ADPCM Transcoder

MC145532DW, L
Case 751G, 620

The MC145532 Adaptive Differential Pulse Code Modulation (ADPCM) Transcoder provides a low cost, full–duplex, single–channel transcoder to (from) a 64 kbps PCM channel from (to) either a 16 kbps, 24 kbps, 32 kbps, or 64 kbps channel.

- Complies with CCITT Recommendation G.721 (1988)
- Complies with the American National Standard (T1.301–1987)
- Full–Duplex, Single–Channel Operation
- Mu–Law or A–Law Coding is Pin Selectable
- Synchronous or Asynchronous Operation
- Easily Interfaces with any Member of Motorola’s PCM Codec–Filter Mono–Circuit Family or Other Industry Standard Codecs
- Serial PCM and ADPCM Data Transfer Rate from 64 kbps to 5.12 Mbps
- Power Down Capability for Low Cost Consumption
- The Reset State is Automatically Initiated when the Reset Pin is Released.
- Simple Time Slot Assignment Timing for Transcoder Applications
- Single 5.0 V Power Supply
- Evaluation Kit MC145536 EVK Supports the MC145532 as well as the MC14LC5480 PCM Codec–Filter. (See PBX Architecture Pages for More Information.)



Calling Line Identification (CLID) Receiver with Ring Detector

MC14LC5447P, DW

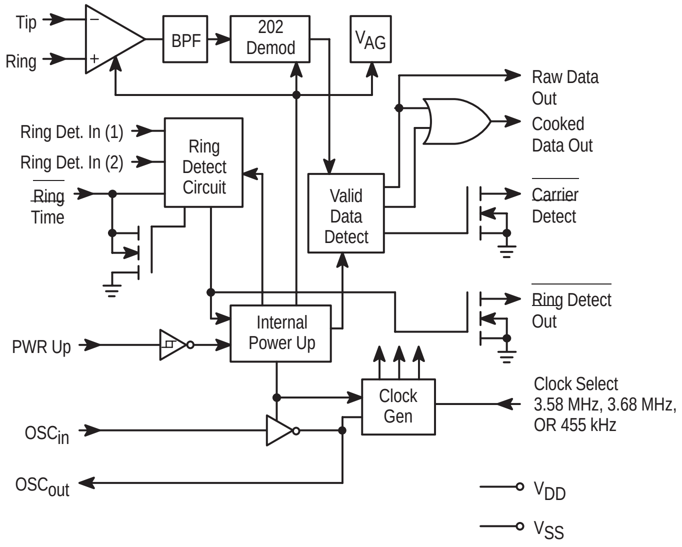
Case 648, 751G

The MC14LC5447 is designed to demodulate Bell 202 1200 baud FSK asynchronous data. Its primary application is in products that will be used to receive and display the calling number, or the message waiting indicator sent to subscribers from participating central office facilities of the public switched telephone network. The device also contains a carrier detect circuit and telephone ring detector which may be used to power up the device.

Applications include adjunct boxes, answering machines, feature phones, fax machines, and computer interface products.

Replaces MC145447P, DW.

- Ring Detector On–Chip
- Ring Detect Output for MCU Interrupt
- Power–Down Mode Less Than 1.0 µA
- Single Supply: 3.5 V to 6.0 V
- Pin Selectable Clock Frequencies: 3.68 MHz, 3.58 MHz, or 455 kHz
- Two–Stage Power–Up for Power Management Control

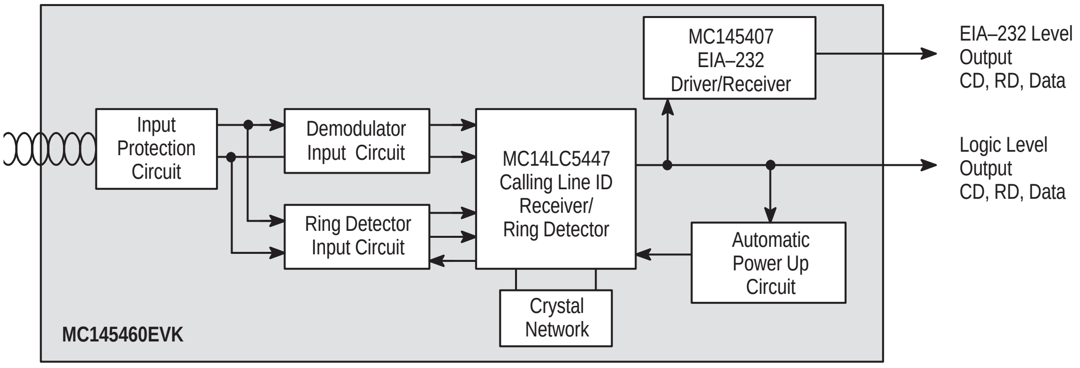


Calling Line ID Receiver Evaluation Kit

MC145460EVK

The MC145460EVK is a low cost evaluation platform for the MC14LC5447. The MC145460EVK facilitates development and testing of products that support the Bellcore customer premises equipment (CPE) data interface, which enables services such as Calling Number Delivery (CND). The MC14LC5447 can be easily incorporated into any telephone, FAX, PBX, key system, answering machine, CND adjunct box or other telephone equipment with the help of the MC145460EVK development kit.

- Easy Clip–On Access to Key MC14LC5447 Signals
- Generous Prototype Area
- Configurable for MC14LC5447 Automatic or External Power Up Control
- EIA–232 and Logic Level Ports for Connection to any PC or MCU Development Platform
- Carrier Detect, Ring Detect and Data Status LEDs
- Optional Tip and Ring Input Protection Network
- MC145460EVK User Guide, MC14LC5447 Data Sheet, and Additional MC14LC5447 Sample Included



Continuously Variable Slope Delta (CVSD) Modulator/Demodulator

MC34115P, DW
T_A = 0° to +70°C, Case 648, 751G

MC3418P, DW
T_A = 0° to +70°C, Case 648, 751G

Provides the A/D–D/A function of voice communications by digital transmission. Designed for speech synthesis and commercial telephone applications. A single IC provides both encoding and decoding.

- Encode and Decode Functions on the Same Chip with a Digital Input
- CMOS Compatible Digital Output
- Digital Input Threshold Selectable (V_{CC}/2 reference provided on Chip)
- MC34115 Has a 3–Bit Algorithm (General Communications)
- MC3418 Has a 4–Bit Algorithm (Commercial Telephone)

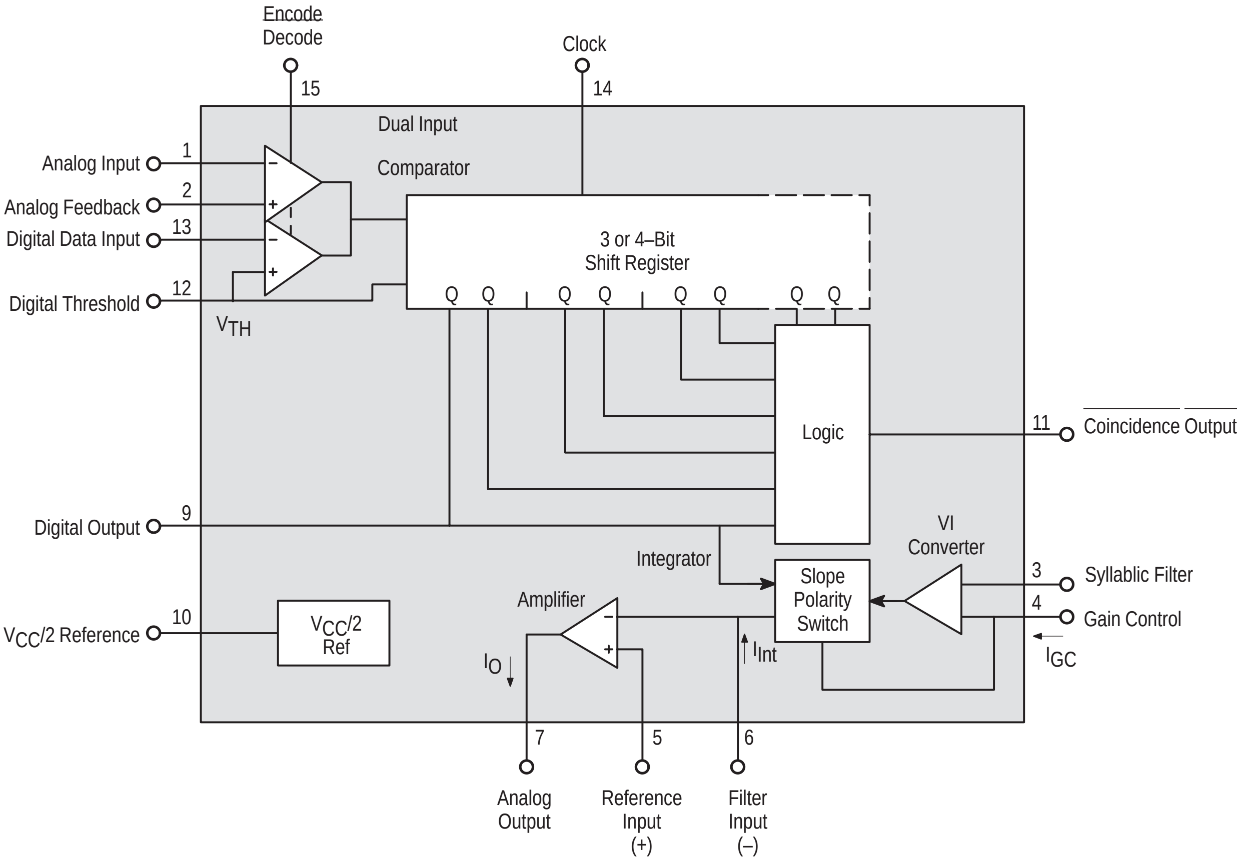


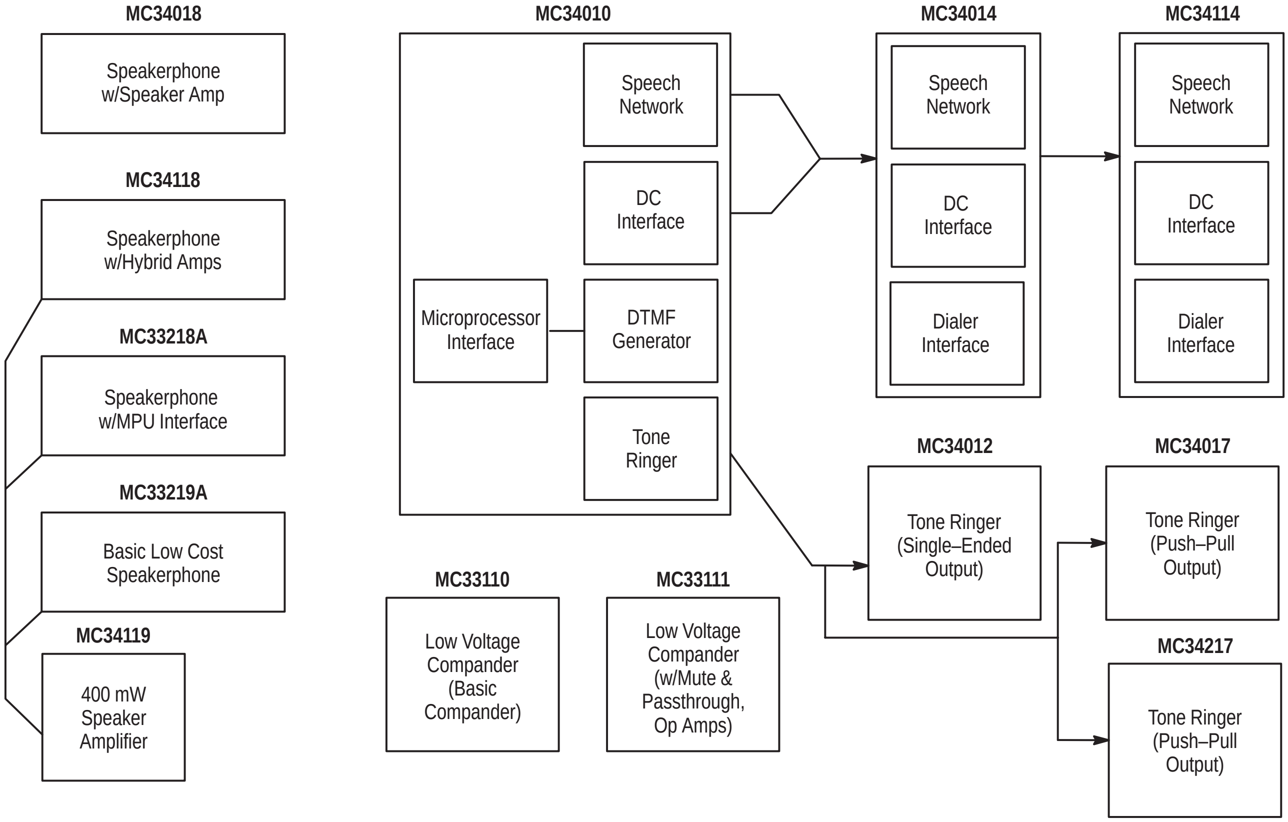
Table 11. Summary of Bipolar Telecommunication Circuits

Function	Features	Suffix/ Package	Device
Subscriber Loop Interface Circuits (SLICs)			
Central Office, Remote Terminals, PBX Applications	All gains externally programmable, most BORSHT functions, current limit adjustable to 50 mA, 58 dB Longitudinal Balance, –21.6 V to –42 V.	P/738, FN/776	MC33121
Central Office, Remote Terminals, PBX Applications	All gains externally programmable, most BORSHT functions, current limit adjustable to 50 mA, 58 dB Longitudinal Balance, –42 V to –58 V.	P/738, FN/776	MC33120
Complete Telephone Circuit			
POTS Circuit + MPU Dialing	Speech network, tone ringer, dc loop current interface, DTMF dialer with serial port control.	P/711, FN/777	MC34010
Tone Ringers			
Adjustable Tone Ringer	Single–ended output, meets FCC requirements, adjustable REN, different warble rates.	P/626, D/751	MC34012–1, 2, 3
Adjustable Tone Ringer	Differential output, meets FCC requirements, adjustable REN, different warble rates.	P/626, D/751	MC34017–1, 2, 3
Adjustable Tone Ringer	Differential output, meets FCC requirements, adjustable REN, single warble rates.	P/626, D/751	MC34217
Ring Signal Converter	Switching regulator to convert ringing voltage to regulated dc output. Provides ring detect output.	DP/626, FP/751	TCA3385
Speech Networks			
Speech Network + Speakerphone	Line powered IC provides handset and speakerphone modes, dialer interface, ac/dc terminations, and AGC. Efficient supply design provides 90% of loop current to the speaker amplifier. Speaker amplifier may be used independently. Handset operation to 4.0 mA.	B/858, FB/848B	MC33215
Basic Phone Line Interface	Loop current interface, speech network, line length compensation, speech/dialing modes, Bell System compliant.	P/707, DW/751D	MC34014
Cordless Universal Telephone Interface	For cordless telephone base for CT0, CT1, CT2 and DECT. European dc masks, double wheatstone bridge sidetone circuit. SPI port for masks, AGC hookswitch, mute and gain settings. Requires 5.0 V and µP.	P/738, DW/751D	MC34016
Basic Phone Line Interface	Loop current interface, speech network, line length compensation, speech/dialing modes, Bell System and foreign countries.	P/707, DW/751D	MC34114
Programmable Telephone Line Interface Circuit with Loudspeaker Amplifier	Group listening–in, DTMF and tones generator, ring generator, country programmable, SPI interface.	DW/751F	MC34216
European Speech Network, Programmable Speaker Amplifier	Line powered. European dc masks, DTMF and pilot tone generator, listening–in mode with anti–howling. 2–wire bus control masks, DTMF tones, speaker gain, pulse dialing, mute, AGC. Requires MCU.	DW/751	MC34216A
European Speech Network	Loop current interface, speech network, line length compensation, speech/dialing modes, programmable masks for French, U.K., low voltage and PABX systems.	DP/738, FP/751	TCA3388

Summary of Bipolar Telecommunications Circuits (continued)

Function	Features	Suffix/ Package	Device
Speakerphone Circuits			
Speech Network + Speakerphone	Line powered IC provides handset and speakerphone modes, dialer interface, ac/dc terminations, and AGC. Efficient supply design provides 90% of loop current to the speaker amplifier. Speaker amplifier may be used independently. Handset operation to 4.0 mA.	B/858, FB/848B	MC33215
Complete Speaker Phone with Speaker Amplifier	All level detection (2 pt.), attenuators, and switching controls, mike and speaker amp.	P/710, DW/751F	MC34018
Complete Speaker Phone with Hybrid, Filter	All level detection (4 pt.), attenuators, and switching controls, mike amp with mute, hybrid, and filter.	P/710, DW/751F	MC34118
Complete Speaker Phone with MPU Interface	All level detection, attenuators, and switching controls, mike amp, MPU interface for: volume control, mode selection, mike mute.	P/724, DW/751E	MC33218A
Basic Low Cost Speakerphone	All level detection, attenuators and switching controls, Mike amplifier with Mute, low voltage operation.	P/724, DW/751E	MC33219A
Audio Amplifiers			
1 Watt Audio Amp	1.0 W output power into 16 Ω, 35 V maximum.	D/751	MC13060
Low Voltage Audio Amp	400 mW, 8.0 to 100 Ω, 2.0 to 16 V, differential outputs, chip–disable input pin.	P/626, D/751	MC34119
Companders			
Basic Compander	2.1 V to 7.0 V, no precision externals, 80 dB range, –40° to +85°C, independent compressor and expander.	P/646, D/751A	MC33110
Compander with Features	3.0 V to 7.0 V, no precision externals, 80 dB range, –40° to +85°C, independent compressor and expander, pass through and mute functions, two op amps.	P/648, D/751B	MC33111
Switching Regulator			
Current Mode Regulator	For phone line power applications, soft–start, current limiting, 2% accuracy.	P/646, D/751A	MC34129
Voice Encoder/Decoders			
Continuously Variable Slope Modulator/Demodulator (CVSD)	Telephone quality voice encoding/decoding, variable clock rate, 3–bit coding, for secure communications, voice storage/retrieval, answering machines, 0° to 70°C.	P/738, DW/751G	MC34115
	Same as above except 4–bit coding.	P/738, DW751G	MC3418

Figure 3. The Motorola Family of Handset Telecom Integrated Circuits



Phase–Locked Loop Components

Motorola offers a choice of phase–locked loop components ranging from complete functional frequency synthesizers for dedicated applications to a wide selection of general purpose PLL circuit elements. Technologies include CMOS for lowest power consumption and bipolar for high speed operation. Typical applications include TV, CATV, radios, scanners, cordless telephones plus home and personal computers.

Table 12. PLL Frequency Synthesizers

Frequency (MHz)	Supply Voltage (V)	Nominal Supply Current (mA)	Phase Detector	Standby	Interface	Device	Suffix/ Case
4.0 @ 5.0 V	4.5 to 12	6.0 @ 5.0 V	Single–ended 3–state	No	Parallel	MC145106	P/707, DW/751D
15 @ 5.0 V	3.0 to 9.0	–	Two single–ended 3–state		Serial	MC145149*	P/738, DW/751D
		7.5 @ 5.0 V	Analog			MC145159–1	P/738, DW/751D
20 @ 5.0 V	3.0 to 9.0	7.5 @ 5.0 V	Single–ended 3–state, double–ended		4–Bit	MC145145–2	P/707, DW/751D
						MC145146–2	P/738, DW/751D
					Parallel	MC145151–2	P/710, DW/751F
			Double–ended			MC145152–2	P/710, DW/751F
			Single–ended 3–state, double–ended		Serial	MC145155–2	P/707, DW/751D
						MC145156–2	P/707, DW/751D
						MC145157–2	P/648, DW/751G
						MC145158–2	P/648, DW/751G
60 @ 3.0 V	2.5 to 5.5	3.0 @ 3.0 V	Two single–ended 3–state	Yes		MC145162*	P/648, DW/751G
60 @ 2.0 V	1.8 to 3.6	1.5 @ 1.8 V				MC145165*	P/648, D/751B
60 @ 3.0 V	2.5 to 5.5	3.0 @ 3.0 V			Parallel	MC145166*	P/648, DW/751G
					Serial	MC145167*	P/648, DW/751G
					Parallel	MC145168*	
					Serial	MC145169*	
85 @ 3.0 V	2.5 to 5.5	3.0 @ 3.0 V				MC145162–1*	P/648, DW/751G
40/130 @ 5.0 V	4.5 to 5.5	9.0 @ 5.0 V	Single–ended 3–state, Current source/sink			MC145173	DW/751E
100 @ 3.0 V 185 @ 5.0 V	2.5 to 5.5	2.0 @ 3.0 V 6.0 @ 5.0 V		No		MC145170–1	P/648, D/751B

* Dual PLL

Phase–Locked Loop Components (continued)

PLL Frequency Synthesizers (continued)

Frequency (MHz)	Supply Voltage (V)	Nominal Supply Current (mA)	Phase Detector	Standby	Interface	Device	Suffix/ Case
1100 @ 5.0 V	4.5 to 5.5	7.0 @ 5.0 V	Current source/sink, double–ended	Yes	Serial	MC145190	F/751J, DT/948D
						MC145191	F/751J, DT/948D
1100 @ 3.0 V	2.7 to 5.0	6.0 @ 2.7 V				MC145192	F/751J, DT/948D
1100 @ 3.0 V	2.7 to 5.5	12	Two current source/sink, double–ended			MC145220*	F/803C, DT/948D
2000 @ 5.0 V	4.5 to 5.5	12 @ 5.0 V	Current source/sink, double–ended			MC145200	F/751J, DT/948D
2000 @ 5.0 V	4.5 to 5.5	12 @ 5.0 V				MC145201	F/751J, DT/948D
2000 @ 3.0 V	2.7 to 5.5	4.0 @ 3.0 V				MC145202	F/751J, DT/948D
1100 @ 3.0 V	2.7 to 5.5	12	Two current source/sink, double–ended			MC145220*	F/803C, DT/948D

* Dual PLL

Table 13. Phase–Locked Loop Functions

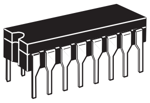
Device	Function	Pins	DIP	SM
MC4016	Programmable Modulo–N Counters (N=0–9)	16	P,L	
MC4018	Programmable Modulo–N Counters (N=0–9)	16	P,L	
MC4024	Dual Voltage–Controlled Multivibrator	14	P,L	
MC4044	Phase–Frequency Detector	14	P,L	D
MC4316	Programmable Modulo–N Counters (N=0–9)	16	P,L	
MC4324	Dual Voltage–Controlled Multivibrator	14	P,L	
MC4344	Phase–Frequency Detector	14	P,L	
MC12002	Analog Mixer	14	P,L	
MC12009	480 MHz ÷5/6 Dual Modulus Prescaler	16	P,L	
MC12011	550 MHz ÷8/9 Dual Modulus Prescaler	16	P,L	
MC12013	550 MHz ÷10/11 Dual Modulus Prescaler	16	P,L	
MC12014	Counter Control Logic	16	P,L	
MC12015	225 MHz ÷32/33 Dual Modulus Prescaler	8	P,L	D
MC12016	225 MHz ÷40/41 Dual Modulus Prescaler	8	P,L	D
MC12017	225 MHz ÷64/65 Dual Modulus Prescaler	8	P,L	D
MC12018	520 MHz ÷128/129 Dual Modulus Prescaler	8	P,L	D
MC12019	225 MHz ÷20/21 Dual Modulus Prescaler	8	P,L	D
MC12022A	1.1 GHz ÷64/65, ÷128/129 Dual Modulus Prescaler	8	P	D
MC12022B	1.1 GHz ÷64/65, ÷128/129 Dual Modulus Prescaler	8	P	D

Phase–Locked Loop Components (continued)

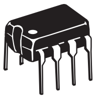
Phase–Locked Loop Functions (continued)

Device	Function	Pins	DIP	SM
MC12022LVA	1.1 GHz ÷64/65, ÷128/129 Low Voltage Dual Modulus Prescaler	8	P	D
MC12022LVB	1.1 GHz ÷64/65, ÷128/129 Low Voltage Dual Modulus Prescaler	8	P	D
MC12022SLA	1.1 GHz ÷64/65, ÷128/129 Dual Modulus Prescaler	8	P	D
MC12022SLB	1.1 GHz ÷64/65, ÷128/129 Dual Modulus Prescaler	8	P	D
MC12022TSA	1.1 GHz ÷64/65, ÷128/129 Dual Modulus Prescaler	8	P	D
MC12022TSB	1.1 GHz ÷64/65, ÷128/129 Dual Modulus Prescaler	8	P	D
MC12022TVA	1.1 GHz ÷64/65, ÷128/129 Low Voltage Dual Modulus Prescaler	8	P	D
MC12022TVB	1.1 GHz ÷64/65, ÷128/129 Low Voltage Dual Modulus Prescaler	8	P	D
MC12023	225 MHz ÷64 Prescaler	8	P	D
MC12025	520 MHz ÷64/65 Dual Modulus Prescaler	8	P	D
MC12026A	1.1 GHz ÷8/9, ÷16/17 Dual Modulus Prescaler	8	P	D
MC12026B	1.1 GHz ÷8/9, ÷16/17 Dual Modulus Prescaler	8	P	D
MC12028A	1.1 GHz ÷32/33, ÷64/65 Dual Modulus Prescaler	8	P	D
MC12028B	1.1 GHz ÷32/33, ÷64/65 Dual Modulus Prescaler	8	P	D
MC12031A	2.0 GHz ÷64/65, ÷128/129 Low Voltage Dual Modulus Prescaler	8	P	D
MC12031B	2.0 GHz ÷64/65, ÷128/129 Low Voltage Dual Modulus Prescaler	8	P	D
MC12032A	2.0 GHz ÷64/65, ÷128/129 Dual Modulus Prescaler	8	P	D
MC12032B	2.0 GHz ÷64/65, ÷128/129 Dual Modulus Prescaler	8	P	D
MC12033A	2.0 GHz ÷32/33, ÷64/65 Low Voltage Dual Modulus Prescaler	8	P	D
MC12033B	2.0 GHz ÷32/33, ÷64/65 Low Voltage Dual Modulus Prescaler	8	P	D
MC12034A	2.0 GHz ÷32/33, ÷64/65 Dual Modulus Prescaler	8	P	D
MC12034B	2.0 GHz ÷32/33, ÷64/65 Dual Modulus Prescaler	8	P	D
MC12036A	1.1 GHz ÷64/65, ÷128/129 Dual Modulus Prescaler with Stand–By Mode	8	P	D
MC12036B	1.1 GHz ÷64/65, ÷128/129 Dual Modulus Prescaler with Stand–By Mode	8	P	D
MC12040	Phase–Frequency Detector	14	P,L	FN
MC12061	Crystal Oscillator	16	P,L	
MC12073	1.1 GHz ÷64 Prescaler	8	P	D
MC12074	1.1 GHz ÷256 Prescaler	8	P	D
MC12076	1.3 GHz ÷256 Prescaler	8	P	D
MC12078	1.3 GHz ÷256 Prescaler	8	P	D
MC12079	2.8 GHz ÷64/128/256 Prescaler	8	P	D
MC12080	1.1 GHz ÷10/20/40/80 Prescaler	8	P	D
MC12083	1.1 GHz ÷2 Low Power Prescaler with Stand–By Mode	8	P	D
MC12089	2.8 GHz ÷64/128/256 Low Power Prescaler	8	P	D
MC12090	750 MHz ÷2 UHF Prescaler	16	P,L	
MC12100	200 MHz Voltage Controlled Multivibrator	20	P	FN
MC12101	130 MHz Voltage Controlled Multivibrator	20	P	FN
MCH12140	Phase–Frequency Detector	8		D
MCK12140	Phase–Frequency Detector	8		D
MC12148	Low Power Voltage Controlled Oscillator	8		D,SD

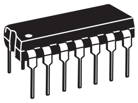
Communications Circuits Package Overview



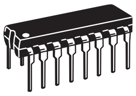
CASE 620
L SUFFIX



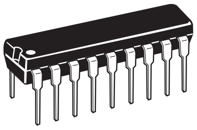
CASE 626
P SUFFIX



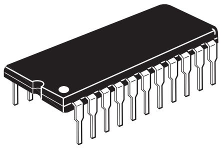
CASE 646
P SUFFIX



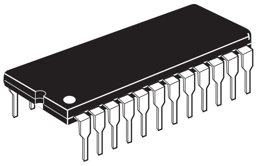
CASE 648
P SUFFIX



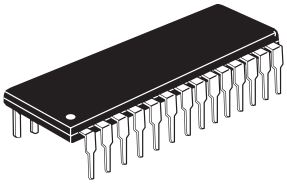
CASE 707
P SUFFIX



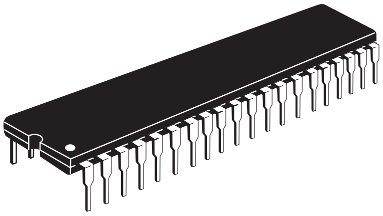
CASE 708
P SUFFIX



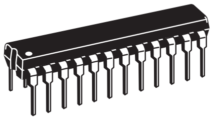
CASE 709
P SUFFIX



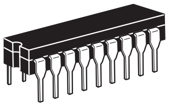
CASE 710
P SUFFIX



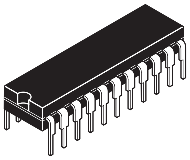
CASE 711
P SUFFIX



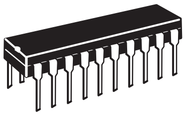
CASE 724
P SUFFIX



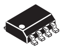
CASE 726
L SUFFIX



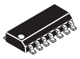
CASE 736B
PB SUFFIX



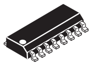
CASE 738
DP, P SUFFIX



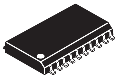
CASE 751
D, D1 SUFFIX



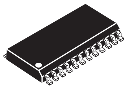
CASE 751A
D SUFFIX



CASE 751B
D SUFFIX

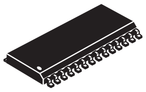


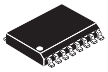
CASE 751D
DW, FP SUFFIX

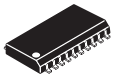


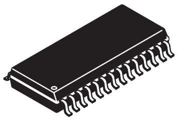
CASE 751E
DW SUFFIX

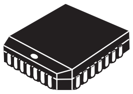
Communications Circuits Package Overview (continued)

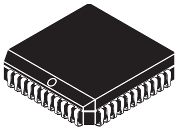

CASE 751F
DW SUFFIX

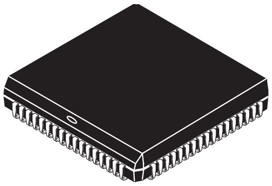

CASE 751G
DW SUFFIX

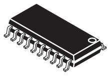

CASE 751J
F SUFFIX

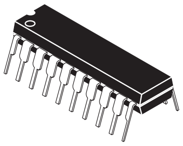

CASE 751M
FW SUFFIX

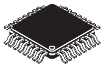

CASE 776
FN SUFFIX

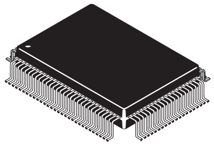

CASE 777
FN SUFFIX

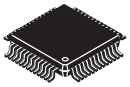

CASE 779
FN SUFFIX

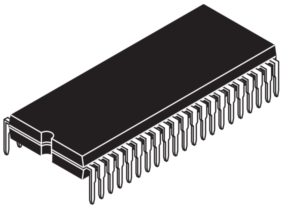

CASE 803C
F SUFFIX

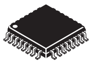

CASE 804
H SUFFIX

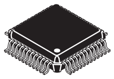

CASE 837A
DW SUFFIX

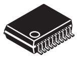

CASE 842D
PB SUFFIX

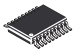

CASE 848B
FB SUFFIX

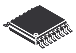

CASE 858
B SUFFIX


CASE 873
FB, FTB, FU SUFFIX


CASE 932
FTA SUFFIX


CASE 940C
SD SUFFIX


CASE 948D
DT SUFFIX


CASE 948F
DTB SUFFIX


CASE 976
FTB SUFFIX


CASE 977
FTA SUFFIX

Device Listing and Related Literature

RF Communications

Device	Function	Page
MC1496	Balanced Modulators/Demodulators	8–45
MC2833	Low Power FM Transmitter System	8–55
MC3335	Low Power Narrowband FM Receiver	8–62
MC3356	Wideband FSK Receiver	8–66
MC3357	Low Power Narrowband FM IF	8–72
MC3359	Low Power Narrowband FM IF	8–76
MC3362	Low Power Narrowband FM Receiver	8–82
MC3363	Low Power Dual Conversion FM Receiver	8–113
MC3371, MC3372	Low Power Narrowband FM IF	8–96
MC3374	Low Voltage FM Narrowband Receiver	8–89
MC13055	Wideband FSK Receiver	8–121
MC13135, MC13136	FM Communications Receivers	8–214
MC13141	Low Power DC – 1.8 GHz LNA and Mixer	8–226
MC13142	Low Power DC – 1.8 GHz LNA, Mixer and VCO	8–235
MC13143	Ultra Low Power DC – 2.4 GHz Linear Mixer	8–245
MC13144	VHF – 2.0 GHz Low Noise Amplifier with Programmable Bus	8–252
MC13150	Narrowband FM Coilless Detector IF Subsystem	8–258
MC13155	Wideband FM IF	8–275
MC13156	Wideband FM IF System	8–290
MC13158	Wideband FM IF Subsystem	8–308
MC13159	Wideband FM IF Amplifier	8–330
MC13173	Infrared Integrated Transceiver IC	8–336
MC13175, MC13176	UHF FM/AM Transmitter	8–353

Telecommunications

Device	Function	Page
MC3418	Continuously Variable Slope Delta Modulator/Demodulator	*
MC13109	Universal Cordless Telephone Subsystem IC	8–128
MC13110	Universal Cordless Telephone Subsystem IC with Scrambler	8–154
MC13111	Universal Cordless Telephone Subsystem IC	8–185
MC33110	Low Voltage Compander	*
MC33111	Low Voltage Compander with Mute and Feedthrough	*
MC33120	Subscriber Loop Interface Circuit	*
MC33121	Low Voltage Subscriber Loop Interface Circuit	*
MC33215	Telephone Line Interface and Speakerphone Circuit	**
MC33218A	Voice Switched Speakerphone with Microprocessor Interface	*
MC33219A	Voice Switched Speakerphone	*
MC34010	Electronic Telephone Circuit	*
MC34012	Telephone Tone Ringer	*
MC34014	Telephone Speech Network with Dialer Interface	*
MC34016	Cordless Universal Telephone Interface	*
MC34017	Telephone Tone Ringer	*
MC34018	Voice Switched Speakerphone Circuit	*
MC34114	Telephone Speech Network with Dialer Interface	*
MC34115	Continuously Variable Slope Delta Modulator/Demodulator	*
MC34117	Telephone Tone Ringer	*
MC34118	Voice Switched Speakerphone Circuit	*

**See Communications Device Data* (DL136)

** Call Sales Office.

Telecommunications (continued)

MC34119	Low Power Audio Amplifier	See Chapter 9
MC34129, MC33129	High Performance Current Mode Controllers	See Chapter 3
MC34216A	Programmable Telephone Line Interface Circuit with Loudspeaker Amplifier	*
TCA3385	Telephone Ring Signal Converter	*
TCA3388	Telephone Speech Network	*

**See Communications Device Data* (DL136)

RELATED APPLICATION NOTES

App Note	Title	Related Device
AN933	A Variety of Uses for the MC34012/MC34017 Tone Ringers	**MC34012, MC34017**
AN937	A Telephone Ringer which Complies with FCC and EIA Impedance Standards	**MC34012, MC34017**
AN957	Interfacing the Speakerphone to the MC34010/11/13 Speech Networks	**MC34010**
AN958	Transmit Gain Adjustments for the MC34014 Speech Network	**MC34014**
AN959	A Speakerphone with Receive Idle Mode	**MC34018**
AN960	Equalization of DTMF Signals Using the MC34014	**MC34014**
AN976	A New High Performance Current Mode Controller Teams Up with Current Sensing Power MOSFETs	**MC34129**
AN980	Low Power FM Dual Conversion Receivers	**MC3362, MC3363**
AN1002	A Handsfree Featurephone Design Using the MC34114 Speech Network and the MC34018 Speakerphone ICs	**MC34018** **MC34114**
AN1003	A Featurephone Design, with Tone Ringer and Dialer, Using the MC34118 Speakerphone IC	**MC34118, MC34017, MC145412, MC34119**
AN1004	A Handsfree Featurephone Design Using the MC34114 Speech Network and the MC34118 Speakerphone ICs	**MC34114, MC34118, MC34119, MC3417, MC145412**
AN1006	Linearize the Volume Control of the MC34118 Speakerphone	**MC34118**
AN1077	Adding Digital Volume Control to Speakerphone Circuits	**MC34018, MC34118**
AN1081	Minimize the “Pop” in the MC34119 Power Audio Amplifiers	**MC34119**
AN1510	A Mode Indicator for the MC34118 Speakerphone Circuit	**MC34118**
AN1544	Design of Continuously Variable Slope Delta Modulation Communications Systems	**MC3418, MC34115**
AN1575	Worldwide Cordless Telephone Frequencies	**MC13109, MC13110, MC13111**

OTHER RELATED LITERATURE

DL136	Communications Device Data
SG98	Linear Telecom Cross Reference

MC1496, B

Balanced Modulators/ Demodulators

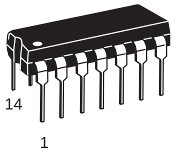
These devices were designed for use where the output voltage is a product of an input voltage (signal) and a switching function (carrier). Typical applications include suppressed carrier and amplitude modulation, synchronous detection, FM detection, phase detection, and chopper applications. See Motorola Application Note AN531 for additional design information.

- Excellent Carrier Suppression –65 dB typ @ 0.5 MHz
  –50 dB typ @ 10 MHz
- Adjustable Gain and Signal Handling
- Balanced Inputs and Outputs
- High Common Mode Rejection –85 dB typical

This device contains 8 active transistors.

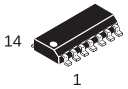
BALANCED MODULATORS/DEMODULATORS

SEMICONDUCTOR TECHNICAL DATA

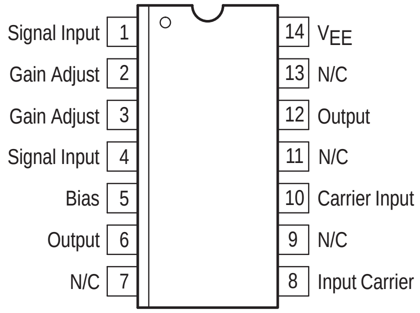


D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO–14)

P SUFFIX
PLASTIC PACKAGE
CASE 646



PIN CONNECTIONS



ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC1496D	T_A = 0°C to +70°C	SO–14
MC1496P		Plastic DIP
MC1496BP	T_A = –40°C to +125°C	Plastic DIP

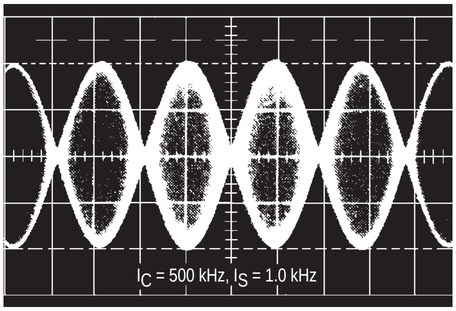


Figure 1. Suppressed Carrier Output Waveform

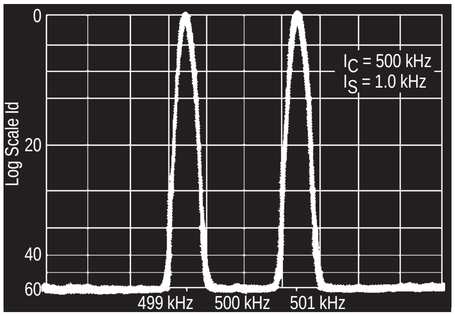


Figure 2. Suppressed Carrier Spectrum

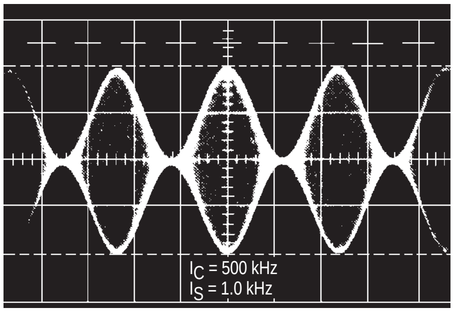
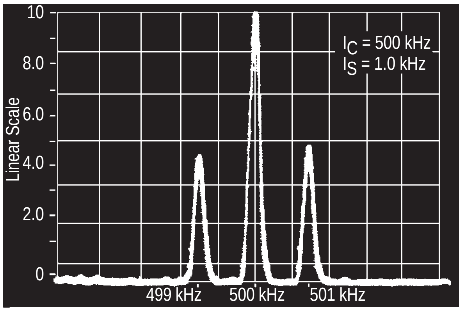


Figure 3. Amplitude Modulation Output Waveform

Figure 4. Amplitude–Modulation Spectrum



MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted.)

Rating	Symbol	Value	Unit
Applied Voltage (V6 – V8, V10 – V1, V12 – V8, V12 – V10, V8 – V4, V8 – V1, V10 – V4, V6 – V10, V2 – V5, V3 – V5)	ΔV	30	Vdc
Differential Input Signal	V8 – V10 V4 – V1	+5.0 $\pm(5 + I5R_e)$	Vdc
Maximum Bias Current	I_5	10	mA
Thermal Resistance, Junction–to–Air Plastic Dual In–Line Package	$R_{\theta JA}$	100	°C/W
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

NOTE: ESD data available upon request.

ELECTRICAL CHARACTERISTICS (V_{CC} = 12 Vdc, V_{EE} = –8.0 Vdc, I5 = 1.0 mAdc, R_L = 3.9 kΩ, R_e = 1.0 kΩ, $T_A = T_{low}$ to T_{high}, all input and output characteristics are single–ended, unless otherwise noted.)

Characteristic	Fig.	Note	Symbol	Min	Typ	Max	Unit
Carrier Feedthrough V_C = 60 mVrms sine wave and f_C = 1.0 kHz offset adjusted to zero f_C = 10 MHz V_C = 300 mVpp square wave: offset adjusted to zero f_C = 1.0 kHz offset not adjusted f_C = 1.0 kHz	5	1	V_{CFT}	 – – – –	 40 140 0.04 20	 – – 0.4 200	µVrms mVrms
Carrier Suppression f_S = 10 kHz, 300 mVrms f_C = 500 kHz, 60 mVrms sine wave f_C = 10 MHz, 60 mVrms sine wave	5	2	V_{CS}	 40 –	 65 50	 – –	dB k
Transadmittance Bandwidth (Magnitude) (R_L = 50 Ω) Carrier Input Port, V_C = 60 mVrms sine wave f_S = 1.0 kHz, 300 mVrms sine wave Signal Input Port, V_S = 300 mVrms sine wave $\|V_C\|$ = 0.5 Vdc	8	8	BW_{3dB}	 – –	 300 80	 – –	MHz
Signal Gain (V_S = 100 mVrms, f = 1.0 kHz; $\|V_C\|$= 0.5 Vdc)	10	3	A_{VS}	2.5	3.5	–	V/V
Single–Ended Input Impedance, Signal Port, f = 5.0 MHz Parallel Input Resistance Parallel Input Capacitance	6	–	 r_{ip} c_{ip}	 – –	 200 2.0	 – –	 kΩ pF
Single–Ended Output Impedance, f = 10 MHz Parallel Output Resistance Parallel Output Capacitance	6	–	 r_{op} c_{oo}	 – –	 40 5.0	 – –	 kΩ pF
Input Bias Current $I_{bS} = \frac{I1 + I4}{2}$; $I_{bC} = \frac{I8 + I10}{2}$	7	–	 I_{bS} I_{bC}	 – –	 12 12	 30 30	µA
Input Offset Current I_{ioS} = I1–I4; I_{ioC} = I8–I10	7	–	 $\|I_{ioS}\|$ $\|I_{ioC}\|$	 – –	 0.7 0.7	 7.0 7.0	µA
Average Temperature Coefficient of Input Offset Current (T_A = –55°C to +125°C)	7	–	$\|TC_{Iio}\|$	–	2.0	–	nA/°C
Output Offset Current (I6–I9)	7	–	$\|I_{oo}\|$	–	14	80	µA
Average Temperature Coefficient of Output Offset Current (T_A = –55°C to +125°C)	7	–	$\|TC_{Ioo}\|$	–	90	–	nA/°C
Common–Mode Input Swing, Signal Port, f_S = 1.0 kHz	9	4	CMV	–	5.0	–	Vpp
Common–Mode Gain, Signal Port, f_S = 1.0 kHz, $\|V_C\|$= 0.5 Vdc	9	–	ACM	–	–85	–	dB
Common–Mode Quiescent Output Voltage (Pin 6 or Pin 9)	10	–	V_{out}	–	8.0	–	Vpp
Differential Output Voltage Swing Capability	10	–	V_{out}	–	8.0	–	Vpp
Power Supply Current I6 +I12 I14	7	6	I_{CC} I_{EE}	– –	2.0 3.0	4.0 5.0	mAdc
DC Power Dissipation	7	5	P_D	–	33	–	mW

GENERAL OPERATING INFORMATION

Carrier Feedthrough

Carrier feedthrough is defined as the output voltage at carrier frequency with only the carrier applied (signal voltage = 0).

Carrier null is achieved by balancing the currents in the differential amplifier by means of a bias trim potentiometer (R1 of Figure 5).

Carrier Suppression

Carrier suppression is defined as the ratio of each sideband output to carrier output for the carrier and signal voltage levels specified.

Carrier suppression is very dependent on carrier input level, as shown in Figure 22. A low value of the carrier does not fully switch the upper switching devices, and results in lower signal gain, hence lower carrier suppression. A higher than optimum carrier level results in unnecessary device and circuit carrier feedthrough, which again degenerates the suppression figure. The MC1496 has been characterized with a 60 mVrms sinewave carrier input signal. This level provides optimum carrier suppression at carrier frequencies in the vicinity of 500 kHz, and is generally recommended for balanced modulator applications.

Carrier feedthrough is independent of signal level, V_S. Thus carrier suppression can be maximized by operating with large signal levels. However, a linear operating mode must be maintained in the signal–input transistor pair – or harmonics of the modulating signal will be generated and appear in the device output as spurious sidebands of the suppressed carrier. This requirement places an upper limit on input–signal amplitude (see Figure 20). Note also that an optimum carrier level is recommended in Figure 22 for good carrier suppression and minimum spurious sideband generation.

At higher frequencies circuit layout is very important in order to minimize carrier feedthrough. Shielding may be necessary in order to prevent capacitive coupling between the carrier input leads and the output leads.

Signal Gain and Maximum Input Level

Signal gain (single–ended) at low frequencies is defined as the voltage gain,

$$A_{VS} = \frac{V_o}{V_S} = \frac{R_L}{R_e + 2r_e} \quad \text{where } r_e = \frac{26\ \text{mV}}{I5(\text{mA})}$$

A constant dc potential is applied to the carrier input terminals to fully switch two of the upper transistors “on” and two transistors “off” ($V_C = 0.5$ Vdc). This in effect forms a cascode differential amplifier.

Linear operation requires that the signal input be below a critical value determined by R_E and the bias current I5.

$$V_S \leqslant I5\ R_E \text{ (Volts peak)}$$

Note that in the test circuit of Figure 10, V_S corresponds to a maximum value of 1.0 V peak.

Common Mode Swing

The common–mode swing is the voltage which may be applied to both bases of the signal differential amplifier, without saturating the current sources or without saturating the differential amplifier itself by swinging it into the upper switching devices. This swing is variable depending on the particular circuit and biasing conditions chosen.

Power Dissipation

Power dissipation, P_D, within the integrated circuit package should be calculated as the summation of the voltage–current products at each port, i.e. assuming V12 = V6, I5 = I6 = I12 and ignoring base current, $P_D = 2\ I5\ (V6 - V14) + I5)\ V5 - V14$ where subscripts refer to pin numbers.

Design Equations

The following is a partial list of design equations needed to operate the circuit with other supply voltages and input conditions.

A. Operating Current

The internal bias currents are set by the conditions at Pin 5. Assume:

$$I5 = I6 = I12,$$
$$I_B << I_C \text{ for all transistors}$$

then :

$$R5 = \frac{V - -\phi}{I5} - 500\ \Omega$$

where: R5 is the resistor between
Pin 5 and ground
$\phi = 0.75$ at $T_A = +25°C$

The MC1496 has been characterized for the condition $I_5 = 1.0$ mA and is the generally recommended value.

B. Common–Mode Quiescent Output Voltage

$$V6 = V12 = V+ - I5\ R_L$$

Biasing

The MC1496 requires three dc bias voltage levels which must be set externally. Guidelines for setting up these three levels include maintaining at least 2.0 V collector–base bias on all transistors while not exceeding the voltages given in the absolute maximum rating table;

$$30 \text{ Vdc} \geq [(V6, V12) - (V8, V10)] \geq 2 \text{ Vdc}$$
$$30 \text{ Vdc} \geq [(V8, V10) - (V1, V4)] \geq 2.7 \text{ Vdc}$$
$$30 \text{ Vdc} \geq [(V1, V4) - (V5)] \geq 2.7 \text{ Vdc}$$

The foregoing conditions are based on the following approximations:

$$V6 = V12, V8 = V10, V1 = V4$$

Bias currents flowing into Pins 1, 4, 8 and 10 are transistor base currents and can normally be neglected if external bias dividers are designed to carry 1.0 mA or more.

Transadmittance Bandwidth

Carrier transadmittance bandwidth is the 3.0 dB bandwidth of the device forward transadmittance as defined by:

$$\gamma 21C = \frac{i_o \text{ (each sideband)}}{v_s \text{ (signal)}} \Bigg|\, V_o = 0$$

Signal transadmittance bandwidth is the 3.0 dB bandwidth of the device forward transadmittance as defined by:

$$\gamma 21S = \frac{i_o \text{ (signal)}}{v_s \text{ (signal)}} \Bigg|\, V_c = 0.5 \text{ Vdc},\ V_o = 0$$

Coupling and Bypass Capacitors

Capacitors C1 and C2 (Figure 5) should be selected for a reactance of less than 5.0 Ω at the carrier frequency.

Output Signal

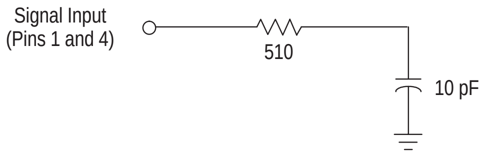
The output signal is taken from Pins 6 and 12 either balanced or single–ended. Figure 11 shows the output levels of each of the two output sidebands resulting from variations in both the carrier and modulating signal inputs with a single–ended output connection.

Negative Supply

V_{EE} should be dc only. The insertion of an RF choke in series with V_{EE} can enhance the stability of the internal current sources.

Signal Port Stability

Under certain values of driving source impedance, oscillation may occur. In this event, an RC suppression network should be connected directly to each input using short leads. This will reduce the Q of the source–tuned circuits that cause the oscillation.



An alternate method for low–frequency applications is to insert a 1.0 kΩ resistor in series with the input (Pins 1, 4). In this case input current drift may cause serious degradation of carrier suppression.

TEST CIRCUITS

Figure 5. Carrier Rejection and Suppression

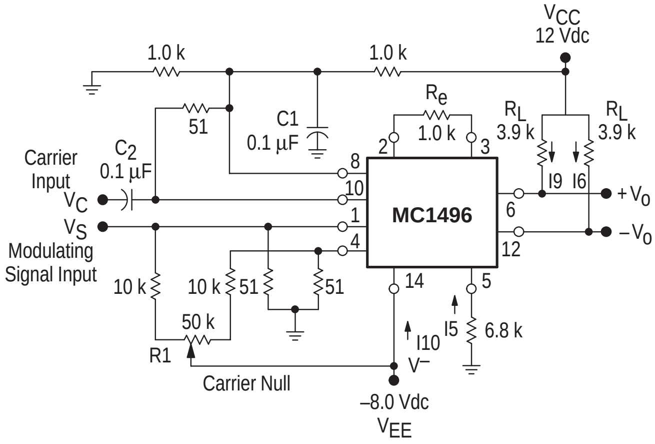
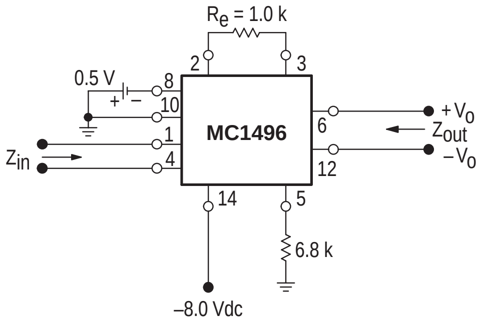


Figure 6. Input–Output Impedance



NOTE: Shielding of input and output leads may be needed to properly perform these tests.

Figure 7. Bias and Offset Currents

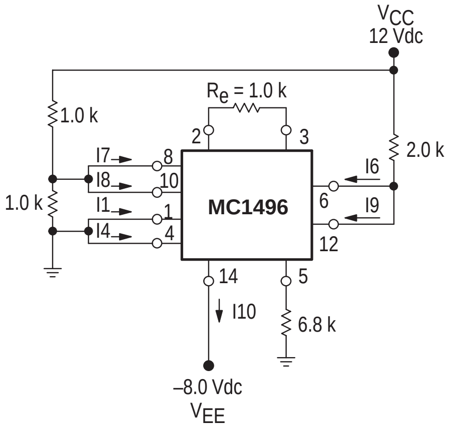
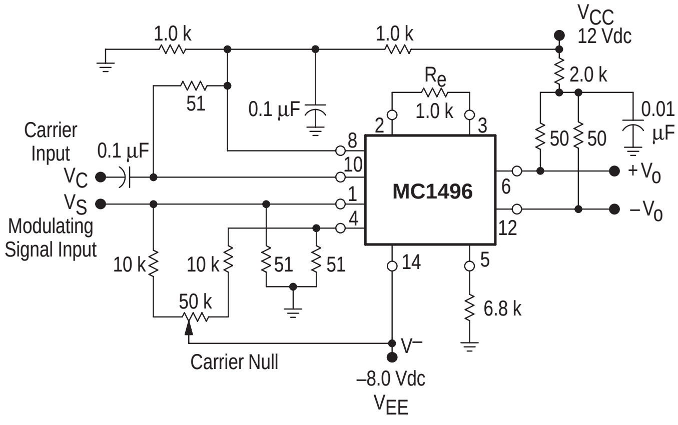


Figure 8. Transconductance Bandwidth



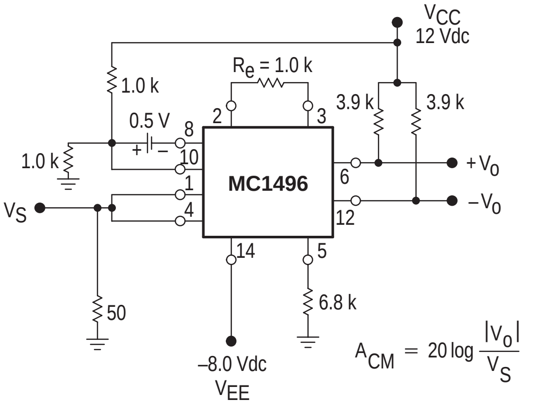


Figure 9. Common Mode Gain

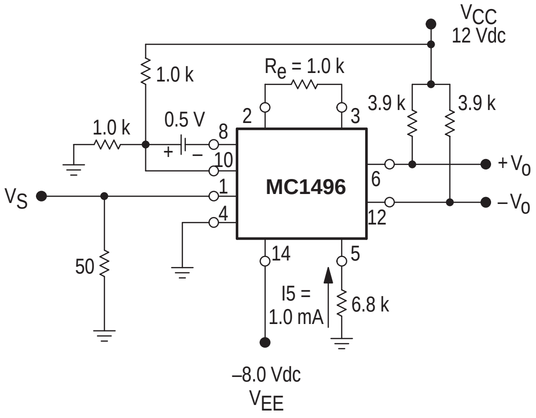


Figure 10. Signal Gain and Output Swing

TYPICAL CHARACTERISTICS

Typical characteristics were obtained with circuit shown in Figure 5, f_C = 500 kHz (sine wave), V_C = 60 mVrms, f_S = 1.0 kHz, V_S = 300 mVrms, T_A = 25°C, unless otherwise noted.

Figure 11. Sideband Output versus Carrier Levels

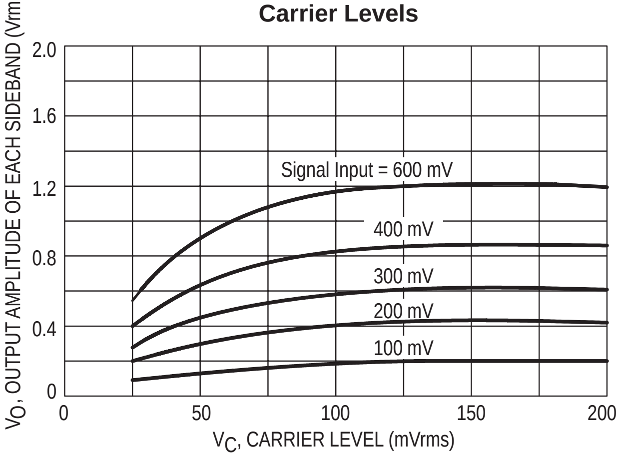


Figure 12. Signal–Port Parallel–Equivalent Input Resistance versus Frequency

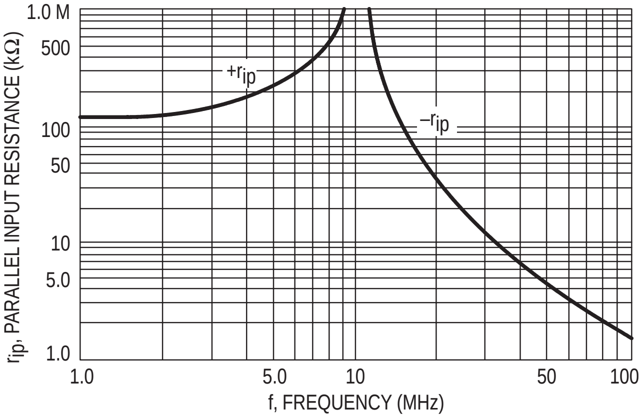


Figure 13. Signal–Port Parallel–Equivalent Input Capacitance versus Frequency

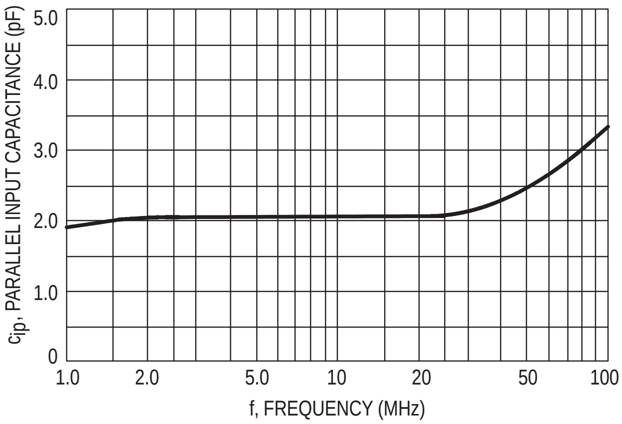
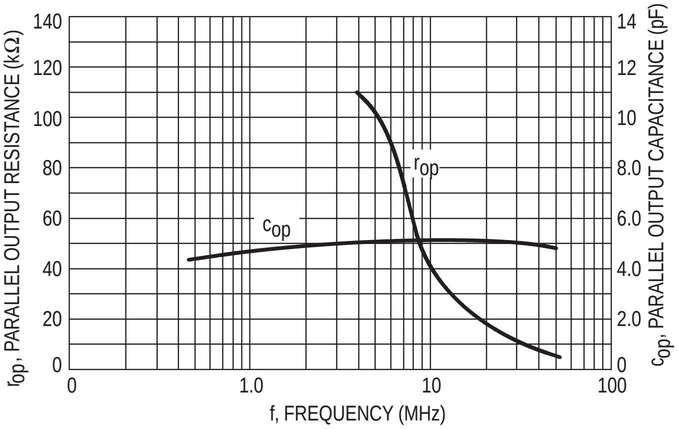


Figure 14. Single–Ended Output Impedance versus Frequency



TYPICAL CHARACTERISTICS (continued)

Typical characteristics were obtained with circuit shown in Figure 5, f_C = 500 kHz (sine wave), V_C = 60 mVrms, f_S = 1.0 kHz, V_S = 300 mVrms, T_A = 25°C, unless otherwise noted.

Figure 15. Sideband and Signal Port Transadmittances versus Frequency

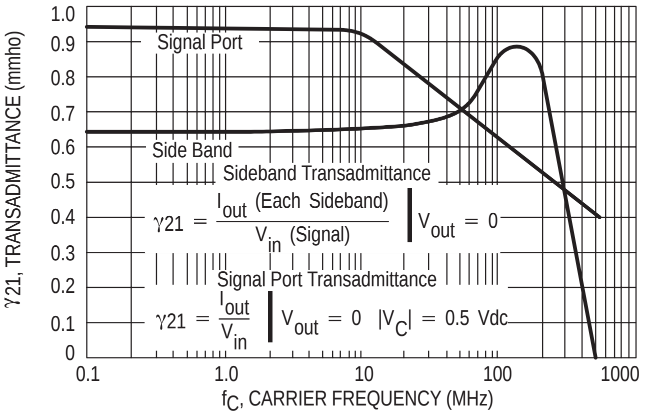


Figure 16. Carrier Suppression versus Temperature

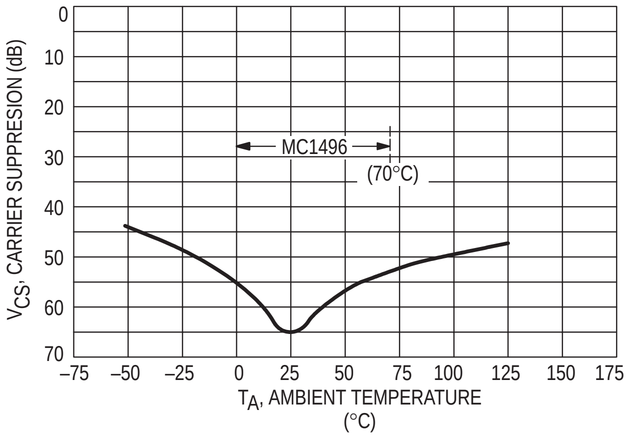


Figure 17. Signal–Port Frequency Response

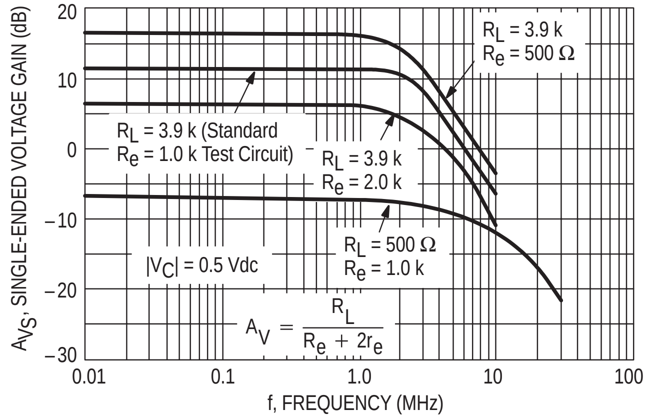


Figure 18. Carrier Suppression versus Frequency

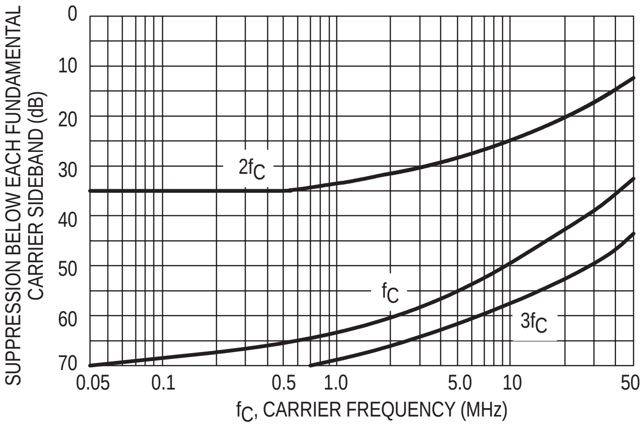


Figure 19. Carrier Feedthrough versus Frequency

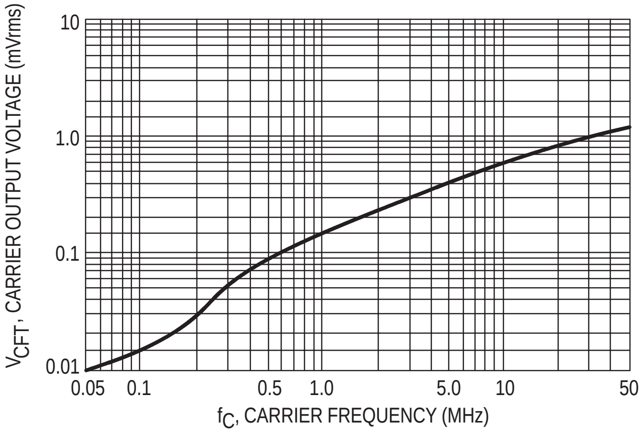


Figure 20. Sideband Harmonic Suppression versus Input Signal Level

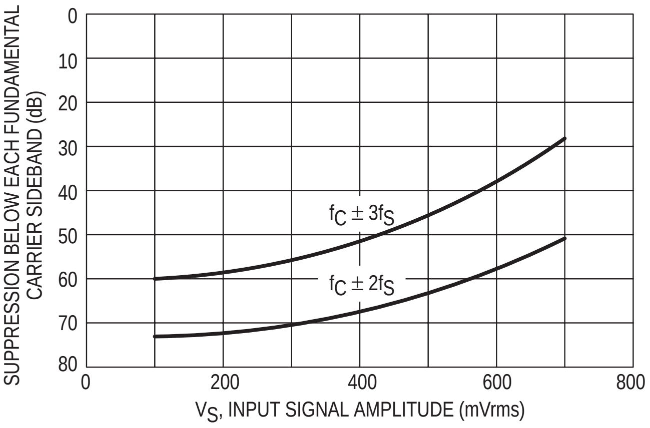


Figure 21. Suppression of Carrier Harmonic Sidebands versus Carrier Frequency

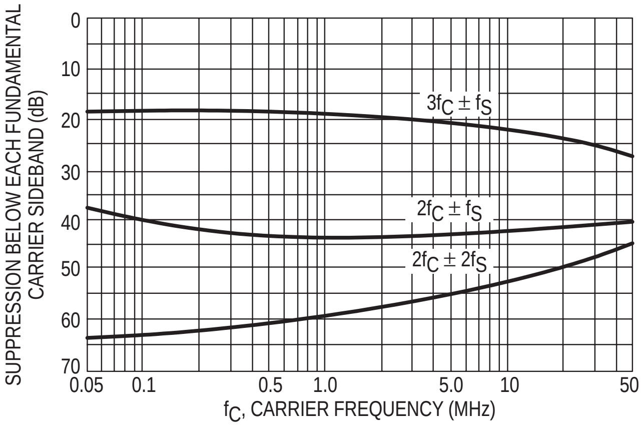
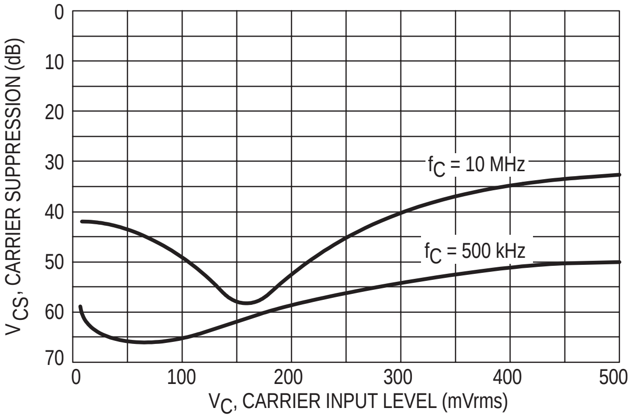


Figure 22. Carrier Suppression versus Carrier Input Level



OPERATIONS INFORMATION

The MC1496, a monolithic balanced modulator circuit, is shown in Figure 23.

This circuit consists of an upper quad differential amplifier driven by a standard differential amplifier with dual current sources. The output collectors are cross–coupled so that full–wave balanced multiplication of the two input voltages occurs. That is, the output signal is a constant times the product of the two input signals.

Mathematical analysis of linear ac signal multiplication indicates that the output spectrum will consist of only the sum and difference of the two input frequencies. Thus, the device may be used as a balanced modulator, doubly balanced mixer, product detector, frequency doubler, and other applications requiring these particular output signal characteristics.

The lower differential amplifier has its emitters connected to the package pins so that an external emitter resistance may be used. Also, external load resistors are employed at the device output.

Signal Levels

The upper quad differential amplifier may be operated either in a linear or a saturated mode. The lower differential amplifier is operated in a linear mode for most applications.

For low–level operation at both input ports, the output signal will contain sum and difference frequency components and have an amplitude which is a function of the product of the input signal amplitudes.

For high–level operation at the carrier input port and linear operation at the modulating signal port, the output signal will contain sum and difference frequency components of the modulating signal frequency and the fundamental and odd harmonics of the carrier frequency. The output amplitude will be a constant times the modulating signal amplitude. Any amplitude variations in the carrier signal will not appear in the output.

The linear signal handling capabilities of a differential amplifier are well defined. With no emitter degeneration, the maximum input voltage for linear operation is approximately 25 mV peak. Since the upper differential amplifier has its emitters internally connected, this voltage applies to the carrier input port for all conditions.

Since the lower differential amplifier has provisions for an external emitter resistance, its linear signal handling range may be adjusted by the user. The maximum input voltage for linear operation may be approximated from the following expression:

$$V = (I5)\ (R_E) \text{ volts peak.}$$

This expression may be used to compute the minimum value of R_E for a given input voltage amplitude.

Figure 23. Circuit Schematic

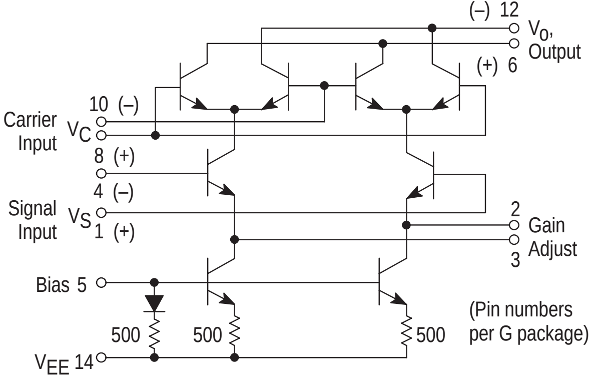


Figure 24. Typical Modulator Circuit

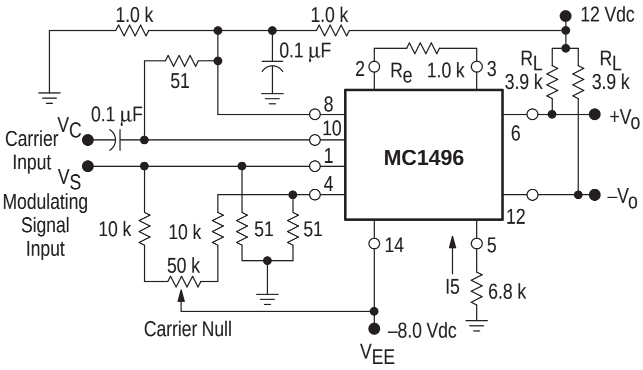


Figure 25. Voltage Gain and Output Frequencies

Carrier Input Signal (V_C)	Approximate Voltage Gain	Output Signal Frequency(s)
Low–level dc	$\frac{R_L \; V_C}{2(R_E + 2r_e)\left(\frac{KT}{q}\right)}$	f_M
High–level dc	$\frac{R_L}{R_E + 2r_e}$	f_M
Low–level ac	$\frac{R_L \; V_C(rms)}{2\sqrt{2}\left(\frac{KT}{q}\right)(R_E + 2r_e)}$	$f_C \pm f_M$
High–level ac	$\frac{0.637 \; R_L}{R_E + 2r_e}$	$f_C \pm f_M, 3f_C \pm f_M, 5f_C \pm f_M, \; . \; . \; .$

NOTES: 1. Low–level Modulating Signal, V_M, assumed in all cases. V_C is Carrier Input Voltage.
2. When the output signal contains multiple frequencies, the gain expression given is for the output amplitude of each of the two desired outputs, $f_C + f_M$ and $f_C - f_M$.
3. All gain expressions are for a single–ended output. For a differential output connection, multiply each expression by two.
4. R_L = Load resistance.
5. R_E = Emitter resistance between Pins 2 and 3.
6. r_e = Transistor dynamic emitter resistance, at 25°C;

$$re \approx \frac{26 \text{ mV}}{I_5 \text{ (mA)}}$$

7. K = Boltzmann's Constant, T = temperature in degrees Kelvin, q = the charge on an electron.

$$\frac{KT}{q} \approx 26 \text{ mV at room temperature}$$

The gain from the modulating signal input port to the output is the MC1496 gain parameter which is most often of interest to the designer. This gain has significance only when the lower differential amplifier is operated in a linear mode, but this includes most applications of the device.

As previously mentioned, the upper quad differential amplifier may be operated either in a linear or a saturated mode. Approximate gain expressions have been developed for the MC1496 for a low–level modulating signal input and the following carrier input conditions:

1) Low–level dc
2) High–level dc
3) Low–level ac
4) High–level ac

These gains are summarized in Figure 25, along with the frequency components contained in the output signal.

APPLICATIONS INFORMATION

Double sideband suppressed carrier modulation is the basic application of the MC1496. The suggested circuit for this application is shown on the front page of this data sheet.

In some applications, it may be necessary to operate the MC1496 with a single dc supply voltage instead of dual supplies. Figure 26 shows a balanced modulator designed for operation with a single 12 Vdc supply. Performance of this circuit is similar to that of the dual supply modulator.

AM Modulator

The circuit shown in Figure 27 may be used as an amplitude modulator with a minor modification.

All that is required to shift from suppressed carrier to AM operation is to adjust the carrier null potentiometer for the proper amount of carrier insertion in the output signal.

However, the suppressed carrier null circuitry as shown in Figure 27 does not have sufficient adjustment range. Therefore, the modulator may be modified for AM operation by changing two resistor values in the null circuit as shown in Figure 28.

Product Detector

The MC1496 makes an excellent SSB product detector (see Figure 29).

This product detector has a sensitivity of 3.0 microvolts and a dynamic range of 90 dB when operating at an intermediate frequency of 9.0 MHz.

The detector is broadband for the entire high frequency range. For operation at very low intermediate frequencies down to 50 kHz the 0.1 μF capacitors on Pins 8 and 10 should be increased to 1.0 μF. Also, the output filter at Pin 12 can be tailored to a specific intermediate frequency and audio amplifier input impedance.

As in all applications of the MC1496, the emitter resistance between Pins 2 and 3 may be increased or decreased to adjust circuit gain, sensitivity, and dynamic range.

This circuit may also be used as an AM detector by introducing carrier signal at the carrier input and an AM signal at the SSB input.

The carrier signal may be derived from the intermediate frequency signal or generated locally. The carrier signal may be introduced with or without modulation, provided its level is sufficiently high to saturate the upper quad differential amplifier. If the carrier signal is modulated, a 300 mVrms input level is recommended.

Doubly Balanced Mixer

The MC1496 may be used as a doubly balanced mixer with either broadband or tuned narrow band input and output networks.

The local oscillator signal is introduced at the carrier input port with a recommended amplitude of 100 mVrms.

Figure 30 shows a mixer with a broadband input and a tuned output.

Frequency Doubler

The MC1496 will operate as a frequency doubler by introducing the same frequency at both input ports.

Figures 31 and 32 show a broadband frequency doubler and a tuned output very high frequency (VHF) doubler, respectively.

Phase Detection and FM Detection

The MC1496 will function as a phase detector. High–level input signals are introduced at both inputs. When both inputs are at the same frequency the MC1496 will deliver an output which is a function of the phase difference between the two input signals.

An FM detector may be constructed by using the phase detector principle. A tuned circuit is added at one of the inputs to cause the two input signals to vary in phase as a function of frequency. The MC1496 will then provide an output which is a function of the input signal frequency.

TYPICAL APPLICATIONS

Figure 26. Balanced Modulator (12 Vdc Single Supply)

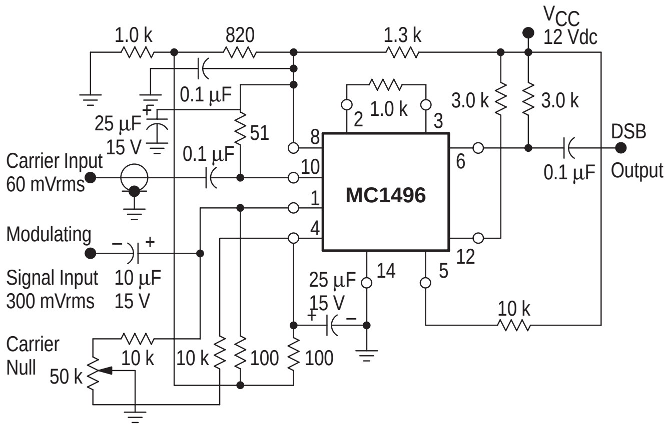


Figure 27. Balanced Modulator–Demodulator

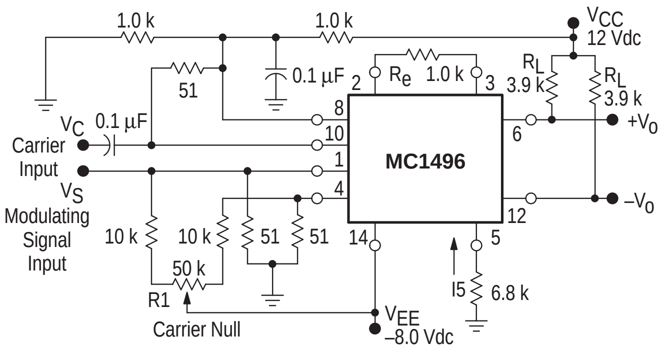


Figure 28. AM Modulator Circuit

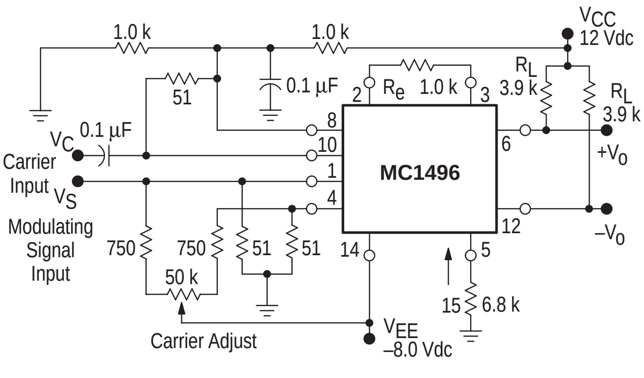


Figure 29. Product Detector (12 Vdc Single Supply)

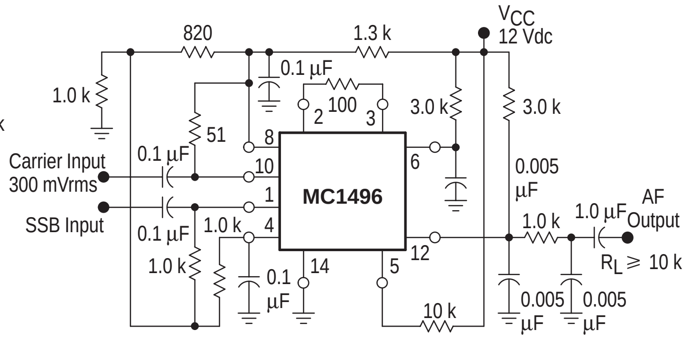
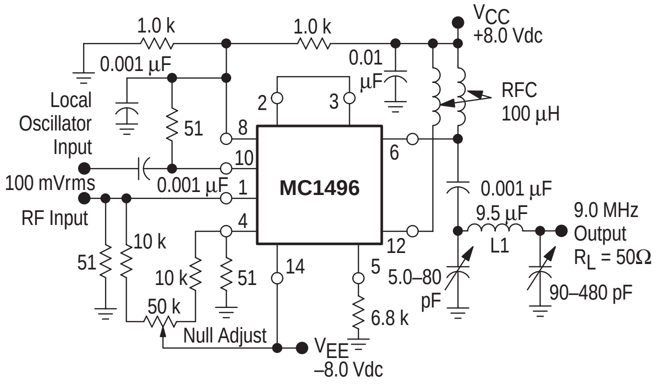


Figure 30. Doubly Balanced Mixer (Broadband Inputs, 9.0 MHz Tuned Output)



L1 = 44 Turns AWG No. 28 Enameled Wire, Wound on Micrometals Type 44–6 Toroid Core.

Figure 31. Low–Frequency Doubler

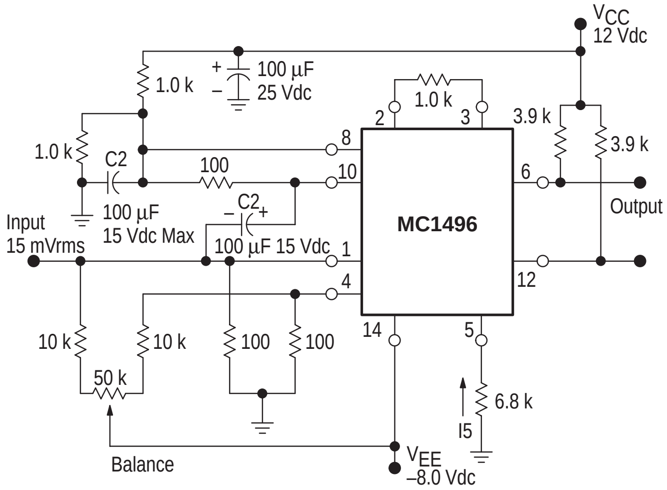
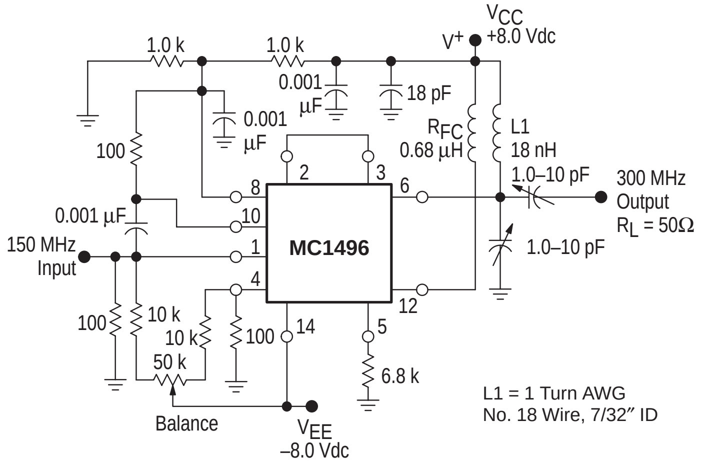
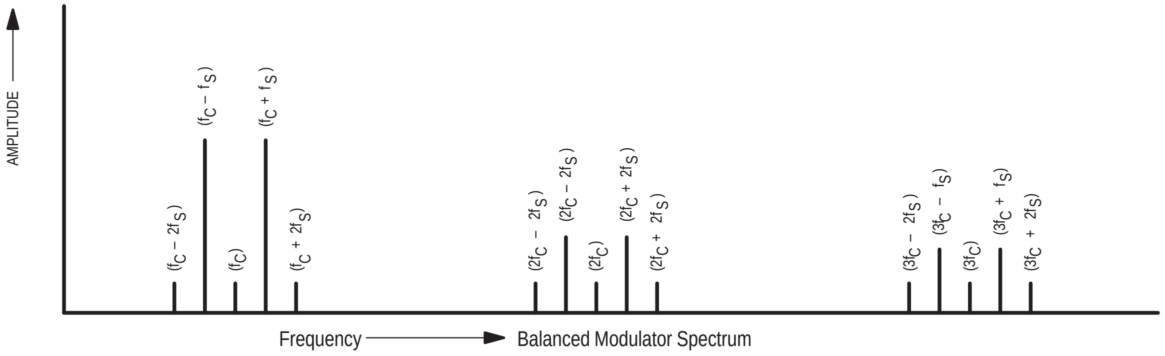


Figure 32. 150 to 300 MHz Doubler



L1 = 1 Turn AWG No. 18 Wire, 7/32″ ID



Balanced Modulator Spectrum

DEFINITIONS

f_C	Carrier Fundamental	$f_C \pm nf_S$	Fundamental Carrier Sideband Harmonics
f_S	Modulating Signal	nf_C	Carrier Harmonics
$f_C \pm f_S$	Fundamental Carrier Sidebands	$nf_C \pm nf_S$	Carrier Harmonic Sidebands

MC2833

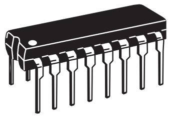
Low Power FM Transmitter System

MC2833 is a one–chip FM transmitter subsystem designed for cordless telephone and FM communication equipment. It includes a microphone amplifier, voltage controlled oscillator and two auxiliary transistors.

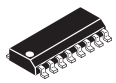
- Wide Range of Operating Supply Voltage (2.8–9.0 V)
- Low Drain Current (I_{CC} = 2.9 mA Typ)
- Low Number of External Parts Required
- – 30 dBm Power Output to 60 MHz Using Direct RF Output
- +10 dBm Power Output Attainable Using On–Chip Transistor Amplifiers
- Users Must Comply with Local Regulations on R.F. Transmission (FCC, DOT, P.T.T., etc)

LOW POWER FM TRANSMITTER SYSTEM

SEMICONDUCTOR TECHNICAL DATA

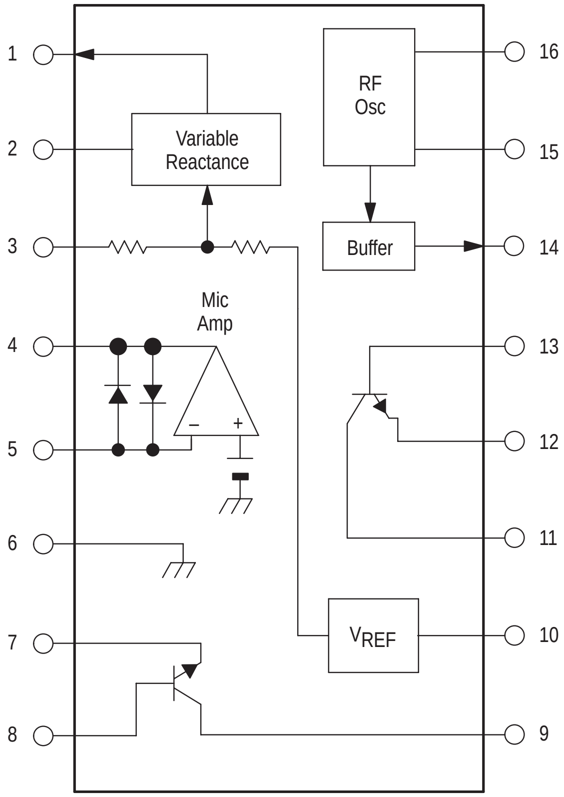


P SUFFIX
PLASTIC PACKAGE
CASE 648

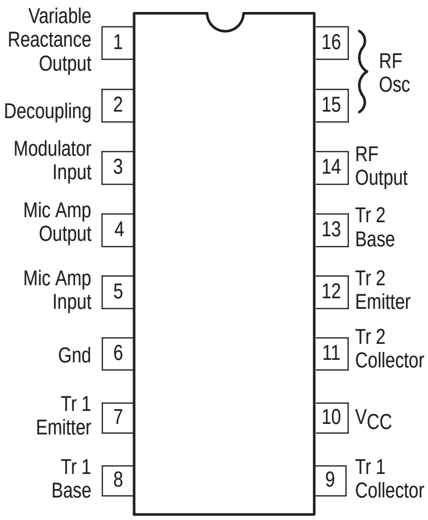


D SUFFIX
PLASTIC PACKAGE
CASE 751B
(SO–16)

Representative Block Diagram



PIN CONNECTIONS



ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC2833D	T_A = – 30 to +75°C	SO–16
MC2833P		Plastic DIP

MAXIMUM RATINGS

Ratings	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	10 (max)	V
Operating Supply Voltage Range	V_{CC}	2.8–9.0	V
Junction Temperature	T_J	+ 150	°C
Operating Ambient Temperature	T_A	– 30 to + 75	°C
Storage Temperature Range	T_{stg}	– 65 to + 150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 4.0 V, T_A = 25°C, unless otherwise noted)

Characteristics	Symbol	Pin	Min	Typ	Max	Unit
Drain Current (No input signal)	I_{CC}	10	1.7	2.9	4.3	mA
FM MODULATOR						
Output RF Voltage (f_o = 16.6 MHz)	V_{out} RF	14	60	90	130	mVrms
Output DC Voltage (No input signal)	Vdc	14	2.2	2.5	2.8	V
Modulation Sensitivity (f_o = 16.6 MHz) (V_{in} = 0.8 V to 1.2 V)	SEN	3 14	7.0 –	10 –	15 –	Hz/mVdc
Maximum Deviation (f_o = 16.6 MHz) (V_{in} = 0 V to 2.0 V)	Fdev	3 14	3.0 –	5.0 –	10 –	kHz
MIC AMPLIFIER						
Closed Loop Voltage Gain (V_{in} = 3.0 mVrms) (f_{in} = 1.0 kHz)	A_V	4 5	27 –	30 –	33 –	dB
Output DC Voltage (No input signal)	V_{out} dc	4	1.1	1.4	1.7	V
Output Swing Voltage (V_{in} = 30 mVrms) (f_{in} = 1.0 kHz)	V_{out} p–p	4	0.8	1.2	1.6	Vp–p
Total Harmonic Distortion (V_{in} = 3.0 mVrms) (f_{in} = 1.0 kHz)	THD	4	–	0.15	2.0	%

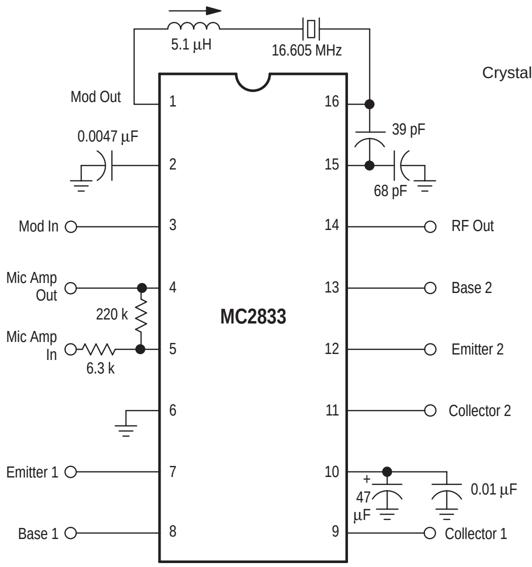
AUXILIARY TRANSISTOR STATIC CHARACTERISTICS

Characteristics	Symbol	Min	Typ	Max	Unit
Collector Base Breakdown Voltage (I_C = 5.0 μA)	$V_{(BR)CBO}$	15	45	–	V
Collector Emitter Breakdown Voltage (I_C = 200 μA)	$V_{(BR)CEO}$	10	15	–	V
Collector Substrate Breakdown Voltage (I_C = 50 μA)	$V_{(BR)CSO}$	–	70	–	V
Emitter Base Breakdown Voltage (I_E = 50 μA)	$V_{(BR)EBO}$	–	6.2	–	V
Collector Base Cut Off Current (V_{CB} = 10 V) (I_E = 0)	I_{CBO}	–	–	200	nA
DC Current Gain (I_C = 3.0 mA) (V_{CE} = 3.0 V)	h_{FE}	40	150	–	–

AUXILIARY TRANSISTOR DYNAMIC CHARACTERISTICS

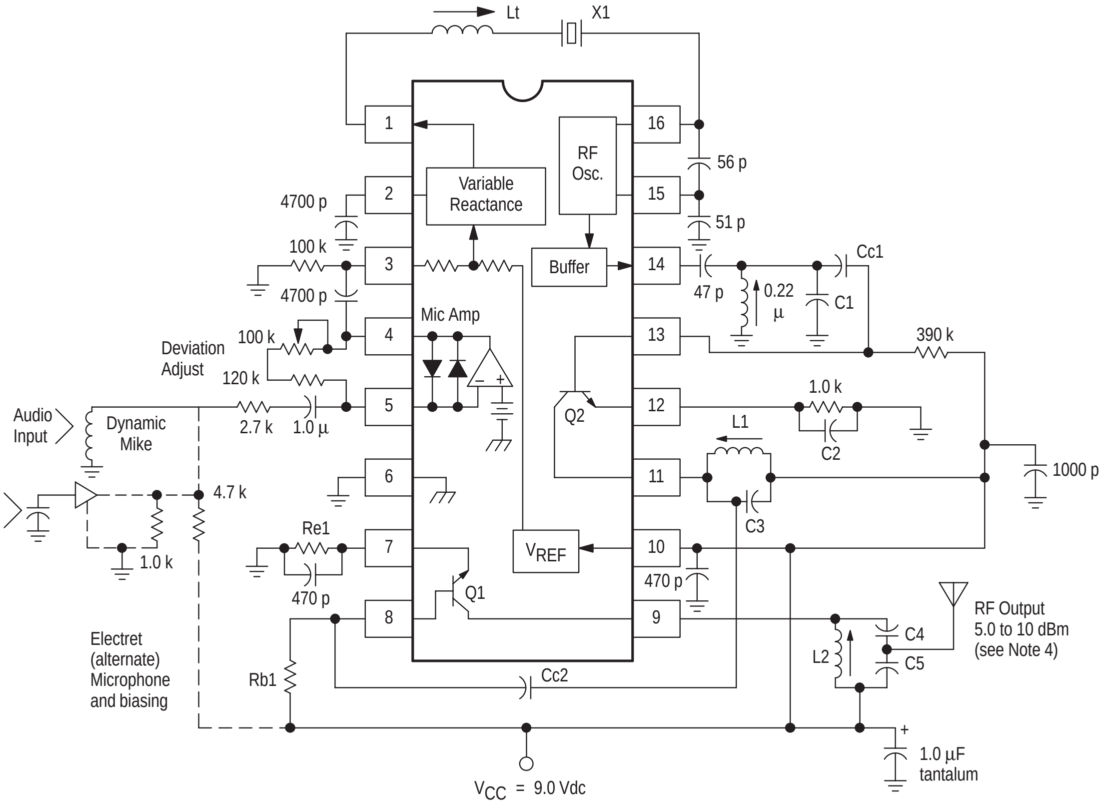
Current Gain Bandwidth Product (V_{CE} = 3.0 V) (I_C = 3.0 mA)	f_T	–	500	–	MHz
Collector Base Capacitance (V_{CE} = 3.0 V) (I_C = 0)	C_{CB}	–	2.0	–	pF
Collector Substrate Capacitance (V_{CS} = 3.0 V) (I_C = 0)	C_{CS}	–	3.3	–	pF

Figure 1. Test Circuit



Crystal: f_o = 16.605 MHz
C_L = 30 pF
C_o = 6.1 pF
R_S = 10 Ω Max

Figure 2. Single Chip VHF Narrowband FM Transmitter



NOTES:

1. Components versus output frequency:

Output RF	X1 (MHz)	Lt (µH)	L1 (µH)	L2 (µH)	Re1	Rb1	Cc1	Cc2	C1	C2	C3	C4	C5
49.7 MHz	16.5667	3.3–4.7	0.22	0.22	330	390 k	33 p	33 p	33 p	470 p	33 p	47 p	220 p
76 MHz	12.6000	5.1	0.22	0.22	150	300 k	68 p	10 p	68 p	470 p	12 p	20 p	120 p
144.6 MHz	12.05	5.6	0.15	0.10	150	220 k	47 p	10 p	68 p	1000 p	18 p	12 p	33 p

2. Crystal X1 is fundamental mode, calibrated for parallel resonance with a 32 pF load. The final output frequency is generated by frequency multiplication within the MC2833 IC. The RF output buffer (Pin 14) and Q2 transistor are used as a frequency tripler and doubler, respectively, in the 76 and 144.6 MHz transmitters. The Q1 output transistor is a linear amplifier in the 49.7 MHz and 76 MHz transmitters, and a frequency doubler in the 144.6 MHz transmitter.
3. All coils used are 7 mm shielded inductors, CoilCraft series M1175A, M1282A–M1289A, M1312A or equivalent.
4. Power output is ≈ + 10 dBm for 49.7 MHz and 76 MHz transmitters, and ≈ + 5.0 dBm for the 144.6 MHz transmitter at V_{CC} = 8.0 V. Power output drops with lower V_{CC}.
5. All capacitors in microfarads, inductors in Henries and resistors in Ohms unless otherwise specified.
6. Other frequency combinations may be set–up by simple scaling of the 3 examples shown.

Figure 3. Buffer/Multiplier (x3, Pin 14)
(16 MHz Fundamental)

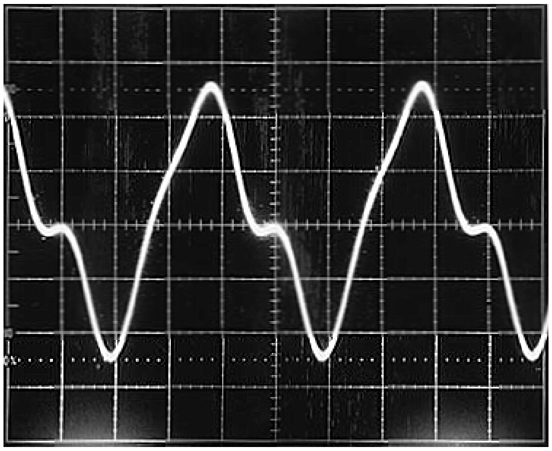


Figure 4. Input to Doubler (Pin 13)
(49.7 MHz x 3 Component)

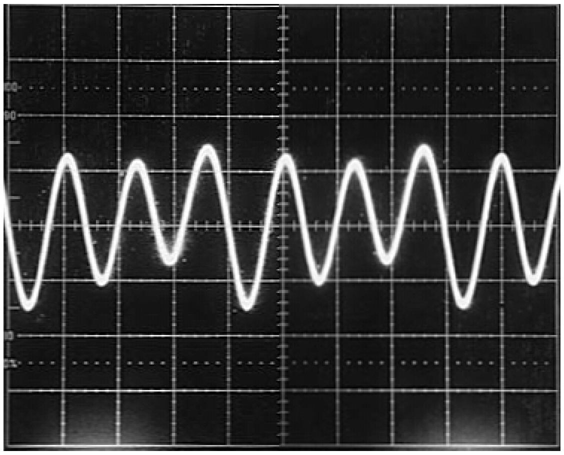


Figure 5. Doubler Output 76 MHz (Pin 11)

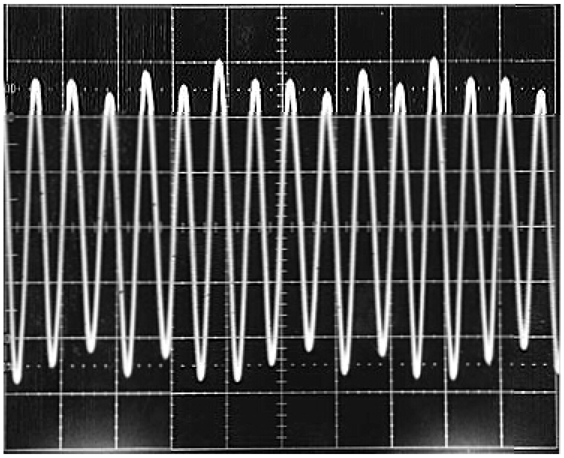


Figure 6. Spectrum

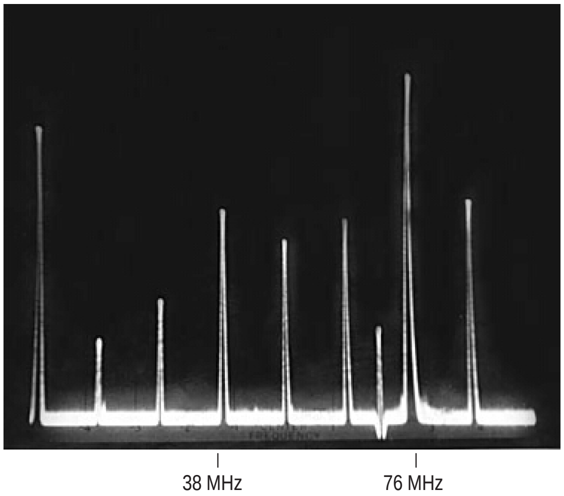


Figure 7. Output Spectrum (49.7 MHz)

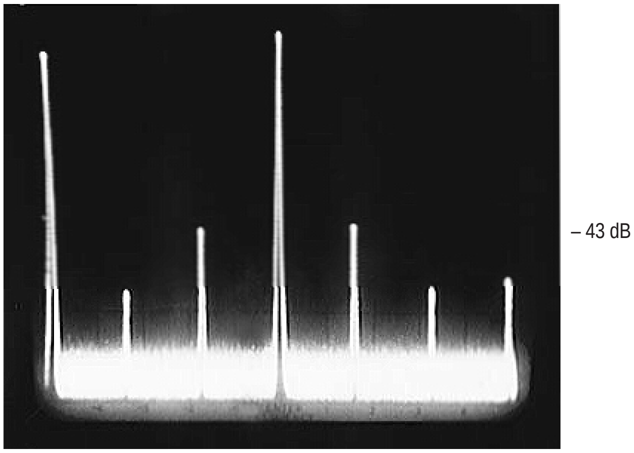
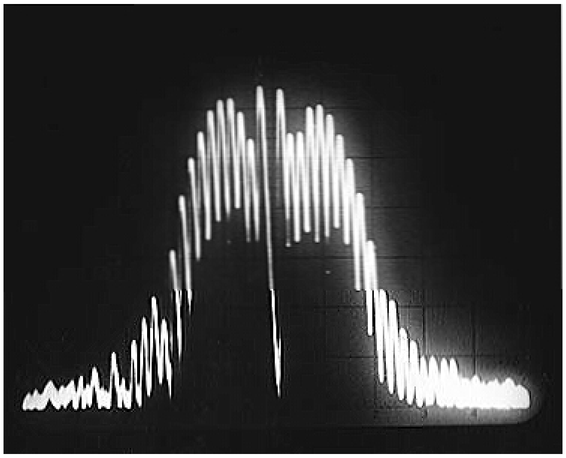


Figure 8. Modulation Spectrum
(1.0 kHz Showing Carrier Null)



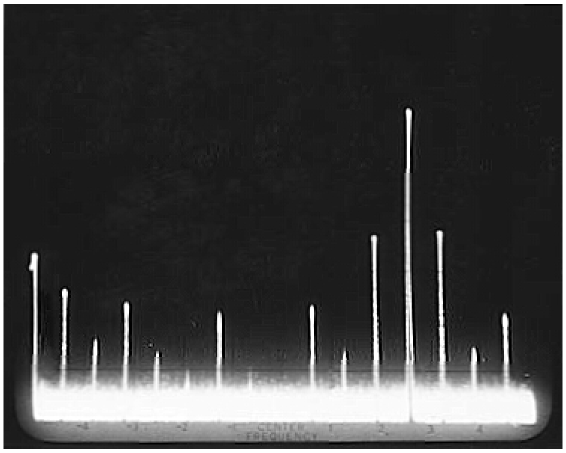


Figure 9. 144.6 MHz/x12 Multiplier

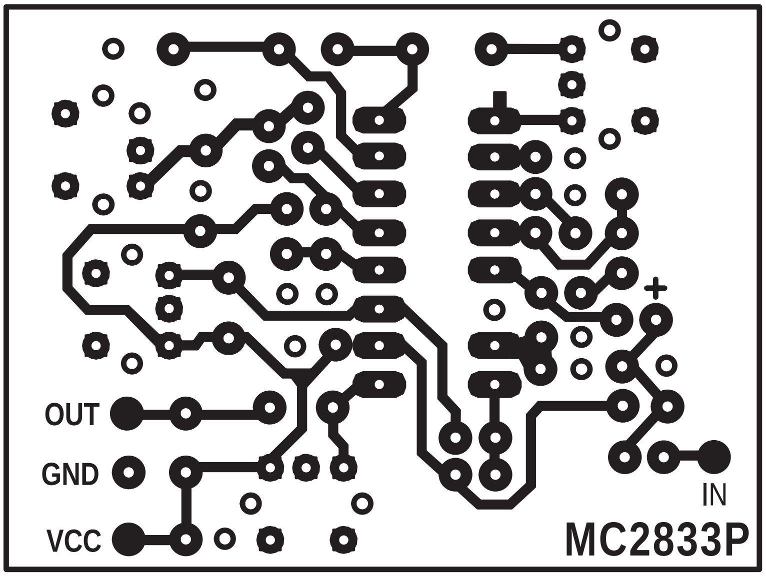


Figure 10. Circuit Side View

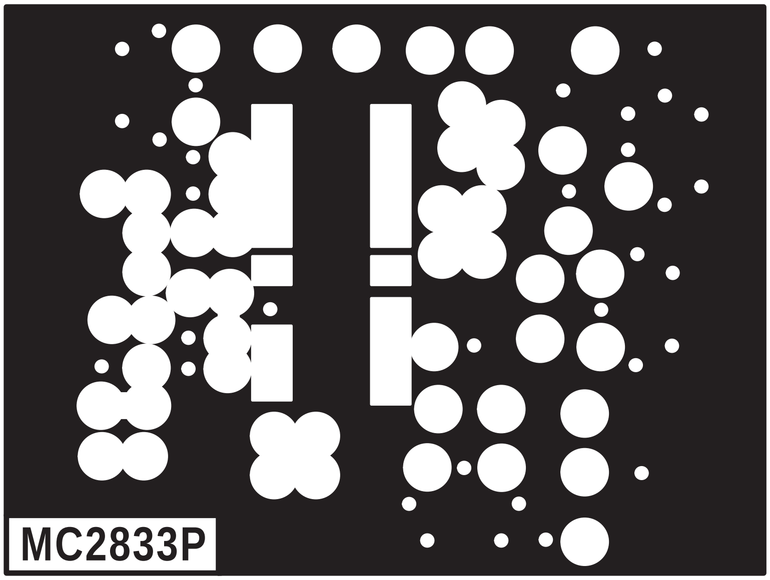
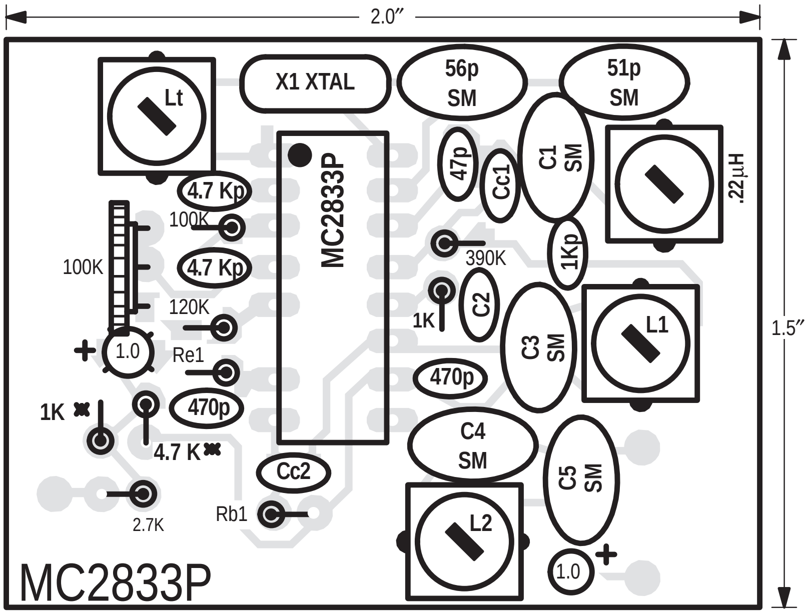


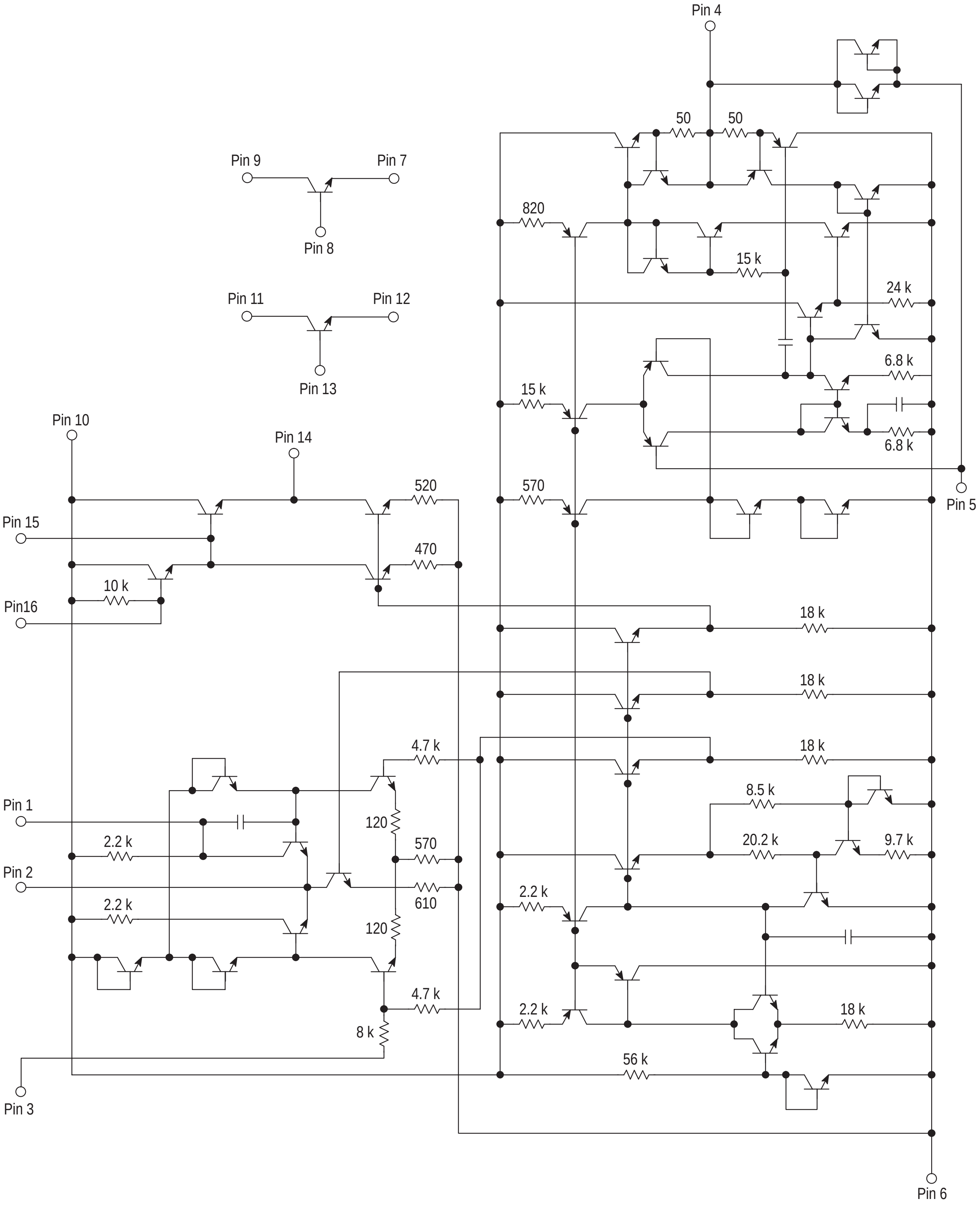
Figure 11. Ground Plane on Component Side

Figure 12. Component View



NOTES:
- Positive artwork provided.
- Drill holes must be plated to ensure making all ground (V_{EE}) connections!
- Resistors labelled * are used for biasing of electret microphone if used.
- Capacitors labelled ″SM″ are silver mica.
- Final board size 1.5″ × 2.0″.

Figure 13. Circuit Schematic



MOTOROLA

Low Power Narrowband FM Receiver

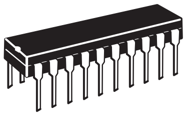
MC3335

LOW POWER DUAL CONVERSION FM RECEIVER

SEMICONDUCTOR TECHNICAL DATA

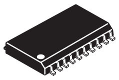
. . . includes dual FM conversion with Oscillators, Mixers, Quadrature Discriminator, and Meter Drive/Carrier Detect Circuitry. The MC3335 also has a comparator circuit for FSK detection.

- Complete Dual Conversion Circuitry
- Low Voltage: V_{CC} = 2.0 to 6.0 Vdc
- Low Drain Current (Typical 3.6 mA with V_{CC} = 3.0 Vdc)
- Excellent Sensitivity: – 3.0 dB Input Limiting = 0.7 µV
- Externally Adjustable Carrier Detect Function
- Separate Data Shaping Output Circuitry
- Data Rate Up to 35000 Baud Detectable
- 60 dB RSSI Range
- Low Number of External Parts Required
- Manufactured in Motorola's MOSAIC® Process Technology
- MC13135 is Preferred for New Designs

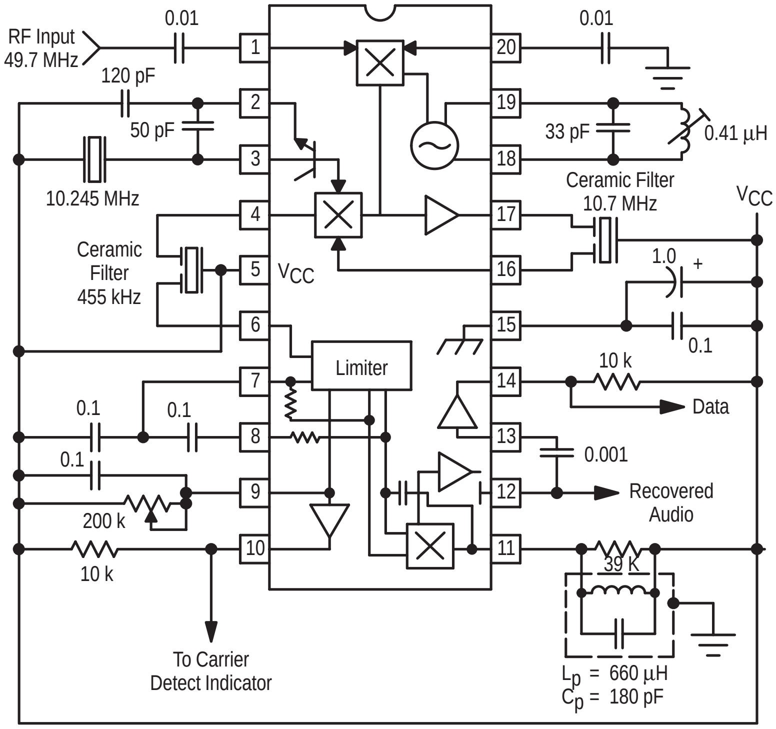


P SUFFIX
PLASTIC PACKAGE
CASE 738

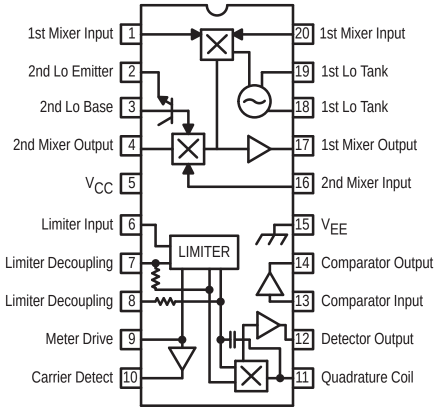
DW SUFFIX
PLASTIC PACKAGE
CASE 751D
(SO–20L)



Simplified Application as a Fixed Receiver



PIN CONNECTIONS



ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC3335DW	T_A = – 40 to +85°C	SO–20
MC3335P		Plastic DIP

MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted)

Rating	Pin	Symbol	Value	Unit
Power Supply Voltage	5	$V_{CC(max)}$	7.0	Vdc
Operating Supply Voltage Range (Recommended)	5	V_{CC}	2.0 to 6.0	Vdc
Input Voltage (V_{CC} > 5.0 Vdc)	1,20	V1–20	1.0	Vrms
Junction Temperature	–	T_J	150	°C
Operating Ambient Temperature Range	–	T_A	– 40 to + 85	°C
Storage Temperature Range	–	T_{stg}	– 65 to + 150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 Vdc, f_o = 49.7 MHz, Deviation = 3.0 kHz, T_A = 25°C, test circuit of Figure 2, unless otherwise noted.)

Characteristic	Pin	Min	Typ	Max	Unit
Drain Current	5	–	4.5	7.0	mAdc
Input for – 3.0 dB Limiting	–	–	0.7	2.0	µVrms
Recovered Audio (RF Signal Level = 1.0 mV)	12	–	250	–	mVrms
Noise Output (RF Signal Level = 0 mV)	12	–	250	–	mVrms
Carrier Detect Threshold (below V_{CC})	9	–	0.64	–	Vdc
Meter Drive Slope	9	–	100	–	µA/dB
Input for 20 dB (S + N/N)	–	–	1.3	–	µVrms
First Mixer 3rd Order Intercept (Input)	–	–	– 20	–	dBm
First Mixer Input Resistance (R_p)	–	–	690	–	Ω
First Mixer Input Capacitance (C_p)	–	–	7.2	–	pF
First Mixer Conversion Voltage Gain	–	–	18	–	dB
Second Mixer Conversion Voltage Gain	–	–	21	–	dB
Detector Output Resistance	12	–	1.4	–	kΩ

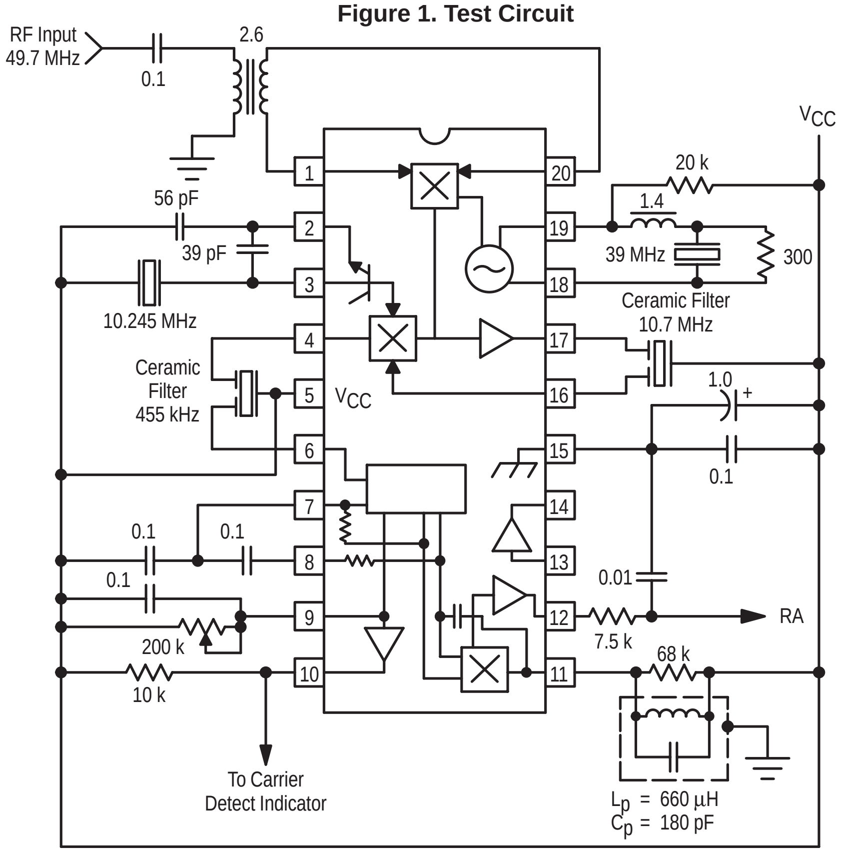


Figure 1. Test Circuit

Figure 2. I_{meter} versus Input

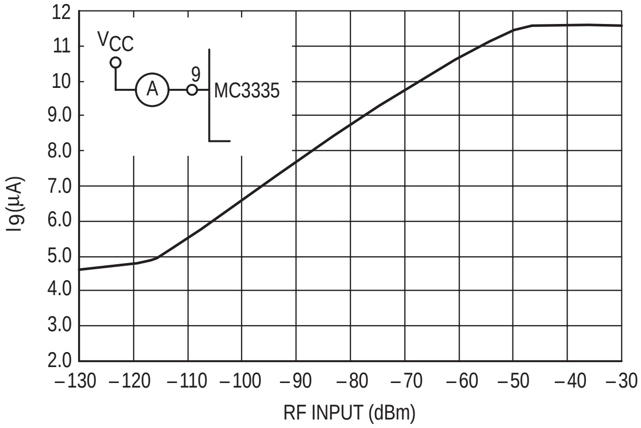


Figure 3. Drain Current, Recovered Audio versus Supply

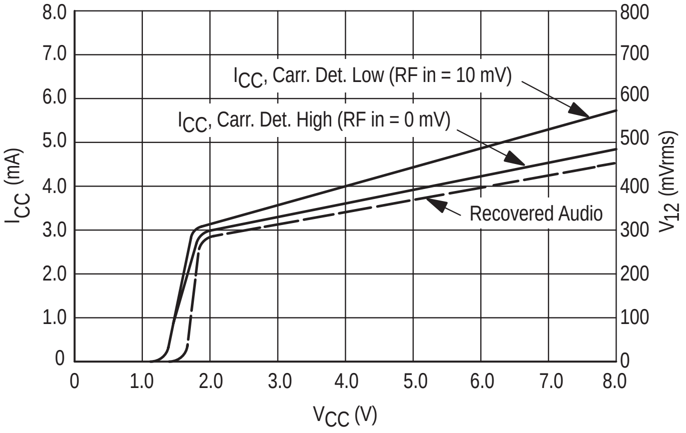


Figure 4. (S + N), N of 2nd Mixer

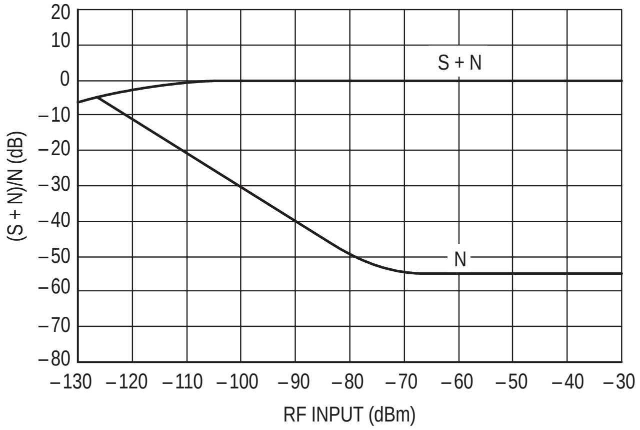


Figure 5. (S + N)/N versus Input

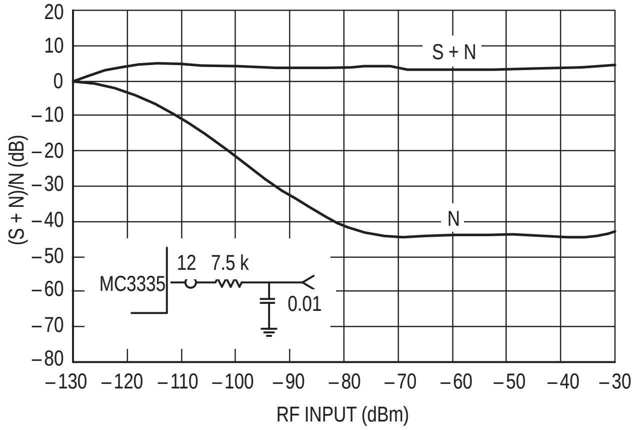


Figure 6. 1st Mixer 3rd Order Intermodulation

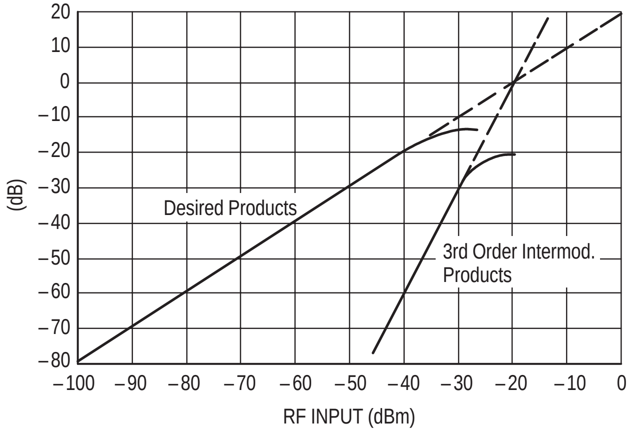
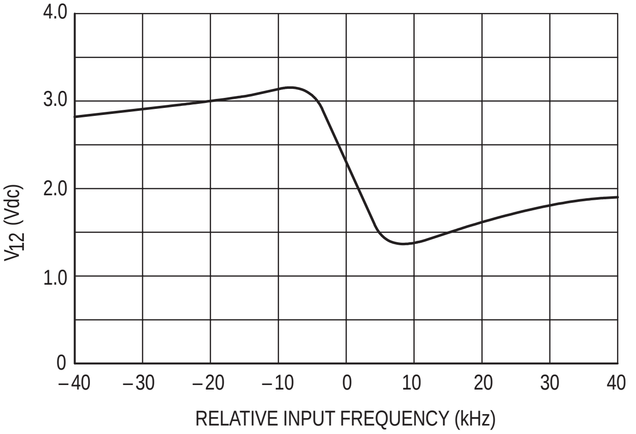


Figure 7. Detector Output versus Frequency



CIRCUIT DESCRIPTION

The MC3335 is a complete FM narrowband receiver from antenna input to audio preamp output. The low voltage dual conversion design yields low power drain, excellent sensitivity and good image rejection in narrowband voice and data link applications.

In the typical application diagram, the first mixer amplifies the signal and converts the RF input to 10.7 MHz. This IF signal is filtered externally and fed into the second mixer, which further amplifies the signal and converts it to a 455 kHz IF signal. After external bandpass filtering, the low IF is fed into the limiting amplifier and detection circuitry. The audio is recovered using a conventional quadrature detector. Twice–IF filtering is provided internally.

The input signal level is monitored by meter drive circuitry which detects the amount of limiting in the limiting amplifier. The voltage at the meter drive pin determines the state of the carrier detect output which is active low.

APPLICATIONS INFORMATION

The first local oscillator can be run using a free running LC tank, as a VCO using PLL synthesis, or driven from an external crystal oscillator. At higher V_{CC} values (6.0 to 7.0 V), it has been run to 170 MHz. The second local oscillator is a common base Colpitts type which is typically run at 10.245 MHz under crystal control.

The mixers are doubly balanced to reduce spurious responses. The first and second mixers have conversion gains of 18 dB and 22 dB (typical), respectively. Mixer gain is stable with respect to supply voltage. For both conversions, the mixer impedances and pin layout are designed to allow the user to employ low cost, readily available ceramic filters. Overall sensitivity is shown in Figure 5. The input level for 20 dB (S + N)/N is 1.3 µV using the two–pole post–detection filter as demonstrated.

Following the first mixer, a 10.7 MHz ceramic bandpass filter is recommended. The 10.7 MHz filtered signal is then fed into one second mixer input pin, the other input pin being connected to V_{CC}. Pin 5 (V_{CC}) is treated as a common point for emitter–driven signals.

The 455 kHz IF is typically filtered using a ceramic bandpass filter, then fed into the limiter input pin. The limiter has 10 µV sensitivity for – 3.0 dB limiting, flat to 1.0 MHz.

The output of the limiter is internally connected to the quadrature detector, including a quadrature capacitor. A parallel LC tank is needed externally from Pin 11 to VCC. A 39 kΩ shunt resistance is included which determines the peak separation of the quadrature detector; a smaller value will increase the spacing and linearity but decrease recovered audio and sensitivity.

A data shaping circuit is available and can be coupled to the recovered audio output of Pin 12. The circuit is a comparator which is designed to detect zero crossings of FSK modulation. Data rates of up to 35000 baud are detectable using the typical application. Hysteresis is available by connecting a high–valued resistor from Pin 13 to Pin 14. Values below 120 kΩ are not recommended as the input signal cannot overcome the hysteresis.

The meter drive circuitry detects input signal level by monitoring the limiting of the limiting amplifier stages. Figure 2 shows the unloaded current at Pin 9 versus input power. The meter drive current can be used directly (RSSI) or can be used to trip the carrier detect circuit at a specified input power. To do this, pick an RF trip level in dBm. Read the corresponding current from Figure 2 and pick a resistor such that:

$$R9 = 0.64\ \text{Vdc} / I9$$

Hysteresis is available by connecting a high–valued resistor RH between Pin 9 and 10. The formula is:

$$\text{Hysteresis} = V_{CC}/(RH \times 10^{-7})\ \text{dB}$$

MOTOROLA

MC3356

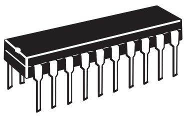
Wideband FSK Receiver

The MC3356 includes Oscillator, Mixer, Limiting IF Amplifier, Quadrature Detector, Audio Buffer, Squelch, Meter Drive, Squelch Status output, and Data Shaper comparator. The MC3356 is designed for use in digital data communciations equipment.

- Data Rates up to 500 kilobaud
- Excellent Sensitivity: – 3 dB Limiting Sensitivity
  30 µVrms @ 100 MHz
- Highly Versatile, Full Function Device, yet Few External Parts are Required
- Down Converter Can be Used Independently — Similar to NE602

WIDEBAND
FSK
RECEIVER

SEMICONDUCTOR
TECHNICAL DATA



P SUFFIX
PLASTIC PACKAGE
CASE 738

DW SUFFIX
PLASTIC PACKAGE
CASE 751D
(SO–20L)

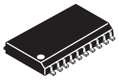
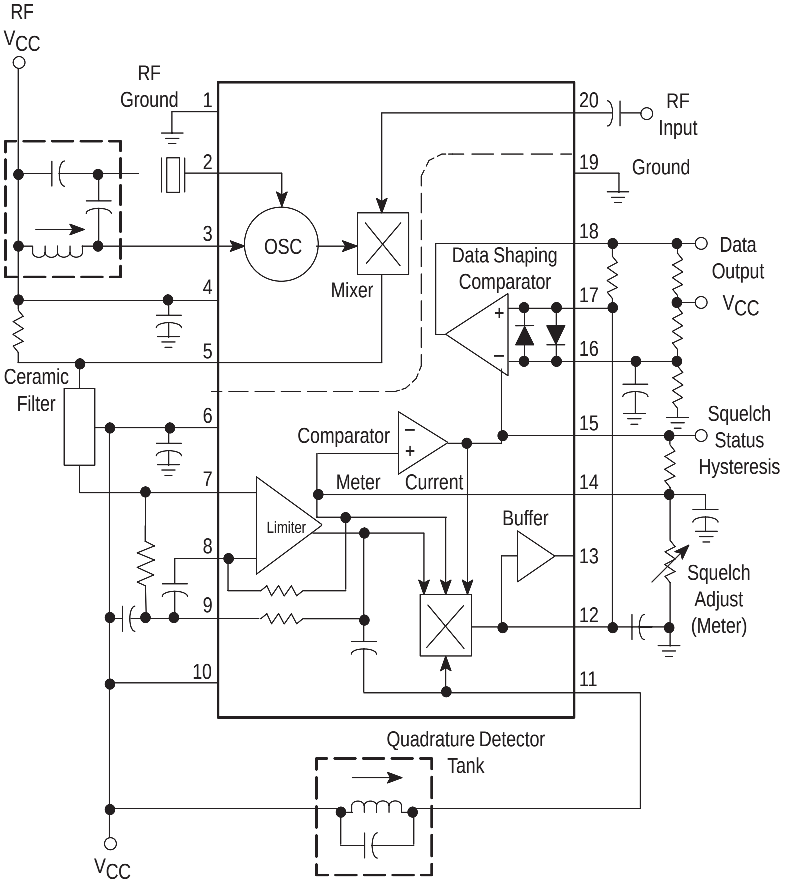
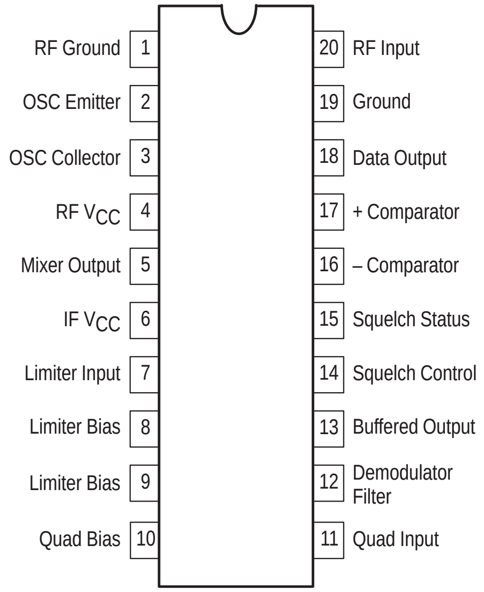


Figure 1. Representative Block Diagram



PIN CONNECTIONS



ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC3356DW	T_A = – 40 to +85°C	SO–20L
MC3356P		Plastic DIP

MAXIMUM RATINGS

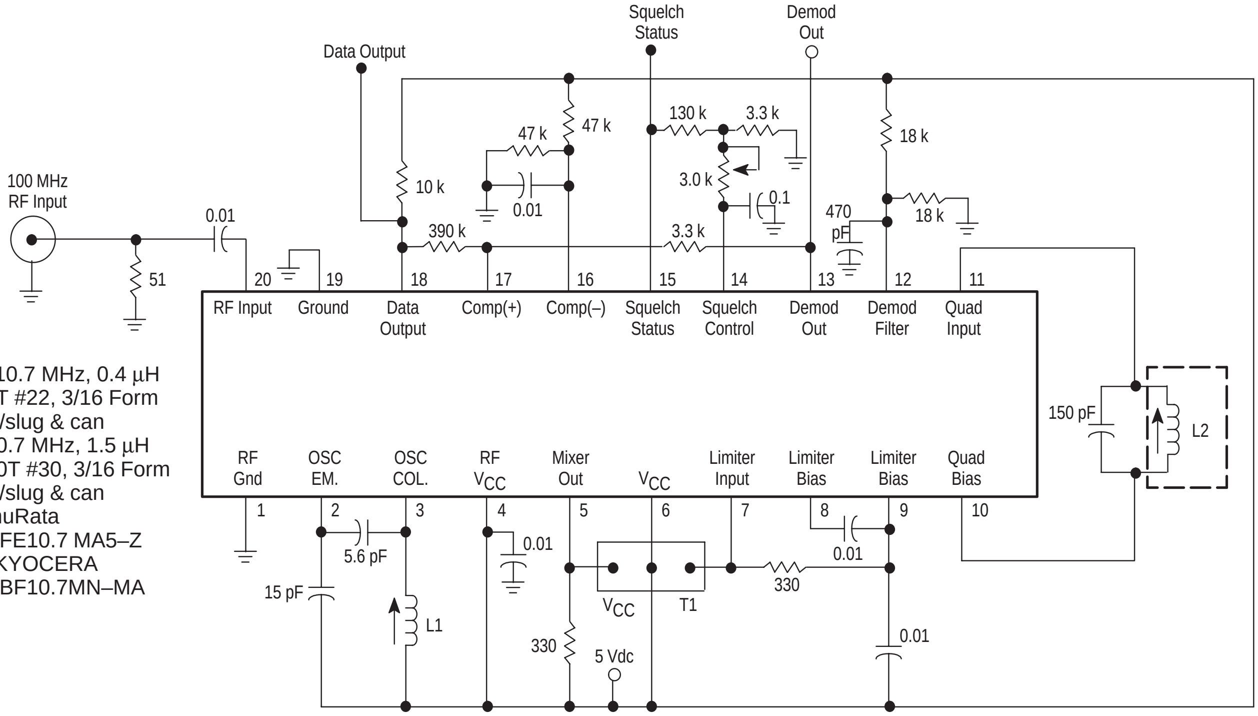
Rating	Symbol	Value	Unit
Power Supply Voltage	$V_{CC(max)}$	15	Vdc
Operating Power Supply Voltage Range (Pins 6, 10)	V_{CC}	3.0 to 9.0	Vdc
Operating RF Supply Voltage Range (Pin 4)	RF V_{CC}	3.0 to 12.0	Vdc
Junction Temperature	T_J	150	°C
Operating Ambient Temperature Range	T_A	– 40 to + 85	°C
Storage Temperature Range	T_{stg}	– 65 to + 150	°C
Power Dissipation, Package Rating	P_D	1.25	W

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 Vdc, f_o = 100 MHz, f_{osc} = 110.7 MHz, Δf = ±75 kHz, f_{mod} = 1.0 kHz, 50 Ω source, T_A = 25°C, test circuit of Figure 2, unless otherwise noted.)

Characteristics	Min	Typ	Max	Unit
Drain Current Total, RF V_{CC} and V_{CC}	–	20	25	mAdc
Input for – 3 dB limiting	–	30	–	µVrms
Input for 50 dB quieting $\left(\frac{S+N}{N}\right)$	–	60	–	µVrms
Mixer Voltage Gain, Pin 20 to Pin 5	2.5	–	–	
Mixer Input Resistance, 100 MHz	–	260	–	Ω
Mixer Input Capacitance, 100 MHz	–	5.0	–	pF
Mixer/Oscillator Frequency Range (Note 1)	–	0.2 to 150	–	MHz
IF/Quadrature Detector Frequency Range (Note 1)	–	0.2 to 50	–	MHz
AM Rejection (30% AM, RF V_{in} = 1.0 mVrms)	–	50	–	dB
Demodulator Output, Pin 13	–	0.5	–	Vrms
Meter Drive	–	7.0	–	µA/dB
Squelch Threshold	–	0.8	–	Vdc

NOTE: 1. Not taken in Test Circuit of Figure 2; new component values required.

Figure 2. Test Circuit



L1 – 110.7 MHz, 0.4 µH
7T #22, 3/16 Form
w/slug & can
L2 – 10.7 MHz, 1.5 µH
20T #30, 3/16 Form
w/slug & can
T1 – muRata
SFE10.7 MA5–Z
or KYOCERA
KBF10.7MN–MA

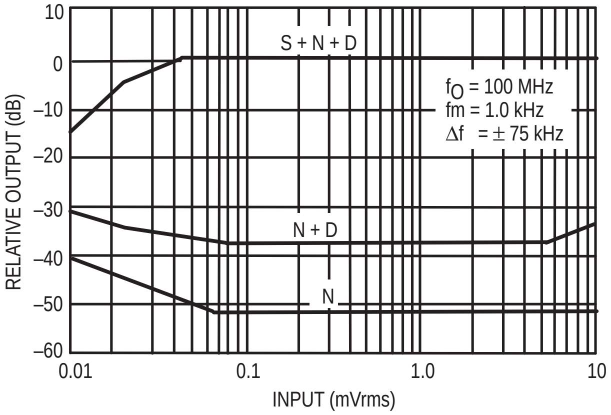


Figure 3. Output Components of Signal, Noise, and Distortion

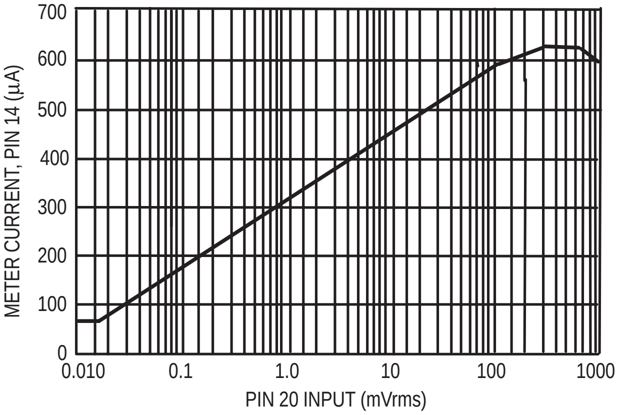


Figure 4. Meter Current versus Signal Input

GENERAL DESCRIPTION

This device is intended for single and double conversion VHF receiver systems, primarily for FSK data transmission up to 500 K baud (250 kHz). It contains an oscillator, mixer, limiting IF, quadrature detector, signal strength meter drive, and data shaping amplifier.

The oscillator is a common base Colpitts type which can be crystal controlled, as shown in Figure 1, or L–C controlled as shown in the other figures. At higher V_{CC}, it has been operated as high as 200 MHz. A mixer/oscillator voltage gain of 2 up to approximately 150 MHz, is readily achievable.

The mixer functions well from an input signal of 10 µVrms, below which the squelch is unpredictable, up to about 10 mVrms, before any evidence of overload. Operation up to 1.0 Vrms input is permitted, but non–linearity of the meter output is incurred, and some oscillator pulling is suspected. The AM rejection above 10 mVrms is degraded.

The limiting IF is a high frequency type, capable of being operated up to 50 MHz. It is expected to be used at 10.7 MHz in most cases, due to the availability of standard ceramic resonators. The quadrature detector is internally coupled to the IF, and a 5.0 pF quadrature capacitor is internally provided. The –3dB limiting sensitivity of the IF itself is approximately 50 µV (at Pin 7), and the IF can accept signals up to 1.0 Vrms without distortion or change of detector quiescent dc level.

The IF is unusual in that each of the last 5 stages of the 6 state limiter contains a signal strength sensitive, current sinking device. These are parallel connected and buffered to produce a signal strength meter drive which is fairly linear for IF input signals of 10 µV to 100 mVrms (see Figure 4).

A simple squelch arrangement is provided whereby the meter current flowing through the meter load resistance flips a comparator at about 0.8 Vdc above ground. The signal strength at which this occurs can be adjusted by changing the meter load resistor. The comparator (+) input and output are available to permit control of hysteresis. Good positive action can be obtained for IF input signals of above 30 µVrms. The 130 kΩ resistor shown in the test circuit provides a small amount of hysteresis. Its connection between the 3.3 k resistor to ground and the 3.0 k pot, permits adjustment of squelch level without changing the amount of hysteresis.

The squelch is internally connected to both the quadrature detector and the data shaper. The quadrature detector output, when squelched, goes to a dc level approximately equal to the zero signal level unsquelched. The squelch causes the data shaper to produce a high (V_{CC}) output.

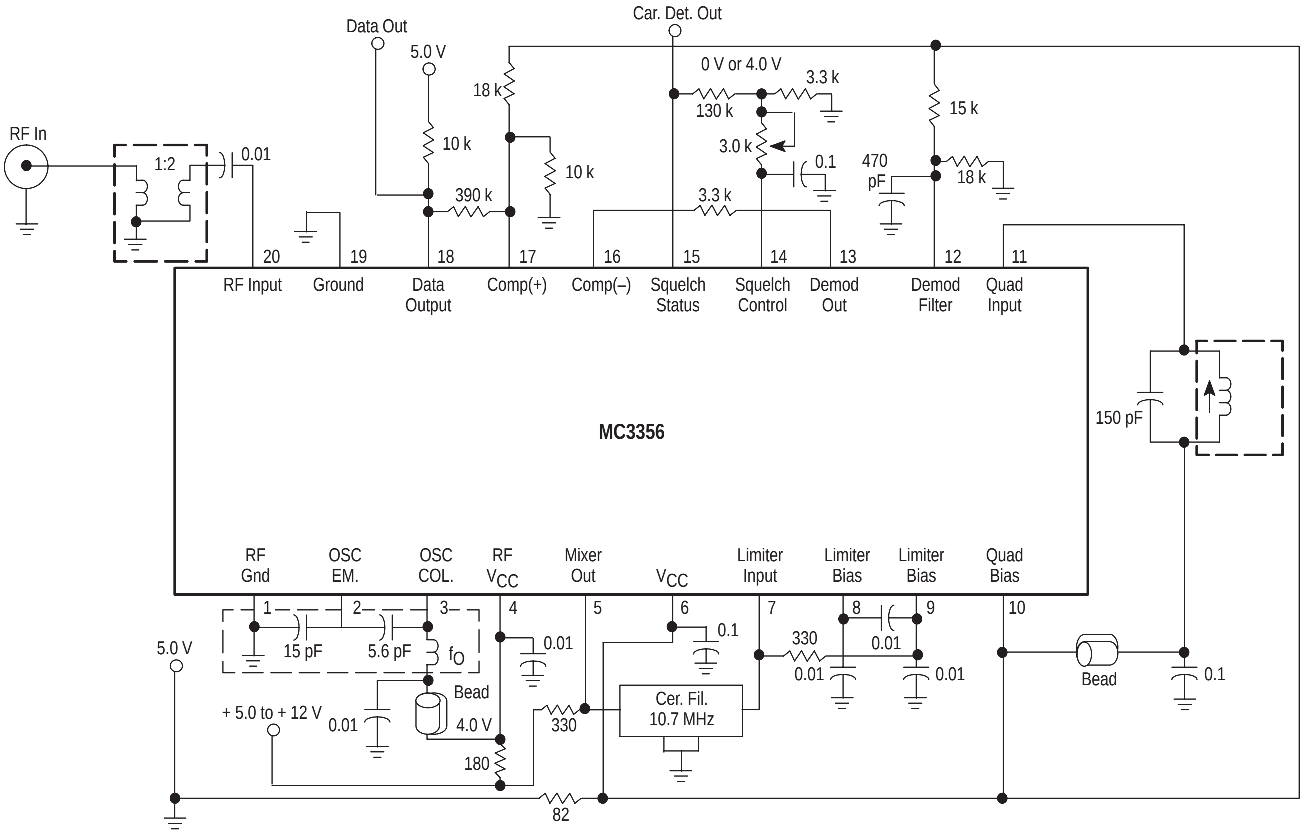
The data shaper is a complete ‘‘floating’’ comparator, with back to back diodes across its inputs. The output of the quadrature detector can be fed directly to either input of this amplifier to produce an output that is either at V_{CC} or V_{EE}, depending upon the received frequency. The impedance of the biasing can be varied to produce an amplifier which “follows” frequency detuning to some degree, to prevent data pulse width changes.

When the data shaper is driven directly from the demodulator output, Pin 13, there may be distortion at Pin 13 due to the diodes, but this is not important in the data application. A useful note in relating high/low input frequency to logic state: low IF frequency corresponds to low demodulator output. If the oscillator is above the incoming RF frequency, then high RF frequency will produce a logic low (input to (+) input of Data Shaper as shown in Figures 1 and 2).

APPLICATION NOTES

The MC3356 is a high frequency/high gain receiver that requires following certain layout techniques in designing a stable circuit configuration. The objective is to minimize or eliminate, if possible, any unwanted feedback.

Figure 5. Application with Fixed Bias on Data Shaper



APPLICATION NOTES (continued)

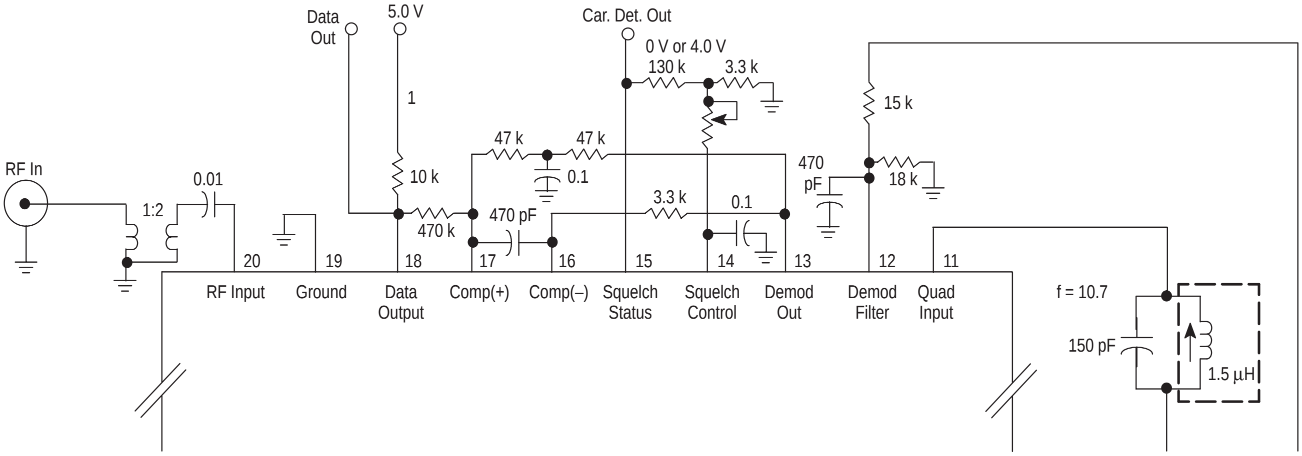
Shielding, which includes the placement of input and output components, is important in minimizing electrostatic or electromagnetic coupling. The MC3356 has its pin connections such that the circuit designer can place the critical input and output circuits on opposite ends of the chip. Shielding is normally required for inductors in tuned circuits.

The MC3356 has a separate V_{CC} and ground for the RF and IF sections which allows good external circuit isolation by minimizing common ground paths.

Note that the circuits of Figures 1 and 2 have RF, Oscillator, and IF circuits predominantly referenced to the plus supply rails. Figure 5, on the other hand, shows a suitable means of ground referencing. The two methods produce identical results when carefully executed. It is important to treat Pin 19 as a ground node for either approach. The RF input should be “grounded” to Pin 1 and then the input and the mixer/oscillator grounds (or RF V_{CC} bypasses) should be connected by a low inductance path to Pin 19. IF and detector sections should also have their bypasses returned by a **separate** path to Pin 19. V_{CC} and RF V_{CC} can be decoupled to minimize feedback, although the configuration of Figure 2 shows a successful implementation on a common 5.0 V supply. Once again, the message is: define a supply node and a ground node and return each section to those nodes by separate, low impedance paths.

The test circuit of Figure 2 has a 3 dB limiting level of 30 µV which can be lowered 6 db by a 1:2 untuned transformer at the input as shown in Figures 5 and 6. For applications that require additional sensitivity, an RF amplifier can be added, but with no greater than 20 db gain. This will give a 2.0 to 2.5 µV sensitivity and any additional gain will reduce receiver dynamic range without improving its sensitivity. Although the test circuit operates at 5.0 V, the mixer/oscillator optimum performance is at 8.0 V to 12 V. A minimum of 8.0 V is recommended in high frequency applications (above 150 MHz), or in PLL applications where the oscillator drives a prescaler.

Figure 6. Application with Self–Adjusting Bias on Data Shaper



APPLICATION NOTES (continued)

Depending on the external circuit, inverted or noninverted data is available at Pin 18. Inverted data makes the higher frequency in the FSK signal a "one" when the local oscillator is above the incoming RF. Figure 5 schematic shows the comparator with hysteresis. In this circuit the dc reference voltage at Pin 17 is about the same as the demodulated output voltage (Pin 13) when no signal is present. This type circuit is preferred for systems where the data rates can drop to zero. Some systems have a low frequency limit on the data rate, such as systems using the MC3850 ACIA that has a start or stop bit. This defines the low frequency limit that can appear in the data stream. Figure 5 circuit can then be changed to a circuit configuration as shown in Figure 6. In Figure 6 the reference voltage for the comparator is derived from the demodulator output through a low pass circuit where τ is much lower than the lowest frequency data rate. This and similar circuits will compensate for small tuning changes (or drift) in the quadrature detector.

Squelch status (Pin 15) goes high (squelch off) when the input signal becomes greater than some preset level set by the resistance between Pin 14 and ground. Hysteresis is added to the circuit externally by the resistance from Pin 14 to Pin 15.

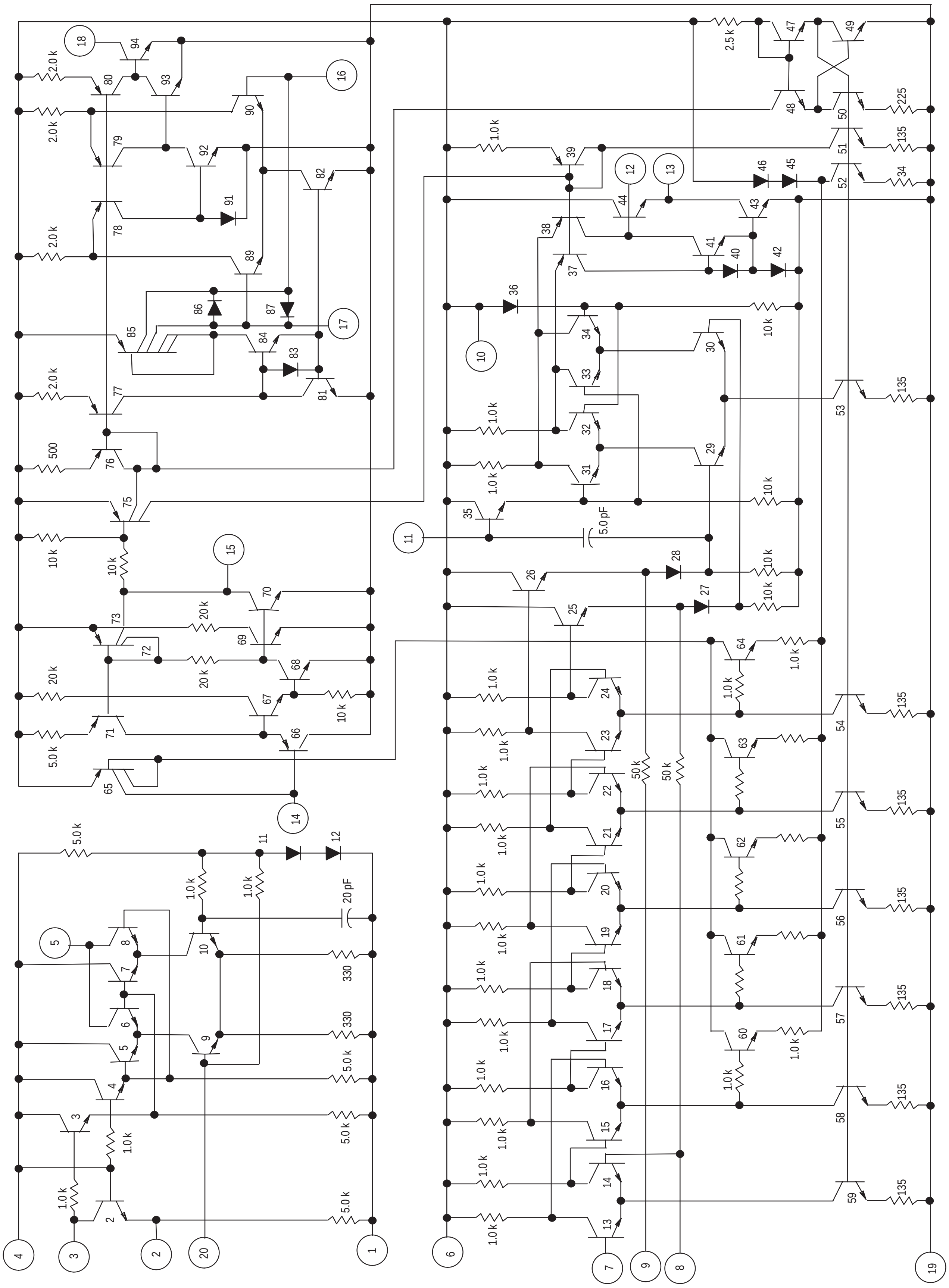


Figure 7. Internal Schematic

MOTOROLA

MC3357

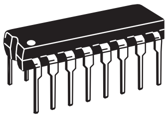
Low Power Narrowband FM IF

. . . includes Oscillator, Mixer, Limiting Amplifier, Quadrature Discriminator, Active Filter, Squelch, Scan Control, and Mute Switch. The MC3357 is designed for use in FM dual conversion communications equipment.

- Low Drain Current (3.0 mA (Typical) @ V_{CC} = 6.0 Vdc)
- Excellent Sensitivity: Input Limiting Voltage – (– 3.0 dB) = 5.0 µV (Typical)
- Low Number of External Parts Required
- Recommend MC3372 for Replacement/Upgrade

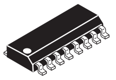
LOW POWER FM IF

SEMICONDUCTOR TECHNICAL DATA



P SUFFIX
PLASTIC PACKAGE
CASE 648

D SUFFIX
PLASTIC PACKAGE
CASE 751B
(SO–16)



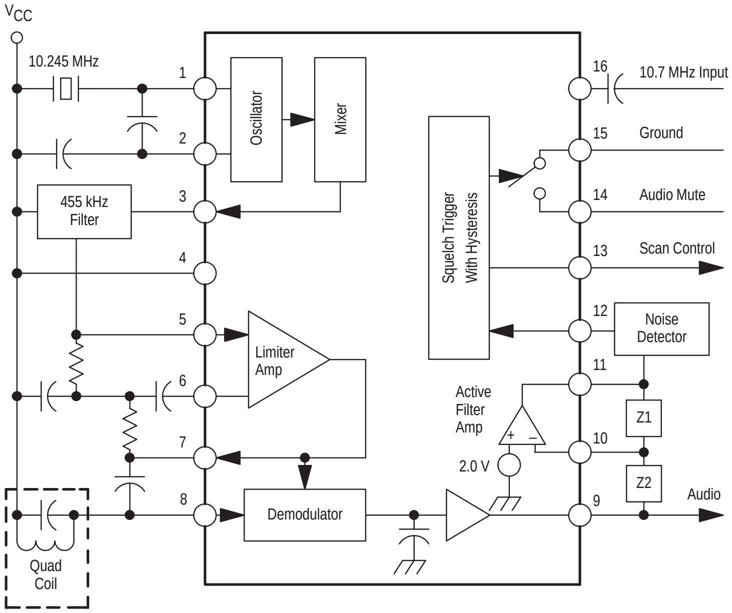
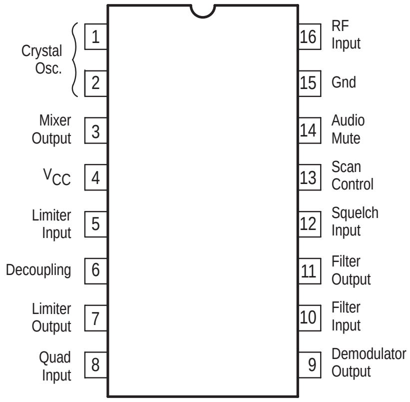


Figure 1. Representative Block Diagram

PIN CONNECTIONS



ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC3357D	T_A = – 30 to +70°C	SO–16
MC3357P		Plastic DIP

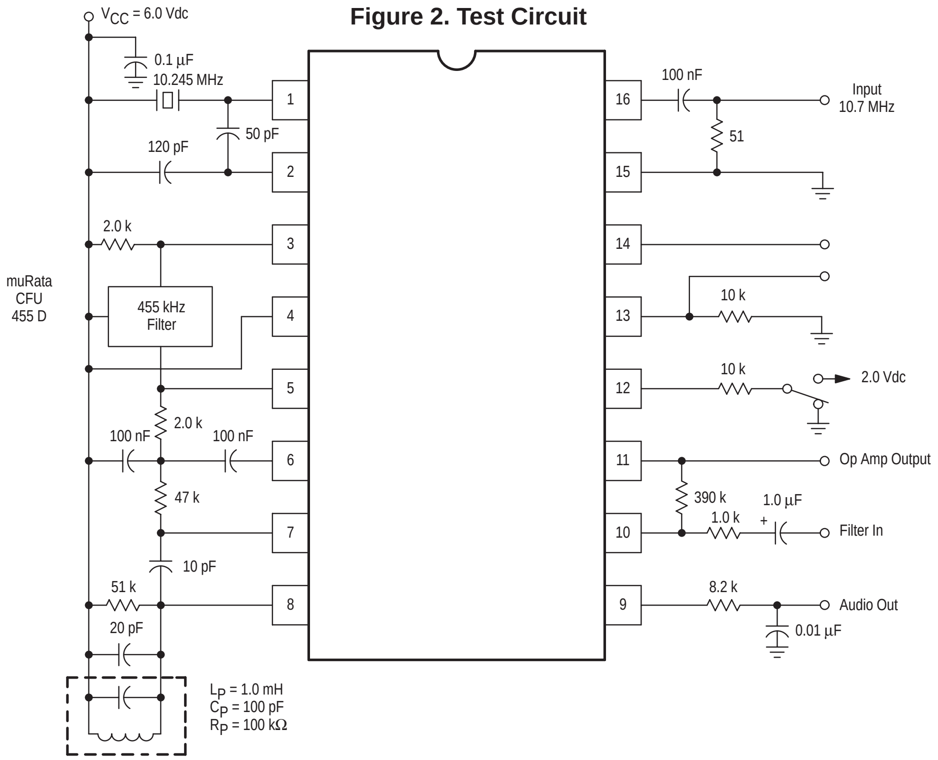
MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted)

Rating	Pin	Symbol	Value	Unit
Power Supply Voltage	4	V_{CC}(max)	12	Vdc
Operating Supply Voltage Range	4	V_{CC}	4 to 8	Vdc
Detector Input Voltage	8	–	1.0	Vp–p
Input Voltage ($V_{CC} \geqslant$ 6.0 Volts)	16	V_{16}	1.0	V_{RMS}
Mute Function	14	V_{14}	–0.5 to 5.0	V_{pk}
Junction Temperature	–	T_J	150	°C
Operating Ambient Temperature Range	–	T_A	– 30 to + 70	°C
Storage Temperature Range	–	T_{stg}	– 65 to + 150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 6.0 Vdc, fo = 10.7 MHz, $\Delta f = \pm$ 3.0 kHz, f_{mod} = 1.0 kHz, T_A = 25°C, unless otherwise noted.)

Characteristic	Pin	Min	Typ	Max	Unit
Drain Current Squelch Off Squelch On	4	– –	2.0 3.0	– 5.0	mA
Input Limiting Voltage (– 3 dB Limiting)	16	–	5.0	10	µV
Detector Output Voltage	9	–	3.0	–	Vdc
Detector Output Impedance	–	–	400	–	Ω
Recovered Audio Output Voltage (V_{in} = 10 mV)	9	200	350	–	mVrms
Filter Gain (10 kHz) (V_{in} = 5 mV)	–	40	46	–	dB
Filter Output Voltage	11	1.8	2.0	2.5	Vdc
Trigger Hysteresis	–	–	100	–	mV
Mute Function Low	14	–	15	50	Ω
Mute Function High	14	1.0	10	–	MΩ
Scan Function Low (Mute Off) (V_{12} = 2 Vdc)	13	–	0	0.5	Vdc
Scan Function High (Mute On) (V_{12} = Gnd)	13	5.0	–	–	Vdc
Mixer Conversion Gain	3	–	20	–	dB
Mixer Input Resistance	16	–	3.3	–	kΩ
Mixer Input Capacitance	16	–	2.2	–	pF

Figure 2. Test Circuit



CIRCUIT DESCRIPTION

The MC3357 is a low power FM IF circuit designed primarily for use in voice communication scanning receivers.

The mixer–oscillator combination converts the input frequency (e.g., 10.7 MHz) down to 455 kHz, where, after external bandpass filtering, most of the amplification is done. The audio is recovered using a conventional quadrature FM detector. The absence of an input signal is indicated by the presence of noise above the desired audio frequencies. This “noise band” is monitored by an active filter and a detector. A squelch trigger circuit indicates the presence of a noise (or a tone) by an output which can be used to control scanning. At the same time, an internal switch is operated which can be used to mute the audio.

The oscillator is an internally–biased Colpitts type with the collector, base, and emitter connections at Pins 4, 1, and 2 respectively. A crystal can be used in place of the usual coil.

The mixer is doubly–balanced to reduce spurious responses. The input impedance at Pin 16 is set by a 3.0 kΩ internal biasing resistor and has low capacitance, allowing the circuit to be preceded by a crystal filter. The collector output at Pin 3 must be dc connected to B +, below which it can swing 0.5 V.

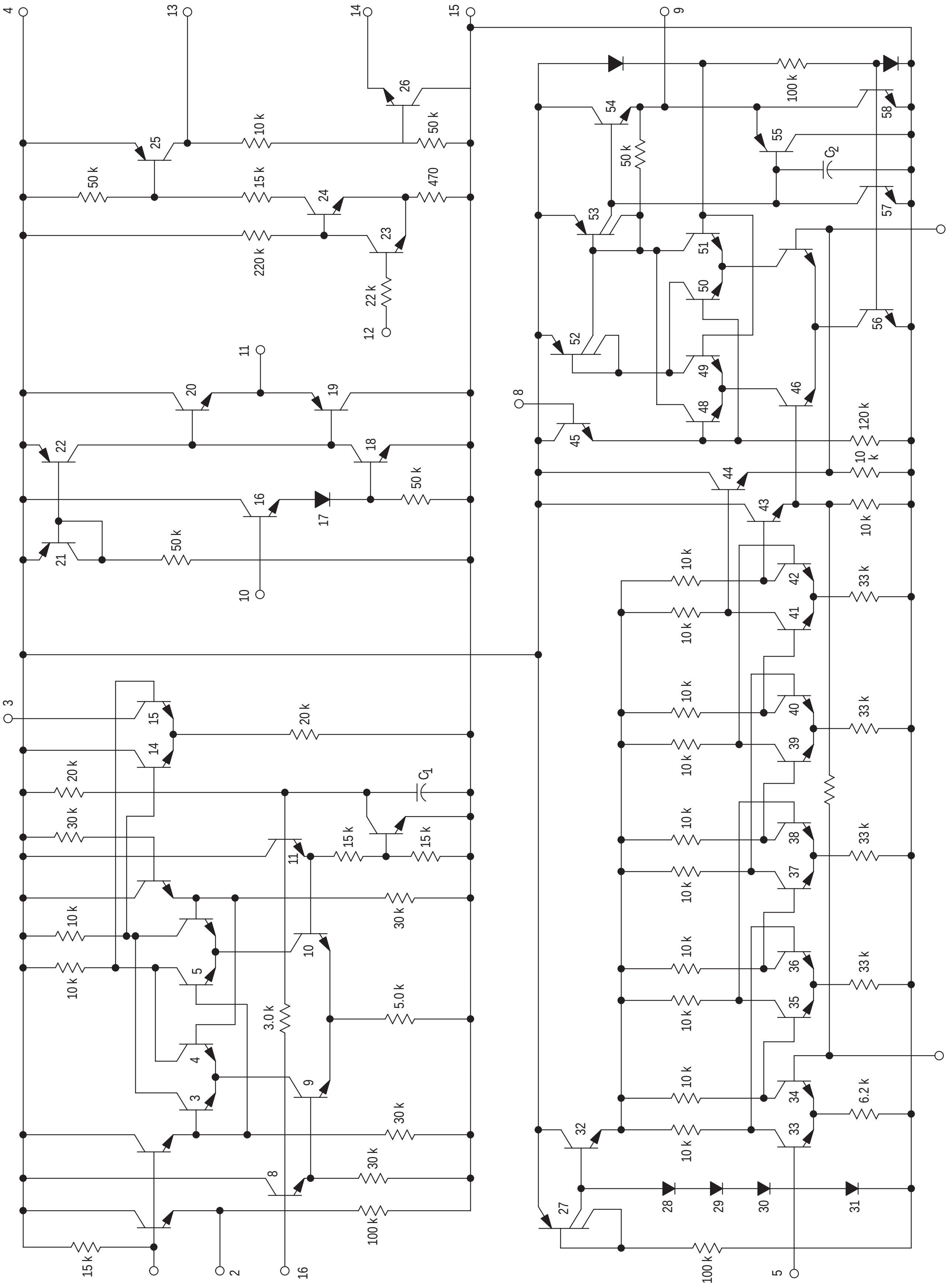
After suitable bandpass filtering (ceramic or LC), the signal goes to the input of a five–stage limiter at Pin 5. The output of the limiter at Pin 7 drives a multiplier, both internally directly, and externally through a quadrature coil, to detect the FM. The output at Pin 7 is also used to supply dc feedback to Pin 5. The other side of the first limiter stage is decoupled at Pin 6.

The recovered audio is partially filtered, then buffered, giving an impedance of around 400 Ω at Pin 9. The signal still requires de–emphasis, volume control and further amplification before driving a loudspeaker.

A simple inverting op amp is provided with an output at Pin 11 providing dc bias (externally) to the input at Pin 10 which is referred internally to 2.0 V. A filter can be made with external impedance elements to discriminate between frequencies. With an external AM detector, the filtered audio signal can be checked for the presence of noise above the normal audio band, or a tone signal. This information is applied to Pin 12.

An external positive bias to Pin 12 sets up the squelch trigger circuit such that Pin 13 is low at an impedance level of around 60 kΩ, and the audio mute (Pin 14) is open circuit. If Pin 12 is pulled down to 0.7 V by the noise or tone detector, Pin 13 will rise to approximately 0.5 Vdc below supply where it can support a load current of around 500 µA and Pin 14 is internally short–circuited to ground. There is 100 mV of hysteresis at Pin 12 to prevent jitter. Audio muting is accomplished by connecting Pin 14 to a high–impedance ground–reference point in the audio path between Pin 9 and the audio amplifier.

Figure 3. Circuit Schematic



MOTOROLA

MC3359

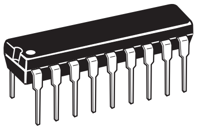
Low Power Narrowband FM IF

. . . includes oscillator, mixer, limiting amplifier, AFC, quadrature discriminator, op/amp, squelch, scan control, and mute switch. The MC3359 is designed to detect narrowband FM signals using a 455 kHz ceramic filter for use in FM dual conversion communications equipment. The MC3359 is similar to the MC3357 except that the MC3359 has an additional limiting IF stage, an AFC output, and an opposite polarity Broadcast Detector. The MC3359 also requires fewer external parts. For low cost applications requiring V_{CC} below 6.0 V, the MC3361BP,BD are recommended. For applications requiring a fixed, tuned, ceramic quadrature resonator, use the MC3357. For applications requiring dual conversion and RSSI, refer to these devices; MC3335, MC3362 and MC3363.

- Low Drain Current: 3.6 mA (Typical) @ V_{CC} = 6.0 Vdc
- Excellent Sensitivity: Input Limiting Voltage –
  – 3.0 dB = 2.0 µV (Typical)
- Low Number of External Parts Required
- For Low Voltage and RSSI, use the MC3371

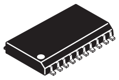
HIGH GAIN
LOW POWER
FM IF

SEMICONDUCTOR
TECHNICAL DATA



P SUFFIX
PLASTIC PACKAGE
CASE 707

DW SUFFIX
PLASTIC PACKAGE
CASE 751D
(SO–20L)



ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC3359DW	T_A = –30 to +70°C	SO–20L
MC3359P		Plastic DIP

Figure 1. Simplified Application in a Scanner Receiver

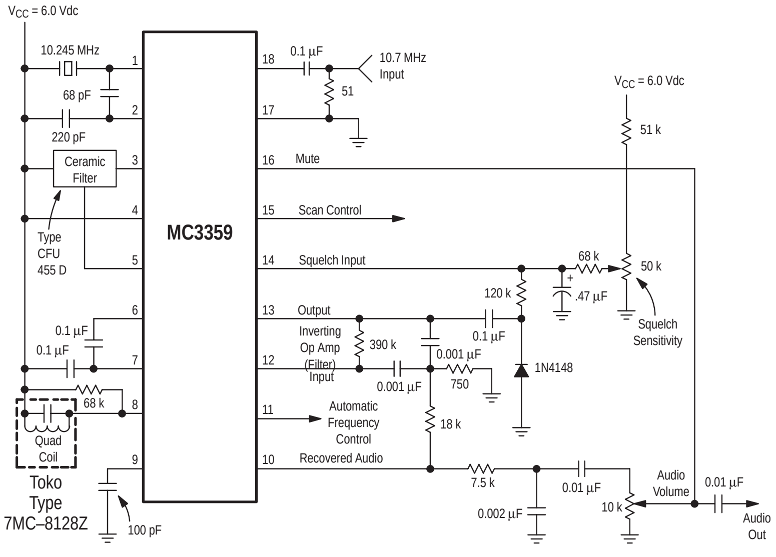
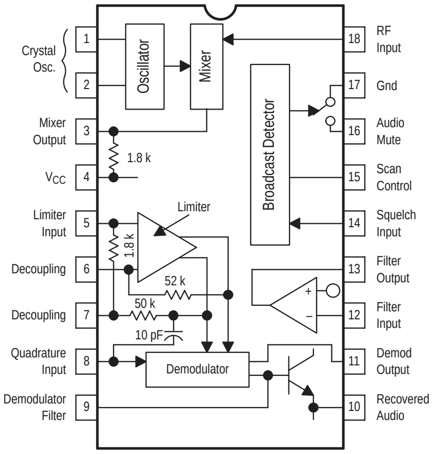
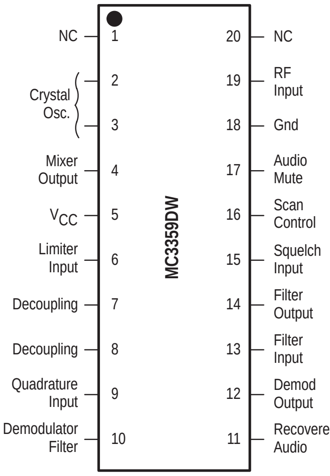


Figure 2. Pin Connections and Functional Block Diagram



CASE 707



CASE 751D

MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted)

Rating	Pin	Symbol	Value	Unit
Power Supply Voltage	4	V_{CC}(max)	12	Vdc
Operating Supply Voltage Range	4	V_{CC}	6 to 9	Vdc
Input Voltage ($V_{CC} \geqslant$ 6.0 Volts)	18	V_{18}	1.0	V_{rms}
Mute Function	16	V_{16}	– 0.7 to 12	V_{pk}
Junction Temperature	–	T_J	150	°C
Operating Ambient Temperature Range	–	T_A	– 30 to + 70	°C
Storage Temperature Range	–	T_{stg}	– 65 to + 150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 6.0 Vdc, f_o = 10.7 MHz, Δf = ± 3.0 kHz, f_{mod} = 1.0 kHz, 50 Ω source, T_A = 25°C test circuit of Figure 3, unless otherwise noted)

Characteristics	Min	Typ	Max	Units
Drain Current (Pins 4 and 8) Squelch Off Squelch On	– –	3.6 5.4	6.0 7.0	mA
Input for 20 dB Quieting	–	8.0	–	μVrms
Input for – 3.0 dB Limiting	–	2.0	–	μVrms
Mixer Voltage Gain (Pin 18 to Pin 3, Open)	–	46	–	
Mixer Third Order Intercept, 50 Ω Input	–	– 1.0	–	dBm
Mixer Input Resistance	–	3.6	–	kΩ
Mixer Input Capacitance	–	2.2	–	pF
Recovered Audio, Pin 10 (Input Signal 1.0 mVrms)	450	700	–	mVrms
Detector Center Frequency Slope, Pin 10	–	0.3	–	V/kHz
AFC Center Slope, Pin 11, Unloaded	–	12	–	V/kHz
Filter Gain (test circuit of Figure 3)	40	51	–	dB
Squelch Threshold, Through 10K to Pin 14	–	0.62	–	Vdc
Scan Control Current, Pin 15 Pin 14 – High – Low	– 2.0	0.01 2.4	1.0 –	μA mA
Mute Switch Impedance Pin 16 to Ground Pin 14 – High – Low	–	5.0 1.5	10 –	Ω MΩ

Figure 3. Test Circuit

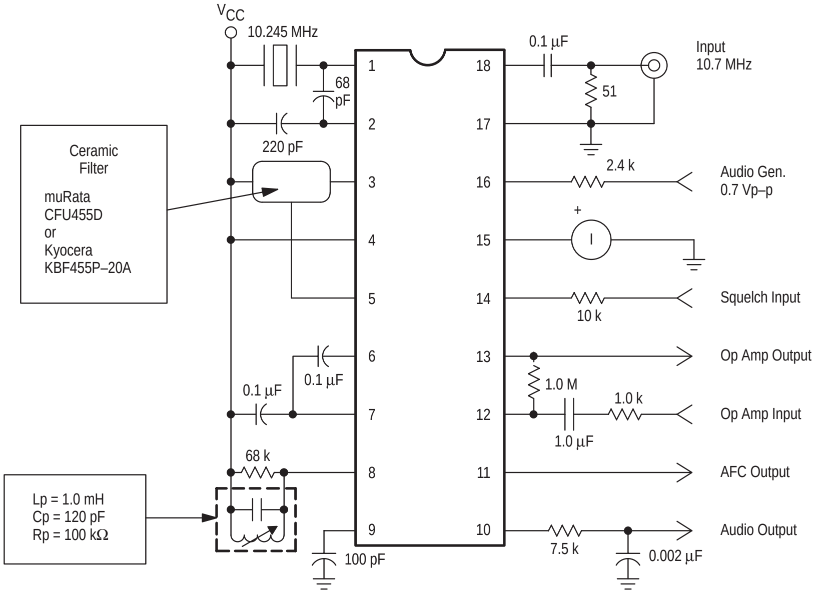


Figure 4. Mixer Voltage Gain

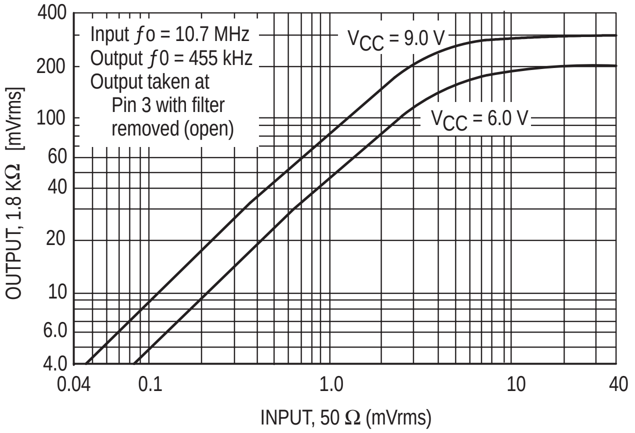


Figure 5. Limiting IF Frequency Response

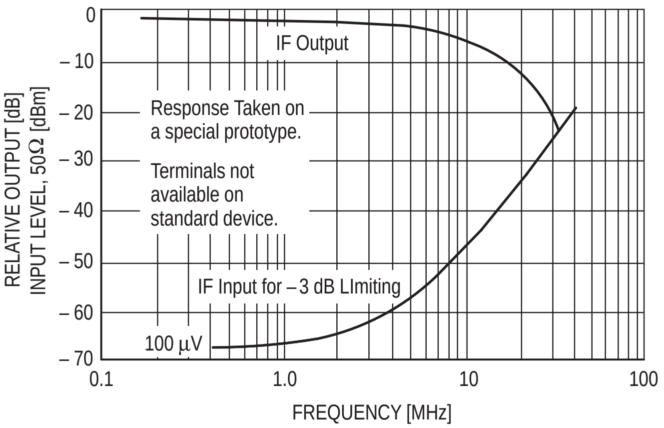


Figure 6. Mixer Third Order Intermodulation Performance

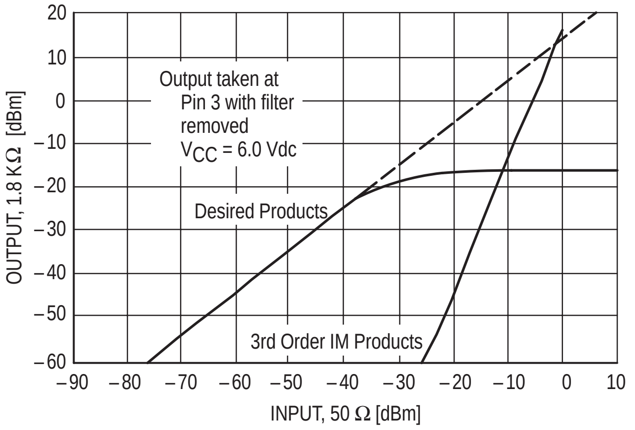


Figure 7. Detector and AFC Responses

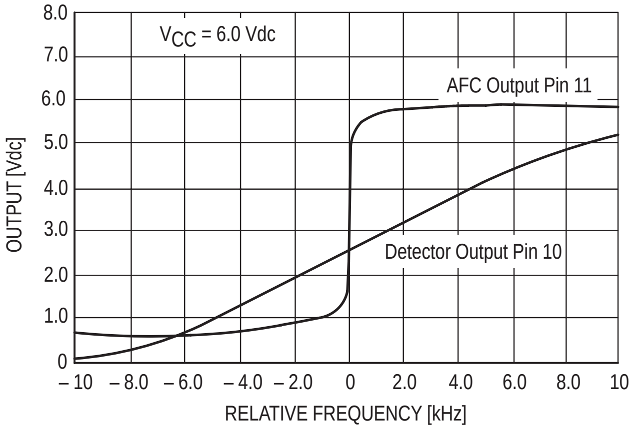


Figure 8. Relative Mixer Gain

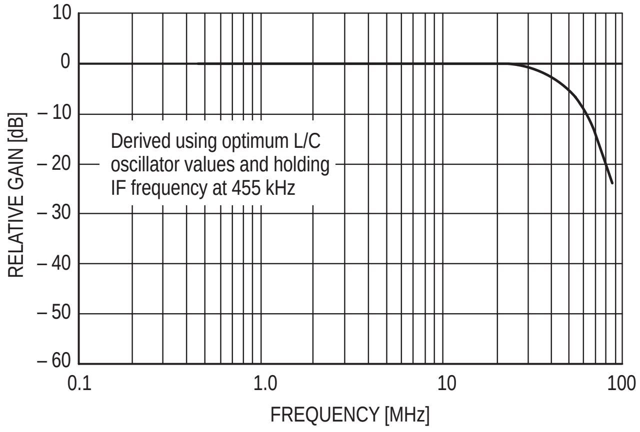


Figure 9. Overall Gain, Noise, and AM Rejection

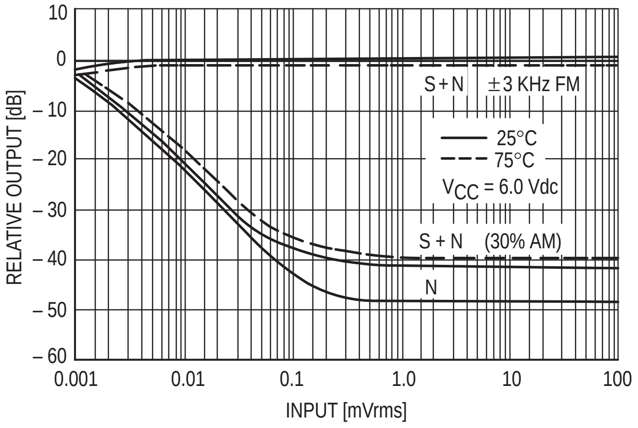


Figure 10. Output Components of Signal, Noise, and Distortion

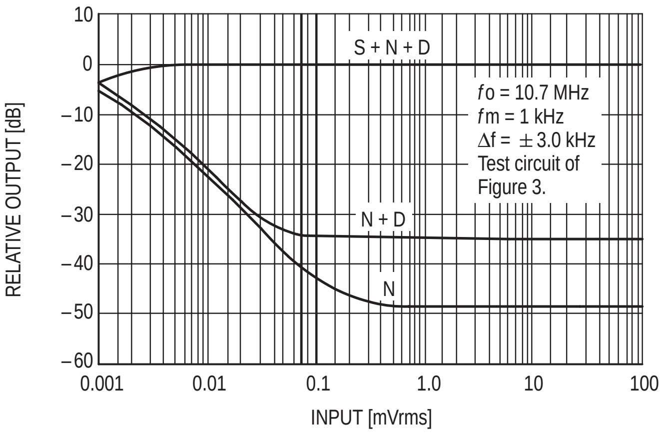


Figure 11. Audio Output and Total Current Drain versus Supply Voltage

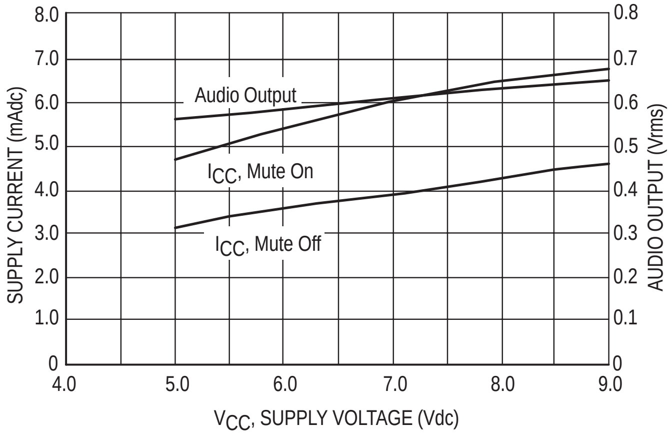


Figure 12. L/C Oscillator, Temperature and Power Supply Sensitivity

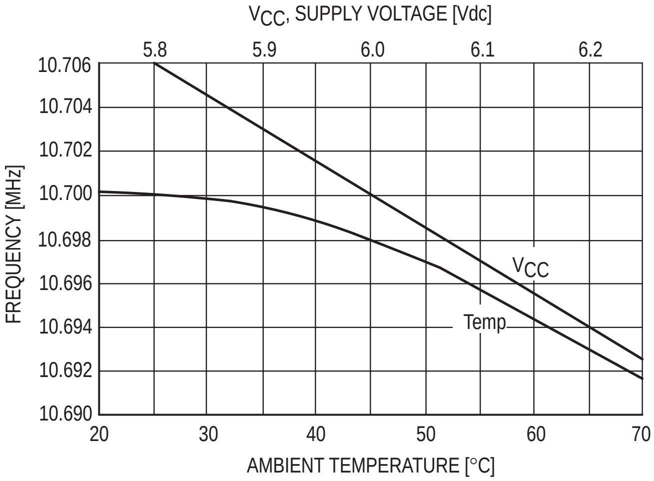


Figure 13. Op Amp Gain and Phase Response

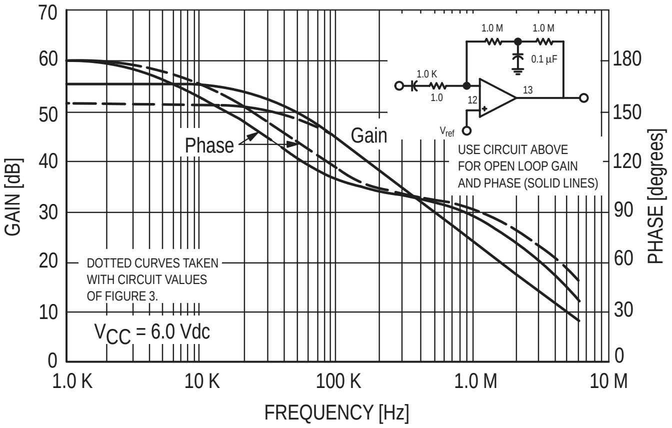


Figure 14. L/C Oscillator Recommended Component Values

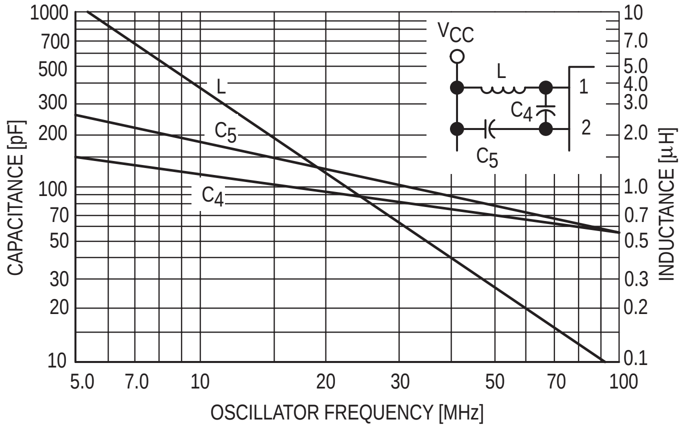
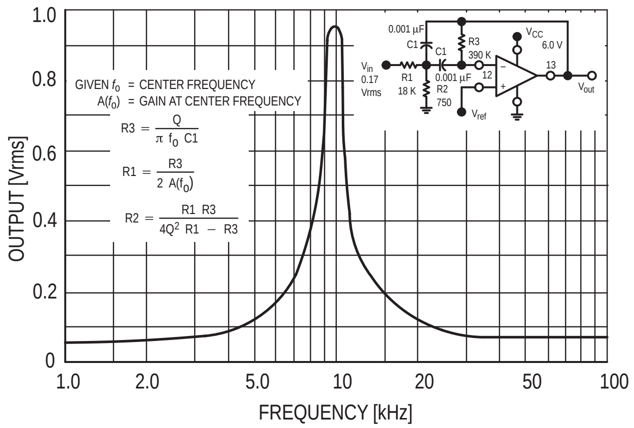


Figure 15. The Op Amp as a Bandpass Filter



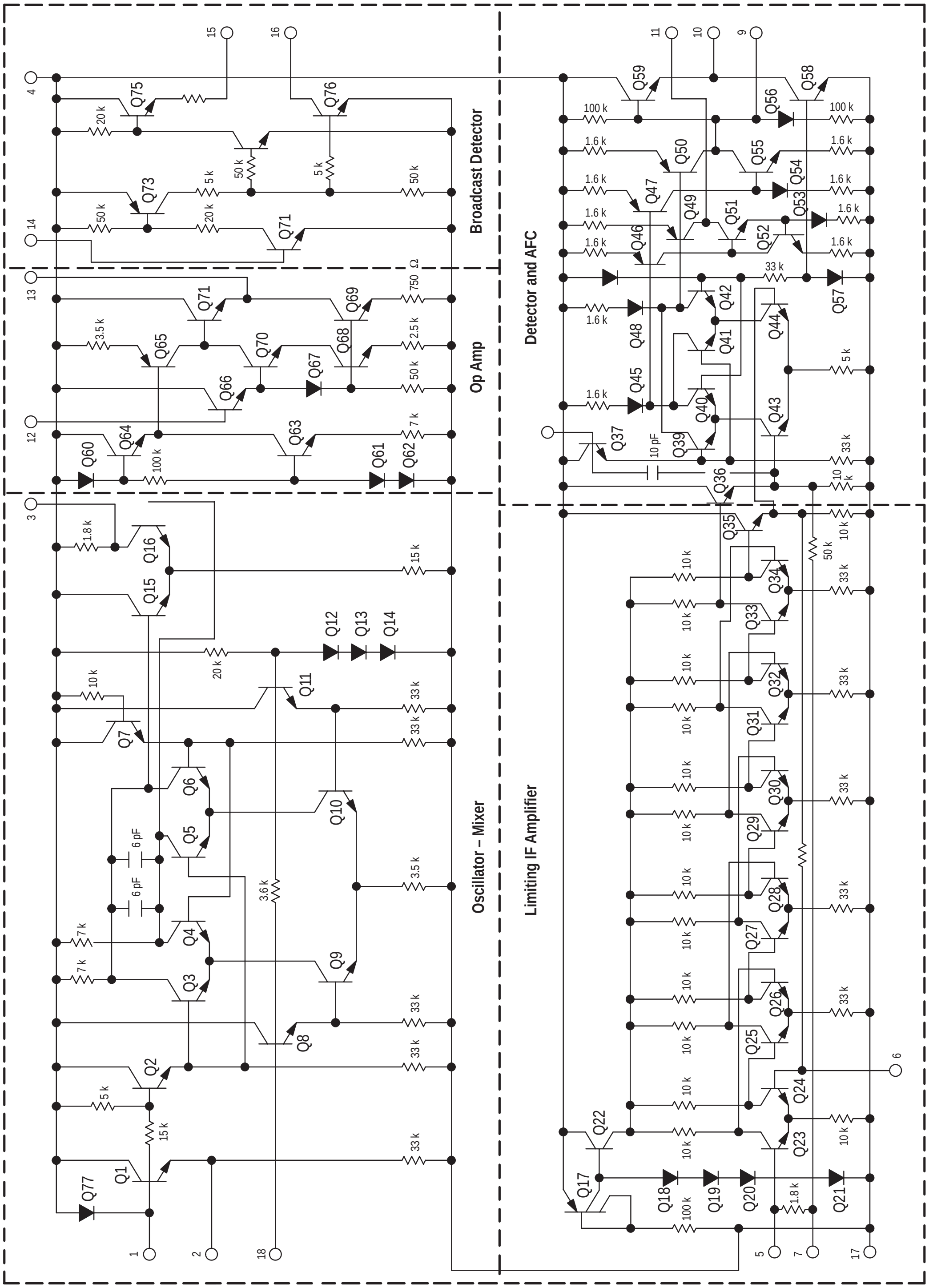


Figure 16. Representative Schematic Diagram

CIRCUIT DESCRIPTION

The MC3359 is a low–power FM IF circuit designed primarily for use in voice–communication scanning receivers. It is also finding a place in narrowband data links.

In the typical application (Figure 1), the mixer–oscillator combination converts the input frequency (10.7 MHz) down to 455 kHz, where, after external bandpass filtering, most of the amplification is done. The audio is recovered using a conventional quadrature FM detector. The absence of an input signal is indicated by the presence of noise above the desired audio frequencies. This “noise band” is monitored by an active filter and a detector. A squelch–trigger circuit indicates the presence of noise (or a tone) by an output which can be used to control scanning. At the same time, an internal switch is operated which can be used to mute the audio.

APPLICATIONS INFORMATION

The oscillator is an internally biased Colpitts type with the collector, base, and emitter connections at Pin 4, 1 and 2, respectively. The crystal is used in fundamental mode, calibrated for parallel resonance at 32 pF load capacitance. In theory this means that the two capacitors in series should be 32 pF, but in fact much larger values do not significantly affect the oscillator frequency, and provide higher oscillator output.

The oscillator can also be used in the conventional L/C Colpitts configuration without loss of mixer conversion gain. This oscillator is, of course, much more sensitive to voltage and temperature as shown in Figure 12. Guidelines for choosing L and C values are given in Figure 14.

The mixer is doubly balanced to reduce spurious responses. The mixer measurements of Figure 4 and 6 were made using an external 50 Ω source and the internal 1.8 k at Pin 3. Voltage gain curves at several V_{CC} voltages are shown in Figure 4. The Third Order Intercept curves of Figure 6 are shown using the conventional dBm scales. Measured power gain (with the 50 Ω input) is approximately 18 dB but the useful gain is much higher because the mixer input impedance is over 3 kΩ. Most applications will use a 330 Ω 10.7 MHz crystal filter ahead of the mixer. For higher frequencies, the relative mixer gain is given in Figure 8.

Following the mixer, a ceramic bandpass filter is recommended. The 455 kHz types come in bandwidths from ± 2 kHz to ± 15 kHz and have input and output impedances of 1.5 k to 2.0 k. For this reason, the Pin 5 input to the 6 stage limiting IF has an internal 1.8 k resistor. The IF has a 3 dB limiting sensitivity of approximately 100 µV at Pin 5 and a useful frequency range of about 5 MHz as shown in Figure 5. The frequency limitation is due to the high resistance values in the IF, which were necessary to meet the low power requirement. The output of the limiter is internally connected to the quadrature detector, including the 10 pF quadrature capacitor. Only a parallel L/C is needed externally from Pin 8 to V_{CC}. A shunt resistance can be added to widen the peak separation of the quadrature detector.

The detector output is amplified and buffered to the audio output, Pin 10, which has an output impedance of approximately 300 Ω. Pin 9 provides a high impedance (50 k) point in the output amplifier for application of a filter or de–emphasis capacitor. Pin 11 is the AFC output, with high gain and high output impedance (1 M). If not needed, it should be grounded, or it can be connected to Pin 9 to double the recovered audio. The detector and AFC responses are shown in Figure 7.

Overall performance of the MC3359 from mixer input to audio output is shown in Figure 9 and 10. The MC3359 can also be operated in “single conversion” equipment; i.e., the mixer can be used as a 455 kHz amplifier. The oscillator is disabled by connecting Pin 1 to Pin 2. In this mode, the overall performance is identical to the 10.7 MHz results of Figure 9.

A simple inverting op amp is provided with an output at Pin 13 providing dc bias (externally) to the input at Pin 12, which is referred internally to 2.0 V. A filter can be made with external impedance elements to discriminate between frequencies. With an external AM detector, the filtered audio signal can be checked for the presence of either noise above the normal audio, or a tone signal.

The open loop response of this op amp is given in Figure13. Bandpass filter design information is provided in Figure 15.

A low bias to Pin 14 sets up the squelch–trigger circuit so that Pin 15 is high, a source of at least 2.0 mA, and the audio mute (Pin 16) is open–circuit. If Pin 14 is raised to 0.7 V by the noise or tone detector, Pin 15 becomes open circuit and Pin 16 is internally short circuited to ground. There is no hysteresis. Audio muting is accomplished by connecting Pin 16 to a high–impedance ground–reference point in the audio path between Pin 10 and the audio amplifier. No dc voltage is needed, in fact it is not desirable because audio “thump” would result during the muting function. Signal swing greater than 0.7 V below ground on Pin 16 should be avoided.

MOTOROLA

MC3362

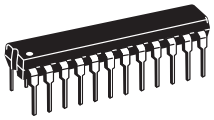
Low-Power Narrowband FM Receiver

. . . includes dual FM conversion with oscillators, mixers, quadrature discriminator, and meter drive/carrier detect circuitry. The MC3362 also has buffered first and second local oscillator outputs and a comparator circuit for FSK detection.

- Complete Dual Conversion Circuitry
- Low Voltage: V_{CC} = 2.0 to 6.0 Vdc
- Low Drain Current (3.6 mA (Typical) @ V_{CC} = 3.0 Vdc)
- Excellent Sensitivity: Input Voltage 0.6 µVrms (Typical) for 12 dB SINAD
- Externally Adjustable Carrier Detect Function
- Low Number of External Parts Required
- Manufactured Using Motorola′s MOSAIC® Process Technology
- MC13135 is Preferred for New Designs

LOW–POWER DUAL CONVERSION FM RECEIVER

SEMICONDUCTOR TECHNICAL DATA



P SUFFIX
PLASTIC PACKAGE
CASE 724

DW SUFFIX
PLASTIC PACKAGE
CASE 751E
(SO-24L)

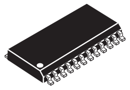


Figure 1. Simplified Application in a PLL Frequency Synthesized Receiver

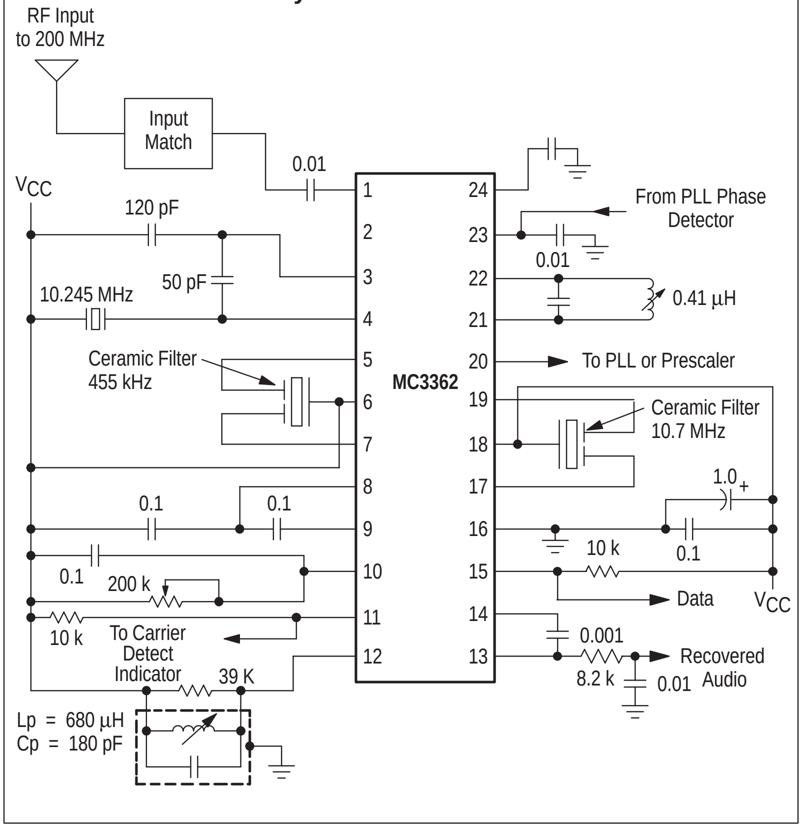
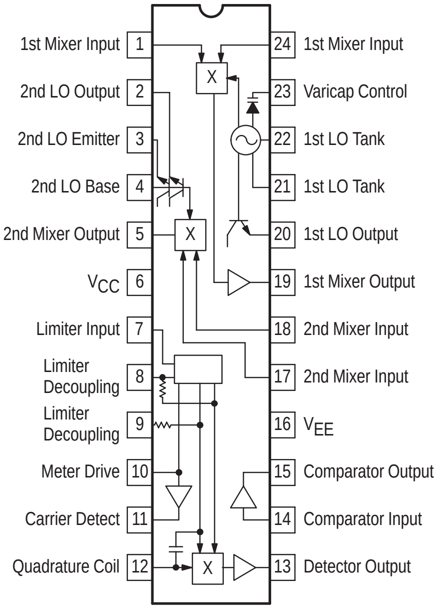


Figure 2. Pin Connections and Representative Block Diagram



ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC3362DW	T_A = – 40 to +85°C	SO–24L
MC3362P		Plastic DIP

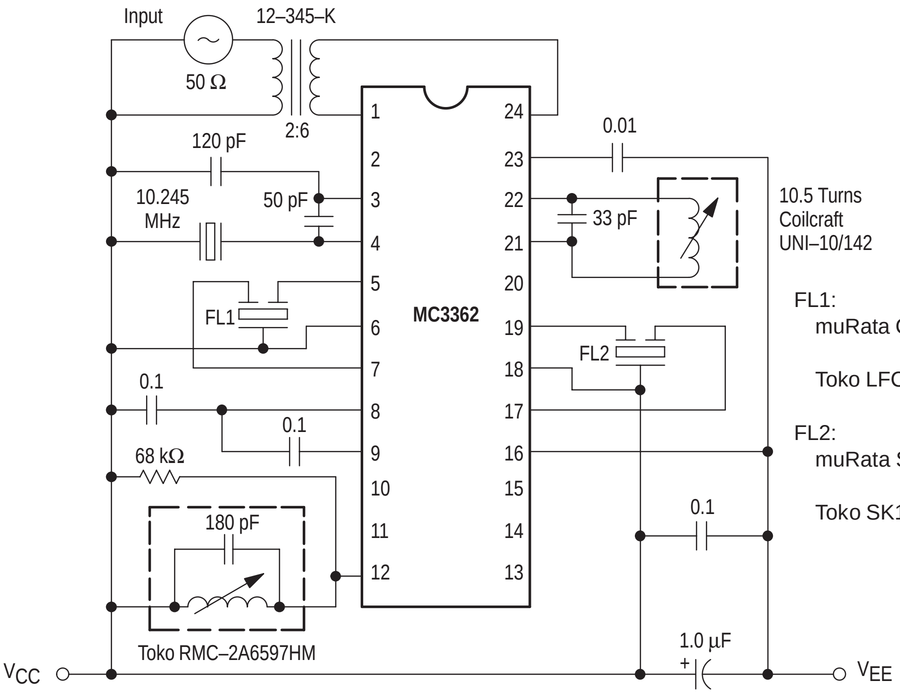
MAXIMUM RATING (T_A = 25°C, unless otherwise noted)

Rating	Pin	Symbol	Value	Unit
Power Supply Voltage (See Figure 2)	6	$V_{CC(max)}$	7.0	Vdc
Operating Supply Voltage Range (Recommended)	6	V_{CC}	2.0 to 6.0	Vdc
Input Voltage ($V_{CC} \geqslant 5.0$ Vdc)	1, 24	V_{1-24}	1.0	Vrms
Junction Temperature	–	T_J	150	°C
Operating Ambient Temperature Range	–	T_A	– 40 to + 85	°C
Storage Temperature Range	–	T_{stg}	– 65 to + 150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 Vdc, f_o = 49.7 MHz, Deviation = 3.0 kHz, T_A = 25°C, Test Circuit of Figure 3, unless otherwise noted)

Characteristic	Pin	Min	Typ	Max	Units
Drain Current (Carrier Detect Low – See Figure 5)	6	–	4.5	7.0	mA
Input for –3.0 dB Limiting		–	0.7	2.0	µVrms
Input for 12 dB SINAD (See Figure 9)		–	0.6	–	µVrms
Series Equivalent Input Impedence		–	450–j350	–	Ω
Recovered Audio (RF signal level = 10 mV)	13	–	350	–	mVrms
Noise Output (RF signal level = 0 mV)	13	–	250	–	mVrms
Carrier Detect Threshold (below V_{CC})	10	–	0.64	–	Vdc
Meter Drive Slope	10	–	100	–	nA/dB
Input for 20 dB (S + N)/N (See Figure 7)		–	0.7	–	µVrms
First Mixer 3rd Order Intercept (Input)		–	–22	–	dBm
First Mixer Input Resistance (Rp)		–	690	–	Ω
First Mixer Input Capacitance (Cp)		–	7.2	–	pF
Conversion Voltage Gain, First Mixer		–	18	–	dB
Conversion Voltage Gain, Second Mixer		–	21	–	
Dector Output Resistance	13	–	1.4	–	kΩ

Figure 3. Test Circuit



FL1:
muRata CFU455D
or
Toko LFC–4551

FL2:
muRata SFE10.7MA
or
Toko SK107M3–A0–10

NOTE: See AN980 for Additional Design Information.

Figure 4. I_{Meter} versus Input

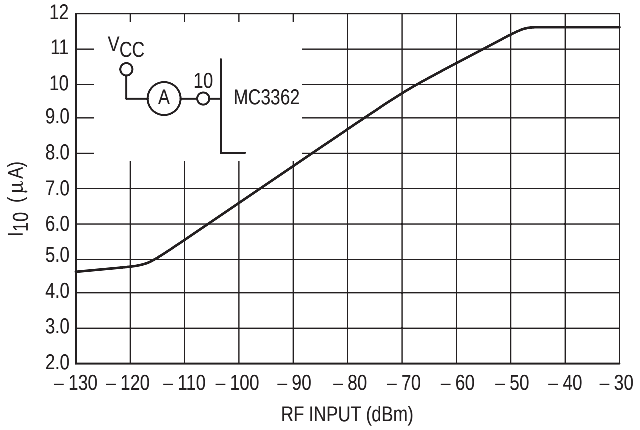


Figure 5. Drain Current, Recovered Audio versus Supply

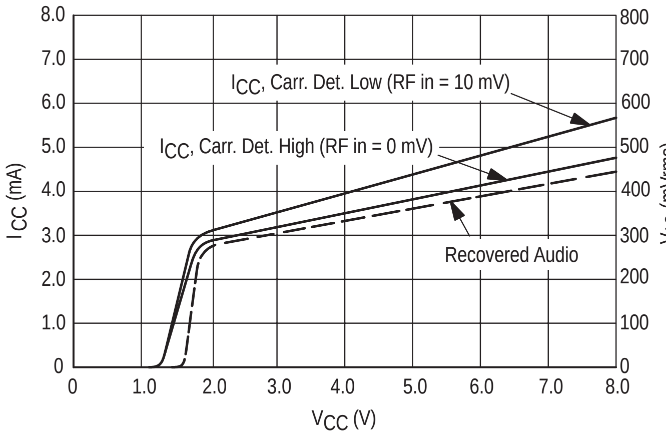


Figure 6. Signal Levels

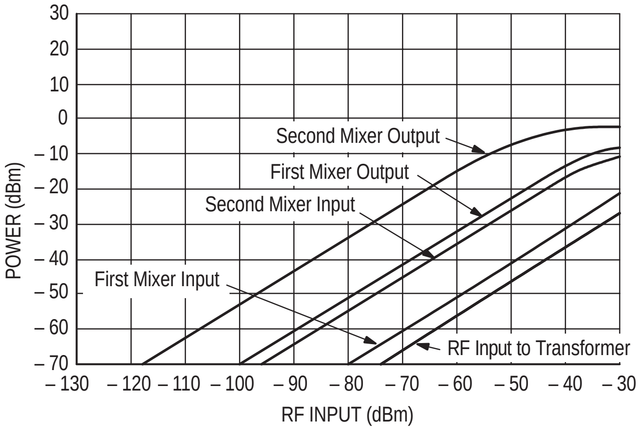


Figure 7. S + N, N, AMR versus Input

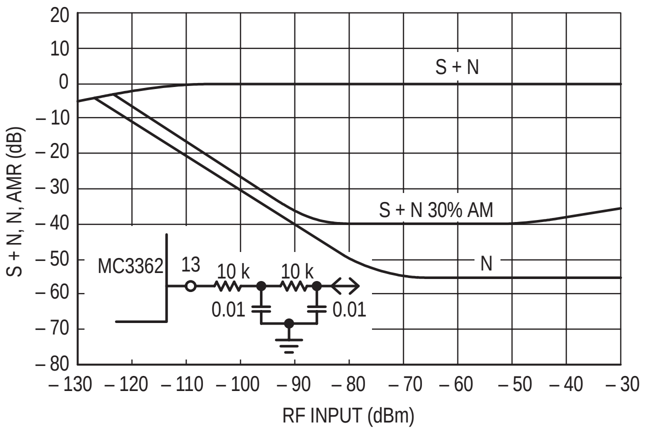


Figure 8. 1st Mixer 3rd Order Intermodulation

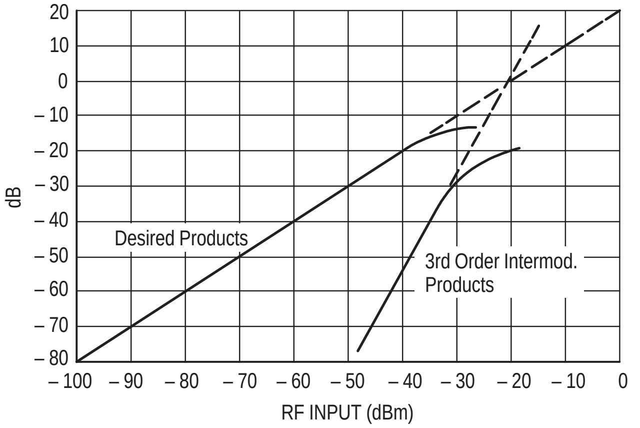


Figure 9. Detector Output versus Frequency

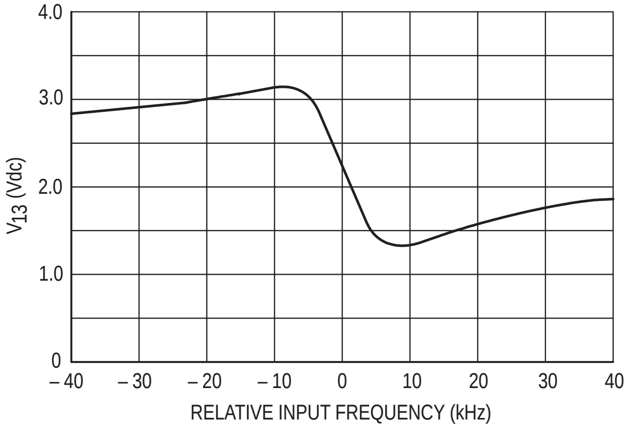
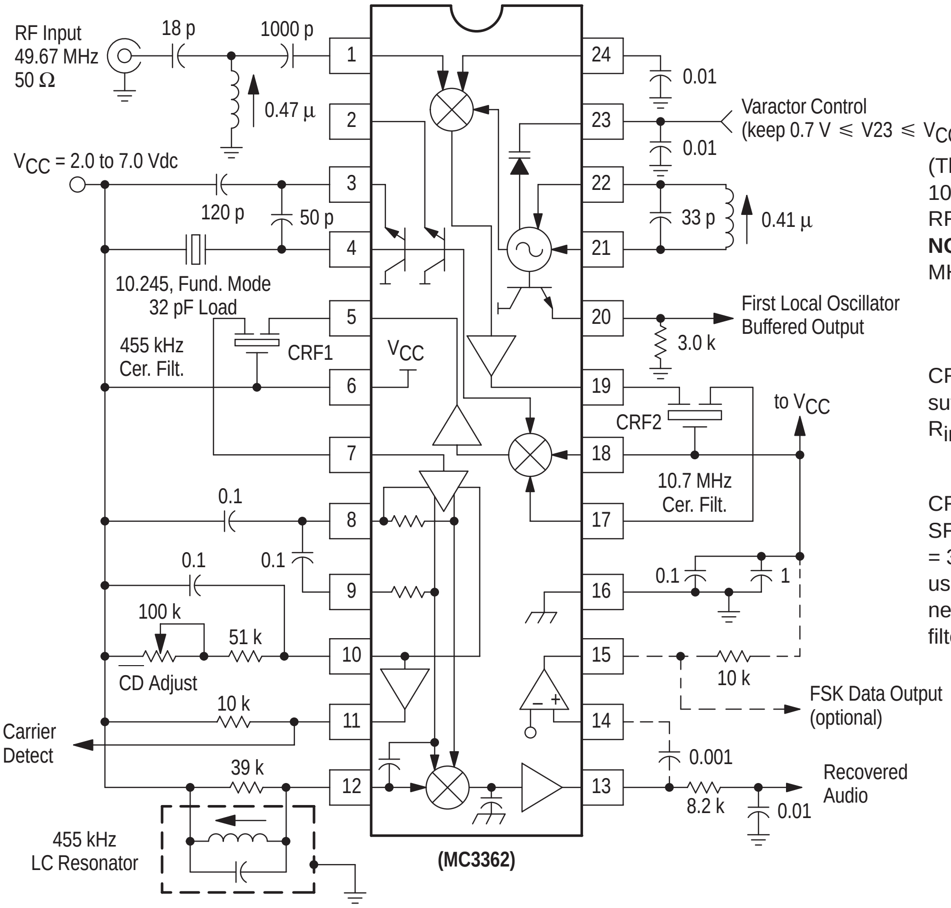


Figure 10. PC Board Test Circuit

(LC Oscillator Configuration Used in PLL Synthesized Receiver)

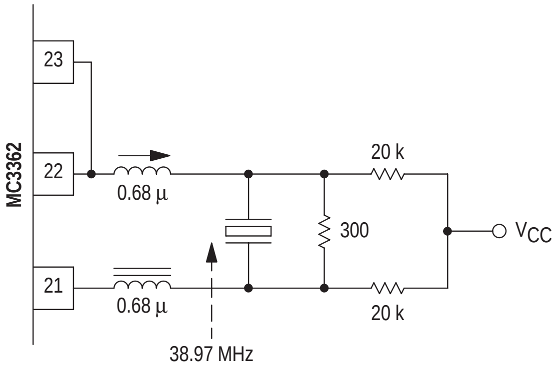


(This network must be tuned to exactly 10.7 MHz above or below the incoming RF signal. **NOTE:** The IF is rolled off above 10.7 MHz to reduce L.O. feedthrough.)

CRF1 = muRata CFU 455X – the X suffix denotes 6.0 dB bandwidth. $R_{in} = R_{out}$ = 1.5 to 2.0 kΩ.

CRF2 = muRata SFA10.7 MF5 or SFE10.7 or equivalent. $R_{in} = R_{out}$ = 330 Ω. Crystal filters can be used but impedance matching will need to be added to ensure proper filter characteristics are realized.

Figure 10A. Crystal Oscillator Configuration for Single Channel Application



Crystal used is series mode resonant (no load capacity specified), 3rd overtone. This method has not proven adequate for fundamental mode, 5th or 7th overtone crystals. The inductor and capacitor will need to be changed for other frequency crystals. See AN980 for further information.

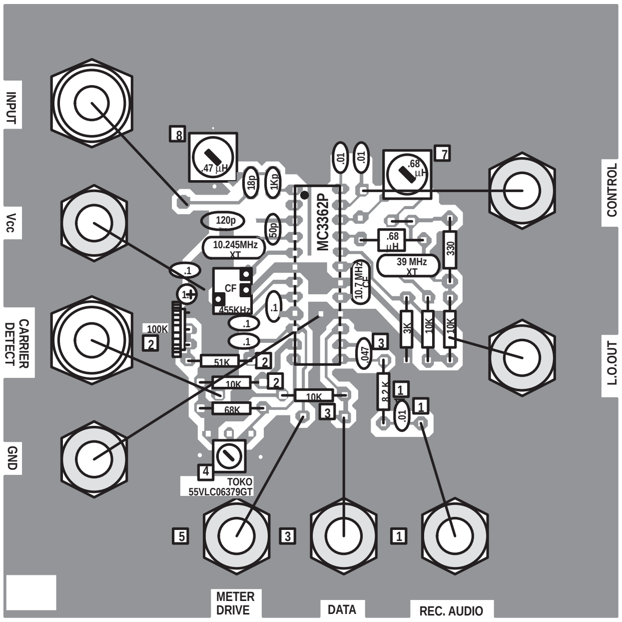


Figure 11. Component Placement View Showing Crystal Oscillator Circuit

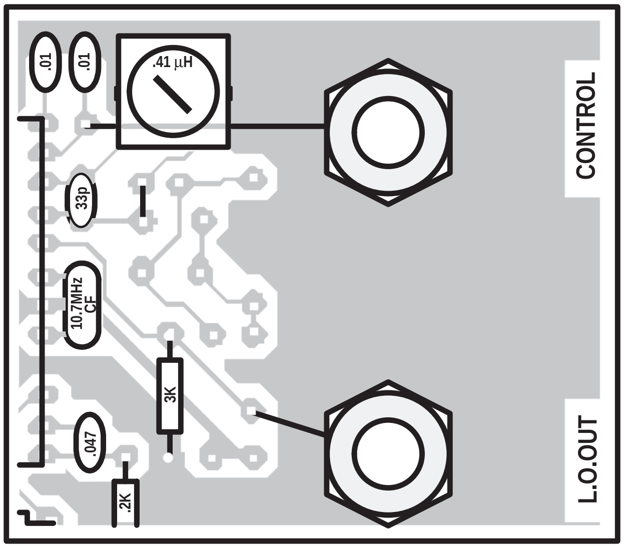


Figure 11A. LC Oscillator Component View

NOTES:
1. Recovered Audio components may be deleted when using data output.
2. Carrier Detect components must be deleted in order to obtain linear Meter Drive output. With these components in place the Meter Drive outputs serve only to trip the Carrier Detect indicator.
3. Data Output components should be deleted in applications where only audio modulation is used. For combined audio/data applications, the 0.047 µF coupling capacitor will add distortion to the audio, so a pull–down resistor at pin 13 may be required.
4. Use Toko 7MC81282 Quadrature coil.
5. Meter Drive cannot be used simultaneously with Carrier Detect output. For analog meter drive, remove components labelled ″2″ and measure meter current (4–12 µA) through ammeter to V_{CC}.
6. Either type of oscillator circuit may be used with any output circuit configuration.
7. LC Oscillator Coil: Coilcraft UNI 10/42 10.5 turns, 0.41 µH Crystal Oscillator circuit: trim coil, 0.68 µH. Coilcraft M1287–A.
8. 0.47 H, Coilcraft M1286–A. Input LC network used to match first mixer input impedance to 50 Ω.

CIRCUIT DESCRIPTION

The MC3362 is a complete FM narrowband receiver from antenna input to audio preamp output. The low voltage dual conversion design yields low power drain, excellent sensitivity and good image rejection in narrowband voice and data link applications.

In the typical application (Figure 1), the first mixer amplifies the signal and converts the RF input to 10.7 MHz. This IF signal is filtered externally and fed into the second mixer, which further amplifies the signal and converts it to a 455 kHz IF signal. After external bandpass filtering, the low IF is fed into the limiting amplifier and detection circuitry. The audio is recovered using a conventional quadrature detector. Twice–IF filtering is provided internally.

The input signal level is monitored by meter drive circuitry which detects the amount of limiting in the limiting amplifier. The voltage at the meter drive pin determines the state of the carrier detect output, which is active low.

APPLICATIONS INFORMATION

The first local oscillator can be run using a free–running LC tank, as a VCO using PLL synthesis, or driven from an external crystal oscillator. It has been run to 190 MHz.* A buffered output is available at Pin 20. The second local oscillator is a common base Colpitts type which is typically run at 10.245 MHz under crystal control. A buffered output is available at Pin 2. Pins 2 and 3 are interchangeable.

The mixers are doubly balanced to reduce spurious responses. The first and second mixers have conversion gains of 18 dB and 22 dB (typical), respectively, as seen in Figure 6. Mixer gain is stable with respect to supply voltage. For both conversions, the mixer impedances and pin layout are designed to allow the user to employ low cost, readily available ceramic filters. Overall sensitivity and AM rejection are shown in Figure 7. The input level for 20 dB (S + N)/N is 0.7 µV using the two–pole post–detection filter pictured.

---

* If the first local oscillator (Pins 21 and/or 22) is driven from a strong external source (100 mVrms), the mixer can be used to over 450 MHz.

Following the first mixer, a 10.7 MHz ceramic band–pass filter is recommended. The 10.7 MHz filtered signal is then fed into one second mixer input pin, the other input pin being connected to V_{CC}. Pin 6 (V_{CC}) is treated as a common point for emitter–driven signals.

The 455 kHz IF is typically filtered using a ceramic bandpass filter then fed into the limiter input pin. The limiter has 10 µV sensitivity for – 3.0 dB limiting, flat to 1.0 MHz.

The output of the limiter is internally connected to the quadrature detector, including a quadrature capacitor. A parallel LC tank is needed externally from Pin 12 to V_{CC}. A 39 kΩ shunt resistance is included which determines the peak separation of the quadrature detector; a smaller value will increase the spacing and linearity but decrease recovered audio and sensitivity.

A data shaping circuit is available and can be coupled to the recovered audio output of Pin 13. The circuit is a comparator which is designed to detect zero crossings of FSK modulation. Data rates are typically limited to 1200 baud to ensure data integrity and avoid adjacent channel “splatter.” Hysteresis is available by connecting a high valued resistor from Pin 15 to Pin 14. Values below 120 kΩ are not recommended as the input signal cannot overcome the hysteresis.

The meter drive circuitry detects input signal level by monitoring the limiting amplifier stages. Figure 4 shows the unloaded current at Pin 10 versus input power. The meter drive current can be used directly (RSSI) or can be used to trip the carrier detect circuit at a specified input power. To do this, pick an RF trip level in dBm. Read the corresponding current from Figure 4 and pick a resistor such that:

$$R_{10} \simeq 0.64 \text{ Vdc} / I_{10}$$

Hysteresis is available by connecting a high valued resistor R_H between Pins 10 and 11. The formula is:

$$\text{Hysteresis} = V_{CC}/(R_H \times 10^{-7}) \text{ dB}$$

Figure 12. Circuit Side View

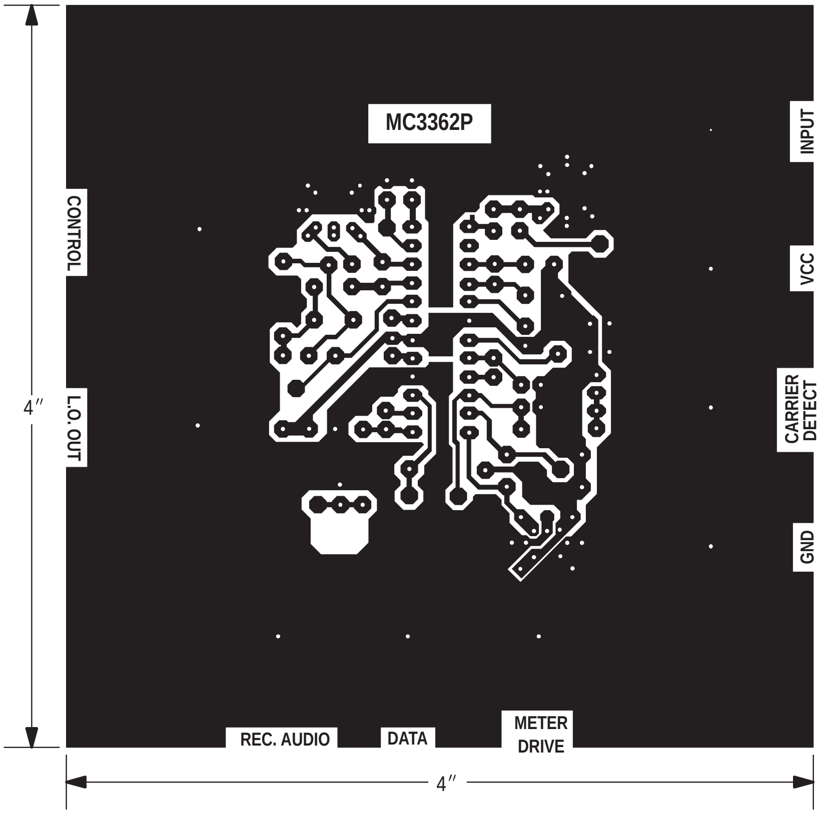
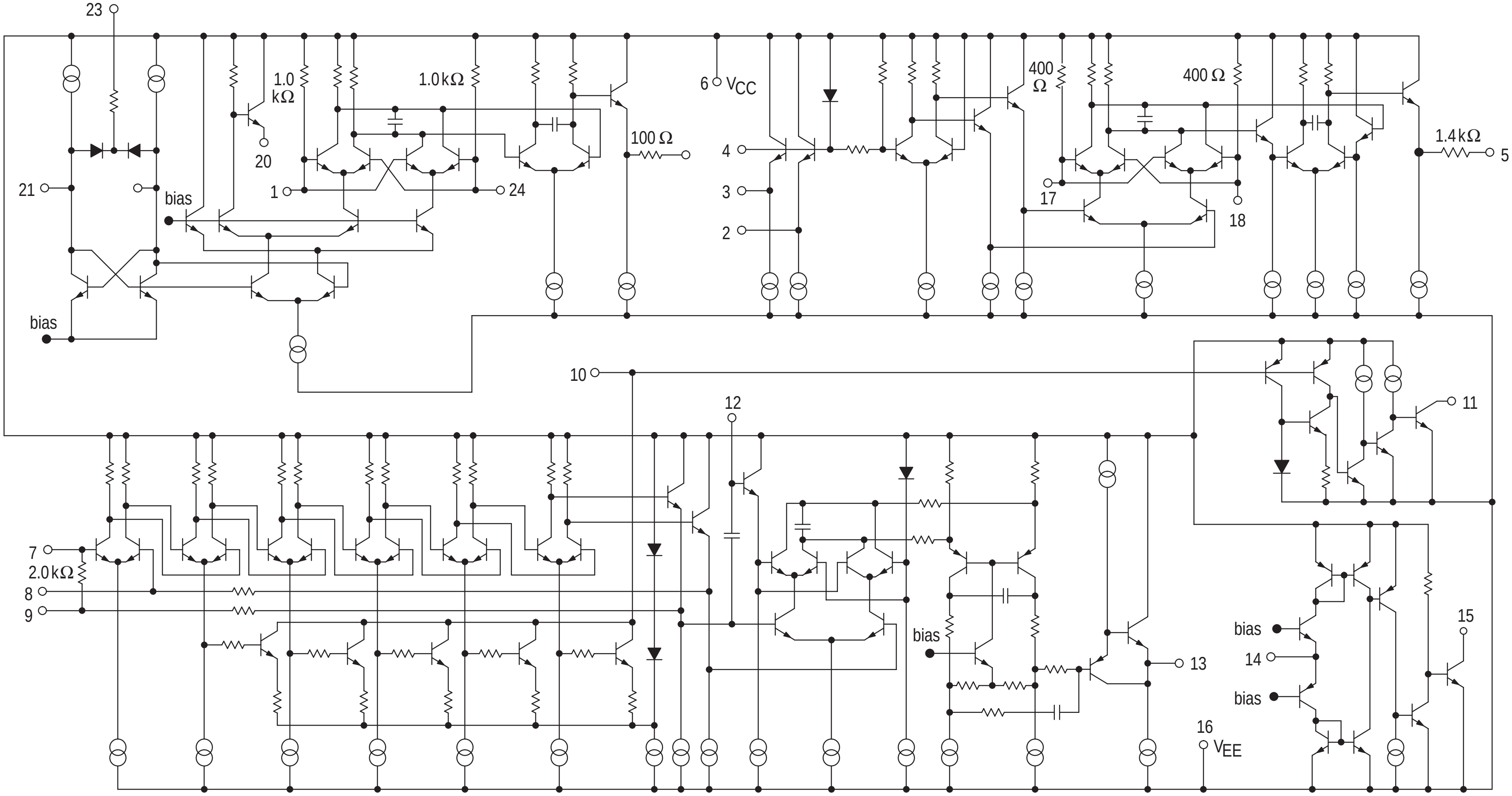


Figure 13. Representative Schematic Diagram



MOTOROLA

Low Voltage FM Narrowband Receiver

. . . with single conversion circuitry including oscillator, mixer, IF amplifiers, limiting IF circuitry, and quadrature discriminator. The MC3374 is perfect for narrowband audio and data applications up to 75 MHz which require extremely low power consumption. Battery powered applications down to V_{CC} = 1.1 V are possible. The MC3374 also includes an on–board voltage regulator, low battery detection circuitry, a receiver enable allowing a power down Sleep–Mode™, two undedicated buffer amplifiers to allow simultaneous audio and data reception, and a comparator for enhancing FSK (Frequency Shift Keyed) data reception to 1200 baud.

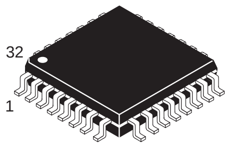
- Low Supply Voltage: V_{CC} = 1.1 to 3.0 Vdc
- Low Power Consumption: P_D = 1.5 to 5.0 mW
- Input Bandwidth 75 MHz
- Excellent Sensitivity: 0.5 µVrms for 12 dB SINAD
- Voltage Regulator Available (Source Capability 3.0 mA)
- Receiver Enable to Allow Active/Standby Operation
- Low Battery Detection Circuitry
- Self Biasing Audio Buffer
- Data Buffer
- FSK Data Shaping Comparator
- Standard 32–Lead QFP Surface Mount Package

Sleep–Mode is a trademark of Motorola, Inc.

MC3374

LOW VOLTAGE SINGLE CONVERSION FM RECEIVER

SEMICONDUCTOR
TECHNICAL DATA

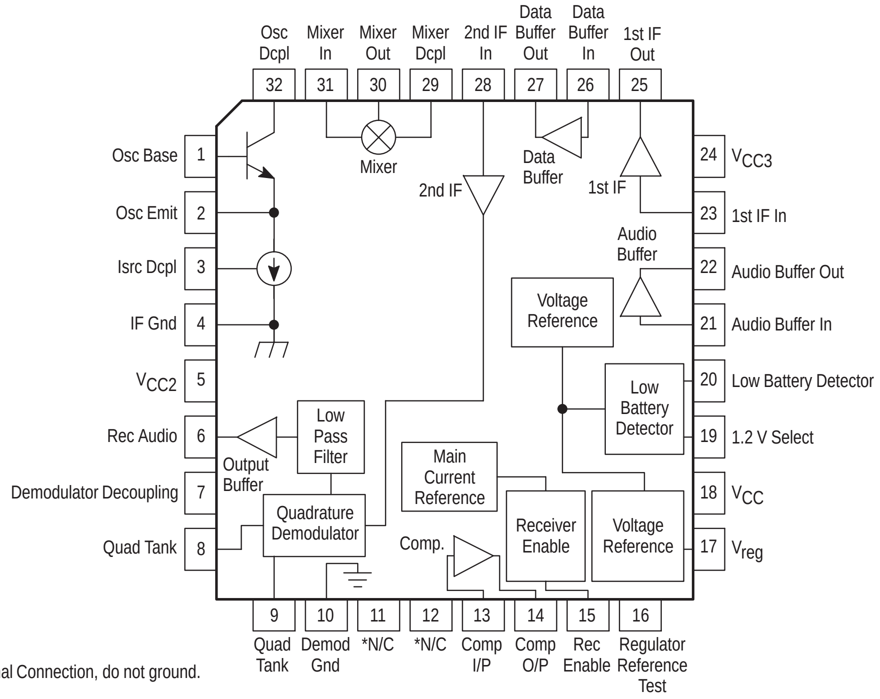


FTB SUFFIX
PLASTIC PACKAGE
CASE 873
(Thin QFP)

ORDERING INFORMATION

Device	Tested Operating Temperature Range	Package
MC3374FTB	T_A = –10° to +70°C	TQFP–32

Simplified Block Diagram



*Internal Connection, do not ground.

This device contains 87 active transistors

MAXIMUM RATINGS (Voltage with respect to Pins 4 and 10; T_A = 25°C.)

Rating	Pin	Value	Unit
Supply Voltage	18	5.0	Vdc
RF Input Signal	31	1.0	Vrms
Audio Buffer Input	21	1.0	Vrms
Data Buffer Input	26	1.0	Vrms
Comparator Input	13	1.0	Vrms
Junction Temperature	–	150	°C
Storage Temperature	–	–65 to +150	°C

Device should not be operated at or outside these values. The “Recommended Operating Limits” provide for actual device operation.

RECOMMENDED OPERATING CONDITIONS

Parameter	Pin	Value	Unit
Supply Voltage	18	1.1 to 3.0	Vdc
Receiver Enable Voltage	15	V_{CC}	Vdc
1.2 V Select Voltage	19	Open or V_{CC}	Vdc
RF Input Signal Level	31	0.001 to 100	mVrms
RF Input Frequency	31	0 to 75	MHz
Intermediate Frequency (IF)	–	455	kHz
Audio Buffer Input	21	0 to 75	mVrms
Data Buffer Input	26	0 to 75	mVrms
Comparator Input	13	10 to 300	mVrms
Ambient Temperature	–	–10 to 70	°C

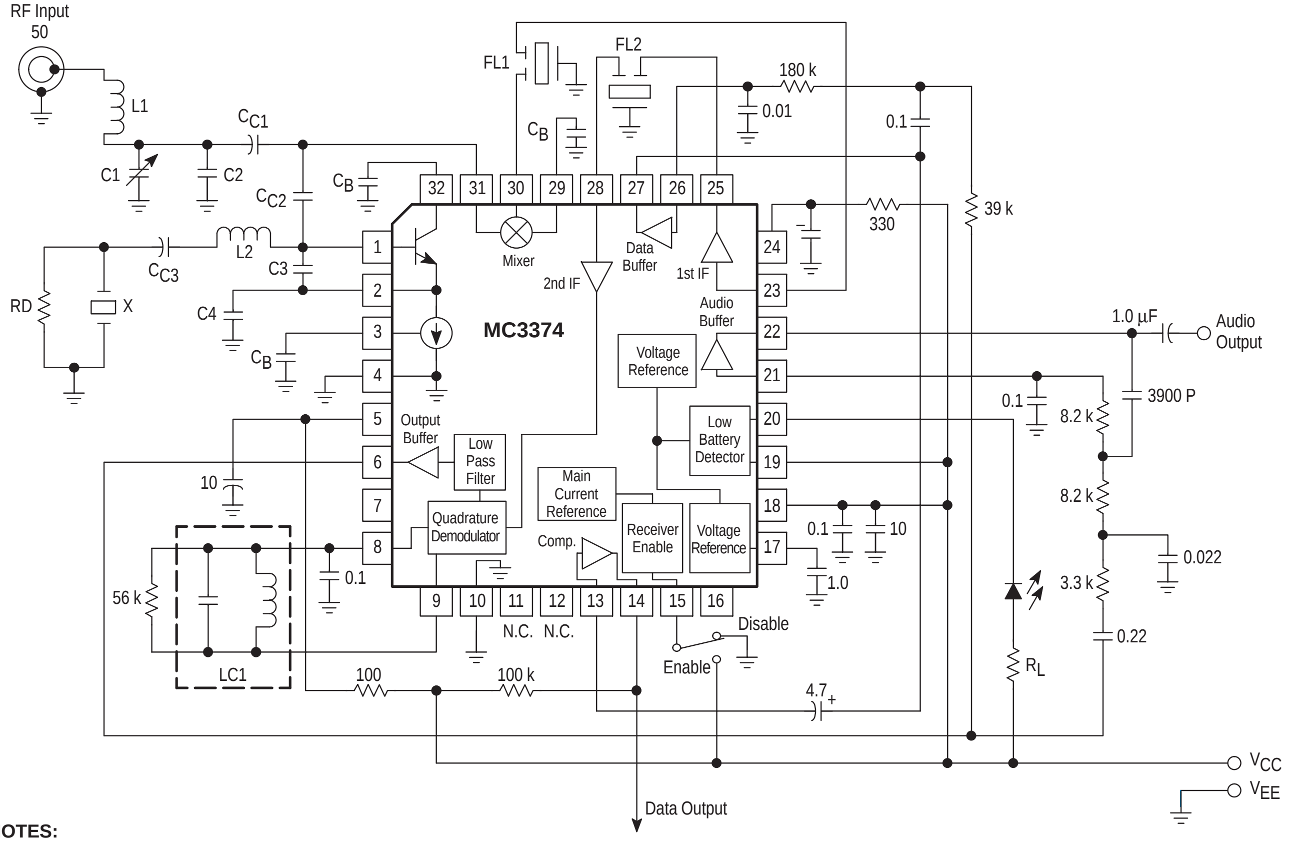
ELECTRICAL CHARACTERISTICS (V_{CC} = 1.3 V, f_o = 10.7 MHz, f_{mod} = 1.0 kHz, Deviation = 3.0 kHz, T_A = 25°C, Test Circuit of Figure 1, unless otherwise noted.)

Characteristic	Pin	Min	Typ	Max	Unit
OVERALL MC3374 PERFORMANCE					
Drain Current – Pin 15 = V_{CC} (Enabled) – Pin 15 = 0 Vdc (Disabled)	5 + 18 + 24 5 + 18 + 24	– –	1.6 0.5	3.0 –	mA µA
Recovered Audio (RF Input = 10 µV)	6	13	18	30	mVrms
Noise Output (RF Input = 0 mV, 300 Hz – 5.0 kHz)	6	–	1.0	–	mVrms
Input for –3.0 dB Limiting	31	–	0.6	–	µVrms
MIXER					
Mixer Input Resistance (Rp)	31	–	1.5	–	kΩ
Mixer Input Capacitance (Cp)	31	–	9.0	–	pF
FIRST IF AMPLIFIER					
First IF Amp Voltage Gain	–	–	27	–	dB
AUDIO BUFFER					
Voltage Gain	–	3.0	4.0	4.7	V/V
Input Resistance	21	–	110	–	kΩ
Maximum Input for Undistorted Output (<5% THD)	21	–	64	–	mVrms
Maximum Output Swing (<5% THD)	22	–	690	–	mV_{pp}
Output Resistance	22	–	780	–	Ω
DATA BUFFER					
Voltage Gain	–	1.4	2.7	4.3	V/V
Input Resistance	26	–	9.8	–	MΩ
Maximum Input for Undistorted Output (<5% THD)	26	–	100	–	mVrms
Maximum Output Swing (<5% THD)	27	–	800	–	mV_{pp}
Output Resistance	27	–	690	–	Ω

ELECTRICAL CHARACTERISTICS (continued) (V_{CC} = 1.3 V, f_o = 10.7 MHz, f_{mod} = 1.0 kHz, Deviation = 3.0 kHz, T_A = 25°C, Test Circuit of Figure 1, unless otherwise noted.)

Characteristic	Pin	Min	Typ	Max	Unit
COMPARATOR					
Minimum Input for Triggering (R_L = 100 kΩ)	13	–	7.0	–	mVrms
Maximum Input Frequency (R_L = 100 kΩ)	13	–	25	–	kHz
Rise Time (10–90%; R_L = 100 kΩ)	14	–	5.0	–	µs
Fall Time (90–10%; R_L = 100 kΩ)	14	–	0.4	–	µs
LOW BATTERY DETECTOR					
Low Battery Trip Point	19	–	1.2	–	Vdc
Low Battery Output – V_{CC} = 0.9 V – V_{CC} = 1.3 V	20 20	– –	0.2 V_{CC}	– –	Vdc
VOLTAGE REGULATOR					
Regulated Output (see Figure 4)	17	0.95	1.07	1.15	Vdc
Source Capability	17	–	–	3.0	mA

Figure 1. MC3374 Pager IF Application Circuit



NOTES:

1. FL1 and FL2 are 455 kHz ceramic bandpass filters, which should have input and output impedances of 1.5 kΩ to 2.0 kΩ. Suggested part numbers are MuRata CFU455X or CFW455x – the ‘X’ suffix denotes bandwidth.
2. LC1 is a 455 kHz LC resonator. Recommended part numbers are Toko America RMC2A6597HM or 5SVLC–0637BGT (smaller). The evaluation board layout shown provides for use of either resonator. Ceramic discriminator elements cannot be used with the MC3374 due to their low input impedance. The damping resistor value can be raised to increase the recovered audio or lowered to increase the quadrature detector’s bandwidth and linearity – practical limits are approximately 27 kΩ to 75 kΩ. Typically the quadrature detector’s bandwidth should match the low IF filter’s bandwidth.
3. The data buffer is set up as a low–pass filter with a corner frequency of approximately 200 Hz. The audio buffer is a bandpass filter with corner frequencies of 300 Hz and 3.0 kHz. The audio amplifier provides bass suppression.
4. C_{C1} and C_{C3} are RF coupling capacitors and should have ≤ 20 Ω impedance at the desired input and oscillator frequencies.
5. C_{C2} provides “light coupling” of the oscillator signal into the mixer, and should have a 3.0 kΩ to 5.0 kΩ impedance at the desired local oscillator frequency.
6. Capacitors labelled C_B are bypass capacitors and should have 20 Ω impedance at the desired RF and local oscillator frequencies.
7. The network of L1, C1 and C2 provides impedance matching of the mixer input (nominally 3.0 kΩ shunted by 9.0 pF) to 50 Ω at the desired RF/IF input frequency. This will allow for bench testing of the receiver from typical RF signal generators or radio service monitors, but additional or different matching will be required to maximize receiver sensitivity when used in conjunction with an antenna, RF preamplifier or mixer.

In. Freq.	L1	L2	C1	C2	C3	C4	C_{C1}/C_{C3}	C_{C2}	C_B	RD
10.7 MHz	6.8 µH	Short	2–82 pF	10 pF	120 pF	50 pF	1.0 nF	5.0 pF	0.1 µF	Open
45 MHz	0.68 µH	1.2 µH	5–25 pF	Open	30 pF	5.0 pF	1.0 nF	1.0 pF	1.0 nF	1.0 k
72 MHz	0.22 µH	0.22 µH	5–25 pF	Open	18 pF	3.0 pF	470 pF	1.0 pF	470 pF	1.0 k

Figure 2. Recovered Audio versus Supply

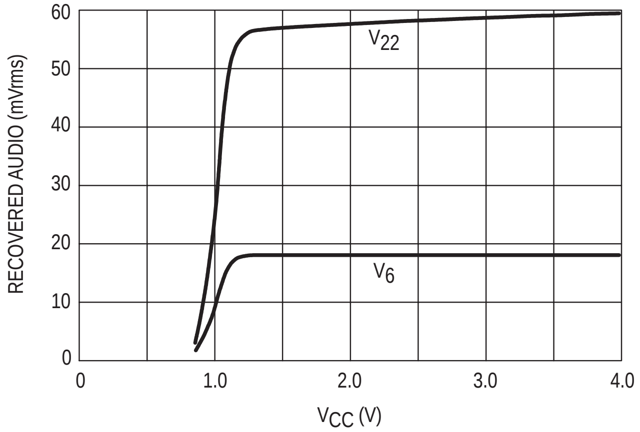


Figure 3. S+N, N versus Input

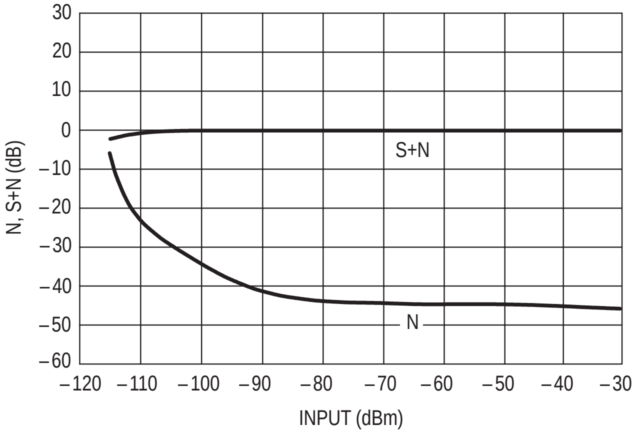


Figure 4. V_{REG} versus Supply

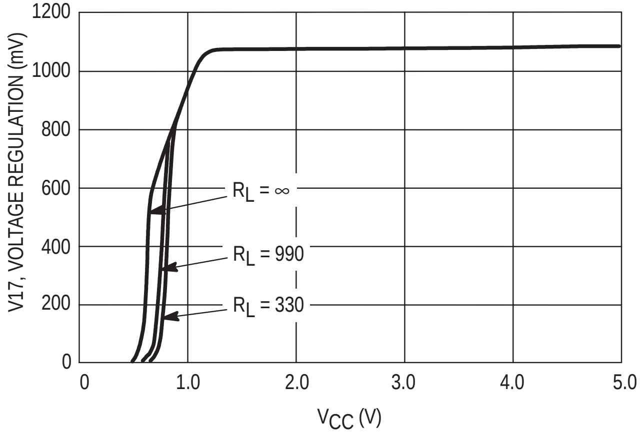


Figure 5. Regulated Output and Recovered Audio versus Temperature

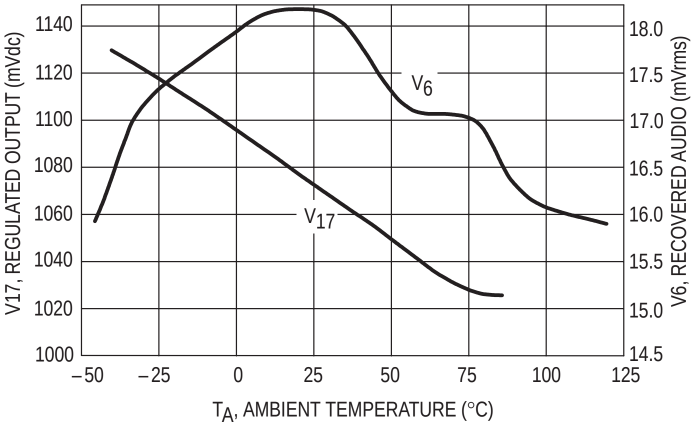


Figure 6. Buffer Amplifier Gains versus Temperature

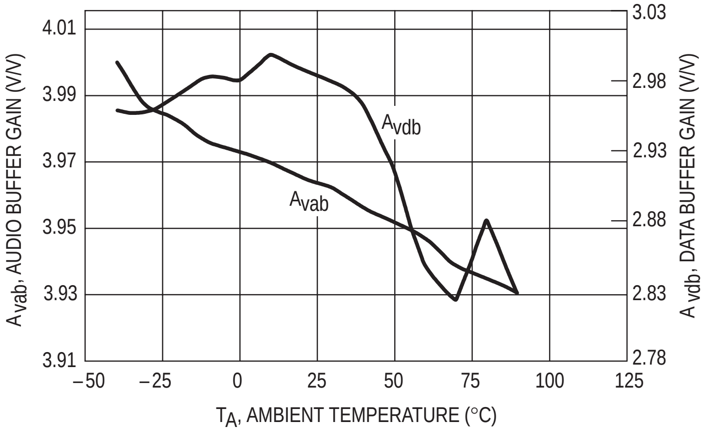
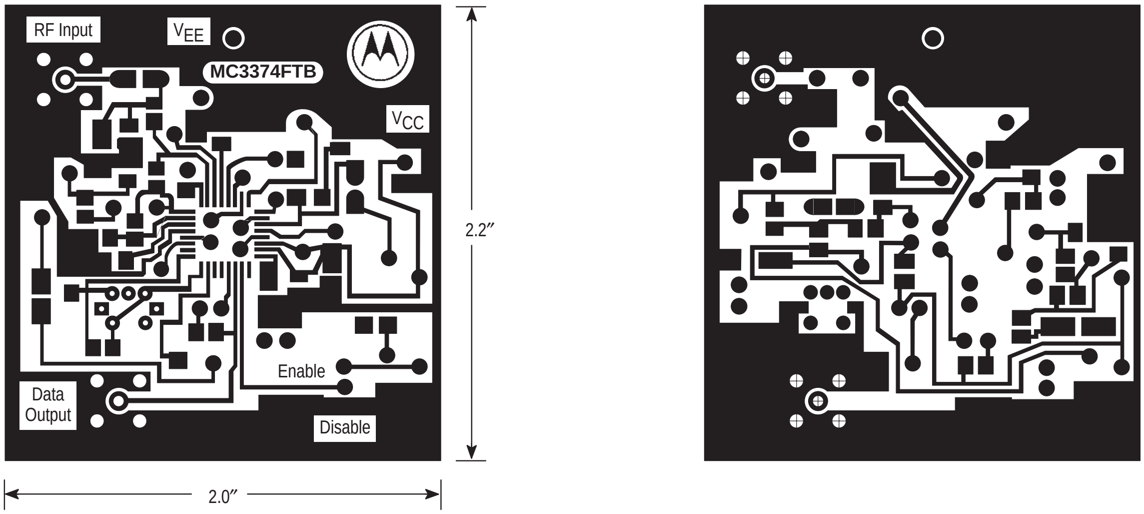
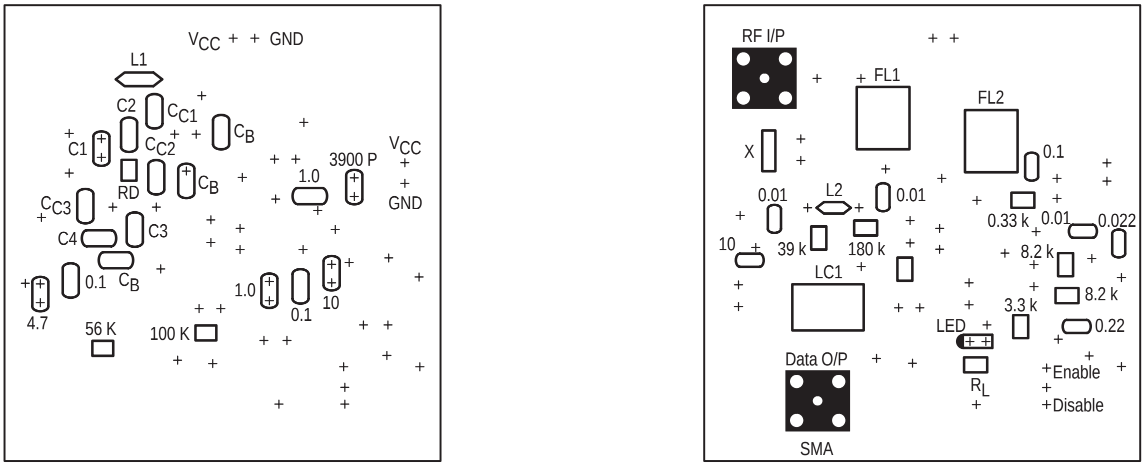


Figure 7. MC3374 Pager Receiver PCB Artwork



COPPER 1 LAYER
(Actual View of Surface Mount Side)

COPPER 2 LAYER
(Caution: Reversed View of Through–Hole Side)



COMPONENT 1 LAYER

COMPONENT 2 LAYER

NOTE: + = Through Hole

CIRCUIT DESCRIPTION

The MC3374 is an FM narrowband receiver capable of operation to 75 MHz. The low voltage design yields low power drain and excellent sensitivity in narrowband voice and data link applications. In the typical application the mixer amplifies the incoming RF or IF signal and converts this frequency to 455 kHz. The signal is then filtered by a 455 kHz ceramic filter and applied to the first intermediate frequency (IF) amplifier input, before passing through a second ceramic filter. The modulated IF signal is then applied to the limiting IF amplifier and detector circuitry. Modulation is recovered by a conventional quadrature detector. The typical modulation bandwidth available is 3.0 to 5.0 kHz.

Features available include buffers for audio/data amplification and active filtering, on board voltage regulator, low battery detection circuitry with programmable level, and receiver disable circuitry. The MC3374 is an FM utility receiver to be used for voice and/or narrowband data reception. It is especially suitable where extremely low power consumption and high design flexibility are required.

APPLICATION

The MC3374 can be used as a high performance FM IF for the use in low power dual conversion receivers. Because of the MC3374's extremely good sensitivity (0.6 μV for 20 dB (S+N/N, see Figure 3)), it can also be used as a stand alone single conversion narrowband receiver to 75 MHz for applications not sensitive to image frequency interference. An RF preamplifier will likely be needed to overcome preselector losses.

The oscillator is a Colpitts type which must be run under crystal control. For fundamental mode crystals choose resonators, parallel resonant, for a 32 pF load. For higher frequencies, use a 3rd overtone series mode type. The coil L2 and RD resistor are needed to ensure proper operation.

The best adjacent channel and sensitivity response occur when two 455 kHz ceramic filters are used, as shown in Figure 1. Either can be replaced by a 0.1 μF coupling capacitor to reduce cost, but some degradation in sensitivity and/or stability is suspected.

The detector is a quadrature type, with the connection from the limiter output to the detector input provided internally. A 455 kHz LC tank circuit must be provided externally. One of the tank pins (Pin 8) must be decoupled using a 0.1 μF capacitor. The 56 kΩ damping resistor (see Figure 1), determines the peak separation of the detector (and thus its bandwidth). Smaller values will increase the separation and bandwidth but decrease recovered audio and sensitivity.

The data buffer is a noninverting amplifier with a nominal voltage gain of 2.7 V/V. This buffer needs its dc bias (approximately 250 mV) provided externally or else debiasing will occur. A 2nd order Sallen–Key low pass filter, as shown in Figure 1, connecting the recovered audio output to the data buffer input provides the necessary dc bias and some post detection filtering. The buffer can also be used as an active filter.

The audio buffer is a noninverting amplifier with a nominal voltage gain of 4.0 V/V. This buffer is self–biasing so its input should be ac coupled. The two buffers, when applied as active filters, can be used together to allow simultaneous audio and very low speed data reception. Another possible configuration is to receive audio only and include a noise–triggered squelch.

The comparator is a noninverting type with an open collector output. Typically, the pull–up resistor used between Pin 14 and V_{CC} is 100 kΩ. With R_L = 100 kΩ the comparator is capable of operation up to 25 kHz. The circuit is self–biasing, so its input should be ac coupled.

The regulator is a 1.07 V reference capable of sourcing 3.0 mA. This pin (Pin 17) needs to be decoupled using a 1.0 – 10 μF capacitor to maintain stability of the MC3374.

All three V_{CC}s on the MC3374 (V_{CC}, V_{CC2}, V_{CC3}) run on the same supply voltage. V_{CC} is typically decoupled using capacitors only. V_{CC2} and V_{CC3} should be bypassed using the RC bypasses shown in Figure 1. Eliminating the resistors on the V_{CC2} and V_{CC3} bypasses may be possible in some applications, but a reduction in sensitivity and quieting will likely occur.

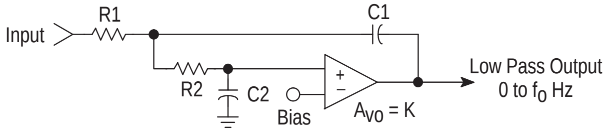
The low battery detection circuit gives an NPN open collector output at Pin 20 which drops low when the MC3374 supply voltage drops below 1.2 V. Typically it would be pulled up via a 100 kΩ resistor to supply.

The 1.2 V Select pin, when connected to the MC3374 supply, programs the low battery detector to trip at V_{CC} < 1.1 V. Leaving this pin open raises the trip voltage on the low battery detector.

Pin 15 is a receiver enable which is connected to V_{CC} for normal operation. Connecting this pin to ground shuts off receiver and reduces current drain to I_{CC} < 0.5 μA.

APPENDIX

Design of 2nd Order Sallen–Key Low Pass Filters



The audio and data buffers can easily be configured as active low pass filters using the circuit configuration shown above. The circuit has a center frequency (f_o) and quality factor (Q) given by the following:

$$f_o = \frac{1}{2\pi\sqrt{R1R2C1C2}}$$

$$Q = \frac{1}{\sqrt{\frac{R2C2}{R1C1}} + \sqrt{\frac{R1C2}{R2C1}} + (1–K)\sqrt{\frac{R1C1}{R2C2}}}$$

If possible, let R1 = R2 or C1 = C2 to simplify the above equations. Be sure to avoid a negative Q value to prevent instability. Setting $Q = 1/\sqrt{2} = 0.707$ yields a maximally flat filter response.

Data Buffer Design

The data buffer is designed as follows:

f_O = 200 Hz
C1 = C2 = 0.01 µF
Q = 0.707 (target)

K = 2.7 (data buffer open loop voltage gain)

Setting C1 = C2 yields:

$$fo = \frac{1}{2\pi C1\sqrt{R1R2}}$$

$$Q = \frac{1}{\sqrt{\frac{R2}{R1}} + (2–K)\sqrt{\frac{R1}{R2}}}$$

Iteration yields R2 = 4.2 (R1) to make Q = 0.707.
Substitution into the equation for f_O yields:
R1 = 38 kΩ (use 39 kΩ)
R2 = 4.2(R1) = 180 kΩ
C1 = C2 = 0.01 µF

Audio Buffer Design

The audio buffer is designed as follows:

f_O = 3000 Hz
R1 = R2 = 8.2 kΩ
Q = 0.707 (target)

K = 3.9 (audio buffer open loop voltage gain)

Setting C1 = C2 yields:

$$fo = \frac{1}{2\pi R1\sqrt{C1C2}}$$

$$Q = \frac{1}{\sqrt{\frac{C2}{C1}} + (1–K)\sqrt{\frac{C1}{C2}}}$$

Iteration yields C2 = 2.65 (C1) to make Q = 0.707.
Substitution into the equation for f_O yields:
C1 = 3900 pF
C2 = 2.65(C1) = 0.01 µF
R1 = R2 = 8.2 kΩ

MOTOROLA

MC3371
MC3372

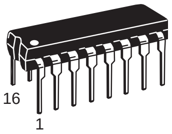
Low Power Narrowband FM IF

The MC3371 and MC3372 perform single conversion FM reception and consist of an oscillator, mixer, limiting IF amplifier, quadrature discriminator, active filter, squelch switch, and meter drive circuitry. These devices are designed for use in FM dual conversion communication equipment. The MC3371/MC3372 are similar to the MC3361/MC3357 FM IFs, except that a signal strength indicator replaces the scan function controlling driver which is in the MC3361/MC3357. The MC3371 is designed for the use of parallel LC components, while the MC3372 is designed for use with either a 455 kHz ceramic discriminator, or parallel LC components.

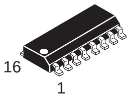
These devices also require fewer external parts than earlier products. The MC3371 and MC3372 are available in dual–in–line and surface mount packaging.

- Wide Operating Supply Voltage Range: V_{CC} = 2.0 to 9.0 V
- Input Limiting Voltage Sensitivity of –3.0 dB
- Low Drain Current: I_{CC} = 3.2 mA, @ V_{CC} = 4.0 V, Squelch Off
- Minimal Drain Current Increase When Squelched
- Signal Strength Indicator: 60 dB Dynamic Range
- Mixer Operating Frequency Up to 100 MHz
- Fewer External Parts Required than Earlier Devices

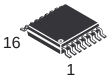
LOW POWER FM IF



P SUFFIX
PLASTIC PACKAGE
CASE 648



D SUFFIX
PLASTIC PACKAGE
CASE 751B
(SO–16)



DTB SUFFIX
PLASTIC PACKAGE
CASE 948F
(TSSOP–16)

MAXIMUM RATINGS

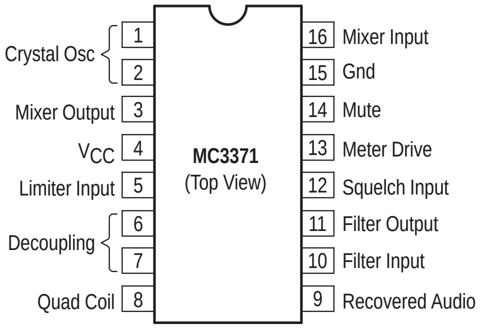
Rating	Pin	Symbol	Value	Unit
Power Supply Voltage	4	V_{CC}(max)	10	Vdc
RF Input Voltage (V_{CC} ⩾ 4.0 Vdc)	16	V16	1.0	Vrms
Detector Input Voltage	8	V8	1.0	Vpp
Squelch Input Voltage (V_{CC} ⩾ 4.0 Vdc)	12	V12	6.0	Vdc
Mute Function	14	V_{14}	–0.7 to 10	V_{pk}
Mute Sink Current	14	I14	50	mA
Junction Temperature	–	T_J	150	°C
Storage Temperature Range	–	T_{stg}	–65 to +150	°C

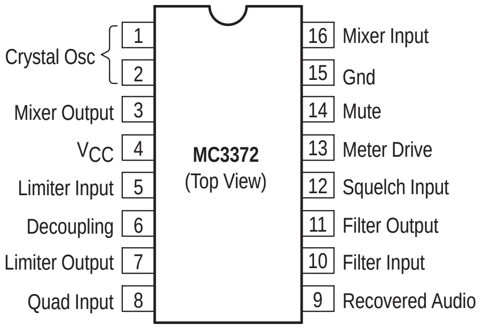
NOTES: 1. Devices should not be operated at these values. The “Recommended Operating Conditions” table provides conditions for actual device operation.
2. ESD data available upon request.

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC3371D	T_A = –30° to +70°C	SO–16
MC3371DTB		TSSOP–16
MC3371P		Plastic DIP
MC3372D		SO–16
MC3372DTB		TSSOP–16
MC3372P		Plastic DIP

PIN CONNECTIONS





RECOMMENDED OPERATING CONDITIONS

Rating	Pin	Symbol	Value	Unit
Supply Voltage (@ T_A = 25°C) (–30°C ⩽ T_A ⩽ +75°C)	4	V_{CC}	2.0 to 9.0 2.4 to 9.0	Vdc
RF Input Voltage	16	V_{rf}	0.0005 to 10	mVrms
RF Input Frequency	16	f_{rf}	0.1 to 100	MHz
Oscillator Input Voltage	1	V_{local}	80 to 400	mVrms
Intermediate Frequency	–	f_{if}	455	kHz
Limiter Amp Input Voltage	5	V_{if}	0 to 400	mVrms
Filter Amp Input Voltage	10	V_{fa}	0.1 to 300	mVrms
Squelch Input Voltage	12	V_{sq}	0 or 2	Vdc
Mute Sink Current	14	I_{sq}	0.1 to 30	mA
Ambient Temperature Range	–	T_A	–30 to +70	°C

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 4.0 Vdc, f_o = 58.1125 MHz, df = ±3.0 kHz, f_{mod} = 1.0 kHz, 50 Ω source, f_{local} = 57.6575 MHz, V_{local} = 0 dBm, T_A = 25°C, unless otherwise noted)

Characteristic	Pin	Symbol	Min	Typ	Max	Unit
Input for 12 dB SINAD Matched Input – (See Figures 11, 12 and 13) Unmatched Input – (See Figures 1 and 2)	–	V_{SIN}	 – –	 1.0 5.0	 – 15	µVrms
Input for 20 dB NQS	–	V_{NQS}	–	3.5	–	µVrms
Recovered Audio Output Voltage V_{rf} = –30 dBm	–	AF_O	 120	 200	 320	mVrms
Recovered Audio Drop Voltage Loss Vrf = –30 dBm, V_{CC} = 4.0 V to 2.0 V	–	AF_{loss}	 –8.0	 –1.5	 –	dB
Meter Drive Output Voltage (No Modulation) V_{rf} = –100 dBm V_{rf} = –70 dBm V_{rf} = –40 dBm	13	M_{Drv} MV1 MV2 MV3	 – 1.1 2.0	 0.3 1.5 2.5	 0.5 1.9 3.1	Vdc
Filter Amp Gain R_S = 600 Ω , f_S = 10 kHz, V_{fa} = 1.0 mVrms	–	$A_{V(Amp)}$	 47	 50	 –	dB
Mixer Conversion Gain V_{rf} = –40 dBm, R_L = 1.8 kΩ	–	$A_{V(Mix)}$	 14	 20	 –	dB
Signal to Noise Ratio V_{rf} = –30 dBm	–	s/n	 36	 67	 –	dB
Total Harmonic Distortion V_{rf} = –30 dBm, BW = 400 Hz to 30 kHz	–	THD	 –	 0.6	 3.4	%
Detector Output Impedance	9	Z_O	–	450	–	Ω
Detector Output Voltage (No Modulation) V_{rf} = –30 dBm	9	DV_O	 –	 1.45	 –	Vdc
Meter Drive V_{rf} = –100 to –40 dBm	13	M_O	 –	 0.8	 –	µA/dB
Meter Drive Dynamic Range RF_{In} IF_{In} (455 kHz)	13	MVD	 – –	 60 80	 – –	dB
Mixer Third Order Input Intercept Point f1 = 58.125 MHz f2 = 58.1375 MHz	–	ITO_{Mix}	 –	 –22	 –	dBm
Mixer Input Resistance	16	R_{in}	–	3.3	–	kΩ
Mixer Input Capacitance	16	C_{in}	–	2.2	–	pF

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 4.0 Vdc, T_A = 25°C, unless otherwise noted)

Characteristic	Pin	Symbol	Min	Typ	Max	Unit
Drain Current (No Input Signal)	4					mA
Squelch Off, V_{sq} = 2.0 Vdc		Icc1	–	3.2	4.2	
Squelch On, V_{sq} = 0 Vdc		Icc2	–	3.6	4.8	
Squelch Off, V_{CC} = 2.0 to 9.0 V		dIcc1	–	1.0	2.0	
Detector Output (No Input Signal)	9	V9				Vdc
DC Voltage, V8 = V_{CC}			0.9	1.6	2.3	
Filter Output (No Input Signal)	11					Vdc
DC Voltage		V11	1.5	2.5	3.5	
Voltage Change, V_{CC} = 2.0 to 9.0 V		dV11	2.0	5.0	8.0	
Trigger Hysteresis	–	Hys	34	57	80	mV

Figure 1. MC3371 Functional Block Diagram and Test Fixture Schematic

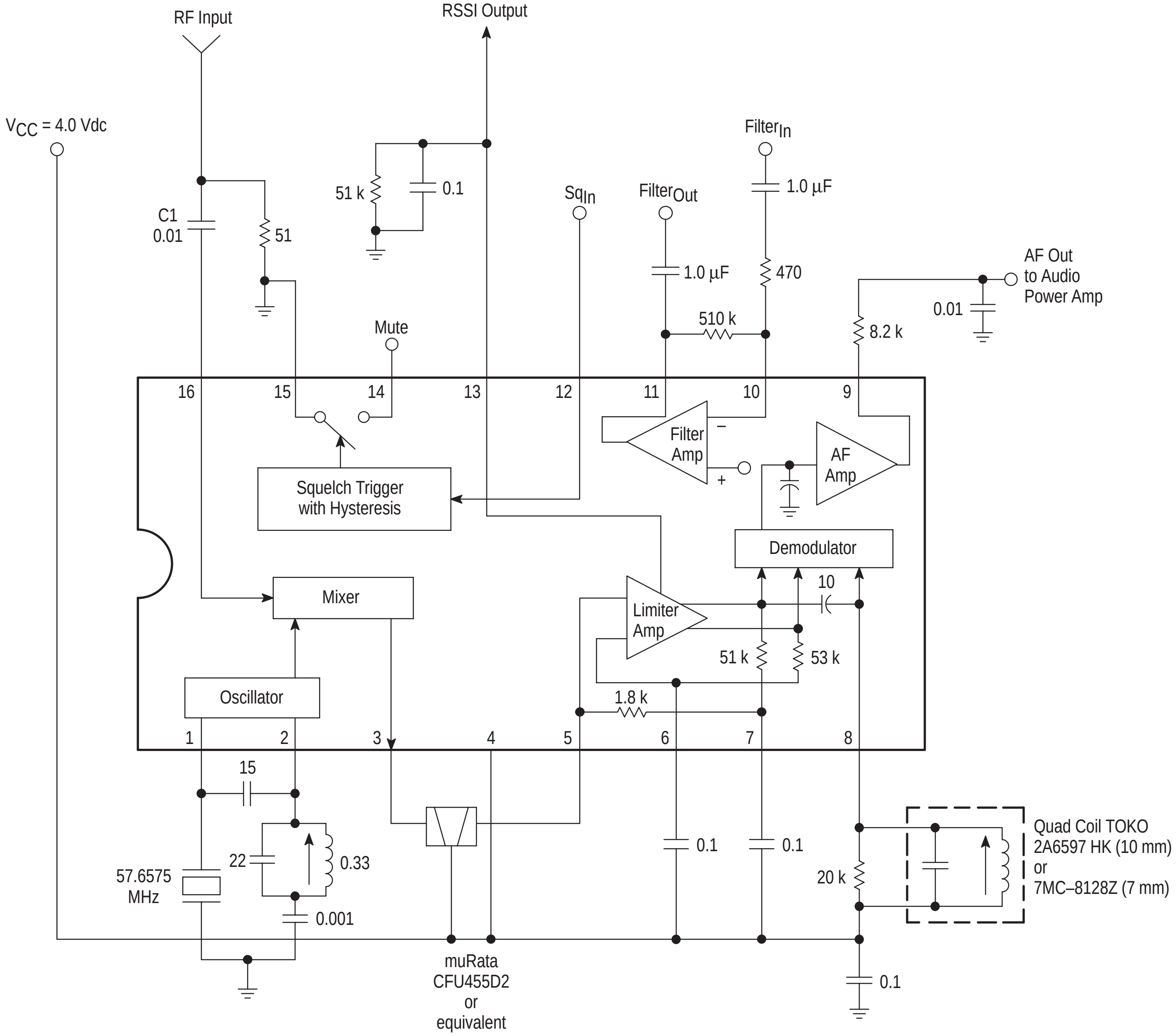
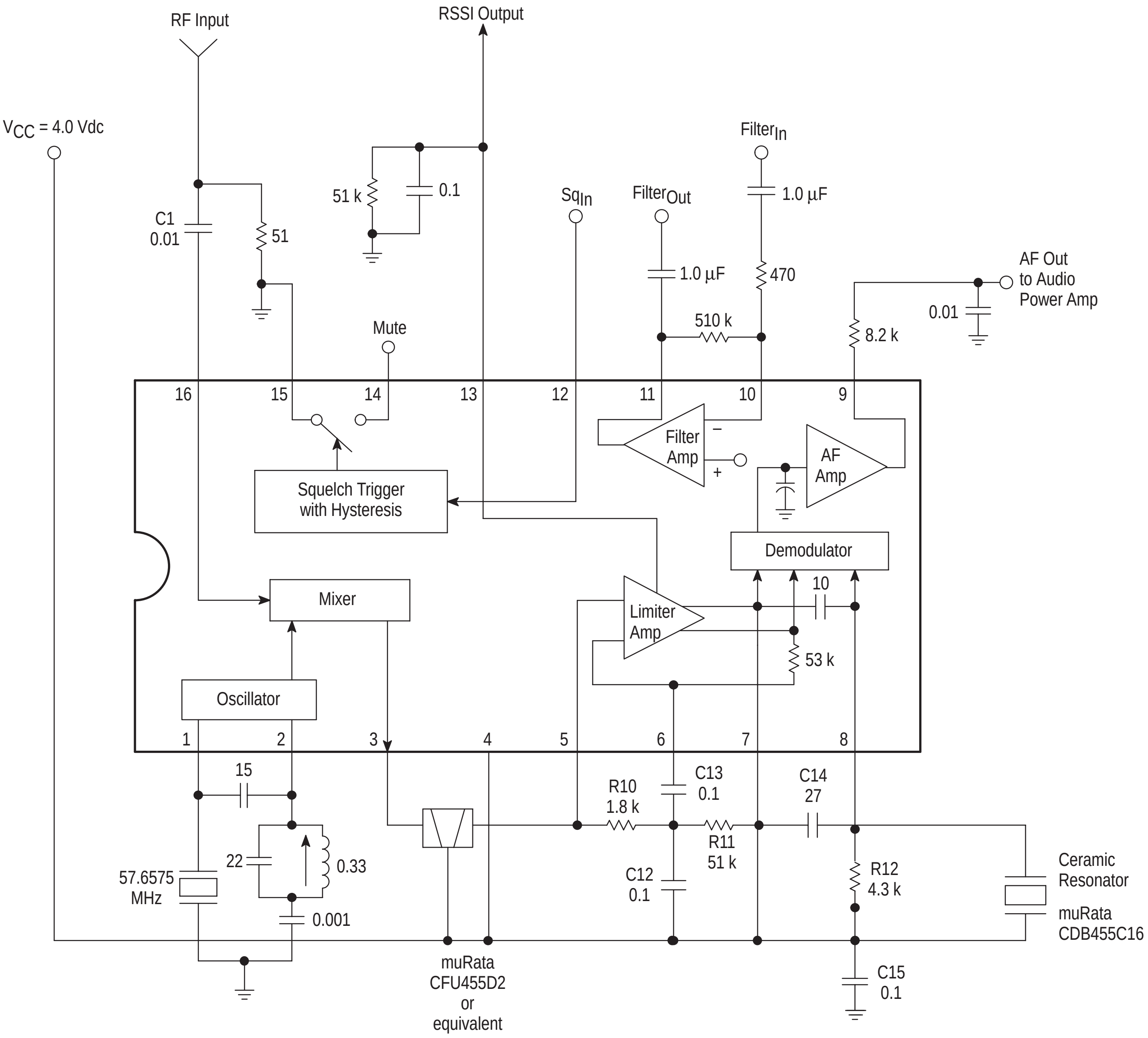


Figure 2. MC3372 Functional Block Diagram and Test Fixture Schematic



TYPICAL CURVES

(Unmatched Input)

Figure 3. Total Harmonic Distortion versus Temperature

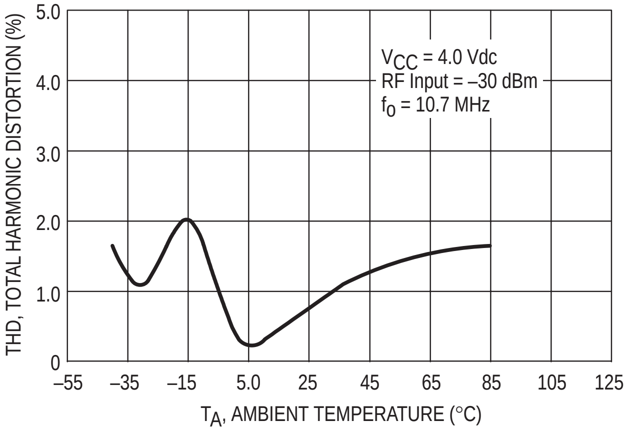


Figure 4. RSSI versus RF Input

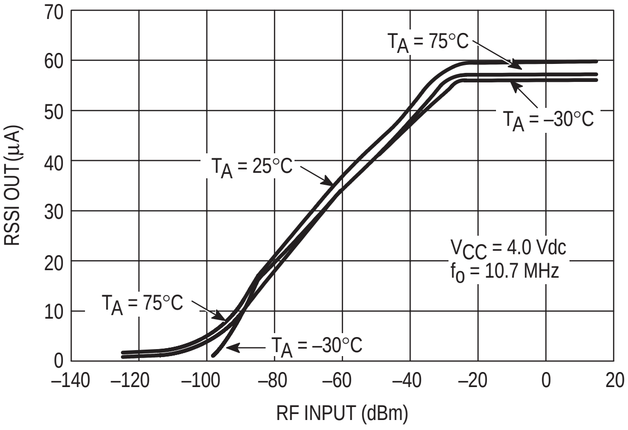


Figure 5. RSSI Output versus Temperature

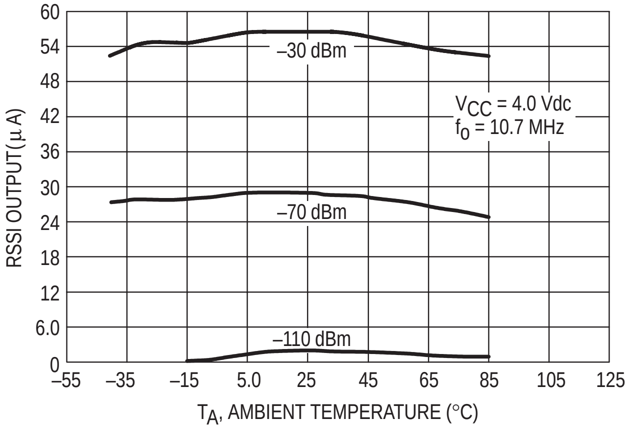


Figure 6. Mixer Output versus RF Input

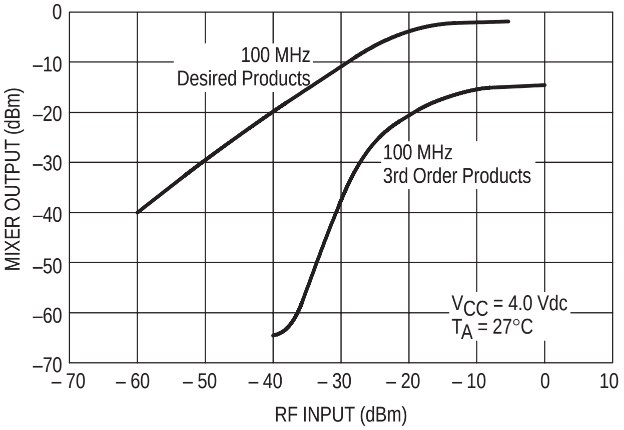


Figure 7. Mixer Gain versus Supply Voltage

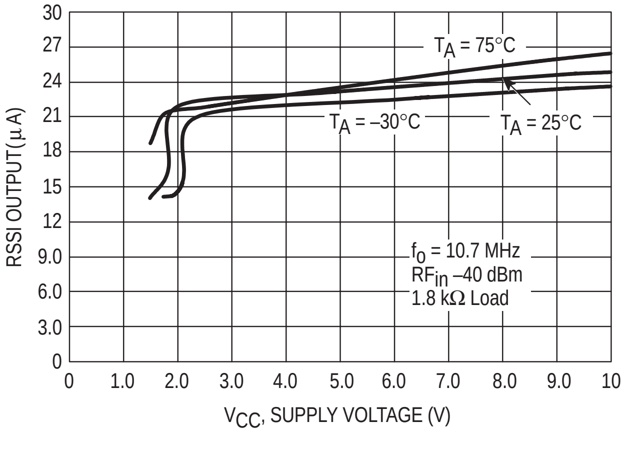
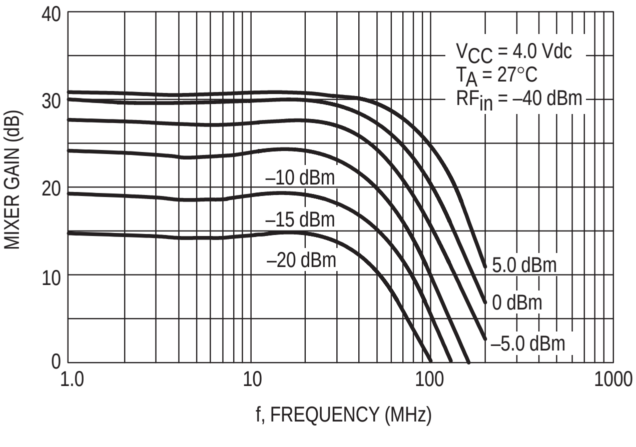
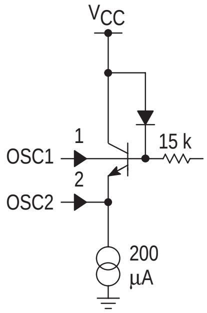
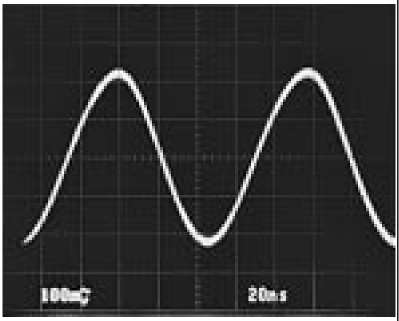
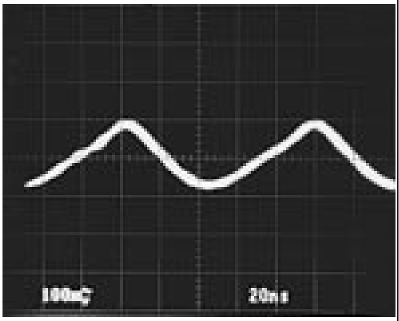
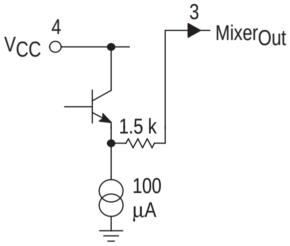
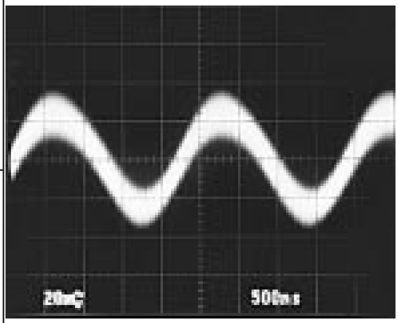
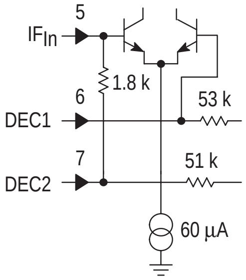
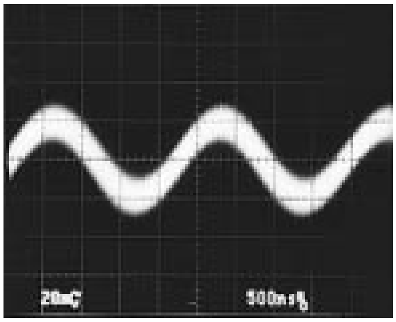
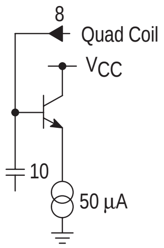
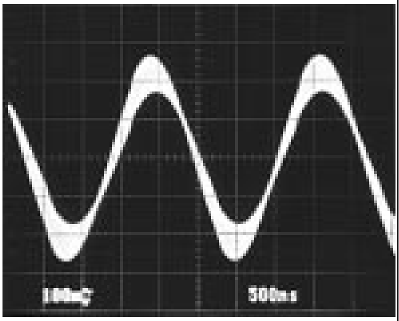


Figure 8. Mixer Gain versus Frequency



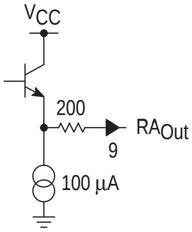
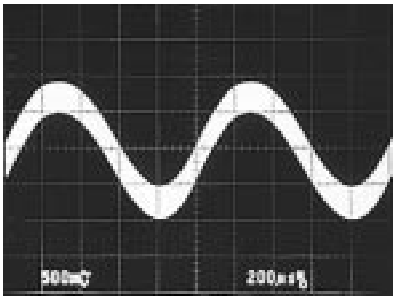
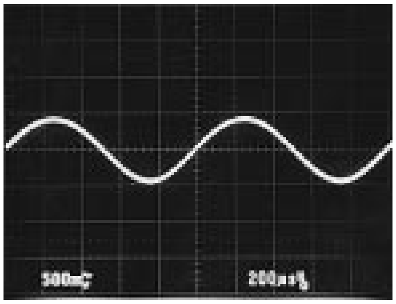
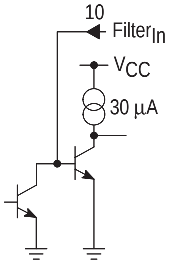
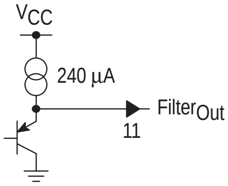
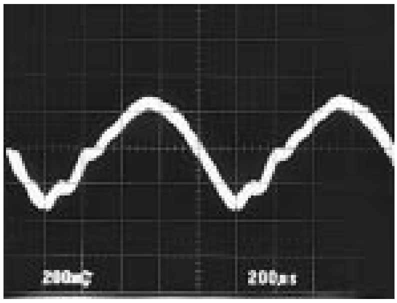
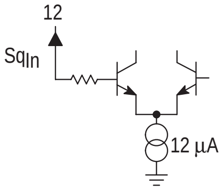
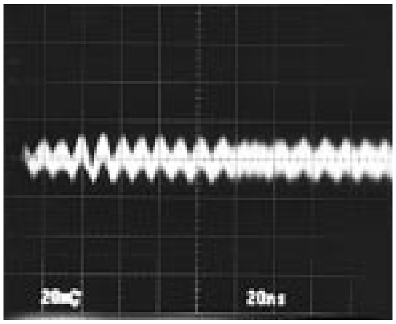
MC3371 PIN FUNCTION DESCRIPTION

OPERATING CONDITIONS V_{CC} = 4.0 Vdc, RF_{In} = 100 µV, f_{mod} = 1.0 kHz, f_{dev} = 3.0 kHz. MC3371 at f_{RF} = 10.7 MHz (see Figure 11).

Pin	Symbol	Internal Equivalent Circuit	Description	Waveform
1	OSC1		The base of the Colpitts oscillator. Use a high impedance and low capacitance probe or a “sniffer” to view the wave–form without altering the frequency. Typical level is 450 mVpp.	
2	OSC2		The emitter of the Colpitts oscillator. Typical signal level is 200 mVpp. Note that the signal is somewhat distorted compared to that on Pin 1.	
3	MX_{Out}		Output of the Mixer. Riding on the 455 kHz is the RF carrier component. The typical level is approximately 60 mVpp.	
4	V_{CC}		Supply Voltage –2.0 to 9.0 Vdc is the operating range. V_{CC} is decoupled to ground.	
5	IF_{In}		Input to the IF amplifier after passing through the 455 kHz ceramic filter. The signal is attenuated by the filter. The typical level is approximately 50 mVpp.	
6 7	DEC1 DEC2		IF Decoupling. External 0.1 µF capacitors connected to V_{CC}.	
8	Quad Coil		Quadrature Tuning Coil. Composite (not yet demodulated) 455 kHz IF signal is present. The typical level is 500 mVpp.	

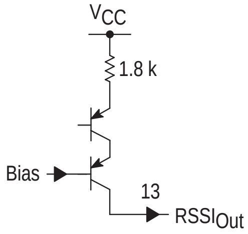
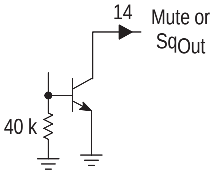
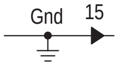
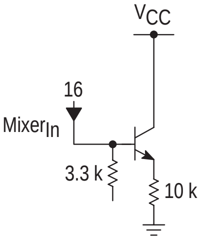
MC3371 PIN FUNCTION DESCRIPTION (continued)

OPERATING CONDITIONS V_{CC} = 4.0 Vdc, RF_{In} = 100 µV, f_{mod} = 1.0 kHz, f_{dev} = 3.0 kHz. MC3371 at f_{RF} = 10.7 MHz (see Figure 11).

Pin	Symbol	Internal Equivalent Circuit	Description	Waveform
9	RA		Recovered Audio. This is a composite FM demodulated output having signal and carrier component. The typical level is 1.4 Vpp.	
			The filtered recovered audio has the carrier component removed and is typically 800 mVpp.	
10	Fil_{In}		Filter Amplifier Input	
11	Fil_{Out}		Filter Amplifier Output. The typical signal level is 400 mVpp.	
12	Sq_{In}		Squelch Input. See discussion in application text.	

MC3371 PIN FUNCTION DESCRIPTION (continued)

OPERATING CONDITIONS V_{CC} = 4.0 Vdc, RF_{In} = 100 µV, f_{mod} = 1.0 kHz, f_{dev} = 3.0 kHz. MC3371 at f_{RF} = 10.7 MHz (see Figure 11).

Pin	Symbol	Internal Equivalent Circuit	Description	Waveform
13	RSSI		RSSI Output. Referred to as the Received Signal Strength Indicator or RSSI. The chip sources up to 60 µA over the linear 60 dB range. This pin may be used many ways, such as: AGC, meter drive and carrier triggered squelch circuit.	
14	MUTE		Mute Output. See discussion in application text.	
15	Gnd		Ground. The ground area should be continuous and unbroken. In a two–sided layout, the component side has the ground plane. In a one–sided layout, the ground plane fills around the traces on the circuit side of the board and is not interrupted.	
16	MIX_{In}		Mixer Input – Series Input Impedance: @ 10 MHz: 309 – j33 Ω @ 45 MHz: 200 – j13 Ω	

*Other pins are the same as pins in MC3371.

MC3372 PIN FUNCTION DESCRIPTION

OPERATING CONDITIONS V_{CC} = 4.0 Vdc, RF_{In} = 100 µV, f_{mod} = 1.0 kHz, f_{dev} = 3.0 kHz. MC3372 at f_{RF} = 45 MHz (see Figure 13).

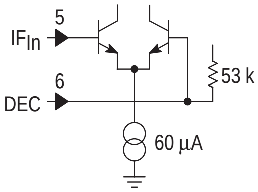
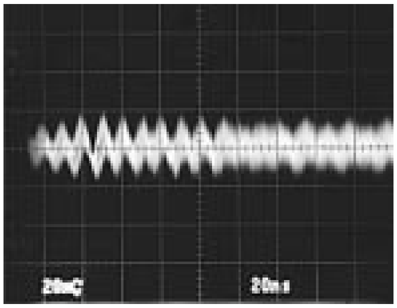
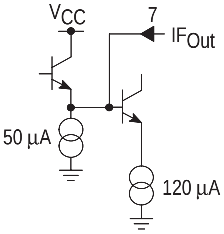
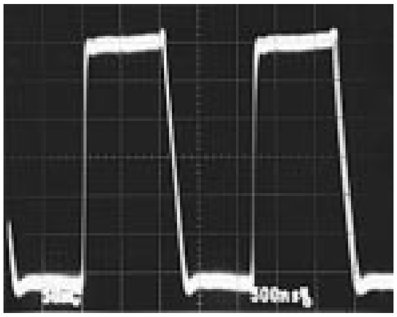
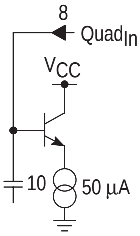
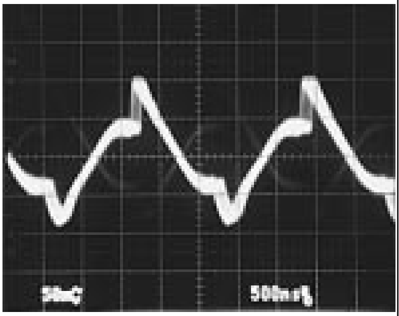
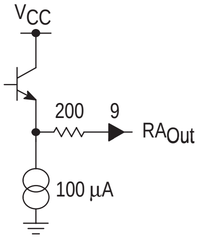
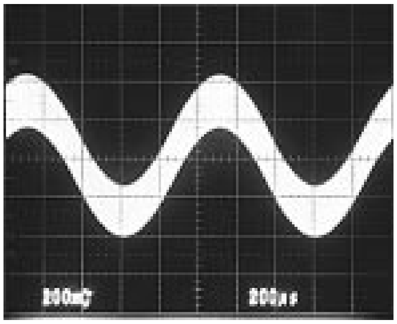
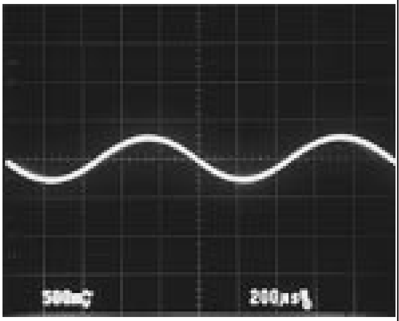
Pin	Symbol	Internal Equivalent Circuit	Description	Waveform
5	IF_{In}		IF Amplifier Input	
6	DEC1		IF Decoupling. External 0.1 µF capacitors connected to V_{CC}.	
7	IF_{Out}		IF Amplifier Output Signal level is typically 300 mVpp.	
8	$Quad_{In}$		Quadrature Detector Input. Signal level is typically 150 mVpp.	
9	RA		Recovered Audio. This is a composite FM demodulated output having signal and carrier components. Typical level is 800 mVpp.	
			The filtered recovered audio has the carrier signal removed and is typically 500 mVpp.	

Figure 9. MC3371 Circuit Schematic

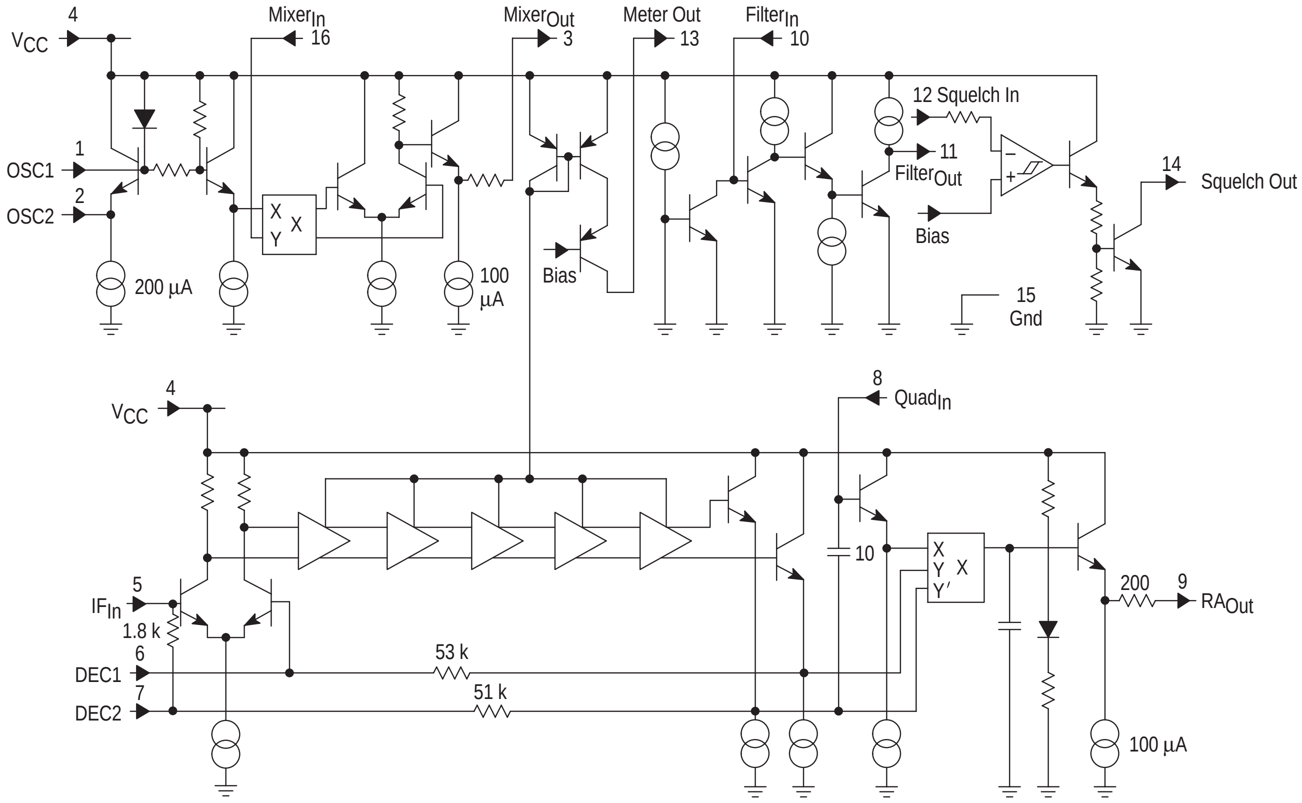
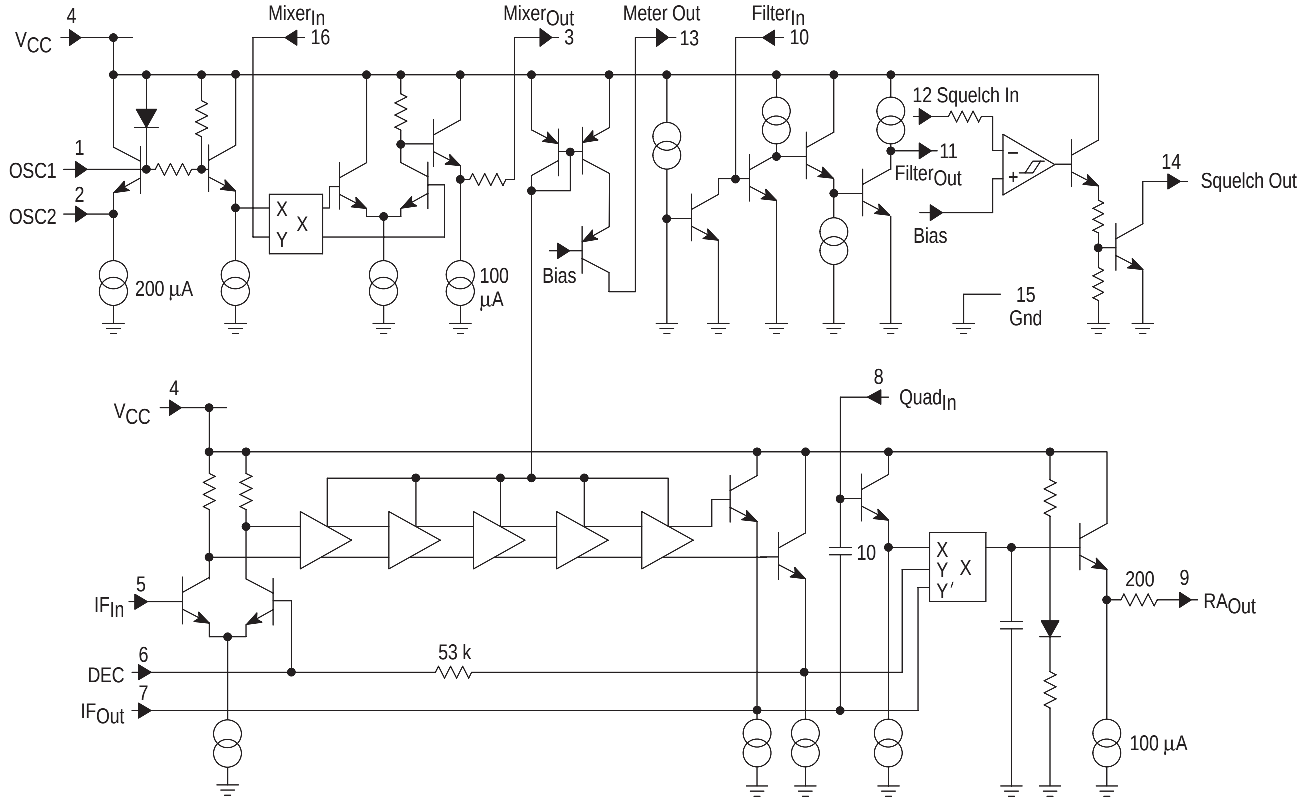


Figure 10. MC3372 Circuit Schematic



CIRCUIT DESCRIPTION

The MC3371 and MC3372 are low power narrowband FM receivers with an operating frequency of up to 60 MHz. Its low voltage design provides low power drain, excellent sensitivity, and good image rejection in narrowband voice and data link applications.

This part combines a mixer, an IF (intermediate frequency) limiter with a logarithmic response signal strength indicator, a quadrature detector, an active filter and a squelch trigger circuit. In a typical application, the mixer amplifier converts an RF input signal to a 455 kHz IF signal. Passing through an external bandpass filter, the IF signal is fed into a limiting amplifier and detection circuit where the audio signal is recovered. A conventional quadrature detector is used.

The absence of an input signal is indicated by the presence of noise above the desired audio frequencies. This “noise band” is monitored by an active filter and a detector. A squelch switch is used to mute the audio when noise or a tone is present. The input signal level is monitored by a meter drive circuit which detects the amount of IF signal in the limiting amplifier.

APPLICATIONS INFORMATION

The oscillator is an internally biased Colpitts type with the collector, base, and emitter connections at Pins 4, 1 and 2 respectively. This oscillator can be run under crystal control. For fundamental mode crystals use crystal characterized parallel resonant for 32 pF load. For higher frequencies, use 3rd overtone series mode type crystals. The coil (L2) and resistor RD (R13) are needed to ensure proper and stable operation at the LO frequency (see Figure 13, 45 MHz application circuit).

The mixer is doubly balanced to reduce spurious radiation. Conversion gain stated in the AC Electrical Characteristics table is typically 20 dB. This power gain measurement was made under stable conditions using a 50 Ω source at the input and an external load provided by a 455 kHz ceramic filter at the mixer output which is connected to the V_{CC} (Pin 4) and IF input (Pin 5). The filter impedance closely matches the 1.8 kΩ internal load resistance at Pin 3 (mixer output). Since the input impedance at Pin 16 is strongly influenced by a 3.3 kΩ internal biasing resistor and has a low capacitance, the useful gain is actually much higher than shown by the standard power gain measurement. The Smith Chart plot in Figure 17 shows the measured mixer input impedance versus input frequency with the mixer input matched to a 50 Ω source impedance at the given frequencies. In order to assure stable operation under matched conditions, it is necessary to provide a shunt resistor to ground. Figures 11, 12 and 13 show the input networks used to derive the mixer input impedance data.

Following the mixer, a ceramic bandpass filter is recommended for IF filtering (i.e. 455 kHz types having a bandwidth of ±2.0 kHz to ±15 kHz with an input and output impedance from 1.5 kΩ to 2.0 kΩ). The 6 stage limiting IF amplifier has approximately 92 dB of gain. The MC3371 and MC3372 are different in the limiter and quadrature detector circuits. The MC3371 has a 1.8 kΩ and a 51 kΩ resistor providing internal dc biasing and the output of the limiter is internally connected, both directly and through a 10 pF capacitor to the quadrature detector; whereas, in the MC3372 these components are not provided internally. Thus, in the MC3371, no external components are necessary to match the 455 kHz ceramic filter, while in the MC3372, external 1.8 kΩ and 51 kΩ biasing resistors are needed between Pins 5 and 7, respectively (see Figures 12 and 13).

In the MC3371, a parallel LCR quadrature tank circuit is connected externally from Pin 8 to V_{CC} (similar to the MC3361). In the MC3372, a quadrature capacitor is needed externally from Pin 7 to Pin 8 and a parallel LC or a ceramic discriminator with a damping resistor is also needed from Pin 8 to V_{CC} (similar to the MC3357). The above external quadrature circuitry provides 90° phase shift at the IF center frequency and enables recovered audio.

The damping resistor determines the peak separation of the detector and is somewhat critical. As the resistor is decreased, the separation and the bandwidth is increased but the recovered audio is decreased. Receiver sensitivity is dependent on the value of this resistor and the bandwidth of the 455 kHz ceramic filter.

On the chip the composite recovered audio, consisting of carrier component and modulating signal, is passed through a low pass filter amplifier to reduce the carrier component and then is fed to Pin 9 which has an output impedance of 450 Ω. The signal still requires further filtering to eliminate the carrier component, deemphasis, volume control, and further amplification before driving a loudspeaker. The relative level of the composite recovered audio signal at Pin 9 should be considered for proper interaction with an audio post amplifier and a given load element. The MC13060 is recommended as a low power audio amplifier.

The meter output indicates the strength of the IF level and the output current is proportional to the logarithm of the IF input signal amplitude. A maximum source current of 60 µA is available and can be used to drive a meter and to detect a carrier presence. This is referred to as a Received Strength Signal Indicator (RSSI). The output at Pin 13 provides a current source. Thus, a resistor to ground yields a voltage proportional to the input carrier signal level. The value of this resistor is estimated by (V_{CC}(Vdc) – 1.0 V)/60 µA; so for V_{CC} = 4.0 Vdc, the resistor is approximately 50 kΩ and provides a maximum voltage swing of about 3.0 V.

A simple inverting op amp has an output at Pin 11 and the inverting input at Pin 10. The noninverting input is connected to 2.5 V. The op amp may be used as a noise triggered squelch or as an active noise filter. The bandpass filter is designed with external impedance elements to discriminate between frequencies. With an external AM detector, the filtered audio signal is checked for a tone signal or for the presence of noise above the normal audio band. This information is applied to Pin 12.

An external positive bias to Pin 12 sets up the squelch trigger circuit such that the audio mute (Pin 14) is open or connected to ground. If Pin 12 is pulled down to 0.9 V or below by the noise or tone detector, Pin 14 is internally shorted to ground. There is about 57 mV of hyteresis at Pin 12 to prevent jitter. Audio muting is accomplished by connecting Pin 14 to the appropriate point in the audio path between Pin 9 and an audio amplifier. The voltage at Pin 14 should not be lower than –0.7 V; this can be assured by connecting Pin 14 to the point that has no dc component.

Another possible application of the squelch switch may be as a carrier level triggered squelch circuit, similar to the MC3362/MC3363 FM receivers. In this case the meter output can be used directly to trigger the squelch switch when the RF input at the input frequency falls below the desired level. The level at which this occurs is determined by the resistor placed between the meter drive output (Pin 13) and ground (Pin 15).

Figure 11. Typical Application for MC3371 at 10.7 MHz

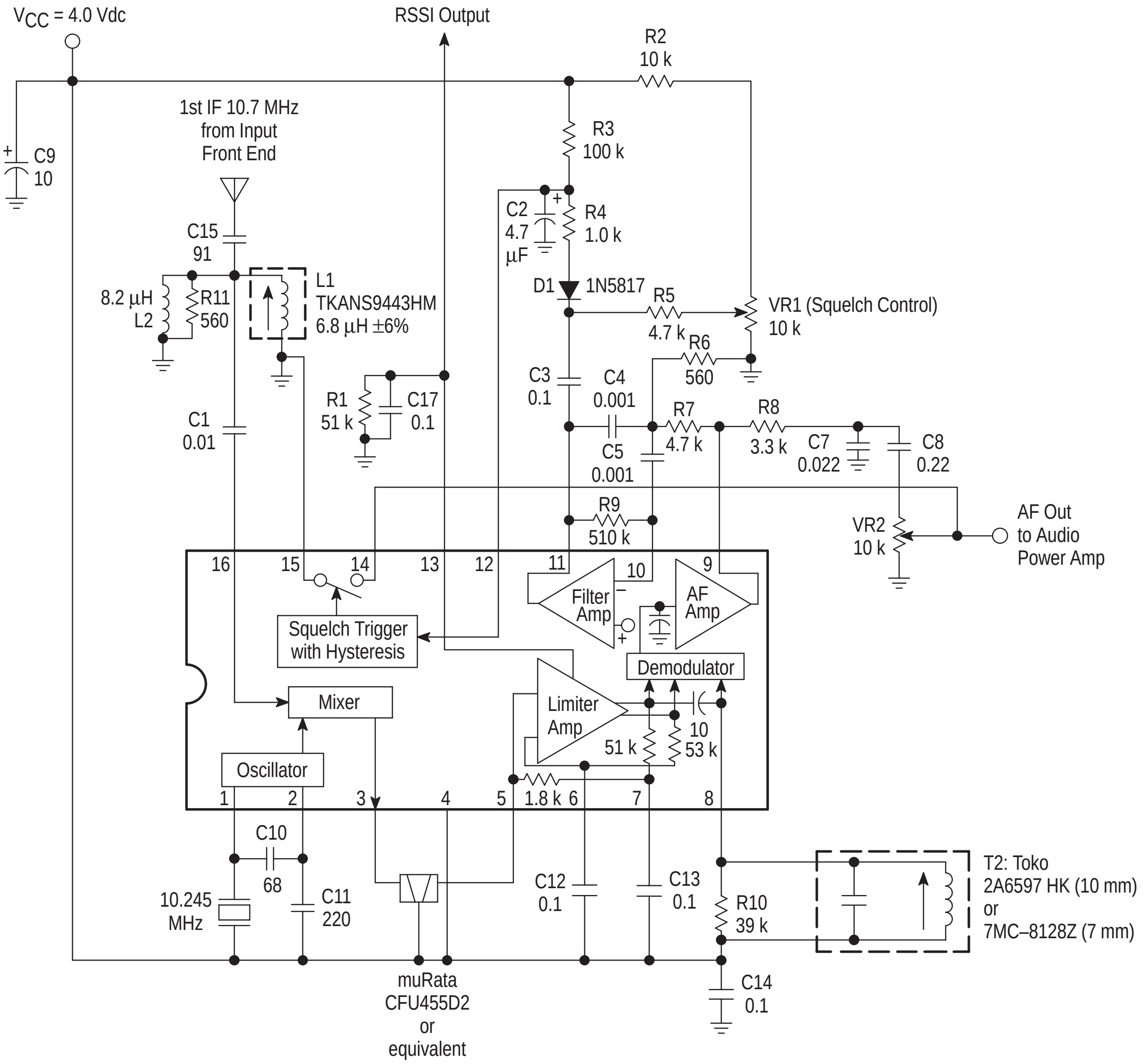


Figure 12. Typical Application for MC3372 at 10.7 MHz

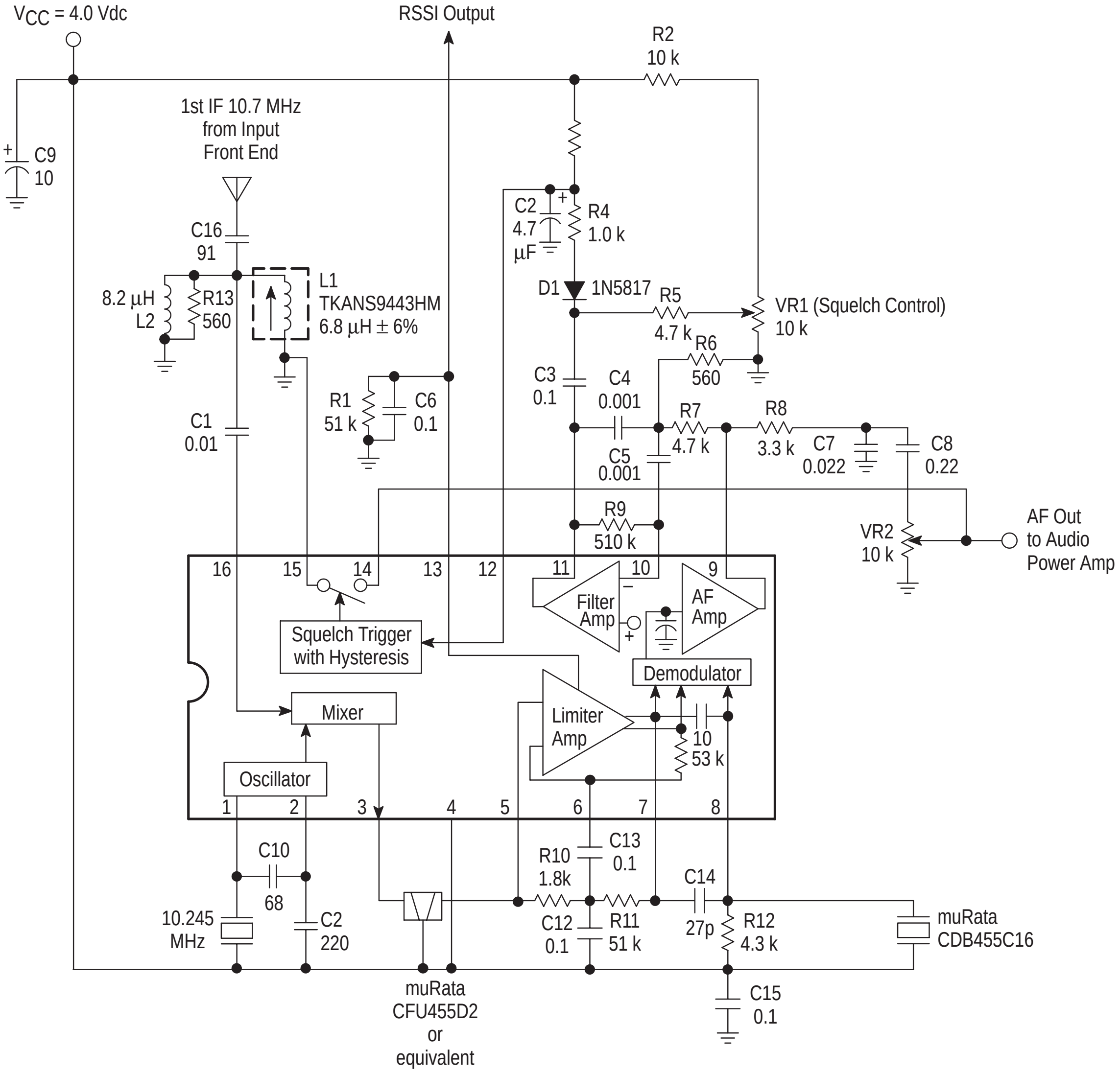


Figure 13. Typical Application for MC3372 at 45 MHz

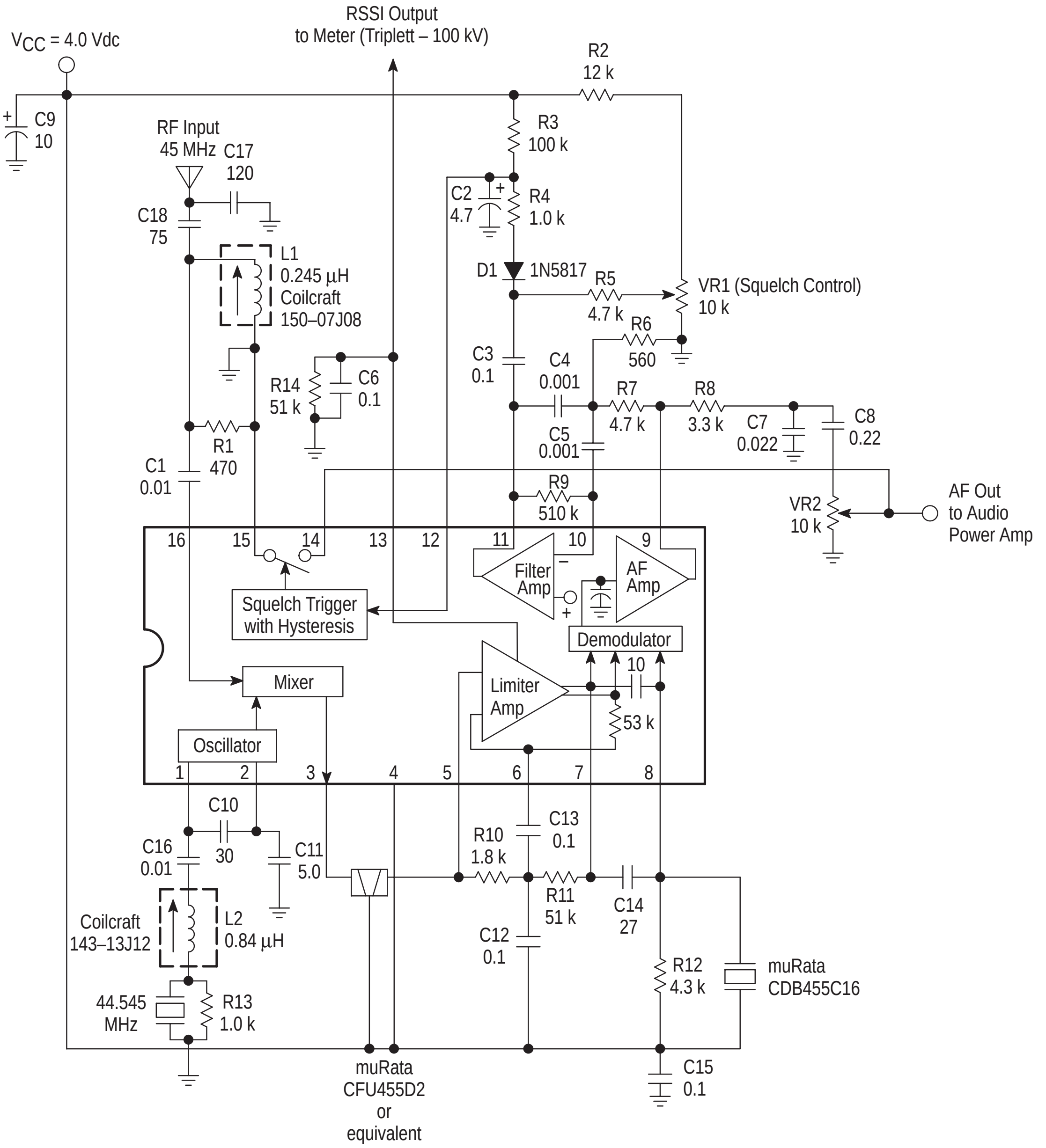


Figure 14. RSSI Output versus RF Input

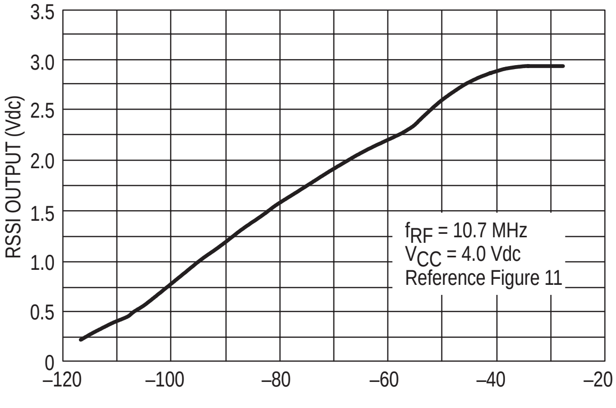


Figure 15. RSSI Output versus RF Input

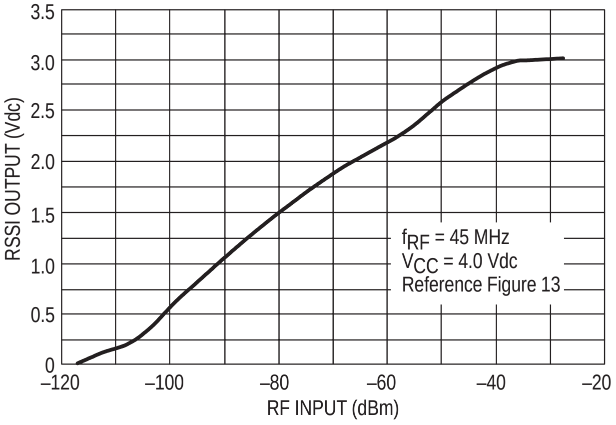
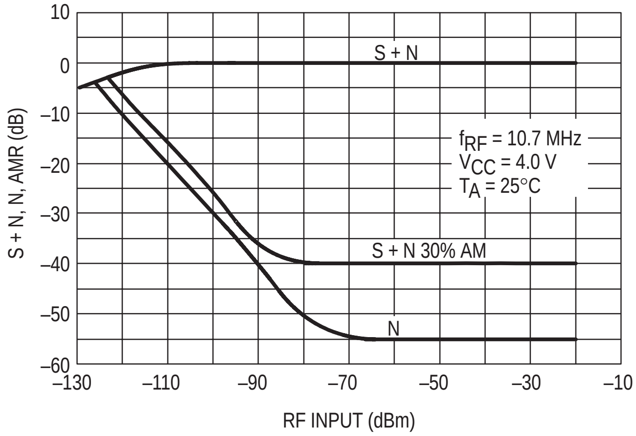


Figure 16. S + N, N, AMR versus Input



* Reference Figures 11, 12 and 13

Figure 17. Mixer Input Impedance versus Frequency

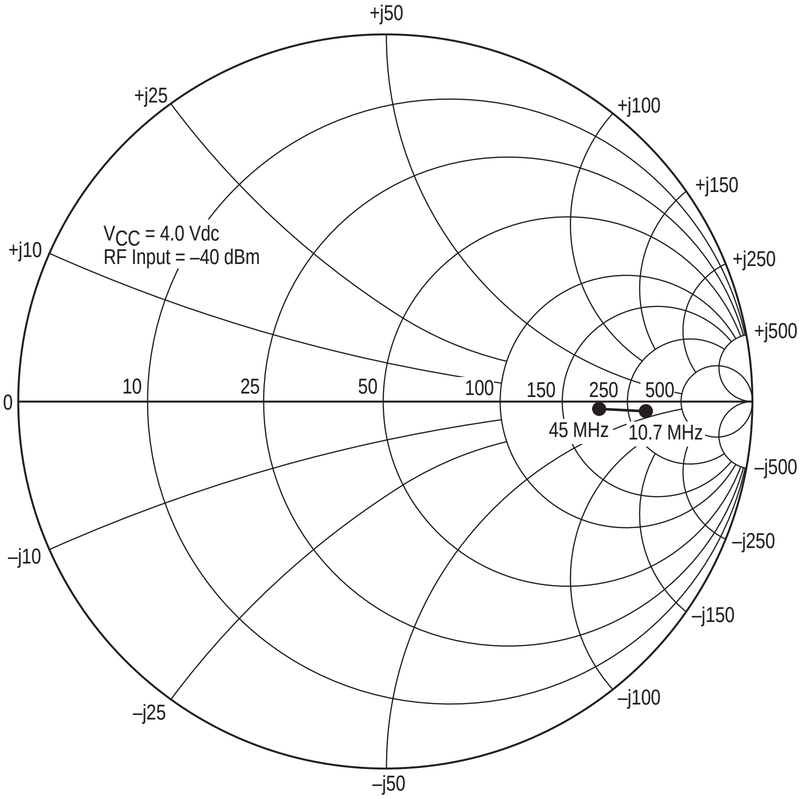


Figure 18. MC3371 PC Board Component View with Matched Input at 10.7 MHz

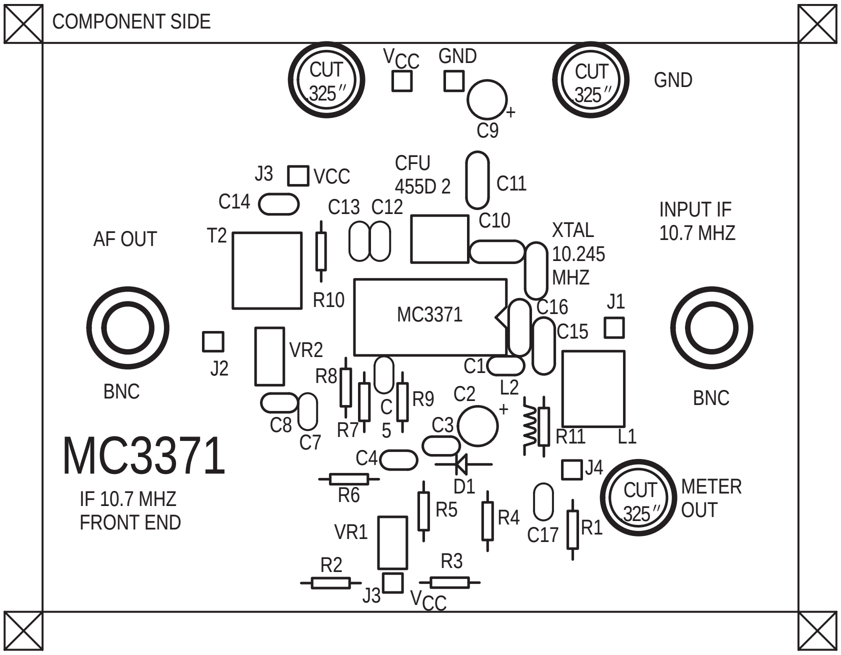
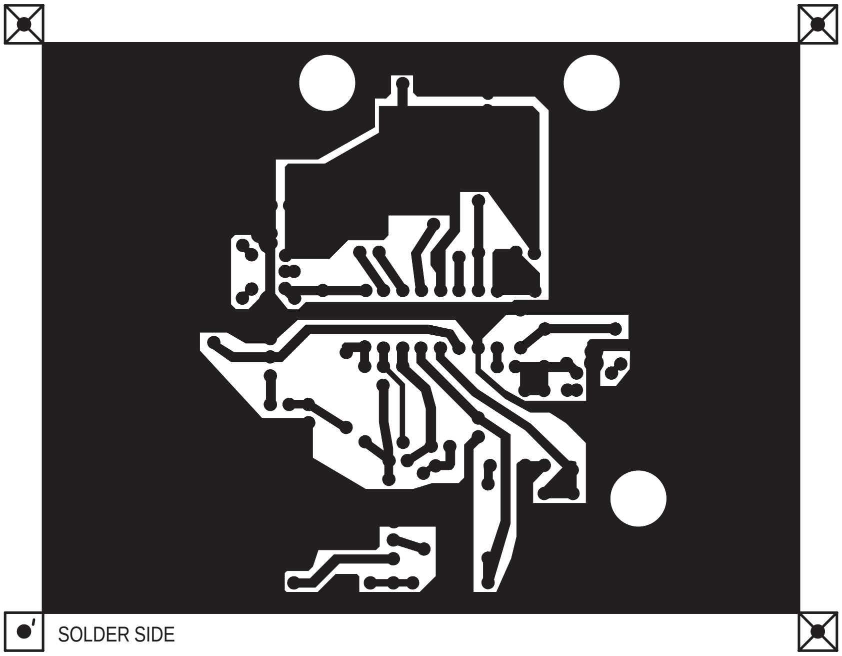


Figure 19. MC3371 PC Board Circuit or Solder Side as Viewed through Component Side



Above PC Board is laid out for the circuit in Figure 11.

Figure 20. MC3372P PC Board Component View with Matched Input at 10.7 MHz

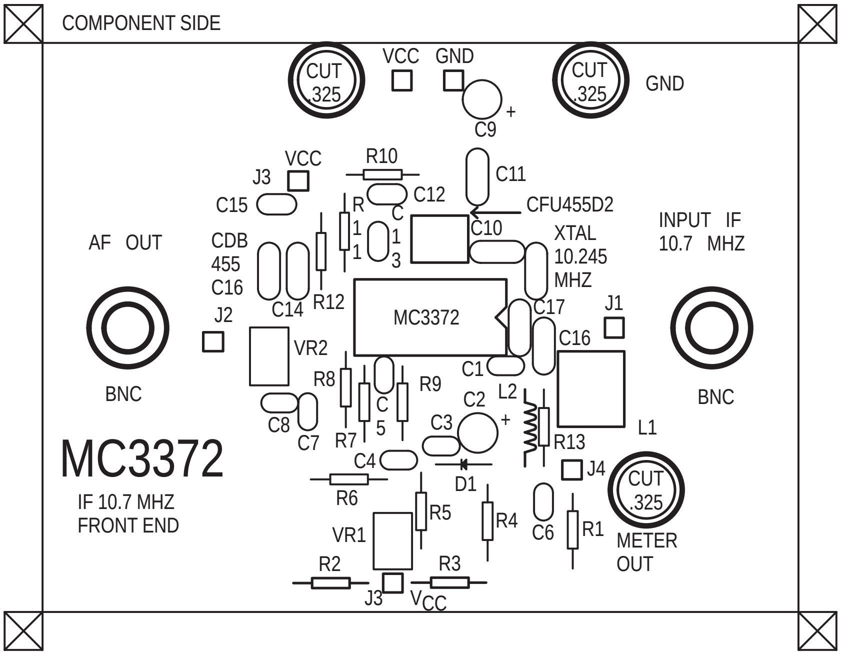
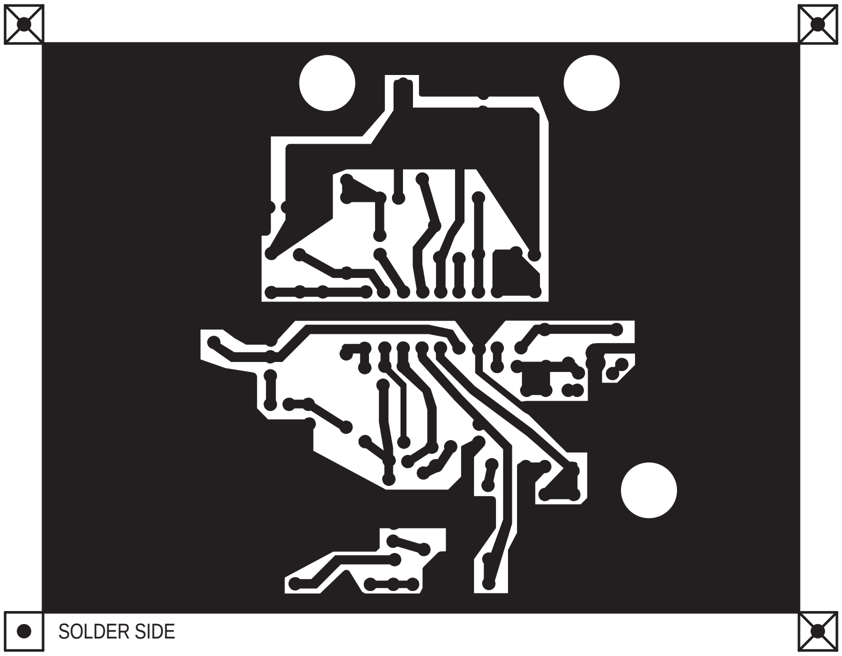


Figure 21. MC3372P PC Board Circuit or Solder Side as Viewed through Component Side



Above PC Board is laid out for the circuit in Figure 12.

MOTOROLA

MC3363

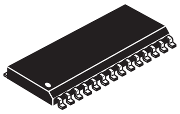
Low Power Dual Conversion FM Receiver

The MC3363 is a single chip narrowband VHF FM radio receiver. It is a dual conversion receiver with RF amplifier transistor, oscillators, mixers, quadrature detector, meter drive/carrier detect and mute circuitry. The MC3363 also has a buffered first local oscillator output for use with frequency synthesizers, and a data slicing comparator for FSK detection.

- Wide Input Bandwidth – 200 MHz Using Internal Local Oscillator
  – 450 MHz Using External Local Oscillator
- RF Amplifier Transistor
- Muting Operational Amplifier
- Complete Dual Conversion
- Low Voltage: V_{CC} = 2.0 V to 6.0 Vdc
- Low Drain Current: I_{CC} = 3.6 mA (Typical) at V_{CC} = 3.0 V, Excluding RF Amplifier Transistor
- Excellent Sensitivity: Input 0.3 µV (Typical) for 12 dB SINAD Using Internal RF Amplifier Transistor
- Data Shaping Comparator
- Received Signal Strength Indicator (RSSI) with 60 dB Dynamic Range
- Low Number of External Parts Required
- Manufactured in Motorola's MOSAIC® Process Technology

LOW POWER DUAL CONVERSION FM RECEIVER

SEMICONDUCTOR TECHNICAL DATA

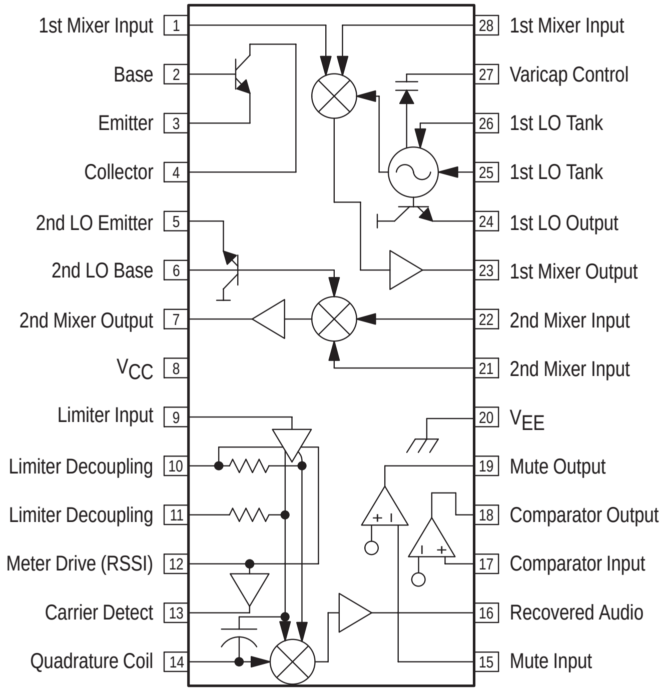


DW SUFFIX
PLASTIC PACKAGE
CASE 751F
(SO-28L)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC3363DW	T_A = – 40 to +85°C	SO–28L

Figure 1. Pin Connections and Representative Block Diagram



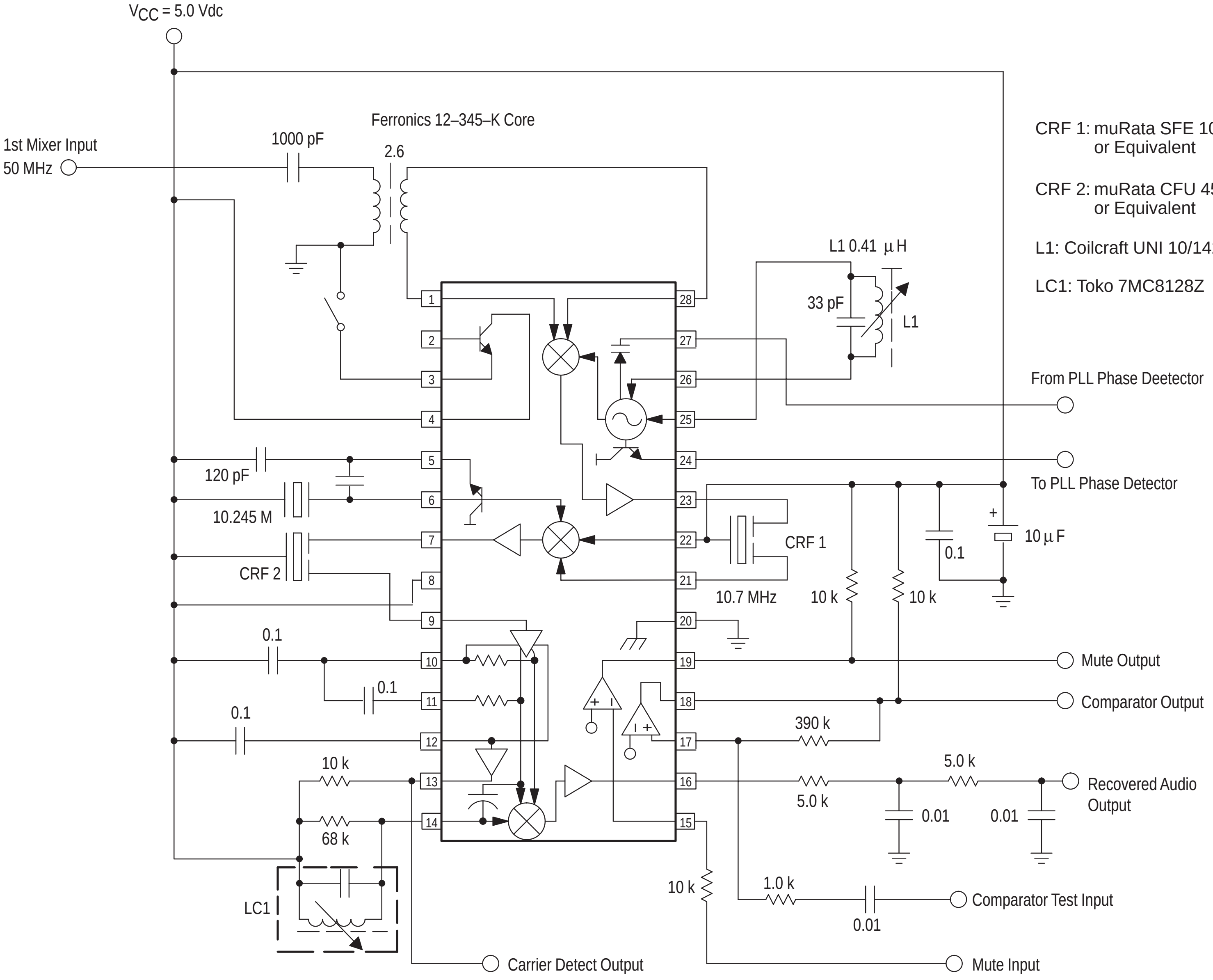
MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Pin	Symbol	Value	Unit
Power Supply Voltage	8	$V_{CC(max)}$	7.0	Vdc
Operating Supply Voltage Range (Recommended)	8	V_{CC}	2.0 to 6.0	Vdc
Input Voltage (V_{CC} = 5.0 Vdc)	1, 28	$V_{1–28}$	1.0	Vrms
Mute Output Voltage	19	V_{19}	– 0.7 to 8.0	Vpk
Junction Temperature	–	T_J	150	°C
Operating Ambient Temperature Range	–	T_A	– 40 to +85	°C
Storage Temperature Range	–	T_{stg}	– 65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 Vdc, f_o = 49.7 MHz, Deviation = ±3.0 kHz, T_A = 25°C, Mod 1.0 kHz, test circuit of Figure 2 unless otherwise noted)

Characteristic	Pin	Min	Typ	Max	Units
Drain Current (Carrier Detect Low)	8	–	4.5	8.0	mA
–3.0 dB Limiting Sensitivity (RF Amplifier Not Used)		–	0.7	2.0	µVrms
Input For 12 dB SINAD		–	0.3	–	
20 dB S/N Sensitivity (RF Amplifier Not Used)		–	1.0	–	
1st Mixer Input Resistance (Parallel – Rp)	1, 28	–	690	–	Ω
1st Mixer Input Capacitance (Parallel – Cp)	1, 28	–	7.2	–	pF
1st Mixer Conversion Voltage Gain (A_{vc1}, Open Circuit)		–	18	–	dB
2nd Mixer Conversion Voltage Gain)A_{vc2}, Open Circuit)		–	21	–	
2nd Mixer Input Sensitivity (20 dB S/N) (10.7 MHz i/p)	21	–	10	–	µVrms
Limiter Input Sensitivity (20 dB S/N) (455 kHz i/p)	9	–	100	–	
RF Transistor DC Current Drain	4	1.0	1.5	2.5	mAdc
Noise Output Level (RF Signal = 0 mV)	16	–	70	–	mVrms
Recovered Audio (RF Signal Level = 1.0 mV)	16	120	200	–	mVrms
THD of Recovered Aduio (RF Signal = 1.0 mV)	16	–	2%	–	%
Detector Output Impedance	16	–	400	–	Ω
Series Equivalent Input Impedance	1	–	450–j350	–	
Data (Comparator) Output Voltage – High – Low	18	– 0.1	– 0.1	V_{CC} –	Vdc
Data (Comparator) Threshold Voltage Difference	17	70	110	150	mV
Meter Drive Slope	12	70	100	135	nA/dB
Carrier Detect Threshold (Below V_{CC})	12	0.53	0.64	0.77	Vdc
Mute Output Impedance – High – Low	19	– –	10 25	– –	MΩ

Figure 2. Test Circuit



CRF 1: muRata SFE 10.7 mA
or Equivalent

CRF 2: muRata CFU 455D
or Equivalent

L1: Coilcraft UNI 10/142 10–1/2 Turns

LC1: Toko 7MC8128Z

CIRCUIT DESCRIPTION

The MC3363 is a complete FM narrowband receiver from RF amplifier to audio preamp output. The low voltage dual conversion design yields low power drain, excellent sensitivity and good image rejection in narrowband voice and data link applications.

In the typical application, the input RF signal is amplified by the RF transistor and then the first mixer amplifies the signal and converts the RF input to 10.7 MHz. This IF signal is filtered externally and fed into the second mixer, which further amplifies the signal and converts it to a 455 kHz IF signal. After external bandpass filtering, the low IF is fed into the limiting amplifier and detection circuitry. The audio is recovered using a conventional quadrature detector. Twice-IF filtering is provided internally.

The input signal level is monitored by meter drive circuitry which detects the amount of limiting in the limiting amplifier. The voltage at the meter drive pin determines the state of the carrier detect output, which is active low.

APPLICATIONS INFORMATION

The first local oscillator is designed to serve as the VCO in a PLL frequency synthesized receiver. The MC3363 can operate together with the MC145166/7 to provide a two-chip ten–channel frequency synthesized receiver in the 46/49 cordless telephone band. The MC3363 can also be used with the MC14515X series of CMOS PLL synthesizers and MC120XX series of ECL prescalers in VHF frequency synthesized applications to 200 MHz.

For single channel applications the first local oscillator can be crystal controlled. The circuit of Figure 4 has been used successfully up to 60 MHz. For higher frequencies an external oscillator signal can be injected into Pins 25 and/or 26 — a level of approximately 100 mVrms is recommended. The first mixer′s transfer characteristic is essentially flat to 450 MHz when this approach is used (keeping a constant 10.7 MHz IF frequency). The second local oscillator is a Colpitts type which is typically run at 10.245 MHz under crystal control.

The mixers are doubly balanced to reduce spurious responses. The first and second mixers have conversion gains of 18 dB and 21 dB (typical), respectively. Mixer gain is stable with respect to supply voltage. For both conversions, the mixer impedances and pin layout are designed to allow the user to employ low cost, readily available ceramic filters.

Following the first mixer, a 10.7 MHz ceramic bandpass filter is recommended. The 10.7 MHz filtered signal is then fed into the second mixer input Pin 21, the other input Pin 22 being connected to V_{CC}.

The 455 kHz IF is filtered by a ceramic narrow bandpass filter then fed into the limiter input Pin 9. The limiter has 10 μV sensitivity for –3.0 dB limiting, flat to 1.0 MHz.

The output of the limiter is internally connected to the quadrature detector, including a quadrature capacitor. A parallel LC tank is needed externally from Pin 14 to V_{CC}. A 68 kΩ shunt resistance is included which determines the peak separation of the quadrature detector; a smaller value will lower the Q and expand the deviation range and linearity, but decrease recovered audio and sensitivity.

A data shaping circuit is available and can be coupled to the recovered audio output of Pin 16. The circuit is a comparator which is designed to detect zero crossings of FSK modulation. Data rates of up to 35000 baud are detectable using the comparator. Best sensitivity is obtained when data rates are limited to 1200 baud maximum. Hysteresis is available by connecting a high-valued resistor from Pin 17 to Pin 18. Values below 120 kΩ are not recommended as the input signal cannot overcome the hysteresis.

The meter drive circuitry detects input signal level by monitoring the limiting of the limiting amplifier stages. Figure 5 shows the unloaded current at Pin 12 versus input power. The meter drive current can used directly (RSSI) or can be used to trip the carrier detect circuit at a specified input power.

A muting op amp is provided and can be triggered by the carrier detect output (Pin 13). This provides a carrier level triggered squelch circuit which is activated when the RF input at the desired input frequency falls below a present level. The level at which this occurs is determined by the resistor placed between the meter drive output (Pin 12) and V_{CC}. Values between 80 – 130 kΩ are recommended. This type of squelch is pictured in Figures 3 and 4.

Hysteresis is available by connecting a high-valued resistor Rh between Pins 12 and 13. The formula is:

$$\text{Hyst} = V_{CC} / (\text{Rh} \times 10^{-7})\ \text{dB}$$

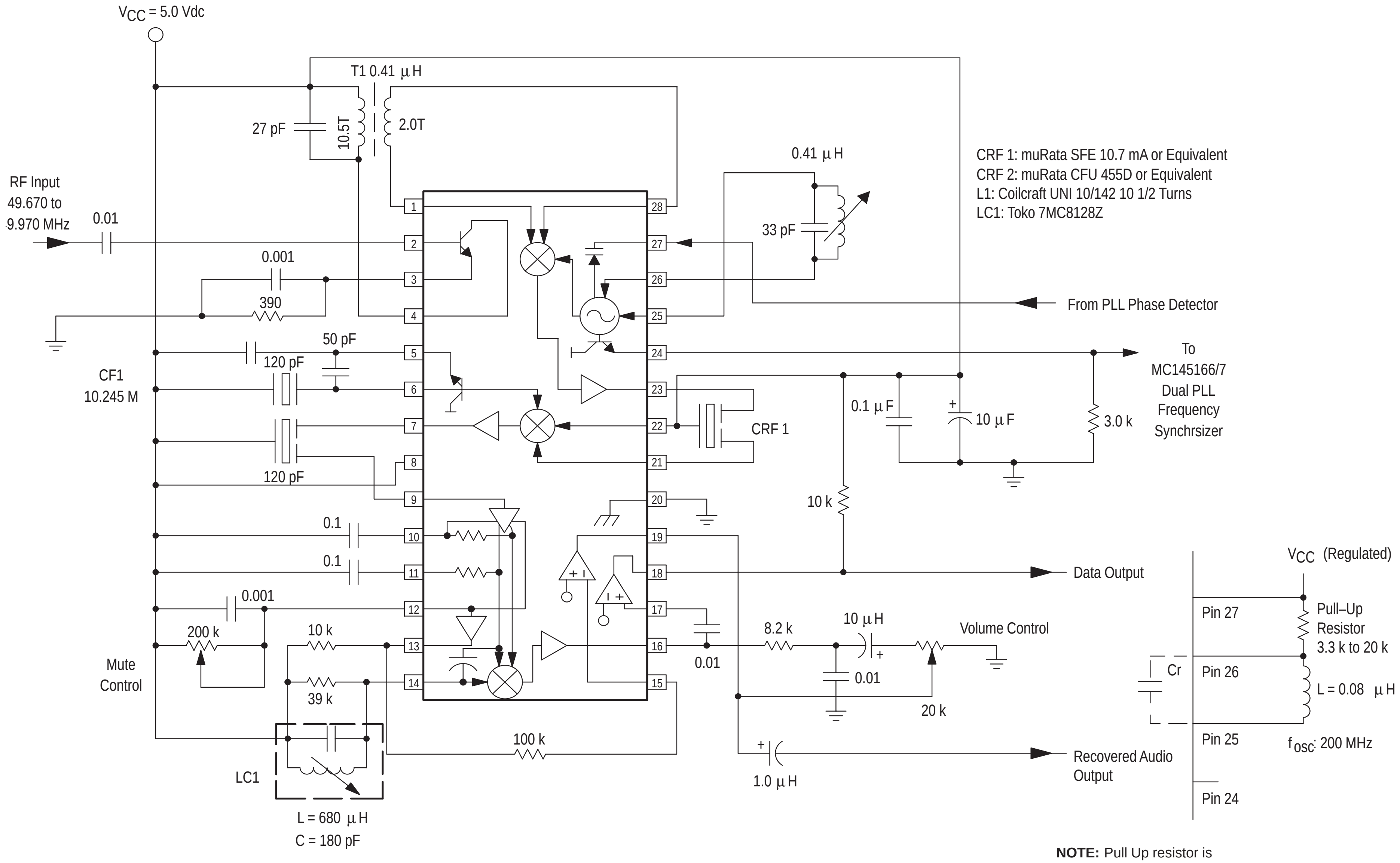
The meter drive can also be used directly to drive a meter or to provide AGC. A current to voltage converter or other linear buffer will be needed for this application.

A second possible application of the op amp would be in a noise triggered squelch circuit, similar to that used with the MC3357/MC3359/MC3361B FM IFs. In this case the op amp would serve as an active noise filter, the output of which would be rectified and compared to a reference on a squelch gate. The MC3363 does not have a dedicated squelch gate, but the NPN RF input stage or data shaping comparator might be used to provide this function if available. The op amp is a basic type with the inverting input and the output available. This application frees the meter drive to allow it to be used as a linear signal strength monitor.

The circuit of Figure 4 is a complete 50 MHz receiver from antenna input to audio preamp output. It uses few components and has good performance. The receiver operates on a single channel and has input sensitivity of < 0.3 μV for 12 dB SINAD.

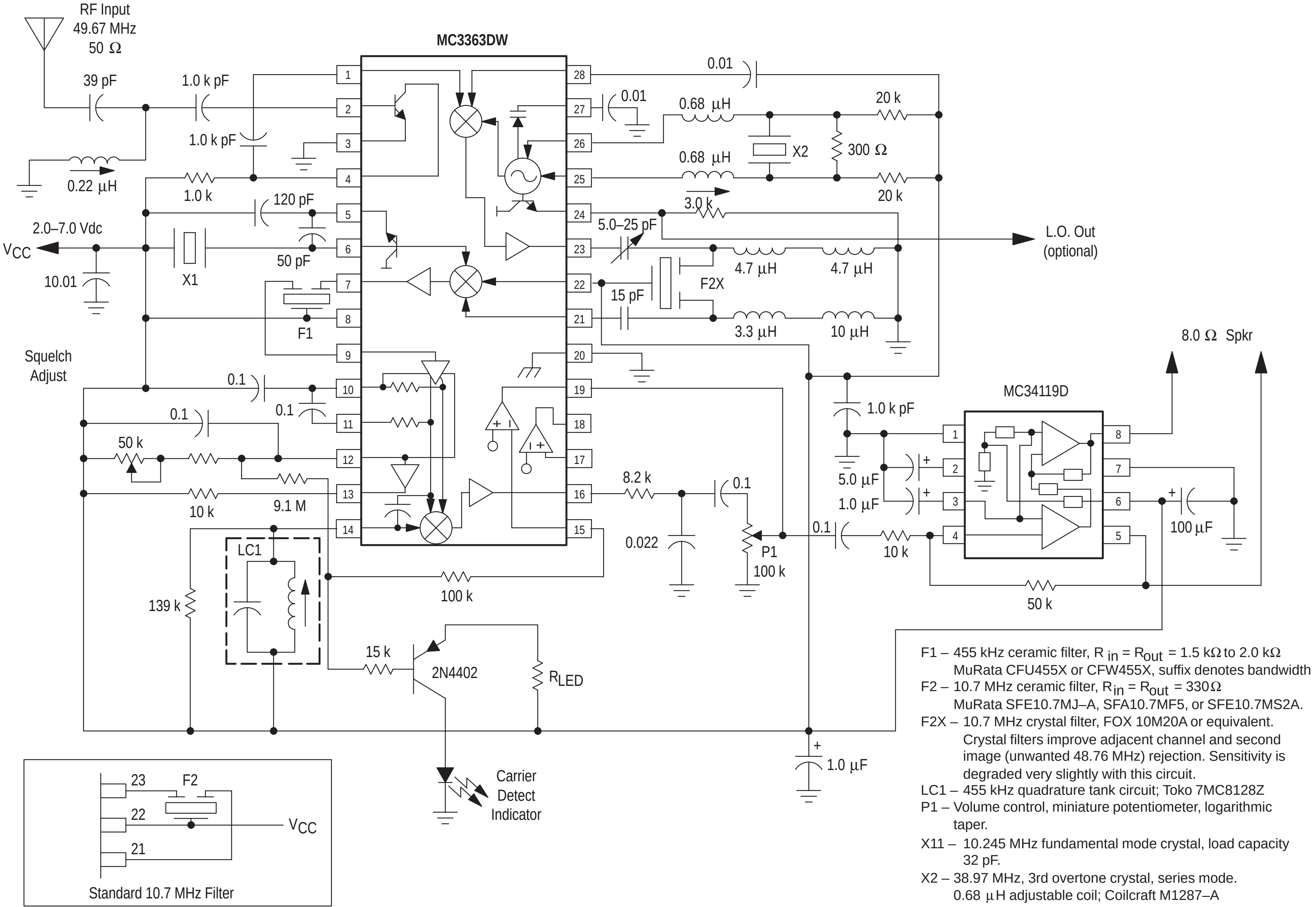
NOTE: For further application and design information, refer to AN980.

Figure 3. Typical Application in a PLL Frequency Synthesized Receiver



NOTE: Pull Up resistor is
used to run the oscillator above 50 MHz.

Figure 4. Single Channel Narrowband FM Receiver at 49.67 MHz



F1 – 455 kHz ceramic filter, $R_{in} = R_{out}$ = 1.5 kΩ to 2.0 kΩ
MuRata CFU455X or CFW455X, suffix denotes bandwidth

F2 – 10.7 MHz ceramic filter, $R_{in} = R_{out}$ = 330 Ω
MuRata SFE10.7MJ–A, SFA10.7MF5, or SFE10.7MS2A.

F2X – 10.7 MHz crystal filter, FOX 10M20A or equivalent. Crystal filters improve adjacent channel and second image (unwanted 48.76 MHz) rejection. Sensitivity is degraded very slightly with this circuit.

LC1 – 455 kHz quadrature tank circuit; Toko 7MC8128Z

P1 – Volume control, miniature potentiometer, logarithmic taper.

X11 – 10.245 MHz fundamental mode crystal, load capacity 32 pF.

X2 – 38.97 MHz, 3rd overtone crystal, series mode.
0.68 µH adjustable coil; Coilcraft M1287–A
0.22 µH adjustable coil; Coilcraft M1175–A

R_{LED} is used to adjust LED current: $I_{LED} \approx \frac{V_{CC} - V_{LED}}{R_{LED}}$

Figure 5. Circuit Schematic

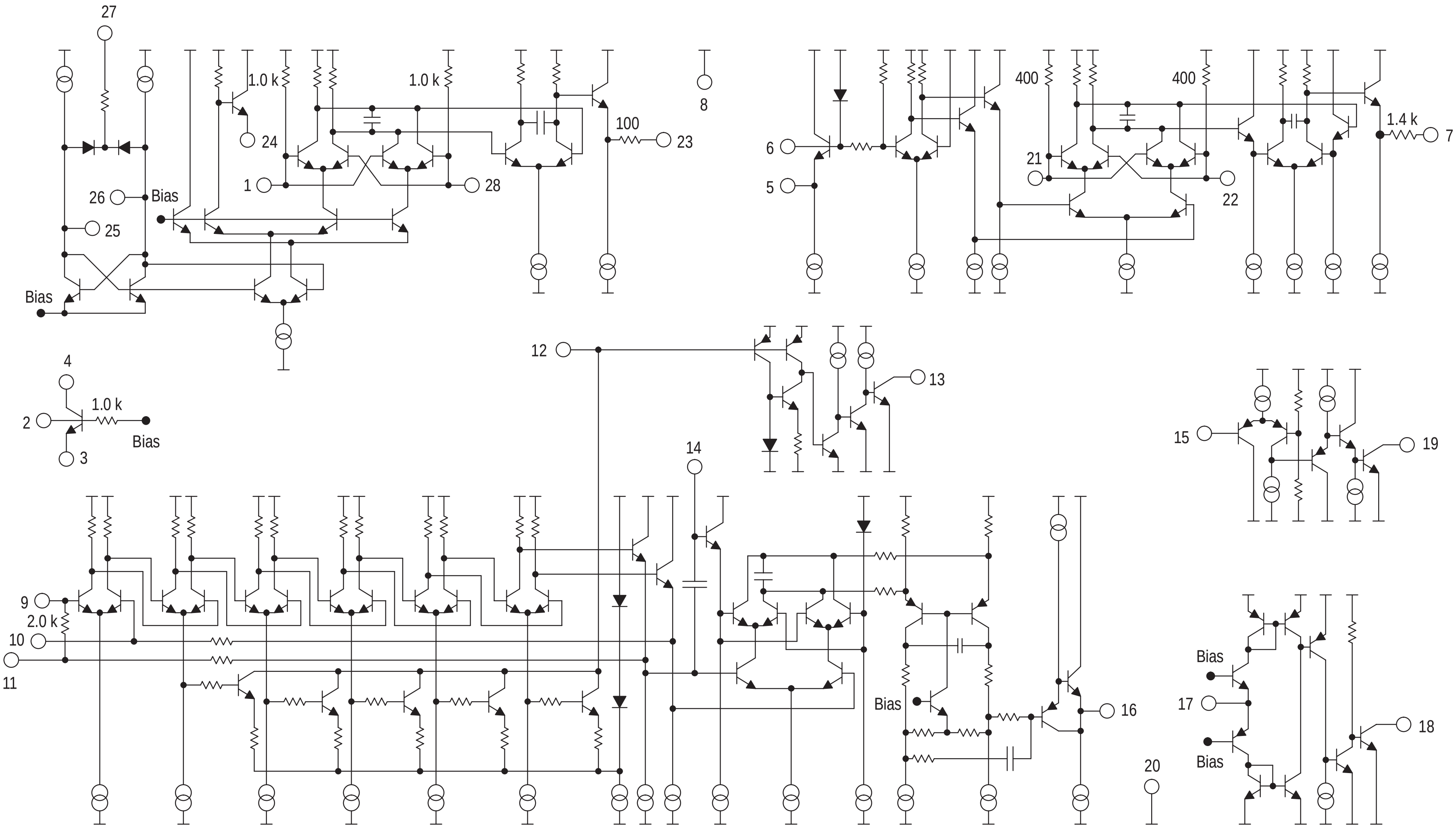


Figure 6. PC Board Component View with High Performance Crystal Filter

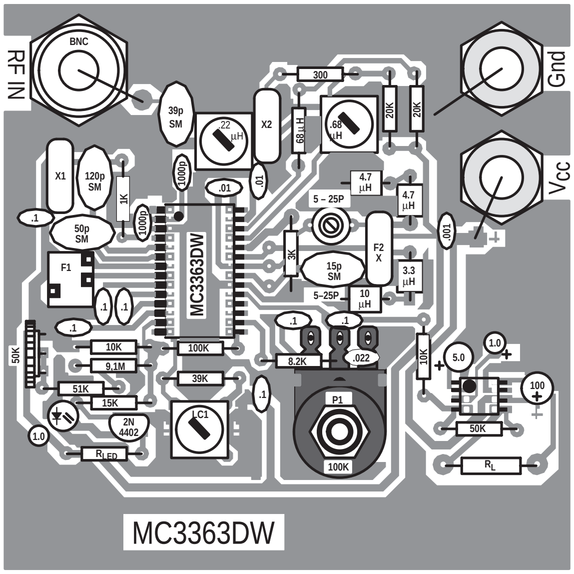


Figure 7. PC Board Circuit Side View

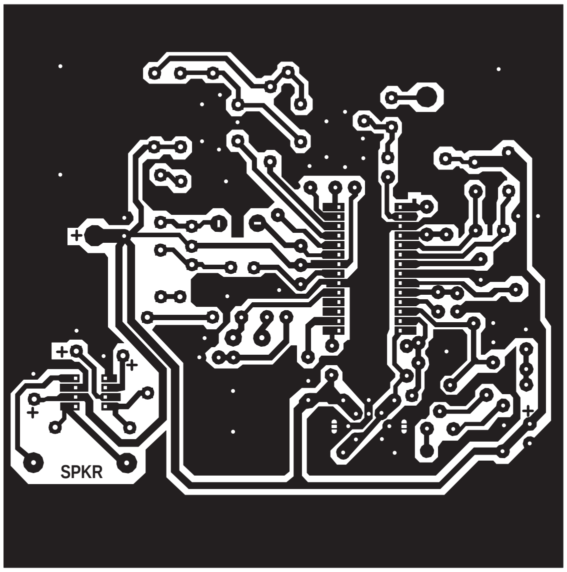
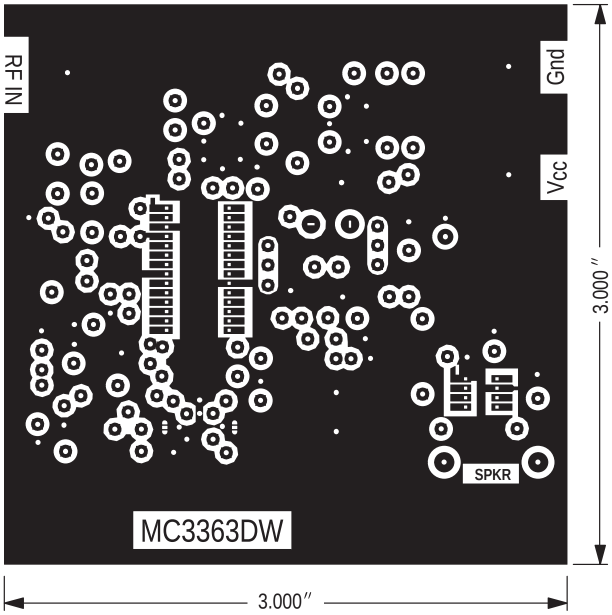


Figure 8. PC Board Component Side Ground Plane



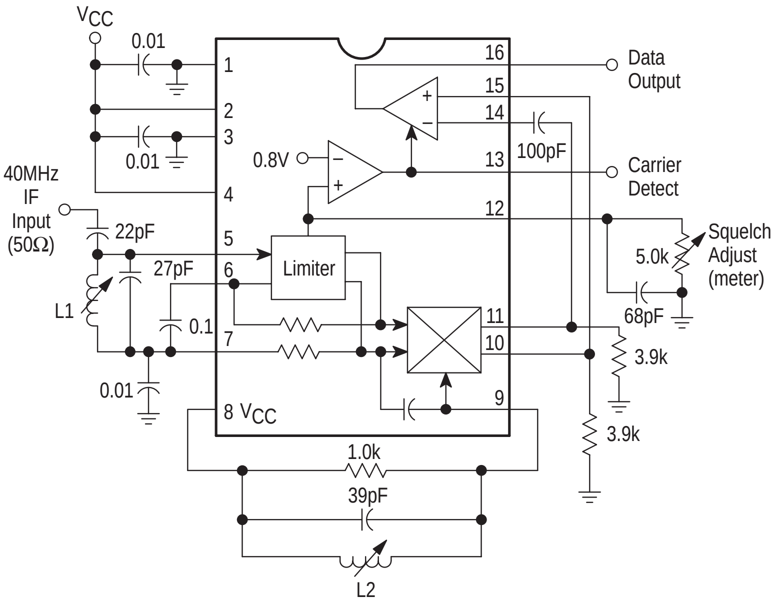
MC13055

Wideband FSK Receiver

The MC13055 is intended fo RF data link systems using carrier frequencies up to 40 MHz and FSK (frequency shift keying) data rates up to 2.0 M Baud (1.0 MHz). This design is similar to the MC3356, except that it does not include the oscillator/mixer. The IF bandwidth has been increased and the detector output has been revised to a balanced configuration. The received signal strength metering circuit has been retained, as has the versatile data slicer/comparator.

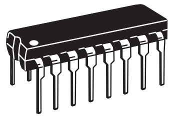
- Input Sensitivity 20 µV @ 40 MHz
- Signal Strength Indicator Linear Over 3 Decades
- Available in Surface Mount Package
- Easy Application, Few Peripheral Components

Figure 1. Block Diagram and Application Circuit



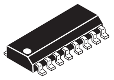
WIDEBAND FSK RECEIVER

SEMICONDUCTOR TECHNICAL DATA

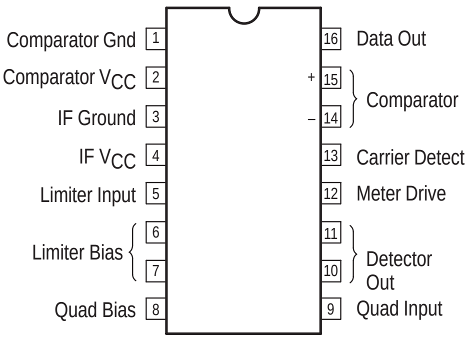


P SUFFIX
PLASTIC PACKAGE
CASE 648

D SUFFIX
PLASTIC PACKAGE
CASE 751B
(SO–16)



PIN CONNECTIONS



ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC13055D	T_A = – 40 to +85°C	SO–16
MC13055P		Plastic DIP

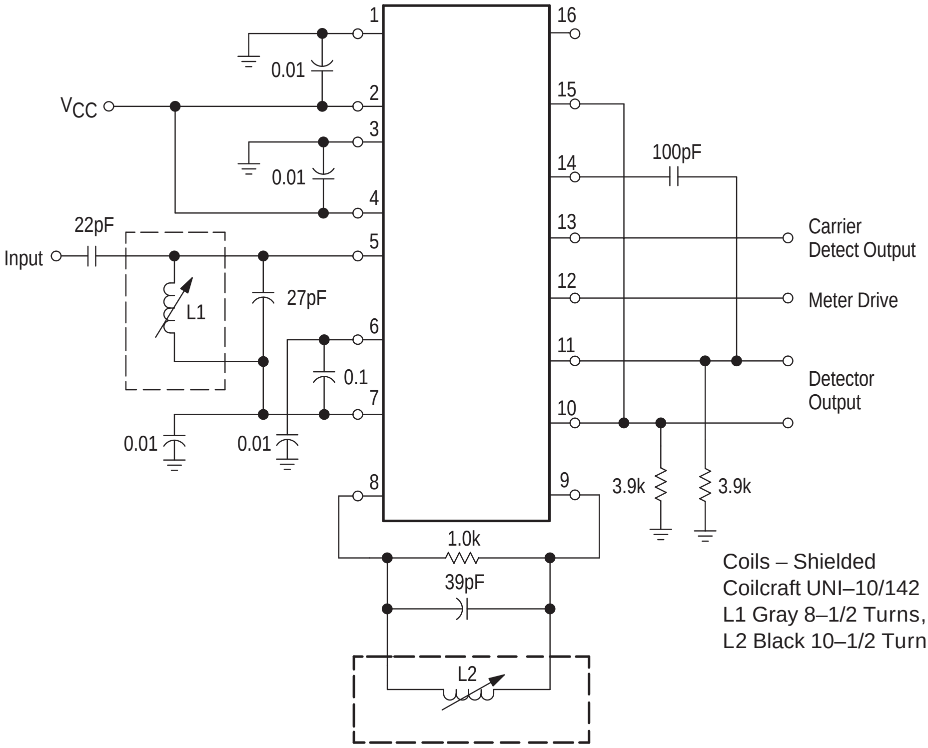
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	$V_{CC(max)}$	15	Vdc
Operating Supply Voltage Range	V2, V4	3.0 to 12	Vdc
Junction Temperature	T_J	150	°C
Operating Ambient Temperature Range	T_A	–40 to +85	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Power Dissipation, Package Rating	P_D	1.25	W

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 Vdc, f_o = 40 MHz, f_{mod} = 1.0 MHz, Δf = ±1.0 MHz, T_A = 25°C, test circuit of Figure 2.)

Characteristic		Conditions	Min	Typ	Max	Unit
Total Drain Current		12 + 14	–	20	25	mA
Data Comparator Pull–Down Current		I16	–	10	–	mA
Meter Drive Slope versus Input		I12	4.5	7.0	9.0	µA/dB
Carrier Detect Pull–Down Current		I13	–	1.3	–	mA
Carrier Detect Pull–Up Current		I13	–	500	–	µA
Carrier Detect Threshold Voltage		V12	690	800	1010	mV
DC Output Current		I10, I11	–	430	–	µA
Recovered Signal		V10 – V11	–	350	–	mVrms
Sensitivity for 20 dB S + N/N, BW = 5.0 MHz		VIN	–	20	–	µVrms
S + N/N at V_{in} = 50 µV		V10 – V11	–	30	–	dB
Input Impedance @ 40 MHz	R_{in} C_{in}	Pin 5, Ground	– –	4.2 4.5	– –	kΩ pF
Quadrature Coil Loading	R_{in} C_{in}	Pin 9 to 8	– –	7.6 5.2	– –	kΩ pF

Figure 2. Test Circuit



Coils – Shielded
Coilcraft UNI–10/142
L1 Gray 8–1/2 Turns, nominal 300 nH
L2 Black 10–1/2 Turns, nominal 380 nH

Figure 3. Overall Gain, Noise, AM Rejection

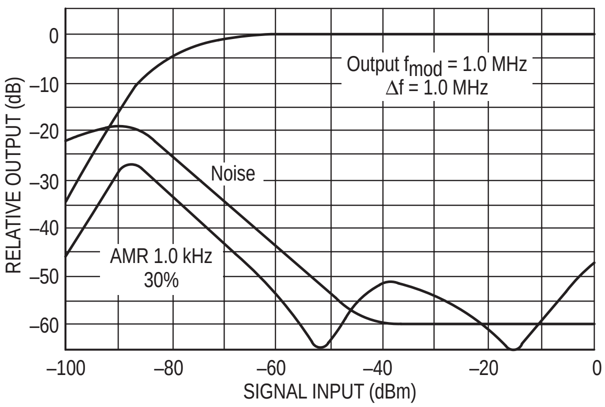


Figure 4. Meter Current versus Signal

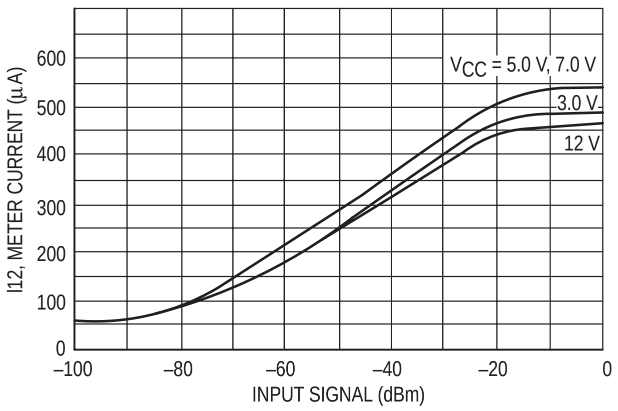


Figure 5. Untuned Input: Limiting Sensitivity versus Frequency

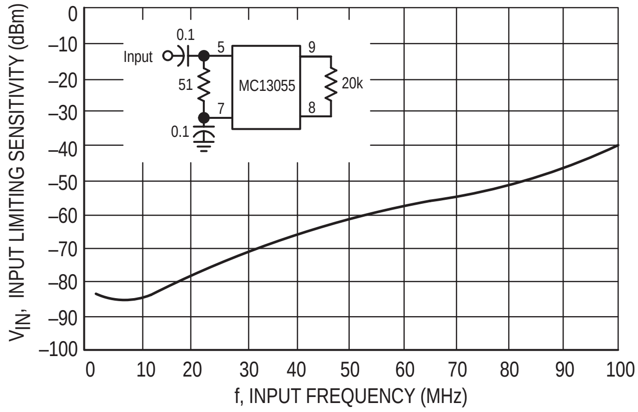


Figure 6. Untuned Input: Meter Current versus Frequency

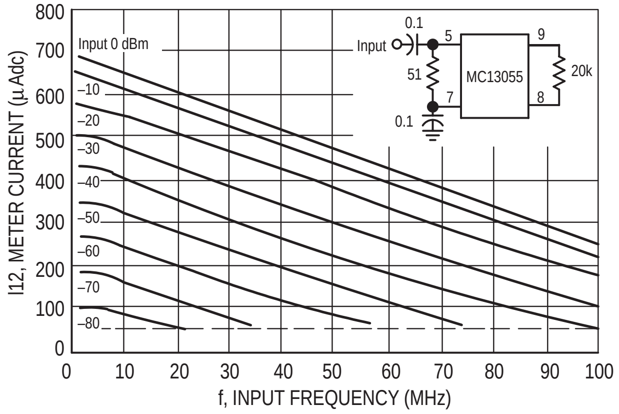


Figure 7. Limiting Sensitivity and Detuning versus Supply Voltage

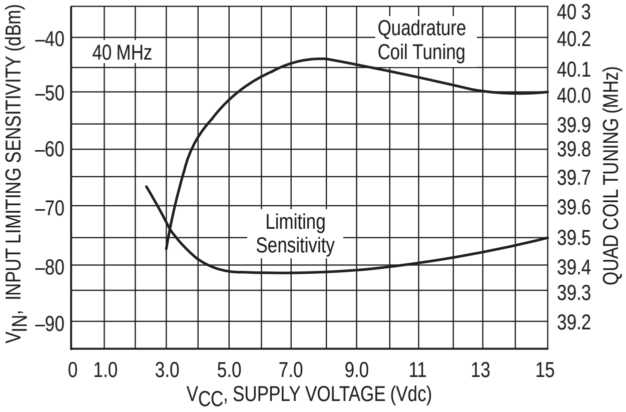


Figure 8. Detector Current and Power Supply Current versus Supply Voltage

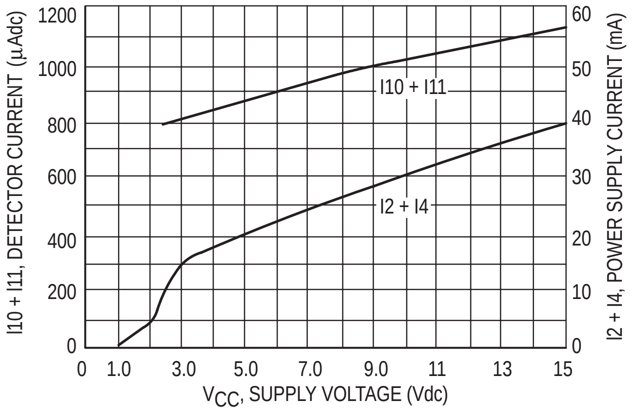


Figure 9. Recovered Audio versus Temperature

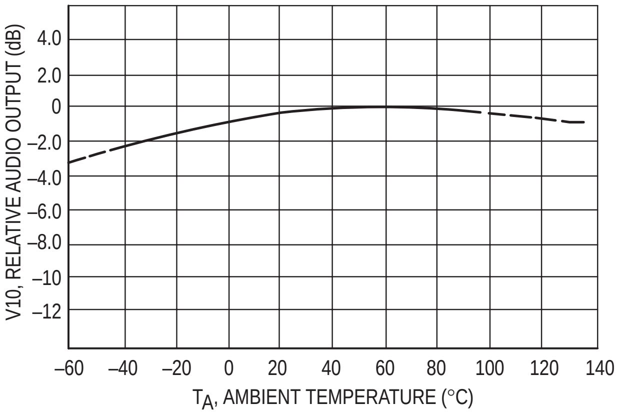


Figure 10. Carrier Detect Threshold versus Temperature

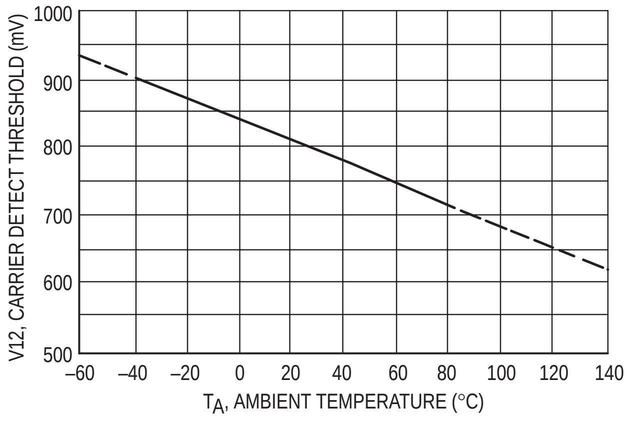


Figure 11. Meter Current versus Temperature

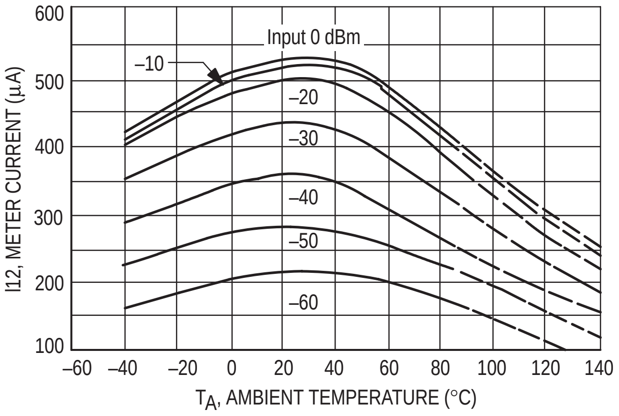


Figure 12. Input Limiting versus Temperature

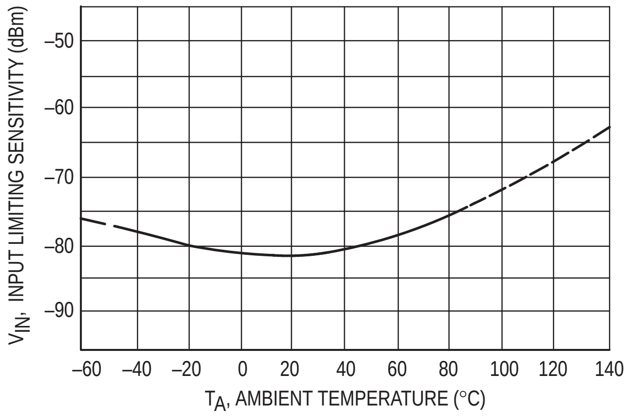


Figure 13. Input Impedance, Pin 5

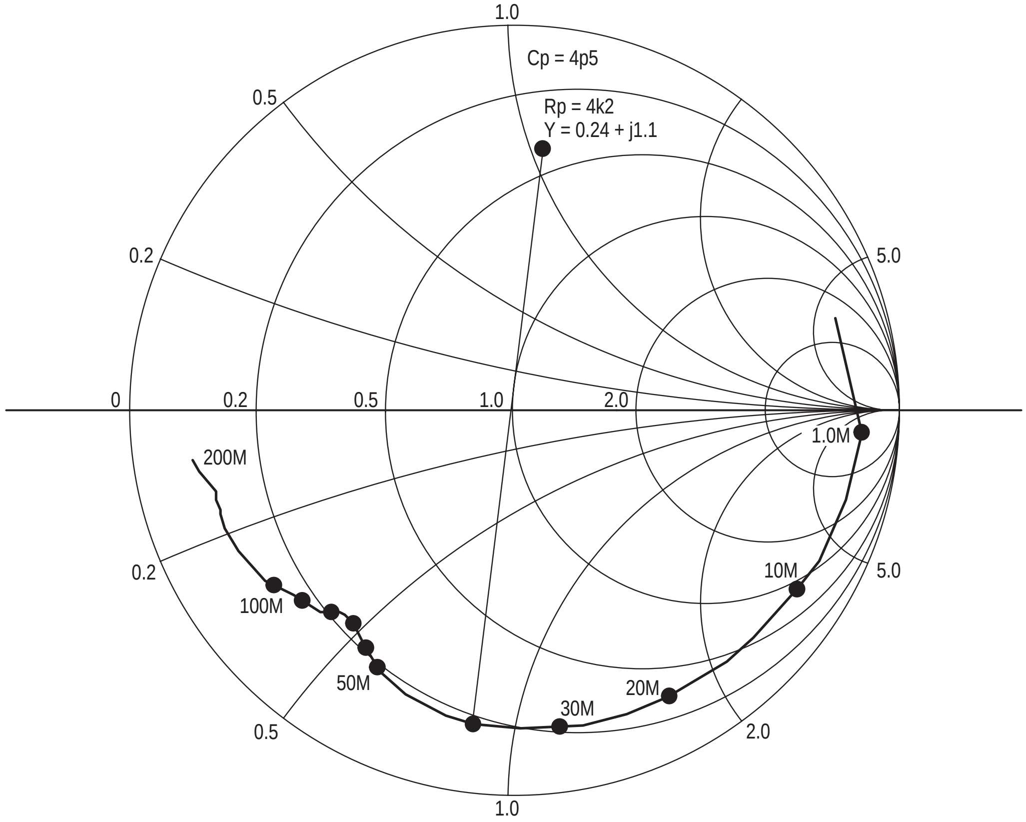
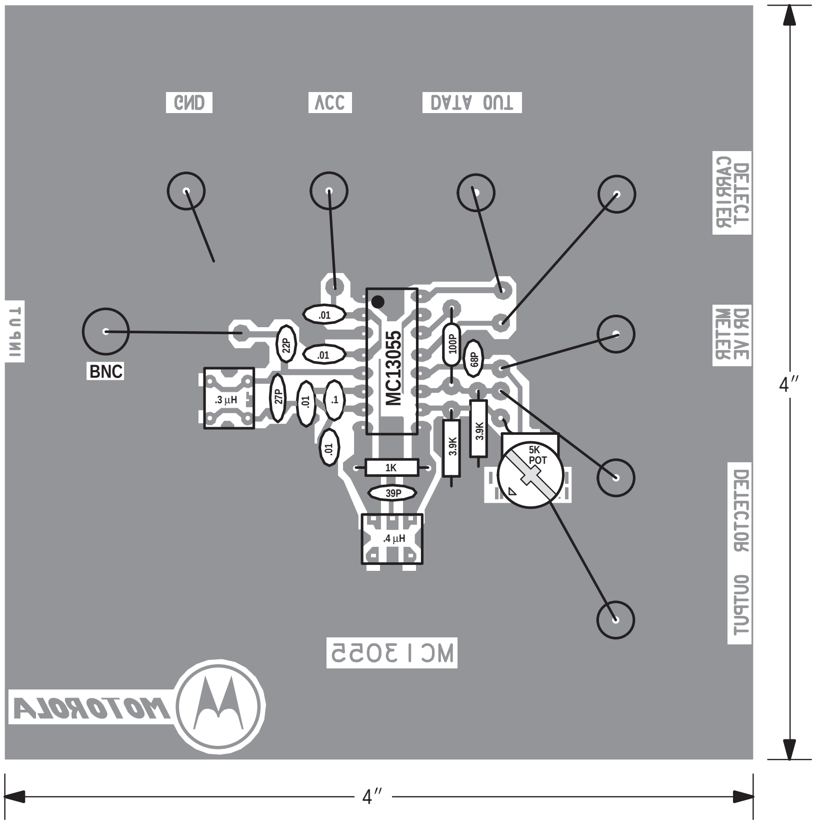
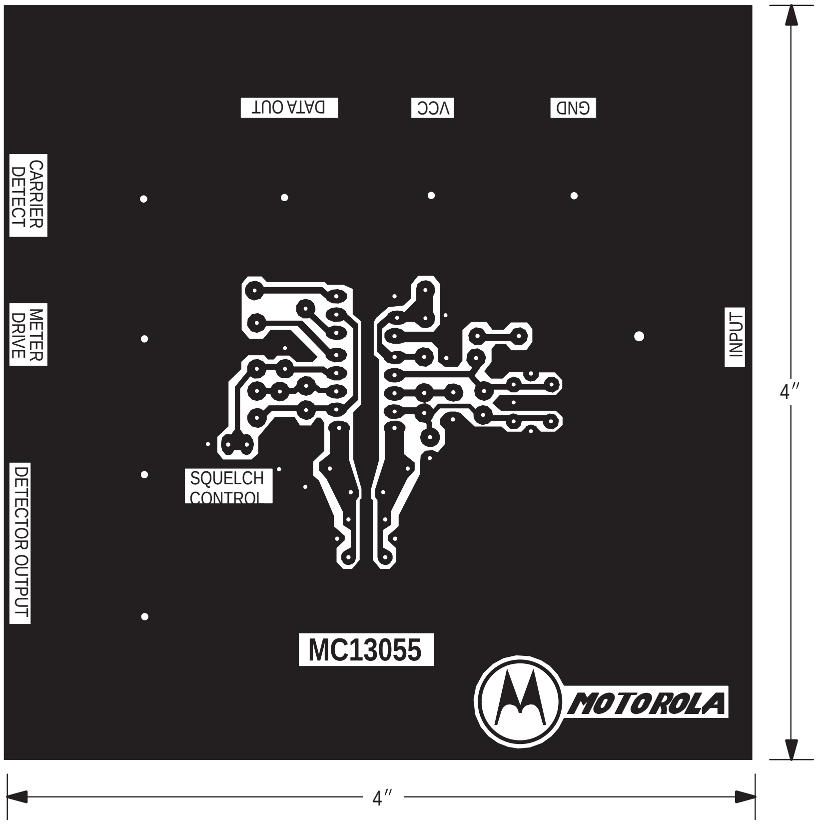


Figure 14. Test Fixture
(Component Layout)



(Circuit Side View)



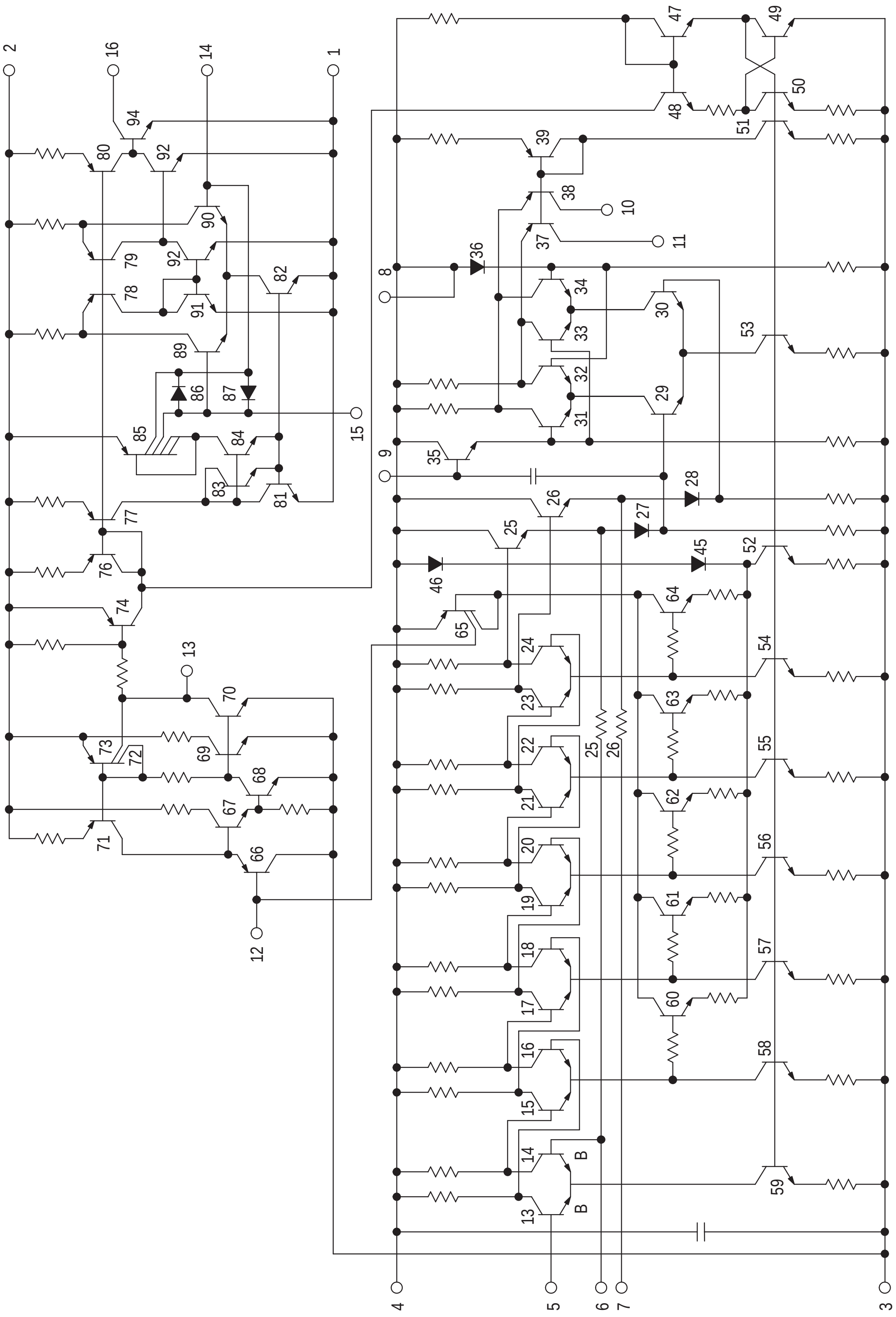


Figure 15. Internal Schematic

GENERAL DESCRIPTION

The MC13055 is an extended frequency range FM IF, quadrature detector, signal strength detector and data shaper. It is intended primarily for FSK data systems. The design is very similar to MC3356 except that the oscillator/mixer has been removed, and the frequency capability of the IF has been raised about 2:1. The detector output configuration has been changed to a balanced, open–collector type to permit symmetrical drive of the data shaper (comparator). Meter drive and squelch features have been retained.

The limiting IF is a high frequency type, capable of being operated up to 100 MHz. It is expected to be used at 40 MHz in most cases. The quadrature detector is internally coupled to the IF, and a 2.0 pF quadrature capacitor is internally provided. The 20 dB quieting sensitivity is approximately 20 μV, tuned input, and the IF can accept signals up to 220 mVrms without distortion or change of detector quiescent DC level.

The IF is unusual in that each of the last 5 stages of the 6 stage limiter contains a signal strength sensitive, current sinking device. These are parallel connected and buffered to produce a signal strength meter drive which is fairly linear for IF input signals of 20 μV to 20 mVrms (see Figure 4).

A simple squelch arrangement is provided whereby the meter current flowing through the meter load resistance flips a comparator at about 0.8 Vdc above ground. The signal strength at which this occurs can be adjusted by changing the meter load resistor. The comparator (+) input and output are available to permit control of hysteresis. Good positive action can be obtained for IF input signals of above 20 μVrms. A resistor (R) from Pin 13 to Pin 12 will provide V_{CC}/R of feedback current. This current can be correlated to an amount of signal strength hysteresis by using Figure 4.

The squelch is internally connected to the data shaper. Squelch causes the data shaper to produce a high (V_{CC}) output.

The data shaper is a complete “floating” comparator, with diodes across its inputs. The outputs of the quadrature detector can be fed directly to either or preferably both inputs of the comparator to produce a squared output swinging from V_{CC} to ground in inverted or noninverted form.

MOTOROLA

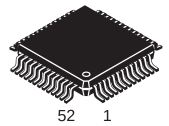
MC13109

Universal Cordless Telephone Subsystem IC

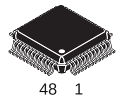
The MC13109 integrates several of the functions required for a cordless telephone into a single integrated circuit. This significantly reduces component count, board space requirements, and external adjustments. It is designed for use in both the handset and the base.

- Dual Conversion FM Receiver
  - Complete Dual Conversion Receiver – Antenna Input to Audio Output 80 MHz Maximum Carrier Frequency
  - RSSI Output
  - Carrier Detect Output with Programmable Threshold
  - Comparator for Data Recovery
  - Operates with Either a Quad Coil or Ceramic Discriminator
- Compander
  - Expandor Includes Mute, Digital Volume Control and Speaker Driver
  - Compressor Includes Mute, ALC and Limiter
- Dual Universal Programmable PLL
  - Supports New 25 Channel U.S. Standard with No External Switches
  - Universal Design for Domestic and Foreign CT–1 Standards
  - Digitally Controlled Via a Serial Interface Port
  - Receive Side Includes 1st LO VCO, Phase Detector, and 14–Bit Programmable Counter and 2nd LO with 12–Bit Counter
  - Transmit Section Contains Phase Detector and 14–Bit Counter
  - MPU Clock Output Eliminates Need for MPU Crystal
- Supply Voltage Monitor
  - Externally Adjustable Trip Point
- 2.0 to 5.5 V Operation with One–Third the Power Consumption of Competing Devices
- AN1575: Refer to Application Note for a List of “Worldwide Cordless Telephone Frequencies” (Chapter 8 Addendum of DL128 Data Book)

**UNIVERSAL CT–1
SUBSYSTEM
INTEGRATED CIRCUIT**



FB SUFFIX
PLASTIC PACKAGE
CASE 848B
(QFP–52)

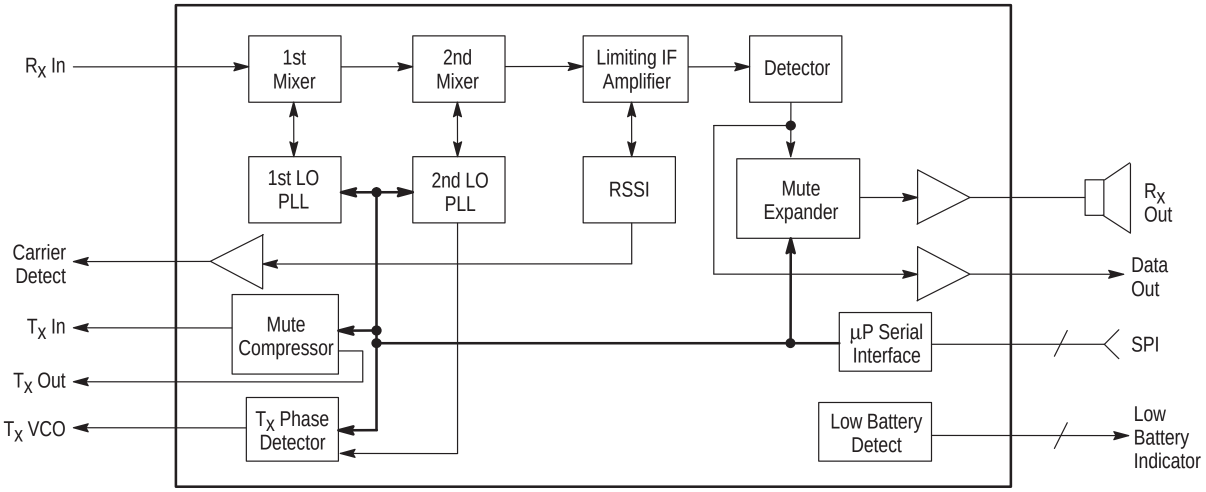


FTA SUFFIX
PLASTIC PACKAGE
CASE 932
(Thin QFP)

ORDERING INFORMATION

Device	Tested Operating Temperature Range	Package
MC13109FB	T_A = –20° to +85°C	QFP–52
MC13109FTA		TQFP–48

Simplified Block Diagram



This device contains 6,609 active transistors.

Figure 1. MC13109FB Test Circuit

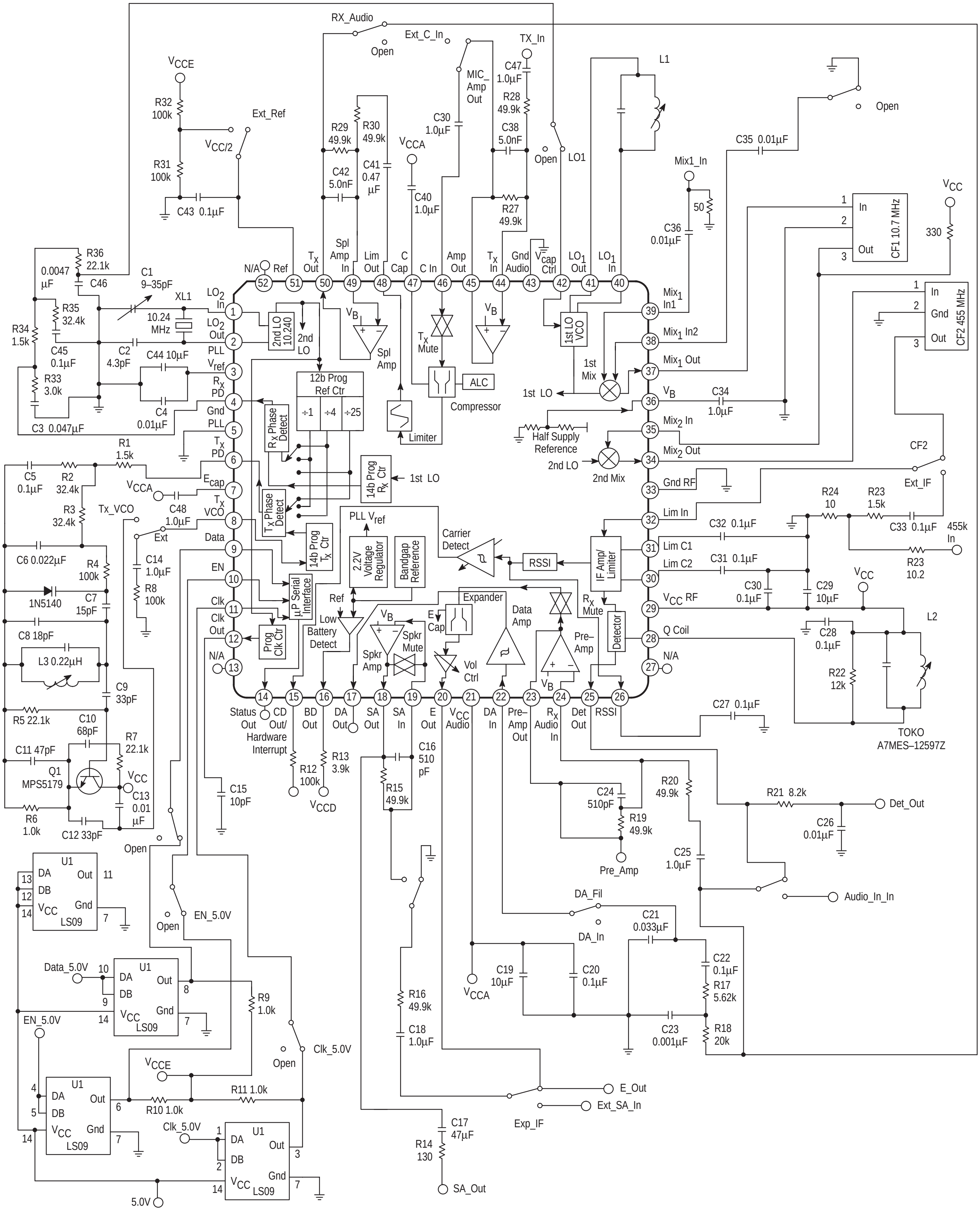
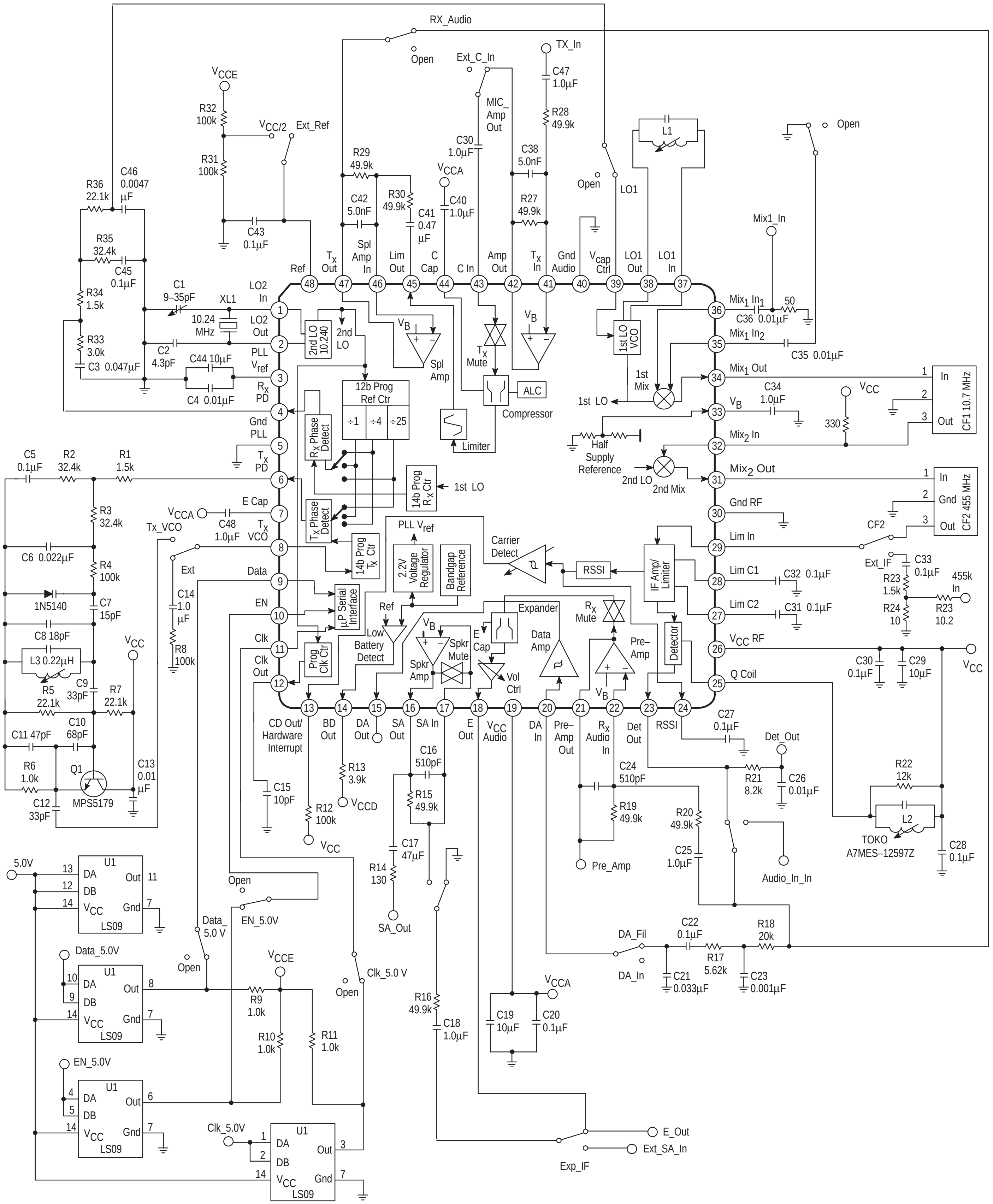


Figure 2. MC13109FTA Test Circuit



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	–0.5 to +5.5	Vdc
Junction Temperature	T_J	–65 to +150	°C

NOTE: 1. Devices should not be operated at these limits. The “Recommended Operating Conditions” provide for actual device operation.
2. ESD data available upon request.

RECOMMENDED OPERATING CONDITIONS

Characteristic	Min	Typ	Max	Unit
V_{CC}	2.0	–	5.5	Vdc
Operating Ambient Temperature	–20	–	85	°C

NOTE: All limits are not necessarily functional concurrently.

ELECTRICAL CHARACTERISTICS (V_{CC} = 2.6 V, T_A = 25°C, RF In = 46.61 MHz, f_{DEV} = ±3.0 kHz, f_{mod} = 1.0 kHz; Test Circuit Figure 1.)

Characteristic	Min	Typ	Max	Unit
POWER SUPPLY				
Static Current				
Active Mode (V_{CC} = 2.6 V)	–	6.7	12	mA
Active Mode (V_{CC} = 3.6 V)	–	7.1	–	mA
Receive Mode (V_{CC} = 2.6 V)	–	4.3	7.0	mA
Receive Mode (V_{CC} = 3.6 V)	–	4.5	–	mA
Standby Mode (V_{CC} = 2.6 V)	–	300	600	µA
Standby Mode (V_{CC} = 3.6 V)	–	600	–	µA
Inactive Mode (V_{CC} = 2.6 V)	–	40	80	µA
Inactive Mode (V_{CC} = 3.6 V)	–	56	–	µA

ELECTRICAL CHARACTERISTICS (continued)

FM Receiver

The FM receivers can be used with either a quad coil or a ceramic resonator. The FM receiver and 1st LO have been designed to work for all country channels, including 25 channel U.S., without the need for any external switching circuitry (see Figure 29).

(Test Conditions: V_{CC} = 2.6 V, T_A = 25°C, f_O = 46.61 MHz, f_{DEV} = ±3.0 kHz, f_{mod} = 1.0 kHz.)

Characteristic	Condition	Input Pin	Measure Pin	Symbol	Min	Typ	Max	Unit
Sensitivity (Input for 12 dB SINAD)	Matched Impedance Differential Input	Mix_1 $In_{1/2}$	Det Out	V_{SIN}	–	0.7	–	μVrms
1st Mixer Conversion Gain	V_{in} = 1.0 mVrms, with CF_1 Load	Mix_1 $In_{1/2}$	CF_1	MX_{gain1}	–	10	–	dB
2nd Mixer Conversion Gain	V_{in} = 3.0 mVrms, with CF_2 Load	Mix_2 In	CF_2	MX_{gain2}	–	20	–	dB
1st and 2nd Mixer Gain Total	V_{in} = 1.0 mVrms, with CF_1 and CF_2 Load	Mix_1 $In_{1/2}$	CF_2	MX_{gainT}	24	30	–	dB
1st Mixer Input Impedance	–	–	Mix_1 In_1 Mix_1 In_2	Z_{in1}	–	1.0	–	kΩ
2nd Mixer Input Impedance	–	–	Mix_2 In	Z_{in2}	–	3.0	–	kΩ
1st Mixer Output Impedance	–	–	Mix_1 Out	Z_{out1}	–	330	–	Ω
2nd Mixer Output Impedance	–	–	Mix_2 Out	Z_{out2}	–	1.5	–	kΩ
IF –3.0 dB Limiting Sensitivity	f_{in} = 455 kHz	Lim In	Det Out	IF Sens	–	55	–	μVrms
Total Harmonic Distortion (CCITT Filter)	With R_C = 8.2 kΩ/ 0.01 μF Filter at Det Out	Mix_1 $In_{1/2}$	Det Out	THD	–	0.7	–	%
Recovered Audio	With R_C = 8.2 kΩ/ 0.01 μF Filter at Det Out	Mix_1 $In_{1/2}$	Det Out	AFO	80	100	154	mVrms
Demodulator Bandwidth	–	Lim In	Det Out	BW	–	20	–	kHz
Signal to Noise Ratio	V_{in} = 10 mVrms, R_C = 8.2 kΩ/0.01 μF	Mix_1 $In_{1/2}$	Det Out	SN	–	49	–	dB
AM Rejection Ratio	30% AM, V_{in} = 10 mVrms, R_C = 8.2 kΩ/0.001 μF	Mix_1 $In_{1/2}$	Det Out	AMR	–	37	–	dB
First Mixer 3rd Order Intercept (Input Referred)	Matched Impedance Input	Mix_1 $In_{1/2}$	Mix_1 Out	TOI_{mix1}	–	–10	–	dBm
Second Mixer 3rd Order Intercept (Input Referred)	Matched Impedance Input	Mix_2 In	Mix_2 Out	TOI_{mix2}	–	–27	–	dBm
Detector Output Impedance	–	–	Det Out	Z_O	–	870	–	Ω

ELECTRICAL CHARACTERISTICS (continued)

RSSI/Carrier Detect

Connect 0.01 µF to Gnd from "RSSI" output pin to form the carrier detect filter. "CD Out" is an open collector output which requires an external 100 kΩ pull–up resistor to V_{CC}. The carrier detect threshold is programmable through the MPU interface.

(R_L = 100 kΩ, V_{CC} = 2.6 V, T_A = 25°C.)

Characteristic	Condition	Input Pin	Measure Pin	Symbol	Min	Typ	Max	Unit
RSSI Output Current Dynamic Range	–	Mix_1 In	RSSI	RSSI	–	65	–	dB
Carrier Sense Threshold	CD Threshold Adjust = (10100)	Mix_1 In	CD Out	V_T	–	22.5	–	µVrms
Hysteresis	–	Mix1 In	CD Out	Hys	–	2.0	–	dB
Output High Voltage	V_{in} = 0 µVrms, R_L = 100 kΩ, CD = (10100)	Mix_1 In	CD Out	V_{OH}	V_{CC} – 0.1	2.6	–	V
Output Low Voltage	V_{in} = 100 µVrms, R_L = 100 kΩ, CD = (10100)	Mix_1 In	CD Out	V_{OL}	–	0.01	0.4	V
Carrier Sense Threshold Adjustment Range	Programmable through MPU Interface	–	–	V_{Trange}	–20	–	11	dB
Carrier Sense Threshold – Number of Steps	Programmable through MPU Interface	–	–	V_{Tn}	–	32	–	–

Data Amp Comparator (see Figure 4)

Inverting hysteresis comparator. Open collector output with internal 100 kΩ pull–up resistor. A band pass filter is connected between the "Det Out" pin and the "DA In" pin with component values as shown in the attached block diagram. The "DA In" input signal is ac coupled.

(V_{CC} = 2.6 V, T_A = 25°C)

Characteristic	Condition	Input Pin	Measure Pin	Symbol	Min	Typ	Max	Unit
Hysteresis	–	DA In	DA Out	Hys	30	40	50	mV
Threshold Voltage	–	DA In	DA Out	V_T	V_{CC} – 0.9	V_{CC} – 0.7	V_{CC} – 0.5	V
Input Impedance	–	–	DA In	Z_I	–	11	–	kΩ
Output Impedance	–	–	DA Out	Z_O	–	100	–	kΩ
Output High Voltage	V_{in} = V_{CC} – 1.0 V, I_{OH} = 0 mA	DA In	DA Out	V_{OH}	V_{CC} – 0.1	2.6	–	V
Output Low Voltage	V_{in} = V_{CC} – 0.4 V, I_{OL} = 0 mA	DA In	DA Out	V_{OL}	–	0.03	0.4	V

ELECTRICAL CHARACTERISTICS (continued)

Pre–Amplifier/Expander/R_X Mute/Volume Control (See Figure 4)

The Pre–Amplifier is an inverting rail–to–rail output swing operational amplifier with the non–inverting input terminal connected to the internal V_B half supply reference. External resistors and capacitors can be connected to set the gain and frequency response. The expander analog ground is set to the half supply reference so the input and output swing capability will increase as the supply voltage increases. The volume control can be adjusted through the MPU interface. The "R_X Audio In" input signal is ac coupled.

(Test Conditions: V_{CC} = 2.6 V, T_A = 25°C, f_{in} = 1.0 kHz, Set External Pre–Amplifier R's for Gain of 1, Volume Control = (0111).)

Characteristic	Condition	Input Pin	Measure Pin	Symbol	Min	Typ	Max	Unit
Pre–Amp Open Loop Gain	–	R_X Audio In	Pre–Amp	A_{VOL}	–	60	–	dB
Pre–Amp Gain Bandwidth	–	R_X Audio In	Pre–Amp	GBW	–	100	–	kHz
Pre–Amp Maximum Output Swing	R_L = 10 kΩ	R_X Audio In	Pre–Amp	V_{Omax}	–	V_{CC} – 0.3	–	V_{pp}
Expander 0 dB Gain Level	V_{in} = –10 dBV	R_X Audio In	E Out	G	–3.0	–0.11	3.0	dB
Expander Gain Tracking	V_{in} = –20 dBV, Output Relative to G V_{in} = –30 dBV, Output Relative to G	R_X Audio In	E Out	G_t	–21 –42	–19.65 –39.42	–19 –37	dB
Total Harmonic Distortion	V_{in} = –10 dBV	R_X Audio In	E Out	THD	–	0.5	–	%
Maximum Output Voltage	Increase input voltage until output voltage THD = 5%, then measure output voltage. R_L = 10 kΩ	R_X Audio In	E Out	V_{Omax}	–	–5.0	–	dBV
Attack Time	E_{cap} = 1.0 µF, R_{filt} = 20 kΩ (See Appendix B)	R_X Audio In	E Out	t_a	–	3.0	–	ms
Release Time	E_{cap} = 1.0 µF, R_{filt} = 20 kΩ (See Appendix B)	R_X Audio In	E Out	t_r	–	13.5	–	ms
Compressor to Expander Crosstalk	V (R_X Audio In) = 0 Vrms, V_{in} = –10 dBV	C In	E Out	C_T	–	–	–70	dB
R_X Mute	V_{in} = –10 dBV No popping detectable during R_X Mute transitions	R_X Audio In	E Out	M_e	–	–70	–	dB
Volume Control Range	Programmable through MPU Interface	–	–	V_{Crange}	–14	–	16	dB
Volume Control Steps	Programmable through MPU Interface	–	–	V_{Cn}	–	16	–	–

ELECTRICAL CHARACTERISTICS (continued)

Speaker Amplifier/SP Mute

The Speaker Amplifier is an inverting rail–to–rail operational amplifier. The non–inverting input terminal is connected to the internal V_B half supply reference. External resistors and capacitors are used to set the gain and frequency response. The “SA In” input is ac coupled.

(Test Conditions: V_{CC} = 2.6 V, T_A = 25°C, f_{in} = 1.0 kHz, External Resistors Set for Gain of 1.)

Characteristic	Condition	Input Pin	Measure Pin	Symbol	Min	Typ	Max	Unit
Maximum Output Swing	V_{CC} = 2.3 V, R_L = 130 Ω V_{CC} = 2.3 V, R_L = 600 Ω V_{CC} = 3.4 V, R_L = 600 Ω	SA In	SA Out	V_{Omax}	– – –	0.8 2.0 3.0	– – –	V_{pp}
SP Mute	V_{in} = –20 dBV R_L = 130 Ω No popping detectable during SP Mute transitions	SA In	SA Out	M_{sp}	–	–70	–	dB

Mic Amplifier (See Figure 6)

The Mic Amplifier is an inverting rail–to–rail output operational amplifier with the non–inverting input terminal connected to the internal V_B half supply reference. External resistors and capacitors are connected to set the gain and frequency response. The “T_X In” input is ac coupled.

(Test Conditions: V_{CC} = 2.6 V, T_A = 25°C, f_{in} = 1.0 kHz, External Resistors Set for Gain of 1.)

Characteristic	Condition	Input Pin	Measure Pin	Symbol	Min	Typ	Max	Unit
Open Loop Gain	–	T_X In	Amp Out	A_{VOL}	–	60	–	dB
Gain Bandwidth	–	T_X In	Amp Out	G_{BW}	–	100	–	kHz
Maximum Output Swing	R_L = 10 kΩ	T_X In	Amp Out	V_{Omax}	–	V_{CC} – 0.3	–	V_{pp}

ELECTRICAL CHARACTERISTICS (continued)

Compressor/ALC/T_X Mute/Limiter (See Figure 5)

The compressor analog gound is set to the half supply reference so the input and output swing capability will increase as the supply voltage increases. The “C In” input is ac coupled. The ALC (Automatic Level Control) provides a soft limit to the output signal swing as the input voltage increases slowly (i.e., a sine wave is maintained). The Limiter circuit limits rapidly changing signal levels by clipping the signal peaks. The ALC and/or Limiter can be disabled through the MPU serial interface.

(Test Conditions: V_{CC} = 2.6 V, f_{in} = 1.0 kHz, T_A = 25°C.)

Characteristic	Condition	Input Pin	Measure Pin	Symbol	Min	Typ	Max	Unit
Compressor 0 dB Gain Level	V_{in} = –10 dBV, ALC disabled, Limiter disabled	C In	Lim Out	G	–3.0	–0.17	3.0	dB
Compressor Gain Tracking	V_{in} = –30 dBV, Output Relative to G V_{in} = –50 dBV, Output Relative to G	C In	Lim Out	G_t	–11 –23	–10.23 –20.23	–9.0 –17	dB
Maximum Compressor Gain	V_{in} –70 dBV	C In	Lim Out	A_{Vmax}	–	30	–	dB
Total Harmonic Distortion	V_{in} –10 dBV, ALC disabled, Limiter disabled	C In	Lim Out	THD	–	0.5	–	%
Input Impedance	–	C In	Lim Out	Z_{in}	–	16	–	kΩ
Attack Time	C_{cap} = 1.0 µF, R_{filt} = 20 kΩ (see Appendix B)	C In	Lim Out	t_a	–	3.0	–	ms
Release Time	C_{cap} = 1.0 µF, R_{filt} = 20 kΩ (see Appendix B)	C In	Lim Out	t_r	–	13.5	–	ms
Expander to Compressor Crosstalk	V (C In) = 0 Vrms, V_{in} = –10 dBV	R_X Audio In	Lim Out	C_T	–	–	–40	dB
T_X Data Mute	V_{in} = –10 dBV, ALC disabled No popping detectable during R_X Mute transitions	C In	Lim Out	M_e	–	–70	–	dB
ALC Dynamic Range	–	C In	Lim Out	DR	–24	–	–2.5	dBV
ALC Output Level	V_{in} = –18 dBV V_{in} = –2.5 dBV	C In	Lim Out	ALC_{out}	– –	–16 –12	– –	dBV
Limiter Output Level	ALC disabled	C In	T_X Out	V_{lim}	–	0.8	–	V_{pp}

ELECTRICAL CHARACTERISTICS (continued)

Splatter Amplifier (see Figure 7)

The Splatter Amplifier is an inverting rail–to–rail output operational amplifier with the non–inverting input terminal connected to the internal V_B half supply reference. External resistors and capacitors can be connected to set the gain and frequency response. The “Spl Amp In” input is ac coupled.

(Test Conditions: V_{CC} = 2.6 V, T_A = 25°C, f_{in} = 1.0 kHz, External resistors Set for Gain of 1.)

Characteristic	Condition	Input Pin	Measure Pin	Symbol	Min	Typ	Max	Unit
Open Loop Gain	–	Spl Amp In	T_X Out	A_{VOL}	–	60	–	dB
Gain Bandwidth	–	Spl Amp In	T_X Out	GBW	–	100	–	kHz
Maximum Output Swing	R_L = 10 kΩ	Spl Amp In	T_X Out	V_{Omax}	–	V_{CC} – 0.3	–	V_{pp}

T_X Audio Path Recommendation

The recommended configuration for the T_X Audio path includes setting the Microphone Amplifier gain to 16 dB using the external gain setting resistors and setting the Splatter Amplifier gain to 9.0 dB using the external gain setting resistors. With these gain values, the total T_X Path transfer characteristic is shown in Figure 7.

PLL Voltage Regulator

The PLL supply voltage is regulated to a nominal of 2.2 V. The “V_{CC} Audio” pin is the supply voltage for the internal voltage regulator. The “PLL V_{ref}” pin is the 2.2 V regulated output voltage. Two capacitors with 10 μF and 0.01 μF values must be connected to the “PLL V_{ref}” pin to filter and stabilize this regulated voltage. The voltage regulator provides power for the 2nd LO, R_X and T_X PLL’s, and MPU Interface. The voltage regulator can also be used to provide a regulated supply voltage for external IC’s. R_X and T_X PLL loop performance are independent of the power supply voltage when the voltage regulator is used. The voltage regulator requires about 200 mV of “headroom”. When the power supply decreases to within about 200 mV of the output voltage, the regulator will go out of regulation but the output voltage will not turn off. Instead, the output voltage will maintain about a 200 mV delta to the power supply voltage as the power supply voltage continues to decrease. The “PLL V_{ref}” pin can be connected to “V_{CC} Audio” by the external wiring if voltage higher than 2.2 V is required. But it should not be connected to other supply except “V_{CC} Audio”. The voltage regulator is “on” in the Active and R_X modes. In the Standby and Inactive modes, the voltage regulator is turned off to reduce current drain and the “PLL V_{ref}” pin is internally connected to “V_{CC} Audio” (i.e., the supply voltage is maintained but is now unregulated).

(Test Conditions: V_{CC} = 2.6 V, T_A = 25°C.)

Characteristic	Condition	Input Pin	Measure Pin	Symbol	Min	Typ	Max	Unit
Output Voltge Level	V_{CC} = 2.6 V, O_L= 0 mA	–	V_{CC} PLL	V_{out}	1.9	2.2	2.5	V
Line Regulation	I_L = 0 mA, V_{CC} = 2.6 to 5.5 V	V_{CC}	V_{CC} PLL	Reg_{line}	–	1.43	40	mV
Load Regulation	V_{CC} = 2.6 V, I_L = 0 to 1.0 mA	V_{CC}	V_{CC} PLL	Reg_{load}	–	–1.86	40	mV
Drop–Out Voltage	I_L = 0 mA	–	–	DO	–	–	V_{out} + 200	mV

ELECTRICAL CHARACTERISTICS (continued)

Low Battery Detect

An external resistor divider is connected to the “Ref” input pin to set the threshold for the low battery detect. The voltage at the “Ref” input pin is compared to an internal 1.23 V Bandgap reference voltage. The “BD Out” pin is open collector and requires and external pull–up resistor to V_{CC}.

(Test Conditions: V_{CC} = 2.6 V, T_A = 25°C.)

Characteristic	Condition	Input Pin	Measure Pin	Symbol	Min	Typ	Max	Unit
Average Threshold Voltage	Take average of rising and falling threshold	Ref	Ref/ BD Out	Threshold	–	1.23	–	V
Hysteresis	–	Ref	Ref/ BD Out	Hys	–	4.0	–	mV
Input Current	V_{in} = 1.6 V	–	Ref	I_{in}	–50	5.71	+50	nA
Output High Voltage	V_{ref} = 1.6, R_L = 3.9 kΩ	Ref	BD Out	V_{OH}	V_{CC} – 0.1	2.6	–	V
Output Low Voltage	V_{ref} = 0.9, R_L = 3.9 kΩ	Ref	BD Out	V_{OL}	–	0.12	0.4	V

Figure 3. Data Amp Operation

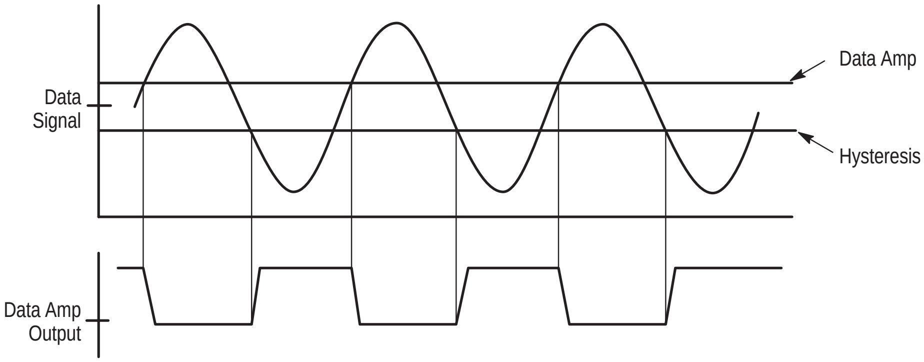


Figure 4. Typical Expander Response

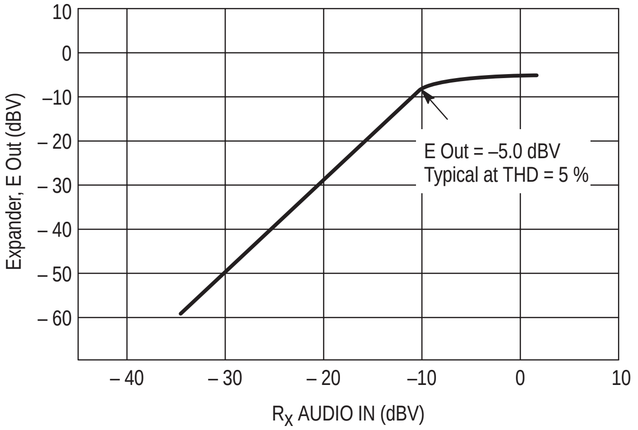


Figure 5. Typical Compressor/ALC/Limiter Response

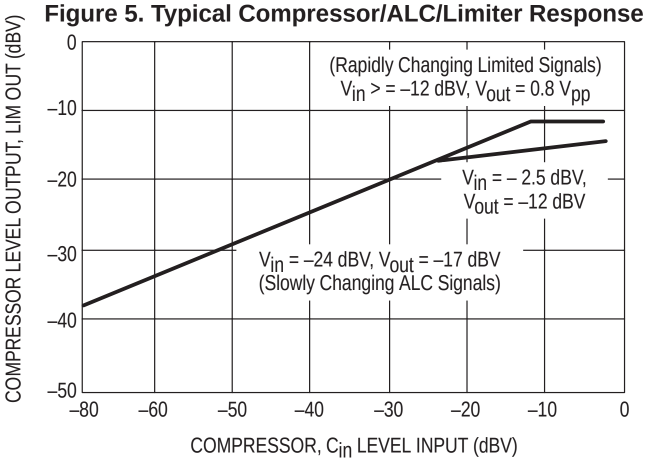


Figure 6. Total T_X Path, Mic Amp Gain = 16 dB, Splatter Amp Gain = 9.0 dB

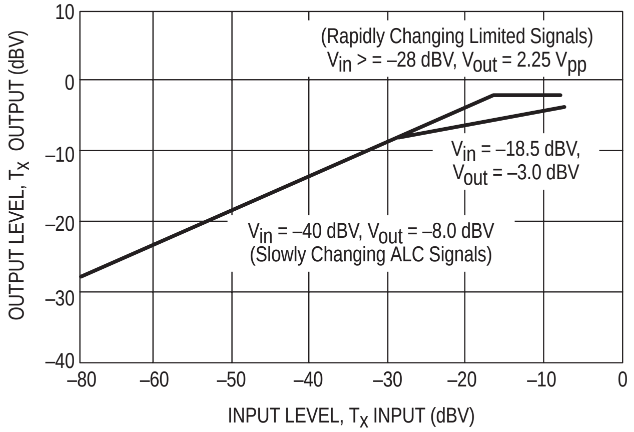
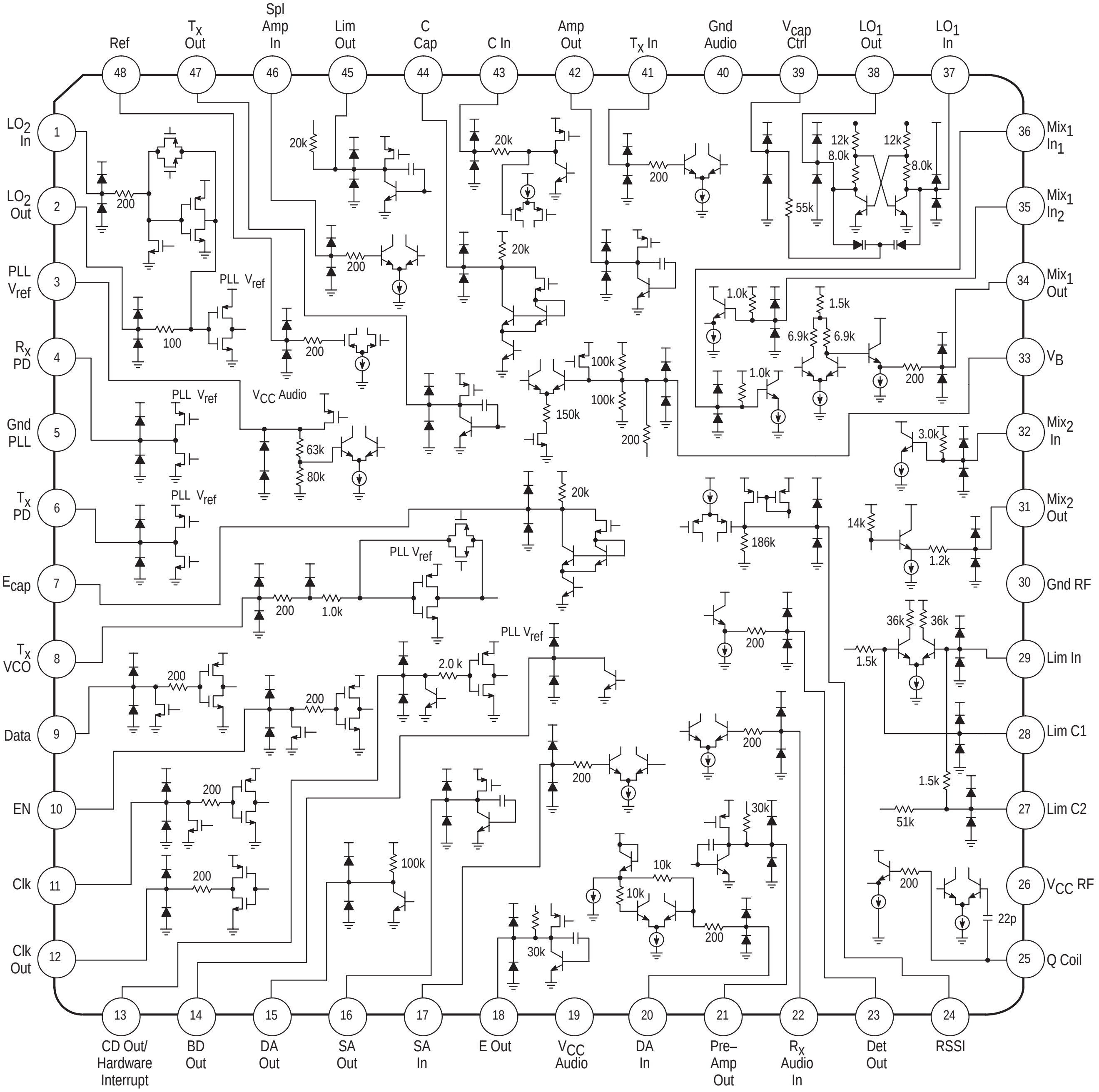


Figure 7. MC13109FTA Internal I/O Block Diagram



PIN FUNCTION DESCRIPTION

48–TQFP Pin	52–QFP Pin	Symbol	Type	Description
1 2	1 2	LO_2 In LO2 Out	–	These pins form the PLL reference oscillator when connected to an external parallel–resonant crystal (10.24 MHz typical). The reference oscillator is also the second Local Oscillator (LO_2) for the RF receiver.
3	3	PLL V_{ref}	Supply	Voltage Regulator output pin. The internal voltage regulator provides a stable power supply voltage for the R_X and T_X PLL's and can also be used as a regulated supply voltage for the other IC's.
4	4	R_X PD	Output	Three state voltage output of the R_X Phase Detector. This pin is either "high", "low", or "high impedance" depending on the phase difference of the phase detector input signals. During lock, very narrow pulses with a frequency equal to the reference frequency are present. This pin drives the external R_X PLL loop filter. It is important to minimize the line length and capacitance of this pin.
5	5	Gnd PLL	Gnd	Ground pin for PLL section of IC.
6	6	T_X PD	Output	Three state voltage output of the T_X Phase Detector. This pin is either "high", "low", or "high impedance" depending on the phase difference of the phase detector input signals. During lock, very narrow pulses with a frequency equal to the reference frequency are present. This pin drives the external T_X PLL loop filter. It is important to minimize the line length and capacitance on this pin.
7	7	E Cap	–	Expander rectifier filter capacitor pin. Connect capacitor to V_{CC}.
8	8	T_X VCO	Input	Transmit divide counter input which is driven by an ac coupled external transmit loop VCO. The minimum signal level is 200 mV_{pp} @ 80.0 MHz. This pin also functions as the test mode input for the counter tests.
9 10 11	9 10 11	Data EN Clk	Input	Microprocessor serial interface input pins for programming various counters and control functions.
12	12	Clk Out	Output	Microprocesor Clock Output which is derived from the 2nd LO crystal oscillator and a programmable divider. It can be used to drive a microprocessor and thereby reduce the number of crystals required in the system design. The driver has an internal resistor in series with the output whch can be combined with an external capacitor to form a low pass filter to reduce radiated noise on the PCB. This output also functions as the output for the counter test modes.
N/A	14	Status Out	Output	This pin indicates when the internal latches may have lost memory due to a power glitch.
13	15	CD Out/ Hardware Interrupt	Output/ Input	Dual function pin; 1) Carrier detect output (open collector with external 100 kΩ pull–up resistor. 2) Hardware interrupt input which can be used to "wake–up" from Inactive Mode.
14	16	BD Out	Output	Low battery detect output (open collector with external pull–up resistor).
15	17	DA Out	Output	Data amplifier output (open collector with internal 100 kΩ pull–up resistor).
16	18	SA Out	Output	Speaker amplifier output.
17	19	SA In	Input	Speaker amplifier input (ac coupled).
18	20	E Out	Output	Expander output.
19	21	V_{CC} Audio	Supply	V_{CC} supply for audio section.
20	22	DA In	Input	Data amplifier input (ac coupled).
21	23	Pre–Amp Out	Output	Pre–amplifier output for connection of pre–amplifier feedback resistor.
22	24	R_X Audio In	Input	R_X audio input to pre–amplifier (ac coupled).
23	25	Det Out	Output	Audio output from FM detector.
24	26	RSSI	–	Receive signal strength indicator filter capacitor.
N/A	27	N/A	–	Note used.
25	28	Q Coil	–	A quad coil or ceramic discriminator are connected to this pin.
26	29	V_{CC} RF	Supply	V_{CC} supply for RF receiver section.
27 28	30 31	Lim C2 Lim C1	–	IF amplifier/limiter capacitor pins.

PIN FUNCTION DESCRIPTION (continued)

48–TQFP Pin	52–QFP Pin	Symbol	Type	Description
29	32	Lim In	Input	Signal input for IF amplifier/limiter.
30	33	Gnd RF	Gnd	Ground pin for RF section of the IC.
31	34	Mix_2 Out	Output	Second mixer output.
32	35	Mix_2 In	Input	Second mixer input.
33	36	V_B	–	Internal half supply analog ground reference.
34	37	Mix_1 Out	Output	First mixer output.
35	38	Mix_1 In_2	Input	Negative polarity first mixer input.
36	39	Mix_1 In_1	Input	Positive polarity first mixer input.
37 38	40 41	LO_1 In LO_1 Out	–	Tank elements for 1st LO multivibrator oscillator are connected to these pins.
39	42	V_{cap} Ctrl	–	1st LO varactor control pin.
40	43	Gnd Audio	Gnd	Ground for audio section of the IC.
41	44	T_x In	Input	T_x path input to Microphone Amplifier (ac coupled).
42	45	Amp Out	Output	Microphone amplifier output.
43	46	C In	Input	Compressor input (ac coupled).
44	47	C Cap	–	Compressor rectifier filter capacitor pin. Connect capacitor to V_{CC}.
45	48	Lim Out	Output	T_x path limiter output.
46	49	Spl Amp In	Input	Splatter amplifier input (ac coupled).
47	50	T_x Out	Output	T_x path audio output.
48	51	Ref	Input	Reference voltage input for low battery detect.
N/A	52	N/A	–	Not used.

Power Supply Voltage

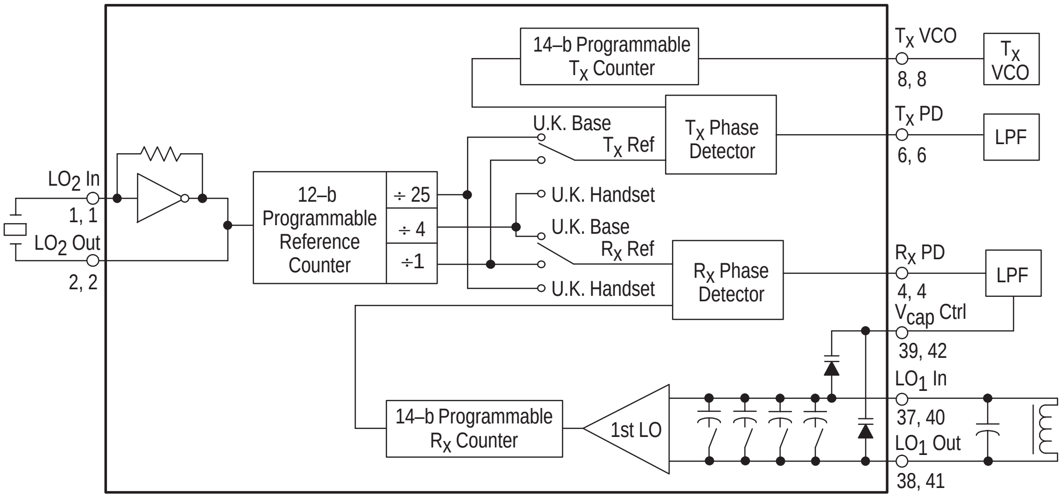
This circuit is used in a cordless telephone handset and base unit. The handset is battery powered and can operate on two ro three NiCad cells or on 5.0 V power.

PLL Frequency Synthesizer General Description

Figure 8 shows a simplified block diagram of the programmable universal dual phase locked loop (PLL). This dual PLL is fully programmable thorugh the MCU serial interface and supports most country channel frequencies including USA (25 ch), France, Spain, Australia, Korea, New Zealand, U.K., Netherlands and China (see channel frequency tables in Appendix A).

The 2nd local oscillator and reference divider provide the reference frequency for the R_x and T_x PLL loops. The programmed divider value for the reference divider is selected based on the crystal frequency and the desired R_x and T_x reference frequency values. Additional divide by 25 and divide by 4 blocks are provided to allow for generation of the 1.0 kHz and 6.25 kHz reference frequencies required for the U.K. The 14–bit T_x counter is programmed for the desired transmit channel frequency. The 14–bit R_x counter is programmed for the desired first local oscillator frequency. All counters power up in the proper default state for USA channel #6 and for a 10.24 MHz reference frequency crystal. Internal fixed capacitors can be connected to the tank circuit of the 1st LO through microprocessor control to extend the sensitivity of the 1st LO for U.S. 25 channel operation.

Figure 8. Dual PLL Simplified Block Diagram



ELECTRICAL CHARACTERISTICS (V_{CC} = 2.6 V, T_A = 25°C)

Characteristic	Condition	Measure Pin	Symbol	Min	Max	Unit
PLL PIN DC						
Input Voltage Low	–	Data Clk EN Hardware Int.	V_{IL}	–	0.3	V
Input Voltage High	–	Data Clk EN	V_{IH}	"PLL V_{ref}" – 0.3	"V_{CC} Audio"	V
Input Current Low	V_{in} = 0.3 V	Data Clk EN	I_{IL}	–5.0	–	µA
Input Current High	V_{in} = (V_{CC} Audio) – 0.3	Data Clk EN	I_{IH}	–	5.0	µA
Hysteresis Voltage	–	Data Clk EN	V_{hys}	1.0	–	V
Output Current High	–	R_X PD T_X PD	I_{OH}	–	–0.7	mA
Output Current Low	–	R_X PD T_X PD	I_{OL}	0.7	–	mA
Output Voltage Low	I_{IL} = 0.7 mA	R_X PD T_X PD	V_{OL}	–	(PLL V_{ref})* 0.2	V
Output Voltage High	I_{IH} = –0. 7mA	R_X PD T_X PD	V_{OH}	(PLL V_{ref})* 0.8	–	V
Tri–State Leakage Current	V = 1.2 V	R_X PD T_X PD	I_{OZ}	–50	50	nA
Input Capacitance	–	Data Clk EN	C_{in}	–	8.0	pF
Output Capacitance	–	R_X PD T_X PD	C_{out}	–	8.0	pF

ELECTRICAL CHARACTERISTICS (continued) (V_{CC} = 2.6 V, T_A = 25°C)

Characteristic	Condition	Measure Pin	Symbol	Min	Max	Unit
PLL PIN INTERFACE						
EN to Clk Setup Time	–	EN, Clk	t_{suEC}	200	–	ns
Data to Clk Setup Time	–	Data, Clk	t_{suDC}	100	–	ns
Hold Time	–	Data, Clk	t_h	90	–	ns
Recovery Time	–	EN, Clk	t_{rec}	90	–	ns
Input Pulse Width	–	EN, Clk	t_w	100	–	ns
Input Rise and Fall Time	–	Data Clk EN	t_r, t_f	– – –	9.0 – –	µs
MPU Interface Power–Up Delay	90% of PLL V_{ref} to Data, Clk, EN	–	t_{puMPU}	–	100	µs

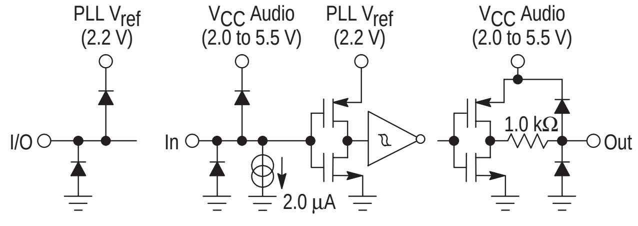
PLL LOOP

Characteristic	Condition	Measure Pin	Symbol	Min	Max	Unit
2nd LO Frequency	–	LO_2 In LO_2 Out	f_{LO}	–	12	MHz
“T_x VCO” Input Frequency	V_{in} = 200 mV_{pp}	T_x VCO	f_{txmax}	–	80	MHz

PLL I/O Pin Specifications

The 2nd LO, R_x and T_x PLL’s and MPU serial interface are normally powered by the internal voltage regulator at the “PLL V_{ref}” pin. The “PLL V_{ref}” pin is the output of a voltage regulator which is powered from the “V_{CC} Audio” power supply pin. Therefore, the maximum input and output levels for most PLL I/O pins (LO_2 In, LO_2 Out, R_x PD, T_x PD, T_x VCO) is the regulated voltage at the “PLL V_{ref}” pin. The ESD protection diodes on these pins are also connected to “PLL V_{ref}”. Internal level shift buffers are provided for the pins (Data, Clk, EN, Clk Out) which connect directly to the microprocessor. The maximum input and output levels for these pins is V_{CC}. Figure 9 shows a simplified schematic of the PLL I/O pins.

Figure 9. PLL I/O Pin Simplified Schematics



LO_2 In, LO_2 Out, R_x PD, T_x PD and T_x VCO Pins

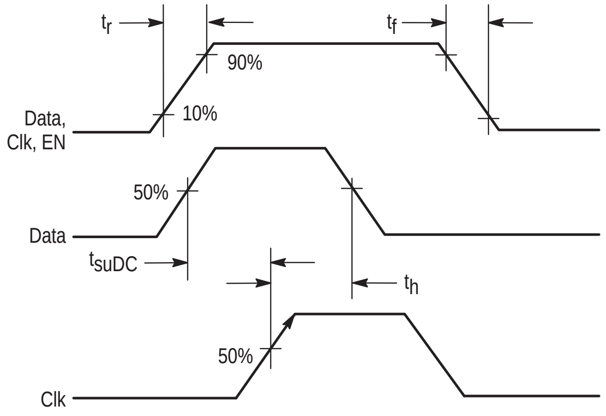
Data, Clk, and EN Pins

Clk Out Pin

Microprocessor Serial Interface

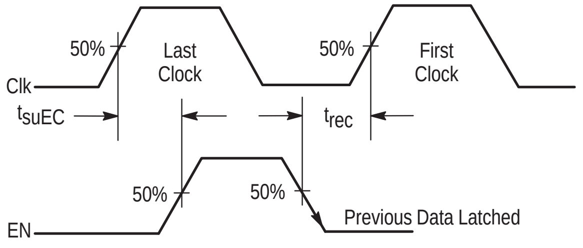
The “Data”, “Clk”, and “EN” pins provide an MPU serial interface for programming the reference counters, the transmit and receive channel divider counter and various control functions. The “Data” and “Clk” pins are used to load data into the shift register. Figure 10 shows “Data” and “Clk” pin timing. Data is clocked on positive clock transitions.

Figure 10. Data and Clock Timing Requirement



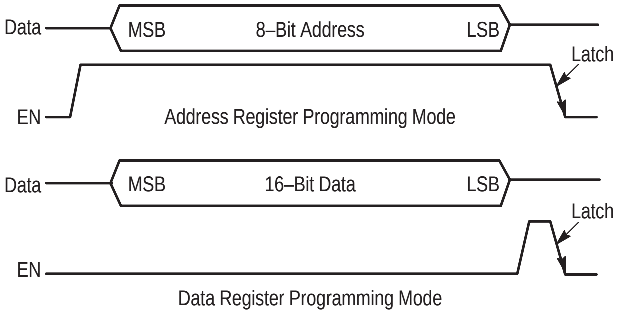
After data is loaded into the shift register, the data is latched into the appropriate latch register using the “EN” pin. This is done in two steps. First, an 8–bit address is loaded into the shift register and latched into the 8–bit address latch register. Then, up to 16–bits of data is loaded into the shift register and latched into the data latch register specified by the address that was previously loaded. Figure 11 shows the timing required on the EN pin. Latching occurs on the negative EN transition.

Figure 11. Enable Timing Requirement



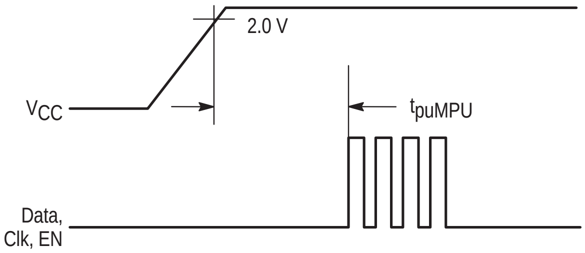
The state of the EN pin when clocking data into the shift register determines whether the data is latched into the address register or a data register. Figure 12 shows the address and data programming diagrams. In the data programming mode, there must not be any clock transitions when “EN” is high. The clock can be in a high state (default high) or a low state (default low) but must not have any transitions during the “EN” high state. The convention in these figures is that latch bits to the left are loaded into the shift register first.

Figure 12. Microprocessor Interface Programming Mode Diagrams



The MPU serial interface is fully operational within 100 µs after the power supply has reached its minimum level during power–up (See Figure 13). The MPU Interface shift registers and data latches are operational in all four power saving modes; Inactive, Standby, R_X, and Active Modes. Data can be loaded into the shift registers and latched into the latch registers in any of the operating modes.

Figure 13. Microprocessor Serial Interface Power–Up Delay



Status Out

This is a digital output which indicates whether the latch registers have been reset to their power–up default values. Latch power–up default values are given in Figure 32. If there is a power glitch or ESD event which causes the latch registers to be reset to their default values, the “Status Out” pin will indicate this to the MPU so it can reload the correct information into the latch registers.

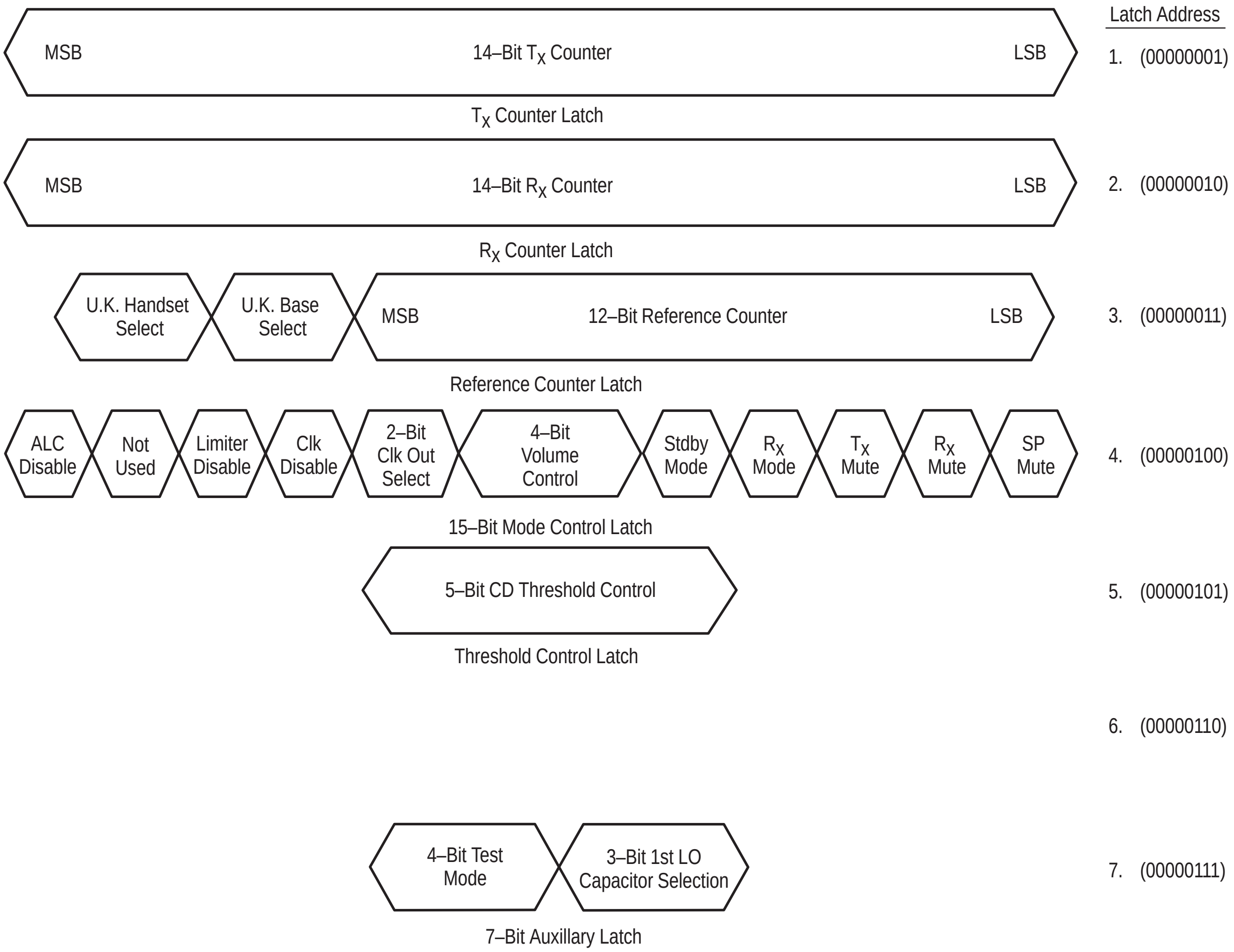
Figure 14. Status Out Operation

Status Latch Register Bits	Status Out Logic Level
Latch bits not at power–up default value	0
Latch bits at power–up default value	1

Data Registers

Figure 15 shows the data latch registers and addresses which are used to select each of these registers. Latch bits to the left (MSB) are loaded into the shift register first. The LSB bit must always be the last bit loaded into the shift register. “Don’t care” bits can be loaded into the shift register first if 8–bit bytes of data are loaded.

Figure 15. Microprocessor Interface Data Latch Registers



Reference Frequency Selection

The “LO_2 In” and “LO_2 Out” pins form a reference oscillator when connected to an external parallel–resonant crystal. The reference oscillator is also the second local oscillator for the RF Receiver. Figure 16 shows the relationship between different crystal frequencies and reference frequencies for cordless phone applications in various countries.

Figure 16. Reference Frequency and Reference Divider Values

Crystal Frequency	Reference Divider Value	U.K. Base/ Handset Divider	Reference Frequency
10.24 MHz	2048	1	5.0 kHz
10.24 MHz	1024	4	2.5 kHz
11.15 MHz	2230	1	5.0 kHz
12.00 MHz	2400	1	5.0 kHz
11.15 MHz	1784	1	6.25 kHz
11.15 MHz	446	4	6.25 kHz
11.15 MHz	446	25	1.0 kHz

Reference Counter

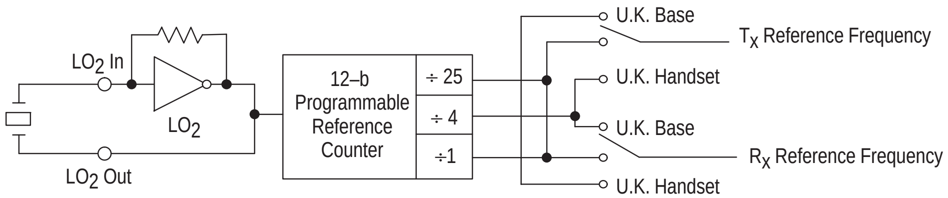
Figure 17 shows how the reference frequencies for the R_X and T_X loops are generated. All countries except U.K. require that the T_X and R_X reference frequencies be identical. In this case, set “U.K. Base Select” and “U.K. Handset Select” bits to “0”. Then the fixed divider is set to “1” and the T_X and R_X reference frequencies will be equal to the crystal oscillator frequency divided by the programmable reference counter value. The U.K. is a special case which requires a different reference frequency value fo T_X and R_X.

For U.K. base operation, set “U.K. Base Select” to “1”. For U.K. handset operation, set “U.K. Handset Select” to “1”. The Netherlands is also a special case since a 2.5 kHz reference frequency is used for both the T_X and R_X reference and the total divider value required is 4096 which is larger than the maximum divide value available from the 12–bit reference divider (4095). In this case, set “U.K. Base Select” to “1” and set “U.K. Handset Select” to “1”. This will give a fixed divide by 4 for both the T_X and R_X reference. Then set the reference divider to 1024 to get a total divider of 4096.

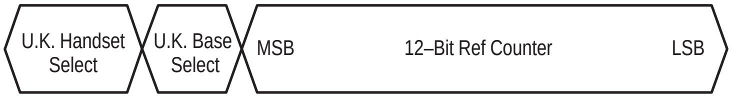
Mode Control Register

Power saving modes, mutes, disables, volume control, and microprocessor clock output frequency are all set by the Control Register. Operation of the Control Register is explained in Figures 18 through 25.

Figure 17. Reference Register Programming Mode



U.K. Handset Select	U.K. Base Select	T_X Divider Value	R_X Divider Value	Application
0	0	1	1	All but U.K. and Netherlands
0	1	25	4	U.K. Base Set
1	0	4	25	U.K. Hand Set
1	1	4	4	Netherlands Base and Hand Set



14–Bit Reference Counter Latch

Figure 18. Control Register Bits

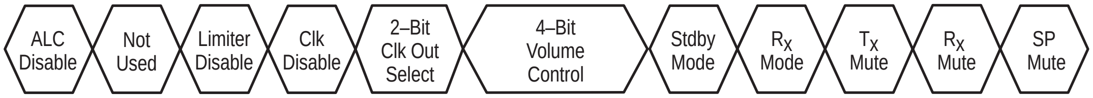


Figure 19. Mute and Disable Control Bit Descriptions

ALC Disable	1 0	Automatic Level Control Disabled Normal Operation
Limiter Disable	1 0	Limiter Disabled Normal Operation
Clock Disable	1 0	MPU Clock Output Disabled Normal Operation
T_X Mute	1 0	Transmit Channel Muted Normal Operation
R_X Mute	1 0	Receive Channel Muted Normal Operation
SP Mute	1 0	Speaker Amp Muted Normal Operation

Power Saving Operating Modes

When the MC13109 is used in a handset, it is important to conserve power in order to prolong battery life. There are five modes of operation; Active, R_X, Standby, Interrupt and Inactive. In Active Mode, all circuit blocks are powered. In R_X mode, all circuitry is powered down exept for those circuit sections needed to receive a transmission from the base. In the Standby and Interrupt Modes, all circuitry is powered down except for the circuitry needed to provide the clock output for the microprocessor. In Inactive Mode, all circuitry is powered down except the MPU interface. Latch memory is maintained in all modes. Figure 20 shows the control register bit values for selection of each power saving mode and Figure 21 show the circuit blocks which are powered in each of these operating mode.

Figure 20. Power Saving Mode Selection

Stdby Mode Bit	R_X Mode Bit	"CD Out/Hardware Interrupt" Pin	Power Saving Mode
0	0	X	Active
0	1	X	R_X
1	0	X	Standby
1	1	1 or High Impedance	Inactive
1	1	0	Inactive

Figure 21. Circuit Blocks Powered During Power Saving Modes

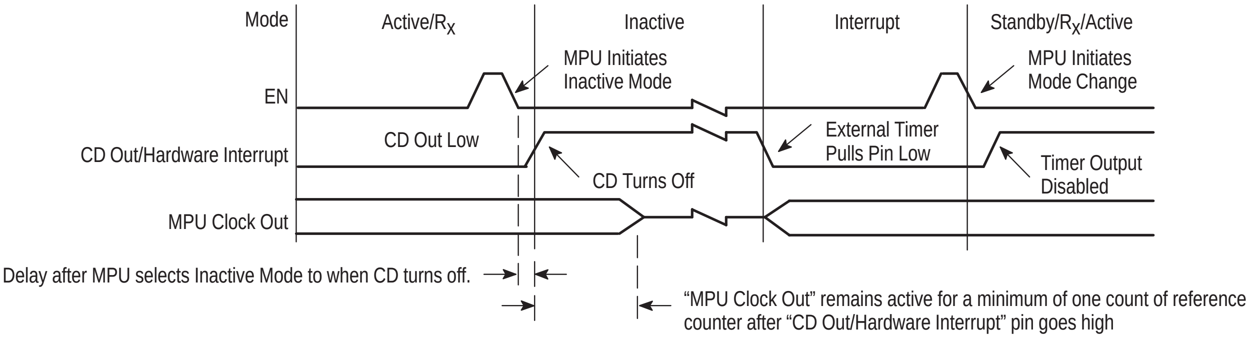
Circuit Blocks	Active	R_X	Standby	Inactive
“PLL V_{ref}” Regulated Voltage	X	X	X[1]	X[1]
MPU Interface	X	X	X	X
2nd LO Oscillator	X	X	X	
MPU Clock Output	X	X	X	
RF Receiver	X	X		
1st LO VCO	X	X		
R_X PLL	X	X		
Carrier Detect	X	X		
Data Amp	X	X		
Low Battery Detect	X	X		
T_X PLL	X			
R_X Audio Path	X			
T_X Audio Path	X			

NOTE: 1. In Standby and Inactive Modes, “PLL V_{ref}” remains powered but is not regulated. It will fluctuate with V_{CC}.

Inactive Mode Operation and Hardware Interrupt

In some handset applications it may be desirable to power down all circuitry including the microprocessor (MPU). First put the MC13109 into the Inactive mode, which turns off the MPU Clock Output (see Figure 22), and then disable the microprocessor. In order to give the MPU adequate time to power down, the MPU Clock output remains active for a minimum of one reference counter cycle (about 200 µs) after the command is given to switch into the “Inactive” mode. An external timing circuit should be used to initiate the turn–on sequence. The “CD Out” pin has a dual function. In the Active and R_X modes it performs the carrier detect function. In the Standby and Inactive modes the carrier detect circuit is disabled and the “CD Out” pin is in a “High” state due to the external pull–up resistor. In the Inactive mode the “CD Out” pin is the input for the hardware interrupt function. When the “CD Out” pin is pulled “low” by the external timing circuit, the MC13109 swtiches from the Inactive to the Interrupt mode thereby turning on the MPU Clock Output. The MPU can then resume control of the combo IC. The “CD Out” pin must remain low until the MPU changes the operating mode from Interrupt to Standby, Active or R_X modes.

Figure 22. Hardware Interrupt Operation



“Clk Out” Divider Programming

The “Clk Out” pin is derived from the 2nd local oscillator and can be used to drive a microprocessor, thereby reducing the number of crystals required. Figure 23 shows the relationship between the crystal frequency and the clock output for different divider values. Figure 24 shows the “Clk Out” register bit values.

Figure 23. Clock Output Values

Crystal Frequency	Clock Output Divider			
	2	3	5	10
10.24 MHz	5.120 MHz	3.413 MHz	2.560 MHz	2.048 MHz
11.15 MHz	5.575 MHz	3.717 MHz	2.788 MHz	2.230 MHz
12.00 MHz	6.000 MHz	4.000 MHz	3.000 MHz	2.400 MHz

Figure 24. Clock Output Divider

Clk Out Bit #1	Clk Out Bit #0	Clk Out Divider Value
0	0	2
0	1	3
1	0	5
1	1	10

MPU “Clk Out“ Power–Up Default Divider Value

The power–up default divider value is “divide by 10”. This provides an MPU clock of about 1.0 MHz after initial power–up. The reason for choosing this relatively low clock frequency after intial power–up is that some microprocessors that operate down to a 2.0 V power supply have a maximum clock frequency fo 1.0 MHz. After initial power–up, the MPU can change the clock divider value to set the clock to the desired operating frequency. Special care has been taken in the design of the clock divider to ensure that the transition between one clock divider value and another is “smooth” (i.e., there will be no narrow clock pulses to disturb the MPU).

MPU “Clk Out” Radiated Noise on Circuit Board

The clock line running between the MC13109 and the microprocessor has the potential to radiate noise which can cause problems in the system especially if the clock is a square wave digital signal with large high frequency harmonics. In order to minimize radiated noise, a 1.0 kΩ resistor is included on–chip in–series with the “Clk Out” output driver. A small capacitor can be connected to the “Clk Out” line on the PCB to form a single pole low pass filter. This filter will significantly reduce noise radiated from the “Clk Out” line.

Volume Control

The volume control can be programmed in 2.0 dB gain steps from –14 dB to +16 dB. The power–up default value is 0 dB.

Figure 25. Volume Control

Volume Control Bit #3	Volume Control Bit #2	Volume Control Bit #1	Volume Control Bit #0	Volume Control #	Gain/Attenuation Amount
0	0	0	0	0	–14 dB
0	0	0	1	1	–12 dB
0	0	1	0	2	–10 dB
0	0	1	1	3	–8.0 dB
0	1	0	0	4	–6.0 dB
0	1	0	1	5	–4.0 dB
0	1	1	0	6	–2.0 dB
0	1	1	1	7	0 dB
1	0	0	0	8	2.0 dB
1	0	0	1	9	4.0 dB
1	0	1	0	10	6.0 dB
1	0	1	1	11	8.0 dB
1	1	0	0	12	10 dB
1	1	0	1	13	12 dB
1	1	1	0	14	14 dB
1	1	1	1	15	16 dB

Gain Control Register

The gain control register contains bits which control the Carrier Detect threshold. Operation of these latch bits are explained in Figures 26 and 27.

Figure 26. Gain Control Latch Bits

Carrier Detect Threshold Programming

Th "CD Out" pin will give an indication to the microprocessor if a carier signal is present on the selected channel. The nominal value and tolerance of the carrier detect threshold is given in the carrier detect specification section of this document. If a different carrier detect threshold value is desired, it can be set through the MPU interface as shown in Figure 27 below.

Figure 27. Carrier Detect Threshold Control

CD Bit #4	CD Bit #3	CD Bit #2	CD Bit #1	CD Bit #0	CD Control #	Carrier Detect Threshold
0	0	0	0	0	0	–20 dB
0	0	0	0	1	1	–19 dB
0	0	0	1	0	2	–18 dB
0	0	0	1	1	3	–17 dB
0	0	1	0	0	4	–16 dB
0	0	1	0	1	5	–15 dB
0	0	1	1	0	6	–14 dB
0	0	1	1	1	7	–13 dB
0	1	0	0	0	8	–12 dB
0	1	0	0	1	9	–11 dB
0	1	0	1	0	10	–10 dB
0	1	0	1	1	11	–9.0 dB
0	1	1	0	0	12	–8.0 dB
0	1	1	0	1	13	–7.0 dB
0	1	1	1	0	14	–6.0 dB
0	1	1	1	1	15	–5.0 dB
1	0	0	0	0	16	–4.0 dB
1	0	0	0	1	17	–3.0 dB
1	0	0	1	0	18	–2.0 dB
1	0	0	1	1	19	–1.0 dB
1	0	1	0	0	20	0 dB
1	0	1	0	1	21	1.0 dB
1	0	1	1	0	22	2.0 dB
1	0	1	1	1	23	3.0 dB
1	1	0	0	0	24	4.0 dB
1	1	0	0	1	25	5.0 dB
1	1	0	1	0	26	6.0 dB
1	1	0	1	1	27	7.0 dB
1	1	1	0	0	28	8.0 dB
1	1	1	0	1	29	9.0 dB
1	1	1	1	0	30	10 dB
1	1	1	1	1	31	11 dB

Auxiliary Register

The auxiliary register contains a 3–bit 1st LO Capacitor Selection latch and a 4–bit Test Mode latch. Operation of these latch bits are explained in Figures 28, 29 and 30.

Figure 28. Auxiliary Register Latch Bits

First Local Oscillator Capacitor Selection for 25 Channel U.S. Operation

There is a very large frequency difference between the minimum and maximum channel frequencies in the proposed 25 Channel U.S. standard. The sensitivity of the 1st LO is not large enough to accommodate this large frequency variation. Fixed capacitors can be connected across the 1st LO tank circuit to change the 1st LO sensitivity. Internal switches and capacitors are provided to enable microprocessor control over internal fixed capacitor values. Figure 29 shows the schematic of the 1st LO tank circuit. Figure 30 shows the latch control bit values.

The internal varactor temperature coefficient is 1800 ppm/°C (C_O = 8.9 pF at 25°C, V_{cap} control voltage = 1.2 V, F_{req} = 36 MHz). Customer is suggested to use a negative temperature coefficient capacitor in 1st LO tank circuit when the whole operating temperature range of –40 to +85°C is considered.

Figure 29. 1st LO Schematic

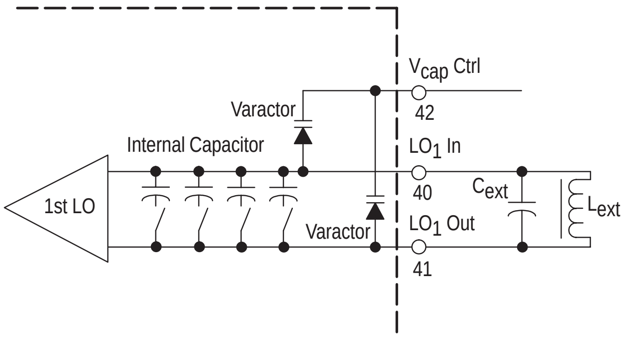


Figure 30. 1st LO Capacitor Select for U.S. 25 Channels

1st LO Cap. Bit 2	1st LO Cap. Bit 1	1st LO Cap Bit 0	1st LO Cap. Select	U.S. Base Channels	U.S. Handset Channels	Internal Cap. Value (Excluding Varactor)	Varactor Value over 0.5 to 2.2 V Range	External Capacitor Value	External Inductor Value
0	0	0	0	16 – 25	–	0.92 pF	10 – 6.4 pF	27 pF	0.47 µH
0	0	0	0	–	16 – 25	0.92 pF	10 – 6.4 pF	33 pF	0.47 µH
0	0	1	1	1 – 6	–	2.61 pF	10 – 6.4 pF	27 pF	0.47 µH
0	1	0	2	7 – 15	–	1.82 pF	10 – 6.4 pF	27 pF	0.47 µH
0	1	1	3	–	1 – 6	8.69 pF	10 – 6.4 pF	33 pF	0.47 µH
1	0	0	4	–	7 – 15	7.19 pF	10 – 6.4 pF	33 pF	0.47 µH

Figure 31. Test Mode Description

TM #	TM 3	TM 2	TM 1	TM 0	Counter Under Test or Test Mode Option	"T_X V_{CO}" Input Signal	"Clk Out" Output Expected
0	0	0	0	0	Normal Operation	>200 mV_{pp}	–
1	0	0	0	1	R_X Counter, upper 6	0 to 2.2 V	Input Frequency/64
2	0	0	1	0	R_X Counter, lower 8	0 to 2.2 V	See Note Below
3	0	0	1	1	R_X Prescaler	0 to 2.2 V	Input Frequency/4
4	0	1	0	0	T_X Counter, upper 6	0 to 2.2 V	Input Frequency/64
5	0	1	0	1	T_X Counter, lower 8	0 to 2.2 V	See Note Below
6	0	1	1	0	T_X Prescaler	>200 mV_{pp}	Input Frequency/4
7	0	1	1	1	Reference Counter	0 to 2.2 V	Input Frequency/Reference Counter Value
8	1	0	0	0	Divide by 4, 25	0 to 2.2 V	Input Frequency/100
9	1	0	0	1	AGC Gain = 10 Option	N/A	–
10	1	0	1	0	AGC Gain = 25 Option	N/A	–

NOTE: To determine the correct output, look at the lower 8 bits in the R_X or T_X register (Divisor (7;0). If the value of the divisor is > 16, then the output divisor value is Divisor (7;2) (the upper 6 bits of the divisor). If Divisor (7;0) < 16 and Divisor (3;2) > = 2, then output divisor value is Divisor (3;2) (bits 2 and 3 of the divisor). If Divisor (7;0) < 16 and Divisor (3;2) < 2, then output divisor value is (Divisor (3;2) + 60).

Test Modes

Test Mode Control latch bits enable independent testing of internal counters and set AGC Gain Options. In test mode, the "T_X VCO" input pin is multiplexed to the input of the counter under test and the output of the counter under test is multiplexed to the "Clk Out" output pin so that each counter can be individually tested. Make sure test mode bits are set to "0" for normal operation. Test mode operation is described in Figure 31. During normal operation and when testing the T_X Prescaler, the "T_X VCO" input can be a minimum of 200 mV_{pp} at 80 MHz and should be ac coupled. For other test modes, input signals should be standard logic levels of 0 to 2.2 V and a maximum frequency of 16 MHz.

Power–Up Defaults for Control and Counter Registers

When the IC is first powered up, all latch registers are initialized to a defined state. The MC13109 is initially placed in the Rx mode with all mutes active and nothing disabled. The reference counter is set to generate a 5.0 kHz reference frequency from a 10.24 MHz crystal. The MPU clock output divider is set to 10 to give the minimum clock output frequency. The T_X and R_X latch registers are set for USA Channel Frequency #21. Figure 32 shows the initial power–up states for all latch registers.

Figure 32. Latch Register Power–Up Defaults

Register	Count	MSB								LSB							
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
T_X	9966	–	–	1	0	0	1	1	0	1	1	1	0	1	1	1	0
R_X	7215	–	–	0	1	1	1	0	0	0	0	1	0	1	1	1	1
Ref	2048	–	–	0	0	1	0	0	0	0	0	0	0	0	0	0	0
Mode	N/A	–	0	0	0	0	1	1	0	1	1	1	0	1	1	1	1
Gain	N/A	–	–	–	–	–	–	–	–	–	–	–	1	0	1	0	0
TM	N/A	–	–	–	–	–	–	–	–	–	0	0	0	0	0	0	0

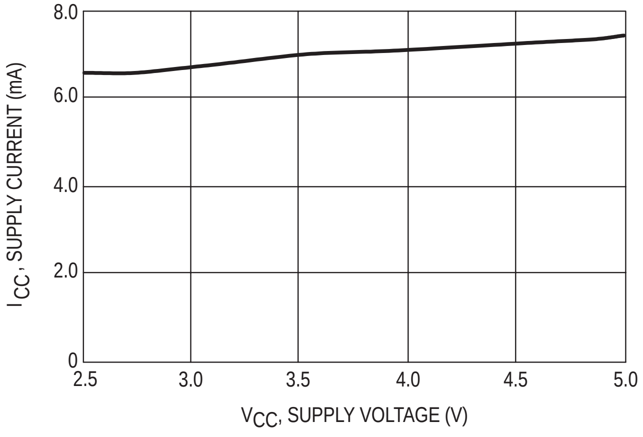


Figure 33. I_{CC} versus V_{CC} at Active Mode

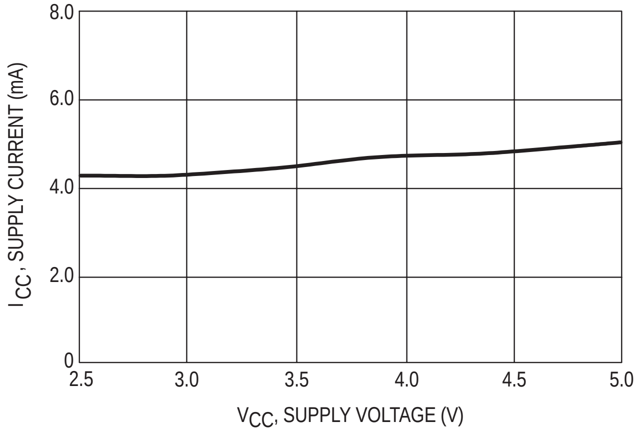


Figure 34. I_{CC} versus V_{CC} at Receive Mode

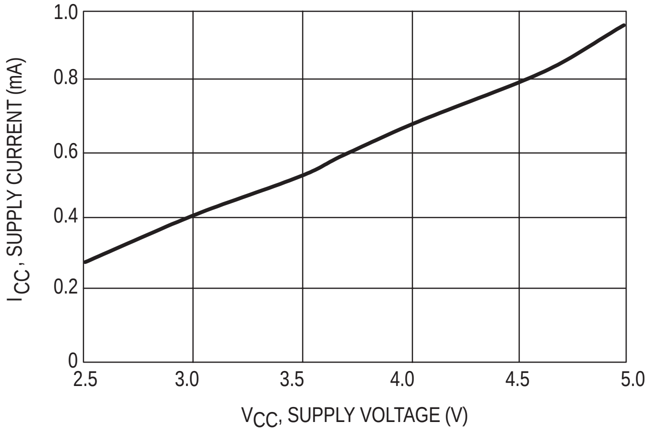


Figure 35. I_{CC} versus V_{CC} at Standby Mode

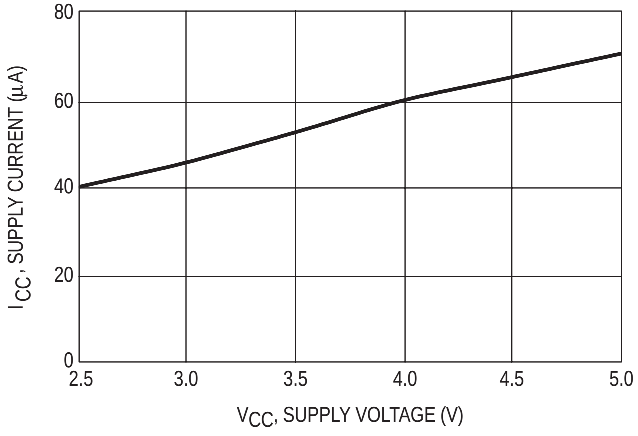


Figure 36. I_{CC} versus V_{CC} at Inactive Mode

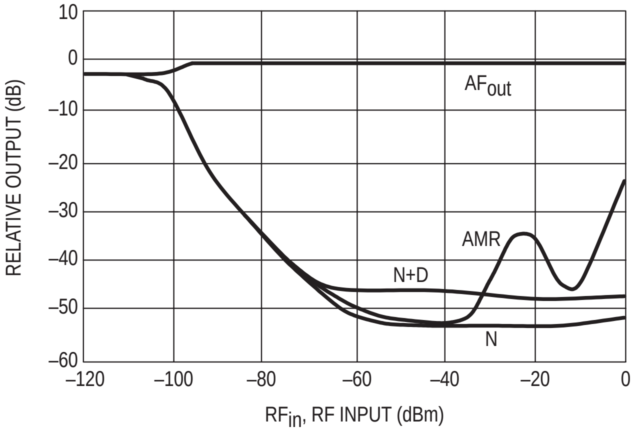


Figure 37. RF_{in} versus AF_{out}, N+D, N, AMR

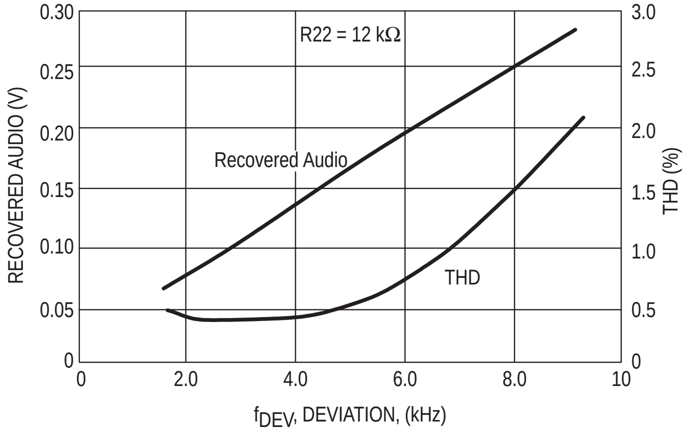


Figure 38. Recovered Audio/THD versus f_{DEV}

Figure 39. RSSI Output versus RF$_{in}$

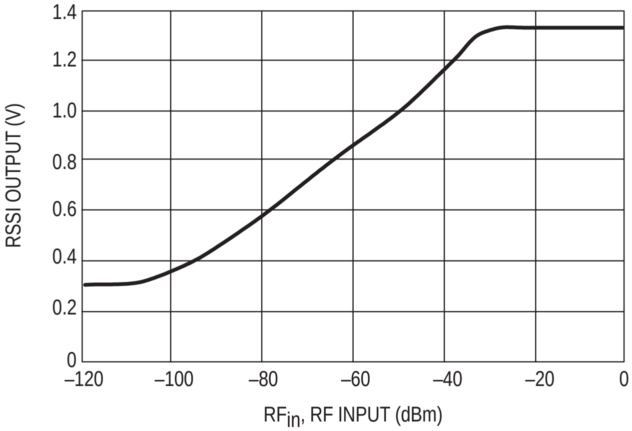
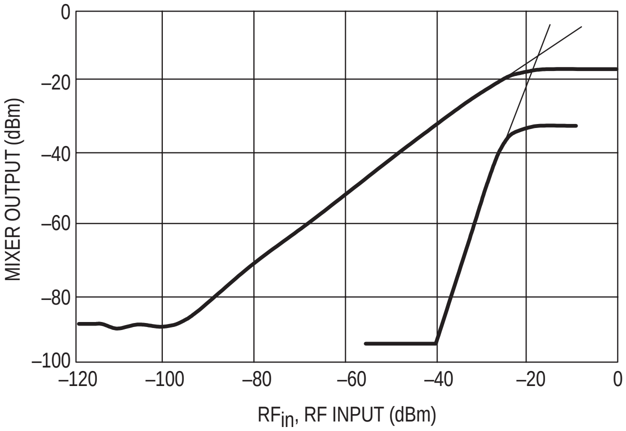


Figure 40. First Mixer Third Order Intercept Performance



APPENDIX A – MEASUREMENT OF COMPANDOR ATTACK/DECAY TIME

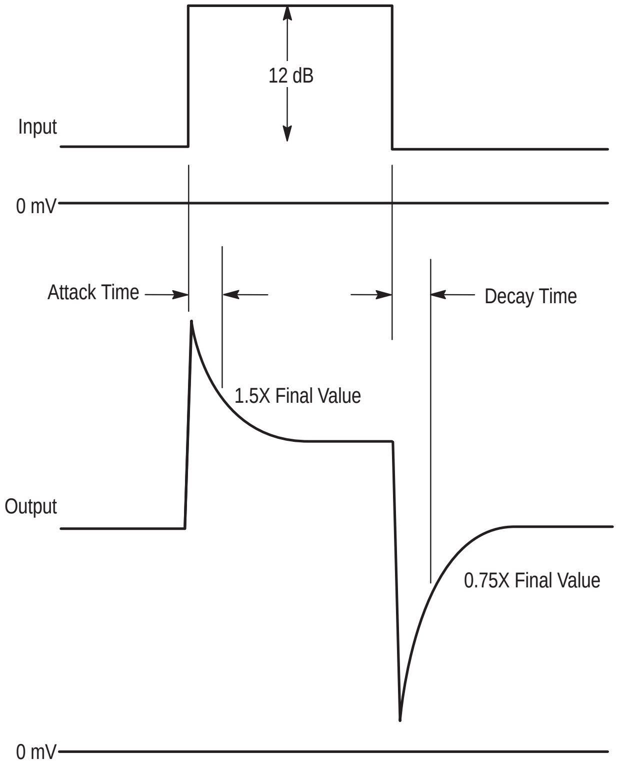
This measurement definition is based on EIA/CCITT recommendations.

Compressor Attack Time

For a 12 dB step up at the input, attack time is defined as the time for the output to settle to 1.5X of the final steady state value.

Compressor Decay Time

For a 12 dB step down at the input, decay time is defined as the time for the input to settle to 0.75X of the final steady state value.

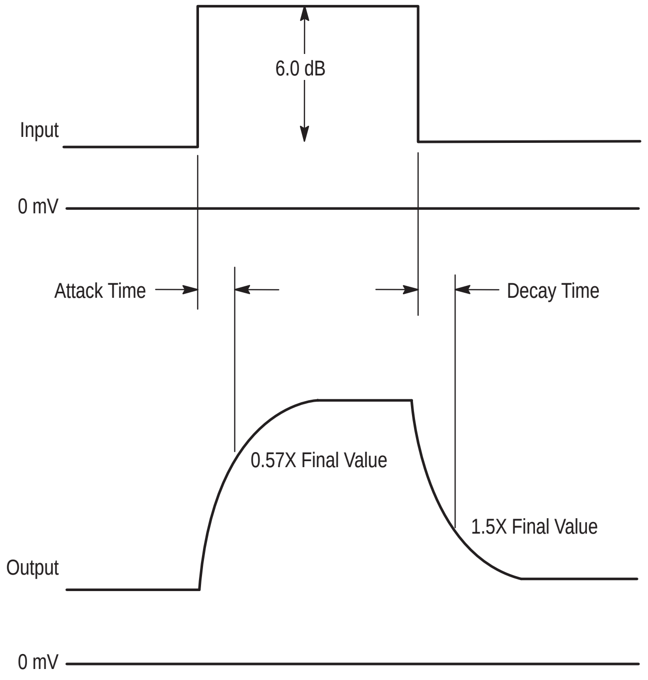


Expander Attack

For a 6.0 dB step up at the input, attack time is defined as the time for the output to settle to 0.57X of the final steady state value.

Expander Decay

For a 6.0 dB step down at the input, decay time is defined as the time for the output to settle to 1.5X of the final steady state value.



MOTOROLA

Universal Cordless Telephone Subsystem IC with Scrambler

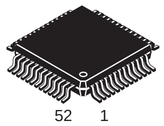
The MC13110 integrates several of the functions required for a cordless telephone into a single integrated circuit. This significantly reduces component count, board space requirements, and external adjustments. It is designed for use in both the handset and the base.

- Dual Conversion FM Receiver
  - Complete Dual Conversion Receiver – Antenna In to Audio Out 80 MHz Maximum Carrier Frequency
  - RSSI Output
  - Carrier Detect Output with Programmable Threshold
  - Comparator for Data Recovery
  - Operates with Either a Quad Coil or Ceramic Discriminator
- Compander
  - Expandor Includes Mute, Digital Volume Control, Speaker Driver, 3.5 kHz Low Pass Filter, and Programmable Gain Block
  - Compressor Includes Mute, 3.5 kHz Low Pass Filter, Limiter, and Programmable Gain Block
- Dual Universal Programmable PLL
  - Supports New 25 Channel U.S. Standard with New External Switches
  - Universal Design for Domestic and Foreign CT–1 Standards
  - Digitally Controlled Via a Serial Interface Port
  - Receive Side Includes 1st LO VCO, Phase Detector, and 14–Bit Programmable Counter and 2nd LO with 12–Bit Counter
  - Transmit Section Contains Phase Detector and 14–Bit Counter
  - MPU Clock Outputs Eliminates Need for MPU Crystal
- Supply Voltage Monitor
  - Provides Two Levels of Monitoring with Separate Outputs
  - Separate, Adjustable Trip Points
- Frequency Inversion Scrambler/Descrambler
  - Can Be Enabled/Disabled Via MPU Interface
  - Programmable Carrier Modulation Frequency
- 2.7 to 5.5 V Operation with One–Third the Power Consumption of Competing Devices
- AN1575: Refer to this Application Note for a List of the “Worldwide Cordless Telephone Frequencies” (List can also be found in Chapter 8 Addendum of DL128 Data Book)

MC13110

UNIVERSAL CT–1 SUBSYSTEM INTEGRATED CIRCUIT

SEMICONDUCTOR TECHNICAL DATA

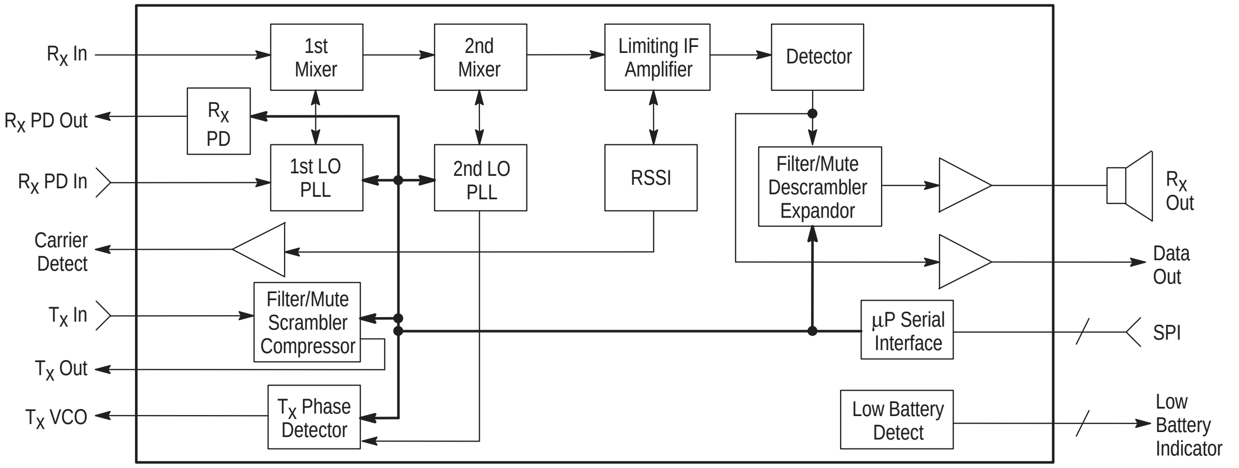


FB SUFFIX
PLASTIC QFP PACKAGE
CASE 848B

ORDERING INFORMATION

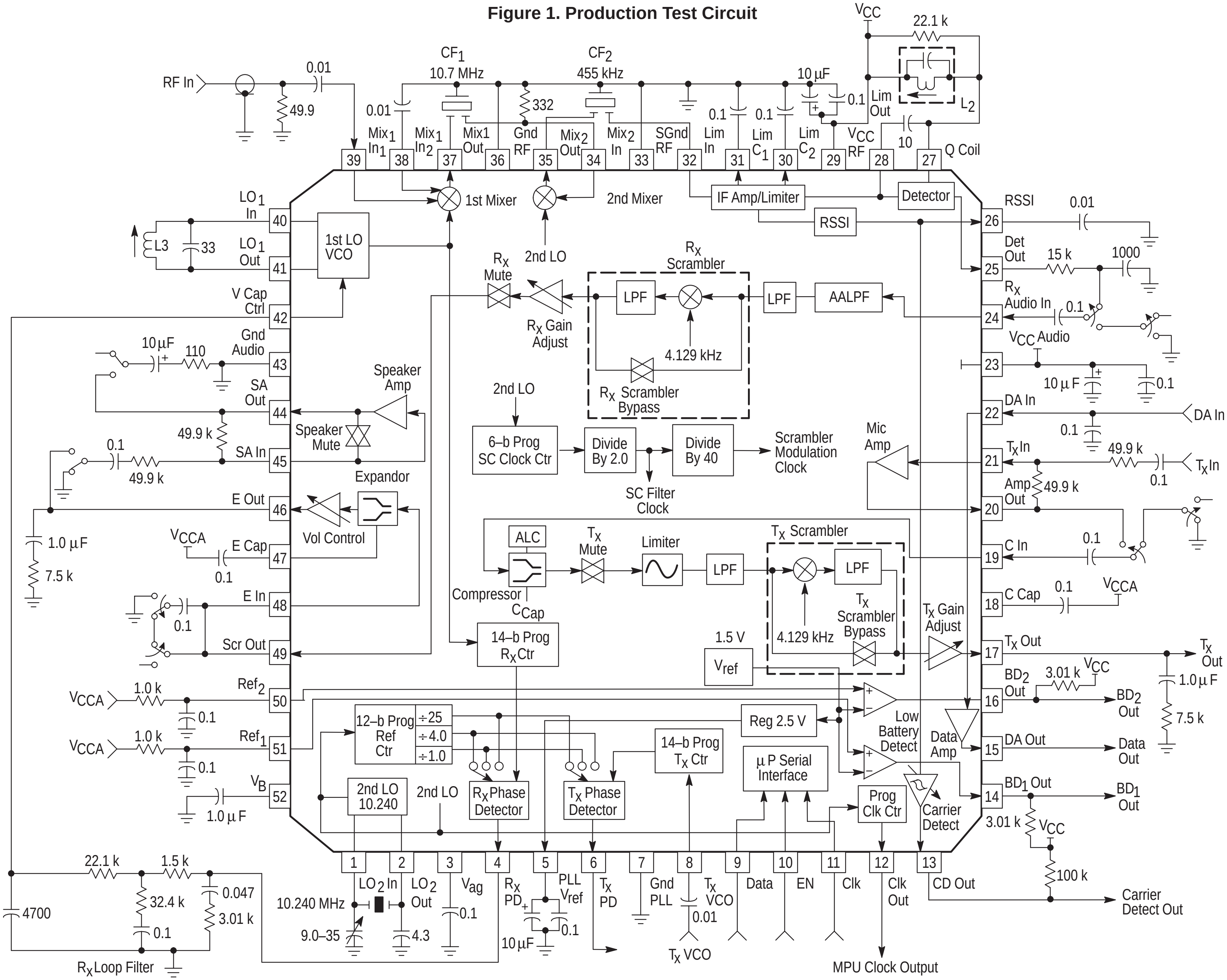
Device	Tested Operating Temperature Range	Package
MC13110FB	T_A = – 40° to +85°C	QFP–52

Simplified Application



This device contains 8,262 active transistors.

Figure 1. Production Test Circuit



NOTE: This schematic is only a representation of the actual production test circuit.

MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	–0.5 to +5.5	Vdc
Junction Temperature	T_J	–65 to +150	°C

NOTES: 1. Devices should not be operated at these limits. The "Recommended Operating Conditions" provide for actual device operation.

2. ESD data available upon request.

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	2.7	3.6	5.0	Vdc
Operating Ambient Temperature	T_A	–40	–	85	°C
Input Voltage Low (Data, Clk, EN)	V_{IL}	–	–	0.3	V
Input Voltage High (Data, Clk, EN)	V_{IH}	2.5	–	–	V
Output Current (R_X PD, T_X PD)					mA
High	I_{OH}	–	–	–0.7	
Low	I_{OL}	0.7	–	–	

NOTE: All limits are not necessarily functional concurrently.

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 3.6 V, T_A = 25°C, unless otherwise specified; Test Circuit Figure 1.)

Characteristic	Symbol	Min	Typ	Max	Unit
Static Current					
Active Mode (2.7 V)	ACT I_{CC}	–	8.1	–	mA
Active Mode	ACT I_{CC}	–	8.6	12	mA
Receive Mode	R_X I_{CC}	–	4.3	5.3	mA
Standby Mode	STD I_{CC}	–	270	500	µA
Inactive Mode	INACT I_{CC}	–	35	80	µA

ELECTRICAL CHARACTERISTICS (V_{CC} = 3.6 V, V_B = 1.5 V, T_A = 25°C, Active or R_X Mode, unless otherwise specified; Test Circuit Figure 1.)

Characteristic	Condition	Input Pin	Measure Pin	Symbol	Min	Typ	Max	Unit
PLL VOLTAGE REGULATOR								
Regulated Output Level	I_L = 0 mA	–	PLL V_{ref}	V_O	2.4	2.5	2.6	V
Line Regulation	I_L = 0 mA, V_{CC} = 3.6 to 5.5 V	V_{CC} Audio	PLL V_{ref}	V_{Reg} Line	–	–0.6	20	mV
Load Regulation	V_{CC} = 3.6 V, I_L = 1.0 mA	V_{CC} Audio	PLL V_{ref}	V_{Reg} Load	–	–1.1	20	mV
PLL LOOP CHARACTERISTICS								
2nd LO Frequency (No Crystal)	–	LO_2 In	–	f_{2ext}	–	12	–	MHz
2nd LO Frequency (With Crystal)	–	–	LO_2 In LO_2 Out	f_{2ext}	–	12	–	MHz
T_X VCO (Input Frequency)	V_{in} = 200 mVpp	–	T_X VCO	f_{txmax}	–	80	–	MHz

ELECTRICAL CHARACTERISTICS (continued) (V_{CC} = 3.6 V, V_B = 1.5 V, T_A = 25°C, Active or R_X Mode, unless otherwise specified; Test Circuit Figure 1.)

Characteristic	Condition	Input Pin	Measure Pin	Symbol	Min	Typ	Max	Unit
PLL PHASE DETECTOR								
Output Voltage Low	I_{IL} = 0.7 mA	–	R_X PD T_X PD	V_{OL}	–	–	(PLL V_{ref}) *.2	V
Output Voltage High	I_{IH} = –0.7 mA	–	R_X PD T_X PD	V_{OL}	(PLL V_{ref}) *.8	–	–	V
3–State Leakage Current	V = 1.2 V	–	R_X PD T_X PD	I_{OZ}	–50	–	50	nA
Output Capacitance	–	–	R_X PD T_X PD	C_{out}	–	8.0	–	pF
Output Rise and Fall Time	C_{Load} = 50 pF	–	R_X PD T_X PD Clk Out	t_r, t_f	–	250	–	ns
MICROPROCESSOR SERIAL INTERFACE								
Input Current Low	V_{in} = 0.3 V Standby Mode	–	Data, Clk, EN	I_{IL}	–5.0	0.3	–	µA
Input Current High	V_{in} = 3.3 V Standby Mode	–	Data, Clk, EN	I_{IH}	–	1.5	5.0	µA
Hysteresis Voltage	–	–	Data, Clk, EN	V_{hys}	–	1.0	–	V
Maximum Clock Frequency	–	Data, EN, Clk	–	–	–	2.0	–	MHz
Input Capacitance	–	Data, Clk, EN	–	C_{in}	–	8.0	–	pF
EN to Clk Setup Time	–	–	EN, Clk	t_{suEC}	–	200	–	ns
Data to Clk Setup Time	–	–	Data, Clk	t_{suDC}	–	100	–	ns
Hold Time	–	–	Data, Clk	t_h	–	90	–	ns
Recovery Time	–	–	EN, Clk	t_{rec}	–	90	–	ns
Input Pulse Width	–	–	EN, Clk	t_w	–	100	–	ns
Input Rise and Fall Time	–	–	Data, Clk, EN	t_r, t_f	–	9.0	–	µs
MPU Interface Power–Up Delay	90% of PLL V_{ref} to Data, Clk, EN	–	–	t_{puMPU}	–	100	–	µs
FM RECEIVER (f_{RF} = 46.77 MHz [USA Ch 21], f_{dev} = ±3.0 kHz, f_{mod} = 1.0 kHz)								
Sensitivity (Input for 12 dB SINAD)	50 Ω Termination	Mix_1 $In_{1/2}$	Det Out	V_{SIN}	– –	2.8 –98	– –	µVrms dBm
	Single–Ended, Matched Input	Mix_1 $In_{1/2}$	Det Out	V_{SIN}	– –	1.0 –107	– –	µVrms dBm
	Differential, Matched Input	Mix_1 $In_{1/2}$	Det Out	V_{SIN}	– –	.56 –112	– –	µVrms dBm
1st Mixer Voltage Conversion Gain	V_{in} = 1.0 mVrms, with CF_1 Filter as Load	Mix_1 $In_{1/2}$	Mix_1 Out	MX_{gain1}	–	12	–	dB
2nd Mixer Voltage Conversion Gain	V_{in} = 3.0 mVrms, with CF_2 Filter as Load	Mix_2 In	Mix_2 Out	MX_{gain2}	–	20	–	dB
1st and 2nd Mixer Voltage Gain Total	V_{in} = 1.0 mVrms, with CF_1 and CF_2 Load	Mix_1 $In_{1/2}$	Mix_2 Out	MX_{gainT}	24	28	–	dB
1st Mixer Input Impedance	Single–Ended Input	–	Mix_1 $In_{1/2}$	R_{P1} C_{P1}	– –	875 2.7	– –	Ω pF
2nd Mixer Input Impedance	f_{in} = 10.7 MHz	–	Mix_2 In	Z_{in2}	–	3.0	–	kΩ

ELECTRICAL CHARACTERISTICS (continued) (V_{CC} = 3.6 V, V_B = 1.5 V, T_A = 25°C, Active or R_X Mode, unless otherwise specified; Test Circuit Figure 1.)

Characteristic	Condition	Input Pin	Measure Pin	Symbol	Min	Typ	Max	Unit
FM RECEIVER (f_{RF} = 46.77 MHz [USA Ch 21], f_{dev} = ±3.0 kHz, f_{mod} = 1.0 kHz)								
1st Mixer Output Impedancet	–	–	Mix$_1$ Out	Z_{out1}	–	330	–	Ω
2nd Mixer Output Impedance	–	–	Mix$_2$ Out	Z_{out2}	–	1.5	–	kΩ
IF –3.0 dB Limiting Sensitivity	f_{in} = 455 kHz	Lim In	Det Out	IF Sens	–	71	100	µVrms
Total Harmonic Distortion	With R_C = 15 k/1.0 nF Filter at Det Out	Mix$_1$ In$_1$	Det Out	THD	–	1.3	2.0	%
Recovered Audio	V_{in} = 3.16 mVrms with R_C = 15 k/1000 pF Filter at Det Out	Mix$_1$ In$_1$	Det Out	AFO	80	105	150	mVrms
Demodulator Bandwidth	–	Lim In	Det Out	BW	–	20	–	kHz
Signal to Noise Ratio	V_{in} = 3.16 mVrms, R_C = 15 k/1000 pF	Mix$_1$ In$_1$	Det Out	SN	–	49	–	dB
AM Rejection Ratio	V_{in} = 3.16 mVrms, 30% AM, @ 1.0 kHz, R_C = 15 k/1000 pF	Mix$_1$ In$_1$	Det Out	AMR	30	47	–	dB
1st Mixer, 1.0 dB Voltage Compression (Input Pin Referred)	–	Mix$_1$ In$_{1/2}$	Mix$_1$ Out	V_O 1.0 dB Mix$_1$	–	15	–	mVrms
2nd Mixer, 1.0 dB Voltage Compression (Input Pin Referred)	50 Ω Input	Mix$_2$ In	Mix$_2$ Out	V_O 1.0 dB Mix$_2$	–	14	–	mVrms
1st Mixer 3rd Order Intercept (Input Pin Referred)	V_{in} = 3.98 mVrms	Mix$_1$ In$_1$	Mix$_1$ Out	TOI_{mix1}	–	56	–	mVrms
2nd Mixer 3rd Order Intercept (Input Pin Referred)	V_{in} = 3.98 mVrms, 50 Ω Input	Mix$_2$ In	Mix$_2$ Out	TOI_{mix2}	–	53	–	mVrms
Detector Output Impedance	–	–	Det Out	Z_O	–	870	–	Ω
RSSI/CARRIER DETECT (R_L = 100 kΩ)								
RSSI Output Current Dynamic Range	–	Mix$_1$ In	RSSI	RSSI	–	80	–	dB
Carrier Sense Threshold	CD Threshold Adjust = (10100)	Mix$_1$ In	CD Out	V_T	–	33	–	µVrms
Hysteresis	–	Mix1 In	CD Out	Hys	–	3.6	7.0	dB
Output High Voltage	V_{in} = 0 Vrms, CD = (10100)	Mix$_1$ In	CD Out	V_{OH}	V_{CC} – 0.1	3.6	–	V
Output Low Voltage	V_{in} = –80 dBV, CD = (10100)	Mix$_1$ In	CD Out	V_{OL}	–	0.02	0.4	V

ELECTRICAL CHARACTERISTICS (continued) (V_{CC} = 3.6 V, V_B = 1.5 V, T_A = 25°C, Active or R_x Mode, unless otherwise specified; Test Circuit Figure 1.)

Characteristic	Condition	Input Pin	Measure Pin	Symbol	Min	Typ	Max	Unit
RSSI/CARRIER DETECT (R_L = 100 kΩ)								
Carrier Sense Threshold Adjustment Range	Programmable through MPU Interface	–	–	V_T low range	–20	–	–	dB
		–	–	V_T hi range	–	–	11	
Carrier Sense Threshold – Number of Steps	Programmable through MPU Interface	–	–	V_{Tn}	–	32	–	–
DATA AMP COMPARATOR								
Hysteresis	–	DA In	DA Out	Hys	30	40	50	mV
Threshold Voltage	–	DA In	DA Out	V_T	2.7	V_{CC} – 0.7	–	V
Input Impedance	–	–	DA In	Z_I	–	11	–	kΩ
Output Impedance	–	–	DA Out	Z_O	–	100	–	kΩ
Output High Voltage	V_{in} = V_{CC} – 1.0 V, I_{OH} = 0 mA	DA In	DA Out	V_{OH}	V_{CC} – 0.1	3.6	–	V
Output Low Voltage	V_{in} = V_{CC} – 0.4 V, I_{OL} = 0 mA	DA In	DA Out	V_{OL}	–	0.04	0.4	V
EXPANDOR/R_X MUTE (f_{in} = 1.0 kHz)								
Absolute Gain	V_{in} = –20 dBV	E In	E Out	G	–3.0	0	3.0	dB
Gain Tracking	V_{in} = –30 dBV V_{in} = –40 dBV	E In	E Out	G_t	–21 –42	–20 –40	–19 –38	dB
Total Harmonic Distortion	V_{in} = –20 dBV	E In	E Out	THD	–	0.5	1.0	%
Maximum Input Voltage	–	R_x Audio In	–	–	–	–11.5	–	dBV
Maximum Output Voltage	Increase input voltage until output voltage THD = 5.0%, then measure output voltage. R_L = 7.5 k/1.0 µF	E In	E Out	V_{Omax}	–	0	–	dBV
Input Impedance	–	R_x Audio In E In	–	Z_{in}	– –	600 7.5	– –	kΩ
Attack Time	E_{cap} = 0.5 µF, R_{filt} = 40 k (See Appendix B)	E In	E Out	t_a	–	3.0	–	ms
Release Time	E_{cap} = 0.5 µF, R_{filt} = 40 k (See Appendix B)	E In	E Out	t_r	–	13.5	–	ms
Compressor to Expandor Crosstalk	V_{in} = –10 dBV, $V_{(E\ In)}$ = AC Gnd	C In	E Out	C_T	–	–90	–70	dB
R_x Data Muting (Δ Gain)	V_{in} = –20 dBV, R_x Gain Adj = (01111)	R_x Audio In	E Out	M_e	–	–83	–60	dB
SPEAKER AMP/SP MUTE								
Maximum Output Swing	V_{in} = 0 dBV, R_L = 130 Ω	SA In	SA Out	V_{Omax}	0.8	0.9	–	Vpp
Speaker Amp Muting	V_{in} = –20 dBV	SA In	SA Out	M_{sp}	–	–90	–60	dB
COMPRESSOR/T_X MUTE (f_{in} = 1.0 kHz, Scrambler Bypass Mode, T_x Gain Adj = (01111), f_{in} = 1.0 kHz)								
Absolute Gain	V_{in} = –10 dBV	T_x In	T_x Out	G	–4.0	0	4.0	dB
Gain Tracking	V_{in} = –30 dBV V_{in} = –40 dBV	T_x In	T_x Out	G_t	–11 –17	–10 –20	–9.0 –13	dB
Total Harmonic Distortion	V_{in} = –10 dBV	T_x In	T_x Out	THD	–	0.6	1.1	%

ELECTRICAL CHARACTERISTICS (continued) (V_{CC} = 3.6 V, V_B = 1.5 V, T_A = 25°C, Active or R_X Mode, unless otherwise specified; Test Circuit Figure 1.)

Characteristic	Condition	Input Pin	Measure Pin	Symbol	Min	Typ	Max	Unit
COMPRESSOR/T_X MUTE (f_{in} = 1.0 kHz, Scrambler Bypass Mode, T_X Gain Adj = (01111), f_{in} = 1.0 kHz)								
Maximum Output Voltage	Increase input voltage until output voltage THD = 5.0%, then measure output voltage. R_L = 7.5 k/1.0 µF	C In	T_X Out	V_{Omax}	–	–5.0	–	dBV
Input Impedance	–	C In	T_X Out	Z_{in}	–	10	–	kΩ
Attack Time	C_{cap} = 0.5 µF, R_{filt} = 40 k (See Appendix B)	C In	T_X Out	t_a	–	3.0	–	ms
Release Time	C_{cap} = 0.5 µF, R_{filt} = 40 k (See Appendix B)	C In	T_X Out	t_r	–	13.5	–	ms
Expandor to Compressor Crosstalk	V_{in} = –20 dBV, Speaker Amp No Load, $V_{(C\ In)}$ = AC Gnd	E In	T_X Out	C_T	–	–60	–40	dB
T_X Muting	V_{in} – 10 dBV	T_X In	T_X Out	M_c	–	–90	–60	dB
ALC Output Level	V_{in} = –10 dBV V_{in} = –2.5 dBV Limiter and Mutes disabled	T_X In	T_X Out	ALC_{out}	–15 –13	–11 –10	–8.0 –6.0	dBV
Limiter Output Level	V_{in} = –2.5 dBV, ALC disabled	T_X In	T_X Out	V_{lim}	–10	–7.0	–	dBV
R_X AND T_X SCRAMBLER (2nd LO = 10.24 MHz, T_X Gain Adj = (01111), R_X Gain Adj = (01111), Volume Control = (0 dB Default Levels), SCF Clock Divider = 31. Total is divide by 62 for SCF clock frequency of 165.16 kHz)								
R_X High Frequency Corner (Note 1)	R_X Path, f = 479 Hz, V R_X Audio In = –20 dBV	R_X Audio In	Scr Out	R_X f_{ch}	–	3.65	–	kHz
T_X High Frequency Corner (Note 1)	T_X Path, f = 250 Hz, V T_X In = –10 dBV, Mic Amp = Unity Gain	T_X In	T_X Out	T_X f_{ch}	–	3.879	–	kHz
Absolute Gain	R_X: V_{in} = –20 dBV T_X: V_{in} = –10 dBV, Limiter disabled	R_X Audio In T_X In	E Out T_X Out	AV	–4.0 –4.0	0 0	4.0 4.0	dB
Pass Band Ripple	R_X + T_X Path – 1.0 µF from T_X Out to R_X Audio In, f_{in} = low corner frequency to high corner frequency	C In	E Out	Ripple	–	2.0	–	dB
Scrambler Modulation Frequency	R_X: 100 mV (–20 dBV) T_X: 316 mV (–10 dBV)	R_X Audio In C In	E Out T_X Out	f_{mod}	4.119	4.129	4.139	kHz
Group Delay	R_X + T_X Path – 1.0 µF from T_X Out to R_X Audio In, f_{in} = 1.0 kHz	C In	E Out	GD	–	1.0	–	ms
	f_{in} = low corner frequency to high corner frequency	C In	E Out	GD	–	4.0	–	
Carrier Breakthrough	R_X + T_X Path – 1.0 µF from T_X Out to R_X Audio In	C In	E Out	CBT	–	–60	–	dB
Baseband Breakthrough	R_X + T_X Path – 1.0 µF from T_X Out to R_X Audio In, f_{in} = 1.0 kHz, f_{meas} = 3.192 kHz	C In	E Out	BBT	–	–50	–	dB

NOTE: 1. The filter specification is based on a 10.24 MHz 2nd LO, and a switched–capacitor (SC) filter counter divider ratio of 31. If other 2nd LO frequencies and/or SC filter counter divider ratios are used, the filter corner frequency will be proportional to the resulting SC filter clock frequency.

ELECTRICAL CHARACTERISTICS (continued) (V_{CC} = 3.6 V, V_B = 1.5 V, T_A = 25°C, Active or R_X Mode, unless otherwise specified; Test Circuit Figure 1.)

Characteristic	Condition	Input Pin	Measure Pin	Symbol	Min	Typ	Max	Unit
MIC AMP (f_{in} = 1.0 kHz, External resistors set to gain of 1)								
Open Loop Gain	–	T_x In	Amp Out	AVOL	–	100,000	–	V/V
Gain Bandwidth	–	T_x In	Amp Out	GBW	–	100	–	kHz
Maximum Output Swing	R_L = 10 kΩ	T_x In	Amp Out	V_{Omax}	–	2.8	–	Vpp
LOW BATTERY DETECT								
Average Threshold Voltage Before Electronic Adjustment	V_{CC} = 3.6 V, $V_{ref_}$Adj = (0111). Take average of rising and falling threshold	Ref_1 Ref_2	BD_1 Out BD_2 Out	VT_i	1.36	1.5	1.64	V
Average Threshold Voltage After Electronic Adjustment	V_{CC} = 3.6 V, $V_{ref_}$Adj = (adjusted value). Take average of rising and falling threshold	Ref_1 Ref_2	BD_1 Out BD_2 Out	VT_f	1.475	1.5	1.525	V
Hysteresis	–	Ref_1 Ref_2	BD_1 Out BD_2 Out	Hys	–	4.0	–	mV
Input Current	V_{in} = 1.0 to 2.0 V	–	Ref_1 Ref_2	I_{in}	–50	–	50	nA
Output High Voltage	V_{in} = 2.0 V, R_L = 3.9 kΩ to V_{CC}	Ref_1 Ref_2	BD_1 Out BD_2 Out	V_{OH}	V_{CC} – 0.1	3.6	–	V
Output Low Voltage	V_{in} = 1.0 V, R_L = 3.9 kΩ to V_{CC}	Ref_1 Ref_2	BD_1 Out BD_2 Out	V_{OL}	–	0.1	0.4	V

PIN FUNCTION DESCRIPTION

Pin	Symbol	Type	Description
1 2	LO_2 In LO2 Out	–	These pins form the PLL reference oscillator when connected to an external parallel–resonant crystal (10.24 MHz typical). The reference oscillator is also the second Local Oscillator (LO_2) for the RF receiver. "LO_2 In" may also serve as an input for an externally generated reference signal which is typically ac–coupled.
3	V_{ag}	–	Internal reference voltage for switched capacitor filter section.
4	R_x PD	Output	Three state voltage output of the R_x Phase Detector. This pin is either "high", "low", or "high impedance" depending on the phase difference of the phase detector input signals. During lock, very narrow pulses with a frequency equal to the reference frequency are present. This pin drives the external R_x PLL loop filter. It is important to minimize the line length and parasitic capacitance of this pin.
5	PLL V_{ref}	–	PLL voltage regulator output pin. An internal voltage regulator provides a stable power supply voltage for the R_x and T_x PLL's and can also be used as a regulated supply voltage for other IC's.
6	T_x PD	Output	Three state voltage output of the T_x Phase Detector. This pin is either "high", "low", or "high impedance" depending on the phase difference of the phase detector input signals. During lock, very narrow pulses with a frequency equal to the reference frequency are present. This pin drives the external T_x PLL loop filter. It is important to minimize the line length and parasitic capacitance of this pin.
7	Gnd PLL	Gnd	Ground pin for PLL section of IC.
8	T_x VCO	Input	Transmit divide counter input which is driven by an ac–coupled external transmit loop VCO. The minimum signal level is 200 mVpp @ 60.0 MHz. This pin also functions as the test mode input for the counter tests.
9 10 11	Data EN Clk	Input	Microprocessor serial interface input pins for programming various counters and control functions.
12	Clk Out	Output	Microprocessor Clock Output which is derived from the 2nd LO crystal oscillator and a programmable divider. It can be used to drive a microprocessor and thereby reduce the number of crystals required in the system design. The driver has an internal resistor in series with the output which can be combined with an external capacitor to form a low pass filter to reduce radiated noise on the PCB. This output also functions as the output for the counter test modes.
13	CD Out	I/O	Dual function pin; 1) Carrier detect output (open collector with external 100 kΩ pull–up resistor. 2) Hardware interrupt input which can be used to "wake–up" from Inactive Mode.
14	BD_1 Out	Output	Low battery detect output #1 (open collector with external pull–up resistor).
15	DA Out	Output	Data amplifier output (open collector with internal 100 kΩ pull–up resistor).
16	BD_2 Out	Output	Low battery detect output #2 (open collector with external pull–up resistor).
17	T_x Out	Output	T_x path audio output.
18	C Cap	–	Compressor rectifier filter capacitor pin. Pull pin high through a capacitor.
19	C In	Input	Compressor input (ac–coupled).
20	Amp Out	Output	Microphone amplifier output.
21	T_x In	Input	T_x path input to microphone amplifier (Mic Amp) (ac–coupled).
22	DA In	Input	Data amplifier input (ac–coupled).
23	V_{CC} Audio	Supply	V_{CC} supply for audio section.
24	R_x Audio In	Input	R_x audio input (ac–coupled).
25	Det Out	Output	Audio output from FM detector.
26	RSSI	Output	Receive Signal Strength Indicator filter capacitor.
27 28	Q Coil Lim Out	–	A quad coil or ceramic discriminator connected to these pins as part of the FM demodulator circuit.
29	V_{CC} RF	Supply	V_{CC} supply for RF receiver section.
30 31	Lim C_2 Lim C_1	–	IF amplifier/limiter capacitor pins.
32	Lim In	Input	Signal input for IF amplifier/limiter.

PIN FUNCTION DESCRIPTION (continued)

Pin	Symbol	Type	Description
33	SGND RF	Gnd	Ground pin for RF section of the IC.
34	Mix_2 In	Input	Second mixer input.
35	Mix_2 Out	Output	Second mixer output.
36	Gnd RF	Gnd	Ground pin for RF section of the IC.
37	Mix_1 Out	Output	First mixer output.
38	Mix_1 In_2	Input	Negative phase first mixer input.
39	Mix_1 In_1	Input	Positive phase first mixer input.
40 41	LO_1 In LO_1 Out	–	Tank Elements for 1st LO Multivibrator Oscillator are connected to these pins.
42	V_{cap} Ctrl	–	1st LO Varactor Control Pin.
43	Gnd Audio	Gnd	Ground for audio section of the IC.
44	SA Out	Output	Speaker amplifier output.
45	SA In	Input	Speaker amplifier input (ac–coupled).
46	E Out	Output	Expandor output.
47	E_{cap}	–	Expandor rectifier filter capacitor pin. Pull pin high through a capacitor.
48	E In	Input	Expandor Input.
49	Scr Out	Output	R_x Scrambler Output.
50	Ref_2	–	Reference voltage input for Low Battery Detect #2.
51	Ref_1	–	Reference voltage input for Low Battery Detect #1.
52	V_B	–	Internal half supply analog ground reference.

FM Receiver

The FM receiver can be used with either a quad coil or a ceramic resonator. The FM receiver and 1st LO have been designed to work for all country channels, including 25 channel U.S., without the need for any external switching circuitry (see Figure 29).

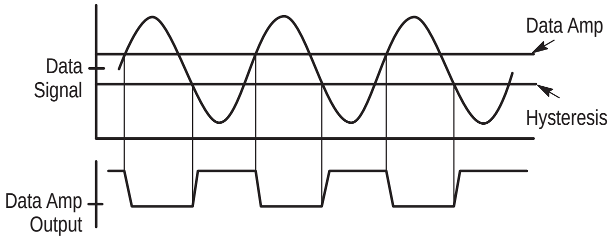
RSSI/Carrier Detect

Connect 0.01 µF to Gnd from “RSSI” output pin to form the carrier detect filter. “CD Out” is an open collector output which requires an external 100 kΩ pull–up resistor to V_{CC}. The carrier detect threshold is programmable through the MPU interface.

Data Amp Comparator

The data amp comparator is an inverting hysteresis comparator. Its open collector output has an internal 100 kΩ pull–up resistor. A band pass filter is connected between the “Det Out” pin and the “DA In” pin with component values as shown in Figure 1 (Test Circuit). The “DA In” input signal is ac–coupled.

Figure 2. Data Amp Operation



Expandor/ Compressor

In Appendix B, the EIA/CCITT recommendations for measurement of the attack and decay times are defined. The curves in Figures 3 and 4 show the typical expandor and compressor output versus input responses.

Figure 3. Expandor Typical Response

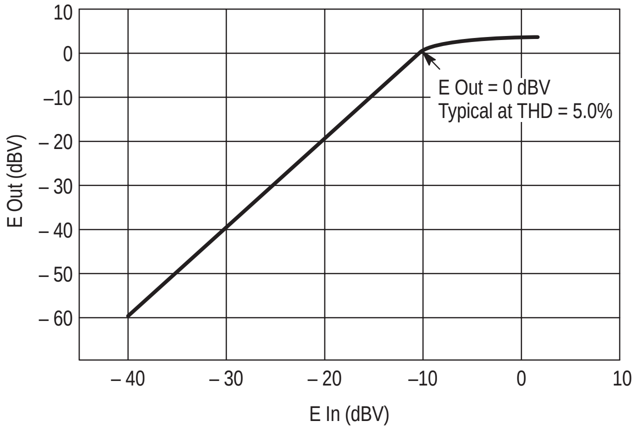
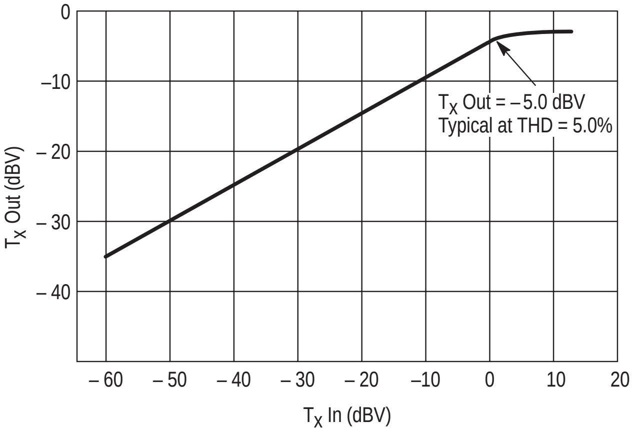


Figure 4. Compressor Typical Response



R_X Audio Path (LPF/R_X Gain Adjust/ R_X Mute/Expandor/Volume Control)

The R_X Audio signal path goes from “R_X Audio In” (Pin 24) to “E Out” (Pin 46). The “R_X Audio In” input signal is ac coupled. AC couple between “Scr Out” and “E In” (see Figure 3).

Speaker Amp/SP Mute

The Speaker Amp is an inverting rail–to–rail operational amplifier. The noninverting input is connected to the internal V_B reference. External resistors and capacitors are used to set the gain and frequency response. The “SA In” Input is ac coupled.

Mic Amp

The Mic Amp is an inverting rail–to–rail operational amplifier with noninverting input terminal connected to internal V_B reference. External resistors and capacitors are set to the gain and frequency response. The “T_X In” input is ac coupled.

T_X Audio Path (Compressor/ALC/T_X Mute/ Limiter/LPF/T_X Gain Adjust)

The T_X Audio signal path goes from “C In” (Pin 19) to “T_X Out” (Pin 17). The “C In” input signal is ac coupled. The ALC (Automatic Level Control) provides a “soft” limit to the output signal swing as the input voltage increases slowly (i.e., a sine wave is maintained). The Limiter circuit limits rapidly changing signal levels by clipping the signal peaks. The ALC and/or Limiter can be disabled through the MPU serial interface (see Figure 4).

T_X and R_X Scrambler

The T_X and R_X signal paths each contain a frequency inversion scrambler in the MC13110. Each scrambler contains a pre–mixer low pass switched capacitor filter (SCF), a double balanced mixer and a post–mixer low pass switched capacitor filter. The scrambler function can be defeated by setting the T_X or R_X Scrambler Bypass bits in the control register to “1” through the MPU interface. In this mode, the mixer and the post–mixer LPF are bypassed and only the pre–mixer LPF remains in the signal path. The SCF corner frequencies are proportional to the SCF clock. The SCF Clock Divider is programmable through the MPU interface, (SCF Clock) = F(2nd LO)/(SCF Divider Value*2). The scrambler modulation frequency is (SCF Clock)/40. Four scrambler modulation frequencies may be selected (see Figures 28 and 29).

PLL Voltage Regulator

The “PLL V_{ref}” pin is the internal supply voltage for the R_X and T_X PLL’s. It is regulated to a nominal 2.5 V. The “V_{CC} Audio” pin is the supply voltage for the internal voltage regulator. Two capacitors with 10 μF and 0.1 μF values must be connected to the “PLL V_{ref}” pin to filter and stabilize this regulated voltage. The “PLL V_{ref}” pin may be used to power other IC’s as long as the total external load current does not exceed 1.0 mA. The tolerance of the regulated voltage is initially ±8.0%, but is improved to ±4.0% after the internal Bandgap voltage reference is adjusted electronically through the MPU serial interface. The voltage regulator is turned off in the Standby and Inactive modes to reduce current drain. In these modes, the “PLL V_{ref}” pin is internally connected to the “V_{CC} Audio” pin (i.e., the power supply voltage is maintained but is now unregulated).

Low Battery Detect

Two external precision resistor dividers are used to set independent thresholds for two battery detect hysteresis comparators. The voltages on “Ref_1” and “Ref_2” are compared to an internally generated 1.5 V reference voltage. The tolerance of the internal reference voltage is initially ±6.0%. The Low Battery Detect threshold tolerance can be improved by adjusting a trim–pot in the external resistor divider. Alternately, the tolerance of the internal reference voltage can be improved to ±1.5% through MPU serial interface programming. The internal reference can be measured directly at the “V_B” pin. During final test of the telephone, the V_B internal reference voltage is measured. Then, the internal reference voltage value is adjusted electronically through the MPU serial interface to achieve the desired accuracy level. The voltage reference register value should be stored in ROM during final test so that it can be reloaded each time the MC13110 IC is powered up. Low Battery Detect outputs are open collector.

Power Supply Voltage

This circuit is used in a cordless telephone handset and base unit. The handset is battery powered and can operate on three NiCad cells or on 5.0 V supply.

PLL Frequency Synthesizer General Description

Figure 5 shows a simplified block diagram of the programmable universal dual phase locked loop (PLL). This dual PLL is fully programmable through the MCU serial interface and supports most country channel frequencies including USA (25 ch), Spain, Australia, Korea, New Zealand, U. K., Netherlands, France, and China.

The 2nd local oscillator and reference divider provide the reference frequency for the receive (R_X) and transmit (T_X) PLL loops. The programmed divider value for the reference divider is selected based on the crystal frequency and the desired R_X and T_X reference frequency values. Additional divide by 25 and divide by 4 blocks are provided to allow for generation of the 1.0 kHz and 6.25 kHz reference frequencies required for the U. K. The 14–bit T_X counter is programmed for the desired transmit channel frequency. The 14–bit R_X counter is programmed for the desired first local oscillator frequency. All counters power up in the proper default state for USA channel #21 (channel #6 for FCC 10 channel band) and for a 10.24 MHz reference frequency crystal. Internal fixed capacitors can be connected to the tank circuit of the 1st LO through microprocessor control to extend the sensitivity of the 1st LO for U.S. 25 channel operation.

PLL I/O Pin Specifications

The 2nd LO, R_X and T_X PLL’s, and MPU serial interface are powered by the internal voltage regulator at the “PLL V_{ref}” pin. The “PLL V_{ref}” pin is the output of a voltage regulator which is powered from the “V_{CC} Audio” power supply pin and is regulated by an internal bandgap voltage reference. Therefore, the maximum input and output levels for most PLL I/O pins (LO_2 In, LO_2 Out, R_X PD, T_X PD, T_X VCO) is the regulated voltage at the “PLL V_{ref}” pin. The ESD protection diodes on these pins are also connected to “PLL V_{ref}”. Internal level shift buffers are provided for the pins (Data, Clk, EN, Clk Out) which connect directly to the microprocessor. The maximum input and output levels for these pins is V_{CC}. Figure 6 shows a simplified schematic of the I/O pins.

Figure 5. Dual PLL Simplified Block Diagram

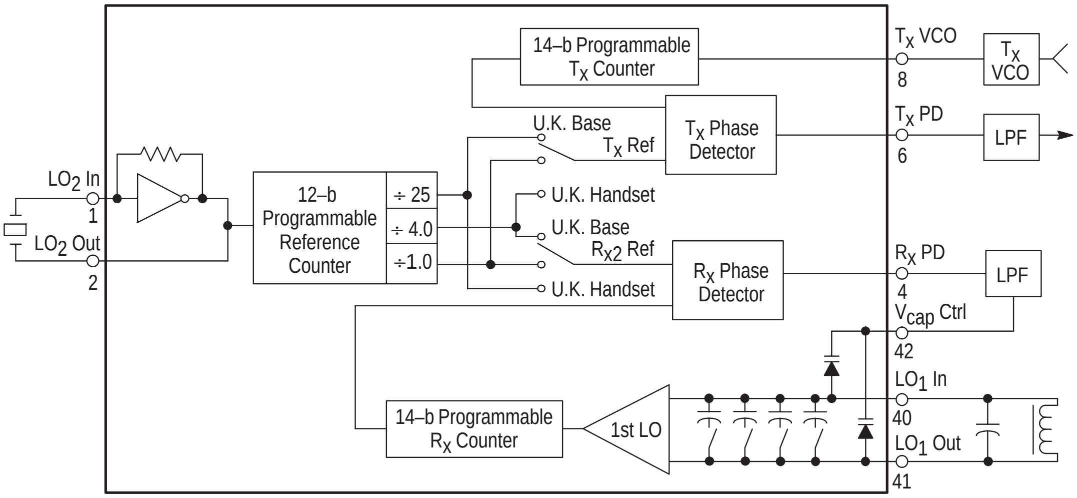
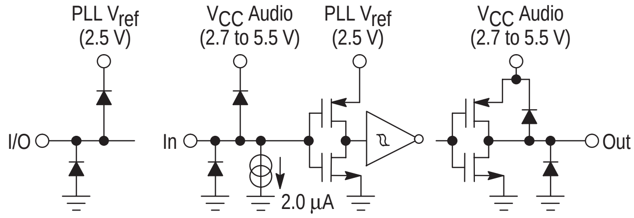


Figure 6. PLL I/O Pin Simplified Schematics



LO_2 In, LO_2 Out, R_X PD, T_X PD and T_X VCO Pins

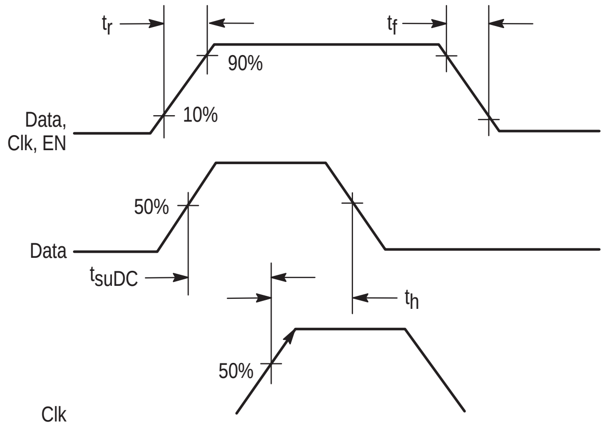
Data, Clk and EN Pins

Clk Out Pin

Microprocessor Serial Interface

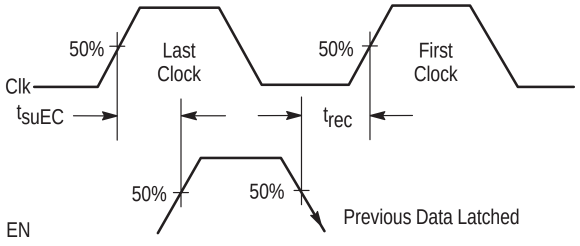
The “Data”, “Clk”, and “EN” pins provide an MPU serial interface for programming the reference counters, the transmit and receive channel divider counters, the switched capacitor filter clock counter, and various control functions. The “Data” and “Clk” pins are used to load data into the shift register. Figure 7 shows the timing required on the “Data” and “Clk” pins. Data is clocked into the shift register on positive clock transitions.

Figure 7. Data and Clock Timing Requirement



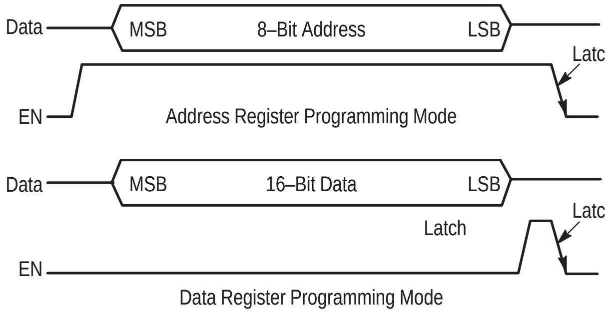
After data is loaded into the shift register, the data is latched into the appropriate latch register using the “EN” pin. This is done in two steps. First, an 8–bit address is loaded into the shift register and latched into the 8–bit address latch register. Then, up to 16–bits of data is loaded into the shift register and latched into the data latch register specified by the address that was previously loaded. Figure 5 shows the timing required on the EN pin. Latching occurs on the negative EN transition.

Figure 8. Enable Timing Requirement



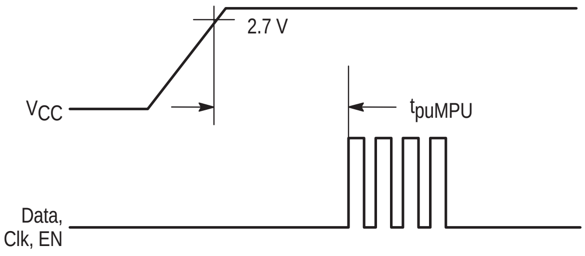
The state of the EN pin when clocking data into the shift register determines whether the data is latched into the address register or a data register. Figure 9 shows the address and data programming diagrams. In the data programming mode, there must not be any clock transitions when “EN” is high. The clock can be in a high state (default high) or a low state (default low) but must not have any transitions during the “EN” high state. The convention in these figures is that latch bits to the left are loaded into the shift register first.

Figure 9. Microprocessor Interface Programming Mode Diagrams



The MPU serial interface is fully operational within 100 µs after the power supply has reached its minimum level during power–up (see Figure 10). The MPU Interface shift registers and data latches are operational in all four power saving modes; Inactive, Standby, R_X, and Active Modes. Data can be loaded into the shift registers and latched into the latch registers in any of the operating modes.

Figure 10. Microprocessor Serial Interface Power–Up Delay



Data Registers

Figure 11 shows shows the data latch registers and addresses which are used to select each of these registers. Latch bits to the left (MSB) are loaded into the shift register first. The LSB bit must always be the last bit loaded into the shift register. Bits preceeding the register must be “0’s” as shown in Figure 11.

Figure 11. Microprocessor Interface Data Latch Registers

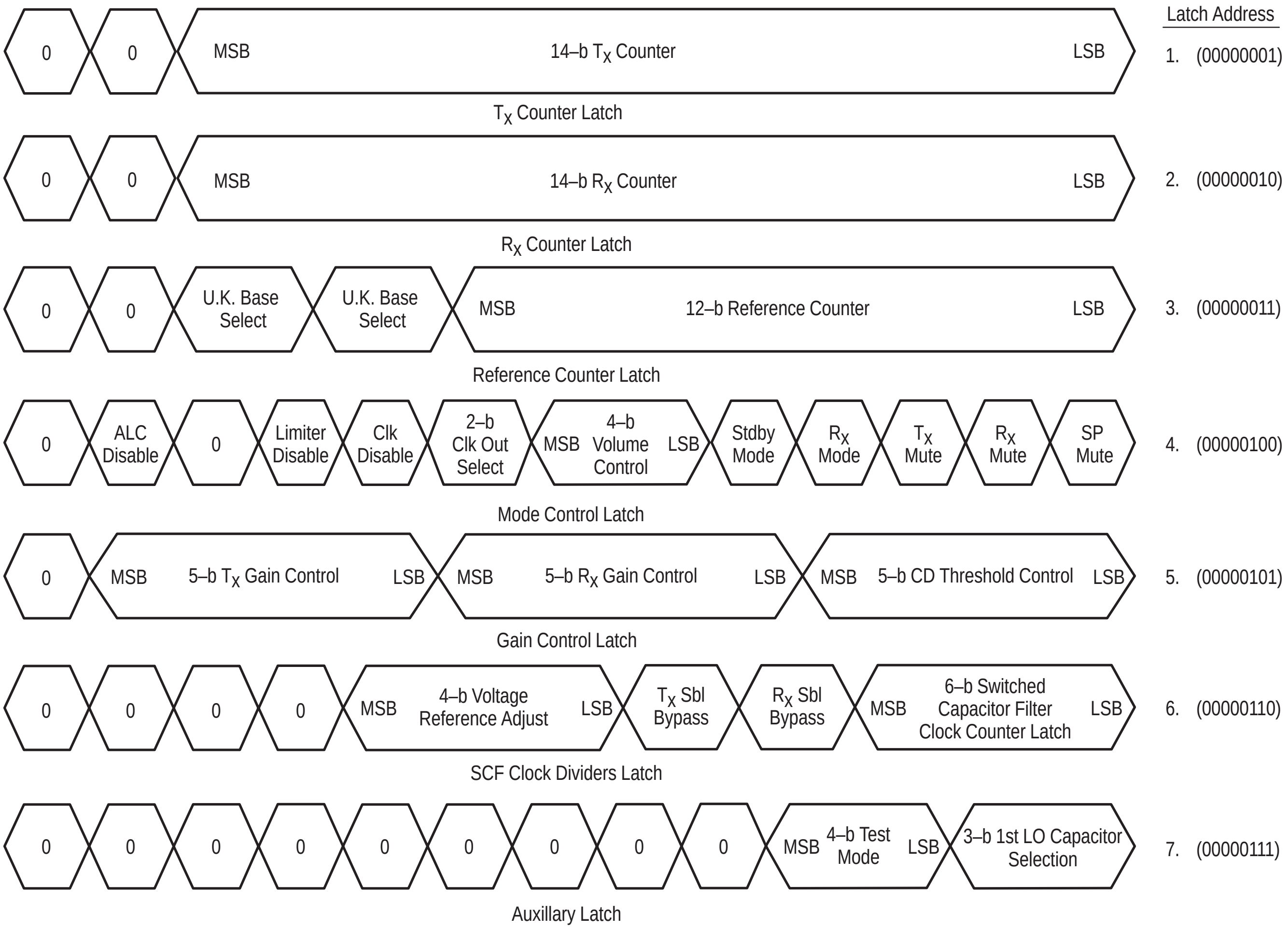


Figure 12. Reference Frequency and Reference Divider Values

Crystal Frequency	Reference Divider Value	U.K. Base/ Handset Divider	Reference Frequency	SC Filter Clock Divider	SC Filter Clock Frequency	Scrambler Modulation Divider	Scrambler Modulation Frequency
10.24 MHz	2048	1.0	5.0 kHz	31	165.16 kHz	40	4.129 kHz
10.24 MHz	1024	4.0	2.5 kHz	31	165.16 kHz	40	4.129 kHz
11.15 MHz	2230	1.0	5.0 kHz	34	163.97 kHz	40	4.099 kHz
12.00 MHz	2400	1.0	5.0 kHz	36	166.67 kHz	40	4.167 kHz
11.15 MHz	1784	1.0	6.25 kHz	34	163.97 kHz	40	4.099 kHz
11.15 MHz	446	4.0	6.25 kHz	34	163.97 kHz	40	4.099 kHz
11.15 MHz	446	25	1.0 kHz	34	163.97 kHz	40	4.099 kHz

Reference Frequency Selection

The “LO_2 In” and “LO_2 Out” pins form a reference oscillator when connected to an external parallel–resonant crystal. The reference oscillator is also the second local oscillator for the RF Receiver. Figure 12 shows the relationship between different crystal frequencies and reference frequencies for cordless phone applications in various countries. “LO_2 In” may also serve as an input for an externally generated reference signal which is ac–coupled. The switched capacitor filter 6–bit programmable counter must be programmed for the crystal frequency that is selected since this clock is derived from the crystal frequency and must be held constant regardless of the crystal that is selected. The actual switched capacitor clock divider ratio is twice the programmed divider ratio since there is a fixed divide by 2.0 after the programmable counter. The scrambler mixer modulation frequency is the switched capacitor clock divided by 40.

Reference Counter

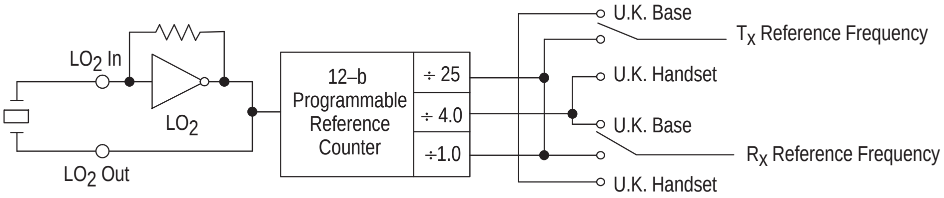
Figure 13 shows how the reference frequencies for the R_X and T_X loops are generated. All countries except the U.K.

require that the T_X and R_X reference frequencies be identical. In this case, set “U.K. Base Select” and “U.K. Handset Select” bits to “0”. Then the fixed divider is set to “1” and the T_X and R_X reference frequencies will be equal to the crystal oscillator frequency divided by the programmable reference counter value. The U.K. is a special case which requires a different reference frequency value for T_X and R_X. For U.K. base operation, set “U.K. Base Select” to “1”. For U.K. handset operation, set “U.K. Handset Select” to “1”.The Netherlands is also a special case since a 2.5 kHz reference frequency is used for both the T_X and R_X reference and the total divider value required is 4096 which is larger than the maximum divide value available from the 12–bit reference divider (4095). In this case, set “U.K. Base Select” to “1” and set “U.K. Handset Select” to “1”. This will give a fixed divide by 4 for both the T_X and R_X reference. Then set the reference divider to 1024 to get a total divider of 4096.

Mode Control Register

Power saving modes, mutes, disables, volume control, and microprocessor clock output frequency are all set by the Mode Control Register. Operation of the Mode Control Register is explained in Figures 14 through 21.

Figure 13. Reference Register Programming Mode



U.K. Handset Select	U.K. Base Select	T_X Divider Value	R_X Divider Value	Application
0	0	1.0	1.0	All but U.K. and Netherlands
0	1	25	4.0	U.K. Base Set
1	0	4.0	25	U.K. Hand Set
1	1	4.0	4.0	Netherlands Base and Hand Set

14–Bit Reference Counter Latch

Figure 14. Mode Control Register Bits

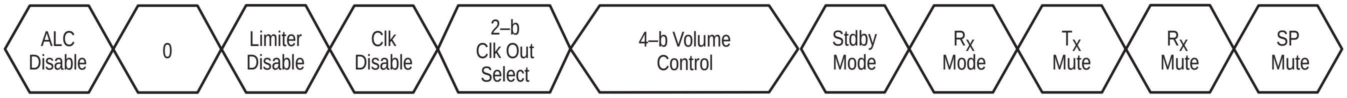


Figure 15. Mute and Disable Control Bit Descriptions

ALC Disable	1 0	Automatic Level Control Disabled Normal Operation
Limiter Disable	1 0	Limiter Disabled Normal Operation
Clock Disable	1 0	MPU Clock Output Disabled Normal Operation
T_X Mute	1 0	Transmit Channel Muted Normal Operation
R_X Mute	1 0	Receive Channel Muted Normal Operation
SP Mute	1 0	Speaker Amp Muted Normal Operation

Power Saving Operating Modes

When the MC13110 is used in a handset, it is important to conserve power in order to prolong battery life. There are five modes of operation; Active, R_X, Standby, Interrupt, and Inactive. In Active mode, all circuit blocks are powered. In R_X mode, all circuitry is powered down except for those circuit sections needed to receive a transmission from the base. In the Standby and Interrupt Modes, all circuitry is powered down except for the circuitry needed to provide the clock output for the microprocessor. In Inactive Mode, all circuitry is powered down except the MPU interface. Latch memory is maintained in all modes. Figure 16 shows the control register bit values for selection of each power saving mode and Figure 17 shows the circuit blocks which are powered in each of these operating modes.

Figure 16. Power Saving Mode Selection

Stdby Mode Bit	R_X Mode Bit	“CD Out/ Hardware Interrupt” Pin	Mode
0	0	X	Active
0	1	X	R_X
1	0	X	Standby
1	1	1 or High Impedance	Inactive
1	1	0	Interrupt

Figure 17. Power Saving Modes

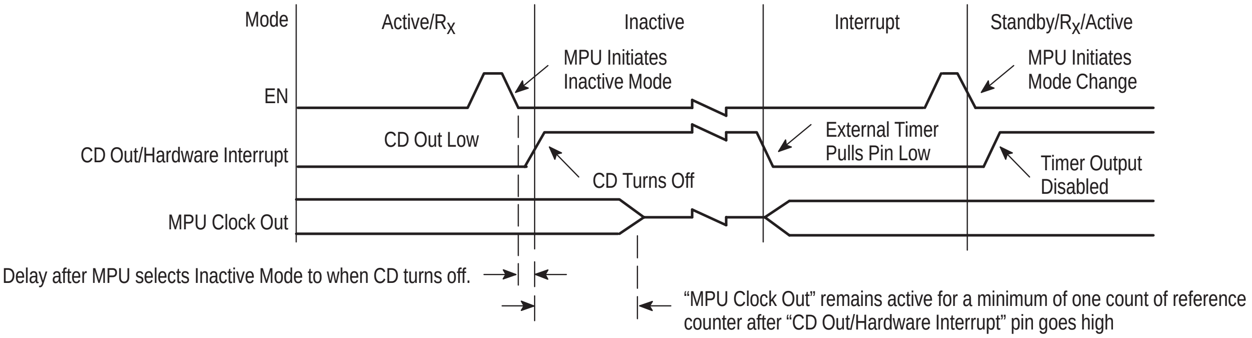
Circuit Blocks	Active	R_X	Standby	Inactive
“PLL V_{ref}” Regulated Voltage	X	X	X[1]	X[1]
MPU Interface	X	X	X	X
2nd LO Oscillator	X	X	X	
MPU Clock Output	X	X	X	
RF Receiver and 1st LO VCO	X	X		
R_X PLL	X	X		
Carrier Detect	X	X		
Data Amp	X	X		
Low Battery Detect	X	X		
T_X PLL	X			
R_X and T_X Audio Paths	X			

NOTE: In Standby and Inactive Modes, “PLL V_{ref}” remains powered but is not regulated. It will fluctuate with V_{CC}.

Inactive Mode Operation and Hardware Interrupt

In some handset applications it may be desirable to power down all circuitry including the microprocessor (MPU). First put the combo IC into the Inactive mode, which turns off the MPU Clock Output (see Figure 18), and then disable the microprocessor. In order to give the MPU adequate time to power down, the MPU Clock output remains active for a minimum of one reference counter cycle (about 200 µs) after the command is given to switch into the “Inactive” mode. An external timing circuit should be used to initiate the turn–on sequence. The “CD Out” pin has a dual function. In the Active and R_X modes it performs the carrier detect function. In the Standby and Inactive modes the carrier detect circuit is disabled and the “CD Out” pin is in a “High” state due to the external pull–up resistor. In the Inactive mode, the “CD Out” pin is the input for the hardware interrupt function. When the “CD Out” pin is pulled “low” by the external timing circuit, the combo IC switches from the Inactive to the Interrupt mode thereby turning on the MPU Clock Output. The MPU can then resume control of the combo IC. The “CD Out” pin must remain low until the MPU changes the operating mode from Interrupt to Standby, Active or R_X modes.

Figure 18. Hardware Interrupt Operation



MPU "Clk Out" Divider Programming

This pin is a clock output which is derived from the crystal oscillator (2nd local oscillator). It can be used to drive a microprocessor and thereby reduce the number of crystals required. Figure 19 shows the relationship between the crystal frequency and the clock output for different divider values. Figure 20 shows the "Clk Out" register bit values.

Figure 19. Clock Output Values

Crystal Frequency	Clock Output Divider			
	2	3	4	5
10.24 MHz	5.120 MHz	3.413 MHz	2.560 MHz	2.048 MHz
11.15 MHz	5.575 MHz	3.717 MHz	2.788 MHz	2.230 MHz
12.00 MHz	6.000 MHz	4.000 MHz	3.000 MHz	2.400 MHz

MPU "Clk Out" Radiated Noise on Circuit Board

The clock line running between the MC13110 and the microprocessor has the potential to radiate noise which can cause problems in the system especially if the clock is a square wave digital signal with large high frequency harmonics. In order to minimize radiated noise, a 1.0 kΩ resistor is included on–chip in series with the "Clk Out" output driver. A small capacitor can be connected to the "Clk Out" line on the PCB to form a single pole low pass filter. This filter will significantly reduce noise radiated from the "Clk Out" line.

Volume Control Programming

The volume control adjustable gain block can be programmed in 2.0 dB gain steps from –14 dB to +16 dB. The power–up default value is 0 dB. (See Figure 21.)

Figure 20. Clock Output Divider

Clk Out Bit #1	Clk Out Bit #0	Clk Out Divider Value
0	0	2
0	1	3
1	0	4
1	1	5

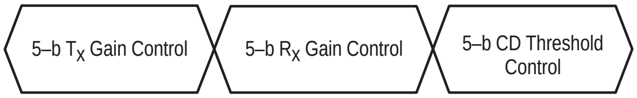
Figure 21. Volume Control

Volume Control Bit #3	Volume Control Bit #2	Volume Control Bit #1	Volume Control Bit #0	Volume Control #	Gain/Attenuation Amount
0	0	0	0	0	–14 dB
0	0	0	1	1	–12 dB
0	0	1	0	2	–10 dB
0	0	1	1	3	–8.0 dB
0	1	0	0	4	–6.0 dB
0	1	0	1	5	–4.0 dB
0	1	1	0	6	–2.0 dB
0	1	1	1	7	0 dB
1	0	0	0	8	2.0 dB
1	0	0	1	9	4.0 dB
1	0	1	0	10	6.0 dB
1	0	1	1	11	8.0 dB
1	1	0	0	12	10 dB
1	1	0	1	13	12 dB
1	1	1	0	14	14 dB
1	1	1	1	15	16 dB

Gain Control Register

The gain control register contains bits which control the T_X Voltage Gain, R_X Voltage Gain, and Carrier Detect threshold. Operation of these latch bits are explained in Figures 22, 23 and 24.

Figure 22. Gain Control Latch Bits



T_X and R_X Gain Programming

The T_X and R_X audio signal paths each have a programmable gain block. If a T_X or R_X voltage gain other than the nominal power–up default is desired, it can be programmed through the MPU interface. Alternately, these programmable gain blocks can be used during final test of the telephone to electronically adjust for gain tolerances in the telephone system as shown in Figure 23. In this case, the T_X and R_X gain register values should be stored in ROM during final test so that they can be reloaded each time the combo IC is powered up.

Figure 23. T_X and R_X Gain Control

Gain Control Bit #4	Gain Control Bit #3	Gain Control Bit #2	Gain Control Bit #1	Gain Control Bit #0	Gain Control #	Gain/Attenuation Amount
0	0	0	0	0	0	–15 dB
0	0	0	0	1	1	–14 dB
0	0	0	1	0	2	–13 dB
0	0	0	1	1	3	–12 dB
0	0	1	0	0	4	–11 dB
0	0	1	0	1	5	–10 dB
0	0	1	1	0	6	–9.0 dB
0	0	1	1	1	7	–8.0 dB
0	1	0	0	0	8	–7.0 dB
0	1	0	0	1	9	–6.0 dB
0	1	0	1	0	10	–5.0 dB
0	1	0	1	1	11	–4.0 dB
0	1	1	0	0	12	–3.0 dB
0	1	1	0	1	13	–2.0 dB
0	1	1	1	0	14	–1.0 dB
0	1	1	1	1	15	0 dB
1	0	0	0	0	16	1.0 dB
1	0	0	0	1	17	2.0 dB
1	0	0	1	0	18	3.0 dB
1	0	0	1	1	19	4.0 dB
1	0	1	0	0	20	5.0 dB
1	0	1	0	1	21	6.0 dB
1	0	1	1	0	22	7.0 dB
1	0	1	1	1	23	8.0 dB
1	1	0	0	0	24	9.0 dB
1	1	0	0	1	25	10 dB
1	1	0	1	0	26	11 dB
1	1	0	1	1	27	12 dB
1	1	1	0	0	28	13 dB
1	1	1	0	1	29	14 dB
1	1	1	1	0	30	15 dB
1	1	1	1	1	31	16 dB

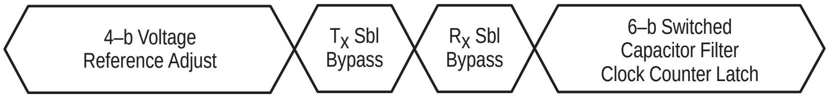
Carrier Detect Threshold Programming

The “CD Out” pin gives an indication to the microprocessor if a carrier signal is present on the selected channel. The nominal value and tolerance of the carrier detect threshold is given in the carrier detect specification section of this document. If a different carrier detect threshold value is desired, it can be programmed through the MPU interface as shown in Figure 24. Alternately, the carrier detect threshold can be electronically adjusted during final test of the telephone to reduce the tolerance of the carrier detect threshold. This is done by measuring the threshold and then by adjusting the threshold through the MPU interface. In this case, it is necessary to store the carrier detect register value in ROM so that the CD register can be reloaded each time the combo IC is powered up.

Figure 24. Carrier Detect Threshold Control

CD Bit #4	CD Bit #3	CD Bit #2	CD Bit #1	CD Bit #0	CD Control #	Carrier Detect Threshold
0	0	0	0	0	0	–20 dB
0	0	0	0	1	1	–19 dB
0	0	0	1	0	2	–18 dB
0	0	0	1	1	3	–17 dB
0	0	1	0	0	4	–16 dB
0	0	1	0	1	5	–15 dB
0	0	1	1	0	6	–14 dB
0	0	1	1	1	7	–13 dB
0	1	0	0	0	8	–12 dB
0	1	0	0	1	9	–11 dB
0	1	0	1	0	10	–10 dB
0	1	0	1	1	11	–9.0 dB
0	1	1	0	0	12	–8.0 dB
0	1	1	0	1	13	–7.0 dB
0	1	1	1	0	14	–6.0 dB
0	1	1	1	1	15	–5.0 dB
1	0	0	0	0	16	–4.0 dB
1	0	0	0	1	17	–3.0 dB
1	0	0	1	0	18	–2.0 dB
1	0	0	1	1	19	–1.0 dB
1	0	1	0	0	20	0 dB
1	0	1	0	1	21	1.0 dB
1	0	1	1	0	22	2.0 dB
1	0	1	1	1	23	3.0 dB
1	1	0	0	0	24	4.0 dB
1	1	0	0	1	25	5.0 dB
1	1	0	1	0	26	6.0 dB
1	1	0	1	1	27	7.0 dB
1	1	1	0	0	28	8.0 dB
1	1	1	0	1	29	9.0 dB
1	1	1	1	0	30	10 dB
1	1	1	1	1	31	11 dB

Figure 25. Switched Capacitor Filter Clock Divider/Voltage Reference Adjust Latch Bits



SCF Clock Divider/Voltage Reference Adjust Register

This register controls the scrambler bypass mode, the divider value for the programmable switched capacitor filter clock divider, and the voltage reference adjust. Operation is explained in Figures 25 through 30.

Figure 26. Bypass Mode Bit Description

T_X Scrambler	1	T_X Scrambler Post–Mixer LPF and Mixer Bypassed
Bypass	0	Normal Operation with T_X Scrambler
R_X Scrambler	1	R_X Scrambler Post–Mixer LPF and Mixer Bypassed
Bypass	0	Normal Operation R_X Scrambler

Switched Capacitor Filter Clock Programming

A block diagram of the switched capacitor filter and scrambler modulation clock dividers is shown in Figure 27. There is a fixed divide by 2 after the programmable divider. The switched capacitor filter clock value is given by the following equation;

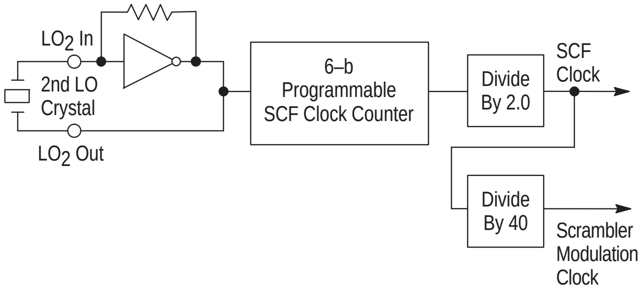
(SCF Clock) = F(2nd LO)/(SCF Divider Value * 2)

The scrambler modulation clock frequency (SMCF) is proportional to the SCF clock and is given by the following equation;

SMCF = (SCF Clock Frequency)/40

The SCF divider should be set to a value which gives a SCF Clock as close to 165.16 kHz as possible based on the 2nd LO frequency which is chosen (see Figure 12).

Figure 27. SCF Clock and Scrambler Carrier Circuit



Scrambler Modulation Frequency Programming

Four different scrambler modulation frequencies may be selected by programming the SCF Clock divider as shown in Figures 28 and 29. Note that all filter corner frequencies will change proportionately with the SCF Clock and Scrambler Modulation Frequency. The power–up default SCF Clock divider value is 31.

Figure 28. Scrambler Modulation Frequency Programming for a 10.240 MHz 2nd LO

SCF Clock Divider	Total Divide Value	SCF Clock Freq. (kHz)	Scrambler Modulation Frequency (Clk/40) (kHz)	Scrambler Lower Corner Frequency (Hz)	Scrambler Upper Corner Frequency (kHz)	R_X Upper (Scrambler Bypassed) Corner Frequency (kHz)	T_X Upper (Scrambler Bypassed) Corner Frequency (kHz)
29	58	176.55	4.414	267.2	3.902	4.147	3.955
30	60	170.67	4.267	258.3	3.772	4.008	3.823
31	62	165.16	4.129	250.0	3.650	3.879	3.700
32	64	160.00	4.000	242.2	3.536	3.758	3.584

NOTE: All filter corner frequencies have a tolerance of ±3%.

Figure 29. Scrambler Modulation Frequency Programming for a 11.15 MHz 2nd LO

SCF Clock Divider	Total Divide Value	SCF Clock Freq. (kHz)	Scrambler Modulation Frequency (Clk/40) (kHz)	Scrambler Lower Corner Frequency (Hz)	Scrambler Upper Corner Frequency (kHz)	R_X Upper (Scrambler Bypassed) Corner Frequency (kHz)	T_X Upper (Scrambler Bypassed) Corner Frequency (kHz)
32	64	174.22	4.355	263.7	3.850	4.092	3.903
33	66	168.94	4.223	255.7	3.733	3.968	3.785
34	68	163.97	4.099	248.2	3.624	3.851	3.673
35	70	159.29	3.982	241.1	3.520	3.741	3.568

NOTE: All filter corner frequencies have a tolerance of ±3%.

Voltage Reference Adjustment

The internal 1.5 V Bandgap voltage reference provides the voltage reference for the “BD1 Out” and “BD2 Out” low battery detect circuits, the “PLL V_{ref}” voltage regulator, the “V_B” reference, and all internal analog ground references. The initial tolerance of the Bandgap voltage reference is ±6%. The tolerance of the internal reference voltage can be improved to ±1.5% through MPU serial interface programming.

During final test of the telephone, the battery detect threshold is measured. Then, the internal reference voltage value is adjusted electronically through the MPU serial interface to achieve the desired accuracy level. The voltage reference register value should be stored in ROM during final test so that it can be reloaded each time the MC13110 is powered up (see Figure 30).

Figure 30. Bandgap Voltage Reference Adjustment

V_{ref} Adj. Bit #3	V_{ref} Adj. Bit #2	V_{ref} Adj. Bit #1	V_{ref} Adj. Bit #0	V_{ref} Adj. #	V_{ref} Adj. Amount
0	0	0	0	0	–9.0%
0	0	0	1	1	–7.8%
0	0	1	0	2	–6.6%
0	0	1	1	3	–5.4%
0	1	0	0	4	–4.2%
0	1	0	1	5	–3.0%
0	1	1	0	6	–1.8%
0	1	1	1	7	–0.6%
1	0	0	0	8	+0.6 %
1	0	0	1	9	+1.8 %
1	0	1	0	10	+3.0 %
1	0	1	1	11	+4.2 %
1	1	0	0	12	+5.4 %
1	1	0	1	13	+6.6 %
1	1	1	0	14	+7.8 %
1	1	1	1	15	+9.0 %

Auxiliary Register

The auxiliary register contains a 3–bit 1st LO Capacitor Selection latch and a 4–bit Test Mode latch. Operation of these latch bits are explained in Figures 31, 32 and 34.

Figure 31. Auxiliary Register Latch Bits

First Local Oscillator Programmable Selection (U.S. Applications)

There is a very large frequency difference between the minimum and maximum channel frequencies in the 25 Channel U.S. Standard.The sensitivity of the 1st LO may not be large enough to accommodate this large frequency variation. Fixed capacitors can be connected across the 1st LO tank circuit to change the 1st LO sensitivity. Internal switches and capacitors are provided to enable microprocessor control over internal fixed capacitor values. Figures 32 and 33 show the schematic representation of the 1st LO and the tank circuit. Figure 34 shows the latch control bit values for microprocessor control.

Figure 32. First Local Oscillator Schematic

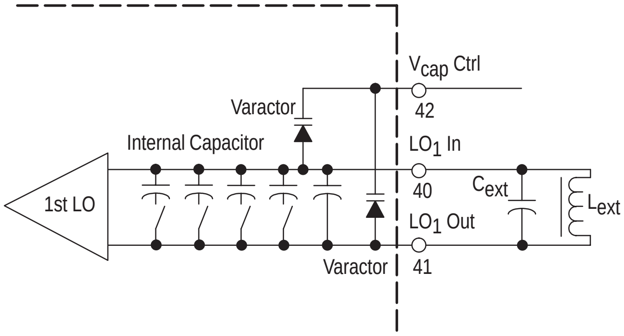


Figure 33. First Local Oscillator Simplified Schematic

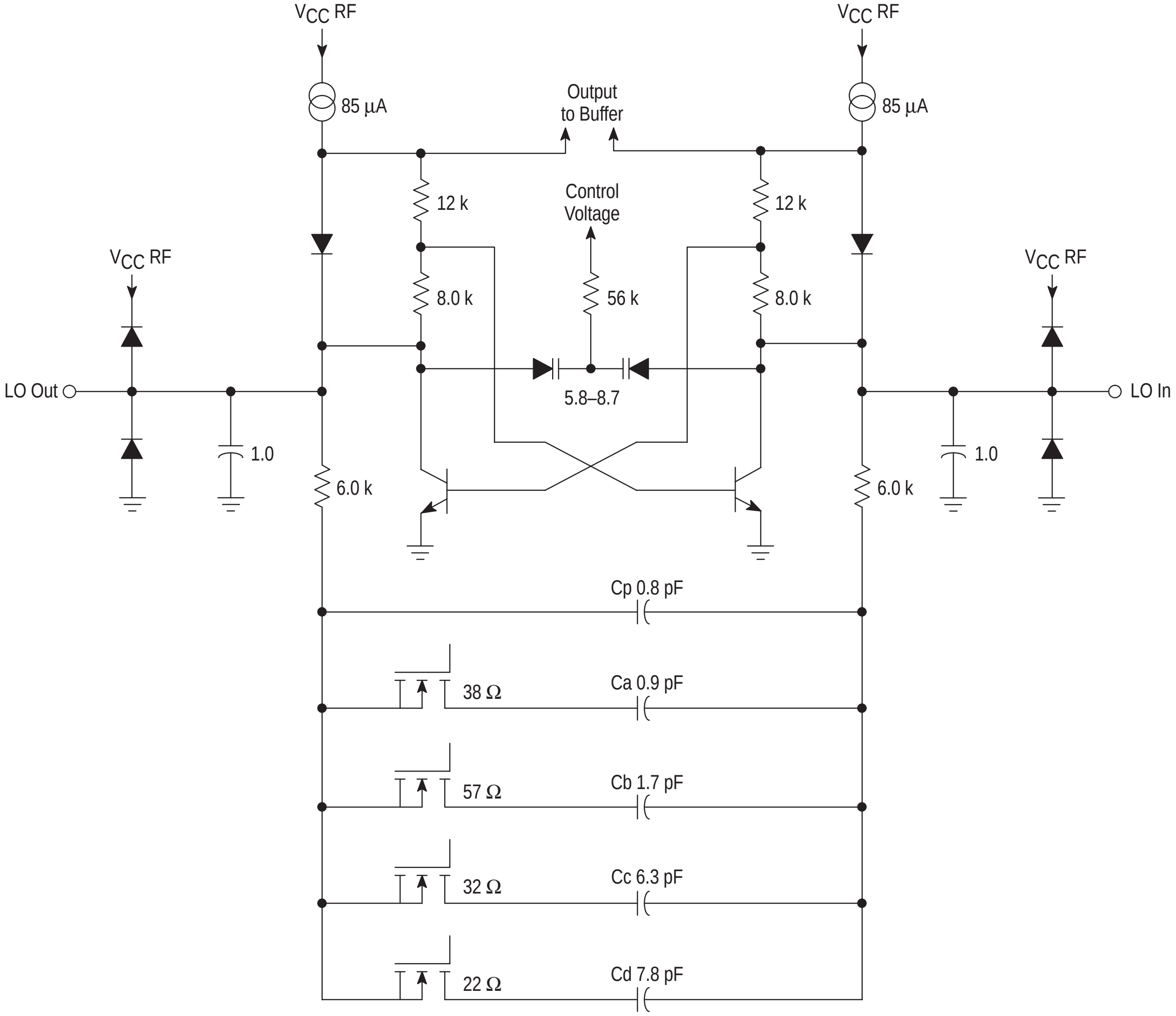


Figure 34. First Local Oscillator Programmable Capacitor Selection for U.S. 25 Channels

1st LO Cap. Bit 2	1st LO Cap. Bit 1	1st LO Cap Bit 0	1st LO Cap. Select	U.S. Base Channels	U.S. Handset Channels	Internal Capacitor Value	Varactor Value over 0.3 to 2.5 V	Equivalent Internal Parallel Resistance at 40 MHz (kΩ)	Equivalent Internal Parallel Resistance at 51 MHz (kΩ)	External Capacitor Value	External Inductor Value
0	0	0	0	1–10	–	0.8 pF	5.8–8.7 pF	>1000	>1000	24 pF	0.47 µH
0	0	0	0	–	1–10	0.8 pF	5.8–8.7 pF	>1000	>1000	33 pF	0.47 µH
0	0	1	1	11–16	–	2.5 pF	5.8–8.7 pF	35	21	24 pF	0.47 µH
0	1	0	2	17–25	–	1.7 pF	5.8–8.7 pF	100	60	24 pF	0.47 µH
0	1	1	3	–	11–16	8.6 pF	5.8–8.7 pF	6.1	3.8	33 pF	0.47 µH
1	0	0	4	–	17–25	7.1 pF	5.8–8.7 pF	8.0	5.0	33 pF	0.47 µH

Figure 35. Digital Test Mode Description

TM #	TM 3	TM 2	TM 1	TM 0	Counter Under Test or Test Mode Option	"T_X V_{CO}" Input Signal	"Clk Out" Output Expected
0	0	0	0	0	Normal Operation	>200 mVpp	–
1	0	0	0	1	R_X Counter, upper 6	0 to 2.5 V	Input Frequency/64
2	0	0	1	0	R_X Counter, lower 8	0 to 2.5 V	See Note Below
3	0	0	1	1	R_X Prescaler	0 to 2.5 V	Input Frequency/4
4	0	1	0	0	T_X Counter, upper 6	0 to 2.5 V	Input Frequency/64
5	0	1	0	1	T_X Counter, lower 8	0 to 2.5 V	See Note Below
6	0	1	1	0	T_X Prescaler	>200 mVpp	Input Frequency/4
7	0	1	1	1	Reference Counter	0 to 2.5 V	Input Frequency/Reference Counter Value
8	1	0	0	0	Divide by 4, 25	0 to 2.5 V	Input Frequency/100
9	1	0	0	1	SC Counter	0 to 2.5 V	Input Frequency/SC Counter Value
10	1	0	1	0	Scrambler Modulation Counter	0 to 2.5 V	Input Frequency/40

NOTE: To determine the correct output, look at the lower 8–bits in the R_X or T_X register (Divisor (7;0). If the value of the divisor is > 16, then the output divisor value is Divisor (7;2) (the upper 6–bits of the divisor). If Divisor (7;0) < 16 and Divisor (3;2) > = 2, then output divisor value is Divisor (3;2) (bits 2 and 3 of the divisor). If Divisor (7;0) < 16 and Divisor (3;2) < 2, then output divisor value is (Divisor (3;2) + 60).

Figure 36. Analog Test Mode Description

TM #	TM 3	TM 2	TM 1	TM 0	Circuit Blocks Under Test	Input Pin	Output Pin
11	1	0	1	1	Compressor	C In	T_X In
12	1	1	0	0	T_X Scrambler	T_X In	T_X Out
13	1	1	0	1	ALC Gain = 10 Option	N/A	N/A
14	1	1	1	0	ALC Gain = 25 Option	N/A	N/A
15	1	1	1	1	Not Used	N/A	N/A

Test Modes

Digital and analog test modes can be selected through the 4–bit Test Mode Register. In digital test mode, the "T_X V_{CO}" input pin is multiplexed to the input of the counter under test and the output of the counter under test is multiplexed to the "Clk Out" output pin so that each counter can be individually tested. Make sure test mode bits are set to "0's" for normal operation. Digital test mode operation is described in Figure 35. During normal operation and when testing the T_X Prescaler, the "T_X VCO" input can be a minimum of 200 mVpp at 80 MHz and should be ac–coupled. For other test modes, input signals should be standard logic levels of 0 to 2.5 V and a maximum frequency of 16 MHz.

The analog test modes enable separate testing of the Compressor and T_X Scrambler blocks as shown in Figure 36. Also, ALC Gain options can be selected through analog test modes.

Power–Up Defaults for Control and Counter Registers

When the IC is first powered up, all latch registers are initialized to a defined state. The device is initially placed in the Rx mode with all mutes active. The reference counter is set to generate a 5.0 kHz reference frequency from a 10.24 MHz crystal. The switched capacitor filter clock counter is set properly for operation with a 10.24 MHz crystal. The scrambler bypass mode control are set for normal operation of scrambler. The T_X and R_X latch registers are set for USA Channel Frequency 21 (Channel 6 for previous FCC 10 Channel Band). Figure 37 shows the initial power–up states for all latch registers.

Figure 37. Latch Register Power–Up Defaults

Register	Count	MSB								LSB							
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
T_X	9966	–	–	1	0	0	1	1	0	1	1	1	0	1	1	1	0
R_X	7215	–	–	0	1	1	1	0	0	0	0	1	0	1	1	1	1
Ref	2048	–	–	0	0	1	0	0	0	0	0	0	0	0	0	0	0
Mode	N/A	–	0	X	0	0	1	1	0	1	1	1	0	1	1	1	1
Gain	N/A	–	0	1	1	1	1	0	1	1	1	1	1	0	1	0	0
SC	31	–	–	–	–	0	1	1	1	0	0	0	1	1	1	1	1
Aux	N/A	–	–	–	–	–	–	–	–	–	0	0	0	0	0	0	0

APPLICATIONS INFORMATION

Evaluation PC Board

The PCB should be double sided with a full ground plane on one side; any leaded components are inserted on the ground plane side. This affords shielding and isolation from the circuit side of the PCB. The other side is the circuit side which has the interconnect traces and the surface mount components. In cases where cost allows, it may be benificial to use multi layer boards.

The placement of certain components specified in the application circuits is very critical. These components should be placed first and the other less critical components are fitted in last. In general, all RF paths should be kept as short as possible, ground pins should be grounded at the pins and V_{CC} pins should have adequate decoupling to ground at the pins. In mixed mode systems where digital and RF/Analog circuitry are present, the V_{EE} and V_{CC} busses are isolated ac–wise from each other.

Component Selection

The evaluation PC board is designed to accommodate specific components, while in some cases it is versatile enough to use components from various manufacturers and coil types. The application circuit schematics specify particular components that were used to achieve the results shown in the typical curves and tables, but alternate components should give similar results.

The MC13110 IC is capable of matching the sensitivity, IMD, adjacent channel rejection, and other performance criteria of a multi–chip analog cordless telephone system. For the most part, the same external components are used as in the multi–chip solution. In the following discussion, various parts of the system are analyzed for best peformance and cost tradeoffs. Specific recommendations are made where certain components or circuit designs offer superior performance. The system analyzed is the USA “CT–1” cordless phone.

Input Matching/Sensitivity

The sensitivity of the IC is typically 0.56 µVrms matched with no preamp. To achieve suitable system performance, a preamp and passive duplexer must be used. In production final test, each section of the IC is separately tested to guarantee its system performance in the specific application. The preamp and duplexer yields typically –114 dBm 12 dB SINAD sensitivity performance under full duplex operation.

The duplexer is important to achieve full duplex operation without significant “de–sensing” of the receiver by the transmitter. The combination of the duplexer and preamp circuit have to attenuate the transmitter power to the receiver by over 60 dB to be effective. They do this while improving the receiver system noise figure and without giving up too much IMD intermodulation performance.

The duplexer may be a single piece unit offered by Shimida and Sansui products (designed for 10 channel CT–1 cordless phone) or a two piece solution offered by Toko (designed for 25 channel operation). The duplexer frequency response at the receiver port has a notch at the transmitter frequency band of about 35 to 40 dB with a 2.0 to 3.0 dB insertion loss at the receiver frequency band.

The preamp circuit utilizes a tuned transformer at the output side of the amplifier; this transformer is designed to bandpass filter the receiver input frequency while rejecting the transmitter frequency. The tuned preamp also improves the noise performance by reducing the bandwidth of the pass band and reducing the second stage contribution of the 1st mixer. The preamp is biased at about 1.0 mA and 3.0 Vdc which yields suitable noise figure and gain.

Mixers

The 1st and 2nd mixers are similar in design. Both are double balanced to suppress the LO and the input frequencies to give only the sum and difference frequencies out. Typically the LO is suppressed about 40 to 60 dB. The 1st mixer may be driven either differentially or single ended. The gain of the 1st mixer has a 3.0 dB corner at 20 MHz and is used at a 10.7 MHz IF. It has an output impedance of 330 Ω and matches to a typical 10.7 MHz ceramic filter with a source and load impedance of 330 Ω. A series resistor may be used to raise the impedance for use with crystal filters which typically have an input impedance much greater than 330 Ω. The 2nd mixer input impedance is typically 3.0 kΩ; it requires an external 360 Ω parallel resistor for use with a standard 330 Ω 10.7 MHz ceramic filter. The second mixer output impedance is 1.5 kΩ making it suitable to match 455 kHz ceramic filters.

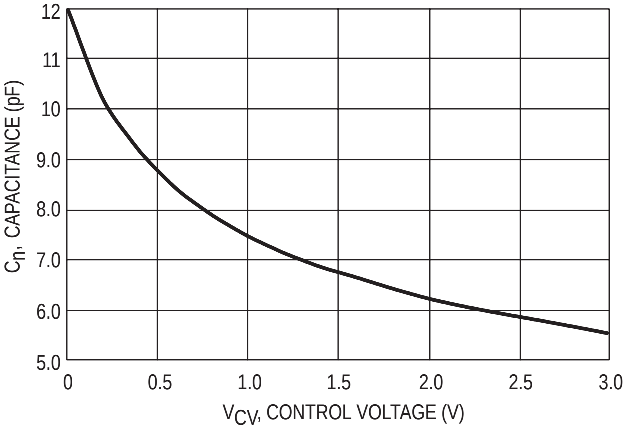
The following table is a list of typical input impedances over frequency for the 1st Mixer. R_P and C_P are represented in parallel form.

Frequency (MHz)	R_P (Ω)	C_P (pF)
20	977.7	2.44
25	944.3	2.60
30	948.8	2.65
35	928	2.55
40	900	2.51
45	873.4	2.65
50	859.3	2.72
55	821	2.72
60	795	2.74

First Local Oscillator

The 1st LO is a multi–vibrator oscillator that takes an external capacitance and inductance. It is voltage controlled to an internal varactor from an external loop filter and an on–board phase–lock loop (PLL). The schematic in Figure 33 shows all the basic parasitic elements of the internal circuitry. The 1st LO internal component values have a tolerance of 15%. A typical dc bias level on the LO Input and LO Output is 0.47 Vdc. The curve in Figure 38 is the varactor control voltage range as it relates to capacitance. It represents the expected capacitance for a given control voltage of the MC13110.

Figure 38. First Local Oscillator Varacter versus Control Voltage



Second Local Oscillator

The 2nd LO is a CMOS oscillator similar to that used in the MC145162. The 2nd LO is also used as the PLL reference oscillator. It is designed to utilize an external parallel resonant crystal.

PLL Design

The 1st LO level is important, as well as the choice of the crystal for the PLL clock reference and 2nd LO. A fundamental, parallel resonant crystal specified with 7.0 to 12 pF load calibration capacitance is recommended. With load calibration capacitance too high, the crystal locks up very slowly. If the LO power is less than –10 dBm, a pull–down resistor at the 1st LO emitter (Pin 41) will increase its drive level. The LO level is primarily a function of the Colpitts capacitive voltage divider formed by the capacitors between the base to emitter and the emitter to ground.

The VCO gain factor expressed in MHz/V is indeed critical to the phase noise performance. If this curve is too steep or too sensitive to changes in control voltage, it may degrade the phase noise performance. The external VCO circuit design needs to consider the typical swing of the control voltage and the corresponding linearity of the transfer function, $\Delta f_{osc}/\Delta V_{control}$. In general, the higher the Q of the VCO circuit inductor, the better phase noise performance.

Adjacent channel rejection and isolation between the 1st and 2nd mixers may be adversely affected due to layout problems and difficulty in getting close to the package pins with the grounds and decoupling capacitors on the RF V_{CC}. These system parameters must be evaluated for sensitivity to layout and external component placement.

Intermodulation and adjacent channel performance problems may also result from spurs around the 1st LO which may be caused by harmonics from the switched capacitor clock driver and too low 1st LO drive level. The clock driver operates at a frequency which is f(2nd LO)/(2 * (SCF Divider)). The harmonics are n * (f(2nd LO)), where n can be any positive integer. The current spikes of the SCF on the supply lines cause the disturbance of the 1st LO. This may be verified by observing the spurs on a spectrum analyzer while changing the clock divider value. The spur frequencies will change when the divider value is changed. The spurious sideband problem may be avoided by changing the clock divider value via software for each channel where it is a problem. Certain channels are worse than others.

The PLL alignment procedure for the application circuit is detailed in Appendix C. Refer to the MC145162 data sheet for PLL design example.

Limiting IF Amplifiers

The limiting IF amplifier typically has about 110 dB of gain; the frequency response starts rolling off at 1.0 MHz. Decoupling capacitors should be placed close to the decoupling Pins 31 and 32 to ensure low noise and stable operation. The IF input impedance is 1.5 kΩ for a suitable match to 455 kHz ceramic filters.

RSSI/Carrier Detect

The Received Signal Strength Indicator (RSSI) indicates the strength of the IF level and the output is proportional to the logarithm of the IF input signal magnitude. The RSSI dynamic range is typically 80 dB. Connect 0.01 µF to GND from “RSSI” output pin to form the carrier detect filter. A resistor needed to convert the RSSI current to voltage is included in the internal circuit. An internal temperature compensated reference current also improves the RSSI accuracy over temperature.

“CD Out” is an open collector output; thus, an external 100 kΩ pull–up resistor to V_{CC} is recommended. The carrier detect threshold is programmable through the MPU interface.

Quadrature Detector

The quadrature detector is coupled to the IF with an external capacitor between Pins 27 and 28; thus, the recovered signal level output is increased for a given bandwidth by increasing the capacitor. The external quadrature component may be either a LCR resonant circuit, which may be adjustable, or a ceramic resonator which is usually fixed tuned.

The bandwidth performance of the detector is controlled by the loaded Q of the LC tank circuit. The following equation defines the components which set the detector circuit’s bandwidth:

$$R_T = Q\,X_L \quad (1)$$

where R_T is the equivalent shunt resistance across the LC Tank. X_L is the reactance of the quadrature inductor at the IF frequency ($X_L = 2\pi fL$).

Specific 455 kHz quadrature LC components are manufactured by Toko in various 5 mm, 7 mm and 10 mm shielded cans in surface mount or leaded packages. Recommended components such as, the 7 mm Toko, is used in the application circuit. When minaturization is a key constraint, a surface mount inductor and capacitor may be chosen to form a resonant LC tank with the PCB and parasitic device capacitance. The 455 kHz IF center frequency is calculated by

(2) $f_c = [2\pi\,(LC_p)^{1/2}]-1$

where L is the parallel tank inductor. C_p is the equivalent parallel capacitance of the parallel resonant tank circuit.

The following is a design example for a detector at 455 kHz and a specific loaded Q. The loaded Q of the quadrature detector is chosen somewhat less than the Q of the IF bandpass. For an IF frequency of 455 kHz and an IF bandpass of 20 kHz, the IF bandpass Q is approximately 23; the loaded Q of the quadrature tank is chosen at 15.

Example:

Let the total external C = 180 pF. Note: the capacitance may be split between a 150 pF chip capacitor and a 5.0 to 25 pF variable capacitor; this allows for tuning to compensate for component tolerance. Since the external capacitance is much greater than the internal device and PCB parasitic capacitance, the parasitic capacitance may be neglected.

Rewrite equation (2) and solve for L:

$L = (0.159)^2/(C\,fc^2)$
L = 678 μH ; Thus, a standard value is chosen:
L = 680 μH (surface mount inductor)

The value of the total damping resistor to obtain the required loaded Q of 15 can be calculated from equation (1):

$R_T = Q(2\pi fL)$
$R_T = 15\,(2\pi)(0.455)(680) = 29.5\ k\Omega$

The internal resistance, R_{int} at the quadrature tank Pin 27 is approximately 100 kΩ and is considered in determining the external resistance, R_{ext} which is calculated from

$R_{ext} = ((R_T)(R_{int}))/(R_{int} - R_T)$
$R_{ext} = 41.8\ k\Omega$; Thus, choose the standard value:
$R_{ext} = 39\ k\Omega$

A ceramic discriminator is recommended for the quadrature circuit in applications where fixed tuning is desired. The ceramic discriminator and a 22 k resistor are placed from Pin 27 to V_{CC}. A 10 pF capacitor is placed from Pin 28 to 27 to properly drive the discriminator.

MuRata Erie has designed a resonator that is compatible with the IC. For US applications the part number is CDBM455C48. For Europe the part number is CDBM450C48. Contact Motorola Analog Marketing for performance data using muRata's parts.

APPENDIX A – APPLICATIONS CIRCUIT

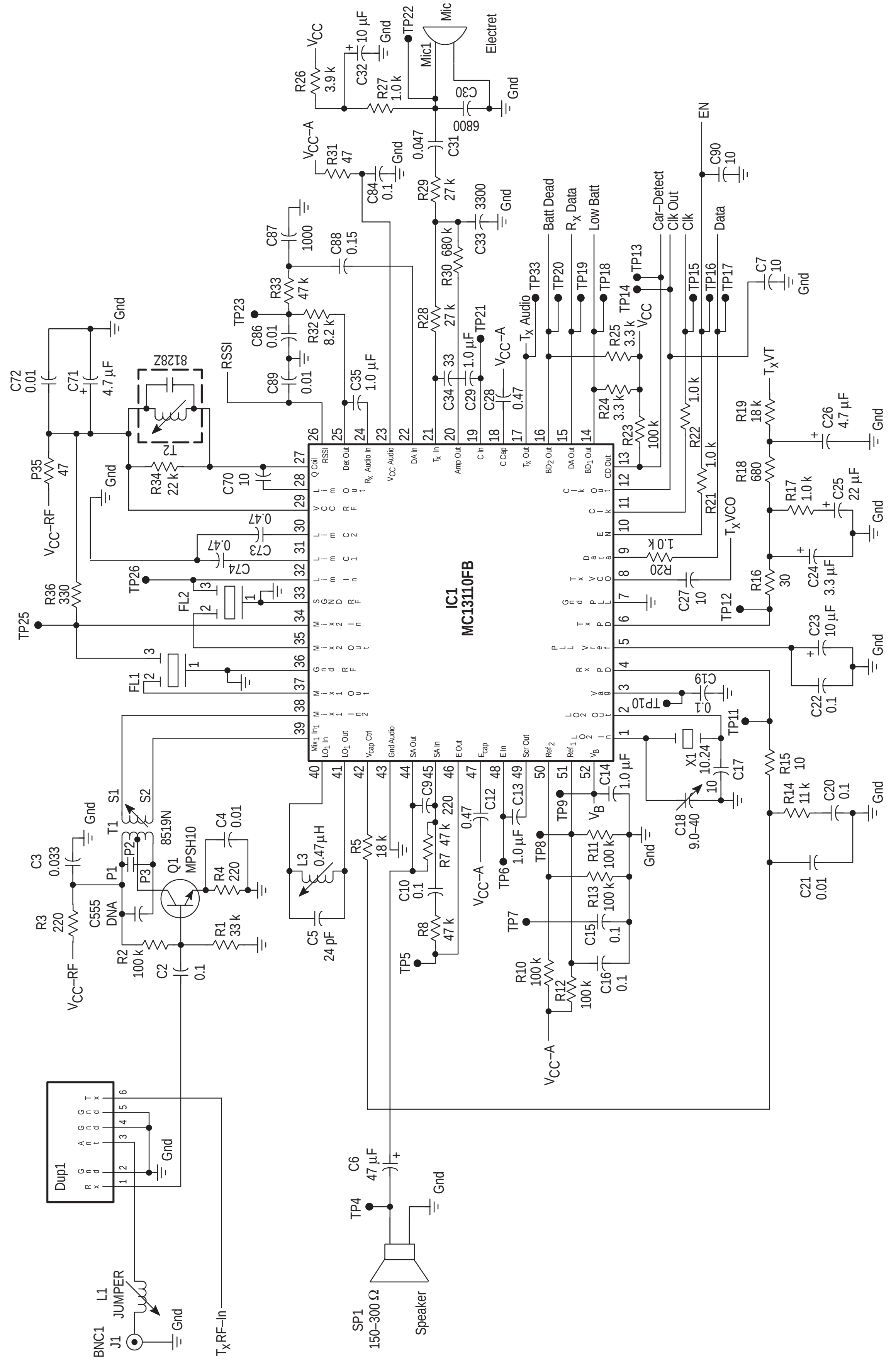
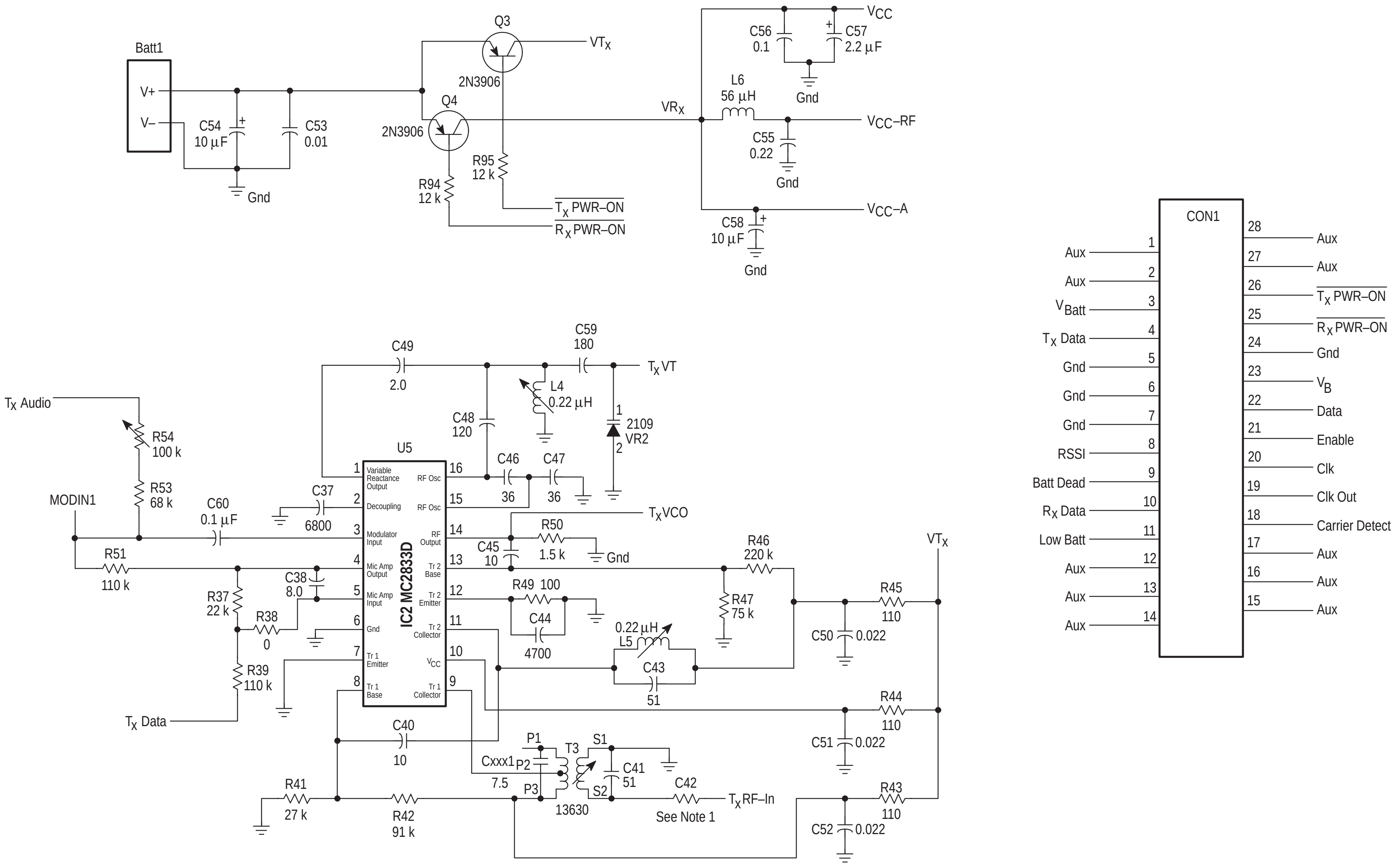


Figure 39a. Baseset RF Applications Circuit

Figure 39a. Baseset RF Applications Circuit (continued)



NOTE 1: C42 = X42 = 51 Ω

Figure 39b. Handset RF Applications Circuit

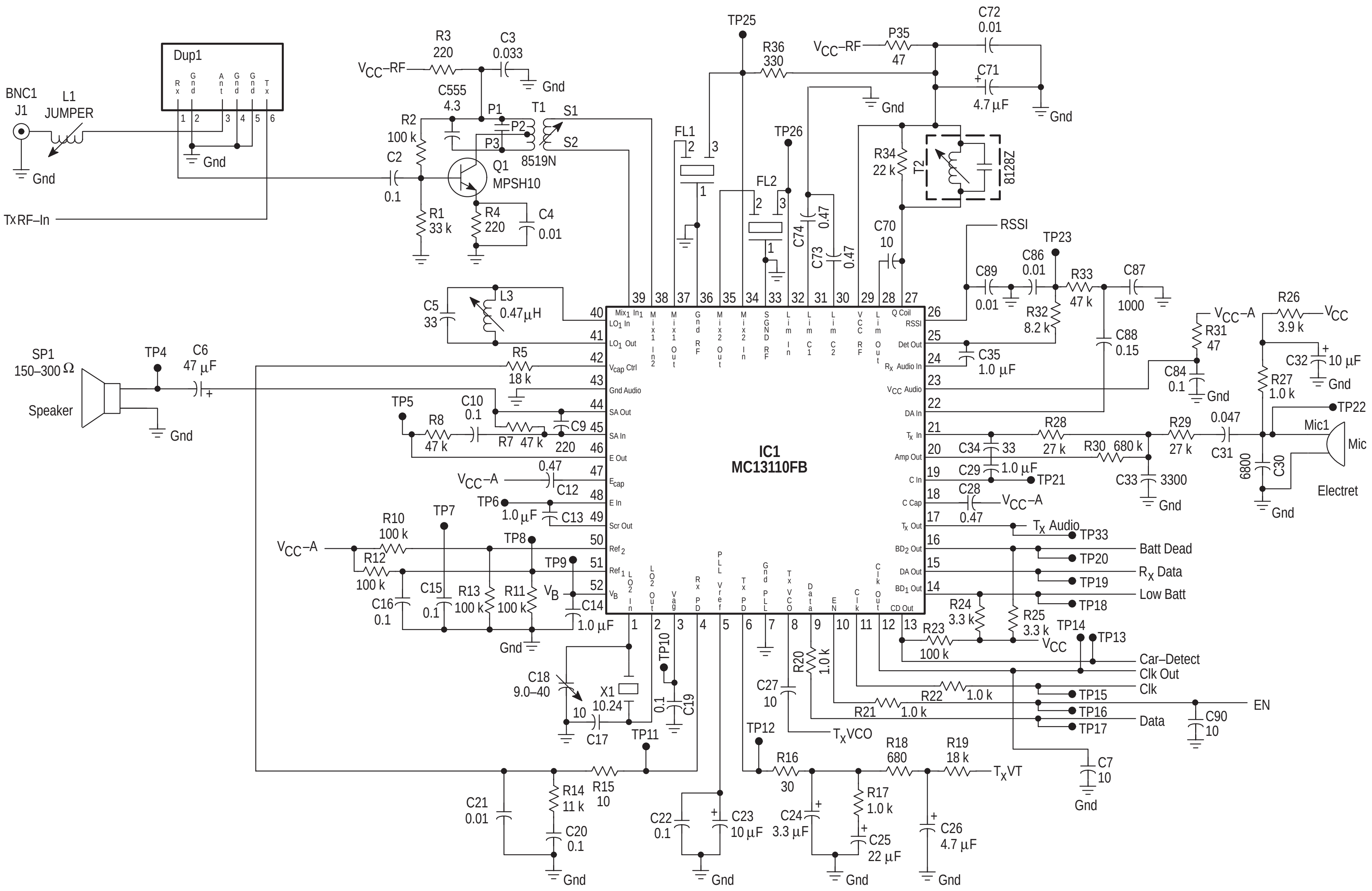
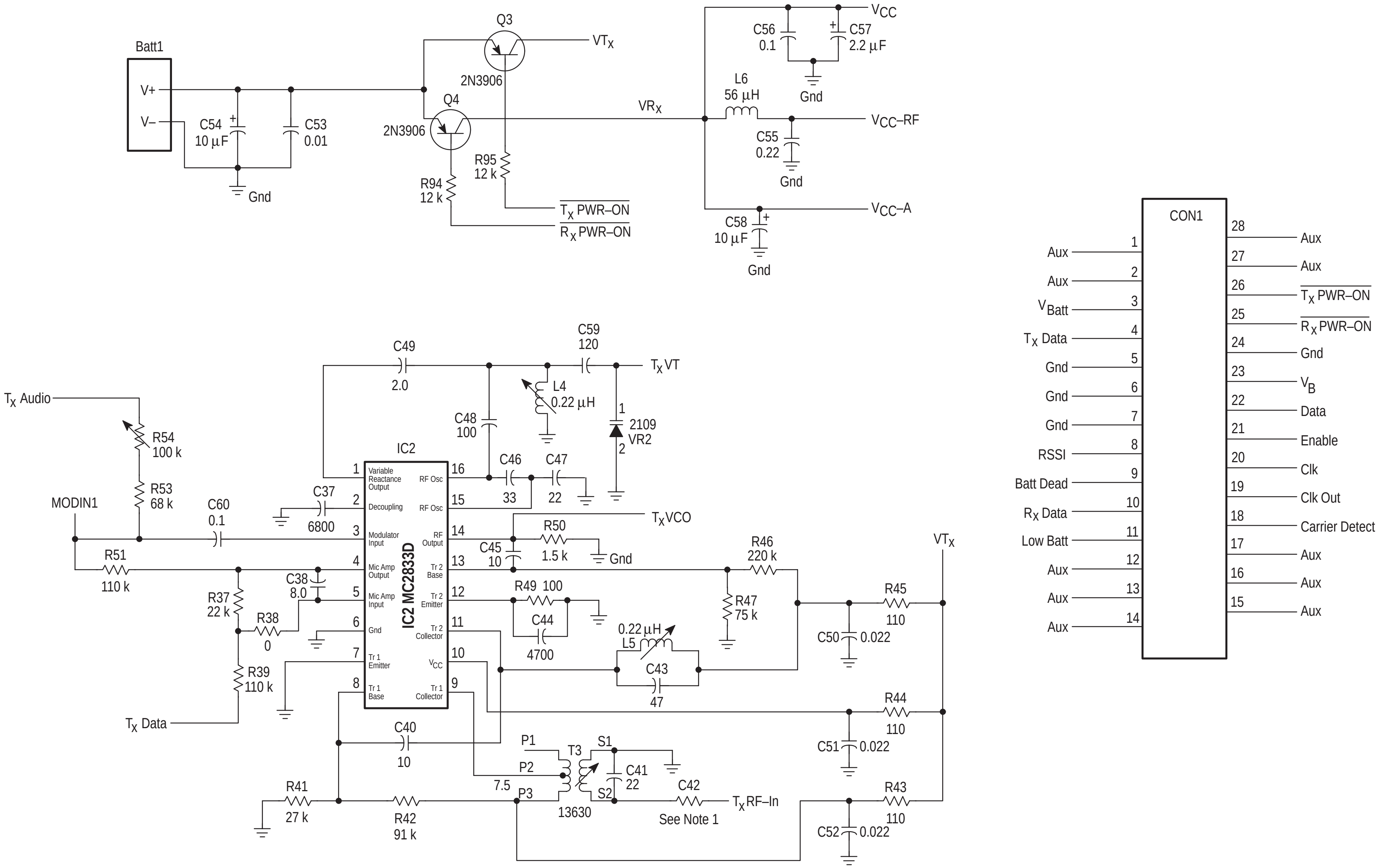


Figure 39b. Handset RF Applications Circuit (continued)



NOTE 1: C42 = X42 = 51 Ω

APPENDIX B – MC13110 APPLICATION BOARD BILL OF MATERIAL (USA)

Reference	Description	Value	Package	Part Number	Vendor
X1	10.24 Crystal (Load Cap <12 pF)	–	HC49US	AAL10M240000FLE10A	Standard Crystal
VR2	Diode	–	Sot23	MMBV2109LT1	Motorola
DUP1	Duplexer (25 Channel)	Baseset	Hybrid	DPX1035 75B–153B	Sumida
DUP1	Duplexer (25 Channel)	Handset	Hybrid	DPX1035 75B–154B	Sumida
FL1	10.7 MHz Filter (Red Dot)	–	–	SFE10.7MS2–A	muRata
FL2	455 kHz Filter	–	–	CFU455E2	muRata
IC1	Universal Cordless Telephone IC	–	QFP	MC13110FB	Motorola
IC2	FM Transmitter IC	–	SO–16	MC2833D	Motorola
L3	Inductor	0.47 μH	Can	292SNS–T1370Z	Toko
L4/L5	Inductor	0.22 μH	Can	292SNS–T1368Z	Toko
T1/T3	Transformer	–	Can	600GCS–8519N	Toko
T2	Quadrature Coil	–	Can	7MCS–8128Z	Toko
Q1	Transistor	–	TO–92	MPSH10	Motorola
Q3	Transistor	–	TO–92	2N3906	Motorola
Q4	Transistor	–	TO–92	2N3906	Motorola

NOTE: Components for the Handset and Baseset are the same, except where noted on the Bill of Material and Schematic.

APPENDIX C – MEASUREMENT OF COMPANDOR ATTACK/DECAY TIME

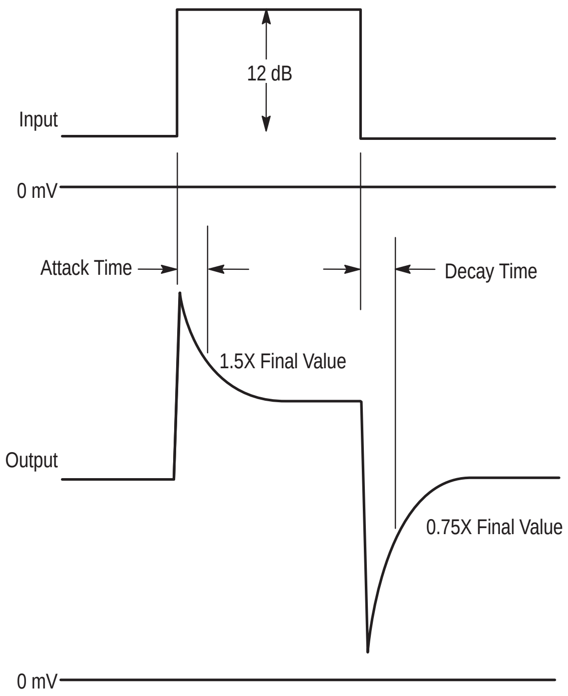
This measurement definition is based on EIA/CCITT recommendations.

Compressor Attack Time

For a 12 dB step up at the input, attack time is defined as the time for the output to settle to 1.5X of the final steady state value.

Compressor Decay Time

For a 12 dB step down at the input, decay time is defined as the time for the input to settle to 0.75X of the final steady state value.

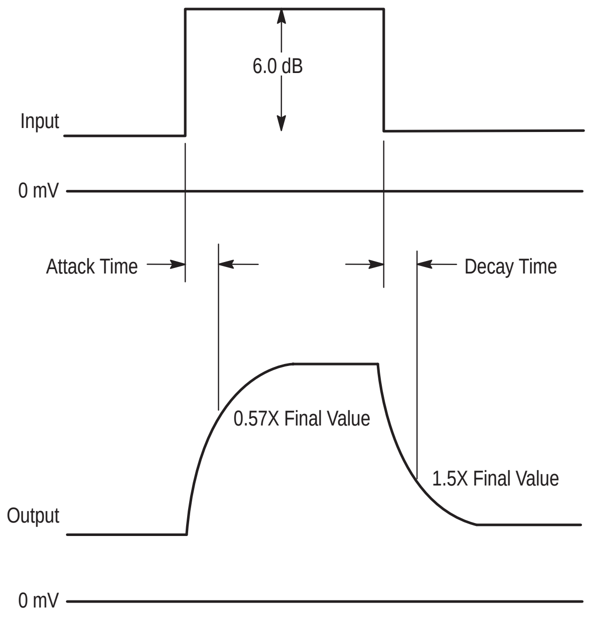


Expandor Attack

For a 6.0 dB step up at the input, attack time is defined as the time for the output to settle to 0.57X of the final steady state value.

Expandor Decay

For a 6.0 dB step down at the input, decay time is defined as the time for the output to settle to 1.5X of the final steady state value.



MOTOROLA

Universal Cordless Telephone Subsystem IC

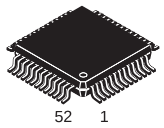
MC13111

**UNIVERSAL CT–1
SUBSYSTEM
INTEGRATED CIRCUIT**

**SEMICONDUCTOR
TECHNICAL DATA**

The MC13111 integrates several of the functions required for a cordless telephone into a single integrated circuit. This significantly reduces component count, board space requirements, external adjustments, and lowers overall costs. It is designed for use in both the handset and the base.

- Dual Conversion FM Receiver
  - Complete Dual Conversion Receiver – Antenna In to Audio Out 80 MHz Maximum Carrier Frequency
  - RSSI Output
  - Carrier Detect Output with Programmable Threshold
  - Comparator for Data Recovery
  - Operates with Either a Quad Coil or Ceramic Discriminator
- Compander
  - Expandor Includes Mute, Digital Volume Control, Speaker Driver, 3.5 kHz Low Pass Filter, and Programmable Gain Block
  - Compressor Includes Mute, 3.5 kHz Low Pass Filter, Limiter, and Programmable Gain Block
- Dual Universal Programmable PLL
  - Supports New 25 Channel U.S. Standard with No External Switches
  - Universal Design for Domestic and Foreign CT–1 Standards
  - Digitally Controlled Via a Serial Interface Port
  - Receive Side Includes 1st LO VCO, Phase Detector, and 14–Bit Programmable Counter and 2nd LO with 12–Bit Counter
  - Transmit Section Contains Phase Detector and 14–Bit Counter
  - MPU Clock Outputs Eliminates Need for MPU Crystal
- Supply Voltage Monitor
  - Provides Two Levels of Monitoring with Separate Outputs
  - Separate, Adjustable Trip Points
- Programmable Corner Frequency Selection
- MC13111 is Pin–for–Pin Compatible with MC13110
- 2.7 to 5.5 V Operation with One–Third the Power Consumption of Competing Devices
- AN1575: Refer to this Application Note for a List of the “Worldwide Cordless Telephone Frequencies” (List can also be found in Chapter 8 Addendum of DL128 Data Book)

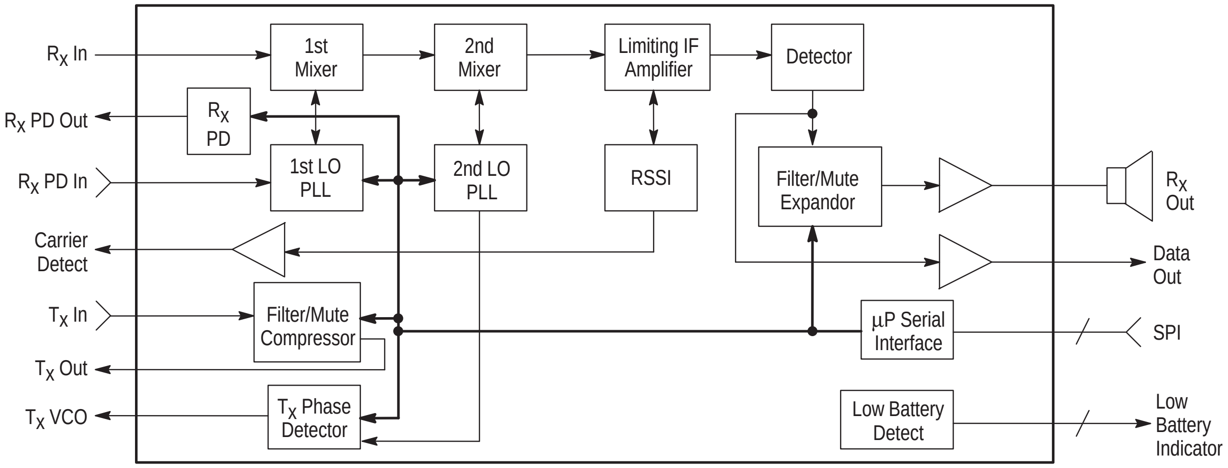


FB SUFFIX
PLASTIC QFP PACKAGE
CASE 848B

ORDERING INFORMATION

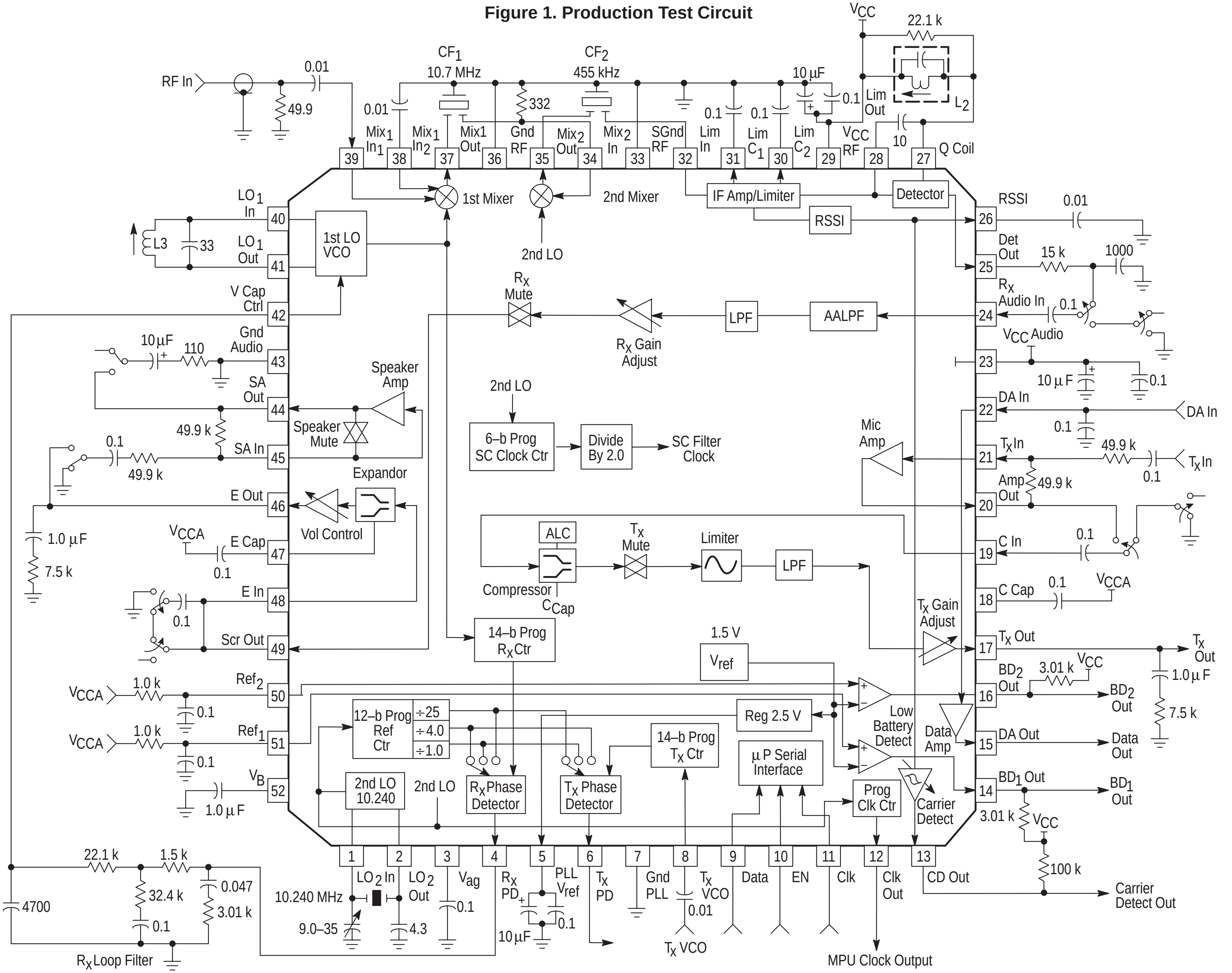
Device	Tested Operating Temperature Range	Package
MC13111FB	T_A = – 40° to +85°C	QFP–52

Simplified Application



This device contains 8,262 active transistors.

Figure 1. Production Test Circuit



NOTE: This schematic is only a representation of the actual production test circuit.

MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	–0.5 to +6.0	Vdc
Junction Temperature	T_J	–65 to +150	°C

NOTES: 1. Devices should not be operated at these limits. The "Recommended Operating Conditions" provide for actual device operation.

2. ESD data available upon request.

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	2.7	3.6	5.5	Vdc
Operating Ambient Temperature	T_A	–40	–	85	°C
Input Voltage Low (Data, Clk, EN)	V_{IL}	–	–	0.3	V
Input Voltage High (Data, Clk, EN)	V_{IH}	2.5	–	–	V
Output Current (R_X PD, T_X PD)					mA
High	I_{OH}	–	–	–0.7	
Low	I_{OL}	0.7	–	–	

NOTE: All limits are not necessarily functional concurrently.

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 3.6 V, T_A = 25°C, unless otherwise specified; Test Circuit Figure 1.)

Characteristic	Symbol	Min	Typ	Max	Unit
Static Current					
Active Mode (2.7 V)	ACT I_{CC}	–	8.1	–	mA
Active Mode	ACT I_{CC}	–	8.6	12	mA
Receive Mode	R_X I_{CC}	–	4.3	5.3	mA
Standby Mode	STD I_{CC}	–	270	500	µA
Inactive Mode	INACT I_{CC}	–	35	80	µA

ELECTRICAL CHARACTERISTICS (V_{CC} = 3.6 V, V_B = 1.5 V, T_A = 25°C, Active or R_X Mode, unless otherwise specified; Test Circuit Figure 1.)

Characteristic	Condition	Input Pin	Measure Pin	Symbol	Min	Typ	Max	Unit
PLL VOLTAGE REGULATOR								
Regulated Output Level	I_L = 0 mA	–	PLL V_{ref}	V_O	2.4	2.5	2.6	V
Line Regulation	I_L = 0 mA, V_{CC} = 3.6 to 5.5 V	V_{CC} Audio	PLL V_{ref}	V_{Reg} Line	–	–0.6	20	mV
Load Regulation	V_{CC} = 3.6 V, I_L = 1.0 mA	V_{CC} Audio	PLL V_{ref}	V_{Reg} Load	–	–1.1	20	mV
PLL LOOP CHARACTERISTICS								
2nd LO Frequency (No Crystal)	–	LO_2 In	–	f_{2ext}	–	12	–	MHz
2nd LO Frequency (With Crystal)	–	–	LO_2 In LO_2 Out	f_{2ext}	–	12	–	MHz
T_X VCO (Input Frequency)	V_{in} = 200 mVpp	–	T_X VCO	f_{txmax}	–	80	–	MHz

ELECTRICAL CHARACTERISTICS (continued) (V_{CC} = 3.6 V, V_B = 1.5 V, T_A = 25°C, Active or R_X Mode, unless otherwise specified; Test Circuit Figure 1.)

Characteristic	Condition	Input Pin	Measure Pin	Symbol	Min	Typ	Max	Unit
PLL PHASE DETECTOR								
Output Voltage Low	I_{IL} = 0.7 mA	–	R_X PD T_X PD	V_{OL}	–	–	(PLL V_{ref}) *.2	V
Output Voltage High	I_{IH} = –0.7 mA	–	R_X PD T_X PD	V_{OL}	(PLL V_{ref}) *.8	–	–	V
3–State Leakage Current	V = 1.2 V	–	R_X PD T_X PD	I_{OZ}	–50	–	50	nA
Output Capacitance	–	–	R_X PD T_X PD	C_{out}	–	8.0	–	pF
Output Rise and Fall Time	C_{Load} = 50 pF	–	R_X PD T_X PD Clk Out	t_r, t_f	–	250	–	ns
MICROPROCESSOR SERIAL INTERFACE								
Input Current Low	V_{in} = 0.3 V Standby Mode	–	Data, Clk, EN	I_{IL}	–5.0	0.3	–	µA
Input Current High	V_{in} = 3.3 V Standby Mode	–	Data, Clk, EN	I_{IH}	–	1.5	5.0	µA
Hysteresis Voltage	–	–	Data, Clk, EN	V_{hys}	–	1.0	–	V
Maximum Clock Frequency	–	Data, EN, Clk	–	–	–	2.0	–	MHz
Input Capacitance	–	Data, Clk, EN	–	C_{in}	–	8.0	–	pF
EN to Clk Setup Time	–	–	EN, Clk	t_{suEC}	–	200	–	ns
Data to Clk Setup Time	–	–	Data, Clk	t_{suDC}	–	100	–	ns
Hold Time	–	–	Data, Clk	t_h	–	90	–	ns
Recovery Time	–	–	EN, Clk	t_{rec}	–	90	–	ns
Input Pulse Width	–	–	EN, Clk	t_w	–	100	–	ns
Input Rise and Fall Time	–	–	Data, Clk, EN	t_r, t_f	–	9.0	–	µs
MPU Interface Power–Up Delay	90% of PLL V_{ref} to Data, Clk, EN	–	–	t_{puMPU}	–	100	–	µs
FM RECEIVER (f_{RF} = 46.77 MHz [USA Ch 21], f_{dev} = ±3.0 kHz, f_{mod} = 1.0 kHz)								
Sensitivity (Input for 12 dB SINAD)	50 Ω Termination	Mix_1 $In_{1/2}$	Det Out	V_{SIN}	– –	2.8 –98	– –	µVrms dBm
	Single–Ended, Matched Input Generator Referred	Mix_1 $In_{1/2}$	Det Out	V_{SIN}	– –	1.0 –107	– –	µVrms dBm
	Differential, Matched Input Generator Referred	Mix_1 $In_{1/2}$	Det Out	V_{SIN}	– –	.56 –112	– –	µVrms dBm
1st Mixer Voltage Conversion Gain	V_{in} = 1.0 mVrms, with CF_1 Filter as Load	Mix_1 $In_{1/2}$	Mix_1 Out	MX_{gain1}	–	12	–	dB
2nd Mixer Voltage Conversion Gain	V_{in} = 3.0 mVrms, with CF_2 Filter as Load	Mix_2 In	Mix_2 Out	MX_{gain2}	–	20	–	dB
1st and 2nd Mixer Voltage Gain Total	V_{in} = 1.0 mVrms, with CF_1 and CF_2 Load	Mix_1 $In_{1/2}$	Mix_2 Out	MX_{gainT}	24	28	–	dB
1st Mixer Input Impedance	Single–Ended Input	–	Mix_1 $In_{1/2}$	R_{P1} C_{P1}	– –	875 2.7	– –	Ω pF
2nd Mixer Input Impedance	f_{in} = 10.7 MHz	–	Mix_2 In	Z_{in2}	–	3.0	–	kΩ

ELECTRICAL CHARACTERISTICS (continued) (V_{CC} = 3.6 V, V_B = 1.5 V, T_A = 25°C, Active or R_x Mode, unless otherwise specified; Test Circuit Figure 1.)

Characteristic	Condition	Input Pin	Measure Pin	Symbol	Min	Typ	Max	Unit
FM RECEIVER (f_{RF} = 46.77 MHz [USA Ch 21], f_{dev} = ±3.0 kHz, f_{mod} = 1.0 kHz)								
1st Mixer Output Impedance	–	–	Mix$_1$ Out	Z_{out1}	–	330	–	Ω
2nd Mixer Output Impedance	–	–	Mix$_2$ Out	Z_{out2}	–	1.5	–	kΩ
IF –3.0 dB Limiting Sensitivity	f_{in} = 455 kHz	Lim In	Det Out	IF Sens	–	71	100	µVrms
Total Harmonic Distortion	With R_C = 15 k/1.0 nF Filter at Det Out	Mix$_1$ In$_1$	Det Out	THD	–	1.3	2.0	%
Recovered Audio	V_{in} = 3.16 mVrms with R_C = 15 k/1000 pF Filter at Det Out	Mix$_1$ In$_1$	Det Out	AFO	80	105	150	mVrms
Demodulator Bandwidth	–	Lim In	Det Out	BW	–	20	–	kHz
Signal to Noise Ratio	V_{in} = 3.16 mVrms, R_C = 15 k/1000 pF	Mix$_1$ In$_1$	Det Out	SN	–	49	–	dB
AM Rejection Ratio	V_{in} = 3.16 mVrms, 30% AM, @ 1.0 kHz, R_C = 15 k/1000 pF	Mix$_1$ In$_1$	Det Out	AMR	30	47	–	dB
1st Mixer, 1.0 dB Voltage Compression (Input Pin Referred)	–	Mix$_1$ In$_{1/2}$	Mix$_1$ Out	V_O 1.0 dB Mix$_1$	–	15	–	mVrms
2nd Mixer, 1.0 dB Voltage Compression (Input Pin Referred)	50 Ω Input	Mix$_2$ In	Mix$_2$ Out	V_O 1.0 dB Mix$_2$	–	14	–	mVrms
1st Mixer 3rd Order Intercept (Input Pin Referred)	V_{in} = 3.98 mVrms	Mix$_1$ In$_1$	Mix$_1$ Out	TOI_{mix1}	–	56	–	mVrms
2nd Mixer 3rd Order Intercept (Input Pin Referred)	V_{in} = 3.98 mVrms, 50 Ω Input	Mix$_2$ In	Mix$_2$ Out	TOI_{mix2}	–	53	–	mVrms
Detector Output Impedance	–	–	Det Out	Z_O	–	870	–	Ω
RSSI/CARRIER DETECT (R_L = 100 kΩ)								
RSSI Output Current Dynamic Range	–	Mix$_1$ In	RSSI	RSSI	–	80	–	dB
Carrier Sense Threshold	CD Threshold Adjust = (10100)	Mix$_1$ In	CD Out	V_T	–	33	–	µVrms
Hysteresis	–	Mix1 In	CD Out	Hys	–	3.6	7.0	dB
Output High Voltage	V_{in} = 0 Vrms, CD = (10100)	Mix$_1$ In	CD Out	V_{OH}	V_{CC} – 0.1	3.6	–	V
Output Low Voltage	V_{in} = –80 dBV, CD = (10100)	Mix$_1$ In	CD Out	V_{OL}	–	0.02	0.4	V

ELECTRICAL CHARACTERISTICS (continued) (V_{CC} = 3.6 V, V_B = 1.5 V, T_A = 25°C, Active or R_X Mode, unless otherwise specified; Test Circuit Figure 1.)

Characteristic	Condition	Input Pin	Measure Pin	Symbol	Min	Typ	Max	Unit
RSSI/CARRIER DETECT (R_L = 100 kΩ)								
Carrier Sense Threshold Adjustment Range	Programmable through MPU Interface	–	–	V_T low range	–20	–	–	dB
		–	–	V_T hi range	–	–	11	
Carrier Sense Threshold – Number of Steps	Programmable through MPU Interface	–	–	V_{Tn}	–	32	–	–
DATA AMP COMPARATOR								
Hysteresis	–	DA In	DA Out	Hys	30	40	50	mV
Threshold Voltage	–	DA In	DA Out	V_T	2.7	V_{CC} – 0.7	–	V
Input Impedance	–	–	DA In	Z_I	–	11	–	kΩ
Output Impedance	–	–	DA Out	Z_O	–	100	–	kΩ
Output High Voltage	V_{in} = V_{CC} – 1.0 V, I_{OH} = 0 mA	DA In	DA Out	V_{OH}	V_{CC} – 0.1	3.6	–	V
Output Low Voltage	V_{in} = V_{CC} – 0.4 V, I_{OL} = 0 mA	DA In	DA Out	V_{OL}	–	0.04	0.4	V
R_X AUDIO PATH (f_{in} = 1.0 kHz)								
Absolute Gain	V_{in} = –20 dBV	E In	E Out	G	–3.0	0	3.0	dB
Gain Tracking	V_{in} = –30 dBV V_{in} = –40 dBV	E In	E Out	G_t	–21 –42	–20 –40	–19 –38	dB
Total Harmonic Distortion	V_{in} = –20 dBV	E In	E Out	THD	–	0.5	1.0	%
Maximum Input Voltage	–	R_X Audio In	–	–	–	–11.5	–	dBV
Maximum Output Voltage	Increase input voltage until output voltage THD = 5.0%, then measure output voltage. R_L = 7.5 k/1.0 µF	E In	E Out	V_{Omax}	–	0	–	dBV
Input Impedance	–	R_X Audio In E In	–	Z_{in}	– –	600 7.5	– –	kΩ
Attack Time	E_{cap} = 0.5 µF, R_{filt} = 40 k (See Appendix B)	E In	E Out	t_a	–	3.0	–	ms
Release Time	E_{cap} = 0.5 µF, R_{filt} = 40 k (See Appendix B)	E In	E Out	t_r	–	13.5	–	ms
Compressor to Expandor Crosstalk	V_{in} = –10 dBV, $V_{(E\ In)}$ = AC Gnd	C In	E Out	C_T	–	–90	–70	dB
R_X Data Muting (Δ Gain)	V_{in} = –20 dBV, R_X Gain Adj = (01111)	R_X Audio In	E Out	M_e	–	–83	–60	dB
R_X High Frequency Corner (Note 1)	R_X Path, V R_X Audio In = –20 dBV	R_X Audio In	Scr Out	R_X f_{ch}	–	3.879	–	kHz
SPEAKER AMP/SP MUTE								
Maximum Output Swing	R_L = 130 Ω	SA In	SA Out	V_{Omax}	0.8	0.9	–	Vpp
Speaker Amp Muting	V_{in} = –20 dBV	SA In	SA Out	M_{sp}	–	–90	–60	dB
T_X AUDIO PATH (f_{in} = 1.0 kHz, T_X Gain Adj = (01111), f_{in} = 1.0 kHz)								
Absolute Gain	V_{in} = –10 dBV, ALC, Lim Disabled	T_X In	T_X Out	G	–4.0	0	4.0	dB
Gain Tracking	V_{in} = –30 dBV V_{in} = –40 dBV	T_X In	T_X Out	G_t	–11 –17	–10 –20	–9.0 –13	dB
Total Harmonic Distortion	V_{in} = –10 dBV	T_X In	T_X Out	THD	–	0.6	1.1	%

ELECTRICAL CHARACTERISTICS (continued) (V_{CC} = 3.6 V, V_B = 1.5 V, T_A = 25°C, Active or R_X Mode, unless otherwise specified; Test Circuit Figure 1.)

T_X AUDIO PATH (f_{in} = 1.0 kHz, T_X Gain Adj = (01111), f_{in} = 1.0 kHz)

Characteristic	Condition	Input Pin	Measure Pin	Symbol	Min	Typ	Max	Unit
Maximum Output Voltage	Increase input voltage until output voltage THD = 5.0%, then measure output voltage. R_L = 7.5 k/1.0 µF	C In	T_X Out	V_{Omax}	–	–5.0	–	dBV
Input Impedance	–	C In	T_X Out	Z_{in}	–	10	–	kΩ
Attack Time	C_{cap} = 0.5 µF, R_{filt} = 40 k (See Appendix B)	C In	T_X Out	t_a	–	3.0	–	ms
Release Time	C_{cap} = 0.5 µF, R_{filt} = 40 k (See Appendix B)	C In	T_X Out	t_r	–	13.5	–	ms
Expandor to Compressor Crosstalk	V_{in} = –20 dBV, Speaker Amp No Load, $V_{(C\ In)}$ = AC Gnd	E In	T_X Out	C_T	–	–60	–40	dB
T_X Muting	V_{in} – 10 dBV	T_X In	T_X Out	M_c	–	–90	–60	dB
ALC Output Level	V_{in} = –10 dBV V_{in} = –2.5 dBV Limiter and Mutes disabled	T_X In	T_X Out	ALC_{out}	–15 –13	–11 –10	–8.0 –6.0	dBV
Limiter Output Level	V_{in} = –2.5 dBV, ALC disabled	T_X In	T_X Out	V_{lim}	–10	–7.0	–	dBV
T_X High Frequency Corner (Note 1)	T_X Path, V T_X In = –10 dBV, Mic Amp = Unity Gain	T_X In	T_X Out	T_X f_{ch}	–	3.7	–	kHz

MIC AMP (f_{in} = 1.0 kHz, External resistors set to gain of 1)

Characteristic	Condition	Input Pin	Measure Pin	Symbol	Min	Typ	Max	Unit
Open Loop Gain	–	T_X In	Amp Out	AVOL	–	100,000	–	V/V
Gain Bandwidth	–	T_X In	Amp Out	GBW	–	100	–	kHz
Maximum Output Swing	R_L = 10 kΩ	T_X In	Amp Out	V_{Omax}	–	2.8	–	Vpp

LOW BATTERY DETECT

Characteristic	Condition	Input Pin	Measure Pin	Symbol	Min	Typ	Max	Unit
Average Threshold Voltage Before Electronic Adjustment	V_{CC} = 3.6 V, $V_{ref_}$Adj = (0111). Take average of rising and falling threshold	Ref_1 Ref_2	BD_1 Out BD_2 Out	VT_i	1.36	1.5	1.64	V
Average Threshold Voltage After Electronic Adjustment	V_{CC} = 3.6 V, $V_{ref_}$Adj = (adjusted value). Take average of rising and falling threshold	Ref_1 Ref_2	BD_1 Out BD_2 Out	VT_f	1.475	1.5	1.525	V
Hysteresis	–	Ref_1 Ref_2	BD_1 Out BD_2 Out	Hys	–	4.0	–	mV
Input Current	V_{in} = 1.0 to 2.0 V	–	Ref_1 Ref_2	I_{in}	–50	–	50	nA
Output High Voltage	V_{in} = 2.0 V, R_L = 3.9 kΩ to V_{CC}	Ref_1 Ref_2	BD_1 Out BD_2 Out	V_{OH}	V_{CC} – 0.1	3.6	–	V
Output Low Voltage	V_{in} = 1.0 V, R_L = 3.9 kΩ to V_{CC}	Ref_1 Ref_2	BD_1 Out BD_2 Out	V_{OL}	–	0.1	0.4	V

NOTE: 1. The filter specification is based on a 10.24 MHz 2nd LO, and a switched–capacitor (SC) filter counter divider ratio of 31. If other 2nd LO frequencies and/or SC filter counter divider ratios are used, the filter corner frequency will be proportional to the resulting SC filter clock frequency.

PIN FUNCTION DESCRIPTION

Pin	Symbol	Type	Description
1 2	LO_2 In LO2 Out	–	These pins form the PLL reference oscillator when connected to an external parallel–resonant crystal (10.24 MHz typical). The reference oscillator is also the second Local Oscillator (LO_2) for the RF receiver. "LO_2 In" may also serve as an input for an externally generated reference signal which is typically ac–coupled.
3	V_{ag}	–	Internal reference voltage for switched capacitor filter section.
4	R_x PD	Output	Three state voltage output of the R_x Phase Detector. This pin is either "high", "low", or "high impedance" depending on the phase difference of the phase detector input signals. During lock, very narrow pulses with a frequency equal to the reference frequency are present. This pin drives the external R_x PLL loop filter. It is important to minimize the line length and parasitic capacitance of this pin.
5	PLL V_{ref}	–	PLL voltage regulator output pin. An internal voltage regulator provides a stable power supply voltage for the R_x and T_x PLL's and can also be used as a regulated supply voltage for other IC's.
6	T_x PD	Output	Three state voltage output of the T_x Phase Detector. This pin is either "high", "low", or "high impedance" depending on the phase difference of the phase detector input signals. During lock, very narrow pulses with a frequency equal to the reference frequency are present. This pin drives the external T_x PLL loop filter. It is important to minimize the line length and parasitic capacitance of this pin.
7	Gnd PLL	Gnd	Ground pin for PLL section of IC.
8	T_x VCO	Input	Transmit divide counter input which is driven by an ac–coupled external transmit loop VCO. The minimum signal level is 200 mVpp @ 60.0 MHz. This pin also functions as the test mode input for the counter tests.
9 10 11	Data EN Clk	Input	Microprocessor serial interface input pins for programming various counters and control functions.
12	Clk Out	Output	Microprocessor Clock Output which is derived from the 2nd LO crystal oscillator and a programmable divider. It can be used to drive a microprocessor and thereby reduce the number of crystals required in the system design. The driver has an internal resistor in series with the output which can be combined with an external capacitor to form a low pass filter to reduce radiated noise on the PCB. This output also functions as the output for the counter test modes.
13	CD Out	I/O	Dual function pin; 1) Carrier detect output (open collector with external 100 kΩ pull–up resistor. 2) Hardware interrupt input which can be used to "wake–up" from Inactive Mode.
14	BD_1 Out	Output	Low battery detect output #1 (open collector with external pull–up resistor).
15	DA Out	Output	Data amplifier output (open collector with internal 100 kΩ pull–up resistor).
16	BD_2 Out	Output	Low battery detect output #2 (open collector with external pull–up resistor).
17	T_x Out	Output	T_x path audio output.
18	C Cap	–	Compressor rectifier filter capacitor pin. Pull pin high through a capacitor.
19	C In	Input	Compressor input (ac–coupled).
20	Amp Out	Output	Microphone amplifier output.
21	T_x In	Input	T_x path input to microphone amplifier (Mic Amp) (ac–coupled).
22	DA In	Input	Data amplifier input (ac–coupled).
23	V_{CC} Audio	Supply	V_{CC} supply for audio section.
24	R_x Audio In	Input	R_x audio input (ac–coupled).
25	Det Out	Output	Audio output from FM detector.
26	RSSI	Output	Receive Signal Strength Indicator filter capacitor.
27 28	Q Coil Lim Out	–	A quad coil or ceramic discriminator connected to these pins as part of the FM demodulator circuit.
29	V_{CC} RF	Supply	V_{CC} supply for RF receiver section.
30 31	Lim C_2 Lim C_1	–	IF amplifier/limiter capacitor pins.
32	Lim In	Input	Signal input for IF amplifier/limiter.

PIN FUNCTION DESCRIPTION (continued)

Pin	Symbol	Type	Description
33	SGND RF	Gnd	Ground pin for RF section of the IC.
34	Mix_2 In	Input	Second mixer input.
35	Mix_2 Out	Output	Second mixer output.
36	Gnd RF	Gnd	Ground pin for RF section of the IC.
37	Mix_1 Out	Output	First mixer output.
38	Mix_1 In_2	Input	Negative phase first mixer input.
39	Mix_1 In_1	Input	Positive phase first mixer input.
40 41	LO_1 In LO_1 Out	–	Tank Elements for 1st LO Multivibrator Oscillator are connected to these pins.
42	V_{cap} Ctrl	–	1st LO Varactor Control Pin.
43	Gnd Audio	Gnd	Ground for audio section of the IC.
44	SA Out	Output	Speaker amplifier output.
45	SA In	Input	Speaker amplifier input (ac–coupled).
46	E Out	Output	Expandor output.
47	E_{cap}	–	Expandor rectifier filter capacitor pin. Pull pin high through a capacitor.
48	E In	Input	Expandor Input.
49	Scr Out	Output	R_x Audio Output.
50	Ref_2	–	Reference voltage input for Low Battery Detect #2.
51	Ref_1	–	Reference voltage input for Low Battery Detect #1.
52	V_B	–	Internal half supply analog ground reference.

FM Receiver

The FM receiver can be used with either a quad coil or a ceramic resonator. The FM receiver and 1st LO have been designed to work for all country channels, including 25 channel U.S., without the need for any external switching circuitry (see Figure 32).

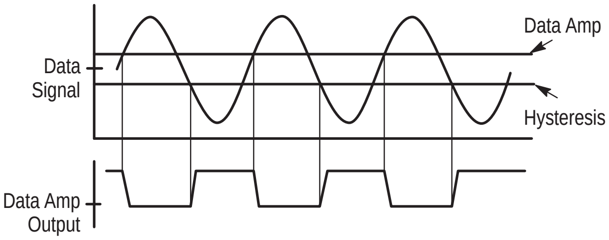
RSSI/Carrier Detect

Connect 0.01 µF to Gnd from “RSSI” output pin to form the carrier detect filter. “CD Out” is an open collector output which requires an external 100 kΩ pull–up resistor to V_{CC}. The carrier detect threshold is programmable through the MPU interface.

Data Amp Comparator

The data amp comparator is an inverting hysteresis comparator. Its open collector output has an internal 100 kΩ pull–up resistor. A band pass filter is connected between the “Det Out” pin and the “DA In” pin with component values as shown in Figure 1 (Test Circuit). The “DA In” input signal is ac–coupled.

Figure 2. Data Amp Operation



Expandor/ Compressor

In Appendix B, the EIA/CCITT recommendations for measurement of the attack and decay times are defined. The curves in Figures 3 and 4 show the typical expandor and compressor output versus input responses.

Figure 3. Expandor Typical Response

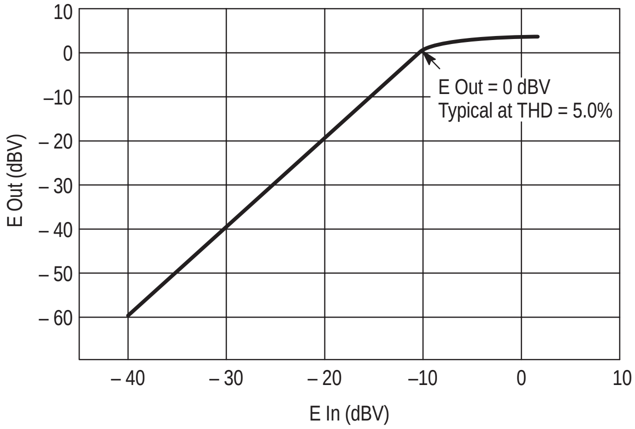
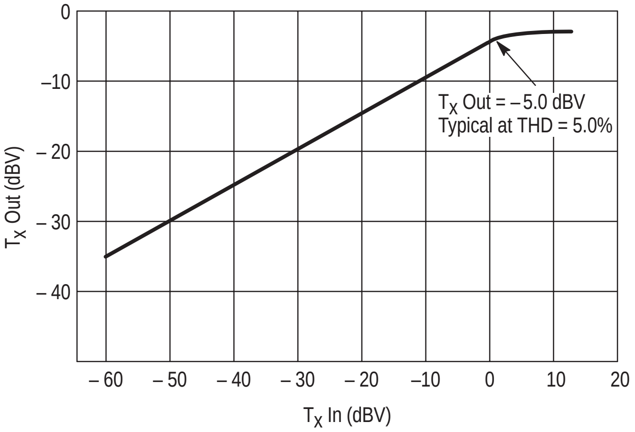


Figure 4. Compressor Typical Response



R_X Audio Path (LPF/R_X Gain Adjust/ R_X Mute/Expandor/Volume Control)

The R_X Audio signal path goes from “R_X Audio In” (Pin 24) to “E Out” (Pin 46). The “R_X Audio In” input signal is ac coupled. AC couple between “Scr Out” and “E In” (see Figure 3).

Speaker Amp/SP Mute

The Speaker Amp is an inverting rail–to–rail operational amplifier. The noninverting input is connected to the internal V_B reference. External resistors and capacitors are used to set the gain and frequency response. The “SA In” Input is ac coupled.

Mic Amp

The Mic Amp is an inverting rail–to–rail operational amplifier with noninverting input terminal connected to internal V_B reference. External resistors and capacitors are set to the gain and frequency response. The “T_X In” input is ac coupled.

T_X Audio Path (Compressor/ALC/T_X Mute/ Limiter/LPF/T_X Gain Adjust)

The T_X Audio signal path goes from “T_X In” (Pin 19) to “T_X Out” (Pin 17). The “C In” input signal is ac coupled from “Amp Out”. The ALC (Automatic Level Control) provides a “soft” limit to the output signal swing as the input voltage increases slowly (i.e., a sine wave is maintained). The Limiter circuit limits rapidly changing signal levels by clipping the signal peaks. The ALC and/or Limiter can be disabled through the MPU serial interface (see Figure 4).

T_X and R_X Audio

Each audio path contains a low–pass switched capacitor filter (SCF). The control register must be set through the MPU interface (Figure 11) for proper operation (T_X and R_X bits must be set to “1”). The SCF corner frequencies are proportional to the SCF Clock. The SCF Clock Divider is programmable through the MPU interface as follows: (SCF) = F(2nd LO) / (SCF Divider Value * 2). The LPF corner frequencies can be selected in from the table in Figures 28 and 29 relative to the 2nd LO operating frequency.

PLL Voltage Regulator

The “PLL V_{ref}” pin is the internal supply voltage for the R_X and T_X PLL’s. It is regulated to a nominal 2.5 V. The “V_{CC} Audio” pin is the supply voltage for the internal voltage regulator. Two capacitors with 10 µF and 0.1 µF values must be connected to the “PLL V_{ref}” pin to filter and stabilize this regulated voltage. The “PLL V_{ref}” pin may be used to power other IC’s as long as the total external load current does not exceed 1.0 mA. The tolerance of the regulated voltage is initially ±8.0%, but is improved to ±4.0% after the internal Bandgap voltage reference is adjusted electronically through the MPU serial interface. The voltage regulator is turned off in the Standby and Inactive modes to reduce current drain. In these modes, the “PLL V_{ref}” pin is internally connected to the “V_{CC} Audio” pin (i.e., the power supply voltage is maintained but is now unregulated).

Low Battery Detect

Two external precision resistor dividers are used to set independent thresholds for two battery detect hysteresis comparators. The voltages on “Ref_1” and “Ref_2” are compared to an internally generated 1.5 V reference voltage. The tolerance of the internal reference voltage is initially ±6.0%. The Low Battery Detect threshold tolerance can be improved by adjusting a trim–pot in the external resistor divider. Alternately, the tolerance of the internal reference voltage can be improved to ±1.5% through MPU serial interface programming. The internal reference can be measured directly at the “V_B” pin. During final test of the telephone, the V_B internal reference voltage is measured. Then, the internal reference voltage value is adjusted electronically through the MPU serial interface to achieve the desired accuracy level. The voltage reference register value should be stored in ROM during final test so that it can be reloaded each time the MC13111 IC is powered up. Low Battery Detect outputs are open collector.

Power Supply Voltage

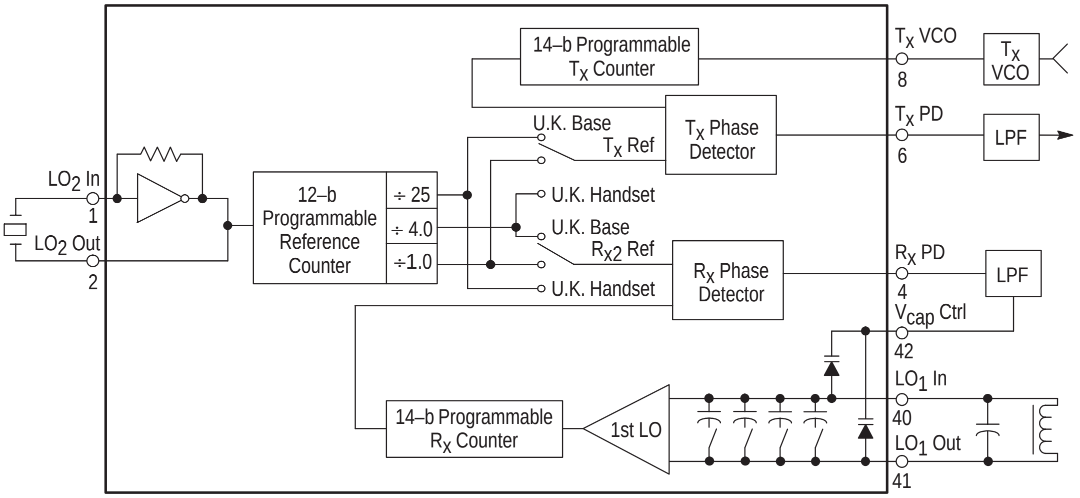
This circuit is used in a cordless telephone handset and base unit. The handset is battery powered and can operate on three NiCad cells or on 5.0 V supply.

PLL Frequency Synthesizer General Description

Figure 5 shows a simplified block diagram of the programmable universal dual phase locked loop (PLL). This dual PLL is fully programmable through the MCU serial interface and supports most country channel frequencies including USA (25 ch), Spain, Australia, Korea, New Zealand, U. K., Netherlands, France, and China.

The 2nd local oscillator and reference divider provide the reference frequency for the receive (R_X) and transmit (T_X) PLL loops. The programmed divider value for the reference divider is selected based on the crystal frequency and the desired R_X and T_X reference frequency values. Additional divide by 25 and divide by 4 blocks are provided to allow for generation of the 1.0 kHz and 6.25 kHz reference frequencies required for the U. K. The 14–bit T_X counter is programmed for the desired transmit channel frequency. The 14–bit R_X counter is programmed for the desired first local oscillator frequency. All counters power up in the proper default state for USA channel #21 (channel #6 for FCC 10 channel band) and for a 10.24 MHz reference frequency crystal. Internal fixed capacitors can be connected to the tank circuit of the 1st LO through microprocessor control to extend the sensitivity of the 1st LO for U.S. 25 channel operation.

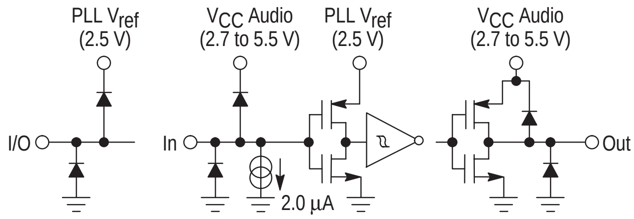
Figure 5. Dual PLL Simplified Block Diagram



PLL I/O Pin Specifications

The 2nd LO, R_X and T_X PLL's, and MPU serial interface are powered by the internal voltage regulator at the "PLL V_{ref}" pin. The "PLL V_{ref}" pin is the output of a voltage regulator which is powered from the "V_{CC} Audio" power supply pin and is regulated by an internal bandgap voltage reference. Therefore, the maximum input and output levels for most PLL I/O pins (LO_2 In, LO_2 Out, R_X PD, T_X PD, T_X VCO) is the regulated voltage at the "PLL V_{ref}" pin. The ESD protection diodes on these pins are also connected to "PLL V_{ref}". Internal level shift buffers are provided for the pins (Data, Clk, EN, Clk Out) which connect directly to the microprocessor. The maximum input and output levels for these pins is V_{CC}. Figure 6 shows a simplified schematic of the I/O pins.

Figure 6. PLL I/O Pin Simplified Schematics



LO_2 In, LO_2 Out, R_X PD, T_X PD and T_X VCO Pins

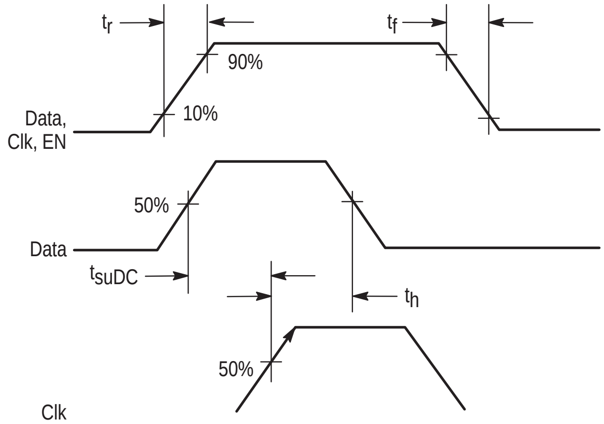
Data, Clk and EN Pins

Clk Out Pin

Microprocessor Serial Interface

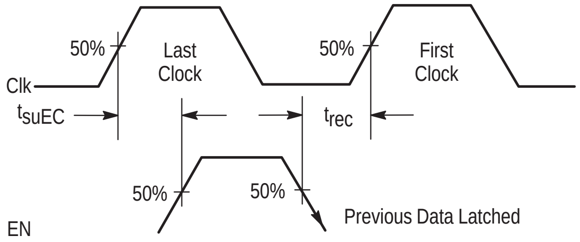
The "Data", "Clk", and "EN" pins provide an MPU serial interface for programming the reference counters, the transmit and receive channel divider counters, the switched capacitor filter clock counter, and various control functions. The "Data" and "Clk" pins are used to load data into the shift register. Figure 7 shows the timing required on the "Data" and "Clk" pins. Data is clocked into the shift register on positive clock transitions.

Figure 7. Data and Clock Timing Requirement



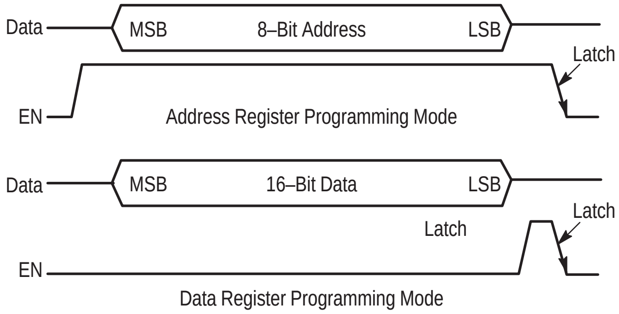
After data is loaded into the shift register, the data is latched into the appropriate latch register using the "EN" pin. This is done in two steps. First, an 8–bit address is loaded into the shift register and latched into the 8–bit address latch register. Then, up to 16–bits of data is loaded into the shift register and latched into the data latch register specified by the address that was previously loaded. Figure 5 shows the timing required on the EN pin. Latching occurs on the negative EN transition.

Figure 8. Enable Timing Requirement



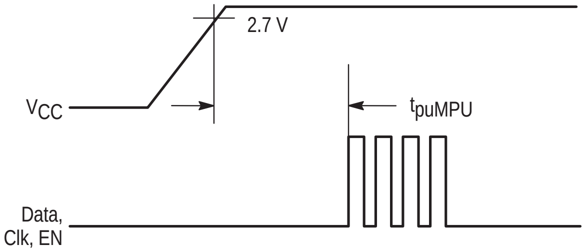
The state of the EN pin when clocking data into the shift register determines whether the data is latched into the address register or a data register. Figure 9 shows the address and data programming diagrams. In the data programming mode, there must not be any clock transitions when "EN" is high. The clock can be in a high state (default high) or a low state (default low) but must not have any transitions during the "EN" high state. The convention in these figures is that latch bits to the left are loaded into the shift register first.

Figure 9. Microprocessor Interface Programming Mode Diagrams



The MPU serial interface is fully operational within 100 µs after the power supply has reached its minimum level during power–up (see Figure 10). The MPU Interface shift registers and data latches are operational in all four power saving modes; Inactive, Standby, R_X, and Active Modes. Data can be loaded into the shift registers and latched into the latch registers in any of the operating modes.

Figure 10. Microprocessor Serial Interface Power–Up Delay



Data Registers

Figure 11 shows shows the data latch registers and addresses which are used to select each of these registers. Latch bits to the left (MSB) are loaded into the shift register first. The LSB bit must always be the last bit loaded into the shift register. Bits preceeding the register must be "0's" as shown in Figure 11.

Figure 11. Microprocessor Interface Data Latch Registers

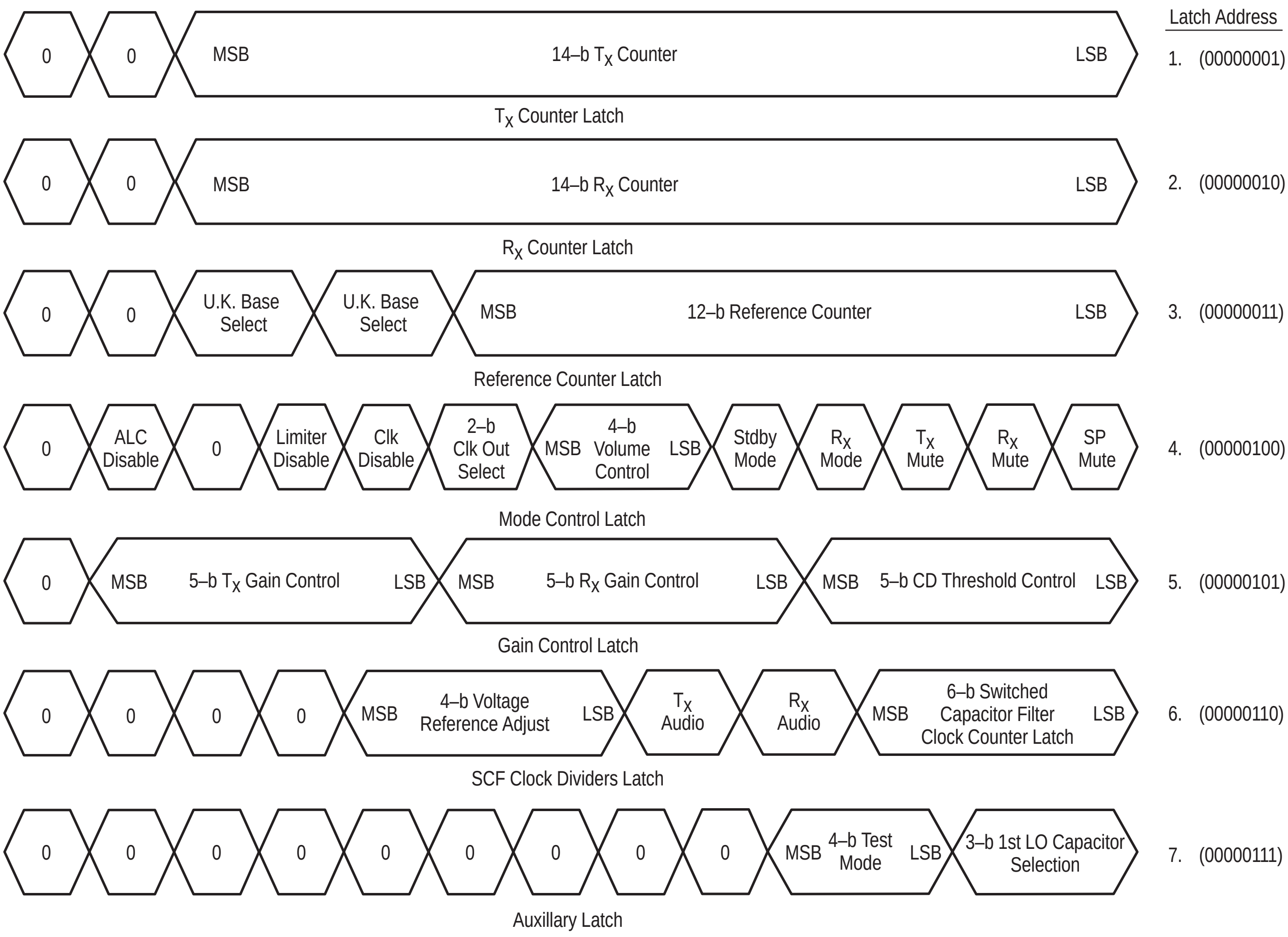


Figure 12. Reference Frequency and Reference Divider Values

Crystal Frequency	Reference Divider Value	U.K. Base/ Handset Divider	Reference Frequency	SC Filter Clock Divider	SC Filter Clock Frequency
10.24 MHz	2048	1.0	5.0 kHz	31	165.16 kHz
10.24 MHz	1024	4.0	2.5 kHz	31	165.16 kHz
11.15 MHz	2230	1.0	5.0 kHz	34	163.97 kHz
12.00 MHz	2400	1.0	5.0 kHz	36	166.67 kHz
11.15 MHz	1784	1.0	6.25 kHz	34	163.97 kHz
11.15 MHz	446	4.0	6.25 kHz	34	163.97 kHz
11.15 MHz	446	25	1.0 kHz	34	163.97 kHz

Reference Frequency Selection

The "LO$_2$ In" and "LO$_2$ Out" pins form a reference oscillator when connected to an external parallel–resonant crystal. The reference oscillator is also the second local oscillator for the RF Receiver. Figure 12 shows the relationship between different crystal frequencies and reference frequencies for cordless phone applications in various countries. "LO$_2$ In" may also serve as an input for an externally generated reference signal which is ac–coupled. The switched capacitor filter 6–bit programmable counter must be programmed for the crystal frequency that is selected since this clock is derived from the crystal frequency and must be held constant regardless of the crystal that is selected. The actual switched capacitor clock divider ratio is twice the programmed divider ratio since there is a fixed divide by 2.0 after the programmable counter.

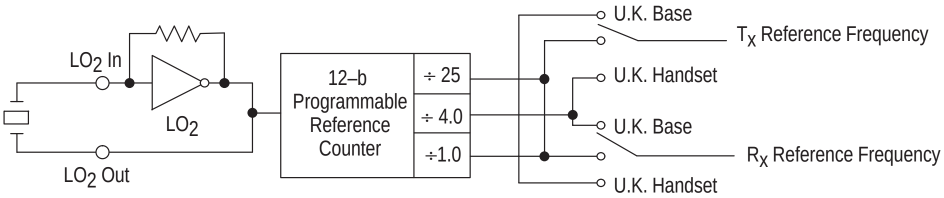
Reference Counter

Figure 13 shows how the reference frequencies for the R_X and T_X loops are generated. All countries except the U.K. require that the T_X and R_X reference frequencies be identical. In this case, set "U.K. Base Select" and "U.K. Handset Select" bits to "0". Then the fixed divider is set to "1" and the T_X and R_X reference frequencies will be equal to the crystal oscillator frequency divided by the programmable reference counter value. The U.K. is a special case which requires a different reference frequency value for T_X and R_X. For U.K. base operation, set "U.K. Base Select" to "1". For U.K. handset operation, set "U.K. Handset Select" to "1".The Netherlands is also a special case since a 2.5 kHz reference frequency is used for both the T_X and R_X reference and the total divider value required is 4096 which is larger than the maximum divide value available from the 12–bit reference divider (4095). In this case, set "U.K. Base Select" to "1" and set "U.K. Handset Select" to "1". This will give a fixed divide by 4 for both the T_X and R_X reference. Then set the reference divider to 1024 to get a total divider of 4096.

Mode Control Register

Power saving modes, mutes, disables, volume control, and microprocessor clock output frequency are all set by the Mode Control Register. Operation of the Mode Control Register is explained in Figures 14 through 21.

Figure 13. Reference Counter Register Programming Mode



U.K. Handset Select	U.K. Base Select	T_X Divider Value	R_X Divider Value	Application
0	0	1.0	1.0	All but U.K. and Netherlands
0	1	25	4.0	U.K. Base Set
1	0	4.0	25	U.K. Hand Set
1	1	4.0	4.0	Netherlands Base and Hand Set

14–Bit Reference Counter Latch

Figure 14. Mode Control Register Bits

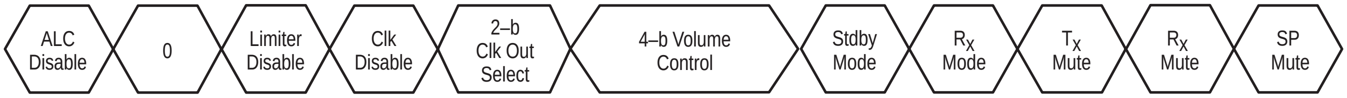


Figure 15. Mute and Disable Control Bit Descriptions

ALC Disable	1 0	Automatic Level Control Disabled Normal Operation
Limiter Disable	1 0	Limiter Disabled Normal Operation
Clock Disable	1 0	MPU Clock Output Disabled Normal Operation
T_X Mute	1 0	Transmit Channel Muted Normal Operation
R_X Mute	1 0	Receive Channel Muted Normal Operation
SP Mute	1 0	Speaker Amp Muted Normal Operation

Power Saving Operating Modes

When the MC13111 is used in a handset, it is important to conserve power in order to prolong battery life. There are five modes of operation; Active, R_X, Standby, Interrupt, and Inactive. In Active mode, all circuit blocks are powered. In R_X mode, all circuitry is powered down except for those circuit sections needed to receive a transmission from the base. In the Standby and Interrupt Modes, all circuitry is powered down except for the circuitry needed to provide the clock output for the microprocessor. In Inactive Mode, all circuitry is powered down except the MPU interface. Latch memory is maintained in all modes. Figure 16 shows the control register bit values for selection of each power saving mode and Figure 17 shows the circuit blocks which are powered in each of these operating modes.

Figure 16. Power Saving Mode Selection

Stdby Mode Bit	R_X Mode Bit	"CD Out/ Hardware Interrupt" Pin	Mode
0	0	X	Active
0	1	X	R_X
1	0	X	Standby
1	1	1 or High Impedance	Inactive
1	1	0	Interrupt

Figure 17. Power Saving Modes

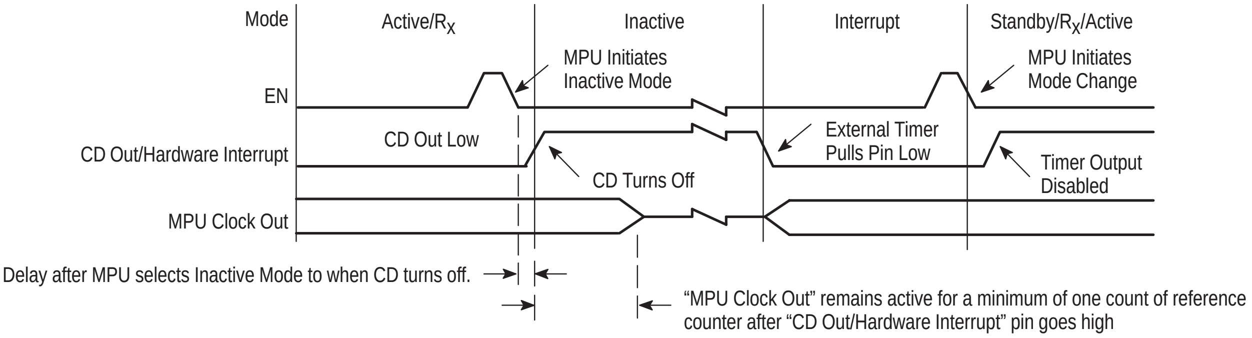
Circuit Blocks	Active	R_X	Standby	Inactive
"PLL V_{ref}" Regulated Voltage	X	X	X[1]	X[1]
MPU Interface	X	X	X	X
2nd LO Oscillator	X	X	X	
MPU Clock Output	X	X	X	
RF Receiver and 1st LO VCO	X	X		
R_X PLL	X	X		
Carrier Detect	X	X		
Data Amp	X	X		
Low Battery Detect	X	X		
T_X PLL	X			
R_X and T_X Audio Paths	X			

NOTE: In Standby and Inactive Modes, "PLL V_{ref}" remains powered but is not regulated. It will fluctuate with V_{CC}.

Inactive Mode Operation and Hardware Interrupt

In some handset applications it may be desirable to power down all circuitry including the microprocessor (MPU). First put the combo IC into the Inactive mode, which turns off the MPU Clock Output (see Figure 18), and then disable the microprocessor. In order to give the MPU adequate time to power down, the MPU Clock output remains active for a minimum of one reference counter cycle (about 200 µs) after the command is given to switch into the "Inactive" mode. An external timing circuit should be used to initiate the turn–on sequence. The "CD Out" pin has a dual function. In the Active and R_X modes it performs the carrier detect function. In the Standby and Inactive modes the carrier detect circuit is disabled and the "CD Out" pin is in a "High" state due to the external pull–up resistor. In the Inactive mode, the "CD Out" pin is the input for the hardware interrupt function. When the "CD Out" pin is pulled "low" by the external timing circuit, the combo IC switches from the Inactive to the Interrupt mode thereby turning on the MPU Clock Output. The MPU can then resume control of the combo IC. The "CD Out" pin must remain low until the MPU changes the operating mode from Interrupt to Standby, Active or R_X modes.

Figure 18. Hardware Interrupt Operation



MPU “Clk Out” Divider Programming

This pin is a clock output which is derived from the crystal oscillator (2nd local oscillator). It can be used to drive a microprocessor and thereby reduce the number of crystals required. Figure 19 shows the relationship between the crystal frequency and the clock output for different divider values. Figure 20 shows the “Clk Out” register bit values.

Figure 19. Clock Output Values

Crystal Frequency	Clock Output Divider			
	2	**3**	**4**	**5**
10.24 MHz	5.120 MHz	3.413 MHz	2.560 MHz	2.048 MHz
11.15 MHz	5.575 MHz	3.717 MHz	2.788 MHz	2.230 MHz
12.00 MHz	6.000 MHz	4.000 MHz	3.000 MHz	2.400 MHz

MPU “Clk Out” Radiated Noise on Circuit Board

The clock line running between the MC13111 and the microprocessor has the potential to radiate noise which can cause problems in the system especially if the clock is a square wave digital signal with large high frequency harmonics. In order to minimize radiated noise, a 1.0 kΩ resistor is included on–chip in series with the “Clk Out” output driver. A small capacitor can be connected to the “Clk Out” line on the PCB to form a single pole low pass filter. This filter will significantly reduce noise radiated from the “Clk Out” line.

Volume Control Programming

The volume control adjustable gain block can be programmed in 2.0 dB gain steps from –14 dB to +16 dB. The power–up default value is 0 dB. (See Figure 21.)

Figure 20. Clock Output Divider

Clk Out Bit #1	Clk Out Bit #0	Clk Out Divider Value
0	0	2
0	1	3
1	0	4
1	1	5

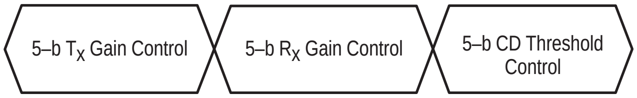
Figure 21. Volume Control

Volume Control Bit #3	Volume Control Bit #2	Volume Control Bit #1	Volume Control Bit #0	Volume Control #	Gain/Attenuation Amount
0	0	0	0	0	–14 dB
0	0	0	1	1	–12 dB
0	0	1	0	2	–10 dB
0	0	1	1	3	–8.0 dB
0	1	0	0	4	–6.0 dB
0	1	0	1	5	–4.0 dB
0	1	1	0	6	–2.0 dB
0	1	1	1	7	0 dB
1	0	0	0	8	2.0 dB
1	0	0	1	9	4.0 dB
1	0	1	0	10	6.0 dB
1	0	1	1	11	8.0 dB
1	1	0	0	12	10 dB
1	1	0	1	13	12 dB
1	1	1	0	14	14 dB
1	1	1	1	15	16 dB

Gain Control Register

The gain control register contains bits which control the T_X Voltage Gain, R_X Voltage Gain, and Carrier Detect threshold. Operation of these latch bits are explained in Figures 22, 23 and 24.

Figure 22. Gain Control Latch Bits



T_X and R_X Gain Programming

The T_X and R_X audio signal paths each have a programmable gain block. If a T_X or R_X voltage gain other than the nominal power–up default is desired, it can be programmed through the MPU interface. Alternately, these programmable gain blocks can be used during final test of the telephone to electronically adjust for gain tolerances in the telephone system as shown in Figure 23. In this case, the T_X and R_X gain register values should be stored in ROM during final test so that they can be reloaded each time the combo IC is powered up.

Figure 23. T_X and R_X Gain Control

Gain Control Bit #4	Gain Control Bit #3	Gain Control Bit #2	Gain Control Bit #1	Gain Control Bit #0	Gain Control #	Gain/Attenuation Amount
0	0	0	0	0	0	–15 dB
0	0	0	0	1	1	–14 dB
0	0	0	1	0	2	–13 dB
0	0	0	1	1	3	–12 dB
0	0	1	0	0	4	–11 dB
0	0	1	0	1	5	–10 dB
0	0	1	1	0	6	–9.0 dB
0	0	1	1	1	7	–8.0 dB
0	1	0	0	0	8	–7.0 dB
0	1	0	0	1	9	–6.0 dB
0	1	0	1	0	10	–5.0 dB
0	1	0	1	1	11	–4.0 dB
0	1	1	0	0	12	–3.0 dB
0	1	1	0	1	13	–2.0 dB
0	1	1	1	0	14	–1.0 dB
0	1	1	1	1	15	0 dB
1	0	0	0	0	16	1.0 dB
1	0	0	0	1	17	2.0 dB
1	0	0	1	0	18	3.0 dB
1	0	0	1	1	19	4.0 dB
1	0	1	0	0	20	5.0 dB
1	0	1	0	1	21	6.0 dB
1	0	1	1	0	22	7.0 dB
1	0	1	1	1	23	8.0 dB
1	1	0	0	0	24	9.0 dB
1	1	0	0	1	25	10 dB
1	1	0	1	0	26	11 dB
1	1	0	1	1	27	12 dB
1	1	1	0	0	28	13 dB
1	1	1	0	1	29	14 dB
1	1	1	1	0	30	15 dB
1	1	1	1	1	31	16 dB

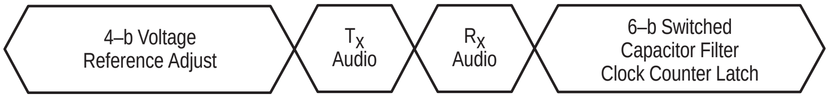
Carrier Detect Threshold Programming

The “CD Out” pin gives an indication to the microprocessor if a carrier signal is present on the selected channel. The nominal value and tolerance of the carrier detect threshold is given in the carrier detect specification section of this document. If a different carrier detect threshold value is desired, it can be programmed through the MPU interface as shown in Figure 24. Alternately, the carrier detect threshold can be electronically adjusted during final test of the telephone to reduce the tolerance of the carrier detect threshold. This is done by measuring the threshold and then by adjusting the threshold through the MPU interface. In this case, it is necessary to store the carrier detect register value in ROM so that the CD register can be reloaded each time the combo IC is powered up.

Figure 24. Carrier Detect Threshold Control

CD Bit #4	CD Bit #3	CD Bit #2	CD Bit #1	CD Bit #0	CD Control #	Carrier Detect Threshold
0	0	0	0	0	0	–20 dB
0	0	0	0	1	1	–19 dB
0	0	0	1	0	2	–18 dB
0	0	0	1	1	3	–17 dB
0	0	1	0	0	4	–16 dB
0	0	1	0	1	5	–15 dB
0	0	1	1	0	6	–14 dB
0	0	1	1	1	7	–13 dB
0	1	0	0	0	8	–12 dB
0	1	0	0	1	9	–11 dB
0	1	0	1	0	10	–10 dB
0	1	0	1	1	11	–9.0 dB
0	1	1	0	0	12	–8.0 dB
0	1	1	0	1	13	–7.0 dB
0	1	1	1	0	14	–6.0 dB
0	1	1	1	1	15	–5.0 dB
1	0	0	0	0	16	–4.0 dB
1	0	0	0	1	17	–3.0 dB
1	0	0	1	0	18	–2.0 dB
1	0	0	1	1	19	–1.0 dB
1	0	1	0	0	20	0 dB
1	0	1	0	1	21	1.0 dB
1	0	1	1	0	22	2.0 dB
1	0	1	1	1	23	3.0 dB
1	1	0	0	0	24	4.0 dB
1	1	0	0	1	25	5.0 dB
1	1	0	1	0	26	6.0 dB
1	1	0	1	1	27	7.0 dB
1	1	1	0	0	28	8.0 dB
1	1	1	0	1	29	9.0 dB
1	1	1	1	0	30	10 dB
1	1	1	1	1	31	11 dB

Figure 25. SCF Clock Divider Latch Bits



SCF Clock Divider

This register controls the divider value for the programmable switched capacitor filter clock divider and the voltage reference adjust. Operation is explained in Figures 25 through 30.

Figure 26. Audio Mode Bit Description

T_X Mode	1 0	Normal T_X Path Operation Undefined State
R_X Mode	1 0	Normal R_X Path Operation Undefined State

NOTES: Power–up bit default mode is “0”. Must change bit to “1” for proper operation.

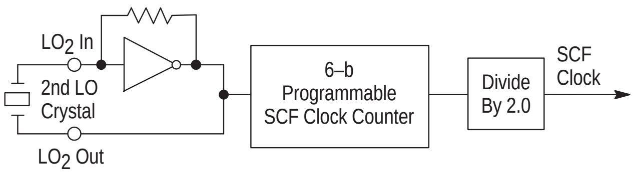
Switched Capacitor Filter Clock Programming

A block diagram of the switched capacitor filter clock dividers is shown in Figure 27. There is a fixed divide by 2 after the programmable divider. The switched capacitor filter clock value is given by the following equation;

$$(\text{SCF Clock}) = F(\text{2nd LO})/(\text{SCF Divider Value} * 2)$$

The SCF divider should be set to a value which gives a SCF Clock as close to 165.16 kHz as possible based on the 2nd LO frequency which is chosen (see Figure 12).

Figure 27. SCF Clock Circuit



Corner Frequency Programming

Four different corner frequencies may be selected by programming the SCF Clock divider as shown in Figures 28 and 29. Note that all filter corner frequencies change proportionately with the SCF Clock Frequency. The power–up default SCF Clock divider is 31.

Figure 28. Corner Frequency Programming for a 10.240 MHz 2nd LO

SCF Clock Divider	Total Divide Value	SCF Clock Freq. (kHz)	R_X Upper Corner Frequency (kHz)	T_X Upper Corner Frequency (kHz)
29	58	176.55	4.147	3.955
30	60	170.67	4.008	3.823
31	62	165.16	3.879	3.700
32	64	160.00	3.758	3.584

NOTE: All filter corner frequencies have a tolerance of ±3%.

Figure 29. Corner Frequency Programming for a 11.15 MHz 2nd LO

SCF Clock Divider	Total Divide Value	SCF Clock Freq. (kHz)	R_X Upper Corner Frequency (kHz)	T_X Upper Corner Frequency (kHz)
32	64	174.22	4.092	3.903
33	66	168.94	3.968	3.785
34	68	163.97	3.851	3.673
35	70	159.29	3.741	3.568

NOTE: All filter corner frequencies have a tolerance of ±3%.

Voltage Reference Adjustment

The internal 1.5 V Bandgap voltage reference provides the voltage reference for the “BD1 Out” and “BD2 Out” low battery detect circuits, the “PLL V_{ref}” voltage regulator, the “V_B” reference, and all internal analog ground references. The initial tolerance of the Bandgap voltage reference is ±6%. The tolerance of the internal reference voltage can be improved to ±1.5% through MPU serial interface programming.

During final test of the telephone, the battery detect threshold is measured. Then, the internal reference voltage value is adjusted electronically through the MPU serial interface to achieve the desired accuracy level. The voltage reference register value should be stored in ROM during final test so that it can be reloaded each time the MC13111 is powered up (see Figure 30).

Figure 30. Bandgap Voltage Reference Adjustment

V_{ref} Adj. Bit #3	V_{ref} Adj. Bit #2	V_{ref} Adj. Bit #1	V_{ref} Adj. Bit #0	V_{ref} Adj. #	V_{ref} Adj. Amount
0	0	0	0	0	–9.0%
0	0	0	1	1	–7.8%
0	0	1	0	2	–6.6%
0	0	1	1	3	–5.4%
0	1	0	0	4	–4.2%
0	1	0	1	5	–3.0%
0	1	1	0	6	–1.8%
0	1	1	1	7	–0.6%
1	0	0	0	8	+0.6 %
1	0	0	1	9	+1.8 %
1	0	1	0	10	+3.0 %
1	0	1	1	11	+4.2 %
1	1	0	0	12	+5.4 %
1	1	0	1	13	+6.6 %
1	1	1	0	14	+7.8 %
1	1	1	1	15	+9.0 %

Auxiliary Register

The auxiliary register contains a 3–bit 1st LO Capacitor Selection latch and a 4–bit Test Mode latch. Operation of these latch bits are explained in Figures 31, 32 and 34.

Figure 31. Auxiliary Register Latch Bits

First Local Oscillator Programmable Selection (U.S. Applications)

There is a very large frequency difference between the minimum and maximum channel frequencies in the 25 Channel U.S. Standard.The sensitivity of the 1st LO may not be large enough to accommodate this large frequency variation. Fixed capacitors can be connected across the 1st LO tank circuit to change the 1st LO sensitivity. Internal switches and capacitors are provided to enable microprocessor control over internal fixed capacitor values. Figures 32 and 33 show the schematic representation of the 1st LO and the tank circuit. Figure 34 shows the latch control bit values for microprocessor control.

Figure 32. First Local Oscillator Schematic

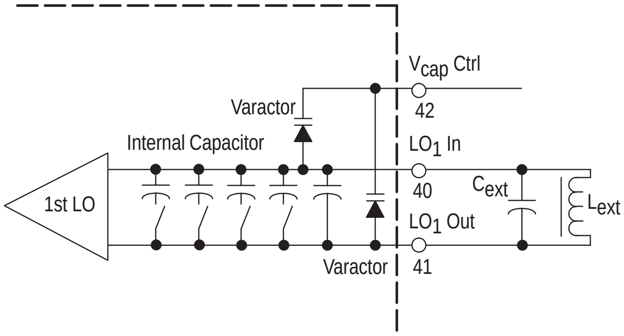


Figure 33. First Local Oscillator Simplified Schematic

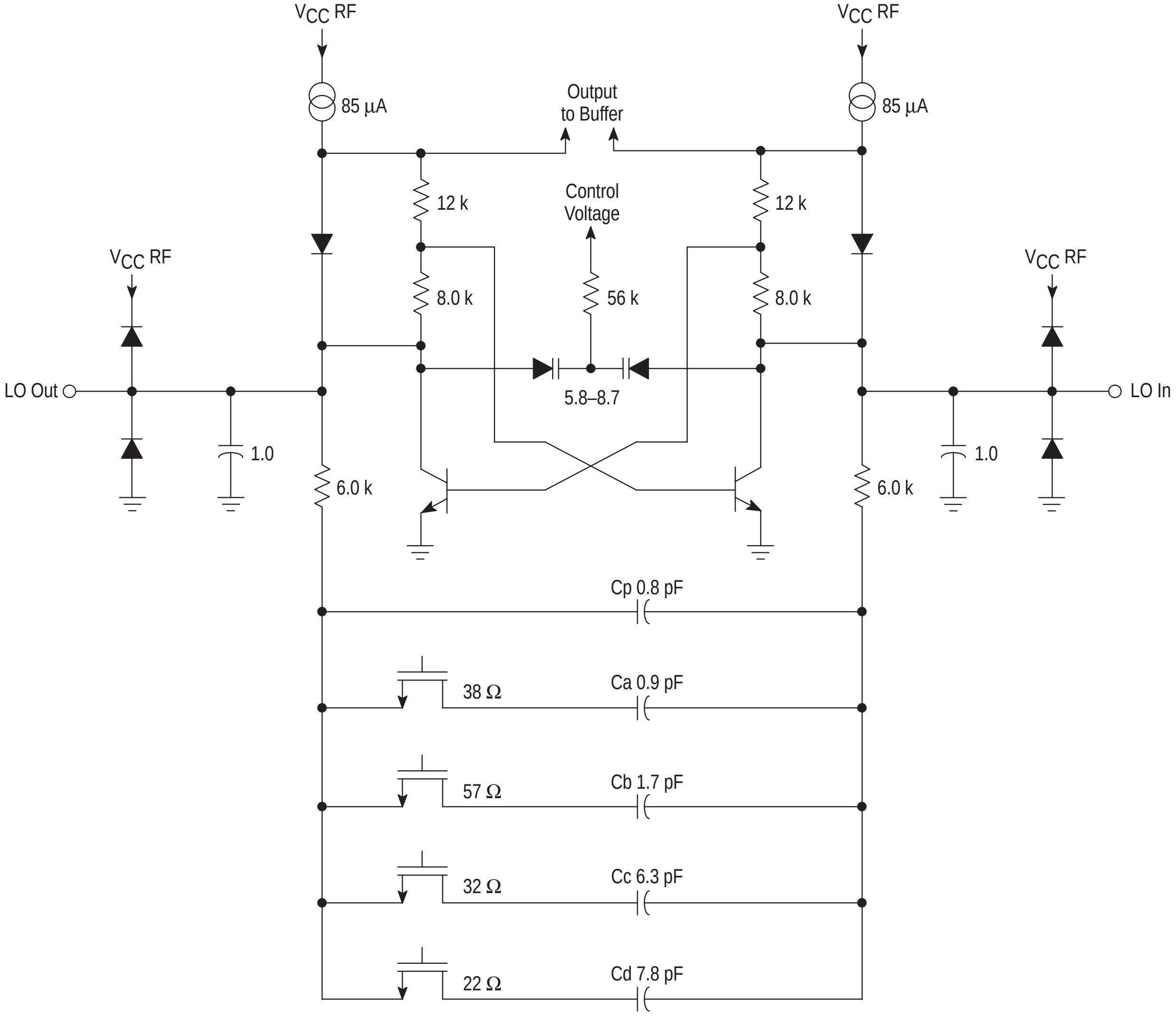


Figure 34. First Local Oscillator Programmable Capacitor Selection for U.S. 25 Channels

1st LO Cap. Bit 2	1st LO Cap. Bit 1	1st LO Cap Bit 0	1st LO Cap. Select	U.S. Base Chan-nels	U.S. Handset Channels	Internal Capacitor Value	Varactor Value over 0.3 to 2.5 V	Equivalent Internal Parallel Resistance at 40 MHz (kΩ)	Equivalent Internal Parallel Resistance at 51 MHz (kΩ)	External Capacitor Value	External Inductor Value
0	0	0	0	1–10	–	0.8 pF	5.8–8.7 pF	>1000	>1000	24 pF	0.47 µH
0	0	0	0	–	1–10	0.8 pF	5.8–8.7 pF	>1000	>1000	33 pF	0.47 µH
0	0	1	1	11–16	–	2.5 pF	5.8–8.7 pF	35	21	24 pF	0.47 µH
0	1	0	2	17–25	–	1.7 pF	5.8–8.7 pF	100	60	24 pF	0.47 µH
0	1	1	3	–	11–16	8.6 pF	5.8–8.7 pF	6.1	3.8	33 pF	0.47 µH
1	0	0	4	–	17–25	7.1 pF	5.8–8.7 pF	8.0	5.0	33 pF	0.47 µH

Figure 35. Digital Test Mode Description

TM #	TM 3	TM 2	TM 1	TM 0	Counter Under Test or Test Mode Option	“T_X V_{CO}” Input Signal	“Clk Out” Output Expected
0	0	0	0	0	Normal Operation	>200 mVpp	–
1	0	0	0	1	R_X Counter, upper 6	0 to 2.5 V	Input Frequency/64
2	0	0	1	0	R_X Counter, lower 8	0 to 2.5 V	See Note Below
3	0	0	1	1	R_X Prescaler	0 to 2.5 V	Input Frequency/4
4	0	1	0	0	T_X Counter, upper 6	0 to 2.5 V	Input Frequency/64
5	0	1	0	1	T_X Counter, lower 8	0 to 2.5 V	See Note Below
6	0	1	1	0	T_X Prescaler	>200 mVpp	Input Frequency/4
7	0	1	1	1	Reference Counter	0 to 2.5 V	Input Frequency/Reference Counter Value
8	1	0	0	0	Divide by 4, 25	0 to 2.5 V	Input Frequency/100
9	1	0	0	1	SC Counter	0 to 2.5 V	Input Frequency/SC Counter Value
10	1	0	1	0	Not Used	N/A	–

NOTE: To determine the correct output, look at the lower 8–bits in the R_X or T_X register (Divisor (7;0). If the value of the divisor is > 16, then the output divisor value is Divisor (7;2) (the upper 6–bits of the divisor). If Divisor (7;0) < 16 and Divisor (3;2) > = 2, then output divisor value is Divisor (3;2) (bits 2 and 3 of the divisor). If Divisor (7;0) < 16 and Divisor (3;2) < 2, then output divisor value is (Divisor (3;2) + 60).

Figure 36. Analog Test Mode Description

TM #	TM 3	TM 2	TM 1	TM 0	Circuit Blocks Under Test	Input Pin	Output Pin
11	1	0	1	1	Compressor	C In	T_X In
12	1	1	0	0	Not Used	N/A	N/A
13	1	1	0	1	ALC Gain = 10 Option	N/A	N/A
14	1	1	1	0	ALC Gain = 25 Option	N/A	N/A
15	1	1	1	1	Not Used	N/A	N/A

Test Modes

Digital and analog test modes can be selected through the 4–bit Test Mode Register. In digital test mode, the “T_X V_{CO}” input pin is multiplexed to the input of the counter under test and the output of the counter under test is multiplexed to the “Clk Out” output pin so that each counter can be individually tested. Make sure test mode bits are set to “0’s” for normal operation. Digital test mode operation is described in Figure 35. During normal operation and when testing the T_X Prescaler, the “T_X VCO” input can be a minimum of 200 mVpp at 80 MHz and should be ac–coupled. For other test modes, input signals should be standard logic levels of 0 to 2.5 V and a maximum frequency of 16 MHz.

The analog test modes enable separate testing of the Compressor blocks as shown in Figure 36. Also, ALC Gain options can be selected through analog test modes.

Power–Up Defaults for Control and Counter Registers

When the IC is first powered up, all latch registers are initialized to a defined state. The device is initially placed in the Rx mode with all mutes active. The reference counter is set to generate a 5.0 kHz reference frequency from a 10.24 MHz crystal. The switched capacitor filter clock counter is set properly for operation with a 10.24 MHz crystal. The audio mode will come up in an undefined state and must be set to a bit format shown in Figure 26 for proper operation. The T_X and R_X latch registers are set for USA Channel Frequency 21 (Channel 6 for previous FCC 10 Channel Band). Figure 37 shows the initial power–up states for all latch registers.

Figure 37. Latch Register Power–Up Defaults

Register	Count	MSB								LSB							
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
T_X	9966	–	–	1	0	0	1	1	0	1	1	1	0	1	1	1	0
R_X	7215	–	–	0	1	1	1	0	0	0	0	1	0	1	1	1	1
Ref	2048	–	–	0	0	1	0	0	0	0	0	0	0	0	0	0	0
Mode	N/A	–	0	X	0	0	1	1	0	1	1	1	0	1	1	1	1
Gain	N/A	–	0	1	1	1	1	0	1	1	1	1	1	0	1	0	0
SC	31	–	–	–	–	0	1	1	1	0	0	0	1	1	1	1	1
Aux	N/A	–	–	–	–	–	–	–	–	–	0	0	0	0	0	0	0

NOTE: Bits 6 and 7 in the SC latch register must be set to “1” after power–up for proper operation.

APPLICATIONS INFORMATION

Evaluation PC Board

The PCB should be double sided with a full ground plane on one side; any leaded components are inserted on the ground plane side. This affords shielding and isolation from the circuit side of the PCB. The other side is the circuit side which has the interconnect traces and the surface mount components. In cases where cost allows, it may be benificial to use multi layer boards.

The placement of certain components specified in the application circuits is very critical. These components should be placed first and the other less critical components are fitted in last. In general, all RF paths should be kept as short as possible, ground pins should be grounded at the pins and V_{CC} pins should have adequate decoupling to ground at the pins. In mixed mode systems where digital and RF/Analog circuitry are present, the V_{EE} and V_{CC} busses are isolated ac –wise from each other.

Component Selection

The evaluation PC board is designed to accommodate specific components, while in some cases it is versatile enough to use components from various manufacturers and coil types. The application circuit schematics specify particular components that were used to achieve the results shown in the typical curves and tables, but alternate components should give similar results.

The MC13111 IC is capable of matching the sensitivity, IMD, adjacent channel rejection, and other performance criteria of a multi–chip analog cordless telephone system. For the most part, the same external components are used as in the multi–chip solution. In the following discussion, various parts of the system are analyzed for best peformance and cost tradeoffs. Specific recommendations are made where certain components or circuit designs offer superior performance. The system analyzed is the USA “CT–1” cordless phone. (CT–0 is a similar cordless application in Europe.)

Input Matching/Sensitivity

The sensitivity of the IC is typically 0.56 µVrms matched with no preamp. To achieve suitable system performance, a preamp and passive duplexer must be used. In production final test, each section of the IC is separately tested to guarantee its system performance in the specific application. The preamp and duplexer (differential, matched input) yields typically –114 dBm 12 dB SINAD sensitivity performance under full duplex operation.

The duplexer is important to achieve full duplex operation without significant “de–sensing” of the receiver by the transmitter. The combination of the duplexer and preamp circuit will attenuate the transmitter power to the receiver by over 60 dB. This will improve the receiver system noise figure without giving up too much IMD intermodulation performance.

The duplexer may be a single piece unit offered by Shimida and Sansui products (designed for 10 channel CT–1 cordless phone) or a two piece solution offered by Toko (designed for 25 channel operation). The duplexer frequency response at the receiver port has a notch at the transmitter frequency band of about 35 to 40 dB with a 2.0 to 3.0 dB insertion loss at the receiver frequency band.

The preamp circuit utilizes a tuned transformer at the output side of the amplifier. This transformer is designed to bandpass filter at the receiver input frequency while rejecting the transmitter frequency. The tuned preamp also improves the noise performance by reducing the bandwidth of the pass band and reducing the second stage contribution of the 1st mixer. The preamp is biased at about 1.0 mA and 3.0 Vdc which yields suitable noise figure and gain.

Mixers

The 1st and 2nd mixers are similar in design. Both are double balanced to suppress the LO and the input frequencies to give only the sum and difference frequencies out. Typically the LO is suppressed about 40 to 60 dB. The 1st mixer may be driven either differentially or single ended. The gain of the 1st mixer has a 3.0 dB corner at 20 MHz and is used at a 10.7 MHz IF. It has an output impedance of 330 Ω and matches to a typical 10.7 MHz ceramic filter with a source and load impedance of 330 Ω. A series resistor may be used to raise the impedance for use with crystal filters which typically have an input impedance much greater than 330 Ω. The 2nd mixer input impedance is typically 3.0 kΩ; it requires an external 360 Ω parallel resistor for use with a standard 330 Ω 10.7 MHz ceramic filter. The second mixer output impedance is 1.5 kΩ making it suitable to match 455 kHz ceramic filters.

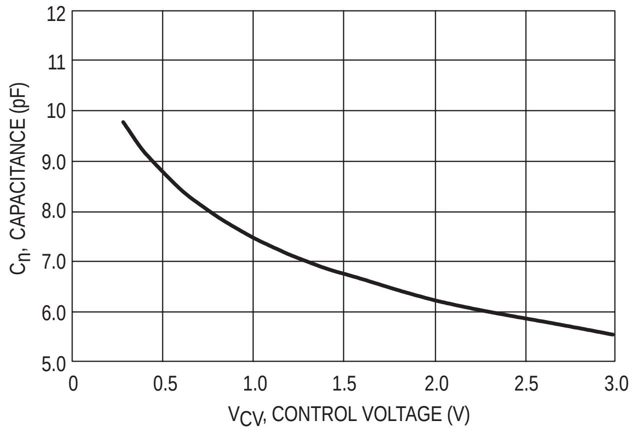
The following table is a list of typical input impedances over frequency for the 1st Mixer. R_P and C_P are represented in parallel form.

Frequency (MHz)	R_P (Ω)	C_P (pF)
20	977.7	2.44
25	944.3	2.60
30	948.8	2.65
35	928	2.55
40	900	2.51
45	873.4	2.65
50	859.3	2.72
55	821	2.72
60	795	2.74

First Local Oscillator

The 1st LO is a multi–vibrator oscillator that takes an external capacitance and inductance. It is voltage controlled to an internal varactor from an external loop filter and an on–board phase–lock loop (PLL). The schematic in Figure 33 shows all the basic parasitic elements of the internal circuitry. The 1st LO internal component values have a tolerance of 15%. A typical dc bias level on the LO Input and LO Output is 0.45 Vdc. The temperature coefficient of the varactor is +0.09%/°C. The curve in Figure 38 is the varactor control voltage range as it relates to capacitance. It represents the expected capacitance for a given control voltage of the MC13111.

Figure 38. First Local Oscillator Varacter versus Control Voltage



Second Local Oscillator

The 2nd LO is a CMOS oscillator similar to that used in the MC145162. The 2nd LO is also used as the PLL reference oscillator. It is designed to utilize an external parallel resonant crystal.

PLL Design

The 1st LO level is important, as well as the choice of the crystal for the PLL clock reference and 2nd LO. A fundamental, parallel resonant crystal specified with 7.0 to 12 pF load calibration capacitance is recommended. If the load calibration capacitance is too high, the crystal locks up very slowly. If the LO power is less than –10 dBm, a pull–down resistor at the 1st LO emitter (Pin 41) will increase its drive level. The LO level is primarily a function of the Colpitts capacitive voltage divider formed by the capacitors between the base to emitter and the emitter to ground.

The VCO gain factor expressed in MHz/V is indeed critical to the phase noise performance. If this curve is too steep or too sensitive to changes in control voltage, it may degrade the phase noise performance. The external VCO circuit design needs to consider the typical swing of the control voltage and the corresponding linearity of the transfer function, $\Delta f_{osc}/\Delta V_{control}$. In general, the higher the Q of the VCO circuit inductor, the better phase noise performance.

Adjacent channel rejection and isolation between the 1st and 2nd mixers may be adversely affected due to layout problems and difficulty in getting up close to the package pins with the grounds and decoupling capacitors on the RF V_{CC}. These system parameters must be evaluated for sensitivity to layout and external component placement.

Intermodulation and adjacent channel performance problems may also result from spurs around the 1st LO. This may be caused by harmonics from the switched capacitor clock driver and too low 1st LO drive level. The clock driver operates at a frequency which is f(2nd LO)/(2 * (SCF Divider)). The harmonics are n * (f(2nd LO)), where n can be any positive integer. The current spikes of the SCF on the supply lines cause the disturbance of the 1st LO. This may be verified by observing the spurs on a spectrum analyzer while changing the clock divider value. The spur frequencies will change when the divider value is changed. The spurious sideband problem may be avoided by changing the clock divider value via software for each channel where it is a problem. Certain channels are worse than others. Refer to the MC145162 data sheet for PLL design example.

Limiting IF Amplifiers

The limiting IF amplifier typically has about 110 dB of gain; the frequency response starts rolling off at 1.0 MHz. Decoupling capacitors should be placed close to Pins 31 and 32 to ensure low noise and stable operation. The IF input impedance is 1.5 kΩ for a suitable match to 455 kHz ceramic filters.

RSSI/Carrier Detect

The Received Signal Strength Indicator (RSSI) indicates the strength of the IF level and the output is proportional to the logarithm of the IF input signal magnitude. The RSSI dynamic range is typically 80 dB. Connect 0.01 µF to GND from “RSSI” output pin to form the carrier detect filter. A resistor needed to convert the RSSI current to voltage is included in the internal circuit. An internal temperature compensated reference current also improves the RSSI accuracy over temperature.

“CD Out” is an open collector output; thus, an external 100 kΩ pull–up resistor to V_{CC} is recommended. The carrier detect threshold is programmable through the MPU interface.

Quadrature Detector

The quadrature detector is coupled to the IF with an external capacitor between Pins 27 and 28; thus, the recovered signal level output is increased for a given bandwidth by increasing the capacitor. The external quadrature component may be either a LCR resonant circuit, which may be adjustable, or a ceramic resonator which is usually fixed tuned.

The bandwidth performance of the detector is controlled by the loaded Q of the LC tank circuit. The following equation defines the components which set the detector circuit's bandwidth:

(1) $R_T = Q\,X_L$

where R_T is the equivalent shunt resistance across the LC Tank. X_L is the reactance of the quadrature inductor at the IF frequency ($X_L = 2\pi fL$).

Specific 455 kHz quadrature LC components are manufactured by Toko in various 5 mm, 7 mm and 10 mm shielded cans in surface mount or leaded packages. Recommended components such as, the 7 mm Toko, is used in the application circuit. When minaturization is a key constraint, a surface mount inductor and capacitor may be chosen to form a resonant LC tank with the PCB and parasitic device capacitance. The 455 kHz IF center frequency is calculated by

(2) $f_c = [2\pi\,(LC_p)^{1/2}] - 1$

where L is the parallel tank inductor. C_p is the equivalent parallel capacitance of the parallel resonant tank circuit.

The following is a design example for a detector at 455 kHz and a specific loaded Q. The loaded Q of the quadrature detector is chosen somewhat less than the Q of the IF bandpass. For an IF frequency of 455 kHz and an IF bandpass of 20 kHz, the IF bandpass Q is approximately 23; the loaded Q of the quadrature tank is chosen at 15.

Example:

Let the total external C = 180 pF. Note: the capacitance may be split between a 150 pF chip capacitor and a 5.0 to 25 pF variable capacitor; this allows for tuning to compensate for component tolerance. Since the external capacitance is much greater than the internal device and PCB parasitic capacitance, the parasitic capacitance may be neglected.

Rewrite equation (2) and solve for L:

$L = (0.159)^2/(C\,fc^2)$
$L = 678\ \mu H$; Thus, a standard value is chosen:
$L = 680\ \mu H$ (surface mount inductor)

The value of the total damping resistor to obtain the required loaded Q of 15 can be calculated from equation (1):

$R_T = Q(2\pi fL)$
$R_T = 15\ (2\pi)(0.455)(680) = 29.5\ k\Omega$

The internal resistance, R_{int} at the quadrature tank Pin 27 is approximately 100 kΩ and is considered in determining the external resistance, R_{ext} which is calculated from

$R_{ext} = ((R_T)(R_{int}))/(R_{int} - R_T)$
$R_{ext} = 41.8\ k\Omega$; Thus, choose the standard value:
$R_{ext} = 39\ k\Omega$

A ceramic discriminator is recommended for the quadrature circuit in applications where fixed tuning is desired. The ceramic discriminator and a 22 k resistor are placed from Pin 27 to V_{CC}. A 10 pF capacitor is placed from Pin 28 to 27 to properly drive the discriminator.

MuRata Erie has designed a resonator that is compatible with the IC. For US applications the part number is CDBM455C48. For Europe the part number is CDBM450C48. Contact Motorola Analog Marketing for performance data using muRata's parts.

APPENDIX A – APPLICATIONS CIRCUIT

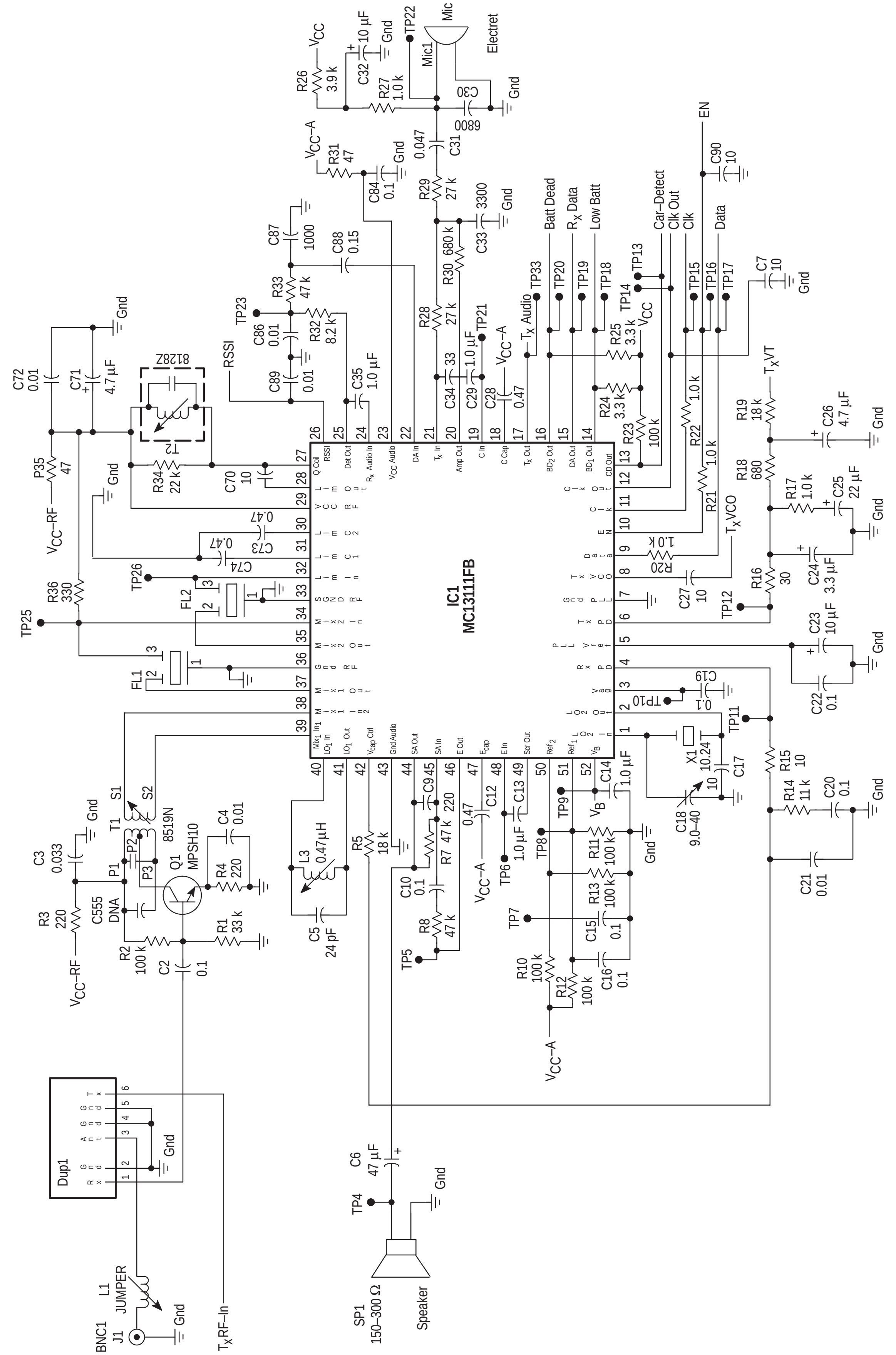
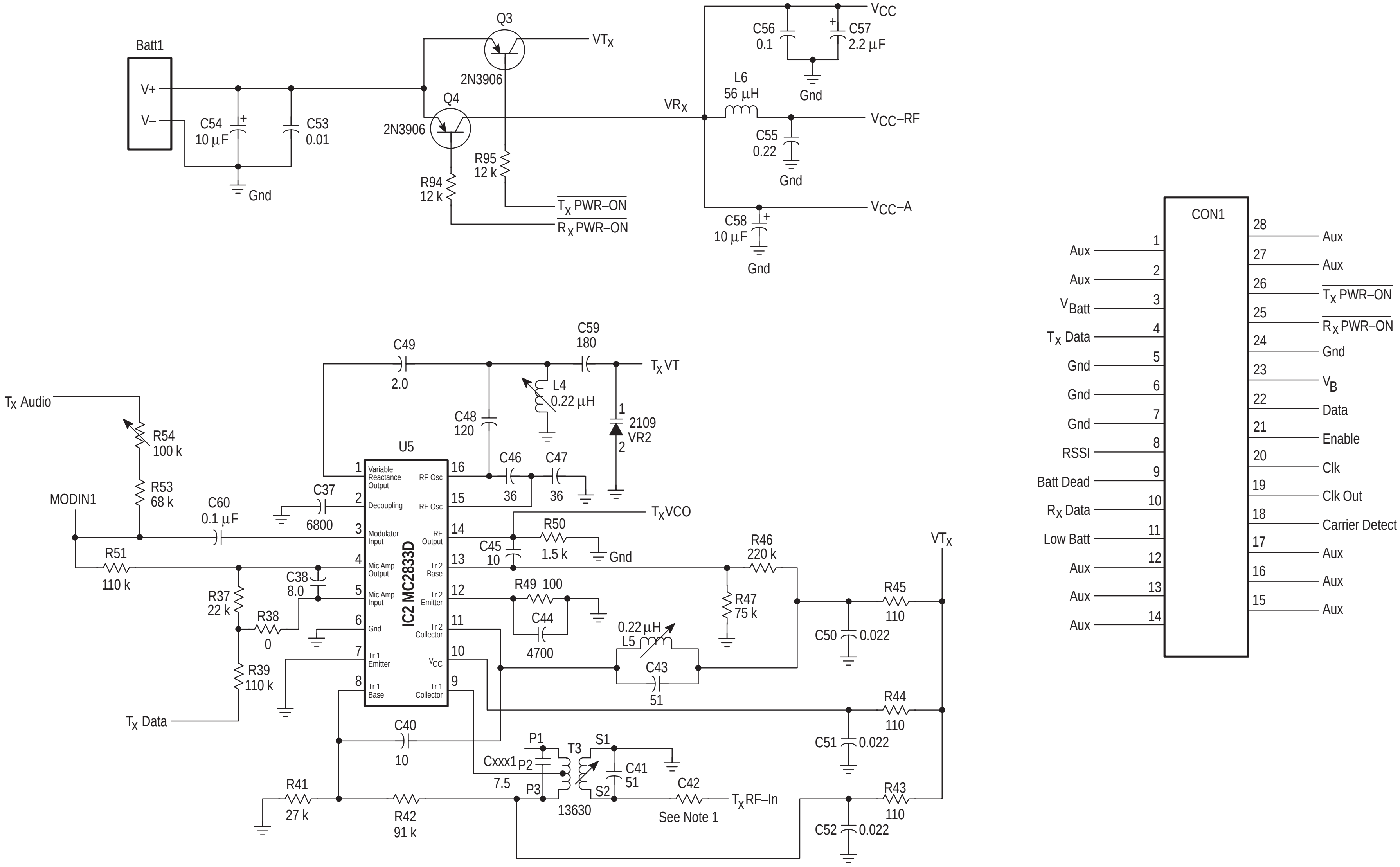


Figure 39a. Baseset RF Applications Circuit

Figure 39a. Baseset RF Applications Circuit (continued)



NOTE 1: C42 = X42 = 51 Ω

APPENDIX B – MC13111 APPLICATION BOARD BILL OF MATERIAL (USA)

Reference	Description	Value	Package	Part Number	Vendor
X1	10.24 Crystal (Load Cap <12 pF)	–	HC49US	AAL10M240000FLE10A	Standard Crystal
VR2	Diode	–	Sot23	MMBV2109LT1	Motorola
DUP1	Duplexer (25 Channel)	Baseset	Hybrid	DPX1035 75B–153B	Sumida
DUP1	Duplexer (25 Channel)	Handset	Hybrid	DPX1035 75B–154B	Sumida
FL1	10.7 MHz Filter (Red Dot)	–	–	SFE10.7MS2–A	muRata
FL2	455 kHz Filter	–	–	CFU455E2	muRata
IC1	Universal Cordless Telephone IC	–	QFP	MC13111FB	Motorola
IC2	FM Transmitter IC	–	SO–16	MC2833D	Motorola
L3	Inductor	0.47 µH	Can	292SNS–T1370Z	Toko
L4/L5	Inductor	0.22 µH	Can	292SNS–T1368Z	Toko
T1/T3	Transformer	–	Can	600GCS–8519N	Toko
T2	Quadrature Coil	–	Can	7MCS–8128Z	Toko
Q1	Transistor	–	TO–92	MPSH10	Motorola
Q3	Transistor	–	TO–92	2N3906	Motorola
Q4	Transistor	–	TO–92	2N3906	Motorola

NOTE: Components for the Handset and Baseset are the same, except where noted on the Bill of Material and Schematic.

APPENDIX C – MEASUREMENT OF COMPANDOR ATTACK/DECAY TIME

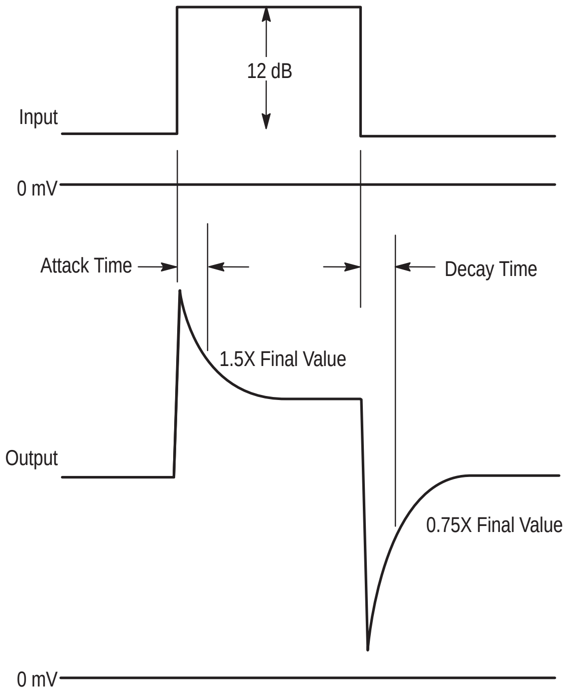
This measurement definition is based on EIA/CCITT recommendations.

Compressor Attack Time

For a 12 dB step up at the input, attack time is defined as the time for the output to settle to 1.5X of the final steady state value.

Compressor Decay Time

For a 12 dB step down at the input, decay time is defined as the time for the input to settle to 0.75X of the final steady state value.

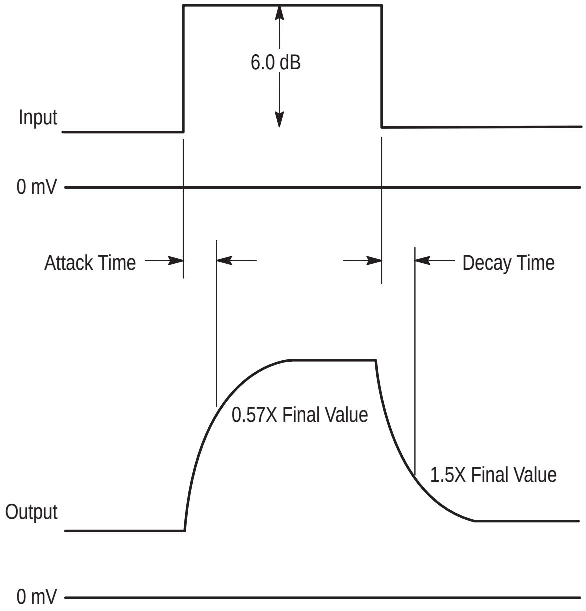


Expandor Attack

For a 6.0 dB step up at the input, attack time is defined as the time for the output to settle to 0.57X of the final steady state value.

Expandor Decay

For a 6.0 dB step down at the input, decay time is defined as the time for the output to settle to 1.5X of the final steady state value.



MOTOROLA

FM Communications Receivers

MC13135
MC13136

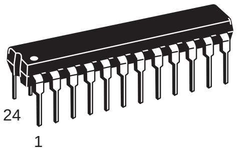
The MC13135/MC13136 are the second generation of single chip, dual conversion FM communications receivers developed by Motorola. Major improvements in signal handling, RSSI and first oscillator operation have been made. In addition, recovered audio distortion and audio drive have improved. Using Motorola's MOSAIC™ 1.5 process, these receivers offer low noise, high gain and stability over a wide operating voltage range.

Both the MC13135 and MC13136 include a Colpitts oscillator, VCO tuning diode, low noise first and second mixer and LO, high gain limiting IF, and RSSI. The MC13135 is designed for use with an LC quadrature detector and has an uncommitted op amp that can be used either for an RSSI buffer or as a data comparator. The MC13136 can be used with either a ceramic discriminator or an LC quad coil and the op amp is internally connected for a voltage buffered RSSI output.

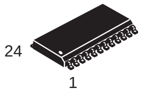
These devices can be used as stand–alone VHF receivers or as the lower IF of a triple conversion system. Applications include cordless telephones, short range data links, walkie–talkies, low cost land mobile, amateur radio receivers, baby monitors and scanners.

- Complete Dual Conversion FM Receiver – Antenna to Audio Output
- Input Frequency Range – 200 MHz
- Voltage Buffered RSSI with 70 dB of Usable Range
- Low Voltage Operation – 2.0 to 6.0 Vdc (2 Cell NiCad Supply)
- Low Current Drain – 3.5 mA Typ
- Low Impedance Audio Output < 25 Ω
- VHF Colpitts First LO for Crystal or VCO Operation
- Isolated Tuning Diode
- Buffered First LO Output to Drive CMOS PLL Synthesizer

DUAL CONVERSION NARROWBAND FM RECEIVERS



P SUFFIX
PLASTIC PACKAGE
CASE 724

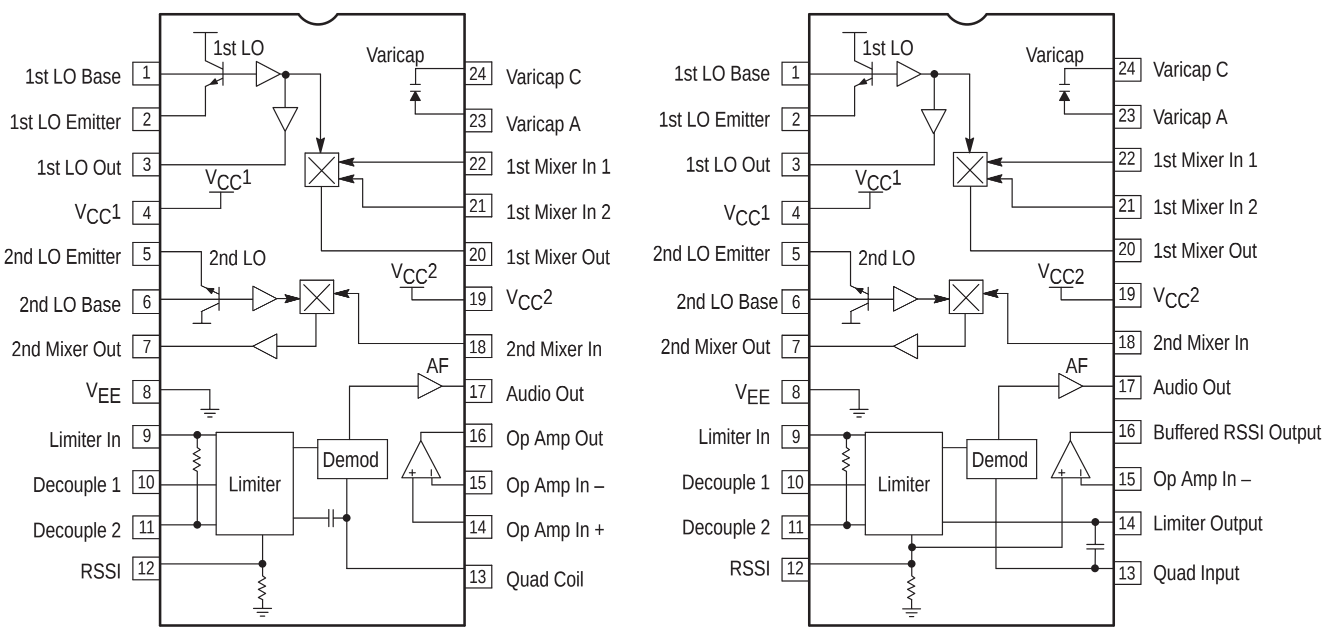


DW SUFFIX
PLASTIC PACKAGE
CASE 751E
(SO–24L)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC13135P	T_A = – 40° to +85°C	Plastic DIP
MC13135DW		SO–24L
MC13136P		Plastic DIP
MC13136DW		SO–24L

PIN CONNECTIONS


MC13135 MC13136

Each device contains 142 active transistors.

MAXIMUM RATINGS

Rating	Pin	Symbol	Value	Unit
Power Supply Voltage	4, 19	V_{CC} (max)	6.5	Vdc
RF Input Voltage	22	RF_{in}	1.0	Vrms
Junction Temperature	–	T_J	+150	°C
Storage Temperature Range	–	T_{stg}	– 65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

Rating	Pin	Symbol	Value	Unit
Power Supply Voltage	4, 19	V_{CC}	2.0 to 6.0	Vdc
Maximum 1st IF	–	f_{IF1}	21	MHz
Maximum 2nd IF	–	f_{IF2}	3.0	MHz
Ambient Temperature Range	–	T_A	– 40 to + 85	°C

ELECTRICAL CHARACTERISTICS

(T_A = 25°C, V_{CC} = 4.0 Vdc, f_o = 49.7 MHz, f_{MOD} = 1.0 kHz, Deviation = ±3.0 kHz, $f_{1st\,LO}$ = 39 MHz, $f_{2nd\,LO}$ = 10.245 MHz, IF1 = 10.7 MHz, IF2 = 455 kHz, unless otherwise noted. All measurements performed in the test circuit of Figure 1.)

Characteristic	Condition	Symbol	Min	Typ	Max	Unit
Total Drain Current	No Input Signal	I_{CC}	–	4.0	6.0	mAdc
Sensitivity (Input for 12 dB SINAD)	Matched Input	V_{SIN}	–	1.0	–	µVrms
Recovered Audio	V_{RF} = 1.0 mV	AF_O				mVrms
MC13135			170	220	300	
MC13136			215	265	365	
Limiter Output Level (Pin 14, MC13136)		V_{LIM}	–	130	–	mVrms
1st Mixer Conversion Gain	V_{RF} = – 40 dBm	MX_{gain1}	–	12	–	dB
2nd Mixer Conversion Gain	V_{RF} = – 40 dBm	MX_{gain2}	–	13	–	dB
First LO Buffered Output	–	V_{LO}	–	100	–	mVrms
Total Harmonic Distortion	V_{RF} = – 30 dBm	THD	–	1.2	3.0	%
Demodulator Bandwidth	–	BW	–	50	–	kHz
RSSI Dynamic Range	–	RSSI	–	70	–	dB
First Mixer 3rd Order Intercept (Input)		TOI_{Mix1}				dBm
	Matched		–	–17	–	
	Unmatched		–	–11	–	
Second Mixer 3rd Order Intercept (RF Input)	Matched Input	TOI_{Mix2}	–	– 27	–	dBm
First LO Buffer Output Resistance	–	R_{LO}	–	–	–	Ω
First Mixer Parallel Input Resistance	–	R	–	722	–	Ω
First Mixer Parallel Input Capacitance	–	C	–	3.3	–	pF
First Mixer Output Impedance	–	ZO	–	330	–	Ω
Second Mixer Input Impedance	–	Z_I	–	4.0	–	kΩ
Second Mixer Output Impedance	–	ZO	–	1.8	–	kΩ
Detector Output Impedance	–	ZO	–	25	–	Ω

TEST CIRCUIT INFORMATION

Although the MC13136 can be operated with a ceramic discriminator, the recovered audio measurements for both the MC13135 and MC13136 are made with an LC quadrature detector. The typical recovered audio will depend on the external circuit; either the Q of the quad coil, or the RC matching network for the ceramic discriminator. On the MC13136, an external capacitor between Pins 13 and 14 can be used with a quad coil for slightly higher recovered audio. See Figures 10 through 13 for additional information.

Since adding a matching circuit to the RF input increases the signal level to the mixer, the third order intercept (TOI) point is better with an unmatched input (50 Ω from Pin 21 to Pin 22). Typical values for both have been included in the Electrical Characterization Table. TOI measurements were taken at the pins with a high impedance probe/spectrum analyzer system. The first mixer input impedance was measured at the pin with a network analyzer.

Figure 1a. MC13135 Test Circuit

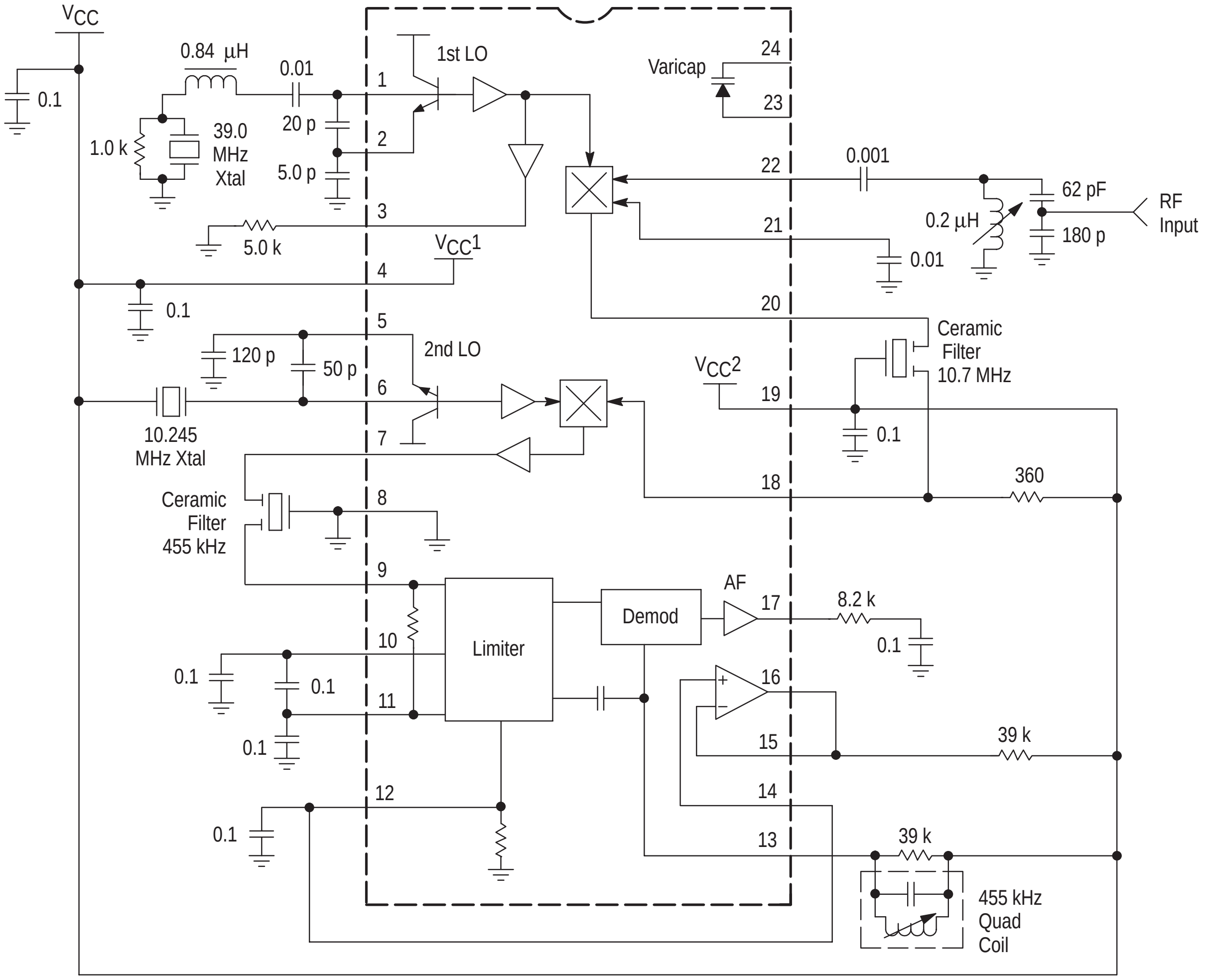


Figure 1b. MC13136 Quad Detector Test Circuit

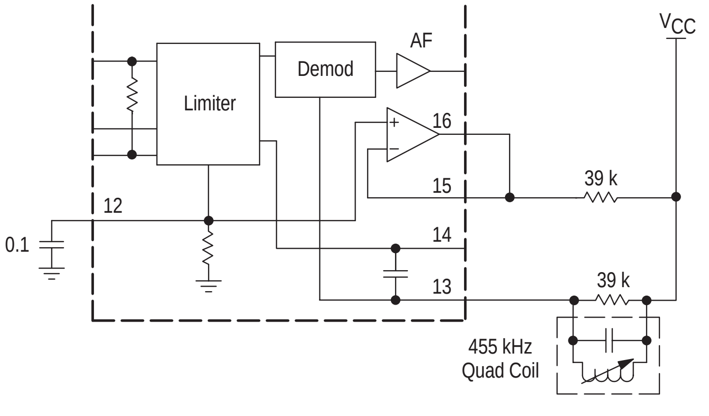


Figure 2. Supply Current versus Supply Voltage

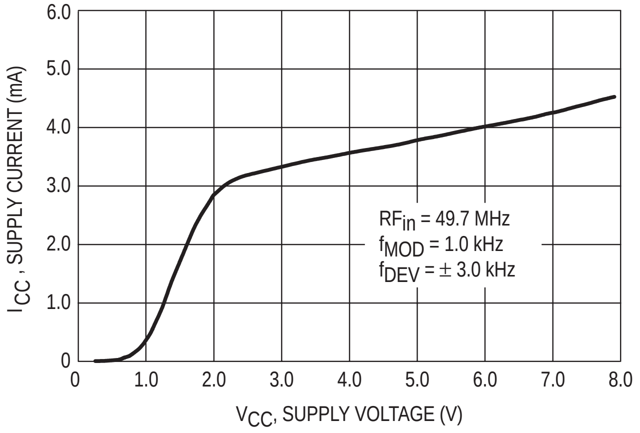


Figure 3. RSSI Output versus RF Input

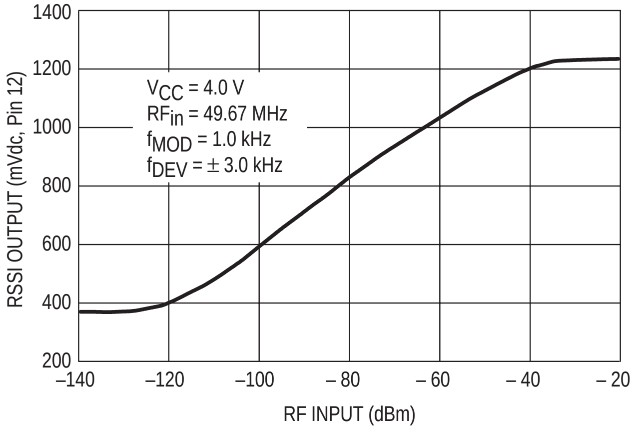


Figure 4. Varactor Capacitance, Resistance versus Bias Voltage

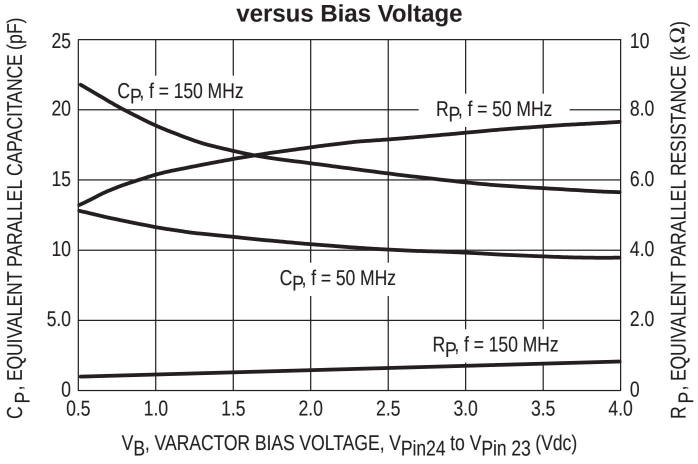


Figure 5. Oscillator Frequency versus Varactor Bias

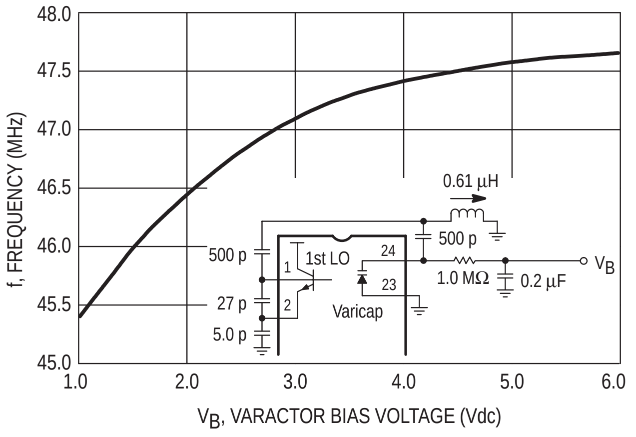


Figure 6. Signal Levels versus RF Input

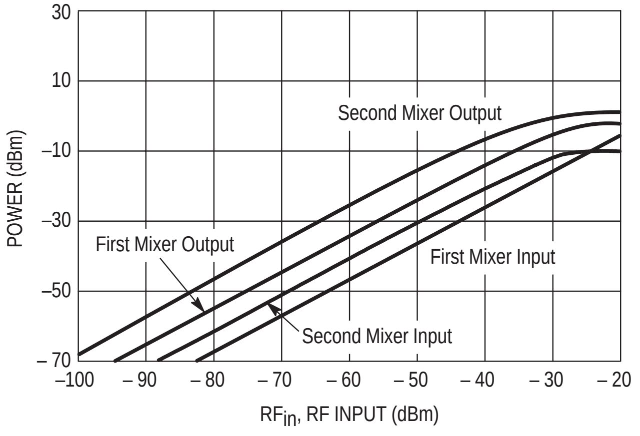


Figure 7. Signal + Noise, Noise, and AM Rejection versus Input Power

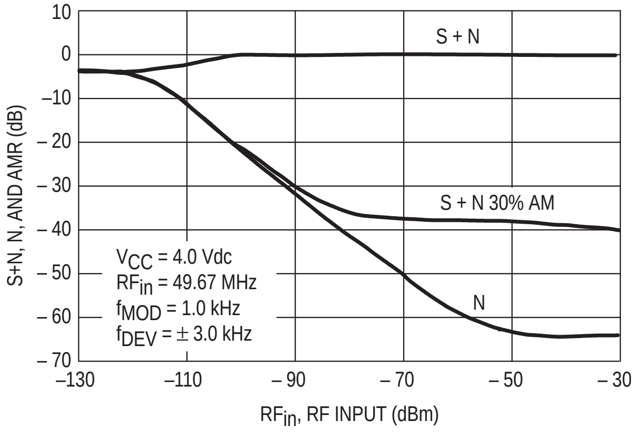


Figure 8. Op Amp Gain and Phase versus Frequency

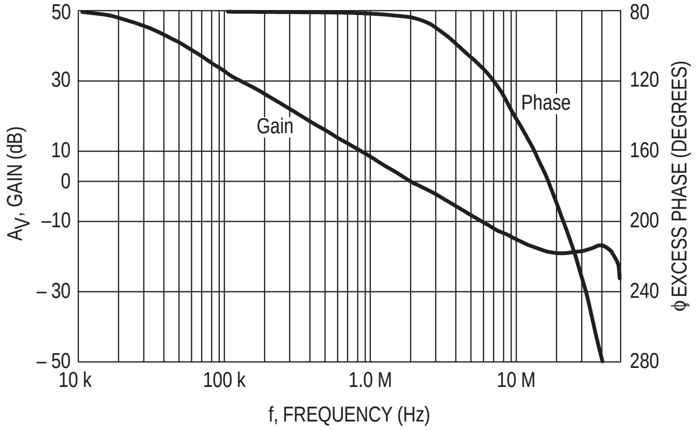


Figure 9. First Mixer Third Order Intermodulation (Unmatched Input)

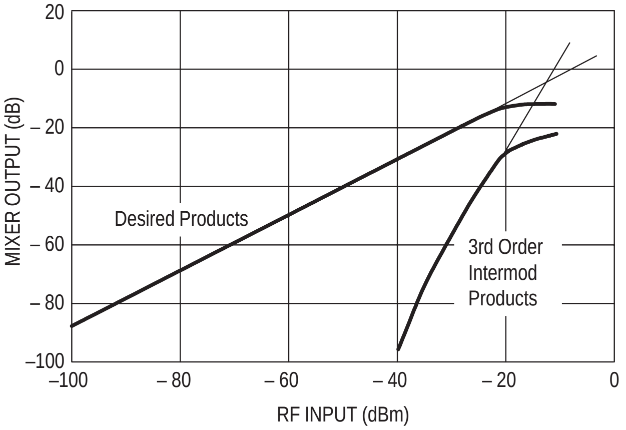


Figure 10. Recovered Audio versus Deviation for MC13135

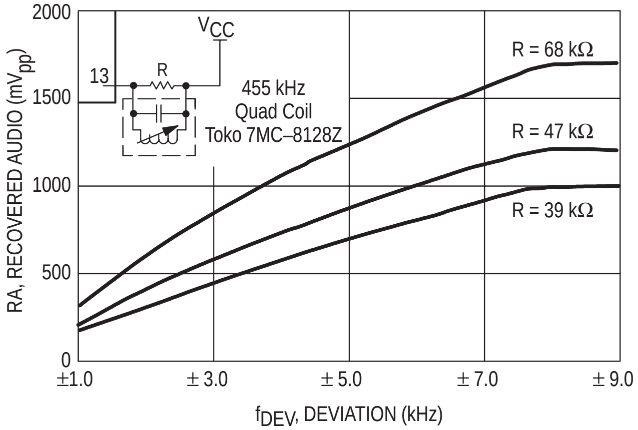


Figure 11. Distortion versus Deviation for MC13135

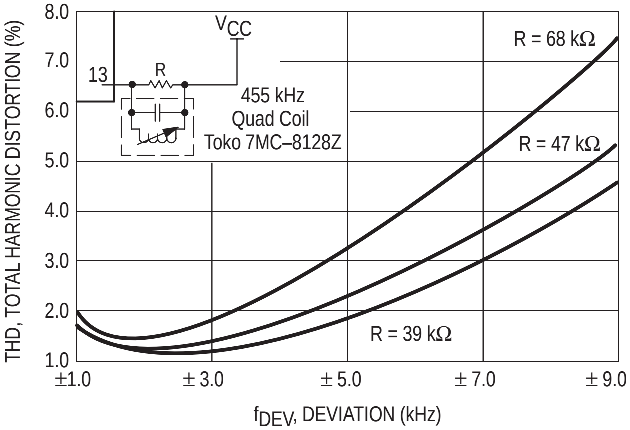


Figure 12. Recovered Audio versus Deviation for MC13136

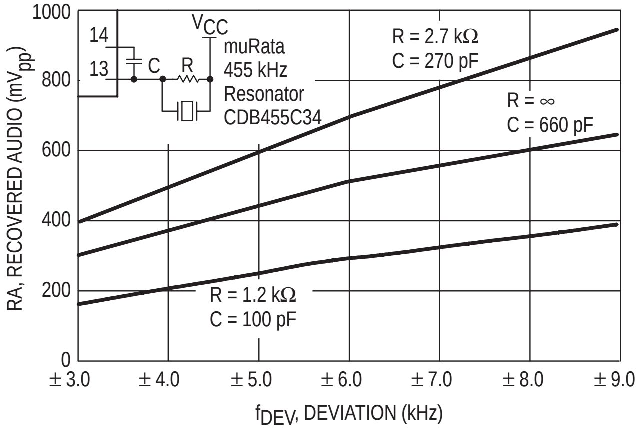
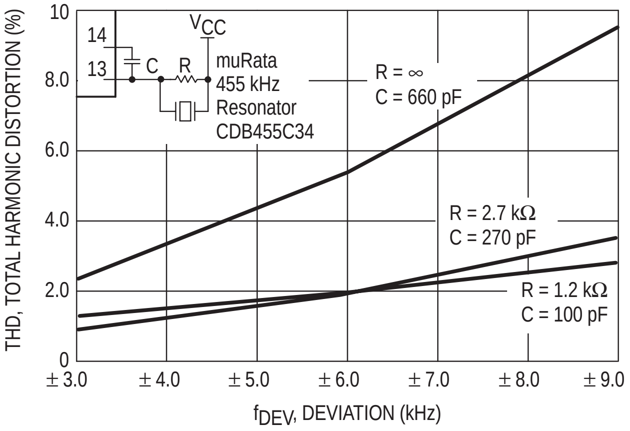


Figure 13. Distortion versus Deviation for MC13136



CIRCUIT DESCRIPTION

The MC13135/13136 are complete dual conversion receivers. They include two local oscillators, two mixers, a limiting IF amplifier and detector, and an op amp. Both provide a voltage buffered RSSI with 70 dB of usable range, isolated tuning diode and buffered LO output for PLL operation, and a separate V_{CC} pin for the first mixer and LO. Improvements have been made in the temperature performance of both the recovered audio and the RSSI.

V_{CC}

Two separate V_{CC} lines enable the first LO and mixer to continue running while the rest of the circuit is powered down. They also isolate the RF from the rest of the internal circuit.

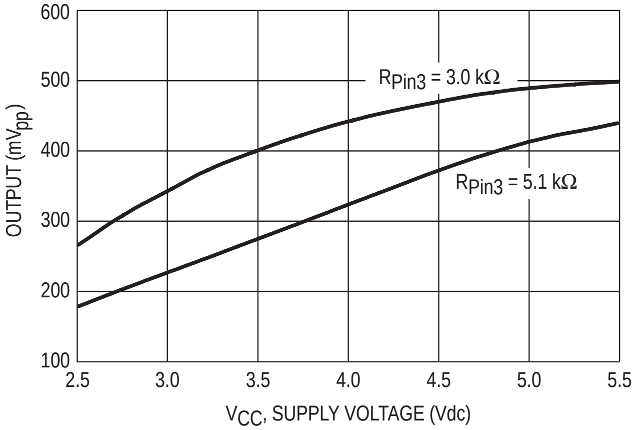
Local Oscillators

The local oscillators are grounded collector Colpitts, which can be easily crystal–controlled or VCO controlled with the on–board varactor and external PLL. The first LO transistor is internally biased, but the emitter is pinned–out and I_Q can be increased for high frequency or VCO operation. The collector is not pinned out, so for crystal operation, the LO is generally limited to 3rd overtone crystal frequencies; typically around 60 MHz. For higher frequency operation, the LO can be provided externally as shown in Figure 16.

Buffer

An amplifier on the 1st LO output converts the single–ended LO output to a differential signal to drive the mixer. Capacitive coupling between the LO and the amplifier minimizes the effects of the change in oscillator current on the mixer. Buffered LO output is pinned–out at Pin 3 for use with a PLL, with a typical output voltage of 320 mV_{pp} at V_{CC} = 4.0 V and with a 5.1 k resistor from Pin 3 to ground. As seen in Figure 14, the buffered LO output varies with the supply voltage and a smaller external resistor may be needed for low voltage operation. The LO buffer operates up to 60 MHz, typically. Above 60 MHz, the output at Pin 3 rolls off at approximately 6.0 dB per octave. Since most PLLs require about 200 mV_{pp} drive, an external amplifier may be required.

Figure 14. Buffered LO Output Voltage versus Supply Voltage



Mixers

The first and second mixer are of similar design. Both are double balanced to suppress the LO and input frequencies to give only the sum and difference frequencies out. This configuration typically provides 40 to 60 dB of LO suppression. New design techniques provide improved mixer linearity and third order intercept without increased noise. The gain on the output of the 1st mixer starts to roll off at about 20 MHz, so this receiver could be used with a 21 MHz first IF. It is designed for use with a ceramic filter, with an output impedance of 330 Ω. A series resistor can be used to raise the impedance for use with a crystal filter, which typically has an input impedance of 4.0 kΩ. The second mixer input impedance is approximately 4.0 kΩ; it requires an external 360 Ω parallel resistor for use with a standard ceramic filter.

Limiting IF Amplifier and Detector

The limiter has approximately 110 dB of gain, which starts rolling off at 2.0 MHz. Although not designed for wideband operation, the bandwidth of the audio frequency amplifier has been widened to 50 kHz, which gives less phase shift and enables the receiver to run at higher data rates. However, care should be taken not to exceed the bandwidth allowed by local regulations.

The MC13135 is designed for use with an LC quadrature detector, and does not have sufficient drive to be used with a ceramic discriminator. The MC13136 was designed to use a ceramic discriminator, but can also be run with an LC quad coil, as mentioned in the Test Circuit Information section. The data shown in Figures 12 and 13 was taken using a muRata CDB455C34 ceramic discriminator which has been specially matched to the MC13136. Both the choice of discriminators and the external matching circuit will affect the distortion and recovered audio.

RSSI/Op Amp

The Received Signal Strength Indicator (RSSI) on the MC13135/13136 has about 70 dB of range. The resistor needed to translate the RSSI current to a voltage output has been included on the internal circuit, which gives it a tighter tolerance. A temperature compensated reference current also improves the RSSI accuracy over temperature. On the MC13136, the op amp on board is connected to the output to provide a voltage buffered RSSI. On the MC13135, the op amp is not connected internally and can be used for the RSSI or as a data slicer (see Figure 17c).

Figure 15. PLL Controlled Narrowband FM Receiver at 46/49 MHz

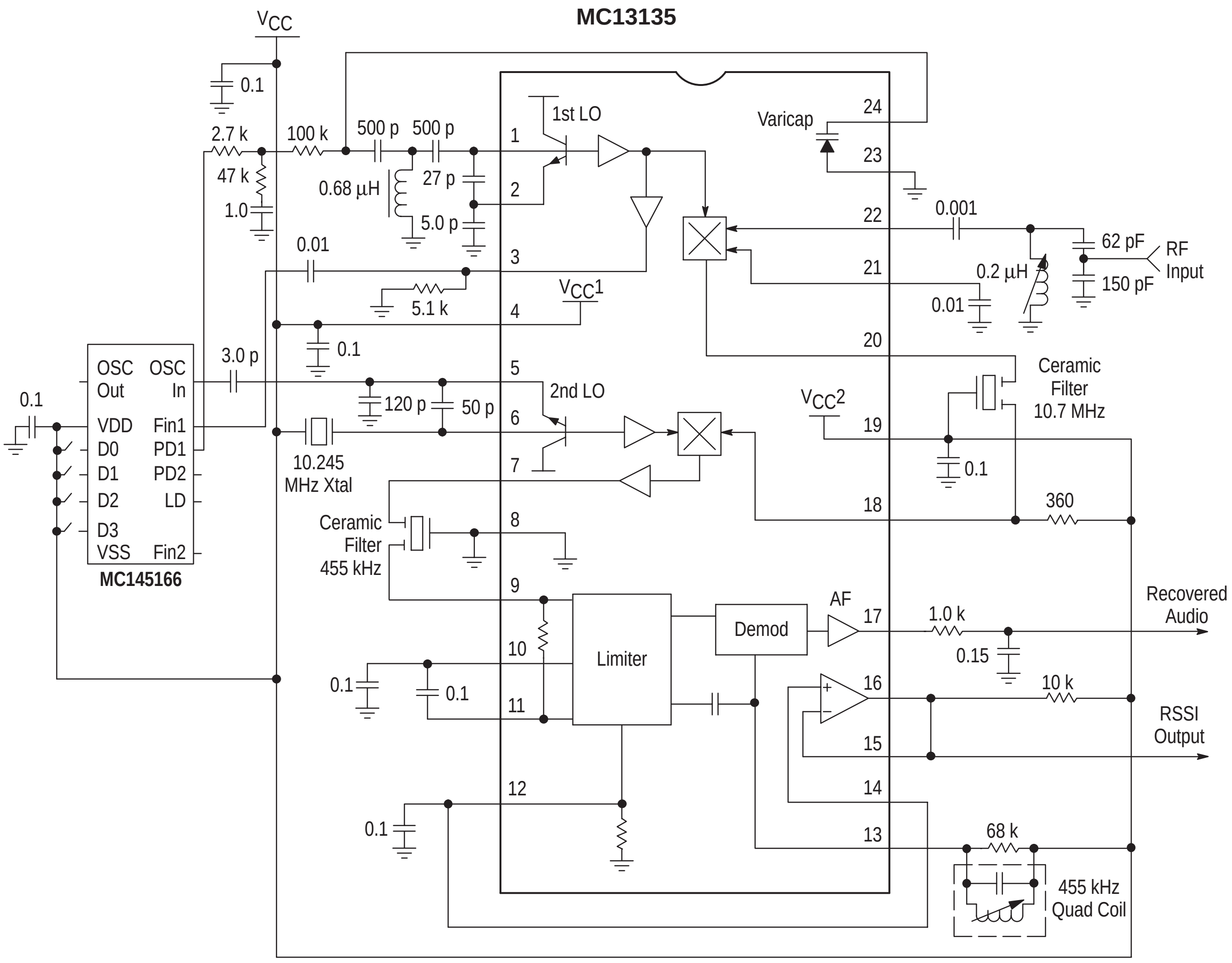
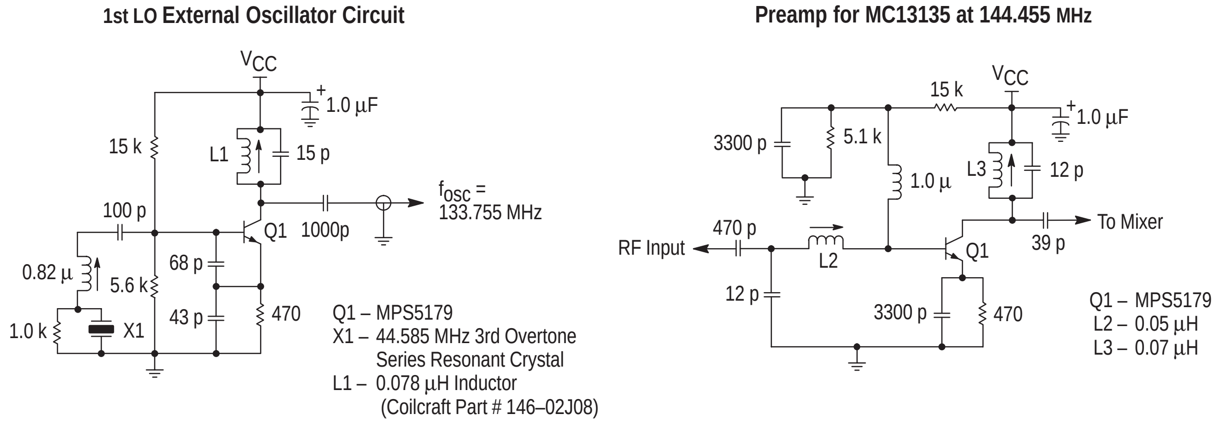


Figure 16. 144 MHz Single Channel Application Circuit


1st LO External Oscillator Circuit

Preamp for MC13135 at 144.455 MHz

Q1 – MPS5179
X1 – 44.585 MHz 3rd Overtone Series Resonant Crystal
L1 – 0.078 µH Inductor (Coilcraft Part # 146–02J08)

Q1 – MPS5179
L2 – 0.05 µH
L3 – 0.07 µH

Figure 17a. Single Channel Narrowband FM Receiver at 49.7 MHz

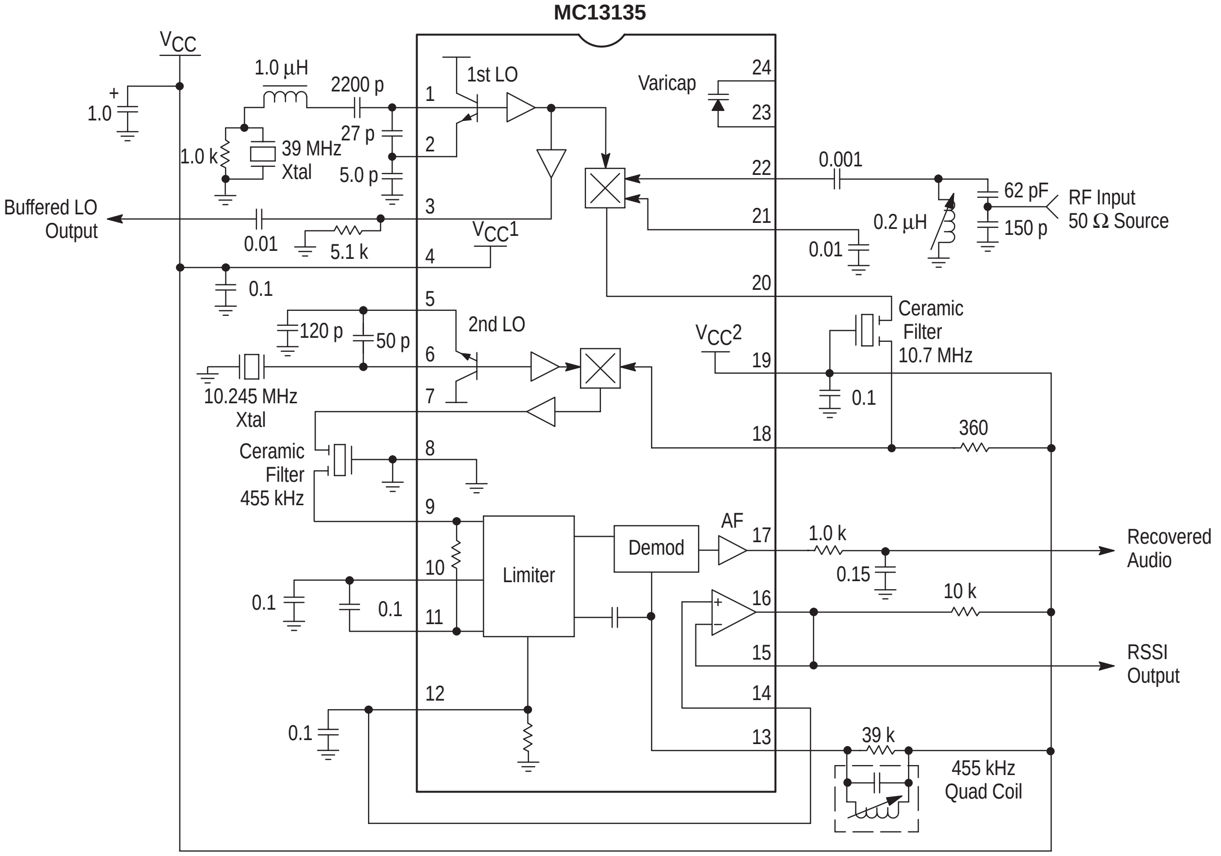
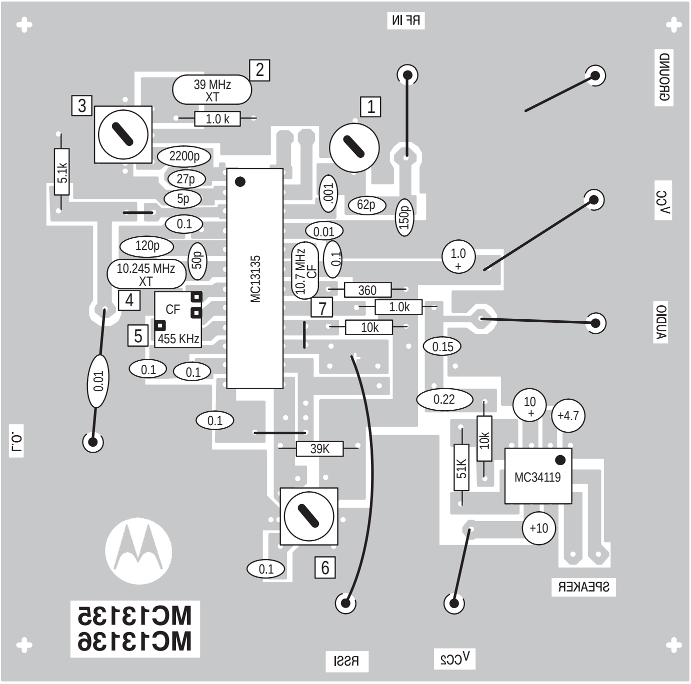


Figure 17b. PC Board Component View



NOTES:
1. 0.2 µH tunable (unshielded) inductor
2. 39 MHz Series mode resonant 3rd Overtone Crystal
3. 1.5 µH tunable (shielded) inductor
4. 10.245 MHz Fundamental mode crystal, 32 pF load
5. 455 kHz ceramic filter, muRata CFU 455B or equivalent
6. Quadrature coil, Toko 7MC–8128Z (7mm) or Toko RMC–2A6597HM (10mm)
7. 10.7 MHz ceramic filter, muRata SFE10.7MJ–A or equivalent

Figure 17c. Optional Data Slicer Circuit
(Using Internal Op Amp)

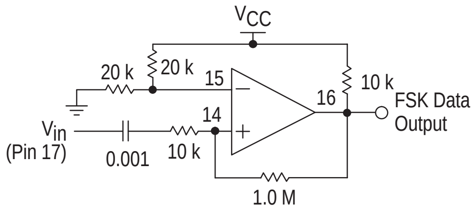
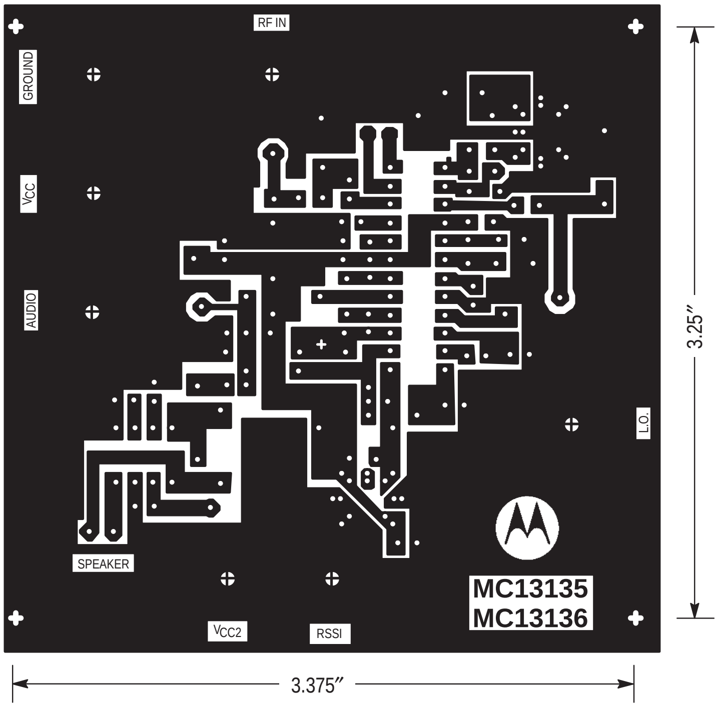
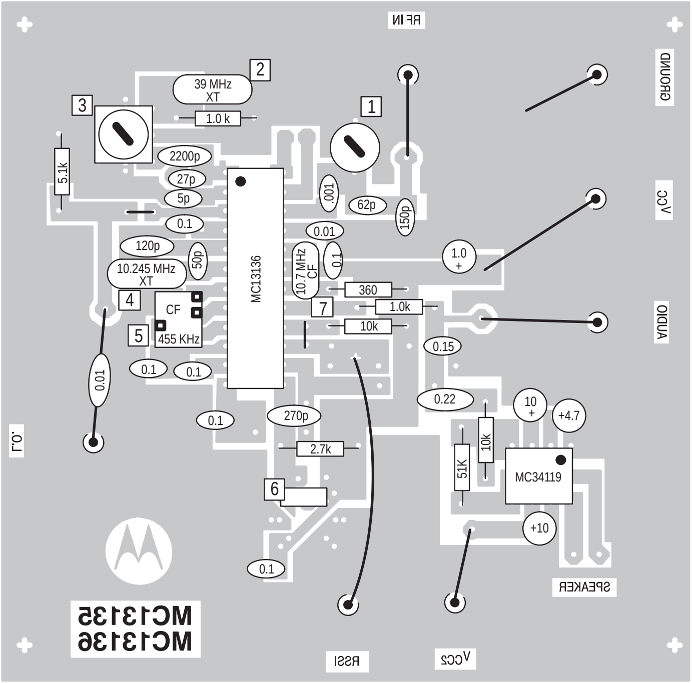


Figure 18. PC Board Solder Side View



(Circuit Side View)

Figure 19. PC Board Component View



NOTES:
1. 0.2 µH tunable (unshielded) inductor
2. 39 MHz Series mode resonant 3rd Overtone Crystal
3. 1.5 µH tunable (shielded) inductor
4. 10.245 MHz Fundamental mode crystal, 32 pF load
5. 455 kHz ceramic filter, muRata CFU 455B or equivalent
6. Ceramic discriminator, muRata CDB455C34 or equivalent
7. 10.7 MHz ceramic filter, muRata SFE10.7MJ–A or equivalent

Figure 20a. Single Channel Narrowband FM Receiver at 49.7 MHz

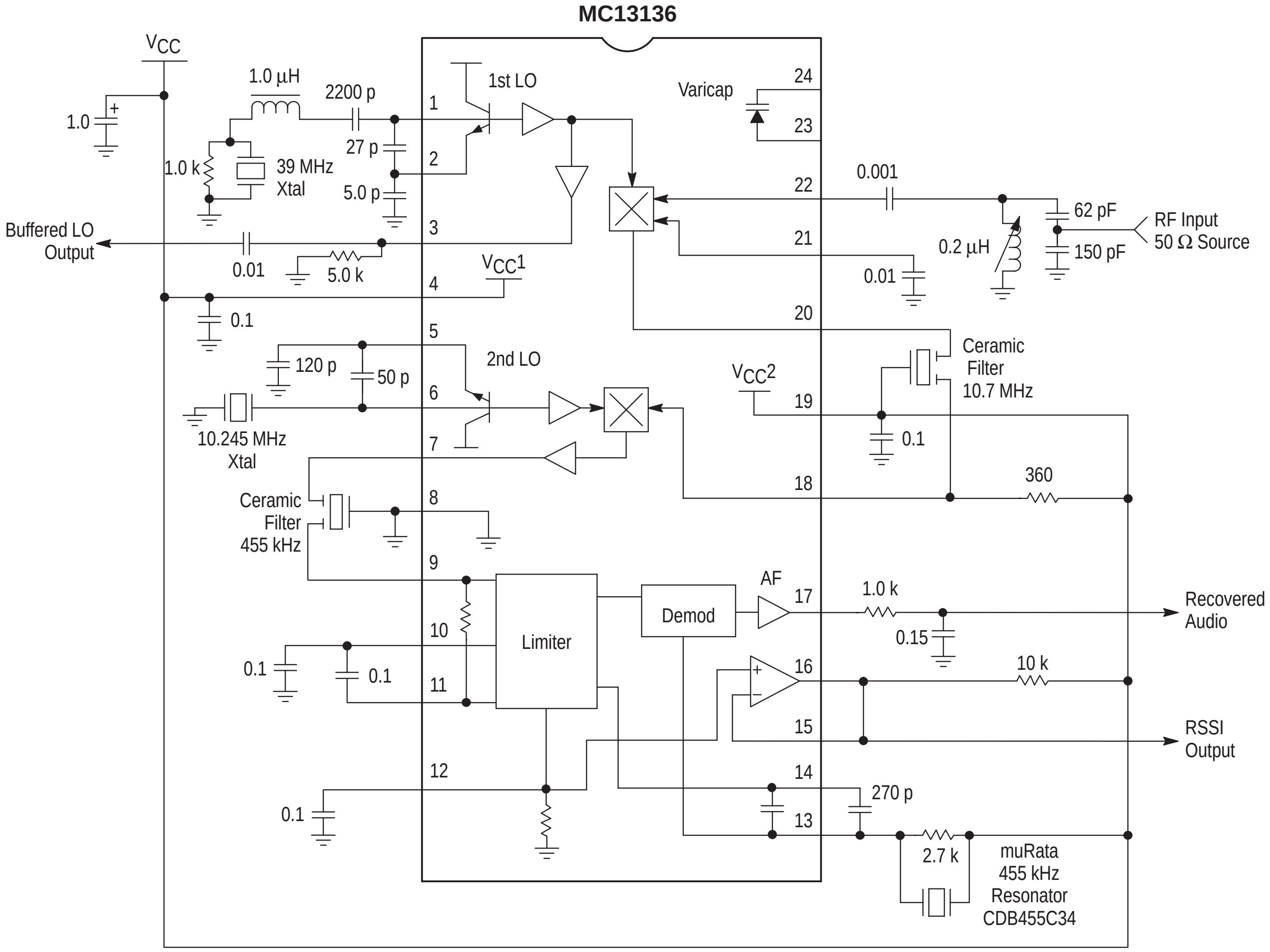


Figure 20b. Optional Audio Amplifier Circuit

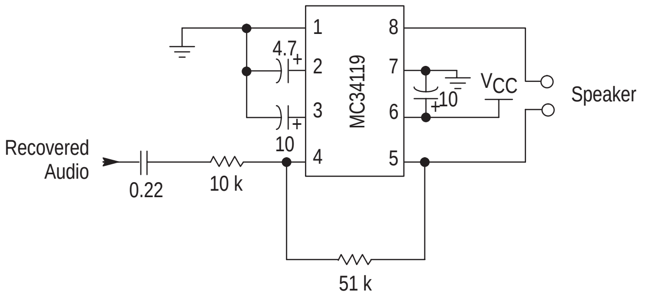
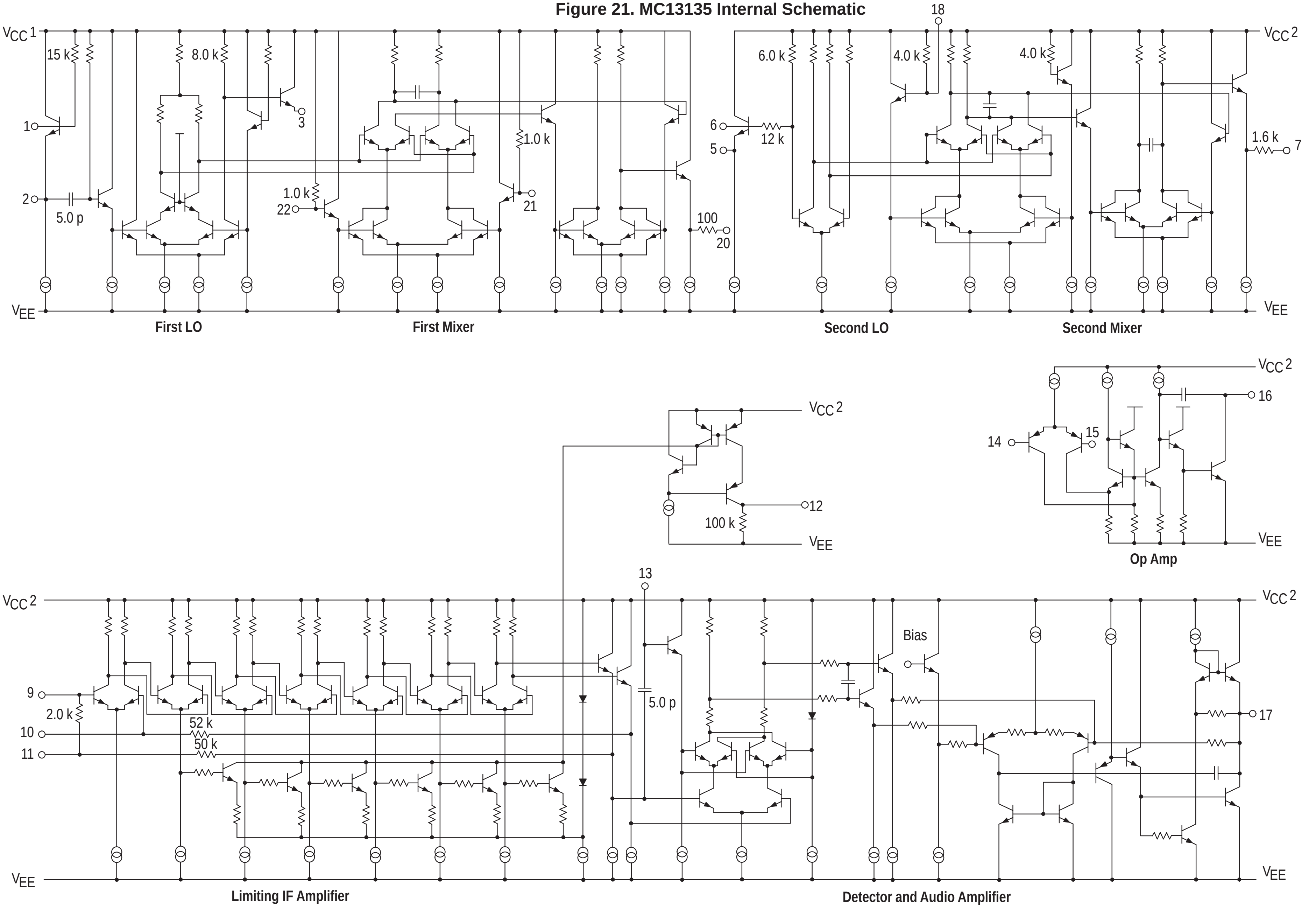
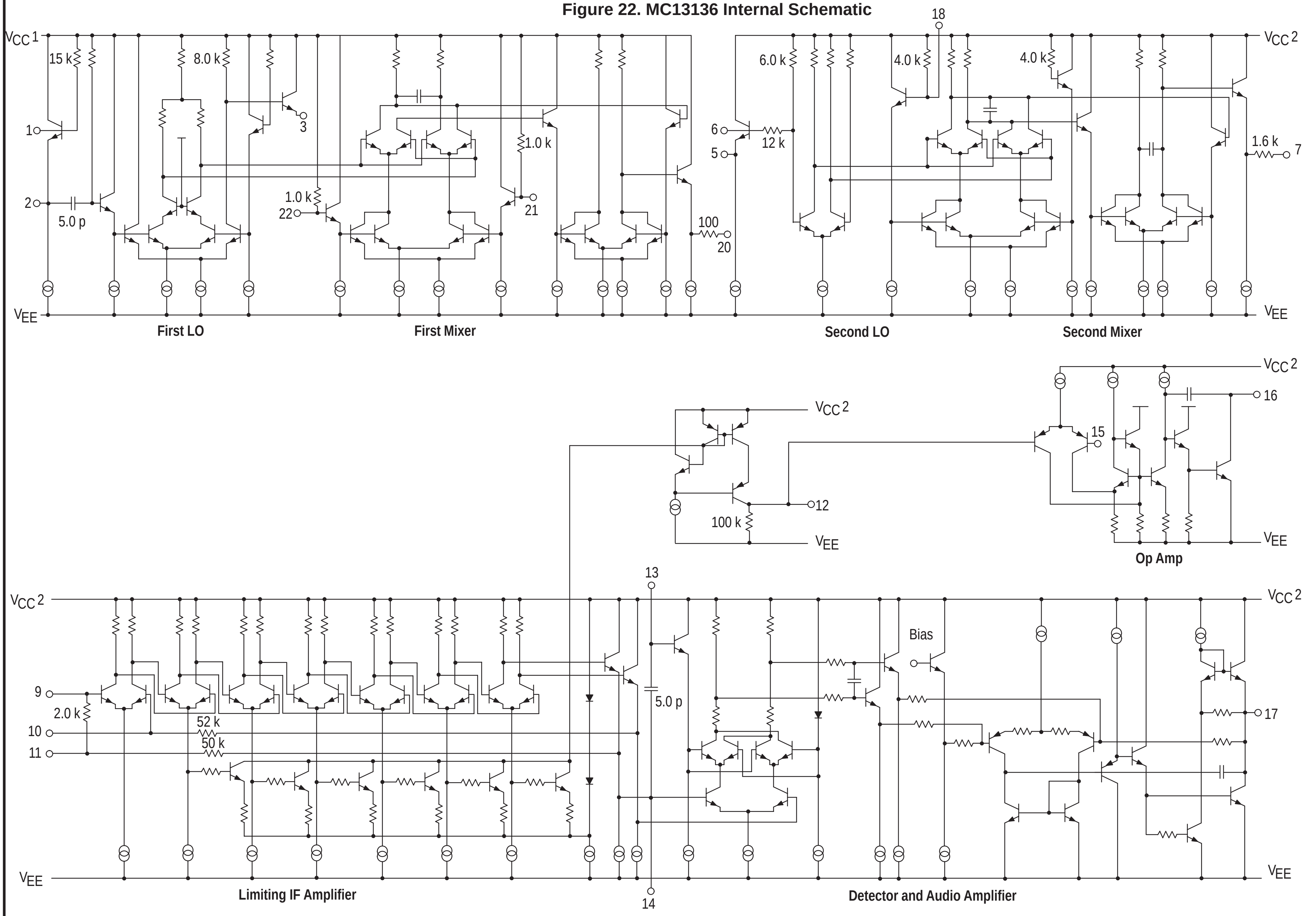


Figure 21. MC13135 Internal Schematic



This device contains 142 active transistors.

Figure 22. MC13136 Internal Schematic



This device contains 142 active transistors.

MOTOROLA

MC13141

Product Preview

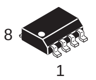
Low Power DC - 1.8 GHz LNA and Mixer

LOW POWER DC – 1.8 GHz LNA AND MIXER

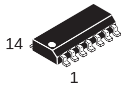
SEMICONDUCTOR TECHNICAL DATA

The MC13141 is intended to be used as a first amplifier and down converter for RF applications. It features wide band operation, low noise, high gain and high linearity while maintaining low current consumption. The circuit consists of a Low Noise Amplifier (LNA), a Local Oscillator amplifier (LO_{amp}), a mixer, an Intermediate Frequency amplifier (IF_{amp}) and a dc control section.

- Wide RF Bandwidth: DC–1.8 GHz
- Wide Mixer Bandwidth: DC–1.8 GHz
- Wide IF Bandwidth: DC–100 MHz
- Low Power: 7.7 mA @ V_{CC} = 2.7–6.5 V
- High Mixer Linearity: $P_{i1.0\ dB}$ = –2.0 dBm, IP_{3in} = 3.0 dBm
- Linearity Adjustment Increases IP_{3in} (Not Available in SOIC8) Up to +20 dBm
- Single–Ended 50 Ω Mixer Input
- Double Balanced Mixer Operation
- Single–Ended 800 Ω Mixer Output
- Single–Ended 50 Ω LO Input



D1 SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)



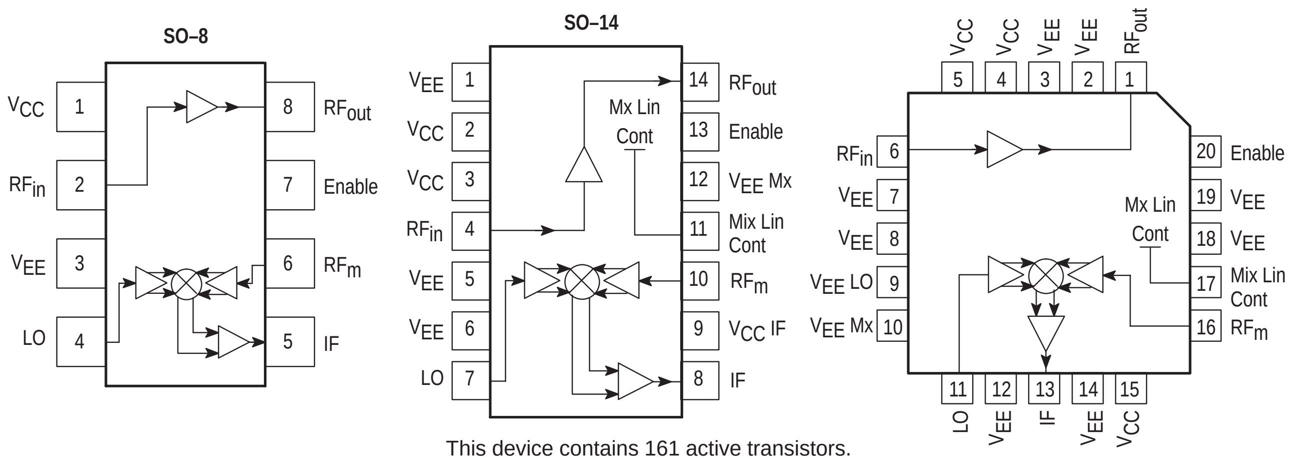
D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO–14)

FTB SUFFIX
PLASTIC PACKAGE
CASE 976
(Thin QFP)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC13141D1	T_A = –40° to +85°C	SO–8
MC13141D		SO–14
MC13141FTB		TQFP–20

PIN CONNECTIONS



This device contains 161 active transistors.

MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	7.0 (max)	Vdc
Operating Supply Voltage Range	V_{CC}	2.7–6.5	Vdc

ELECTRICAL CHARACTERISTICS (SOIC8 Package, V_{CC} = 3.0 V, T_A = 25°C, LO_{in} = –10 dBm @ 950 MHz, IF @ 50 MHz.)

Characteristic	Symbol	Min	Typ	Max	Unit
Supply Current (Power Down)	I_{CC}	–	100	–	pA
Supply Current (Power Up)	I_{CC}	–	7.7	–	mA
Amplifier Gain (50 Ω Insertion Gain)	S21	–	12	–	dB
Amplifier Reverse Isolation	S12	–	–33	–	dB
Amplifier Input Match	$\Gamma_{in\ amp}$	–	–10	–	dB
Amplifier Output Match	$\Gamma_{out\ amp}$	–	–15	–	dB
Amplifier 1.0 dB Gain Compression	$Pin_{–1.0\ dB}$	–	–15	–	dBm
Amplifier Input Third Order Intercept	$IP3_{in}$	–	– 5.0	–	dBm
Amplifier Gain @ N.F. (Application Circuit)	G_{NF}	–	17	–	dB
Amplifier Noise Figure (50 Ω)	NF	–	1.8	–	dB
Mixer Voltage Conversion Gain (R_P = R_L = 800 Ω)	VG_C	–	15	–	dB
Mixer Power Conversion Gain (R_P = R_L = 800 Ω)	PG_C	–	7.0	–	dB
Mixer Input Match	$\Gamma_{in\ M}$	–	–20	–	dB
Mixer SSB Noise Figure	NF_{SSBM}	–	16.0	–	dB
Mixer 1.0 dB Gain Compression	$Pin_{–1.0\ dBM}$	–	–10	–	dBm
Mixer Input Third Order Intercept	$IP3_{inM}$	–	–3.0	–	dBm
Mixer 3 dB RF Bandwidth	$M_{X–3\ dBBW}$	–	1.8	–	GHz
LO Drive Level	LO_{In}	–	–10	–	dBm
LO Input Match	$\Gamma_{in\ LO}$	–	–20	–	dB
RF_{in} Feedthrough to RF_m	$P_{RFin–RFin}$	–	–13	–	dB
RF_{out} Feedthrough to RF_m	$P_{RFout–RFm}$	–	–30	–	dB
LO Feedthrough to IF	$P_{LO–IF}$	–	–25	–	dB
LO Feedthrough to RF_{in}	$P_{LO–RFin}$	–	–30	–	dB
LO Feedthrough to RF_m	$P_{LO–RFm}$	–	–50	–	dB
Mixer RF Feedthrough to IF	$P_{RFm–IF}$	–	–50	–	dB
Mixer RF Feedthrough to RF_{in}	$P_{RFm–RFin}$	–	–25	–	dB

CIRCUIT DESCRIPTION

General

The MC13141 is a low power LNA, double–balanced mixer. This device is designated for use as the front–end section in analog and digital FM systems such as Digital European Cordless Telephone (DECT), PHS, PCS, Cellular, UHF and 800 MHz Special Mobile Radio (SMR), UHF Family Radio Services and 902 to 928 MHz cordless telephones. It features a mixer linearity control to preset or auto preset or auto program the mixer dynamic range, an enable function and buffered IF output for increased overall gain. Further details are covered in the Pin Function Description which shows the equivalent internal circuit and external circuit requirements.

Current Regulation/Enable

Temperature compensating voltage independent current regulators are controlled by the the enable function in which “high” powers up the IC.

Low Noise Amplifier (LNA)

The LNA is internally biased at low supply current (approximately 2.0 mA emitter current) for optimal noise figure and gain. Input and output matching may be achieved at various frequencies using few external components (see Application Circuit). Matching the LNA for maximum stable gain (MSG) yields noise performance within a few tenths of a dB of the minimum noise figure. Typical performance at 1.0 GHz is 17 dB gain and 1.8 dB noise figure for Vcc at 3.0 to 5.0 Vdc.

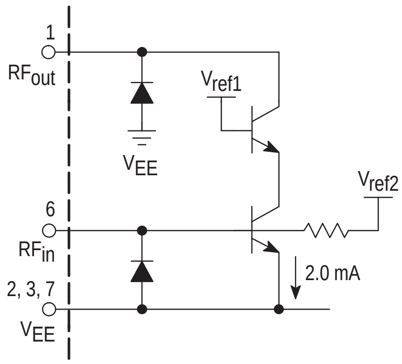
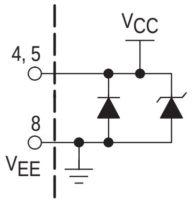
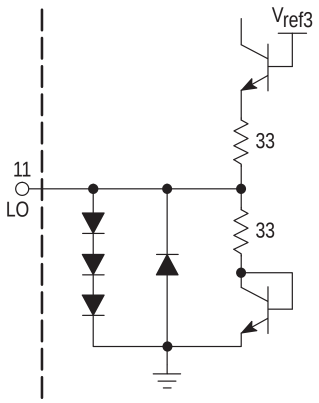
Mixer

The mixer is a double–balanced four quadrant multiplier biased class AB allowing for programmable linearity control via an external current source. An input third order intercept point of 20 dBm may be achieved. All 3 ports of the mixer are designed to work up to 1.8 GHz. The mixer has a 50 Ω single–ended RF input and IF output buffer amplifier. The linear gain of the mixer is approximately 7.0 dB with a SSB noise figure of 16 dB.

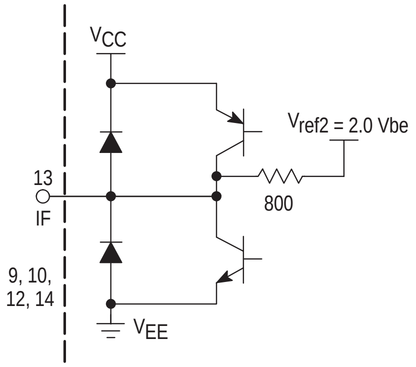
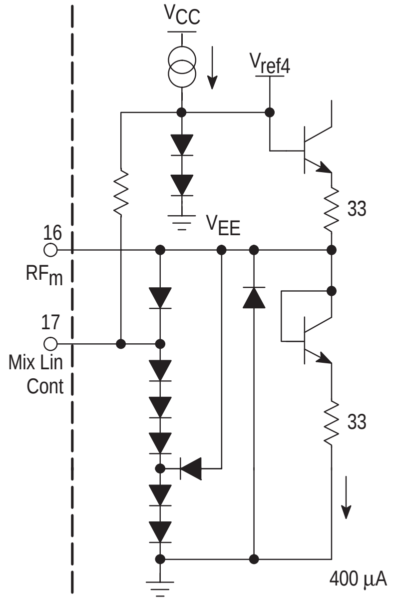
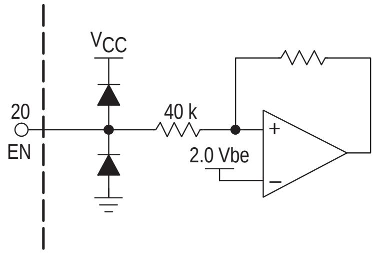
Local Oscillator

It requires an external local oscillator source at –10 dBm input level to maximize the mixer gain.

PIN FUNCTION DESCRIPTION

14 Pin SOIC	20 Pin TQFP	Symbol	Equivalent Internal Circuit (20 Pin TQFP)	Functional Description/External Circuit Requirements
4	6	RF_{in}	 	**RF Input** The input is the base of an NPN low noise amplifier. Minimum external matching is required to optimize the input return loss and gain.
2, 3	4, 5	V_{CC}		**V_{CC} – Positive Supply Voltage** Two V_{CC} pins are provided for the Local Oscillator and LO Buffer Amplifier. The operating supply voltage range is from 2.7 Vdc to 6.5 Vdc. In the PCB layout, the V_{CC} trace must be kept as wide as feasible to minimize inductive reactances along the trace. V_{CC} should be decoupled to V_{EE} at the IC pin as shown in the component placement view.
1, 5	2, 3, 7 and 8	V_{EE}		**V_{EE} – Negative Supply** V_{EE} pin is taken to an ample dc ground plane through a low impedance path. The path should be kept as short as possible. A two sided PCB is implemented so that ground returns can be easily made through via holes.
14	1	RF_{out}		**RF Output** The output is from the collector of the LNA. As shown in the 926 MHz application receiver the output is conjugately matched with a shunt L, and series L and C network.
7	11	LO		**Local Oscillator Input** 50 Ω single–ended buffered LO input.

PIN FUNCTION DESCRIPTION (continued)

14 Pin SOIC	20 Pin TQFP	Symbol	Equivalent Internal Circuit (20 Pin TQFP)	Functional Description/External Circuit Requirements
5, 6	9, 10, 12, 14	V_{EE}		**V_{EE} – Negative Supply** These pins are V_{EE} supply for the IF and LO. In the application PC board these pins are tied to a common V_{EE} trace with other V_{EE} pins.
8	13	IF		**IF Output** The IF is a 800 Ω single–ended output which must be externally matched to 50 Ω for optimal performance.
10	16	RF_m		**Mixer RF Input** The mixer input impedance is broadband 50 Ω for applications up to 1.8 GHz. It easily interfaces with a RF ceramic filter as shown in the application schematic. The pin dc bias is set at 1.0 Vbe.
11	17	Mix Lin Cont		**Mixer Linearity Control** The mixer linearity control circuit accepts approximately 0 to 2.3 mA control current to set the dynamic range of the mixer. An Input Third Order Intercept Point, IIP3 of 20 dBm may be achieved at 2.3 mA of control current (approximately 7.0 mA of additional supply current). The pin dc bias is set at 2.0 Vbe.
12	18, 19	V_{EE}		**V_{EE} – Negative Supply** These pins are V_{EE} supply for the mixer input.
13	20	EN		**Enable** The device is enabled by pulling up to V_{CC} or greater than 2.0 Vbe.

APPLICATIONS INFORMATION

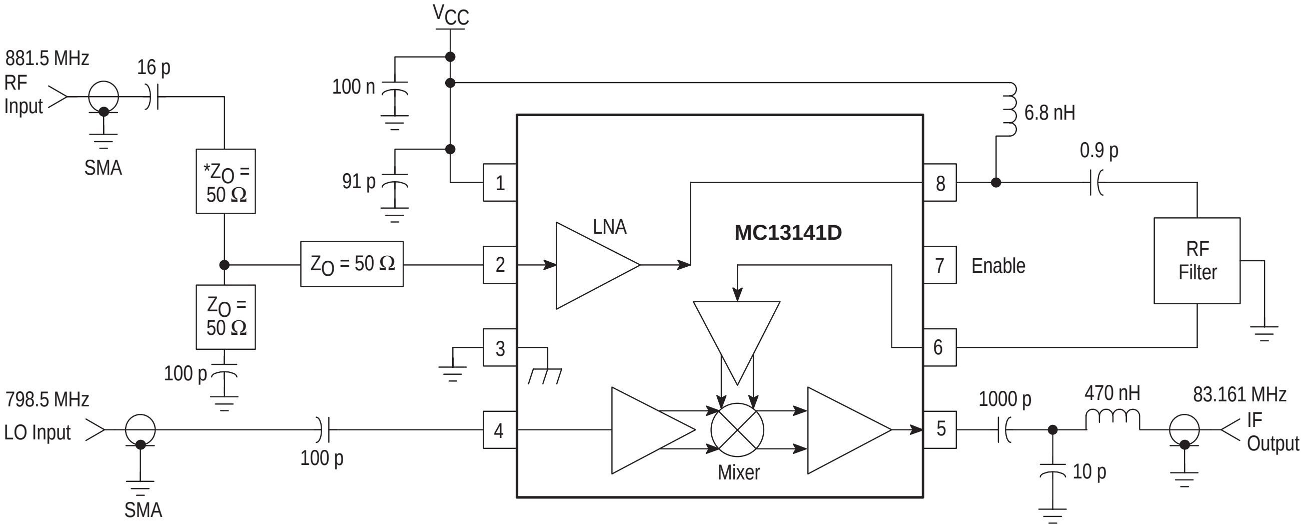
Evaluation PC Board

The evaluation PCB is very versatile and is intended to be used across the entire useful frequency range of this device. The PC board accommodates all SMT components on the circuit side (see Circuit Side Component Placement View). This evaluation board will be discussed and referenced in this section.

Component Selection

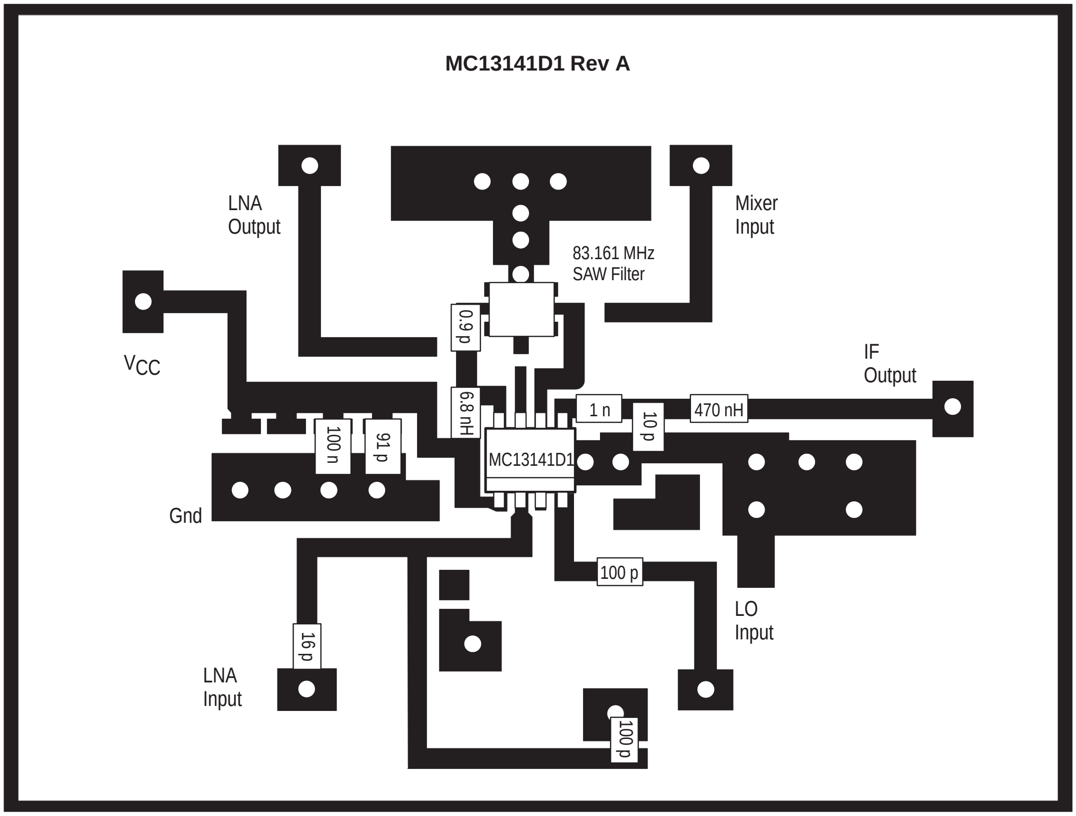
The evaluation PC board is designed to accommodate specific components, while also being versatile enough to use components from various manufacturers and coil types. The circuit side placement view is illustrated for the components specified in the application circuit. The application circuit schematic specifies particular components that were used to achieve the results given and specified in the tables but alternate components of the same Q and value should give similar results.

Figure 1. MC13141D1 Application Circuit (881.5 MHZ)



NOTE: *50 Ω Microstrip Transmission Line; length shown in Figure 2.

Figure 2. Circuit Side Component Placement View

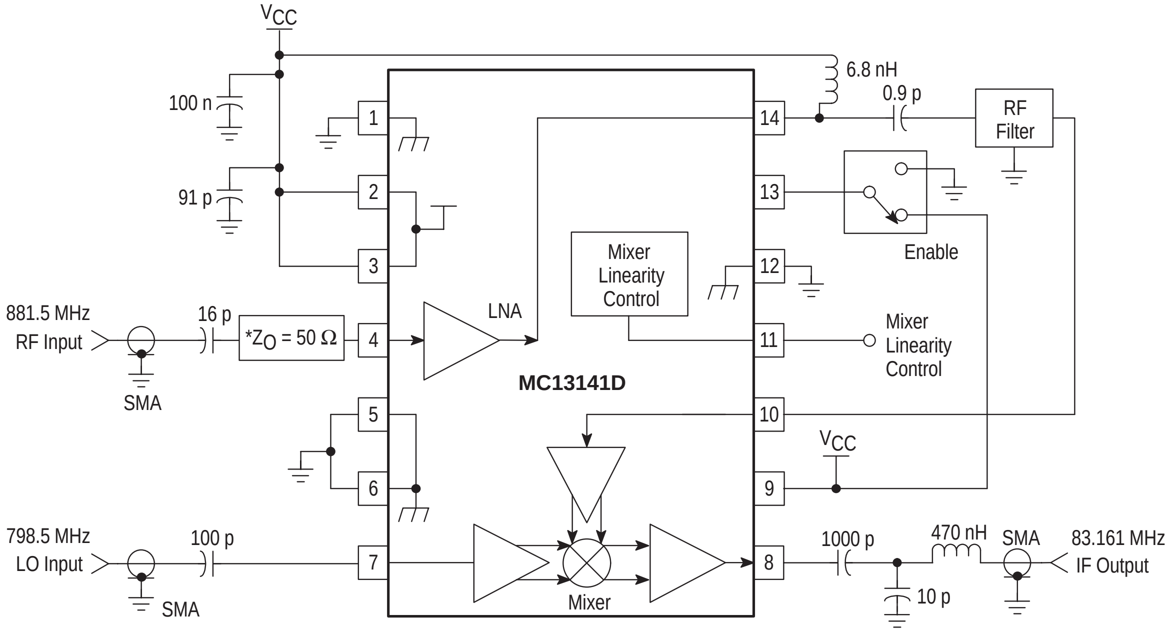


NOTES: 881.5 MHz SAW filter in the ceramic surface mount package is available from several sources: Siemens part # B39881–B4608–Z010 is an example. Other suppliers include Toko and Murata.

The PCB accommodates ceramic dielectric filters for applications in Cellular, DECT, PHS and ISM bands at 902–928 and 2.4–2.5 GHz. Toko makes a full line–up covering the above bands.

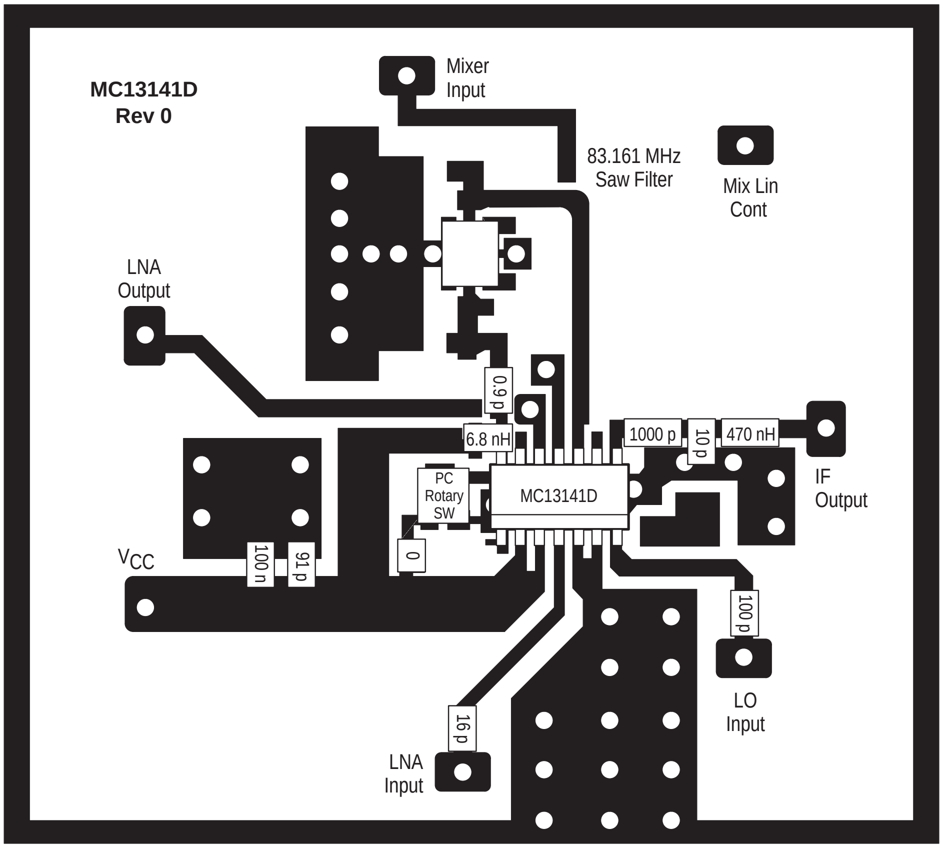
The PCB may be used without an image filter; ac couple the LNA to the mixer. Traces are provided on the PCB to evaluate the LNA and mixer separately. The component placement view shows external circuit components used in the 881.5 MHz application circuit. It is necessary to cut a section in the trace before placing the 0.9 pF capacitor. Capacitors should be 0805 size; the 6.8 nH inductor is a Toko type LL2012.

Figure 3. MC13141D Application Circuit (881.5)



NOTE: *50 Ω Microstrip Transmission Line; length shown in Figure 4.

Figure 4. Circuit Side Component Placement View



NOTES: 881.5 MHz SAW filter in the ceramic surface mount package is available from several sources: Siemens part # B39881–B4608–Z010 is an example. Other suppliers include Toko and Murata.

The PCB accommodates ceramic dielectric filters for applications in Cellular, DECT, PHS and ISM bands at 902–928 and 2.4–2.5 GHz. Toko makes a full line–up covering the above bands.

The PCB may be used without an image filter; ac couple the LNA to the mixer. Traces are provided on the PCB to evaluate the LNA and mixer separately. The component placement view shows external circuit components used in the 881.5 MHz application circuit. It is necessary to cut a section in the trace before placing the 0.9 pF capacitor. Capacitors should be 0805 size; the 6.8 nH inductor is a Toko type LL2012.

Input Matching/Components

It is desirable to use a RF ceramic or SAW filter before the mixer to provide image frequency rejection. The filter is selected based on cost, size and performance tradeoffs. Typical RF filters have 3.0 to 5.0 dB insertion loss. The PC board layout accommodates both ceramic and SAW RF filters which are offered by various suppliers such as Siemens, Toko and Murata. Interface matching between the LNA, RF filter and the mixer will be required. The interface matching networks shown in the application circuit are designed for 50 Ω interfaces.

The LNA is conjugately matched to 50 Ω input and output at 3.0 Vdc V_{CC}. 17 dB gain and 1.8 dB noise figure is typical at 881.5 MHz. The mixer measures 7.0 dB gain and 16 dB noise figure as shown in the application circuit. Typical insertion loss of the Siemens SAW filter is 3.0 dB.

System Noise Considerations

The block diagram shows the cascaded noise stages of the MC13141 in the front–end receiver subsystem; it represents the application circuit. In the cascaded noise analysis the system noise equation is:

$$F_{system} = F1 + \left[(F2 - 1)/G1\right] + \left[(F3 - 1)\right] / \left[(G1)(G2)\right]$$

where:

F1 = the Noise Factor of the MC13142 LNA
G1 = the Gain of the LNA
F2 = the Noise factor of the RF Ceramic Filter
G2 = the Gain of the Ceramic Filter
F3 = the Noise factor of the Mixer

Note: the above terms are defined as linear relationships and are related to the log form for gain and noise figure by the following:

$F = \text{Log}^{-1}\left[(\text{NF in dB})/10\right]$ and similarly
$G = \text{Log}^{-1}\left[(\text{Gain in dB})/10\right]$

Calculating in terms of gain and noise factor yields the following:

F1 = 1.51 ; G1 = 50.11
F2 = 1.99 ; G2 = 0.5
F3 = 39.8

Thus, substituting in the equation for subsystem noise factor:

$F_{subsystem} = 3.08$; $NF_{subsystem} = 4.9$ dB
Overall Subsystem Gain = 21 dB

Figure 5. Front–End Subsystem Block Diagram for Noise Analysis

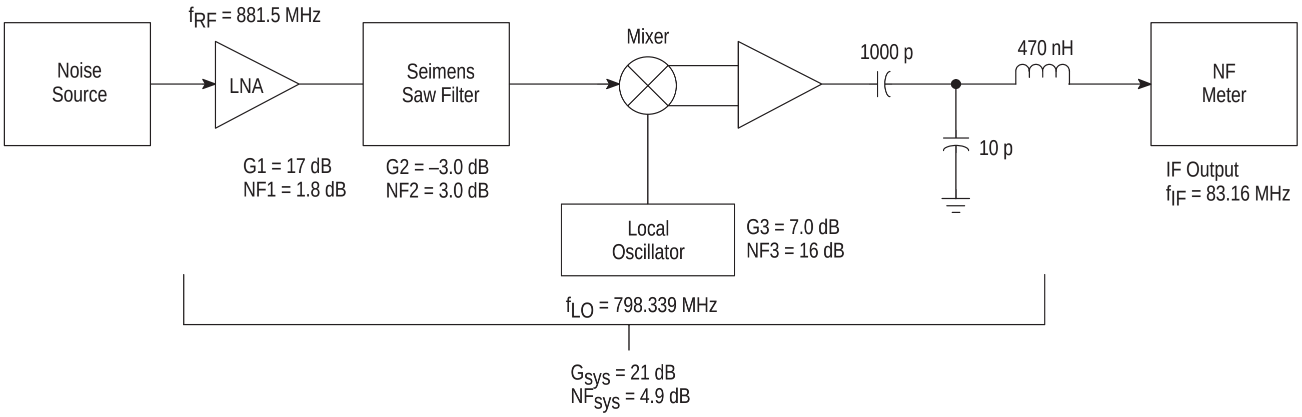
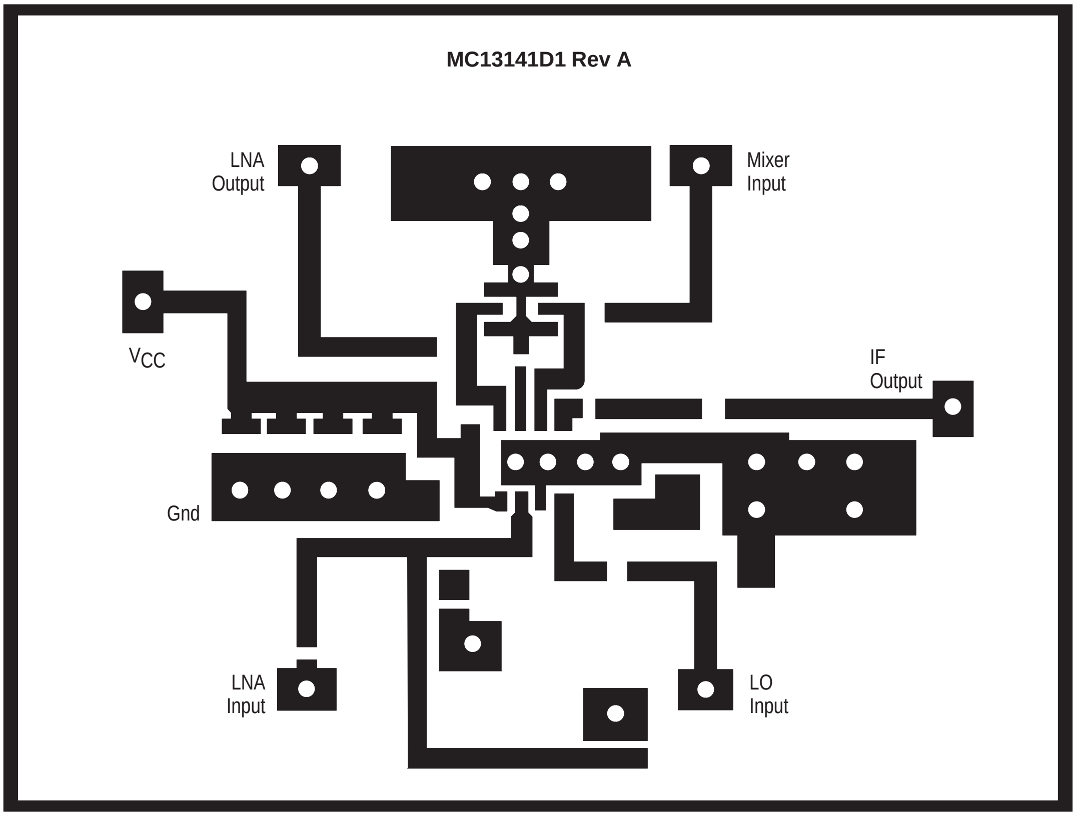
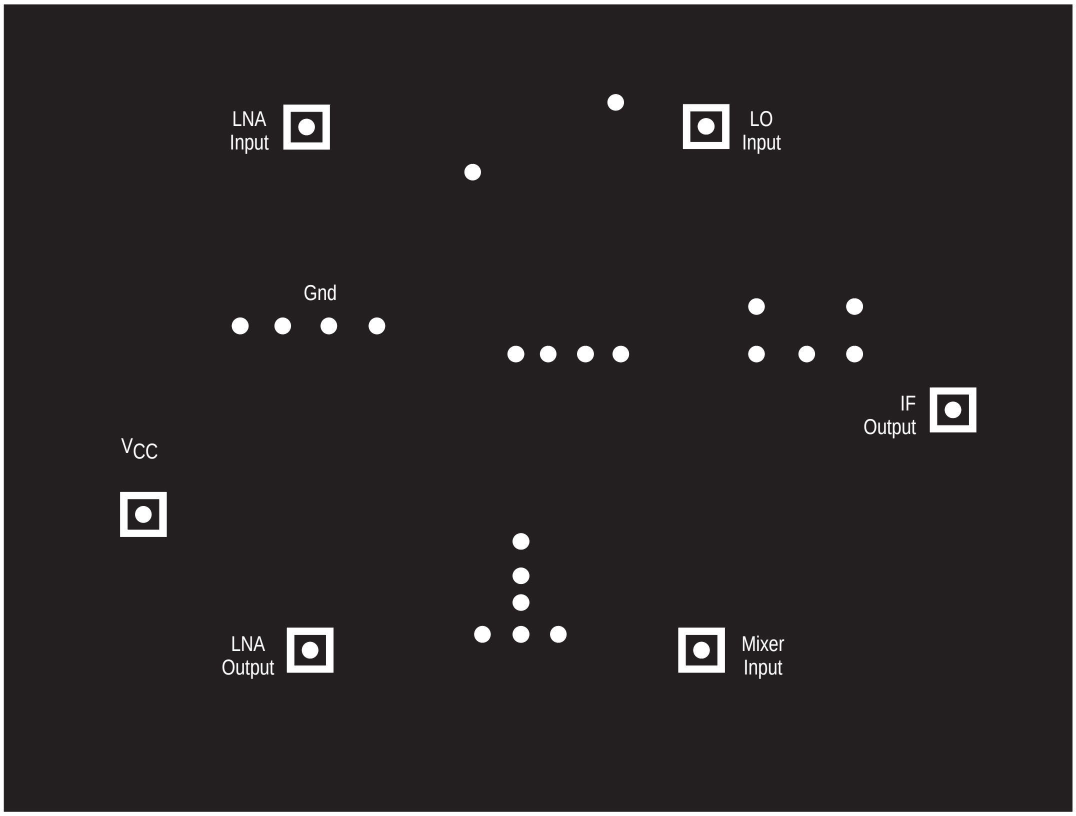


Figure 6. Circuit Side View



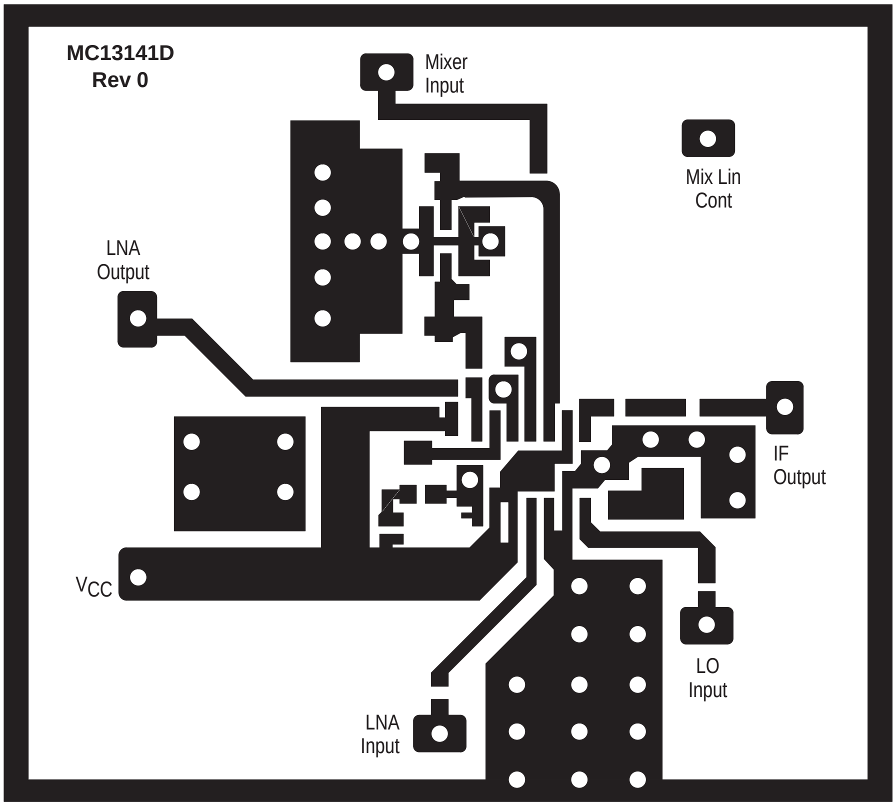
NOTES: Critical dimensions are 50 mil centers lead to lead in SO–8 footprint.
Also line widths to labeled ports excluding V_{CC} are 50 mil (0.050 inch).
FR4 PCB, 1/32 inch.

Figure 7. MC13141D1 Rev A – Ground Side View



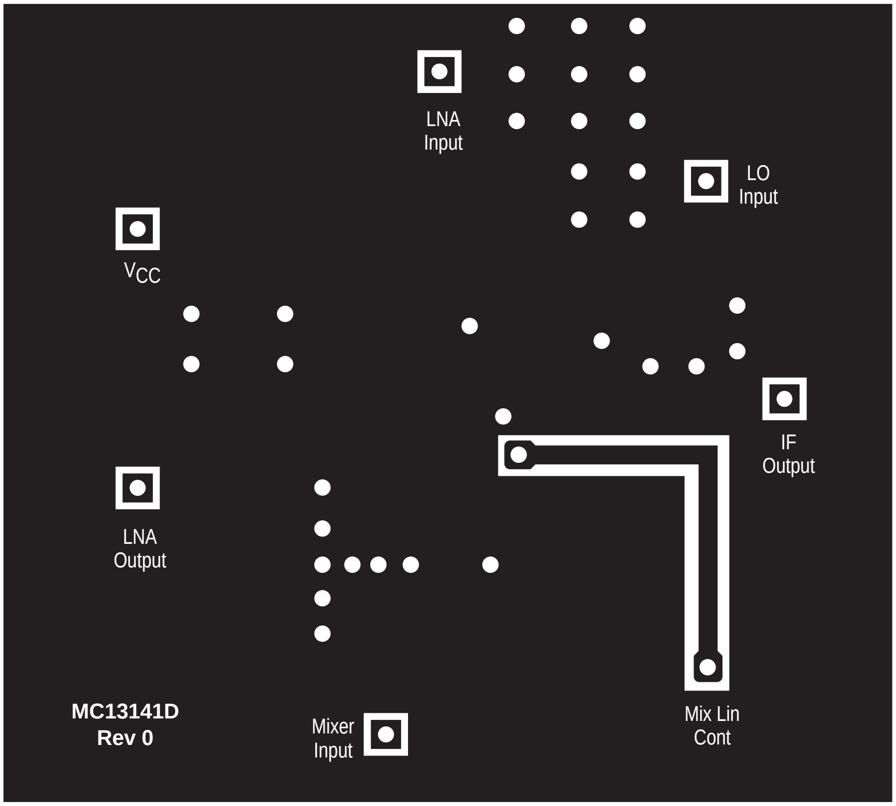
NOTE: FR4 PCB, 1/32 inch.

Figure 8. Circuit Side View



NOTES: Critical dimensions are 50 mil centers lead to lead in SO–14 footprint.
Also line widths to labeled ports excluding V_{CC} are 50 mil (0.050 inch).
FR4 PCB, 1/32 inch.

Figure 9. Ground Side View



NOTE: FR4 PCB, 1/32 inch.

MOTOROLA

MC13142

Product Preview

Low Power DC - 1.8 GHz LNA, Mixer and VCO

The MC13142 is intended to be used as a first amplifier, voltage controlled oscillator and down converter for RF applications. It features wide band operation, low noise, high gain and high linearity while maintaining low current consumption. The circuit consists of a Low Noise Amplifier (LNA), a Voltage Controlled Oscillator (VCO), a buffered oscillator output, a mixer, an Intermediate Frequency amplifier (IF_{amp}) and a dc control section. The wide mixer IF bandwidth allows this part also to be used as an up converter and exciter amplifier.

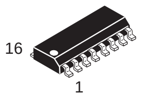
- Wide RF Bandwidth: DC–1.8 GHz
- Wide LO Bandwidth: DC–1.8 GHz
- Wide IF Bandwidth: DC–1.8 GHz
- Low Power: 13 mA @ V_{CC} = 2.7–6.5 V
- High Mixer Linearity: $P_{i1.0\ dB}$ = +3.0 dBm
- Linearity Adjustment Increases IP_{3in} Up to +20 dBm
- Single–Ended 50 Ω Mixer Input
- Double Balanced Mixer Operation
- Open Collector Mixer Output
- Single Transistor Oscillator with Collector, Base and Emitter Pinned Out
- Buffered Oscillator Output
- Mixer and Oscillator Can be Enabled Independently in TQFP–20 Package Only

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC13142D	T_A = –40° to +85°C	SO–16
MC13142FTB		TQFP–20

LOW POWER DC – 1.8 GHz LNA, MIXER and VCO

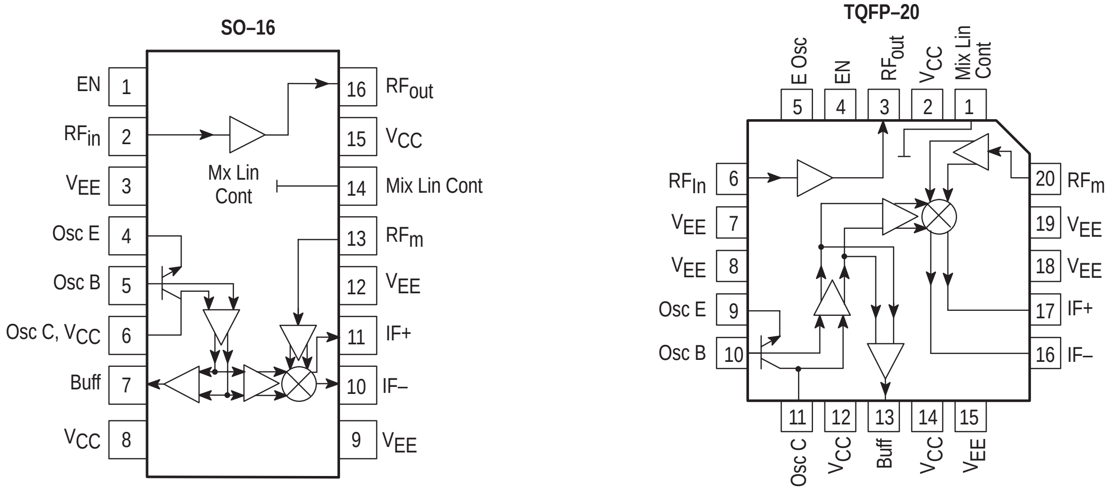
SEMICONDUCTOR TECHNICAL DATA



D SUFFIX
PLASTIC PACKAGE
CASE 751B
(SO–16)

FTB SUFFIX
PLASTIC PACKAGE
CASE 976
(Thin QFP)

PIN CONNECTIONS



This device contains 176 active transistors.

MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	7.0 (max)	Vdc
Operating Supply Voltage Range	V_{CC}	2.7–6.5	Vdc

NOTE: ESD data available upon request.

ELECTRICAL CHARACTERISTICS (V_{CC} = 3.0 V, T_A = 25°C, LO_{in} = –10 dBm @ 950 MHz, IF @ 50 MHz.)

Characteristic	Symbol	Min	Typ	Max	Unit
Supply Current (Power Down)	I_{CC}	–	100	–	pA
Supply Current (Power Up)	I_{CC}	–	13.5	–	mA
Amplifier Gain (50 Ω Insertion Gain)	S_{21}	–	12	–	dB
Amplifier Reverse Isolation	S_{12}	–	–33	–	dB
Amplifier Input Match	$\Gamma_{in\ amp}$	–	–10	–	dB
Amplifier Output Match	$\Gamma_{out\ amp}$	–	–15	–	dB
Amplifier 1.0 dB Gain Compression	$Pin_{–1.0\ dB}$	–	–15	–	dBm
Amplifier Input Third Order Intercept	$IP3_{in}$	–	–5.0	–	dBm
Amplifier Noise Figure (Application Circuit)	NF	–	1.8	–	dB
Amplifier Gain @ N.F.	G_{NF}	–	17	–	dB
Mixer Voltage Conversion Gain (R_P = R_L = 800 Ω)	VG_C	–	9.0	–	dB
Mixer Power Conversion Gain (R_P = R_L = 800 Ω)	PG_C	–	–3.0	–	dB
Mixer Input Match	$\Gamma_{in\ M}$	–	–20	–	dB
Mixer SSB Noise Figure	NF_{SSBM}	–	12	–	dB
Mixer 1.0 dB Gain Compression	$Pin_{–1.0\ dBM}$	–	3.0	–	dBm
Mixer Input Third Order Intercept	$IP3_{InM}$	–	–1.0	–	dBm
Oscillator Buffer Drive (50 Ω)	P_{VCO}	–	–16	–	dBm
Oscillator Phase Noise @ 25 kHz Offset	N_{Φ}	–	–90	–	dBc/Hz
RF_{in} Feedthrough to RF_m	$P_{RFin–RFm}$	–	–35	–	dB
RF_{out} Feedthrough to RF_m	$P_{RFout–RFm}$	–	–35	–	dB
LO Feedthrough to IF	$P_{LO–IF}$	–	–35	–	dBm
LO Feedthrough to RF_{in}	$P_{LO–RFin}$	–	–35	–	dBm
LO Feedthrough to RF_m	$P_{LO–RFm}$	–	–35	–	dBm
Mixer RF Feedthrough to IF	$P_{RFm–IF}$	–	–25	–	dB
Mixer RF Feedthrough to RF_{in}	$P_{RFm–RFin}$	–	–25	–	dB

CIRCUIT DESCRIPTION

General

The MC13142 is a low power LNA, double–balanced Mixer, and VCO. This device is designated for use as the frontend section in analog and digital FM systems such as Digital European Cordless Telephone (DECT), PHS, PCS, Cellular, UHF and 800 MHz Special Mobile Radio (SMR), UHF Family Radio Services and 902 to 928 MHz cordless telephones. It features a mixer linearity control to preset or auto program the mixer dynamic range, an enable function and a wideband IF so the IC may be used either as a down converter or an up converter. Further details are covered in the Pin by Pin Description which shows the equivalent internal circuit and external circuit requirements.

Current Regulation/Enable

Temperature compensating voltage independent current regulators are controlled by the enable function in which “high” powers up the IC.

Low Noise Amplifier (LNA)

The LNA is internally biased at low supply current (approximately 2.0 mA emitter current) for optimal noise figure and gain. The LNA output is biased internally with a 600 Ω resistor to V_{CC}. Input and output matching may be achieved at various frequencies using few external components. Matching the LNA for Maximum stable gain (MSG) yields noise performance within a few tenths of a dB of the minimum noise figure.

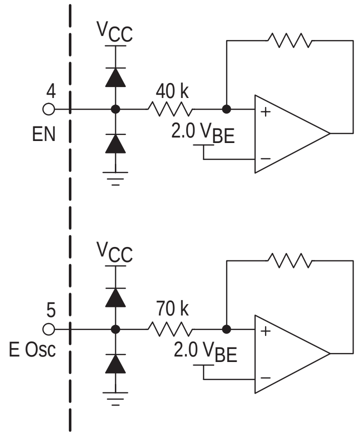
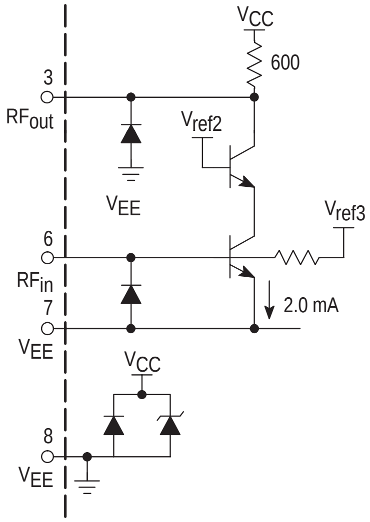
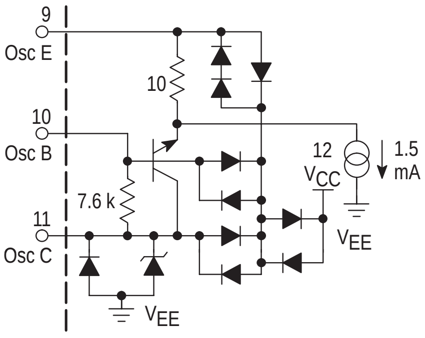
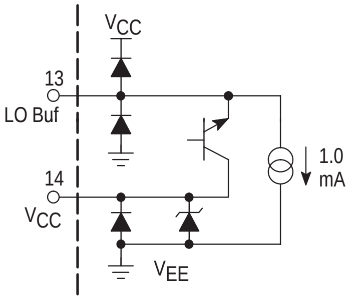
Mixer

The mixer is a double–balanced four quadrant multiplier biased class AB allowing for programmable linearity control via an external current source. An input third order intercept point of 20 dBm may be achieved. All 3 ports of the mixer are designed to work up to 1.8 GHz. The mixer has a 50 Ω single–ended RF input and open collector differential IF outputs. An on–board Local Oscillator transistor has the emitter, base and collector pinned out to implement a low phase noise VCO in various configurations. Additionally, a buffered LO output is provided for operation with a frequency synthesizer. The linear gain of the mixer is approximately 0 dB with a SSB noise figure of 12 dB in the IF output circuit configuration shown in the application example.

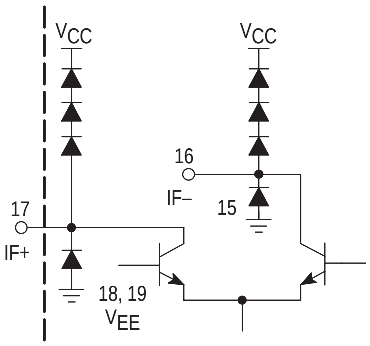
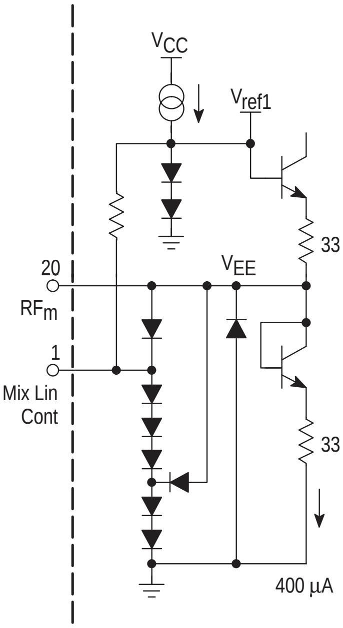
Local Oscillator

The on–chip transistor operates with coaxial transmission line or LC resonant elements to over 2.0 GHz. Biasing is done with a temperature compensated current source in the emitter and a collector to base internal resistor of 7.6 kΩ; however, an RFC from V_{CC} to base is recommended. The application circuit shows a voltage controlled Clapp oscillator operating at center frequency of 975 MHz.

PIN FUNCTION DESCRIPTION

Pin 16 Pin SOIC	 20 Pin TQFP	Symbol	Equivalent Internal Circuit (20 Pin TQFP)	Description
1	4 5	EN E Osc		**Enable, E Osc** In SO–16, both enables, (for the Oscillator/LO Buffer and LNA/Mixer) are bonded to Pin 1. In the TQFP, two pins are provided, Pin 5, E Osc enables the oscillator and buffer while Pin 4, EN enables the LNA/Mixer. Enable by pulling up to V_{CC} or to greater than 2.0 V_{BE}.
2	6	RF_{in}		**RF Input** The input is the base of an NPN low noise amplifier. Minimum external matching is required to optimize the input return loss and gain.
3	7, 8	V_{EE}		**V_{EE} – Negative Supply** V_{EE} pin is taken to an ample dc ground plane through a low impedance path. The path should be kept as short as possible. A two sided PCB is implemented so that ground returns can be easily made through via holes.
16	3	RF_{out}		**RF Output** The output is from the collector of the LNA; it is internally biased with a 600 Ω resistor to V_{CC}. As shown in the 926 MHz application receiver the output is conjugately matched with a shunt L, and series L and C network.
4 5 6	9 10 11	Osc E Osc B Osc C		**On–Board VCO Transistor** The transistor has the emitter, base and collector + V_{CC} pins available. Internal biasing which is compensated for stability over temperature is provided. It is recommended that the base pin is pulled up to V_{CC} through an RFC chosen for the particular oscillator center frequency. The application circuit shows a modified Colpitts or Clapp oscillator configuration and its design is discussed in detail in the application section.
6 8	12 14	V_{CC} V_{CC}		**Supply Voltage (V_{CC})** Two V_{CC} pins are provided for the Local Oscillator and LO Buffer Amplifier. The operating supply voltage range is from 2.7 Vdc to 6.5 Vdc. In the PCB layout, the V_{CC} trace must be kept as wide as feasible to minimize inductive reactances along the trace. V_{CC} should be decoupled to V_{EE} at the IC pin as shown in the component placement view.
7	13	LO Buff		**Local Oscillator Buffer** This is a buffered output providing –16 dBm (50 Ω termination) to drive the f_{in} pin of a PLL synthesizer. Impedance matching to the synthesizer may be necessary to deliver the optimal signal and to improve the phase noise performance of the VCO.

PIN FUNCTION DESCRIPTION (continued)

Pin		Symbol	Equivalent Internal Circuit (20 Pin TQFP)	Description
16 Pin SOIC	20 Pin TQFP			
9, 12	15, 18, 19	V_{EE}		**V_{EE}, Negative Supply** These pins are V_{EE} supply for the mixer IF output. In the application PC board these pins are tied to a common V_{EE} trace with other V_{EE} pins.
10, 11	16, 17	IF–, IF+		**IF Output** The IF is a differential open collector configuration which designed to use over a wide frequency range for up conversion as well as down conversion. Differential to single–ended circuit configuration and matching options are discussed in the application section. 6.0 dB of additional Mixer gain can be achieved by conjugately matching at the desired IF frequency.
13	20	RF_m		**Mixer RF Input** The mixer input impedance is broadband 50 Ω for applications up to 1.8 GHz. It easily interfaces with a RF ceramic filter as shown in the application schematic.
14	1	Mix Lin Cont		**Mixer Linearity Control** The mixer linearity control circuit accepts approximately 0 to 2.3 mA control current to set the dynamic range of the mixer. An Input Third Order Intercept Point, IIP3 of 20 dBm may be achieved at 2.3 mA of control current (approximately 7.0 mA of additional supply current).

APPLICATIONS INFORMATION

Evaluation PC Board

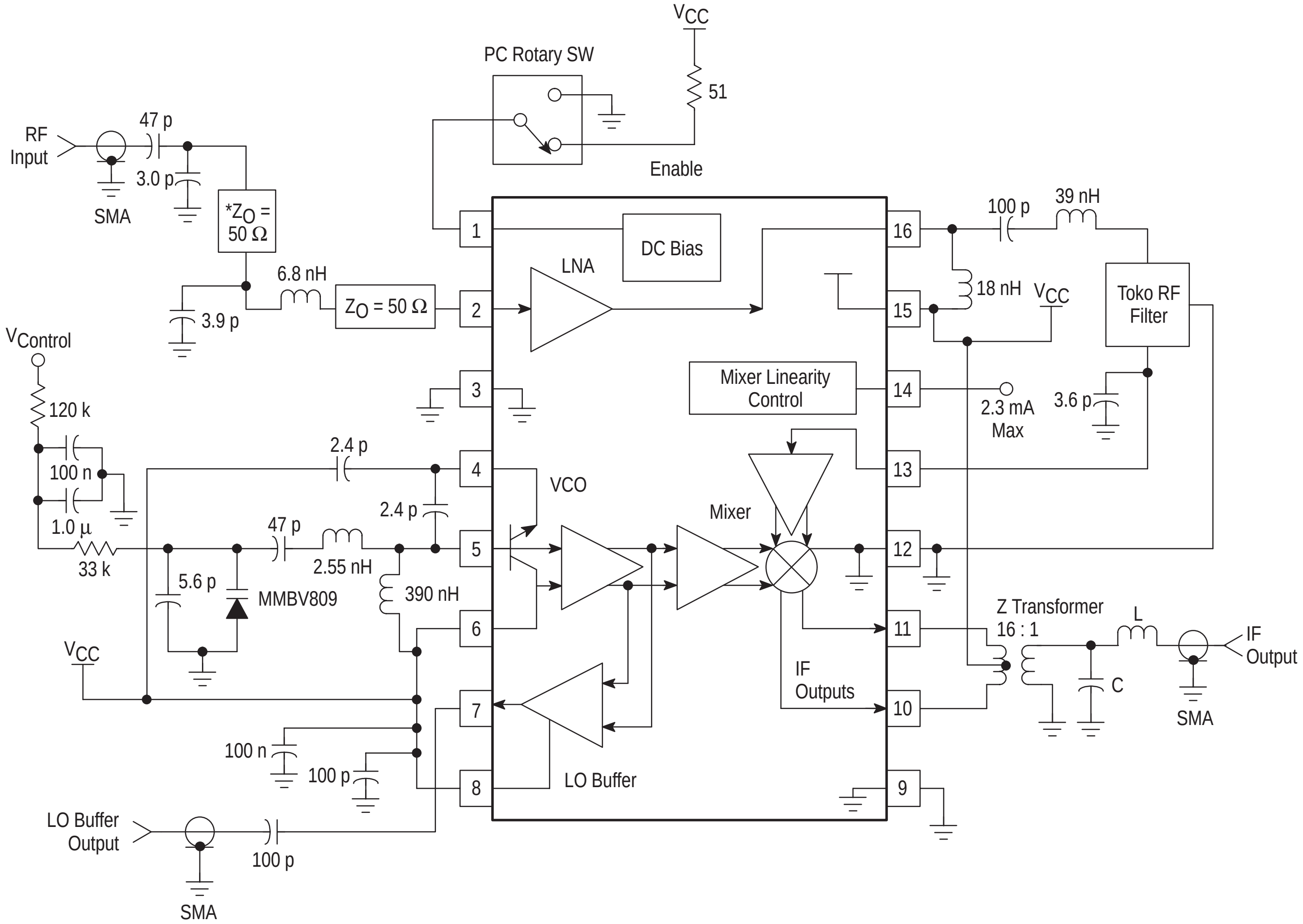
The evaluation PCB is very versatile and is intended to be used across the entire useful frequency range of this device. The PC board accommodates all SMT components on the circuit side (see Circuit Side Component Placement View). This evaluation board will be discussed and referenced in this section.

Component Selection

The evaluation PC board is designed to accommodate specific components, while also being versatile enough to use components from various manufacturers. The circuit side placement view is illustrated for the components specified in the application circuit. The application circuit schematic specifies particular components that were used to achieve the results given and specified in the tables but alternate components of the same Q and value should give equivalent results.

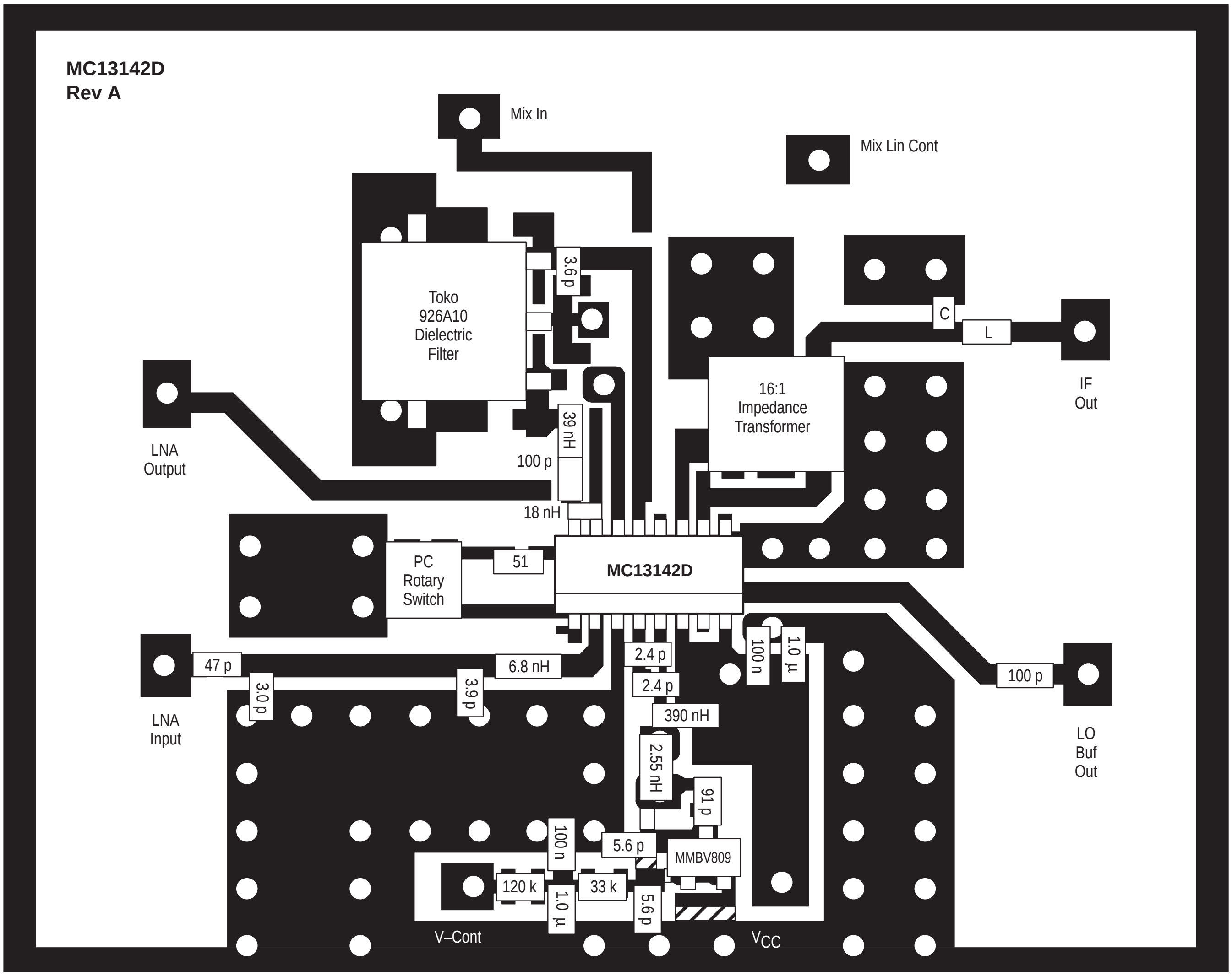
Figure 1. Application Circuit

(926.5 MHz)



NOTE: *50 Ω Microstrip Transmission Line; length shown in Figure 2.

Figure 2. Circuit Side Component Placement View



NOTES: The PCB is laidout for the 4DFA (2 pole SMD type) and 4DFB (3 pole SMD type) filters which are available for applications in cellular and GSM,GPS (1.2–1.5 GHz), DECT, PHS and PCS (1.8–2.0 GHz) and ISM Bands (902–928 MHz and 2.4–2.5 GHz). In the component placement shown above, the 926.5 MHz dielectric type image filter is used (Toko Part # 4DFA–926A10).

The PCB also accommodates a surface mount SAW filter in an eight or six pin ceramic package for the cellular base and handset frequencies. Recommended manufacturers are Siemens and Murata.

Traces are provided on the PCB to evaluate the LNA and mixer separately. The component placement view shows external circuit components used for the 926.5 MHz application circuit. Note: some traces must be cut to accommodate placement of components; likewise some traces must be shorted. The voltage controlled oscillator is shown with the varactor referenced to V_{EE} ground. The PCB is modified as shown to do this.

16:1 broadband impedance transformer is mini circuits part #TX16–R3T; it is in the leadless surface mount “TX” package. Components L and C comprise a low pass filter used to provide narrowband matching at a given IF frequency. For example at 49 MHz C = 36 p and L = 330 nH.
The microstrip trace on the ground side of the PCB is intended for a microstrip resonator; it is cut free when using a lump inductor as done above.

Input Matching/Components

It is desirable to use a RF ceramic or SAW filter before the mixer to provide image frequency rejection. The filter is selected based on cost, size and performance tradeoffs. Typical RF filters have 3.0 to 5.0 dB insertion loss. The PC board layout accommodates both ceramic and SAW RF filters which are offered by various suppliers such as Siemens, Toko and Murata.

Interface matching between the LNA, RF filter and the mixer will be required. The interface matching networks shown in the application circuit are designed for 50 Ω interfaces.

In the application circuit, the LNA is conjugately matched to 50 Ω input and output for 3.0 to 5.0 Vdc V_{CC}. 17 dB gain and 1.8 dB noise figure is typical at 926 MHz. The mixer measures 0 dB gain and 12 dB noise figure as shown in the application circuit. Typical insertion loss of the Toko ceramic filter is 3.0 dB. Thus, the overall gain of the frontend receiver is 14 dB with a 3.3 dB noise figure.

System Noise Considerations

The block diagram shows the cascaded noise stages of the MC13142 in the frontend receiver subsystem; it represents the application circuit. In the cascaded noise analysis the system noise equation is:

Fsystem = F1 + [(F2 –1)/G1] + [(F3–1)]/[(G1)(G2)]

where:

F1 = the Noise Factor of the MC13142 LNA
G1 = the Gain of the LNA
F2 = the Noise factor of the RF Ceramic Filter
G2 = the Gain of the Ceramic Filter
F3 = the Noise factor of the Mixer

Note: the above terms are defined as linear relationships and are related to the log form for gain and noise figure by the following:

F = Log $^{-1}$ [(NF in dB)/10] and similarly
G = Log $^{-1}$ [(Gain in dB)/10].

Calculating in terms of gain and noise factor yields the following:

F1 = 1.51; G1 = 50.11
F2 = 1.99; G2 = 0.5
F3 = 15.85

Thus, substituting in the equation for system noise factor:

Fsystem = 2.12; NFsystem = 3.3 dB

Figure 3. Frontend Subsystem Block Diagram for Noise Analysis

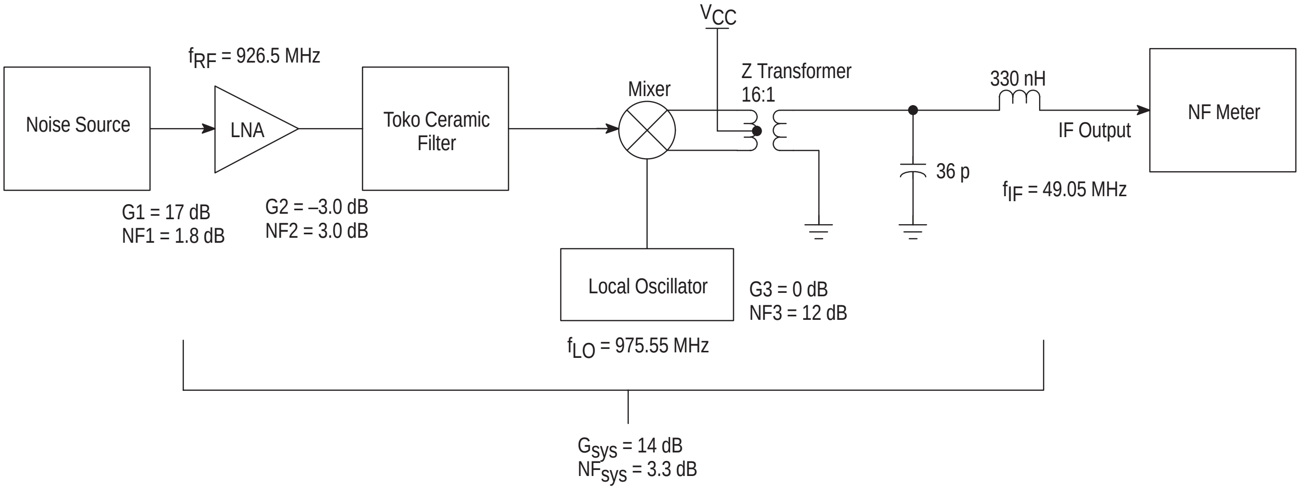
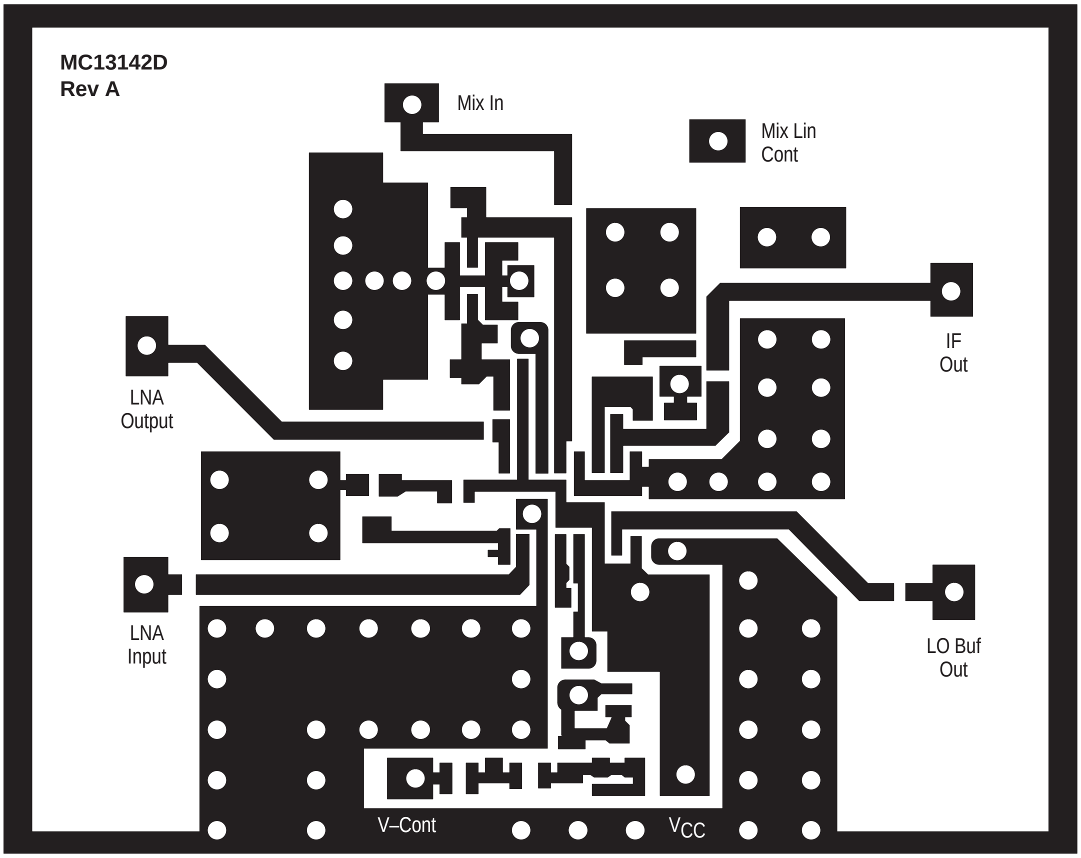
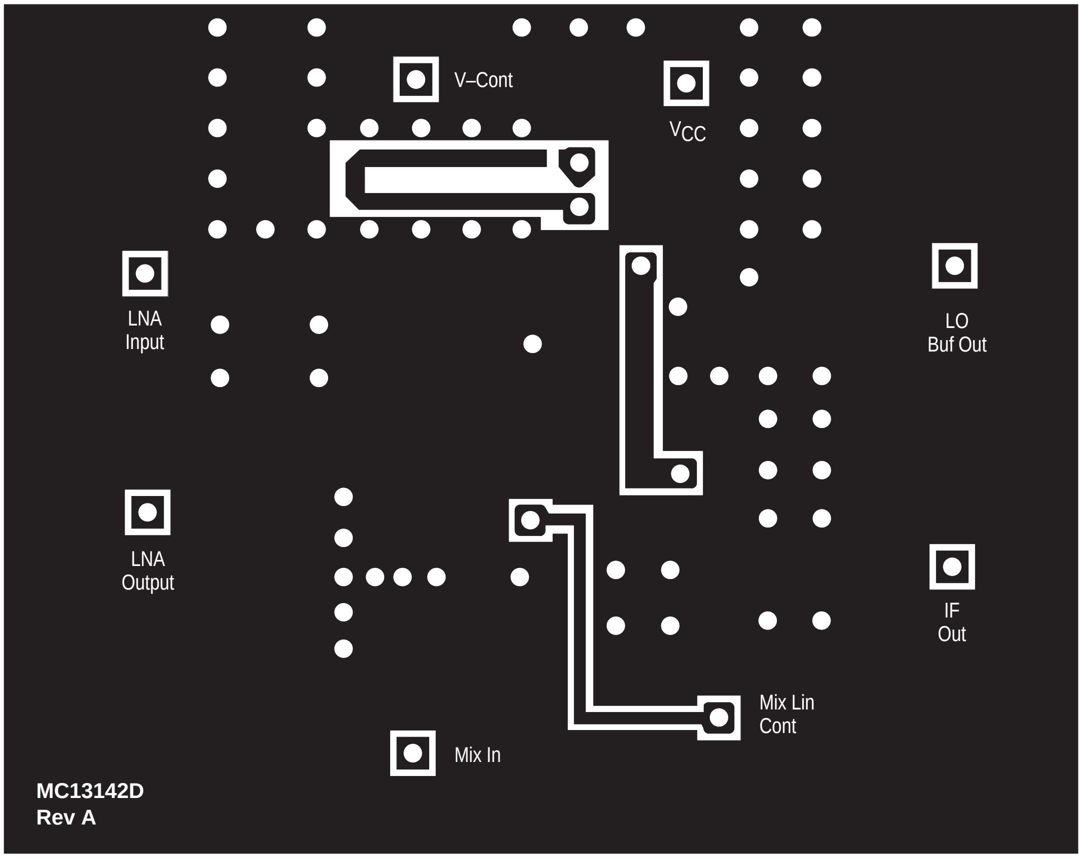


Figure 4. Circuit Side View



NOTES: Critical dimensions are 50 mil centers lead to lead in SO–16 footprint.
Also line widths to labeled ports excluding V_{CC} are 50 mil (0.050 inch).
FR4 PCB, 1/32 inch.

Figure 5. Ground Side View



NOTES: FR4 PCB, 1/32 inch.

MOTOROLA

MC13143

Product Preview

Ultra Low Power DC - 2.4 GHz Linear Mixer

The MC13143 is a high compression linear mixer with single–ended RF input, differential IF output and differential LO inputs which consumes as little as 1.8 mW. A new circuit topology is used to achieve a high third order intermodulation intercept point, high linearity and high 1.0 dB output compression point while maintaining a linear 50 Ω input impedance. It is designed for Up or Down conversion anywhere from dc to 2.4 GHz.

Ultra Low Power: 1.0 mA @ V_{CC} = 1.8–6.5 V

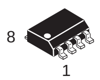
- Wide Input Bandwidth: DC–2.4 GHz
- Wide Output Bandwidth: DC–2.4 GHz
- Wide LO Bandwidth: DC–2.4 GHz
- High Mixer Linearity: $P_{i1.0\ dB}$ = + 3.0 dBm

Linearity Adjustment of up to IP_{3in} = +20 dBm

- 50 Ω Mixer Input
- Single–Ended Mixer Input
- Double Balanced Mixer Operation
- Differential Open Collector Mixer Output

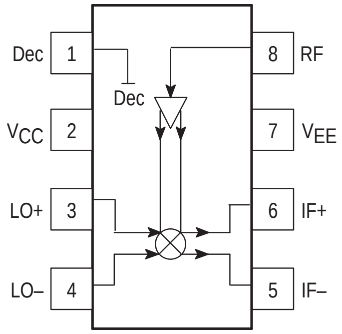
ULTRA LOW POWER DC – 2.4 GHz LINEAR MIXER

SEMICONDUCTOR
TECHNICAL DATA



D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC13143D	T_A = –40° to +85°C	SO–8

MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted.)

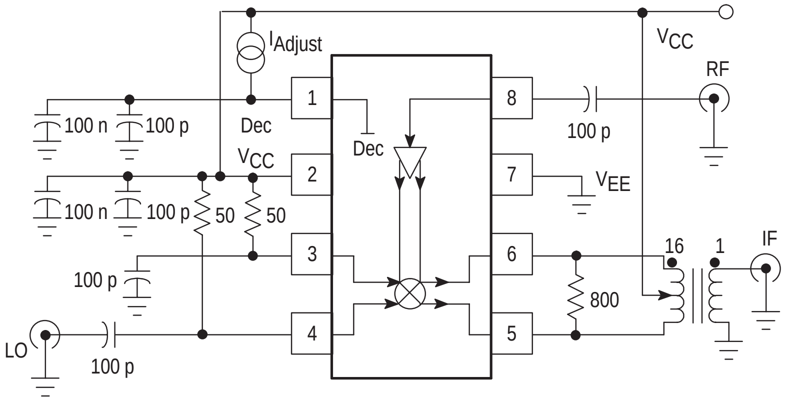
Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	7.0 (max)	Vdc
Operating Supply Voltage Range	V_{CC}	1.8–6.5	Vdc

NOTE: ESD data available upon request.

ELECTRICAL CHARACTERISTICS (V_{CC} = 2.0 V, T_A = 25°C, RF = – 30 dBm @ 900 MHz, LO = 0 dBm @ 950 MHz, IF @ 50 MHz.)

Characteristic	Symbol	Min	Typ	Max	Unit
Supply Current	I_{CC}	–	1.0	–	mA
Mixer Voltage Conversion Gain (R_P = R_L = 800 Ω)	VG_C	–	9.0	–	dB
Mixer Power Conversion Gain (R_P = R_L = 800 Ω)	PG_C	–	–5.0	–	dB
Mixer Input Match	Γ_{in}	–	–20	–	dB
Mixer SSB Noise Figure	NF_{SSB}	–	12	–	dB
Mixer 1.0 dB Gain Compression	$Pin_{–1.0\ dB}$	–	3.0	–	dBm
Mixer Input Third Order Intercept	$IP3_{in}$	–	–3.0	–	dBm
LO Drive Level	LO_{in}	–	–5.0	–	dBm
LO Feedthrough to Mixer Out	$P_{LO–IF}$	–	–25	–	dB
Mixer Input Feedthrough Output	$P_{RFm–IF}$	–	–25	–	dB
Mixer Input Feedthrough to LO	$P_{RFm–LO}$	–	–25	–	dB

Figure 1. Test Circuit



This device contains 29 active transistors.

TYPICAL PERFORMANCE CURVES

Figure 2. Power Conversion Gain and Supply Current versus Supply Voltage

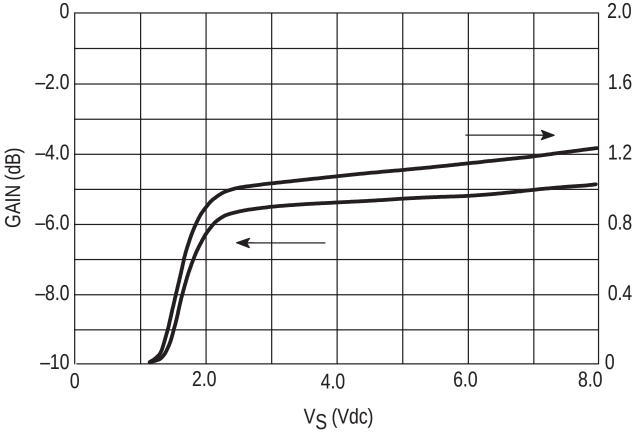


Figure 3. Noise Figure and Gain versus LO Power

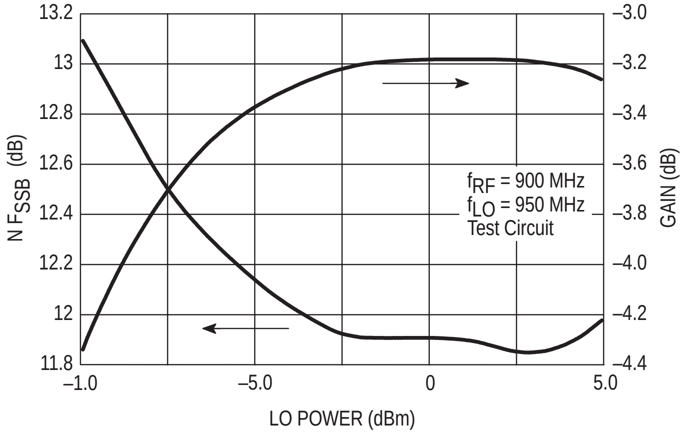


Figure 4. Mixer Input Return Loss versus RF Input Frequency

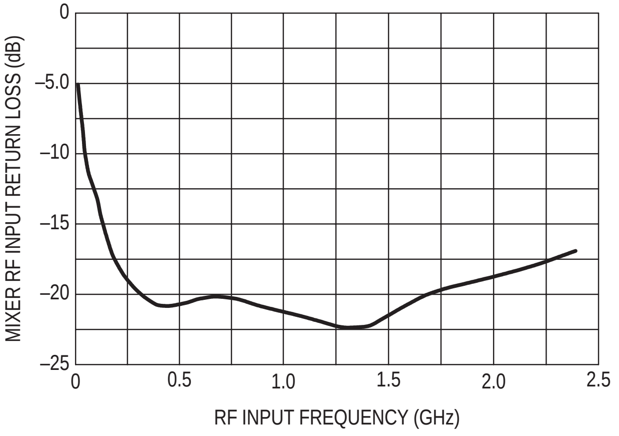


Figure 5. Power Conversion Gain and Supply Current versus RF Input Power

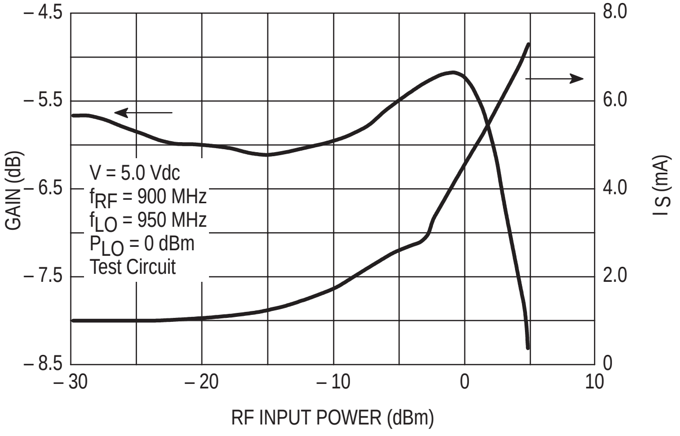


Figure 6. Noise Figure and Gain versus RF Frequency

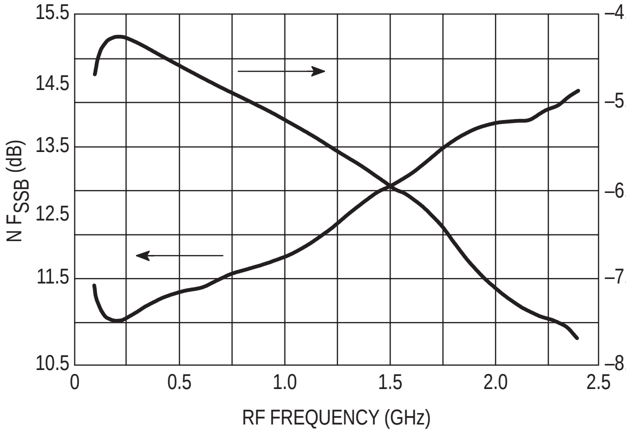
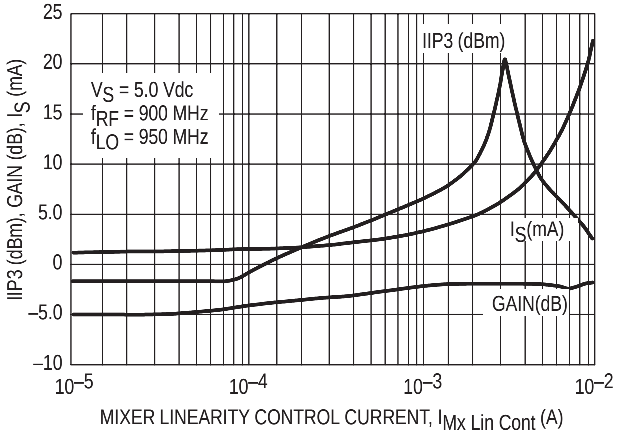


Figure 7. IIP3, Gain, Supply Current versus Mixer Linearity Control Current



CIRCUIT DESCRIPTION

General

The MC13143 is a double–balanced Mixer. This device is designated for use as the frontend section in analog and digital FM systems such as Wireless Local Area Network (LAN), Digital European Cordless Telephone (DECT), PHS, PCS, GPS, Cellular, UHF and 800 MHz Special Mobile Radio (SMR), UHF Family Radio Services and 902 to 928 MHz cordless telephones. It features a mixer linearity control to preset or auto program the mixer dynamic range, an enable function and a wideband IF so the IC may be used either as a down converter or an up converter.

Current Regulation

Temperature compensating voltage independent current regulators provide typical supply current at 1.0 mA with no mixer linearity control current.

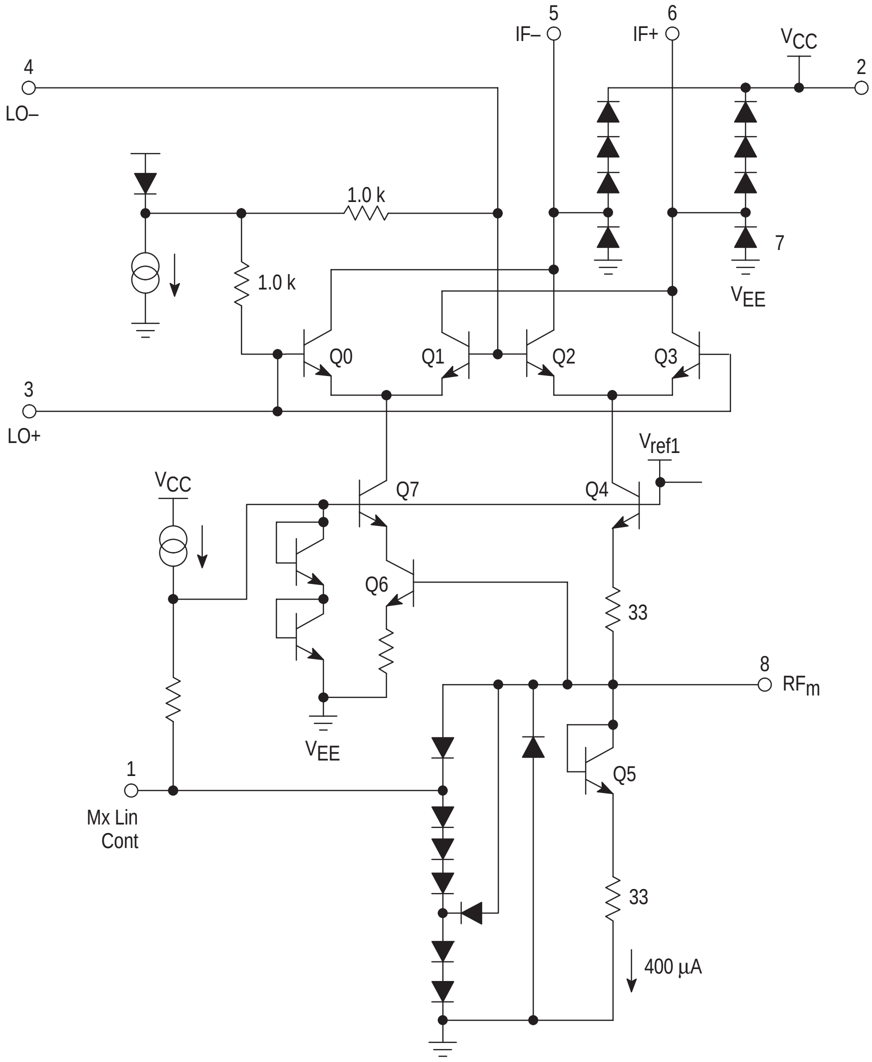
Mixer

The mixer is a unique and patented double–balanced four quadrant multiplier biased class AB allowing for programmable linearity control via an external current source. An input third order intercept point of 20 dBm may be achieved. All 3 ports of the mixer are designed to work up to 2.4 GHz. The mixer has a 50 Ω single–ended RF input and open collector differential IF outputs (see Internal Circuit Schematic for details). The linear gain of the mixer is approximately –5.0 dB with a SSB noise figure of 12 dB.

Local Oscillator

The local oscillator has differential input configuration that requires typically –10 dBm input from an external source to achieve the optimal mixer gain.

Figure 8. MC13143 Internal Circuit*



NOTE: * The MC13143 uses a unique and patented circuit topology.

APPLICATIONS INFORMATION

Evaluation PC Board

The evaluation PCB is very versatile and is intended to be used across the entire useful frequency range of this device. The PC board is laid out to accommodate all SMT components on the circuit side (see Circuit Side Component Placement View).

Component Selection

The evaluation PC board is designed to accommodate specific components, while also being versatile enough to use components from various manufacturers. The circuit side placement view is illustrated for the components specified in the application circuit. The Component Placement View specifies particular components that were used to achieve the results shown in the typical curves and tables.

Mixer Input

The mixer input impedance is broadband 50 Ω for applications up to 2.4 GHz. It easily interfaces with a RF ceramic filter as shown in the application schematic.

Mixer Linearity Control

The mixer linearity control circuit accepts approximately 0 to 2.3 mA control current. An Input Third Order Intercept Point, IIP3 of 20 dBm may be achieved at 2.3 mA of control current (approximately 7.0 mA of additional supply current).

Local Oscillator Inputs

The differential LO inputs are internally biased at V_{CC} – 1.0 V_{BE}; this is suitable for high voltage and high gain operation.

For low voltage operation, the inputs are taken to V_{CC} through 51 Ω.

IF Output

The IF is a differential open collector configuration which is designed to use over a wide frequency range for up conversion as well as down conversion.

Input/Output Matching

It is desirable to use a RF ceramic or SAW filter before the mixer to provide image frequency rejection. The filter is selected based on cost, size and performance tradeoffs. Typical RF filters have 3.0 to 5.0 dB insertion loss. The PC board layout accommodates both ceramic and SAW RF filters which are offered by various suppliers such as Siemens, Toko and Murata.

Interface matching between the RF input, RF filter and the mixer will be required. The interface matching networks shown in the application circuit are designed for 50 Ω interfaces.

Differential to single–ended circuit configuration is shown in the test circuit. 6.0 dB of additional mixer gain can be achieved by conjugately matching the output of the MiniCircuits transformer to 50 Ω at the desired IF frequency. With narrowband IF output matching the mixer performance is 3.0 dB gain and 12 dB noise figure (see Narrowband 49 and 83 MHz IF Output Matching Options). Typical insertion loss of the Toko ceramic filter is 3.0 dB. Thus, the overall gain of the circuit is 0 dB with a 15 dB noise figure.

Figure 9. Narrowband IF Output Matching with 16:1 Z Transformer and LC Network

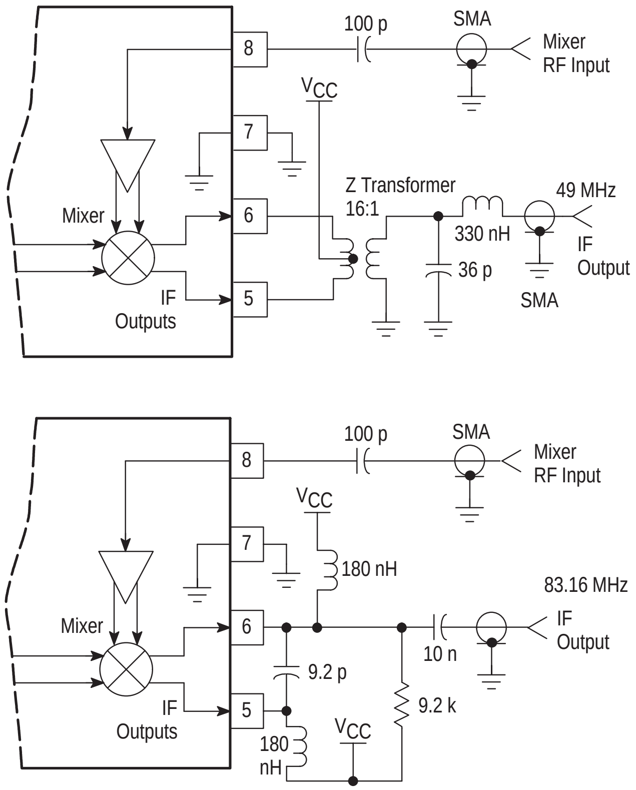
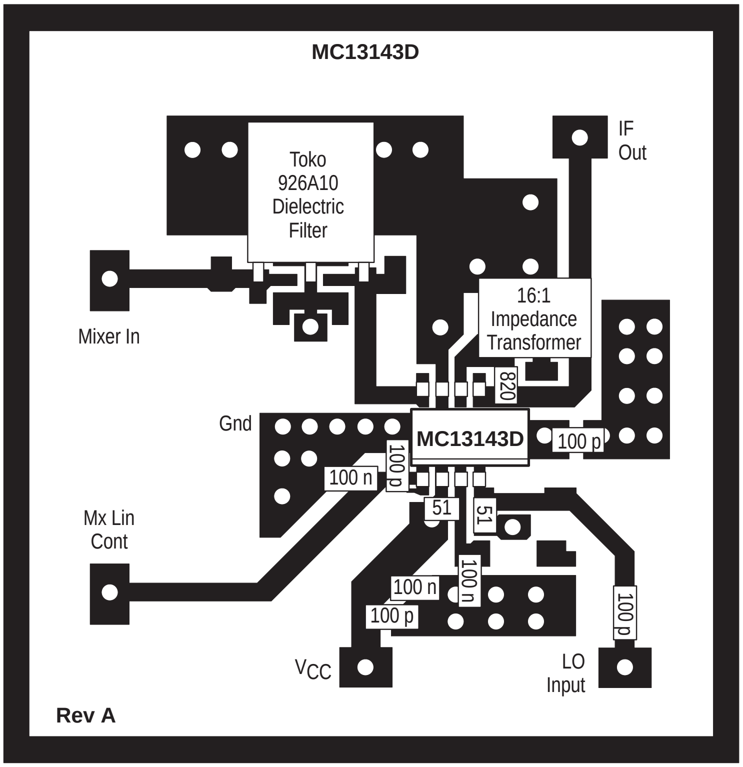


Figure 10. Circuit Side Component Placement View



NOTES: 926.5 MHz preselect dielectric filter is Toko part # 4DFA–926A10; the 4DFA (2 and 3 pole SMD type) filters are available for applications in cellular and GSM, GPS, DECT, PHS, PCS and ISM bands at 902–928 MHz, 1.8–1.9 GHz at 2.4–2.5 GHz.

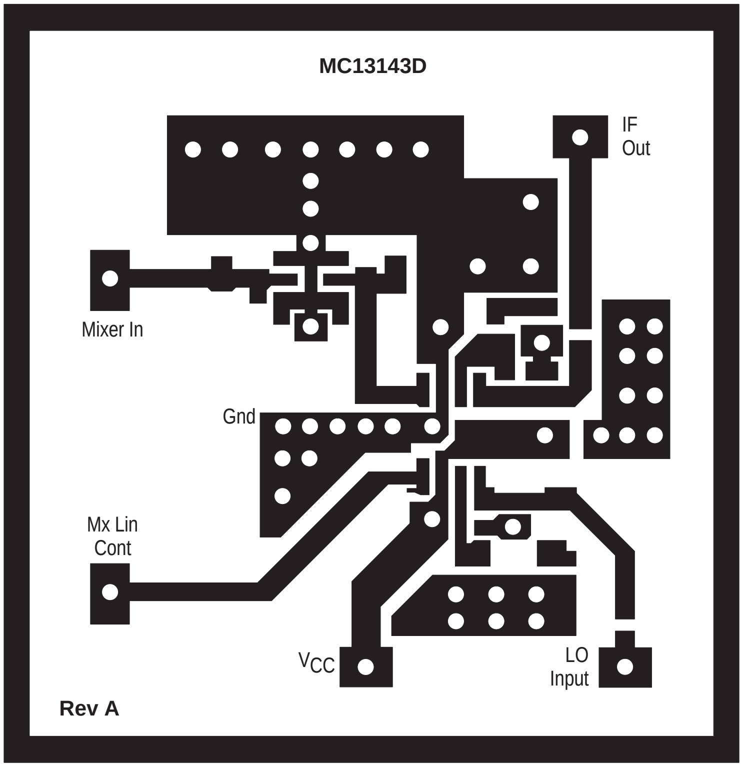
The PCB also accommodates a surface mount RF SAW filter in an eight or six pin ceramic package for the cellular base and handset frequencies. Recommended manufacturers are Siemens and Murata.

The PCB may also be used without a preselector filter; AC coupled to the mixer as shown in the test circuit schematic. All other external circuit components shown in the PCB layout above are the same as used in the test circuit schematic.

16:1 broadband impedance transformer is mini circuits part #TX16–R3T; it is in the leadless surface mount “TX” package. For a more selective narrowband match, a lowpass filter may be used after the transformer. The PCB is designed to accommodate lump inductors and capacitors in more selective narrowband matching of the mixer differential outputs to a single–ended output at a given IF frequency.

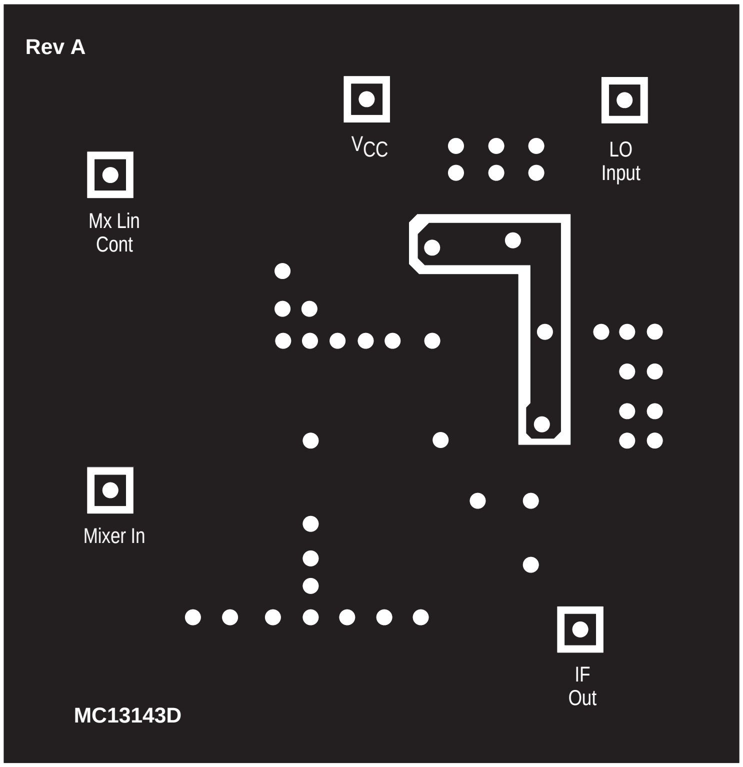
. The local oscillator may also be driven in a differential configuration using a coaxial transformer. Recommended sources are the Toko Balun transformers type B4F, B5FL and B5F (SMD component).

Figure 11. Circuit Side View



NOTES: Critical dimensions are 50 mil centers lead to lead in SO–8 footprint.
Also line widths to labeled ports excluding V_{CC} are 50 mil.

Figure 12. Ground Side View



MOTOROLA

MC13144

Product Preview

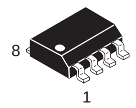
VHF - 2.0 GHz Low Noise Amplifier with Programmable Bias

The MC13144 is designed in the Motorola High Frequency Bipolar MOSIAC V™ wafer process to provide excellent performance in analog and digital communication systems. It includes a cascoded LNA usable up to 2.0 GHz and at 1.8 Vdc, with 2 bit digital programming of the LNA bias. Targeted applications are in the UHF Family Radio Services, UHF and 800 MHz Special Mobile Radio, 800 MHz Cellular and GSM, PCS, DECT and PHS at 1.8 to 2.0 GHz and Cordless Telephones in the 902 to 928 MHz band covered by FCC Title 47; Part 15. The MC13144 offers the following features:

- 17 dB Gain at 900 MHz
- 1.4 dB Noise Figure at 900 MHz
- 1.0 dB Compression Point of –7.0 dBm; Input Third Order Intercept Point of –5.0 dBm
- Low Operating Supply Voltage (1.8 to 6.0 Vdc)
- Programmable Bias with Enable 1 and Enable 2
- Enable 1 and Enable 2 Programmed High for Optimal Noise Figure and Gain Associated with NF
- Can Override Enable and Externally Program In Up to 15 mA

VHF – 2.0 GHz LOW NOISE AMPLIFIER WITH PROGRAMMABLE BIAS

SEMICONDUCTOR TECHNICAL DATA



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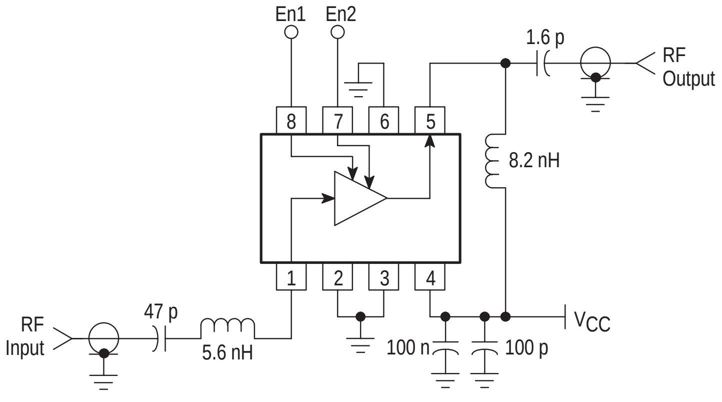
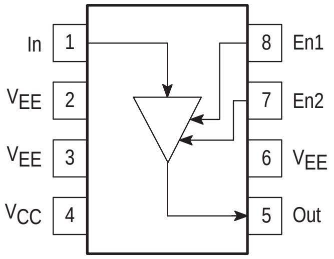
CASE 751
(SO–8)

Typical Application as 900 MHz Low Noise Amplifier



This device contains 67 active transistors.

PIN CONNECTIONS AND FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC13144D	T_A = – 40° to +85°C	SO–8

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}(max)	7.0	Vdc
Junction Temperature	T_{Jmax}	+150	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

NOTES: 1. Devices should not be operated at or outside these values. The "Recommended Operating Conditions" provide for actual device operation.

2. ESD data available upon request.

RECOMMENDED OPERATING CONDITIONS

Rating	Pin	Symbol	Value	Unit
Power Supply Voltage	4	V_{CC}	1.8 to 6.0	Vdc

DC ELECTRICAL CHARACTERISTICS (T$_A$ = 25°C; V$_{CC}$ = 3.0 Vdc; No Input Signal)

Characteristic	Condition	Pin	Symbol	Min	Typ	Max	Unit
Supply Current (Power Down)	En1 = En2 = Low	4	I_{CC}	–	100	–	pA
Supply Current (Power Up)	En1 = High En2 = Low	4	I_{CC}	–	4.2	–	mA

AC ELECTRICAL CHARACTERISTICS (T$_A$ = 25°C; V$_{CC}$ = 3.0 Vdc; f$_{RF}$ = 926.5 MHz; En1 = High; En2 = Low)

Characteristic	Condition	Pin	Symbol	Min	Typ	Max	Unit
Amplifier Gain (50 Ω Insertion Gain)	–	1, 5	S_{21}^2	–	12	–	dB
Amplifier Reverse Isolation	–	5, 1	S12	–	–35	–	dB
Amplifier Input Return Loss	–	1	Γin_{amp}	–	–10	–	dB
Amplifier Output Return Loss	–	5	Γout_{amp}	–	–15	–	dB
Input 3rd Order Intercept Point	df = 100 kHz df = 1.0 MHz	1, 5 1, 5	IIP3 IIP3	– –	–12 –5.0	– –	dBm dBm
Amplifier Gain @ NF	See Typical Application Figure	1, 5	G_{NF}	–	17	–	dB
Amplifier Noise Figure	See Typical Application Figure	1, 5	NF	–	1.4	–	dB

CIRCUIT DESCRIPTION

General

The MC13144 is a low noise amplifier with programmable bias. This device is designated for use in the front end section in analog and digital FM systems such as Wireless Local Area Network (LAN), Digital European Cordless Telephone (DECT), PHS, PCS, GPS, Cellular, UHF and 800 MHz Special Mobile Radio (SMR), UHF Family Radio Services and 902 to 928 MHz cordless telephones.

Current Regulation/Enable

Temperature compensating voltage independent current regulation is digitally controlled by a 2 bit programmable bias/enable circuit.

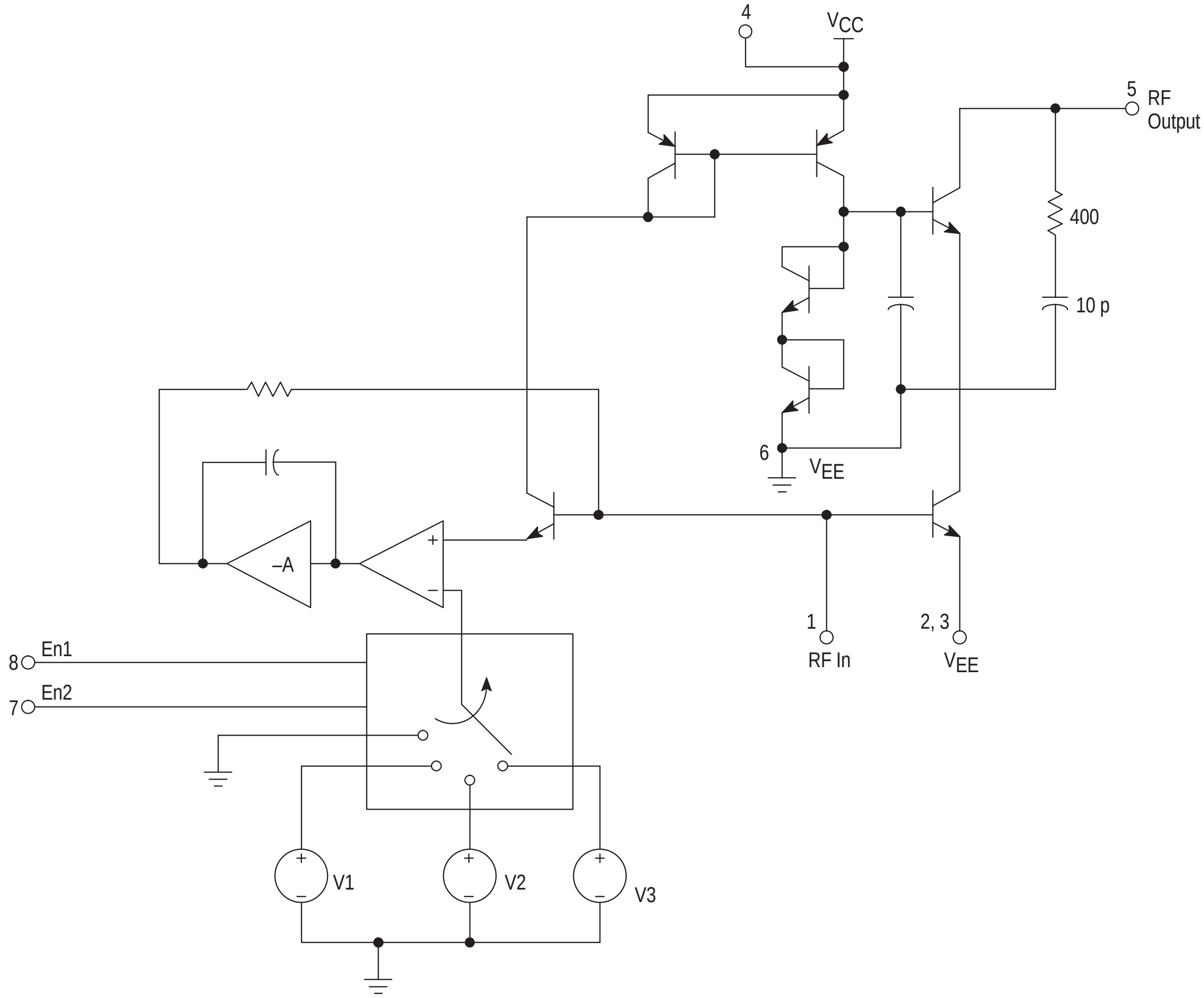
LNA

The LNA is a unique and patented cascode amplifier with digitally (2 bit) programmable bias (see Internal Circuit Schematic). Typical gain of the LNA is 17 dB for minimum noise figure of 1.4 dB at 900 MHz.

Programmable Bias/Enable Circuit

This unique circuit allows for 3 bias levels and a standby mode in which the LNA can be externally biased as desired.

Figure 1. MC13144 Internal Circuit*



NOTE: * The MC13144 uses a unique and patent pending circuit topology.

APPLICATIONS INFORMATION

Evaluation PC Board

The evaluation PCB is very versatile and is intended to be used across the entire useful frequency range of this device. The PC board layout accommodates all SMT components on the circuit side (see Circuit Side Component Placement View).

Component Selection

The evaluation PC board is laid out for the 4DFA (2 pole SMD Type) and 4DFB (3 pole SMD Type) filters which are available for applications in Cellular and GSM, GPS (1.2 to 1.5 GHz), DECT, PHS and PCS (1.8 to 2.0 GHz) and ISM Bands (902 to 928 MHz and 2.4 to 2.5 GHz). In the 926.5 MHz Application Circuit, a ceramic deielectric filter is used (Toko part # 4DFA–926A10).

LNA Input/Output

The LNA input impedance is the base of a common emitter cascode amplifier. The LNA output is the collector of the cascode stage and it is loaded with a series resistor of 400 Ω and a capacitor of 10 pF to provide stability.

Digitally Programmable Bias/Enable

The LNA is enabled by a 2 bit (En1 and En2) programmable bias circuit. The internal circuit shows the comparator circuit which programs the internal regulator. The logic table below shows the bias and typical performance.

I_{CC}/Gain	En2 Low	En2 High
En1 Low	0 mA/0 dB	2.0 mA/13 dB
En1 High	4.2 mA/17.0 dB	9.4 mA/18 dB

Input/Output Matching

A typical application at 900 MHz yields 17 dB gain and 1.4 dB noise figure. In this circuit a series inductor of 5.6 nH is used to match the input and a shunt inductor of 8.2 nH which also serves as an RFC and a series capacitor of 0.9 p is used to match the LNA output to 50 Ω load impedance.

It may be desirable to use a RF ceramic or SAW filter after the LNA when driving a mixer to provide image frequency rejection. The image filter is selected based on cost, size and performance tradeoffs. Typical RF filters have 3.0 to 5.0 dB insertion loss. Interface matching between the RF input, RF filter and the mixer is shown in Application Circuit and the Component Placement View.

Figure 2. MC13144D Application Circuit
(926.5 MHz)

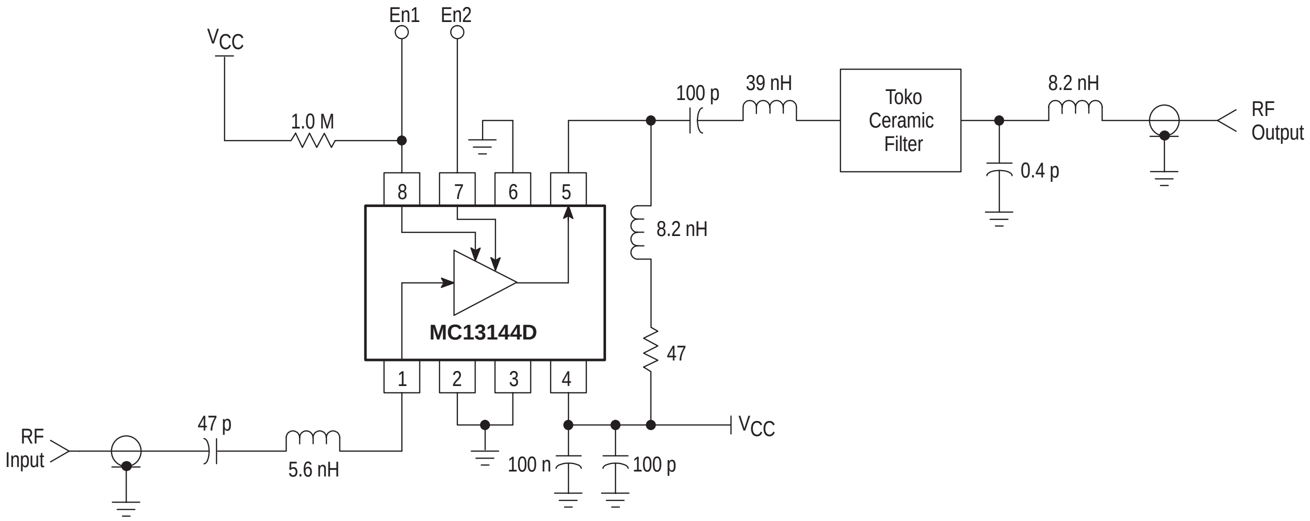


Figure 3. Circuit Side Component Placement View

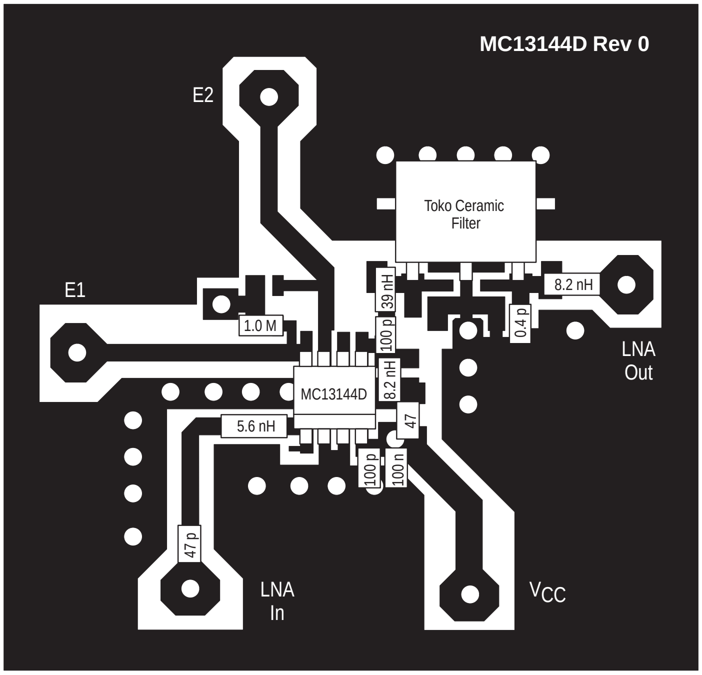
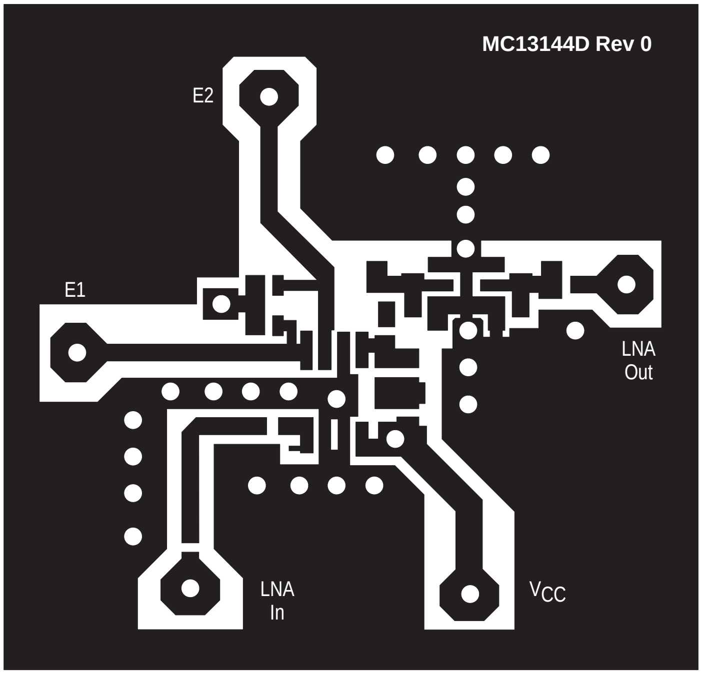
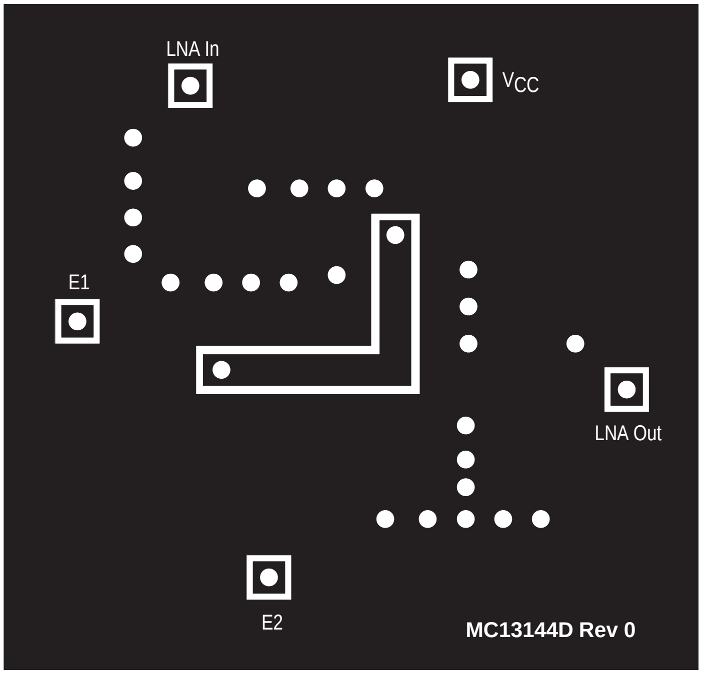


Figure 4. Circuit Side View



NOTES: Critical dimensions are 50 MIL centers lead to lead in SO–8 footprint.
Also line widths to labeled ports excluding V_{CC}, E1 and E2 are 50 MIL (0.050 inch).
FR4 PCB, 1/32 inch.

Figure 5. Ground Side View



NOTES: FR4 PCB, 1/32 inch.

MOTOROLA

MC13150

Narrowband FM Coilless Detector IF Subsystem

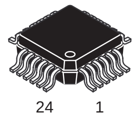
The MC13150 is a narrowband FM IF subsystem targeted at cellular and other analog applications. Excellent high frequency performance is achieved, with low cost, through use of Motorola's MOSAIC 1.5™ RF bipolar process. The MC13150 has an onboard Colpitts VCO for Crystal controlled second LO in dual conversion receivers. The mixer is a double balanced configuration with excellent third order intercept. It is useful to beyond 200 MHz. The IF amplifier is split to accommodate two low cost cascaded filters. RSSI output is derived by summing the output of both IF sections. The quadrature detector is a unique design eliminating the conventional tunable quadrature coil.

Applications for the MC13150 include cellular, CT–1 900 MHz cordless telephone, data links and other radio systems utilizing narrowband FM modulation.

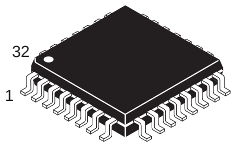
- Linear Coilless Detector
- Adjustable Demodulator Bandwidth
- 2.5 to 6.0 Vdc Operation
- Low Drain Current: < 2.0 mA
- Typical Sensitivity of 2.0 µV for 12 dB SINAD
- IIP3, Input Third Order Intercept Point of 0 dBm
- RSSI Range of Greater Than 100 dB
- Internal 1.4 kΩ Terminations for 455 kHz Filters
- Split IF for Improved Filtering and Extended RSSI Range

NARROWBAND FM COILLESS DETECTOR IF SUBSYSTEM FOR CELLULAR AND ANALOG APPLICATIONS

SEMICONDUCTOR TECHNICAL DATA



FTA SUFFIX
PLASTIC PACKAGE
CASE 977
(Thin QFP)

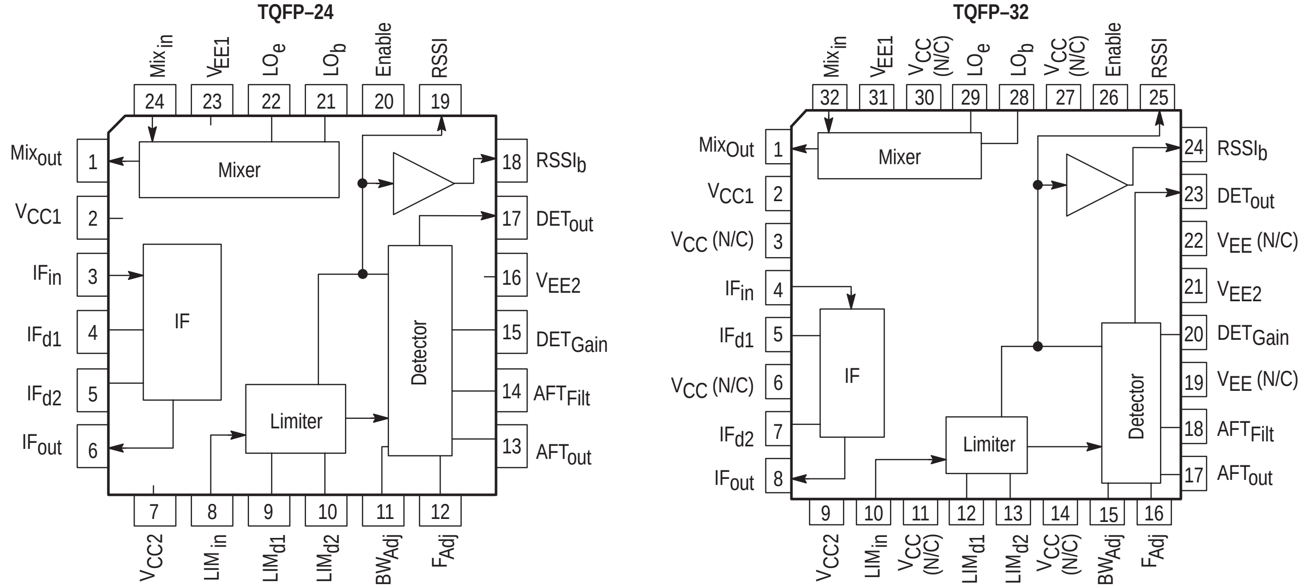


FTB SUFFIX
PLASTIC PACKAGE
CASE 873
(Thin QFP)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC13150FTA	T_A = –40 ° to +85°C	TQFP–24
MC13150FTB		TQFP–32

PIN CONNECTIONS



MAXIMUM RATINGS

Rating	Pin	Symbol	Value	Unit
Power Supply Voltage	2, 9	V_{CC}(max)	6.5	Vdc
Junction Temperature	–	T_{Jmax}	+150	°C
Storage Temperature Range	–	T_{stg}	– 65 to +150	°C

NOTE: 1. Devices should not be operated at or outside these values. The "Recommended Operating Limits" provide for actual device operation.

2. ESD data available upon request.

RECOMMENDED OPERATING CONDITIONS

Rating	Pin	Symbol	Value	Unit
Power Supply Voltage T_A = 25°C – 40°C ≤ T_A ≤ 85°C (See Figure 22)	2, 9 21, 31	V_{CC} V_{EE}	2.5 to 6.0 0	Vdc
Input Frequency	32	f_{in}	10 to 500	MHz
Ambient Temperature Range	-	T_A	– 40 to + 85	°C
Input Signal Level	32	V_{in}	0	dBm

DC ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC1} = V_{CC2} = 3.0 Vdc, No Input Signal.)

Characteristics	Condition	Pin	Symbol	Min	Typ	Max	Unit
Total Drain Current (See Figure 2)	V_S = 3.0 Vdc	2 + 9	I_{TOTAL}	–	1.7	3.0	mA
Supply Current, Power Down (See Figure 3)	–	2 + 9	–	–	40	–	nA

AC ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_S = 3.0 Vdc, f_{RF} = 50 MHz, f_{LO} = 50.455 MHz, LO Level = –10 dBm, see Figure 1 Test Circuit*, unless otherwise specified.)

Characteristics	Condition	Pin	Symbol	Min	Typ	Max	Unit
12 dB SINAD Sensitivity (See Figure 15)	f_{mod} = 1.0 kHz; f_{dev} = ± 5.0 kHz	32	–	–	–100	–	dBm
RSSI Dynamic Range (See Figure 7)	–	25	–	–	100	–	dB
Input 1.0 dB Compression Point Input 3rd Order Intercept Point (See Figure 18)	– –	– –	1.0 dB C. Pt. IIP3	– –	–11 –1.0	– –	dBm
Coilless Detector Bandwidth Adjust (See Figure 11)	Measured with No IF Filters	–	ΔBW adj	–	26	–	kHz/µA
MIXER							
Conversion Voltage Gain (See Figure 5)	P_{in} = – 30 dBm; PLO = –10 dBm	32	–	–	10	–	dB
Mixer Input Impedance	Single–Ended	32	–	–	200	–	Ω
Mixer Output Impedance	–	1	–	–	1.5	–	kΩ
LOCAL OSCILLATOR							
LO Emitter Current (See Figure 26)	–	29	–	30	63	100	µA
IF & LIMITING AMPLIFIERS SECTION							
IF and Limiter RSSI Slope	Figure 7	25	–	–	0.4	–	µA/dB
IF Gain	Figure 8	4, 8	–	–	42	–	dB
IF Input & Output Impedance	–	4, 8	–	–	1.5	–	kΩ
Limiter Input Impedance	–	10	–	–	1.5	–	kΩ
Limiter Gain	–	–	–	–	96	–	dB

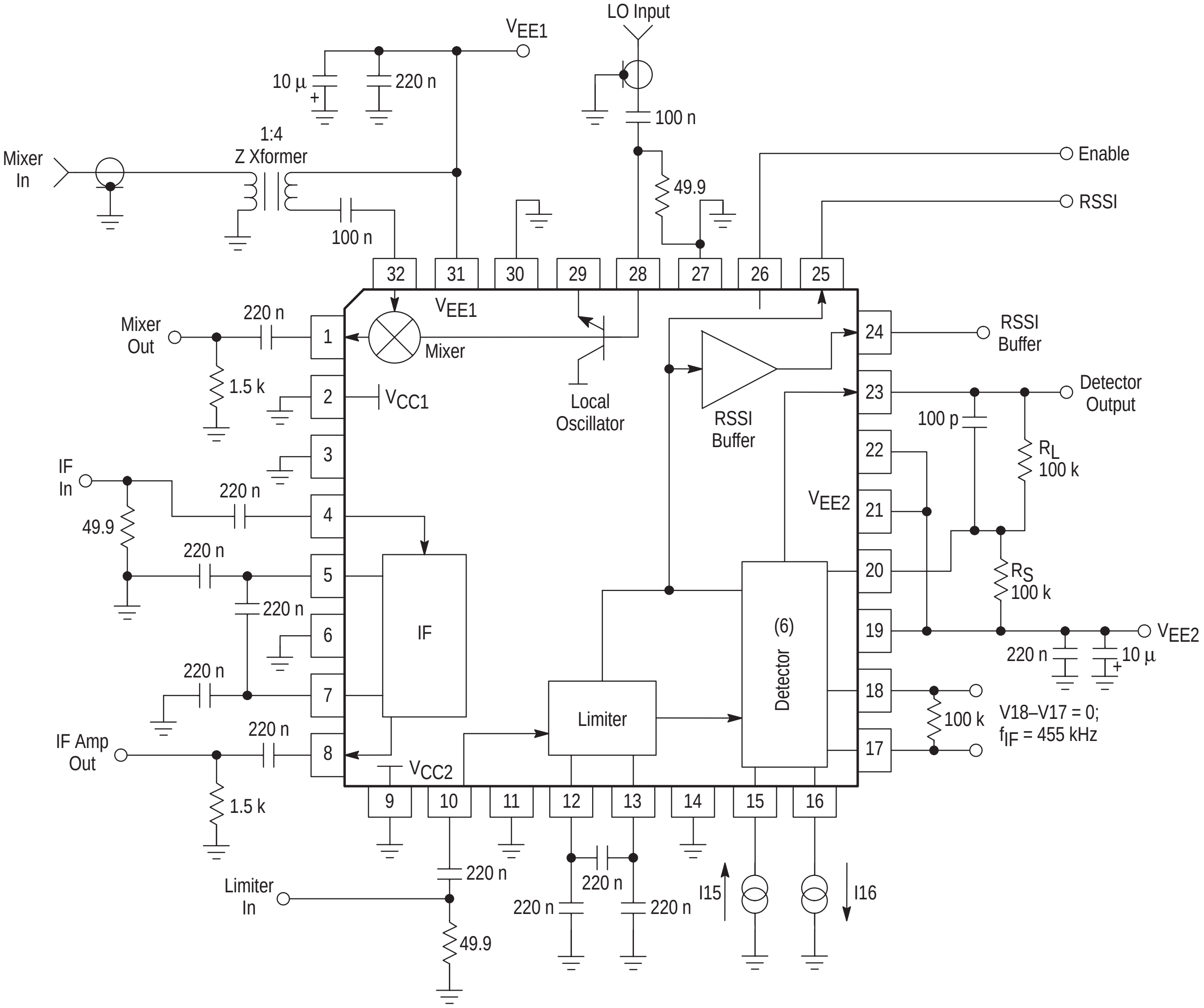
* Figure 1 Test Circuit uses positive (V_{CC}) Ground.

AC ELECTRICAL CHARACTERISTICS (continued) (T_A = 25°C, V_S = 3.0 Vdc, f_{RF} = 50 MHz, f_{LO} = 50.455 MHz, LO Level = –10 dBm, see Figure 1 Test Circuit*, unless otherwise specified.)

Characteristics	Condition	Pin	Symbol	Min	Typ	Max	Unit
DETECTOR							
Frequency Adjust Current	Figure 9, f_{IF} = 455 kHz	16	–	41	49	56	µA
Frequency Adjust Voltage	Figure 10, f_{IF} = 455 kHz	16	–	600	650	700	mVdc
Bandwidth Adjust Voltage	Figure 12, I_{15} = 1.0 µA	15	–	–	570	–	mVdc
Detector DC Output Voltage (See Figure 25)	–	23	–	–	1.36	–	Vdc
Recovered Audio Voltage	f_{dev} = ±3.0 kHz	23	–	85	122	175	mVrms

* Figure 1 Test Circuit uses positive (V_{CC}) Ground.

Figure 1. Test Circuit



This device contains 292 active transistors.

MC13150 CIRCUIT DESCRIPTION

General

The MC13150 is a very low power single conversion narrowband FM receiver incorporating a split IF. This device is designated for use as the backend in analog narrowband FM systems such as cellular, 900 MHz cordless phones and narrowband data links with data rates up to 9.6 k baud. It contains a mixer, oscillator, extended range received signal strength indicator (RSSI), RSSI buffer, IF amplifier, limiting IF, a unique coilless quadrature detector and a device enable function (see Package Pin Outs/Block Diagram).

Low Current Operation

The MC13150 is designed for battery and portable applications. Supply current is typically 1.7 mAdc at 3.0 Vdc. Figure 2 shows the supply current versus supply voltage.

Enable

The enable function is provided for battery powered operation. The enabled pin is pulled down to enable the regulators. Figure 3 shows the supply current versus enable voltage, V_{enable} (relative to V_{CC}) needed to enable the device. Note that the device is fully enabled at V_{CC} – 1.3 Vdc. Figure 4 shows the relationship of enable current, I_{enable} to enable voltage, V_{enable}.

Mixer

The mixer is a double–balanced four quadrant multiplier and is designed to work up to 500 MHz. It has a single ended input. Figure 5 shows the mixer gain and saturated output response as a function of input signal drive and for –10 dBm LO drive level. This is measured in the application circuit shown in Figure 15 in which a single LC matching network is used. Since the single–ended input impedance of the mixer is 200 Ω, an alternate solution uses a 1:4 impedance transformer to match the mixer to 50 Ω input impedance. The linear voltage gain of the mixer alone is approximately 4.0 dB (plus an additional 6.0 dB for the transformer). Figure 6 shows the mixer gain versus the LO input level for various mixer input levels at 50 MHz RF input.

The buffered output of the mixer is internally loaded, resulting in an output impedance of 1.5 kΩ.

Local Oscillator

The on–chip transistor operates with crystal and LC resonant elements up to 220 MHz. Series resonant, overtone crystals are used to achieve excellent local oscillator stability. 3rd overtone crystals are used through about 65 to 70 MHz. Operation from 70 MHz up to 200 MHz is feasible using the on–chip transistor with a 5th or 7th overtone crystal. To enhance operation using an overtone crystal, the internal transistor's bias is increased by adding an external resistor from Pin 29 (in 32 pin QFP package) to V_{EE} to keep the oscillator on continuously or it may be taken to the enable pin to shut it off when the receiver is disabled. –10 dBm of local oscillator drive is needed to adequately drive the mixer (Figure 6). The oscillator configurations specified above are described in the application section.

RSSI

The received signal strength indicator (RSSI) output is a current proportional to the log of the received signal amplitude. The RSSI current output is derived by summing the currents from the IF and limiting amplifier stages. An external resistor at Pin 25 (in 32 pin QFP package) sets the voltage range or swing of the RSSI output voltage. Linearity of the RSSI is optimized by using external ceramic bandpass filters which have an insertion loss of 4.0 dB. The RSSI circuit is designed to provide 100+ dB of dynamic range with temperature compensation (see Figures 7 and 23 which show the RSSI response of the applications circuit).

RSSI Buffer

The RSSI buffer has limitations in what loads it can drive. It can pull loads well towards the positive and negative supplies, but has problems pulling the load away from the supplies. The load should be biased at half supply to overcome this limitation.

Figure 2. Supply Current versus Supply Voltage

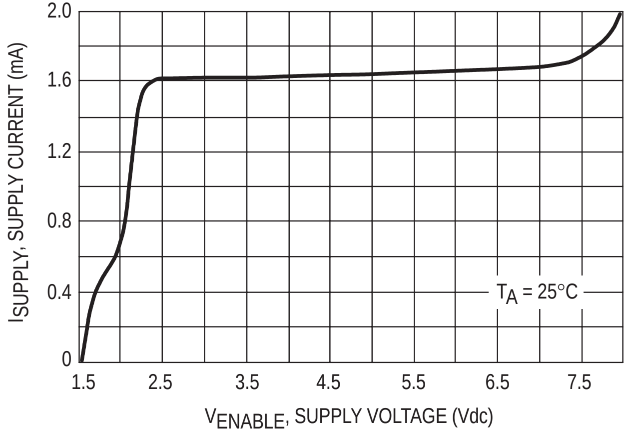


Figure 3. Supply Current versus Enable Voltage

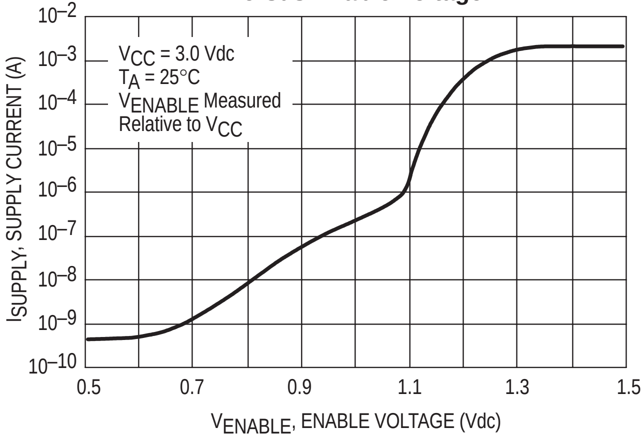


Figure 4. Enable Current versus Enable Voltage

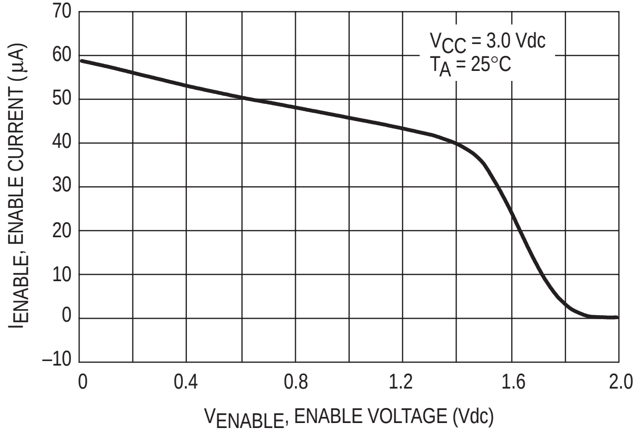


Figure 5. Mixer IF Output Level versus RF Input Level

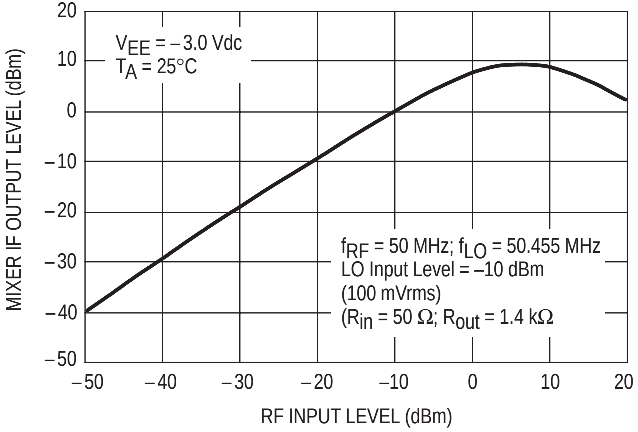


Figure 6. Mixer IF Output Level versus Local Oscillator Input Level

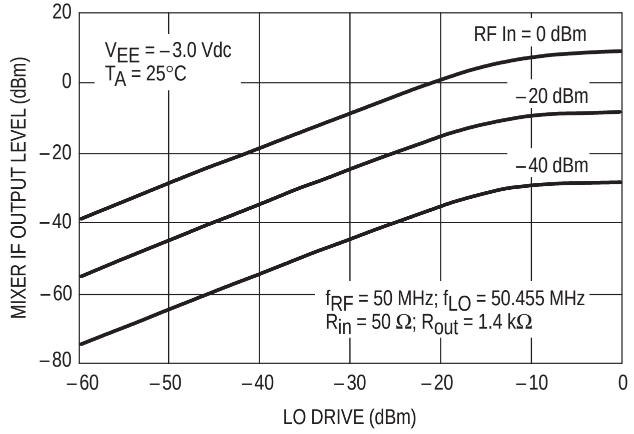
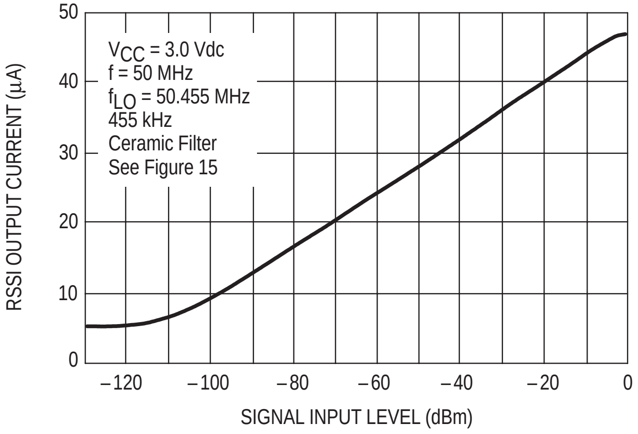


Figure 7. RSSI Output Current versus Input Signal Level



IF Amplifier

The first IF amplifier section is composed of three differential stages. This section has internal dc feedback and external input decoupling for improved symmetry and stability. The total gain of the IF amplifier block is approximately 42 dB at 455 kHz. Figure 8 shows the gain of the IF amplifier as a function of the IF frequency.

The fixed internal input impedance is 1.5 kΩ; it is designed for applications where a 455 kHz ceramic filter is used and no external output matching is necessary since the filter requires a 1.5 kΩ source and load impedance.

Overall RSSI linearity is dependent on having total midband attenuation of 10 dB (4.0 dB insertion loss plus 6.0 dB impedance matching loss) for the filter. The output of the IF amplifier is buffered and the impedance is 1.5 kΩ.

Limiter

The limiter section is similar to the IF amplifier section except that six stages are used. The fixed internal input impedance is 1.5 kΩ. The total gain of the limiting amplifier section is approximately 96 dB. This IF limiting amplifier section internally drives the quadrature detector section.

Figure 8. IF Amplifier Gain versus IF Frequency

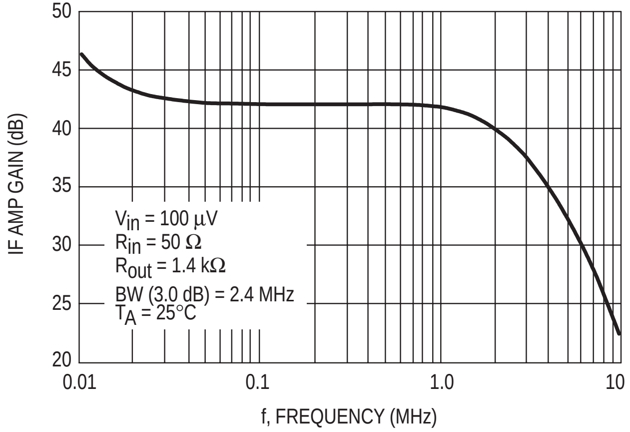


Figure 9. F_{adj} Current versus IF Frequency

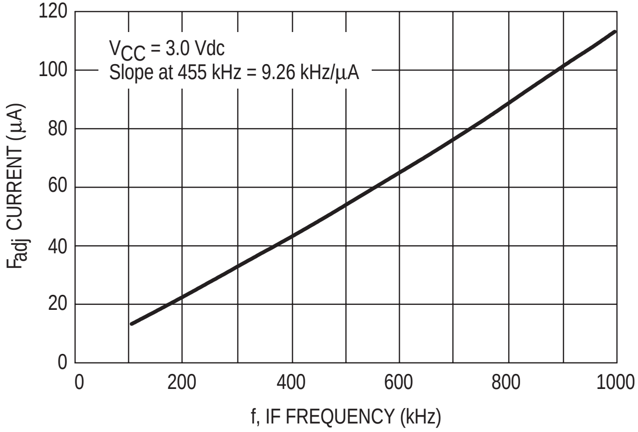


Figure 10. F_{adj} Voltage versus F_{adj} Current

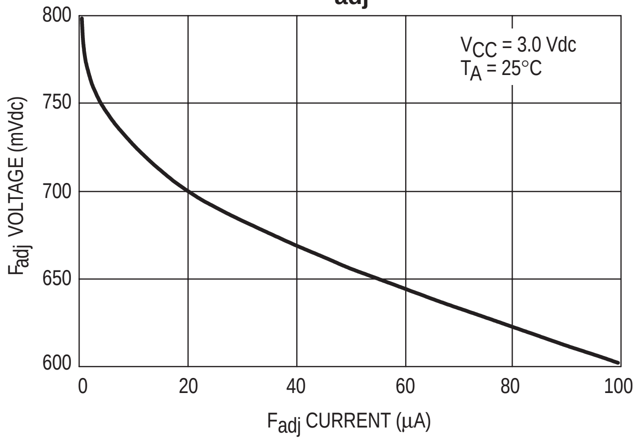
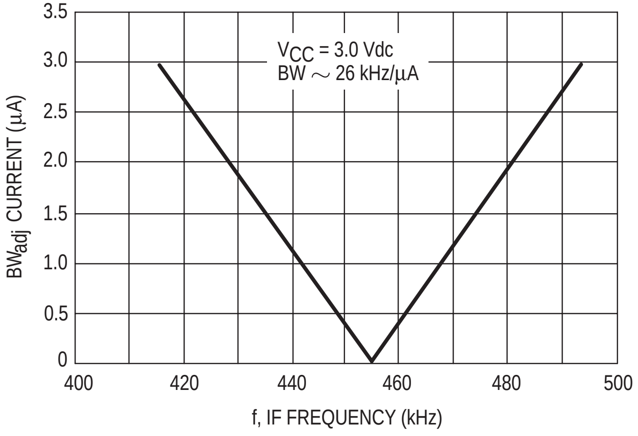


Figure 11. BW_{adj} Current versus IF Frequency



Coilless Detector

The quadrature detector is similar to a PLL. There is an internal oscillator running at the IF frequency and two detector outputs. One is used to deliver the audio signal and the other one is filtered and used to tune the oscillator.

The oscillator frequency is set by an external resistor at the F_{adj} pin. Figure 9 shows the control current required for a particular frequency; Figure 10 shows the pin voltage at that current. From this the value of R_F is chosen. For example, 455 kHz would require a current of around 50 µA. The pin voltage (Pin 16 in the 32 pin QFP package) is around 655mV giving a resistor of 13.1 kΩ. Choosing 12 kΩ as the nearest standard value gives a current of approximately 55 µA. The 5.0 µA difference can be taken up by the tuning resistor, R_T.

The best nominal frequency for the AFT_{out} pin (Pin 17) would be half supply. A supply voltage of 3.0 Vdc suggests a resistor value of (1.5 – 0.655)V/5µA = 169 kΩ. Choosing 150 kΩ would give a tuning current of 3/150 k = 20 µA. From Figure 9 this would give a tuning range of roughly 10 kHz/µA or ± 100 kHz which should be adequate.

The bandwidth can be adjusted with the help of Figure 11. For example, 1.0 µA would give a bandwidth of ± 13 kHz. The voltage across the bandwidth resistor, R_B from Figure 12 is V_{CC} – 2.44 Vdc = 0.56 Vdc for V_{CC} = 3.0 Vdc., so R_B = 0.56V/1.0 µA = 560 kΩ. Actually the locking range will be ±13 kHz while the audio bandwidth will be approximately ±8.4 kHz due to an internal filter capacitor. This is verified in Figure 13. For some applications it may be desirable that the audio bandwidth is increased; this is done by reducing R_B. Reducing R_B widens the detector bandwidth and improves the distortion at high input levels at the expense of 12 dB SINAD sensitivity. The low frequency 3.0dB point is set by the tuning circuit such that the product

$$R_T C_T = 0.68/f3dB.$$

So, for example, 150 k and 1.0 µF give a 3.0 dB point of 4.5 Hz. The recovered audio is set by R_L to give roughly 50mV per kHz deviation per 100 k of resistance. The dc level can be shifted by R_S from the nominal 0.68 V by the following equation:

$$\text{Detector DC Output} = ((R_L + R_S)/R_S)\ 0.68\ \text{Vdc}$$

Thus, $R_S = R_L$ sets the output at 2 x 0.68 = 1.36 V; $R_L = 2R_S$ sets the output at 3 x 0.68 = 2.0 V.

Figure 12. BW_{adj} Current versus BW_{adj} Voltage

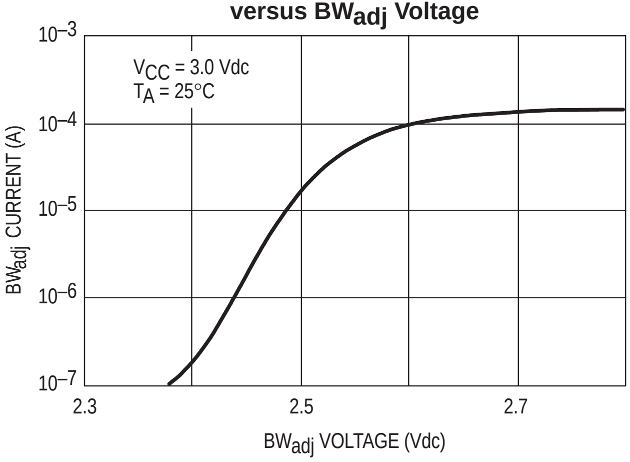
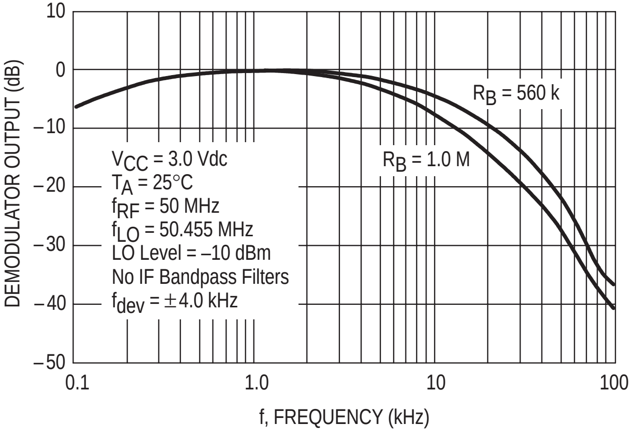


Figure 13. Demodulator Output versus Frequency



APPLICATIONS INFORMATION

Evaluation PC Board

The evaluation PCB is very versatile and is intended to be used across the entire useful frequency range of this device. The center section of the board provides an area for attaching all SMT components to the circuit side and radial leaded components to the component ground side (see Figures 29 and 30). Additionally, the peripheral area surrounding the RF core provides pads to add supporting and interface circuitry as a particular application dictates. There is an area dedicated for a LNA preamp. This evaluation board will be discussed and referenced in this section.

Component Selection

The evaluation PC board is designed to accommodate specific components, while also being versatile enough to use components from various manufacturers and coil types. The applications circuit schematic (Figure 15) specifies particular components that were used to achieve the results shown in the typical curves but equivalent components should give similar results. Component placement views are shown in Figures 27 and 28 for the application circuit in Figure 15 and for the 83.616 MHz crystal oscillator circuit in Figure 16.

Input Matching Components

The input matching circuit shown in the application circuit schematic (Figure 15) is a series L, shunt C single L section which is used to match the mixer input to 50 Ω. An alternative input network may use 1:4 surface mount transformers or BALUNs. The 12 dB SINAD sensitivity using the 1:4 impedance transformer is typically –100 dBm for f_{mod} = 1.0 kHz and f_{dev} = ±5.0 kHz at f_{in} = 50 MHz and f_{LO} = 50.455 MHz (see Figure 14).

It is desirable to use a SAW filter before the mixer to provide additional selectivity and adjacent channel rejection and improved sensitivity. SAW filters sourced from Toko (Part # SWS083GBWA) and Murata (Part # SAF83.16MA51X) are excellent choices to easily interface with the MC13150 mixer. They are packaged in a 12 pin low profile surface mount ceramic package. The center frequency is 83.161 MHz and the 3.0 dB bandwidth is 30 kHz.

Figure 14. S+N+D, N+D, N, 30% AMR versus Input Signal Level

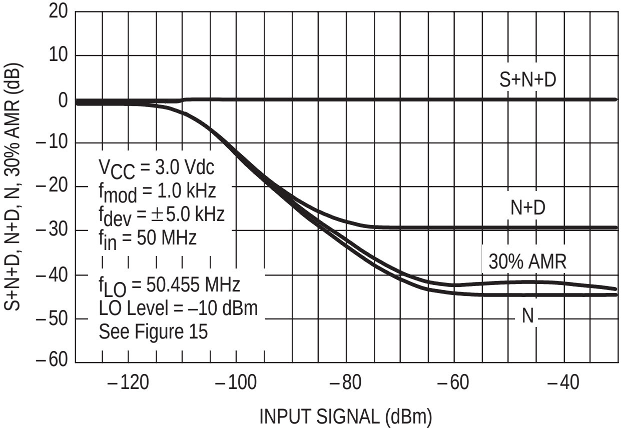
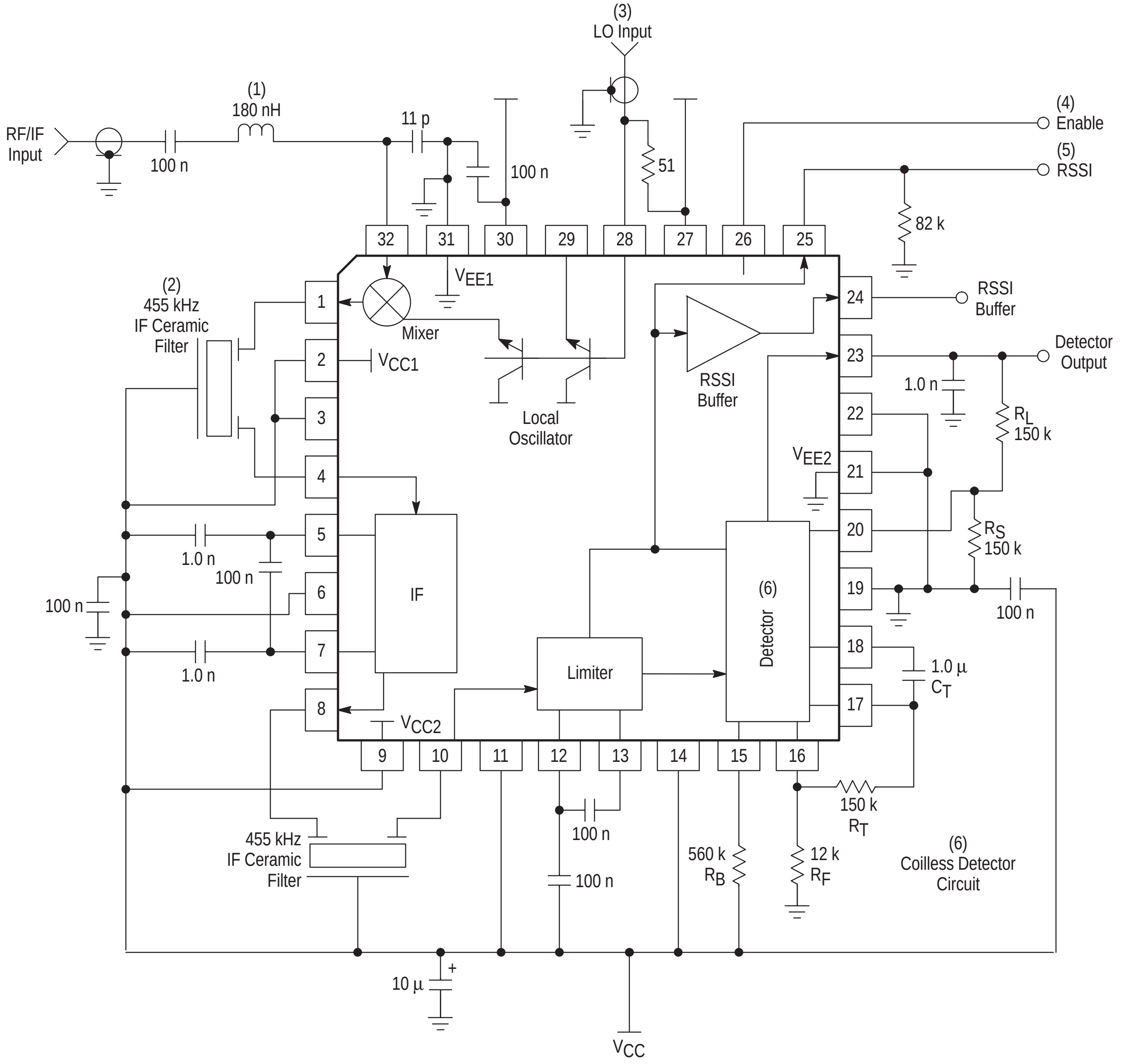


Figure 15. Application Circuit



NOTES: 1. Alternate solution is 1:4 impedance transformer (sources include Mini Circuits, Coilcraft and Toko).
2. 455 kHz ceramic filters (source Murata CFU455 series which are selected for various bandwidths).
3. For external LO source, a 51 Ω pull–up resistor is used to bias the base of the on–board transistor as shown in Figure 15. Designer may provide local oscillator with 3rd, 5th, or 7th overtone crystal oscillator circuit. The PC board is laid out to accommodate external components needed for a Butler emitter coupled crystal oscillator (see Figure 16).
4. Enable IC by switching the pin to V_{EE}.
5. The resistor is chosen to set the range of RSSI voltage output swing.
6. Details regarding the external components to setup the coilless detector are provided in the application section.

Local Oscillators

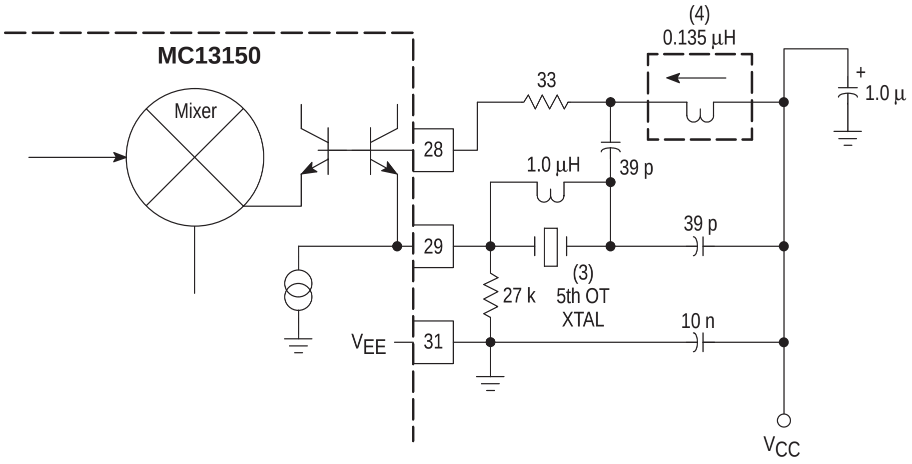
HF & VHF Applications

In the application schematic, an external sourced local oscillator is utilized in which the base is biased via a 51 Ω resistor to V_{CC}. However, the on–chip grounded collector transistor may be used for HF and VHF local oscillators with higher order overtone crystals. Figure 16 shows a 5th overtone oscillator at 83.616 MHz. The circuit uses a Butler overtone oscillator configuration. The amplifier is an emitter follower. The crystal is driven from the emitter and is coupled to the high impedance base through a capacitive tap network. Operation at the desired overtone frequency is ensured by the parallel resonant circuit formed by the variable inductor and the tap capacitors and parasitic capacitances of the on–chip transistor and PC board. The variable inductor specified in the schematic could be replaced with a high tolerance, high Q ceramic or air wound surface mount component if the other components have tight enough tolerances. A variable inductor provides an adjustment for gain and frequency of the resonant tank ensuring lock up and start–up of the crystal oscillator. The overtone crystal is chosen with ESR of typically 80 Ω and 120 Ω maximum; if the resistive loss in the crystal is too high the performance of oscillator may be impacted by lower gain margins.

A series LC network to ac ground (which is V_{CC}) is comprised of the inductance of the base lead of the on–chip transistor and PC board traces and tap capacitors. Parasitic oscillations often occur in the 200 to 800 MHz range. A small resistor is placed in series with the base (Pin 28) to cancel the negative resistance associated with this undesired mode of oscillation. Since the base input impedance is so large, a small resistor in the range of 27 to 68 Ω has very little effect on the desired Butler mode of oscillation.

The crystal parallel capacitance, C_o, provides a feedback path that is low enough in reactance at frequencies of 5th overtones or higher to cause trouble. C_o has little effect near resonance because of the low impedance of the crystal motional arm (R_m–L_m–C_m). As the tunable inductor, which forms the resonant tank with the tap capacitors, is tuned off the crystal resonant frequency, it may be difficult to tell if the oscillation is under crystal control. Frequency jumps may occur as the inductor is tuned. In order to eliminate this behavior an inductor, L_o, is placed in parallel with the crystal. L_o is chosen to resonant with the crystal parallel capacitance, C_o, at the desired operation frequency. The inductor provides a feedback path at frequencies well below resonance; however, the parallel tank network of the tap capacitors and tunable inductor prevent oscillation at these frequencies.

Figure 16. MC13150FTB Overtone Oscillator
f_{RF} = 83.16 MHz; f_{LO} = 83.616 MHz
5th Overtone Crystal Oscillator



Receiver Design Considerations

The curves of signal levels at various portions of the application receiver with respect to RF input level are shown in Figure 17. This information helps determine the network topology and gain blocks required ahead of the MC13150 to achieve the desired sensitivity and dynamic range of the receiver system. The PCB is laid out to accommodate a low noise preamp followed by the 83.16 MHz SAW filter. In the application circuit (Figure 15), the input 1.0 dB compression point is –10 dBm and the input third order intercept (IP3) performance of the system is approximately 0 dBm (see Figure 18).

Typical Performance Over Temperature

Figures 19–26 show the device performance over temperature.

Figure 17. Signal Levels versus RF Input Signal Level

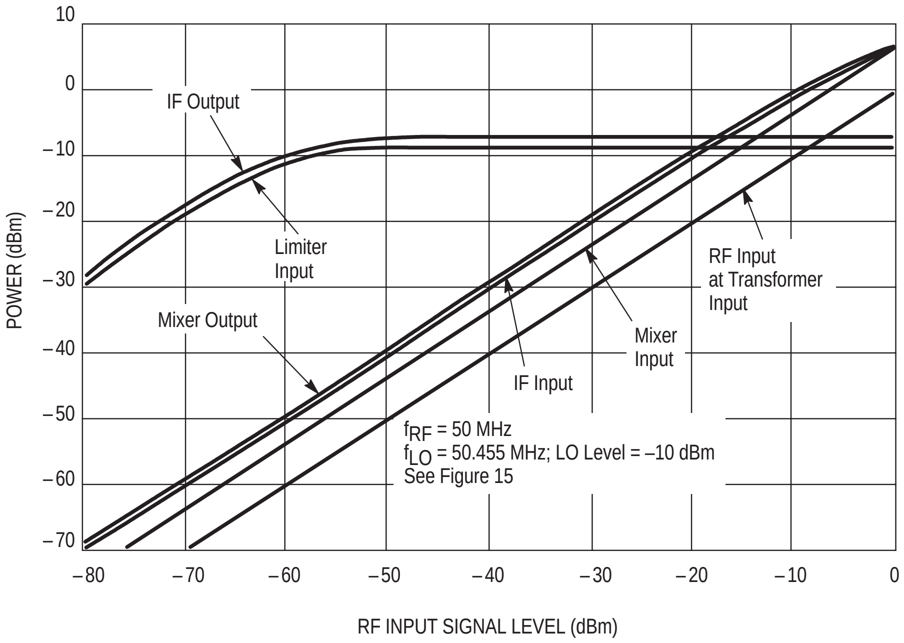
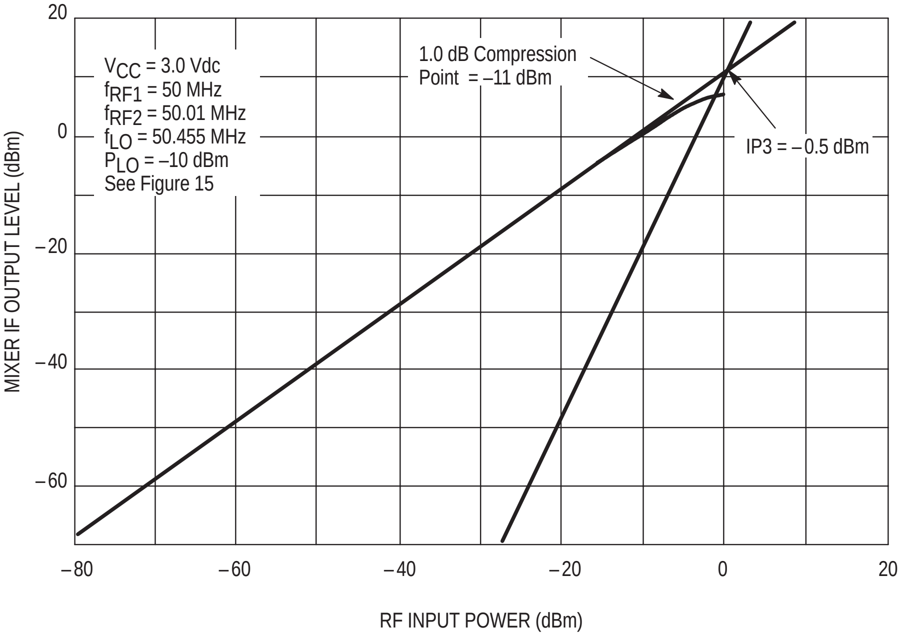


Figure 18. 1.0 dB Compression Point and Input Third Order Intercept Point versus Input Power



TYPICAL PERFORMANCE OVER TEMPERATURE

Figure 19. Supply Current, I_{VEE1} versus Signal Input Level

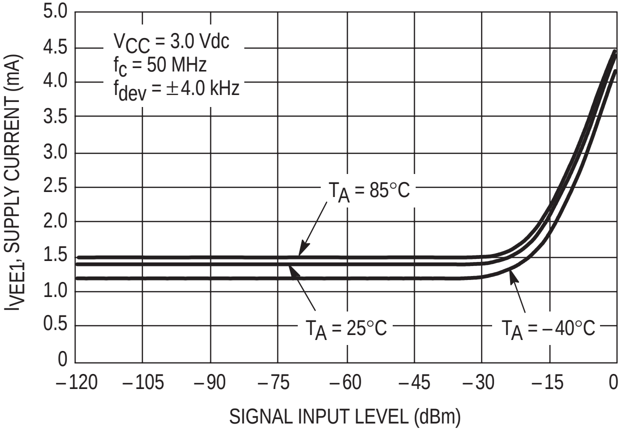
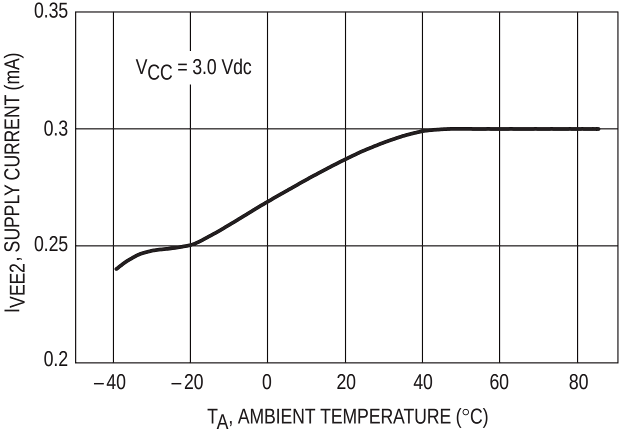


Figure 20. Supply Current, I_{VEE2} versus Ambient Temperature



TYPICAL PERFORMANCE OVER TEMPERATURE

Figure 21. Total Supply Current versus Ambient Temperature

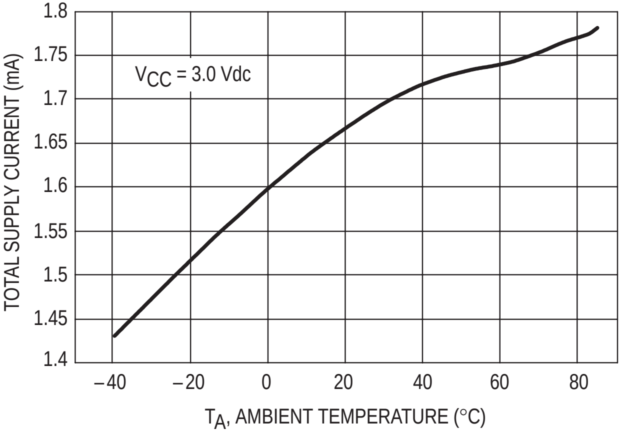


Figure 22. Minimum Supply Voltage versus Ambient Temperature

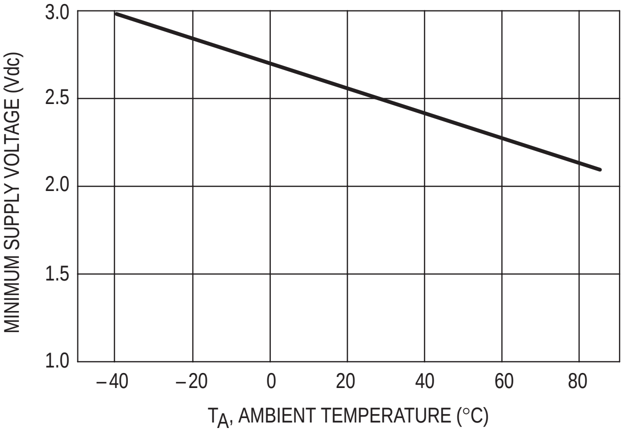


Figure 23. RSSI Current versus Ambient Temperature and Signal Level

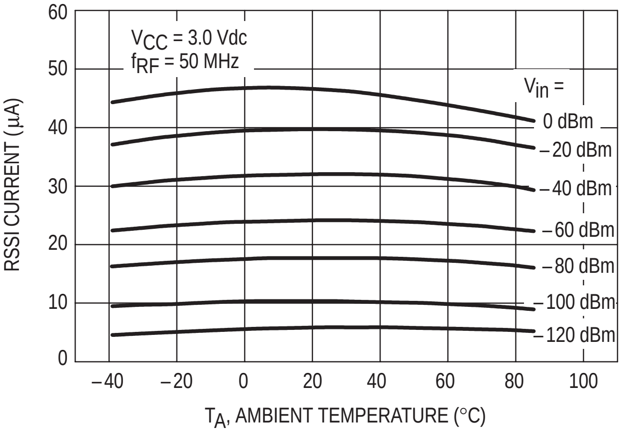


Figure 24. Recovered Audio versus Ambient Temperature

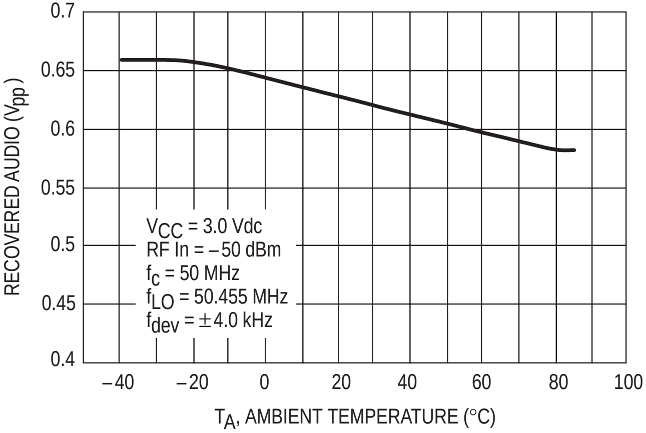


Figure 25. Demod DC Output Voltage versus Ambient Temperature

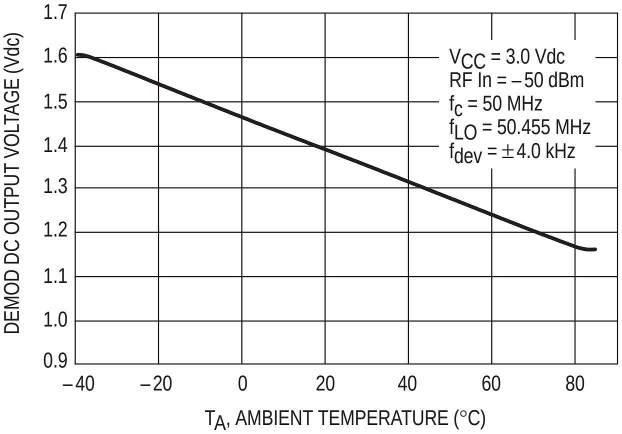


Figure 26. LO Current versus Ambient Temperature

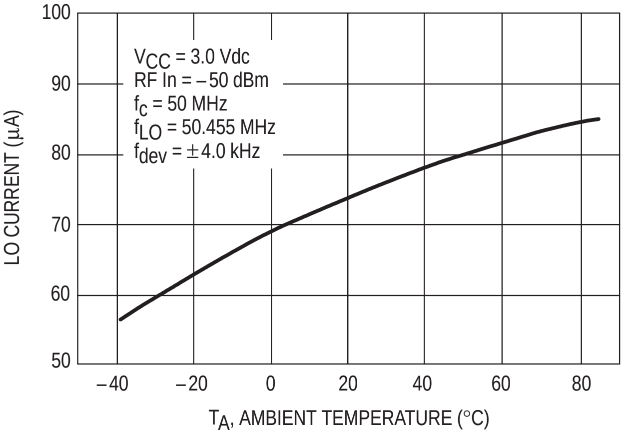


Figure 27. Component Placement View – Circuit Side

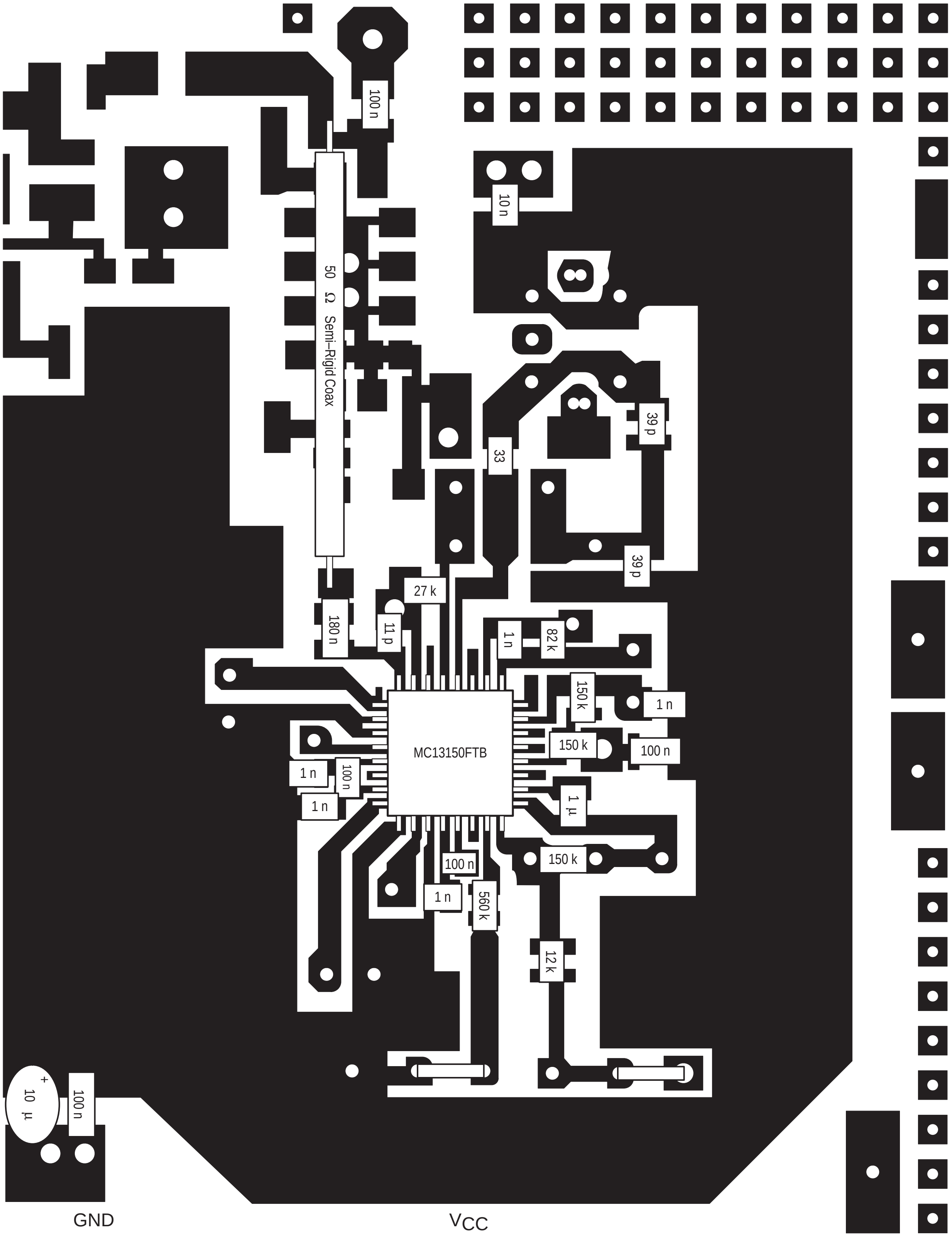


Figure 28. Component Placement View – Ground Side

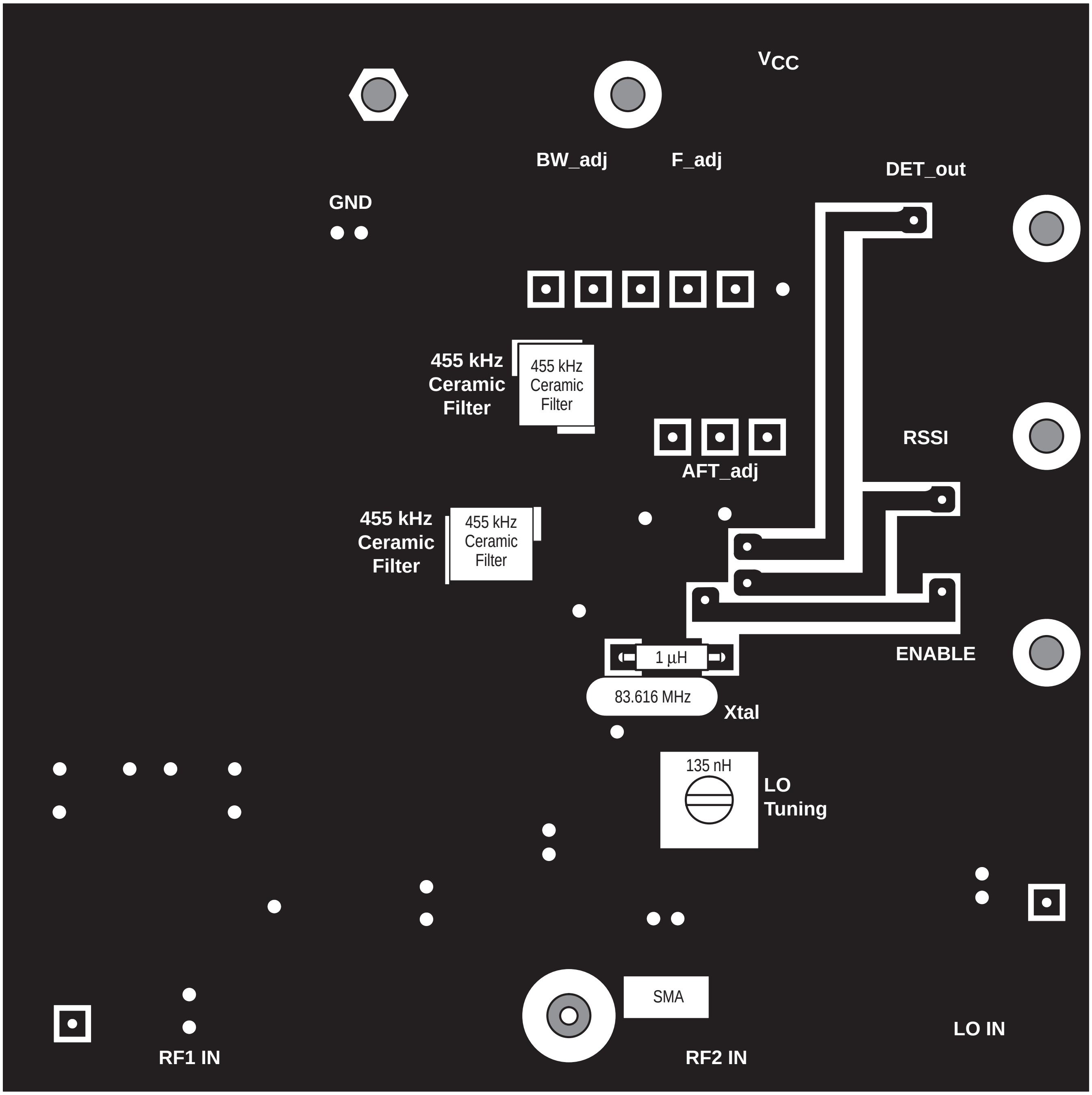


Figure 29. PCB Circuit Side View

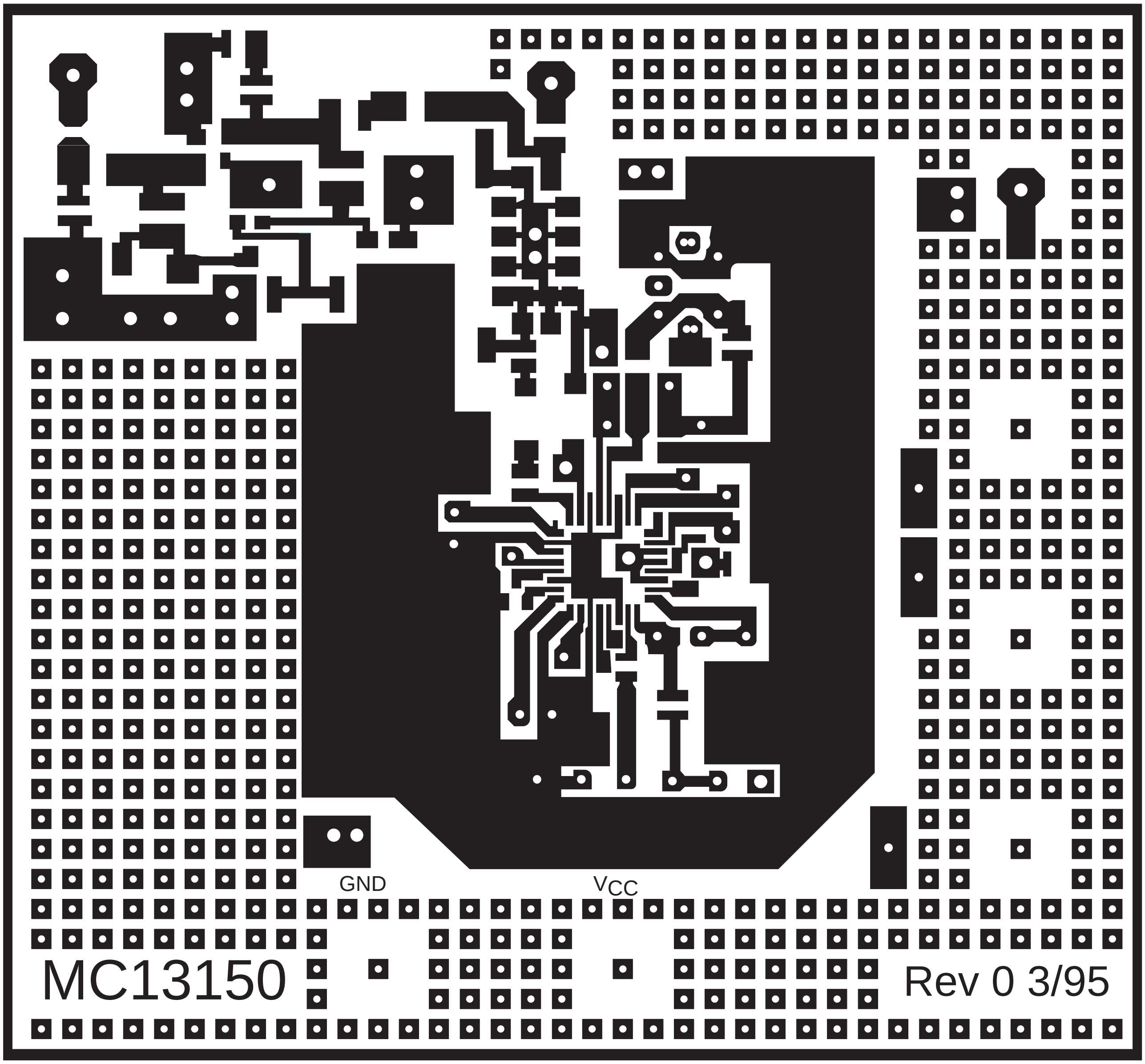
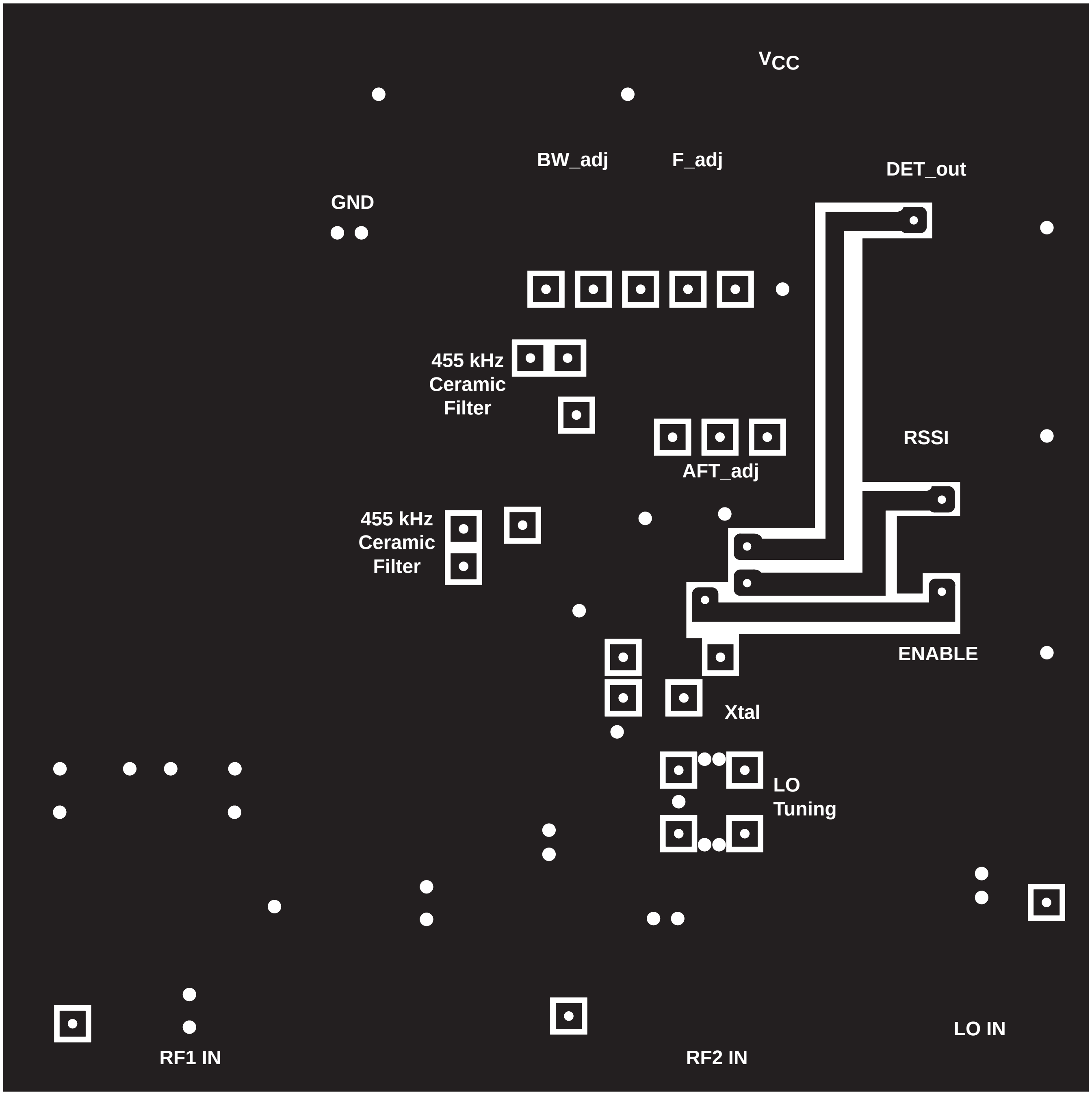


Figure 30. PCB Ground Side View



MOTOROLA

Wideband FM IF

The MC13155 is a complete wideband FM detector designed for satellite TV and other wideband data and analog FM applications. This device may be cascaded for higher IF gain and extended Receive Signal Strength Indicator (RSSI) range.

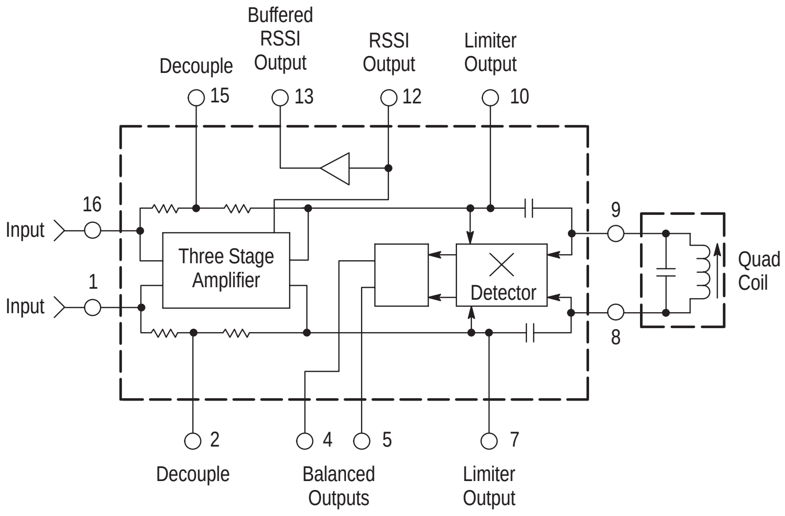
- 12 MHz Video/Baseband Demodulator
- Ideal for Wideband Data and Analog FM Systems
- Limiter Output for Cascade Operation
- Low Drain Current: 7.0 mA
- Low Supply Voltage: 3.0 to 6.0 V
- Operates to 300 MHz

MAXIMUM RATINGS

Rating	Pin	Symbol	Value	Unit
Power Supply Voltage	11, 14	V_{EE} (max)	6.5	Vdc
Input Voltage	1, 16	V_{in}	1.0	Vrms
Junction Temperature	–	T_J	+150	°C
Storage Temperature Range	–	T_{stg}	– 65 to +150	°C

NOTE: Devices should not be operated at or outside these values. The “Recommended Operating Conditions” provide for actual device operation.

Figure 1. Representative Block Diagram

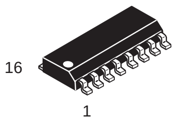


NOTE: This device requires careful layout and decoupling to ensure stable operation.

MC13155

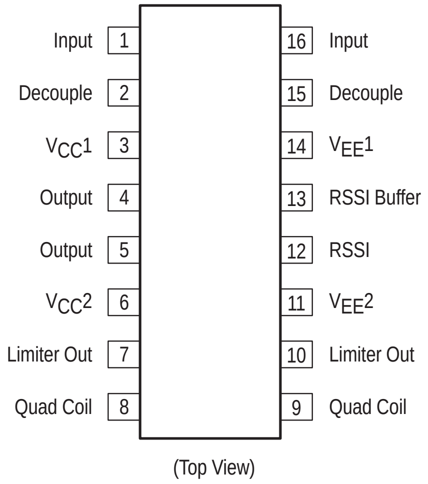
WIDEBAND FM IF

SEMICONDUCTOR TECHNICAL DATA



D SUFFIX
PLASTIC PACKAGE
CASE 751B
(SO–16)

PIN CONNECTIONS



ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC13155D	T_A = – 40 to +85°C	SO–16

RECOMMENDED OPERATING CONDITIONS

Rating	Pin	Symbol	Value	Unit
Power Supply Voltage (T_A= 25°C) – 40°C ≤ T_A ≤ 85°C	11, 14 3, 6	V_{EE} V_{CC}	– 3.0 to – 6.0 Grounded	Vdc
Maximum Input Frequency	1, 16	f_{in}	300	MHz
Ambient Temperature Range	–	T_J	– 40 to + 85	°C

DC ELECTRICAL CHARACTERISTICS (T_A = 25°C, no input signal.)

Characteristic	Pin	Symbol	Min	Typ	Max	Unit
Drain Current	11	I_{11}	2.0	2.8	4.0	mA
(V_{EE} = – 5.0 Vdc)	14	I_{14}	3.0	4.3	6.0	
(V_{EE} = – 5.0 Vdc)	14	I_{14}	3.0	4.3	6.0	
Drain Current Total (see Figure 3)	11, 14	I_{Total}	5.0	7.1	10	mA
(V_{EE} = – 5.0 Vdc)			5.0	7.5	10.5	
(V_{EE} = – 6.0 Vdc)			5.0	7.5	10.5	
(V_{EE} = – 3.0 Vdc)			4.7	6.6	9.5	

AC ELECTRICAL CHARACTERISTICS (T_A = 25°C, f_{IF} = 70 MHz, V_{EE} = – 5.0 Vdc Figure 2, unless otherwise noted.)

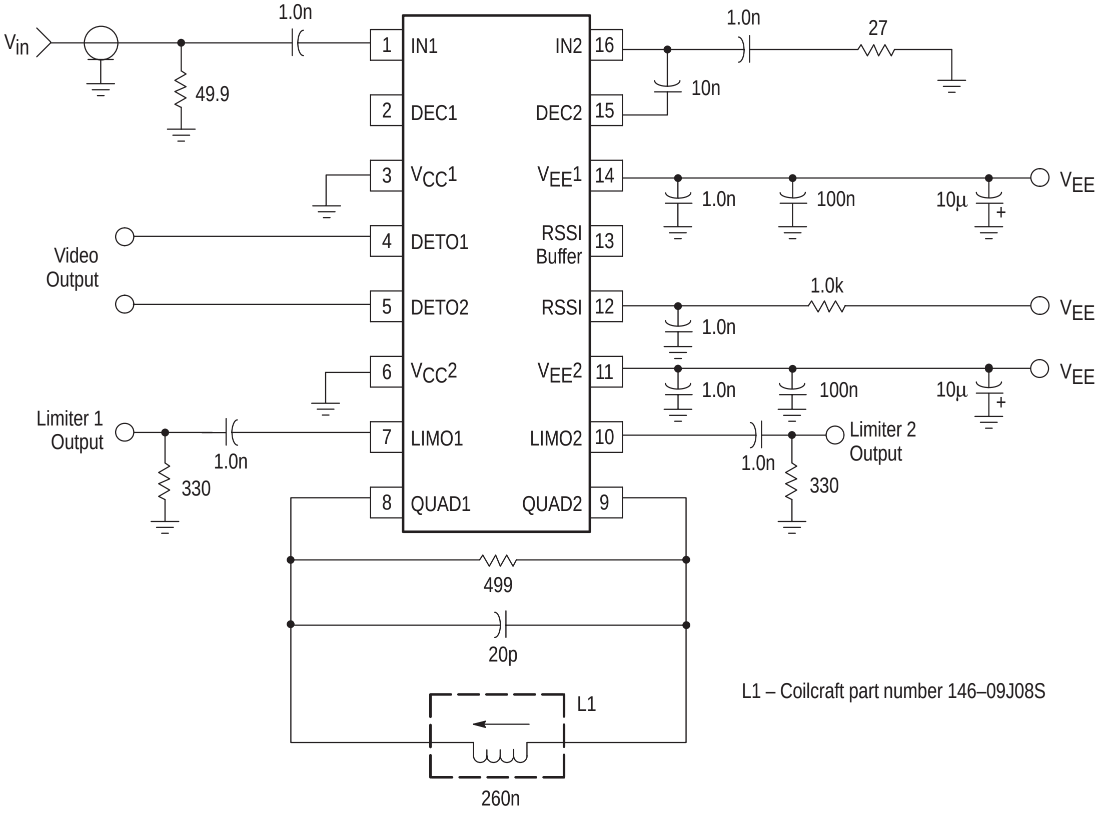
Characteristic	Pin	Min	Typ	Max	Unit
Input for – 3 dB Limiting Sensitivity	1, 16	–	1.0	2.0	mVrms
Differential Detector Output Voltage (V_{in} = 10 mVrms)	4, 5				$mV_{p–p}$
(f_{dev} = ± 3.0 MHz) (V_{EE} = – 6.0 Vdc)		470	590	700	
(V_{EE} = – 5.0 Vdc)		450	570	680	
(V_{EE} = – 3.0 Vdc)		380	500	620	
Detector DC Offset Voltage	4, 5	– 250	–	250	mVdc
RSSI Slope	13	1.4	2.1	2.8	µA/dB
RSSI Dynamic Range	13	31	35	39	dB
RSSI Output	12				µA
(V_{in} = 100 µVrms)		–	2.1	–	
(V_{in} = 1.0 mVrms)		–	2.4	–	
(V_{in} = 10 mVrms)		16	24	36	
(V_{in} = 100 mVrms)		–	65	–	
(V_{in} = 500 mVrms)		–	75	–	
RSSI Buffer Maximum Output Current (V_{in} = 10 mVrms)	13	–	2.3	–	mAdc
Differential Limiter Output					mVrms
(V_{in} = 1.0 mVrms)	7, 10	100	140	–	
(V_{in} = 10 mVrms)		–	180	–	
Demodulator Video 3.0 dB Bandwidth	4, 5	–	12	–	MHz
Input Impedance (Figure 14)	1, 16				
@ 70 MHz Rp (V_{EE} = – 5.0 Vdc)		–	450	–	Ω
Cp (C_2=C_{15} = 100 p)		–	4.8	–	pF
Differential IF Power Gain	1, 7, 10, 16	–	46	–	dB

NOTE: Positive currents are out of the pins of the device.

CIRCUIT DESCRIPTION

The MC13155 consists of a wideband three–stage limiting amplifier, a wideband quadrature detector which may be operated up to 200 MHz, and a received signal strength indicator (RSSI) circuit which provides a current output linearly proportional to the IF input signal level for approximately 35 dB range of input level.

Figure 2. Test Circuit



L1 – Coilcraft part number 146–09J08S

APPLICATIONS INFORMATION

Evaluation PC Board

The evaluation PCB shown in Figures 19 and 20 is very versatile and is designed to cascade two ICs. The center section of the board provides an area for attaching all surface mount components to the circuit side and radial leaded components to the component ground side of the PCB (see Figures 17 and 18). Additionally, the peripheral area surrounding the RF core provides pads to add supporting and interface circuitry as a particular application dictates. This evaluation board will be discussed and referenced in this section.

Limiting Amplifier

Differential input and output ports interfacing the three stage limiting amplifier provide a differential power gain of typically 46 dB and useable frequency range of 300 MHz. The IF gain flatness may be controlled by decoupling of the internal feedback network at Pins 2 and 15.

Scattering parameter (S–parameter) characterization of the IF as a two port linear amplifier is useful to implement maximum stable power gain, input matching, and stability over a desired bandpass response and to ensure stable operation outside the bandpass as well. The MC13155 is unconditionally stable over most of its useful operating frequency range; however, it can be made unconditionally stable over its entire operating range with the proper decoupling of Pins 2 and 15. Relatively small decoupling capacitors of about 100 pF have a significant effect on the wideband response and stability. This is shown in the scattering parameter tables where S–parameters are shown for various values of C2 and C15 and at V_{EE} of – 3.0 and – 5.0 Vdc.

TYPICAL PERFORMANCE AT TEMPERATURE

(See Figure 2. Test Circuit)

Figure 3. Drain Current versus Supply Voltage

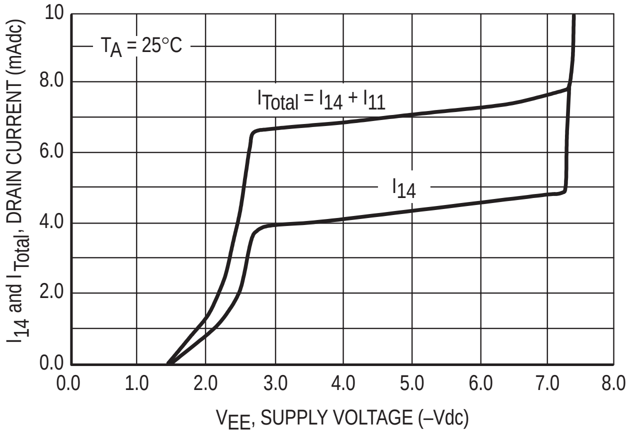


Figure 4. RSSI Output versus Frequency and Input Signal Level

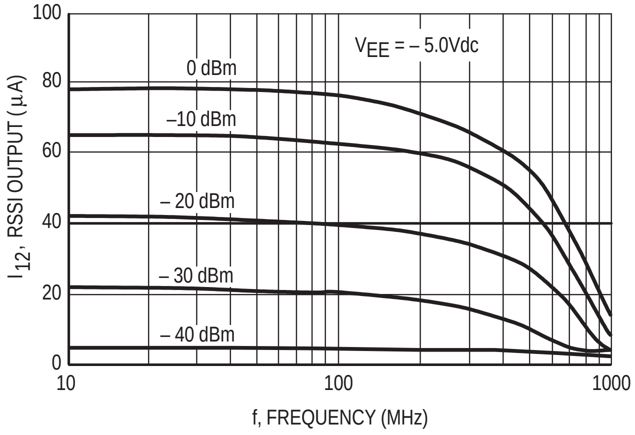


Figure 5. Total Drain Current versus Ambient Temperature and Supply Voltage

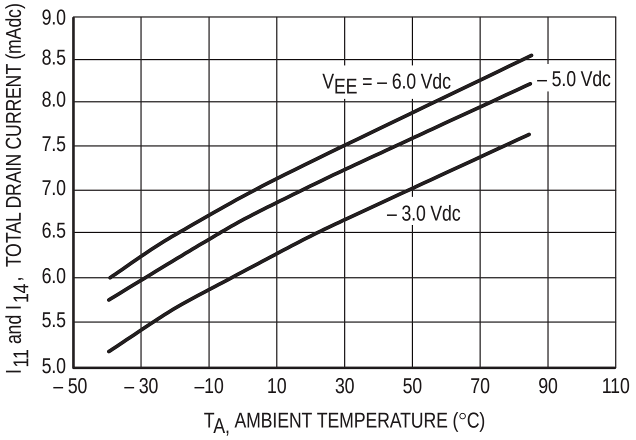


Figure 6. Detector Drain Current and Limiter Drain Current versus Ambient Temperature

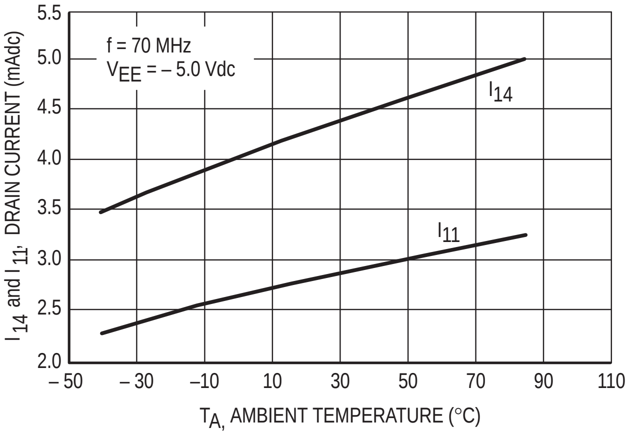


Figure 7. RSSI Output versus Ambient Temperature and Supply Voltage

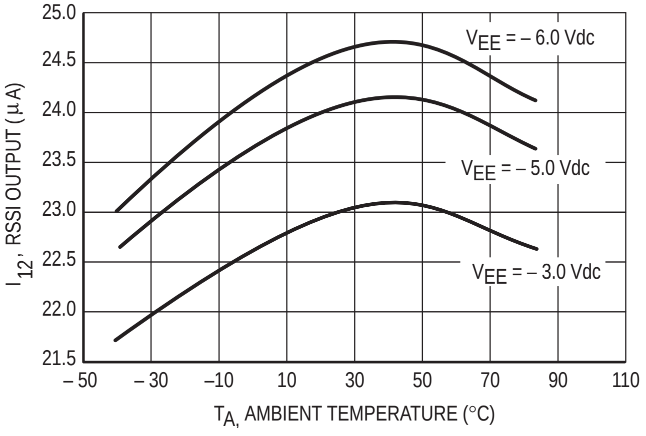


Figure 8. RSSI Output versus Input Signal Voltage (V_{in} at Temperature)

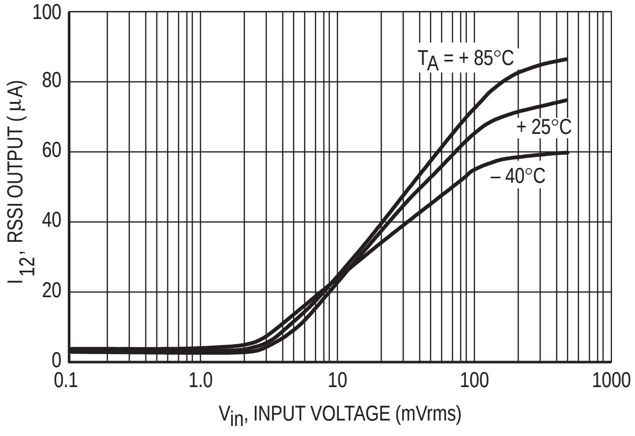


Figure 9. Differential Detector Output Voltage versus Ambient Temperature and Supply Voltage

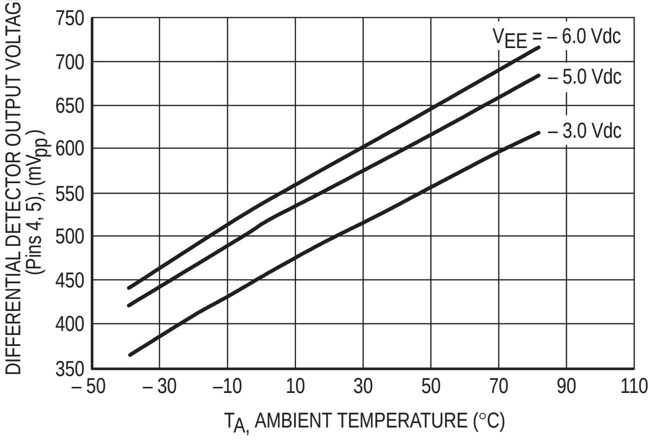


Figure 10. Differential Limiter Output Voltage versus Ambient Temperature
(V$_{in}$ = 1 and 10 mVrms)

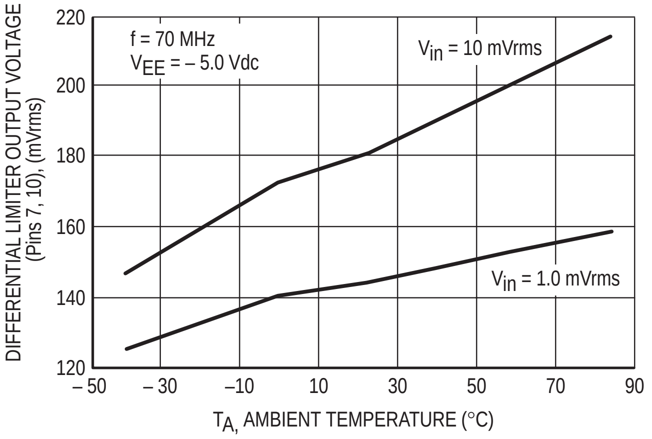


Figure 11A. Differential Detector Output Voltage versus Q of Quadrature LC Tank

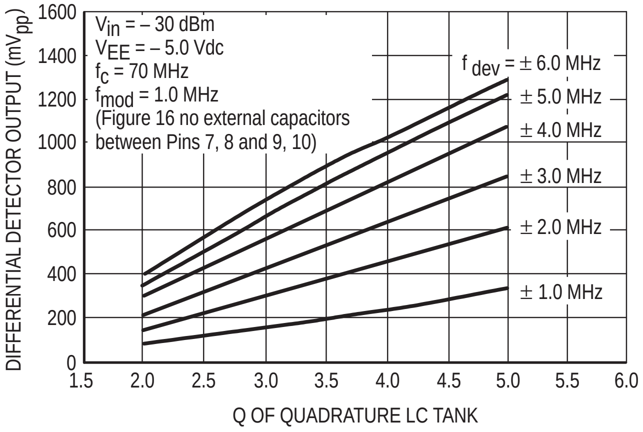


Figure 11B. Differential Detector Output Voltage versus Q of Quadrature LC Tank

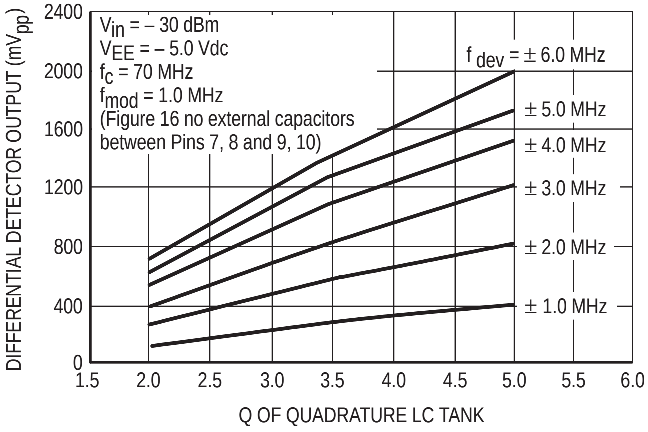


Figure 12. RSSI Output Voltage versus IF Input

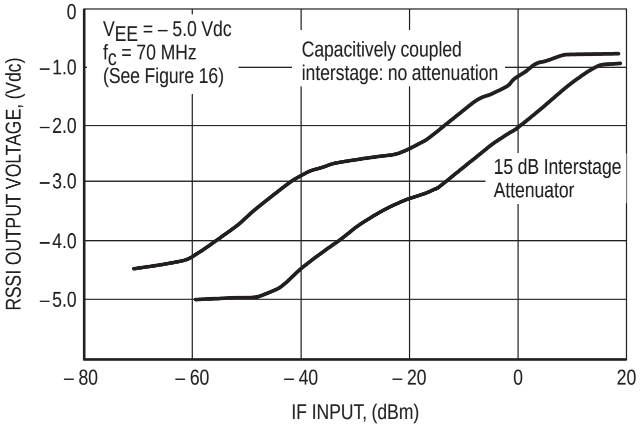
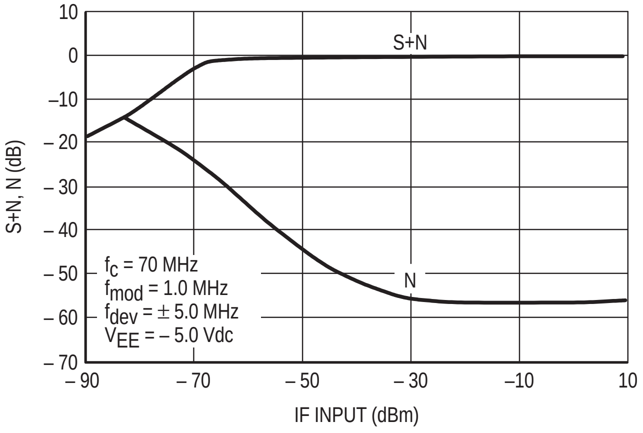


Figure 13. – S+N, N versus IF Input



In the S–parameters measurements, the IF is treated as a two–port linear class A amplifier. The IF amplifier is measured with a single–ended input and output configuration in which the Pins 16 and 7 are terminated in the series combination of a 47 Ω resistor and a 10 nF capacitor to V_{CC} ground (see Figure 14. S–Parameter Test Circuit).

The S–parameters are in polar form as the magnitude (MAG) and angle (ANG). Also listed in the tables are the calculated values for the stability factor (K) and the Maximum Available Gain (MAG). These terms are related in the following equations:

$$K = (1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2) / (2 |S_{12} S_{21}|)$$

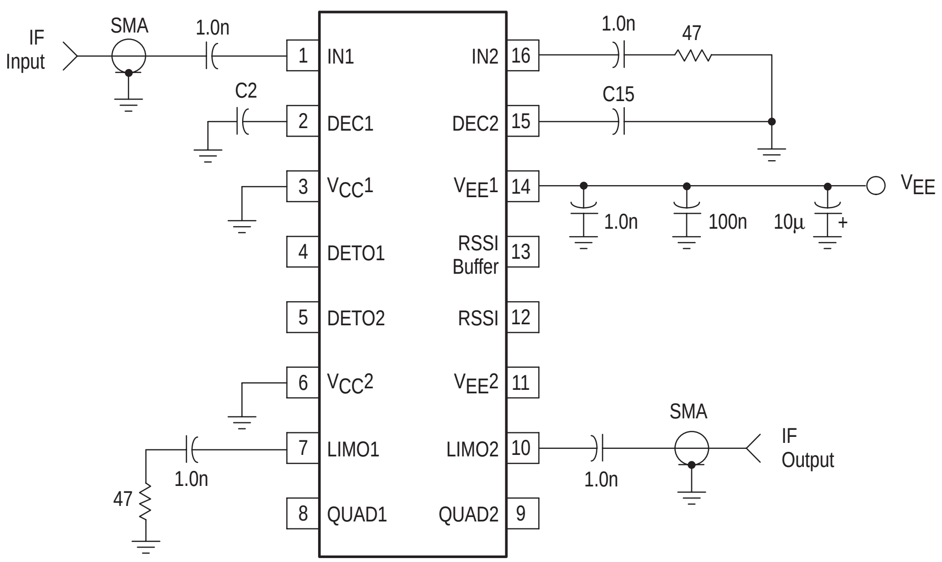
where: $|\Delta| = |S_{11} S_{22} - S_{12} S_{21}|$.

$$MAG = 10 \log |S_{21}| / |S_{12}| + 10 \log |K - (K^2 - 1)^{1/2}|$$

where: K > 1. The necessary and sufficient conditions for unconditional stability are given as K > 1:

$$B1 = 1 + |S_{11}|^2 - |S_{22}|^2 - |\Delta|^2 > 0$$

Figure 14. S–Parameter Test Circuit



S–Parameters (V_{EE} = – 5.0 Vdc, T_A = 25°C, C_2 and C_{15} = 0 pF)

Frequency	Input S11		Forward S21		Rev S12		Output S22		K	MAG
MHz	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG	MAG	dB
1.0	0.94	–13	8.2	143	0.001	7.0	0.87	– 22	2.2	32
2.0	0.78	– 23	23.5	109	0.001	– 40	0.64	– 31	4.2	33.5
5.0	0.48	1.0	39.2	51	0.001	– 97	0.34	–17	8.7	33.7
7.0	0.59	15	40.3	34	0.001	– 41	0.33	–13	10.6	34.6
10	0.75	17	40.9	19	0.001	– 82	0.41	–1.0	5.7	36.7
20	0.95	7.0	42.9	– 6.0	0.001	– 42	0.45	0	1.05	46.4
50	0.98	–10	42.2	– 48	0.001	– 9.0	0.52	– 3.0	0.29	–
70	0.95	–16	39.8	– 68	0.001	112	0.54	–16	1.05	46.4
100	0.93	– 23	44.2	– 93	0.001	80	0.53	– 22	0.76	–
150	0.91	– 34	39.5	–139	0.001	106	0.50	– 34	0.94	–
200	0.87	– 47	34.9	–179	0.002	77	0.42	– 44	0.97	–
500	0.89	–103	11.1	– 58	0.022	57	0.40	–117	0.75	–
700	0.61	–156	3.5	–164	0.03	0	0.52	179	2.6	13.7
900	0.56	162	1.2	92	0.048	– 44	0.47	112	4.7	4.5
1000	0.54	131	0.8	42	0.072	– 48	0.44	76	5.1	0.4

S–Parameters (V_{EE} = – 5.0 Vdc, T_A = 25°C, C_2 and C_{15} = 100 pF)

Frequency	Input S11		Forward S21		Rev S12		Output S22		K	MAG
MHz	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG	MAG	dB
1.0	0.98	–15	11.7	174	0.001	–14	0.84	– 27	1.2	37.4
2.0	0.50	– 2.0	39.2	85.5	0.001	–108	0.62	– 35	6.0	35.5
5.0	0.87	8.0	39.9	19	0.001	100	0.47	– 9.0	4.2	39.2
7.0	0.90	5.0	40.4	9.0	0.001	– 40	0.45	– 8.0	3.1	40.3
10	0.92	3.0	41	1.0	0.001	– 40	0.44	– 5.0	2.4	41.8
20	0.92	– 2.0	42.4	–14	0.001	– 87	0.49	– 6.0	2.4	41.9
50	0.91	– 8.0	41.2	– 45	0.001	85	0.50	– 5.0	2.3	42
70	0.91	–11	39.1	– 63	0.001	76	0.52	– 4.0	2.2	41.6
100	0.91	–15	43.4	– 84	0.001	85	0.50	–11	1.3	43.6
150	0.90	– 22	38.2	–126	0.001	96	0.43	– 22	1.4	41.8
200	0.86	– 33	35.5	–160	0.002	78	0.43	– 21	1.3	39.4
500	0.80	– 66	8.3	– 9.0	0.012	75	0.57	– 63	1.7	23.5
700	0.62	– 96	2.9	– 95	0.013	50	0.49	–111	6.3	12.5
900	0.56	–120	1.0	–171	0.020	53	0.44	–150	13.3	2.8
1000	0.54	–136	0.69	154	0.034	65	0.44	–179	12.5	– 0.8

S–Parameters (V_{EE} = – 5.0 Vdc, T_A = 25°C, C_2 and C_{15} = 680 pF)

Frequency	Input S11		Forward S21		Rev S12		Output S22		K	MAG
MHz	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG	MAG	dB
1.0	0.74	4.0	53.6	110	0.001	101	0.97	– 35	0.58	–
2.0	0.90	3.0	70.8	55	0.001	60	0.68	– 34	1.4	45.6
5.0	0.91	0	87.1	21	0.001	–121	0.33	– 60	1.1	49
7.0	0.91	0	90.3	11	0.001	–18	0.25	– 67	1.2	48.4
10	0.91	– 2.0	92.4	2.0	0.001	33	0.14	– 67	1.5	47.5
20	0.91	– 4.0	95.5	–16	0.001	63	0.12	–15	1.3	48.2
50	0.90	– 8.0	89.7	– 50	0.001	– 43	0.24	26	1.8	46.5
70	0.90	–10	82.6	–70	0.001	92	0.33	21	1.4	47.4
100	0.91	–14	77.12	–93	0.001	23	0.42	–1.0	1.05	49
150	0.94	– 20	62.0	–122	0.001	96	0.42	– 22	0.54	–
200	0.95	– 33	56.9	–148	0.003	146	0.33	– 62	0.75	–
500	0.82	– 63	12.3	–12	0.007	79	0.44	– 67	1.8	26.9
700	0.66	– 98	3.8	–107	0.014	84	0.40	–115	4.8	14.6
900	0.56	–122	1.3	177	0.028	78	0.39	–166	8.0	4.7
1000	0.54	–139	0.87	141	0.048	76	0.41	165	7.4	0.96

S–Parameters (V_{EE} = – 3.0 Vdc, T_A = 25°C, C_2 and C_{15} = 0 pF)

Frequency	Input S11		Forward S21		Rev S12		Output S22		K	MAG
MHz	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG	MAG	dB
1.0	0.89	–14	9.3	136	0.001	2.0	0.84	– 27	3.2	30.7
2.0	0.76	– 22	24.2	105	0.001	– 90	0.67	– 37	3.5	34.3
5.0	0.52	5.0	35.7	46	0.001	– 32	0.40	–13	10.6	33.3
7.0	0.59	12	38.1	34	0.001	– 41	0.40	–10	9.1	34.6
10	0.78	15	37.2	16	0.001	– 92	0.40	–1.0	5.7	36.3
20	0.95	5.0	38.2	– 9.0	0.001	47	0.51	– 4.0	0.94	–
50	0.96	–11	39.1	– 50	0.001	–103	0.48	– 6.0	1.4	43.7
70	0.93	–17	36.8	– 71	0.001	– 76	0.52	–13	2.2	41.4
100	0.91	– 25	34.7	– 99	0.001	–152	0.51	–19	3.0	39.0
150	0.86	– 37	33.8	–143	0.001	53	0.49	– 34	1.7	39.1
200	0.81	– 49	27.8	86	0.003	76	0.55	– 56	2.4	35.1
500	0.70	– 93	6.2	– 41	0.015	93	0.40	–110	2.4	19.5
700	0.62	–144	1.9	–133	0.049	56	0.40	–150	3.0	8.25
900	0.39	–176	0.72	125	0.11	–18	0.25	163	5.1	–1.9
1000	0.44	166	0.49	80	0.10	– 52	0.33	127	7.5	– 4.8

S–Parameters (V_{EE} = – 3.0 Vdc, T_A = 25°C, C_2 and C_{15} = 100 pF)

Frequency	Input S11		Forward S21		Rev S12		Output S22		K	MAG
MHz	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG	MAG	dB
1.0	0.97	–15	11.7	171	0.001	– 4.0	0.84	– 27	1.4	36.8
2.0	0.53	2.0	37.1	80	0.001	– 91	0.57	– 31	6.0	34.8
5.0	0.88	7.0	37.7	18	0.001	– 9.0	0.48	– 7.0	3.4	39.7
7.0	0.90	5.0	37.7	8.0	0.001	–11	0.49	– 7.0	2.3	41
10	0.92	2.0	38.3	1.0	0.001	– 59	0.51	– 9.0	2.0	41.8
20	0.92	– 2.0	39.6	–15	0.001	29	0.48	– 3.0	1.9	42.5
50	0.91	– 8.0	38.5	– 46	0.001	– 21	0.51	– 7.0	2.3	41.4
70	0.91	–11	36.1	– 64	0.001	49	0.50	– 8.0	2.3	40.8
100	0.91	–15	39.6	– 85	0.001	114	0.52	–13	1.7	37.8
150	0.89	– 22	34.4	–128	0.001	120	0.48	– 23	1.6	40.1
200	0.86	– 33	32	–163	0.002	86	0.40	– 26	1.7	37.8
500	0.78	– 64	7.6	–12	0.013	94	0.46	– 71	1.9	22.1
700	0.64	– 98	2.3	–102	0.027	58	0.42	–109	4.1	10.1
900	0.54	–122	0.78	179	0.040	38.6	0.35	–147	10.0	– 0.14
1000	0.53	–136	0.47	144	0.043	23	0.38	–171	15.4	– 4.52

S–Parameters (V_{EE} = – 3.0 Vdc, T_A = 25°C, C_2 and C_{15} = 680 pF)

Frequency	Input S11		Forward S21		Rev S12		Output S22		K	MAG
MHz	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG	MAG	dB
1.0	0.81	3.0	37	101	0.001	–19	0.90	– 32	1.1	43.5
2.0	0.90	2.0	47.8	52.7	0.001	– 82	0.66	– 39	0.72	–
5.0	0.91	0	58.9	20	0.001	104	0.37	– 56	2.3	44
7.0	0.90	–1	60.3	11	0.001	– 76	0.26	– 55	2.04	44
10	0.91	– 2.0	61.8	3.0	0.001	105	0.18	– 52	2.2	43.9
20	0.91	– 4.0	63.8	– 15	0.001	59	0.11	–13	2.0	44.1
50	0.90	– 8.0	60.0	– 48	0.001	96	0.22	33	2.3	43.7
70	0.90	–11	56.5	– 67	0.001	113	0.29	15	2.3	43.2
100	0.91	–14	52.7	– 91	0.001	177	0.36	5.0	2.0	43
150	0.93	– 21	44.5	–126	0.001	155	0.35	–17	1.8	42.7
200	0.90	– 43	41.2	–162	0.003	144	0.17	– 31	1.6	34.1
500	0.79	– 65	7.3	–13	0.008	80	0.44	– 75	3.0	22
700	0.65	– 97	2.3	–107	0.016	86	0.38	–124	7.1	10.2
900	0.56	–122	0.80	174	0.031	73	0.38	–174	12	0.37
1000	0.55	–139	0.52	137	0.50	71	0.41	157	11.3	– 3.4

DC Biasing Considerations

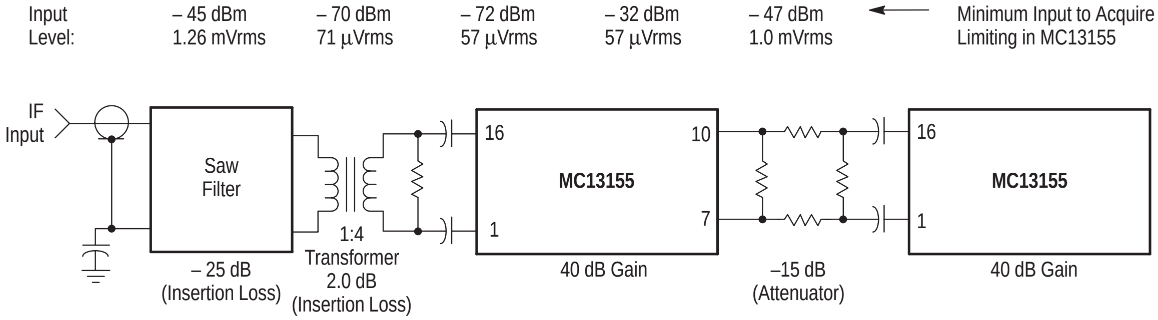
The DC biasing scheme utilizes two V_{CC} connections (Pins 3 and 6) and two V_{EE} connections (Pins 14 and 11). $V_{EE}1$ (Pin 14) is connected internally to the IF and RSSI circuits' negative supply bus while $V_{EE}2$ (Pin 11) is connected internally to the quadrature detector's negative bus. Under positive ground operation, this unique configuration offers the ability to bias the RSSI and IF separately from the quadrature detector. When two ICs are cascaded as shown in the 70 MHz application circuit and provided by the PCB (see Figures 17 and 18), the first MC13155 is used without biasing its quadrature detector, thereby saving approximately 3.0 mA. A total current of 7.0 mA is used to fully bias each IC, thus the total current in the application circuit is approximately 11 mA. Both V_{CC} pins are biased by the same supply. $V_{CC}1$ (Pin 3) is connected internally to the positive bus of the first half of the IF limiting amplifier, while $V_{CC}2$ is internally connected to the positive bus of the RSSI, the quadrature detector circuit, and the second half of the IF limiting amplifier (see Figure 15). This distribution of the V_{CC} enhances the stability of the IC.

RSSI Circuitry

The RSSI circuitry provides typically 35 dB of linear dynamic range and its output voltage swing is adjusted by selection of the resistor from Pin 12 to V_{EE}. The RSSI slope is typically 2.1 µA/dB ; thus, for a dynamic range of 35 dB, the current output is approximately 74 µA. A 47 k resistor will yield an RSSI output voltage swing of 3.5 Vdc. The RSSI buffer output at Pin 13 is an emitter–follower and needs an external emitter resistor of 10 k to V_{EE}.

In a cascaded configuration (see circuit application in Figure 16), only one of the RSSI Buffer outputs (Pin 13) is used; the RSSI outputs (Pin 12 of each IC) are tied together and the one closest to the V_{EE} supply trace is decoupled to V_{CC} ground. The two pins are connected to V_{EE} through a 47 k resistor. This resistor sources a RSSI current which is proportional to the signal level at the IF input; typically, 1.0 mVrms (– 47 dBm) is required to place the MC13155 into limiting. The measured RSSI output voltage response of the application circuit is shown in Figure 12. Since the RSSI current output is dependent upon the input signal level at the IF input, a careful accounting of filter losses, matching and other losses and gains must be made in the entire receiver system. In the block diagram of the application circuit shown below, an accounting of the signal levels at points throughout the system shows how the RSSI response in Figure 12 is justified.

Block Diagram of 70 MHz Video Receiver Application Circuit

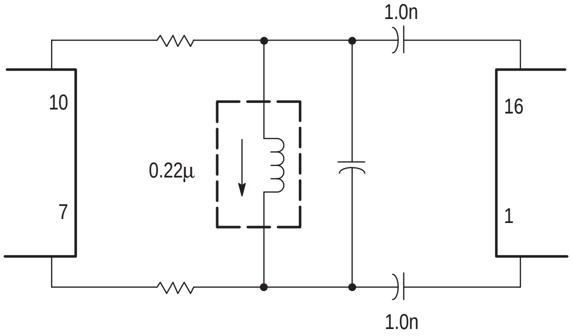


Cascading Stages

The limiting IF output is pinned–out differentially, cascading is easily achieved by AC coupling stage to stage. In the evaluation PCB, AC coupling is shown, however, interstage filtering may be desirable in some applications. In which case, the S–parameters provide a means to implement a low loss interstage match and better receiver sensitivity.

Where a linear response of the RSSI output is desired when cascading the ICs, it is necessary to provide at least 10 dB of interstage loss. Figure 12 shows the RSSI response with and without interstage loss. A 15 dB resistive attenuator is an inexpensive way to linearize the RSSI response. This has its drawbacks since it is a wideband noise source that is dependent upon the source and load impedance and the amount of attenuation that it provides. A better, although more costly, solution would be a bandpass filter designed to the desired center frequency and bandpass response while carefully selecting the insertion loss. A network topology shown below may be used to provide a bandpass response with the desired insertion loss.

Network Topology



Quadrature Detector

The quadrature detector is coupled to the IF with internal 2.0 pF capacitors between Pins 7 and 8 and Pins 9 and 10. For wideband data applications, such as FM video and satellite receivers, the drive to the detector can be increased with additional external capacitors between these pins, thus, the recovered video signal level output is increased for a given bandwidth (see Figure 11A and Figure 11B).

The wideband performance of the detector is controlled by the loaded Q of the LC tank circuit. The following equation defines the components which set the detector circuit's bandwidth:

$$Q = R_T/X_L \qquad (1)$$

where: R_T is the equivalent shunt resistance across the LC Tank and X_L is the reactance of the quadrature inductor at the IF frequency ($X_L = 2\pi fL$).

The inductor and capacitor are chosen to form a resonant LC Tank with the PCB and parasitic device capacitance at the desired IF center frequency as predicted by:

$$fc = (2\pi \sqrt{(LC_p)})^{-1} \qquad (2)$$

where: L is the parallel tank inductor and C_p is the equivalent parallel capacitance of the parallel resonant tank circuit.

The following is a design example for a wideband detector at 70 MHz and a loaded Q of 5. The loaded Q of the quadrature detector is chosen somewhat less than the Q of the IF bandpass. For an IF frequency of 70 MHz and an IF bandpass of 10.9 MHz, the IF bandpass Q is approximately 6.4.

Example:

Let the external Cext = 20 pF. (The minimum value here should be greater than 15 pF making it greater than the internal device and PCB parasitic capacitance, Cint ≈ 3.0 pF).

$$C_p = Cint + Cext = 23 \text{ pF}$$

Rewrite Equation 2 and solve for L:

$L = (0.159)^2 / (C_p\, fc^2)$

L = 198 nH, thus, a standard value is chosen.

L = 0.22 µH (tunable shielded inductor).

The value of the total damping resistor to obtain the required loaded Q of 5 can be calculated by rearranging Equation 1:

$$R_T = Q(2\pi fL)$$

$$R_T = 5\,(2\pi)(70)(0.22) = 483.8\ \Omega.$$

The internal resistance, Rint between the quadrature tank Pins 8 and 9 is approximately 3200 Ω and is considered in determining the external resistance, Rext which is calculated from:

Rext = $((R_T)(Rint))/ (Rint – R_T)$

Rext = 570, thus, choose the standard value.

Rext = 560 Ω.

SAW Filter

In wideband video data applications, the IF occupied bandwidth may be several MHz wide. A good rule of thumb is to choose the IF frequency about 10 or more times greater than the IF occupied bandwidth. The IF bandpass filter is a SAW filter in video data applications where a very selective response is needed (i.e., very sharp bandpass response). The evaluation PCB is laid out to accommodate two SAW filter package types: 1) A five–leaded plastic SIP package. Recommended part numbers are Siemens X6950M which operates at 70 MHz; 10.4 MHz 3 dB passband, X6951M (X252.8) which operates at 70 MHz; 9.2 MHz 3 dB passband; and X6958M which operates at 70 MHz, 6.3 MHz 3 dB passband, and 2) A four–leaded TO–39 metal can package. Typical insertion loss in a wide bandpass SAW filter is 25 dB.

The above SAW filters require source and load impedances of 50 Ω to assure stable operation. On the PC board layout, space is provided to add a matching network, such as a 1:4 surface mount transformer between the SAW filter output and the input to the MC13155. A 1:4 transformer, made by Coilcraft and Mini Circuits, provides a suitable interface (see Figures 16, 17 and 18). In the circuit and layout, the SAW filter and the MC13155 are differentially configured with interconnect traces which are equal in length and symmetrical. This balanced feed enhances RF stability, phase linearity, and noise performance.

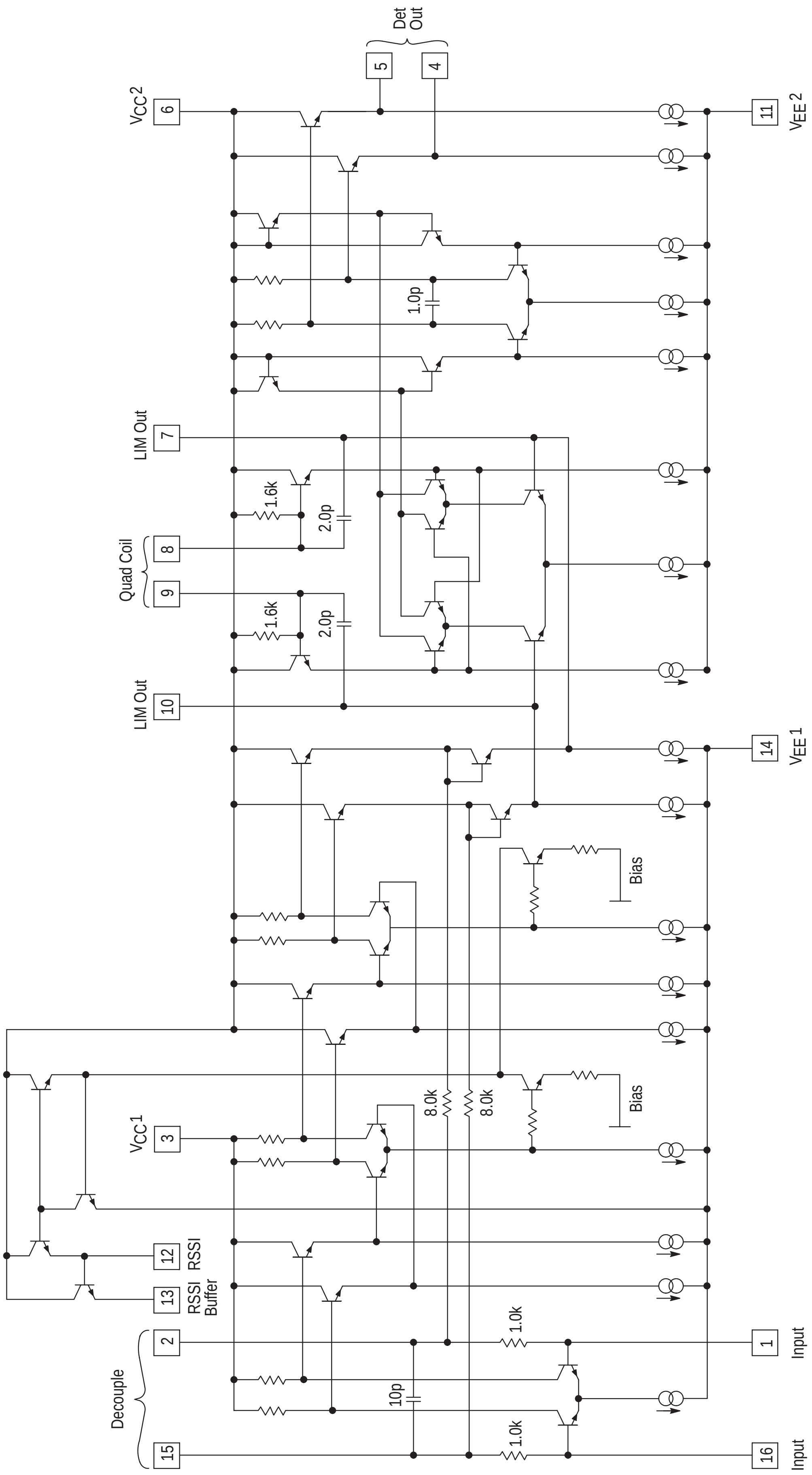


Figure 15. Simplified Internal Circuit Schematic

Figure 16. 70 MHz Video Receiver Application Circuit

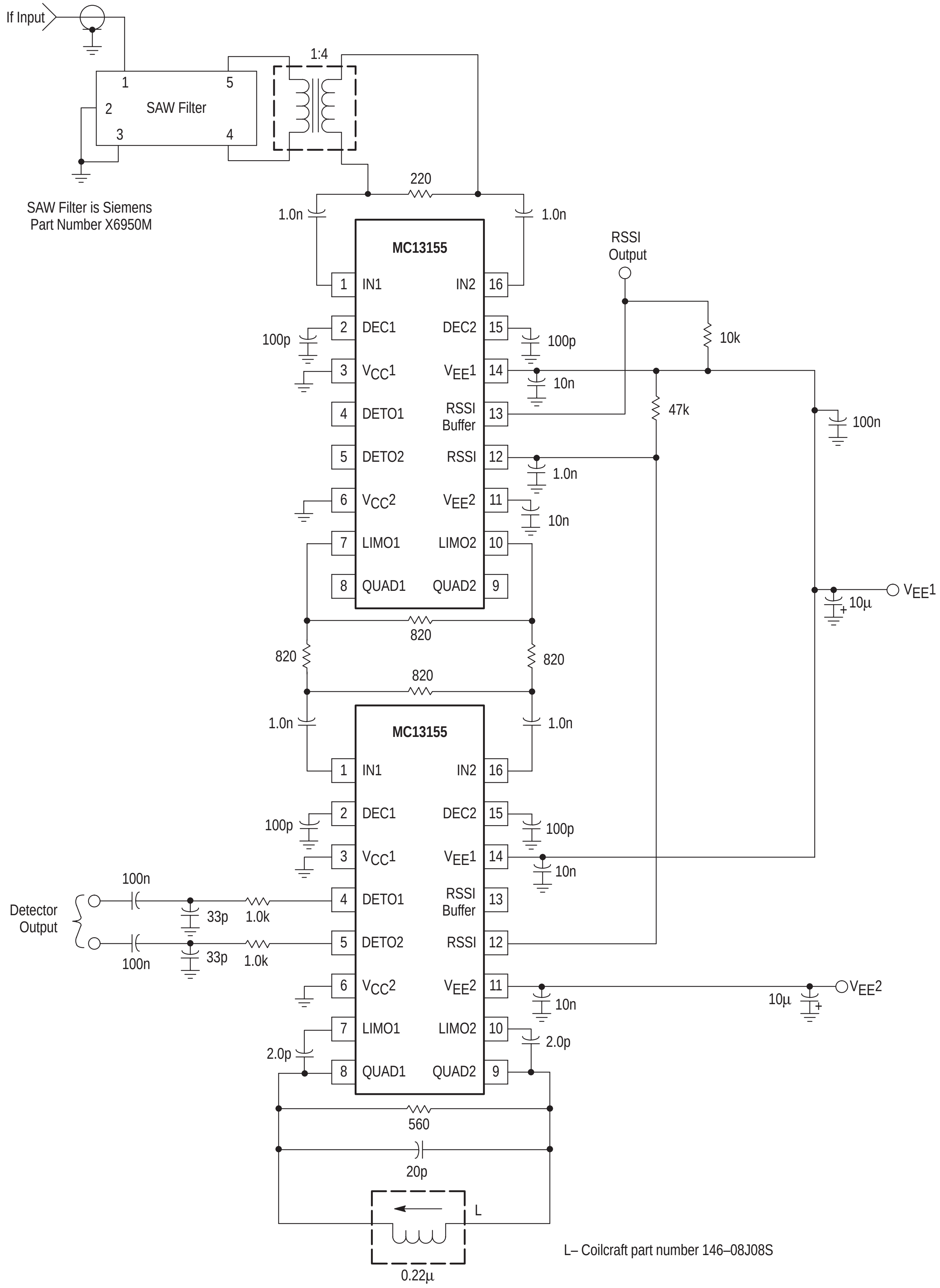


Figure 17. Component Placement (Circuit Side)

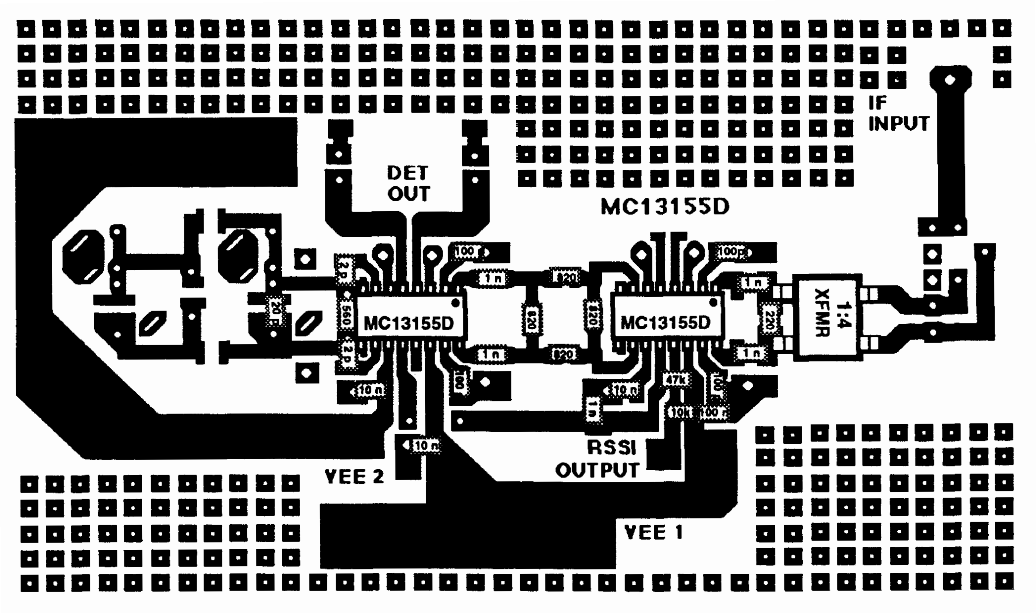


Figure 18. Component Placement (Ground Side)

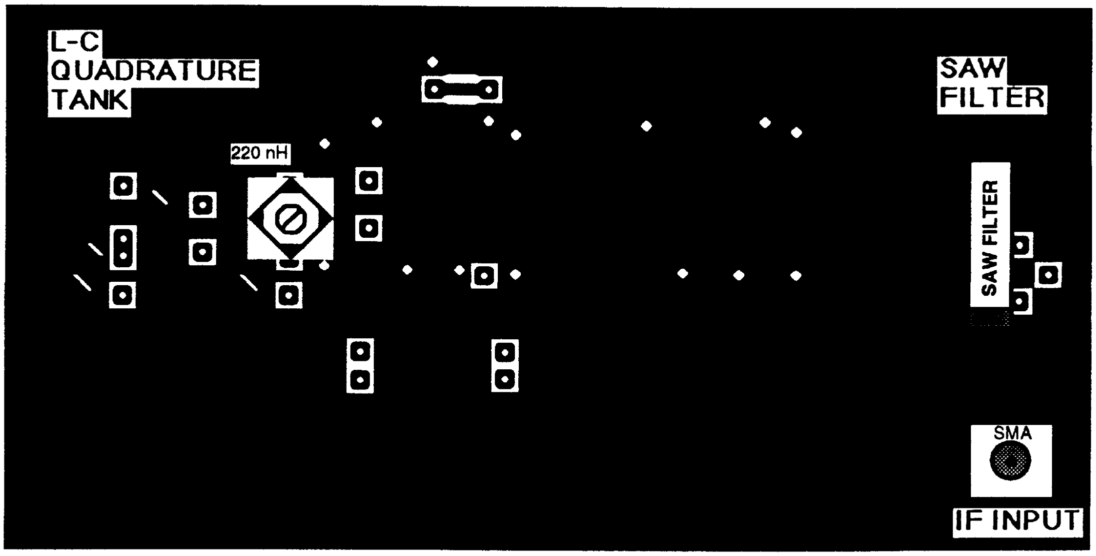


Figure 19. Circuit Side View

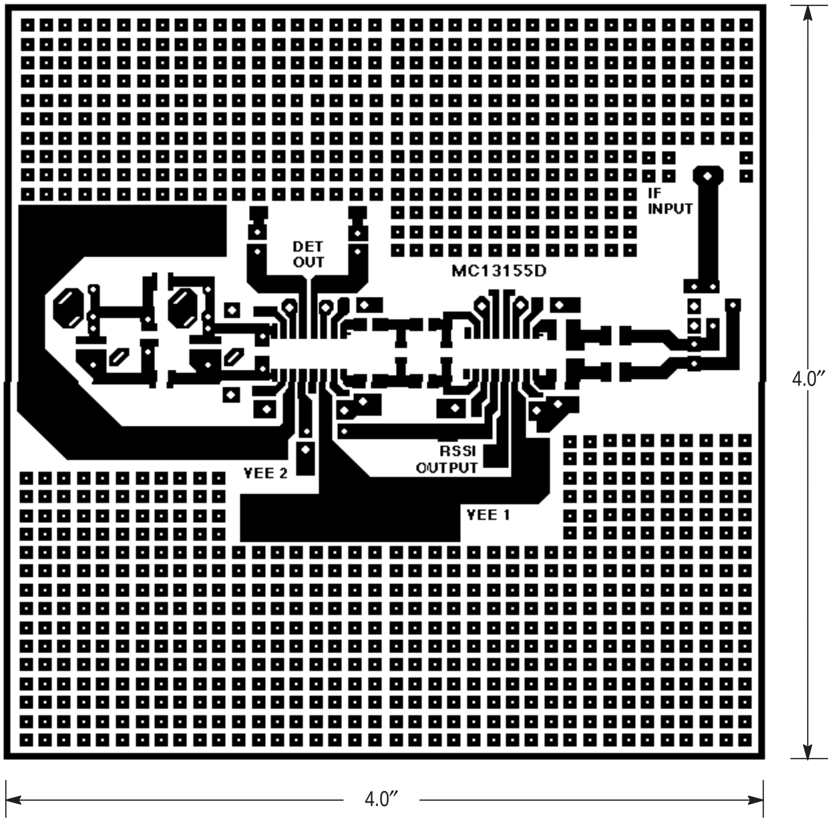
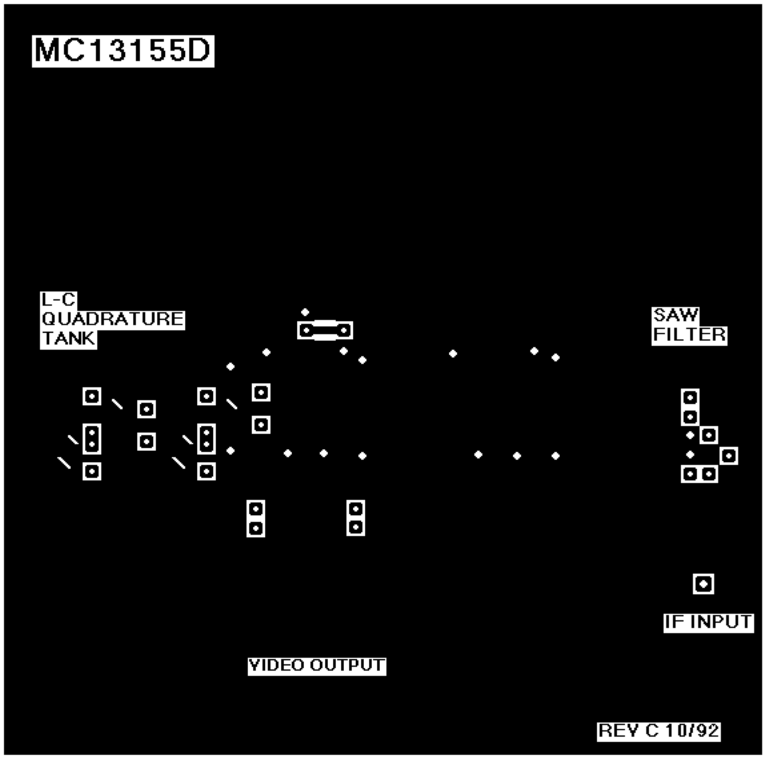


Figure 20. Ground Side View



MC13156

Wideband FM IF System

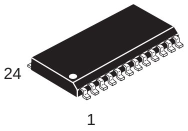
The MC13156 is a wideband FM IF subsystem targeted at high performance data and analog applications. Excellent high frequency performance is achieved at low cost using Motorola's MOSAIC 1.5™ bipolar process. The MC13156 has an onboard grounded collector VCO transistor that may be used with a fundamental or overtone crystal in single channel operation or with a PLL in multichannel operation. The mixer is useful to 500 MHz and may be used in a balanced–differential, or single–ended configuration. The IF amplifier is split to accommodate two low cost cascaded filters. RSSI output is derived by summing the output of both IF sections. A precision data shaper has a hold function to preset the shaper for fast recovery of new data.

Applications for the MC13156 include CT–2, wideband data links and other radio systems utilizing GMSK, FSK or FM modulation.

- 2.0 to 6.0 Vdc Operation
- Typical Sensitivity at 200 MHz of 2.0 μV for 12 dB SINAD
- RSSI Dynamic Range Typically 80 dB
- High Performance Data Shaper for Enhanced CT–2 Operation
- Internal 330 Ω and 1.4 kΩ Terminations for 10.7 MHz and 455 kHz Filters
- Split IF for Improved Filtering and Extended RSSI Range
- 3rd Order Intercept (Input) of –25 dBm (Input Matched)

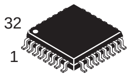
WIDEBAND FM IF SYSTEM FOR DIGITAL AND ANALOG APPLICATIONS

SEMICONDUCTOR TECHNICAL DATA

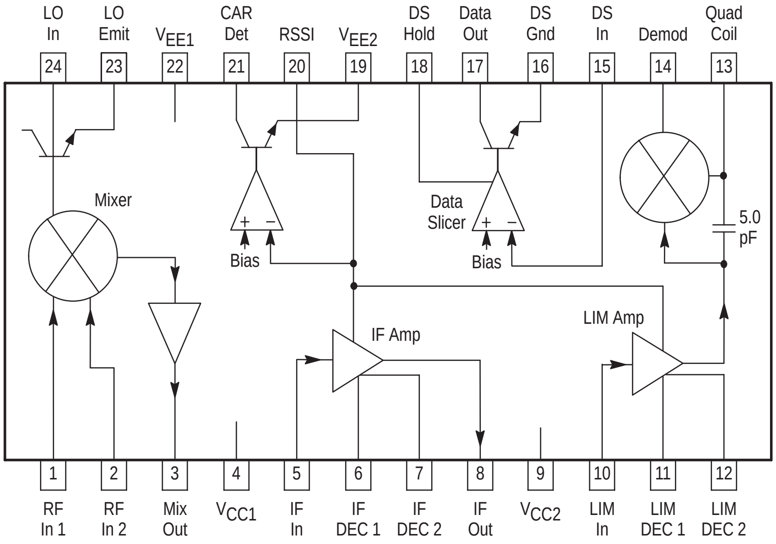


DW SUFFIX
PLASTIC PACKAGE
CASE 751E
(SO–24L)

FB SUFFIX
PLASTIC QFP PACKAGE
CASE 873



Simplified Block Diagram



NOTE: Pin Numbers shown for SOIC package only. Refer to Pin Assignments Table.

This device contains 197 active transistors.

PIN CONNECTIONS

Function	SO–24L	QFP
RF Input 1	1	31
RF Input 2	2	32
Mixer Output	3	1
V_{CC1}	4	2
IF Amp Input	5	3
IF Amp Decoupling 1	6	4
IF Amp Decoupling 2	7	5
V_{CC} Connect (N/C Internal)	–	6
IF Amp Output	8	7
V_{CC2}	9	8
Limiter IF Input	10	9
Limiter Decoupling 1	11	10
Limiter Decoupling 2	12	11
V_{CC} Connect (N/C Internal)	–	12, 13, 14
Quad Coil	13	15
Demodulator Output	14	16
Data Slicer Input	15	17
V_{CC} Connect (N/C Internal)	–	18
Data Slicer Ground	16	19
Data Slicer Output	17	20
Data Slicer Hold	18	21
V_{EE2}	19	22
RSSI Output/Carrier Detect In	20	23
Carrier Detect Output	21	24
V_{EE1} and Substrate	22	25
LO Emitter	23	26
LO Base	24	27
V_{CC} Connect (N/C Internal)	–	28, 29, 30

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC13156DW	T_A = –40 to +85°C	SO–24L
MC13156FB		QFP

MAXIMUM RATINGS

Rating	Pin	Symbol	Value	Unit
Power Supply Voltage	16, 19, 22	$V_{EE(max)}$	–6.5	Vdc
Junction Temperature	–	$T_{J(max)}$	150	°C
Storage Temperature Range	–	T_{stg}	–65 to +150	°C

NOTES: 1. Devices should not be operated at or outside these values. The “Recommended Operating Conditions” table provides for actual device operation.
2. ESD data available upon request.

RECOMMENDED OPERATING CONDITIONS

Rating	Pin	Symbol	Value	Unit
Power Supply Voltage @ T_A = 25°C	4, 9	V_{CC}	0 (Ground)	Vdc
–40°C ≤ T_A ≤ +85°C	16, 19, 22	V_{EE}	–2.0 to –6.0	
Input Frequency	1, 2	f_{in}	500	MHz
Ambient Temperature Range	–	T_A	–40 to +85	°C
Input Signal Level	1, 2	V_{in}	200	mVrms

DC ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC1} = V_{CC2} = 0, no input signal.)

Characteristic	Pin	Symbol	Min	Typ	Max	Unit
Total Drain Current (See Figure 2)	19, 22	I_{Total}				mA
V_{EE} = –2.0 Vdc			–	4.8	–	
V_{EE} = –3.0 Vdc			3.0	5.0	8.0	
V_{EE} = –5.0 Vdc			–	5.2	–	
V_{EE} = –6.0 Vdc			–	5.4	–	
Drain Current, I_{22} (See Figure 3)	22	I_{22}				mA
V_{EE} = –2.0 Vdc			–	3.0	–	
V_{EE} = –3.0 Vdc			–	3.1	–	
V_{EE} = –5.0 Vdc			–	3.3	–	
V_{EE} = –6.0 Vdc			–	3.4	–	
Drain Current, I_{19} (See Figure 3)	19	I_{19}				mA
V_{EE} = –2.0 Vdc			–	1.8	–	
V_{EE} = –3.0 Vdc			–	1.9	–	
V_{EE} = –5.0 Vdc			–	1.9	–	
V_{EE} = –6.0 Vdc			–	2.0	–	

DATA SLICER (Input Voltage Referenced to V_{EE} = –3.0 Vdc, no input signal; See Figure 15.)

Input Threshold Voltage (High V_{in})	15	V_{15}	1.0	1.1	1.2	Vdc
Output Current (Low V_{in}) Data Slicer Enabled (No Hold) V_{15} > 1.1 Vdc V_{18} = 0 Vdc	17	I_{17}	–	1.7	–	mA

AC ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{EE} = –3.0 Vdc, f_{RF} = 130 MHz, f_{LO} = 140.7 MHz, Figure 1 test circuit, unless otherwise specified.)

Characteristic	Pin	Symbol	Min	Typ	Max	Unit
12 dB SINAD Sensitivity (See Figures 17, 25) f_{in} = 144.45 MHz; f_{mod} = 1.0 kHz; f_{dev} = ±75 kHz	1, 14	–	–	–100	–	dBm

MIXER

Conversion Gain P_{in} = –37 dBm (Figure 4)	1, 3	–	–	22	–	dB
Mixer Input Impedance	1, 2	R_p	–	1.0	–	kΩ
Single–Ended (Table 1)		C_p	–	4.0	–	pF
Mixer Output Impedance	3	–	–	330	–	Ω

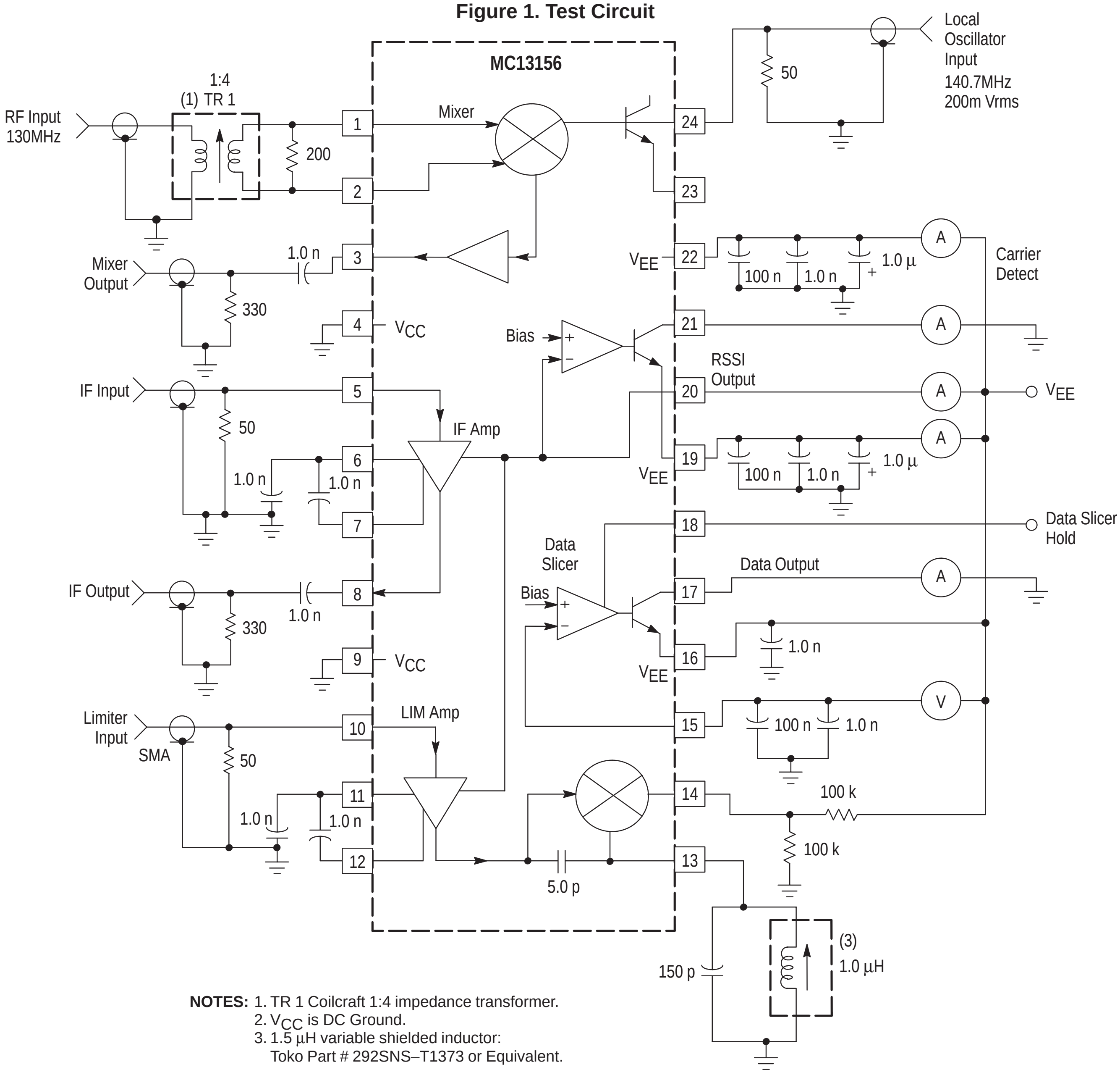
IF AMPLIFIER SECTION

IF RSSI Slope (Figure 6)	20	–	0.2	0.4	0.6	µA/dB
IF Gain (Figure 5)	5, 8	–	–	39	–	dB
Input Impedance	5	–	–	1.4	–	kΩ
Output Impedance	8	–	–	290	–	Ω

AC ELECTRICAL CHARACTERISTICS (continued) (T_A = 25°C, V_{EE} = –3.0 Vdc, f_{RF} = 130 MHz, f_{LO} = 140.7 MHz, Figure 1 test circuit, unless otherwise specified.)

Characteristic	Pin	Symbol	Min	Typ	Max	Unit
LIMITING AMPLIFIER SECTION						
Limiter RSSI Slope (Figure 7)	20	–	0.2	0.4	0.6	µA/dB
Limiter Gain	–	–	–	55	–	dB
Input Impedance	10	–	–	1.4	–	kΩ
CARRIER DETECT						
Output Current – Carrier Detect (High V_{in})	21	–	–	0	–	µA
Output Current – Carrier Detect (Low V_{in})	21	–	–	3.0	–	mA
Input Threshold Voltage – Carrier Detect Input Voltage Referenced to V_{EE} = –3.0 Vdc	20	–	0.9	1.2	1.4	Vdc

Figure 1. Test Circuit



NOTES:
1. TR 1 Coilcraft 1:4 impedance transformer.
2. V_{CC} is DC Ground.
3. 1.5 µH variable shielded inductor:
   Toko Part # 292SNS–T1373 or Equivalent.

Figure 2. Total Drain Current versus Supply Voltage and Temperature

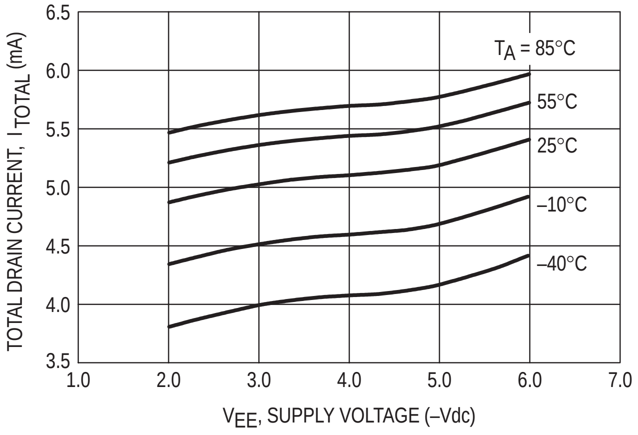


Figure 3. Drain Currents versus Supply Voltage

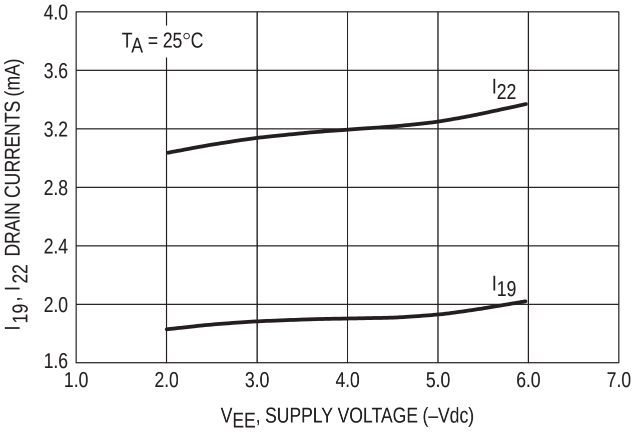


Figure 4. Mixer Gain versus Input Signal Level

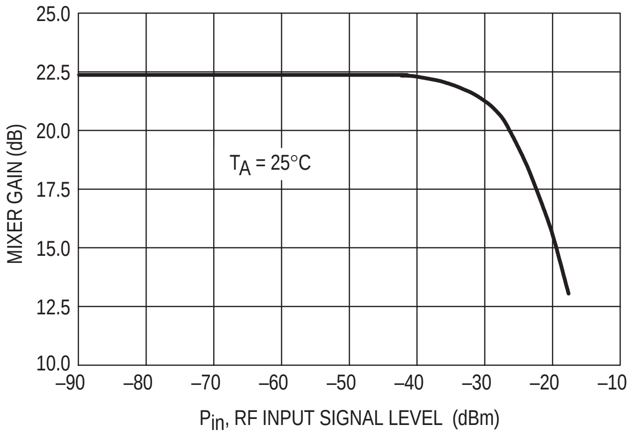


Figure 5. IF Amplifier Gain versus Input Signal Level and Ambient Temperature

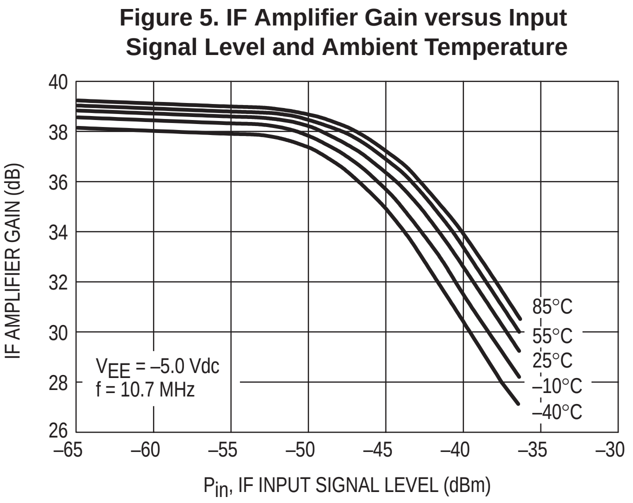


Figure 6. IF Amplifier RSSI Output Current versus Input Signal Level and Ambient Temperature

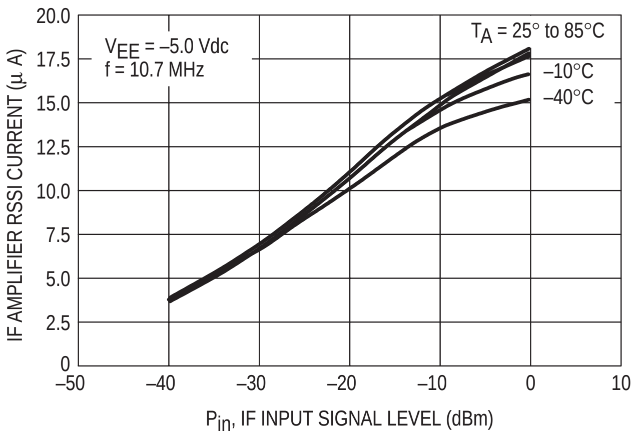


Figure 7. Limiter Amplifier RSSI Output Current versus Input Signal Level and Temperature

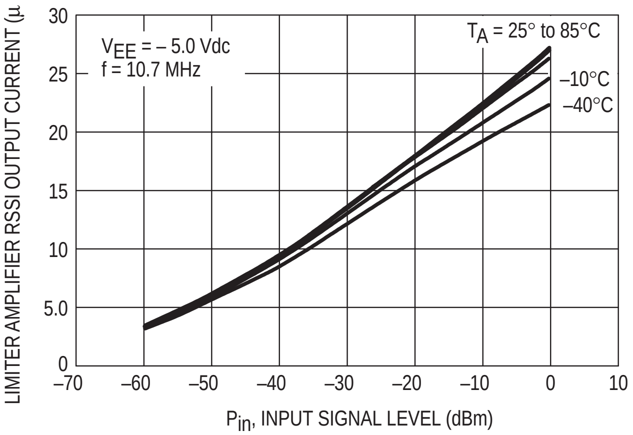
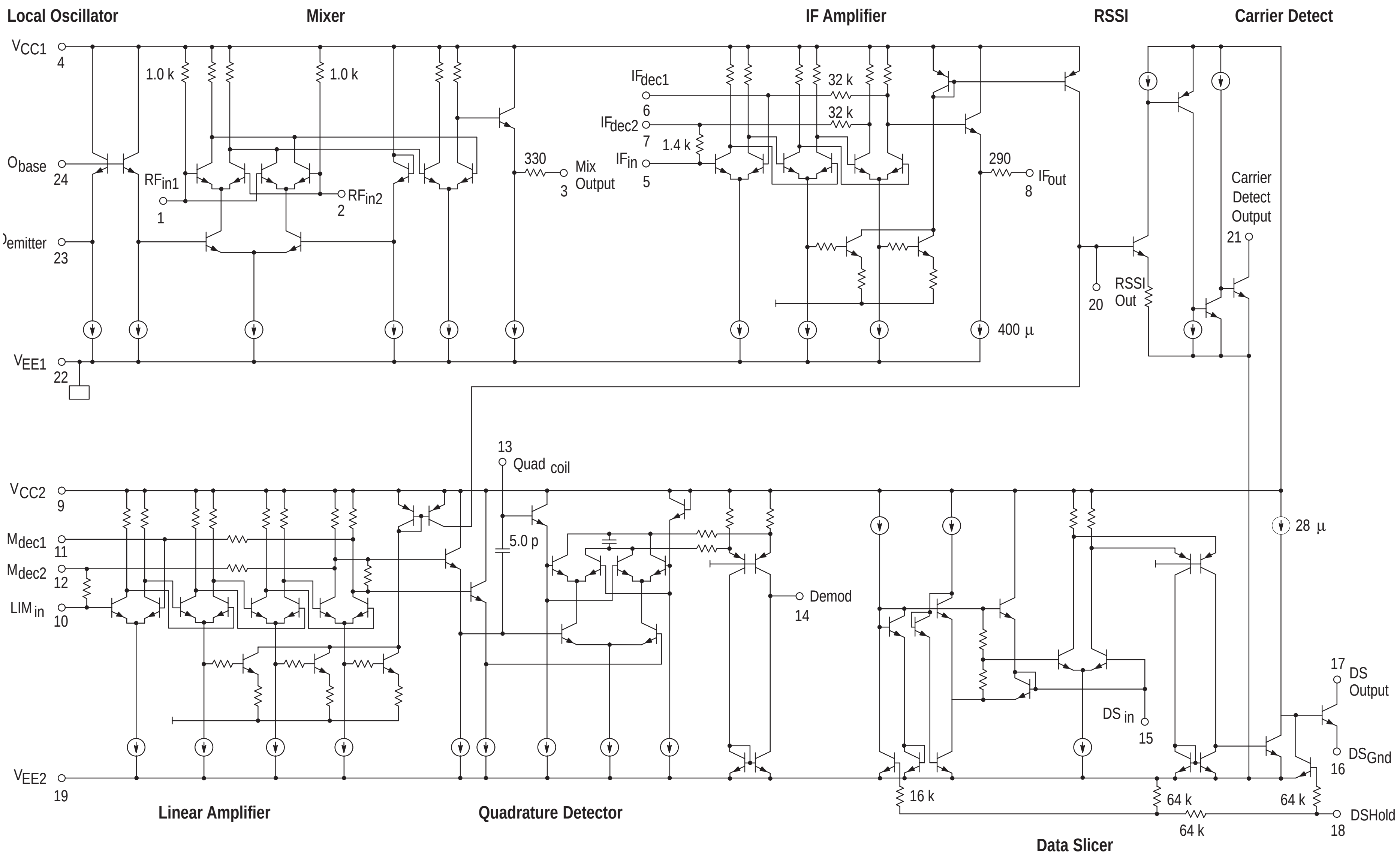


Figure 8. MC13156DW Internal Circuit Schematic



CIRCUIT DESCRIPTION

General

The MC13156 is a low power single conversion wideband FM receiver incorporating a split IF. This device is designated for use as the backend in digital FM systems such as CT–2 and wideband data links with data rates up to 500 kbaud. It contains a mixer, oscillator, signal strength meter drive, IF amplifier, limiting IF, quadrature detector and a data slicer with a hold function (refer to Figure 8, Simplified Internal Circuit Schematic).

Current Regulation

Temperature compensating voltage independent current regulators are used throughout.

Mixer

The mixer is a double–balanced four quadrant multiplier and is designed to work up to 500 MHz. It can be used in differential or in single–ended mode by connecting the other input to the positive supply rail.

Figure 4 shows the mixer gain and saturated output response as a function of input signal drive. The circuit used to measure this is shown in Figure 1. The linear gain of the mixer is approximately 22 dB. Figure 9 shows the mixer gain versus the IF output frequency with the local oscillator of 150 MHz at 100 mVrms LO drive level. The RF frequency is swept. The sensitivity of the IF output of the mixer is shown in Figure 10 for an RF input drive of 10 mVrms at 140 MHz and IF at 10 MHz.

The single–ended parallel equivalent input impedance of the mixer is Rp ~ 1.0 kΩ and Cp ~ 4.0 pF (see Table 1 for details). The buffered output of the mixer is internally loaded resulting in an output impedance of 330 Ω.

Local Oscillator

The on–chip transistor operates with crystal and LC resonant elements up to 220 MHz. Series resonant, overtone crystals are used to achieve excellent local oscillator stability. 3rd overtone crystals are used through about 65 to 70 MHz. Operation from 70 MHz up to 180 MHz is feasible using the on–chip transistor with a 5th or 7th overtone crystal. To enhance operation using an overtone crystal, the internal transistor’s bias is increased by adding an external resistor from Pin 23 to V_{EE}. –10 dBm of local oscillator drive is needed to adequately drive the mixer (Figure 10).

The oscillator configurations specified above, and two others using an external transistor, are described in the application section:

1) A 133 MHz oscillator multiplier using a 3rd overtone crystal, and
2) A 307.8 to 309.3 MHz manually tuned, varactor controlled local oscillator.

RSSI

The Received Signal Strength Indicator (RSSI) output is a current proportional to the log of the received signal amplitude. The RSSI current output is derived by summing the currents from the IF and limiting amplifier stages. An external resistor at Pin 20 sets the voltage range or swing of the RSSI output voltage. Linearity of the RSSI is optimized by using external ceramic or crystal bandpass filters which have an insertion loss of 8.0 dB. The RSSI circuit is designed to provide 70+ dB of dynamic range with temperature compensation (see Figures 6 and 7 which show RSSI responses of the IF and Limiter amplifiers). Variation in the RSSI output current with supply voltage is small (see Figure 11).

Carrier Detect

When the meter current flowing through the meter load resistance reaches 1.2 Vdc above ground, the comparator flips, causing the carrier detect output to go high. Hysteresis can be accomplished by adding a very large resistor for positive feedback between the output and the input of the comparator.

IF Amplifier

The first IF amplifier section is composed of three differential stages with the second and third stages contributing to the RSSI. This section has internal dc feedback and external input decoupling for improved symmetry and stability. The total gain of the IF amplifier block is approximately 39 dB at 10.7 MHz. Figure 5 shows the gain and saturated output response of the IF amplifier over temperature, while Figure 12 shows the IF amplifier gain as a function of the IF frequency.

The fixed internal input impedance is 1.4 kΩ. It is designed for applications where a 455 kHz ceramic filter is used and no external output matching is necessary since the filter requires a 1.4 kΩ source and load impedance.

For 10.7 MHz ceramic filter applications, an external 430 Ω resistor must be added in parallel to provide the equivalent load impedance of 330 Ω that is required by the filter; however, no external matching is necessary at the input since the mixer output matches the 330 Ω source impedance of the filter. For 455 kHz applications, an external 1.1 kΩ resistor must be added in series with the mixer output to obtain the required matching impedance of 1.4 kΩ of the filter input resistance. Overall RSSI linearity is dependent on having total midband attenuation of 12 dB (6.0 dB insertion loss plus 6.0 dB impedance matching loss) for the filter. The output of the IF amplifier is buffered and the impedance is 290 Ω.

Limiter

The limiter section is similar to the IF amplifier section except that four stages are used with the last three contributing to the RSSI. The fixed internal input impedance is 1.4 kΩ. The total gain of the limiting amplifier section is approximately 55 dB. This IF limiting amplifier section internally drives the quadrature detector section.

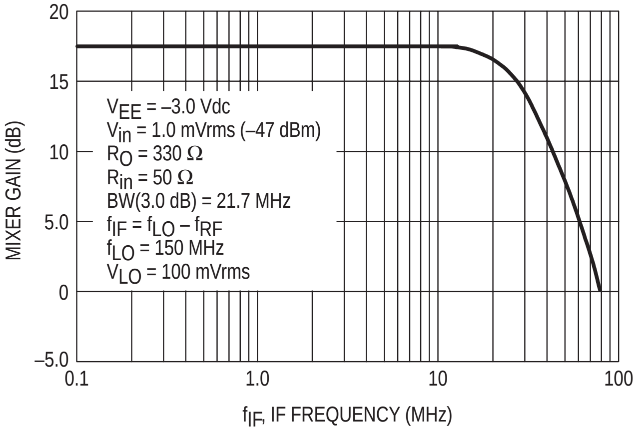


Figure 9. Mixer Gain versus IF Frequency

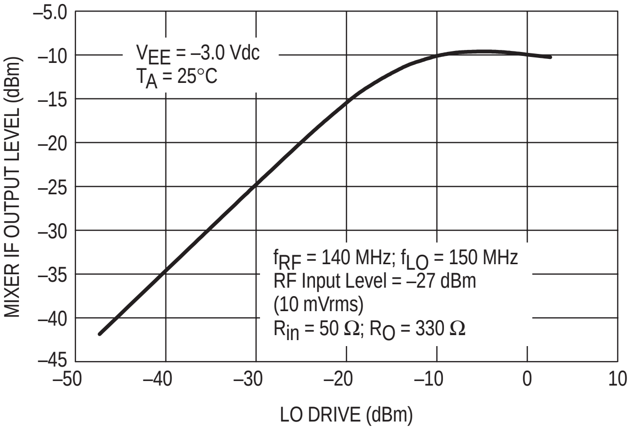


Figure 10. Mixer IF Output Level versus Local Oscillator Input Level

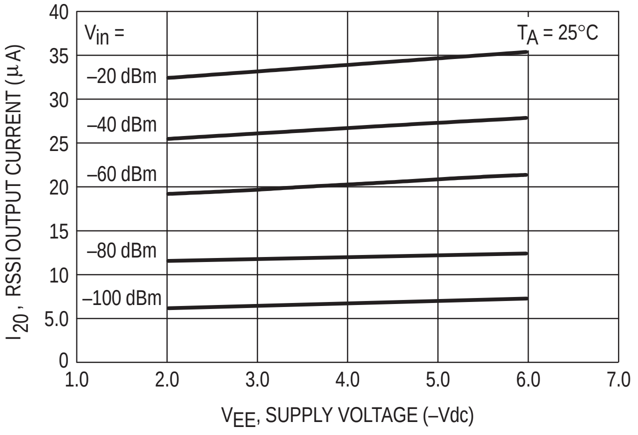


Figure 11. RSSI Output Current versus Supply Voltage and RF Input Signal Level

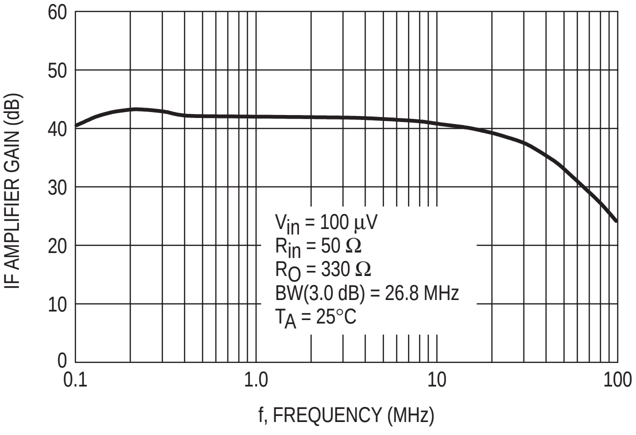


Figure 12. IF Amplifier Gain versus IF Frequency

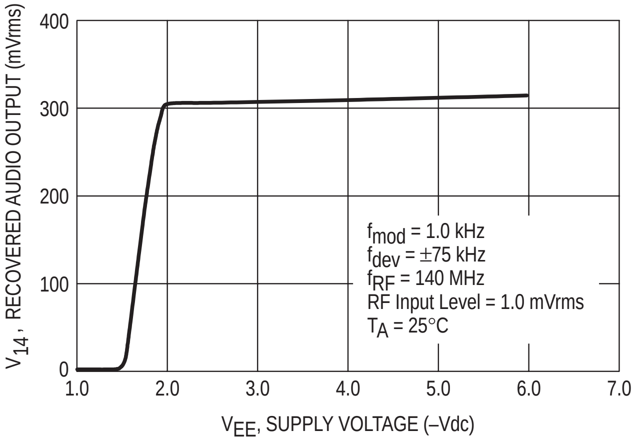


Figure 13. Recovered Audio Output Voltage versus Supply Voltage

Quadrature Detector

The quadrature detector is a doubly balanced four quadrant multiplier with an internal 5.0 pF quadrature capacitor to couple the IF signal to the external parallel RLC resonant circuit that provides the 90 degree phase shift and drives the quadrature detector. A single pin (Pin 13) provides for the external LC parallel resonant network and the internal connection to the quadrature detector.

The bandwidth of the detector allows for recovery of relatively high data rate modulation. The recovered signal is converted from differential to single ended through a push–pull NPN/PNP output stage. Variation in recovered audio output voltage with supply voltage is very small (see Figure 13). The output drive capability is approximately ±9.0 µA for a frequency deviation of ±75 kHz and 1.0 kHz modulating frequency (see Application Circuit).

Data Slicer

The data slicer input (Pin 15) is self centering around 1.1 V with clamping occurring at 1.1 ± 0.5 V_{be} Vdc. It is designed to square up the data signal. Figure 14 shows a detailed schematic of the data slicer.

The Voltage Regulator sets up 1.1 Vdc on the base of Q12, the Differential Input Amplifier. There is a potential of 1.0 V_{be} on the base–collector of transistor diode Q11 and 2.0 V_{be} on the base–collector of Q10. This sets up a 1.5 V_{be} (~ 1.1 Vdc) on the node between the 36 kΩ resistors which is connected to the base of Q12. The differential output of the data slicer Q12 and Q13 is converted to a single–ended output by the Driver Circuit. Additional circuitry, not shown in Figure 14, tends to keep the data slicer input centered at 1.1 Vdc as input signal levels vary.

The Input Diode Clamp Circuit provides the clamping at 1.0 V_{be} (0.75 Vdc) and 2.0 V_{be} (1.45 Vdc). Transistor diodes Q7 and Q8 are on, thus, providing a 2.0 V_{be} potential at the base of Q1. Also, the voltage regulator circuit provides a potential of 2.0 Vbe on the base of Q3 and 1.0 V_{be} on the emitter of Q3 and Q2. When the data slicer input (Pin 15) is pulled up, Q1 turns off; Q2 turns on, thereby clamping the input at 2.0 V_{be}. On the other hand, when Pin 15 is pulled down, Q1 turns on; Q2 turns off, thereby clamping the input at 1.0 V_{be}.

The recovered data signal from the quadrature detector is ac coupled to the data slicer via an input coupling capacitor. The size of this capacitor and the nature of the data signal determine how faithfully the data slicer shapes up the recovered signal. The time constant is short for large peak to peak voltage swings or when there is a change in dc level at the detector output. For small signal or for continuous bits of the same polarity which drift close to the threshold voltage, the time constant is longer. When centered there is no input current allowed, which is to say, that the input looks high in impedance.

Another unique feature of the data slicer is that it responds to various logic levels applied to the Data Slicer Hold Control pin (Pin 18). Figure 15 illustrates how the input and output currents under “no hold” condition relate to the input voltage. Figure 16 shows how the input current and input voltage relate for both the “no hold” and “hold” condition.

The hold control (Pin18) does three separate tasks:

1) With Pin 18 at 1.0 V_{be} or greater, the output is shut off (sets high). Q19 turns on which shunts the base drive from Q20, thereby turning the output off.

2) With Pin 18 at 2.0 V_{be} or greater, internal clamping diodes are open circuited and the comparator input is shut off and effectively open circuited. This is accomplished by turning off the current source to emitters of the input differential amplifier, thus, the input differential amplifier is shut off.

3) When the input is shut off, it allows the input capacitor to hold its charge during transmit to improve recovery at the beginning of the next receive period. When it is turned on, it allows for very fast charging of the input capacitor for quick recovery of new tuning or data average. The above features are very desirable in a TDD digital FM system.

Figure 14. Data Slicer Circuit

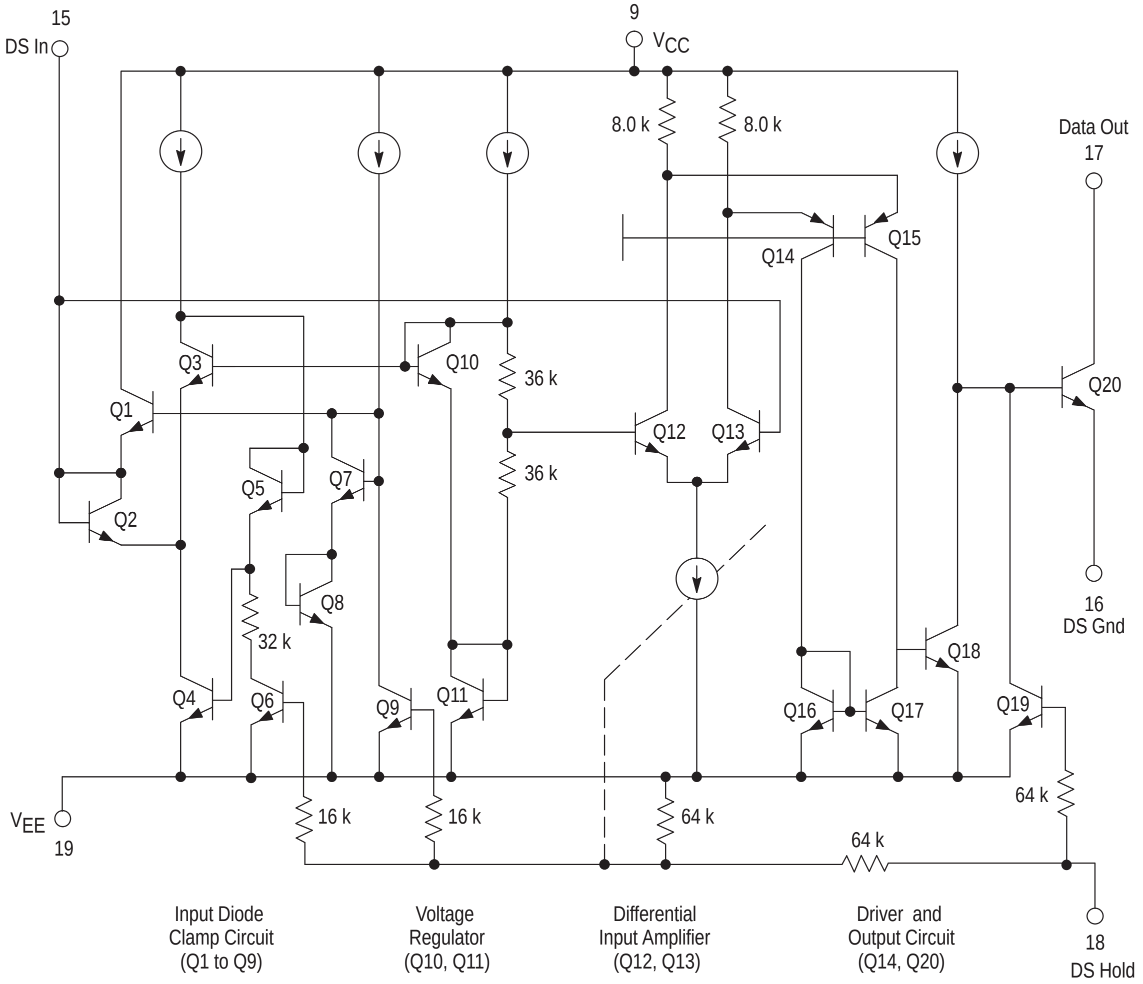


Figure 15. Data Slicer Input/Output Currents versus Input Voltage

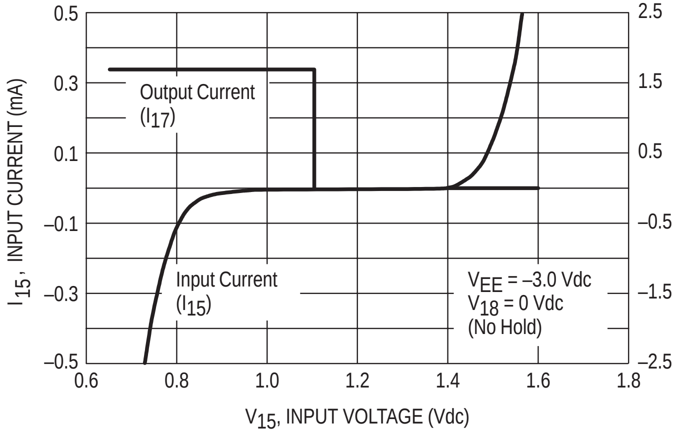


Figure 16. Data Slicer Input Current versus Input Voltage

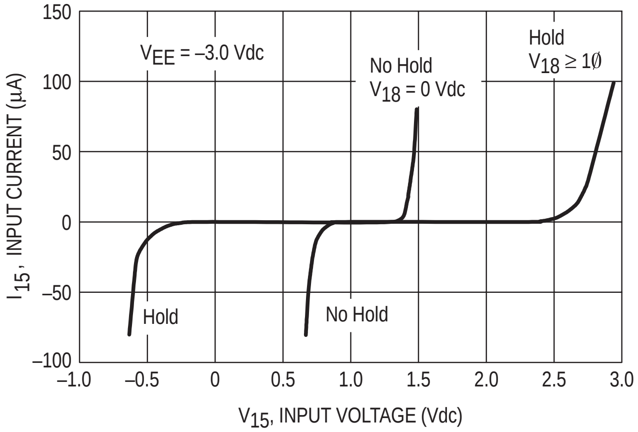
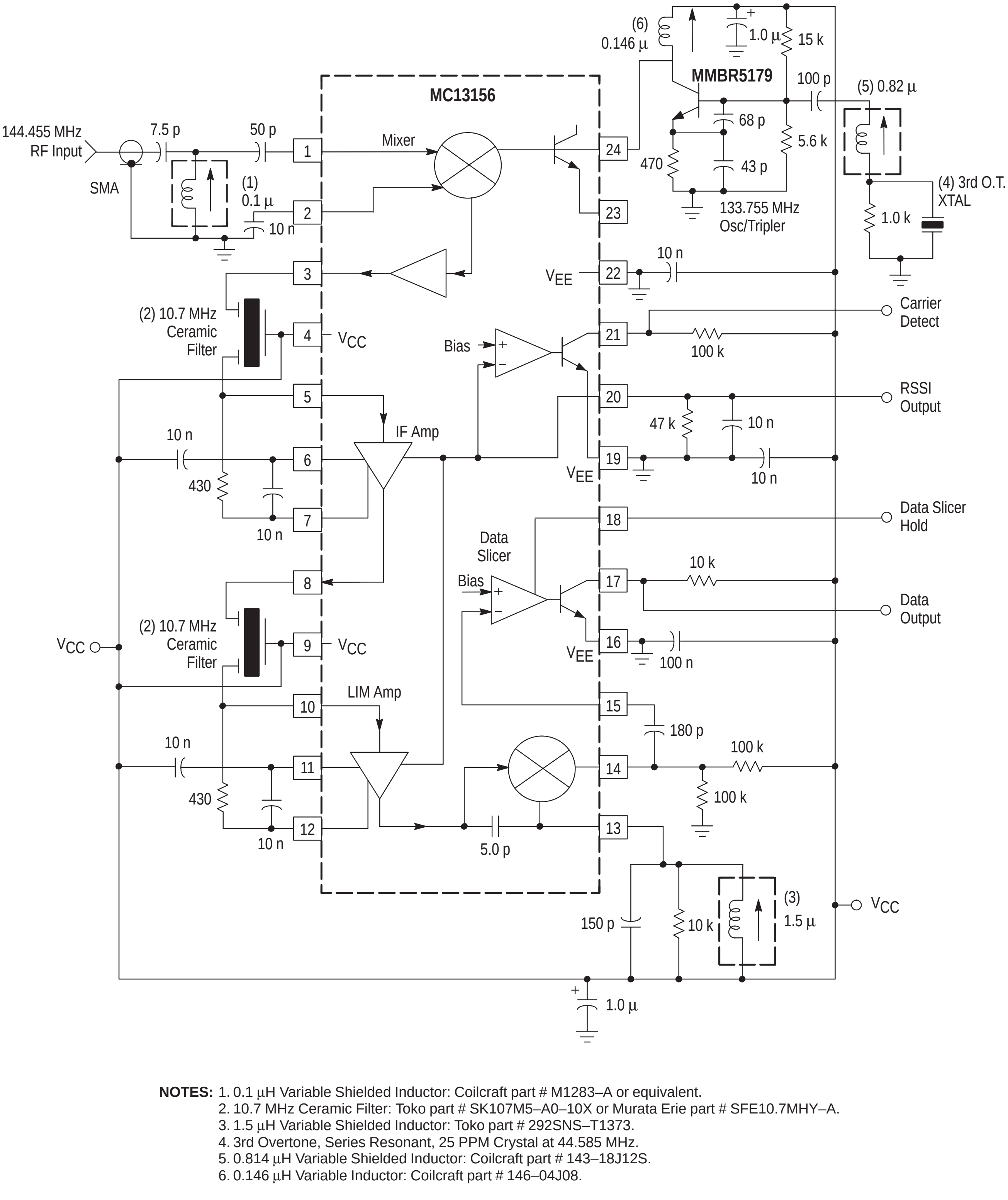


Figure 17. MC13156DW Application Circuit



NOTES:
1. 0.1 µH Variable Shielded Inductor: Coilcraft part # M1283–A or equivalent.
2. 10.7 MHz Ceramic Filter: Toko part # SK107M5–A0–10X or Murata Erie part # SFE10.7MHY–A.
3. 1.5 µH Variable Shielded Inductor: Toko part # 292SNS–T1373.
4. 3rd Overtone, Series Resonant, 25 PPM Crystal at 44.585 MHz.
5. 0.814 µH Variable Shielded Inductor: Coilcraft part # 143–18J12S.
6. 0.146 µH Variable Inductor: Coilcraft part # 146–04J08.

Figure 18. MC13156DW Circuit Side Component Placement

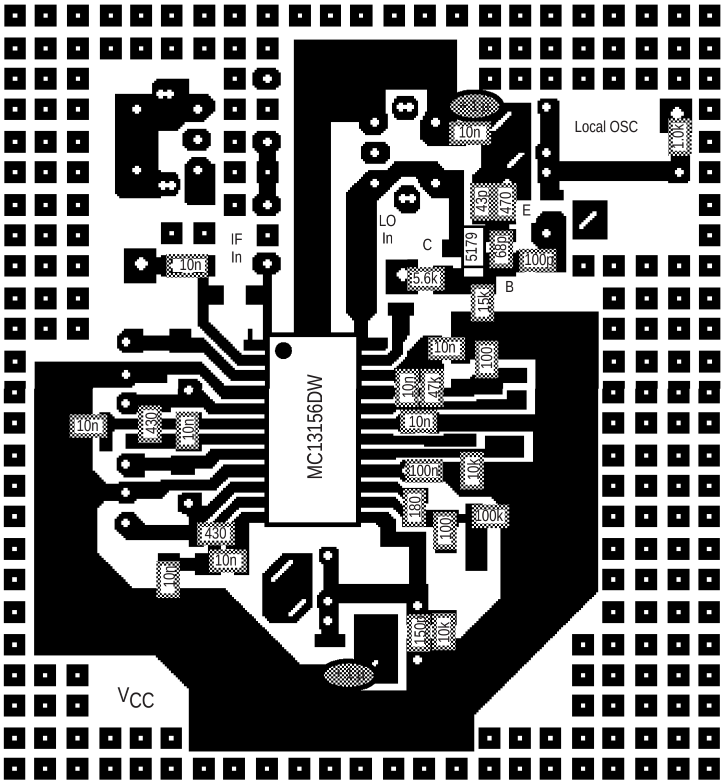
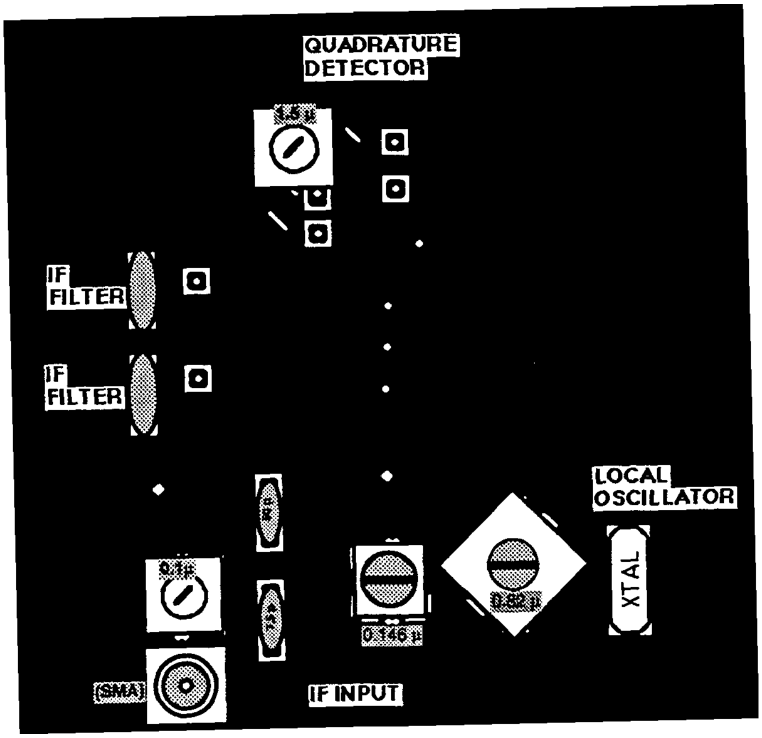


Figure 19. MC13156DW Ground Side Component Placement



APPLICATIONS INFORMATION

Component Selection

The evaluation PC board is designed to accommodate specific components, while also being versatile enough to use components from various manufacturers and coil types. Figures 18 and 19 show the placement for the components specified in the application circuit (Figure 17). The applications circuit schematic specifies particular components that were used to achieve the results shown in the typical curves and tables but equivalent components should give similar results.

Input Matching Networks/Components

The input matching circuit shown in the application circuit schematic is passive high pass network which offers effective image rejection when the local oscillator is below the RF input frequency. Silver mica capacitors are used for their high Q and tight tolerance. The PC board is not dedicated to any particular input matching network topology; space is provided for the designer to breadboard as desired.

Alternate matching networks using 4:1 surface mount transformers or BALUNs provide satisfactory performance. The 12 dB SINAD sensitivity using the above matching networks is typically –100 dBm for f_{mod} = 1.0 kHz and f_{dev} = ±75 kHz at f_{IN} = 144.45 MHz and f_{OSC} = 133.75 MHz (see Figure 25).

It is desirable to use a SAW filter before the mixer to provide additional selectivity and adjacent channel rejection and improved sensitivity. The SAW filter should be designed to interface with the mixer input impedance of approximately 1.0 kΩ. Table 1 displays the series equivalent single–ended mixer input impedance.

Local Oscillators

VHF Applications – The local oscillator circuit shown in the application schematic utilizes a third overtone crystal and an RF transistor. Selecting a transistor having good phase noise performance is important; a mandatory criteria is for the device to have good linearity of beta over several decades of collector current. In other words, if the low current beta is suppressed, it will not offer good 1/f noise performance. A third overtone series resonant crystal having at least 25 ppm tolerance over the operating temperature is recommended. The local oscillator is an impedance inversion third overtone Colpitts network and harmonic generator. In this circuit a 560 to 1.0 kΩ resistor shunts the crystal to ensure that it operates in its overtone mode; thus, a blocking capacitor is needed to eliminate the dc path to ground. The resulting parallel LC network should “free–run” near the crystal frequency if a short to ground is placed across the crystal. To provide sufficient output loading at the collector, a high Q variable inductor is used that is tuned to self resonate at the 3rd harmonic of the overtone crystal frequency.

The on–chip grounded collector transistor may be used for HF and VHF local oscillator with higher order overtone crystals. Figure 20 shows a 5th overtone oscillator at 93.3 MHz and Figure 21 shows a 7th overtone oscillator at 148.3 MHz. Both circuits use a Butler overtone oscillator configuration. The amplifier is an emitter follower. The crystal is driven from the emitter and is coupled to the high impedance base through a capacitive tap network. Operation at the desired overtone frequency is ensured by the parallel resonant circuit formed by the variable inductor and the tap capacitors and parasitic capacitances of the on–chip transistor and PC board. The variable inductor specified in the schematic could be replaced with a high tolerance, high Q ceramic or air wound surface mount component if the other components have good tolerances. A variable inductor provides an adjustment for gain and frequency of the resonant tank ensuring lock up and startup of the crystal oscillator. The overtone crystal is chosen with ESR of typically 80 Ω and 120 Ω maximum; if the resistive loss in the crystal is too high, the performance of the oscillator may be impacted by lower gain margins.

Table 1. Mixer Input Impedance Data
(Single–ended configuration, V_{CC} = 3.0 Vdc, local oscillator drive = 100 mVrms)

Frequency (MHz)	Series Equivalent Complex Impedance (R + jX) (Ω)	Parallel Resistance Rp (Ω)	Parallel Capacitance Cp (pF)
90	190 – j380	950	4.7
100	160 – j360	970	4.4
110	130 – j340	1020	4.2
120	110 – j320	1040	4.2
130	97 – j300	1030	4.0
140	82 – j280	1040	4.0
150	71 – j270	1100	4.0
160	59 – j260	1200	3.9
170	52 – j240	1160	3.9
180	44 – j230	1250	3.8
190	38 – j220	1300	3.8

A series LC network to ground (which is V_{CC}) is comprised of the inductance of the base lead of the on–chip transistor and PC board traces and tap capacitors. Parasitic oscillations often occur in the 200 to 800 MHz range. A small resistor is placed in series with the base (Pin 24) to cancel the negative resistance associated with this undesired mode of oscillation. Since the base input impedance is so large a small resistor in the range of 27 to 68 Ω has very little effect on the desired Butler mode of oscillation.

The crystal parallel capacitance, C_o, provides a feedback path that is low enough in reactance at frequencies of 5th overtone or higher to cause trouble. C_o has little effect near resonance because of the low impedance of the crystal motional arm (R_m–L_m–C_m). As the tunable inductor which forms the resonant tank with the tap capacitors is tuned off the crystal resonant frequency, it may be difficult to tell if the oscillation is under crystal control. Frequency jumps may occur as the inductor is tuned. In order to eliminate this behavior an inductor (L_o) is placed in parallel with the crystal. L_o is chosen to resonant with the crystal parallel capacitance (C_o) at the desired operation frequency. The inductor provides a feedback path at frequencies well below resonance; however, the parallel tank network of the tap capacitors and tunable inductor prevent oscillation at these frequencies.

UHF Application

Figure 22 shows a 318.5 to 320 MHz receiver which drives the mixer with an external varactor controlled (307.8 to 309.3 MHz) LC oscillator using an MPS901 (RF low power transistor in a TO–92 plastic package; also MMBR901 is available in a SOT–23 surface mount package). With the 50 kΩ 10 turn potentiometer this oscillator is tunable over a range of approximately 1.5 MHz. The MMBV909L is a low voltage varactor suitable for UHF applications; it is a dual back–to–back varactor in a SOT–23 package. The input matching network uses a 1:4 impedance matching transformer (Recommended sources are Mini–Circuits and Coilcraft).

Using the same IF ceramic filters and quadrature detector circuit as specified in the applications circuit in Figure 17, the 12 dB SINAD performance is –95 dBm for a f_{mod} = 1.0 kHz sinusoidal waveform and f_{dev} ±40 kHz.

This circuit is breadboarded using the evaluation PC board shown in Figures 32 and 33. The RF ground is V_{CC} and path lengths are minimized. High quality surface mount components were used except where specified. The absolute values of the components used will vary with layout placement and component parasitics.

RSSI Response

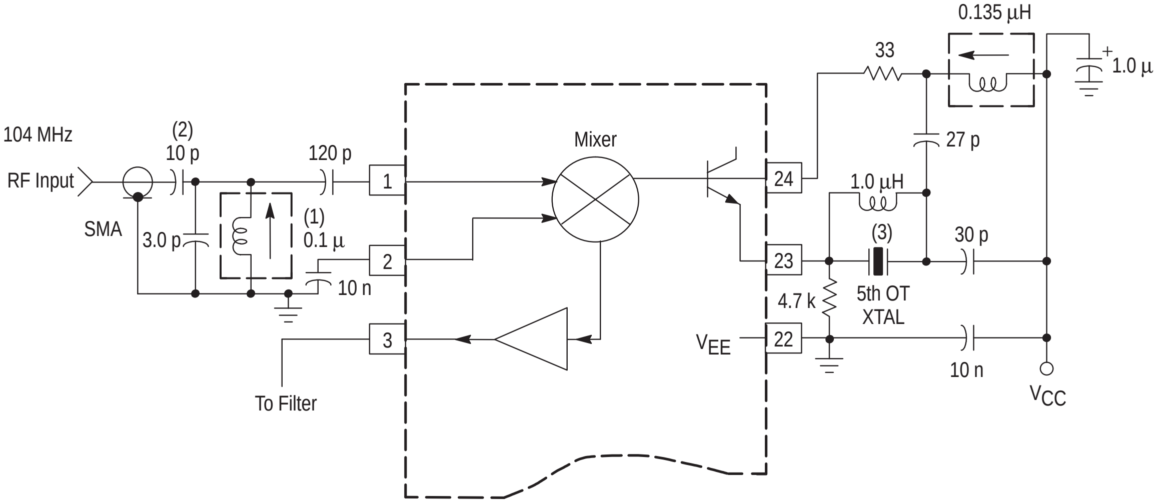
Figure 26 shows the full RSSI response in the application circuit. The 10.7 MHz, 110 kHz wide bandpass ceramic filters (recommended sources are TOKO part # SK107M5–AO–10X or Murata Erie SFE10.7MHY–A) provide the correct bandpass insertion loss to linearize the curve between the limiter and IF portions of RSSI. Figure 25 shows that limiting occurs at an input of –100 dBm. As shown in Figure 26, the RSSI output linear from –100 dBm to –30 dBm.

The RSSI rise and fall times for various RF input signal levels and R20 values are measured at Pin 20 without 10 nF filter capacitor. A 10 kHz square wave pulses the RF input signal on and off. Figure 27 shows that the rise and fall times are short enough to recover greater than 10 kHz ASK data; with a wider IF bandpass filters data rates up to 50 kHz may be achieved. The circuit used is the application circuit in Figure 17 with no RSSI output filter capacitor.

Figure 20. MC13156DW Application Circuit

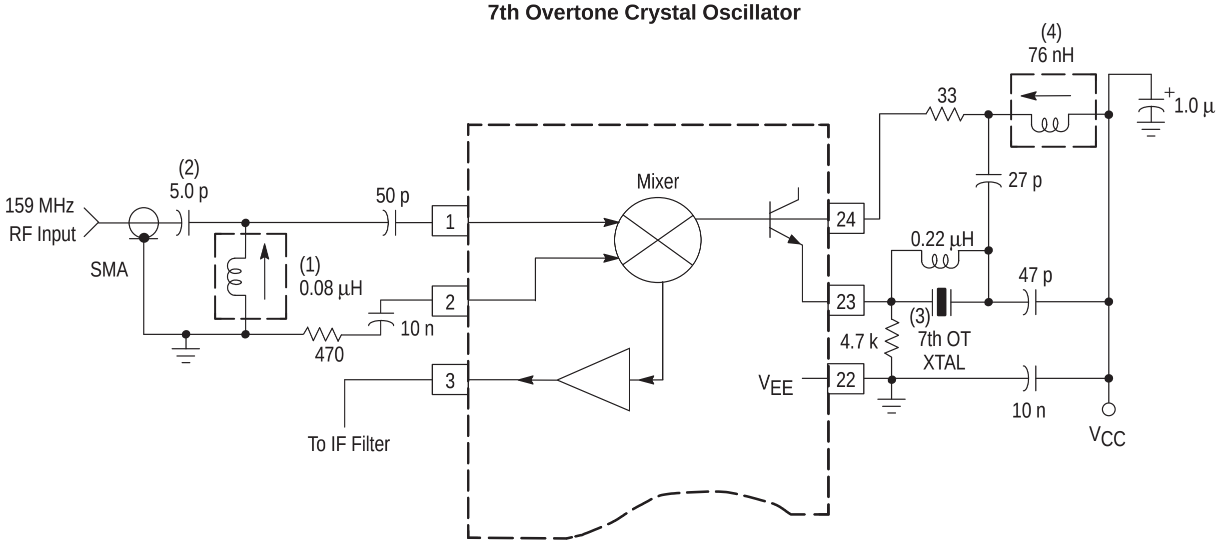
f_{RF} = 104 MHz; f_{LO} = 93.30 MHz

5th Overtone Crystal Oscillator



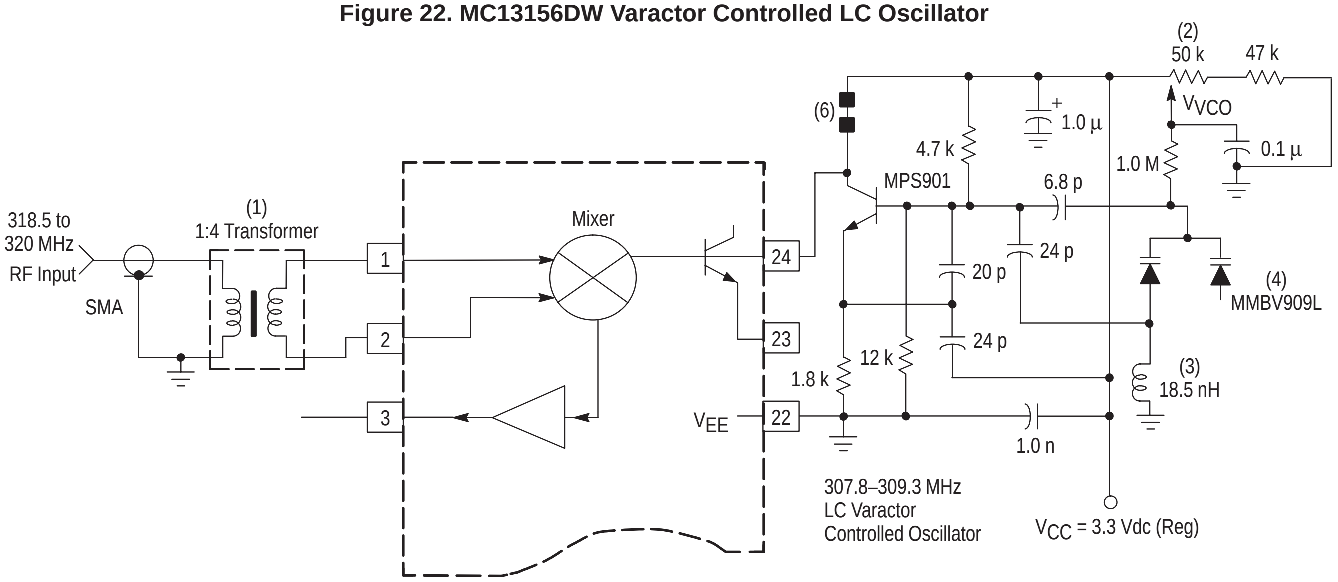
NOTES: 1. 0.1 µH Variable Shielded Inductor: Coilcraft part # M1283–A or equivalent.
2. Capacitors are Silver Mica.
3. 5th Overtone, Series Resonant, 25 PPM Crystal at 93.300 MHz.
4. 0.135 µH Variable Shielded Inductor: Coilcraft part # 146–05J08S or equivalent.

Figure 21. MC13156DW Application Circuit
f_{RF} = 159 MHz; f_{LO} = 148.30 MHz
7th Overtone Crystal Oscillator



NOTES: 1. 0.08 µH Variable Shielded Inductor: Toko part # 292SNS–T1365Z or equivalent.
2. Capacitors are Silver Mica.
3. 7th Overtone, Series Resonant, 25 PPM Crystal at 148.300 MHz.
4. 76 nH Variable Shielded Inductor: Coilcraft part # 150–03J08S or equivalent.

Figure 22. MC13156DW Varactor Controlled LC Oscillator



NOTES: 1. 1:4 Impedance Transformer: Mini–Circuits.
2. 50 k Potentiometer, 10 turns.
3. Spring Coil; Coilcraft A05T.
4. Dual Varactor in SOT–23 Package.
5. All other components are surface mount components.
6. Ferrite beads through loop of 24 AWG wire.

45 MHz Narrowband Receiver

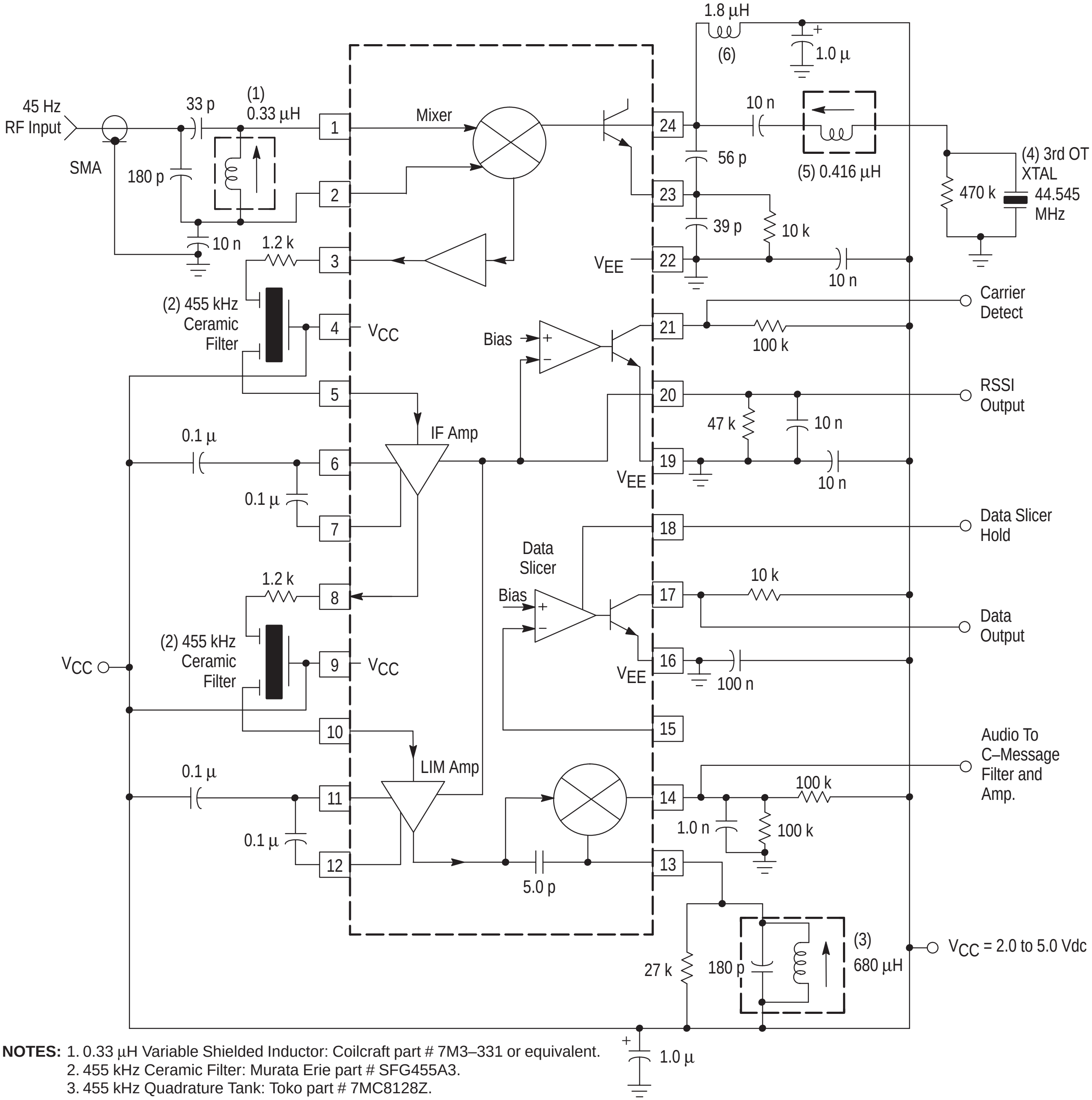
The above application examples utilize a 10.7 MHz IF. In this section a narrowband receiver with a 455 kHz IF will be described. Figure 23 shows a full schematic of a 45 MHz receiver that uses a 3rd overtone crystal with the on–chip oscillator transistor. The oscillator configuration is similar to the one used in Figure 17; it is called an impedance inversion Colpitts. A 44.545 MHz 3rd overtone, series resonant crystal is used to achieve an IF frequency at 455 kHz. The ceramic IF filters selected are Murata Erie part # SFG455A3. 1.2 kΩ chip resistors are used in series with the filters to achieve the terminating resistance of 1.4 kΩ to the filter. The IF decoupling is very important; 0.1 μF chip capacitors are used at Pins 6, 7, 11 and 12. The quadrature detector tank circuit uses a 455 kHz quadrature tank from Toko.

The 12 dB SINAD performance is –109 dBm for a f_{mod} = 1.0 kHz and a f_{dev} = ±4.0 kHz. The RSSI dynamic range is approximately 80 dB of linear range (see Figure 24).

Receiver Design Considerations

The curves of signal levels at various portions of the application receiver with respect to RF input level are shown in Figure 28. This information helps determine the network topology and gain blocks required ahead of the MC13156 to achieve the desired sensitivity and dynamic range of the receiver system. In the application circuit the input third order intercept (IP3) performance of the system is approximately –25 dBm (see Figure 29).

Figure 23. MC13156DW Application Circuit at 45 MHz



NOTES: 1. 0.33 μH Variable Shielded Inductor: Coilcraft part # 7M3–331 or equivalent.
2. 455 kHz Ceramic Filter: Murata Erie part # SFG455A3.
3. 455 kHz Quadrature Tank: Toko part # 7MC8128Z.
4. 3rd Overtone, Series Resonant, 25 PPM Crystal at 44.540 MHz.
5. 0.416 μH Variable Shielded Inductor: Coilcraft part # 143–10J12S.
6. 1.8 μH Molded Inductor.

Figure 24. RSSI Output Voltage versus Input Signal Level

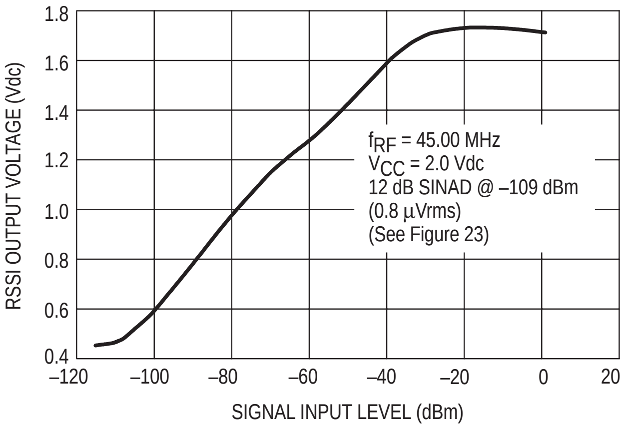


Figure 25. S + N/N versus RF Input Signal Level

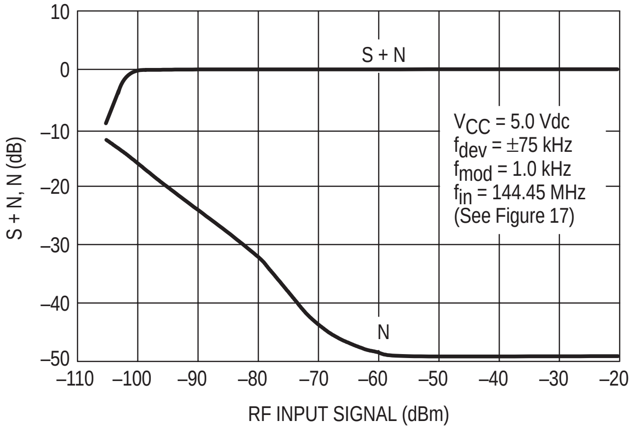


Figure 26. RSSI Output Voltage versus Input Signal Level

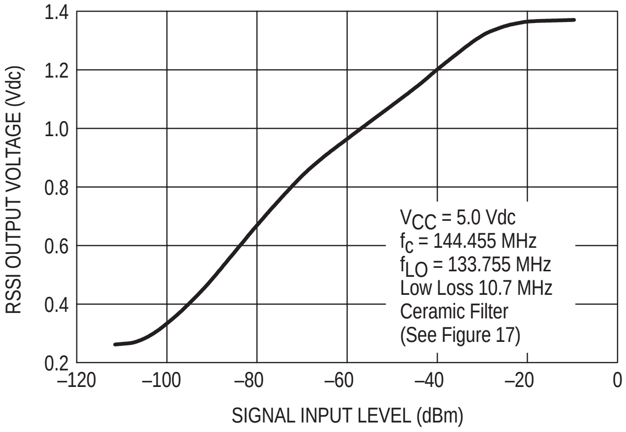


Figure 27. RSSI Output Rise and Fall Times versus RF Input Signal Level

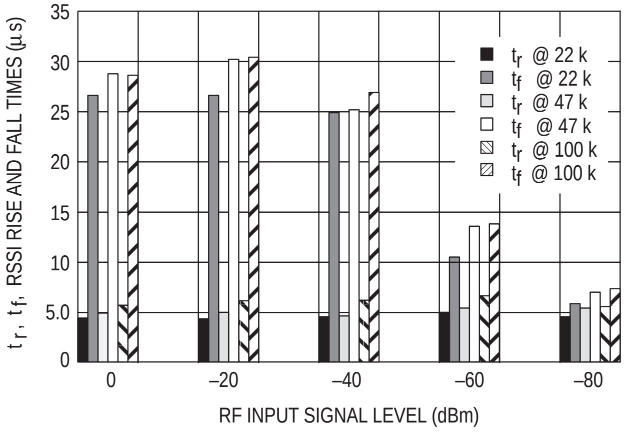


Figure 28. Signal Levels versus RF Input Signal Level

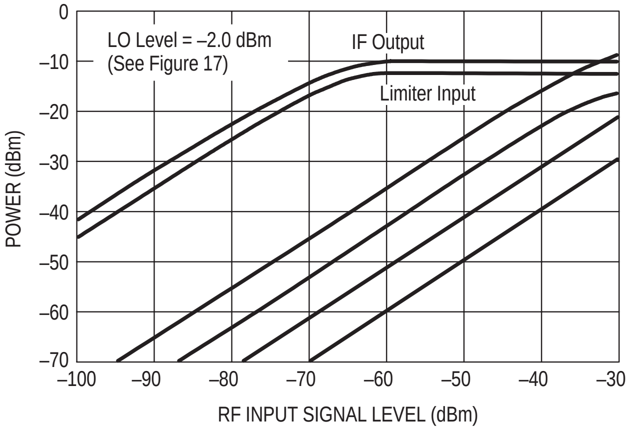
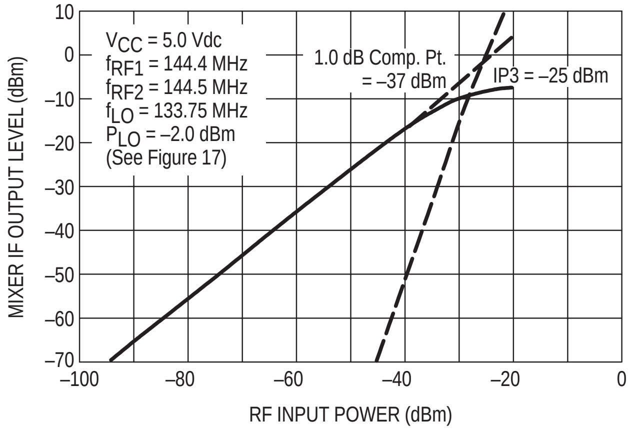


Figure 29. 1.0 dB Compression Pt. and Input Third Order Intercept Pt. versus Input Power



BER TESTING AND PERFORMANCE

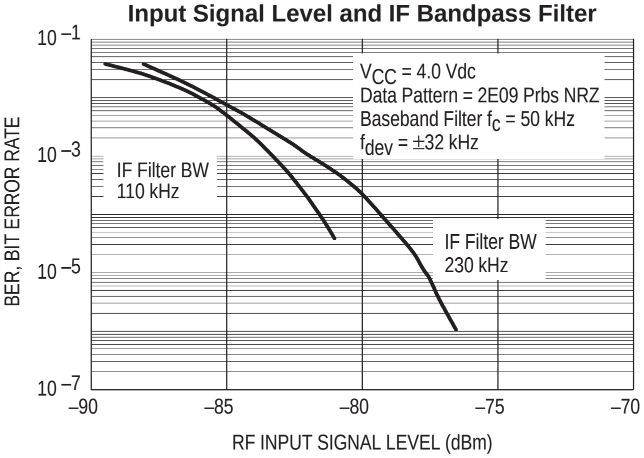
Description

The test setup shown in Figure 30 is configured so that the function generator supplies a 100 kHz clock source to the bit error rate tester. This device generates and receives a repeating data pattern and drives a 5 pole baseband data filter. The filter effectively reduces harmonic content of the baseband data which is used to modulate the RF generator which is running at 144.45 MHz. Following processing of the signal by the receiver (MC13156), the recovered baseband sinewave (data) is AC coupled to the data slicer. The data slicer is essentially an auto–threshold comparator which tracks the zero crossing of the incoming sinewave and provides logic level data at its ouput. Data errors associated with the recovered data are collected by the bit error rate receiver and displayed.

Bit error rate versus RF signal input level and IF filter bandwidth are shown in Figure 31. The bit error rate data was taken under the following test conditions:

- Data rate = 100 kbps
- Filter cutoff frequency set to 39% of the data rate or 39 kHz.
- Filter type is a 5 pole equal–ripple with 0.5° phase error.
- V_{CC} = 4.0 Vdc
- Frequency deviation = ±32 kHz.

Figure 31. Bit Error Rate versus RF Input Signal Level and IF Bandpass Filter



Evaluation PC Board

The evaluation PCB is very versatile and is intended to be used across the entire useful frequency range of this device. The center section of the board provides an area for attaching all SMT components to the circuit side and radial leaded components to the component ground side (see Figures 32 and 33). Additionally, the peripheral area surrounding the RF core provides pads to add supporting and interface circuitry as a particular application dictates.

Figure 30. Bit Error Rate Test Setup

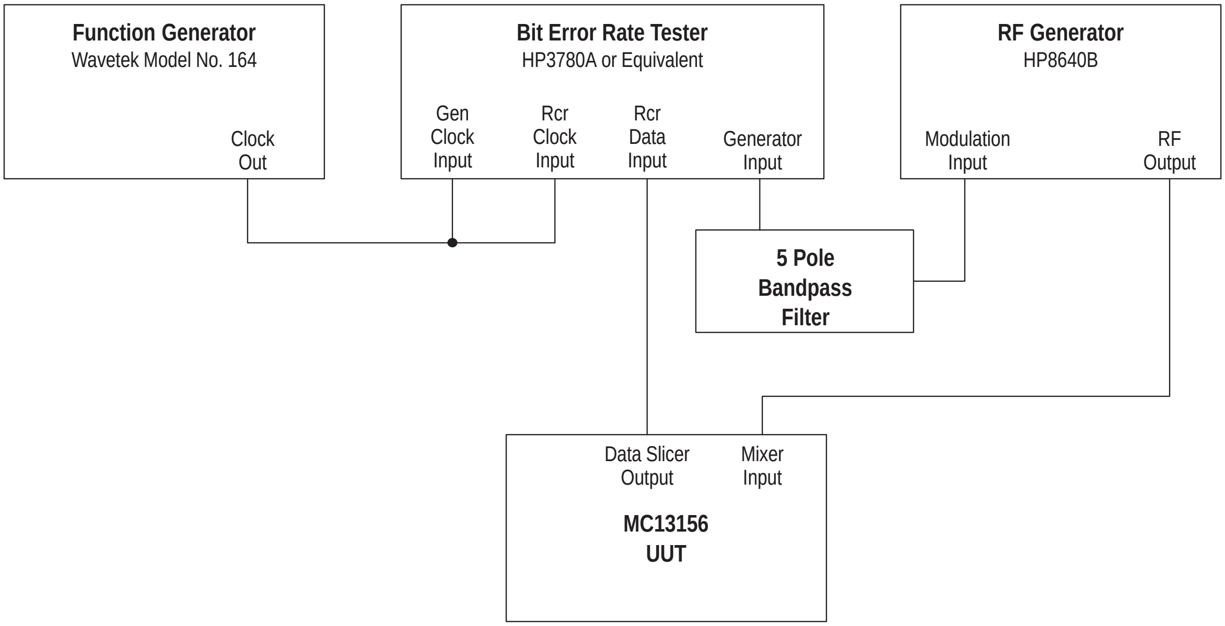


Figure 32. Circuit Side View

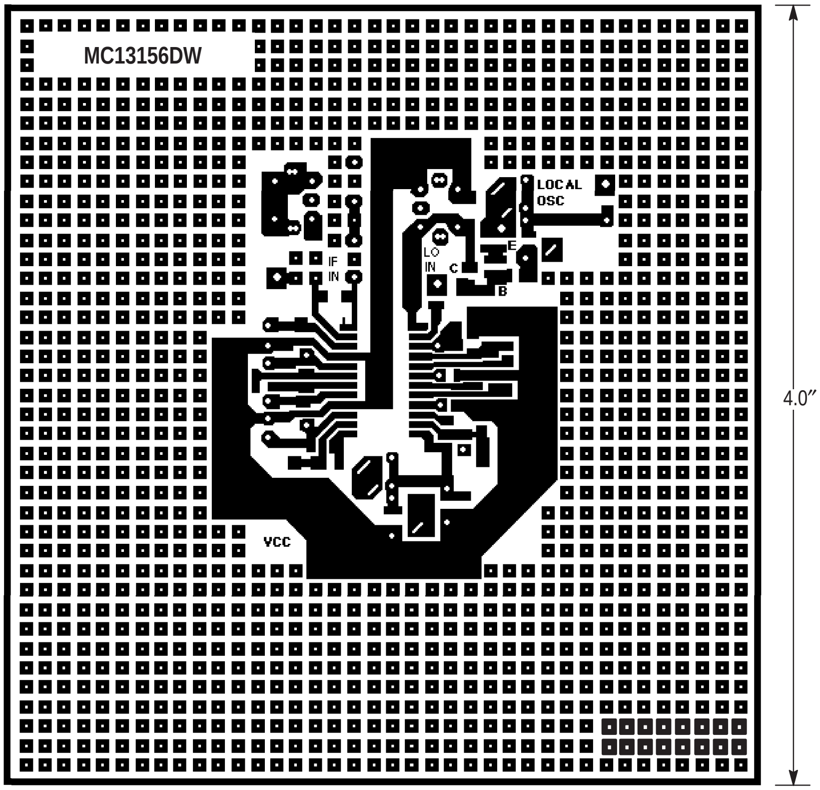
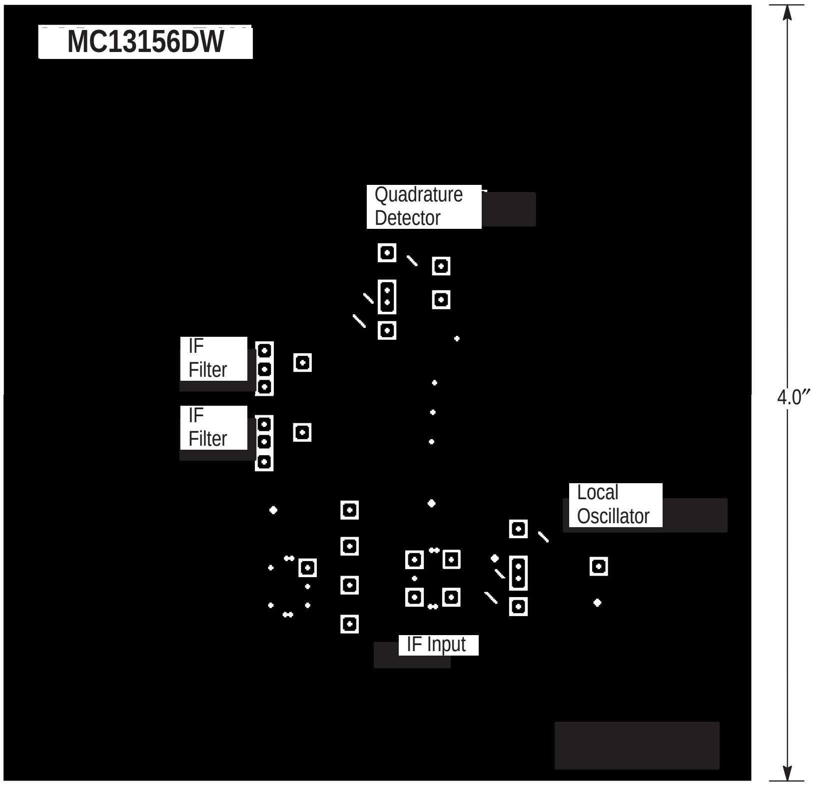


Figure 33. Ground Side View



MOTOROLA

MC13158

Wideband FM IF Subsystem

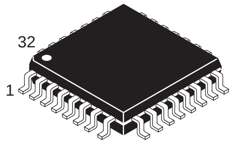
The MC13158 is a wideband IF subsystem that is designed for high performance data and analog applications. Excellent high frequency performance is achieved, with low cost, through the use of Motorola's MOSAIC 1.5™ RF bipolar process. The MC13158 has an on–board grounded collector VCO transistor that may be used with a fundamental or overtone crystal in single channel operation or with a PLL in multi–channel operation. The mixer is useful to 500 MHz and may be used in a balanced differential or single ended configuration. The IF amplifier is split to accommodate two low cost cascaded filters. RSSI output is derived by summing the output of both IF sections. A precision data shaper has an Off function to shut the output off to save current. An enable control is provided to power down the IC for power management in battery operated applications.

Applications include DECT, wideband wireless data links for personal and portable laptop computers and other battery operated radio systems which utilize GFSK, FSK or FM modulation.

- Designed for DECT Applications
- 1.8 to 6.0 Vdc Operating Voltage
- Low Power Consumption in Active and Standby Mode
- Greater than 600 kHz Detector Bandwidth
- Data Slicer with Special Off Function
- Enable Function for Power Down of Battery Operated Systems
- RSSI Dynamic Range of 80 dB Minimum
- Low External Component Count

WIDEBAND FM IF SUBSYSTEM FOR DECT AND DIGITAL APPLICATIONS

SEMICONDUCTOR
TECHNICAL DATA

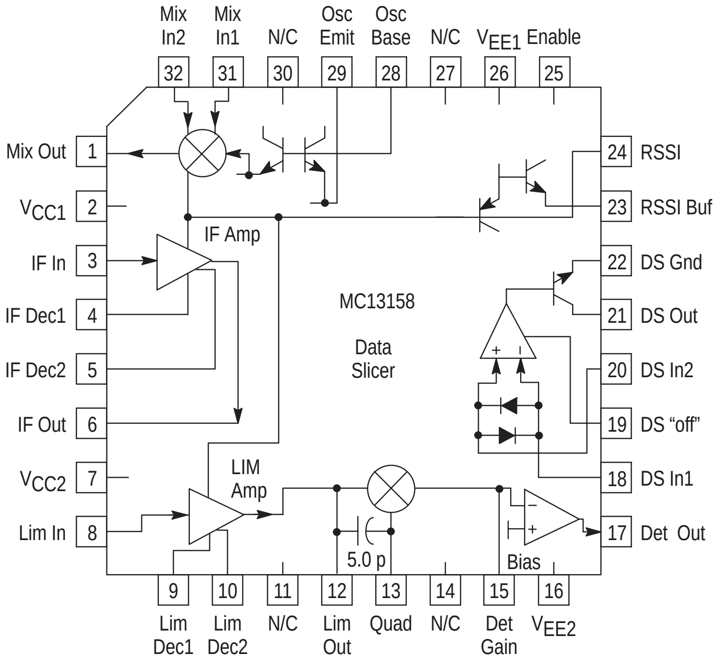


FTB SUFFIX
PLASTIC PACKAGE
CASE 873
(Thin QFP)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC13158FTB	T_A = – 40 to +85°C	TQFP–32

Representative Block Diagram



This device contains 234 active transistors.

MAXIMUM RATINGS

Rating	Pin	Symbol	Value	Unit
Power Supply Voltage	16, 26	$V_{S(max)}$	6.5	Vdc
Junction Temperature		T_{JMAX}	+150	°C
Storage Temperature Range		T_{stg}	–65 to +150	°C

NOTE: 1. Devices should not be operated at or outside these values. The “Recommended Operating Conditions” provide for actual device operation.

RECOMMENDED OPERATING CONDITIONS ($V_{CC} = V_2 = V_7$; $V_{EE} = V_{16} = V_{22} = V_{26}$; $V_S = V_{CC} – V_{EE}$)

Rating	Pin	Symbol	Value	Unit
Power Supply Voltage $T_A = 25°C$ $–40°C \le T_A \le 85°C$	2, 7 16, 26	V_S	2.0 to 6.0	Vdc
Input Frequency	31, 32	F_{in}	10 to 500	MHz
Ambient Temperature Range		T_A	–40 to +85	°C
Input Signal Level	31, 32	V_{in}	200	mVrms

DC ELECTRICAL CHARACTERISTICS ($T_A = 25°C$; $V_S = 3.0$ Vdc; No Input Signal; See Figure 1.)

Characteristic	Condition	Pin	Symbol	Min	Typ	Max	Unit
Total Drain Current	$V_S = 2.0$ Vdc	16, 26	I_{TOTAL}	2.5	5.5	8.5	mA
	$V_S = 3.0$ Vdc			3.5	5.7	8.5	
	$V_S = 6.0$ Vdc See Figure 2			3.5	6.0	9.5	
DATA SLICER (Input Voltage Referenced to V_{EE}; $V_S = 3.0$ Vdc; No Input Signal)							
Output Current; V_{18} LO; Data Slicer Enabled (DS “on”)	$V_{19} = V_{EE}$ $V_{18} < V_{20}$ $V_{20} = V_S/2$ See Figure 3	21	I_{21}	2.0	5.9	–	mA
Output Current; V_{18} HI; Data Slicer Enabled (DS “on”)	$V_{19} = V_{EE}$ $V_{18} > V_{20}$ $V_{20} = V_S/2$ See Figure 4	21	I_{21}	–	0.1	1.0	µA
Output Current; Data Slicer Disabled (DS “off”)	$V_{19} = V_{CC}$ $V_{20} = V_S/2$	21	I_{21}	–	0.1	1.0	µA

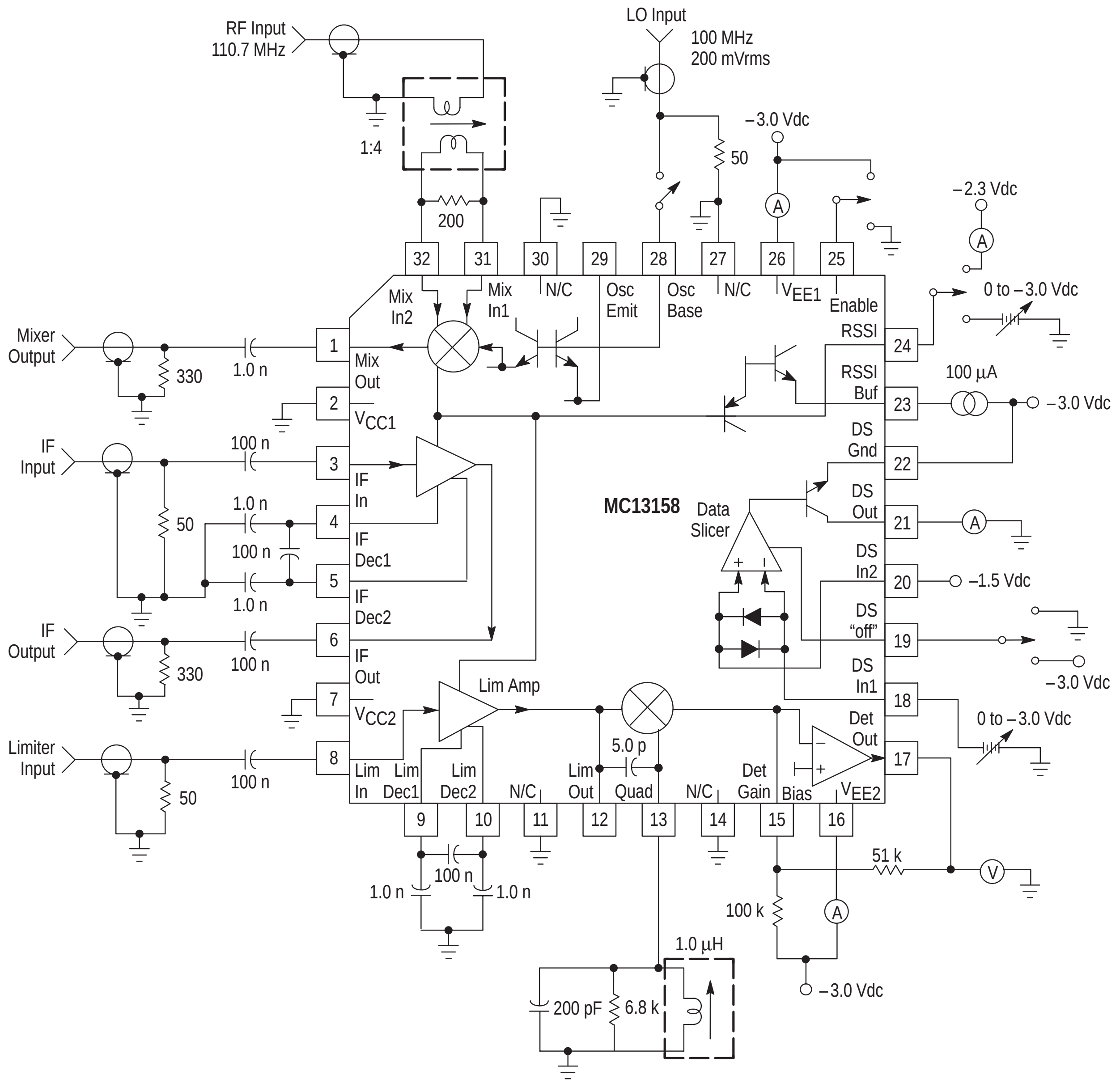
AC ELECTRICAL CHARACTERISTICS ($T_A = 25°C$; $V_S = 3.0$ Vdc; $f_{RF} = 110.7$ MHz; $f_{LO} = 100$ MHz; See Figure 1.)

Characteristic	Condition	Pin	Symbol	Min	Typ	Max	Unit
MIXER							
Mixer Conversion Gain	$V_{in} = 1.0$ mVrms See Figure 5	31, 32, 1	–	–	22	–	dB
Noise Figure	Input Matched	31, 32, 1	NF	–	14	–	dB
Mixer Input Impedance	Single–Ended See Figure 15	31, 32	Rp Cp	– –	865 1.6	– –	Ω pF
Mixer Output Impedance		1	–	–	330	–	Ω

AC ELECTRICAL CHARACTERISTICS (continued) (T_A = 25°C; V_S = 3.0 Vdc; f_{RF} = 110.7 MHz; f_{LO} = 100 MHz; See Figure 1.)

Characteristic	Condition	Pin	Symbol	Min	Typ	Max	Unit
IF AMPLIFIER SECTION							
IF RSSI Slope	See Figure 8	23	–	0.15	0.3	0.4	µA/dB
IF Gain	f = 10.7 MHz See Figure 7	3, 6	–	–	36	–	dB
Input Impedance		3	–	–	330	–	Ω
Output Impedance		6	–	–	330	–	Ω
LIMITING AMPLIFIER SECTION							
Limiter RSSI Slope	See Figure 9	23	–	0.15	0.3	0.4	µA/dB
Limiter Gain	f = 10.7 MHz	8, 12	–	–	70	–	dB
Input Impedance		8	–	–	330	–	Ω

Figure 1. Test Circuit



Typical Performance Over Temperature

(per Figure 1)

Figure 2. Total Supply Current versus Ambient Temperature, Supply Voltage

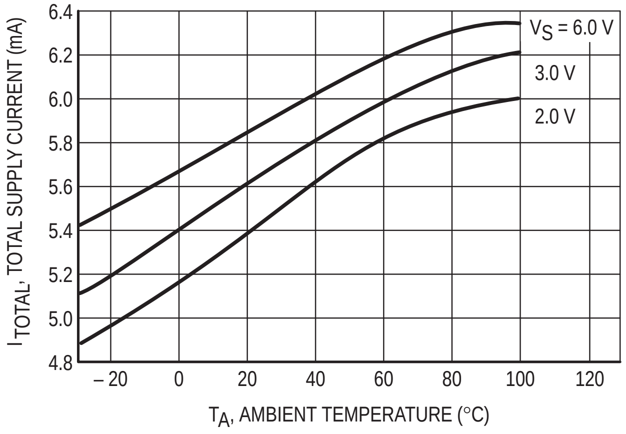


Figure 3. Data Slicer On Output Current versus Ambient Temperature

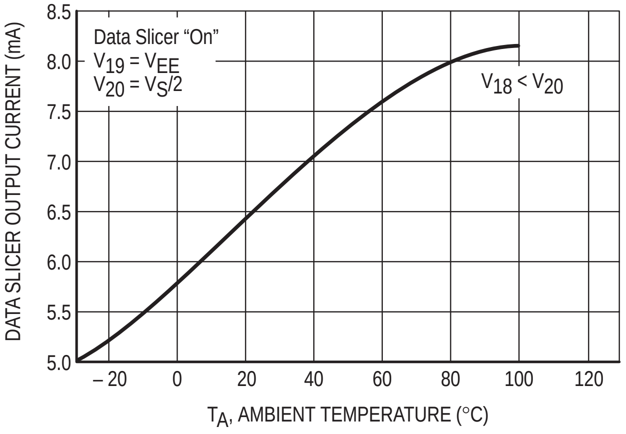


Figure 4. Data Slicer On Output Current versus Ambient Temperature

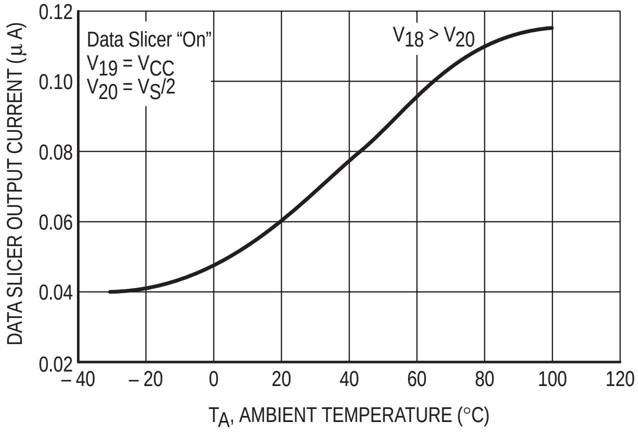


Figure 5. Normalized Mixer Gain versus Ambient Temperature

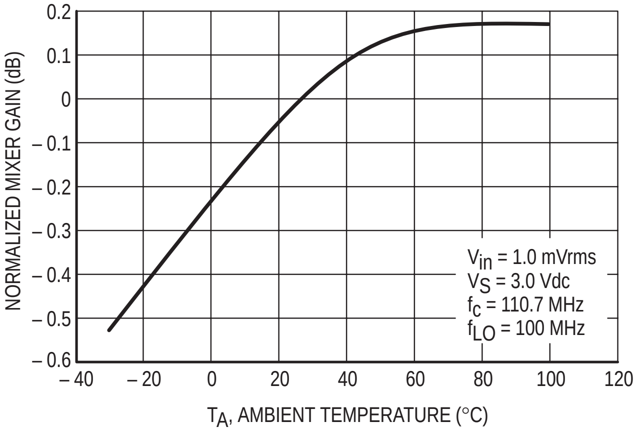


Figure 6. Mixer RSSI Output Current versus Ambient Temperature, Mixer Input Level

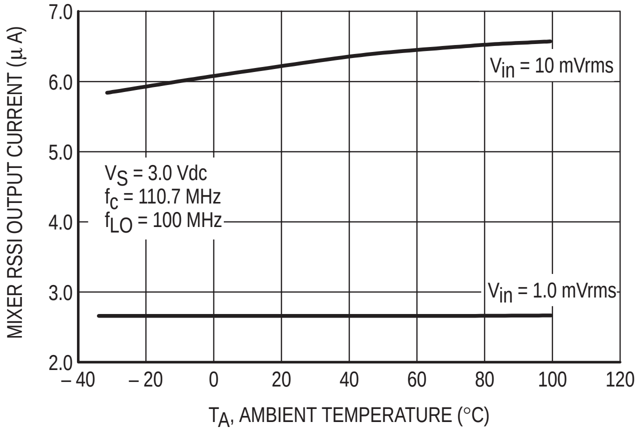
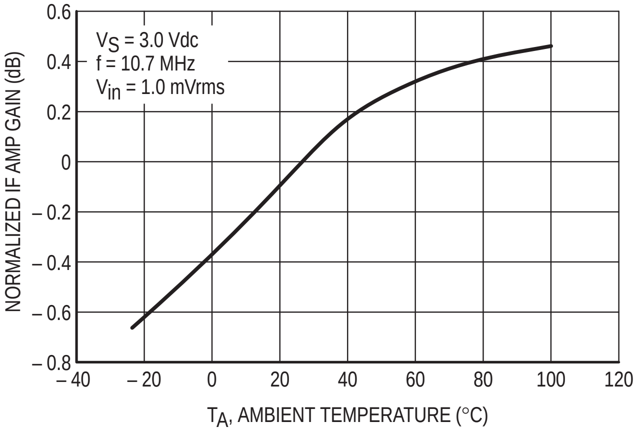


Figure 7. Normalized IF Amp Gain versus Ambient Temperature



tTypical Performance Over Temperature

(per Figure 1)

Figure 8. IF Amp RSSI Output Current versus Ambient Temperature, IF Input Level

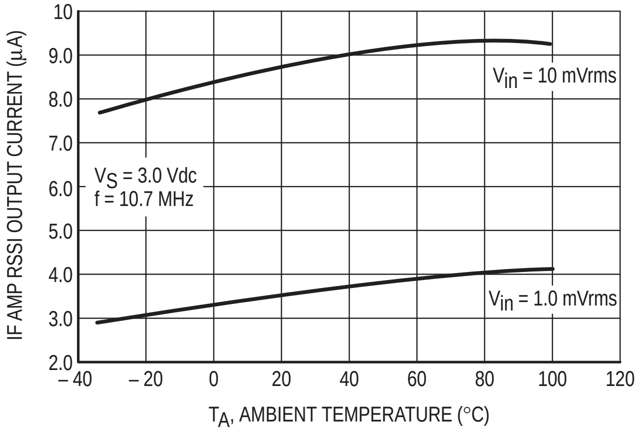


Figure 9. Limiter Amp RSSI Output Current versus Ambient Temperature, Input Signal Level

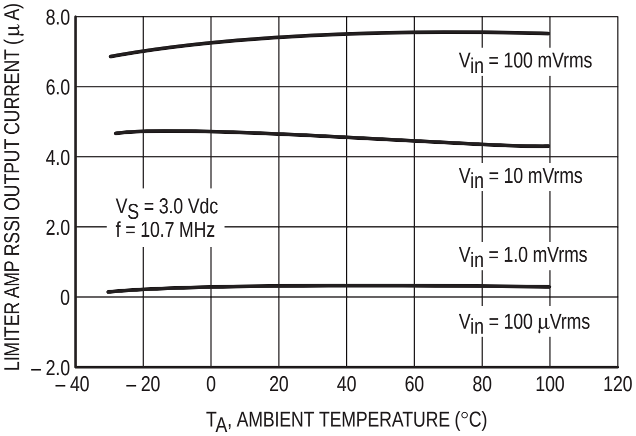


Figure 10. Total RSSI Output Current versus Ambient Temperature (No Signal)

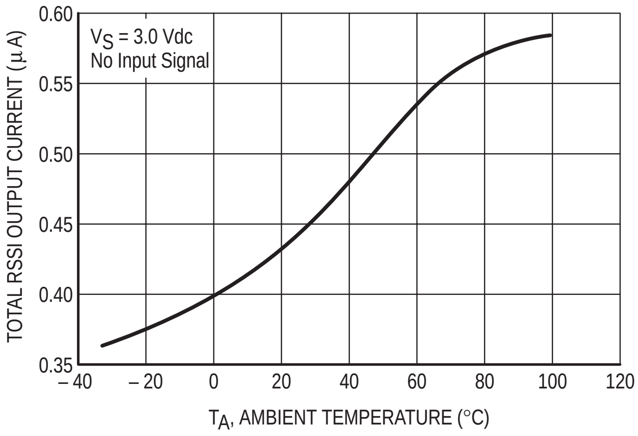
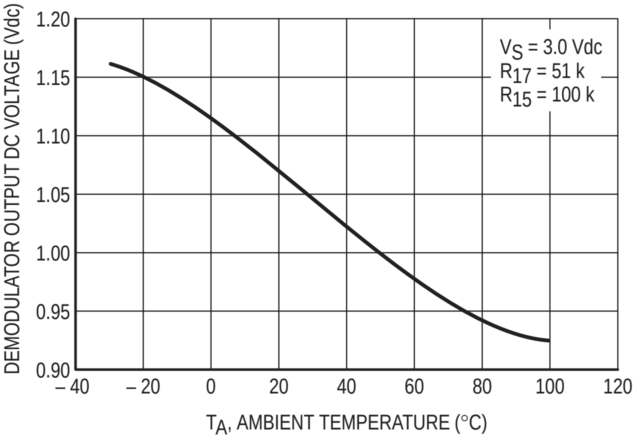


Figure 11. Demodulator DC Voltage versus Ambient Temperature



SYSTEM LEVEL AC ELECTRICAL CHARACTERISTICS (T_A = 25°C; V_S = 3.0 Vdc; f_{RF} = 112 MHz; f_{LO} = 122.7 MHz)

Characteristic	Condition	Notes	Symbol	Typ	Unit
12 dB SINAD Sensitivity: Narrowband Application	f_{RF} = 112 MHz f_{mod} = 1.0 kHz f_{dev} = ±125 kHz SINAD Curve	1	–		dBm
Without Preamp	Figure 25			–101	
With Preamp	Figure 26			–113	
Third Order Intercept Point	f_{RF1} = 112 MHz f_{RF2} = 112.1 MHz	2	IIP3	–32	dBm
1.0 dB Comp. Point	V_S = 3.5 Vdc Figure 28		1.0 dB C.Pt.	–39	

NOTES: 1. Test Circuit & Test Set per Figure 24.
2. Test Circuit & Test Set per Figure 27.

CIRCUIT DESCRIPTION

General

The MC13158 is a low power single conversion wideband FM receiver incorporating a split IF. This device is designated for use as the backend in digital FM systems such as Digital European Cordless Telephone (DECT) and wideband data links with data rates up to 2.0 Mbps. It contains a mixer, oscillator, Received Signal Strength Indicator (RSSI), IF amplifier, limiting IF, quadrature detector, power down or enable function, and a data slicer with output off function. Further details are covered in the Pin Function Description which shows the equivalent internal circuit and external circuit requirements.

Current Regulation/Enable

Temperature compensating voltage independent current regulators which are controlled by the enable pin (Pin 25) where “low” powers up and “high” powers down the entire circuit.

Mixer

The mixer is a double–balanced four quadrant multiplier and is designed to work up to 500 MHz. It can be used in differential or in single ended mode by connecting the other input to the positive supply rail. The linear gain of the mixer is approximately 22 dB at 100 mVrms LO drive level. The mixer gain and noise figure have been emphasized at the expense of intermodulation performance. RSSI measurements are added in the mixer to extend the range to higher signal levels. The single–ended parallel equivalent input impedance of the mixer is Rp ~ 1.0 kΩ and Cp ~ 2.0 pF. The buffered output of the mixer is internally loaded resulting in an output impedance of 330 Ω.

Local Oscillator

The on–chip transistor operates with crystal and LC resonant elements up to 220 MHz. Series resonant, overtone crystals are used to achieve excellent local oscillator stability. Third overtone crystals are used through about 65 to 70 MHz. Operation from 70 MHz up to 180 MHz is feasible using the on–chip transistor with a 5th or 7th overtone crystal. To enhance operation using an overtone crystal, the internal transistor bias is increased by adding an external resistor from Pin 29 to V_{EE}; however, with an external resistor the oscillator stays on during power down. Typically, –10 dBm of local oscillator drive is needed to adequately drive the mixer. With an external oscillator source, the IC can be operated up to 500 MHz.

RSSI

The received signal strength indicator (RSSI) output is a current proportional to the log of the received signal amplitude. The RSSI current output is derived by summing the currents from the mixer, IF and limiting amplifier stages. An increase in RSSI dynamic range, particularly at higher input signal levels is achieved. The RSSI circuit is designed to provide typically 85 dB of dynamic range with temperature compensation.

Linearity of the RSSI is optimized by using external ceramic bandpass filters which have an insertion loss of 4.0 dB and 330 Ω source and load impedance. For higher data rates used in DECT and related applications, LC bandpass filtering is necessary to acquire the desired bandpass response; however, the RSSI linearity will require the same insertion loss.

RSSI Buffer

The RSSI output current creates a voltage across an external resistor. A unity voltage–gain amplifier is used to buffer this voltage. The output of this buffer has an active pull–up but no pull–down, so it can also be used as a peak detector. The negative slew rate is determined by external capacitance and resistance to the negative supply.

IF Amplifier

The first IF amplifier section is composed of three differential stages with the second and third stages contributing to the RSSI. This section has internal DC feedback and external input decoupling for improved symmetry and stability. The total gain of the IF amplifier block is approximately 40 dB at 10.7 MHz.

The fixed internal input impedance is 330 Ω. When using ceramic filters requiring source and loss impedances of 330 Ω, no external matching is necessary. Overall RSSI linearity is dependent on having total midband attenuation of 10 dB (4.0 dB insertion loss plus 6.0 dB impedance matching loss) for the filter. The output of the IF amplifier is buffered and the impedance is 330 Ω.

Limiter

The limiter section is similar to the IF amplifier section except that five differential stages are used. The fixed internal input impedance is 330 Ω. The total gain of the limiting amplifier section is approximately 70 dB. This IF limiting amplifier section internally drives the quadrature detector section and it is also brought out on Pin 12.

Quadrature Detector

The quadrature detector is a doubly balanced four quadrant multiplier with an internal 5.0 pF quadrature capacitor between Pins 12 and 13. An external capacitor may be added between these pins to increase the IF signal to the external parallel RLC resonant circuit that provides the 90 degree phase shift and drives the quadrature detector. A single pin (Pin 13) provides for the external LC parallel resonant network and the internal connection to the quadrature detector.

Internal low pass filter capacitors have been selected to control the bandwidth of the detector. The recovered signal is brought out by the inverting amplifier buffer. An external feedback resistor from the output (Pin 17) to the input of the inverting amplifier (Pin 15) controls the output amplitude; it is combined with another external resistor from the input to the negative supply (Pin 16) to set the output dc level. For a resistor ratio of 1, the DC level at the detector output is 2.0 V_{BE} (see Figure 12). A small capacitor C_{17} across the first resistor (from Pin 17 to 15) can be used to reduce the bandwidth.

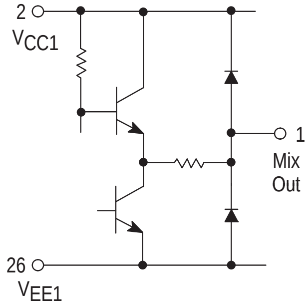
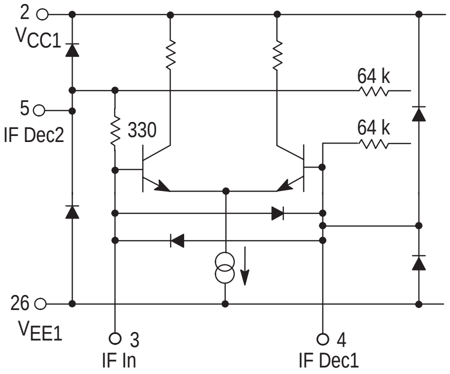
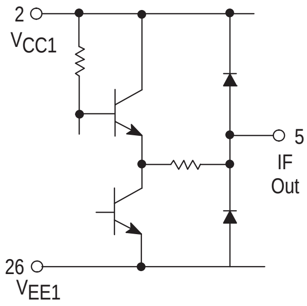
Data Slicer

The data slicer is a comparator that is designed to square up the data signal. Across the data slicer inputs (Pins 18 and 20) are back to back diodes.

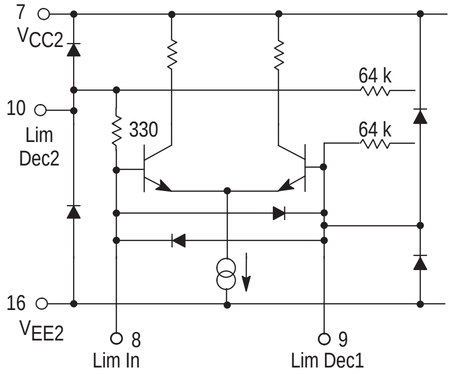
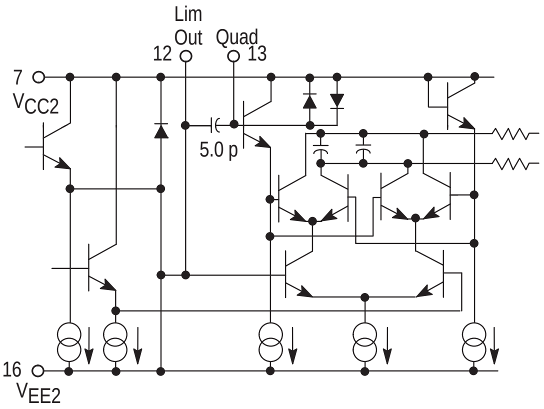
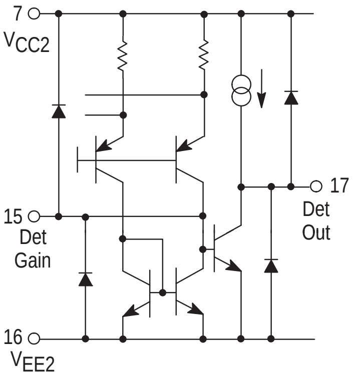
The recovered data signal from the quadrature detector can be DC coupled to the data slicer DS IN1 (Pin 18). In the application circuit shown in Figure 1 it will be centered at 2.0 V_{BE} and allowed to swing ± V_{BE}. A capacitor is placed from DS IN2 (Pin 20) to V_{EE}. The size of this capacitor and the nature of the data signal determine how faithfully the data slicer shapes up the recovered signal. The time constant is short for large peak to peak voltage swings or when there is a change in DC level at the detector output. For small signal or for continuous bits of the same polarity which drift close to the threshold voltage, the time constant is longer.

A unique feature of the data slicer is that the inverting switching stages in the comparator are supplied through the emitter pin of the output transistor (Pin 22 – DS Gnd) to V_{EE} rather than internally to V_{EE}. This is provided in order to reduce switching feedback to the front end. A control pin is provided to shut the data slicer output off (DS “off” – Pin 19). With DS “off” pin at V_{CC} the data slicer output is shut off by shutting down the base drive to the output transistor. When a channel is being monitored to make an RSSI measurement, but not to collect data, the data output may be shut off to save current.

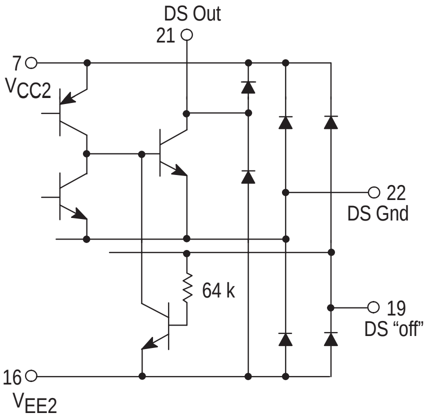
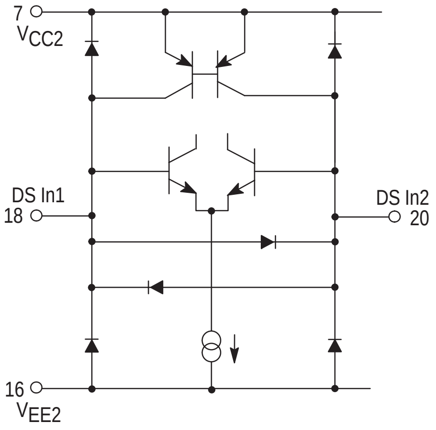
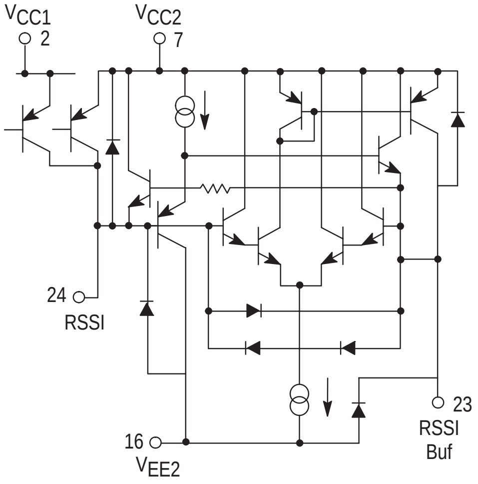
PIN FUNCTION DESCRIPTION

Pin	Symbol	Internal Equivalent Circuit	Description/External Circuit Requirements
1	Mix Out		**Mixer Output** The mixer output impedance is 330 Ω; it matches to 10.7 MHz ceramic filters with 330 Ω input impedance.
2	V_{CC1}		**Supply Voltage (V_{CC1})** This pin is the V_{CC} pin for the Mixer, Local Oscillator, and IF Amplifer. The operating supply voltage range is from 1.8 Vdc to 5.0 Vdc. In the PCB layout, the V_{CC} trace must be kept as wide as possible to minimize inductive reactances along the trace; it is best to have it completely fill around the surface mount components and traces on the circuit side of the PCB.
3	IF In		**IF Input** The input impedance at Pin 3 is 330 Ω. It matches the 330 Ω load impedance of a 10.7 MHz ceramic filter. Thus, no external matching is required.
4	IF Dec1		**IF DEC1 & DEC2** IF decoupling pins. Decoupling capacitors should be placed directly at the pins to enhance stability. Two capacitors are decoupled to the RF ground V_{CC1}; one is placed between DEC1 & DEC2.
5	IF Dec2		
6	IF Out		**IF Output** The output impedance is 330 Ω; it matches the 330 input resistance of a 10.7 MHz ceramic filter.

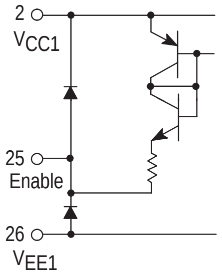
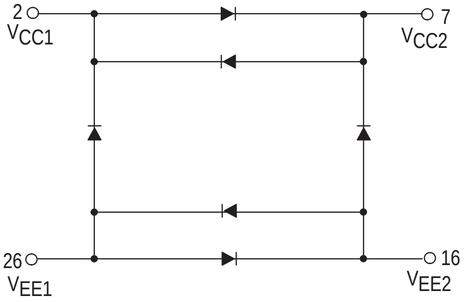
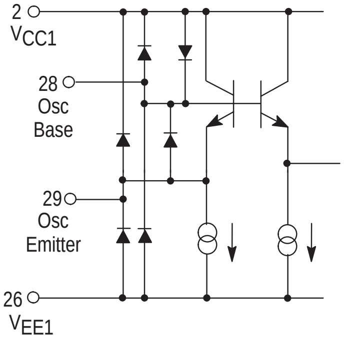
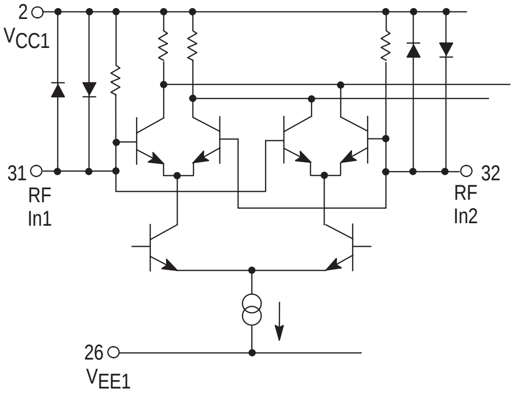
PIN FUNCTION DESCRIPTION (continued)

Pin	Symbol	Internal Equivalent Circuit	Description/External Circuit Requirements
7	V_{CC2}		**Supply Voltage (V_{CC2})** This pin is V_{CC} supply for the Limiter, Quadrature Detector, data slicer and RSSI buffer circuits. In the application PC board this pin is tied to a common V_{CC} trace with V_{CC1}.
8	Lim In		**Limiter Input** The limiter input impedance is 330 Ω.
9	Lim Dec1		**Limiter Decoupling** Decoupling capacitors are placed directly at these pins and to V_{CC} (RF ground). Use the same procedure as in the IF decoupling.
10	Lim Dec2		
11,14, 27 & 28	N/C		**No Connects** There is no internal connection to these pins; however it is recommended that these pins be connected externally to V_{CC} (RF ground).
12	Lim Out		**Limiter Output** The output impedance is low. The limiter drives a quadrature detector circuit with in–phase and quadrature phase signals.
13	Quad		**Quadrature Detector Circuit** The quadrature detector is a doubly balanced four–quadrant multiplier with an internal 5.0 pF capacitor between Pins 12 and 13. An external capacitor may be added to increase the IF signal to Pin 13. The quadrature detector pin is provided to connect the external RLC parallel resonant network which provides the 90 degree phase shift and drives the quadrature detector.
15	Det Gain		**Detector Buffer Amplifier** This is an inverting amplifier. An external feed-back resistor from Pin 17 to 15, (the inverting input) controls the output amplitude; another resistor from Pin 15 to the negative supply (Pin 16) sets the DC output level. A 1:1 resistor ratio sets the output DC level at two V_{BE} with respect to V_{EE}. A small capacitor from Pin 17 to 15 can be used to set the bandwidth.
17	Det Out		
16	V_{EE2}		**Supply Ground (V_{EE2})** In the PCB layout, the ground pins (also applies to Pin 26) should be connected directly to chassis ground. Decoupling capacitors to V_{CC} should be placed directly at the ground pins.

PIN FUNCTION DESCRIPTION (continued)

Pin	Symbol	Internal Equivalent Circuit	Description/External Circuit Requirements
19 21 22	DS “off” DS Out DS Gnd		**Data Slicer Off** The data output may be shut off to save current by placing DS “off” (Pin 19) at V_{CC}. **Data Slicer Output** In the application example a 10 kΩ pull–up resistor is connected to the collector of the output transistor at Pin 21. **Data Slicer Ground** All the inverting switching stages in the comparator are supplied through the emitter pin of the output transistor (Pin 22) to ground rather than internally to V_{EE} in order to reduce switching feedback to the front end.
18 20	DS In1 DS In2		**Data Slicer Inputs** The data slicer has differential inputs with back to back diodes across them. The recovered signal is DC coupled to DS IN1 (Pin 18) at nominally V_{18} with respect to V_{EE}; thus, it will maintain $V_{18} \pm V_{BE}$ at Pin 18. DS IN2 (Pin 20) is AC coupled to V_{EE}. The choice of coupling capacitor is dependent on the nature of the data signal. For small signal or continuous bits of the same polarity, the response time is relatively large. On the other hand, for large peak to peak voltage swings or when the DC level at the detector output changes, the response time is short. See the discussion in the application section for external circuit design details.
23 24	RSSI Buf RSSI		**RSSI Buffer** A unity gain amplifier is used to buffer the voltage at Pin 24 to 23.The output of the unity gain buffer (Pin 23) has an active pull up but no pull down. An external resistor is placed from Pin 23 to V_{EE} to provide the pull down. **RSSI** The RSSI output current creates a voltage drop across an external resistor from Pin 24 to V_{EE}. The maximum RSSI current is 26 μA; thus, the maximum RSSI voltage using a 100 kΩ resistor is approximately 2.6 Vdc. Figure 22 shows the RSSI Output Voltage versus Input Signal Level in the application circuit. The negative slew rate is determined by an external capacitor and resistor to V_{EE} (negative supply). The RSSI rise and fall times for various RF input signal levels and R_{24} values without the capacitor, C_{24} are displayed in Figure 24. This is the maximum response time of the RSSI.

PIN FUNCTION DESCRIPTION (continued)

Pin	Symbol	Internal Equivalent Circuit	Description/External Circuit Requirements
25 26	Enable V_{EE1}		**Enable** The IC regulators are enabled by placing this pin at V_{EE}.
			**V_{CC} and V_{EE} ESD Protection** ESD protection diodes exist between the V_{CC} and V_{EE} pins. It is important to note that significant differences in potential (> 0.5 V_{BE}) between the two V_{CC} pins or between the V_{EE} pins can cause these structures to start to conduct, thus compromising isolation between the supply busses. V_{CC1} & V_{CC2} should be maintained at the same DC potential, as should V_{EE1} & V_{EE2}.
28 29	Osc Base Osc Emitter		**Oscillator Base** This pin is connected to the base lead of the common collector transistor. Since there is no internal bias resistor to the base, V_{CC} is applied through an external choke or coil. **Oscillator Emitter** This pin is connected to the emitter lead; the emitter is connected internally to a current source of about 200 μA. Additional emitter current may be obtained by connecting an external resistor to V_{EE}; $I_E = V_{29}/R_{29}$. Details of circuits using overtone crystal and LC varactor controlled oscillators are discussed in the application section.
31 32	Mix In1 Mix In2		**Mixer Inputs** The parallel equivalent differential input impedance of the mixer is approximately 2.0 kΩ in parallel with 1.0 pF. This equates to a single ended input impedance of 1.0 kΩ in parallel with 2.0 pF. The application circuit utilizes a SAW filter having a differential output that requires a 2.0 kΩ II 2.0 pF load. Therefore, little matching is required between the SAW filter and the mixer inputs. This and alternative circuits are discussed in more detail in the application section.

APPLICATIONS INFORMATION

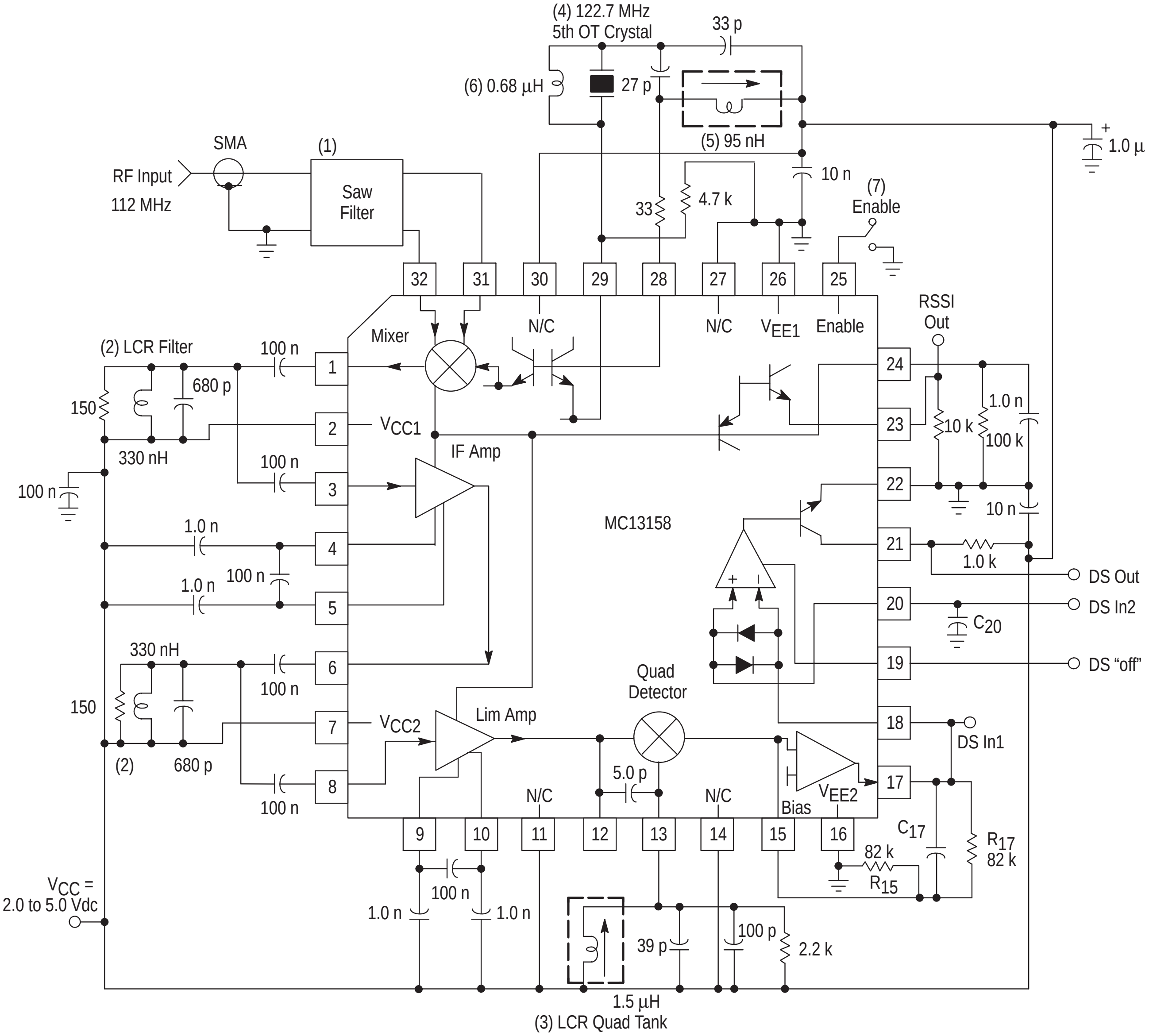
Evaluation PC Board

The evaluation PCB is very versatile and is intended to be used across the entire useful frequency range of this device. The center section of the board provides an area for attaching all SMT components to the circuit side and radial leaded components to the component ground side (see Figures 29 and 30). Additionally, the peripheral area surrounding the RF core provides pads to add supporting and interface circuitry as a particular application dictates. This evaluation board will be discussed and referenced in this section.

Component Selection

The evaluation PC board is designed to accommodate specific components, while also being versatile enough to use components from various manufacturers and coil types. Figures 13 and 14 show the placement for the components specified in the application circuit (Figure 12). The application circuit schematic specifies particular components that were used to achieve the results shown in the typical curves and tables but alternate components should give similar results.

Figure 12. Application Circuit



NOTES:
1. Saw Filter – Siemens part number Y6970M(5 pin SIP plastic package).
2. An LCR filter reduces the broadband noise in the IF; ceramic filters may be used for data rates under 500 kHz. 4.0 dB insertion loss filters optimize the linearity of RSSI.
3. The quadrature tank components are chosen to optimize linearity of the recovered signal while maintaining adequate recovered signal level. 1.5 µH 7.0 mm variable shielded inductor: Toko part # 292SNS–T1373Z. The shunt resistor is approximately equal to Q(2πfL), where Q ~ 18 (3.0 dB BW = 600 kHz).
4. The local oscillator circuit utilizes a 122.7 MHz, 5th overtone, series resonant crystal specified with a frequency tolerance of 25 PPM, ESR of 120 Ω max. The oscillator configuration is an emitter coupled butler.
5. The 95 NH (Nominal) inductor is a 7.0 mm variable shielded inductor: Coilcraft part # 150–04J08S or equivalent.
6. 0.68 µH axial lead chokes (molded inductor): Coilcraft part # 90–11.
7. To enable the IC, Pin 25 is taken to V_{EE}. The external pull down resistor at Pin 29 could be linked to the enable function; otherwise if it is taken to V_{EE} as shown, it will keep the oscillator biased at about 500 µA depending on the V_{CC} level.
8. The other resistors and capacitors are surface mount components.

Figure 13. Circuit Side Component Placement

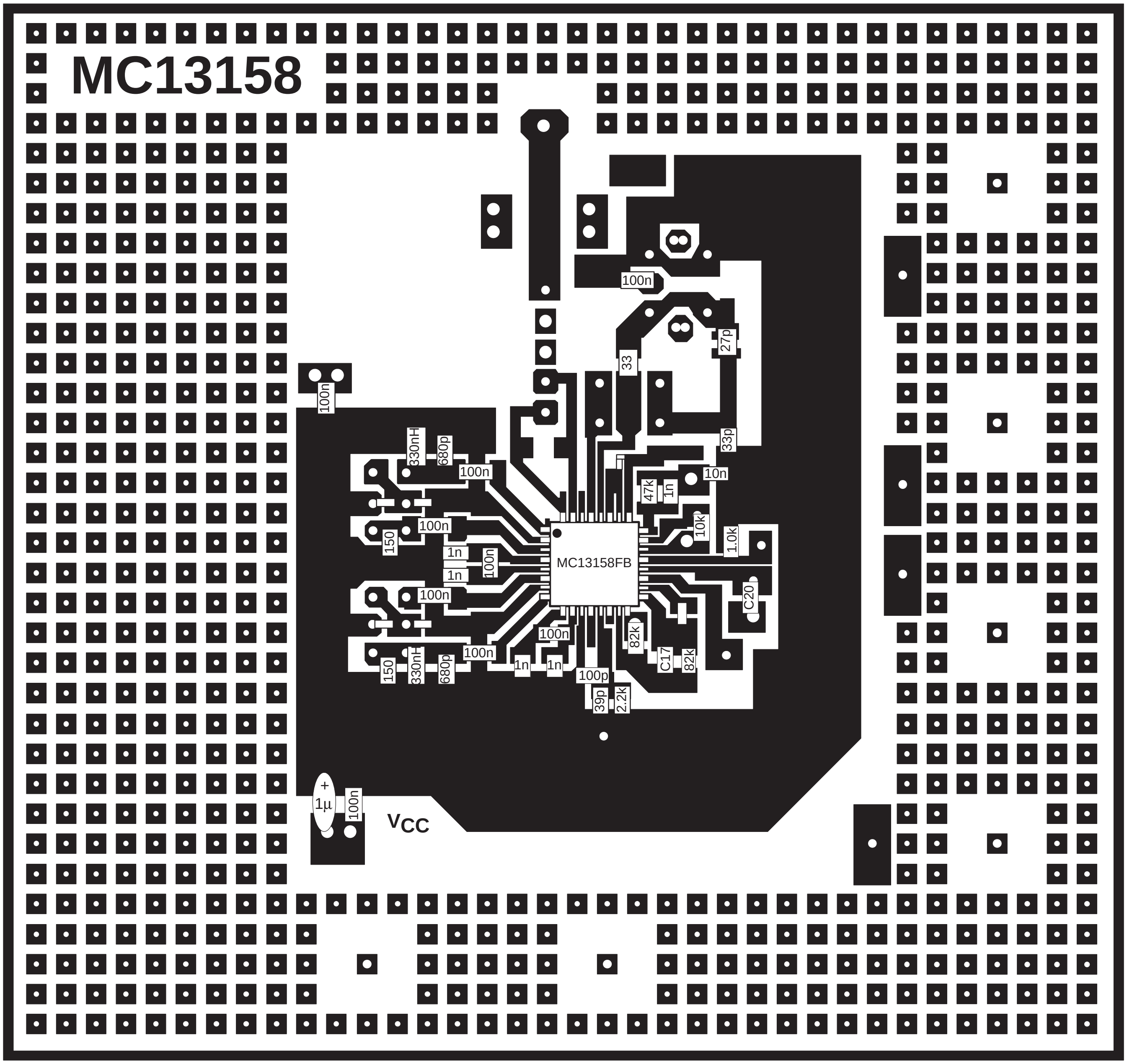
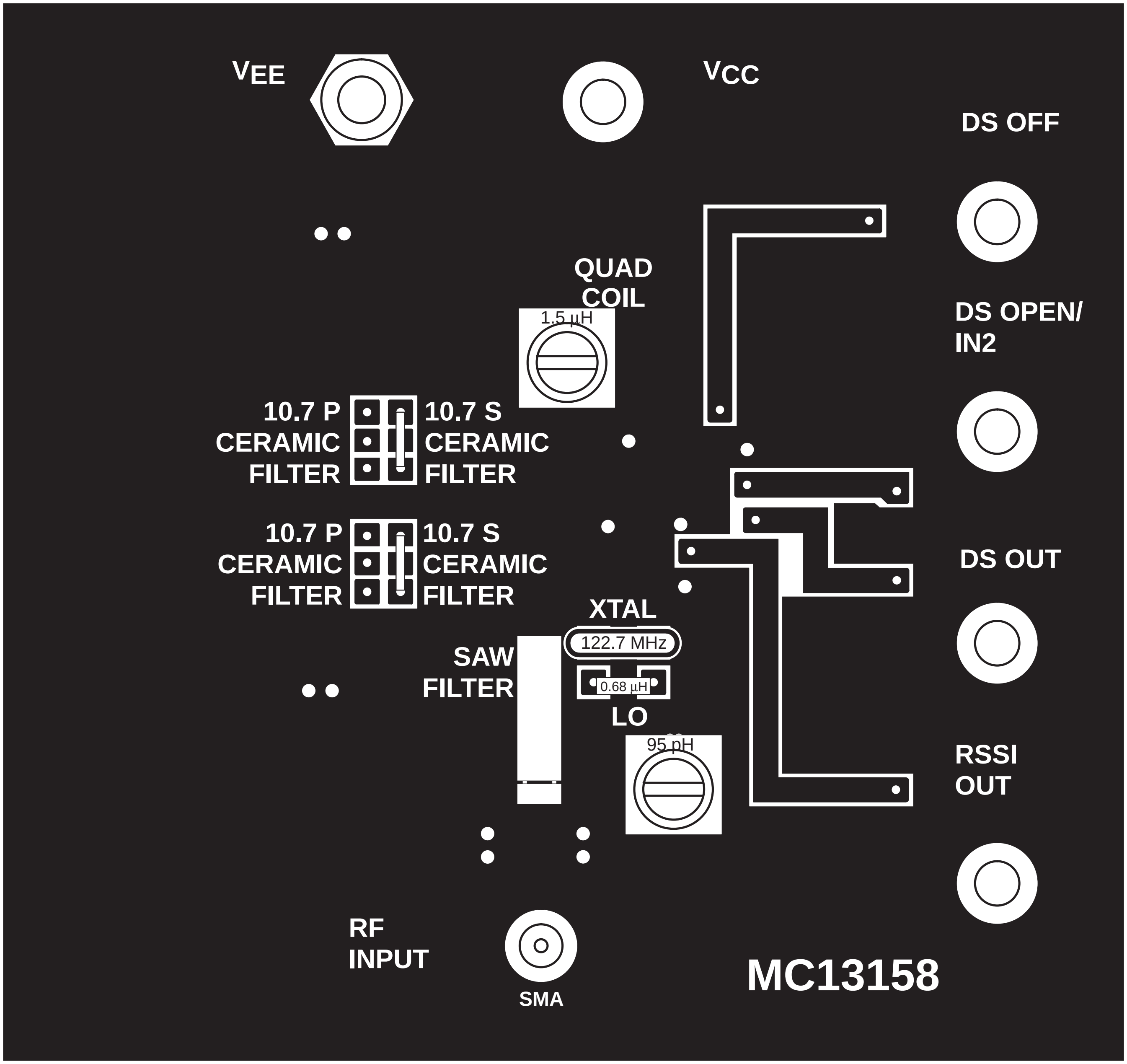


Figure 14. Ground Side Component Placement



Input Matching/Components

It is desirable to use a SAW filter before the mixer to provide additional selectivity and adjacent channel rejection. In a wideband system the primary sensitivity of the receiver backend may be achieved before the last mixer. Bandpass filtering in the limiting IF is costly and difficult to achieve for bandwidths greater than 280 kHz.

The SAW filter should be selected to easily interface with the mixer differential input impedance of approximately 2.0 kΩ in parallel with 1.0 pF. The PC board is dedicated to the Siemens SAW filter (part number Y6970M); the part is designed for DECT at 112 MHz 1st IF frequency. It is designed for a load impedance of 2.0 kΩ in parallel with 2.0 pF; thus, no or little input matching is required between the SAW filter and the mixer.

The Siemens SAW filter has an insertion loss of typically 10 dB and a 3.0 dB bandwidth of 1.0 MHz. The relatively high insertion loss significantly contributes to the system noise and a filter having lower insertion loss would be desirable. In existing low loss SAW filters, the required load impedance is 50 Ω; thus, interface matching between the filter and the mixer will be required. Figure 15 is a table of the single–ended mixer input impedance. A careful noise analysis is necessary to determine the secondary contribution to system noise.

Figure 15. Mixer Input Impedance

(Single–ended)

f (MHz)	Rs (Ω)	Xs (Ω)	Rp (Ω)	Xp (Ω)	Cp (pF)
50	930	–350	1060	–2820	1.1
100	480	–430	865	–966	1.6
150	270	–400	860	–580	1.8
200	170	–320	770	–410	1.9
250	130	–270	690	–330	1.85
300	110	–250	680	–300	1.8
400	71	–190	580	–220	1.8
500	63	–140	370	–170	1.9
600	49	–110	300	–130	2.0

System Noise Considerations

The system block diagram in Figure 16 shows the cascaded noise stages contributing to the system noise; it represents the application circuit in Figure 12 and a low noise preamp using a MRF941 transistor (see Figure 17). The preamp is designed for a conjugately matched input and output at 2.0 Vdc V_{CE} and 3.0 mAdc I_c. S–parameters at 2.0 V, 3.0 mA and 100 MHz are:

S11 = 0.86, –20
S21 = 9.0, 164
S12 = 0.02, 79
S22 = 0.96, –12

The bias network sets V_{CE} at 2.0 V and I_c at 3.0 mA for V_{CC} = 3.0 to 3.5 Vdc. The preamp operates with 18 dB gain and 2.7 dB noise figure.

In the cascaded noise analysis the system noise equation is:

$$F_{system} = F1 + [(F2–1)/G1] + [(F3–1)]/[(G1)(G2)]$$

where:

F1 = the Noise Factor of the Preamp
G1 = the Gain of the Preamp
F2 = the Noise factor of the SAW Filter
G2 = the Gain of the SAW Filter
F3 = the Noise factor of the Mixer

Note: the proceeding terms are defined as linear relationships and are related to the log form for gain and noise figure by the following:

$$F = \log^{-1}[(\text{NF in dB})/10] \quad \text{and similarly}$$

$$G = \log^{-1}[(\text{Gain in dB})/10]$$

The noise figure and gain measured in dB are shown in the system block diagram. The mixer noise figure is typically 14 dB and the SAW filter adds typically 10 dB insertion loss. Addition of a low noise preamp having a 18 dB gain and 2.7 dB noise figure not only improves the system noise figure but it increases the reverse isolation from the local oscillator to the antenna input at the receiver. Calculating in terms of gain and noise factor yields the following:

$F1 = 1.86;\ G1 = 63.1$
$F2 = 10;\ G2 = 0.1$
$F3 = 25.12$

Thus, substituting in the equation for system noise factor:

$F_{system} = 5.82;\ NF_{system} = 7.7\ \text{dB}$

Figure 16. System Block Diagram for Noise Analysis

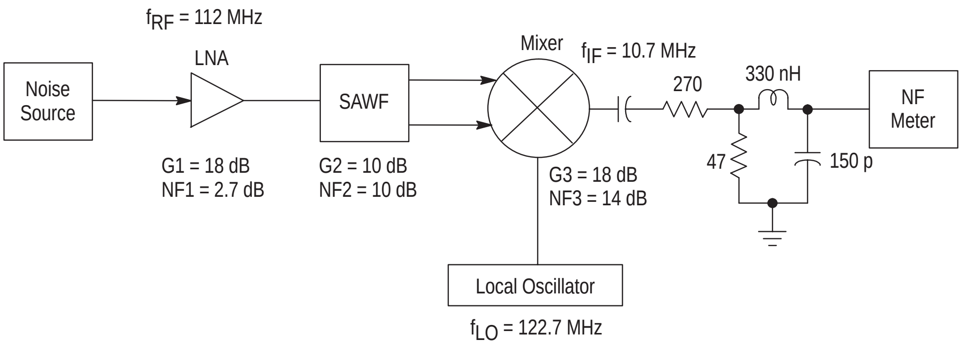
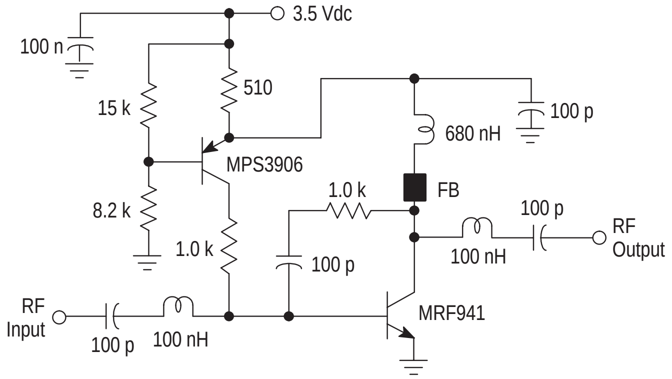


Figure 17. 112 MHz LNA



LOCAL OSCILLATORS

VHF Applications

The on–chip grounded collector transistor may be used for HF and VHF local oscillator with higher order overtone crystals. The local oscillator in the application circuit (Figure 12) shows a 5th overtone oscillator at 122.7 MHz. This circuit uses a Butler overtone oscillator configuration. The amplifier is an emitter follower. The crystal is driven from the emitter and is coupled to the high impedance base through a capacitive tap network. Operation at the desired overtone frequency is ensured by the parallel resonant circuit formed by the variable inductor and the tap capacitors and parasitic capacitances of the on–chip transistor and PC board. The variable inductor specified in the schematic could be replaced with a high tolerance, high Q ceramic or air wound surface mount component if the other components have tight enough tolerances. A variable inductor provides an adjustment for gain and frequency of the resonant tank ensuring lock up and start–up of the crystal oscillator. The overtone crystal is chosen with ESR of typically 80 Ω and 120 Ω maximum; if the resistive loss in the crystal is too high the performance of oscillator may be impacted by lower gain margins.

A series LC network to ground (which is V_{CC}) is comprised of the inductance of the base lead of the on–chip transistor and PC board traces and tap capacitors. Parasitic oscillations often occur in the 200 to 800 MHz range. A small resistor is placed in series with the base (Pin 28) to cancel the negative resistance associated with this undesired mode of oscillation. Since the base input impedance is so large a small resistor in the range of 27 to 68 Ω has very little effect on the desired Butler mode of oscillation.

The crystal parallel capacitance, C_o, provides a feedback path that is low enough in reactance at frequencies of 5th overtones or higher to cause trouble. C_o has little effect near resonance because of the low impedance of the crystal motional arm (R_m–L_m–C_m). As the tunable inductor which forms the resonant tank with the tap capacitors is tuned “off” the crystal resonant frequency it may be difficult to tell if the oscillation is under crystal control. Frequency jumps may occur as the inductor is tuned. In order to eliminate this behavior an inductor, L_o, is placed in parallel with the crystal. L_o is chosen to be resonant with the crystal parallel capacitance, C_o, at the desired operation frequency. The inductor provides a feedback path at frequencies well below resonance; however, the parallel tank network of the tap capacitors and tunable inductor prevent oscillation at these frequencies.

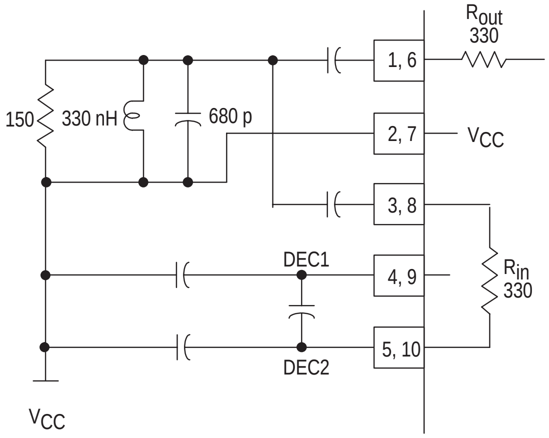
IF Filtering/Matching

In wideband data systems the IF bandpass needed is greater than can be found in low cost ceramic filters operating at 10.7 MHz. It is necessary to bandpass limit with LC networks or series–parallel ceramic filter networks. Murata offers a series–parallel resonator pair (part number

KMFC545) with a 3.0 dB bandwidth of ± 325 kHz and a maximum insertion loss of 5.0 dB. The application PC board is laid out to accommodate this filter pair (a filter pair is used at both locations of the split IF). However, even using a series parallel ceramic filter network yields only a maximum bandpass of 650 kHz. In some applications a wider band IF bandpass is necessary.

A simple LC network yields a bandpass wider than the SAW filter but it does reduce an appreciable amount of wideband IF noise. In the application circuit an LC network is specified using surface mount components. The parallel LC components are placed from the outputs of the mixer and IF amplifier to the V_{CC} trace; internal 330 loads are connected from the mixer and IF amplifier outputs to DEC2 (Pin 5 and 10 respectively).This loads the outputs with the optimal load impedance but creates a low insertion loss filter. An external shunt resistor may be used to widen the bandpass and to acquire the 10 dB composite loss necessary to linearize the RSSI output. The equivalent circuit is shown in Figure 18.

Figure 18. IF LCR Filter



The following equations satisfy the 12 dB loss (1:4 resistive ratio):

$$(\text{Rext})(330)/(\text{Rext} + 330) = \text{Requivalent}$$
$$\text{Requivalent}/(\text{Requivalent} + 330) = 1/4$$

Solve for Requivalent:

$$4(\text{Requivalent}) = \text{Requivalent} + 330$$
$$3(\text{Requivalent}) = 330$$
$$\text{Requivalent} = 110$$

Substitute for Requivalent and solve for Rext:

$$330(\text{Rext}) = 110(\text{Rext}) + (330)(110)$$
$$\text{Rext} = (330)(110)/220$$
$$\text{Rext} = 165\ \Omega$$

The IF is 10.7 MHz although any IF between 10 to 20 MHz could be used. The value of the coil is lowered from that used in the quadrature circuit because the unloaded Q must be maintained in a surface mount component. A standard value component having an unloaded Q = 100 at 10.7 MHz is 330 nH; therefore the capacitor is 669 pF. Standard values have been chosen for these components;

$$\text{Rext} = 150\ \Omega$$
$$C = 680\ \text{pF}$$
$$L = 330\ \text{nH}$$

Computation of the loaded Q of this LCR network is

$$Q = \text{Requivalent}/X_L$$

where: $X_L = 2\pi fL$ and Requivalent is 103 Ω

$$\text{Thus,}\ Q = 4.65$$

The total system loss is

$$20\ \log\ (103/433) = -12.5\ \text{dB}$$

Quadrature Detector

The quadrature detector is coupled to the IF with an internal 5.0 pF capacitor between Pins 12 and 13. For wideband data applications, the drive to the detector can be increased with an additional external capacitor between these pins; thus, the recovered signal level output is increased for a given bandwidth

The wideband performance of the detector is controlled by the loaded Q of the LC tank circuit. The following equation defines the components which set the detector circuit's bandwidth:

$$Q = R_T/X_L \qquad [1]$$

where R_T is the equivalent shunt resistance across the LC Tank

X_L is the reactance of the quadrature inductor at the IF frequency ($X_L = 2\pi fL$).

The inductor and capacitor are chosen to form a resonant LC tank with the PCB and parasitic device capacitance at the desired IF center frequency as predicted by

$$f_c = [2\pi\ (LC_p)^{1/2}]^{-1} \qquad [2]$$

where L is the parallel tank inductor C_p is the equivalent parallel capacitance of the parallel resonant tank circuit.

The following is a design example for a wideband detector at 10.7 MHz and a loaded Q of 18. The loaded Q of the quadrature detector is chosen somewhat less than the Q of the IF bandpass. For an IF frequency of 10.7 MHz and an IF bandpass of 600 kHz, the IF bandpass Q is approximately 6.4.

Example:

Let the external Cext = 139 pF. (The minimum value here should be much greater than the internal device and PCB parasitic capacitance, Cint ≈ 3.0 pF). Thus, C_p = Cint + Cext = 142 pF.

Rewrite equation (2) and solve for L:

$$L = (0.159)^2/(C_p fc^2)$$

$L = 1.56\ \mu H$; Thus, a standard value is choosen:

$$L = 1.56\ \mu H \text{ (tunable shielded inductor)}$$

The value of the total damping resistor to obtain the required loaded Q of 18 can be calculated by rearranging equation (1):

$$R_T = Q(2\pi fL)$$
$$R_T = 18(2\pi)(10.7)(1.5) = 1815\ \Omega$$

The internal resistance, Rint at the quadrature tank Pin 13 is approximately 13 kΩ and is considered in determining the external resistance, Rext which is calculated from

$$\text{Rext} = ((R_T)(\text{Rint}))/(\text{Rint} - R_T)$$

$\text{Rext} = 2110$; Thus, choose the standard value:

$$\text{Rext} = 2.2\ \text{k}\Omega$$

It is important to set the DC level of the detector output at Pin 17 to center the peak to peak swing of the recovered signal. In the equivalent internal circuit shown in the Pin Function Description, the reference voltage at the positive terminal of the inverting op amp buffer amplifier is set at 1.0 V_{BE}. The detector DC level, V_{17} is determined by the following equation:

$$V_{17} = [((R_{15}/R_{17}) + 1)/(R_{15}/R_{17})]\ V_{BE}$$

Thus, for a 1:1 ratio of R_{15}/R_{17}, V_{17} = 2.0 V_{BE} = 1.4 Vdc. Similarly for a 2:1, V_{17} = 1.5 V_{BE} = 1.05 Vdc; and for 3:1, V_{17} = 1.33 V_{BE} = 0.93 Vdc.

Figure 19 shows the detector “S–Curves”, in which the resistor ratio is varied while maintaining a constant gain (R_{17} is held at 62 k). R_{15} is 62 k for a 1:1 ratio; while R_{15} = 120 k and 180 k to produce the 2:1 and 3:1 ratios. The IF signal into the detector is swept ± 500 kHz about the 10.7 MHz IF center frequency. The resulting curve show how the resistor ratio and the supply voltage effects the symmetry of the “S–curve” (Figure 21 Test Setup). For the 3:1 and 2:1 ratio, symmetry is maintained with V_S from 2.0 to 5.0 Vdc; however, for the 1:1 ratio, symmetry is lost at 2.0 Vdc.

Figure 19. Detector Output Voltage versus Frequency Deviation

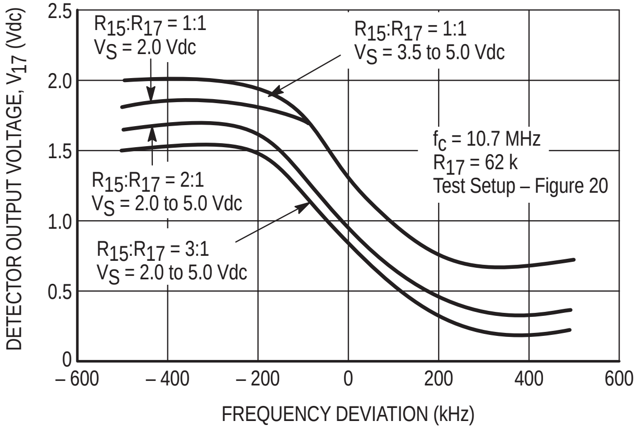
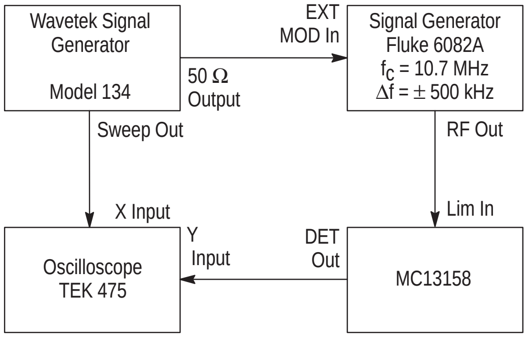


Figure 20. Demodulator “S–Curve” Test Setup



Data Slicer Circuit

C_{20} at the input of the data slicer is chosen to maintain a time constant long enough to hold the charge on the capacitor for the longest strings of bits at the same polarity. For a data rate at 576 kHz a bit stream of 15 bits at the same polarity would equate to an apparent data rate of approximately 77 kbps or 38 kHz. The time constant would be approximately 26 µs. The following expression equates the time constant, t, to the external components:

$$t = 2\pi\ (R_{18})(C_{20})$$

Solve for C_{20}:

$$C_{20} = t/2\pi\ (R_{18})$$

where the effective resistance R_{18} is a complex function of the demodulator feedback resistance and the data slicer input circuit. In the data input network the back to back diodes form a charge and discharge path for the capacitor at Pin 20; however, the diodes create a non–linear response. This resistance is loaded by the ß, beta of the detector output transistor; beta =100 is a typical value (see Figure 21). Thus, the apparent value of the resistance at Pin 18 (DS IN1) is approximately equal to:

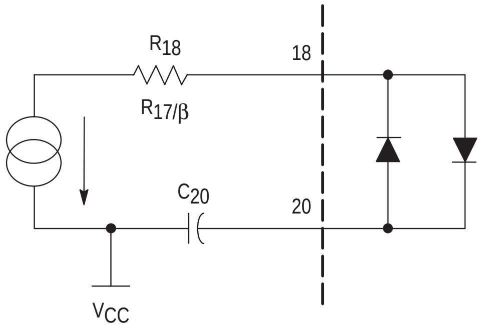
$$R_{18} \frown R_{17}/100$$

where R_{17} is 82 kΩ, the feedback resistor from Pin 17 to 15. Therefore, substituting for R_{18} and solving for C_{20}:

$$C_{20} = 15.9\ (t)/R_{17} = 5.04\ \text{nF}$$

The closest standard value is 4.7 nF.

Figure 21. Data Slicer Equivalent Input Circuit



SYSTEM PERFORMANCE DATA

RSSI

In Figure 22, the RSSI versus RF Input Level shows the linear response of RSSI over a 65 dB range but it has extended capability over 80 dB from –80 dBm to +10 dBm. The RSSI is measured in the application circuit (Figure 12) in which a SAW filter is used before the mixer; thus, the overall sensitivity is compromised for the sake of selectivity. The curves are shown for three filters having different bandwidths:

1) LCR Filter with 2.3 MHz 3.0 dB BW (Circuit and Component Placement is shown in Figure 12)
2) Series–Parallel Ceramic Filter with 650 kHz 3.0 dB BW (Murata Part # KMFC–545)
3) Ceramic Filter with 280 kHz 3.0 dB BW.

Figure 22. RSSI Output Voltage versus Signal Input Level

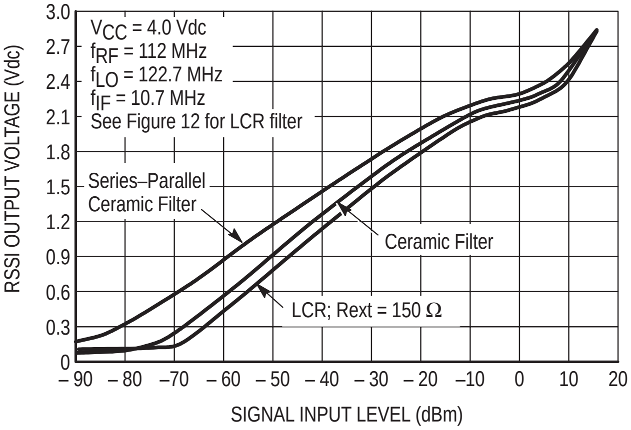
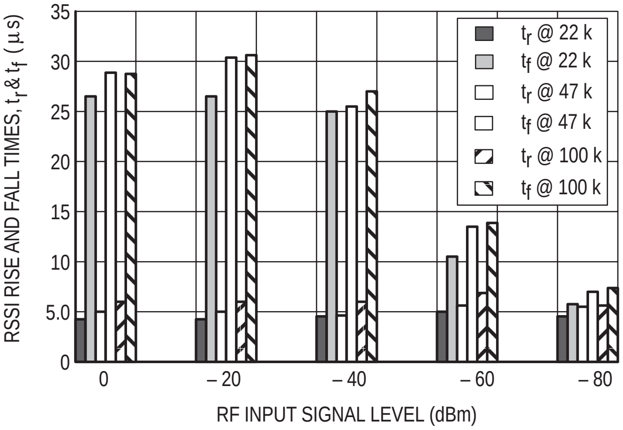


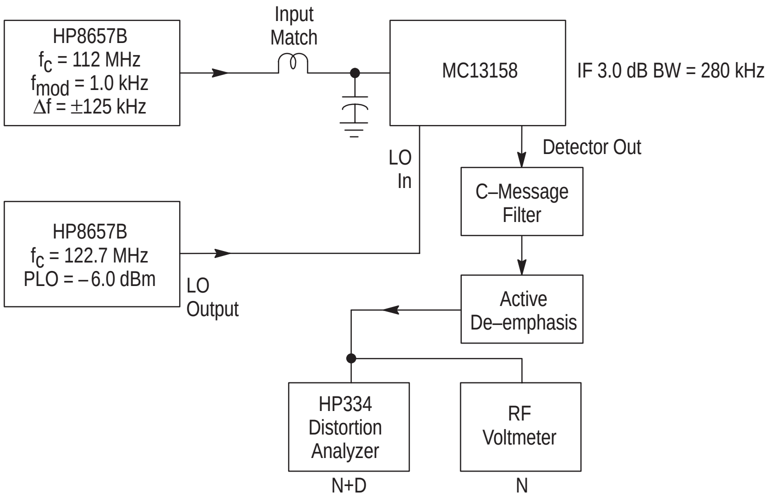
Figure 23. RSSI Output Rise and Fall Times versus RF Input Signal Level



SINAD Performance

Figure 24 shows a test setup for a narrowband demodulator output response in which a C–message filter and an active de–emphasis filter is used following the demodulator. The input is matched using a 1:4 impedance transformer. The SINAD performance is shown in Figure 25 with no preamp and in Figure 26 with a preamp (Preamp – Figure 16). The 12 dB SINAD sensitivity is –101 dBm with no preamp and –113 dBm with the preamp.

Figure 24. Test Setup for Narrowband SINAD



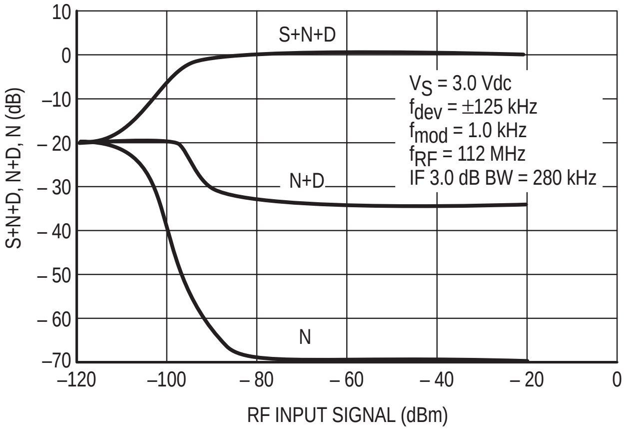


Figure 25. S+N+D, N+D, N versus Input Signal Level (without preamp)

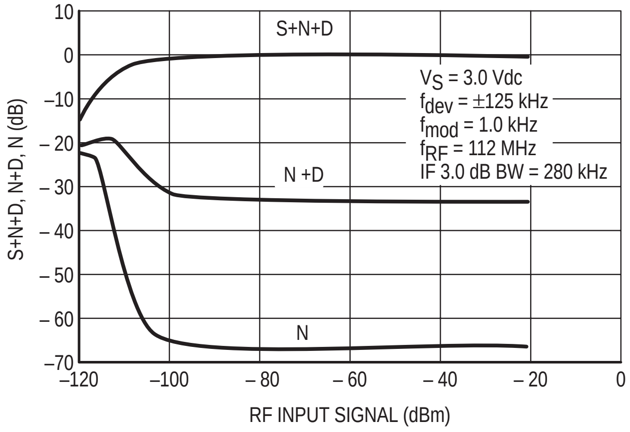


Figure 26. S+N+D, N+D, N versus Input Signal Level (with preamp)

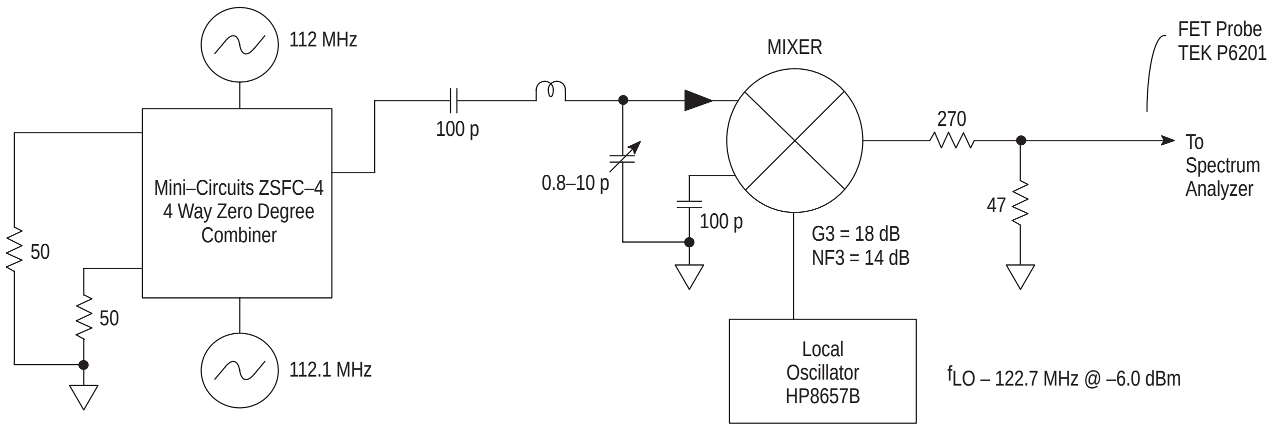


Figure 27. Input IP3, 1.0 dB Compression Pt. Test Setup

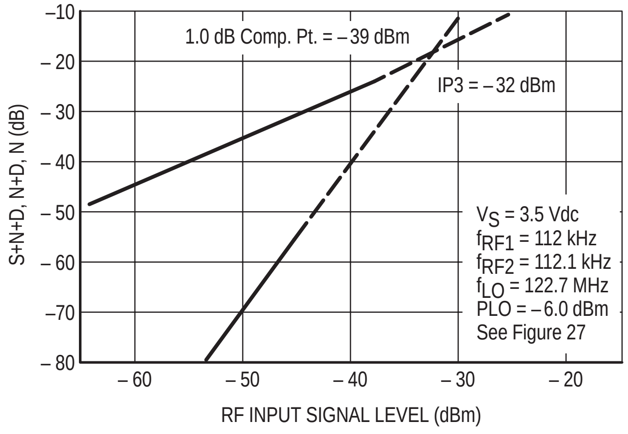


Figure 28. –1.0 dB Compression Pt. and Input Third Order Intercept

Figure 29. Circuit Side View

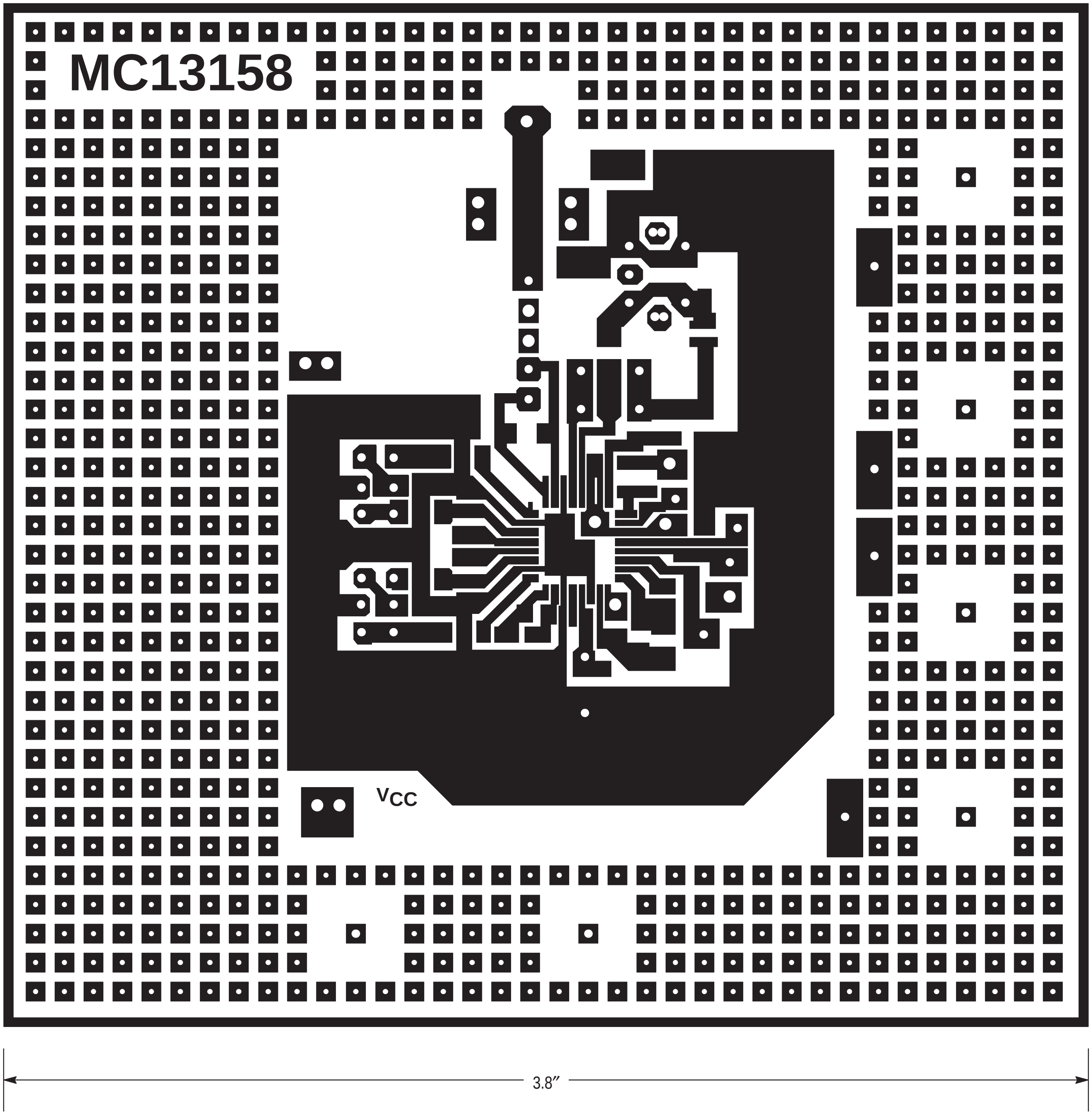
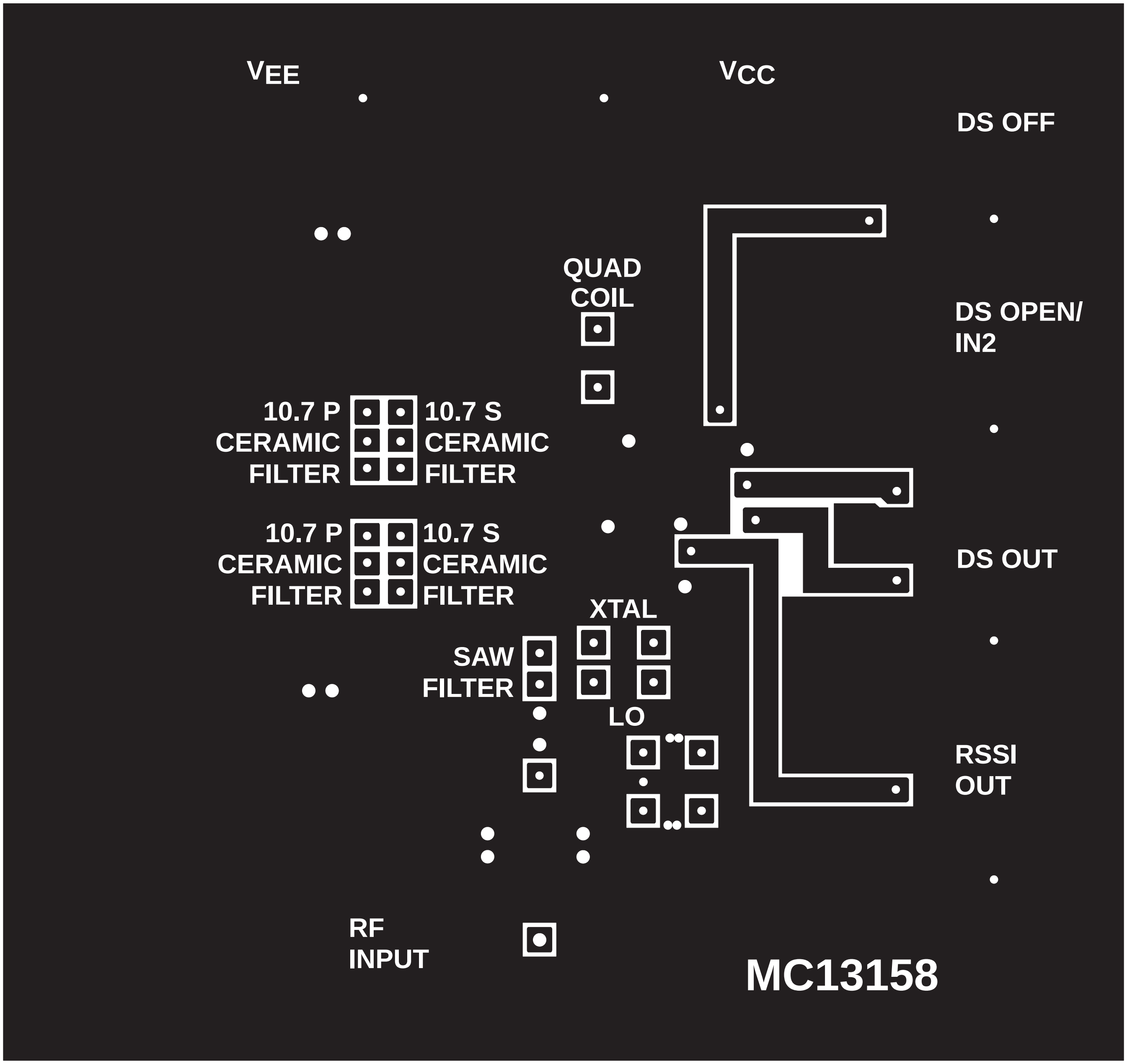


Figure 30. Ground Side View



MOTOROLA

MC13159

WIDEBAND FM IF SUBSYSTEM FOR PHS AND DIGITAL APPLICATIONS

SEMICONDUCTOR TECHNICAL DATA

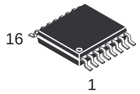
Advance Information

Wideband FM IF Amp

The MC13159 is a wideband FM IF subsystem that is designed for high performance data and digital applications. Excellent high frequency performance is achieved, with low cost, through the use of Motorola’s RF bipolar process. The MC13159 includes a mixer, Local Oscillator Buffer amplifier, IF amplifier, Limiter amplifier and RSSI functions. The mixer is useful for 240 MHz input used in a single–ended/balanced differential configuration. The IF and Limiter amplifier are separated for using the external filter in series or connecting directly by an external capacitor. RSSI output is derived by summing the output of both IF and Limiter sections. An enable control is provided to power down the IC for power management in battery operated applications.

Applications are suitable for PHS, DECT, PDC, GSM, PCS, wideband wireless data links and other battery operated radio systems.

- Designed for PHS Applications
- 2.7 to 5.5 V Operating Voltage
- Low Drain Current: 5.5 mA (Typ)
- Wide Input Dynamic Range of Mixer (Maximum –16 dBm Input)
- Enable Function for Power Down Mode
- Over 80 dB of RSSI Dynamic Range (AC Coupling Between IF Amplifier and Limiter Amplifier)
- Low External Component Count

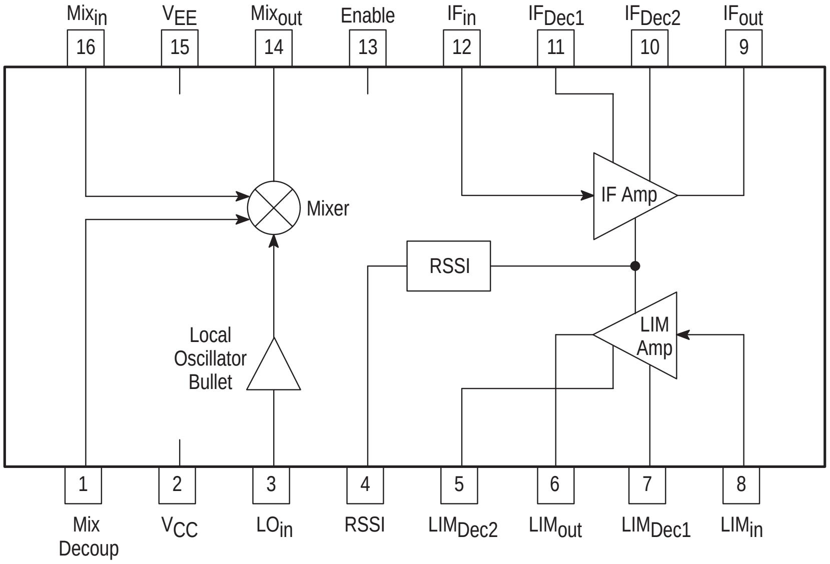


DTB SUFFIX
PLASTIC PACKAGE
CASE 948F
(TSSOP–16L)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC13159DTB	T_A = –30° to +85°C	TSSOP–16L

Simplified Application



This device contains 164 active transistors.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	$V_{S(max)}$	6.0	Vdc
Junction Temperature	T_{Jmax}	150	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

NOTE: ESD data available upon request.

RECOMMENDED OPERATING CONDITIONS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_S	2.7 to 5.5	Vdc
Input Frequency	f_{in}	10 to 600	MHz
Ambient Temperature Range	T_A	–30 to +85	°C
Input Signal Level at Local Input	V_{in}	–10	dBm

DC ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_S = 3.0 V; No Input Signal)

Characteristics	Conditions	Symbol	Min	Typ	Max	Unit
Total Drain Current 1	Active Mode	I_{CC1}	4.5	5.5	7.5	mA
Total Drain Current 2	Disable Mode	I_{CC2}	–	0.1	10	µA

AC ELECTRICAL CHARACTERISTICS

Characteristics	Conditions	Symbol	Min	Typ	Max	Unit
MIXER (T_A = 25°C; V_S = 3.0; f_{RF} = 240 MHz, f_{LO} = 229.3 MHz)						
Mixer Conversion Gain	50 Ω Termination Input Matched	–	11 –	14 21	17 –	dB
Noise Figure	Input Matched	NF	–	14	–	dB
Mixer Input Impedance	Single–Ended	Rp Cp	– –	400 4.0	– –	Ω pF
Mixer Output Impendance	–	–	–	330	–	Ω
1.0 dB Gain Compression	@Mix$_{in}$	Vicp	–	–16	–	dBm
3rd Order Input Intercept	50 Ω Termination	IIP3	–	–8.0	–	dBm
IF AMPLIFIER SECTION (T_A = 25°C; V_S = 3.0 V; f_{IF} = 10.7 MHz)						
IF Gain	f = 10.7 MHz	–	32	36	45	dB
Input Impedance	–	–	–	330	–	Ω
Output Impedance	–	–	–	330	–	Ω
LIMITING AMPLIFIER SECTION (T_A = 25°C; V_S = 3.0 V; f_{IF} = 10.7 MHz)						
Limiter Gain	f = 10.7 MHz	–	–	70	–	dB
Input Impedance	–	–	–	330	–	Ω
Output Swing	–	–	400	500	600	mVpp
Output Rise Time	–	–	–	10	–	ns
Output Fall Time	–	–	–	20	–	ns
RSSI SECTION (T_A= 25°C; V_S = 3.0 V; f_{IF} = 10.7 MHz)						
RSSI Slope	–	–	10	14	18	mV/dB
RSSI Output DC Voltage 1	No Input Signal	–	0.8	0.9	1.0	V
RSSI Output DC Voltage 2	V_{IF} = –85 dBm	–	0.82	0.95	1.02	V
RSSI Output DC Voltage 3	V_{IF} = –80 dBm	–	0.85	1.0	1.15	V
RSSI Output DC Voltage 4	V_{IF} = –40 dBm	–	1.4	1.5	1.6	V
RSSI Output DC Voltage 5	V_{in} = 0 dBm	–	1.95	2.1	2.25	V

Figure 1. Test Circuit

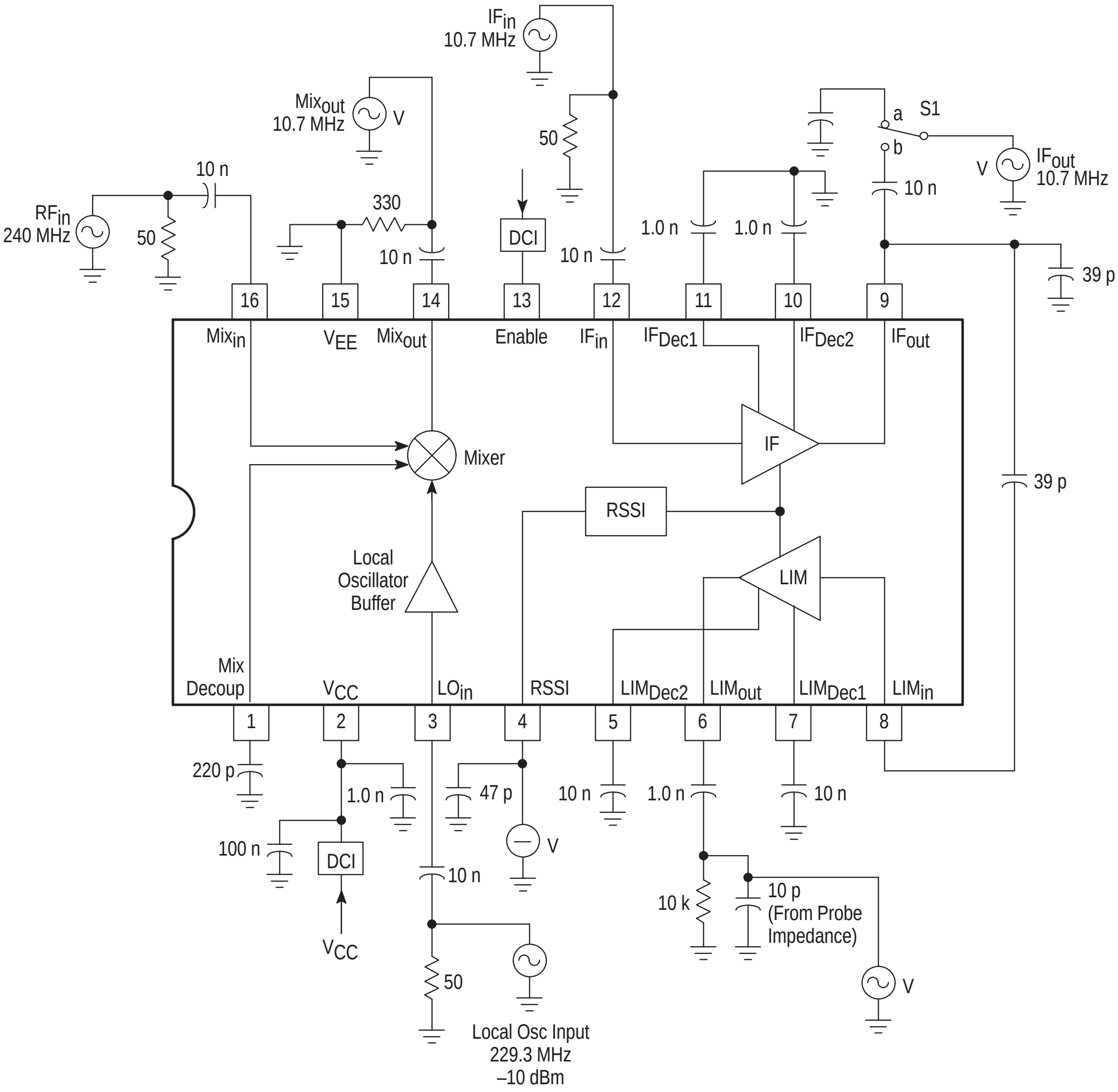
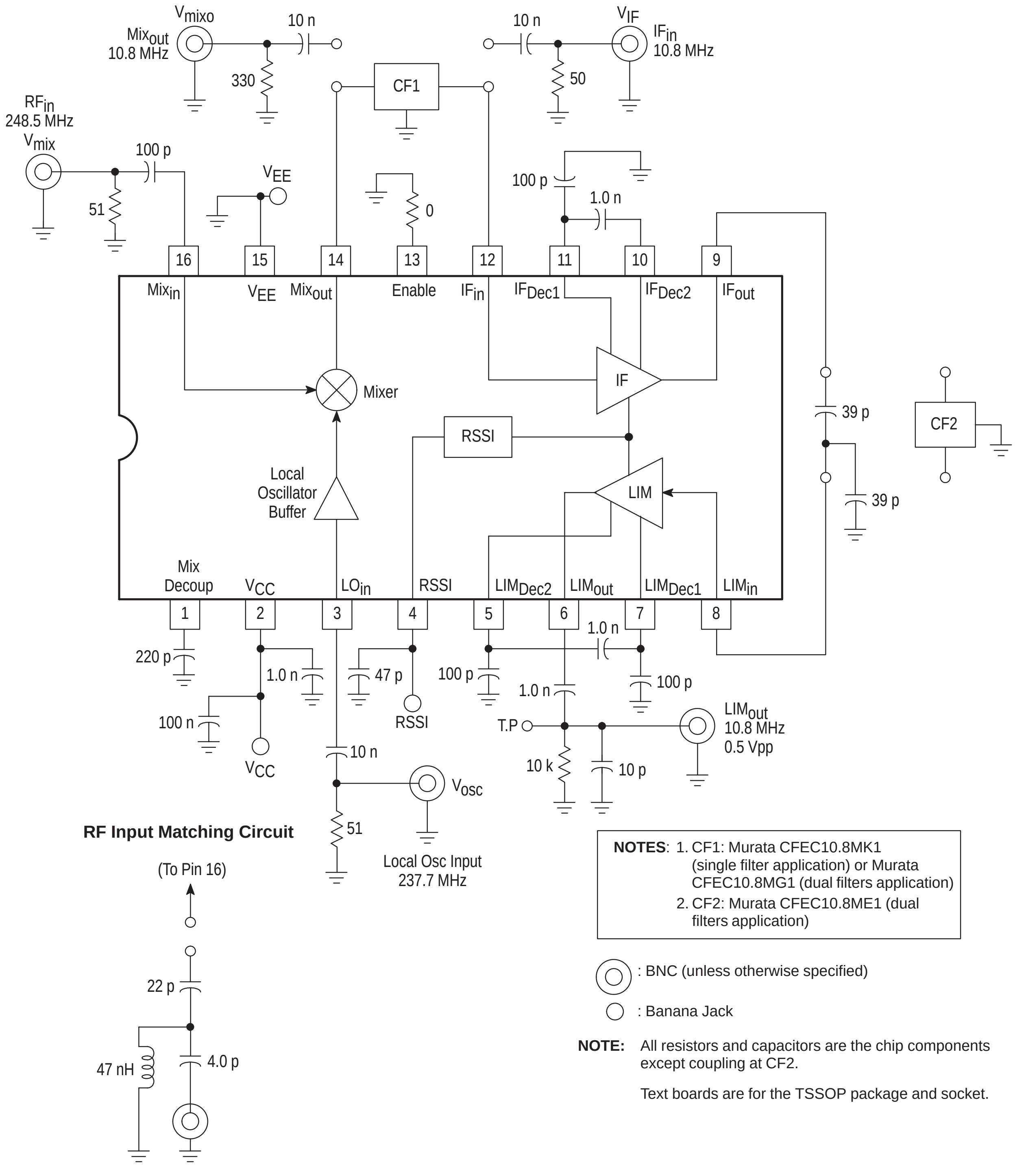


Figure 2. Test Circuit for Evaluation



NOTES: 1. CF1: Murata CFEC10.8MK1 (single filter application) or Murata CFEC10.8MG1 (dual filters application)
2. CF2: Murata CFEC10.8ME1 (dual filters application)

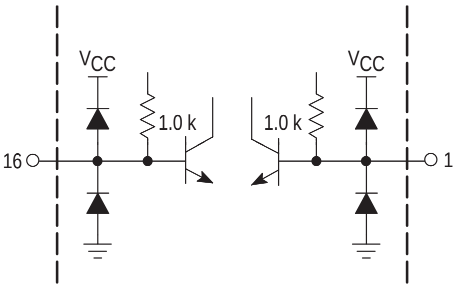
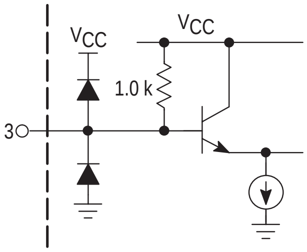
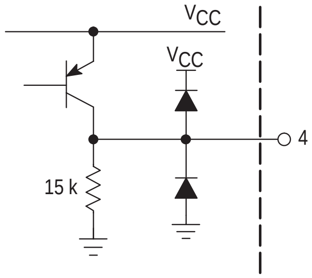
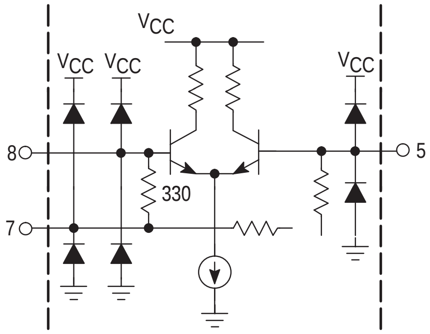
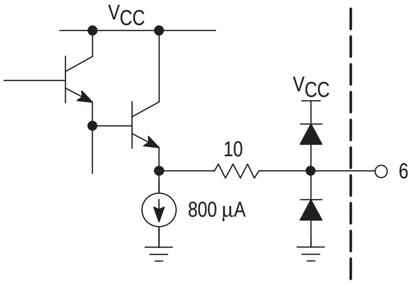
◎ : BNC (unless otherwise specified)

○ : Banana Jack

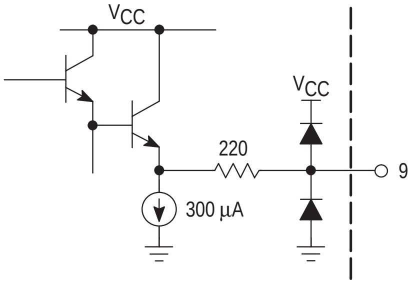
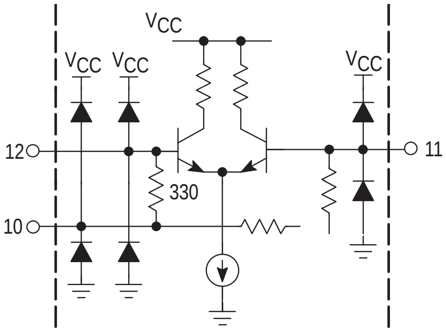
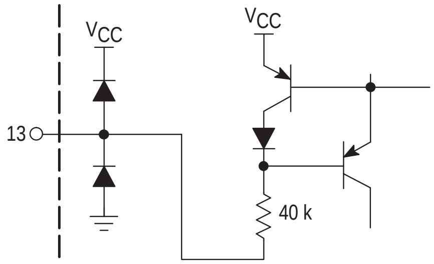
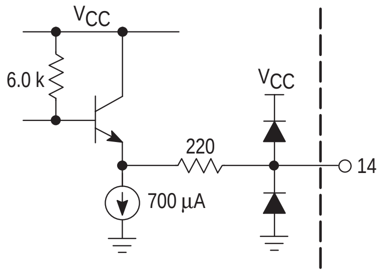
NOTE: All resistors and capacitors are the chip components except coupling at CF2.

Text boards are for the TSSOP package and socket.

PIN FUNCTION DESCRIPTION

Pin	Symbol	Internal Equivalent Circuit	Description
1	Mix Decoup		**Mixer Decoupling** Mixer decoupling pin. 220 pF is decoupled to the RF ground. This pin also can be used for differential input with Mix_{in}.
16	Mix_{in}		**Mixer Input** Input impedance is about 400 Ω at 240 MHz. Single–ended matching section at 240 MHz is referenced at application circuit.
2	V_{CC}		**Supply Voltage** Supply voltage range range is from 2.7 Vdc to 5.5 Vdc. 1.0 nF of decoupling capacitor is placed directly at this pin to reduce the floor noise.
3	LO_{in}		**Local Oscillator Input** Connected to external local oscillator. Input impedance is about 900 Ω at 230 MHz.
4	RSSI		**RSSI** The RSSI current creates a voltage drop across an internal 15 kΩ resistor.
5 7	LIM_{Dec2} LIM_{Dec1}		**Limiter Decoupling** Limiter decoupling pins. Decoupling capacitors are connected to the RF ground, and one is placed between Dec1 and Dec2.
8	LIM_{in}		**Limiter Input** The input impedance is 330 Ω; it matches the 330 input resistance of a 10.7/10.8 MHz ceramic filter.
6	LIM_{out}		**Limiter Output** The output level is about 0.5 Vpp.

PIN FUNCTION DESCRIPTION (continued)

Pin	Symbol	Internal Equivalent Circuit	Description
9	IF_{out}		**IF Output** The output impedance is 330 Ω; it matches the 330 input resistance of a 10.7/10.8 MHz ceramic filter.
10 11	IF_{Dec2} IF_{Dec1}		**IF Decoupling** IF decoupling pins. Decoupling capacitor is connected from Dec1 to the RF ground, and one is placed between Dec1 and Dec2.
12	IF_{in}		**IF Input** The input impedance is 330 Ω; it matches the 330 input resistance of a 10.7/10.8 MHz ceramic filter.
13	Enable		**Enable** The IC regulators are enabled by placing this pin at V_{EE}.
14	Mix_{out}		**Mixer Output** The mixer output impedance is 330 Ω; it matches the 330 input resistance of a 10.7/10.8 MHz ceramic filter.
15	V_{EE}		**Supply Ground**

MOTOROLA

MC13173

Infrared Integrated Transceiver IC

INFRARED TRANSCEIVER

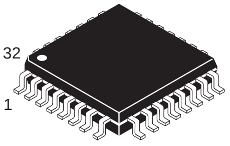
SEMICONDUCTOR TECHNICAL DATA

The MC13173 is a low power infrared integrated system (IRIS). It is a unique blend of a split IF wideband FM receiver and a specialized infrared LED transmitter. This device was designed to provide communications between portable computers via a half duplex infrared link at data rates up to 200 kbps.

The receiver includes a mixer, IF amplifier and limiter and data slicer. The IF amplifier is split to accommodate two low cost cascaded filters. The RSSI output is derived by summing the output of both IF sections.

The transmitter section includes a frequency synthesizer, FSK modulator, harmonic low pass filter and an IR LED driver.

- Transmitter Operates in Two Modes:
  - On/Off Pulsing for Remote Control
  - FSK Modulation at 1.4 MHz for Data Communications
- Over 70 dB of RSSI Range
- Split IF for Improved Filtering and Extended RSSI Range
- Digitally controlled Via a Six Line Interface Bus
- Individual Circuit Blocks Can Be Powered Down When Not In Use for Power Conservation

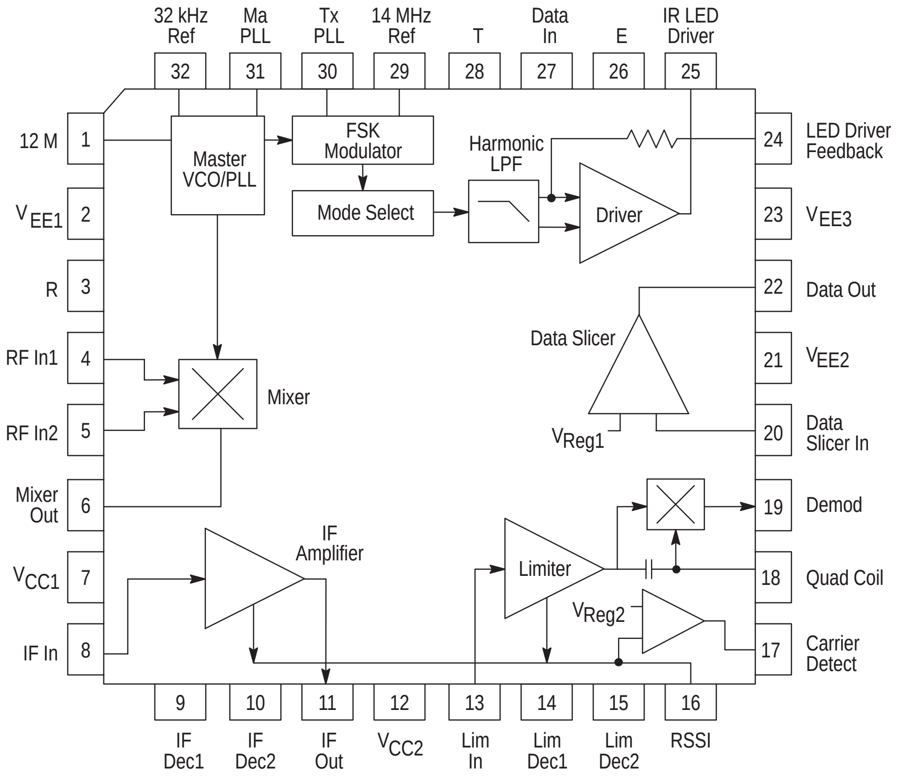


FTB SUFFIX
PLASTIC PACKAGE
CASE 873
(Thin QFP)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC13173FTB	T_A = – 40° to +85°C	TQFP–32

Simplified Block Diagram



This device contains 914 active transistors.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	$V_{CC} – V_{EE}$	6.0	Vdc
Junction Temperature	T_J	150	°C
Storage Temperature	T_{stg}	– 55 to +150	°C

NOTE: Devices should not be operated at or outside these values. The “Recommended Operating Conditions” table provides for actual device operation.

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Value	Unit
Power Supply Voltage	$V_{CC} – V_{EE}$	2.7 to 5.5	Vdc
Ambient Temperature Range	T_A	– 40 to +85	°C

DC ELECTRICAL CHARACTERISTICS (T_A = +25°C, V_{CC} = 3.3 Vdc, f_{REF} = 32.768 kHz. Measured using test circuit in Figure 1, unless otherwise noted.)

Characteristic	Control Pin Logic State			Pin	Symbol	Min	Typ	Max	Unit
	T	R	E						
Supply Current (See Table 2)				7, 12	I_{CC}				
Receive Mode	0	1	0			–	6.5	9.0	mA
Communications Mode	1	0	0			–	4.75	8.0	
A/V Mode	1	0	1			–	1.5	–	
Standby Mode	0	0	0			–	<10	–	nA
Master PLL Charge Current				31	I_{MA}	–	±25	–	µA
DATA SLICER									
Data Slicer Threshold Voltage				20	V_{TH1}	0.85	1.1	1.4	Vdc
Maximum Pull–Down Current				22	I_{DS}	1.0	1.8	–	mA
CARRIER DETECT									
Carrier Detect Threshold Voltage				16	V_{TH2}	1.0	1.15	1.3	Vdc
Maximum Pull–Down Current				17	I_{CD}	1.1	3.0	–	mA
TRANSMITTER									
Maximum Pull–Up Current				25	I_{OH}	5.8	7.0	–	mA
Maximum Pull–Down Current				25	I_{OL}	–	150	700	µA
DC Output Voltage				24	V_O	–	200	–	mV
Transmit PLL Charge Current				30	I_{TX}	–	±25	–	µA

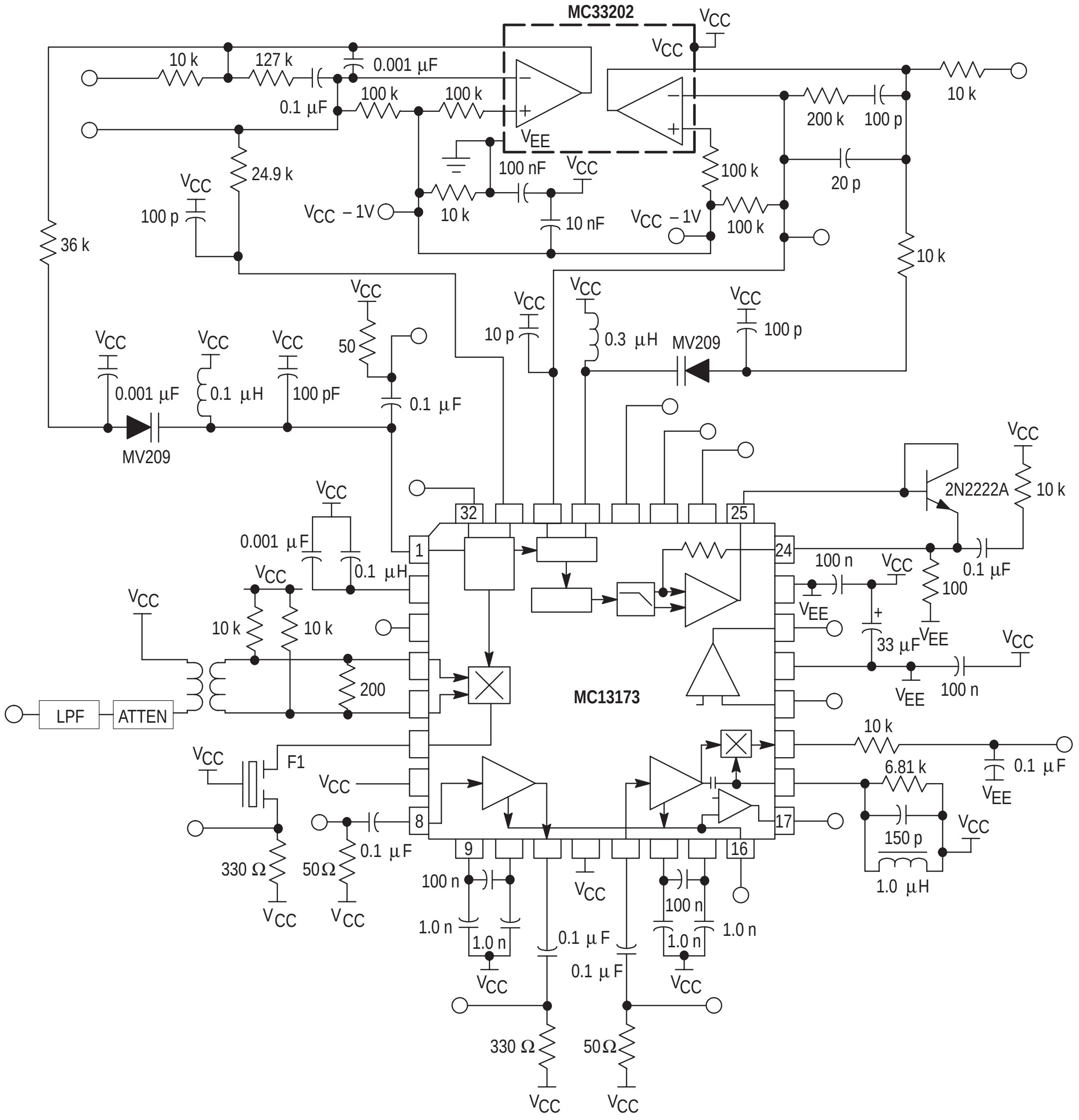
AC ELECTRICAL CHARACTERISTICS (T_A = +25°C, V_{CC} = 3.3 Vdc, f_{REF} = 32.768 kHz. Measured using test circuit in Figure 1, unless otherwise noted.)

Characteristic	Pin	Symbol	Min	Typ	Max	Unit
TRANSMITTER						
Upper Sideband Frequency (Mark)	24	f_{HI}	–	1.427	–	MHz
Lower Sideband Frequency (Space)	24	f_{LO}	–	1.317	–	MHz
Upper and Lower Sideband Amplitude	24	V_{SB}	40	54	70	mVrms
RECEIVER						
Receiver Sensitivity – 12 dB SINAD	4, 19	V_{SIN}	–	5.0	–	µV
MIXER						
Mixer Conversion Gain	4, 5, 6	$AV_{(Mix)}$	–	23.5	–	dB
Mixer Output Impedance	6	Z_O	–	330	–	Ω

AC ELECTRICAL CHARACTERISTICS (continued) (T_A = +25°C, V_{CC} = 3.3 Vdc, f_{REF} = 32.768 kHz. Measured using test circuit in Figure 1, unless otherwise noted.)

Characteristic	Pin	Symbol	Min	Typ	Max	Unit
IF AMPLIFIER						
IF Amplifier Gain	8, 11	–	–	54	–	dB
IF Amplifier RSSI Slope	16	–	–	275	–	nA/dB
Input Impedance	8	Z_{IN}	–	330	–	Ω
Output Impedance	11	Z_O	–	330	–	Ω
RSSI Current Range	16	–	–	20	–	µA
RSSI Dynamic Range	16	–	–	70	–	dB
LIMITING AMPLIFIER						
Input Impedance	13	Z_{IN}	–	330	–	Ω
Limiter RSSI Slope	16	–	–	360	–	nA/dB
RSSI Current Range	16	–	–	20	–	µA
RSSI Dynamic Range	16	–	–	58	–	dB

Figure 1. Test Circuit



CIRCUIT DESCRIPTION

General

The MC13173 infrared transceiver integrates a split IF wideband FM receiver and an IR LED transmitter into a single IC. The transmitter is comprised of an FSK modulator, harmonic low pass filter, and IR LED driver. The receiver consists of a mixer, IF amplifier and limiting IF, detector, and data slicer. It includes RSSI and carrier detect functions.

The transmitter is capable of two modes of operation. It was primarily designed for use in the Communications Mode, which enables point–to–point data links, such as the communication from keyboard to computer, or for the exchange of data between portable computers. In this mode it is capable of 200 kbps half duplex FSK operation.

The transmitter can also operate in an “A/V” Mode, which pulses the LED on and off with no carrier. (See Figure 11).

Digital Interface Bus

The MC13173 is controlled via a six line 3.3 V digital interface bus. That includes three control pins, data in and out pins, and a carrier detect pin. Listed below is a brief description of each pin and its function.

Table 1. Digital Interface Pin Descriptions

Pin	Pin Name	Symbol	I/O	Description
28	Transmit Enable	T	I	High – Transmitter is enabled Low – Transmitter is disabled
27	Data In	DI	I	Data Input – 38.2 kbps Communication Mode
3	Receive Enable	R	I	High – Receiver is enabled Low – Receiver is disabled
22	Data Out	DO	O	Demodulated Output Signal
17	Carrier Detect	CD	O	High – Carrier is present Low – Carrier is not present
26	Transmit Modulation Enable	E	I	High – Transmitter is in A/V Mode Low – Transmitter is in Communications Mode

This transceiver was designed for use in battery powered, hand–held consumer products. To minimize power consumption, the digital interface enables individual system blocks to be powered down while not in use. The following diagram shows the mode of the IC and the power state of each circuit block for a given set of control levels.

Table 2. Power State Table

Control Pins*				Circuit Block Power States (See Figures 2 and 3)				Supply Current (Typical)
T	R	E	Mode	Master VCO	FSK Modulator	Receiver	LED Driver	
0	0	0	OFF	Off	Off	Off	Off	10 nA
0	0	1	OFF	Off	Off	Off	Off	70 μA
0	1	X	Receive	On	Off	On	Off	6.5 mA
1	1	1	Receive	On	Off	On	On	7.5 mA
1	1	0	Transmit – Comm Mode	On	On	On	On	9.0 mA
1	0	0	Transmit – Comm Mode	On	On	Off	On	4.75 mA
1	0	1	Transmit – A/V Mode	Off	Off	Off	On	1.5 mA

* With Data In Pin Low

Master VCO/PLL

The master VCO provides the reference frequency for the FSK modulator and the LO frequency for the receiver downconverter. With a 32.768 kHz input frequency to the master VCO on Pin 1, the LO frequency for the receiver will be at 12.075 MHz. The reference frequency for the FSK modulator will be at approximately 1.1 MHz. The master VCO and FSK modulator are not used when the transmitter is used in A/V mode, and both are powered down.

Receiver Description

The single conversion receiver portion of the MC13173 is low power and wideband, and incorporates a split IF. This section includes a mixer, IF amplifier, limiting IF, quadrature detector and data slicer.

Mixer

The mixer is a double balanced four quadrant multiplier. It can be driven either differentially or single–ended by connecting the unused input to the positive supply rail.

The buffered output is internally loaded for an output impedance of 330 Ω for use with a standard ceramic filter.

IF Amplifier

The first IF amplifier section is composed of three differential stages with the second and third stages contributing to the RSSI. This section has internal DC feedback and external input decoupling for improved symmetry and stability. The total gain of the IF amplifier block is approximately 40 dB. The fixed internal input impedance is 330 Ω for use with a 10.7 MHz ceramic filter. The output of the IF amplifier is buffered and the impedance is 330 Ω.

Limiter

The limiter section is similar to the IF amplifier section, except that four stages are used with the last three contributing to the RSSI. This IF limiting amplifier section drives the quadrature detector internally.

RSSI/Carrier Detect

The received signal strength indicator (RSSI) outputs a current proportional to the log of the received signal amplitude. The RSSI current output is derived by summing the currents from the IF and limiting amplifier stages. An external resistor sets the output voltage range.

The carrier detect threshold is set at approximately 1.2 Vdc. When the RSSI level exceeds that threshold, the carrier detect output will go high. A large resistor may be added externally between the comparator output and the positive input for hysteresis.

Quadrature Detector

The demodulator is a conventional quadrature type with an external LC tank driven through an internal 5 pF capacitor. The output is buffered to give an output impedance of less than 1.0 kΩ at an average DC level of around 1.1 V.

Data Slicer

The data slicer is designed to square up the data signal. It is self centering at about 1.1 V, and clips at about 0.75 V and 1.45 V. There is a short time constant for large peak–to–peak voltage swings or when there is a change in DC level at the detector output. The time constant is longer for small signals or for continuous bits of the same polarity which drift close to the threshold voltage.

Transmission Description

The MC13173 uses a dual modulus PLL to frequency shift key (FSK) modulate the baseband digital input signal, producing the necessary logic high and low frequencies for transmission. The transmit frequency for a logic high is 1.427 MHz, and the frequency for a low is 1.317 MHz with a 32.768 kHz reference frequency.

FSK Modulator

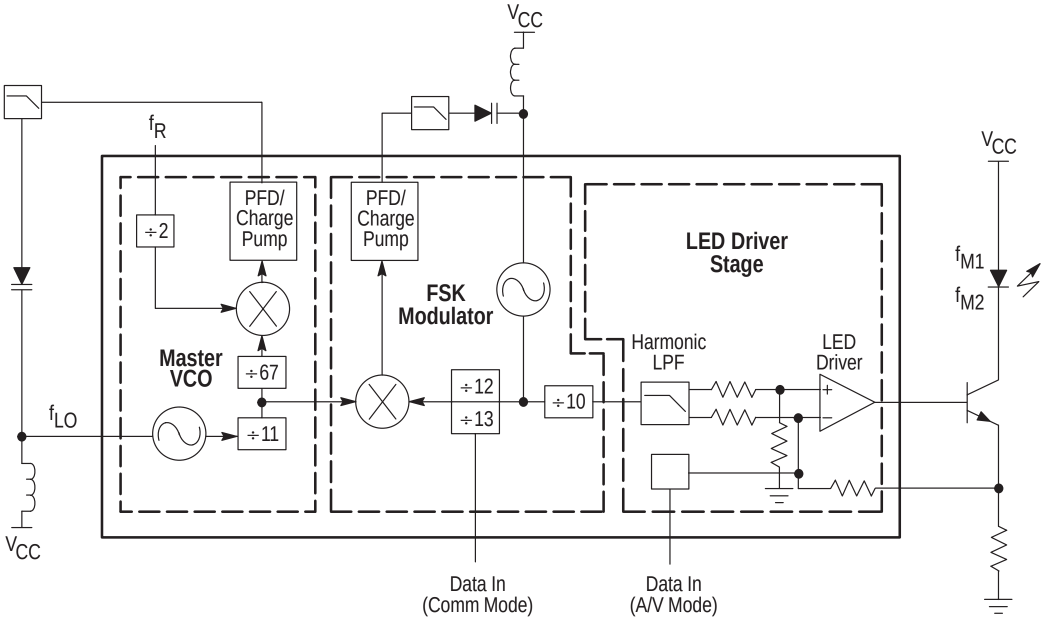
In the communications mode, the FSK modulator uses the reference frequency from the Master VCO to produce the two frequencies required for a logic high and a logic low. In the A/V mode, the FSK modulator is not used and is powered down.

LED Driver Stage

A low pass filter following the FSK modulator removes the undesired harmonic frequencies from the square–wave output of the divider circuits in PLLs. The resulting sinusoidal waveforms are fed into a unity gain difference amplifier, which drives the base of an external transistor, modulating the IR LED.

In A/V mode, the data is input directly into the inverting input of the op amp, and the low pass filter is not used.

Figure 2. Transmitter Block Diagram



f_R = 32.768 kHz

$f_{LO} = \frac{67 \times 11}{2} f_R$

Data High: $f_{M1} = \frac{13}{11 \times 10} f_{LO}$

Data Low: $f_{M2} = \frac{12}{11 \times 10} f_{LO}$

Figure 3. Receiver Block Diagram

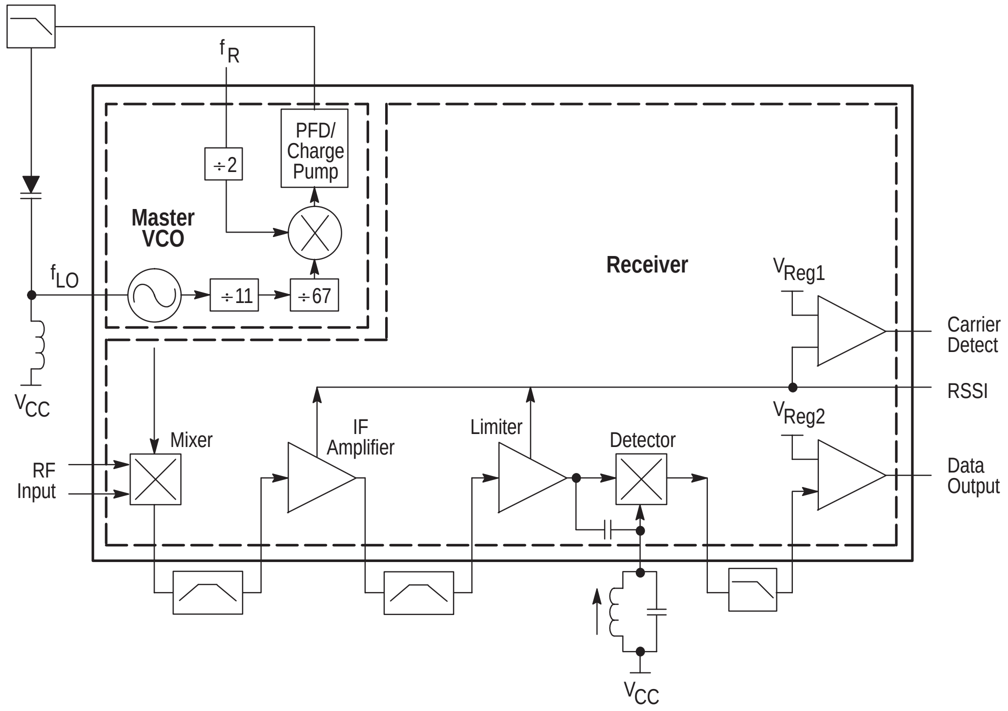


Table 3. PIN FUNCTION DESCRIPTION (T_A = 25°C, V_{CC} = 5.0 Vdc, f_{REF} = 32.768 kHz, f_{MOD} = 32.768 kHz)

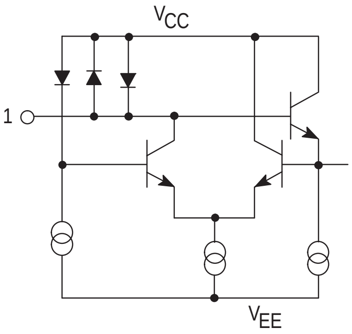
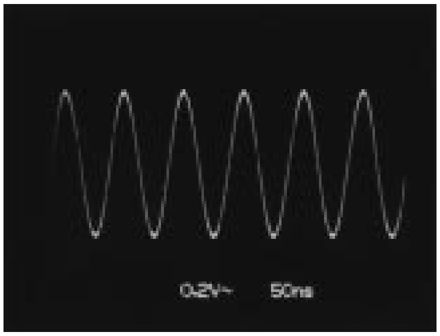
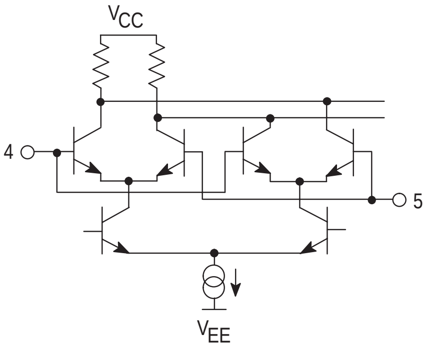
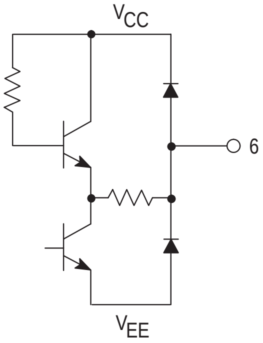
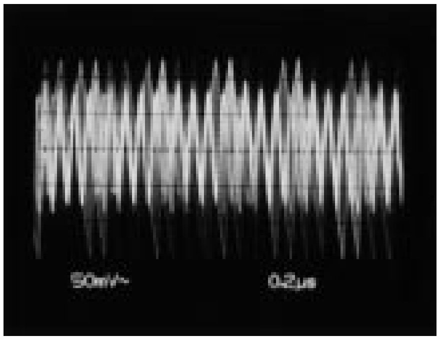
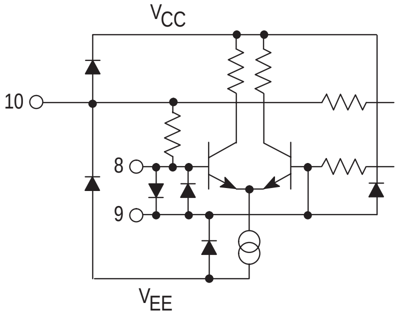
Pin	Symbol	Description	Internal Equivalent Circuit	Waveform
1	12 M	VCO for Master PLL. (Measured using a low capacitance FET probe. Standard oscilloscope probes can pull oscillator off frequency. See Figure 14.)		
2, 21, 23	V_{EE}	DC ground. Should be connected to a continuous ground plane on the PCB.		
3	R	Receive Enable Pin. See Tables 1 & 2.		
4, 5	RF In1 RF In2	RF Input to the mixer. 1.375 MHz average carrier frequency with ± 50 kHz deviation.		
6	Mixer Out	10.7 MHz IF Z_O = 330 Ω RF In = – 20 dBm Modulation = 32.768 kHz		
7, 12	V_{CC}	Supply voltage and RF ground, should be decoupled to V_{EE}.		
8	IF In	IF input impedance is 330 Ω. RF In = – 20 dBm Modulation = 32.768 kHz		

Table 3. PIN FUNCTION DESCRIPTION (continued) (T_A = 25°C, V_{CC} = 5.0 Vdc, f_{REF} = 32.768 kHz, f_{MOD} = 32.768 kHz)

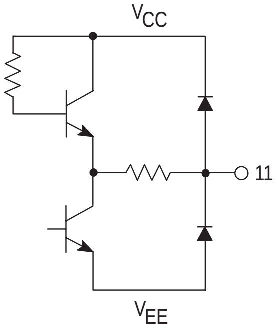
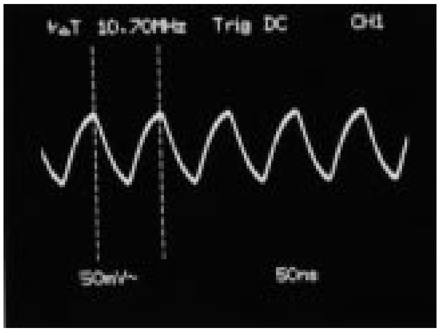
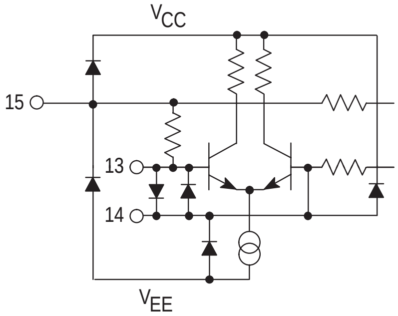
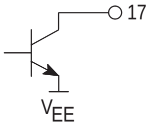
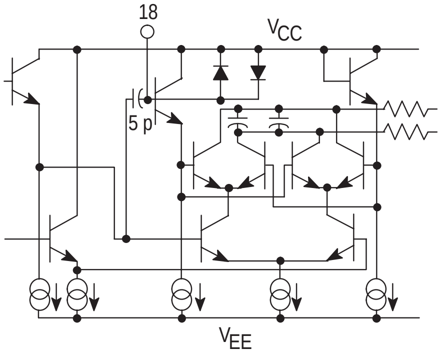
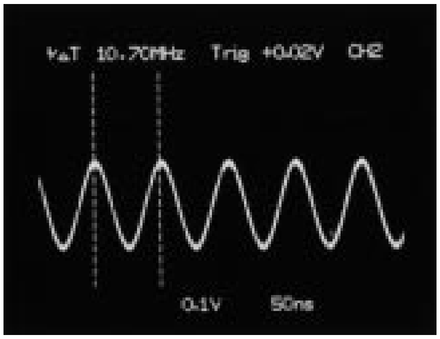
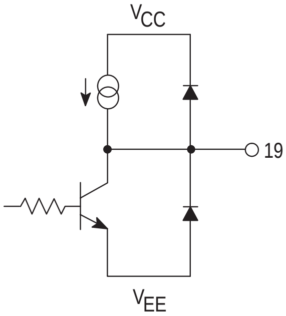
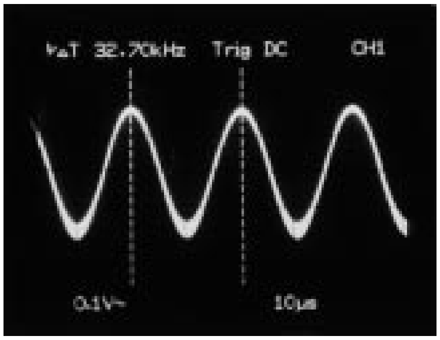
Pin	Symbol	Description	Internal Equivalent Circuit	Waveform
9, 10	IF Dec	IF decoupling as shown in Figure 15.	See Circuit for Pin 8.	
11	IF Out	IF Output. Z_O = 330 Ω. –20 dBm RF input level. Output is sinusoidal with lower drive levels.		
13	Lim In	Limiter input. Z_{In} = 330 Ω.		
14, 15	Lim Dec	External limiter decoupling as shown in application circuit.		
16	RSSI	Received Signal Strength Indicator Output. (See Figure 13)		
17	Carrier Detect	Logic output of the carrier detect comparator.		
18	Quad Coil	Quadrature tuning circuit. Modulated 10.7 MHz IF. Measured with a low capacitance FET probe.		
19	Demod	Demodulated signal output measured at the pin (before filtering). Modulation = 32.768 kHz sine wave.		

Table 3. PIN FUNCTION DESCRIPTION (continued) (T_A = 25°C, V_{CC} = 5.0 Vdc, f_{REF} = 32.768 kHz, f_{MOD} = 32.768 kHz)

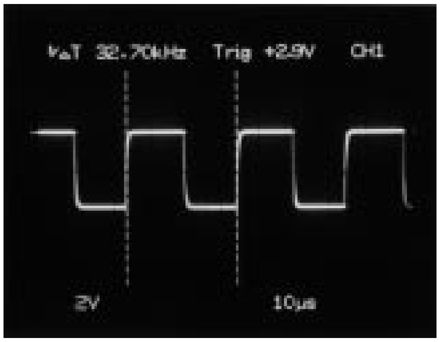
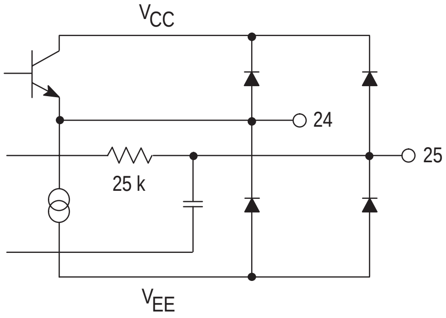
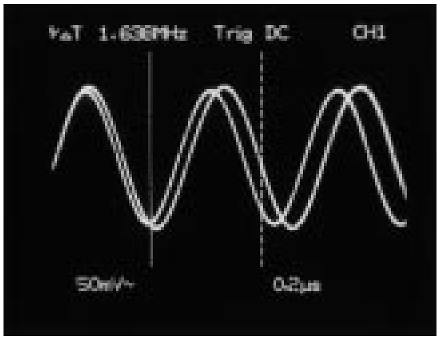
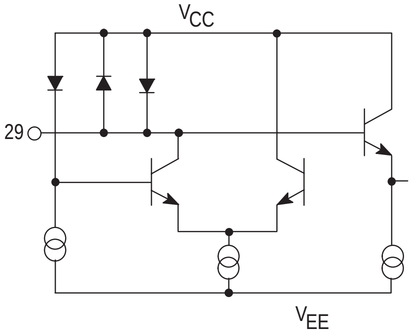
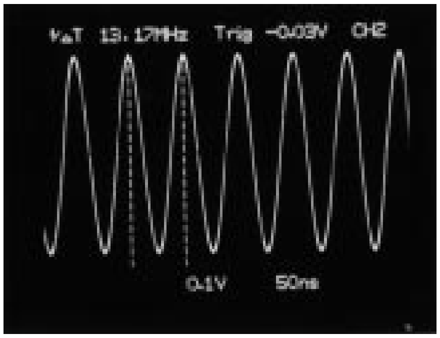
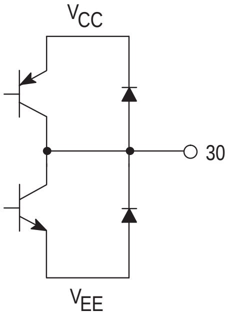
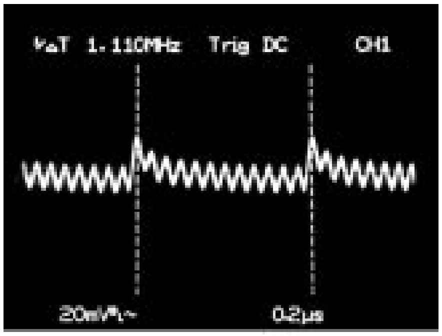
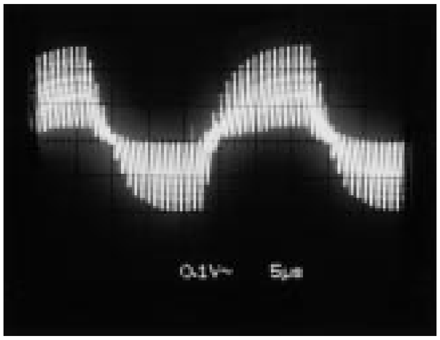
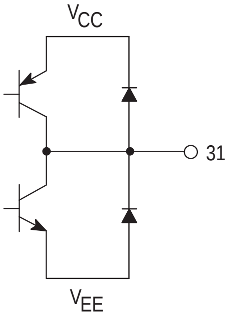
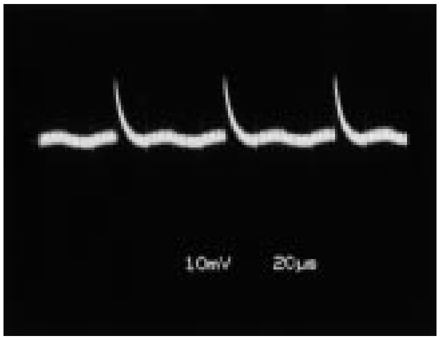
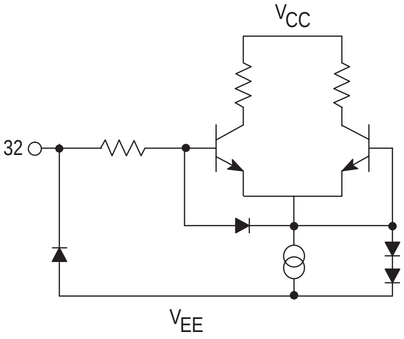
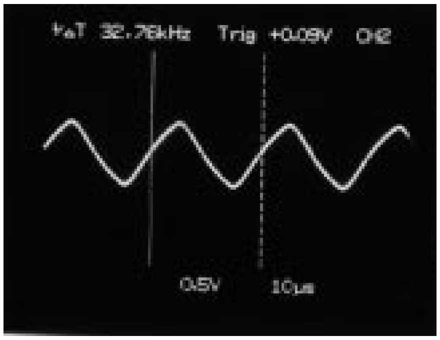
Pin	Symbol	Description	Internal Equivalent Circuit	Waveform
20	Data Slicer In	Input from the receiver demodulated output.		
22	Data Out	Output from the receiver data slicer. Modulation = 32.768 kHz sine wave. RF input driven by frequency generator. See also Figure 10.		
24	LED Driver Feed-back	Feedback for the LED driver op amp.		
25	IR LED Driver	Output of the unity gain output buffer in Communications Mode. See Figure 11 for transmit output in A/V mode. Modulation = 32.768 kHz square wave. .		
26	E	Transmit Modulation Enable. See Tables 1 & 2.		
27	Data In	Modulation input for transmit data.		
28	T	Transmit Enable pin. See Tables 1 & 2.		
29	14 MHz Ref	VCO for FSK Modulator phase locked loop. (Measured using a low capacitance FET probe. Standard oscilloscope probes can pull oscillator off frequency. See Figure 14.) No modulation (Data In low).		

Table 3. PIN FUNCTION DESCRIPTION (continued) (T_A = 25°C, V_{CC} = 5.0 Vdc, f_{REF} = 32.768 kHz, f_{MOD} = 32.768 kHz)

Pin	Symbol	Description	Internal Equivalent Circuit	Waveform
30	Tx PLL	Phase detector output for the FSK Modulator. (With loop closed and locked.) No modulation (Data In low).		
		With 32.768 kHz square wave modulation. Note: Probing the output of the phase detectors directly may disturb the loop. It is best to probe the output of the op amp when evaluating loop response.		
31	Ma PLL	Output of the phase detector charge pump for the Master PLL. (With loop closed and locked.)		
32	32 kHz Ref	Input to 32.768 kHz reference. Filtered from TTL oscillator using application circuit in Figure 15. Approximately 1.0 Vp–p triangle wave at 32.768 kHz.		

Typical Performance Over Temperature

(Measured using test circuit in Figure 1)

Figure 4. Normalized Mixer Gain versus Temperature

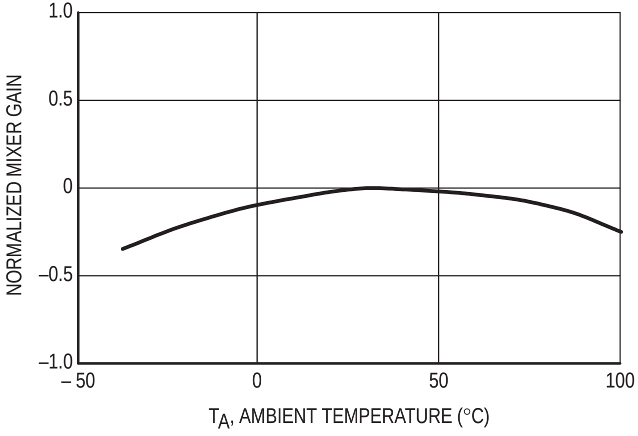


Figure 5. Normalized IF Amp Gain versus Temperature

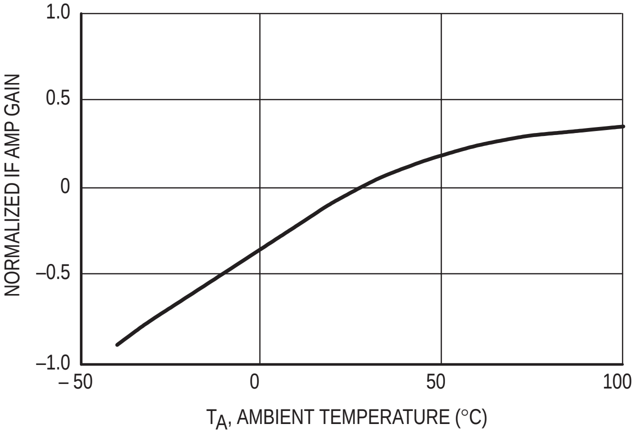


Figure 6. Maximum Pull–Up Current versus Temperature (Pin 25)

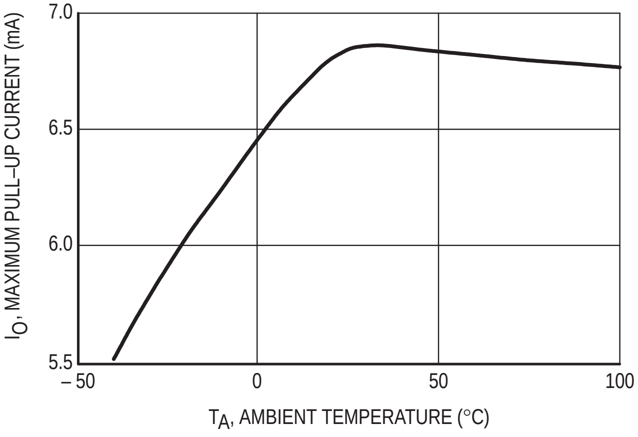


Figure 7. Maximum Pull–Down Current versus Temperature (Pin 25)

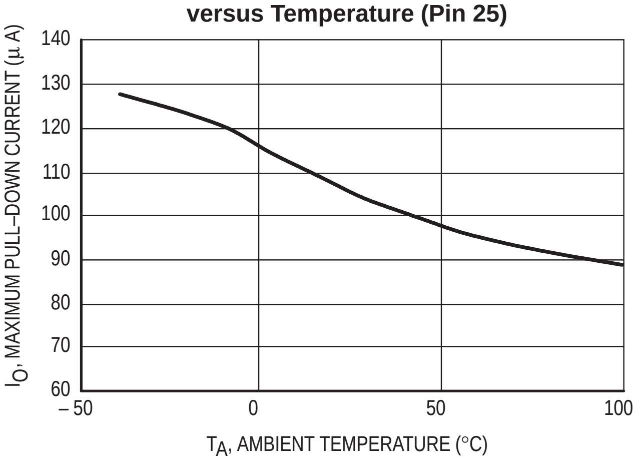


Figure 8. Supply Current versus Temperature

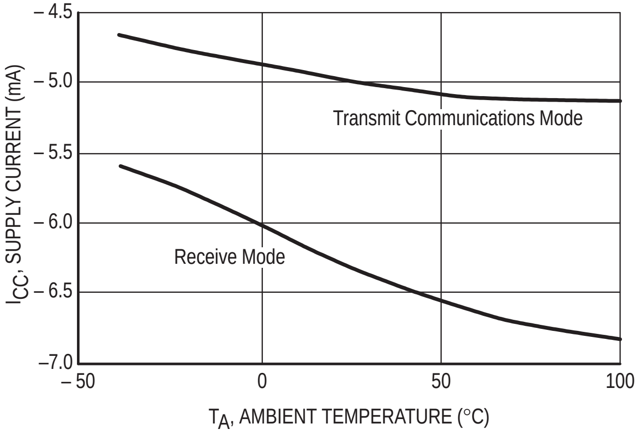
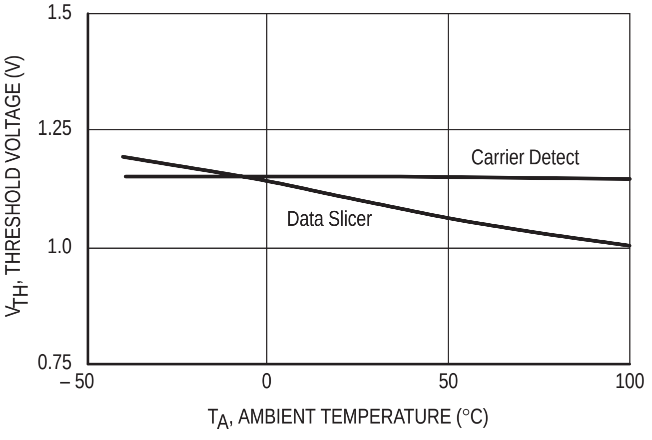


Figure 9. Data Slicer and Carrier Detect Threshold Voltages versus Temperature



APPLICATIONS INFORMATION

The MC13173 transceiver is specially designed to operate from a 32.768 kHz reference which is readily available in most computer applications. The frequency synthesizer on chip generates a receiver local oscillator frequency and the transmit mark and space frequencies from this fixed reference frequency, eliminating the need for additional crystals or manual tuning.

Large divide ratios are needed to generate these frequencies, however. For example, the receiver LO frequency is 368.5 times the 32.768 kHz reference frequency. This requires that the reference frequency be both accurate and stable. A two percent error in the reference frequency would pull the LO off frequency by over 240 kHz, putting the IF frequency out of the usable bandwidth of the filters and discriminator. For this reason, a 32.768 kHz oscillator circuit has been included on the demonstration board design. Although TTL crystal oscillators are available, this oscillator circuit uses an inexpensive tuning fork crystal and a hex inverter to generate a square wave reference frequency, which is then filtered and level adjusted to a 1.0 Vp–p triangle wave to drive pin 32. A TTL Clock Oscillator could also be used with the filter circuit as shown.

Frequency Synthesizer

The recommended op amp for the external loop filter is the MC33202. For low voltage operation, ($V_{CC} \leq 3.3$ V) an op amp that is rail–to–rail on both the input and output is advisable to obtain the widest possible output voltage range without distortion. Sufficient distortion from the op amp such as phase reversal on the output caused by overdriving the inputs could prevent the loop from locking to the reference.

In debugging the loop filter, it is important to note that the FSK Modulator phase locked loop will not lock until the Master VCO is locked to the reference. If the application circuit in Figure 15 is used, both loops should lock without the need for any additional tweaking. Since the VCO has ±2.0 MHz of range using the MV209 varactor diode (see Figure 11), neither precision components nor tuning should be required. To ensure both loops are operating properly, first evaluate each VCO with the loop open and a voltage equal to $V_{CC}/2$ applied to the resistor in series with the varactor. Since there is a relatively small capacitance (<40 pF) in series with the LC tank circuit, the VCO pin is sensitive to any parasitic capacitance. Thus when using a standard oscilloscope probe having 10 to 20 pF capacitance it is difficult to measure the VCO frequency without shifting its frequency. A low capacitance FET probe used with a frequency counter will enable you to accurately measure the VCO frequency without altering it in the process.

The free running frequency of the VCO should be approximately on frequency when the loop is open and the varactor is biased at mid–supply. The VCO for the Master PLL should run at 12.05 MHz. The free running frequency of the FSK Modulator should be at 13.72 MHz, midway between the two VCO frequencies needed to generate the transmit mark and space frequencies. The FSK Modulator loop is only active when the transmitter is enabled and the device is in the communications mode (see Tables 1 & 2). **If either the “T” pin is low or the “E” pin is high, the VCO will be off and you will see no oscillation on Pin 29.**

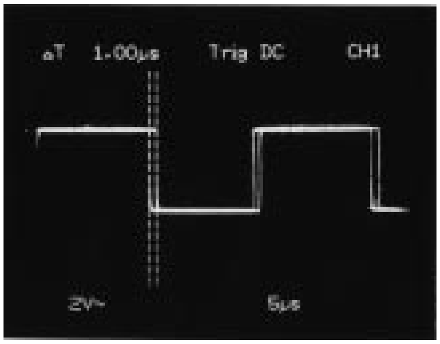
Once the loops are closed, the VCO frequencies should track the reference frequency within the hold–in range of the loop. Although the FSK Modulator loop is dependent on the Master VCO, the Master VCO is completely independent of the FSK Modulator. In fact, the FSK Modulator can be powered down (see Table 2) without affecting the Master VCO operation. In the application circuit in Figure 15 a single reference voltage for both op amps in the loop filters is provided by two diodes to V_{CC}. If the Master VCO is affected by the FSK Modulator loop, this generally indicates a problem with the common reference voltage to the op amp, and may mean the diodes are in backwards.

Once the loops are closed you should see a phase detector output such as is shown in the Pin Function Description in Table 3. If the VCO was on frequency when the loop was open, the phase detector outputs should swing around mid supply and not hit against either the positive or negative rail. Latching to V_{CC} or V_{EE} may indicate the loop filter circuitry is not implemented correctly.

Due to the digital design of the phase detectors, the transmitter can only transition between mark and space frequencies on a clock edge. On the receive side this may be seen as a double image on the detector output, with a discrete time delay which does not vary with the frequency of the data input (see Figure 10). This is a normal consequence of using a digital phase detector and should not be confused with jitter from the data slicer.

Figure 10. Receive Data Output

(Data Transmitted from Companion MC13173)



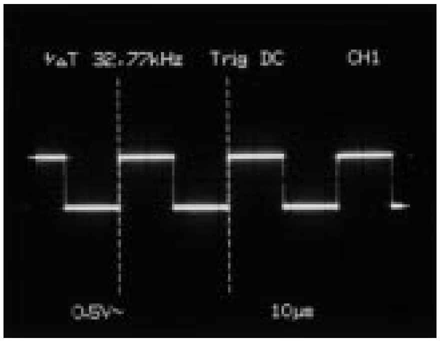
Transmitter

The light emitting diode (LED) driver in the transmitter is capable of 6.0 to 10 mA of pull–up current. Selection of the external transistor and biasing resistor will depend on the LEDs used. Typical infrared LEDs require 50 to 100 mA of current and have a forward voltage of 1.5V. Sufficient current is needed to obtain the maximum power output without distorting the output by overdriving the LED. Key specifications include rise and fall time, wavelength, beam width (generally given in half–angle), maximum power output and efficiency. Choice of wavelengths is generally determined by cost and power efficiency, which may vary between vendors. The LEDs used in this application are at 880 nm and were chosen for best efficiency. However LEDs in general are very inefficient, converting only 1 or 2 percent of the electrical power into optical power. Multiple LEDs can be used to increase transceiver range.

Disabling the transmitter via the data bus turns off the output of the LED driver, removing the base current from the external transistor and thereby turning off the IR LED. Because of the high current drawn by the LED, this offers considerable power savings when the transmitter is not in use and can be easily controlled by a microcontroller with no additional circuitry.

In the “A/V” transmit mode, the data output is on/off keyed, with the LED on for a data high, and off for a data low. It is a baseband signal, with no carrier present (see Figure 11).

Figure 11. LED Driver Output in A/V Mode



Receiver

The receiver portion of the MC13173 is similar to the design of Motorola’s MC13156 Wideband FM Receiver. Instead of using the mixer to downconvert from a higher RF frequency, this application is designed to upconvert the 1.372 MHz input to a 10.7 MHz IF. The wide deviation, relative to the RF input frequency, requires a low Q tuned circuit to recover this bandwidth:

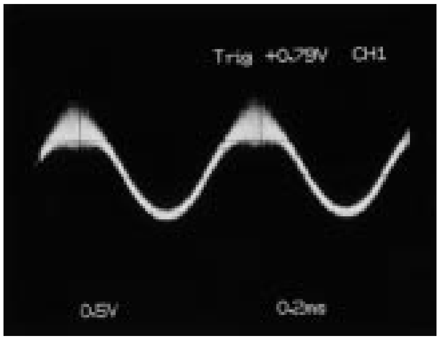
$$Q \approx \frac{f_C}{BW_{3\ dB}},\ \text{where } f_C = 1.372\ \text{MHz}$$

By Carson’s Rule, the BW = 2(fdev + fmod). Since for mark/space frequencies of 1.317 MHz and 1.427 MHz the deviation is fixed at ±50 kHz, the bandwidth for a 50 kHz square wave (100 kbps) would be 200 kHz, and the tuned input requires a Q of less than 7. The low Q of the tank circuit reduces both the selectivity and the sensitivity of the receiver. For a Q of 7, the resistor required across the 56 µH inductor can be calculated:

$$R = QX_L = (7) \bullet (2\pi) \bullet (1.372\ E6) \bullet (56\ E{-}6)$$
$$R = 3.3\ k\Omega$$

The 10.7 MHz ceramic filters also need to be wide enough to pass the full frequency range which will include some harmonics. In the application circuit in Figure 15, Toko filters with a bandwidth of 330 kHz or 360 kHz are recommended to accommodate higher data rates. If the IF filters are too narrow, the recovered signal may have noise on the peaks (see Figure 12).

Figure 12. Receive Data Output



The RSSI has over 70 dB of dynamic range and 20 µA of current range. The RSSI output provides the input to the carrier detect comparator (see Figure 13) and a logarithmic output proportional to the input signal level. It can, therefore, be used to recover amplitude shift keyed (ASK) data.

The key specifications for the infrared detectors are response time, sensitivity, acceptance angle, and wavelength. Some vendors offer detectors in a black package with a built–in daylight filter. Although the transparent packages offer better sensitivity, the detectors with the daylight filter offer a much better signal to noise ratio. Response time (or maximum frequency) of the system is generally limited by the capability of the emitters rather than the detectors. For this application, a rise and fall time of 500 ns is sufficient.

Design and Layout Considerations

Although the frequencies in this design are low by RF standards, careful layout and good decoupling are still good practice. The high gain limiter and IF blocks should be decoupled as shown in the application circuit as near the IC as possible for best receiver performance. Also the TTL levels from the reference oscillator and the wide current swing applied to the IR LEDs can easily be picked up on V_{CC}, creating problems for the sensitive phase detector circuits and receiver RF inputs. Avoid long parallel traces and use plenty of decoupling to keep the supply rail clean.

Typical Performance

(Measured using Application Circuit in Figure 15)

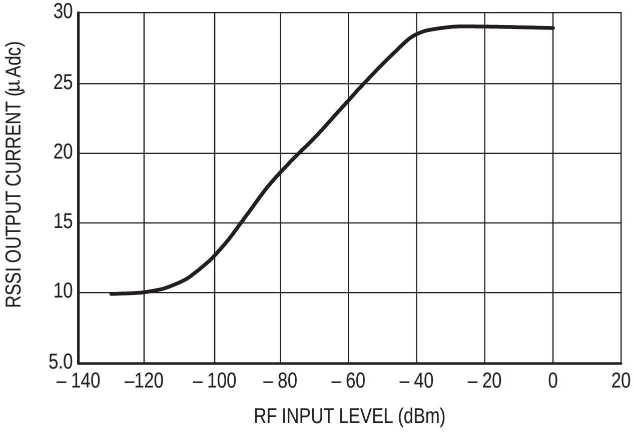


Figure 13. RSSI Output Current versus RF Input Level

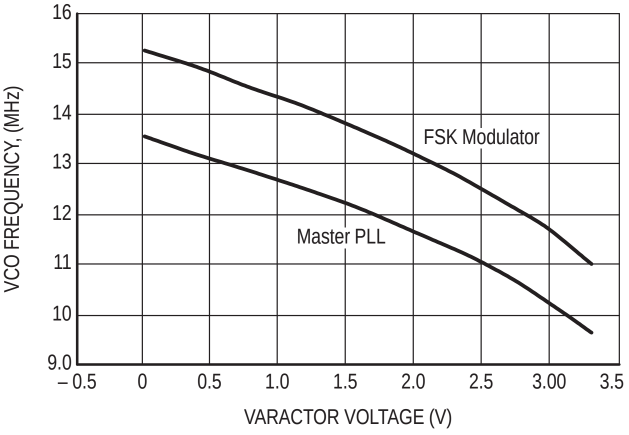
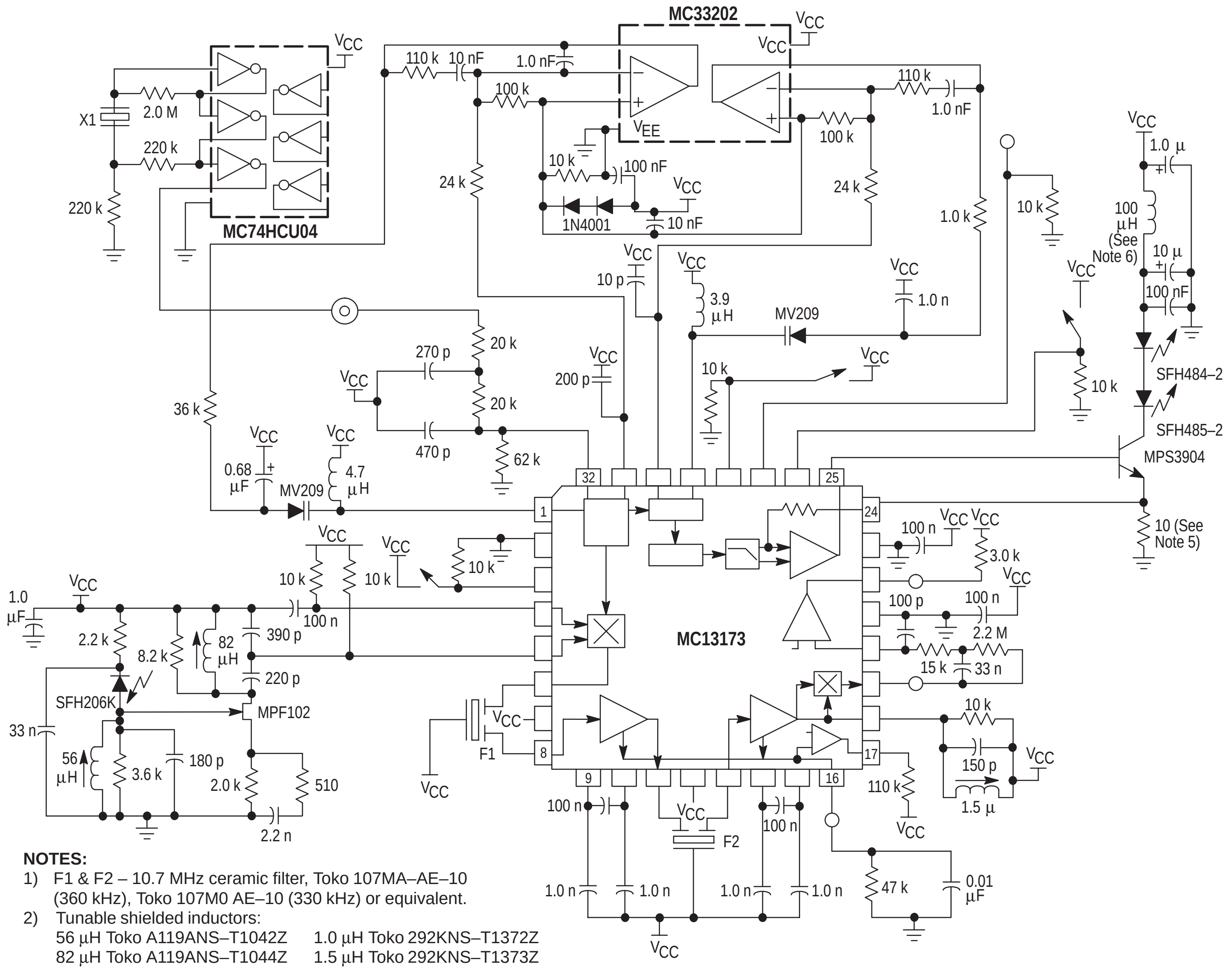


Figure 14. VCO Frequency versus Varactor Voltage

Figure 15. Application Circuit



NOTES:

1) F1 & F2 – 10.7 MHz ceramic filter, Toko 107MA–AE–10 (360 kHz), Toko 107M0 AE–10 (330 kHz) or equivalent.
2) Tunable shielded inductors:
   56 µH Toko A119ANS–T1042Z   1.0 µH Toko 292KNS–T1372Z
   82 µH Toko A119ANS–T1044Z   1.5 µH Toko 292KNS–T1373Z
3) Crystal – 32.768 kHz C – Type tuning fork crystal. Digikey part number SE3201 or equivalent.
4) LEDs and Detectors SFH484–2, SFH485–2 and SFH206K are made by Siemens.
5) Optimum bias resistor depends on the LEDs used.
6) May be fixed or tunable.

Figure 16. Component Placement

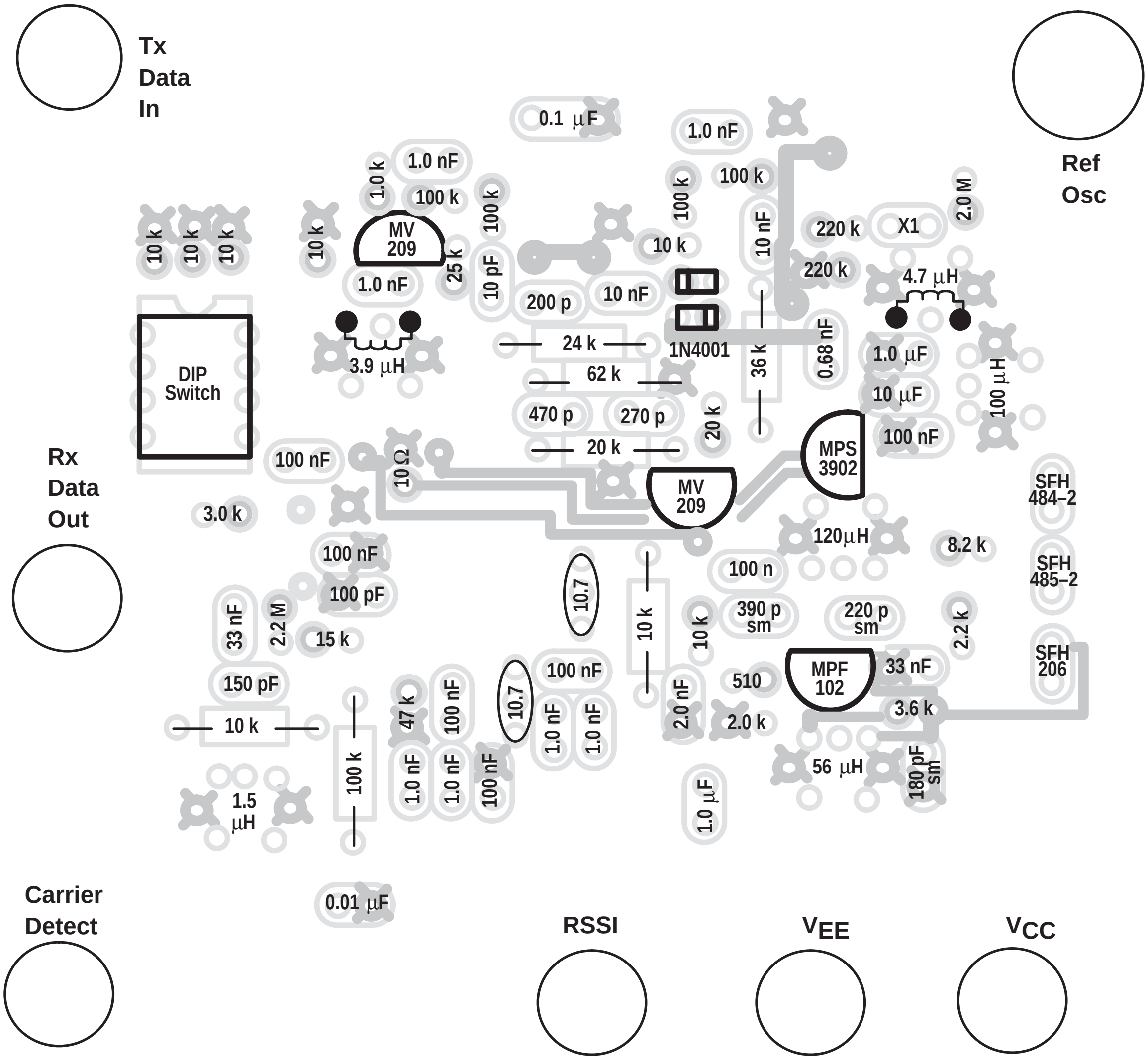


Figure 17. Solder Side View

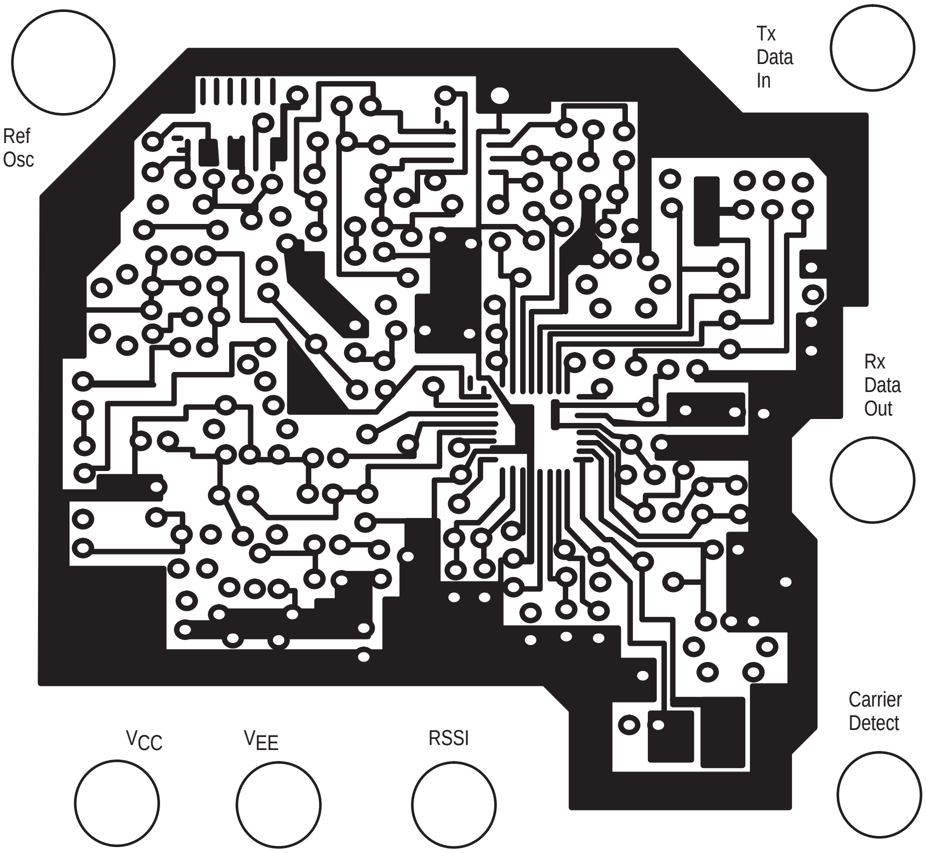


Figure 18. Component Side View

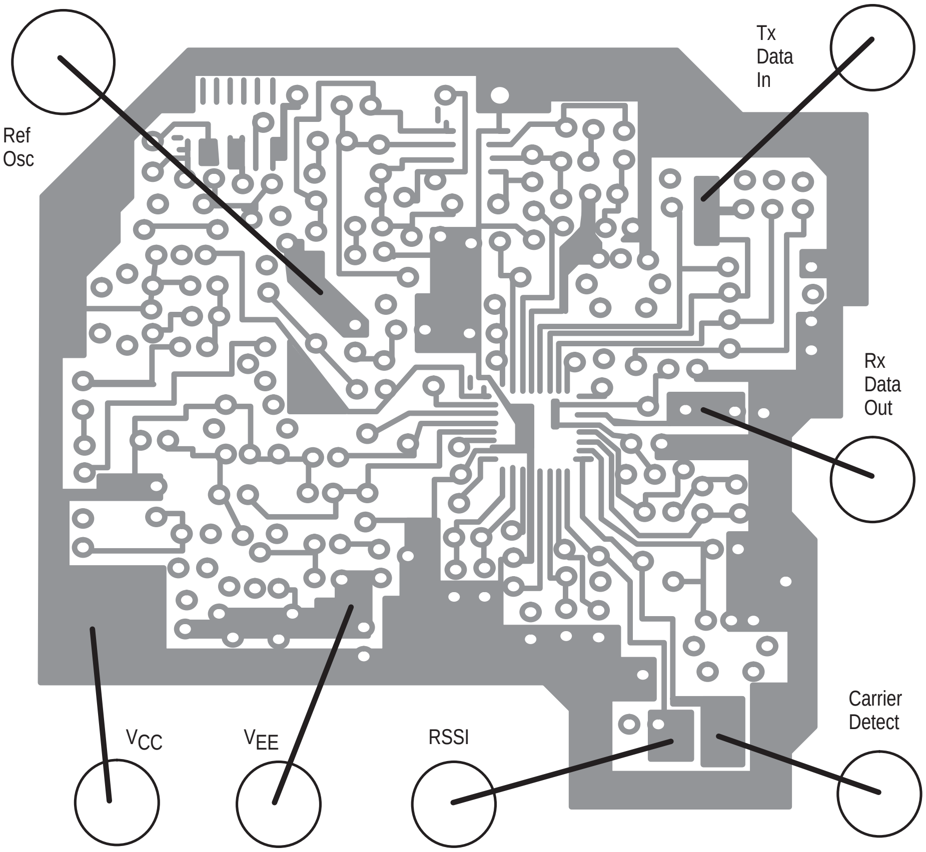
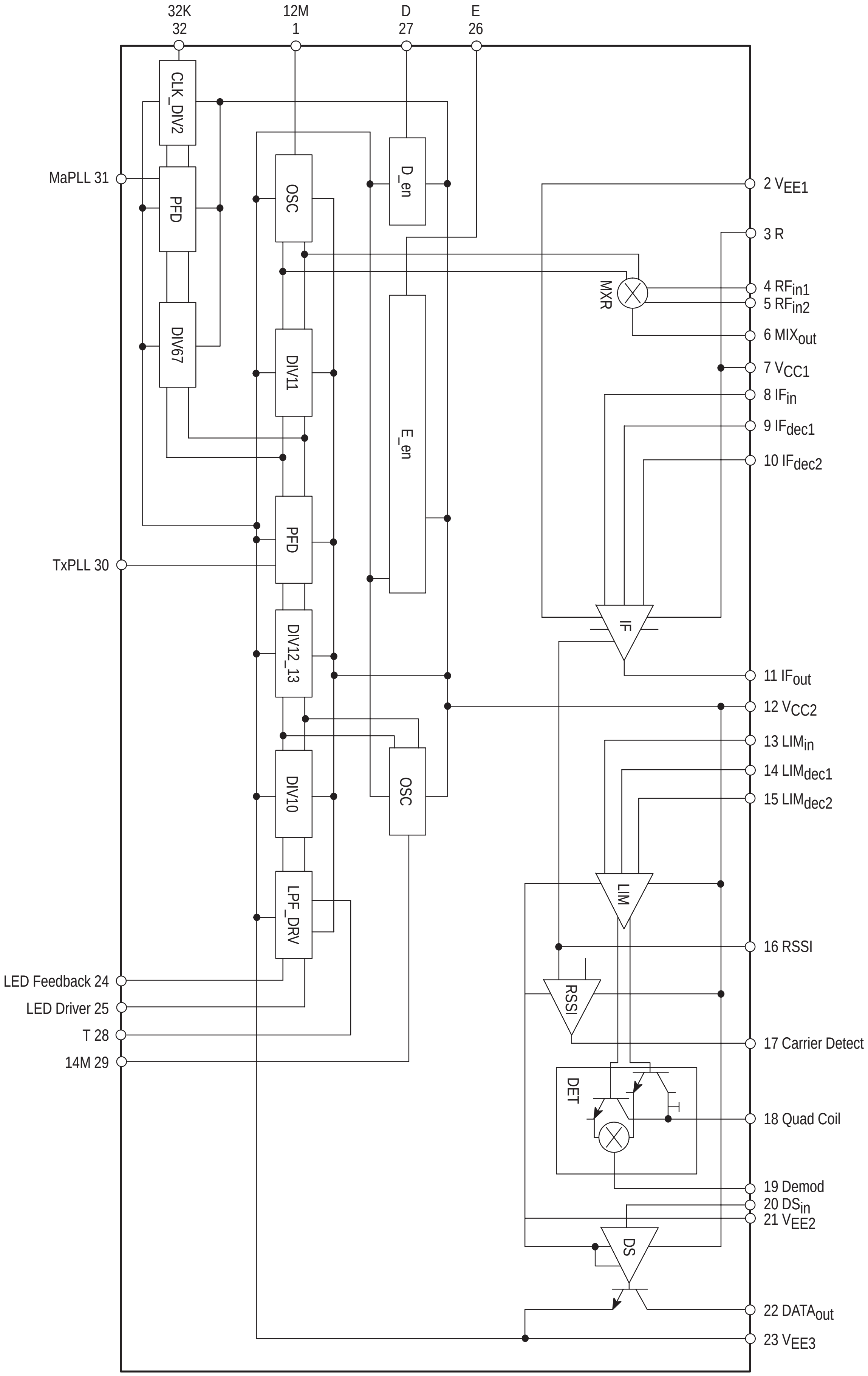


Figure 19. Detailed Internal Block Diagram



MOTOROLA

MC13175
MC13176

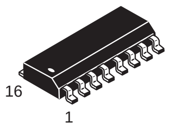
UHF FM/AM Transmitter

UHF FM/AM TRANSMITTER

SEMICONDUCTOR TECHNICAL DATA

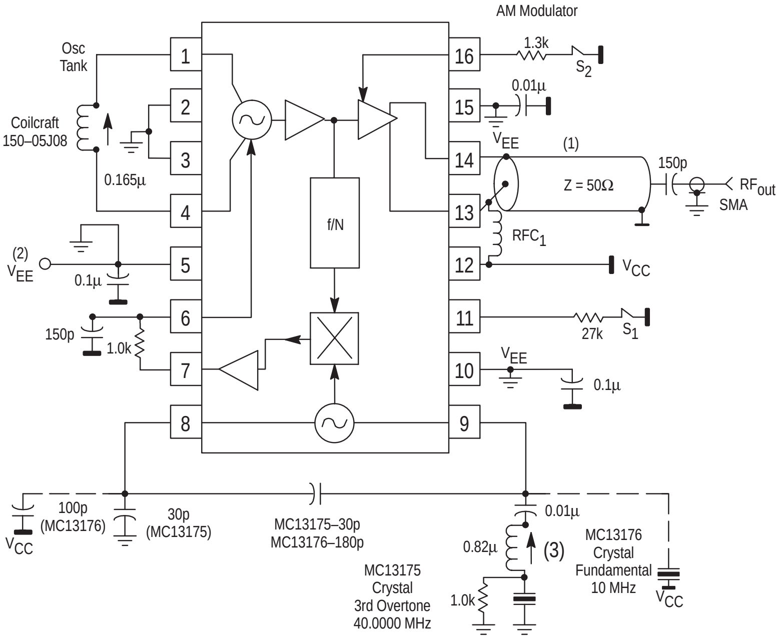
The MC13175 and MC13176 are one chip FM/AM transmitter subsystems designed for AM/FM communication systems. They include a Colpitts crystal reference oscillator, UHF oscillator, ÷ 8 (MC13175) or ÷ 32 (MC13176) prescaler and phase detector forming a versatile PLL system. Targeted applications are in the 260 to 470 MHz band and 902 to 928 MHz band covered by FCC Title 47; Part 15. Other applications include local oscillator sources in UHF and 900 MHz receivers, UHF and 900 MHz video transmitters, RF Local Area Networks (LANs), and high frequency clock drivers. The MC13175/76 offer the following features:

- UHF Current Controlled Oscillator
- Uses Easily Available 3rd Overtone or Fundamental Crystals for Reference
- Fewer External Parts Required
- Low Operating Supply Voltage (1.8 to 5.0 Vdc)
- Low Supply Drain Currents
- Power Output Adjustable (Up to +10 dBm)
- Differential Output for Loop Antenna or Balun Transformer Networks
- Power Down Feature
- ASK Modulated by Switching Output On and Off
- (MC13175) $f_o = 8 \times f_{ref}$; (MC13176) $f_o = 32 \times f_{ref}$



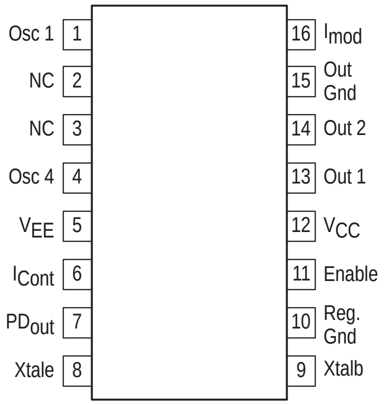
D SUFFIX
PLASTIC PACKAGE
CASE 751B
(SO–16)

Figure 1. Typical Application as 320 MHz AM Transmitter



NOTES: 1. 50 Ω coaxial balun, 1/10 wavelength at 320 MHz equals 1.5 inches.
2. Pins 5, 10 & 15 are ground and connected to V_{EE} which is the component/DC ground plane side of PCB. These pins must be decoupled to V_{CC}; decoupling capacitors should be placed as close as possible to the pins.
3. The crystal oscillator circuit may be adjusted for frequency with the variable inductor (MC13175); recommended source is Coilcraft “slot seven” 7mm tuneable inductor, Part #7M3–821. 1.0k resistor. Shunting the crystal prevents it from oscillating in the fundamental mode.

PIN CONNECTIONS



ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC13175D	T_A = – 40° to +85°C	SO–16
MC13176D		SO–16

MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted.)

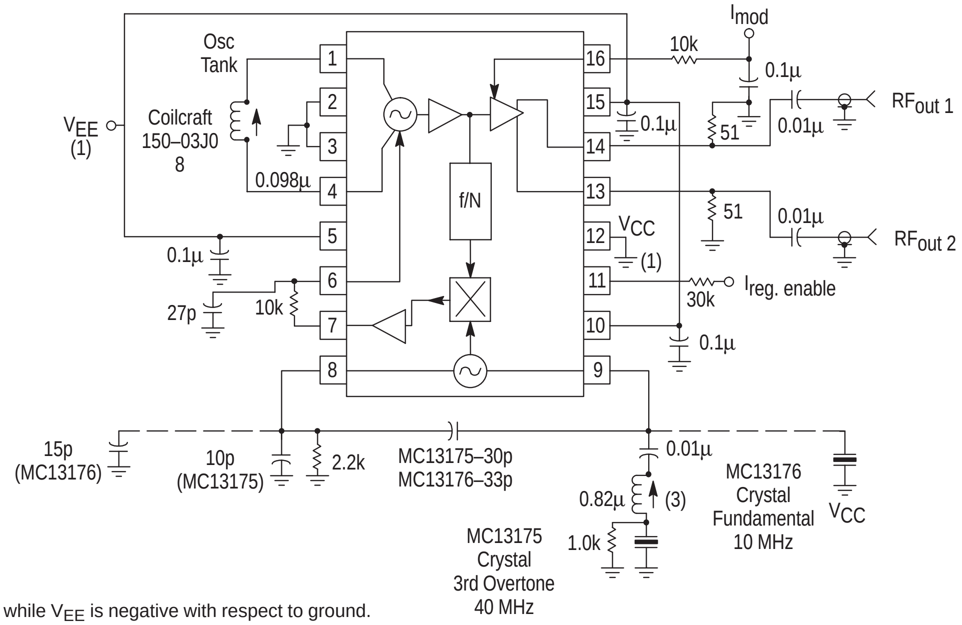
Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	7.0 (max)	Vdc
Operating Supply Voltage Range	V_{CC}	1.8 to 5.0	Vdc
Junction Temperature	T_J	+150	°C
Operating Ambient Temperature	T_A	– 40 to + 85	°C
Storage Temperature	T_{stg}	– 65 to +150	°C

ELECTRICAL CHARACTERISTICS (Figure 2; V_{EE} = – 3.0 Vdc, T_A = 25°C, unless otherwise noted.)*

Characteristic	Pin	Symbol	Min	Typ	Max	Unit
Supply Current (Power down: I_{11} & I_{16} = 0)	–	I_{EE1}	– 0.5	–	–	µA
Supply Current (Enable [Pin 11] to V_{CC} thru 30 k, I_{16} = 0)	–	I_{EE2}	–18	–14	–	mA
Total Supply Current (Transmit Mode) (I_{mod} = 2.0 mA; f_o = 320 MHz)	–	I_{EE3}	– 39	– 34	–	mA
Differential Output Power (f_o = 320 MHz; V_{ref} [Pin 9] = 500 $mV_{p–p}$; f_o = N x f_{ref})	13 & 14	P_{out}				dBm
I_{mod} = 2.0 mA (see Figure 7, 8)			2.0	+ 4.7	–	
I_{mod} = 0 mA			–	– 45	–	
Hold–in Range (± Δf_{ref} x N)	13 & 14	± Δf_H				MHz
MC13175 (see Figure 7)			3.5	6.5	–	
MC13176 (see Figure 8)			4.0	8.0	–	
Phase Detector Output Error Current	7	I_{error}				µA
MC13175			20	25	–	
MC13176			22	27	–	
Oscillator Enable Time (see Figure 22b)	11 & 8	t_{enable}	–	4.0	–	ms
Amplitude Modulation Bandwidth (see Figure 24)	16	BW_{AM}	–	25	–	MHz
Spurious Outputs (I_{mod} = 2.0 mA)	13 & 14	P_{son}	–	– 50	–	dBc
Spurious Outputs (I_{mod} = 0 mA)	13 & 14	P_{soff}	–	– 50	–	
Maximum Divider Input Frequency	–	f_{div}	–	950	–	MHz
Maximum Output Frequency	13 & 14	f_o	–	950	–	

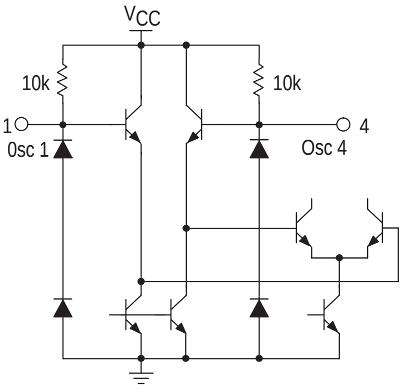
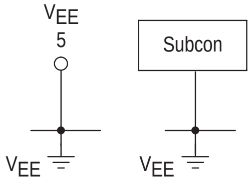
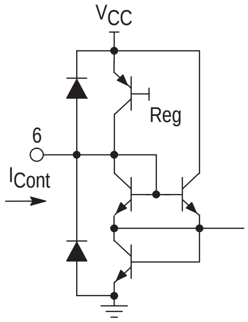
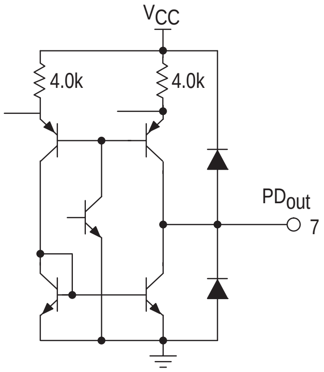
* For testing purposes, V_{CC} is ground (see Figure 2).

Figure 2. 320 MHz Test Circuit



NOTES: 1. V_{CC} is ground; while V_{EE} is negative with respect to ground.
2. Pins 5, 10 and 15 are brought to the circuit side of the PCB via plated through holes. They are connected together with a trace on the PCB and each Pin is decoupled to V_{CC} (ground).
3. Recommended source is Coilcraft "slot seven" inductor, part number 7M3–821.

PIN FUNCTION DESCRIPTIONS

Pin	Symbol	Internal Equivalent Circuit	Description/External Circuit Requirements
1 & 4	Osc 1, Osc 4		**CCO Inputs** The oscillator is a current controlled type. An external oscillator coil is connected to Pins 1 and 4 which forms a parallel resonance LC tank circuit with the internal capacitance of the IC and with parasitic capacitance of the PC board. Three base–emitter capacitances in series configuration form the capacitance for the parallel tank. These are the base–emitters at Pins 1 and 4 and the base–emitter of the differential amplifier. The equivalent series capacitance in the differential amplifier is varied by the modulating current from the frequency control circuit (see Pin 6, internal circuit). A more thorough discussion is found in the Applications Information section.
5	V_{EE}		**Supply Ground (V_{EE})** In the PCB layout, the ground pins (also applies to Pins 10 and 15) should be connected directly to chassis ground. Decoupling capacitors to V_{CC} should be placed directly at the ground returns.
6	I_{Cont}		**Frequency Control** For V_{CC} = 3.0 Vdc, the voltage at Pin 6 is approximately 1.55 Vdc. The oscillator is current controlled by the error current from the phase detector. This current is amplified to drive the current source in the oscillator section which controls the frequency of the oscillator. Figures 9 and 10 show the Δf_{osc} versus I_{Cont}, Figure 5 shows the Δf_{osc} versus I_{Cont} at – 40°C, + 25°C and + 85°C for 320 MHz. The CCO may be FM modulated as shown in Figure 17, MC13176 320 MHz FM Transmitter. A detailed discussion is found in the Applications Information section.
7	PD_{out}		**Phase Detector Output** The phase detector provides ± 30 µA to keep the CCO locked at the desired carrier frequency. The output impedance of the phase detector is approximately 53 kΩ. Under closed loop conditions there is a DC voltage which is dependent upon the free running oscillator and the reference oscillator frequencies. The circuitry between Pins 7 and 6 should be selected for adequate loop filtering necessary to stabilize and filter the loop response. Low pass filtering between Pin 7 and 6 is needed so that the corner frequency is well below the sum of the divider and the reference oscillator frequencies, but high enough to allow for fast response to keep the loop locked. Refer to the Applications Information section regarding loop filtering and FM modulation.

PIN FUNCTION DESCRIPTIONS

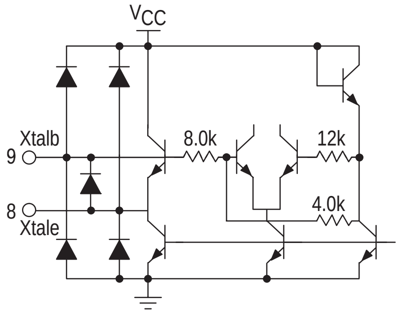
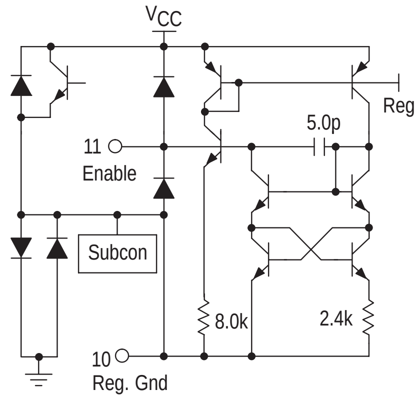
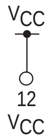
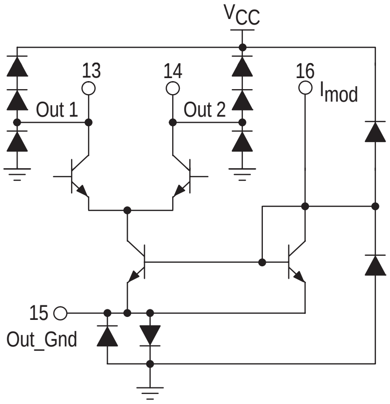
Pin	Symbol	Internal Equivalent Circuit	Description/External Circuit Requirements
8	Xtale		**Crystal Oscillator Inputs** The internal reference oscillator is configured as a common emitter Colpitts. It may be operated with either a fundamental or overtone crystal depending on the carrier frequency and the internal prescaler. Crystal oscillator circuits and specifications of crystals are discussed in detail in the applications section. With V_{CC} = 3.0 Vdc, the voltage at Pin 8 is approximately 1.8 Vdc and at Pin 9 is approximately 2.3 Vdc. 500 to 1000 mVp–p should be present at Pin 9. The Colpitts is biased at 200 μA; additional drive may be acquired by increasing the bias to approximately 500 μA. Use 6.2 k from Pin 8 to ground.
9	Xtalb		
10	Reg. Gnd		**Regulator Ground** An additional ground pin is provided to enhance the stability of the system. Decoupling to the V_{CC} (RF ground) is essential; it should be done at the ground return for Pin 10.
11	Enable		**Device Enable** The potential at Pin 11 is approximately 1.25 Vdc. When Pin 11 is open, the transmitter is disabled in a power down mode and draws less than 1.0 μA I_{CC} if the MOD at Pin 16 is also open (i.e., it has no current driving it). To enable the transmitter a current source of 10 μA to 90 μA is provided. Figures 3 and 4 show the relationship between I_{CC}, V_{CC} and $I_{reg.\ enable}$. Note that I_{CC} is flat at approximately 10 mA for $I_{reg.\ enable}$ = 5.0 to 100 μA (I_{mod} = 0).
12	V_{CC}		**Supply Voltage (V_{CC})** The operating supply voltage range is from 1.8 Vdc to 5.0 Vdc. In the PCB layout, the V_{CC} trace must be kept as wide as possible to minimize inductive reactances along the trace; it is best to have it completely fill around the surface mount components and traces on the circuit side of the PCB.
13 & 14	Out 1 and Out 2		**Differential Output** The output is configured differentially to easily drive a loop antenna. By using a transformer or balun, as shown in the application schematic, the device may then drive an unbalanced low impedance load. Figure 6 shows how much the Output Power and Free–Running Oscillator Frequency change with temperature at 3.0 Vdc; I_{mod} = 2.0 mA.
15	Out_Gnd		**Output Ground** This additional ground pin provides direct access for the output ground to the circuit board V_{EE}.
16	I_{mod}		**AM Modulation/Power Output Level** The DC voltage at this pin is 0.8 Vdc with the current source active. An external resistor is chosen to provide a source current of 1.0 to 3.0 mA, depending on the desired output power level at a given V_{CC}. Figure 23 shows the relationship of Power Output to Modulation Current, I_{mod}. At V_{CC} = 3.0 Vdc, 3.5 dBm power output can be acquired with about 35 mA I_{CC}. For FM modulation, Pin 16 is used to set the desired output power level as described above. For AM modulation, the modulation signal must ride on a positive DC bias offset which sets a static (modulation off) modulation current. External circuitry for various schemes is further discussed in the Applications Information section.

Figure 3. Supply Current versus Supply Voltage

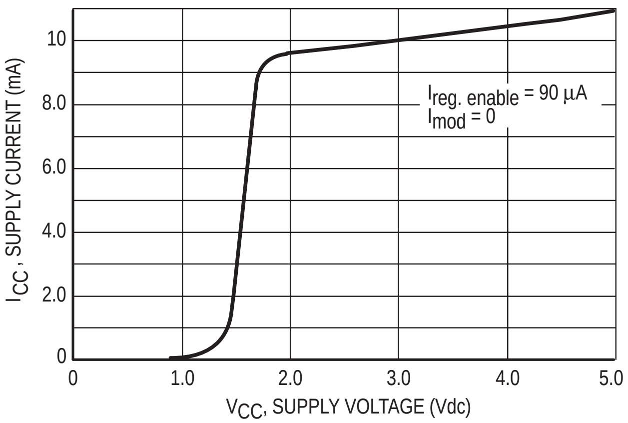


Figure 4. Supply Current versus Regulator Enable Current

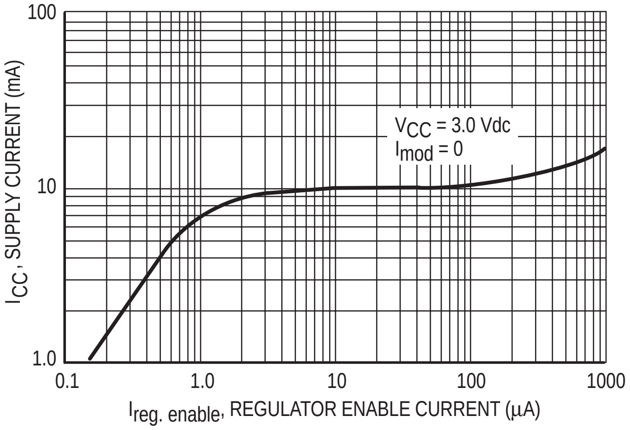


Figure 5. Change Oscillator Frequency versus Oscillator Control Current

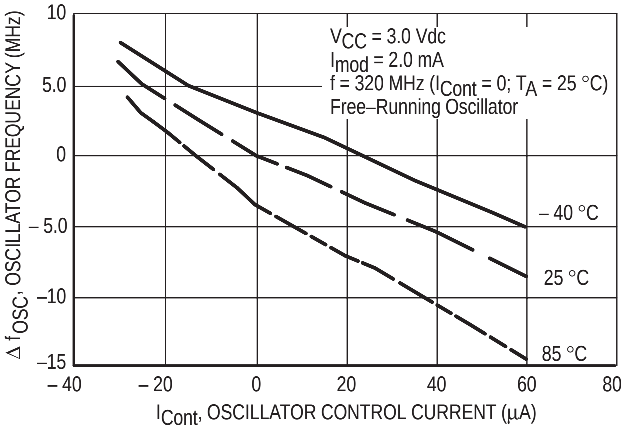


Figure 6. Change in Oscillator Frequency and Output Power versus Ambient Temperature

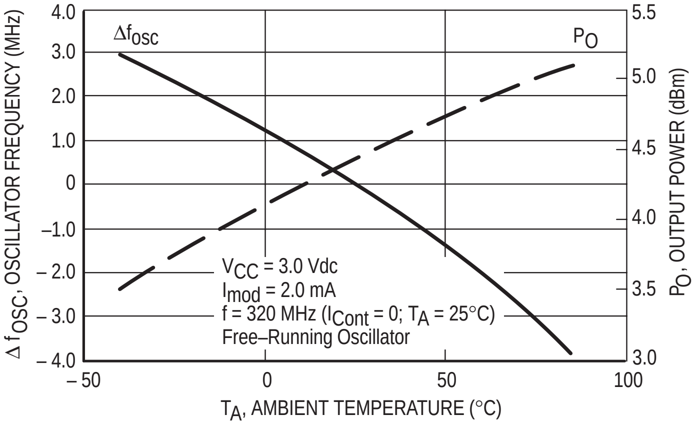


Figure 7. MC13175 Reference Oscillator Frequency versus Phase Detector Current

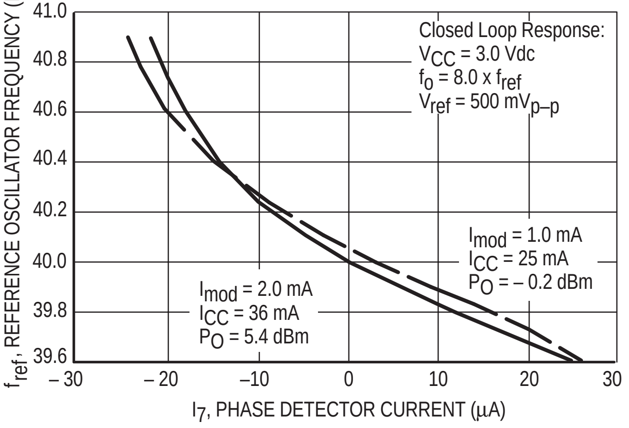


Figure 8. MC13176 Reference Oscillator Frequency versus Phase Detector Current

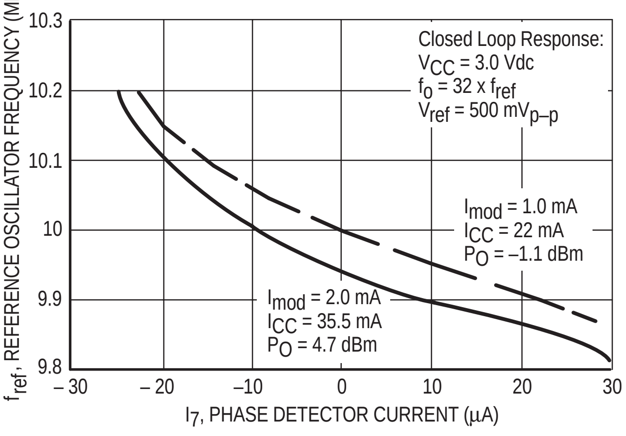


Figure 9. Change in Oscillator Frequency versus Oscillator Control Current

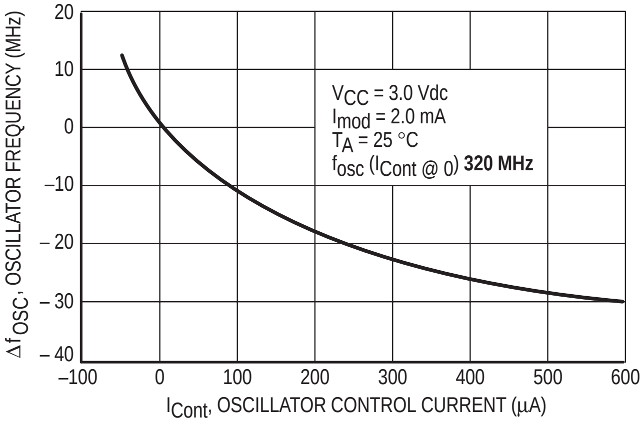
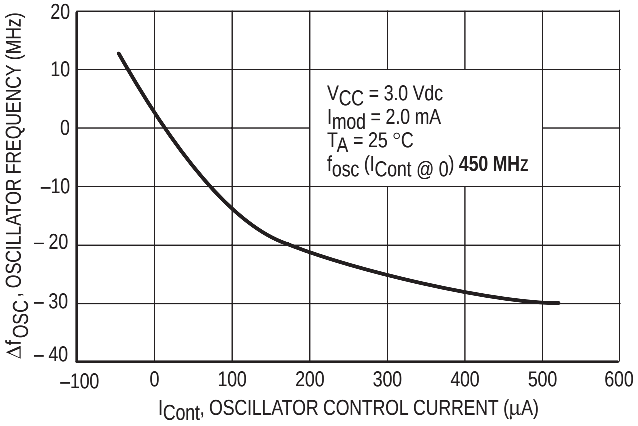


Figure 10. Change in Oscillator Frequency versus Oscillator Control Current



APPLICATIONS INFORMATION

Evaluation PC Board

The evaluation PCB, shown in Figures 26 and 27, is very versatile and is intended to be used across the entire useful frequency range of this device. The center section of the board provides an area for attaching all SMT components to the circuit side and radial leaded components to the component ground side of the PCB (see Figures 28 and 29). Additionally, the peripheral area surrounding the RF core provides pads to add supporting and interface circuitry as a particular application dictates. This evaluation board will be discussed and referenced in this section.

Current Controlled Oscillator (Pins 1 to 4)

It is critical to keep the interconnect leads from the CCO (Pins 1 and 4) to the external inductor symmetrical and equal in length. With a minimum inductor, the maximum free running frequency is greater than 1.0 GHz. Since this inductor will be small, it may be either a microstrip inductor, an air wound inductor or a tuneable RF coil. An air wound inductor may be tuned by spreading the windings, whereas tuneable RF coils are tuned by adjusting the position of an aluminum core in a threaded coilform. As the aluminum core coupling to the windings is increased, the inductance is decreased. The temperature coefficient using an aluminum core is better than a ferrite core. The UniCoil™ inductors made by Coilcraft may be obtained with aluminum cores (Part No. 51–129–169).

Ground (Pins 5, 10 and 15)

Ground Returns: It is best to take the grounds to a backside ground plane via plated through holes or eyelets at the pins. The application PCB layout implements this technique. Note that the grounds are located at or less than 100 mils from the devices pins.

Decoupling: Decoupling each ground pin to V_{CC} isolates each section of the device by reducing interaction between sections and by localizing circulating currents.

Loop Characteristics (Pins 6 and 7)

Figure 11 is the component block diagram of the MC1317XD PLL system where the loop characteristics are described by the gain constants. Access to individual components of this PLL system is limited, inasmuch as the loop is only pinned out at the phase detector output and the frequency control input for the CCO. However, this allows for characterization of the gain constants of these loop components. The gain constants K_p, K_o and K_n are well defined in the MC13175 and MC13176.

Phase Detector (Pin 7)

With the loop in lock, the difference frequency output of the phase detector is DC voltage that is a function of the phase difference. The sinusoidal type detector used in this IC has the following transfer characteristic:

$$I_e = A \text{ Sin } \theta_e$$

The gain factor of the phase detector, K_p (with the loop in lock) is specified as the ratio of DC output current, I_e to phase error, θ_e:

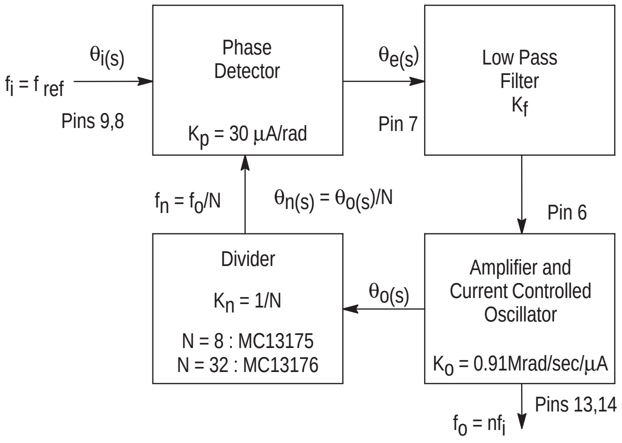
$K_p = I_e/\theta_e$ (Amps/radians)
$K_p = A \text{ Sin } \theta_e/\theta_e$
$\text{Sin } \theta_e \sim \theta_e$ for $\theta_e \leq 0.2$ radians;
thus, $K_p = A$ (Amps/radians)

Figures 7 and 8 show that the detector DC current is approximately 30 µA where the loop loses lock at $\theta_e = \pm \pi/2$ radians; therefore, K_p is 30 µA/radians.

Current Controlled Oscillator, CCO (Pin 6)

Figures 9 and 10 show the non–linear change in frequency of the oscillator over an extended range of control current for 320 and 450 MHz applications. K_o ranges from approximately 6.3×10^5 rad/sec/µA or 100 kHz/µA (Figure 9) to 8.8×10^5 rad/sec/µA or 140 kHz/µA (Figure 10) over a relatively linear response of control current (0 to 100 µA). The oscillator gain factor depends on the operating range of the control current (i.e., the slope is not constant). Included in the CCO gain factor is the internal amplifier which can sink and source at least 30 µA of input current from the phase detector. The internal circuitry at Pin 6 limits the CCO control current to 50 µA of source capability while its sink capability exceeds 200 µA as shown in Figures 9 and 10. Further information to follow shows how to use the full capabilities of the CCO by addition of an external loop amplifier and filter (see Figure 15). This additional circuitry yields at K_o = 0.145 MHz/µA or 9.1×10^5 rad/sec/µA.

Figure 11. Block Diagram of MC1317XD PLL



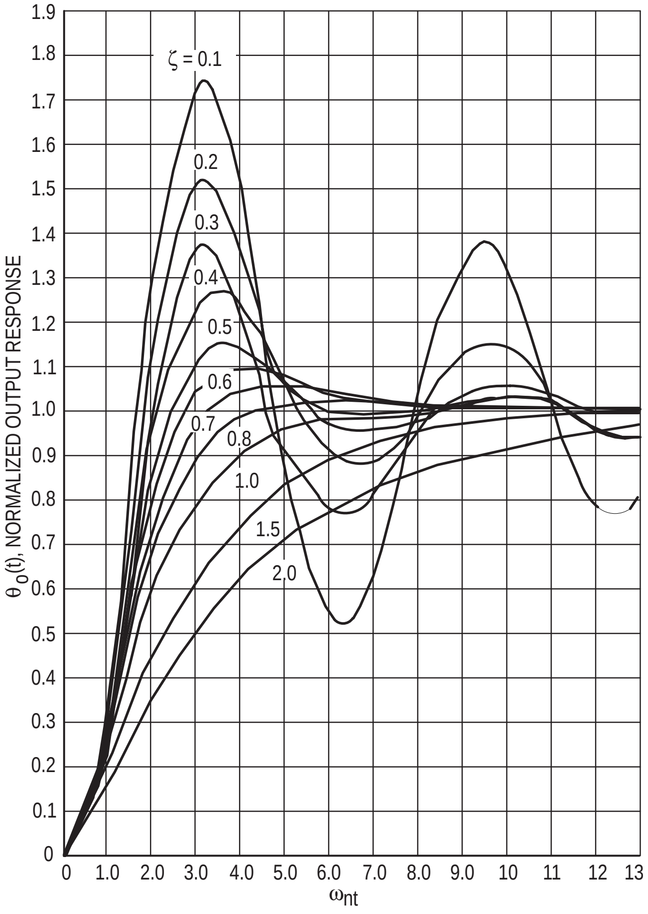
Where: K_p = Phase detector gain constant in µA/rad; K_p = 30 µA/rad
K_f = Filter transfer function
K_n = 1/N; N = 8 for the MC13175 and N = 32 for the MC13176
K_o = CCO gain constant in rad/sec/µA
K_o = 9.1 x 10^5 rad/sec/µA

Loop Filtering

The fundamental loop characteristics, such as capture range, loop bandwidth, lock–up time and transient response are controlled externally by loop filtering.

The natural frequency (ω_n) and damping factor (∂) are important in the transient response to a step input of phase or frequency. For a given ∂ and lock time, ω_n can be determined from the plot shown in Figure 12.

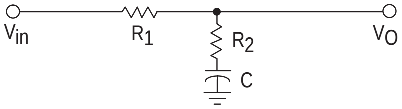
Figure 12. Type 2 Second Order Response



For ∂ = 0.707 and lock time = 1.0 ms;
then ω_n = 5.0/t = 5.0 krad/sec.

The loop filter may take the form of a simple low pass filter or a lag–lead filter which creates an additional pole at origin in the loop transfer function. This additional pole along with that of the CCO provides two pure integrators ($1/s^2$). In the lag–lead low pass network shown in Figure 13, the values of the low pass filtering parameters R_1, R_2 and C determine the loop constants ω_n and ∂. The equations $t_1 = R_1C$ and $t_2 = R_2C$ are related in the loop filter transfer functions $F(s) = 1 + t_2s/1 + (t_1 + t_2)s$.

Figure 13. Lag–Lead Low Pass Filter



The closed loop transfer function takes the form of a 2nd order low pass filter given by,

$$H(s) = K_vF(s)/s + K_vF(s)$$

From control theory, if the loop filter characteristic has F(0) = 1, the DC gain of the closed loop, K_v is defined as,

$$K_v = K_pK_oK_n$$

and the transfer function has a natural frequency,

$$\omega_n = (K_v/t_1 + t_2)^{1/2}$$

and a damping factor,

$$\partial = (\omega_n/2)\,(t_2 + 1/K_v)$$

Rewriting the above equations and solving for the MC13176 with ∂ = 0.707 and ω_n = 5.0 k rad/sec:

$$K_v = K_pK_oK_n = (30)\,(0.91 \times 10^6)\,(1/32) = 0.853 \times 10^6$$
$$t_1 + t_2 = K_v/\omega_n2 = 0.853 \times 10^6/(25 \times 106) = 34.1 \text{ ms}$$
$$t_2 = 2\partial/\omega_n = (2)\,(0.707)/(5 \times 10^3) = 0.283 \text{ ms}$$
$$t_1 = (K_v/\omega_n2) - t_2 = (34.1 - 0.283) = 33.8 \text{ ms}$$

For $C = 0.47\ \mu$;

then, $R_1 = t_1/C = 33.8 \times 10^{-3}/0.47 \times 10^{-6} = 72\ k$

dthus, $R_2 = t_2/C = 0.283 \times 10^{-3}/0.47 \times 10^{-6} = 0.60\ k$

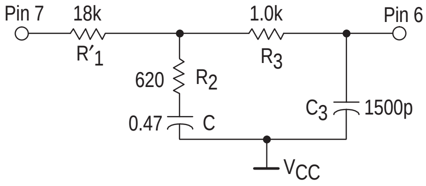
In the above example, the following standard value components are used,

$$C = 0.47\ \mu;\ R_2 = 620 \text{ and } R'_1 = 72\ k - 53\ k \sim 18\ k$$

(R'_1 is defined as R_1 – 53 k, the output impedance of the phase detector.)

Since the output of the phase detector is high impedance (~50 k) and serves as a current source, and the input to the frequency control, Pin 6 is low impedance (impedance of the two diode to ground is approximately 500 Ω), it is imperative that the second order low pass filter design above be modified. In order to minimize loading of the R_2C shunt network, a higher impedance must be established to Pin 6. A simple solution is achieved by adding a low pass network between the passive second order network and the input to Pin 6. This helps to minimize the loading effects on the second order low pass while further suppressing the sideband spurs of the crystal oscillator. A low pass filter with R_3 = 1.0 k and C_2 = 1500 p has a corner frequency (f_c) of 106 kHz; the reference sideband spurs are down greater than – 60 dBc.

Figure 14. Modified Low Pass Loop Filter



Hold–In Range

The hold–in range, also called the lock range, tracking range and synchronization range, is the ability of the CCO frequency, f_o to track the input reference signal, $f_{ref} \bullet N$ as it gradually shifted away from the free running frequency, f_f. Assuming that the CCO is capable of sufficient frequency deviation and that the internal loop amplifier and filter are not overdriven, the CCO will track until the phase error, θ_e approaches $\pm\pi/2$ radians. Figures 5 through 8 are a direct measurement of the hold–in range (i.e. $\Delta f_{ref} \times N = \pm\Delta f_H \times 2\pi$). Since $\sin \theta_e$ cannot exceed ±1.0, as θ_e approaches $\pm\pi/2$ the hold–in range is equal to the DC loop gain, $K_v \times N$.

$$\pm\Delta\omega_H = \pm K_v \times N$$

$$\text{where, } K_v = K_p K_o K_n.$$

In the above example,

$$\pm\Delta\omega_H = \pm\ 27.3 \text{ Mrad/sec}$$
$$\pm\Delta f_H = \pm\ 4.35 \text{ MHz}$$

Extended Hold–in Range

The hold–in range of about 3.4% could cause problems over temperature in cases where the free–running oscillator drifts more than 2 to 3% because of relatively high temperature coefficients of the ferrite tuned CCO inductor. This problem might worsen for lower frequency applications where the external tuning coil is large compared to internal capacitance at Pins 1 and 4. To improve hold–in range performance, it is apparent that the gain factors involved must be carefully considered.

K_n = is either 1/8 in the MC13175 or 1/32 in the MC13176.

K_p = is fixed internally and cannot be altered.

K_o = Figures 9 and 10 suggest that there is capability of greater control range with more current swing. However, this swing must be symmetrical about the center of the dynamic response. The suggested zero current operating point for ±100 µA swing of the CCO is at about + 70 µA offset point.

Ka = External loop amplification will be necessary since the phase detector only supplies ± 30 µA.

In the design example in Figure 15, an external resistor (R_5) of 15 k to V_{CC} (3.0 Vdc) provides approximately 100 µA of current boost to supplement the existing 50 µA internal source current. R_4 (1.0 k) is selected for approximately 0.1 Vdc across it with 100 µA. R_1, R_2 and R_3 are selected to set the potential at Pin 7 and the base of 2N4402 at approximately 0.9 Vdc and the emitter at 1.55 Vdc when error current to Pin 6 is approximately zero µA. C_1 is chosen to reduce the level of the crystal sidebands.

Figure 15. External Loop Amplifier

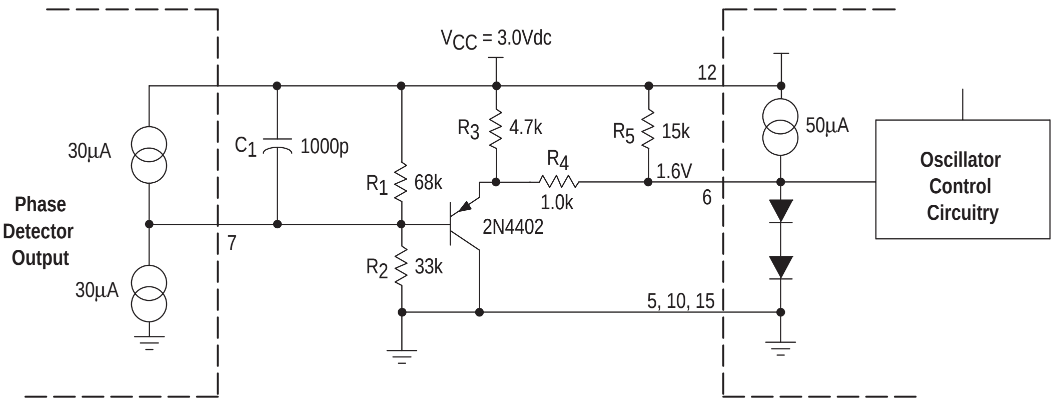
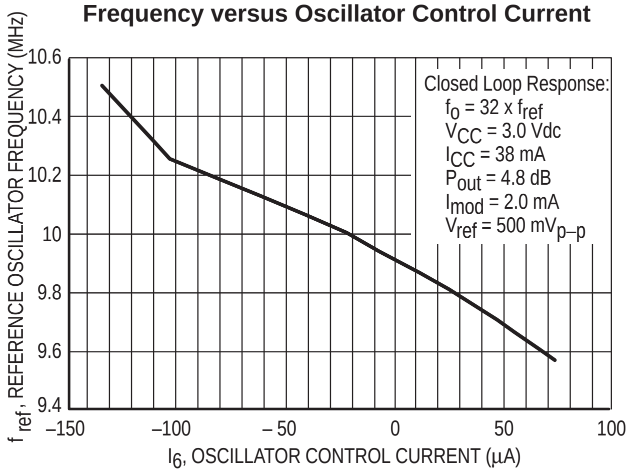


Figure 16 shows the improved hold–in range of the loop. The Δf_{ref} is moved 950 kHz with over 200 µA swing of control current for an improved hold–in range of ±15.2 MHz or ± 95.46 Mrad/sec.

Figure 16. MC13176 Reference Oscillator Frequency versus Oscillator Control Current



Lock–in Range/Capture Range

If a signal is applied to the loop not equal to free running frequency, f_f, then the loop will capture or lock–in the signal by making $f_s = f_o$ (i.e. if the initial frequency difference is not too great). The lock–in range can be expressed as $\Delta\omega_L \sim \pm 2\partial\omega_n$

FM Modulation

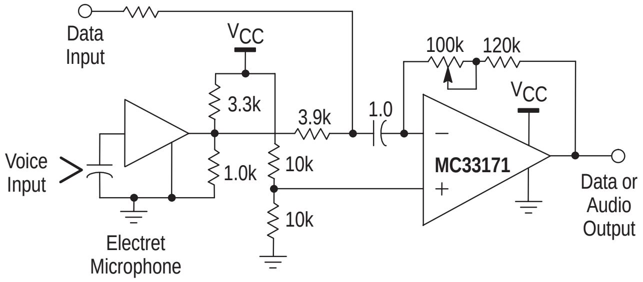
Noise external to the loop (phase detector input) is minimized by narrowing the bandwidth. This noise is minimal in a PLL system since the reference frequency is usually derived from a crystal oscillator. FM can be achieved by applying a modulation current superimposed on the control current of the CCO. The loop bandwidth must be narrow enough to prevent the loop from responding to the modulation frequency components, thus, allowing the CCO to deviate in frequency. The loop bandwidth is related to the natural frequency ω_n. In the lag–lead design example where the natural frequency, ω_n = 5.0 krad/sec and a damping factor, ∂ = 0.707, the loop bandwidth = 1.64 kHz. Characterization data of the closed loop responses for both the MC13175 and MC13176 at 320 MHz (Figures 7 and 8, respectively) show satisfactory performance using only a simple low–pass loop filter network. The loop filter response is strongly influenced by the high output impedance of the push–pull current output of the phase detector.

f_c = 0.159/RC;
For R = 1.0 k + R_7 (R_7 = 53 k) and C = 390 pF
f_c = 7.55 kHz or ω_c = 47 krad/sec

The application example in Figure 17a of a 320 MHz FM transmitter demonstrates the FM capabilities of the IC. A high value series resistor (100 k) to Pin 6 sets up the current source to drive the modulation section of the chip. Its value is dependent on the peak to peak level of the encoding data and the maximum desired frequency deviation. The data input is AC coupled with a large coupling capacitor which is selected for the modulating frequency. The component placements on the circuit side and ground side of the PC board are shown in Figures 28 and 29, respectively. Figure 18a illustrates the input data of a 10 kHz modulating signal at 1.6 Vp–p. Figures 18b and 18c depict the deviation and resulting modulation spectrum showing the carrier null at – 40 dBc. Figure 18d shows the unmodulated carrier power output at 3.5 dBm for V_{CC} = 3.0 Vdc.

For voice applications using a dynamic or an electret microphone, an op amp is used to amplify the microphone's low level output. The microphone amplifier circuit is shown in Figure 19. Figure 17b shows an application example for NBFM audio or direct FSK in which the reference crystal oscillator is modulated.

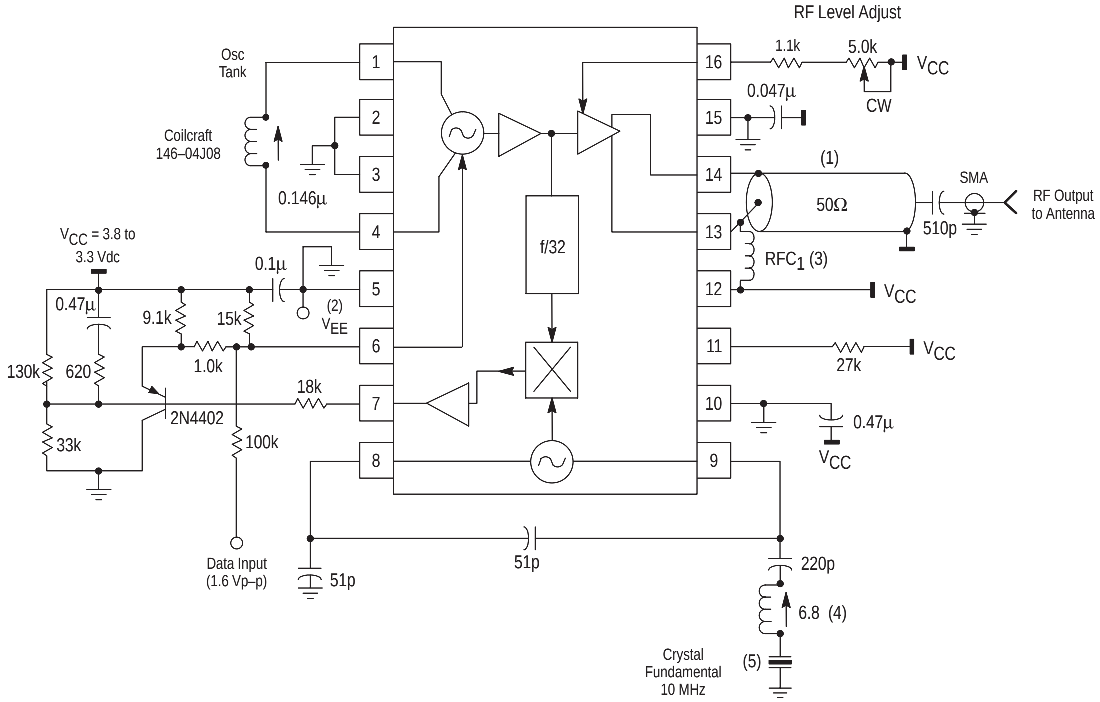
Figure 19. Microphone Amplifier



Local Oscillator Application

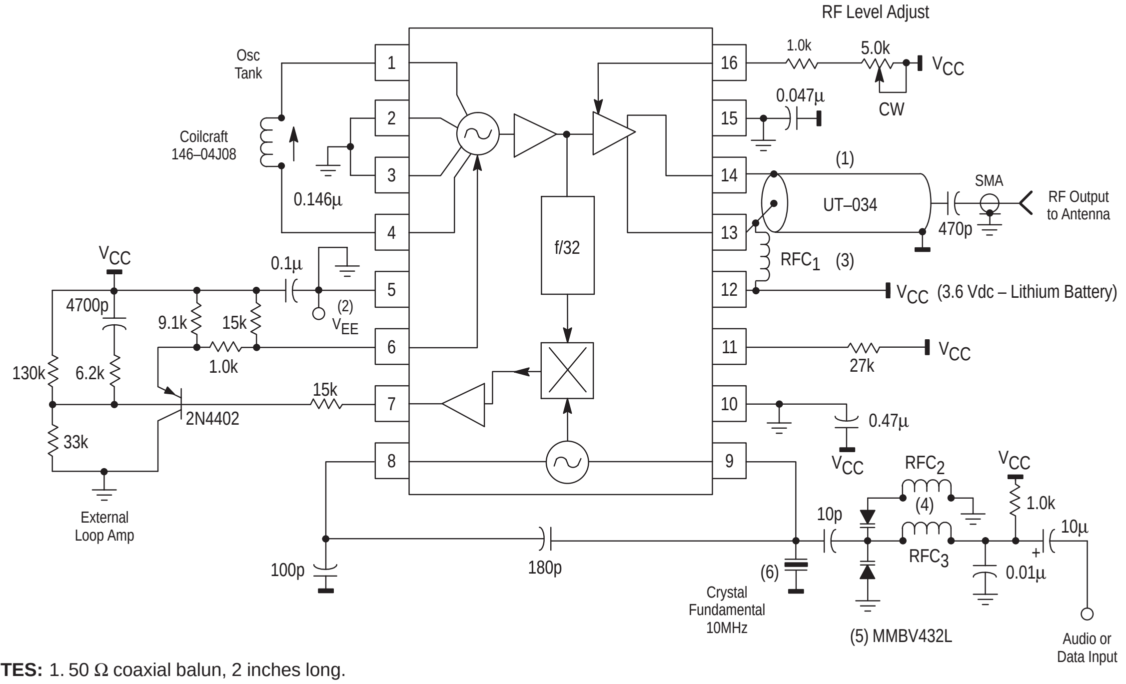
To reduce internal loop noise, a relatively wide loop bandwidth is needed so that the loop tracks out or cancels the noise. This is emphasized to reduce inherent CCO and divider noise or noise produced by mechanical shock and environmental vibrations. In a local oscillator application the CCO and divider noise should be reduced by proper selection of the natural frequency of the loop. Additional low pass filtering of the output will likely be necessary to reduce the crystal sideband spurs to a minimal level.

Figure 17a. 320 MHz MC13176D FM Transmitter



NOTES:
1. 50 Ω coaxial balun, 2 inches long.
2. Pins 5, 10 and 15 are grounds and connnected to V_{EE} which is the component's side ground plane. These pins must be decoupled to V_{CC}; decoupling capacitors should be placed as close as possible to the pins.
3. RFC_1 is 180 nH Coilcraft surface mount inductor or 190 nH Coilcraft 146–05J08.
4. Recommended source is a Coilcraft "slot seven" 7.0 mm tuneable inductor, part #7M3–682.
5. The crystal is a parallel resonant, fundamental mode calibrated with 32 pF load capacitance.

Figure 17b. 320 MHz NBFM Transmitter



NOTES:
1. 50 Ω coaxial balun, 2 inches long.
2. Pins 5, 10 and 15 are grounds and connnected to V_{EE} which is the component's side ground plane. These pins must be decoupled to V_{CC}; decoupling capacitors should be placed as close as possible to the pins.
3. RFC_1 is 180 nH Coilcraft surface mount inductor.
4. RFC_2 and RFC_3 are high impedance crystal frequency of 10 MHz; 8.2 µH molded inductor gives XL > 1000 Ω..
5. A single varactor like the MV2105 may be used whereby RFC_2 is not needed.
6. The crystal is a parallel resonant, fundamental mode calibrated with 32 pF load capacitance.

Figure 18a. Input Data Waveform

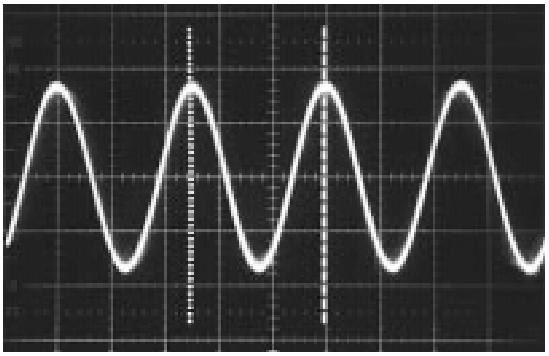
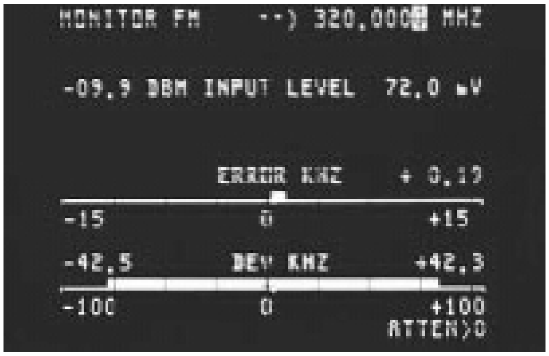


Figure 18b. Frequency Deviation



MONITOR FM --) 320.000█ MHZ

-09.9 DBM INPUT LEVEL 72.0 mV

ERROR KHZ + 0.13

-15 0 +15

-42.5 DEV KHZ +42.3

-100 0 +100

ATTEN>0

Figure 18c. Modulation Spectrum

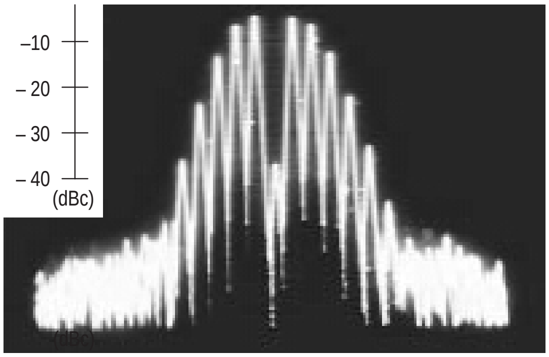
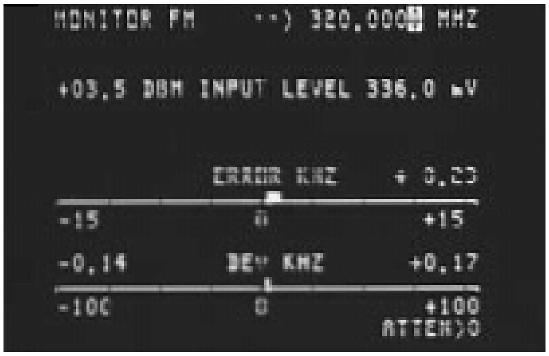


Figure 18d. Unmodulated Carrier



MONITOR FM --) 320.000█ MHZ

+03.5 DBM INPUT LEVEL 336.0 mV

ERROR KHZ + 0.23

-15 0 +15

-0.14 DEV KHZ +0.17

-100 0 +100

ATTEN>0

Reference Crystal Oscillator (Pins 8 and 9)

Selection of Proper Crystal: A crystal can operate in a number of mechanical modes. The lowest resonant frequency mode is its fundamental while higher order modes are called overtones. At each mechanical resonance, a crystal behaves like a RLC series–tuned circuit having a large inductor and a high Q. The inductor L_S is series resonance with a dynamic capacitor, C_S determined by the elasticity of the crystal lattice and a series resistance R_S, which accounts for the power dissipated in heating the crystal. This series RLC circuit is in parallel with a static capacitance, C_p which is created by the crystal block and by the metal plates and leads that make contact with it.

Figure 20 is the equivalent circuit for a crystal in a single resonant mode. It is assumed that other modes of resonance are so far off frequency that their effects are negligible.

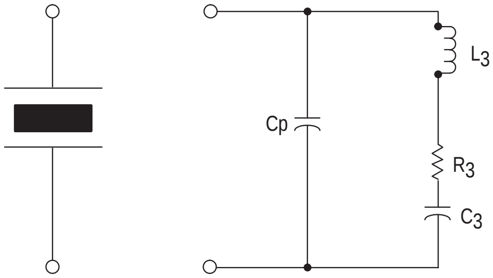
Series resonant frequency, f_S is given by;

$$f_S = 1/2\pi(L_S C_S)^{1/2}$$

and parallel resonant frequency, f_p is given by;

$$f_p = f_S(1 + C_S/C_p)^{1/2}$$

Figure 20. Crystal Equivalent Circuit



the frequency separation at resonance is given by;

$$\Delta f = f_p – f_S = f_S[1 – (1 + C_S/C_p)^{1/2}]$$

Usually f_p is less than 1% higher than f_S, and a crystal exhibits an extremely wide variation of the reactance with frequency between f_p and f_S. A crystal oscillator circuit is very stable with frequency. This high rate of change of impedance with frequency stabilizes the oscillator, because any significant change in oscillator frequency will cause a large phase shift in the feedback loop keeping the oscillator on frequency.

Manufacturers specify crystal for either series or parallel resonant operation. The frequency for the parallel mode is calibrated with a specified shunt capacitance called a “load capacitance.” The most common value is 30 to 32 pF. If the load capacitance is placed in series with the crystal, the equivalent circuit will be series resonance at the specified parallel–resonant frequency. Frequencies up to 20 MHz use parallel resonant crystal operating in the fundamental mode, while above 20 MHz to about 60 MHz, a series resonant crystal specified and calibrated for operation in the overtone mode is used.

Application Examples

Two types of crystal oscillator circuits are used in the applications circuits: 1) fundamental mode common emitter Colpitts (Figures 1, 17a, 17b, and 21), and 2) third overtone impedance inversion Colpitts (also Figures 1 and 21).

The fundamental mode common emitter Colpitts uses a parallel resonant crystal calibrated with a 32 pf load capacitance. The capacitance values are chosen to provide excellent frequency stability and output power of > 500 mVp–p at Pin 9. In Figures 1 and 21, the fundamental mode reference oscillator is fixed tuned relying on the repeatability of the crystal and passive network to maintain the frequency, while in the circuit shown in Figure 17, the oscillator frequency can be adjusted with the variable inductor for the precise operating frequency.

The third overtone impedance inversion Colpitts uses a series resonance crystal with a 25 ppm tolerance. In the application examples (Figures 1 and 21), the reference oscillator operates with the third overtone crystal at 40.0000 MHz. Thus, the MC13175 is operated at 320 MHz (f_o/8 = crystal; 320/8 = 40.0000 MHz. The resistor across the crystal ensures that the crystal will operate in the series resonant mode. A tuneable inductor is used to adjust the oscillation frequency; it forms a parallel resonant circuit with the series and parallel combination of the external capacitors forming the divider and feedback network and the base–emitter capacitance of the device. If the crystal is shorted, the reference oscillator should free–run at the frequency dictated by the parallel resonant LC network.

The reference oscillator can be operated as high as 60 MHz with a third overtone crystal. Therefore, it is possible to use the MC13175 up to at least 480 MHz and the MC13176 up to 950 MHz (based on the maximum capability of the divider network).

Enable (Pin 11)

The enabling resistor at Pin 11 is calculated by:

$$R_{eg.\ enable} = V_{CC} - 1.0\ Vdc/I_{reg.\ enable}$$

From Figure 4, $I_{reg.\ enable}$ is chosen to be 75 µA. So, for a V_{CC} = 3.0 Vdc $R_{reg.\ enable}$ = 26.6 kΩ, a standard value 27 kΩ resistor is adequate.

Layout Considerations

Supply (Pin 12): In the PCB layout, the V_{CC} trace must be kept as wide as possible to minimize inductive reactance along the trace; it is best that V_{CC} (RF ground) completely fills around the surface mounted components and interconnect traces on the circuit side of the board. This technique is demonstrated in the evaluation PC board.

Battery/Selection/Lithium Types

The device may be operated from a 3.0 V lithium battery. Selection of a suitable battery is important. Because one of the major problems for long life battery powered equipment is oxidation of the battery terminals, a battery mounted in a clip–in socket is not advised. The battery leads or contact post should be isolated from the air to eliminate oxide build–up. The battery should have PC board mounting tabs which can be soldered to the PCB. Consideration should be given for the peak current capability of the battery. Lithium batteries have current handling capabilities based on the composition of the lithium compound, construction and the battery size. A 1300 mA/hr rating can be achieved in the cylindrical cell battery. The Rayovac CR2/3A lithium–manganese dioxide battery is a crimp sealed, spiral wound 3.0 Vdc, 1300 mA/hr cylindrical cell with PC board mounting tabs. It is an excellent choice based on capacity and size (1.358″ long by 0.665″ in diameter).

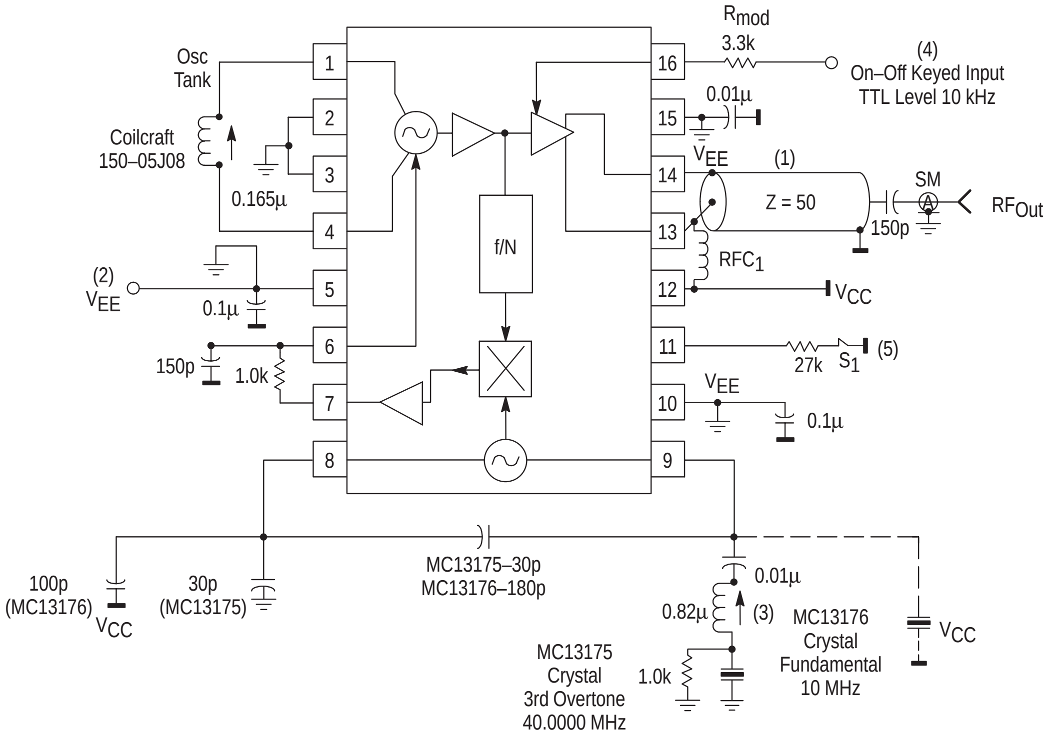
Differential Output (Pins 13, 14)

The availability of micro–coaxial cable and small baluns in surface mount and radial–leaded components allows for simple interface to the output ports. A loop antenna may be directly connected with bias via RFC or 50 Ω resistors. Antenna configuration will vary depending on the space available and the frequency of operation.

AM Modulation (Pin 16)

Amplitude Shift Key: The MC13175 and MC13176 are designed to accommodate Amplitude Shift Keying (ASK). ASK modulation is a form of digital modulation corresponding to AM. The amplitude of the carrier is switched between two or more values in response to the PCM code. For the binary case, the usual choice is On–Off Keying (often abbreviated OOK). The resultant amplitude modulated waveform consists of RF pulses called marks, representing binary 1 and spaces representing binary 0.

Figure 21. ASK 320 MHz Application Circuit



NOTES: 1. 50 Ω coaxial balun, 1/10 wavelength line (1.5″) provides the best match to a 50 Ω load.

2. Pins 5, 10 and 15 are ground and connnected to V_{EE} which is the component/DC ground plane side of PCB. These pins must be decoupled to V_{CC}; decoupling capacitors should be placed as close as possible to the pins.

3. The crystal oscillator circuit may be adjusted for frequency with the variable inductor (MC13175); 1.0 k resistor shunting the crystal prevents it from oscillating in the fundamental mode. Recommended source is Coilcraft “slot seven” 7.0 mm tuneable inductor, part #7M3–821.

4. The On–Off keyed signal turns the output of the transmitter off and on with TTL level pulses through R_{mod} at Pin 16. The “On” power and I_{CC} is set by the resistor which sets I_{mod} = VTTL – 0.8 / R_{mod}. (see Figure 23).

5. S1 simulates an enable gate pulse from a microprocessor which will enable the transmitter. (see Figure 4 to determine precise value of the enabling resistor based on the potential of the gate pulse and the desired enable.)

Figure 21 shows a typical application in which the output power has been reduced for linearity and current drain. The current draw on the device is 16 mA I_{CC} (average) and – 22.5 dBm (average power output) using a 10 kHz modulating rate for the on–off keying. This equates to 20 mA and – 2.3 dBm “On”, 13 mA and – 41 dBm “Off”. In Figure 22a, the device’s modulating waveform and encoded carrier are displayed. The crystal oscillator enable time is needed to set the acquisition timing. It takes typically 4.0 msec to reach full magnitude of the oscillator waveform (see Figure 22b, Oscillator Waveform, at Pin 8). A square waveform of 3.0 V peak with a period that is greater than the oscillator enable time is applied to the Enable (Pin 11).

Figure 22a. ASK Input Waveform and Modulated Carrier

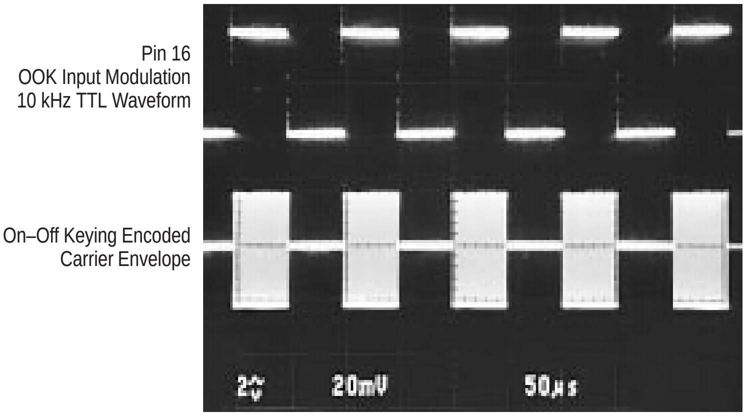


Figure 22b. Oscillator Enable Time, T_{enable}

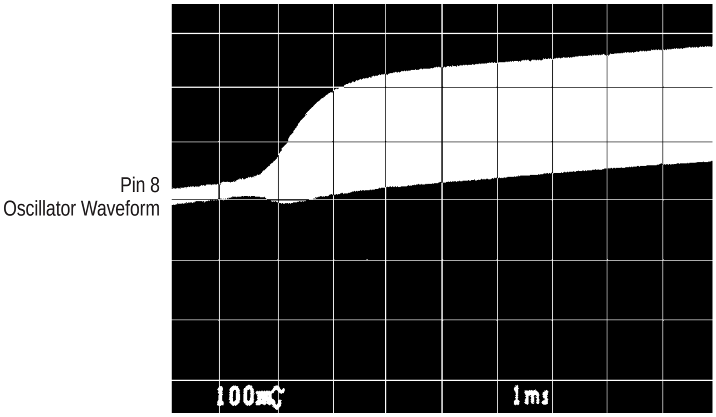
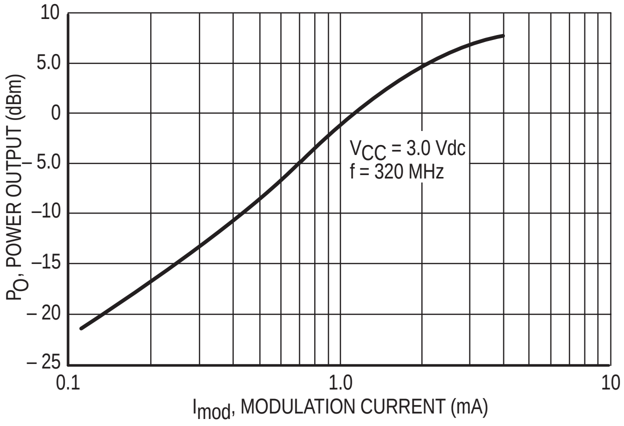


Figure 23. Power Output versus Modulation Current



Analog AM

In analog AM applications, the output amplifier’s linearity must be carefully considered. Figure 23 is a plot of Power Output versus Modulation Current at 320 MHz, 3.0 Vdc. In order to achieve a linear encoding of the modulating sinusoidal waveform on the carrier, the modulating signal must amplitude modulate the carrier in the linear portion of its power output response. When using a sinewave modulating signal, the signal rides on a positive DC offset called V_{mod} which sets a static (modulation off) modulation current, I_{mod}. I_{mod} controls the power output of the IC. As the modulating signal moves around this static bias point the modulating current varies causing power output to vary or to be AM modulated. When the IC is operated at modulation current levels greater than 2.0 mAdc the differential output stage starts to saturate.

In the design example, shown in Figure 24, the operating point is selected as a tradeoff between average power output and quality of the AM.

For V_{CC} = 3.0 Vdc; I_{CC} = 18.5 mA and I_{mod} = 0.5 mAdc and a static DC offset of 1.04 Vdc, the circuit shown in Figure 24 completes the design. Figures 25a, 25b and 25c show the results of – 6.9 dBm output power and 100% modulation by the 10 kHz and 1.0 MHz modulating sinewave signals. The amplitude of the input signals is approximately 800 mVp–p.

Where R_{mod} = (V_{CC} – 1.04 Vdc)/0.5 mA = 3.92 k, use a standard value resistor of 3.9 k.

Figure 24. Analog AM Transmitter

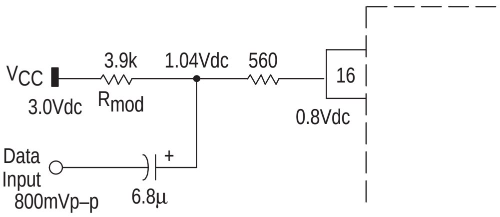
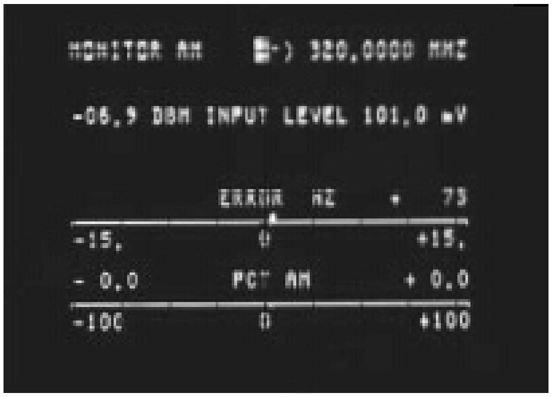


Figure 25a. Power Output of Unmodulated Carrier



```
MONITOR AM    ▇-) 320.0000 MHZ

-06.9 DBM INPUT LEVEL 101.0 mV

              ERROR  HZ      +   73
-15.          0                +15.
- 0.0         PCT AM          + 0.0
-100          0                +100
```

Figure 25b. Input Signal and AM Modulated
Carrier for f_{mod} = 10 kHz

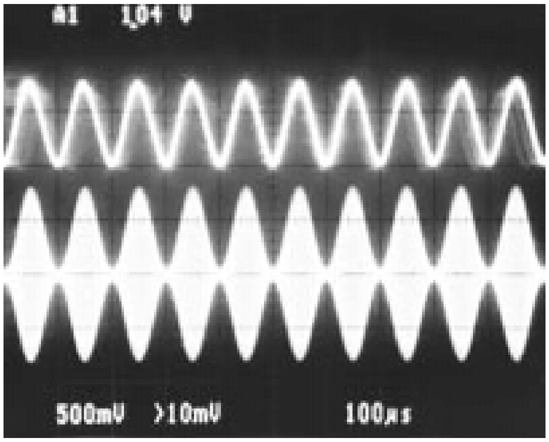


Figure 25c. Input Signal and AM Modulated
Carrier for f_{mod} = 1.0 MHz

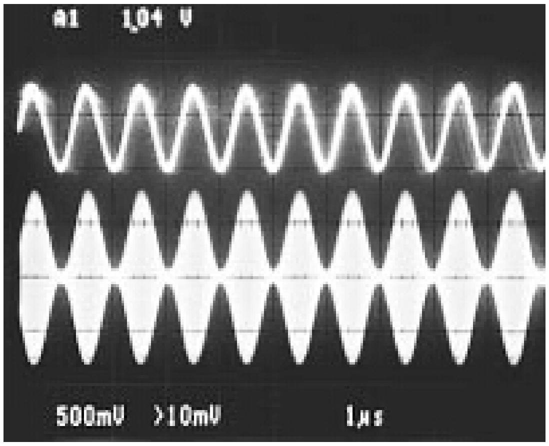


Figure 26. Circuit Side View of MC1317XD

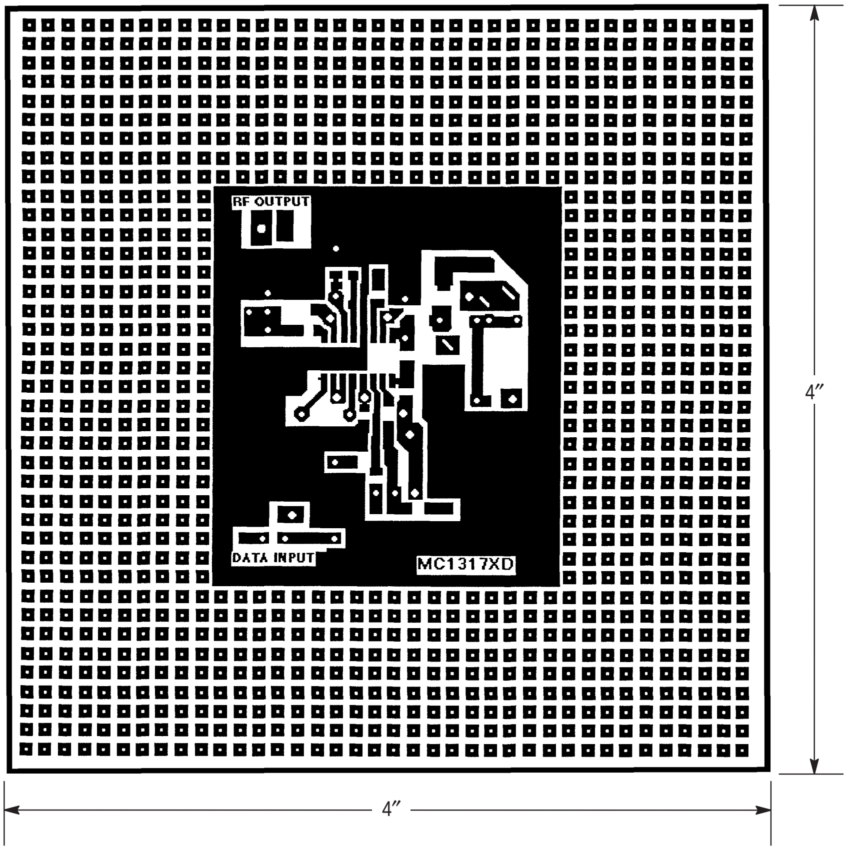


Figure 27. Ground Side View

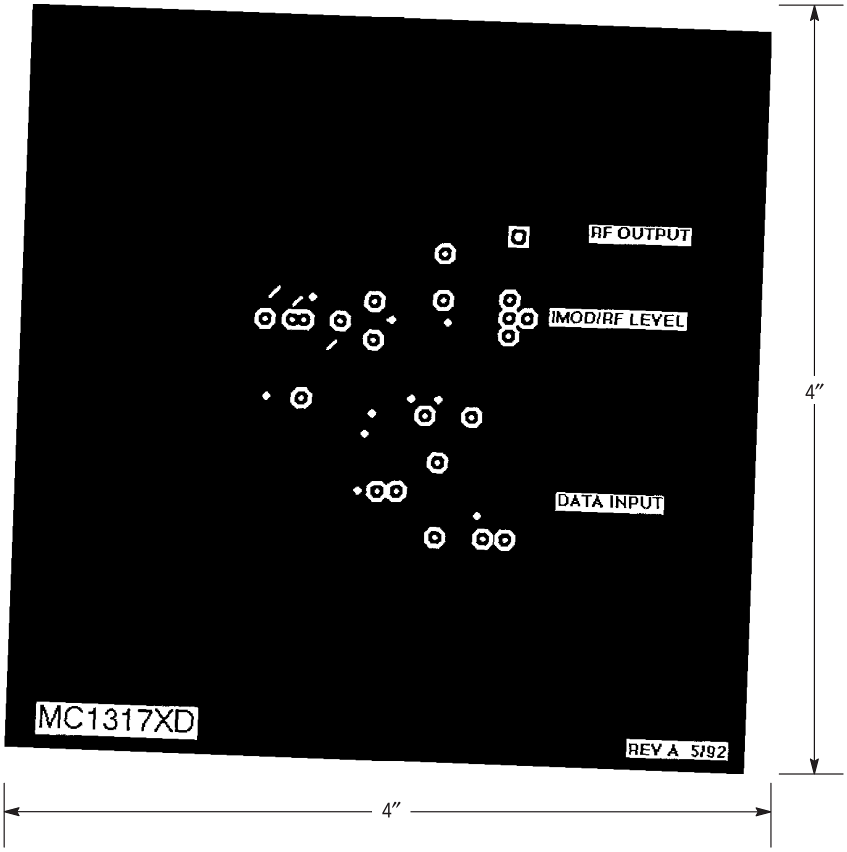


Figure 28. Surface Mounted Components Placement
(on Circuit Side)

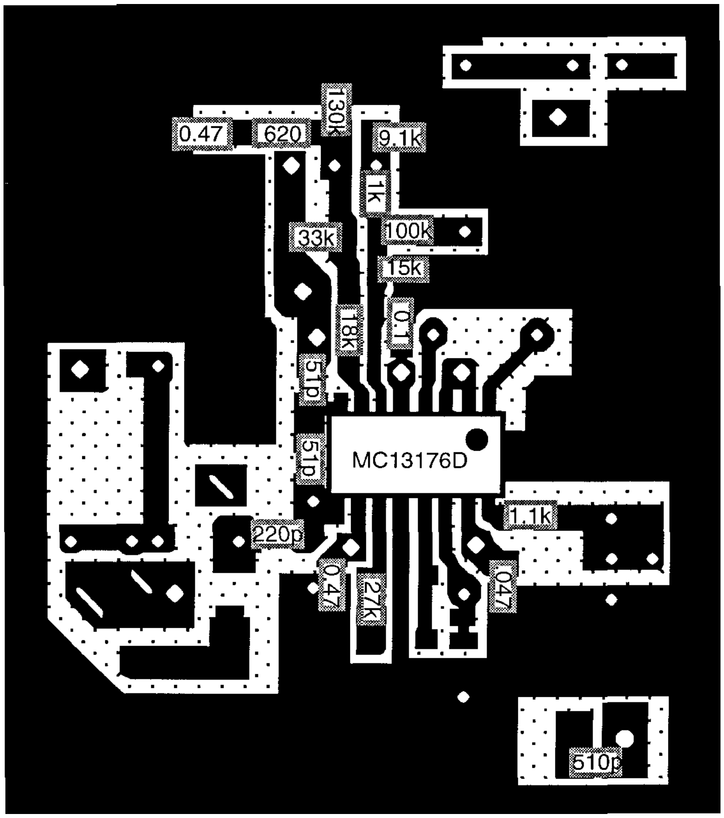
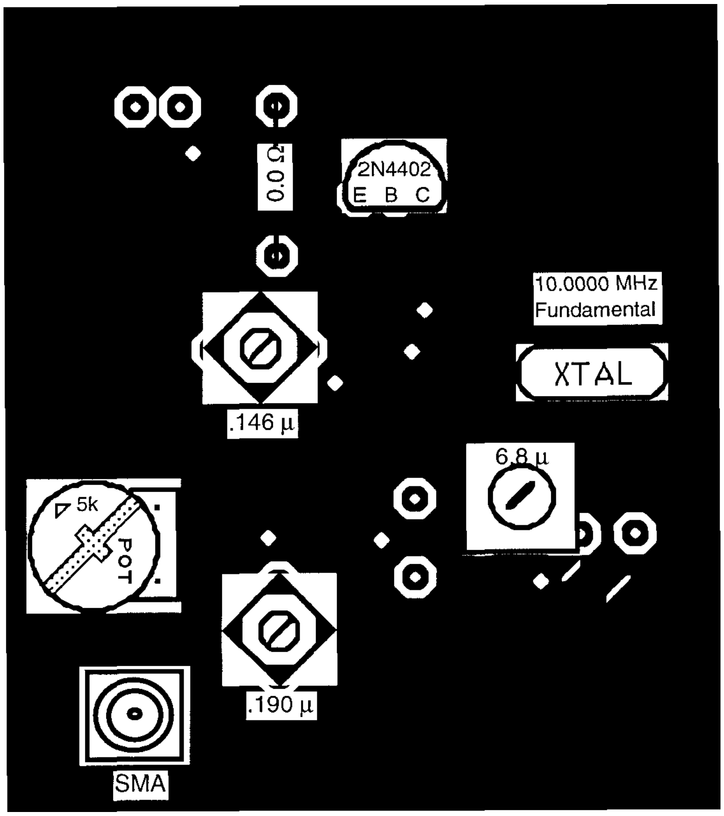


Figure 29. Radial Leaded Components Placement
(on Ground Side)



Addendum
An Introduction to Motorola RF Communications IC Applications

In Brief . . .

The RF devices described in Chapter 8 are targeted for the consumer communications market. In addition, most of these parts are capable of superior performance in professional and industrial applications. These devices represent the latest technology in cost effective RF and audio subsystems for cordless telephones (CT-1), RF LANs, land mobile radio, scanners, cellular telephones, remote control spread spectrum, and amateur radio. The purpose of this addendum is to help the user explore all the opportunities presented by this growing family of wireless communications ICs from Motorola Analog.

Page

REGULATORY ISSUES

Each country has its own specific set of regulations regarding radio frequency systems and equipment built and sold within its jurisdiction. These regulations are strongly applicable to transmitting devices. The rules are based on both local needs and international treaties. The regulations are established to provide maximum utilization of the limited available radio spectrum. Motorola strongly recommends that you, the user of these communication ICs, obtain the applicable regulations and abide by them.

In the United States, the regulations of the Federal Communications Commission (F.C.C.) are published in the Code of Federal Regulations (CFR), Title 47, Parts 0 through 99. In the U.S. most of the consumer applications fall under CFR 47, Part 15, covering nonlicensed intentional radiators, or Part 68 which covers public network interconnections. CFR 47 may be obtained at most libraries (in the reference section), or from the U.S. Government Printing Office. You may call their office at (213) 894-5841, or (202) 274-2054 for price and availability. In addition, private contractors such as the Rules Service Company, (301) 424-9402 can provide both the CFR data and an automatic update service. In the U.S., further information is available from the FCC field organization.

For the address and telephone number of the nearest office, contact:

FCC CONSUMER OFFICE AND
SMALL BUSINESS DIVISION
1919 M STREET WEST
WASHINGTON, D.C. 20554
(202) 632-7000

In other countries, the Ministry of Posts or Telecommunications should be contacted. *Motorola Semiconductor does not warrant that the applications shown in this data book meet all the conditions prescribed by government regulations.*

INDUSTRY STANDARDS

Throughout the world the telecommunications industry has established working standards committees to ensure equipment compatibility by setting minimum standards. These standards also help make the best use of the available radio spectrum. In the U.S., the Electronic Industries Association (E.I.A.) has developed a series of these recommended standards which have become the defacto global guidelines.

The following EIA Standards apply to Frequency Modulation (FM) systems.

EIA/TIA-204C	FM/PM RECEIVER STANDARDS
EIA/TIA-152B	FM/PM TRANSMITTER STANDARDS
EIA/TIA-316B	TEST CONDITIONS, PORTABLE PERSONAL RADIO

For additional information and pricing, contact the E.I.A. at the following address:

ELECTRONIC INDUSTRIES ASSOCIATION
ENGINEERING DEPARTMENT
2001 EYE STREET N.W.
WASHINGTON, D.C. 20006
(202) 457-4900

COMMUNICATIONS SYSTEMS

For the most part, the devices described in Chapter 8 use frequency modulation (FM) for both analog voice and data. FM is generally considered the simplest and most cost efficient type of modulation today. FM offers excellent: noise rejection; good sensitivity; reduction of interference due to the FM capture effect; simple circuitry; and an array of test equipment, most of which has spun-off the land mobile market. Direct digital transmission may also be accomplished using Frequency Shift Keying (FSK) or Amplitude Shift Keying (ASK).

The devices shown in Chapter 8 are designed to operate at frequencies below 1.0 GHz (1000 MHz). Today, that frequency range offers the best compromise among performance, complexity and cost. Over the next decade there will be an increasing movement to 1.0 to 3.0 GHz, as the demand for more complex personal communications systems comes on-line. Motorola will add products to its portfolio as these microwave applications become better defined.

Several reference books on Communications Theory and Design are listed below. These books are generally available at major public and university libraries.

THE RADIO AMATEUR'S HANDBOOK, American Radio Relay League, Newington, CT.

MICROWAVE THEORY AND APPLICATIONS, Steven F. Adam, Hewlett Packard, Prentice Hall.

SOLID STATE RADIO ENGINEERING, Herbert L. Krauss, Charles W. Bosdan, F.H. Raab, Wiley 1980.*R*

F CIRCUIT DESIGN, Chris Bowick, Howard Sams & Co., 1982.

INTRODUCTION TO COMMUNICATIONS SYSTEMS, Ferrel Stremler, Addison Wesley.

ARRL ANTENNA HANDBOOK, American Radio Relay League, Newington, CT.

STANDARD RADIO COMMUNICATIONS MANUAL, R.H. Kinley, CET, Prentice Hall, 1985.

In addition, you may find very timely design and component information in the following magazines:

R.F. DESIGN, Cardiff Publishing (708) 647-0756.
MICROWAVES AND RF, Penton Publishing (216) 696-7000.

PASSIVE COMPONENTS

The availability of passive components; coils, filters, crystals, capacitors, resonators, resistors, etc., is often a larger problem than finding the RF or analog IC to meet a designer's needs. The Motorola applications engineering team considers this a key issue when developing the circuits shown in our data sheets. Analog Applications has worked with many suppliers to develop practical and reasonably priced passive component selections. Suppliers who have a global support structure and can supply both prototype and production quantities are listed. The following table lists a number of suppliers which have been used in recent applications. The design engineer will also need information on the performance of the components as a function of temperature, frequency, solderability and reliability. Most of these suppliers have applications-engineering support with a wealth of specific technical information. *Motorola, however, cannot warrant the suppliers' quality, availability, or prices.*

Motorola suggests contacting the suppliers directly to obtain technical information and competitive quotes.

In many cases, recommendations have been made to use readily available sources such as “Radio Shack” for small parts and construction material. The user is encouraged to develop a core of dependable and local, if possible, suppliers for his or her passive components. Please note that many data sheets have specific passive components which have been used to develop and characterize the integrated circuit. Constructing a benchmark circuit with these components is an excellent starting point in the development of a new design.

COMPONENT SUPPLIERS

QUARTZ CRYSTALS — FREQUENCY CONTROL:

California Crystal Laboratories	(800) 333-9825
Fox Electronics	(813) 693-0099
International Crystals	(405) 236-3741
Standard Crystal Corporation	(818) 443-2121

GENERAL COMPONENTS — PROTOTYPE QUANTITIES — ASSEMBLY MATERIAL — PC BOARD MATERIAL:

Digi-Key Corporation	(800) 344-4539
Radio Shack Division, Tandy Corporation	(See local telephone directory)

INDUCTORS, COILS, RF TRANSFORMERS, FIXED AND VARIABLE:

Coilcraft	(800) 322-COIL (708) 639-6400
Toko America, Inc.	(708) 297-0070

CERAMIC FILTERS AND RESONATORS, IF FILTERS — AM & FM TYPES:

muRata Erie	(404) 436-1300 (Todd Brown, Harry Moore)
TDK Corporation of America	(708) 803-6100
Toko America, Inc.	(708) 297-0070

BREADBOARDING

Breadboarding RF or other high speed analog circuits can be a very frustrating process for the newcomer or even an experienced digital designer. Most of these circuits deal with very high gain (100+ dB), very small signals of less than a few microvolts, or with very high frequencies with wavelengths that are a fraction of a meter. Once “friendly” 0.1 µF capacitors may act as inductors, due to their parasitic inductance, while conventional construction methods may yield only circuits that oscillate.

What to avoid (never use these):

- Wire wrap for RF or high frequency breadboards.
- Conventional push-in prototype boards.
- Digital printed protoboards with ground and power supply bus lines.

What to use:

- Carefully laid-out double-sided groundplane PC boards.
- Grid boards with a backside ground plane.
- Single-sided PC layouts with continuous full ground fill.
- High frequency qualified components.
- Adequate decoupling.

The RF designer will find recommended PC board layouts for most of the communications circuits in Chapter 8. These layouts are strongly recommended as starting points for new designs. They will allow you to develop your own benchmark standard circuit to be used as a standard of comparison during further design iterations. Many Motorola communications ICs have supporting development kits which include a PC board. These boards are meant to provide performance equivalent to the data sheet specifications, and are easy to modify for other uses however, these boards are not optimized or intended for production applications. Contact your Motorola sales office or Motorola distributor for information on the availability of these development kits.

In addition, there are many PC and Macintosh-based CAD programs available today. In general, these programs work well for digital and low frequency analog circuits, but are of very limited value in RF applications. SPICE models are not currently available for the communications circuits. Several circuits do show S-Parameter data or admittance plane information which may be used to optimize input or output matching for gain or noise. The most useful method of utilizing the applications circuits at different frequencies is simple linear scaling of the tuning and reactive elements. This method is generally applicable over a 2:1 frequency range lower than the documented application.

Many communication applications include some digital signaling, data conversion, or microcontroller interface. The RF Designer must take great caution to avoid interference with the low level analog circuits in these mixed-mode systems. The receivers are particularly susceptible to interference as they respond to signals of only a few microvolts. Make sure the clock frequency is not a submultiple of the receiver input or IF frequencies. Be sure to keep the dc supply lines for the digital and analog portions separate. Avoid ground paths carrying common digital and analog currents. Common sense as well as analytical skill is required for a successful RF design. A good consultant may well save many times their fee in material, lost time, and rework expenses.

TEST EQUIPMENT

Establishing a new RF/Communications lab can be a very costly investment. The normal DVMs and regulated power supplies are generally acceptable, if they do not generate spurious RF, and are not sensitive to RF voltages. The Designer should choose an oscilloscope with a frequency response three or more times higher than the operating frequency. In addition, a low capacitance probe, a FET probe, would be useful. Remember, while conventional probes have very high input resistance, their capacitive reactance decreases with frequency and becomes a limiting factor above 30 MHz. For most transmitter work, a basic spectrum analyzer is a must to help confirm power output, spurious output levels, stability, and modulation characteristics.

Rental and used equipment are often a good source of test equipment. Communications System Analysers have recently become available at very moderate prices. The Motorola R2600, for example, combines 16 different instruments into one portable package. The signal generator, receiver, counter, oscilloscope and a “best-in-class” modulation meter make this instrument a very attractive design and production test tool. Further information, including a demonstration, are available from your local Motorola Communications and Electronics sales office.

WORLDWIDE CORDLESS TELEPHONE FREQUENCIES

The following tables contain CT–1 USA and Asia Pacific (CT–0 Europe) frequencies for cordless telephone. These tables reference application information provided in MC13109, MC13110, and MC13111 Universal Cordless Telephone Subsystem Integrated Circuit Technical Data Sheets. Channel number, T_X channel frequency, 1st LO frequency, and T_X and R_X divider values are listed in this addendum. The device data sheets can be found in Chapter 8 of this Data Book (DL128).

Note: USA cordless frequency band listed herein is specified in the Code of Federal Regulations (CFR), Title 47 (FCC Rules), Part 15, paragraph 15.233, dated June 5, 1995 (25 channel band).

CHANNEL FREQUENCIES

USA CT–1 BASESET CHANNEL FREQUENCIES (2nd LO = 10.240 MHz, Ref Divider = 2048)

Channel Number	T_X Channel Frequency (MHz)	T_X Divider (5.0 kHz Ref)	1st LO Frequency (MHz) 1st IF = 10.695 MHz	R_X Divider (5.0 kHz Ref)
1	43.720	8744	38.065	7613
2	43.740	8748	38.145	7629
3	43.820	8764	38.165	7633
4	43.840	8768	38.225	7645
5	43.920	8784	38.325	7665
6	43.960	8792	38.385	7677
7	44.120	8824	38.405	7681
8	44.160	8832	38.465	7693
9	44.180	8836	38.505	7701
10	44.200	8840	38.545	7709
11	44.320	8864	38.585	7717
12	44,360	8872	38.665	7733
13	44.400	8880	38.705	7741
14	44.460	8892	38.765	7753
15	44.480	8896	38.805	7761
16	46.610	9322	38.975	7795
17	46.630	9326	39.150	7830
18	46.670	9334	39.165	7833
19	46.710	9342	39.075	7815
20	46.730	9346	39.180	7836
21	46.770	9354	39.135	7827
22	46.830	9366	39.195	7839
23	46.870	9374	39.235	7847
24	46.930	9386	39.295	7859
25	46.970	9394	39.275	7855

USA CT–1 HANDSET CHANNEL FREQUENCIES (2nd LO = 10.240 MHz, Ref Divider = 2048)

Channel Number	T_X Channel Frequency (MHz)	T_X Divider (5.0 kHz Ref)	1st LO Frequency (MHz) 1st IF = 10.695 MHz	R_X Divider (5.0 kHz Ref)
1	48.760	9752	33.025	6605
2	48.840	9768	33.045	6609
3	48.860	9772	33.125	6625
4	48.920	9784	33.145	6629
5	49.020	9804	33.225	6645
6	49.080	9816	33.265	6653
7	49.100	9820	33.425	6685
8	49.160	9832	33.465	6693
9	49.200	9840	33.485	6697
10	49.240	9848	33.505	6701
11	49.280	9856	33.625	6725
12	49.360	9872	33.665	6733
13	49.400	9880	33.705	6741
14	49.460	9892	33.765	6753
15	49.500	9900	33.785	6757
16	49.670	9934	35.915	7183
17	49.845	9969	35.935	7187
18	49.860	9972	35.975	7195
19	49.770	9954	36.015	7203
20	49.875	9975	36.035	7207
21	49.830	9966	36.075	7215
22	49.890	9978	36.135	7227
23	49.930	9986	36.175	7235
24	49.990	9998	36.235	7247
25	49.970	9994	36.275	7255

SPAIN CT–1 BASESET CHANNEL FREQUENCIES (2nd LO = 10.240 MHz, Ref Divider = 2048)

Channel Number	T_X Channel Frequency (MHz)	T_X Divider (5.0 kHz Ref)	1st LO Frequency (MHz) 1st IF = 10.695 MHz	R_X Divider (5.0 kHz Ref)
1	31.025	6205	29.230	5846
2	31.050	6210	29.255	5851
3	31.075	6215	29.280	5856
4	31.100	6220	29.305	5861
5	31.125	6225	29.330	5866
6	31.150	6230	29.355	5871
7	31.175	6235	29.380	5876
8	31.200	6240	29.405	5881
9	31.250	6250	29.455	5891
10	31.275	6255	29.480	5896
11	31.300	6260	29.505	5901
12	31.325	6265	29.530	5906

SPAIN CT–1 HANDSET CHANNEL FREQUENCIES (2nd LO = 10.240 MHz, Ref Divider = 2048)

Channel Number	T_X Channel Frequency (MHz)	T_X Divider (5.0 kHz Ref)	1st LO Frequency (MHz) 1st IF = 10.695 MHz	R_X Divider (5.0 kHz Ref)
1	39.925	7985	20.330	4066
2	39.950	7990	20.355	4071
3	39.975	7995	20.380	4076
4	40.000	8000	20.405	4081
5	40.025	8005	20.430	4086
6	40.050	8010	20.455	4091
7	40.075	8015	20.480	4096
8	40.100	8020	20.505	4101
9	40.150	8030	20.555	4111
10	40.175	8035	20.580	4116
11	40.200	8040	20.605	4121
12	40.225	8045	20.630	4126

AUSTRALIA CT–1 BASESET CHANNEL FREQUENCIES (2nd LO = 10.240 MHz, Ref Divider = 2048)

Channel Number	T_X Channel Frequency (MHz)	T_X Divider (5.0 kHz Ref)	1st LO Frequency (MHz) 1st IF = 10.695 MHz	R_X Divider (5.0 kHz Ref)
1	30.075	6015	29.080	5816
2	30.125	6025	29.130	5826
3	30.175	6035	29.180	5836
4	30.225	6045	29.230	5846
5	30.275	6055	29.280	5856
6	30.100	6020	29.105	5821
7	30.150	6030	29.155	5831
8	30.200	6040	29.205	5841
9	30.250	6050	29.255	5851
10	30.300	6060	29.305	5861

AUSTRALIA CT–1 HANDSET CHANNEL FREQUENCIES (2nd LO = 10.240 MHz, Ref Divider = 2048)

Channel Number	T_X Channel Frequency (MHz)	T_X Divider (5.0 kHz Ref)	1st LO Frequency (MHz) 1st IF = 10.695 MHz	R_X Divider (5.0 kHz Ref)
1	39.775	7955	19.380	3876
2	39.825	7965	19.430	3886
3	39.875	7975	19.480	3896
4	39.925	7985	19.530	3906
5	39.975	7995	19.580	3916
6	39.800	7960	19.405	3881
7	39.850	7970	19.455	3891
8	39.900	7980	19.505	3901
9	39.950	7990	19.555	3911
10	40.000	8000	19.605	3921

KOREA CT–1 BASESET CHANNEL FREQUENCIES (2nd LO = 10.240 MHz, Ref Divider = 2048)

Channel Number	T_X Channel Frequency (MHz)	T_X Divider (5.0 kHz Ref)	1st LO Frequency (MHz) 1st IF = 10.695 MHz	R_X Divider (5.0 kHz Ref)
1	46.610	9322	38.975	7795
2	46.630	9326	39.150	7830
3	46.670	9334	39.165	7833
4	46.710	9342	39.075	7815
5	46.730	9346	39.180	7836
6	46.770	9354	39.135	7827
7	46.830	9366	39.195	7839
8	46.870	9374	39.235	7847
9	46.930	9386	39.295	7859
10	46.970	9394	39.275	7855
11	46.510	9302	39.000	7800
12	46.530	9306	39.015	7803
13	46.550	9310	39.030	7806
14	46.570	9314	39.045	7809
15	46.590	9318	39.060	7812

KOREA CT–1 HANDSET CHANNEL FREQUENCIES (2nd LO = 10.240 MHz, Ref Divider = 2048)

Channel Number	T_X Channel Frequency (MHz)	T_X Divider (5.0 kHz Ref)	1st LO Frequency (MHz) 1st IF = 10.695 MHz	R_X Divider (5.0 kHz Ref)
1	49.670	9934	35.915	7183
2	49.845	9969	35.935	7187
3	49.860	9972	35.975	7195
4	49.770	9954	36.015	7203
5	49.875	9975	36.035	7207
6	49.830	9966	36.075	7215
7	49.890	9978	36.135	7227
8	49.930	9986	36.175	7235
9	49.990	9998	36.235	7247
10	49.970	9994	36.275	7255
11	49.695	9939	35.815	7163
12	49.710	9942	35.835	7167
13	49.725	9945	35.855	7171
14	49.740	9948	35.875	7175
15	49.755	9951	35.895	7179

NEW ZEALAND CT–1 BASESET CHANNEL FREQUENCIES (2nd LO = 10.240 MHz, Ref Divider = 2048)

Channel Number	T_X Channel Frequency (MHz)	T_X Divider (5.0 kHz Ref)	1st LO Frequency (MHz) 1st IF = 10.695 MHz	R_X Divider (5.0 kHz Ref)
11	34.250	6850	29.555	5911
12	34.275	6855	29.580	5916
13	34.300	6860	29.605	5921
14	34.325	6865	29.630	5926
15	34.350	6870	29.655	5931
16	34.375	6875	29.680	5936
17	34.400	6880	29.705	5941
18	34.425	6885	29.730	5946
19	34.450	6890	29.755	5951
20	34.475	6895	29.780	5956

NEW ZEALAND CT–1 HANDSET CHANNEL FREQUENCIES (2nd LO = 10.240 MHz, Ref Divider = 2048)

Channel Number	T_X Channel Frequency (MHz)	T_X Divider (5.0 kHz Ref)	1st LO Frequency (MHz) 1st IF = 10.695 MHz	R_X Divider (5.0 kHz Ref)
11	40.250	8050	23.555	4711
12	40.275	8055	23.580	4716
13	40.300	8060	23.605	4721
14	40.325	8065	23.630	4726
15	40.350	8070	23.655	4731
16	40.375	8075	23.680	4736
17	40.400	8080	23.705	4741
18	40.425	8085	23.730	4746
19	40.450	8090	23.755	4751
20	40.475	8095	23.780	4756

U.K. BASESET CHANNEL FREQUENCIES (2nd LO = 11.150 MHz, Ref Divider = 446 + divide by 4/25)

Channel Number	T_X Channel Frequency (MHz)	T_X Divider (1.0 kHz Ref)	1st LO Frequency (MHz) 1st IF = 10.7 MHz	R_X Divider (6.25 kHz Ref)
1	1.642	1642	36.75625	5881
2	1.662	1662	36.76875	5883
3	1.682	1682	36.78125	5885
4	1.702	1702	36.79375	5887
5	1.722	1722	36.80625	5889
6	1.742	1742	36.81875	5891
7	1.762	1762	36.83125	5893
8	1.782	1782	36.84375	5895

U.K. HANDSET CHANNEL FREQUENCIES (2nd LO = 11.150 MHz, Ref Divider = 446 + divide by 4/25)

Channel Number	T_X Channel Frequency (MHz)	T_X Divider (6.25 kHz Ref)	1st LO Frequency (MHz) 1st IF = 10.7 MHz	R_X Divider (1.0 kHz Ref)
1	47.45625	7593	12.342	12342
2	47.46875	7595	12.362	12362
3	47.48125	7597	12.382	12382
4	47.49375	7599	12.402	12402
5	47.50625	7601	12.422	12422
6	47.51875	7603	12.442	12442
7	47.53125	7605	12.462	12462
8	47.54375	7607	12.482	12482

FRANCE BASESET CHANNEL FREQUENCIES (2nd LO = 11.150 MHz, Ref Divider = 1784)

Channel Number	T_X Channel Frequency (MHz)	T_X Divider (6.25 kHz Ref)	1st LO Frequency (MHz) 1st IF = 10.7 MHz	R_X Divider (6.25 kHz Ref)
1	26.3125	4210	30.6125	4898
2	26.3250	4212	30.6250	4900
3	26.3375	4214	30.6375	4902
4	26.3500	4216	30.6500	4904
5	26.3625	4218	30.6625	4906
6	26.3750	4220	30.6750	4908
7	26.3875	4222	30.6875	4910
8	26.4000	4224	30.7000	4912
9	26.4125	4226	30.7125	4914
10	26.4250	4228	30.7250	4916
11	26.4375	4230	30.7375	4918
12	26.4500	4232	30.7500	4920
13	26.4625	4234	30.7625	4922
14	26.4750	4236	30.7750	4924
15	26.4875	4238	30.7875	4926

FRANCE HANDSET CHANNEL FREQUENCIES (2nd LO = 11.150 MHz, Ref Divider = 1784)

Channel Number	T_X Channel Frequency (MHz)	T_X Divider (6.25 kHz Ref)	1st LO Frequency (MHz) 1st IF = 10.7 MHz	R_X Divider (6.25 kHz Ref)
1	41.3125	6610	37.0125	5922
2	41.3250	6612	37.0250	5924
3	41.3375	6614	37.0375	5926
4	41.3500	6616	37.0500	5928
5	41.3625	6618	37.0625	5930
6	41.3750	6620	37.0750	5932
7	41.3875	6622	37.0875	5934
8	41.4000	6624	37.1000	5936
9	41.4125	6626	37.1125	5938
10	41.4250	6628	37.1250	5940
11	41.4375	6630	37.1375	5942
12	41.4500	6632	37.1500	5944
13	41.4625	6634	37.1625	5946
14	41.4750	6636	37.1750	5948
15	41.4875	6638	37.1875	5950

CHINA BASESET CHANNEL FREQUENCIES (2nd LO = 10.240 MHz, Ref Divider = 2048)

Channel Number	T_X Channel Frequency (MHz)	T_X Divider (5.0 kHz Ref)	1st LO Frequency (MHz) 1st IF = 10.695 MHz	R_X Divider (5.0 kHz Ref)
1	45.250	9050	37.555	7511
2	45.275	9055	37.580	7516
3	45.300	9060	37.605	7521
4	45.325	9065	37.630	7526
5	45.350	9070	37.655	7531
6	45.375	9075	37.680	7536
7	45.400	9080	37.705	7541
8	45.425	9085	37.730	7546
9	45.450	9090	37.755	7551
10	45.475	9095	37.780	7556

CHINA HANDSET CHANNEL FREQUENCIES (2nd LO = 10.240 MHz, Ref Divider = 2048)

Channel Number	T_X Channel Frequency (MHz)	T_X Divider (5.0 kHz Ref)	1st LO Frequency (MHz) 1st IF = 10.695 MHz	R_X Divider (5.0 kHz Ref)
1	48.250	9650	34.555	6911
2	48.275	9655	34.580	6916
3	48.300	9660	34.605	6921
4	48.325	9665	34.630	6926
5	48.350	9670	34.655	6931
6	48.375	9675	34.680	6936
7	48.400	9680	34.705	6941
8	48.425	9685	34.730	6946
9	48.450	9690	34.755	6951
10	48.475	9695	34.780	6956

NETHERLANDS CT–1 BASESET CHANNEL FREQUENCIES

(2nd LO = 10.240 MHz, Ref Divider = 1024 + divide by 4, 2nd IF = 455 Hz)

Channel Number	T_X Channel Frequency (MHz)	T_X Divider (2.5 kHz Ref)	1st LO Frequency (MHz) 1st IF = 10.695 MHz	R_X Divider (2.5 kHz Ref)
1	31.0375	12415	29.2425	11697
2	31.0625	12425	29.2675	11707
3	31.0875	12435	29.2925	11717
4	31.1125	12445	29.3175	11727
5	31.1375	12455	29.3425	11737
6	31.1625	12465	29.3675	11747
7	31.1875	12475	29.3925	11757
8	31.2125	12485	29.4175	11767
9	31.2375	12495	29.4425	11777
10	31.2625	12505	29.4675	11787
11	31.2875	12515	29.4925	11797
12	31.3125	12525	29.5175	11807

NETHERLANDS CT–1 HANDSET CHANNEL FREQUENCIES

(2nd LO = 10.240 MHz, Ref Divider = 1024 + divide by 4, 2nd IF = 455 Hz)

Channel Number	T_X Channel Frequency (MHz)	T_X Divider (2.5 kHz Ref)	1st LO Frequency (MHz) 1st IF = 10.695 MHz	R_X Divider (2.5 kHz Ref)
1	39.9375	15975	20.3425	8137
2	39.9625	15985	20.3675	8147
3	39.9875	15995	20.3925	8157
4	40.0125	16005	20.4175	8167
5	40.0375	16015	20.4425	8177
6	40.0625	16025	20.4675	8187
7	40.0875	16035	20.4925	8197
8	40.1125	16045	20.5175	8207
9	40.1375	16055	20.5425	8217
10	40.1625	16065	20.5675	8227
11	40.1875	16075	20.5925	8237
12	40.2125	16085	20.6175	8247

Consumer Electronic Circuits

In Brief . . .

These integrated circuits reflect Motorola's continuing commitment to semiconductor products necessary for consumer system designs. This tabulation is arranged to simplify selection of consumer integrated circuit devices that satisfy the primary functions for home entertainment products, including television, hi–fi audio and AM/FM radio.

Entertainment Radio Receiver Circuits

Table 1. Entertainment Receiver RF/IF

Function	Features	Suffix/ Package	Device
E.T.R. Front End	Mixer/VCO/AGC for Electronically Tuned AM Stereo Receivers	P/648, D/751B	MC13025
AMAX Front End	Mixer/VCO/AGC with RF and Audio Noise Blanking	DW/751D, P/738	MC13027
Dual Conversion AM Receiver	1st Mixer/OSC, 2nd Mixer/OSC, High Gain IF, AGC, Detector	DW/751F	MC13030

Table 2. C–Quam® AM Stereo Decoders

Function	Features	Suffix/ Package	Device
Basic AM Stereo Decoder	Monaural/Stereo AM Detector/Indicator, 6.0 to 10 V Operation	P/738	MC13020
Advanced AM Stereo Decoder	Medium Voltage 4.0 to 10 V, Decoder and IF Amp	P/710, DW/751F	MC13022
Advanced AM Stereo Decoder	Medium Voltage 6.0 to 10 V, Decoder and IF Amp	P/710, DW/751F	MC13022A
Low V AM Stereo Receiver	IF/Decoder for Advanced C–Quam Receivers	P/648, D/751B	MC13028A
Medium V AM Stereo Decoder	IF/Decoder for Advanced C–Quam Receivers with AM/FM Switch	DW/751D, H/738	MC13029A
AMAX Stereo Decoder	Am Stereo Decoder with Audio Noise Blanker	DW/751F, P/710	MC13122

Table 3. Audio Amplifiers

Function	P_O (Watts)	V_{CC} Vdc Max	V_{in} @ Rated P_O mV Typ	I_D mA Typ	R_L (Ohms)	Suffix/ Package	Device
Mini Watt SOIC Audio Amp	1.0 W	35	80	11	16	D/751	MC13060
Low Power Audio Amp	500 mW	16	–	2.5 mA	8 – ∞	D/751, P/626, DTB/948J	MC34119

Video Circuits

Table 4. Video Circuits

Function	Features	Suffix/ Package	Device
Encoders			
RGB to PAL/NTSC Encoder	RGB and Sync inputs, Composite Video out; PAL/NTSC selectable.	P/738, DW/751D	MC1377
Video Overlay Synchronizer	Complete Color TV Video Overlay Synchronizer, remote or local system control and RGB encoder.	P/711, FN/777	MC1378
Advanced RGB to PAL/NTSC Encoder	RGB and Sync inputs, Composite Video and S–VHS out; PAL/NTSC selectable; subcarrier from crystal or external source.	P/738, DW/751D	MC13077
TV Decoder			
Chroma 4 Multistandard Decoders (TV Set)	PAL/NTSC/SECAM decoding, Composite Video/S–VHS Inputs, RGB Outputs, horizontal and vertical drive outputs, geometry correction and beam current monitor, digital internal filters, no external tank, 16:9 capability, µP and crystal controlled.	P/711	MC44002
	Same as MC44002, but without SECAM decoding.	P/711	MC44007
	Same as MC44002, but with internal chroma delay line.	P/711	MC44030
	Same as MC44030, but without SECAM decoding.	P/711	MC44035
Video Capture Chip Sets			
Chroma 4 Multistandard Video Processor (Multimedia)	PAL/NTSC/S–VHS input, RGB/YUV outputs; horizontal and vertical timing outputs; all digital internal filters, no external tanks; µP and crystal controlled.	FN/777, FB/824E	MC44011
Chroma Digital Delay Line	For PAL and SECAM applications of the MC44011, MC44002, MC44007.	P/648, DW/751G	MC44140
Pixel Clock PLL/Sync Sep.	PAL/NTSC sync separator, 6.0–40 MHz pixel clock PLL.	D/751A	MC44145
Triple 8–Bit Video DAC	TTL inputs, 75 Ω drive outputs.	FB/824A	MC44200
Triple 8–Bit Video A/D	Video clamps for RGB/YUV, 18 MHz, High Z TTL outputs.	FN/777	MC44251
TV Picture–in–Picture			
Picture–in–Picture (PIP) Controller	Completely self–contained NTSC picture–in–picture function.	B/859	MC44461
Y–C Picture–in–Picture (PIP) Controller	Completely self–contained NTSC picture–in–picture function, with Y–C input and output capability, for use in high performance S–Video systems.	B/859	MC44462
Replay and Multiple Picture–in–Picture (PIP) Controller	Offers either multiple PIP windows or several seconds of replay. Used with external DRAM.	B/859	MC44463
Comb Filters			
Enhanced Comb Filter	Fast 8–Bit A/D Converter, Two 8–Bit D/A Converters, Two Line–Delay Memories, utilizes NTSC Subcarrier Frequency clock, CMOS Technology.	FU/898	MC141620
Advanced Comb Filter (ACF)	Composite Video input; YC outputs in digital and analog form; all digital internal filters.	FU/898	MC141621A
Advanced Comb Filter – II (ACF–II)	Composite Video input; YC outputs in digital and analog form; all digital internal filters; vertical enhancer circuit.	P/898	MC141622A
Advanced Comb Filter – I (ACF–I)	Low cost Ih filter.	FU/873 SP/TBD	MC141624
Advanced PAL/NTSC Comb Filter	Composite Video input; YC outputs in digital and analog form; all digital internal filters.	FB/898	MC141627
Deflection			
Horizontal Processor	Linear balanced phase detector, oscillator and predriver, adjustable DC loop gain and duty cycle.	P/626	MC1391
TV IF Circuits			
IF Amplifier	1st and 2nd video IF amplifiers, 50 dB gain at 45 MHz, 60 dB AGC range.	D/751, P/626	MC1350

Table 4. Video Circuits (continued)

Function	Features	Suffix/ Package	Device
Tuner PLL Circuits			
PLL Tuning Circuits	1.3 GHz, 10 mV sensitivity selectable prescaler (MC44817), op amp, 4 band buffers, 3–wire bus interface, lock detect.	D/751B	MC44817, B
	1.3 GHz, 10 mV sensitivity prescaler, op amp, 4 band buffers, I^2C interface, lock detect.	D/751B	MC44818
	1.3 GHz, 10 mV sensitivity prescaler, 3 band buffers, I^2C interface, replacement for Siemens MPG3002.	D/751, D/751B	MC44824, MC44825
	Similar to MC44817, with lower power consumption, push–pull lock detector output, no divide–by–8 bypass, in a TSSOP package.	DTB/948F	MC44827
	Similar to MC44818, with lower power consumption, push–pull lock detector output, in a TSSOP package.	DTB/948F	MC44828
	1.3 GHz prescaler, 10 mV sensitivity 50 to 950 MHz, op amp, 3 band buffers, Mixer/Osc Decoder and I^2C Bus.	D/751A	MC44829
	1.3 GHz, 10 mV sensitivity selectable prescaler, op amp, 4 band buffers, I^2C interface, 3 DACs for automatic tuner alignment.	M/967	MC44864
Modulator			
Color TV Modulator with Sound	RF oscillator/modulator, and FM sound oscillator/modulator.	P/646	MC1374
UHF TV Modulator	Multi–standard PLL tuned UHF TV modulator with AM or FM sound.	DTB/948E, DW/751D	MC44353, MC44354, MC44355
Video Data Converters			
Single Channel A/D	8–Bit, 25 MHz, 2.0 V input range, ±5.0 V supplies, TTL output, no pipeline delay.	P/709, DW/751E	MC10319
Triple 8–Bit Video A/D	Video clamps for RGB/YUV, 18 MHz conversion, high Z outputs.	FN/777	MC44251
Triple 8–Bit Video DAC	TTL inputs, 75 Ω drive outputs.	FB/824	MC44200
Monitor Subsystem			
Multimode Color Monitor Processor	Adaptable to 30 kHz to 64 kHz horizontal, 45 to 100 Hz vertical frequency, multiple sync including sync–on–green, horizontal and vertical drive outputs, double PLL, 70 MHz RGB pre–amps, contrast and brightness controls.	B/859	MC13081X
RGB Video Processor	80 MHz bandwidth, blank and clamp inputs, main contrast and subcontrast controls.	P/738	MC13280AY
	Same as above, except 100 MHz bandwidth.	P/738	MC13281B
	Same as above, except 100 MHz bandwidth and pin compatible with MC13282A.	P/724	MC13281A
RGB Video Processor with OSD Inputs	100 MHz bandwidth, blank and clamp inputs, main contrast and subcontrast controls, OSD inputs, OSD contrast control, pin compatible with MC13281A.	P/724	MC13282A
	Same as above, except 130 MHz bandwidth.	P/724	MC13283
Sound			
Sound IF Detector	Interchangeable with ULN2111A.	P/646, D/751A	MC1357
Miscellaneous			
Subcarrier Reference Generator	Provides continuous subcarrier sine wave and 4x subcarrier, locked to incoming burst.	P/626, D/751	MC44144
Closed Caption Decoder	Conforms to FCC, NTSC standards, underline and italics control.	P/707	MC144143
Enhanced Closed Caption Decoder	Conforms to FCC, NTSC, XDS standards, underline, italics and OSC.	P/707	MC144144
Sync Separator/Pixel Clock PLL	PAL/NTSC sync separator with vertical and composite sync output, 6 to 40 MHz pixel clock PLL.	D/751A	MC44145
Dual Video Amplifiers	Gain @ 4.43 MHz = 6.0 dB ±1.0 dB, fixed gain, internally compensated, CMOS Technology.	P/626, F/904	MC14576C
	Gain @ 5.0 MHz = 10 dB max, 10 MHz = 6.0 dB max, adjustable gain, internally compensated, CMOS Technology.	P/626, F/904	MC14577C

Table 4. Video Circuits (continued)

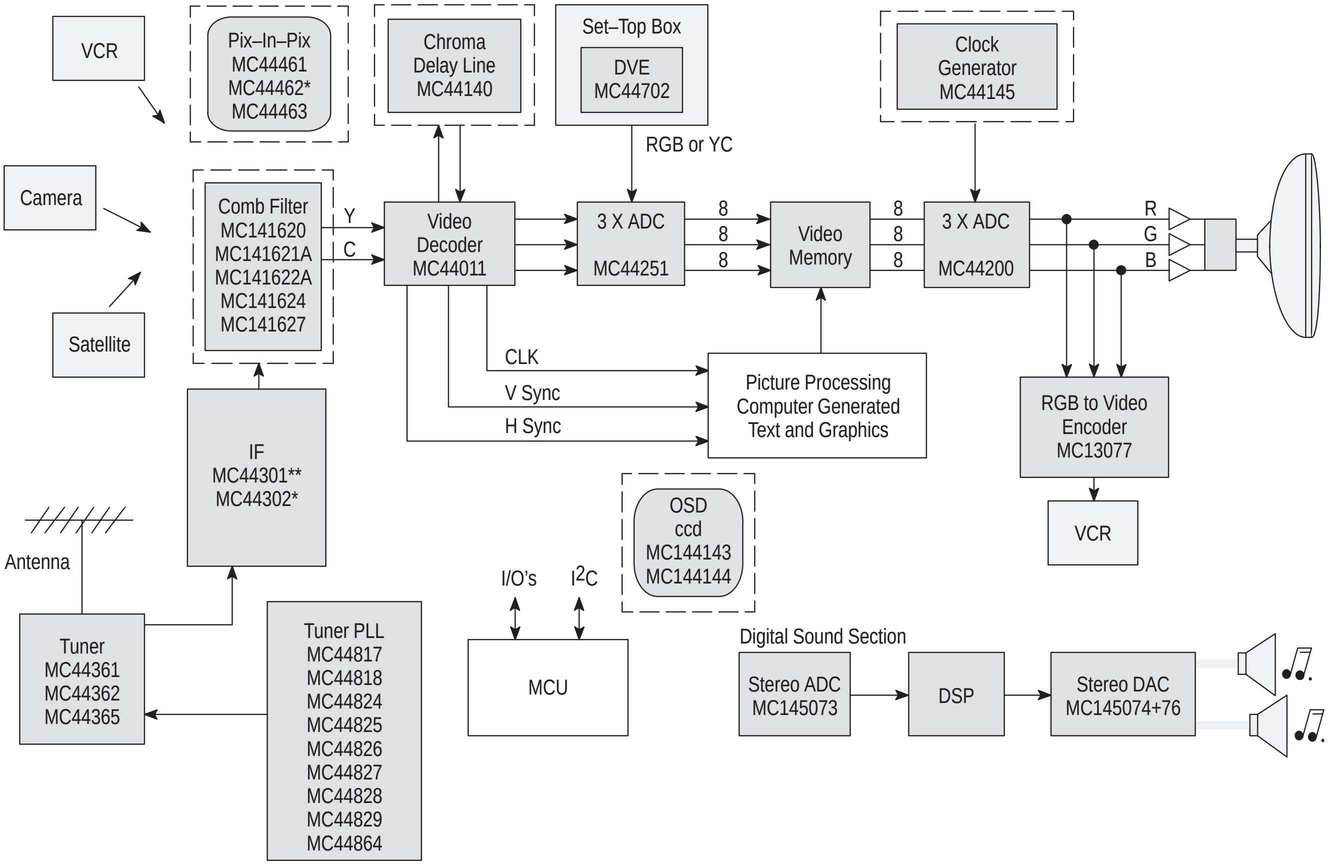
Function	Features	Suffix/ Package	Device
Miscellaneous			
Transistor Array	One differential pair and 3 isolated transistors, 15 V, 50 mA.	P/646, D/751A	MC3346
General Purpose Transistor Array	One differential pair and 3 isolated transistors, 130 V, 50 mA.	D/751A	CA3146

Table 5. Video Decoders

Function	MC44002	MC44007	MC44030(1)	MC44035	MC44011
For TV Set Applications (RGB Outputs for CRT Driver)	Yes		Yes		No
For Video Capture Applications (RGB/YUV Outputs)	No		No		Yes
PAL/NTSC Decoding	Yes		Yes		Yes
SECAM Decoding	Yes	No	Yes	No	No
Chroma Delay Line	External		Internal		External
Composite Video Inputs	2		2		2
Y/C Inputs	1 set (Note 2)		1 set (Note 2)		1 set (Note 2)
RGB Inputs (3 Pins)	1 set		1 set		1 set
YUV Outputs/Inputs	Yes		Yes		Yes
Video Output for Teletext or Closed Caption	No		No		No
16:9 Capability on 4:3 Screen	Yes		Yes		No
Single 5.0 V Supply	Yes		Yes		Yes
Supply Current (Typical)	120 mA		150 mA		110 mA
Video Mute (Blanking Control)	No		Yes		No
Pixel Clock Generator for A/D	No		No		Yes

NOTES: 1. The MC44030 with integrated chroma delay line can replace the MC44002 + MC44140. A single PC board pattern can be made to accept either device and the software can be written to be compatible, although the MC44030 has several additional functions.
2. In Y/C mode the two CVBS inputs become Y and C inputs.
3. One set uses SCART Video input as Y and SCART Red input as C. The second set are independent inputs.

Video Capture Block Diagram



* In Development
** Not recommended for new designs.

Digitally Controlled Video Processor for Multimedia Applications

MC44011FN, FB

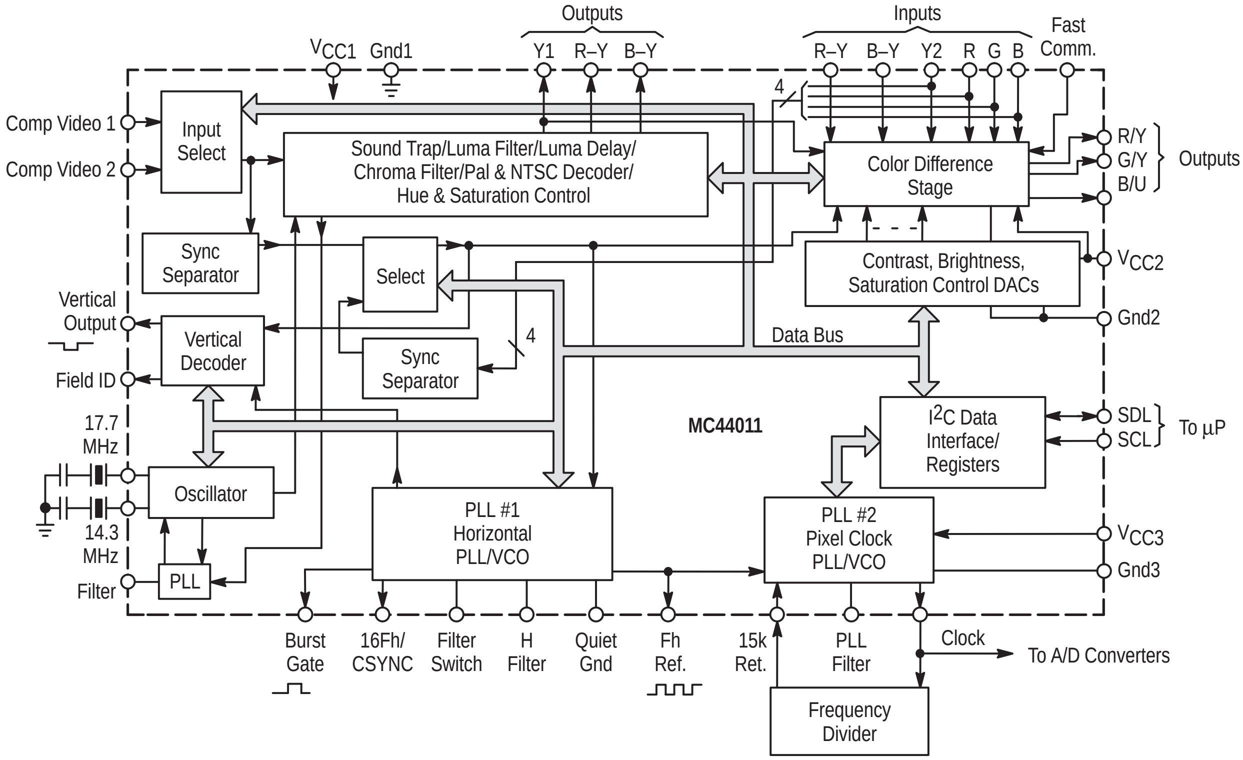
Case 777, 824E

The MC44011, a member of the MC44000 Chroma 4 family, is designed to provide RGB or YUV outputs from a variety of inputs. The inputs may be either PAL or NTSC composite video (two inputs), S–VHS, RGB, and color difference (R–Y, B–Y).

The MC44011 provides a sampling clock output for use by a subsequent analog to digital converter. The sampling clock (6.0 to 40 MHz) is phase–locked to the horizontal frequency. Additional outputs include composite sync, vertical sync, field identification, luminance, burst gate, and horizontal frequency.

Control of the MC44011, and reading of status flags is accomplished via an I^2C bus.

- Multistandard Decoder, Accepts NTSC and PAL Composite Video
- Dual Composite Video or S–VHS Inputs
- All Chroma and Luma Channel Filtering, and Luma Delay Line are Integrated Using Sampled Data Filters Requiring no External components
- Digitally Controlled via I^2C Bus
- Auxiliary Y, R–Y, B–Y Inputs
- Switched RGB Inputs with Separate Saturation Control
- Line–Locked Sampling Clock for Digitizing Video Signals
- Burst Gate Pulse Output for External Clamping
- Vertical Sync and Field Ident Outputs
- Software Selectable YUV or RGB Outputs Able to Drive A/D Converters



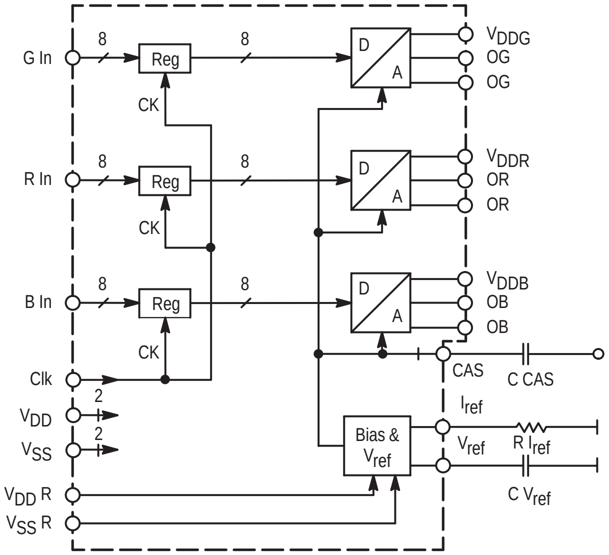
Triple 8–Bit D/A Converter

MC44200FB

Case 824A

The MC44200 is a monolithic digital to analog converter for three independent channels fabricated in CMOS technology. The part is specifically designed for video applications. Differential outputs are provided, allowing for a large output voltage range.

- 8–Bit Resolution
- Differential Outputs
- 55 msps Conversion Speed
- Large Output Voltage Range
- Low Current Mode
- Single 5.0 V Power Supply
- TTL Compatible Inputs
- Integrated Reference Voltage



Triple 8–Bit A/D Converter

MC44251FN

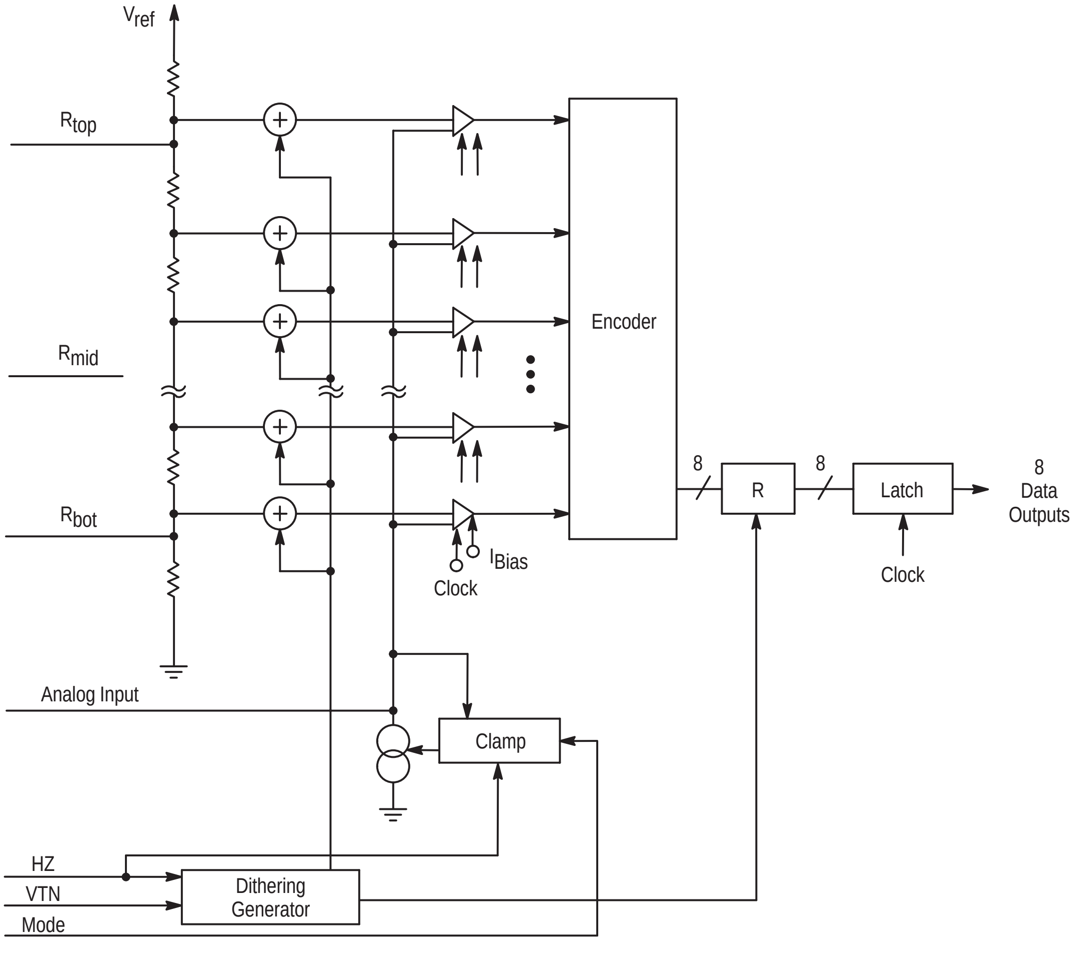
Case 777

The MC44251 contains three independent parallel analog to digital converters. Each ADC consists of 256 latching comparators and an encoder. Input clamps allow for AC coupling of the input signals, and dc coupling is also allowed. For video processing performance enhancements, a dither generator with subsequent digital correction is provided to each ADC. The outputs of the MC44251 can be set to a high impedance state.

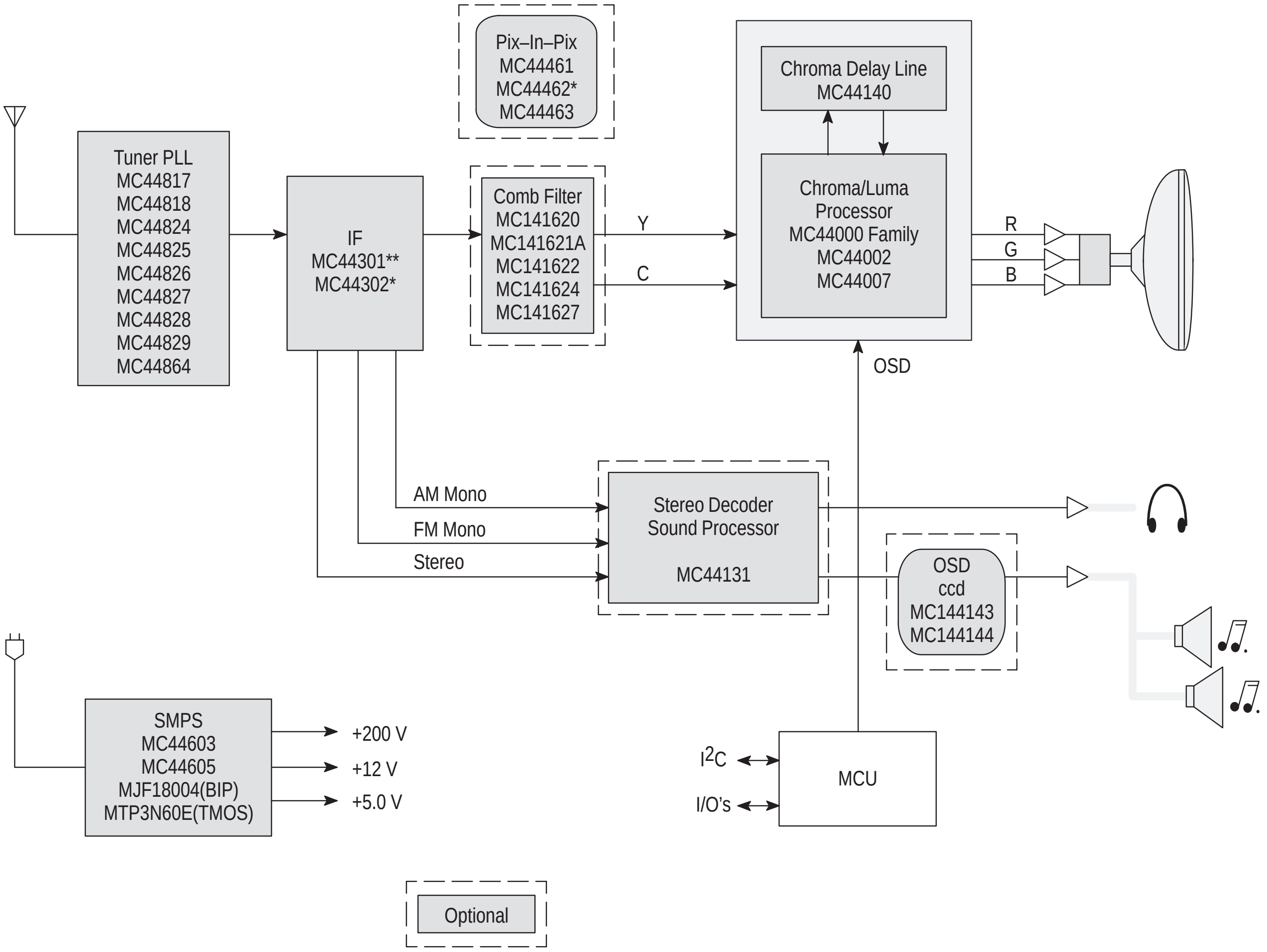
These A/Ds are especially suitable as front end converters in TV picture processing.

- 18 MHz Maximum Conversion Speed (MC44251)
- Input Clamps Suitable for RGB and YUV Applications
- Built–in Dither Generator with Subsequent Digital Correction
- Single 5.0 V Power Supply

Simplified Diagram of One of the ADCs



Color TV Block Diagram



* In Development
** Not recommended for new designs.

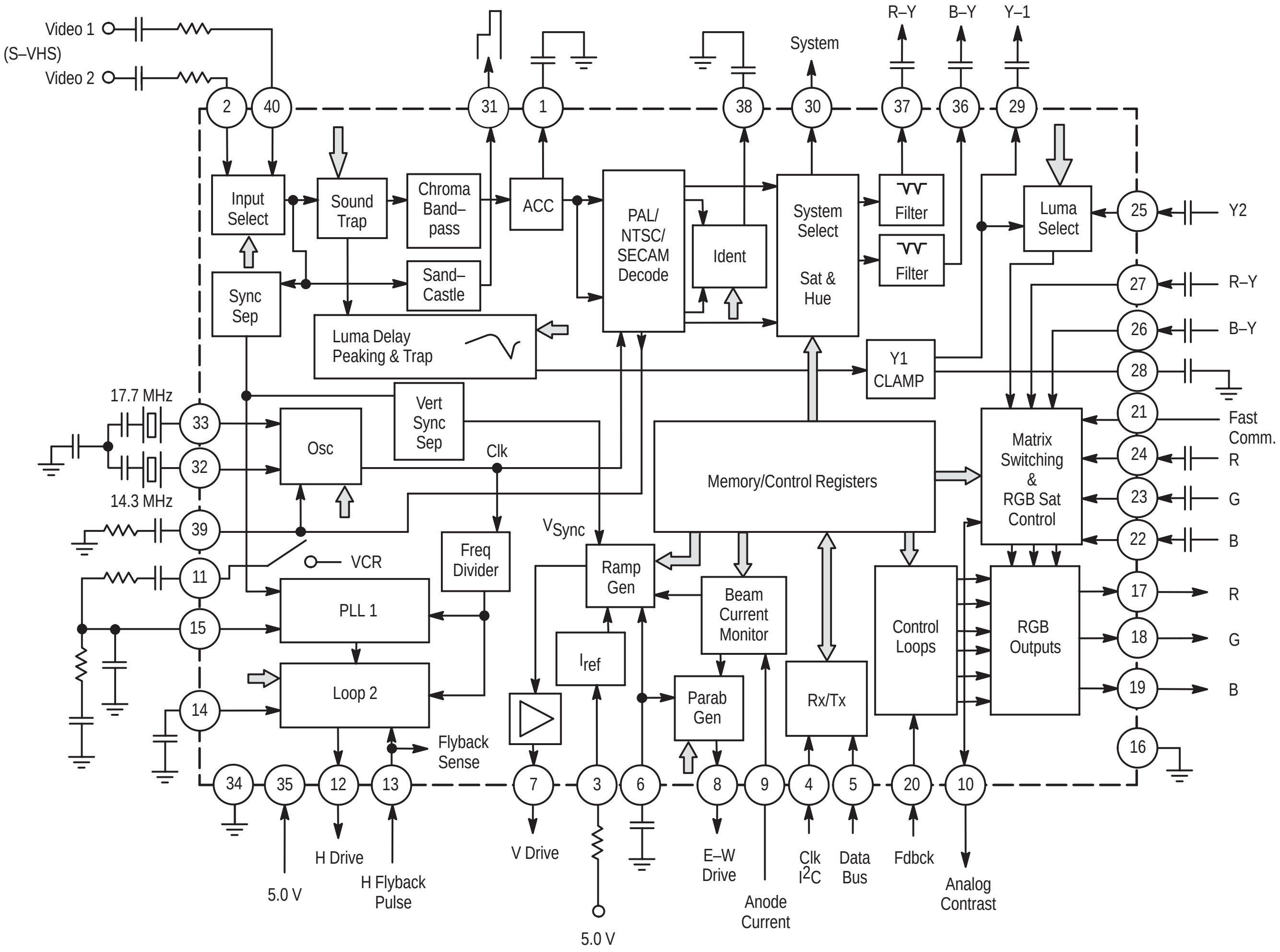
Multistandard Video/Timebase Processor

MC44002P, MC44007P

Case 711

The MC44002/7 is a highly advanced circuit which performs most of the basic functions required for a color TV. All of its advanced features are under processor control via an I^2C bus, enabling potentiometer controls to be removed completely. In this way the component count may be reduced dramatically to allow significant cost savings and the possibility of implementing sophisticated automatic test routines. Using the MC44002/7, TV manufacturers will be able to build a standard chassis for anywhere in the world.

- Operation from a Single 5.0 V Supply; Typical Current Consumption Only 120 mA
- Full PAL/SECAM/NTSC Capability (MC44002 Only)
- MC44007 Decodes PAL/NTSC Only
- Dual Composite Video or S–VHS Inputs
- All Chroma/Luma Channel Filtering, and Luma Delay Line are Integrated Using Sampled Data Filters Requiring No External Components
- Filters Automatically Commutate with Change of Standard
- Chroma Delay Line is Realized with Companion Device (MC44140)
- RGB Drives Incorporate Contrast and Brightness Controls and Auto Gray Scale
- Switched RGB Inputs with Saturation Control
- Auxiliary Y, R–Y, B–Y Inputs
- Line Timebase Featuring H–Phase Control and Switchable Phase Detector Gain and Time Constant
- Vertical Timebase Incorporating the Vertical Geometry Corrections
- E–W Parabola Drive Incorporating the Horizontal Geometry Corrections
- Beam Current Monitor with Breathing Compensation
- 16:9 Display Mode Capability

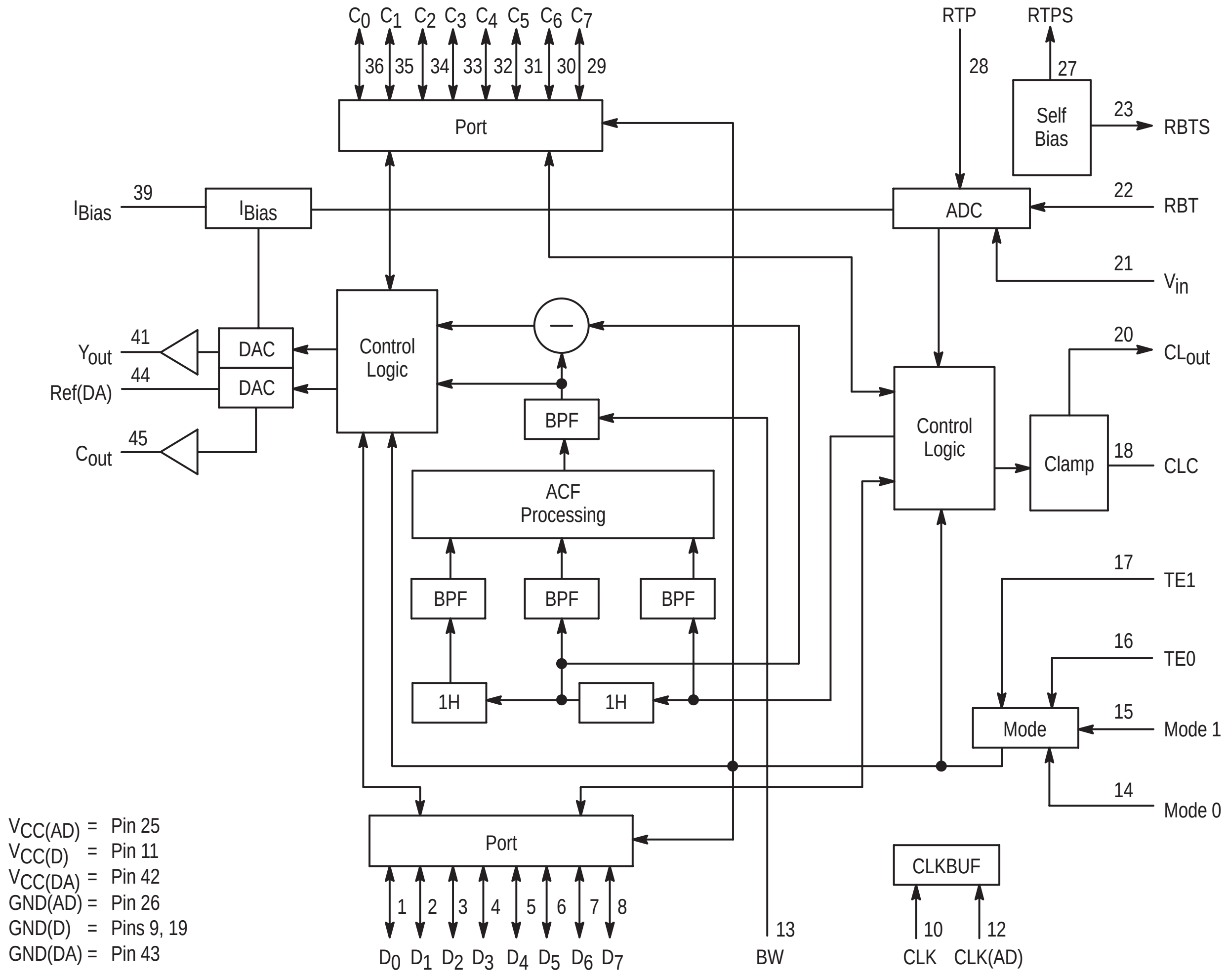


Advanced NTSC Comb Filter

MC141621FB
Case 898

The MC141621 is an advanced NTSC comb filter for VCR and TV applications. It separates the luminance (Y) and chrominance (C) signals from the NTSC composite video signal by using digital signal processing techniques. This filter allows a video signal input of an extended frequency bandwidth by using a 4.0 F_{SC} clock. In addition, the filter minimizes dot crawl and cross color effects. The built–in A/D and D/A converters allow easy connections to analog video circuits.

- Built–in High Speed 8–Bit A/D Converter
- Two Line Memories (1820 Bytes)
- Advanced Combing Process
- Two 8–Bit D/A Converters
- Built–in Clamp Circuit
- On–Chip Reference Voltage Regulator for ADC
- Digital Interface Mode



$V_{CC(AD)}$ = Pin 25
$V_{CC(D)}$ = Pin 11
$V_{CC(DA)}$ = Pin 42
GND(AD) = Pin 26
GND(D) = Pins 9, 19
GND(DA) = Pin 43

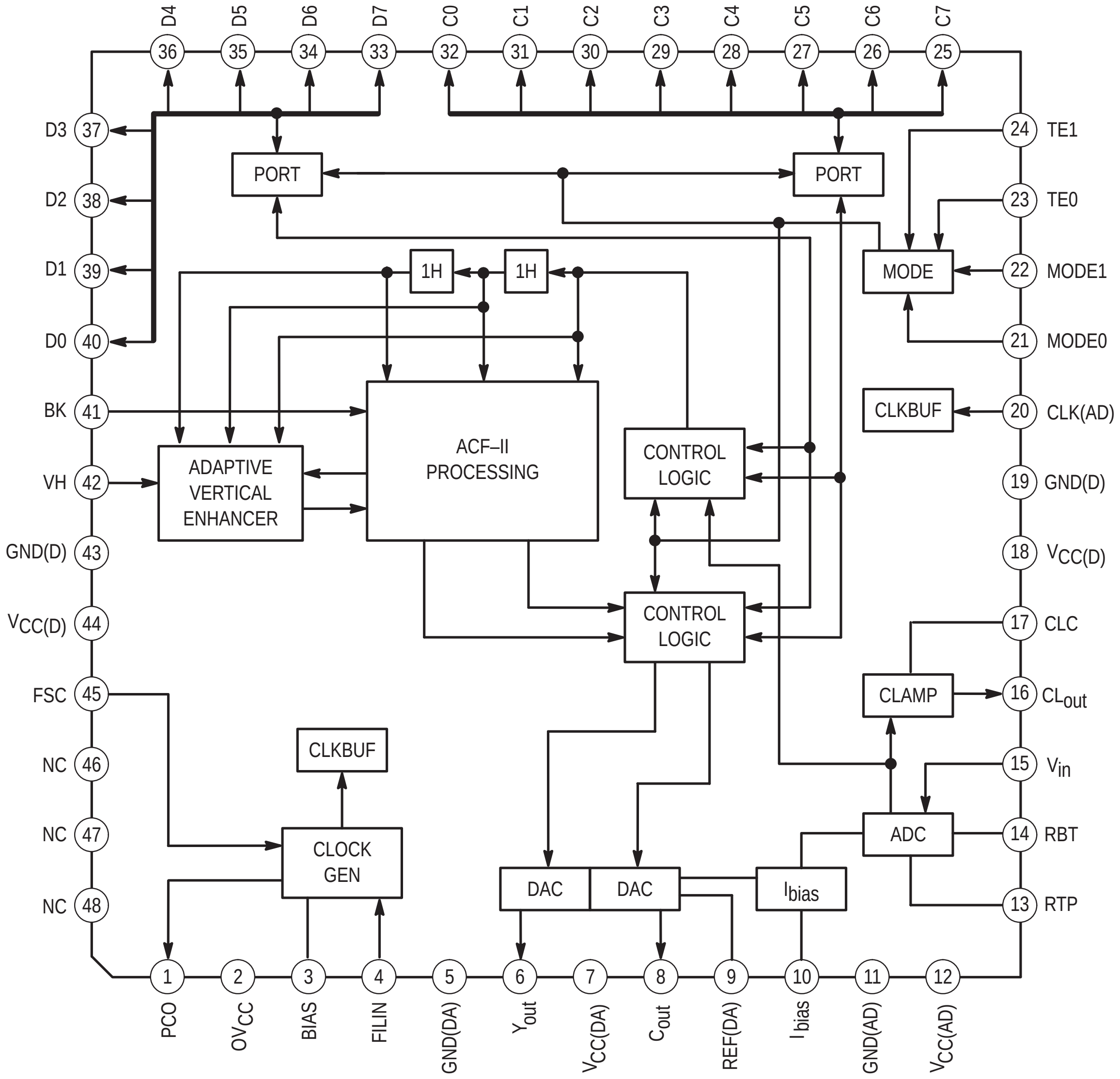
Advanced Comb Filter–II (ACF–II)

MC141622AFU

Case 898

The Advanced Comb Filter–II is a video signal processor for VCRs and TVs. It's function is to separate the Luminance Y and Chrominance C signals from the NTSC composite video signal. The ACF–II minimizes dot–crawl and cross–color. A built–in PLL provides a 4xfsc clock from either an NTSC subcarrier signal or a 4xfsc input. This allows a video signal input of an extended frequency bandwidth. The built–in vertical enhancer circuit improves the quality of the Luminance Y signal. The built–in A/D and D/A converters allow easy connection to analog video circuits.

- Built–in High Speed 8–Bit A/D Converter
- Two Line Memories (1820 Bytes)
- Advanced Comb–II Process
- Vertical Enhancer Circuit
- Two High Speed 8–Bit D/A Converters
- 4xfsc PLL Circuit
- Built–in Clamp Circuit
- Digital Interface Mode
- On–Chip Reference Voltage Regulator for A/D Converter

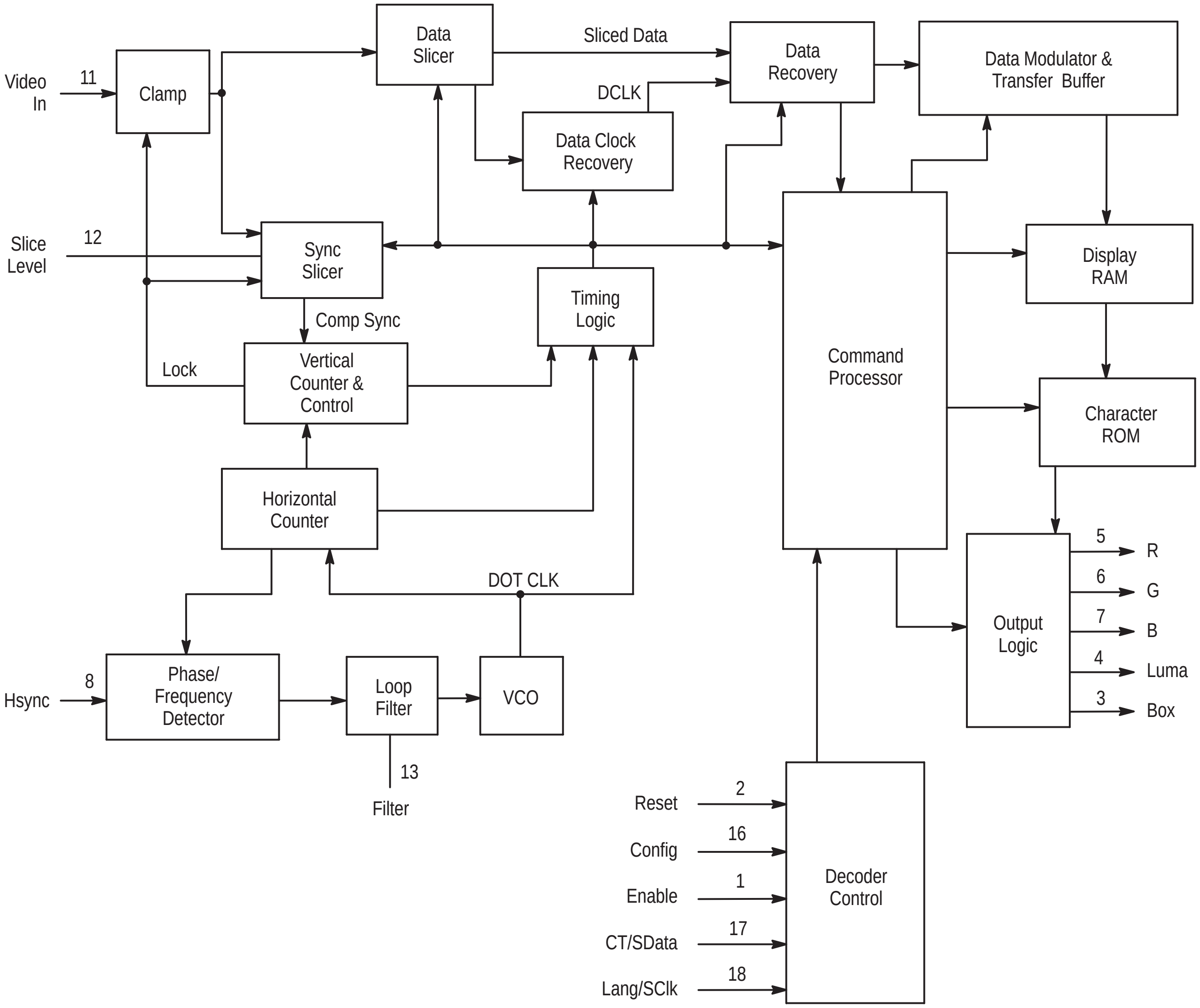


Closed–Caption Decoder

MC144143P
Case 707

The MC144143 is a Line 21 closed–caption decoder for use in television receivers or set top decoders conforming to the NTSC broadcast standard. Capability for processing and displaying all of the latest standard Line 21 closed–caption format transmissions is included. The device requires a closed–caption encoded composite video signal, a horizontal sync signal, and an external keyer to produce captioned video. RGB outputs are provided, along with a luminance and a box signal, allowing simple interface to both color and black and white receivers.

- Conforms to the FCC Report and Order as Amended by the Petition for Reconsideration on Gen. Doc. 91–1
- Supports Four Different Data Channels, Time Multiplexed within the Line 21 Data Stream: Captions Utilizing Languages 1 & 2, Plus Text Utilizing Languages 1 & 2
- Output Logic Provides Hardware Underline Control and Italics Slant Generation
- Single Supply Operating Voltage Range: 4.75 to 5.25 V
- Composite Video Input Range: 0.7 to 1.4 V_{pp}
- Horizontal Sync Input Polarity can be either Positive or Negative
- Internal Timing/Sync Signals Derived from On–Chip VCO



Enhanced Closed–Caption Decoder

MC144144P
Case 707

The MC144144 is a Line 21 closed–caption decoder for use in television receivers or set–top decoders conforming to the NTSC standard. Capability for processing and displaying all of the latest standard Line 21 closed–caption format transmissions is included. The device requires a closed–caption encoded composite video signal, a horizontal sync signal, and an external keyer to produce captioned video. RGB and box signal outputs are provided, which along with the mode select, allow simple interfacing to either color or black–and–white TV receivers.

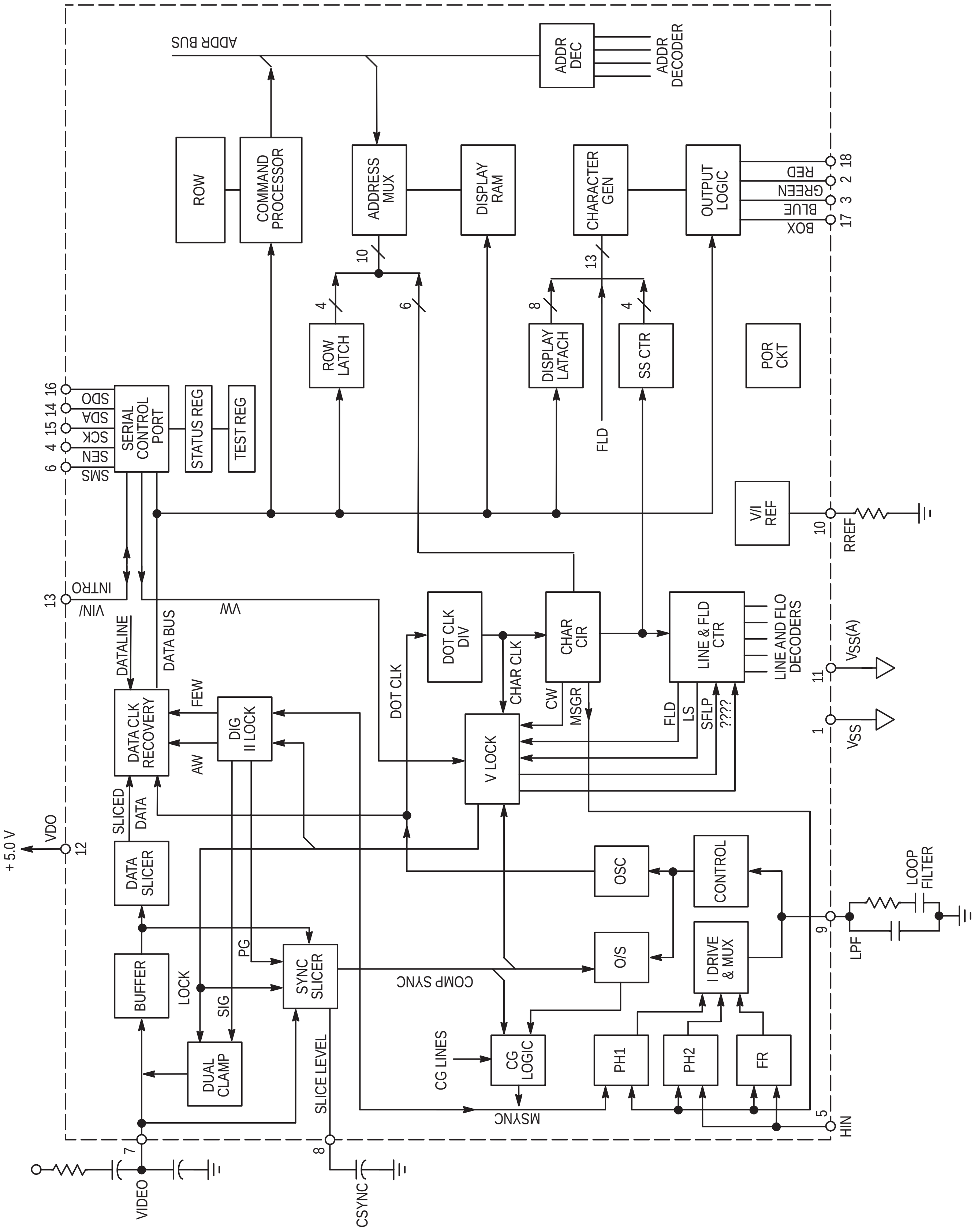
Display storage is accomplished with an on–chip RAM. A modified ASCII character set, which includes several non–English characters, is decoded by an on–chip ROM. An on–screen character appears as a white or colored dot matrix on a black background.

Captions (video–related information) can be up to four rows appearing anywhere on the screen and can be displayed in two modes: roll–up, paint–on, or pop–on. With rollup captions, the row scrolls up and new information appears at the bottom row each time a carriage return is received. Pop–on captions work with two memories. One memory is displayed while the other is used to accumulate new data. A special command causes the information to be exchanged in the two memories, thus causing the entire caption to appear at once.

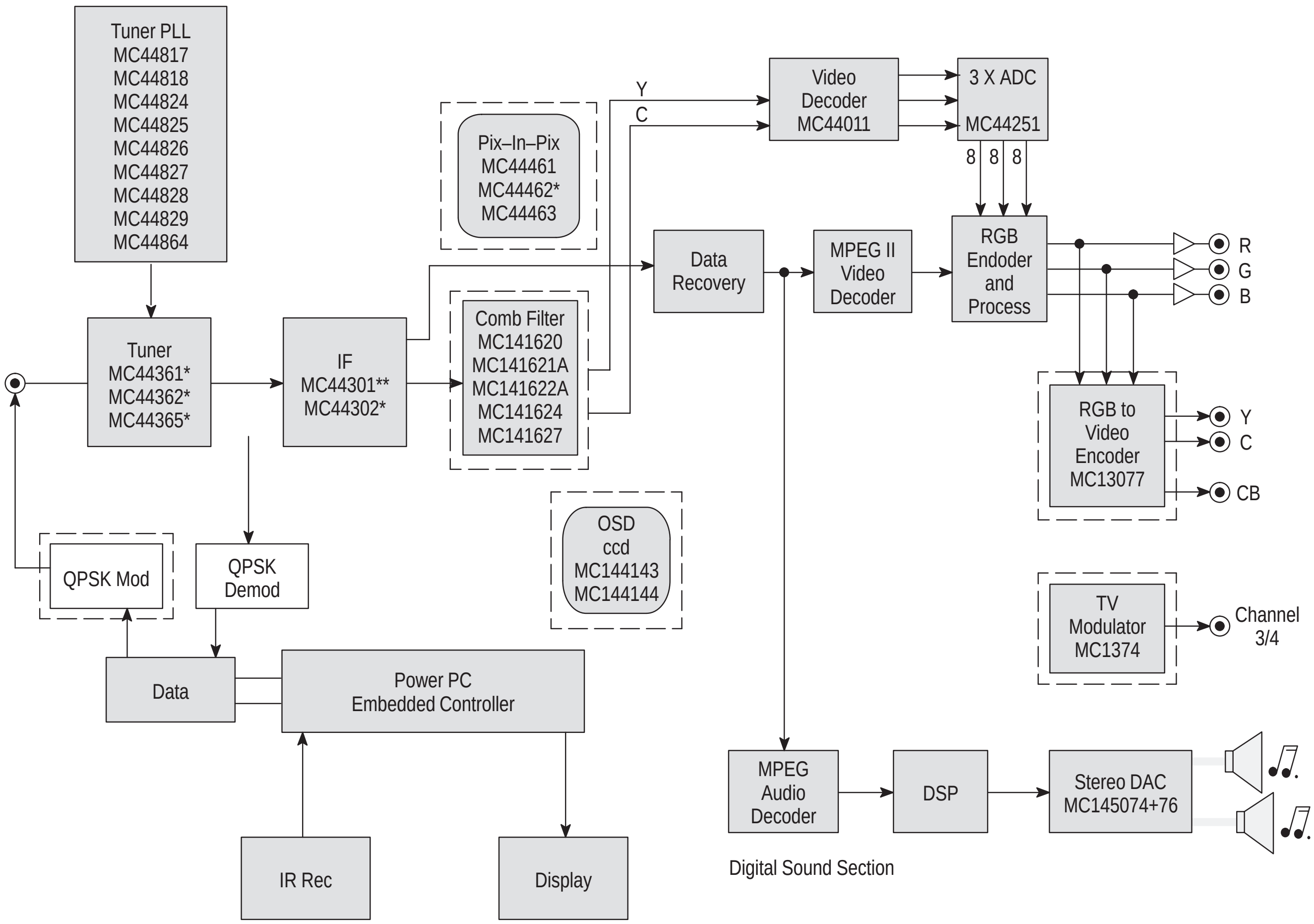
When text (non–video related information) is displayed, the rows contain a maximum of 32 characters over a black box which overwrites the screen. Fifteen rows of characters are displayed in the text mode.

An on–chip processor controls the manipulation of data for storage and display. Also controlled are the loading, addressing, and clearing of the display RAM. The processor transfers the data received to the RAM during scan lines 21 through 42. The operation of the display RAM, character ROM, and output logic circuits are controlled during scan lines 43 through 237. The functions of the MC144144 are controlled via a serial port which may be configured to be either I^2C or SPI.

- Conforms to FCC Report and Order as Amended by the Petition for Reconsideration on Gen. Doc. 91–1
- Conforms to EIA–608 for XDS Data Structure
- Supports Four Different Data Channels for Field 1 and Five Different Data Channels for Field 2, Time Multiplexed within the Line 21 Data Stream: Captions Utilizing Languages 1 and 2, Text Utilizing Languages 1 and 2 and XDS Support
- Output Logic Provides Hardware Underline Control and Italics Slant Generation
- Single Supply, Operating Voltage Range: 4.75 to 5.25 V
- Supply Current: 20 mA (Preliminary)
- Operating Temperature Range: 0 to 70°C
- Composite Video Input Range: 0.7 to 1.4 V_{pp}
- Horizontal Input Polarity: Either Positive or Negative
- Internal Timing and Sync Signals Derived from On–Chip VCO


ADDR BUS
ADDR DEC
ADDR DECODER
ROW
COMMAND PROCESSOR
ADDRESS MUX
DISPLAY RAM
CHARACTER GEN
OUTPUT LOGIC
RED
GREEN
BLUE
BOX
18
2
3
17
10
4
6
13
8
4
ROW LATCH
DISPLAY LATACH
SS CTR
POR CKT
FLD
SMS
SEN
SCK
SDA
SDO
6
4
15
14
16
SERIAL CONTROL PORT
STATUS REG
TEST REG
V/I REF
10
RREF
13
INTRO
VIN/
DATALINE
DATA BUS
VW
DOT CLK DIV
CHAR CIR
LINE & FLD CTR
LINE AND FLD DECODERS
11
VSS(A)
1
VSS
DATA CLK RECOVERY
FEW
AW
DIG II LOCK
DOT CLK
CHAR CLK
CW
MSGR
FLD
LS
SFLP
????
V LOCK
+ 5.0 V
VDO
12
SLICED DATA
DATA SLICER
OSC
CONTROL
LOOP FILTER
9
LPF
BUFFER
LOCK
SIG
PG
SYNC SLICER
COMP SYNC
O/S
I DRIVE & MUX
DUAL CLAMP
SLICE LEVEL
CG LINES
CG LOGIC
PH1
PH2
FR
MSYNC
5
HIN
7
VIDEO
8
CSYNC

Set–Top Block Diagram



* In Development
** Not recommended for new designs.

PLL Tuning Circuits with 3–Wire Bus

MC44817BD, D

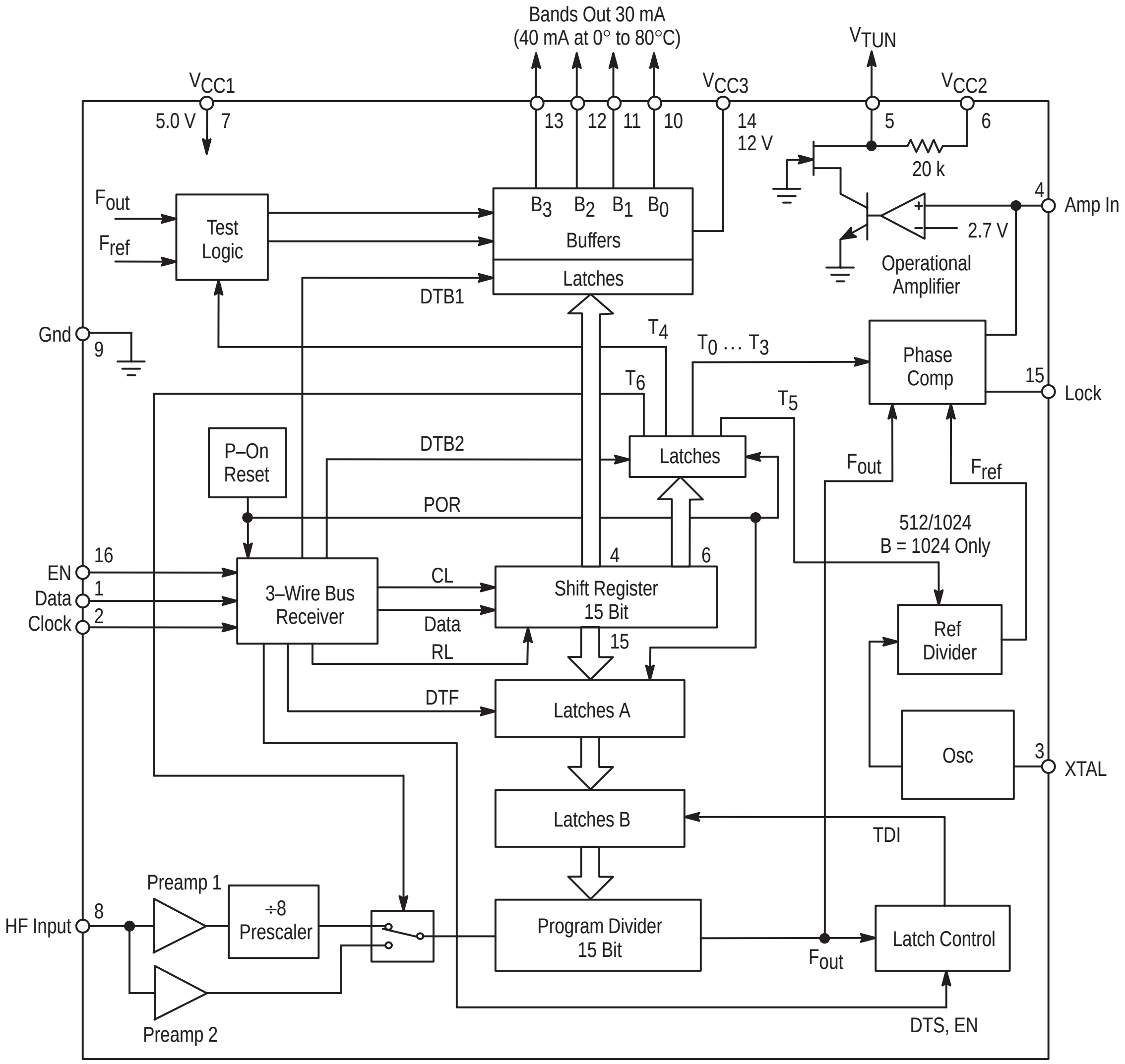
Case 751B

The MC44817/17B are tuning circuits for TV and VCR tuner applications. They contain on one chip all the functions required for PLL control of a VCO. The integrated circuits also contain a high frequency prescaler and thus can handle frequencies up to 1.3 GHz.

The MC44817 has programmable 512/1024 reference dividers while the MC44817B has a fixed reference divider of 1024.

The MC44817/17B are manufactured on a single silicon chip using Motorola's high density bipolar process, MOSAIC™ (Motorola Oxide Self Aligned Implanted Circuits).

- Complete Single Chip System for MPU Control (3–Wire Bus). Data and Clock Inputs are IIC Bus Compatible
- Divide–by–8 Prescaler Accepts Frequencies up to 1.3 GHz
- 15 Bit Programmable Divider Accepts Input Frequencies up to 165 MHz
- Reference Divider: Programmable for Division Ratios 512 and 1024. The MC44817B has a Fixed 1024 Reference Divider
- 3–State Phase/Frequency Comparator
- Operational Amplifier for Direct Tuning Voltage Output (30 V)
- Four Integrated PNP Band Buffers for 40 mA (V_{CC1} to 14.4 V)
- Output Options for the Reference Frequency and the Programmable Divider
- Bus Protocol for 18 or 19 Bit Transmission
- Extra Protocol for 34 Bit for Test and Further Features
- High Sensitivity Preamplifier
- Circuit to Detect Phase Lock
- Fully ESD Protected



PLL Tuning Circuit with I^{2}C Bus

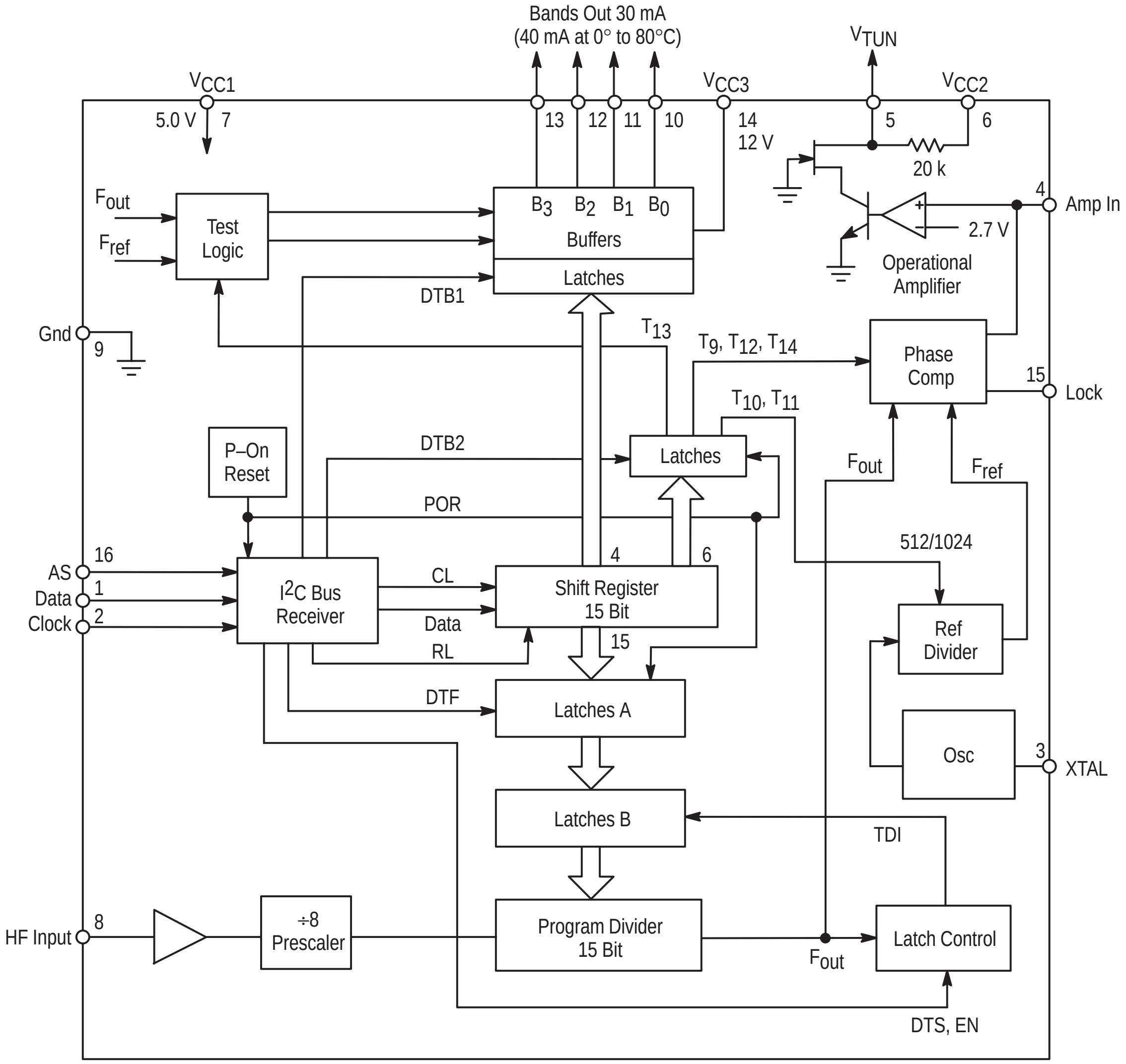
MC44818D

Case 751B

The MC44818 is a tuning circuit for TV and VCR tuner applications. It contains, on one chip, all the functions required for PLL control of a VCO. This integrated circuit also contains a high frequency prescaler and thus can handle frequencies up to 1.3 GHz. The MC44818 is a pin compatible drop–in replacement for the MC44817, where the only difference is the MC44818 has a fixed divide–by–8 prescaler (cannot be bypassed) and the MC44817 uses the three wire bus.

The MC44818 has programmable 512/1024 reference dividers and is manufactured on a single silicon chip using Motorola's high density bipolar process, MOSAIC™ (Motorola Oxide Self Aligned Implanted Circuits).

- Complete Single Chip System for MPU Control (I^{2}C Bus). Data and Clock Inputs are 3–Wire Bus Compatible
- Divide–by–8 Prescaler Accepts Frequencies up to 1.3 GHz
- 15 Bit Programmable Divider Accepts Input Frequencies up to 165 MHz
- Reference Divider: Programmable for Division Ratios 512 and 1024.
- 3–State Phase/Frequency Comparator
- Operational Amplifier for Direct Tuning Voltage Output (30 V)
- Four Integrated PNP Band Buffers for 40 mA (V_{CC1} to 14.4 V)
- Output Options for the Reference Frequency and the Programmable Divider
- High Sensitivity Preamplifier
- Circuit to Detect Phase Lock
- Fully ESD Protected



PLL Tuning Circuits with I^{2}C Bus

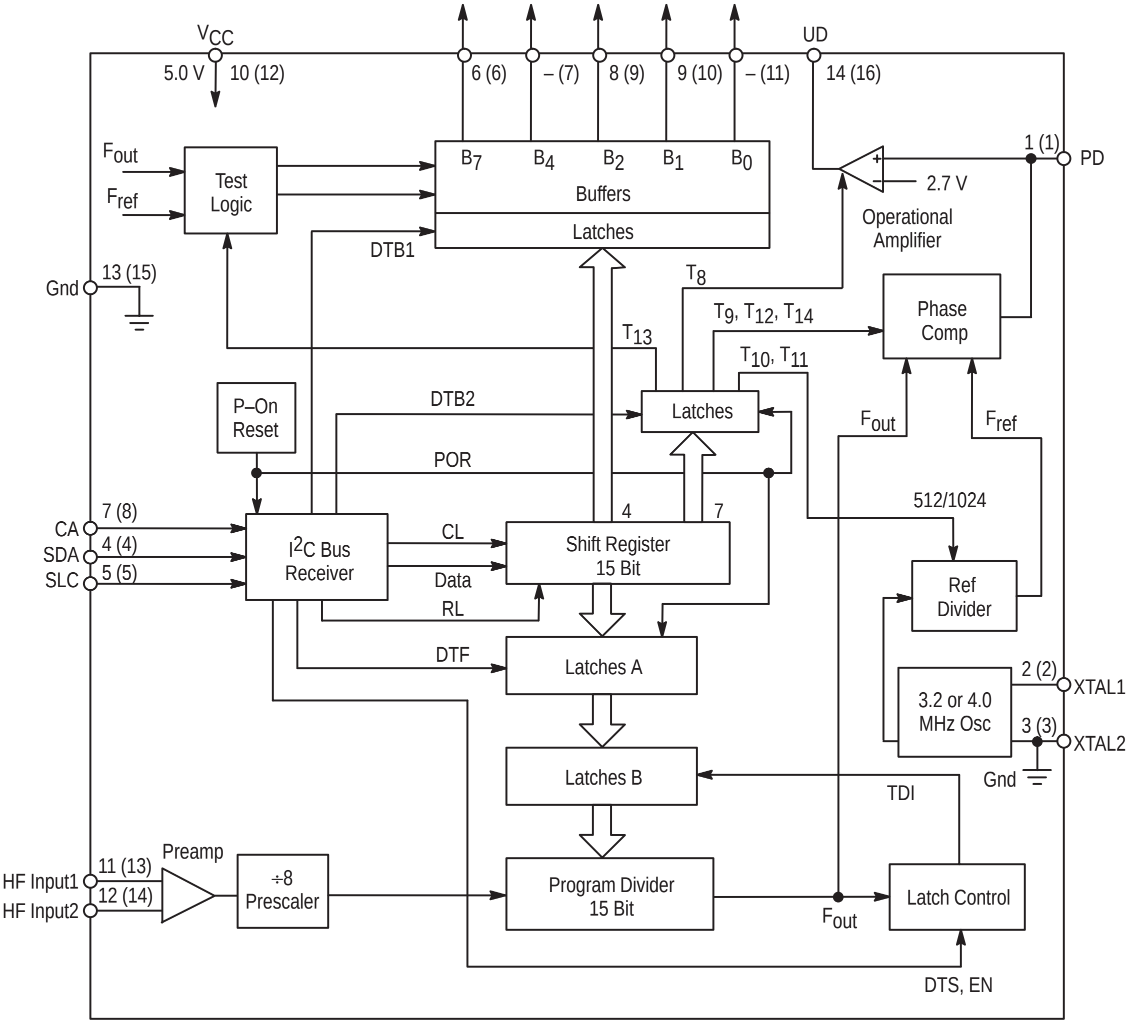
MC44824/25D

Case 751A, 751B

The MC44824/25 are tuning circuits for TV and VCR tuner applications. They contain on one chip all the functions required for PLL control of a VCO. The integrated circuits also contain a high frequency prescaler and thus can handle frequencies up to 1.3 GHz.

The MC44824/25 are manufactured on a single silicon chip using Motorola’s high density bipolar process, MOSAIC™ (Motorola Oxide Self Aligned Implanted Circuits).

- Complete Single Chip System for MPU Control (I^{2}C Bus). Data and Clock Inputs are 3–Wire Bus Compatible
- Divide–by–8 Prescaler Accepts Frequencies up to 1.3 GHz
- 15 Bit Programmable Divider
- Reference Divider: Programmable for Division Ratios 512 and 1024
- 3–State Phase/Frequency Comparator
- 4 Programmable Chip Addresses
- 3 Output Buffers (MC44824) respectively; 5 Output Buffers (MC44825) for 10 mA/15 V
- Operational Amplifier for use with External NPN Transistor
- SO–14 Package for MC44824 and SO–16 for MC44825
- High Sensitivity Preamplifier
- Fully ESD Protected



MC44825 Pin Numbers ( )

PLL Tuning Circuit with 3–Wire Bus

MC44827DTB

Case 948F

The MC44827 is a tuning circuit for TV and VCR tuner applications. This device contains on one chip all the functions required for PLL control of a VCO. This integrated circuit also contains a high frequency prescaler and thus can handle frequencies up to 1.3 GHz.

The MC44827 is controlled by a 3–wire bus. It has the same function as the MC44828 which is I^2C bus controlled. The MC44827 and MC44828 can replace each other to allow conversion between 3–wire bus and I^2C bus control.

The MC44827 is manufactured on a single silicon chip using Motorola's high density bipolar process, MOSAIC™ (Motorola Oxide Self Aligned Implanted Circuits).

The MC44827 has the same features as MC44817 with the following differences:

- Lower Power Consumption, 200 mW Typical
- Improved Prescaler with Higher Margins for Sensitivity and Temperature Range. (A typical device is functional in a temperature range greater than –40 to 100°C.)
- Lock Detector with Push–Pull Output
- No Bypass of Divide–by–8 Prescaler
- TSSOP Package

PLL Tuning Circuit with I^2C Bus

MC44828DTB

Case 948F

The MC44828 is a tuning circuit for TV and VCR tuner applications. This device contains on one chip all the functions required for PLL control of a VCO. This integrated circuit also contains a high frequency prescaler and thus can handle frequencies up to 1.3 GHz.

The MC44828 is controlled by an I^2C bus. It has the same function as the MC44827 which is 3–wire bus controlled. The MC44827 and MC44828 can replace each other to allow conversion between 3–wire bus and I^2C bus control.

The MC44828 is manufactured on a single silicon chip using Motorola's high density bipolar process, MOSAIC™ (Motorola Oxide Self Aligned Implanted Circuits).

The MC44828 has the same features as MC44818 with the following differences:

- Lower Power Consumption, 200 mW Typical
- Improved Prescaler with Higher Margins for Sensitivity and Temperature Range. (A typical device is functional in a temperature range greater than –40 to 100°C.)
- Lock Detector with Push–Pull Output
- TSSOP Package

PLL Tuning Circuit with I^2C Bus

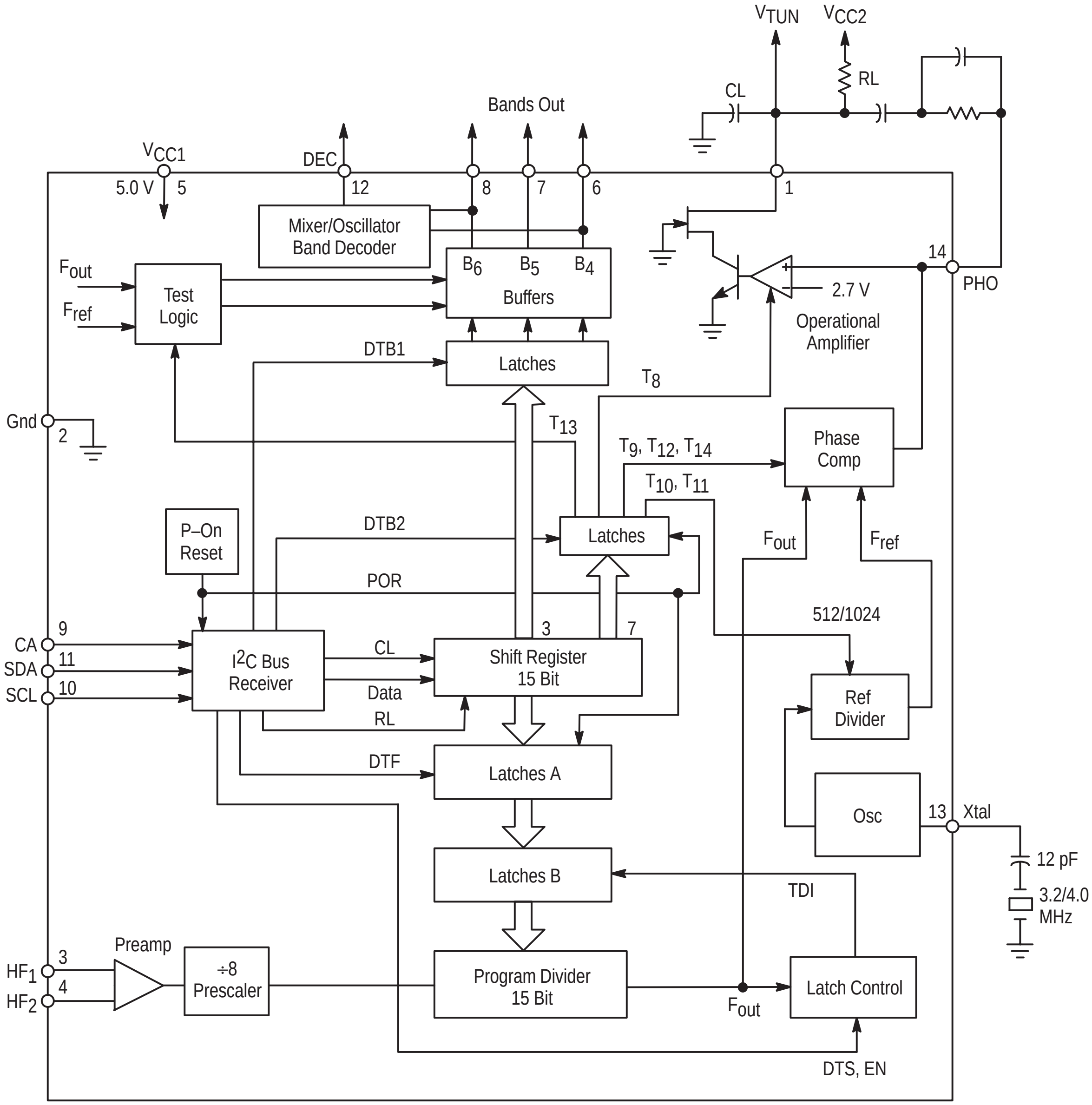
MC44829D

Case 751A

The MC44829 is a tuning circuit for TV and VCR tuner applications. It contains, on one chip, all the functions required for PLL control of a VCO. This integrated circuit also contains a high frequency prescaler and thus can handle frequencies up to 1.3 GHz. The circuit has a band decoder that provides the band switching signal for the mixer/oscillator circuit. The decoder is controlled by the buffer bits.

The MC44829 has programmable 512/1024 reference dividers and is manufactured on a single silicon chip using Motorola's high density bipolar process, MOSAIC™ (Motorola Oxide Self Aligned Implanted Circuits).

- Complete Single Chip System for MPU Control (I^2C Bus)
- Divide–by–8 Prescaler Accepts Frequencies up to 1.3 GHz
- 15 Bit Programmable Divider
- Reference Divider: Programmable for Division Ratios 512 and 1024
- 3–State Phase/Frequency Comparator
- Operational Amplifier for Direct Tuning Voltage Output (30 V)
- Four Programmable Chip Addresses
- Integrated Band Decoder for the Mixer/Oscillator Circuit
- Band Buffers with Low "On" Voltage (0.4 V Maximum at 5.0 mA)
- Fully ESD Protected to MIL–STD–883C, Method 3015.7 (2000 V, 1.5 kΩ, 150 pF)



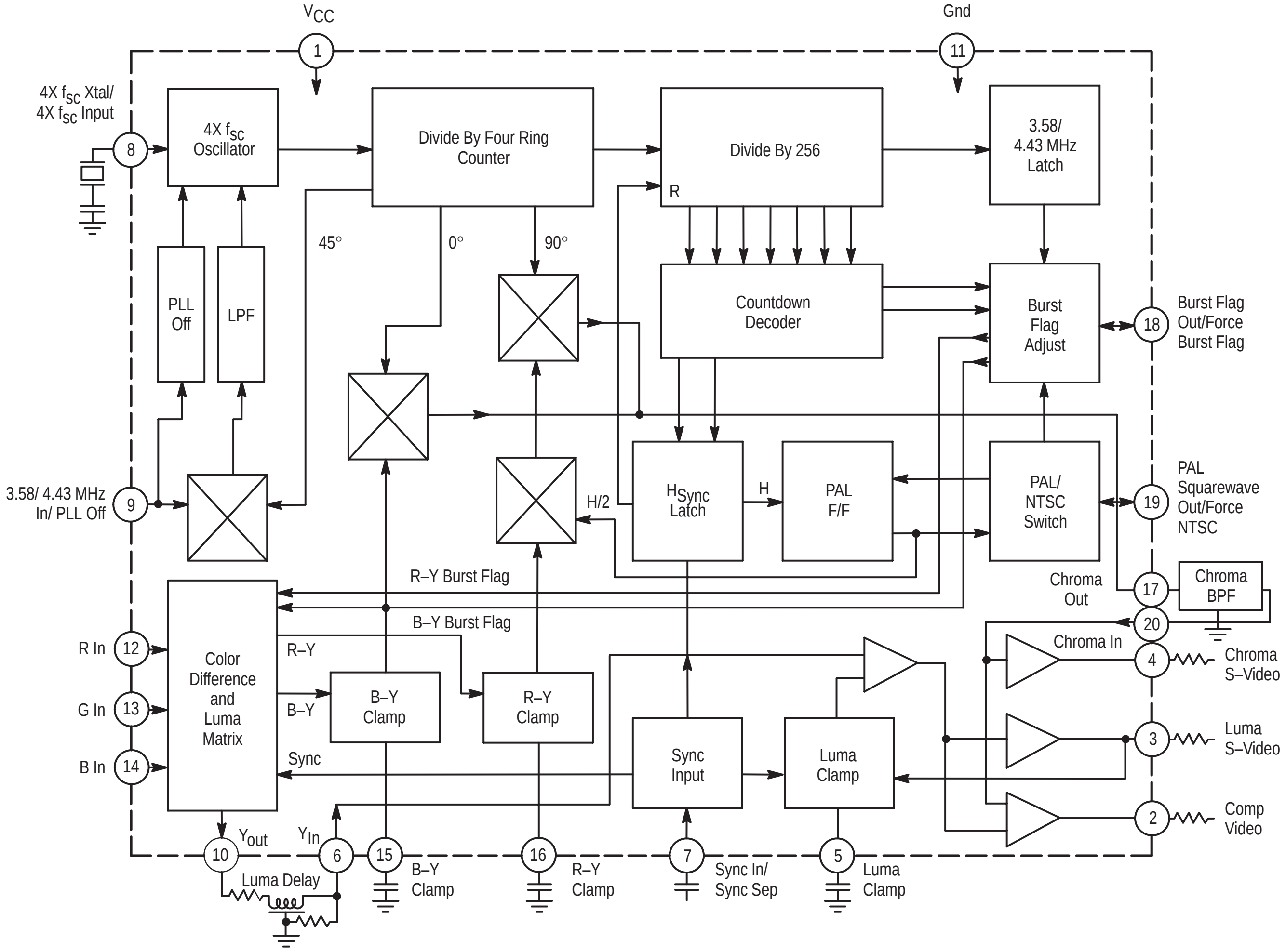
Advanced PAL/NTSC Encoder

MC13077P, DW

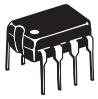
Case 738, 751D

The MC13077 is an economical, high quality, RGB encoder for PAL or NTSC applications. It accepts red, green, blue and composite sync inputs and delivers either composite PAL or NTSC video, and S–Video Chroma and Luma outputs. The MC13077 is manufactured using Motorola's high density, bipolar MOSAIC® process.

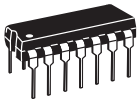
- Single 5.0 V Supply
- Composite Output
- S–Video Outputs
- PAL/NTSC Switchable
- PAL Squarewave Output
- PAL Sequence Resettable
- Internal/External Burst Flag
- Modulator Angles Accurate to 90°
- Burst Position/Duration Determined Digitally
- Subcarrier Reference from a Crystal or External Source



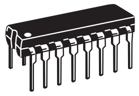
Consumer Electronic Circuits Package Overview



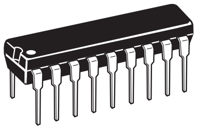
CASE 626
P SUFFIX



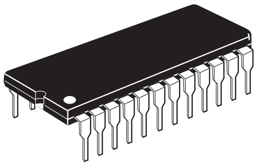
CASE 646
P SUFFIX



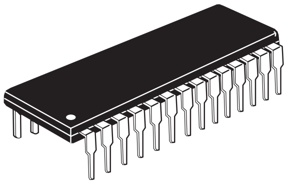
CASE 648
P SUFFIX



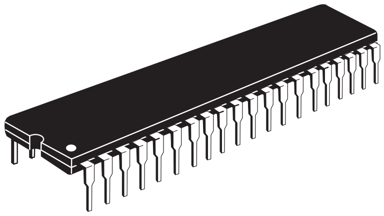
CASE 707
P SUFFIX



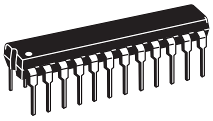
CASE 709
P SUFFIX



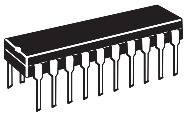
CASE 710
P SUFFIX



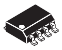
CASE 711
P SUFFIX



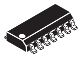
CASE 724
P SUFFIX



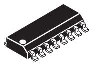
CASE 738
H, P SUFFIX



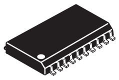
CASE 751
D SUFFIX



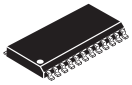
CASE 751A
D SUFFIX



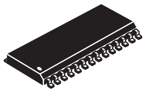
CASE 751B
D SUFFIX



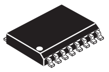
CASE 751D
DW SUFFIX



CASE 751E
DW SUFFIX

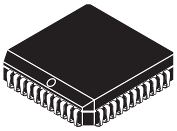


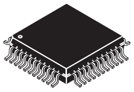
CASE 751F
DW SUFFIX

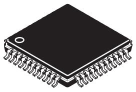


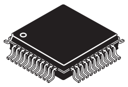
CASE 751G
DW SUFFIX

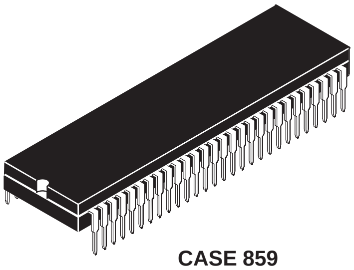
Consumer Electronic Circuits Package Overview (continued)

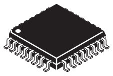

CASE 777
FN SUFFIX

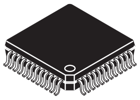

CASE 824, 824A
FB SUFFIX

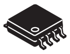

CASE 824D
FTB SUFFIX

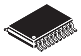

CASE 824E
FB SUFFIX

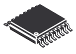

CASE 859
B SUFFIX


CASE 873
FU SUFFIX

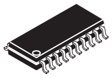

CASE 898
FB, FU, P SUFFIX


CASE 904
F SUFFIX


CASE 948E
DTB SUFFIX


CASE 948F
DTB SUFFIX


CASE 948J
DTB SUFFIX


CASE 967
M SUFFIX

Device Listing and Related Literature

Entertainment Radio Receiver Circuits

Device	Function	Page
MC3340	Electronic Attenuator	9–66
MC13020	Motorola C-QUAM AM Stereo Decoder	9–76
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MC13022A	Advanced Medium Voltage AM Stereo Decoder	9–86
MC13025	Electronically Tuned Radio Front End	9–91
MC13027, MC13122	AMAX Stereo Chipset	9–94
MC13028A	Advanced Wide Voltage IF and C–QUAM AM Stereo Decoder	9–119
MC13029A	Advanced Medium Voltage IF and C–QUAM AM Stereo Decoder with FM Amplifier and AM/FM Internal Switch	9–137
MC13030	Dual Conversion AM Receiver	9–156
MC13060	Mini-Watt Audio Output	9–171
MC34119	Low Power Audio Amplifier	9–227

Video Circuits

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MC1350	Monolithic IF Amplifier	9–30
MC1374	TV Modulator Circuit	9–34
MC1377	Color Television RGB to PAL/NTSC Encoder	9–42
MC1378	Color Television Composite Video Overlay Synchronizer	9–58
MC1391	TV Horizontal Processor	9–62
MC3346	General Purpose Transistor Array One Differentially Connected Pair and Three Isolated Transistor Arrays	9–69
MC13077	Advanced PAL/NTSC Encoder	9–175
MC13081X	Multimode Color Monitor Horizontal, Vertical, and Video Combination Processor	9–187
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MC13282A	100 MHz Video Processor with OSD Interface	9–215
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MC44002, MC44007	Chroma 4 Multistandard Video Processor	9–236
MC44011	Bus Controlled Multistandard Video Processor	9–275
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MC44144	Subcarrier Phase–Locked Loop	9–326
MC44145	Pixel Clock Generator/Sync Separator	9–331
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MC44462	Y–C Picture–in–Picture (PIP) Controller	9–354
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Video Circuits (continued)

Device	Function	Page
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MC44818	PLL Tuning Circuit with I^{2}C Bus	9–374
MC44824, MC44825	PLL Tuning Circuits with I^{2}C Bus	9–381
MC44826	PLL Tuning Circuit with I^{2}C Bus	9–388
MC44827	PLL Tuning Circuit with 3–Wire Bus	9–395
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MC44829	PLL Tuning Circuit with I^{2}C Bus	9–397
MC44864	PLL Tuning Circuit with 1.3 GHz Prescaler and D/A Converters for Automatic Tuner Alignment	9–405

Remote Control Circuit

Device	Function	Page
MC3373*	Remote Control Amplifier/Detector	9–72

RELATED APPLICATION NOTES

App Note	Title	Related Device
AN545A	Television IF Amplifiers	**MC1350**
AN829	Application of the MC1374 TV Modulator	**MC1374**
AN921	Horizontal APC/AFC Loops	**MC1391**
AN932	Application of the MC1377 Color Encoder	**MC1377**
AN1044	A Monolithic Composite Video Synchronizer	**MC1378**
AN1548	Guidelines for Debugging the MC44011 Video Decoder	**MC44011**

NOTE: * Not recommended for new designs.

MOTOROLA

CA3146

General Purpose Transistor Array

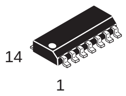
One Differentially Connected Pair and Three Isolated Transistor Arrays

The CA3146 is designed for general purpose, low power applications in the dc through VHF range.

- Guaranteed Base–Emitter Voltage Matching
- Operating Current Range Specified: 10 µA to 10 mA
- Five General Purpose Transistors in One Package

GENERAL PURPOSE TRANSISTOR ARRAY

SEMICONDUCTOR TECHNICAL DATA



D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO–14)

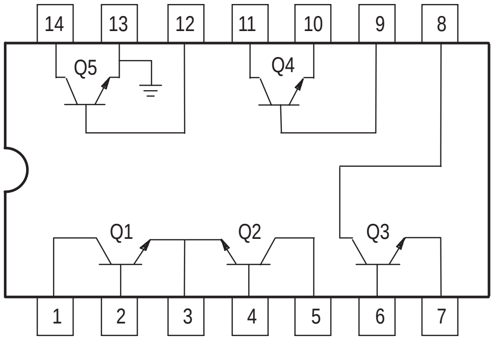
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	130	Vdc
Collector–Base Voltage	V_{CBO}	20	Vdc
Collector–Substrate Voltage	V_{CIO}	20	Vdc
Emitter–Base Voltage	V_{EBO}	5.0	Vdc
Collector Current	I_C	50	mAdc
Operating Temperature Range	T_A	–40 to +85	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

ORDERING INFORMATION

Device	Operating Temperature Range	Package
CA3146D	T_A = – 40° to +85°C	SO–14

PIN CONNECTIONS



Pin 13 is connected to substrate and must remain at the lowest circuit potential.

ELECTRICAL CHARACTERISTICS

Characteristics	Symbol	Min	Typ	Max	Unit
STATIC CHARACTERISTICS					
Collector–Base Breakdown Voltage (I_C = 10 μAdc)	$V_{(BR)CBO}$	40	89	–	Vdc
Collector–Emitter Breakdown Voltage (I_C = 1.0 mAdc)	$V_{(BR)CEO}$	35	45	–	Vdc
Collector–Substrate Breakdown Voltage (I_{CI} = 10 μA)	$V_{(BR)CIO}$	40	85	–	Vdc
Emitter–Base Breakdown Voltage (I_E = 10 μA)	$V_{(BR)EBO}$	5.0	–	–	Vdc
Collector–Base Cutoff Current (V_{CB} = 10 Vdc, I_E = 0)	I_{CBO}	–	0.68	40	nAdc
DC Current Gain (I_C = 10 mAdc, V_{CE} = 5.0 Vdc) (I_C = 1.0 mAdc, V_{CE} = 5.0 Vdc)	h_{FE}	– –	171 188	– –	–
Base–Emitter Voltage (V_{CE} = 5.0 Vdc, I_E = 1.0 mAdc)	V_{BE}	–	0.7	–	Vdc
Collector–Emitter Saturation Voltage (I_C = 10 mA, I_B = 0.4 mA)	$V_{CE(sat)}$	–	0.28	0.5	Vdc
Magnitude of Input Offset Current $\|I_{IO1} – I_{IO2}\|$ (V_{CE} = 5.0 Vdc, $I_{C1} = I_{C2}$ = 1.0 mAdc)	I_{IO}	–	0.03	2.0	μAdc
Magnitude of Input Offset Voltage $\|V_{BE1} = V_{BE2}\|$ (V_{CE} = 5.0 Vdc, I_E = 1.0 mAdc)	$\|V_{IO}\|$	–	0.13	2.0	mVdc
DYNAMIC CHARACTERISTICS					
Low Frequency Noise Figure (V_{CE} = 5.0 Vdc, I_C = 100 μAdc, R_S = 1.0 kΩ, f = 1.0 kHz)	NF	–	3.25	–	dB
Forward Current Transfer Ratio (V_{CE} = 5.0 Vdc, I_C = 1.0 mAdc, f = 1.0 kHz)	h_{fe}	–	201.5	–	–
Short Circuit Input Impedance (V_{CE} = 5.0 Vdc, I_C = 1.0 mAdc, f = 1.0 kHz)	h_{ie}	–	6.7	–	kΩ
Open Circuit Output Impedance (V_{CE} = 5.0 Vdc, I_C = 1.0 mAdc, f = 1.0 kHz)	h_{oe}	–	15.6	–	μmho
Reverse Voltage Transfer Ratio (V_{CE} = 5.0 Vdc, I_C = 1.0 mAdc, f = 1.0 kHz)	h_{re}	–	3.5	–	$X10^{–4}$
Input Admittance (V_{CE} = 5.0 Vdc, I_C = 1.0 mAdc, f = 1.0 kHz)	Y_{ie}	–	0.14 + j0.16	–	mmho
Forward Transfer Admittance (V_{CE} = 5.0 Vdc, I_C = 1.0 mAdc, f = 1.0 kHz)	Y_{fe}	–	34.6 – j0.63	–	mmho
Reverse Transfer Admittance (V_{CE} = 5.0 Vdc, I_C = 1.0 mAdc, f = 1.0 kHz)	Y_{re}	–	62.0 – j59.4	–	μmho
Output Admittance (V_{CE} = 5.0 Vdc, I_C = 1.0 mAdc, f = 1.0 kHz)	Y_{oe}	–	0.16 + j0.14	–	mmho
Current–Gain – Bandwidth Product (V_{CE} = 5.0 Vdc, I_C = 3.0 mAdc)	f_T	300	500	–	MHz
Emitter–Base Capacitance (V_{EB} = 5.0 Vdc, I_E = 0 mAdc)	C_{EB}	–	1.17	–	pF
Collector–Base Capacitance (V_{CB} = 5.0 Vdc, I_E = 0 mAdc)	C_{CB}	–	0.68	–	pF
Collector–Substrate Capacitance (V_{CS} = 5.0 Vdc, I_C = 0 mAdc)	C_{CI}	–	1.92	–	pF

MC1350

Monolithic IF Amplifier

The MC1350 is an integrated circuit featuring wide range AGC for use as an IF amplifier in radio and TV over an operating temperature range of 0° to +75°C.

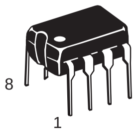
- Power Gain: 50 dB Typ at 45 MHZ
  50 dB Typ at 58 MHZ
- AGC Range: 60 dB Min, DC to 45 MHz
- Nearly Constant Input & Output Admittance over the Entire AGC Range
- Y_{21} Constant (–3.0 dB) to 90 MHz
- Low Reverse Transfer Admittance: < < 1.0 µmho Typ
- 12 V Operation, Single–Polarity Power Supply

MAXIMUM RATINGS (T_A = +25°C, unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V^+	+18	Vdc
Output Supply Voltage	V_1, V_8	+18	Vdc
AGC Supply Voltage	V_{AGC}	V^+	Vdc
Differential Input Voltage	V_{in}	5.0	Vdc
Power Dissipation (Package Limitation) Plastic Package Derate above 25°C	P_D	 625 5.0	 mW mW/°C
Operating Temperature Range	T_A	0 to +75	°C

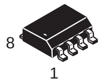
IF AMPLIFIER

SEMICONDUCTOR TECHNICAL DATA



P SUFFIX
PLASTIC PACKAGE
CASE 626

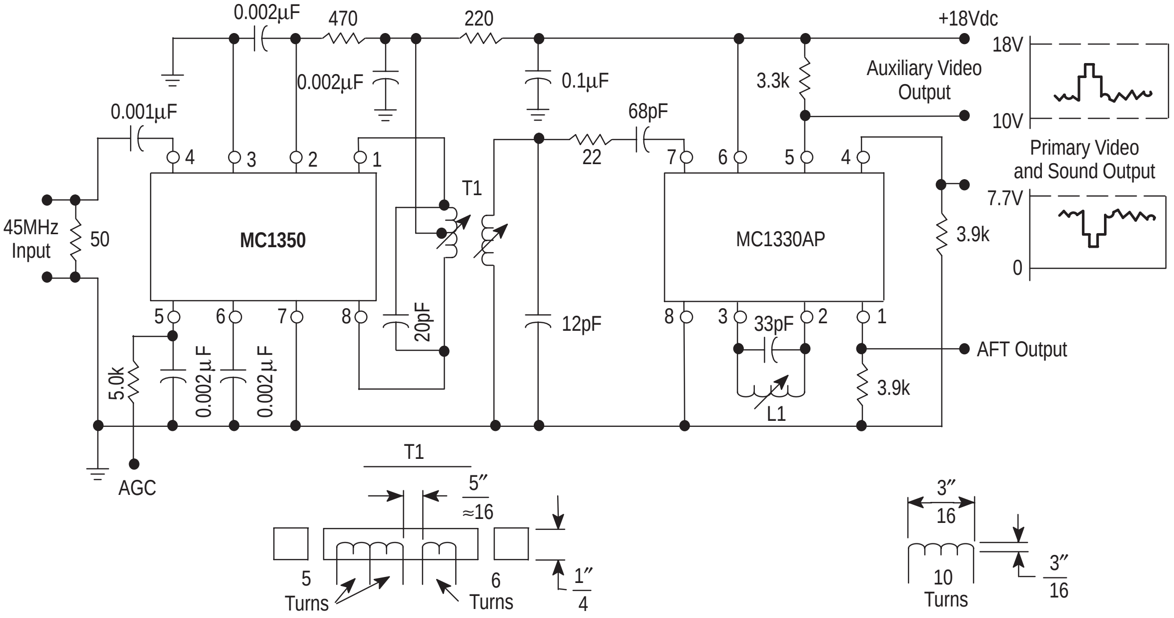
D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)



ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC1350P	T_A = 0° to +75°C	Plastic DIP
MC1350D		SO–8

Figure 1. Typical MC1350 Video IF Amplifier and MC1330 Low–Level Video Detector Circuit



All windings #30 AWG tinned nylon acetate wire tuned with Carbonyl E or J slugs.

L1 wound with #26 AWG tinned nylon acetate wire tuned by distorting winding.

ELECTRICAL CHARACTERISTICS (V^+ = +12 Vdc, T_A = +25°C, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
AGC Range, 45 MHz (5.0 V to 7.0 V) (Figure 1)		60	68	–	dB
Power Gain (Pin 5 grounded via a 5.1 kΩ resistor) f = 58 MHz, BW = 4.5 MHz See Figure 6(a) f = 45 MHz, BW = 4.5 MHz See Figure 6(a), (b) f = 10.7 MHz, BW = 350 kHz See Figure 7 f = 455 kHz, BW = 20 kHz	A_p	 – 46 – –	 48 50 58 62	 – – – –	dB
Maximum Differential Voltage Swing 0 dB AGC –30 dB AGC	V_O	 – –	 20 8.0	 – –	V_{pp}
Output Stage Current (Pins 1 and 8)	$I_1 + I_8$	–	5.6	–	mA
Total Supply Current (Pins 1, 2 and 8)	I_S	–	14	17	mAdc
Power Dissipation	P_D	–	168	204	mW

DESIGN PARAMETERS, Typical Values (V^+ = +12 Vdc, T_A = +25°C, unless otherwise noted.)

		Frequency				
Parameter	Symbol	455 kHz	10.7 MHz	45 MHz	58 MHz	Unit
Single–Ended Input Admittance	g_{11} b_{11}	0.31 0.022	0.36 0.50	0.39 2.30	0.5 2.75	mmho
Input Admittance Variations with AGC (0 dB to 60 dB)	Δg_{11} Δb_{11}	– –	– –	60 0	– –	µmho
Differential Output Admittance	g_{22} b_{22}	4.0 3.0	4.4 110	30 390	60 510	µmho
Output Admittance Variations with AGC (0 dB to 60 dB)	Δg_{22} Δb_{22}	– –	– –	4.0 90	– –	µmho
Reverse Transfer Admittance (Magnitude)	$\lvert y_{12} \rvert$	< < 1.0	< < 1.0	< < 1.0	< < 1.0	µmho
Forward Transfer Admittance Magnitude Angle (0 dB AGC) Angle (–30 dB AGC)	 $\lvert y_{21} \rvert$ $< y_{21}$ $< y_{21}$	 160 –5.0 –3.0	 160 –20 –18	 200 –80 –69	 180 –105 –90	 mmho Degrees Degrees
Single–Ended Input Capacitance	C_{in}	7.2	7.2	7.4	7.6	pF
Differential Output Capacitance	C_O	1.2	1.2	1.3	1.6	pF

Figure 2. Typical Gain Reduction

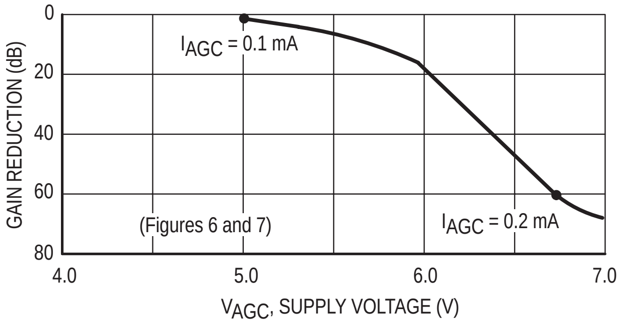
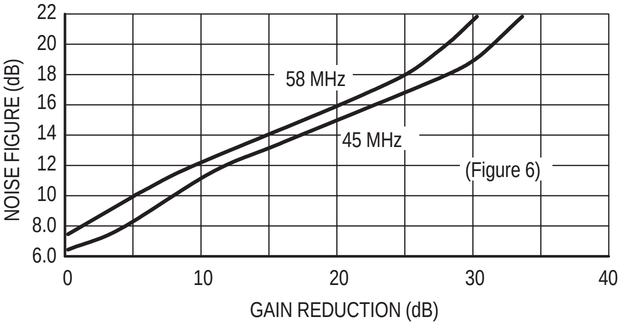


Figure 3. Noise Figure versus Gain Reduction



GENERAL OPERATING INFORMATION

The input amplifiers (Q1 and Q2) operate at constant emitter currents so that input impedance remains independent of AGC action. Input signals may be applied single–ended or differentially (for ac) with identical results. Terminals 4 and 6 may be driven from a transformer, but a dc path from either terminal to ground is not permitted.

AGC action occurs as a result of an increasing voltage on the base of Q4 and Q5 causing these transistors to conduct more heavily thereby shunting signal current from the interstage amplifiers Q3 and Q6. The output amplifiers are supplied from an active current source to maintain constant quiescent bias thereby holding output admittance nearly constant. Collector voltage for the output amplifier must be supplied through a center–tapped tuning coil to Pins 1 and 8. The 12 V supply (V^+) at Pin 2 may be used for this purpose, but output admittance remains more nearly constant if a separate 15 V supply (V^{++}) is used, because the base voltage on the output amplifier varies with AGC bias.

Figure 4. Circuit Schematic

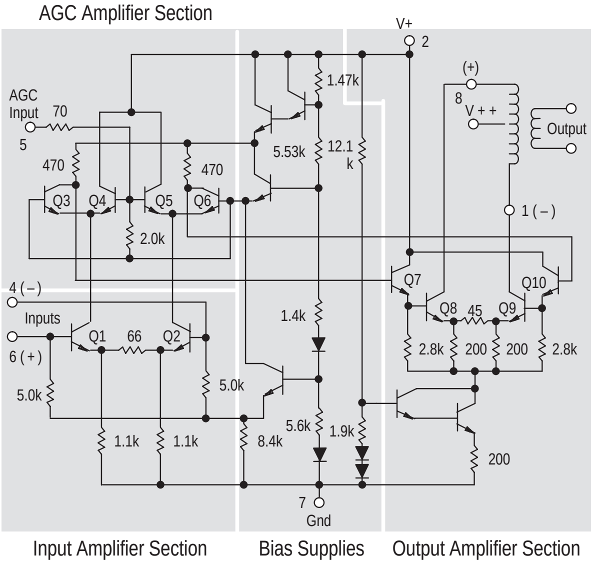


Figure 5. Frequency Response Curve (45 MHz and 58 MHz)

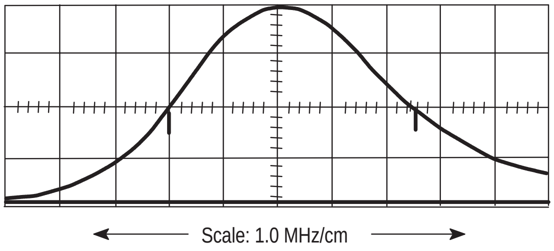
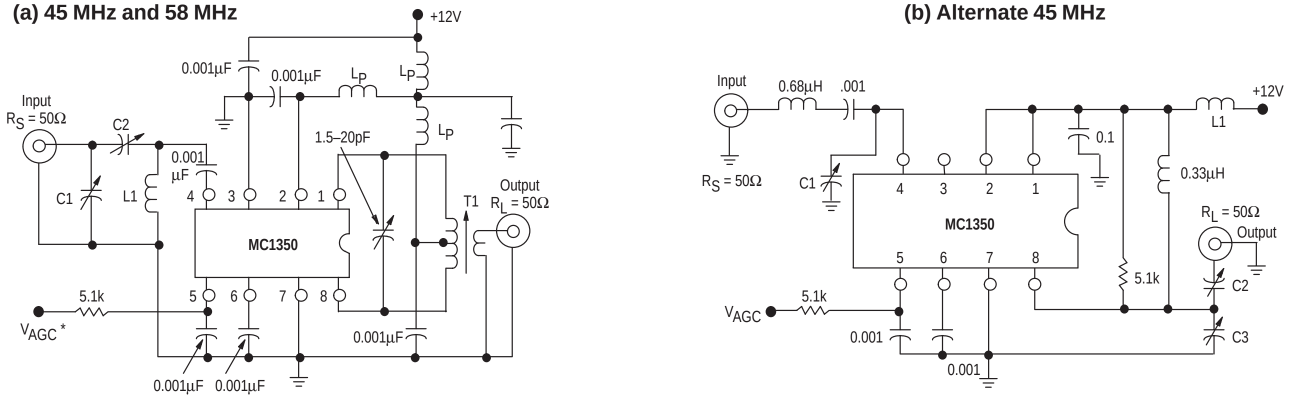


Figure 6. Power Gain, AGC and Noise Figure Test Circuits


(a) 45 MHz and 58 MHz

(b) Alternate 45 MHz

*Connect to ground for maximum power gain test.
All power supply chokes (Lp), are self–resonant at input frequency. $L_P \geq 20\ k\Omega$.
See Figure 5 for Frequency Response Curve.

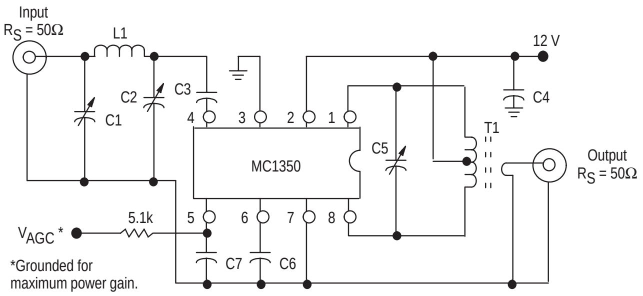
L1 @ 45 MHz = 7 1/4 Turns on a 1/4″ coil form
@ 58 MHz = 6 Turns on a 1/4″ coil form

T1 Primary Winding = 18 Turns on a 1/4″ coil form, center–tapped, #25 AWG
Secondary Winding = 2 Turns centered over Primary Winding @ 45 MHz
= 1 Turn @ 58 MHz
Slug = Carbonyl E or J

L1	Ferrite Core 14 Turns 28 S.W.G.
C1	5–25 pF
C2	5–25 pF
C3	5–25 pF

	45 MHz		58 MHz	
L1	0.4 µH	Q ≥ 100	0.3 µH	Q ≥ 100
T1	1.3 µH to 3.4 µH	Q ≥ 100 @ 2.0 µH	1.2 µH to 3.8 µH	Q ≥ 100 @ 2.0 µH
C1	50 pF to160 pF		8.0 pF to 60 pF	
C2	8.0 pF to 60 pF		3.0 pF to 35 pF	

Figure 7. Power Gain and AGC Test Circuit (455 kHz and 10.7 MHz)



Component	Frequency	
	455 kHz	10.7 MHz
C1	–	80–450 pF
C2	–	5.0–80 pF
C3	0.05 µF	0.001 µF
C4	0.05 µF	0.05 µF
C5	0.001 µF	36 pF
C8	0.05 µF	0.05 µF
C7	0.05 µF	0.05 µF
L1	–	4.6 µF
T1	Note 1	Note 2

NOTES: 1. Primary: 120 µH (center–tapped)
Q_u = 140 at 455 kHz
Primary: Secondary turns ratio ≈ 13
2. Primary: 6.0 µH
Primary winding = 24 turns #36 AWG
(close–wound on 1/4″ dia. form)
Core = Carbonyl E or J
Secondary winding = 1–1/2 turns #36 AWG, 1/4″ dia.
(wound over center–tap)

Figure 8. Single–Ended Input Admittance

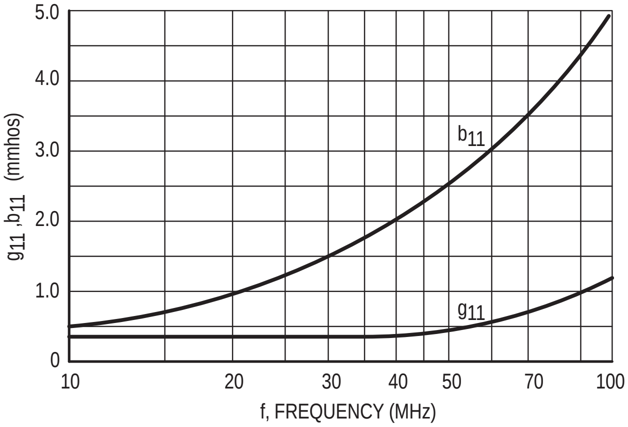


Figure 9. Forward Transfer Admittance

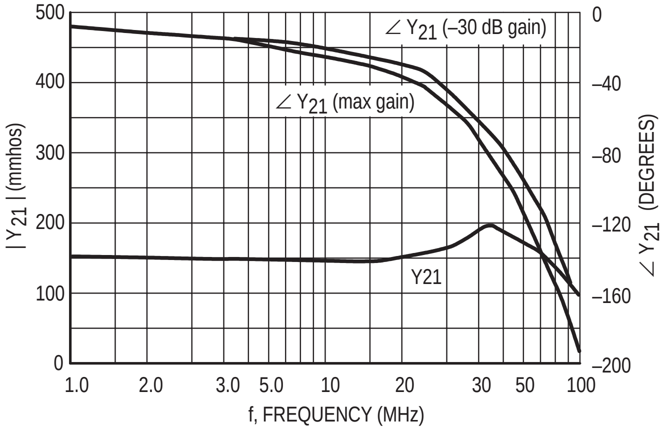


Figure 10. Differential Output Admittance

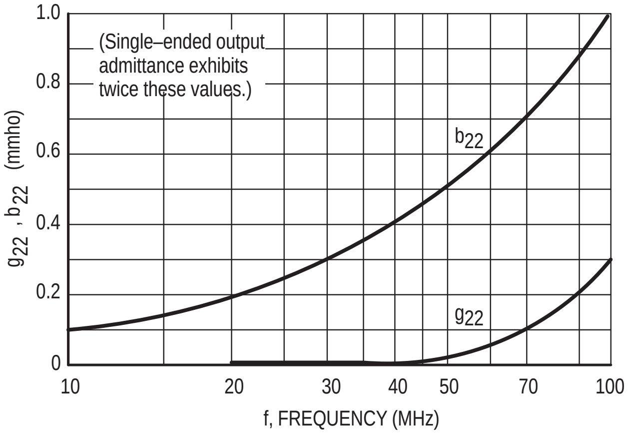
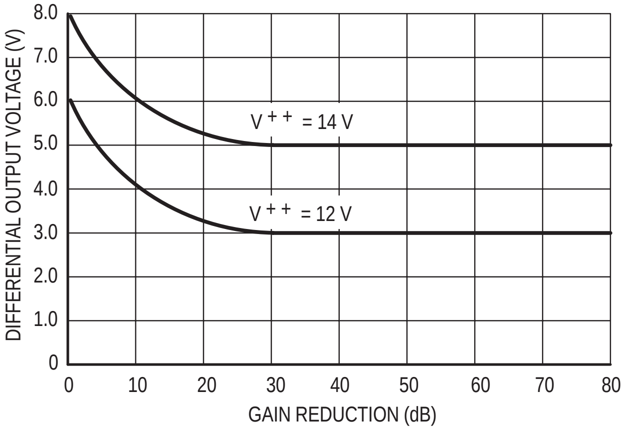


Figure 11. Differential Output Voltage



MOTOROLA

MC1374

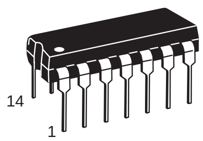
TV Modulator Circuit

The MC1374 includes an FM audio modulator, sound carrier oscillator, RF oscillator, and RF dual input modulator. It is designed to generate a TV signal from audio and video inputs. The MC1374's wide dynamic range and low distortion audio make it particularly well suited for applications such as video tape recorders, video disc players, TV games and subscription decoders.

- Single Supply, 5.0 V to 12 V
- Channel 3 or 4 Operation
- Variable Gain RF Modulator
- Wide Dynamic Range
- Low Intermodulation Distortion
- Positive or Negative Sync
- Low Audio Distortion
- Few External Components

TV MODULATOR CIRCUIT

SEMICONDUCTOR
TECHNICAL DATA

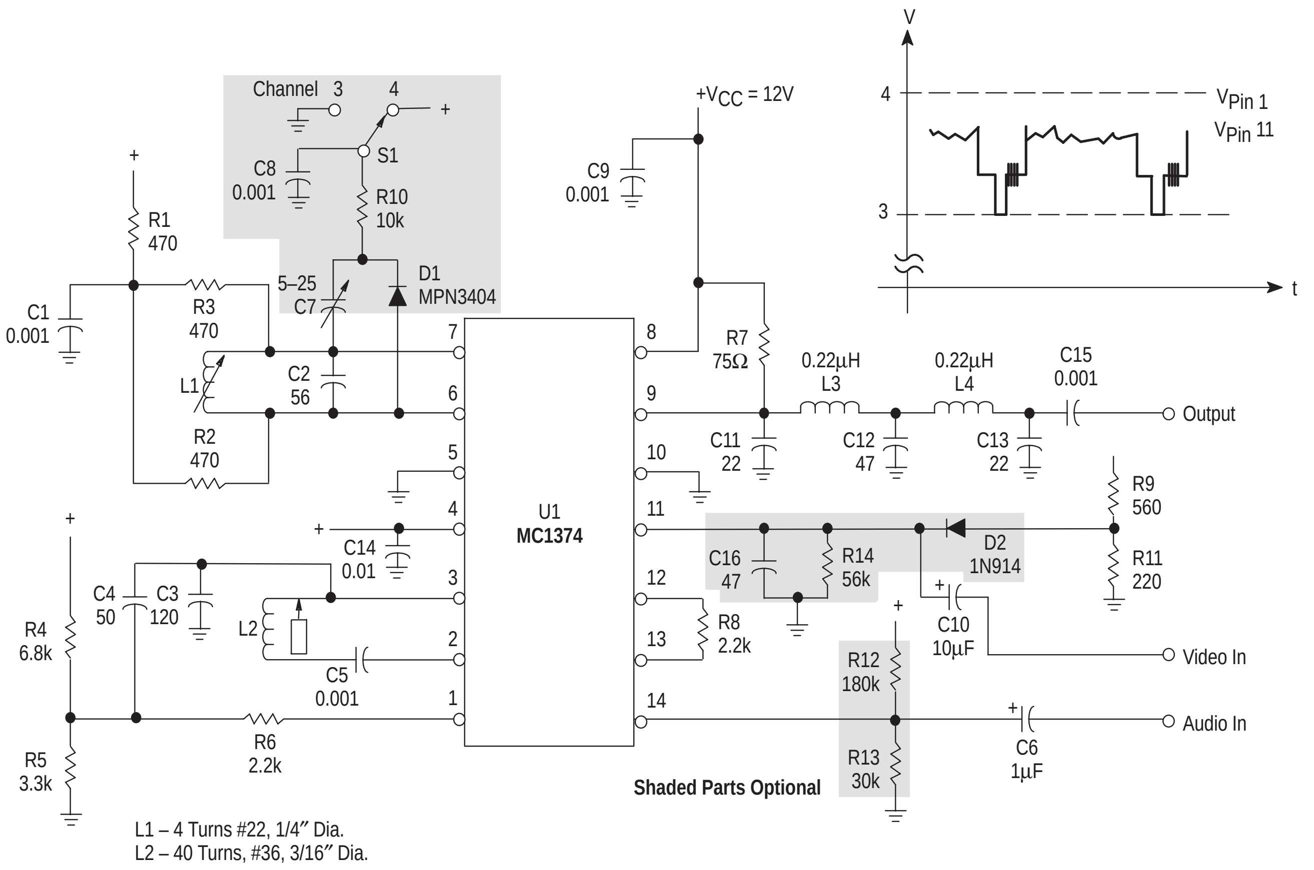


P SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC1374P	T_A = 0° to +70°C	Plastic DIP

Figure 1. Simplified Application



MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted.)

Rating	Value	Unit
Supply Voltage	14	Vdc
Operating Ambient Temperature Range	0 to +70	°C
Storage Temperature Range	–65 to +150	°C
Junction Temperature	150	°C
Power Dissipation Package Derate above 25°C	1.25 10 mW/°C	W

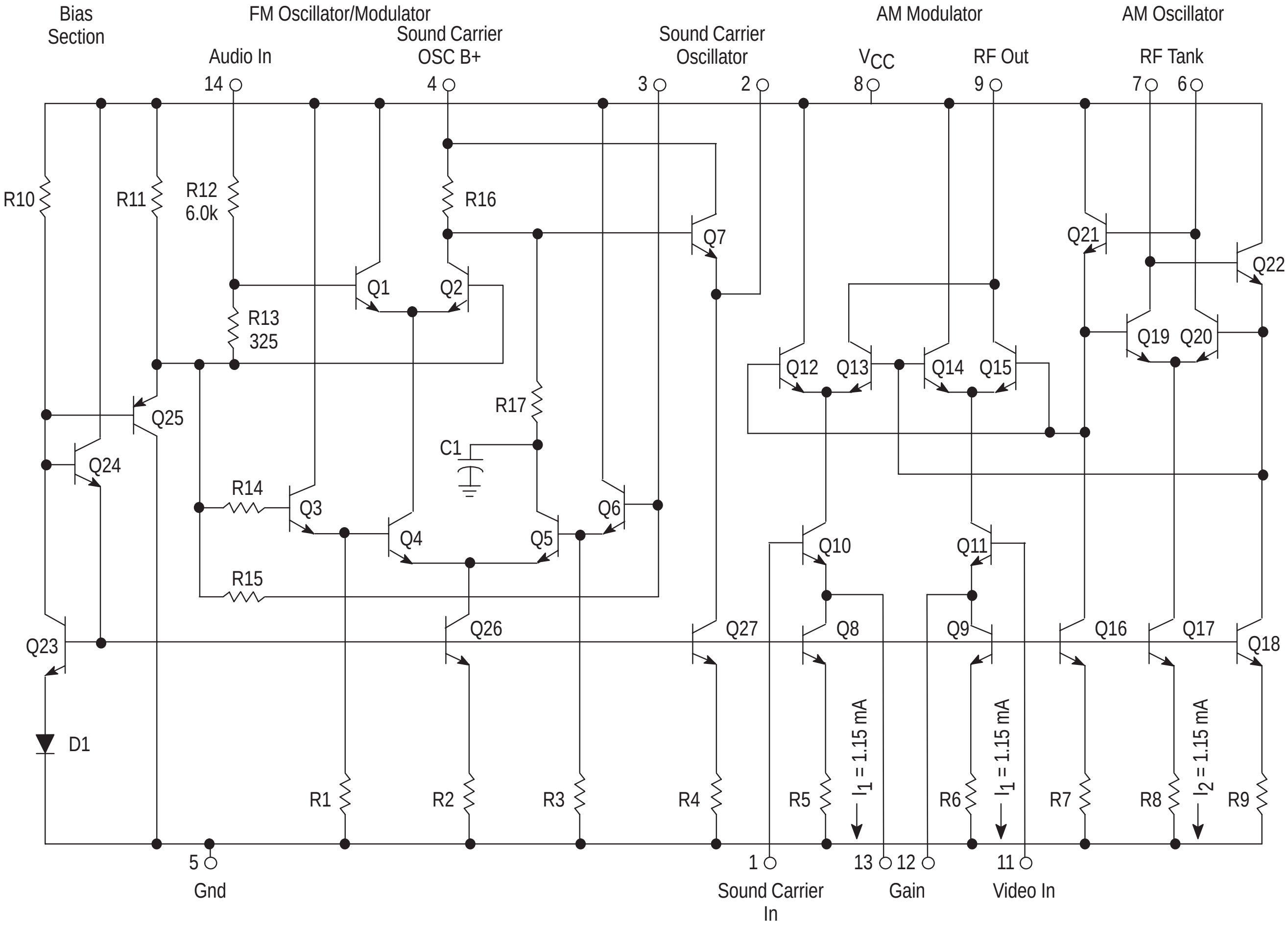
ELECTRICAL CHARACTERISTICS (V_{CC} = 12 Vdc, T_A = 25°C, f_c = 67.25 MHz, Figure 4 circuit, unless otherwise noted.)

Characteristics	Min	Typ	Max	Unit
AM OSCILLATOR/MODULATOR				
Operating Supply Voltage	5.0	12	12	V
Supply Current (Figure 1)	–	13	–	mA
Video Input Dynamic Range (Sync Amplitude)	0.25	1.0	1.0	V Pk
RF Output (Pin 9, R7 = 75 Ω, No External Load)	–	170	–	mV pp
Carrier Suppression	36	40	–	dB
Linearity (75% to 12.5% Carrier, 15 kHz to 3.58 MHz)	–	–	2.0	%
Differential Gain Distortion (IRE Test Signal)	5.0	7.0	10	%
Differential Phase Distortion (3.58 MHz IRE Test Signal)	–	1.5	2.0	Degrees
920 kHz Beat (3.58 MHz @ 30%, 4.5 MHz @ 25%)	–	–57	–	dB
Video Bandwidth (75 Ω Input Source)	30	–	–	MHz
Oscillator Frequency Range	–	105	–	MHz
Internal Resistance across Tank (Pin 6 to Pin 7) Internal Capacitance across Tank (Pin 6 to Pin 7)	– –	1.8 4.0	– –	kΩ pF

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC} = 12 Vdc, 4.5 MHz, Test circuit of Figure 11, unless otherwise noted.)

Characteristics	Min	Typ	Max	Unit
FM OSCILLATOR/MODULATOR				
Frequency Range of Modulator Frequency Shift versus Temperature (Pin 14 open) Frequency Shift versus V_{CC} (Pin 14 open) Output Amplitude (Pin 3 not loaded) Output Harmonics, Unmodulated	14 – – – –	4.5 0.2 – 900 –	14 0.3 4.0 – –40	MHz kHz/°C kHz/V mVpp dB
Modulation Sensitivity 1.7 MHz 4.5 MHz 10.7 MHz	– – –	0.20 0.24 0.80	– – –	MHz/V
Audio Distortion (±25 kHz Deviation, Optimized Bias Pin 14) Audio Distortion (±25 kHz Deviation, Pin 14 self biased) Incidental AM (±25 kHz FM)	– – –	0.6 1.4 2.0	1.0 – –	%
Audio Input Resistance (Pin 14 to ground) Audio Input Capacitance (Pin 14 to ground)	– –	6.0 5.0	– –	kΩ pF
Stray Tuning Capacitance (Pin 3 to ground) Effective Oscillator Source Impedance (Pin 3 to load)	– –	5.0 2.0	– –	pF kΩ

Figure 2. TV Modulator



GENERAL INFORMATION

The MC1374 contains an RF oscillator, RF modulator, and a phase shift type FM modulator, arranged to permit good printed circuit layout of a complete TV modulation system. The RF oscillator is similar to the one used in MC1373, and is coupled internally in the same way. Its frequency is controlled by an external tank on Pins 6 and 7, or by a crystal circuit, and will operate to approximately 105 MHz. The video modulator is a balanced type as used in the well known MC1496. Modulated sound carrier and composite video information can be put in separately on Pins 1 and 11 to minimize unwanted crosstalk. A single resistor on Pins 12 and 13 is selected to set the modulator gain. The RF output at Pin 9 is a current source which drives a load connected from Pin 9 to V_{CC}.

The FM system was designed specifically for the TV intercarrier function. For circuit economy, one phase shift circuit was built into the ship. Still, it will operate from 1.4 MHz to 14 MHz, low enough to be used in a cordless telephone base station (1.76 MHz), and high enough to be used as an FM IF test signal source (10.7 MHz). At 4.5 MHz, a deviation of ±25 kHz can be achieved with 0.6% distortion (typical).

In the circuit above, devices Q1 through Q7 are active in the oscillator function. Differential amplifier Q3, Q4, Q5, and Q6 acts as a gain stage, sinking current from input section Q1, Q2 and the phase shift network R17, C1. Input amplifier Q1, Q2 can vary the amount of “in phase” Q4 current to be combined with phase shifter current in load resistor R16. The R16 voltage is applied to emitter follower Q7 which drives an external L–C circuit. Feedback from the center of the L–C circuit back to the base of Q6 closes the loop. As audio input is applied which would offset the stable oscillatory phase, the frequency changes to counteract. The input to Pin 14 can include a dc feedback current for AFC over a limited range.

The modulated FM signal from Pin 3 is coupled to Pin 1 of the RF modulator and is then modulated onto the AM carrier.

AM Section

The AM modulator transfer function in Figure 3 shows that the video input can be of either polarity (and can be applied at either input). When the voltages on Pin 1 and Pin 11 are equal, the RF output is theoretically zero. As the difference between $V_{Pin\ 11}$ and $V_{Pin\ 1}$ increases, the RF output increases linearly until all of the current from both I_1 current sources (Q8 and Q9) is flowing in one side of the modulator. This occurs when $\pm(V_{Pin11} - V_{Pin1}) = I_1 R_G$, where I_1 is typically 1.15 mA. The peak–to–peak RF output is the $2I_1 R_L$. Usually the value of R_L is chosen to be 75 Ω to ease the design of the output filter and match into TV distribution systems. The theoretical range of input voltage and R_G is quite wide, but noise and available sound level limit the useful video (sync tip) amplitude to between 0.25 Vpk and 1.0 Vpk. It is recommended that the value of R_G be chosen so that only about half of the dynamic range will be used at sync tip level.

The operating window of Figure 5 shows a cross–hatched area where Pin 1 and Pin 11 voltages must always be in order to avoid saturation in any part of the modulator. The letter ϕ represents one diode drop, or about 0.75 V. The oscillator Pins 6 and 7 must be biased to a level of $V_{CC} - \phi - 2I_1 R_L$ (or lower) and the input Pins 1 and 11 must always be at least 2ϕ below that. It is permissible to operate down to 1.6 V, saturating the current sources, but whenever possible, the minimum should be 3ϕ above ground.

The oscillator will operate dependably up to about 105 MHz with a broad range of tank circuit component values. It is desirable to use a small L and a large C to minimize the dependence on IC internal capacitance. An operating Q between 10 and 20 is recommended. The values of R_1, R_2 and R_3 are chosen to produce the desired Q and to set the Pin 6 and 7 dc voltage as discussed above. Unbalanced operation, i.e., Pin 6 or 7 bypassed to ground, is not recommended. Although the oscillator will still run, and the modulator will produce a useable signal, this mode causes substantial base–band video feedthrough. Bandswitching, as Figure 1 shows, can still be accomplished economically without using the unbalanced method.

The oscillator frequency with respect to temperature in the test circuit shows less than ±20 kHz total shift from 0° to 50°C as shown in Figure 7. At higher temperatures the slope approaches 2.0 kHz/°C. Improvement in this region would require a temperature compensating tuning capacitor of the N75 family.

Crystal control is feasible using the circuit shown in Figure 21. The crystal is a 3rd overtone series type, used in series resonance. The L1, C2 resonance is adjusted well below the crystal frequency and is sufficiently tolerant to permit fixed values. A frequency shift versus temperature of less than 1.0 Hz/°C can be expected from this approach. The resistors Ra and Rb are to suppress parasitic resonances.

Coupling of output RF to wiring and components on Pins 1 and 11 can cause as much as 300 kHz shift in carrier (at 67 MHz) over the video input range. A careful layout can keep this shift below 10 kHz. Oscillator may also be inadvertently coupled to the RF output, with the undesired effect of preventing a good null when $V_{11} = V_1$. Reasonable care will yield carrier rejection ratios of 36 to 40 dB below sync tip level carrier.

In television, one of the most serious concerns is the prevention of the intermodulation of color (3.58 MHz) and sound (4.5 MHz) frequencies, which causes a 920 kHz signal to appear in the spectrum. Very little (3rd order) nonlinearity is needed to cause this problem. The results in Figure 6 are unsatisfactory, and demonstrate that too much of the available dynamic range of the MC1374 has been used. Figures 8 and 10 show that by either reducing standard signal level, or reducing gain, acceptable results may be obtained.

At VHF frequencies, small imbalances within the device introduce substantial amounts of 2nd harmonic in the RF output. At 67 MHz, the 2nd harmonic is only 6 to 8 dB below the maximum fundamental. For this reason, a double pi low pass filter is shown in the test circuit of Figure 3 and works well for Channel 3 and 4 lab work. For a fully commercial application, a vestigial sideband filter will be required. The general form and approximate values are shown in Figure 19. It must be exactly aligned to the particular channel.

Figure 3. AM Modulator Transfer Function

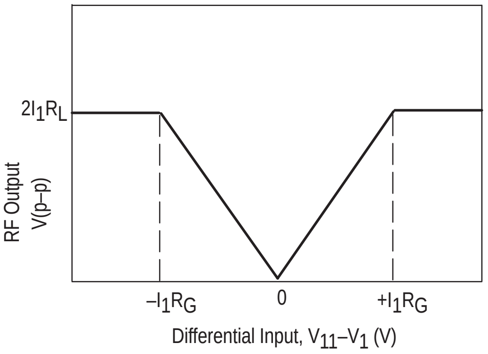


Figure 4. AM Test Circuit

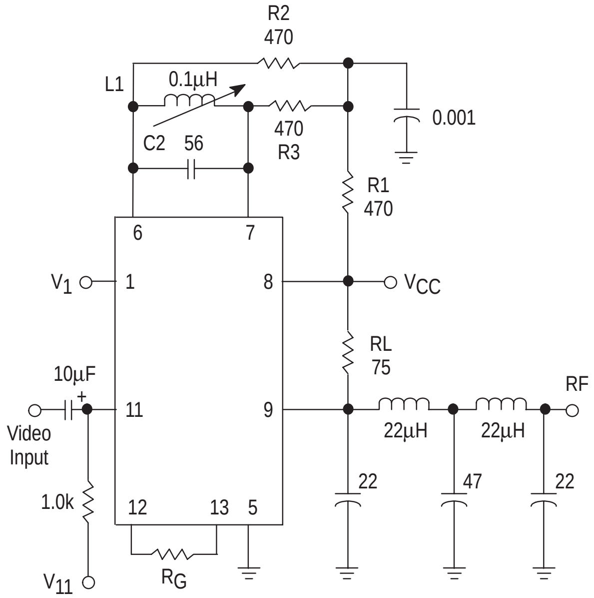


Figure 5. The Operating Window

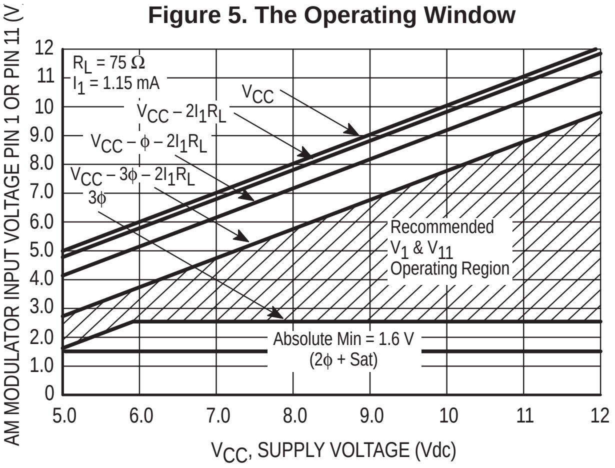


Figure 6. 920 kHz Beat

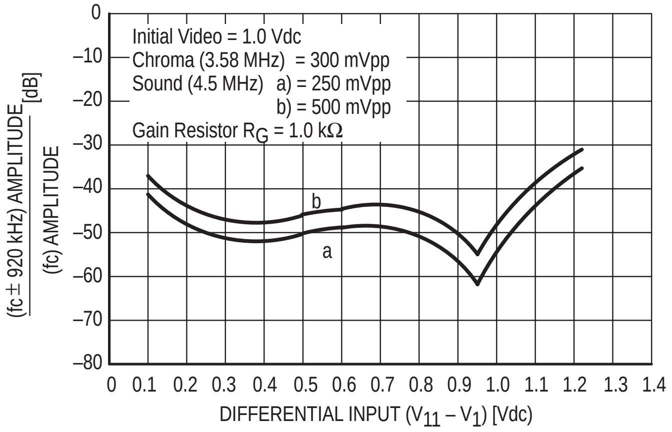


Figure 7. RF Oscillator Frequency versus Temperature

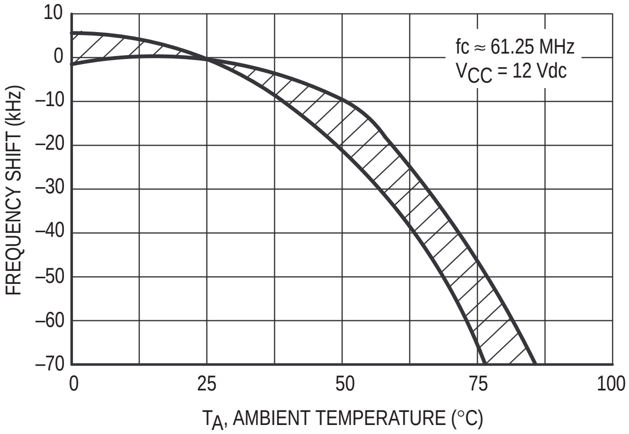


Figure 8. 920 kHz Beat

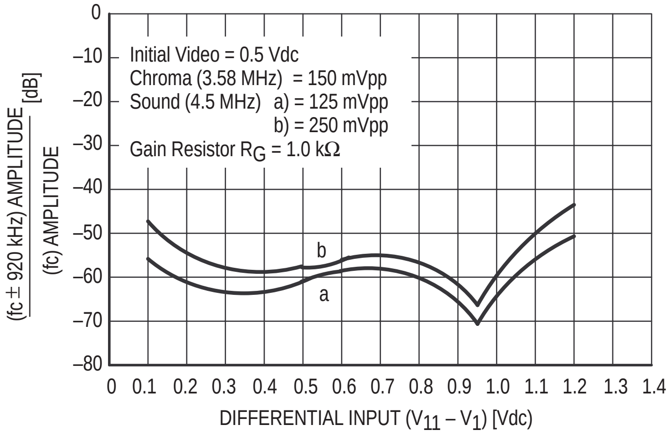


Figure 9. RF Oscillator Frequency versus Supply Voltage

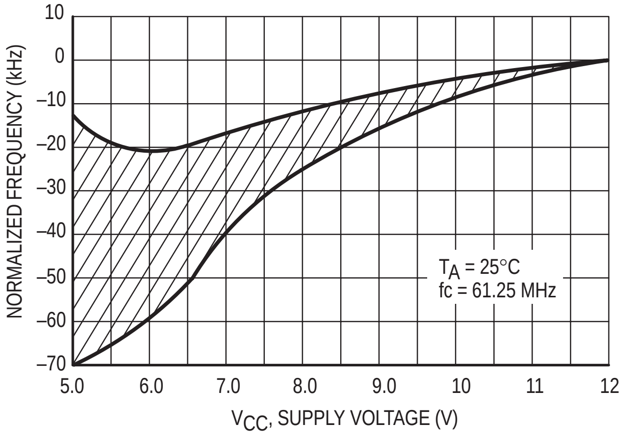
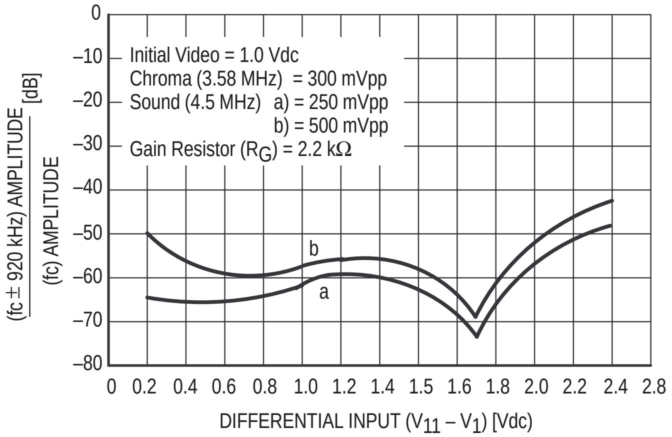


Figure 10. 920 kHz Beat



FM Section

The oscillator center is approximately the resonance of the inductor L_2 from Pin 2 to Pin 3 and the effective capacitance C_3 from Pin 3 to ground. For overall oscillator stability, it is best to keep X_L in the range of 300 Ω to 1.0 kΩ.

The modulator transfer characteristic at 4.5 MHz is shown in Figure 15. Transfer curves at other frequencies have a very similar shape, but differ in deviation per input volt, as shown in Figures 13 and 17.

Most applications will not require DC connection to the audio input, Pin 14. However, some improvements can be achieved by the addition of biasing circuitry. The unaided device will establish its own Pin 14 bias at 4 θ, or about 3.0 V. This bias is a little too high for optimum modulation linearity. Figure 14 shows better than 2 to 1 improvement in distortion between the unaided device and pulling Pin 14 down to 2.6 V to 2.7 V. This can be accomplished by a simple divider, if the supply voltage is relatively constant.

The impedance of the divider has a bearing on the frequency versus temperature stability of the FM system. A divider of 180 kΩ and 30 kΩ (for V_{CC} = 12 V) will give good temperature stabilization results. However, as Figure 18 shows, a divider is not a good method if the supply voltage varies. The designer must make the decisions here, based on considerations of economy, distortion and temperature requirements and power supply capability. If the distortion requirements are not stringent, then no bias components are needed. If, in this case, the temperature compensation needs to be improved in the high ambient area, the tuning capacitor from Pin 3 to ground can be selected from N75 or N150 temperature compensation types.

Another reason for DC input to Pin 14 is the possibility of automatic frequency control. Where high accuracy of inter–carrier frequency is required, it may be desirable to feed back the DC output of an AFC or phase detector for nominal carrier frequency control. Only limited control range could be used without adversely affecting the distortion performance, but very little frequency compensation will be needed.

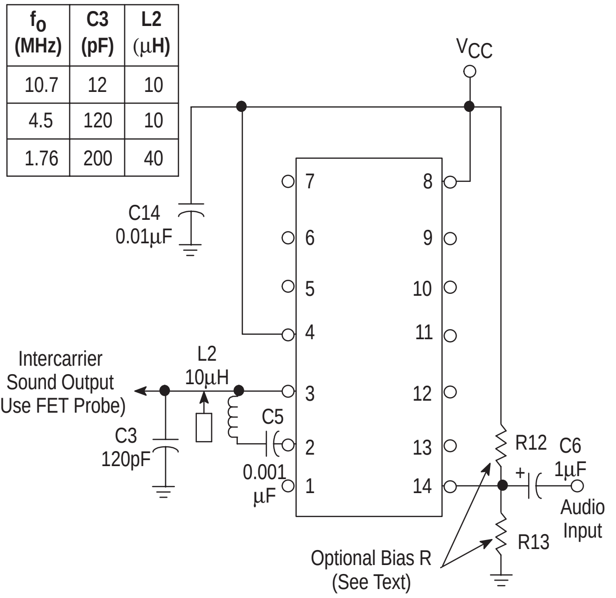
One added convenience in the FM section is the separate Pin "oscillator B+" which permits disabling of the sound system during alignment of the AM section. Usually it can be hard wired to the V_{CC} source without decoupling.

Standard practice in television is to provide pre–emphasis of higher audio frequencies at the transmitter and a matching de–emphasis in the TV receiver audio amplifier. The purpose of this is to counteract the fact that less energy is usually present in the higher frequencies, and also that fewer modulation sidebands are within the deviation window. Both factors degrade signal to noise ration. Pre–emphasis of 75 µs is standard practice. For cases where it has not been provided, a suitable pre–emphasis network is covered in Figure 20.

It would seem natural to take the FM system output from Pin 2, the emitter follower output, but this output is high in harmonic content. Taking the output from Pin 3 sacrifices somewhat in source impedance but results in a clean output fundamental, with all harmonics more than 40 dB down. This choice removes the need for additional filtering components. The source impedance of Pin 3 is approximately 2.0 kΩ, and the open circuit amplitude is about 900 mV pp for the test circuit shown in Figure 11.

The application circuit of Figure 1 shows the recommended approach to coupling the FM output from Pin 3 to the AM modulator input, Pin 1. The input impedance at Pin 1 is very high, so the intercarrier level is determined by the source impedance of Pin 3 driving through C4 into the video bias circuit impedance of R4 and R5, about 2.2 k. This provides an intercarrier level of 500 mV pp, which is correct for the 1.0 V peak video level chosen in this design. Resistor R6 and the input capacitance of Pin 1 provide some decoupling of stray pickup of RF oscillator or AM output which may be coupled to the sound circuitry.

Figure 11. FM Test Circuit



f_O (MHz)	C3 (pF)	L2 (µH)
10.7	12	10
4.5	120	10
1.76	200	40

Figure 12. Modulator Sensitivity

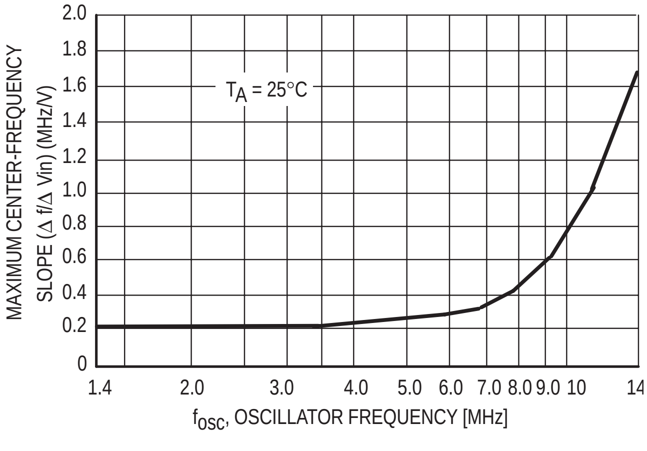


Figure 13. Modulator Transfer Function

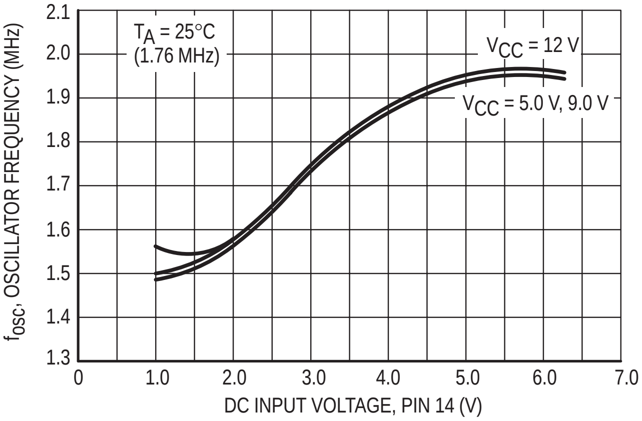


Figure 14. Distortion versus Modulation Depth

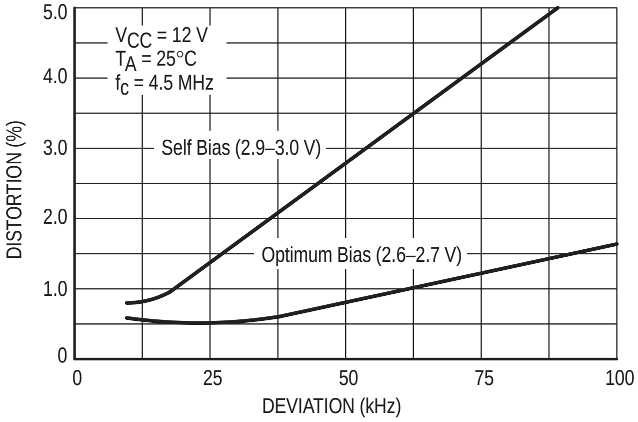


Figure 15. Modulator Transfer Function

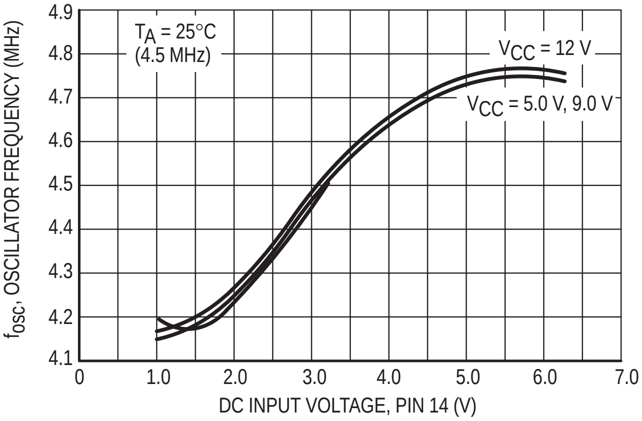


Figure 16. FM System Frequency versus Temperature

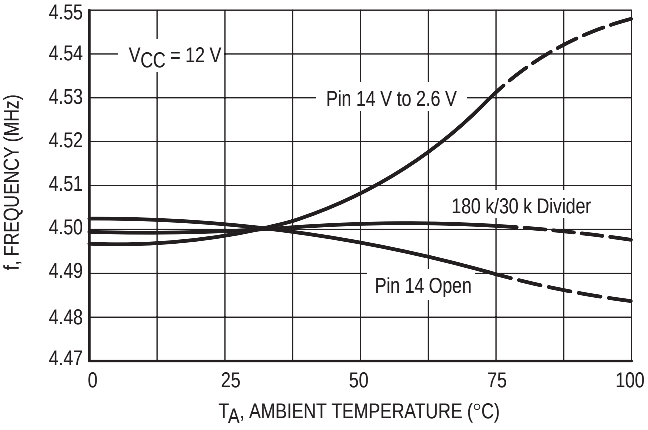


Figure 17. Modulator Transfer Function

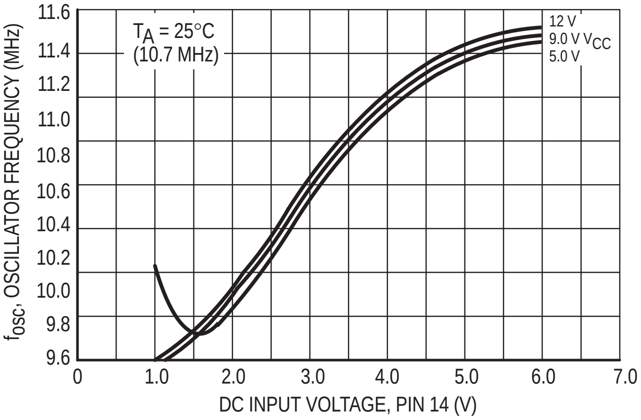


Figure 18. FM System Frequency versus V_{CC}

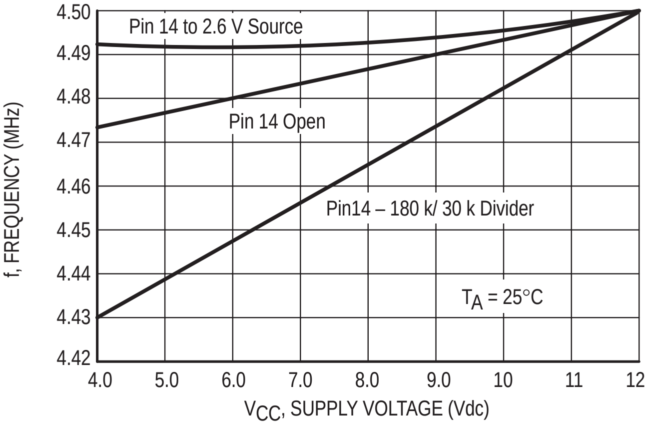


Figure 19. A Channel 4 Vestigial Sideband Filter

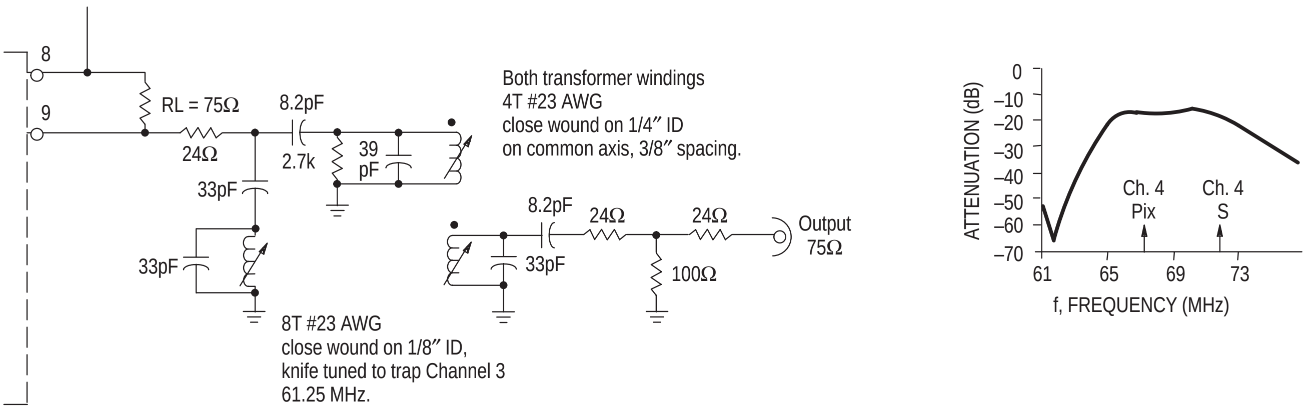
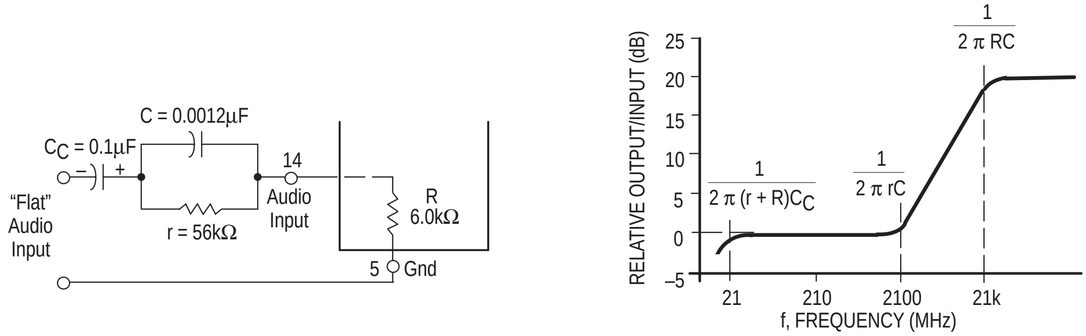
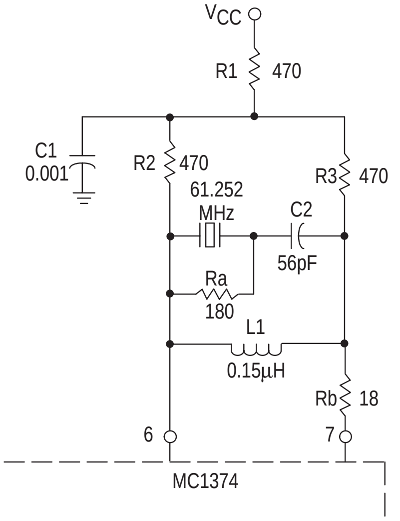


Figure 20. Audio Pre–Emphasis Circuit



Pre–emphasis = 75 µs = rC = $\frac{1}{2\pi\,(2100\ \text{Hz})}$

Figure 21. Crystal Controlled RF Oscillator for Channel 3, 61.25 MHz



NOTE: See Application Note AN829 for further information.

MOTOROLA

MC1377

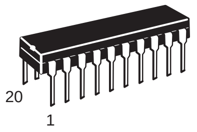
Color Television RGB to PAL/NTSC Encoder

The MC1377 will generate a composite video from baseband red, green, blue, and sync inputs. On board features include: a color subcarrier oscillator; voltage controlled 90° phase shifter; two double sideband suppressed carrier (DSBSC) chroma modulators; and RGB input matrices with blanking level clamps. Such features permit system design with few external components and accordingly, system performance comparable to studio equipment with external components common in receiver systems.

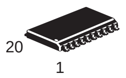
- Self–contained or Externally Driven Reference Oscillator
- Chroma Axes, Nominally 90° (±5°), are Optionally Trimable
- PAL/NTSC Compatible
- Internal 8.2 V Regulator

COLOR TELEVISION
RGB to PAL/NTSC ENCODER

SEMICONDUCTOR
TECHNICAL DATA



P SUFFIX
PLASTIC PACKAGE
CASE 738

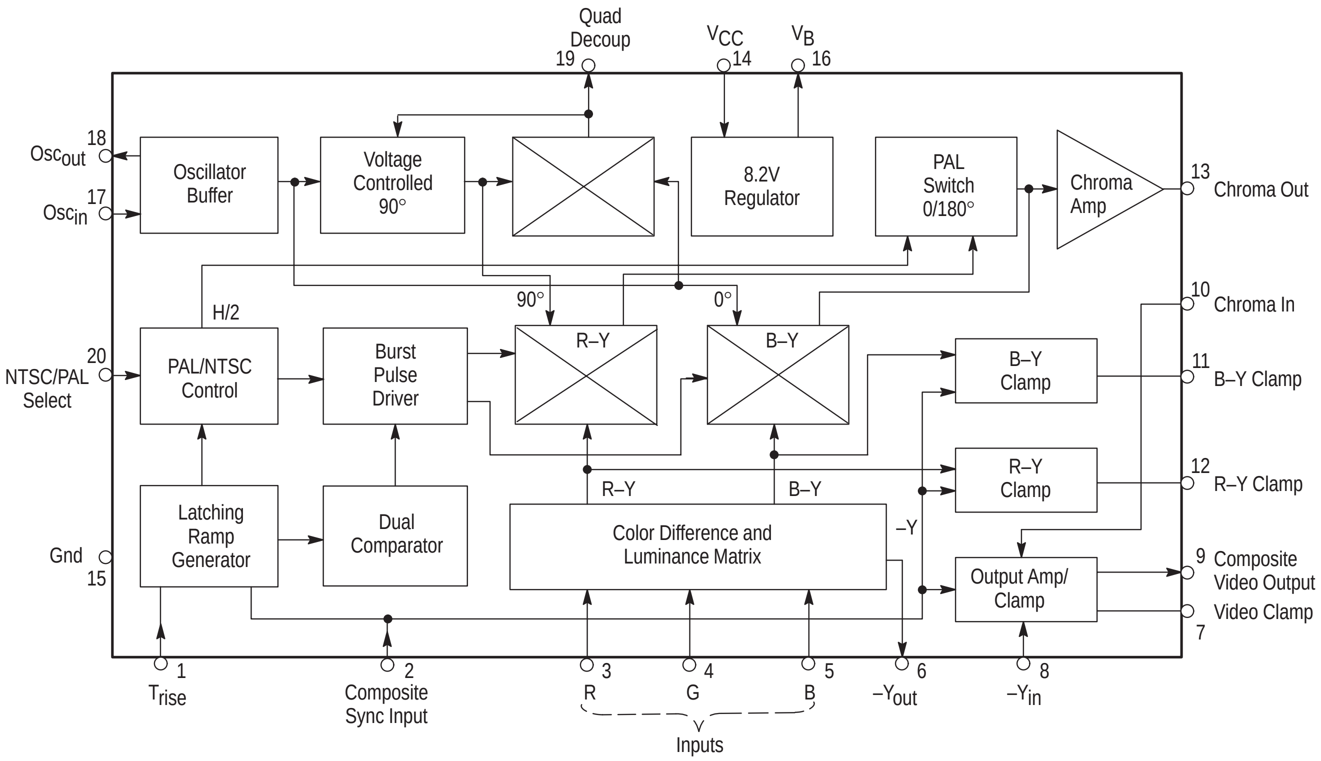


DW SUFFIX
PLASTIC PACKAGE
CASE 751D
(SO–20L)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC1377DW	T_A = 0° to +70°C	SO–20L
MC1377P		Plastic DIP

Figure 1. Representative Block Diagram



MAXIMUM OPERATING CONDITIONS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	15	Vdc
Storage Temperature	T_{stg}	–65 to +150	°C
Power Dissipation Package	P_D	1.25	W
Derate above 25°C		10	mW/°C
Operating Temperature	T_A	0 to +70	°C

RECOMMENDED OPERATING CONDITIONS

Characteristics	Min	Typ	Max	Unit
Supply Voltage	10	12	14	Vdc
I_B Current (Pin 16)	0	–	–10	mA
Sync, Blanking Level (DC level between pulses, see Figure 9e)	1.7	–	8.2	Vdc
Sync Tip Level (see Figure 9e)	–0.5	0	0.9	
Sync Pulse Width (see Figure 9e)	2.5	–	5.2	μs
R, G, B Input (Amplitude)	–	1.0	–	V_{pp}
R, G, B Peak Levels for DC Coupled Inputs, with Respect to Ground	2.2	–	4.4	V
Chrominance Bandwidth (Non–comb Filtered Applications), (6 dB)	0.5	1.5	2.0	MHz
Ext. Subscarrier Input (to Pin 17) if On–Chip Oscillator is not used.	0.5	0.7	1.0	V_{pp}

ELECTRICAL CHARACTERISTICS (V_{CC} = 12 Vdc, T_A = 25°C, circuit of Figure 7, unless otherwise noted.)

Characteristics	Pins	Symbol	Min	Typ	Max	Unit
SUPPLY CURRENT						
Supply Current into V_{CC}, No Load, on Pin 9. Circuit Figure 7 V_{CC} = 10 V	14	I_{CC}	–	33	–	mA
V_{CC} = 11 V			–	34	–	
V_{CC} = 12 V			20	35	40	
V_{CC} = 13 V			–	36	–	
V_{CC} = 14 V			–	37	–	
VOLTAGE REGULATOR						
V_B Voltage (I_B = –10 mA, V_{CC} = 12 V, Figure 7)	16	V_B	7.7	8.2	8.7	Vdc
Load Regulation ($0 < I_B \leq 10$ mA, V_{CC} = 12 V)		Reg_{load}	–20	120	+30	mV
Line Regulation (I_B = 0 mA, 10 V < V_{CC} < 14 V)		Reg_{line}	–	4.5	–	mV/V
OSCILLATOR AND MODULATION						
Oscillator Amplitude with 3.58 MHz/4.43 MHz crystal	17	Osc	–	0.6	–	V_{pp}
Subcarrier Input: Resistance at 3.58 MHz	17	R_{osc}	–	5.0	–	kΩ
4.43 MHz			–	4.0	–	
Capacitance		C_{osc}	–	2.0	–	pF
Modulation Angle (R–Y) to (B–Y)	–	∅m	–	±5	–	Deg
Angle Adjustment (R–Y)	19	Δ∅m	–	0.25	–	Deg/μA
DC Bias Voltage	19	V_{19}	–	6.4	–	Vdc
CHROMINANCE AND LUMINANCE						
Chroma Input DC Level	10	V_{in}	–	4.0	–	Vdc
Chroma Input Level for 100% Saturation			–	0.7	–	V_{pp}
Chroma Input: Resistance		R_{in}	–	10	–	kΩ
Capacitance		C_{in}	–	2.0	–	pF
Chroma DC Output Level	13	V_{out}	8.9	10	10.9	Vdc
Chroma Output Level at 100% Saturation			–	1.0	–	V_{pp}
Chroma Output Resistance		R_{out}	–	50	–	Ω
Luminance Bandwidth (–3.0 dB), Less Delay Line	9	BW_{Luma}	–	8.0	–	MHz

ELECTRICAL CHARACTERISTICS (V_{CC} = 12 Vdc, T_A = 25°C, circuit of Figure 7, unless otherwise noted.)

Characteristics	Pins	Symbol	Min	Typ	Max	Unit
VIDEO INPUT						
R, G, B Input DC Levels	3, 4, 5	RGB	2.8	3.3	3.8	Vdc
R, G, B Input for 100% Color Saturation			–	1.0	–	V_{pp}
R, G, B Input: Resistance		R_{RGB}	8.0	10	17	kΩ
Capacitance		C_{RGB}	–	2.0	–	pF
Sync Input Resistance (1.7 V < Input < 8.2)	2	Sync	–	10	–	kΩ
COMPOSITE VIDEO OUTPUT						
Composite Output, 100% Saturation (see Figure 8d) Sync	9	CV_{out}	–	0.6	–	V_{pp}
Luminance			–	1.4	–	
Chroma			–	1.7	–	
Burst			–	0.6	–	
Output Impedance (Note 1)		R_{video}	–	50	–	Ω
Subcarrier Leakage in Output (Note 2)		V_{lk}	–	20	–	mV_{pp}

NOTES: 1. Output Impedance can be reduced to less than 10 Ω by using a 150 Ω output load from Pin 9 to ground. Power supply current will increase to about 60 mA.

2. Subcarrier leakage can be reduced to less than 10 mV with optional circuitry (see Figure 12).

PIN FUNCTION DESCRIPTIONS

Symbol	Pin	Description
t_r	1	External components at this pin set the rise time of the internal ramp function generator (see Figure 10).
Sync	2	Composite sync input. Presents 10 kΩ resistance to input.
R	3	Red signal input. Presents 10 kΩ impedance to input. 1.0 V_{pp} required for 100% saturation.
G	4	Green signal input. Presents 10 kΩ impedance to input. 1.0 V_{pp} required for 100% saturation.
B	5	Blue signal Input. Presents 10 kΩ impedance to input. 1.0 V_{pp} required for 100% saturation.
$–Y_{out}$	6	Luma (–Y) output. Allows external setting of luma delay time.
V_{clamp}	7	Video Clamp pin. Typical connection is a 0.01 μF capacitor to ground.
$–Y_{in}$	8	Luma (–Y) input. Presents 10 kΩ input impedance.
CV_{out}	9	Composite Video output. 50 Ω output impedance.
$Chroma_{In}$	10	Chroma input. Presents 10 kΩ input impedance.
$B–Y_{clamp}$	11	B–Y clamp. Clamps B–Y during blanking with a 0.1 μF capacitor to ground. Also used with R–Y clamp to null residual color subcarrier in output.
$R–Y_{clamp}$	12	R–Y clamp. Clamps R–Y during blanking with a 0.1 μF capacitor to ground. Also used with B–Y clamp to null residual color subcarrier in output.
$Chroma_{Out}$	13	Chroma output. 50 Ω output impedance.
V_{CC}	14	Power supply pin for the IC; +12, ± 2.0 V, required at 35 mA (typical).
Gnd	15	Ground pin.
V_B	16	8.2 V reference from an internal regulator capable of delivering 10 mA to external circuitry.
Osc_{in}	17	Oscillator input. A transistor base presents 5.0 kΩ to an external subcarrier input, or is available for constructing a Colpitts oscillator (see Figure 4).
Osc_{out}	18	Oscillator output. The emitter of the transistor, with base access at Pin 17, is accessible for completing the Colpitts oscillator. See Figure 4.
$\varnothing_m$	19	Quad decoupler. With external circuitry, R–Y to B–Y relative angle errors can be corrected. Typically, requires a 0.01 μF capacitor to ground.
NTSC/PAL Select	20	NTSC/PAL switch. When grounded, the MC1377 is in the NTSC mode; if unconnected, in the PAL mode.

FUNCTIONAL DESCRIPTION

Figure 2. Power Supply and V_B

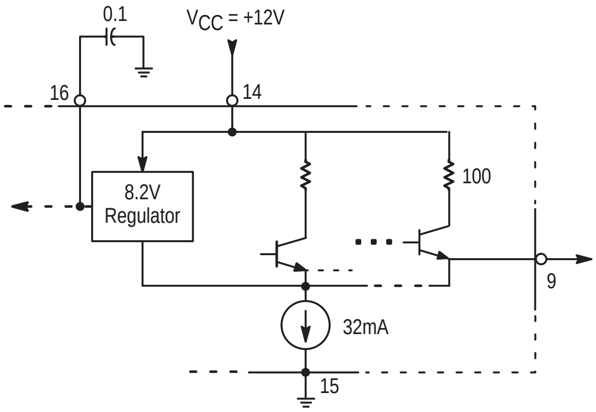


Figure 3. RGB Input Circuitry

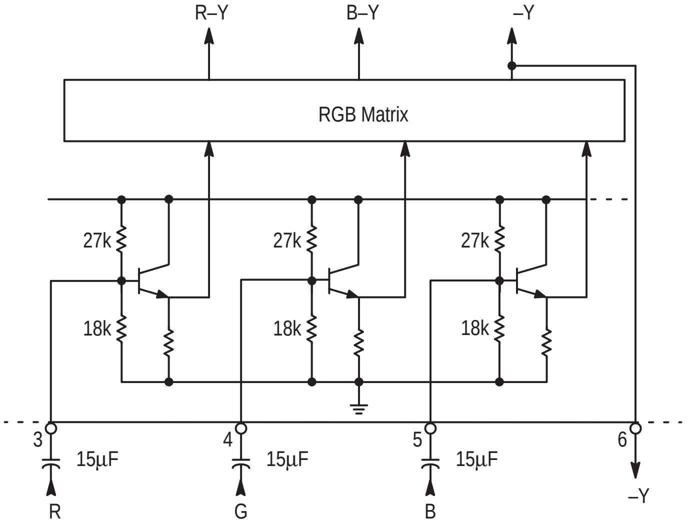
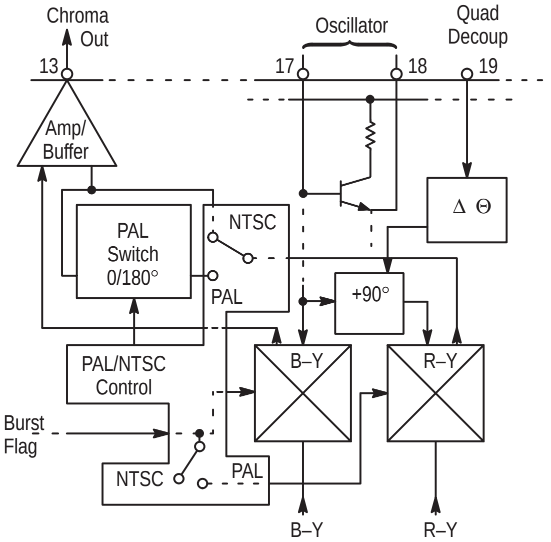


Figure 4. Chroma Section



Power Supply and V_B (8.2 V Regulator)

The MC1377 pin for power supply connection is Pin 14. From the supply voltage applied to this pin, the IC biases internal output stages and is used to power the 8.2 V internal regulator (V_B at Pin 16) which biases the majority of internal circuitry. The regulator will provide a nominal 8.2 V and is capable of 10 mA before degradation of performance. An equivalent circuit of the supply and regulator is shown in Figure 2.

R, G, B Inputs

The RGB inputs are internally biased to 3.3 V and provide 10 kΩ of input impedance. Figure 3 shows representative input circuitry at Pins 3, 4, and 5.

The input coupling capacitors of 15 µF are used to prevent tilt during the 50/60 Hz vertical period. However, if it is desired to avoid the use of the capacitors, then inputs to Pins 3, 4, and 5 can be dc coupled provided that the signal levels are always between 2.2 V and 4.4 V.

After input, the separate RGB information is introduced to the matrix circuitry which outputs the R–Y, B–Y, and –Y signals. The –Y information is routed out at Pin 6 to an external delay line (typically 400 ns).

DSBSC Modulators and 3.58 MHz Oscillator

The R–Y and B–Y outputs (see (B–Y)/(R–Y) Axes versus I/Q Axes, Figure 22) from the matrix circuitry are amplitude modulated onto the 3.58/4.43 MHz subcarrier. These signals are added and color burst is included to produce composite chroma available at Pin 13. These functions plus others, depending on whether NTSC or PAL operation is chosen, are performed in the chroma section. Figure 4 shows a block diagram of the chroma section.

The MC1377 has two double balanced mixers, and regardless of which mode is chosen (NTSC or PAL), the mixers always perform the same operation. The B–Y mixer modulates the color subcarrier directly, the R–Y mixer receives a 90° phase shifted color subcarrier before being modulated by the R–Y baseband information. Additional operations are then performed on these two signals to make them NTSC or PAL compatible.

In the NTSC mode, the NTSC/PAL control circuitry allows an inverted burst of 3.58 MHz to be added only to the B–Y signal. A gating pulse or “burst flag” from the timing section permits color burst to be added to the B–Y signal. This color burst is 180° from the B–Y signal and 90° away from the R–Y signal (see Figure 22) and permits decoding of the color information. These signals are then added and amplified before being output, at Pin 13, to be bandpassed and then reintroduced to the IC at Pin 10.

In the PAL mode, NTSC/PAL control circuitry allows an inverted 4.43 MHz burst to be added to both R–Y and B–Y equally to produce the characteristic PAL 225°/135 burst phase. Also, the R–Y information is switched alternately from 180° to 0° of its original position and added to the B–Y information to be amplified and output.

Timing Circuitry

The composite sync input at Pin 2 performs three important functions: it provides the timing (but not the amplitude) for the sync in the final output; it drives the black level clamps in the modulators and output amplifier; and it triggers the ramp generator at Pin 1, which produces burst envelope and PAL switching. A representative block diagram of the timing circuitry is shown in Figure 5.

In order to produce a color burst, a burst envelope must be generated which “gates” a color subcarrier into the R–Y and B–Y modulators. This is done with the ramp generator at Pin 1.

The ramp generator at Pin 1 is an R–C type in which the pin is held low until the arrival of the *leading* edge of sync. The rising ramp function, with time constant R–C, passes through two level sensors – the first one starts the gating pulse and the second stops it (see Figure 10). Since the “early” part of the exponential is used, the timing provided is relatively accurate from chip–to–chip and assembly–to–assembly. Fixed components are usually adequate. The ramp continues to rise for more than half of the line interval, thereby inhibiting burst generation on “half interval” pulses on vertical front and back porches. The ramp method will produce burst on the vertical front and back “porches” at full line intervals.

R–Y, B–Y Clamps and Output Clamp/Amplifier

The sync signal, shown in the block diagram of Figure 6, drives the R–Y and B–Y clamps which clamp the R–Y and B–Y signals to reference black during the blanking periods. The output amplifier/clamp provides this same function plus combines and amplifies the chroma and luma components for composite video output.

Application Circuit

Figure 7 illustrates the block diagram of the MC1377 and the external circuitry required for typical operation.

Figure 5. Timing Circuitry

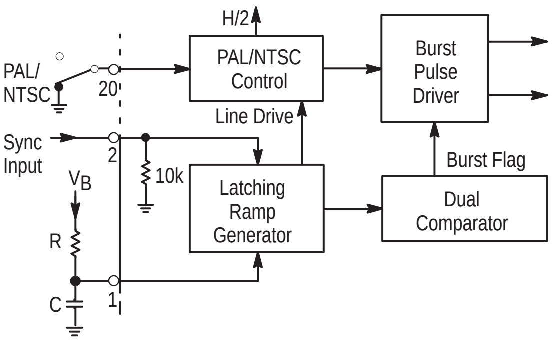


Figure 6. R–Y, B–Y and Output Amplifier Clamps

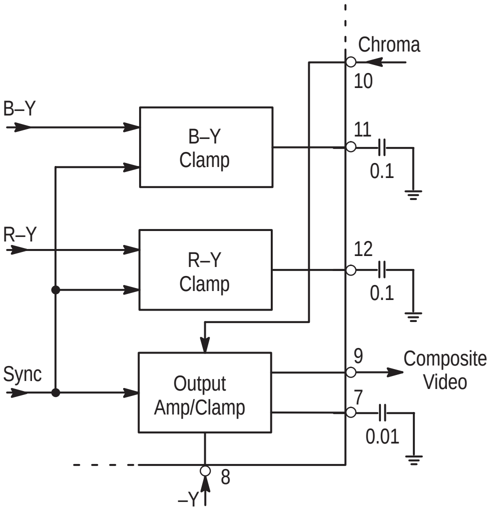
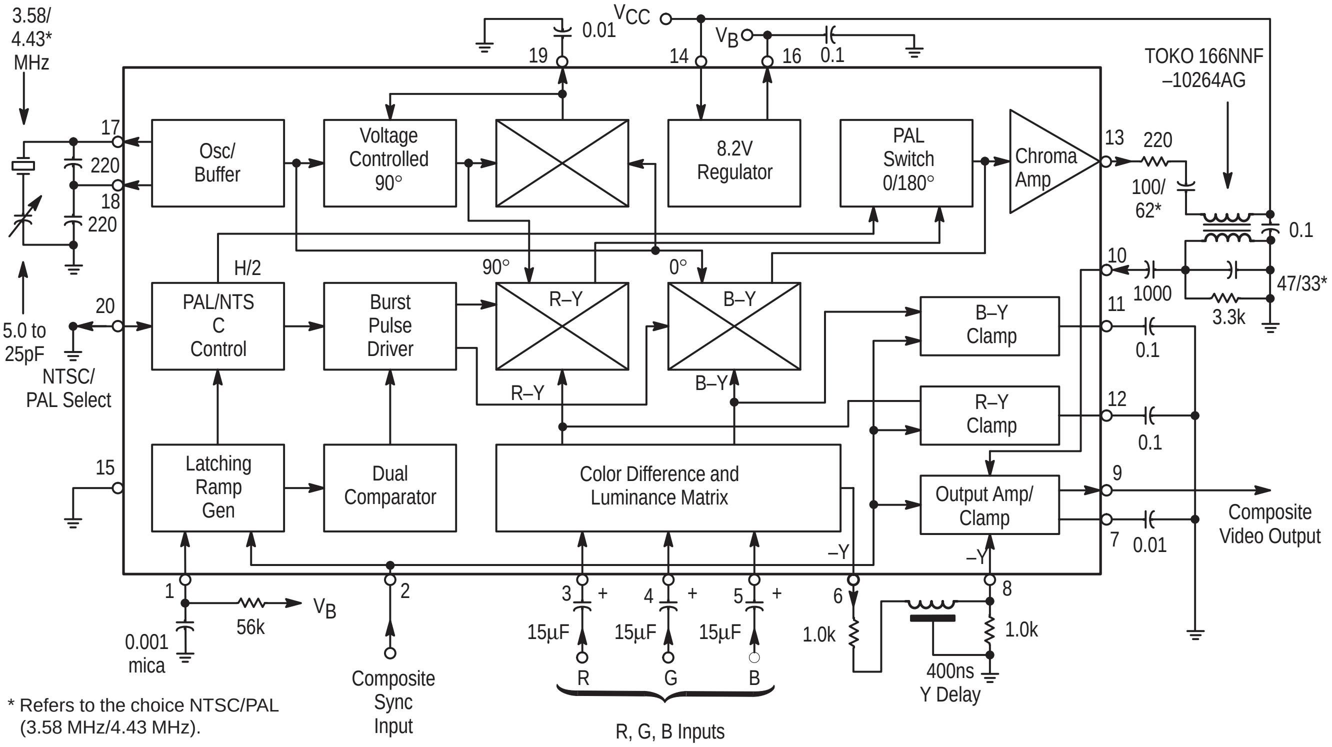


Figure 7. Block Diagram and Application Circuit



* Refers to the choice NTSC/PAL (3.58 MHz/4.43 MHz).

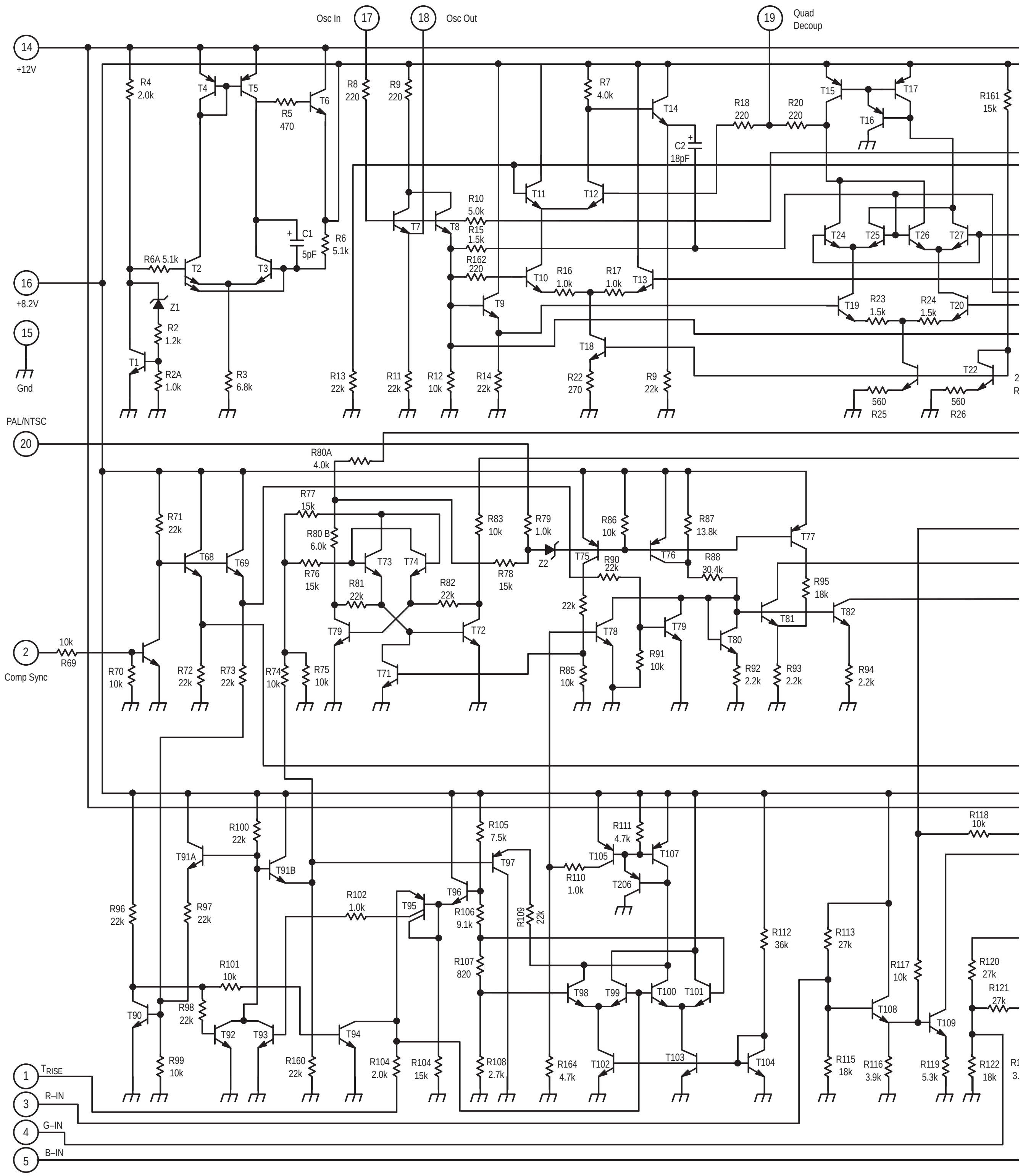
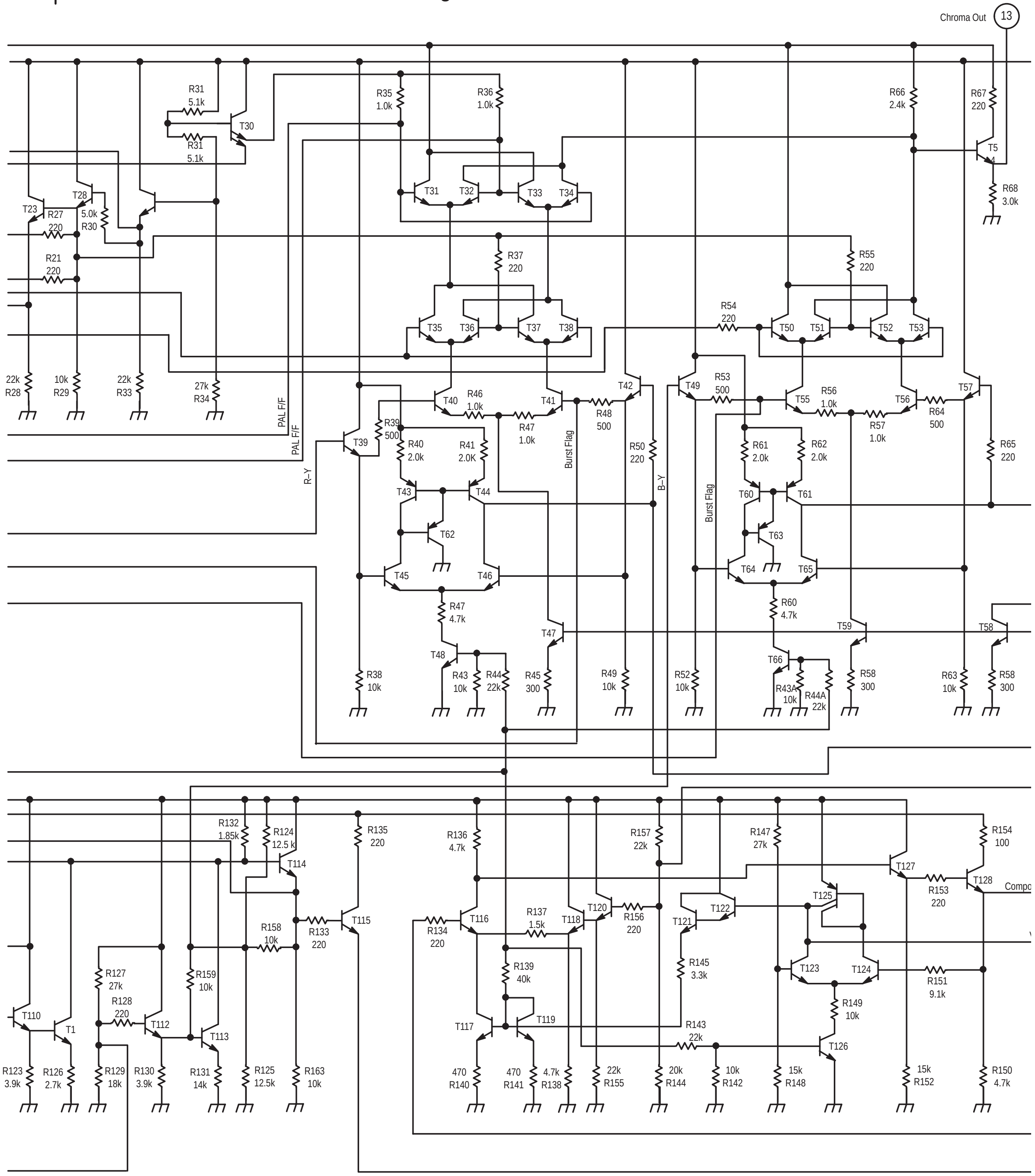
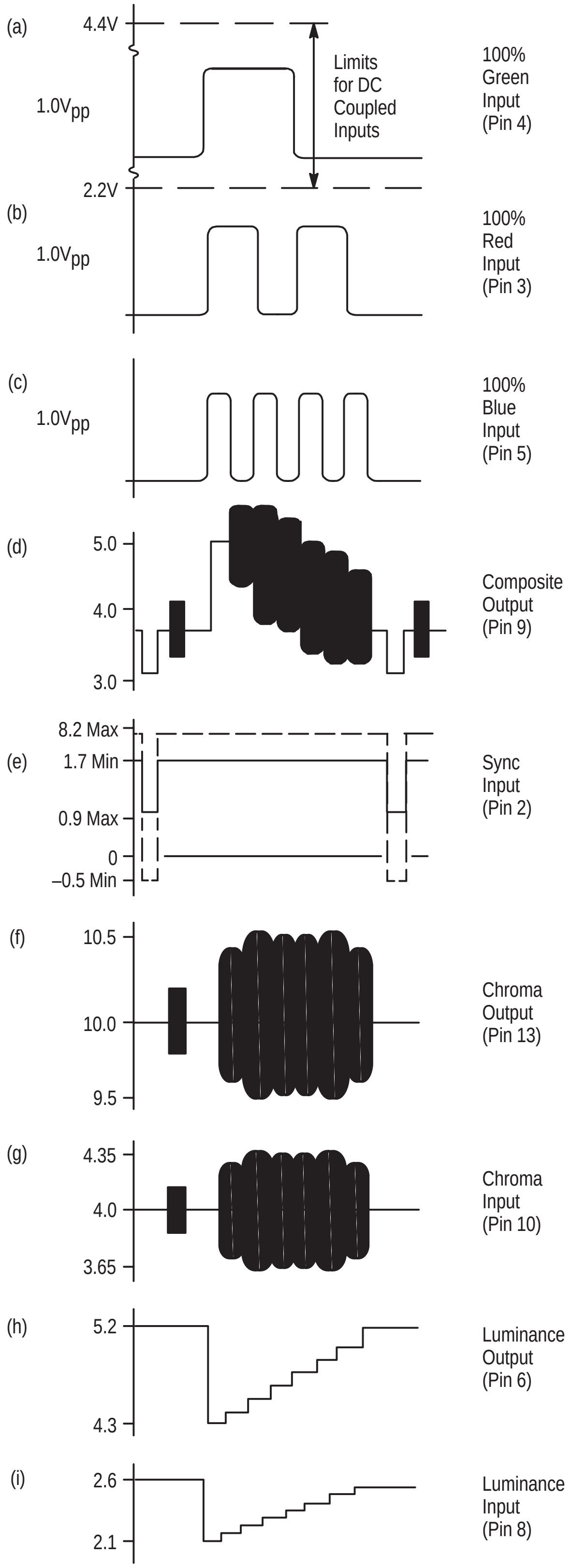

Osc In
17
18
Osc Out
19
Quad Decoup
14
+12V
16
+8.2V
15
Gnd
PAL/NTSC
20
2
Comp Sync
1
TRISE
3
R–IN
4
G–IN
5
B–IN
R4 2.0k
T4
T5
T6
R5 470
R8 220
R9 220
R7 4.0k
T14
C2 18pF
R18 220
R20 220
T15
T16
T17
R161 15k
T11
T12
R10 5.0k
R15 1.5k
R162 220
T7
T8
C1 5pF
R6 5.1k
R6A 5.1k
T2
T3
T10
R16 1.0k
R17 1.0k
T13
T24
T25
T26
T27
T19
R23 1.5k
R24 1.5k
T20
Z1
R2 1.2k
T9
T18
T1
R2A 1.0k
R3 6.8k
R13 22k
R11 22k
R12 10k
R14 22k
R22 270
R9 22k
560 R25
560 R26
T22
R80A 4.0k
R77 15k
R71 22k
R80 B 6.0k
R83 10k
R79 1.0k
R86 10k
R87 13.8k
T77
T68
T69
T73
T74
R76 15k
R78 15k
Z2
T75
R90 22k
T76
R88 30.4k
R95 18k
R81 22k
R82 22k
22k
T81
T82
T79
T72
T78
T79
T80
10k R69
T71
R91 10k
R70 10k
R72 22k
R73 22k
R74 10k
R75 10k
R85 10k
R92 2.2k
R93 2.2k
R94 2.2k
R118 10k
R100 22k
R105 7.5k
R111 4.7k
T91A
T91B
T97
T105
T107
R110 1.0k
T206
R102 1.0k
T96
T95
R106 9.1k
R109 22k
R96 22k
R97 22k
R112 36k
R113 27k
R107 820
R117 10k
R120 27k
R101 10k
T98
T99
T100
T101
R121 27k
T90
R98 22k
T92
T93
T94
T108
T109
T103
T102
T104
R99 10k
R160 22k
R104 2.0k
R104 15k
R108 2.7k
R164 4.7k
R115 18k
R116 3.9k
R119 5.3k
R122 18k

Figure 8. Internal Schematic



APPLICATION INFORMATION

Figure 8. Signal Voltages (Circuit Values of Figure 7)



R, G, B Input Levels

The signal levels into Pins 3, 4, 5 should be 1.0 V_{pp} for fully saturated, standard composite video output levels as shown in Figure 9(d). The inputs require 1.0 V_{pp} since the internally generated sync pulse and color burst are at fixed and predetermined amplitudes.

Further, it is essential that the portion of each input which occurs during the sync interval represent black for that input since that level will be clamped to reference black in the color modulators and output stage. This implies that a refinement, such as a difference between black and blanking levels, must be incorporated in the RGB input signals.

If Y, R–Y, B–Y and burst flag components are available and the MC1377 is operating in NTSC, inputs may be as follows: the Y component can be coupled through a 15 pF capacitor to Pins 3, 4 and 5 tied together; the (–[R–Y]) component can be coupled to Pin 12 through a 0.1 µF capacitor, and the (–[B–Y]) and burst flag components can be coupled to Pin 11 in a similar manner.

Sync Input

As shown in Figure 9(e), the sync input amplitude can be varied over a wide latitude, but will require bias pull–up from most sync sources. The important requirements are:

1) The voltage level between sync pulses must be between 1.7 V and 8.2 V, see Figure 9(e).
2) The voltage level for the sync tips must be between +0.9 V and – 0.5 V, to prevent substrate leakage in the IC, see Figure 9(e).
3) The width of the sync pulse should be no longer than 5.2 µs and no shorter than 2.5 µs.

For PAL operation, correctly serrated vertical sync is necessary to properly trigger the PAL divider. In NTSC mode, simplified “block” vertical sync can be used but the loss of proper horizontal timing may cause “top hook” or “flag waving” in some monitors. An interesting note is that composite video can be used directly as a sync signal, provided that it meets the sync input criteria.

Latching Ramp (Burst Flag) Generator

The recommended application is to connect a close tolerance (5%) 0.001 µF capacitor from Pin 1 to ground and a resistor of 51 kΩ or 56 kΩ from Pin 1 to V_B (Pin 16). This will produce a burst pulse of 2.5 µs to 3.5 µs in duration, as shown in Figure 10. As the ramp on Pin 1 rises toward the charging voltage of 8.2 V, it passes first through a burst “start threshold” at 1.0 V, then a “stop threshold” at 1.3 V, and finally a ramp reset threshold at 5.0 V. If the resistor is reduced to 43 kΩ, the ramp will rise more quickly, producing a narrower and earlier burst pulse (starting approx. 0.4 µs after sync and about 0.6 µs wide). The burst will be wider and later if the resistor is raised to 62 kΩ, but more importantly, the 5.0 V reset point may not be reached in one full line interval, resulting in loss of alternate burst pulses.

As mentioned earlier, the ramp method does produce burst at full line intervals on the “vertical porches.” If this is not desired, and the MC1377 is operating in the NTSC mode, burst flag may be applied to Pin 1 provided that the tip of the pulse is between 1.0 Vdc and 1.3 Vdc. In PAL mode this method is not suitable, since the ramp isn't available to drive the PAL flip–flop. Another means of inhibiting the burst pulse is to set Pin 1 either above 1.3 Vdc or below 1.0 Vdc for the duration that burst is not desired.

Color Reference Oscillator/Buffer

As stated earlier in the general description, there is an on–board common collector Colpitts color reference oscillator with the transistor base at Pin 17 and the emitter at Pin 18. When used with a common low–cost TV crystal and capacitive divider, about 0.6 V_{pp} will be developed at Pin 17. The frequency adjustment can be done with a series 30 pF trimmer capacitor over a total range of about 1.0 kHz. Oscillator frequency should be adjusted for each unit, keeping in mind that most monitors and receivers can pull in 1200 Hz.

If an external color reference is to be used exclusively, it must be continuous. The components on Pins 17 and 18 can be removed, and the external source capacitively coupled into Pin 17. The input at Pin 17 should be a sine wave with amplitude between 0.5 V_{pp} and 1.0 V_{pp}.

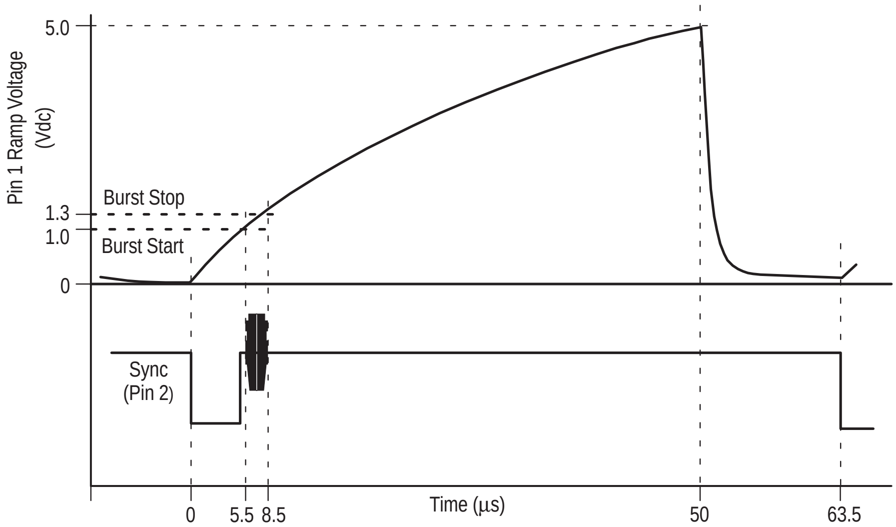
Also, it is possible to do both; i.e., let the oscillator "free run" on its own crystal and override with an external source. An extra coupling capacitor of 50 pF from the external source to Pin 17 was adequate with the experimentation attempted.

Voltage Controlled 90°

The oscillator drives the (B–Y) modulator and a voltage controlled phase shifter which produces an oscillator phase of 90° ± 5° at the (R–Y) modulator. In most situations, the result of an error of 5° is very subtle to all but the most expert eye. However, if it is necessary to adjust the angle to better accuracy, the circuit shown in Figure 11 can be used.

Pulling Pin 19 up will increase the (R–Y) to (B–Y) angle by about 0.25°/µA. Pulling Pin 19 down reduces the angle by the same sensitivity. The nominal Pin 19 voltage is about 6.3 V, so even though it is unregulated, the 12 V supply is best for good control. For effective adjustment, the simplest approach is to apply RGB color bar inputs and use a vectorscope. A simple bar generator giving R, G, and B outputs is shown in Figure 26.

Figure 9. Ramp/Burst Gate Generator



Residual Feedthrough Components

As shown in Figure 9(d), the composite output at Pin 9 for fully saturated color bars is about 2.6 V_{pp}, output with full chroma on the largest bars (cyan and red) being 1.7 V_{pp}. The typical device, due to imperfections in gain, matrixing, and modulator balance, will exhibit about 20 mV_{pp} residual color subcarrier in both white and black. Both residuals can be reduced to less than 10 mV_{pp} for the more exacting applications.

The subcarrier feedthrough in black is due primarily to imbalance in the modulators and can be nulled by sinking or sourcing small currents into clamp Pins 11 and 12 as shown in Figure 12. The nominal voltage on these pins is about 4.0 Vdc, so the 8.2 V regulator is capable of supplying a pull up source. Pulling Pin 11 down is in the 0° direction, pulling it up is towards 180°. Pulling Pin 12 down is in the 90° direction, pulling it up is towards 270°. Any direction of correction may be required from part to part.

White carrier imbalance at the output can only be corrected by juggling the relative levels of R, G, and B inputs for perfect balance. Standard devices are tested to be within 5% of balance at full saturation. Black balance should be adjusted first, because it affects all levels of gray scale equally. There is also usually some residual baseband video at the chroma output (Pin 13), which is most easily observed by disabling the color oscillator. Typical devices show 0.4 V_{pp} of residual luminance for saturated color bar inputs. This is not a major problem since Pin 13 is always coupled to Pin 10 through a bandpass or a high pass filter, but it serves as a warning to pay proper attention to the coupling network.

Figure 10. Adjusting Modulator Angle

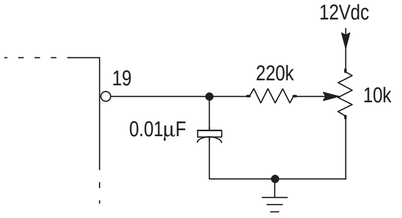


Figure 11. Nulling Residual Color in Black

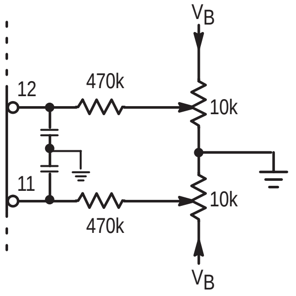
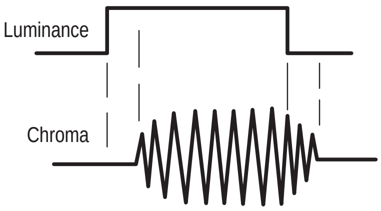


Figure 12. Delay of Chroma Information



The Chroma Coupling Circuits

With the exception of S–VHS equipped monitors and receivers, it is generally true that most monitors and receivers have color IF 6.0 dB bandwidths limited to approximately ±0.5 MHz. It is therefore recommended that the encoder circuit should also limit the chroma bandwidth to approximately ±0.5 MHz through insertion of a bandpass circuit between Pin 13 and Pin 10. However, if S–VHS operation is desired, a coupling circuit which outputs the composite chroma directly for connection to a S–VHS terminal is given in the S–VHS application (see Figure 19).

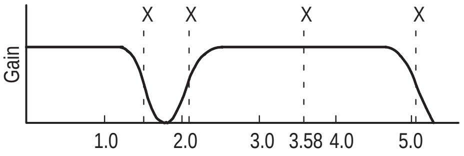
For proper color level in the video output, a ±0.5 MHz bandwidth and a midband insertion loss of 3.0 dB is desired. The bandpass circuit shown in Figure 7, using the TOKO fixed tuned transformer, couples Pin 10 to Pin 13 and gives this result. However, this circuit introduces about 350 ns of delay to the chroma information (see Figure 13). This must be accounted for in the luminance path.

A 350 ns delay results in a visible displacement of the color and black and white information on the final display. The solution is to place a delay line in the luminance path from Pins 6 to 8, to realign the two components. A normal TV receiver delay line can be used. These delay lines are usually of 1.0 kΩ to 1.5 kΩ characteristic impedance, and the resistors at Pins 6 and 8 should be selected accordingly. A very compact, lumped constant delay line is available from TDK (see Figure 25 for specifications). Some types of delay lines have very low impedances (approx. 100 Ω) and should not be used, due to drive and power dissipation requirements.

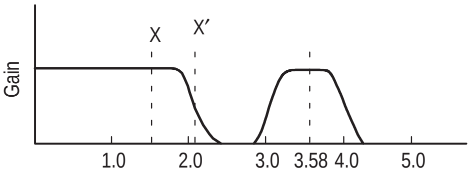
In the event of very low resolution RGB, the transformer and the delay line may be omitted from the circuit. Very low resolution for the MC1377 can be considered RGB information of less than 1.5 MHz. However, in this situation, a bandwidth reduction scheme is still recommended due to the response of most receivers.

Figure 14(a) shows the output of the MC1377 with low resolution RGB inputs. If no bandwidth reduction is employed then a monitor or receiver with frequency response shown in Figure 14(b), which is fairly typical of non–comb filtered monitors and receivers, will detect an incorrect luma sideband at X′. This will result in cross–talk in the form of chroma information in the luma channel. To avoid this situation, a simpler bandpass circuit as shown in Figure 15(a), can be used.

Figure 13. MC1377 Output with Low Resolution RGB Inputs



(a) Encoder Output with Low Resolution Inputs and No Bandpass Transformer



(b) Standard Receiver Response

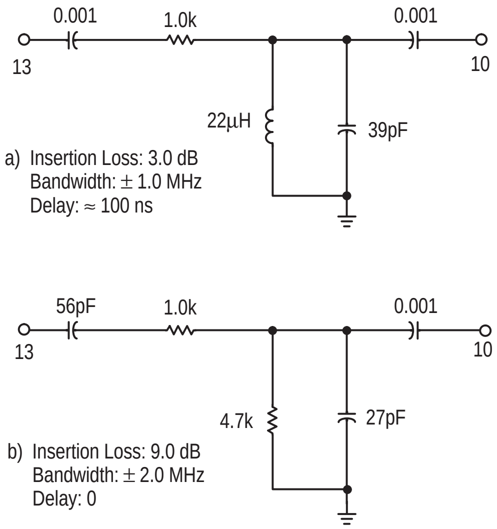
A final option is shown in Figure 15(b). This circuit provides very little bandwidth reduction, but enough to remove the chroma to luma feedthrough, with essentially no delay. There is, however, about a 9 dB insertion loss from this network.

It will be left to the designer to decide which, if any, compromises are acceptable. Color bars viewed on a good monitor can be used to judge acceptability of step luminance/chrominance alignment and step edge transients, but signals containing the finest detail to be encountered in the system must also be examined before settling on a compromise.

The Output Stage

The output amplifier normally produces about 2.0 V_{pp} and is intended to be loaded with 150 Ω as shown in Figure 16. This provides about 1.0 V_{pp} into 75 Ω, an industry standard level (RS–343). In some cases, the input to the monitor may be through a large coupling capacitor. If so, it is necessary to connect a 150 Ω resistor from Pin 9 to ground to provide a low impedance path to discharge the capacitor. The nominal average voltage at Pin 9 is over 4.0 V. The 150 Ω dc load causes the current supply to rise another 30 mA (to approximately 60 mA total into Pin 14). Under this (normal) condition the total device dissipation is about 600 mW. The calculated worst case die temperature rise is 60°C, but the typical device in a test socket is only slightly warm to the touch at room temperature. The solid copper 20–pin lead frame in a printed circuit board will be even more effectively cooled.

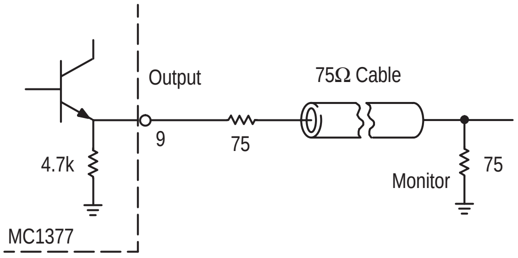
Figure 14. Optional Chroma Coupling Circuits



Power Supplies

The MC1377 is designed to operate from an unregulated 10 V to 14 Vdc power supply. Device current into Pin 14 with open output is typically 35 mA. To provide a stable reference for the ramp generator and the video output, a high quality 8.2 V regulator can supply up to 10 mA for external uses, with an effective source impedance of less than 1.0 Ω. This regulator is convenient for a tracking dc reference for dc coupling the output to an RF modulator. Typical turn–on drift for the regulator is approximately –30 mV over 1 to 2 minutes in otherwise stable ambient conditions.

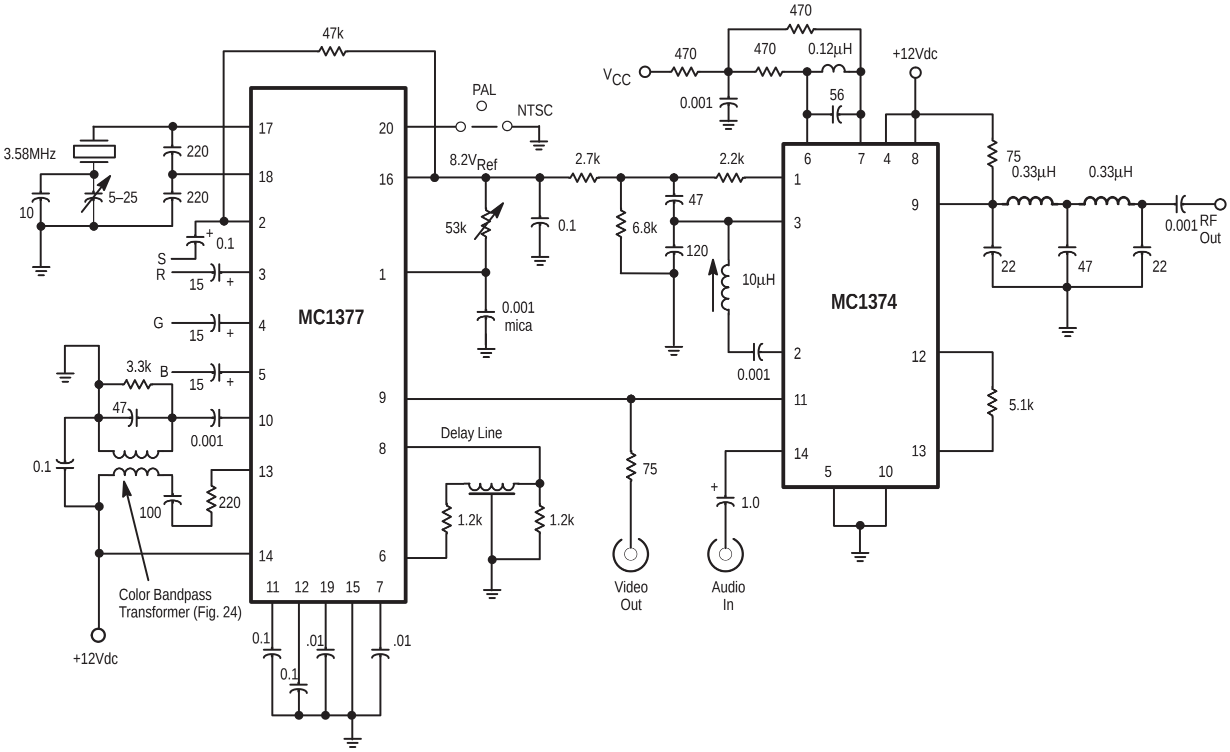
Figure 15. Output Termination



SUMMARY

The preceding information was intended to detail the application and basis of circuit choices for the MC1377. A complete MC1377 application with the MC1374 VHF modulator is illustrated in Figure 17. The internal schematic diagram of the MC1377 is provided in Figure 8.

Figure 16. Application with VHF Modulator



APPLICATIONS INFORMATION

S–VHS

In full RGB systems (Figure 18), three information channels are provided from the signal source to the display to permit unimpaired image resolution. The detail reproduction of the system is limited only by the signal bandwidth and the capability of the color display device. Also, higher than normal sweep rates may be employed to add more lines within a vertical period and three separate projection picture tubes can be used to eliminate the “shadow mask” limitations of a conventional color CRT.

Figure 21 shows the “baseband” components of a studio NTSC signal. As in the previous example, energy is concentrated at multiples of the horizontal sweep frequency. The system is further refined by precisely locating the color subcarrier midway between luminance spectral components. This places all color spectra between luminance spectra and can be accomplished in the MC1377 only if “full interlaced” external color reference and sync are applied. The individual components of luminance and color can then be separated by the use of a comb filter in the monitor or receiver. This technique has not been widely used in consumer products, due to cost, but it is rapidly becoming less expensive and more common. Another technique which is gaining popularity is S–VHS (Super VHS).

In S–VHS, the chroma and luma information are contained on separate channels. This allows the bandwidth of both the chroma and luma channels to be as wide as the monitors ability to reproduce the extra high frequency information. An output coupling circuit for the composite chroma using the TOKO transformer is shown in Figure 19. It is composed of the bandpass transformer and an output buffer and has the frequency performance shown in Figure 20. The composite output (Pin 9) then produces the luma information as well as composite sync and blanking.

Figure 17. Spectra of a Full RGB System

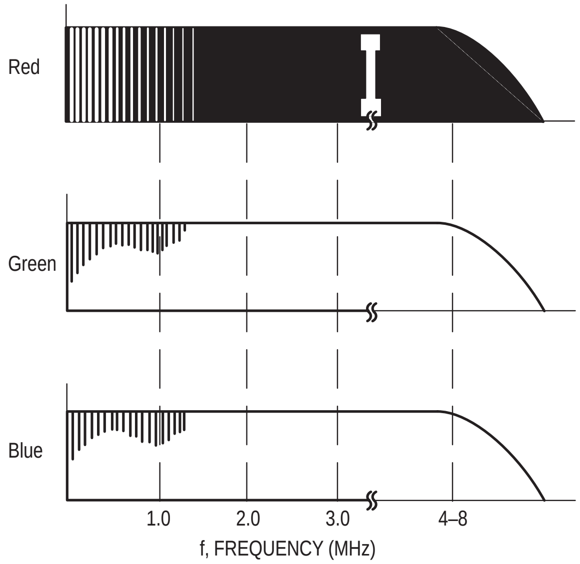
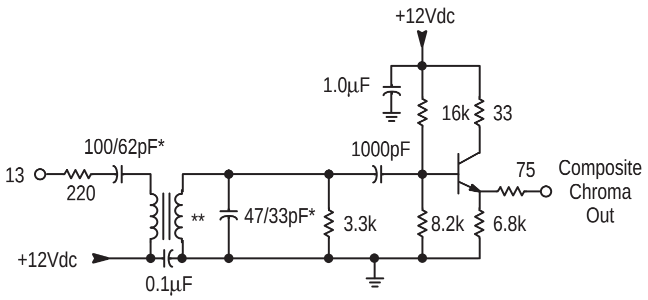
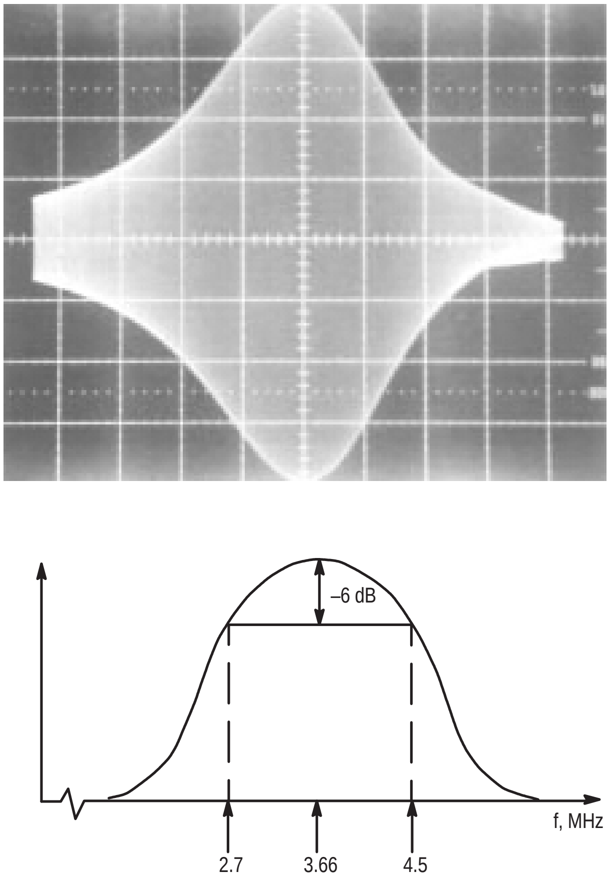


Figure 18. S–VHS Output Buffer



*Refers to different component values used for NTSC/PAL (3.58 MHz/4.43 MHz).
**Toko 166NNF–1026AG

Figure 19. Frequency Response of Chroma Coupling Circuit



I/Q System versus (R–Y)/(B–Y) System

The NTSC standard calls for unequal bandwidths for I and Q (Figure 21). The MC1377 has no means of processing the unequal bandwidths because the I and Q axes are not used (Figure 22) and because the outputs of the (R–Y) and the (B–Y) modulators are added before being output at Pin 13. Therefore, any bandwidth reduction intended for the chroma information must be performed on the composite chroma information. This is generally not a problem, however, since most monitors compromise the standard quite a bit.

Figure 23 shows the typical response of most monitors and receivers. This figure shows that some crosstalk between luma and chroma information is always present. The acceptability of the situation is enhanced by the limited ability of the CRT to display information above 2.5 MHz. If the signal from the MC1377 is to be used primarily to drive conventional non–comb filtered monitors or receivers, it would be best to reduce the bandwidth at the MC1377 to that of Figure 23 to lessen crosstalk.

Figure 20. NTSC Standard Spectral Content

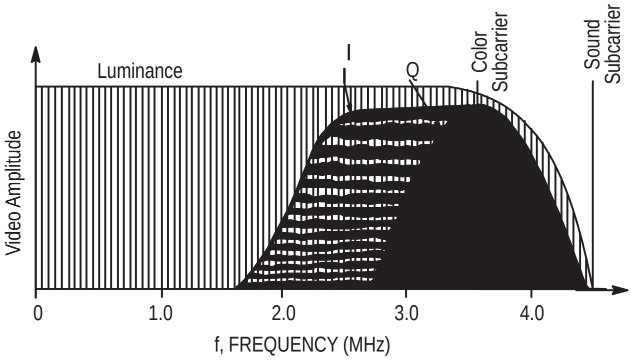


Figure 21. Color Vector Relationship (Showing Standard Colors)

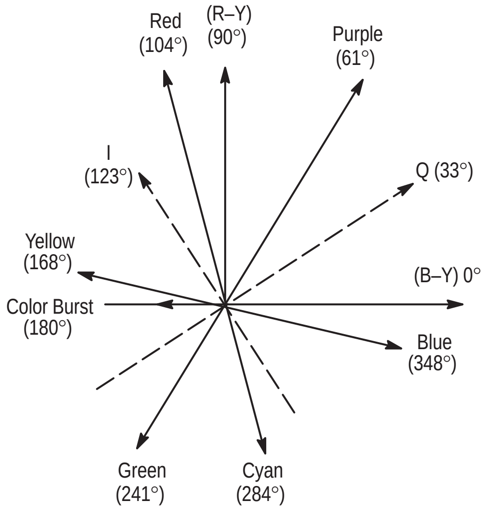


Figure 22. Frequency Response of Typical Monitor/TV

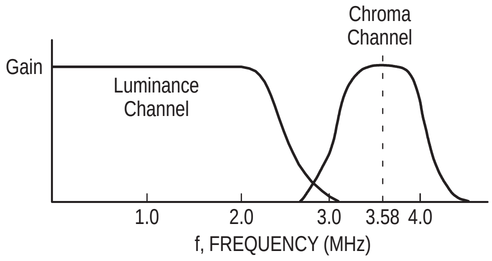
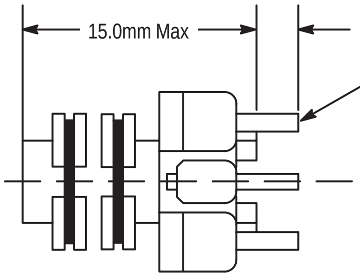
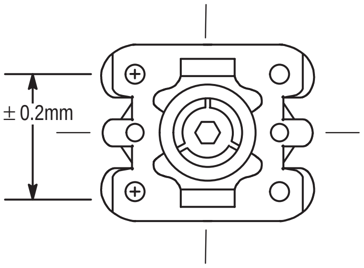
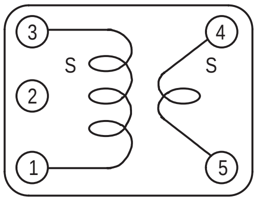


Figure 23. A Prototype Chroma Bandpass Transformer Toko Sample Number 166NNF–10264AG





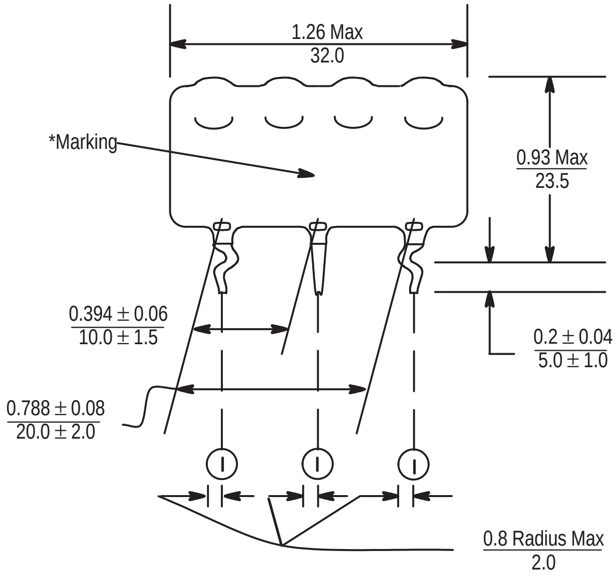


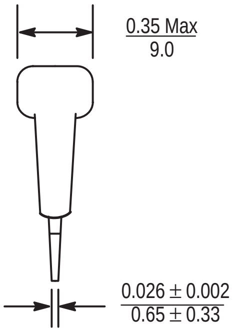
(Drawing Provided By:
Toko America, Skokie, IL)

Connection Diagram
Bottom View

Unloaded Q (Pins 1–3): 15 @ 2.5 MHz
Inductance: 30 μH ± 10% @ 2.5 MHz
Turns: 60 (each winding)
Wire: #38 AWG (0.1 m/m)

Figure 24. A Prototype Delay Line TDK Sample Number DL122301D–1533

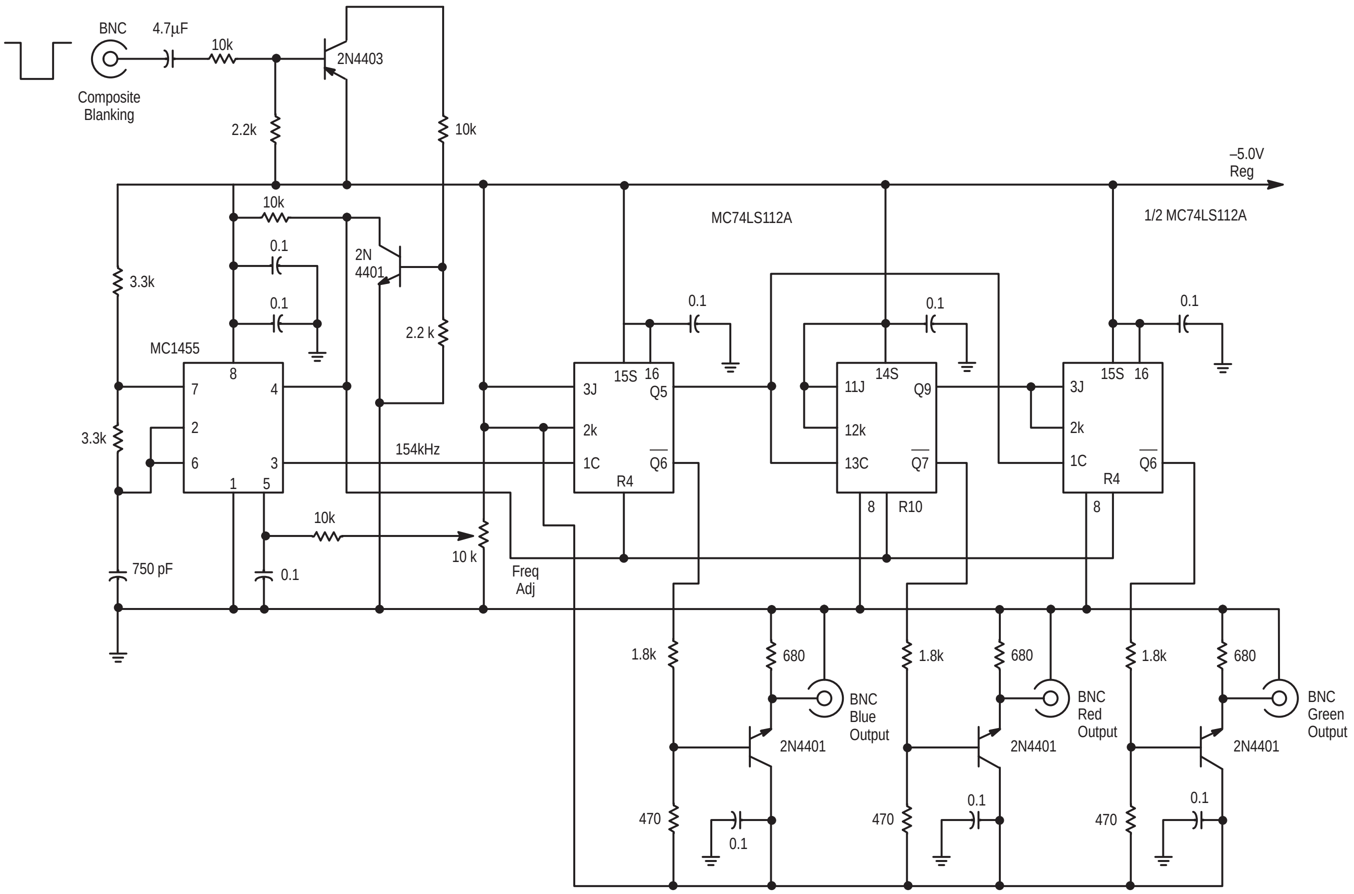




*Marking: Part Number, Manufacturer’s Identification, Date Code and Lead Number.
Skokie, IL (TDK Corporation of America)

Item	Specifications
Time Delay	400 ns ± 10%
Impedance	1200 Ω ± 10%
Resistance	Less Than 15 Ω
Transient Response with 20 ns Rise Time Input Pulse	Preshoot: 10% Max
	Overshoot: 10% Max
	Rise Time: 120 ns Max
Attenuation	3 dB Max at 6.0 MHz

Figure 25. RGB Pulse Generator



RGB Pulse Generator Timing Diagram for NTSC

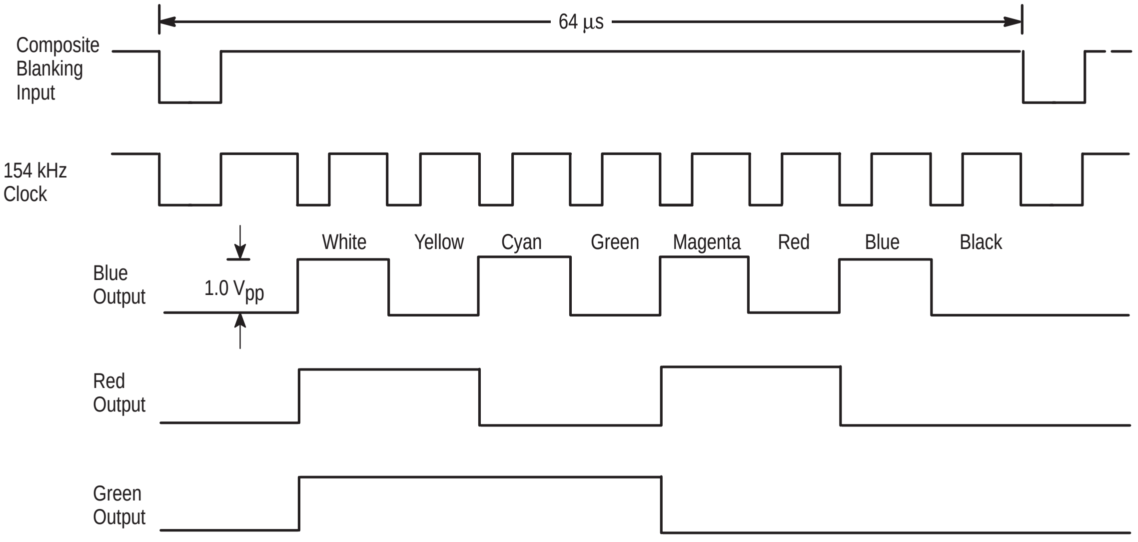
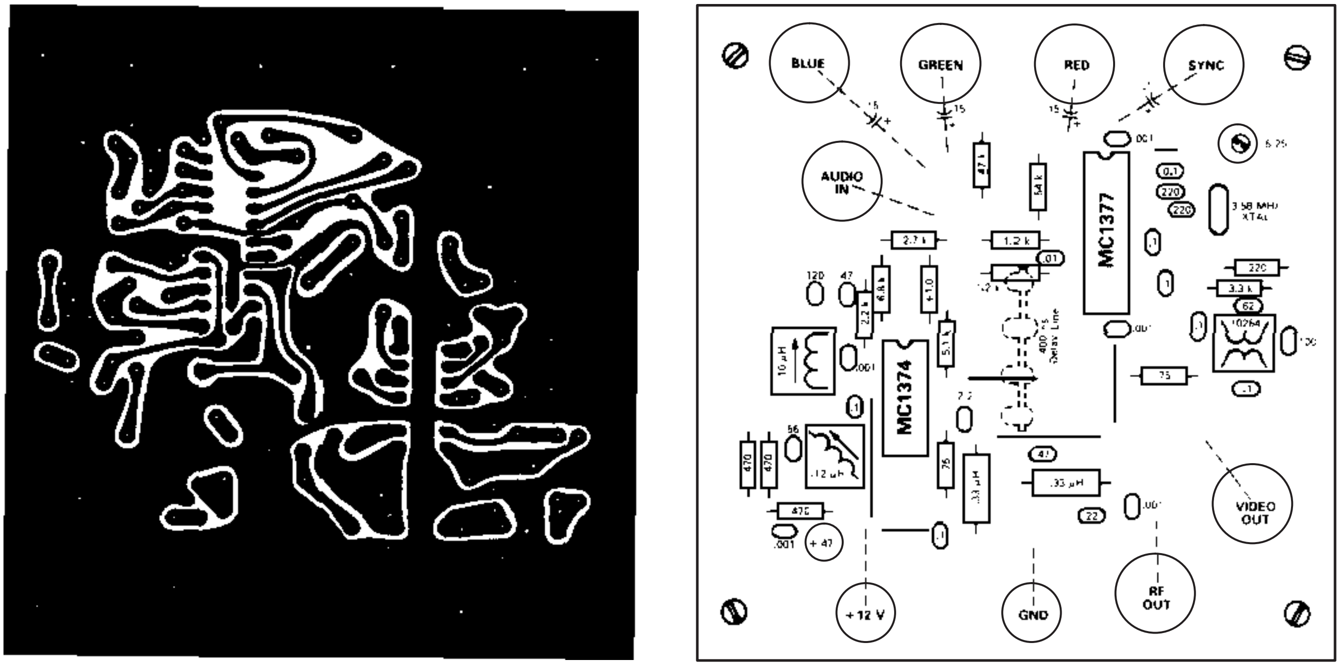


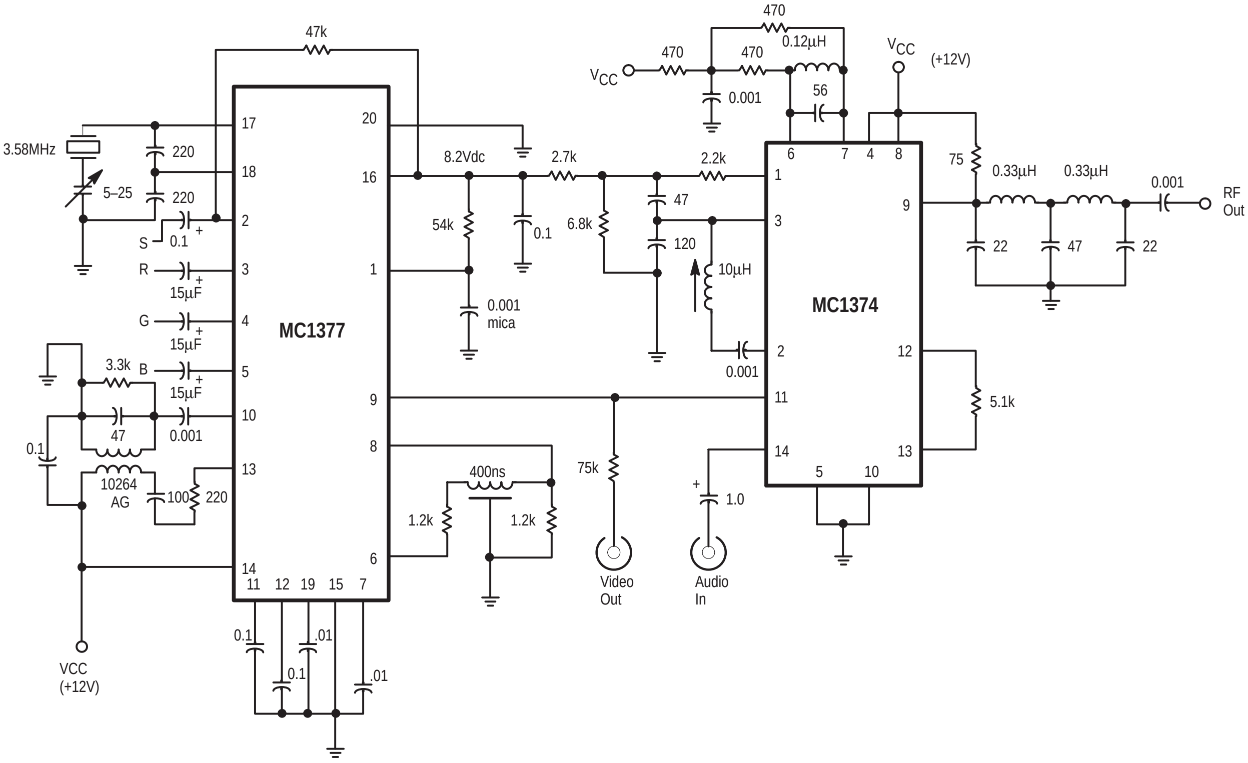
Figure 26. Printed Circuit Boards for the MC1377



(CIRCUIT SIDE)

(COMPONENT SIZE)

Figure 27. Color TV Encoder – Modulator



MOTOROLA

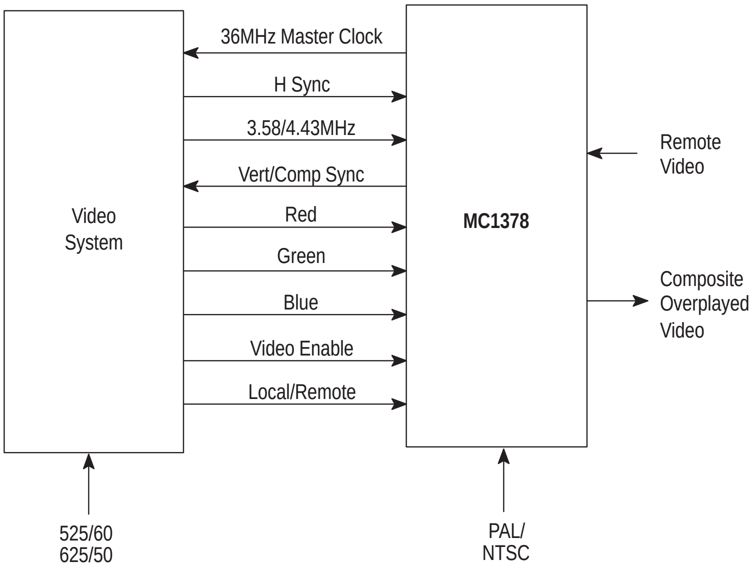
MC1378

Color Television Composite Video Overlay Synchronizer

The MC1378 is a bipolar composite video overlay encoder and microcomputer synchronizer. The MC1378 contains the complete encoder function of the MC1377, i.e., quadrature color modulators, RGB matrix, and blanking level clamps, plus a complete complement of synchronizers to lock a microcomputer–based video source to any remote video source. The MC1378 can be used as a local system timing and encoding source, but it is most valuable when used to lock the microcomputer source to a remotely originated video signal.

- Contains All Needed Reference Oscillators
- Can Be Operated in PAL or NTSC Mode, 625 or 525 Line
- Wideband, Full–Fidelity Color Encoding
- Local or Remote Modes of Operation
- Minimal External Components
- Designed to Operate from 5.0 V supply
- Will Work with non standard Video

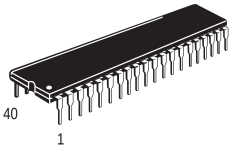
Figure 1. Simplified Application

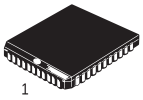


COLOR TELEVISION COMPOSITE VIDEO OVERLAY SYNCHRONIZER

SEMICONDUCTOR TECHNICAL DATA

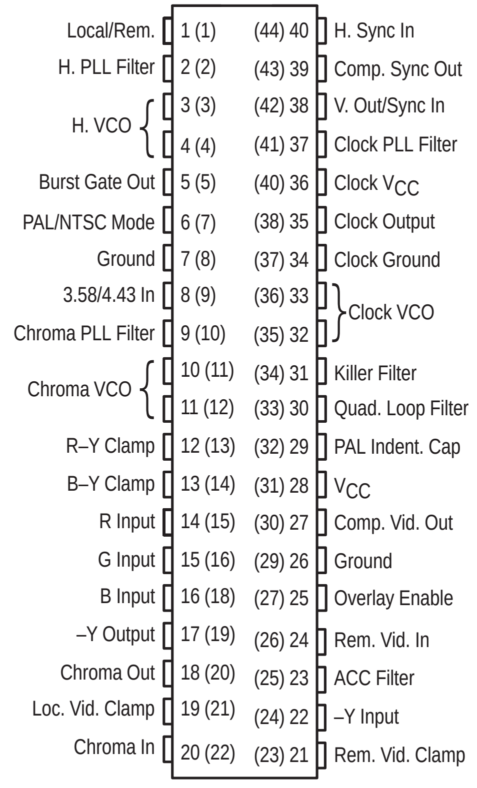
P SUFFIX
PLASTIC PACKAGE
CASE 711





FN SUFFIX
PLASTIC PACKAGE
CASE 777
(PLCC–44)

PIN CONNECTIONS



* ( ) PLCC Pin Assignments

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC1378P	T_A = 0° to +70°C	Plastic DIP
MC1378FN		PLCC–44

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	6.0	Vdc
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	–65 to +150	°C
Junction Temperature	$T_{J(max)}$	150	°C
Power Dissipation, Package Derate above 25°C	P_D	1.25 10	W mW/°C

RECOMMENDED OPERATING CONDITIONS

Condition	Pin	Value	Unit
Supply Voltage	28, 36	5.4 ± 0.25	Vdc
RGB Input for 100% Saturation	14, 15, 16	1.0	Vpp
Color Oscillator Input Level	8	0.5	Vpp
Video Input, Positive	24	1.0	Vpp

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C, circuit of Figure 4 or 5)

Characteristics		Pin	Min	Typ	Max	Unit
Supply Current		28, 36	–	100	–	mAdc
Video Output, Open Circuit, Positive		27	–	2.0	9.4	V_{pp}
Modulation Angle (R – Y) to (B – Y)		–	87	90	93	Degrees
RGB Input Impedance		14, 15, 16	–	10	–	kΩ
Local/Remote Switch (TTL)	High Low	1	–	Remote Local	–	–
Horizontal Sync Input, Negative Going	(TTL)	40	–	4.3	–	V_{pp}
Vertical Sync Output, Negative Going, Remote Mode	(TTL)	38	–	4.3	–	V_{pp}
Composite Sync Output, Negative Going	(TTL)	39	–	4.3	–	V_{pp}
Burst Gate Output, Positive Going	(TTL)	5	–	4.3	–	V_{pp}

Description of Operation – Refer to Figures 3, 4

Remote Mode	Local Mode
The incoming remote video signal (Pin 24) supplies all synchronizing information. A discussion of the function of the phase detectors helps to clarify the lockup method: PD1 — locks the internally counted–down 4 MHz horizontal VCO to the incoming horizontal sync. It is fast acting, to follow VCR source fluctuations. PD2 — locks the 36 MHz clock VCO, which is divided down by the video system, to the divided down horizontal VCO. PD3 — is a gated phase detector which locks the 14 MHz crystal oscillator, divided by 4, to the incoming color burst. PD4 — controls an internal phase shifter to assure that the outgoing color burst is the same phase as incoming burst at PD3. PD5 — not used in REMOTE MODE Vertical lock is obtained by continuously resetting the sync generator in the video system with separated vertical sync from the MC1378, Pin 38. This signal is TTL level vertical block sync, negative going. The horizontal sync from the video system to Pin 40 is also TTL level with sync negative going. The local/remote switch, Pin 1, is in local mode when grounded, remote mode when taken to 5.0 V. The overlay control, Pin 25, has an analog characteristic, centered about 1.0 V, which allows fading from local to remote.	The MC1378 and a video system combine to provide a fully synchronized standard signal source. In this case, composite sync must be supplied by the video system or other time base system. In the MC1378 the phase detectors operate as follows: PD1 — locks the internally counted–down 4 MHz horizontal VCO to a Horizontal Sync signal (at Pin 40) from the video system (counted down from 36 MHz) PD2 — not used in LOCAL MODE. PD3 — not used in LOCAL MODE. PD4 — active, but providing an arbitrary phase shift setting between the color oscillator and the output burst phase. PD5 — locks the 36 MHz clock VCO (which is divided down by the video system) to the 14 MHz (crystal) color oscillator. The 14 MHz is, therefore, the system standard in LOCAL MODE, and is not DC controlled.
	COMPOSITE VIDEO GENERATION The color encoding at the RGB signals is done exactly as in the MC1377. Composite chroma is looped out at Pins 18 and 20 to allow the designer to choose band shaping. Luminance is similarly brought out (Pins 17 and 22) to permit installation of the appropriate delay. Composite sync output, Pin 39, and burst gate output, Pin 5, are provided for convenience only.

Figure 2. Representative Block Diagram

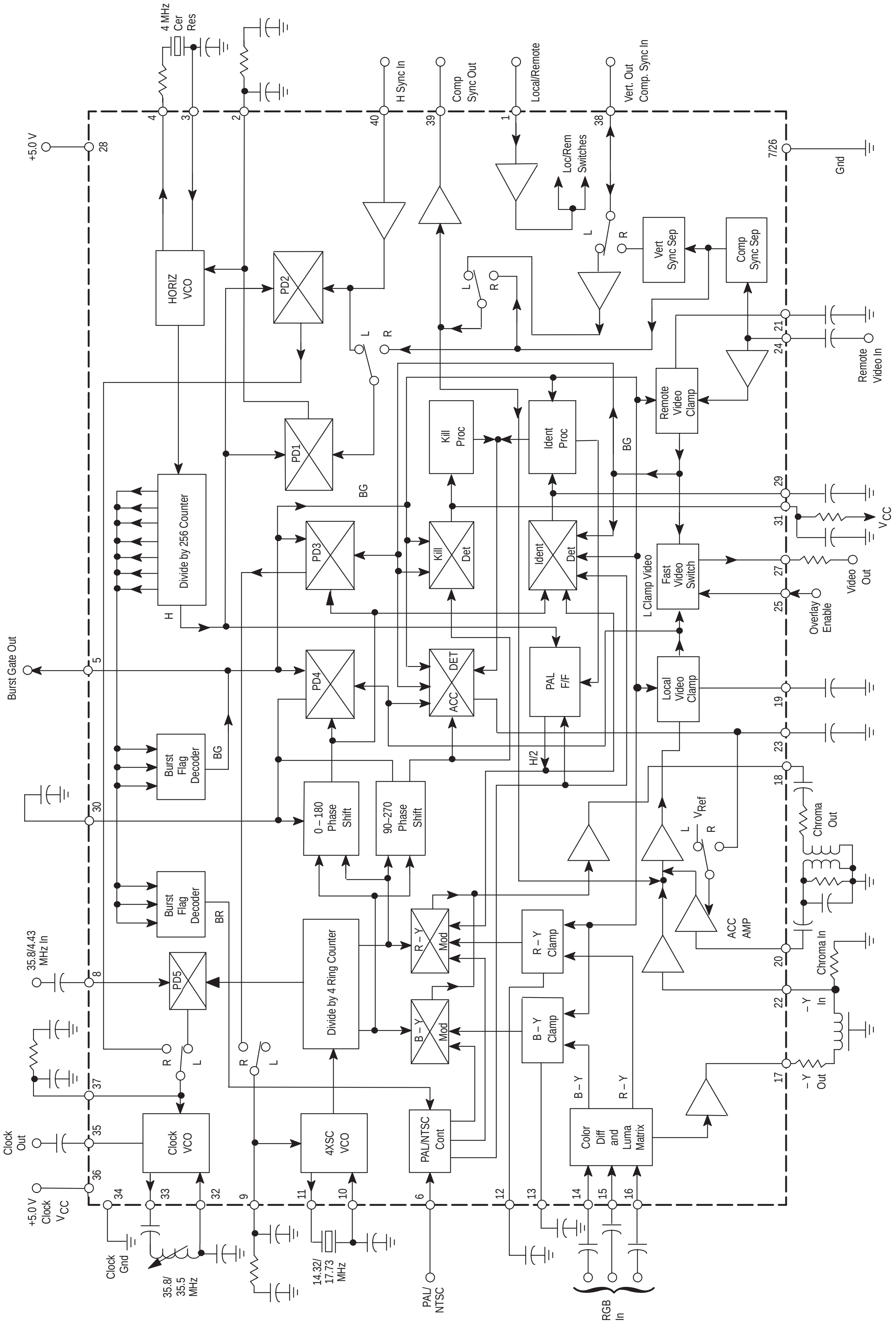


Figure 3. Remote Mode

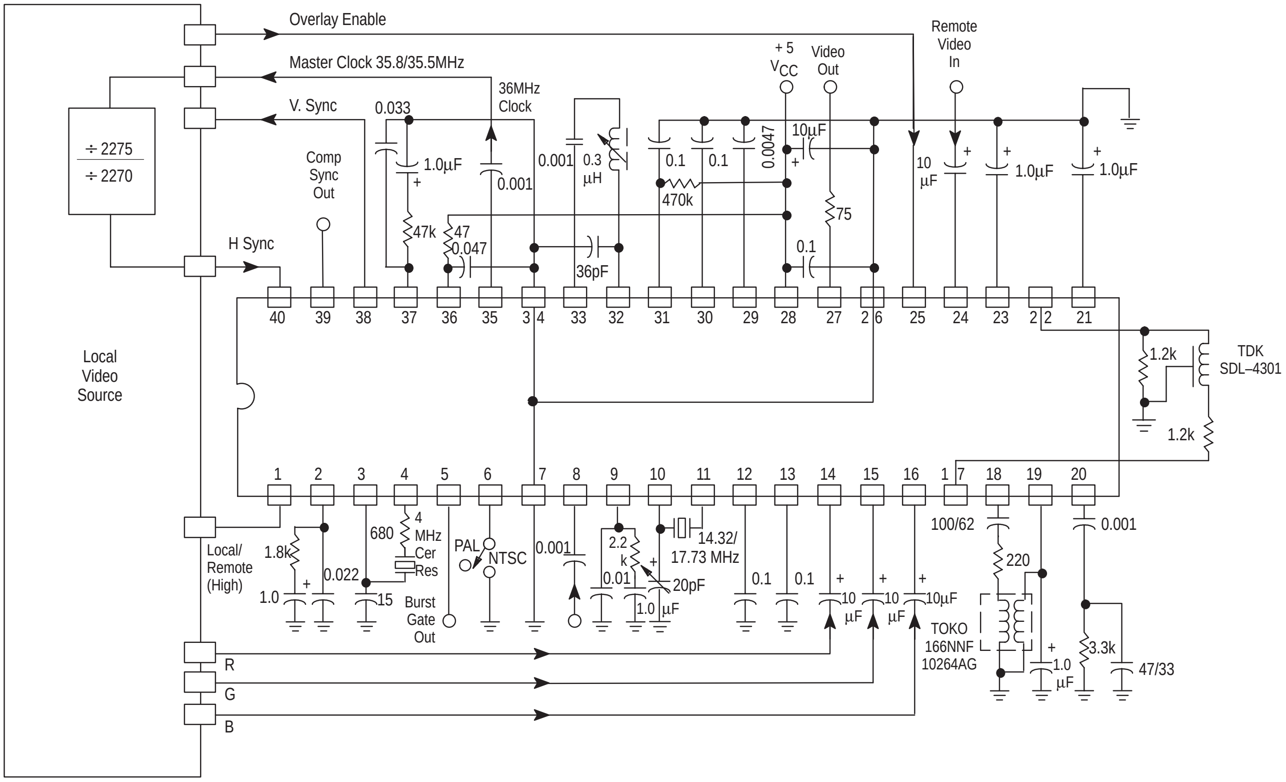
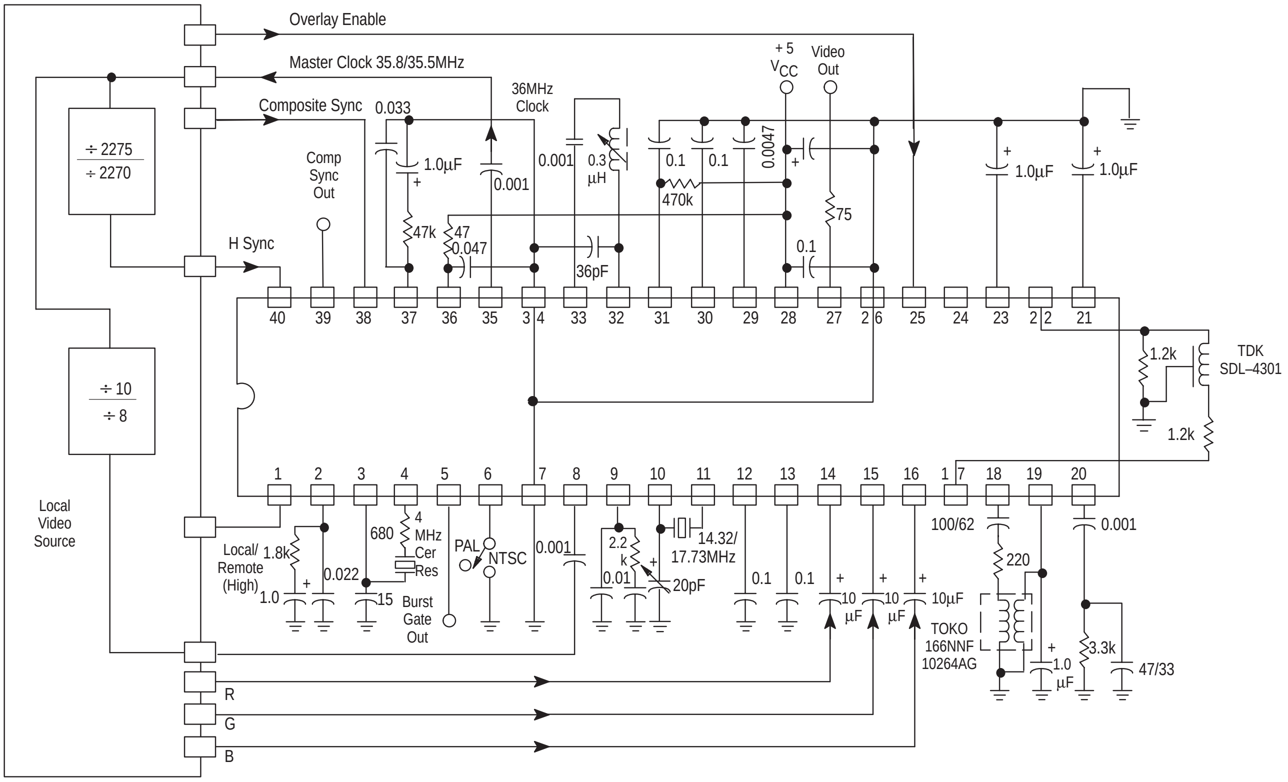


Figure 4. Local Mode



MOTOROLA

MC1391

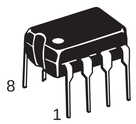
TV Horizontal Processor

The MC1391 provides low–level horizontal sections including phase detector, oscillator and pre–driver. This device was designed for use in all types of television receivers.

- Internal Shunt Regulator
- Preset Hold Control Capability
- ±300 Hz Typical Pull–In
- Linear Balanced Phase Detector
- Variable Output Duty Cycle for Driving Tube or Transistor
- Low Thermal Frequency Drift
- Small Static Phase Error
- Adjustable DC Loop Gain
- Positive Flyback Inputs

TV HORIZONTAL PROCESSOR

SEMICONDUCTOR TECHNICAL DATA

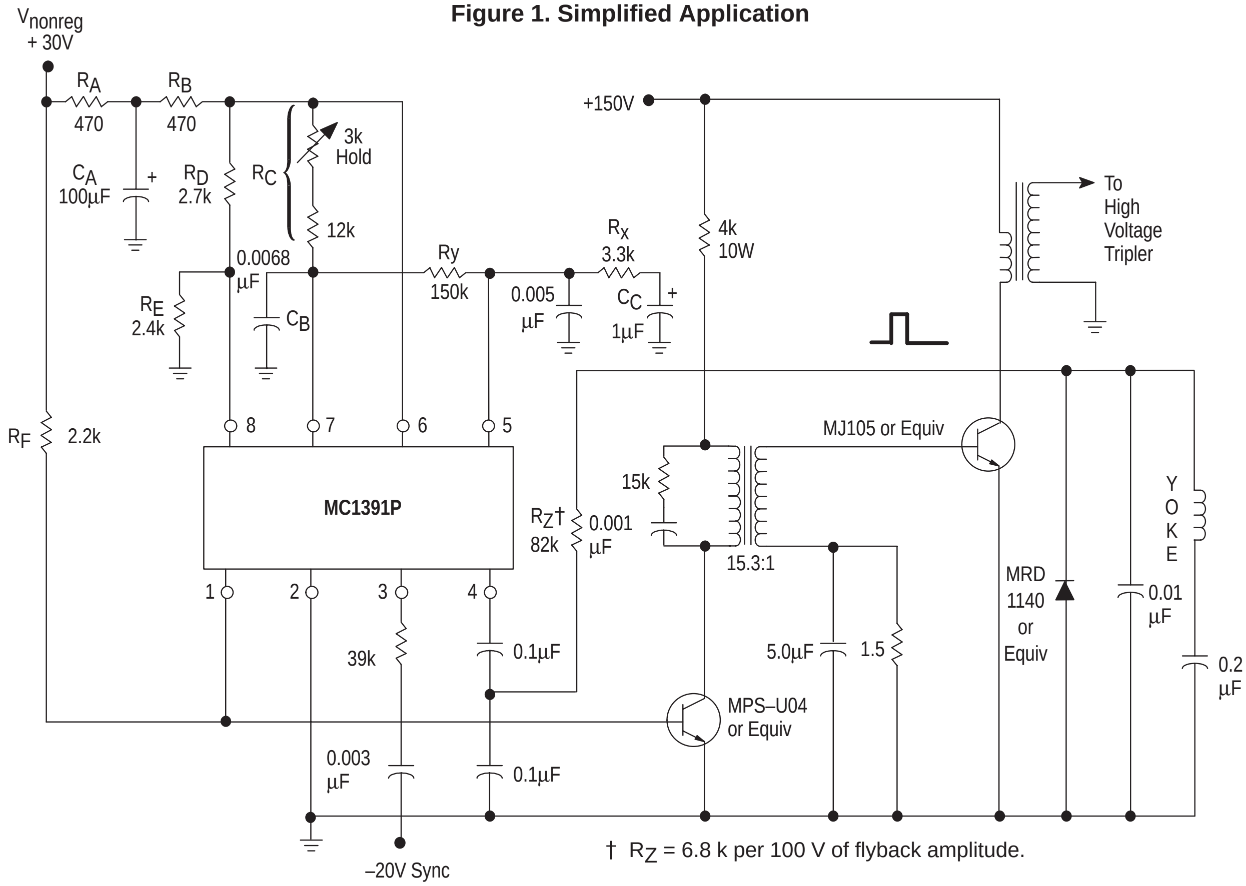


P SUFFIX
PLASTIC PACKAGE
CASE 626

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC1391P	T_A = 0° to +70°C	Plastic DIP

Figure 1. Simplified Application



† R_Z = 6.8 k per 100 V of flyback amplitude.

This circuit has an oscillator pull–in range of ±300 Hz, a noise bandwidth of 320 Hz, and a damping factor of 0.8.

MAXIMUM RATINGS (T_A = +25°C, unless otherwise noted.)

Rating	Value	Unit
Supply Current	40	mAdc
Output Voltage	40	Vdc
Output Current	30	mAdc
Sync Input Voltage (Pin 3)	5.0	V_{pp}
Flyback Input Voltage (Pin 4)	5.0	V_{pp}
Power Dissipation (Package Limitation) Plastic Package Derate above T_A = +25°C	 625 5.0	 mW mW/°C
Operating Temperature Range (Ambient)	0 to +70	°C
Storage Temperature Range	–65 to +150	°C

ELECTRICAL CHARACTERISTICS (T_A = +25°C, unless otherwise noted. See Test Circuit of Figure 2, all switches in position 1.)

Characteristics	Min	Typ	Max	Unit
Regulated Voltage (Pin 6)	8.0	8.6	9.4	Vdc
Supply Current (Pin 6)	–	20	–	mAdc
Collector–Emitter Saturation Voltage (Output Transistor Q1 in Figure 6) (I_C = 20 mA, Pin 1) Vdc	–	0.15	0.25	Vdc
Voltage (Pin 4)	–	2.0	–	Vdc
Oscillator Pull–in Range (Adjust R_H in Figure 2)	–	±300	–	Hz
Oscillator Hold–in Range (Adjust R_H in Figure 2)	–	±900	–	Hz
Static Phase Error (Δf = 300 Hz)	–	0.5	–	µs
Free–running Frequency Supply Dependance (S1 in position 2)	–	±3.0	–	Hz/Vdc
Phase Detector Leakage (Pin 5) (All switches in position 2)	–	–	±1.0	µA
Sync Input Voltage (Pin 3)	2.0	–	5.0	V_{pp}
Sawtooth Input Voltage (Pin 4)	1.0	–	3.0	V_{pp}

Figure 2. Test Circuit

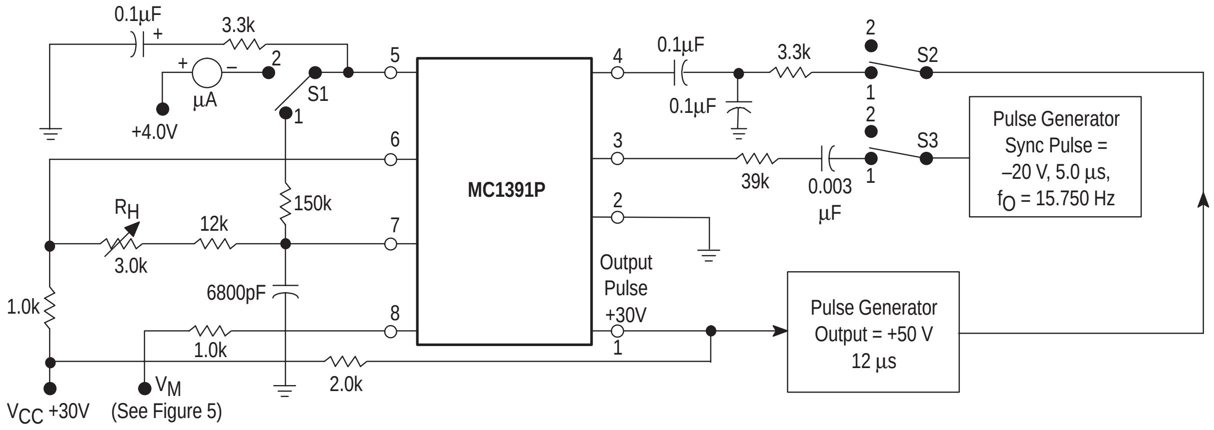


Figure 3. Frequency versus Temperature

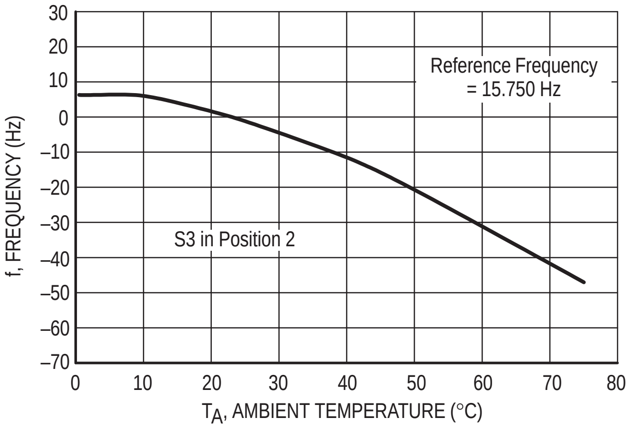


Figure 4. Frequency Drift versus Warm–Up Time

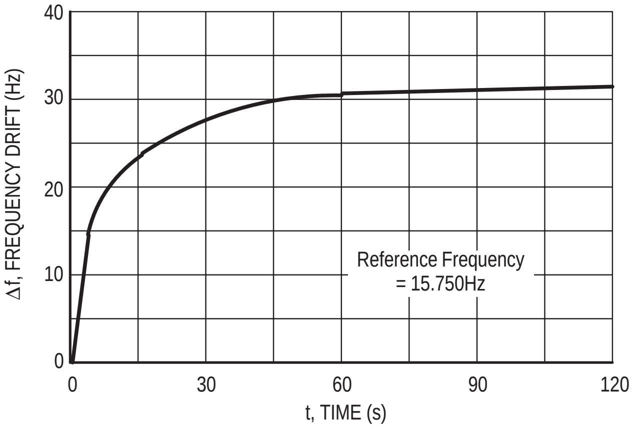


Figure 5. Mark Space Ratio

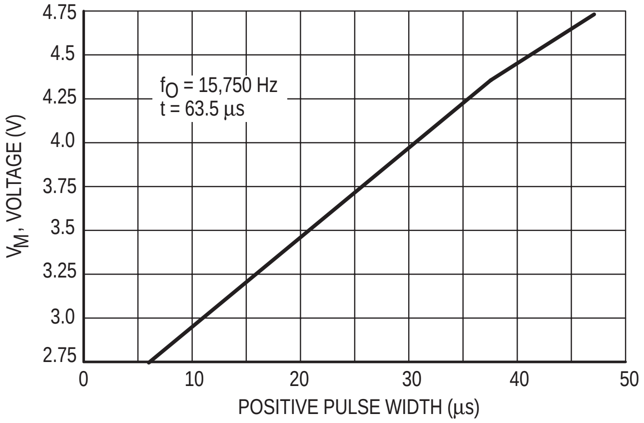
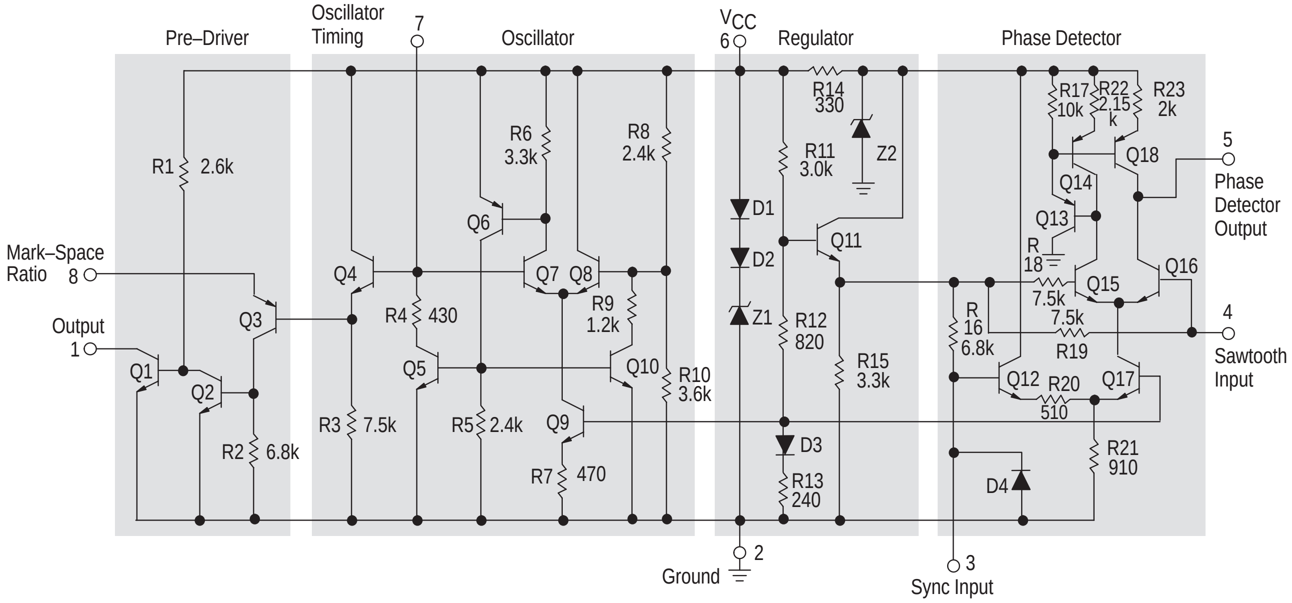


Figure 6. Representative Schematic Diagram



CIRCUIT OPERATION

The MC1391P contains the oscillator, phase detector and predriver sections needed for a television horizontal APC loop.

The oscillator is an RC type with one pin (Pin 7) used to control the timing. The basic operation can be explained easily. If it is assumed that Q7 is initially off, then the capacitor connected from Pin 7 to ground will be charged by an external resistor (R_C) connected to Pin 6. As soon as the voltage at Pin 7 exceeds the potential set at the base of Q8 by resistors R8 and R10, Q7 will turn on and Q6 will supply base current to Q5 and Q10. Transistor Q10 will set a new, lower potential at the base of Q8 determined by R8, R9 and R10. At the same time, transistor Q5 will discharge the capacitor through R4 until the base bias of Q7 falls below that of Q8, at which time Q7 will turn off and the cycle repeats.

The sawtooth generated at the base of Q4 will appear across R3 and turn off Q3 whenever it exceeds the bias set on Pin 8. By adjusting the potential at Pin 8, the duty cycle (MSR) at the predriver output pin (Pin 1) can be changed to accommodate either tube or transistor horizontal output stages.

The phase detector is isolated from the remainder of the circuit by R14 and Z2. The phase detector consists of the comparator Q15, Q16 and the gated current source Q17. Negative going sync pulses at Pin 3 turn off Q12 and the current division between Q15 and Q16 will be determined by the phase relationship of the sync and the sawtooth waveform at Pin 4, which is derived from the horizontal flyback pulse. If there is no phase difference between the sync and sawtooth, equal currents will flow in the collectors of Q15 and Q16 each of half the sync pulse period. The current in Q15 is turned around by Q18 so that there is no net output current at Pin 5 for balanced conditions. When a phase offset occurs, current will flow either in or out of Pin 5. This pin is connected via an external low–pass filter to Pin 7, thus controlling the oscillator.

Shunt regulation for the circuit is obtained with a zero temperature coefficient from the series combination of D1, D2 and Z1.

APPLICATION INFORMATION

Although it is an integrated circuit, the MC1391P has all the flexibility of a conventional discrete component horizontal APC loop. The internal temperature compensated voltage regulator allows a wide supply voltage variation to be tolerated, enabling operation from nonregulated power supplies. A minimum value for supply current into Pin 6 to maintain zener regulation is about 18 mA. Allowing 2.0 mA for the external dividers

$$R_A + R_B = \frac{V_{nonreg(min)} - 8.8}{20 \times 10^{-3}}$$

Components R_A, R_B and C_A are used for ripple rejection. If the supply voltage ripple is expected to be less than 100 mV (for a 30 V supply) then R_A and R_B can be combined and C_A omitted.

The output pulse width can be varied from 6.0 µs to 48 µs by changing the voltage at Pin 8 (see Figure 5). However, care should be taken to keep the lead lengths to Pin 8 as short as possible at Pin 1. The parallel impedance of R_D and R_E should be close to 1.0 kΩ to ensure stable pulse widths. For 15 mA drive at saturation

$$R_F = \frac{V_{nonreg} - 0.3}{15 \times 10^{-3}}$$

The oscillator free–running frequency is set by R_C and C_B connected to Pin 7. For values of $R_C \geq R_{discharge}$ (R4 in Figure 6), a useful approximation for the free–running frequency is

$$f_O = \frac{1}{0.6\, R_C C_B}$$

Proper choice of R_C and C_B will give a wide range of oscillator frequencies – operation at 31.5 kHz for countdown circuits is possible for example. As long as the product $R_C C_B \approx 10^{-4}$ many combinations of values of R_C and C_B will satisfy the free–running frequency requirement of 15.734 kHz. However, the sensitivity of the oscillator (β) to control–current from the phase detector is directly dependent on the magnitude of R_C, and this provides a convenient method of adjusting the dc loop gain (fc).

For a given phase detector sensitivity (µ) = 1.60 x 10^{-4} A/rad

$$fc = \mu\beta \text{ and } \beta = 3.15 \times R_C \text{ Hz/mA}$$

Increasing R_C will raise the dc loop gain and reduce the static phase error (S.P.E.) for a given frequency offset. Secondary effects are to increase the natural resonant frequency of the loop (ω_n) and give a wider pull–in range from an out–of–lock condition. The loop will also tend to be underdamped with fast pull–in times, producing good airplane flutter performance. However, as the loop becomes more underdamped impulse noise can cause shock excitation of the loop. Unlimited increase in the dc loop gain will also raise the noise bandwidth excessively causing horizontal jitter with thermal noise. Once the dc loop gain has been selected for adequate SPE performance, the loop filter can be used to produce the balance between other desirable characteristics. Damping of the loop is achieved most directly by changing the resistor R_X with respect to R_Y which modifies the ac/dc gain ration (m) of the loop. Lowering this ratio will reduce the pull–in range and noise bandwidth (fnn). (Note: very large values of R_Y will limit the control capability of the phase detector with a corresponding reduction in hold–in range.)

Static phasing can be adjusted simply by adding a small resistor between the flyback pulse integrating capacitor and ground. The sync coupling capacitor should not be too small or it can charge during the vertical pulse and this may result in picture bends at the top of the CRT.

Note: In adjusting the loop parameters, the following equations may prove useful:

$$f_{nn} = \frac{1 \times \chi^2 T\omega_C}{4\chi T} \qquad \chi = \frac{R_X}{RY}$$

$$w_n = \sqrt{\frac{\omega_C}{(1 + c)T}} \qquad \omega_C = 2\pi fc$$

$$T = Ry\, CC$$

$$K = \frac{\chi^2 T\omega_C}{4}$$

where: K = loop damping coeffecient

MOTOROLA

MC3340

Electronic Attenuator

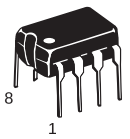
The MC3340 is a simple but very effective electronic attenuator. This device offers up to 80 dB of attenuation control for frequencies to 1.0 MHz. THD (distortion) is less than 1% – up to 15 dB attenuation and less than 3% – up to 40 dB.

Typical uses include instrumentation control, remote control audio amplifiers, electronic games, and CATV (cable TV) set–top converter audio control.

- Designed for use in:
  - DC Operated Volume Control
  - Compression and Expansion Amplifier Applications
- Controlled by DC Voltage or External Variable Resistor
- Economical 8–Pin Dual–In–Line Package

ELECTRONIC ATTENUATOR

SEMICONDUCTOR
TECHNICAL DATA



P SUFFIX
PLASTIC PACKAGE
CASE 626

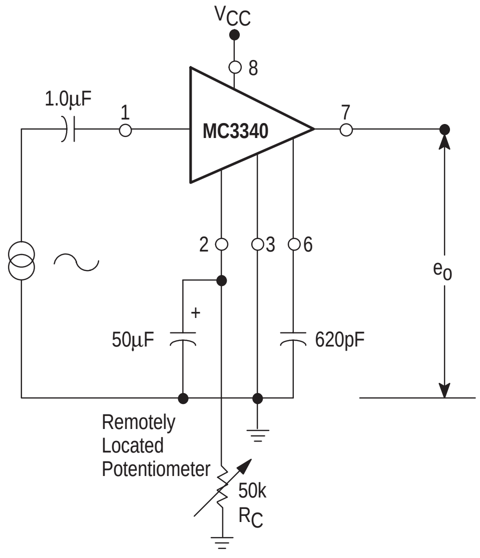
MAXIMUM RATINGS (T_A = +25°C, unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	20	Vdc
Power Dissipation @ T_A = 25°C Derate above T_A = 25°C	P_D	1.2 10	W mW/°C
Operating Ambient Temperature Range	T_A	0 to +75	°C

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC3340P	T_A = 0° to +75°C	Plastic DIP

Figure 1. Typical DC Remote Volume Control



ELECTRICAL CHARACTERISTICS (e_{in} = 100 mVrms, f = 1.0 kHz, V_{CC} = 16 Vdc, T_A = +25°C, unless otherwise noted.)

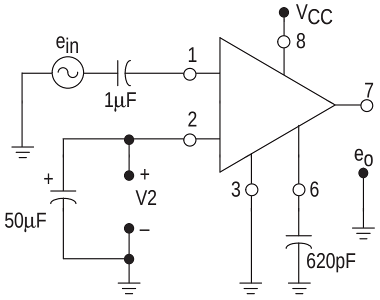
Circuit	Characteristics	Min	Typ	Max	Unit
	Operating Power Supply Voltage	0.8	–	18	Vdc
	Control Terminal Sink Current, Pin 2 (e_{in} = 0)	–	–	2.0	mAdc
	Maximum Input Voltage	–	–	0.5	Vrms
	Voltage Gain	11	13	–	dB
	Attenuation Range from Maximum Gain (V2 = 6.5 Vdc)	70	80	–	dB
	Total Harmonic Distortion (Pin 2 Gnd) (e_{in} = 100 mVrms, $e_o = A_v \bullet e_{in}$)	–	0.6	1.0	%

Figure 2. Representative Schematic Diagram

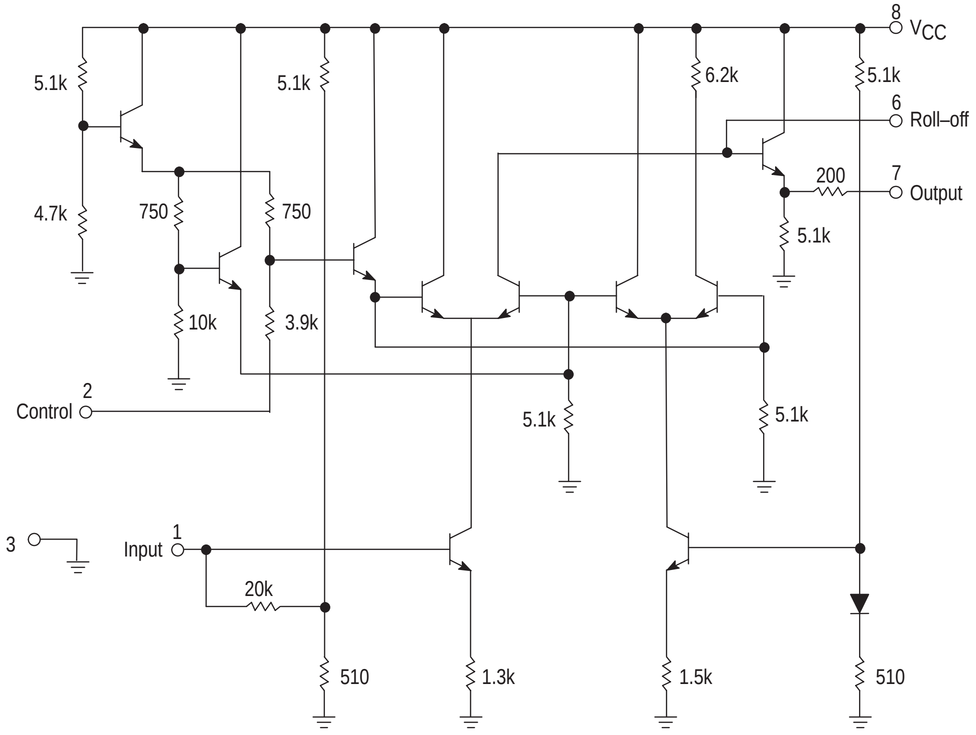


Figure 3. Attenuation versus DC Control Voltage

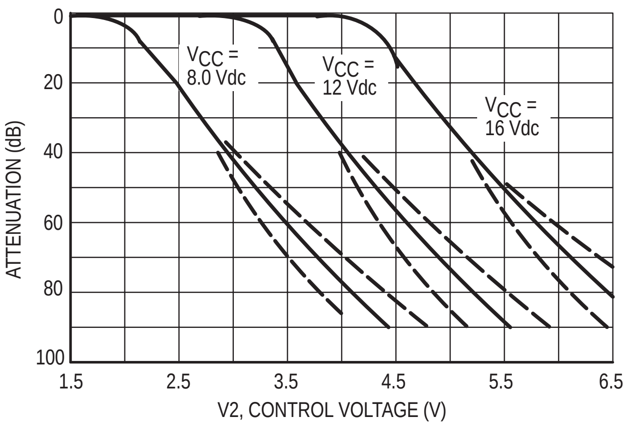


Figure 4. Attenuation versus Control Resistor

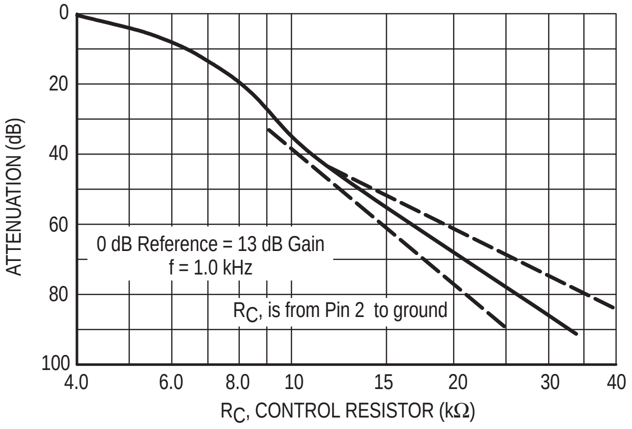


Figure 5. Frequency Response

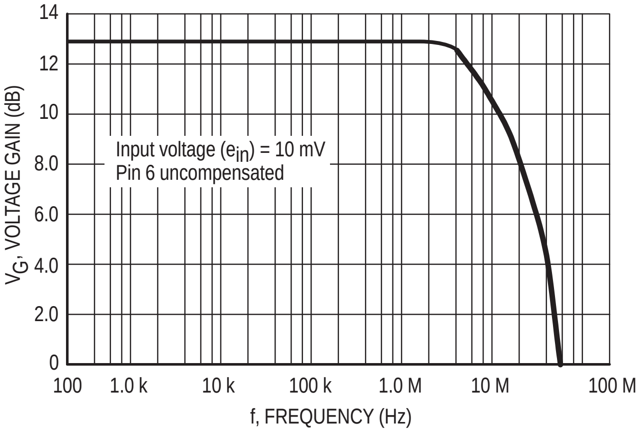


Figure 6. Output Voltage Swing

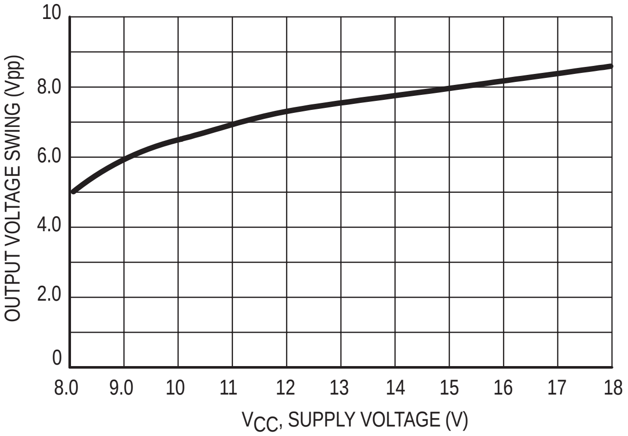
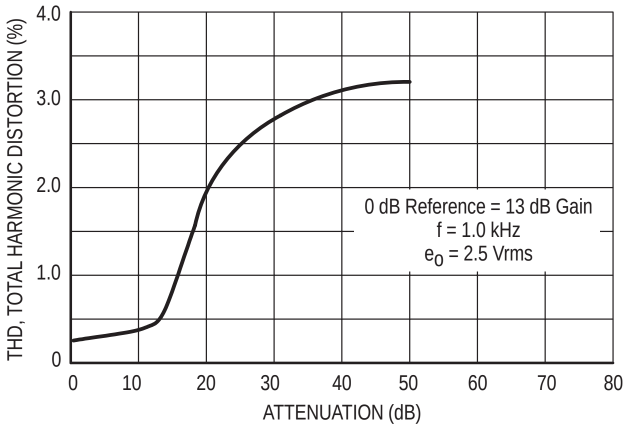


Figure 7. Total Harmonic Distortion



MOTOROLA

MC3346

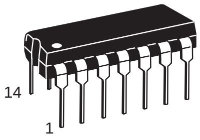
General Purpose Transistor Array One Differentially Connected Pair and Three Isolated Transistor Arrays

GENERAL PURPOSE TRANSISTOR ARRAY

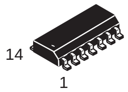
SEMICONDUCTOR TECHNICAL DATA

The MC3346 is designed for general purpose, low power applications for consumer and industrial designs.

- Guaranteed Base–Emitter Voltage Matching
- Operating Current Range Specified: 10 µA to 10 mA
- Five General Purpose Transistors in One Package



P SUFFIX
PLASTIC PACKAGE
CASE 646



D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO–14)

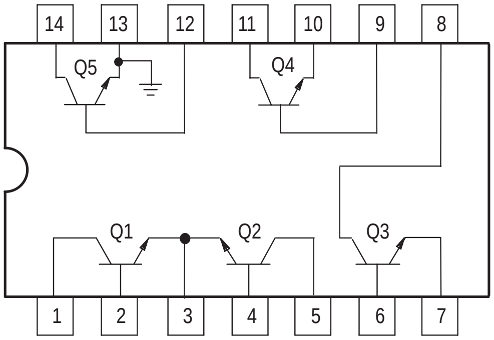
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	15	Vdc
Collector–Base Voltage	V_{CBO}	20	Vdc
Emitter–Base Voltage	V_{EB}	5.0	Vdc
Collector–Substrate Voltage	V_{CIO}	20	Vdc
Collector Current – Continuous	I_C	50	mAdc
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	1.2 10	W mW/°C
Operating Temperature Range	T_A	–40 to +85	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC3346D	T_A = –40° to +85°C	SO–14
MC3356P		Plastic DIP

PIN CONNECTIONS



Pin 13 is connected to substrate and must remain at the lowest circuit potential.

ELECTRICAL CHARACTERISTICS (T_A = +25°C, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
STATIC CHARACTERISTICS					
Collector–Base Breakdown Voltage (I_C = 10 μAdc)	$V_{(BR)CBO}$	20	60	–	Vdc
Collector–Emitter Breakdown Voltage (I_C = 1.0 mAdc)	$V_{(BR)CEO}$	15	–	–	Vdc
Collector–Substrate Breakdown Voltage (I_C = 10 μA)	$V_{(BR)CIO}$	20	60	–	Vdc
Emitter–Base Breakdown Voltage (I_E = 10 μAdc)	$V_{(BR)EBO}$	5.0	7.0	–	Vdc
Collector–Base Cutoff Current (V_{CB} = 10 Vdc, I_E = 0)	I_{CBO}	–	–	40	nAdc
DC Current Gain (I_C = 10 mAdc, V_{CE} = 3.0 Vdc) (I_C = 1.0 mAdc, V_{CE} = 3.0 Vdc) (I_C = 10 μAdc, V_{CE} = 3.0 Vdc)	h_{FE}	 – 40 –	 140 130 60	 – – –	–
Base–Emitter Voltage (V_{CE} = 3.0 Vdc, I_E = 1.0 mAdc) (V_{CE} = 3.0 Vdc, I_E = 10 mAdc)	V_{BE}	 – –	 0.72 0.8	 – –	Vdc
Input Offset Current for Matched Pair Q1 and Q2 (V_{CE} = 3.0 Vdc, I_C = 1.0 mAdc)	$\|I_{IO1} - I_{IO2}\|$	–	0.3	2.0	μAdc
Magnitude of Input Offset Voltage (V_{CE} = 3.0 Vdc, I_C = 1.0 mAdc)	–	–	0.5	5.0	mVdc
Temperature Coefficient of Base–Emitter Voltage (V_{CE} = 3.0 Vdc, I_C = 1.0 mAdc)	$\frac{\Delta V_{BE}}{\Delta T}$	–	–1.9	–	mV/°C
Temperature Coefficient	$\frac{\|\Delta V_{IO}\|}{\Delta T}$	–	1.0	–	μV/°C
Collector–Emitter Cutoff Current (V_{CE} = 10 Vdc, I_B = 0)	I_{CEO}	–	–	0.5	μAdc
DYNAMIC CHARACTERISTICS					
Low Frequency Noise Figure (V_{CE} = 3.0 Vdc, I_C = 100 μAdc, R_S = 1.0 kΩ, f = 1.0 kHz)	NF	–	3.25	–	dB
Forward Current Transfer Ratio (V_{CE} = 3.0 Vdc, I_C = 1.0 mAdc, f = 1.0 kHz)	h_{FE}	–	110	–	–
Short Circuit Input Impedance (V_{CE} = 3.0 Vdc, I_C = 1.0 mAdc)	h_{ie}	–	3.5	–	kΩ
Open Circuit Output Impedance (V_{CE} = 3.0 Vdc, I_C = 1.0 mAdc)	h_{oe}	–	15.6	–	μmhos
Reverse Voltage Transfer Ratio (V_{CE} = 3.0 Vdc, I_C = 1.0 mAdc)	h_{re}	–	1.8	–	$x10^{-4}$
Forward Transfer Admittance (V_{CE} = 3.0 Vdc, I_C = 1.0 mAdc, f = 1.0 MHz)	y_{fe}	–	31–j1.5	–	–
Input Admittance (V_{CE} = 3.0 Vdc, I_C = 1.0 mAdc, f = 1.0 MHz)	y_{ie}	–	0.3 + j0.04	–	–
Output Admittance (V_{CE} = 3.0 Vdc, I_C = 1.0 mAdc, f = 1.0 MHz)	y_{oe}	–	0.001 + j0.03	–	–
Current–Gain – Bandwidth Product (V_{CE} = 3.0 Vdc, I_C = 3.0 mAdc)	f_T	300	550	–	MHz
Emitter–Base Capacitance (V_{EB} = 3.0 Vdc, I_E = 0)	C_{eb}	–	0.6	–	pF
Collector–Base Capacitance (V_{CB} = 3.0 Vdc, I_C = 0)	C_{cb}	–	0.58	–	pF
Collector–Substrate Capacitance (V_{CS} = 3.0 Vdc, I_C = 0)	C_{CI}	–	2.8	–	pF

Figure 1. Collector Cutoff Current versus Temperature (Each Transistor)

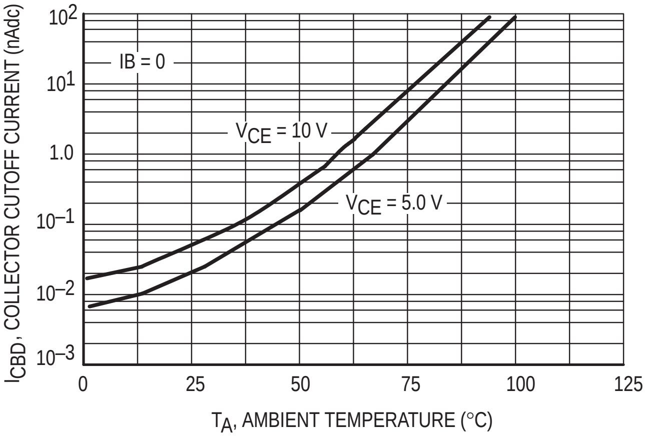


Figure 2. Collector Cutoff Current versus Temperature (Each Transistor)

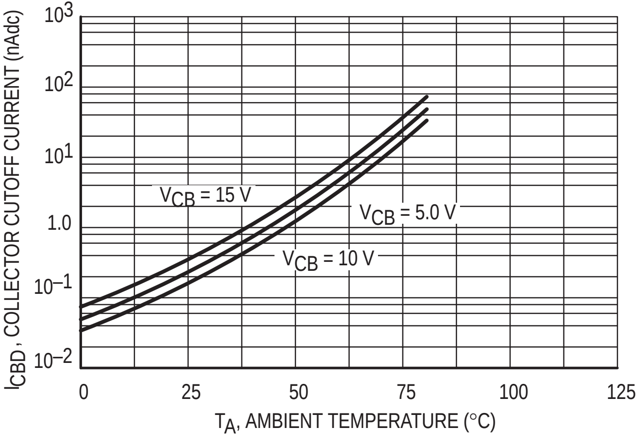


Figure 3. Input Offset Characteristics for Q1 and Q2

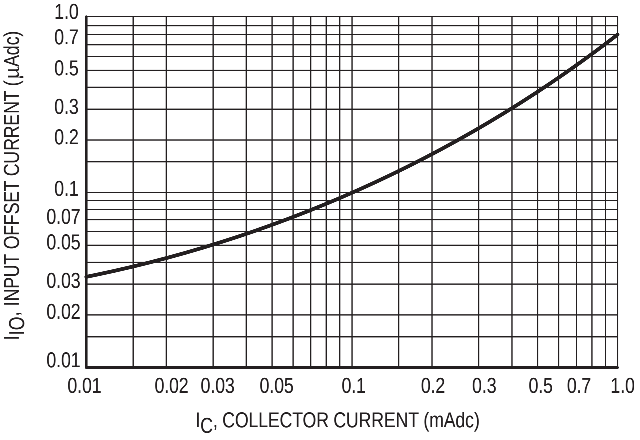


Figure 4. Base–Emitter and Input Offset Voltage Characteristics

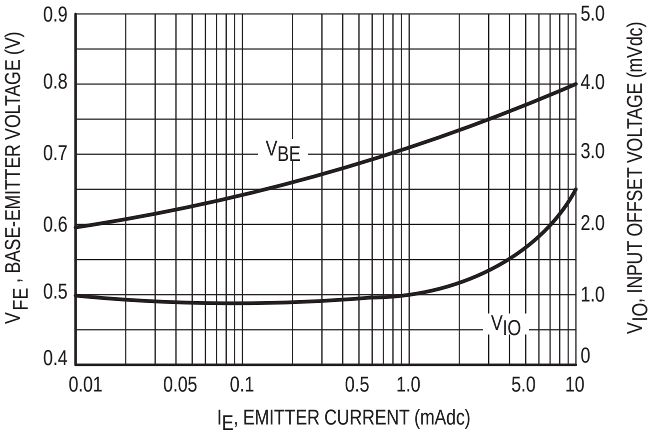
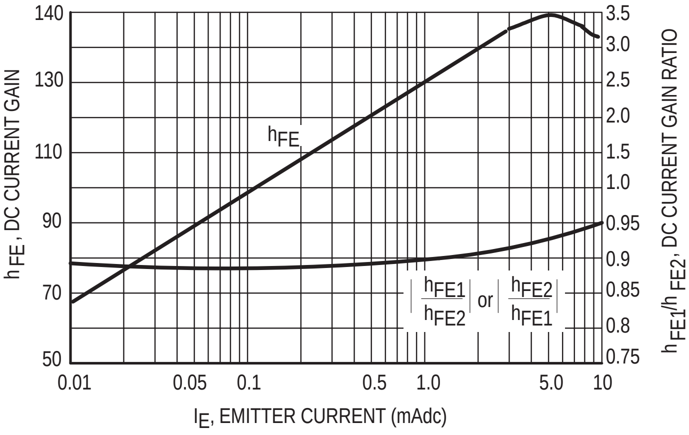


Figure 5. DC Current Gain



MC3373

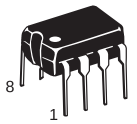
Remote Control Amplifier/Detector

The MC3373 is intended for application in infrared remote controls. It provides the high gain and pulse shaping needed to couple the signal from an IR receiver diode to the tuning control system logic.

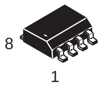
- High Gain Pre–Amp
- Envelope Detector for PCM Demodulation
- Simple Interface to Microcomputer Remote Control Decoder
- Use with Tuned Circuit for Narrow Bandwidth, Lower Noise Operation
- Minimum External Components
- Wide Operating Supply Voltage Range
- Low Current Drain
- Improved Retrofit for NEC Part No. µPC1373
- MC14497 Recommended IR Transmitter
- MLED81 Complementary Emitter
- MRD821 Complementary Detector Diode

REMOTE CONTROL WIDEBAND AMPLIFIER WITH DETECTOR

SEMICONDUCTOR TECHNICAL DATA

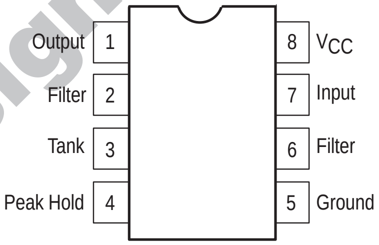


P SUFFIX
PLASTIC PACKAGE
CASE 626



D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

PIN CONNECTIONS



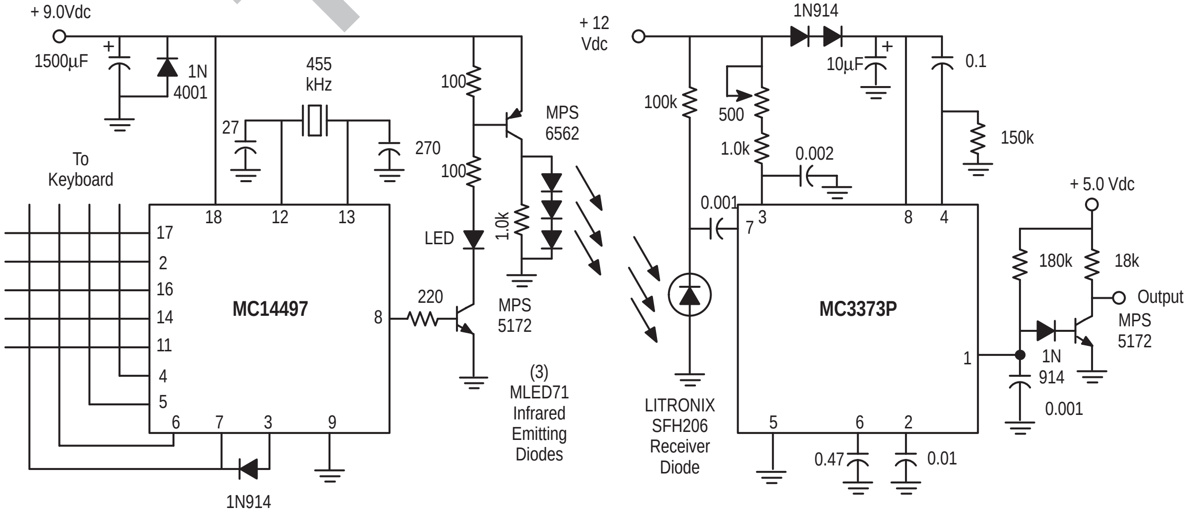
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	15	Vdc
Operating Temperature Range	T_A	0 to 75	°C
Storage Temperature Range	T_{stg}	–55 to +125	°C
Junction Temperature	T_J	150	°C
Power Dissipation, Package Rating Derate above 25°C	P_D $1/\theta_{JA}$	1.25 10	W mW/°C

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC3373P	T_A = 0 to +75°C	Plastic DIP
MC3373D		SO–8

Figure 1. Remote Control Application
40 kHz Carrier



RECOMMENDED OPERATING CONDITIONS

Characteristics	Symbol	Min	Typ	Max	Unit
Power Supply Voltage (25°C)	V_{CC}	4.75	–	15	Vdc
Power Supply Voltage (0°C)	V_{CC}	5.0	–	15	Vdc
Input Frequency	f_{in}	30	40	80	kHz

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0 V, f_{in} = 40 kHz, Test circuit of Figure 2)

Characteristics	Symbol	Min	Typ	Max	Unit
Power Supply Current	I_{CC}	1.5	2.5	3.5	mAdc
Input Terminal Voltage	V(Pin 7)	2.4	2.8	3.0	Vdc
Input Voltage Threshold	V_{in}	–	50	100	µVpp
Input Amplifier Voltage Gain (V[Pin 3] = 500 mVpp)	A_V	–	60	–	dB
Input Impedance	r_{in}	40	60	80	kΩ
Output Voltage, V_{in} = 1.0 mVpp	V_{OL}	–	–	0.5	V
Output Leakage, V_{CC} = V_{OH} = 15 Vdc	I_{OH}	–	–	2.0	µA
Output Voltage, Input Open	V_{OH}	–	–	5.0	Vdc

Figure 2. Test Circuit

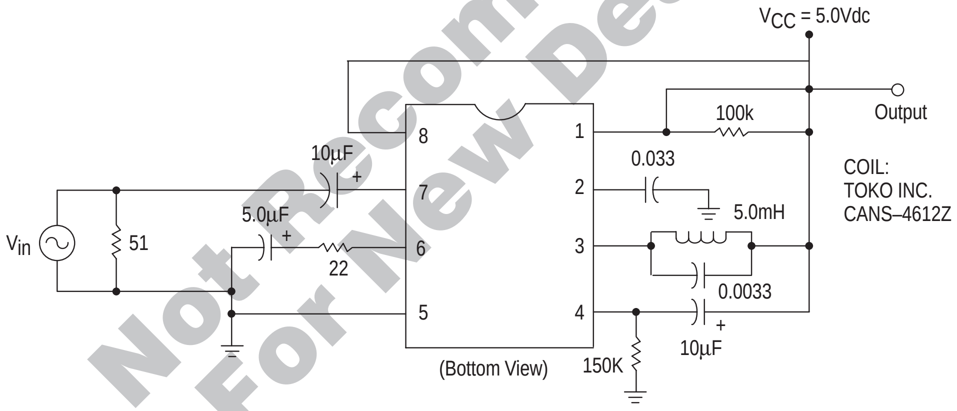


Figure 3. Representative Block Diagram

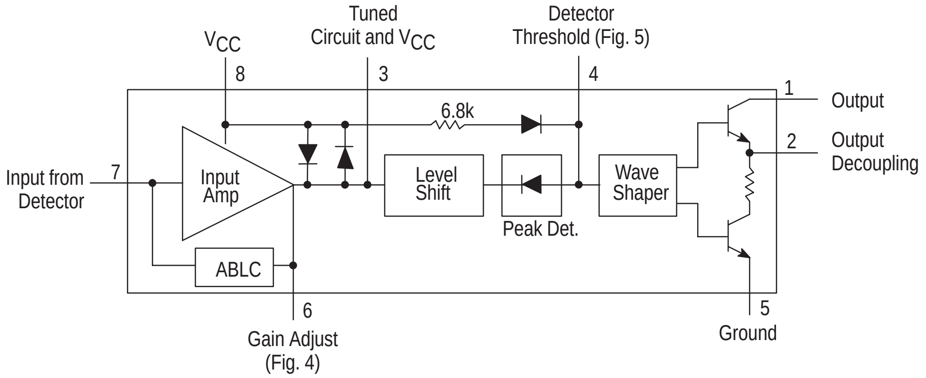


Figure 4. Input Amplifier Gain

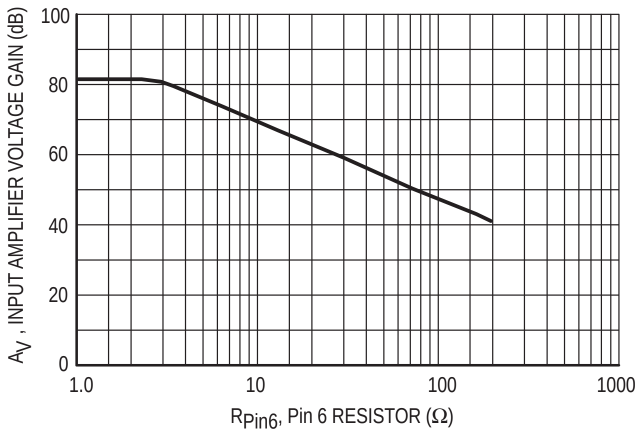
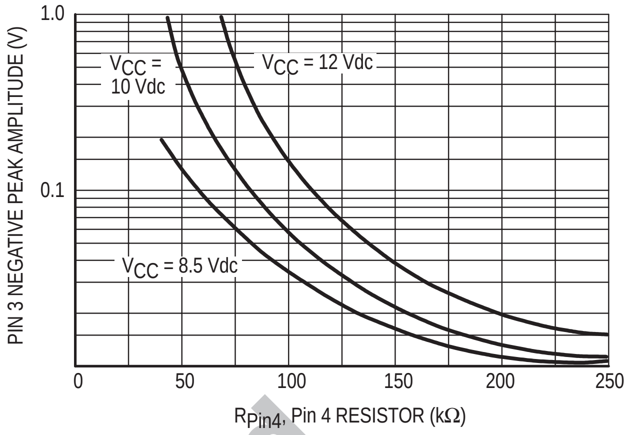


Figure 5. Detector Threshold

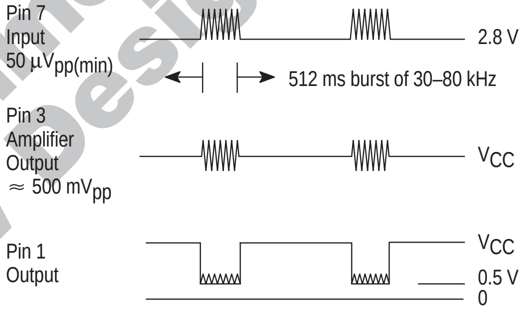


APPLICATIONS INFORMATION

The MC3373 is a specialized high gain amplifier/signal processor bipolar analog IC designed to be the core of infrared carrier signaling systems. The amplifier section has an Automatic Bias Level Control (ABLC) for simplified direct connection to an IR detector diode. Generally, it is operated ac coupled, utilizing an input high–pass filter to eliminate power line related noise, particularly that from florescent and gas vapor lamps. The use of a high frequency carrier is strongly recommended as opposed to simply detecting “dc” bursts of IR energy. In the carrier mode setup the MC3373 acts like an AM receiver subsystem, amplifying the incoming signal, demodulating it, and providing some basic wave shaping of the demodulated envelope. The tuned circuit at Pin 3 provides the main system selectivity reducing random noise interference and permitting multichannel operation in the same physical area without falsing. In the multichannel case the carriers must not be harmonically related. The bandwidth is determined primarily by the “Q” of the coil. Bandwidth may be increased by loading, shunting, the coil with a resistor.

Since this is a very high gain system operating at relatively high frequencies, care **must** be taken in the circuit layout and construction. Do not use wire wrap or non–ground plane protoboard. A simple single sided PCB with ground fill or a two–sided board with a solid groundplane and top side point–to–point will provide consistent high performance. There is a wide array of IR emitter/detectors available. The Motorola MLED81 and MRD821 are an excellent low cost combination to use with the MC3373. Multiple emitters are recommended for extended range.

Figure 6. Typical Signal Waveforms



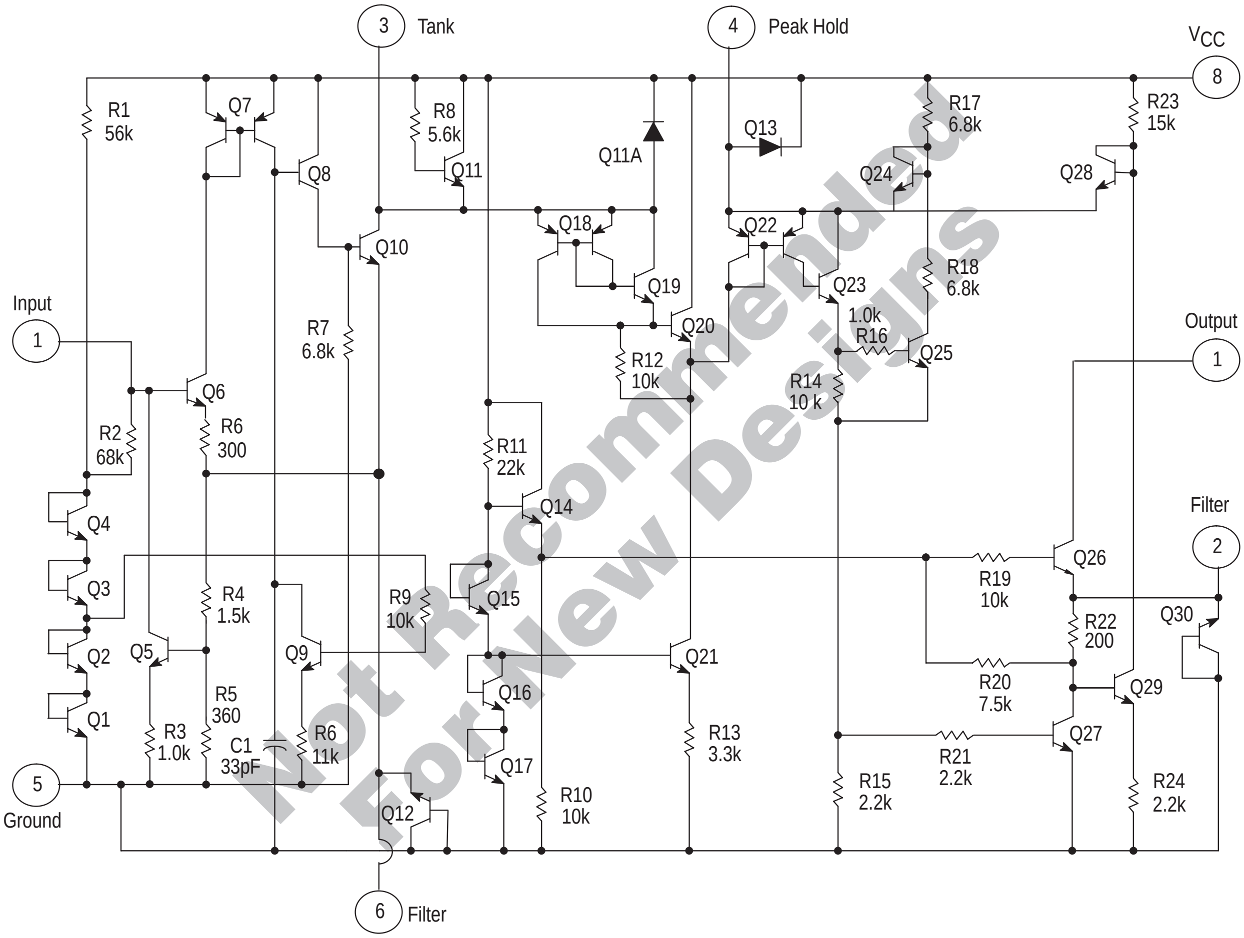
The input amplifier gain is approximately equal to the load impedance at Pin 3, divided by the resistor from Pin 6 to ground. Again, the low frequency gain can be reduced by using a small coupling capacitor in series with the Pin 6 resistor.

The load may be resistive, with only, or tuned, as in the test circuit. The amplifier output is limited by back–to–back clamping diodes, level shifted, buffered and fed to a negative peak detector. The detector threshold is set by the external resistor on Pin 4, and an internal 6.8 kΩ resistor and diode to V_{CC}. The capacitor from V_{CC} to Pin 4 quickly charges during the negative peaks and then settles toward the set–up voltage between signal bursts at a rate roughly determined by the value of the capacitor and the 6.8 k resistor. The external capacitor at Pin 2 filters the ultrasonic carrier from the pulses.

CIRCUIT DESCRIPTION

Q1 to Q4 set the bias on the amplifier input at approximately 2.8 V. Q6 to Q10 form the input amplifier, which has a gain of about 80 dB when R(Pin 6) = 0, Q5 sinks input current from the photo diode and keeps the amplifier properly biased. Q18 to Q20 level shift and buffer the signal to the negative peak detector, Q22 and Q23. Output devices Q26 and Q27 conduct during peaks and pull the output (Pin 1) low. The capacitor on Pin 2 filters out the carrier.

Figure 7. Representative Schematic Diagram



MC13020

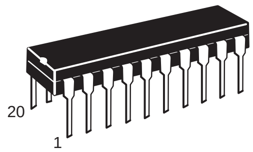
Motorola C-QUAM® AM Stereo Decoder

This circuit is a complete one ship, full feature AM stereo decoding and pilot detection system. It employs full–wave envelope signal detection at all times for the L + R signal, and decodes L – R signals only in the presence of valid stereo transmission.

- No Adjustments, No Coils
- Few Peripheral Components
- True Full–Wave Envelope Detection for L + R
- PLL Detection for L – R
- 25 Hz Pilot Presence Required to Receive L – R
- Pilot Acquisition Time 300 ms for Strong Signals, Time Extended for Noise Conditions to Prevent “Falsing”
- Internal Level Detector can be used as AGC Source

MOTOROLA C–QUAM® AM STEREO DECODER

SEMICONDUCTOR TECHNICAL DATA

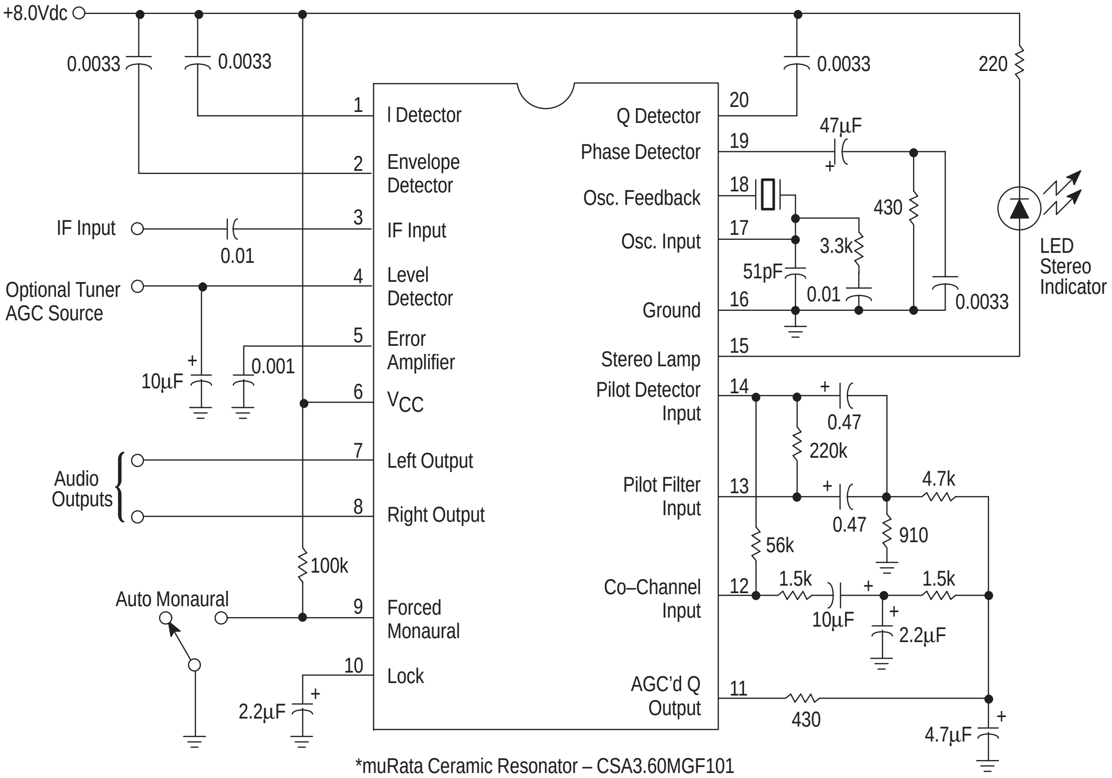


P SUFFIX
PLASTIC PACKAGE
CASE 738

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC13020P	T_A = – 40 to +85°C	Plastic DIP

Figure 1. Simplified Application



*muRata Ceramic Resonator – CSA3.60MGF101

The purchase of the Motorola C–QUAM® AM Stereo Decoder does not carry with such purchase any license by implication, estoppel or otherwise, under any patent rights of Motorola or others covering any combination of this decoder with other elements including use in a radio receiver. Upon application by an interested party, licenses are available from Motorola on its patents applicable to AM Stereo radio receivers.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	14	Vdc
Pilot Lamp Current, Pin 15		50	mAdc
Operating Temperature	T_A	–40 to +85	°C
Storage Temperature	T_{stg}	–65 to +150	°C
Junction Temperature	$T_{J(max)}$	150	°C
Power Dissipation Derate above 25°C	P_D	1.25 10	W mW/°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 8.0 Vdc, T_A = 25°C, Input Signal = 200 mVrms. Unmodulated carrier, circuit of Figure 1, unless otherwise noted.)

Characteristics		Min	Typ	Max	Unit
Supply Line Current Drain, Pin 6		20	30	40	mAdc
Input Signal Level, Unmodulated, Pin 3, for Full Operation		112	200	357	mVrms
Audio Output Level, 50% Modulation	L only or R only	160	220	280	mVrms
	Monaural	80	110	140	
Channel Balance, 50% Modulation, Monaural		–	–	±1.0	dB
Output THD, 50% Modulation	Monaural	–	–	0.5	%
	Stereo	–	–	1.0	
Output THD, 90% Modulation	Monaural	–	–	1.0	
Channel Separation, L only or R only, 50% Modulation		23	30	–	dB
Input Impedance	R_{in}	20	27	–	kΩ
	C_{in}	–	6.0	–	pF
Output Impedance		–	100	150	Ω
Pilot Acquisition Time					
VCO locked (after release of forced monaural)		–	280	300	ms
Bad Signal Condition		1.48	–	–	sec
Lock Detector Filter Voltage, Pin 10	In Lock	7.7	8.0	–	Vdc
	Out of Lock	–	0.8	1.0	
Force to Monaural, Pin 9					
Pull–Down for Monaural Mode		2.0	2.5	–	Vdc
		–	0.15	1.0	µA
Pull–Up for Automatic Mode		–	3.5	3.7	Vdc
		–	<0.001	1.0	µA

Figure 2. Basic Quadrature AM (QUAM)

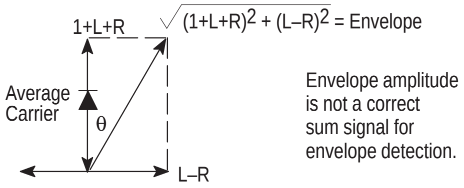


Figure 3. Motorola C–QUAM®

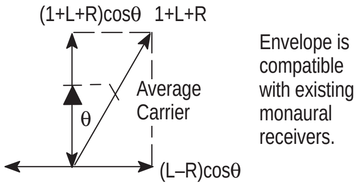
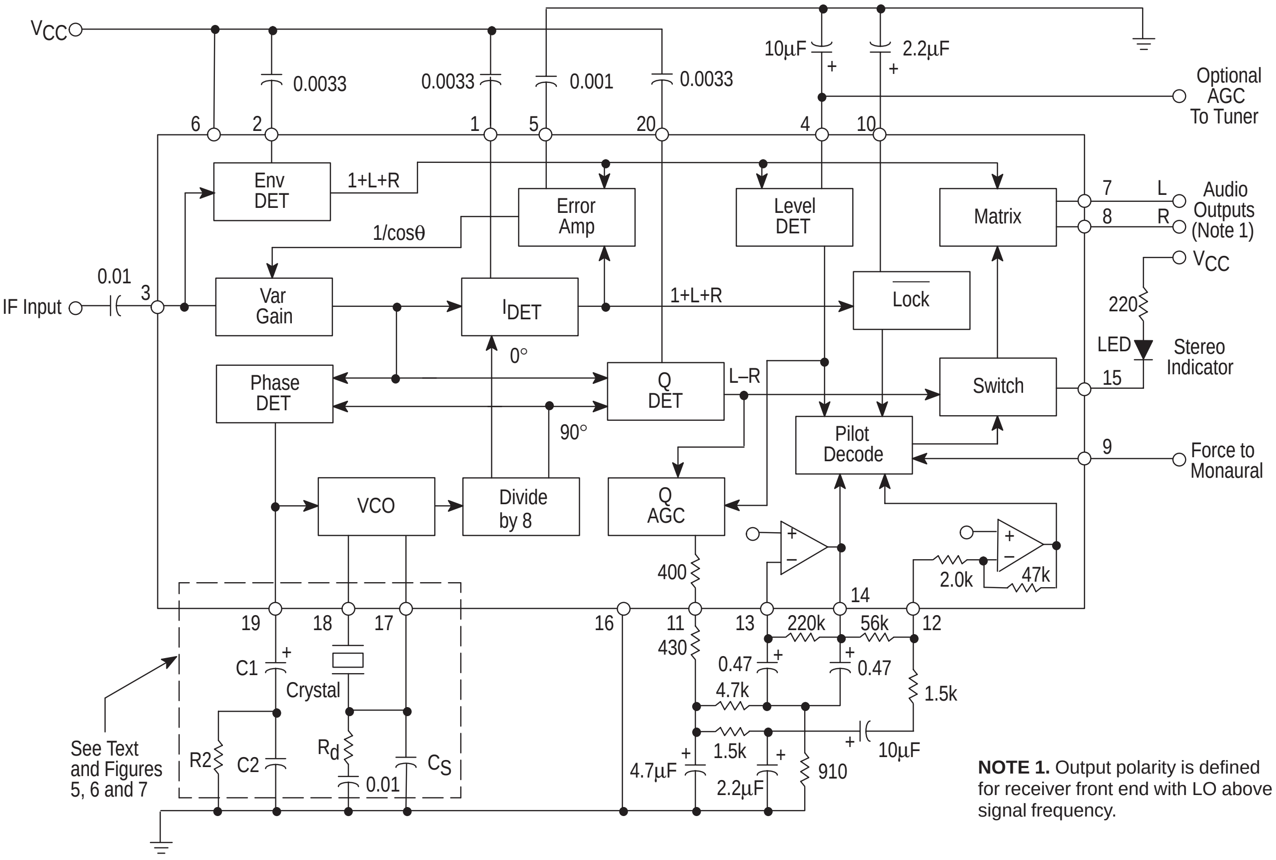


Figure 4. Representative Block Diagram



NOTE 1. Output polarity is defined for receiver front end with LO above signal frequency.

MOTOROLA C–QUAM® – COMPATIBLE QUADRATURE AM STEREO

Introduction

In C–QUAM®, conventional quadrature amplitude modulation has been modified by multiplying each axis by cosθ as shown in Figures 2 and 3. The resulting carrier envelope is 1 + L + R, i.e., a correct sum signal for monaural receivers and for stereo receivers operating in monaural mode. A 25 Hz pilot signal is added to the L – R information at a 4% modulation level.

Decoder

The MC13020P takes the output of the AM IF amplifier and performs the complete C–QUAM® decoding function. In the absence of a good stereo signal, it produces an undegraded monaural output. Note in Figure 4 that the L + R information delivered to the output always comes from the envelope detector (Env DET).

The MC13020P decodes the stereo information by first converting the C–QUAM® signal to QUAM, and then detecting QUAM. The conversion is accomplished by comparing the output of the Env DET and the I DET in the Err AMP. This provides 1/cosθ correction factor, which is then multiplied by the C–QUAM® incoming signal in the Var Gain block. Thus, the output of the Var Gain block is a QUAM signal, which can then be synchronously detected by conventional means. The I and Q detectors are held at 0° and 90° relative demodulation angles by reference signals from the phase–locked, divided–down VCO. The output of the I DET is 1 + L + R, with the added benefit (over the Env DET) of being able to produce a negative output on strong co–channel or noise interference. This is used to tell the Lock circuit to go to monaural operation. The output of the Q DET is the L – R and pilot information.

VCO

The VCO operates at 8 times the IF input frequency, which ensures that it is out–of–band, even when a 260 kHz IF frequency is used. Typically, a 450 kHz IF frequency is used with synthesized front ends. This places the VCO at 3.6 MHz, which permits economic crystal and ceramic resonators. A crystal VCO is very stable, but cannot be pulled very far to follow front–end mis–tuning. Pull–in capability of ±100 Hz at 450 kHz is typical, and de–Q–ing with a resistor (see Figure 7) can increase the range only slightly. Therefore, the crystal approach can only be used with very accurate, stable front–ends. By comparison, ceramic and L – C VCO circuits offer pull–in range in the order of ±2.5 kHz (at 450 kHz). Ceramic devices accurate enough to avoid trimming adjustment can be obtained with a matched capacitor for Cs (see Figure 1 and 5).

In the PLL filter circuit on Pin 19, C1 is the primary factor in setting a loop corner frequency of 8.0 to 10 Hz, in–lock. An internally controlled fast pull–in is provided. R2 is selected to slightly overdamp the control loop, and C2 prevents high frequency instability.

The Level DET block senses carrier level and provides an optional tuner AGC source. It also operates on the Q AGC block to provide a constant amplitude of 25 Hz pilot at Pin 11, and it delivers information to the pilot decoder regarding signal strength.

Pilot and Co–Channel Filters

The Q AGC output drives a low pass filter, made up of 400 Ω internal and 430 Ω and 5 μF external. From this point, an active 25 Hz band–pass filter is coupled to the Pilot Decoder, Pin 14, and another low–pass filter is connected to the Co–channel Input, Pin 12. A 2:1 reduction of 25 Hz pilot level to the Pilot Decode circuit will cause the system to go monaural, with the components shown. Refer to Figure 8 for the formulas governing the active band–pass filter. The co–channel input signal contains any low frequency intercarrier beat notes, and, at the selected level, prevents the Pilot Decode circuit from going into stereo. The co–channel input, Pin 12, gain can be adjusted by changing the external 1.5 k resistor. The values shown set the “trip” level at about 7% modulation. The 25 Hz pilot signal at the output of the active filter is opposite in phase to the pilot signal coming from the second low–pass filter. The 56 k resistor from Pin 14 to Pin 12 causes the pilot to be cancelled at the co–channel input. This allows a more sensitive setting of the co–channel trip level.

Pilot Decoder

The Pilot Decoder has two modes of operation. When signal conditions are good, the decoder will switch to stereo after 7 consecutive cycles of the 25 Hz pilot tone. When signal conditions are bad, the detected interference changes the pilot counter so as to require 37 consecutive cycles of pilot to go to stereo. In a frequency synthesized radio. the logic that mutes the audio when tuning can be connected to Pin 9. When this pin is held low it holds the decoder in monaural mode and switches it to the short count. This pin should be held low until the synthesizer and decoder have both locked onto a new station. A 300 ms delay should be sufficient. If the synthesizer logic does not provide sufficient delay, the circuit shown in Figure 9 may be added. Once Pin 9 goes high, the Pilot Decoder starts counting. If no pilot is detected for seven consecutive counts, it is assumed to be a good monaural station and the decoder is switched to the long count. This reduces the possibility of false stereo triggering due to signal level fluctuation or noise. If the PLL goes out of lock, or interference is detected by the co–channel protection circuit before seven cycles are counted, the decoder goes into the long count mode. Each disturbance will reset the counter to zero. The Level Detector will keep the decoder from going into stereo if the IF input level drops 10 dB, but will not change the operation of the pilot counter.

Once the decoder has gone into the stereo mode, it will go instantly back to monaural if either the lock detector on Pin 10 goes low, or if the carrier level drops below the present threshold. Seven consecutive counts of no pilot will also put the decoder in monaural. In stereo, the co–channel input is disabled, and co–channel or other noise is detected by negative excursions of the I DET, as mentioned earlier. When these excursions reach a level caused by approximately 20% modulation of co–channel, the lock detector puts the system in monaural, even though the PLL may still actually be locked. This higher level of co–channel tolerance provides the hysteresis to prevent chattering in and out of stereo on a marginal signal.

When all inputs to the Pilot Decode block are correct, and it has completed its count, it turns on the Switch, sending the L – R to the Matrix, and switches the pilot lamp pin to a low impedance to ground.

Summary

It should be noted that in C–QUAM®, with both channels AM modulated, the noise increase in stereo is a maximum of 3.0 dB, less on program material. Therefore, this is not the major concern in the choice of monaural to stereo switching point as it was in FM, and blend is not needed.

PIN FUNCTION DESCRIPTION

Pin	Description
1, 2	Detector Filters, R_{out} = 4.3 k, recommend 0.0033 μF to V_{CC} to filter 450 kHz components.
3	IF Signal Input
4	Level Detector filter pin, R_{out} = 8.2 k, 10 μF to ground sets the AGC time constant. High impedance output, needs buffer.
5	Error Amp compensation to stabilize the Var Gain feedback loop
6	V_{CC}, 6.0 to 10 Vdc, suitable for low V_{bat} automotive operation, but must be protected from “high line” condition.
7, 8	Left and Right Outputs, NPN emitter–followers
9	Forced Monaural, MOS or TTL controllable
10	Lock detector filter, R_{out} = 27 k, recommend 2.2 μF to ground
11	AGC’d Q output, NPN emitter–follower with 400 Ω from emitter to Pin 11
12	Co–channel input, 2.0 k series in and 47 k feedback
13	Pilot Filter input to op amp, see Figure 8.
14	Pilot Decode Input (op amp output) emitter–follower, R_{out} = 100 Ω
15	Stereo Lamp, open–collector of an NPN common emitter stage, can sink 50 mA, V_{sat} = 0.3 V at 5.0 mA.
16	Ground
17	Oscillator input, R_{in} = 10k, do not DC connect to Pin 18 or ground.
18	Oscillator feedback, NPN emitter, R_{out} = 100 Ω
19	Phase Detector output, current source to filter.
20	Detector Filter, R_{out} = 4.3 k, recommend 0.0033 μF to V_{CC} to filter 450 kHz.

Figure 5. Ceramic VCO

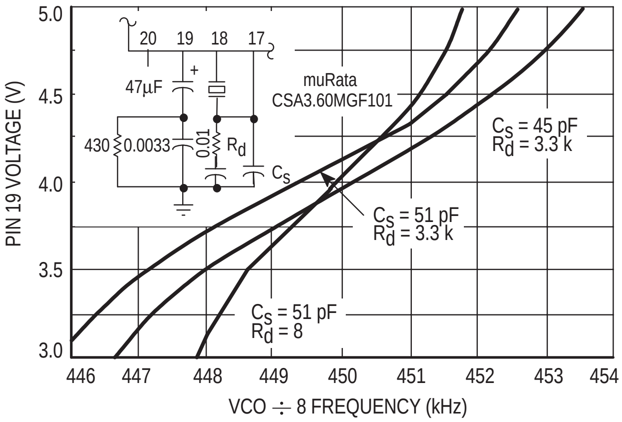


Figure 6. L–C VCO

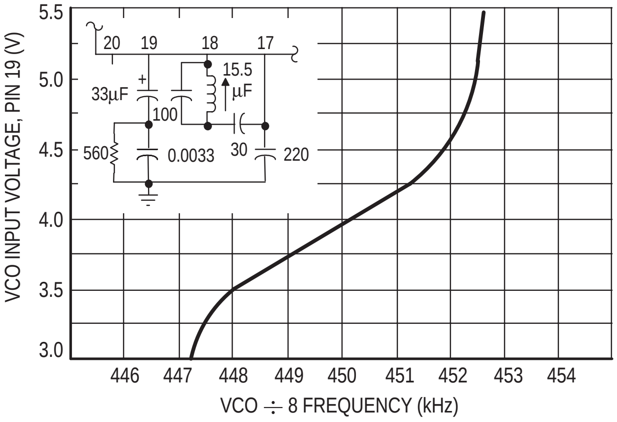


Figure 7. Crystal VCO

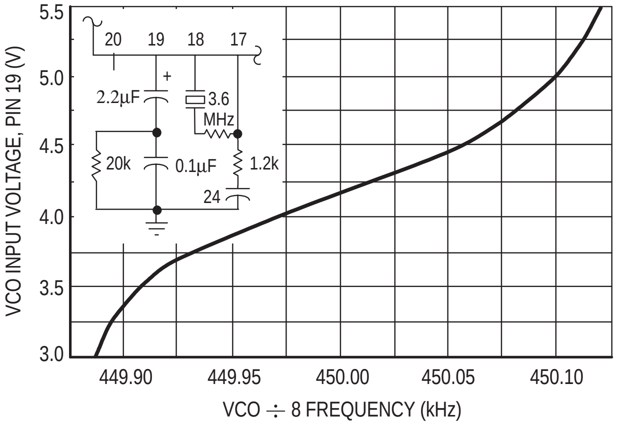


Figure 8. Forced Monaural Optional Delay Circuit

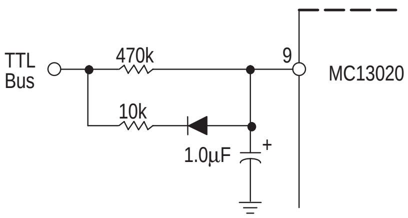
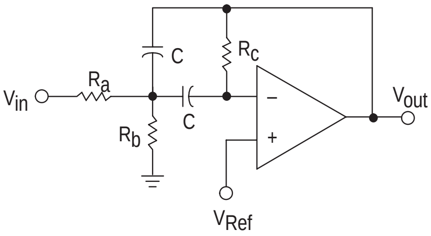


Figure 9. Active Bandpass Filter



$$R_c = \frac{Q}{\pi f_O C}$$

$$R_a = \frac{R_c}{2 A_o}$$

$$R_b = \frac{R_a R_c}{4Q^2 R_a - R_c}$$

C ± 5%	R_a ± 5%	R_b ± 1%	R_c ± 1%
0.47 µF	4.7 k	910	220 k
0.33 µF	8.2 k	1.3 k	330 k

NOTE: Capacitor C should be a good grade, low ESR.

Where in this application: f_O = center frequency = 25 Hz
A_o = gain at $f_O \le 25$
$Q \le 10$

Choose values for f_O, A_o, Q, and convenient C, solve for resistors.

MOTOROLA

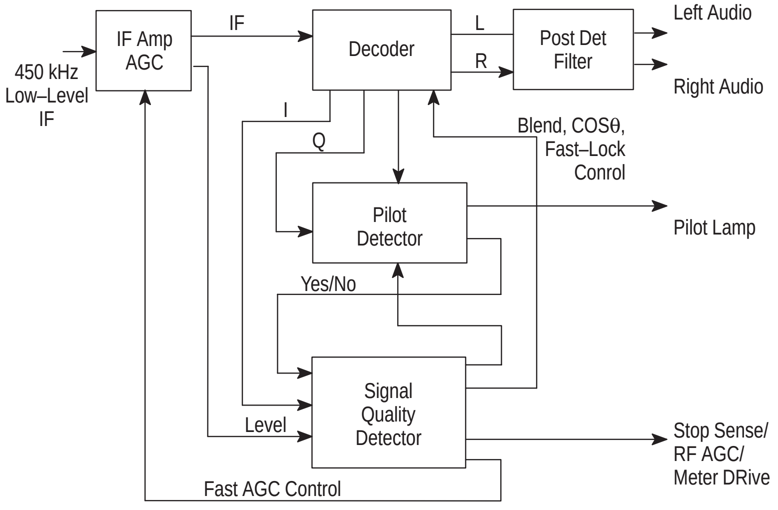
MC13022

Advanced Medium Voltage AM Stereo Decoder

The MC13022 is designed for home, portable and automotive AM stereo radio applications. The circuits and functions included in the design allow implementation of a full–featured C–QUAM® AM stereo radio with relatively few, inexpensive external parts. It is available in either 28–lead DIP or EIAJ compatible wide–bodied 28–lead SOIC.

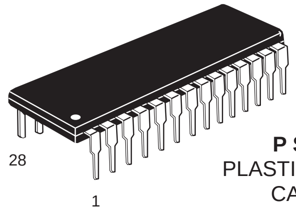
- Operation from 4.0 V to 10 V Supply with Current Drain of 18 mA Typ
- IF Amplifier with Two Speed AGC
- Post Detection Filters that Allow Manual or Automatic Adjustable Audio Bandwidth Control and 9.0 or 10 kHz Notch Filtering
- Signal Quality Controlled Stereo Blend and Noise Reduction
- Noise and Co–Channel Discriminating Stop–On–Station
- Signal Strength Indicator Output for RF AGC and/or Meter Drive
- Signal Strength Controlled IF and Audio Bandwidth
- Noise Immune Pilot Detector Needs no Precision Filter Components
- MC13023 Complementary Tuning System IC

Simplified Application

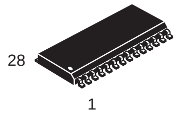


C–QUAM ADVANCED
MEDIUM VOLTAGE
AM STEREO DECODER

SEMICONDUCTOR
TECHNICAL DATA

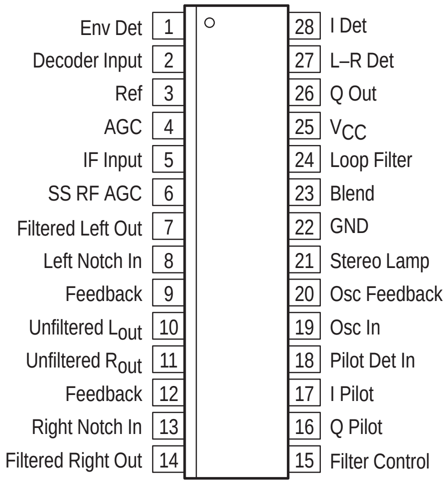


P SUFFIX
PLASTIC PACKAGE
CASE 710



DW SUFFIX
PLASTIC PACKAGE
CASE 751F
(SO–28L)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC13022P	T_A = – 40° to +85°C	Plastic Power
MC13022DW		SO–28L

MAXIMUM RATINGS

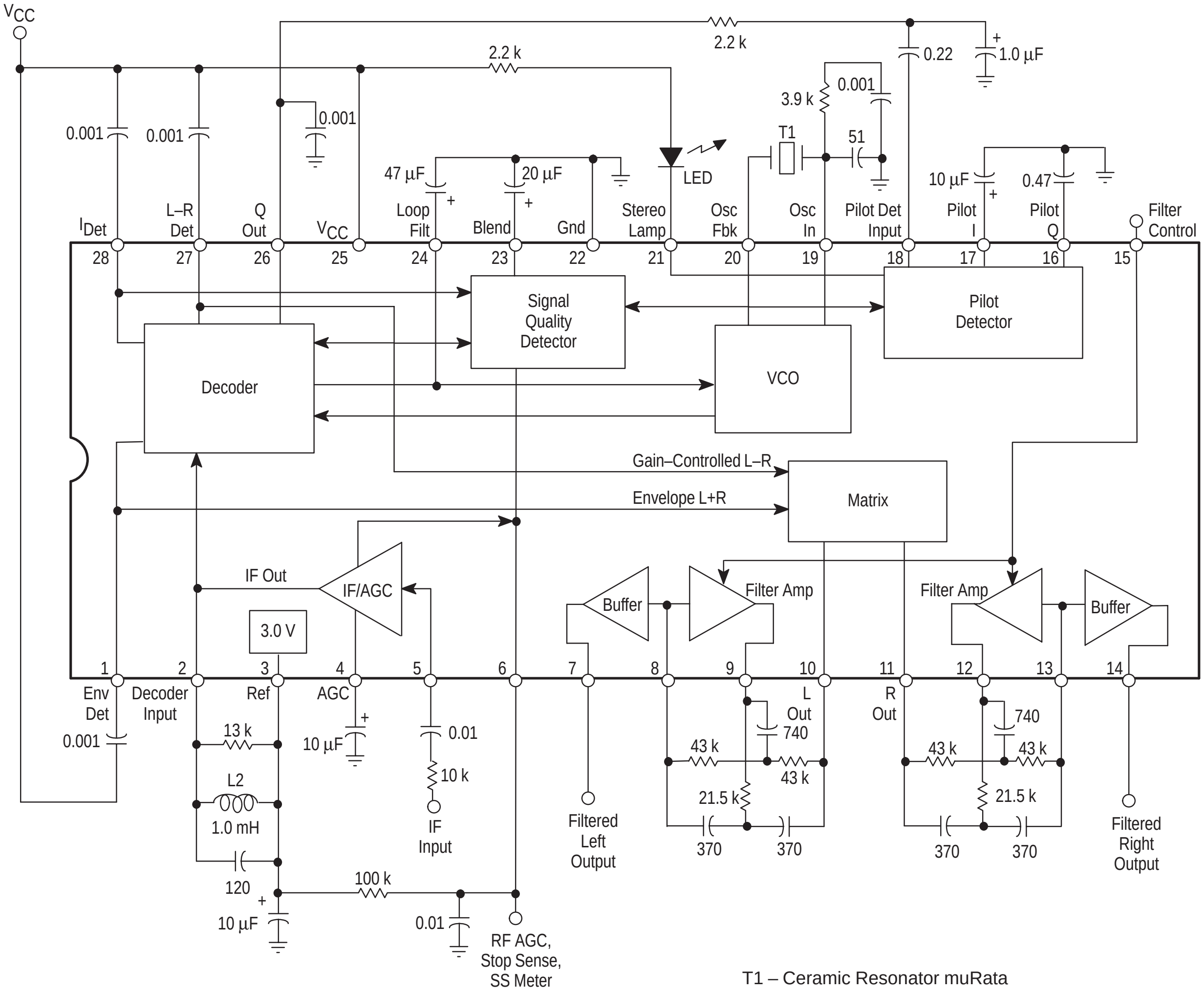
Rating	Symbol	Value	Unit
Power Supply Input Voltage	V_{CC}	12	Vdc
Stereo Indicator Lamp Current (Pin 21)	–	30	mAdc
Operating Ambient Temperature	T_A	–40 to +85	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Operating Junction Temperature	$T_{J(max)}$	150	°C
Power Dissipation Derate above 25°C	P_D	1.25 10	W mW/°C

NOTE: ESD data available upon request.

ELECTRICAL CHARACTERISTICS (V_{CC} = 8.0 V, T_A = 25°C, Test Circuit of Figure 1, unless otherwise noted.)

Characteristic	Min	Typ	Max	Unit
Power Supply Operating Range	4.0	8.0	10	Vdc
Supply Line Current Drain (Pin 25)	11	16	22	mAdc
Minimum Input Signal Level, Unmodulated for Full Operation (Pin 5)	–	5.0	–	mVrms
Audio Output Level, 50% Modulation, L only or R only (Pins 10, 11) Stereo	100	140	180	mVrms
Audio Output Level, 50% Modulation (Pins 10, 11) Monaural	50	70	90	mVrms
Output THD, 50% Modulation				%
Monaural	–	0.3	0.5	
Stereo	–	0.5	2.0	
Channel Separation, L only or R only, 50% Modulation Stereo	22	35	–	dB
Pilot Acquisition Time Following Blend Reset to 0.3 Vdc	–	–	600	ms
Audio Output Impedance at 1.0 kHz (Pins 7, 14)	–	300	–	Ω
Stereo Indicator Lamp Pin Saturation Voltage at 3.0 mA Load Current (V_{sat} Pin 21)	–	–	200	mVdc
Stereo Indicator Lamp Pin Leakage Current (Pin 21)	–	–	1.0	µAdc
Notch Filter Control (Pin 15), Response versus Voltage	(See Figure 2)			

Figure 1. Test Circuit



T1 – Ceramic Resonator muRata
CSA 3.60 MGF103
L2 – Miller 9230–92

EXPLANATION OF FEATURES

Blend and Noise Reduction

Although AM stereo does not have the extreme difference in S/N between mono and stereo that FM does (typically less than 3.0 dB versus greater than 20 dB for FM), sudden switching between mono and stereo is quite apparent. Some forms of interference such as co–channel have a large L–R component that makes them more annoying than would ordinarily be expected for the measured level. The MC13022 measures the interference level and reduces L–R as interference increases, blending smoothly to monaural. The pilot indicator remains on as long as a pilot signal is detected, even when interference is severe, to minimize annoying pilot light flickering.

RF AGC/Meter Drive

A dc voltage proportional to the log of signal strength is provided at Pin 6. This can be used for RF AGC, signal strength indication, and/or control of the post detection filter. Normal operation is above 2.2 V as shown is Figure 4.

Stop Sense

Multiplexed with the signal strength information is the stop sense signal. The stop sense is activated when scanning by externally pulling the blend capacitor on Pin 23 below 0.5 V. This would typically be done from the mute line in a frequency synthesizer.

If at any time Pin 23 is low and there is either no signal in the IF or a noisy signal of a predetermined interference level, Pin 6 will go low. This low can be used to tell the frequency synthesizer to immediately scan to the next channel. The interference detection prevents stopping on many unlistenable stations, a feature particularly useful at night when many frequencies may have strong signals from multiple co–channel stations.

IF Bandwidth Control

IF AGC attenuates the signal by shunting the signal at the IF input. This widens the IF bandwidth by decreasing the loaded Q of the input coupling coil as signal strength increases.

Post Detection Filtering

With weak, noisy signals, high frequency rolloff greatly improves the sound. Conventional tone controls do not attenuate the highs sufficiently to control noise without also significantly affecting the mid–range. Also, notch filters are necessary with any wide–band AM radio to eliminate the 10 kHz whistle from adjacent stations.

By using a twin–T filter with variable feedback to the normally grounded center leg, a variable Q notch filter is formed that provides both the 10 kHz notch and variable high frequency rolloff functions. Typical range of response is shown in Figure 3. Response is controlled by the dc voltage on Pin 15.

Pin 15 could interface with a dc operated tone control such as the TDA1524, or could be tied to Pin 6 for automatic audio bandwidth control as a function of signal strength.

Figure 2. High Performance Home Type AM Stereo Receiver

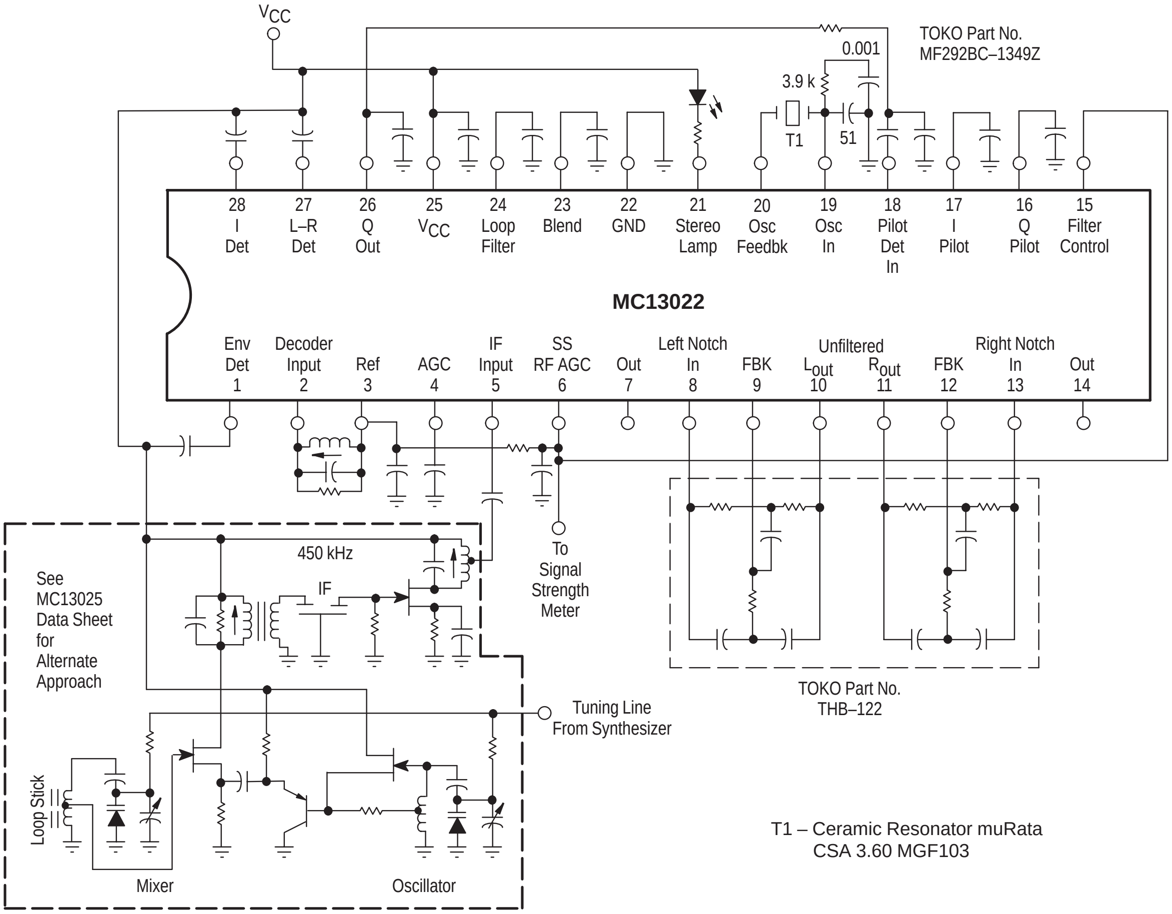


Figure 3. Overall Selectivity of a Typical Receiver versus Filter Control Voltage

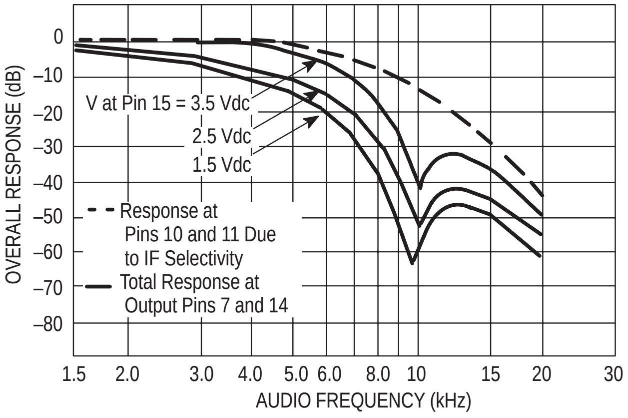
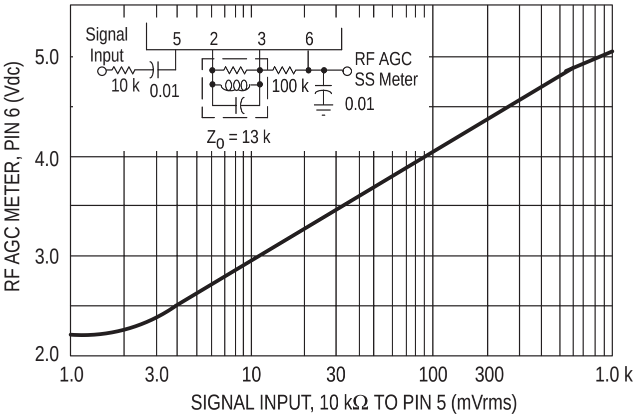


Figure 4. RF AGC/Signal Strength Output versus Input Signal



MC13022A

Advance Information

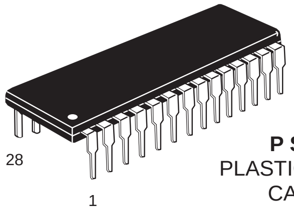
Advanced Medium Voltage AM Stereo Decoder

The MC13022A is designed for home and automotive AM stereo radio applications. The circuits and functions included in the design allow implementation of a full–featured C–QUAM® AM stereo radio with relatively few, inexpensive external parts. It is available in either 28–lead DIP or EIAJ compatible wide–bodied 28–lead SOIC. Functionally, the MC13022A and MC13022 are very similar. The MC13022A has 10 dB more audio output and a CMOS compatible logic level output (Pin 15) for stop sense. The stop sense/AGC function has been internally connected to the output notch filter control.

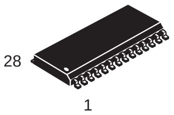
- Operation from 6.0 V to 10 V Supply with Current Drain of 20 mA Typ
- IF Amplifier with Two Speed AGC
- Post Detection Filters that Allow Automatic Adjustable Audio Bandwidth Control and Notch Filtering (9.0 or 10 kHz)
- Signal Quality Controlled Stereo Blend and Noise Reduction
- Noise and Co–Channel Discriminating Stop–On–Station
- Signal Strength Indicator Output for Stop Sense and/or Meter Drive
- Signal Strength Controlled IF and Audio Bandwidth
- Noise Immune Pilot Detector Needs no Precision Filter Components
- MC13025 Complementary Electronically Tuned Radio Front End
- CMOS Compatible Driver for Stop Sense

C–QUAM ADVANCED MEDIUM VOLTAGE AM STEREO DECODER

SEMICONDUCTOR TECHNICAL DATA

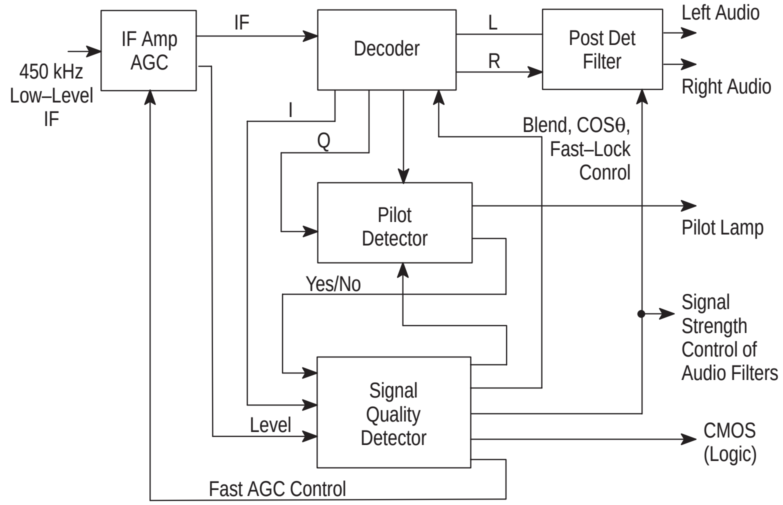


P SUFFIX
PLASTIC PACKAGE
CASE 710

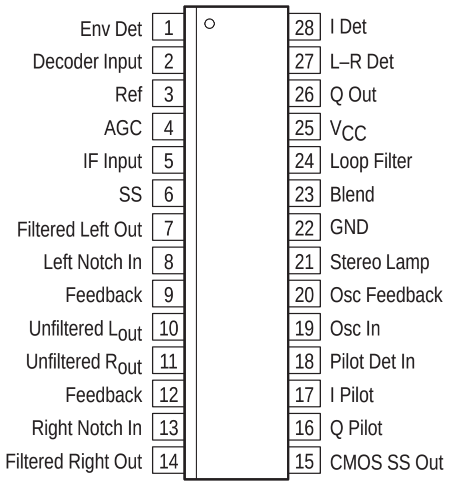


DW SUFFIX
PLASTIC PACKAGE
CASE 751F
(SO–28L)

Simplified Application



PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC13022AP	T_A = – 40° to +85°C	Plastic Power
MC13022ADW		SO–28L

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Input Voltage	V_{CC}	12	Vdc
Stereo Indicator Lamp Current (Pin 21)	–	30	mAdc
Operating Ambient Temperature	T_A	–40 to +85	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Operating Junction Temperature	$T_{J(max)}$	150	°C
Power Dissipation Derate above 25°C	P_D	1.25 10	W mW/°C

NOTE: ESD data available upon request.

ELECTRICAL CHARACTERISTICS (V_{CC} = 8.0 V, T_A = 25°C, Test Circuit of Figure 1, unless otherwise noted.)

Characteristic	Min	Typ	Max	Unit
Power Supply Operating Range	6.0	8.0	10	Vdc
Supply Line Current Drain (Pin 25)	10	20	25	mAdc
Minimum Input Signal Level, Unmodulated for Full Operation (Pin 5)	–	5.0	–	mVrms
Audio Output Level, 50% Modulation, L only or R only (Pins 10, 11) Stereo	290	400	530	mVrms
Audio Output Level, 50% Modulation (Pins 10, 11) Monaural	140	200	265	mVrms
Output THD, 50% Modulation				%
Monaural	–	0.3	0.8	
Stereo	–	0.5	1.6	
Channel Separation, L only or R only, 50% Modulation Stereo	22	35	–	dB
Pilot Acquisition Time Following Blend Reset to 0.3 Vdc	–	–	600	ms
Audio Output Impedance at 1.0 kHz (Pins 7, 14)	–	300	–	Ω
Stereo Indicator Lamp Pin Saturation Voltage at 3.0 mA Load Current (V_{sat} Pin 21)	–	–	200	mVdc
Stereo Indicator Lamp Pin Leakage Current (Pin 21)	–	–	1.0	µAdc
Oscillator Capture Range	–	±3.0	–	kHz

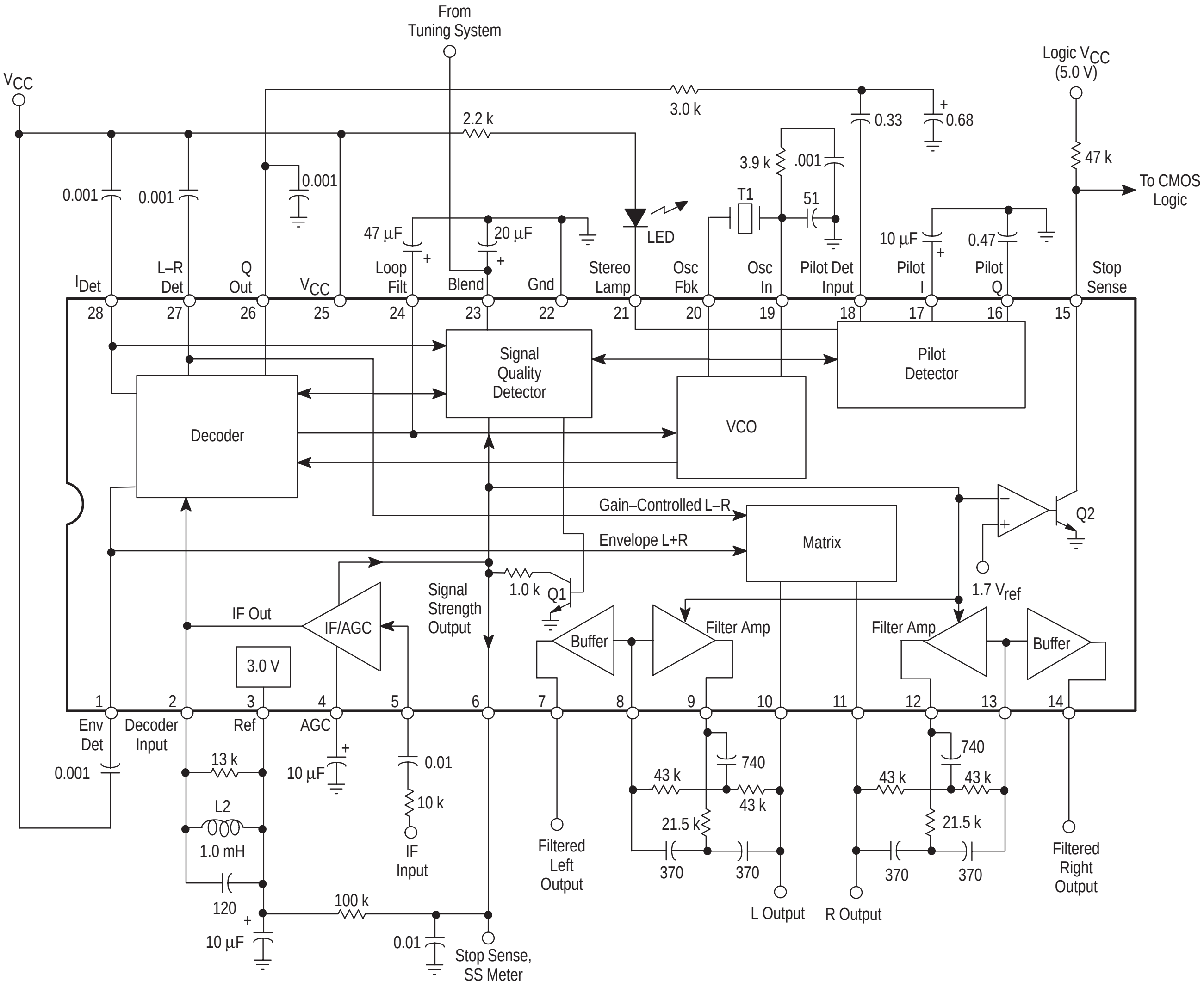


Figure 1. Test Circuit

T1 – Ceramic Resonator muRata
CSA 3.60 MGF103
L2 – Miller 9230–92

NOTES:
1. Q1 is switched on when the Blend Pin 23 is externally held low and the signal is weak or has 110% negative modulation. In this condition Q1 pulls Pin 6 low (0.25 to 1.3 V). At all other times, Pin 6 follows the curve in Figure 4.
2. Q2 (Pin 15) is switched on when Pin 6 voltage is below 1.7 V. Q2 could then be used as a logic output to the tuning system, telling the tuning system to continue searching for a good signal.
3. User is cautioned not to require more than 1.0 mA from Pin 6.

EXPLANATION OF FEATURES

Blend and Noise Reduction

Although AM stereo does not have the extreme difference in S/N between mono and stereo that FM does (typically less than 3.0 dB versus greater than 20 dB for FM), sudden switching between mono and stereo is quite apparent. Some forms of interference such as co–channel have a large L–R component that makes them more annoying than would ordinarily be expected for the measured level. The MC13022A measures the interference level and reduces L–R as interference increases, blending smoothly to monaural. The pilot indicator remains on as long as a pilot signal is detected, even when interference is severe, to minimize annoying pilot light flickering.

Signal Strength

A dc voltage proportional to the log of signal strength is provided at Pin 6. This can be used for signal strength indication, and it directly controls the post detection filter. Normal operation is above 2.2 V as shown is Figure 4.

Stop Sense

The signal strength information is multiplexed with the stop sense signal. The stop sense is activated when scanning by externally pulling the blend, Pin 23, below 0.3 V. This would typically be done from the mute line in a frequency synthesizer.

If at any time Pin 23 is low and there is either no signal in the IF or a noisy signal of a predetermined interference level, Pins 6 and 15 will go low. This low can be used to tell the frequency synthesizer to immediately scan to the next channel. The interference detection prevents stopping on many unlistenable stations, a feature particularly useful at night when many frequencies may have strong signals from multiple co–channel stations. Pin 6 drives a comparator which has a 1.7 V reference. Therefore the comparator output, Pin 15, is low if Pin 6 is <1.7 V and high if Pin 6 is >1.7 V.

IF Bandwidth Control

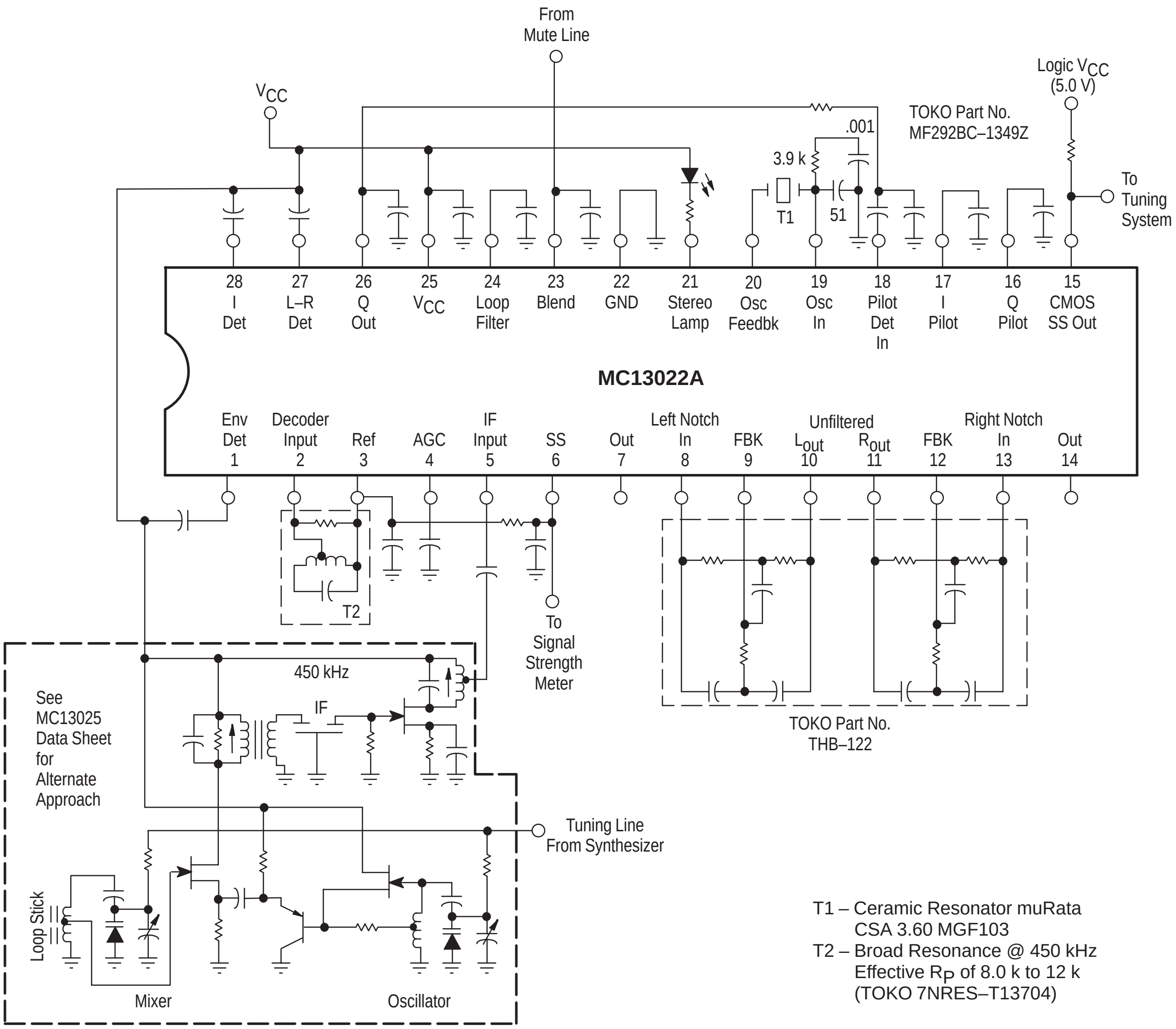
IF AGC attenuates the signal by shunting the signal at the IF input. This widens the IF bandwidth by decreasing the loaded Q of the input coupling coil as signal strength increases.

Post Detection Filtering

With weak, noisy signals, high frequency rolloff greatly improves the sound. Conventional tone controls do not attenuate the highs sufficiently to control noise without also significantly affecting the mid–range. Also, notch filters are necessary with any wide–band AM radio to eliminate the 10 kHz whistle from adjacent stations.

By using a twin–T filter with variable feedback to the normally grounded center leg, a variable Q notch filter is formed that provides both the 10 kHz notch and variable high frequency rolloff functions. Typical range of response is shown in Figure 3. Response is controlled by Pin 6 for automatic audio bandwidth control as a function of signal strength.

Figure 2. High Performance Home Type AM Stereo Receiver



T1 – Ceramic Resonator muRata
CSA 3.60 MGF103
T2 – Broad Resonance @ 450 kHz
Effective R_P of 8.0 k to 12 k
(TOKO 7NRES–T13704)

Figure 3. Overall Selectivity of a Typical Receiver versus Filter Control Voltage

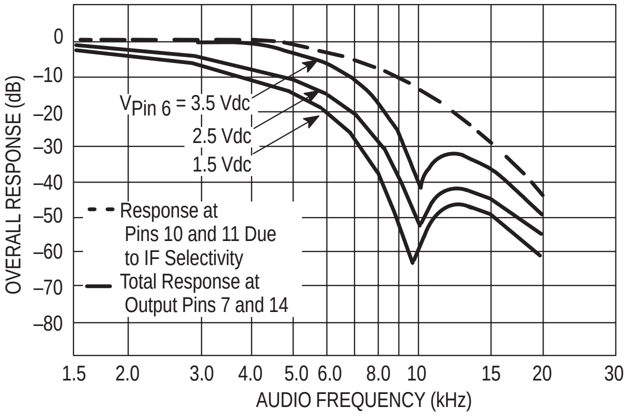
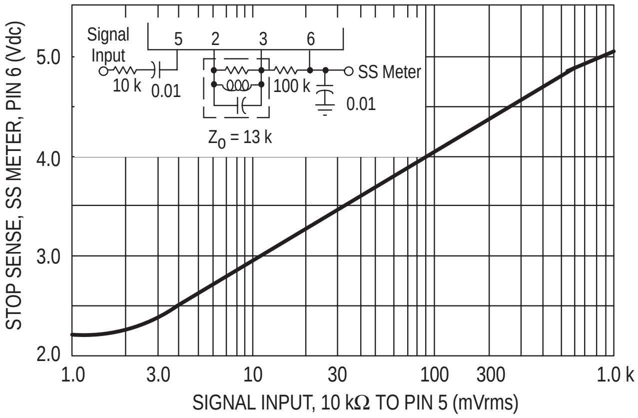


Figure 4. Strength Output versus Input Signal



MOTOROLA

MC13025

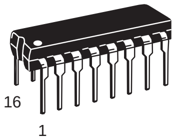
Electronically Tuned Radio Front End

ETR® FRONT END for C–QUAM® AM STEREO

SEMICONDUCTOR TECHNICAL DATA

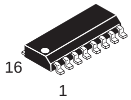
The MC13025 is the complementary ETR® Electronically Tuned Radio front–end for the second generation MC13022 C–QUAM® AM stereo IF and decoder. The MC13025 provides a high dynamic range mixer, voltage controlled oscillator, and first IF that with the MC13022 and synthesizer form a complete digitally controlled AM stereo tuner system. This system in turn may drive a dual channel audio processor and high power amplifiers for car radio or home stereo applications. Other applications include portable radio “boom boxes”, table radios and component stereo systems.

- Operates Over a Wide Range of Supply Voltages: 6.0 V_{CC} to 10 V_{CC}
- Wideband AGC Voltage to RF Amp for Extended Dynamic Range
- Buffered VCO Output to Frequency Synthesizer
- No External RF Amp Needed for Most Home Stereo and Portable Radios
- IF Drive Output Matches the MC13022 for Optimum Performance
- VCO Operates at Four Times Local Oscillator Injection Frequency



P SUFFIX
PLASTIC PACKAGE
CASE 648

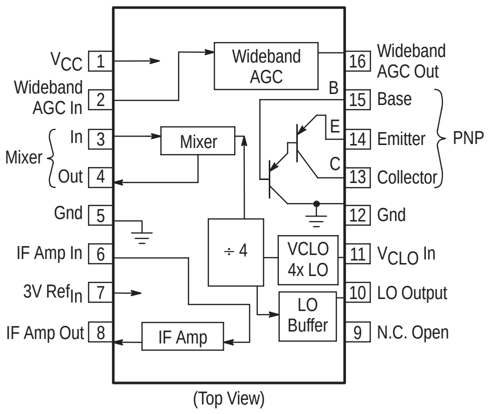
D SUFFIX
PLASTIC PACKAGE
CASE 751B
(SO–16)



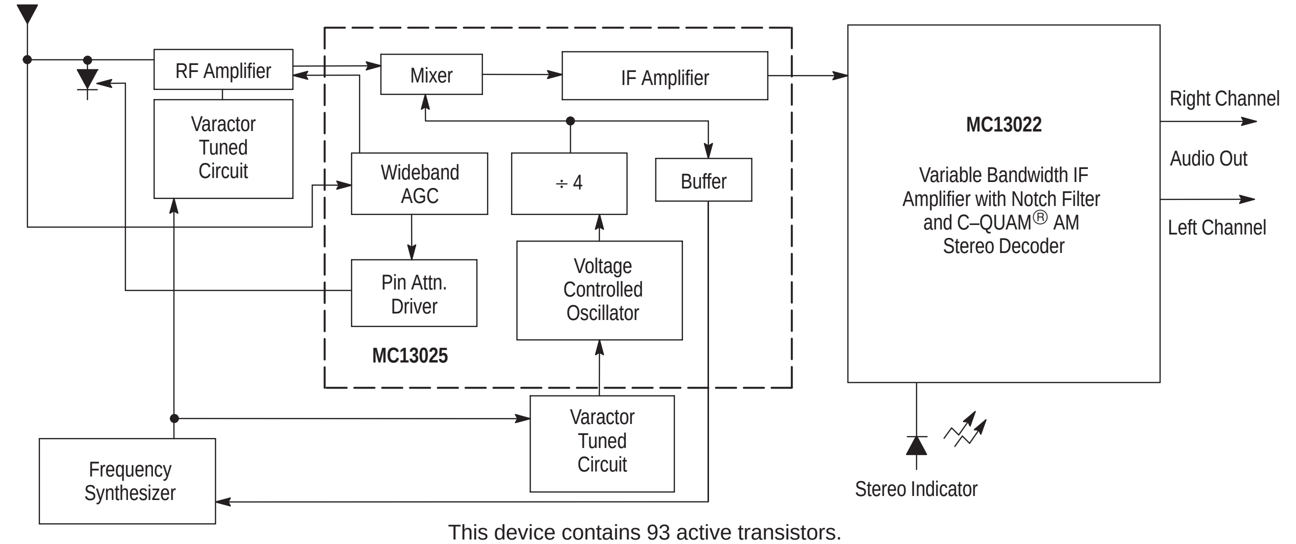
ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC13025D	$T_A = -40°$ to $+85°C$	SO–16
MC13025P		Plastic DIP

PIN CONNECTIONS



Simplified Block Diagram



This device contains 93 active transistors.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	12	Vdc
Ambient Operating Temperature	T_A	–40 to +85	°C
Storage Temperature	T_{stg}	–65 to +150	°C
Junction Temperature	T_J	150	°C
Power Dissipation Derate above 25°C	P_D	1.25 10	W mW/°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C, 8.0 V_{CC} test circuit as shown in Figure 2.)

Characteristics	Pin	Min	Typ	Max	Unit
Supply Current	1	7.0	8.2	10	mAdc
3.0 V Ref, Current In	7	–50	7.0	90	µAdc
IF Out DC Current	8	0.9	1.05	1.2	mAdc
Mixer DC Current Output	4	0.70	0.77	0.82	mAdc
IF Output Amplitude, RF Input @ 1.7 MHz, 31.6 mV	8	270	330	390	mVrms
Local Oscillator Output	10	160	181	220	mVrms
Wideband AGC Pull–Down Current	16	0.5	1.0	1.5	mAdc
PNP Darlington (DC Beta @ 5.0 mA I_E)		1000	2500	–	
PNP Darlington Collector Leakage (V_E = V_B = 8.0 V)	13	–0.13	–0.06	–	µAdc

Figure 1. Test Circuit

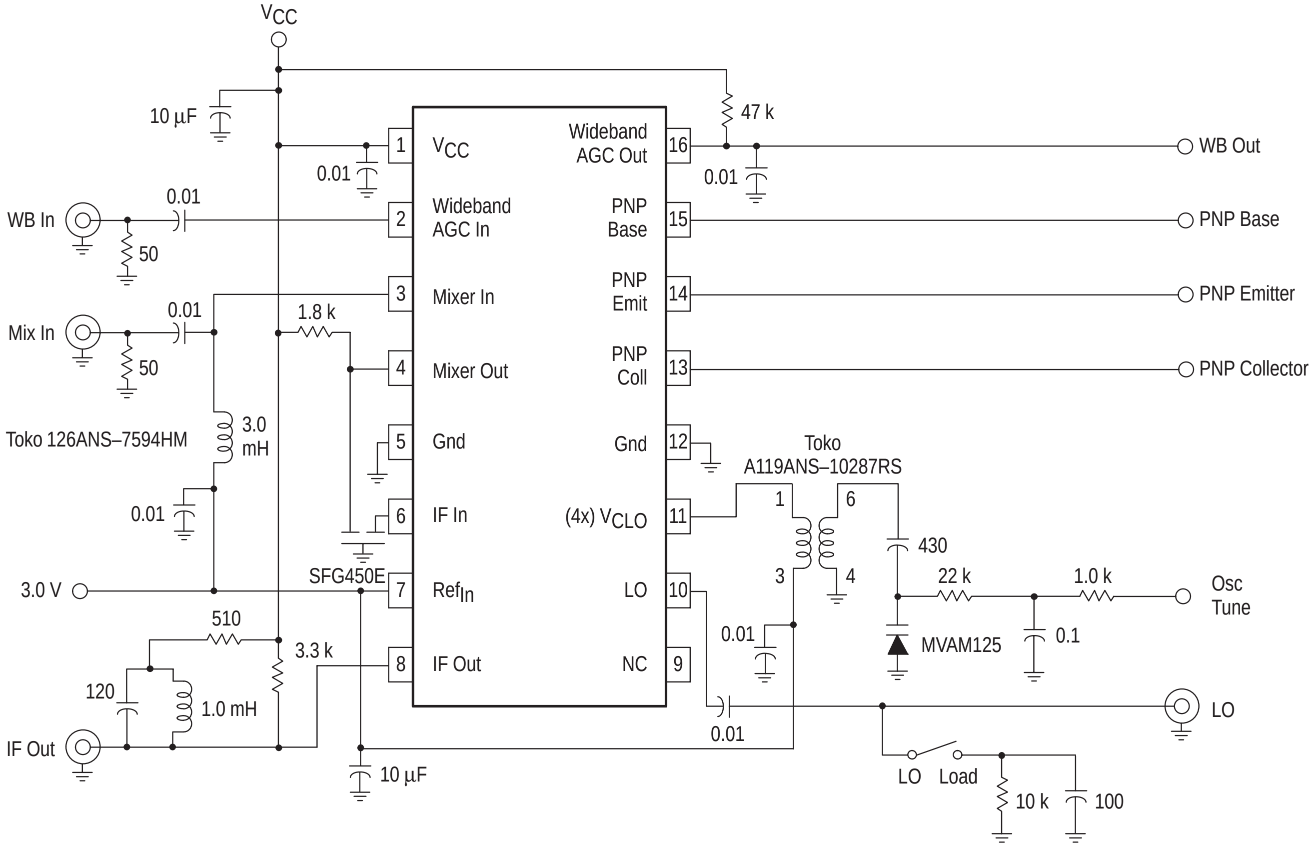
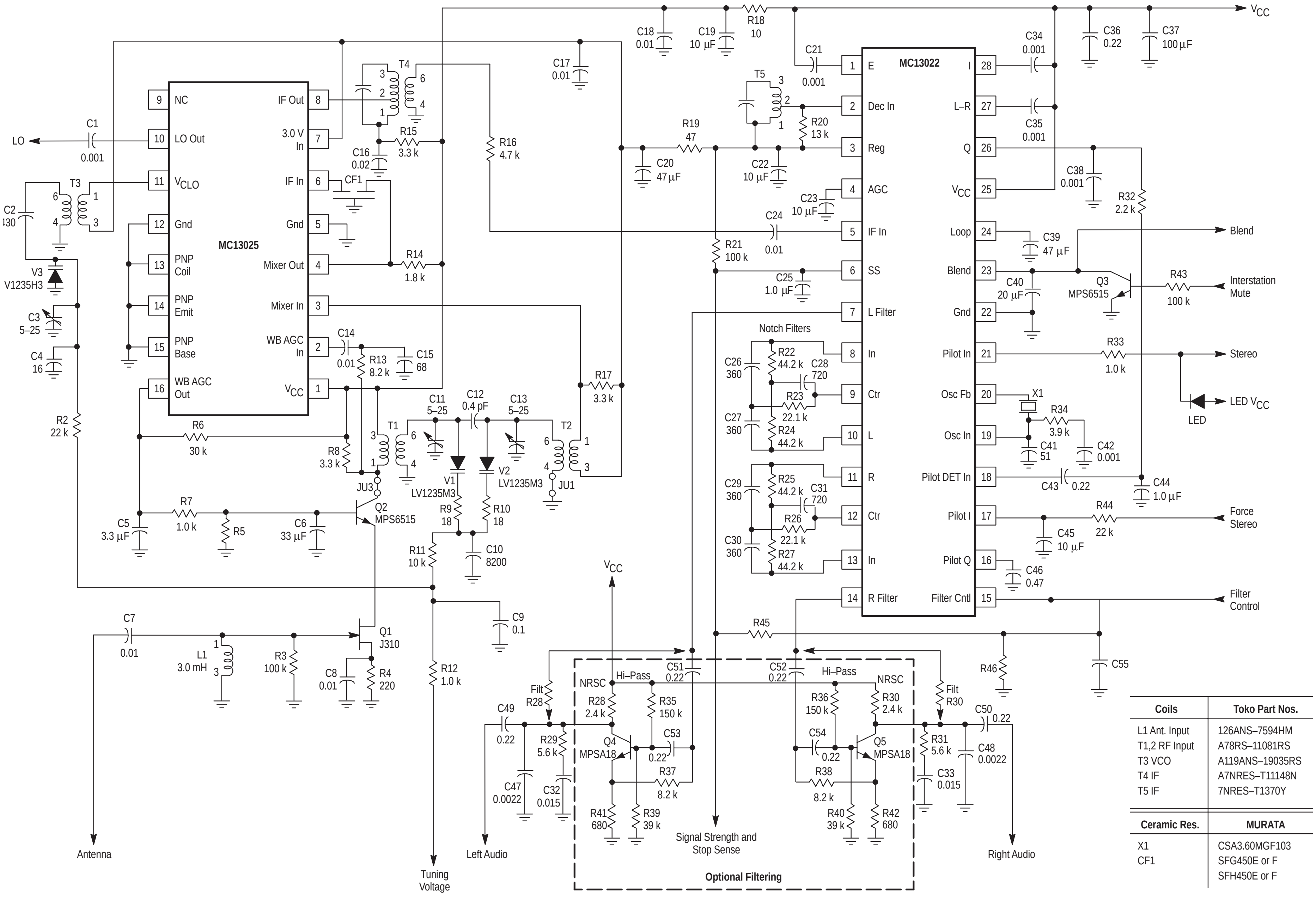


Figure 2. Cascode RF ETR Application

(NRSC – Notch Filters – Optional Pilot High Pass)



Coils	Toko Part Nos.
L1 Ant. Input	126ANS–7594HM
T1,2 RF Input	A78RS–11081RS
T3 VCO	A119ANS–19035RS
T4 IF	A7NRES–T11148N
T5 IF	7NRES–T1370Y

Ceramic Res.	MURATA
X1	CSA3.60MGF103
CF1	SFG450E or F SFH450E or F

MOTOROLA

MC13027
MC13122

Product Preview

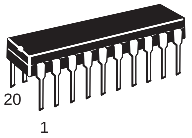
AMAX Stereo Chipset

AMAX STEREO IC CHIPSET

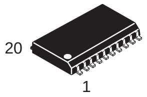
The MC13027 and MC13122 have been specifically designed for AM radio which can meet the EIA/NAB AMAX requirements. They are essentially the same as the MC13022A and MC13025 with the addition of noise blanking circuitry. The noise blanker consists of a wide band amplifier with an RF switch for blanking ahead the IF amplifier and a stereo audio blanker with adjustable delay and blanking times.

- Operating Voltage Range of 6.0 V to 10 V
- RF Blanker with Built–In Wide Band AGC Amplifier
- Audio Noise Blanker with Audio Track and Hold
- Mixer Third Order Intercept of 8.0 dBm (115 dBμV)
- Wide Band AGC Detector for RF Amplifier
- Local Oscillator VCO Divide–by–4 for Better Phase Noise
- Buffered Local Oscillator Output at the Fundamental Frequency
- Fast Stereo Decoder Lock
- Soft Stereo Blend
- Signal Quality Detector to Control Variable Q–Notch Filters for Adaptive Audio Bandwidth and Whistle Reduction
- Signal Quality Detector for AM Stereo
- Very Low Distortion Envelope and Synchronous Detectors
- Variable Bandwidth IF

MC13027

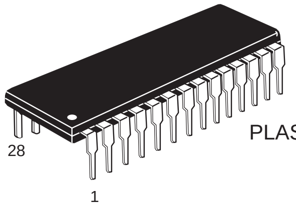


P SUFFIX
PLASTIC PACKAGE
CASE 738

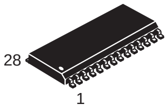


DW SUFFIX
PLASTIC PACKAGE
CASE 751D
(SO–20L)

MC13122



P SUFFIX
PLASTIC PACKAGE
CASE 710

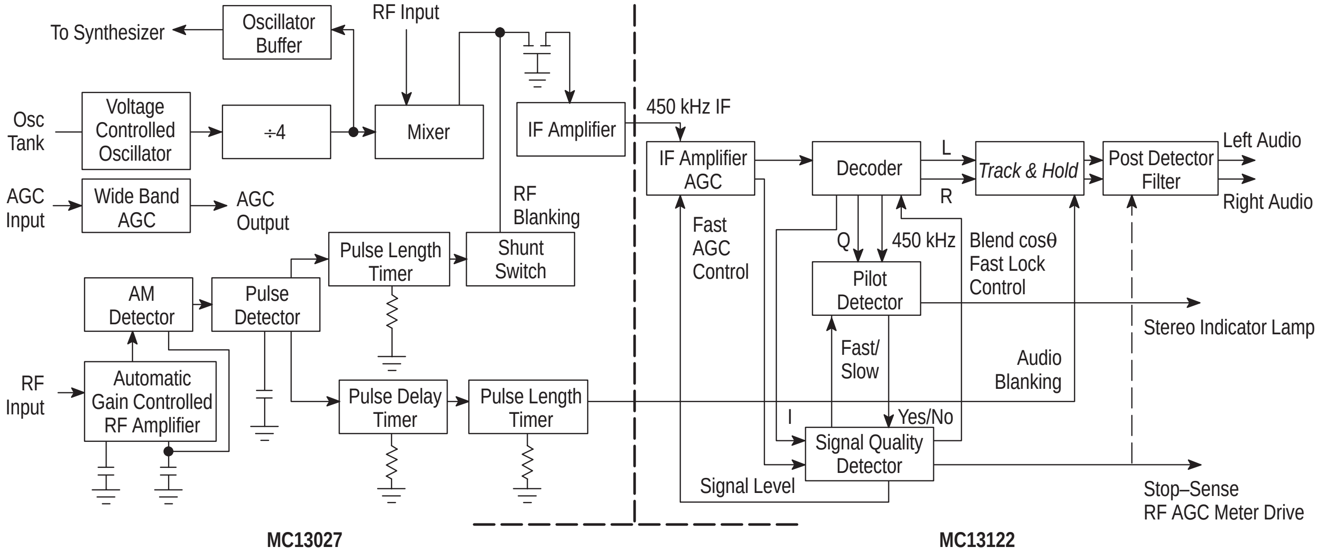


DW SUFFIX
PLASTIC PACKAGE
CASE 751F
(SO–28L)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC13027DW	T_A = –40 ° to +85°C	SO–20L
MC13027P		Plastic DIP
MC13122DW		SO–28L
MC13122P		Plastic DIP

Functional Block Diagram



This device contains 428 active transistors.

This device contains 670 active transistors.

MC13027
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Input Voltage	V_{CC}	12	Vdc
Ambient Operating Temperature	T_A	–40 to +85	°C
Storage Temperature Range	T_{stg}	–60 to +150	°C
Operating Junction Temperature	T_J	150	°C

NOTE: ESD data available upon request.

MC13027
ELECTRICAL CHARACTERISTICS (T$_A$ = 25°C, 8.0 V$_{CC}$ Test Circuit as shown in Figure 1.)

Characteristic	Min	Typ	Max	Unit
Supply Voltage Range (Pin 8)	–	6.0 to 10	–	V
Wideband (WB) AGC Threshold	–	1.0	–	mVrms
IF Output DC Current	–	1.0	–	mAdc
Mixer DC Current Output	–	0.83	–	mAdc
Local Oscillator Output	–	600	–	mVpp
Wideband AGC Pull–Down Current (Pin 20)	–	1.0	–	mAdc
Power Supply Current	–	16	–	mAdc
Mixer 3rd Order Intercept Point (Pin 6)	–	8.0	–	dBm
Mixer Conversion Gain	–	2.9	–	mS
IF Amplifier Input Impedance (Pin 14)	–	2.2	–	kΩ
IF Amplifier Transconductance	–	2.8	–	mS
IF Amplifier Load Resistance (Pin 16)	–	5.7	–	kΩ
IF Amplifier Collector Current (Pin 16)	–	990	–	µA

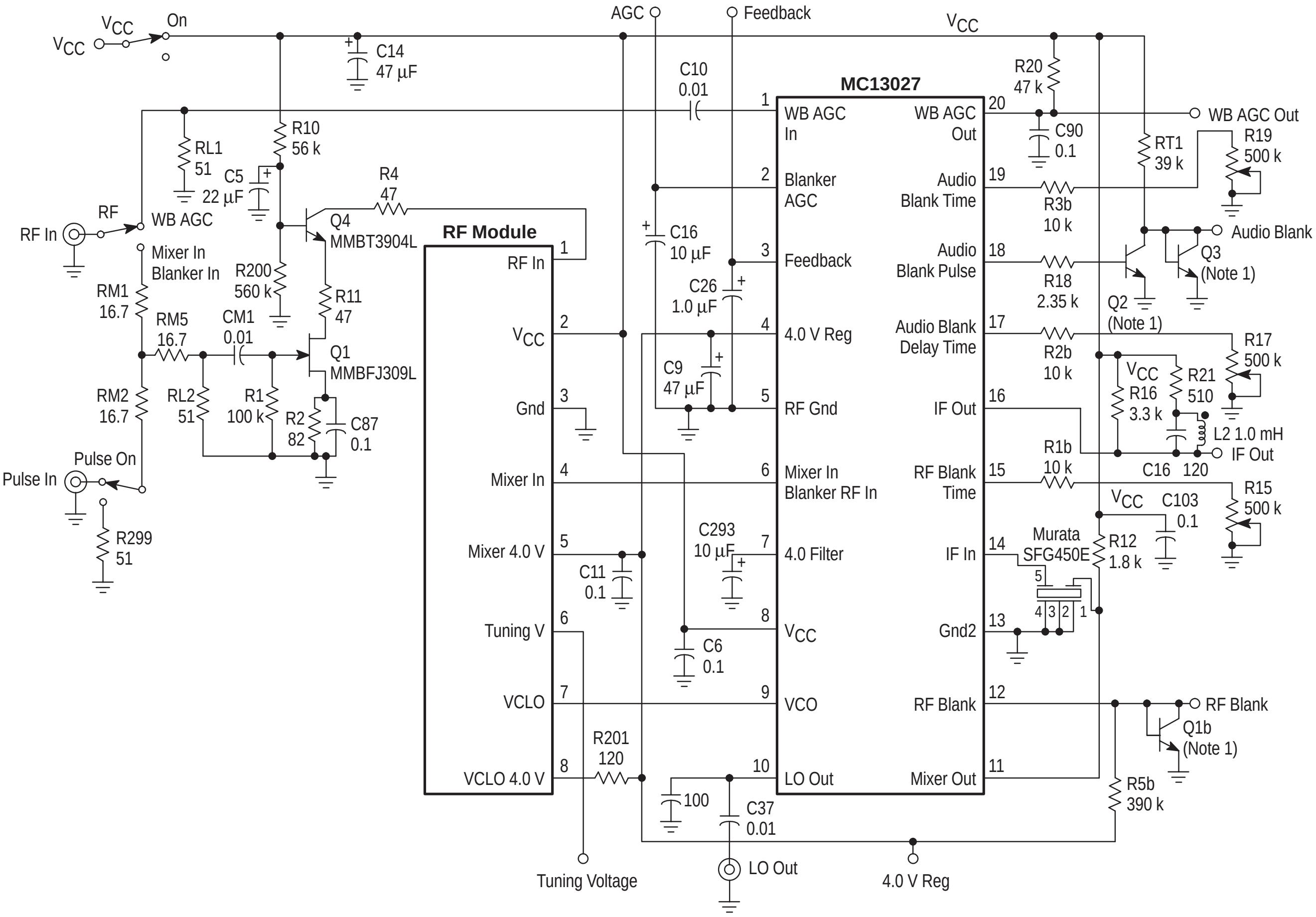


Figure 1. MC13027 Test Circuit

NOTE: 1. General purpose NPN transistor 2N3904 or equivalent.

MC13122
MAXIMUM RATINGS

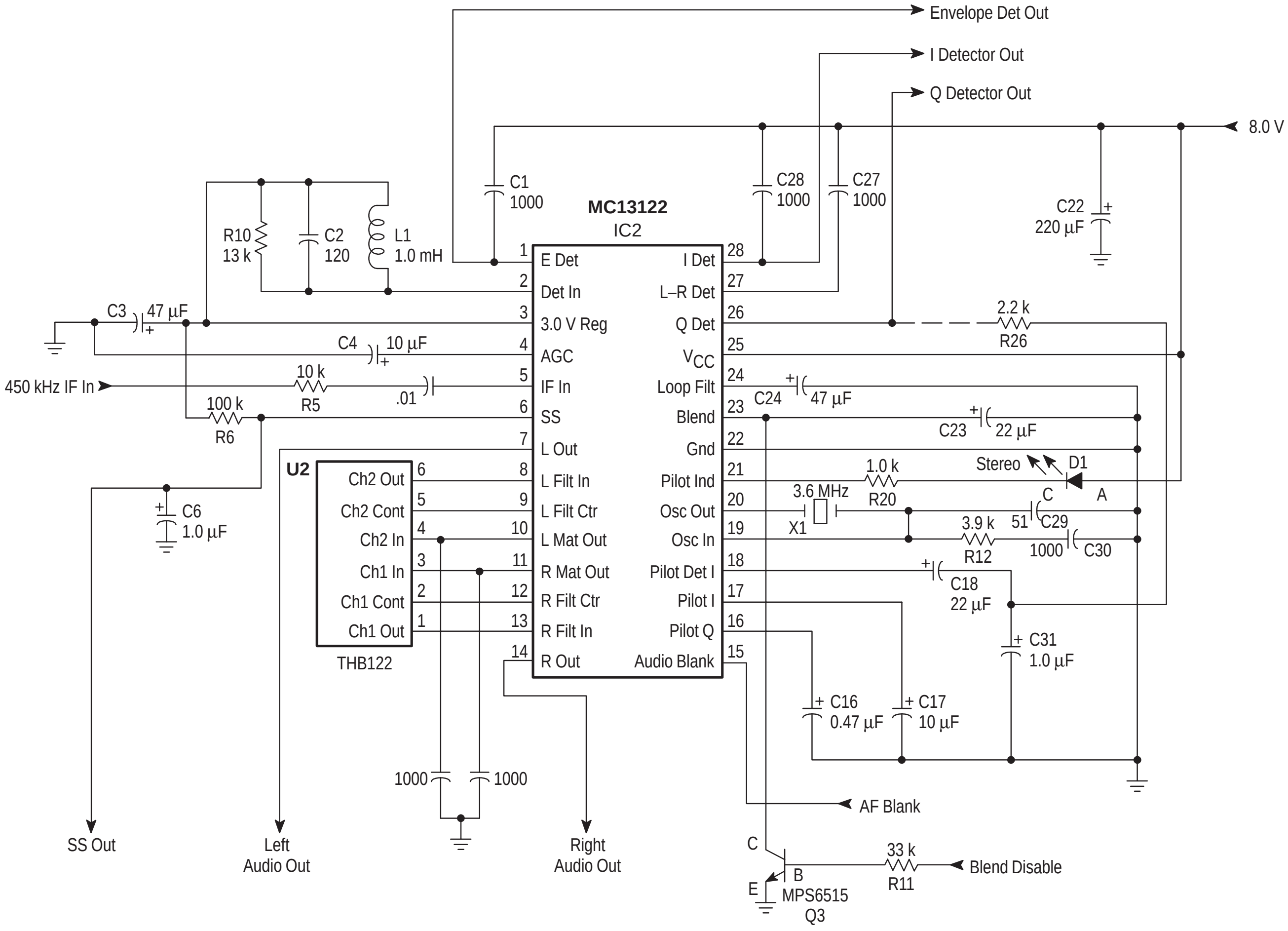
Rating	Symbol	Value	Unit
Power Supply Input Voltage	V_{CC}	12	Vdc
Stereo (Pilot) Indicator Lamp Current (Pin 21)	–	30	mAdc
Operating Ambient Temperature	T_A	–40 to +85	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Operating Junction Temperature	$T_{J(max)}$	150	°C
Power Dissipation Derated above 25°C	P_D	1.25 10	Ω mW/C

NOTE: ESD data available upon request.

MC13122
ELECTRICAL CHARACTERISTICS (V$_{CC}$ = 8.0 V, T$_A$ = 25°C, Test Circuit of Figure 2.)

Characteristic	Min	Typ	Max	Unit
Power Supply Operating Range	6.0	8.0	10	V
Supply Current Drain (Pin 25)	10	20	25	mA
Minimum Input Signal Level, Unmodulated, for AGC Start	–	5.0	–	mV
Audio Output Level, 50% Modulation, L Only or R Only	290	400	530	mVrms
Audio Output Level, 50% Mono	140	200	265	mVrms
Output THD, 50% Modulation (Monaural Stereo)	– –	0.3 0.5	0.8 1.6	%
Channel Separation, L Only or R Only, 50% Modulation	22	35	–	dB
IF Input Voltage Range	–	1.0–1000	–	mV
IF Input Resistance Range	–	10 to 50	–	kΩ
IF Amplifier Transconductance	–	9.6	–	mS
IF Detector Circuit Impedance	–	8.3	–	kΩ
Input AGC Threshold	–	5.0	–	mV
Stop–Sense Output Range	–	2.2 to 4.0	–	V
Audio Output Impedance at 1.0 kHz (Pins 7 and 14)	–	300	–	Ω
Stereo Indicator Lamp Leakage	–	–	1.0	µA
Stereo Indicator Saturation Voltage @ 3.0 mA	–	–	200	mVdc
Oscillator Capture Range	–	±3.0	–	kHz

Figure 2. MC13122 Test Circuit



AMAX STEREO CHIPSET

What is AMAX?

In 1993, a joint proposal by the EIA (Electronic Industries Association) and the NAB (National Association of Broadcasters) was issued. It included a unified standard for pre–emphasis and distortion for broadcasters as well as a set of criteria for the certification of receivers. The purpose of this proposal was to restore quality and uniformity to the AM band and to make it possible for the consumer to receive high quality signals using the AM band. The FCC has been supportive of this initiative and has required all new broadcast licensees to meet AMAX standards. The NAB and EIA have continued to encourage receiver manufacturers by offering the AMAX certification logo to be displayed on all qualifying radios. This logo is shown below.

or

The Receiver Criteria

An AMAX receiver must have wide bandwidth: 7.5kHz for home and auto, 6.5 kHz for portables. It must have some form of bandwidth control, either manual or automatic, including at least two bandwidth provisions, such as “narrow” and “wide”. It must meet NRSC receiver standards for distortion and deemphasis. It must have provisions for an external antenna. It must be capable of tuning the expanded AM band (up to 1700 kHz). And finally, home and auto receivers must have effective noise blanking. All of these requirements, except the noise blanking, have been met by Motorola’s previous AM radio products, such as MC13025 Front End and the MC13022A C–QUAM stereo decoder. It is the Noise Blanker requirement which is met by the two devices on this data sheet, the MC13027 and MC13122.

Noise blanking, especially in AM auto radios, has become extremely important. The combination of higher energy ignitions, using multiple spark coils, along with increased use of plastic in the auto body, have increased the noise energy at the radio. Also, the consumer has learned to expect higher quality audio due to advances in many other media. For the AM band to sustain interest to the consumer, a truly effective noise blanker is required.

The block diagram below shows the Motorola AMAX stereo chipset. It offers a two–pronged approach to noise blanking which is believed to be the most effective yet offered in the consumer market. The initial blanking takes place in the output of the mixer, using a shunt circuit triggered by a carefully defined wideband receiver. For most noises, some residual audible disturbance is almost always still present after this process. The disturbance becomes stretched and delayed as it passes through the rest of the selectivity in the receiver. The stretching and delay are predictable, so the MC13027 can provide a noise blanking pulse with the correct delay and stretch to the output stages of the MC13122 decoder. The MC13122 has a Track and Hold circuit which receives the blanking signal from the Front End and uses it to gently hold the audio wherever it is as the pulse arrives, and hold that value until the noise has passed. The combined effect is dramatic. A wide range of types of noise is successfully suppressed and the resulting audio seems almost clean until the noise is so intense that the blanking approaches full–time.

The amount of extra circuitry to accomplish noise blanking is relatively small. The external components for this added capability are shown in Figure 3. In the MC13027 Front end, the noise receiver/detector requires two capacitors. The presettings for blanking timing and blanking delay require three external fixed resistors. Finally the decoder requires two track and hold capacitors to store the “audio” voltage during the track and hold function.

Figure 3. AMAX Stereo Receiver with Noise Blanker

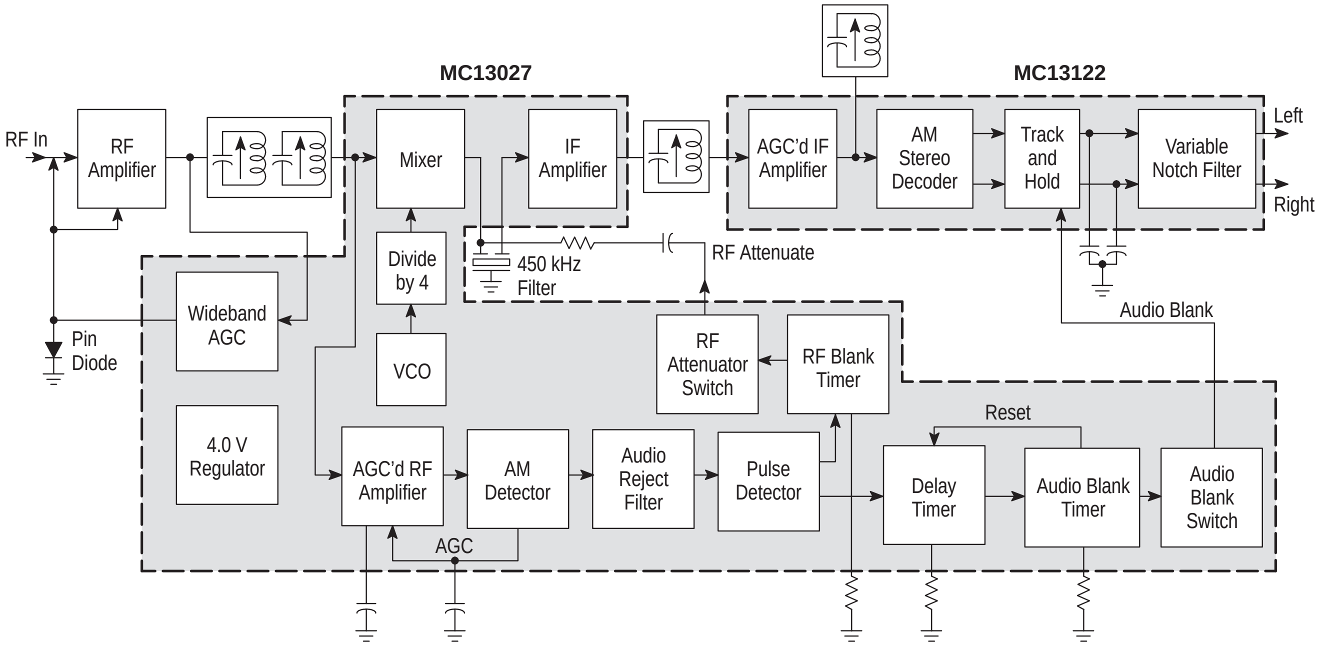
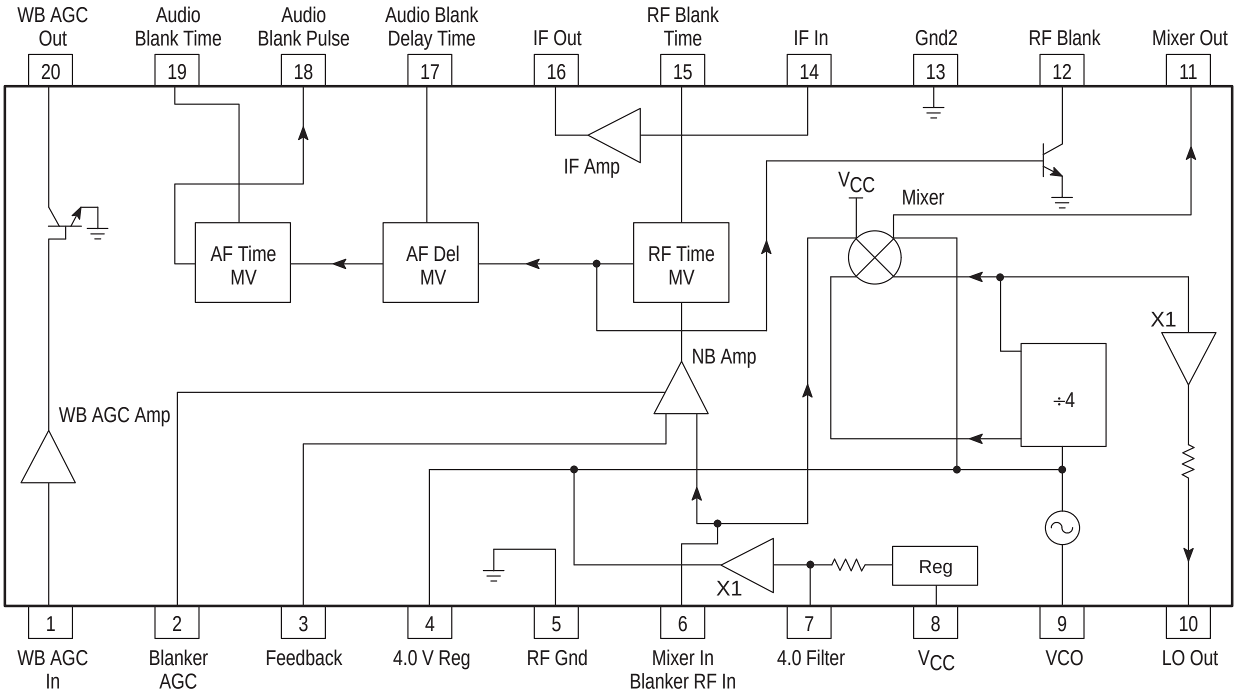


Figure 4. MC13027 Internal Block Diagram



MC13027 FUNCTIONAL DESCRIPTION

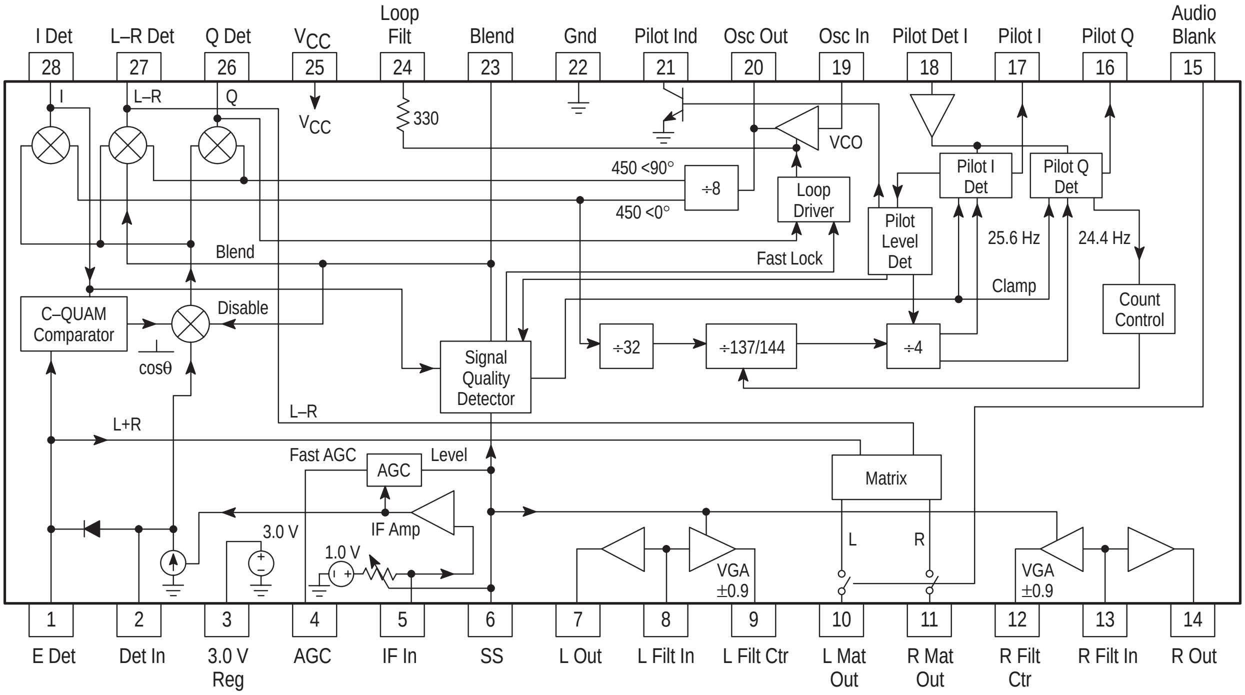
The MC13027 contains the mixer, wide band AGC system, local oscillator, IF pre–amplifier and noise blanker for an AM radio receiver. It is designed to be used with the MC13122 to produce a complete AM stereo receiver. The VCO runs at 4 (F_{in}+F_{IF}) and is divided internally by 4 for the mixer input and local oscillator buffered output. Dividing the VCO reduces the phase noise for AM stereo applications.

The noise blanker input is connected in parallel with the mixer input at Pin 6. The noise blanker circuitry contains a high gain amplifier with its own AGC so it remains linear throughout the mixer's linear range. It can detect noise pulses as low as 120 µV and generates three pulses when the noise threshold is exceeded. The width and timing of the blanking pulses is set by the resistors connected to Pins 15, 17 and 19. The resistor on Pin 15 sets the length of the RF blanking pulse and determines the time the transistor on Pin 12 is "on". The audio blanking pulse delay is set by the resistor on Pin 17 and the width by the resistor on Pin 19. This is necessary because the IF filtering delays and stretches the noise as it arrives at the detector. The transistor on Pin 18 goes "on" to cause noise blanking in the track and hold circuit in the MC13122 (Pin 15).

Wideband AGC is used in auto receivers to prevent overload – it drives the base of a cascode transistor RF amplifier and also a pin diode at the antenna (See Figures 6 and 7).

A low gain IF amplifier between Pins 14 and 16 is used as a buffer amplifier between the mixer output filter and IF filter. The input resistance of the IF amplifier is designed to match a ceramic IF filter. The gain of the IF amplifier is determined by the impedance of the load on Pin 16.

Figure 5. MC13122 Internal Block Diagram



MC13122 FUNCTIONAL DESCRIPTION

The MC13122 is designed to accept a 450 kHz C–QUAM input signal from approximately 1.0 mV to 1.0 V and produce L and R audio output signals. It has additional features: stop signal, variable bandwidth IF and audio response, stereo indicator driver and track and hold noise blanking.

The IF amplifier on Pin 5 has its own AGC system. It operates by varying the input resistance on Pin 5. With weak signals below approximate 5.0 mV, the input resistance is very high and the amplifier is at maximum gain. For this AGC to be effective, it is necessary to feed the IF input signal from a relatively high impedance. The input resistance variation also reduces the Q of the coil (T1 in the application) so the receiver bandwidth is narrow for weak signals and wide for strong signals. The value of the input resistor (R5) is selected for the desired loading of the IF coil. The impedance of the IF coil on Pin 2 determines the IF gain. Pin 2 is also the input to the C–QUAM decoder.

The IF signal drives the envelope (E), in–phase (I), quadrature (Q) and (L–R) detectors. The E detector is a quasi–synchronous true envelope detector. The others are true synchronous detectors. The E detector output provides the L+R portion of the C–QUAM signal directly to the matrix. The AGC signal of the IF amplifier drives the signal strength output at Pin 6. An external resistor on Pin 6 (sets the gain of the AGC). The Pin 6 voltage is used to control the Q of the audio notch filter, causing the audio bandwidth and depth of the 10 kHz notch to change with signal strength. It is also used as one of the inputs to the signal quality detector which generates the stop–sense and blend signal on Pins 6 and 23 respectively and tells the signal quality detector that the RF input is below the AGC threshold.

VCO

The 3.6 MHz ceramic resonator on Pins 19 and 20 is part of a phase locked loop which locks to the 450 kHz IF signal. The 3.6 MHz is divided by 8 to produce in–phase and quadrature signals for the I, Q and L–R detectors. It is also divided by 32, and 137/144 to provide signals for the pilot I and Q detectors. The pilot detector is a unique circuit which does not need filtering to detect the 25 Hz pilot.

Blend Circuit

The purpose of the blend circuit is to provide an AM stereo radio with the capability of very fast lock times, protection against stereo falsing when there is no pilot present and control of the L–R signal so as to provide as much stereo information as possible, while still sounding good in the presence of noise or interference. The circuit also provides an optional stop–sense usable by a radio with seek and/or scan. The stop–sense signal provides a “stop” signal only when the radio is locked on station, signal strength is above minimum level, and the level of interference is less than a predetermined amount. The last feature prevents stopping on frequencies where there is is a multiplicity of strong co–channel stations. It is common for AM radios without this capability to stop on many frequencies with unlistenable stations, especially at night.

The blend circuit controls the PLL fast lock, pilot detector, IF amplifier AGC rate, decoder L–R gain, cosθ compensation and stop–sense as a function of the voltage on a signal external blend capacitor. Timing is determined by the rate of change of voltage on the blend cap. Timing is changed by varying charge and discharge current and pulled down by a current source, switch, and optionally an external switch. The current sources and switches are controlled by various measures of signal quality, signal strength, and presence or absence of pilot tone.

Detectors

In AM stereo operation, the Q detector delivers pilot signal via an external low–pass filter to the pilot detector input (Pin 18). The E and I detectors drive the C–QUAM comparator. The L–R signal and the output of the envelope detector are combined in the matrix to produce the L and R signals. The C–QUAM system modifies the in–phase and quadrature components of the transmitted signal by the cosine of the phase angle of the resultant carrier, for proper stereo decoding. An uncompensated L–R would be distorted, primarily by second harmonics. Where there is noise or interference in the L–R, it has been subjectively determined that reducing the cosθ compensation at the expense of increased distortion sounds better than full decoding. The blend line operates over a small voltage range to eliminate cosine compensation.

Signal Quality Detector – Blend Voltage Control

The signal quality detector output is dependent on signal strength, over–modulation, and whether or not the blend pin has been pulled low prior to searching. Over–modulation usually occurs when a radio is tuned one channel away from a desired strong signal, so this prevents stopping one channel away from a strong signal.

In a radio tuned to a strong, interference free C–QUAM station, the blend voltage will be approximately 3.6 V. In the presence of noise or interference, when the modulation envelope is at a minimum, it is possible for the I detector to produce a negative, or below zero carrier signal. The Signal Quality Detector produces an output each time the negative I exceeds 4%. The output of the detector sets a latch. The output of the latch turns on current source which pulls down the voltage of the blend cap at a predetermined rate. The latch is then reset by a low frequency signal from the pilot detector logic. This produces about a 200 mV change each time 4% negative I is detected. Tables 1 and 2 describe the blend behavior under various conditions.

When the blend voltage reaches 2.2 V a blend control circuit starts to reduce the amplitude of the L–R signal fed to the decoder matrix. By 1.5 V the L–R has been reduced by about 40 dB. At lower voltages it is entirely off and the decoder output is monaural. This reduction of L–R signal, or blend as it is commonly called when done in FM stereo radios, reduces undesirable interference effects as a function of the amount of interference present.

Stop–Sense

Stop–sense is enabled when the blend voltage is externally pulled below 0.45 V. An input from the AGC indicating minimum signal, or detection of 10% negative I will cause the stop–sense pin to be pulled low. With signals greater than the AGC corner and less than 10% interference the stop–sense will be a minimum of 1.0 V below the 3.0 V line. Very rapid scanning is possible because the radio can scan to the next frequency as soon as the stop–sense goes low. The maximum wait time, set by the radio, is only reached on good stations.

The decoder will not lock on an adjacent channel because it is out of the lock range of the PLL. The beat note produced in the I detector by the out of lock condition will trigger the 10% negative I detector.

Sequence For Seek Scan

- Change Station – Pull–Down Blend
- Wait Approximately 50 ms for Synthesizer and Decoder PLL to Lock
- Observe Pin 6 Voltage
- If it is Above 2.0 V and Stays Above 2.0 V for Approximately 800 ms, Stay on the Station
- No IF Count Now Needed
- No AGC Level Detector Needed

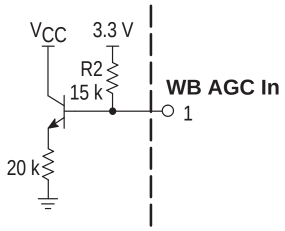
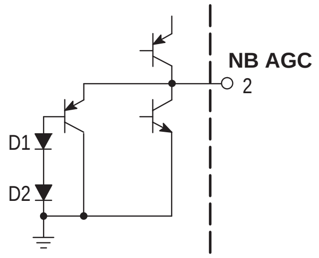
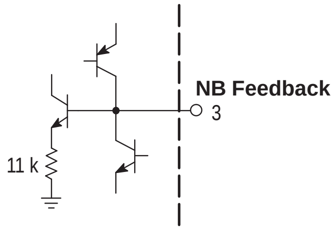
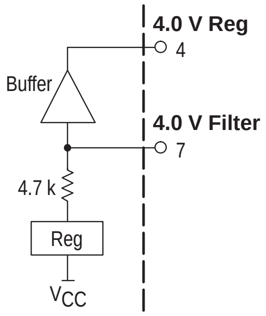
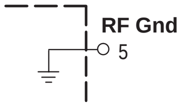
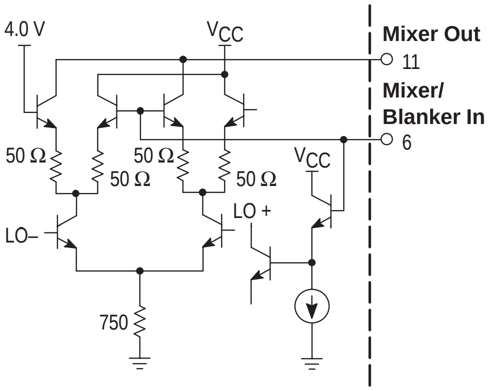
Table 1. Normal Sequence When Changing Stations

External Pull–Down of Blend Capacitor to Under 0.47 V	– Increased Current Supplied to Loop Driver for Fast Lock – Fast AGC Activated – Extra Current Pull–Up Activated on Blend Capacitor – Pilot Detector Disabled – Loop Locks – Stop–Sense Activated
Blend Released	– Blend Capacitor Pulled Up to 0.7 V – Stops – Fast Lock Current Removed – Fast AGC Turned Off – Pilot Detector Enabled
Pilot Detected	– Stereo Indicator Pin Pulled Low – Blend Voltage Pulled Positive Rapidly
Blend Voltage Reaches 1.4 V	– Audio Starts Into Stereo – 10% Negative I Detector Enabled
Blend Voltage Reaches 2.2 V	– Stereo Separator Reaches 20 to 25 dB – Rapid Current Pull–Up Turned Off – 4% Negative I Detector Enabled
Blend Voltage Reaches 3.0 V	– cosθ Enabled – Full C–QUAM Decoding – Blend Voltage Continues to Rise to 3.6 V and Stops

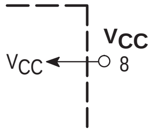
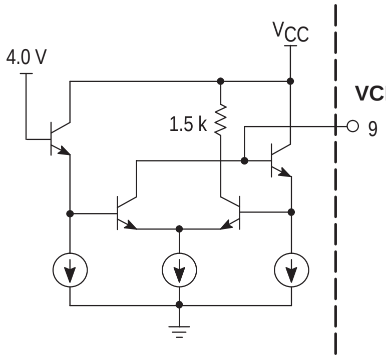
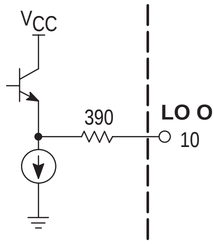
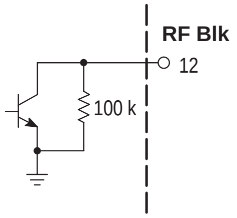
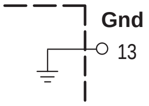
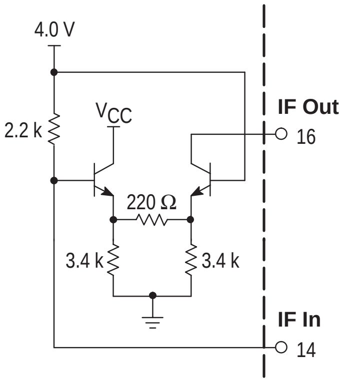
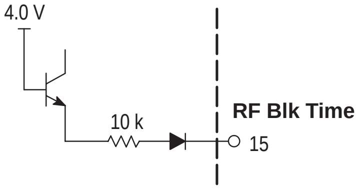
Table 2. Operation In Adverse Conditions

4% Negative I Detected	– Blend Pulls Down Approximately 200 mV for Each Event – Acts Like One–Shot – Stops at 2.2 V – cosθ Has Been Defeated, Almost Full Stereo Remains
10% Negative I Detected	– Blend Pulls Down 200 mV for Each Event – Stops at 1.4 V – Stereo Has Blended to Mono – Resets Fast Pull–Up if Blend Has Not Been Above 2.2 V
50% Negative I Detected (Out of Lock)	– Blend Pulls Down Fast During Event – Stops at 0.47 V – Resets Fast Pull–Up – Pilot Indicator Turned Off
Minimum Signal Level Detected	– Resets Fast Pull–Up – Pulls Down to 0.7 V

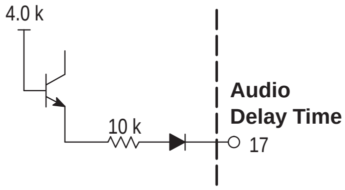
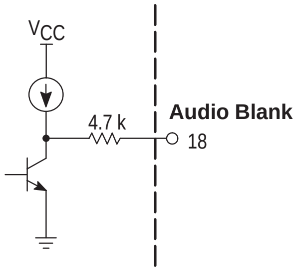
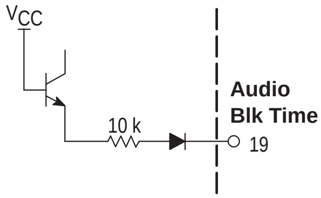
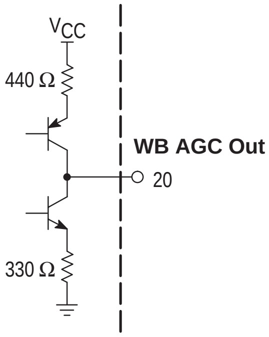
MC13027 PIN FUNCTION DESCRIPTION

Pin	Name	Internal Equivalent Circuit	Description
1	WB AGC In		**Wideband AGC Input** The input impedance to the WB AGC detector is 15 k and is internally biased so it must be coupled through a capacitor. The threshold can be increased by adding a resistor in series with the input. The WB AGC begins at about 1.0 mV. In car radios, this input should be connected to the collector of the RF amplifier cascode stage through a resistor and capacitor. A 68 pF to ground will prevent undesired high frequency signals from activating the WB AGC and make the sensitivity more uniform across the band.
2	Blanker AGC		**Blanker AGC** The capacitor to ground is the bypass for the noise blanker AGC circuit. The noise blanker can be disabled by grounding this pin. 10 µF is used in the application, but it can be changed to match the time constant of the main IF AGC in the MC13122, Pin 4.
3	Feedback		**Blanker Feedback** This pin is the dc feedback to the input stage of the wide band amplifier.
4	4.0 V Reg		**4.0 V Regulator** The 4.0 V regulator supplies low impedance bias to many of the circuits in the IC. It should be bypassed to a ground near Pin 5.
7	4.0 V Filt		**4.0 V Filter** The external capacitor works with internal 4.7 k to filter noise from the bandgap regulator.
5	Gnd		**RF Ground** This pin is the ground for the RF section, blanker RF, filters and all radio circuits except the IF. In the PCB layout, the ground pin should be used as the internal return ground in the RF circuits.
6	Blk$_{RF}$/Mix$_{In}$		**Mixer Input/Blanker RF Input** The blanker RF input must be biased from the 4.0 V on Pin 4. The mixer input is to two bases of the upper mixer transistors. A low impedance dc path to the 4.0 V on Pin 4 is required. Normally, this would be a coil secondary connected between Pins 6 and 4.
11	Mixer Out		**Mixer Output** A single ended output of a double balanced mixer. A load resistor to supply is chosen to match the ceramic filter, typically 1.5 k to 1.8 k. Output current is 830 µA.

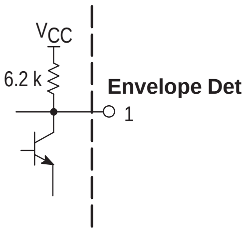
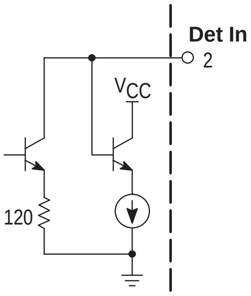
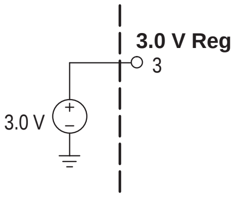
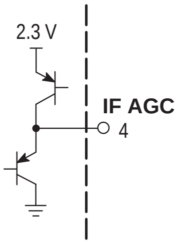
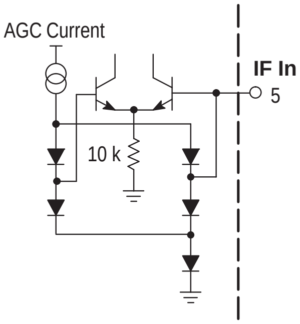
MC13027 PIN FUNCTION DESCRIPTION (continued)

Pin	Name	Internal Equivalent Circuit	Description
8	V_{CC}		**Supply Voltage** The normal operating voltage range is 6.0 to 10 V.
9	VCLO		**Voltage Control Local Oscillator** The oscillator is a cross coupled negative resistance type and this pin must be connected through a low dc resistance to Pin 4, the 4.0 V regulator. Normally, this would be the secondary of the oscillator coil. The impedance of the secondary winding should be around 2.8 kΩ to guarantee that the oscillator will run. It operates at 4 times the LO frequency: $f_{osc} = 4(F_{in}+F_{IF})$.
10	LO Out		**Local Oscillator Output** This is an emitter follower for LO output to drive a synthesizer. It is a square wave output, the internal series resistance and allows a small bypass to reduce high frequency harmonics.
12	RF Blank		**RF Blanker** An unbiased NPN acts as a SHUNT impedance when turned on. The 100 k resistor provides a dc path for the capacitor.
13	Gnd2		**IF Ground** Pin 13 is the ground for the IF section and the timing and switching circuits in the blanker. In the application circuit this should be common to the MC13122 ground.
14	IF In		**IF Input** A degenerated differential amplifier internally biased to 4.0 V. The IF input impedance is approximately 1.8 k to match a ceramic filter. The IF amplifier is used as a buffer between the ceramic filter and the detector coil and has a fixed gain determined by the impedance of the output coil.
16	IF Out		**IF Output** An open collector provides high–impedance drive to the MC13122; the IF gain is set by the ac impedance on this pin.
15	RF Time		**RF Blank Time** A resistor to ground sets the RF blanking time. The time is set to the minimum required to attenuate the pulse received. This is normally longest at the low end of the band. The value is best approved by ear. A fixed value can be chosen for production. (50 µs is typical.)

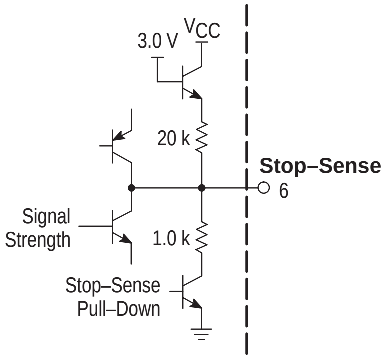
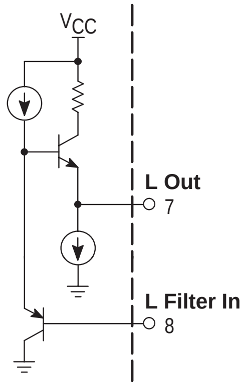
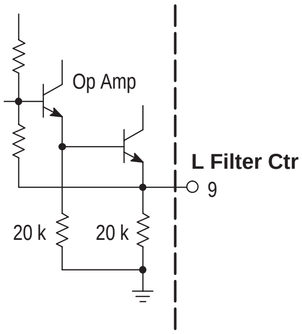
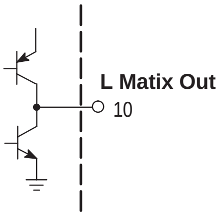
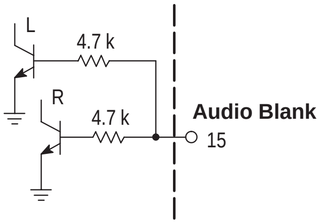
MC13027 PIN FUNCTION DESCRIPTION (continued)

Pin	Name	Internal Equivalent Circuit	Description
17	Delay Time		**Audio Blank Delay Time** A resistor to ground sets the delay time from the beginning of the RF blanking pulse to the beginning of the audio blanking pulse. This normally is about 50 µs for a wide AMAX filter. The ear is the most sensitive measure of the correct delay; start low, say 20 µs, and vary delay until noise is heard, and then reduce somewhat.
18	Audio Blank Cntl		**Audio Blank Pulse** When the blanker is operating, a positive pulse from this pin is fed to Pin 15 of the MC13122 to blank the audio signal.
19	Audio Time		**Audio Blank Time** A resistor to ground sets the width of the blanking pulse on Pin 18. This is usually selected by applying a pulse to the antenna of the receiver and adjusting a variable resistor. The blanking signal should be just long enough to suppress the audio pulse. Again the ear is the most sensitive tool. Start long, approximately 250 µs and reduce until noise is audible then increase.
20	WB AGC Out		**Wideband AGC Output** A push–pull current output. The resistor to voltage source (normally V_{CC}) determines the gain. Used to bias a cascode transistor in series with the input FET and can also be used to drive a PNP transistor which drives a pin diode attenuator (refer to Application Circuit Figure 6.)

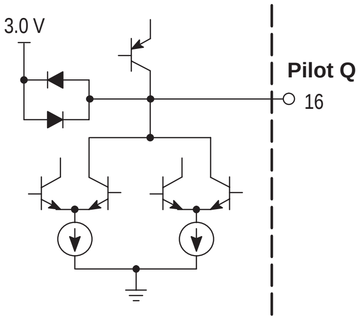
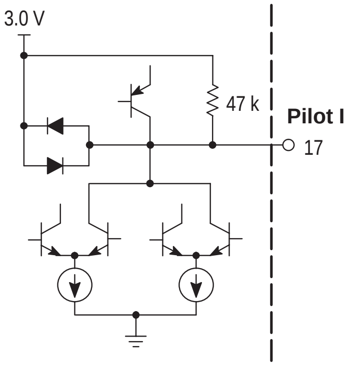
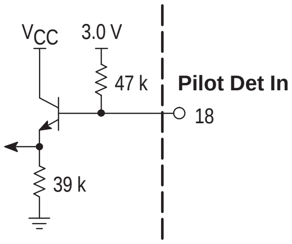
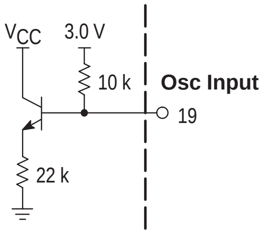
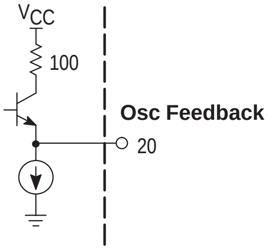
MC13122 PIN FUNCTION DESCRIPTION

Pin	Name	Internal Equivalent Circuit	Description
1	E Detector		**Envelope Detector** This is the output of the envelope detector and is used for one input to the comparator that generates cosθ signal and the L+R input to the matrix. It is a quasi–synchronous full wave detector with very low distortion (<1% at 100% modulation). The output impedance is 6.2 k, and it is bypassed to V_{CC} with 1.0 nF to eliminate 900 kHz components. The bypass capacitor must be the same as the one on Pin 27 and 28 for lowest stereo distortion and best separation.
2	Detector In		**IF Out/Decoder Input** The IF coil is connected from Pin 2 to Pin 3, the 3.0 V regulator. The IF amplifier output is a current source. The gain is determined by the impedance between Pins 2 and 3. Bandwidth and gain is set by the resistance across the coil.
3	3.0 V Reg		**3.0 V Regulator** This bandgap regulator supplies bias to many of the circuits in the IC.
4	AGC Byp		**IF AGC Bypass** The AGC has a fast and slow time constant. The fast AGC is 18X the slow one and is active when the 450 kHz loop is not locked. This allows for fast scanning in car radios. This capacitor should be selected for distortion for low frequencies at 80% modulation.
5	IF In		**IF Input** The IF AGC varies the current through attenuator diodes. The diodes vary the input impedance shunting the IF signal. The varying impedance also varies the Q and therefore the bandwidth. The IF AGC is accomplished by turning on the diodes and lowering the IF input impedance.

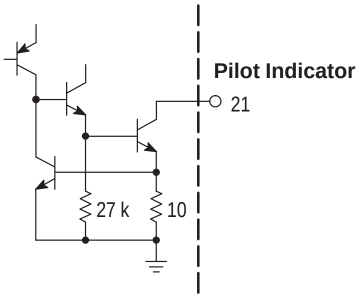
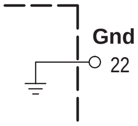
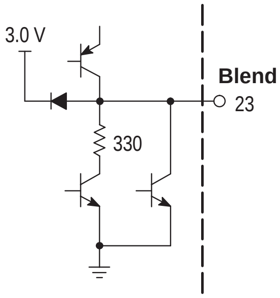
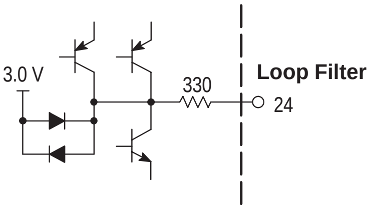
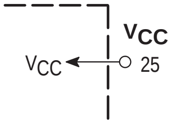
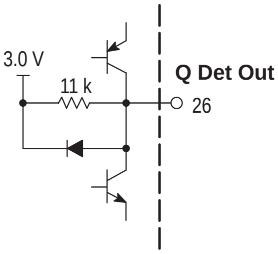
MC13122 PIN FUNCTION DESCRIPTION (continued)

Pin	Name	Internal Equivalent Circuit	Description
6	SS		**Signal Strength/Stop–Sense** The signal strength is a push–pull circuit. The voltage is 2.2 V at minimum signal and 3.5 to 5.0 V at strong signal. This dc voltage is also used to control the audio output notch filters. If the Blend pin is low the stop–sense is activated and this pin can go low. This can be used to control the seek–scan in the radio.
7 14	Left Out Right Out		**Filtered Left and Filtered Right Output** This can drive a de–emphasis filter to bring audio contour to AMAX specifications. Since the output is an emitter follower, the output impedance is low, and a series R should be used with the de–emphasis network as shown on the application circuit.
8 13	L Filt In R Filt In		**Input to Notch Filter** DC bias is supplied through the external filter components.
9 12	L Filt Ctr R Filt Ctr		**Left Filter and Right Filter Center** Drives the center leg of a twin–T filter, varying the Q. At strong signal, positive feedback narrows the notch, and there is little HF roll–off. At weak signal, negative feedback produces a broad notch and HF roll–off.
10 11	L Matrix Out R Matrix Out		**Track and Hold Output** This is a unity gain operational amplifier output. The current is turned off by the blanking pulse. The capacitor holds output voltage constant until unblanked. Internal feedback causes the output impedance to be low.
15	AF Blank In		**Audio Blank Control** The current to the output drivers is turned off.

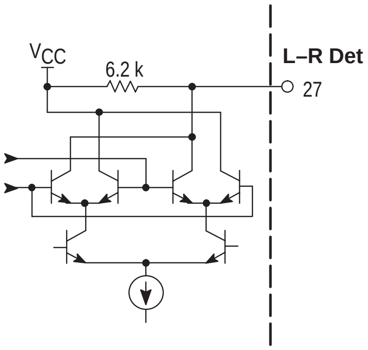
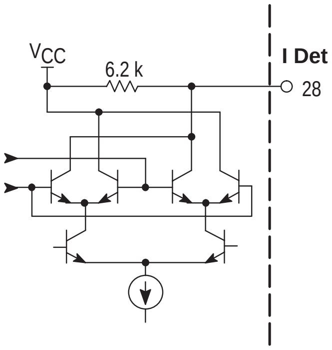
MC13122 PIN FUNCTION DESCRIPTION (continued)

Pin	Name	Internal Equivalent Circuit	Description
16	Pilot Q		**Pilot Q** This is the output of a quadrature detector of a narrowband phase locked loop system. It is used to control the pilot detector circuitry. The pilot Q is clamped to the 3.0 V reference when the blend voltage is pulled low. This results in faster pilot detection when a stereo station is tuned in. If the blend is not pulled low, the pilot Q will drift up approximately 0.5 V when there is no pilot, and it will take longer to detect the pilot. The capacitor to ground is the loop filter. It sets the pilot loop bandwidth: if it is too large, the loop bandwidth maybe too small, and the pilot may not be re–acquired if it is lost unless the blend pin is externally pulled low again.
17	Pilot I		**Pilot I** When the loop is locked to a 25 Hz AM stereo pilot, this is the output of a an in–phase synchronous detector. The capacitor filters the output, which is used to drive the pilot indicator driver on Pin 21. The time constant for the pilot indicator output is determined by this capacitor and the internal 47 k resistor. If the capacitor is too small, it can lead to pilot falsing due to noise. If the capacitor is too large, the acquisition time increases. The cap is charged to 3.0 V when the blend voltage is low to shorten lock time.
18	Pilot Det In		**Pilot Detector Input** The pilot detector will detect a pilot tone between 24.4 and 25.6 Hz. The pilot signal is fed from Q detector through a low pass filter on Pin 26. The audio signals from the Q detector must be filtered out, so a low–pass filter is used. The capacitor in series with Pin 18 blocks dc and prevents large low frequency transients from knocking the decoder out of stereo mode.
19	Osc In		**Oscillator Input** The input impedance is 10 k, but the recommended circuit adds 3.9 k in parallel with this to control the capture range of the VCO to be around ±3.0 kHz. using the recommended ceramic resonator.
20	Osc Out		**Oscillator Output** The internal phase shift of the VCO is 90 degrees, and the output impedance is low. It is designed to drive a resonant circuit with a 90 degree phase shift at the center frequency.

MC13122 PIN FUNCTION DESCRIPTION (continued)

Pin	Name	Internal Equivalent Circuit	Description
21	Pilot Indicator		**Pilot Indicator** The maximum current is internally limited to protect the IC, but it should be operated with a current limiting resistor.
22	Gnd		**Ground** Use good practices to keep oscillator returns and RF bypasses to good copper near this point
23	Blend Cont		**Blend Control** There are pull–up and pull–down currents provided to this pin. The external capacitor controls the rate of change of this voltage and 22 µF is recommended. This is an important voltage affecting many functions in the IC.
24	Loop Filt		**Loop Filter** The phase detector is a current source, so only a single RC loop filter is needed for a second order loop. The internal 330 Ω resistor together with a 47 µF gives the correct corner frequency and damping for the proper operation on the decoder loop. The cap should be low leakage to avoid static phase error.
25	V_{CC}		**V_{CC}** The operating voltage is normally 8.0 to 10 V in car radios. The MC13122 will work from 6.0 to 10 V.
26	Q Detector		**Q Detector Output** This is a synchronous detector in quadrature with the 450 kHz IF signal. The output impedance is 11 k. This signal is normally used for input to the pilot detector and internally for the fast lock.

MC13122 PIN FUNCTION DESCRIPTION (continued)

Pin	Name	Internal Equivalent Circuit	Description
27	L–R Detector		**L–R Detector** This is similar to the Q detector output but its level is controlled by the blend circuit. When the blend is active, the L–R output is reduced in level by reducing the dc current until mono operation is reached. It operates in the same way as the blend circuit in FM stereo decoders. The bypass capacitor should be 1.0 nF as on Pin 1 for optimum channel separation.
28	I Detector		**I Detector** This is a synchronous detector in phase with the 450 kHz IF signal. It is used internally to generate the cosθ signal and as an input to the signal quality detector. The bypass capacitor should be the same as the one on Pin 1 for best separation and lowest stereo distortion.

CAR RADIO APPLICATION

Figure 6 shows a car radio circuit using a TOKO pre–tuned RF module. The RF module includes a 4 diode tracking circuit to eliminate mistracking between the oscillator and RF circuits over the 530 to 1700 kHz AM band. This is important for stereo performance because mistracking will cause mono distortion and will significantly reduce the stereo separation. The THB122 module contains the variable 10 kHz notch filter. This module can be replaced with discrete components as shown in Figure 8, using 1% resistors and 5% capacitors.

Some manufacturers add a PIN diode attenuator at the antenna input. An example is shown in Figure 7.

The WB AGC sensitivity can be adjusted by changing R4 in series with the WB AGC input, Pin 1. The internal input resistance is 15 k.

R15, R17 and R19 are the blanker timing resistors. They were setup for this circuit and can be changed if desired.

FL1 is a linear phase IF filter . We recommend a Gaussian (rounded) filter, such as SFG or SFH for lower distortion and better separation than one with a flatter amplitude response. The SFG types of filters have poorer selectivity than the ones with flat GDT (group delay time) so some compromise has been made on adjacent channel selectivity.

The blanker can be disabled for testing by grounding the blanker AGC on Pin 2 in the MC13027.

The blanker and mixer inputs must be biased from the 4.0 V regulator through a low dc resistance like the secondary winding of the RF coil.

The receiver VCO operates at 4 times the local oscillator frequency and is divided internally in the MC13027 so that both the mixer input and the LO out is the same as in other receivers. This receiver can be connected to an existing synthesizer. For AM stereo, the synthesizer must have low phase noise. The Motorola MC145173 is recommended. For bench testing of this receiver, the Motorola MC145151 parallel input synthesizer may be useful. It will operate on 9.0 V and the phase detector can provide tuning voltage without a buffer amplifier.

The SS (stop–sense) output can be used for station searching and scanning. The best way to use it is to connect the SS signal to a comparator or A–D converter in the control microprocessor. If Pin 23 is grounded during searching by turning on Q3, the SS voltage changes from less than 0.5 V to around 2.2 V when an RF threshold is exceeded, as is shown in the graph in Figure 15. This system results in very reliable stopping on usable signals and fast detection of AM stereo signals. After a station is detected, Q3 should be turned off.

This receiver is very easy to set up because the TOKO module is pre–aligned. The only adjustments are to tune T1 and T2 for maximum voltage of the SS out line or maximum audio with a weak signal. If desired, they can be changed slightly to maximize stereo separation.

If different components are used, the blanker resistors can be setup as follows:

Ground Pin 2 of the MC13027. Apply a 1.0 μs pulse or 50 Hz square wave of about 10 mV through a dummy antenna and synchronize an oscilloscope to the pulse generator. Observe the signal at the mixer collector (Pin 11). It should be a sine wave burst. Remove the ground on Pin 2 and adjust R15 so the burst is just suppressed. Check the performance at the ends and middle of the band because the width might change due to RF circuit bandwidth.

Mix the pulse signal with a CW signal of about 300 μV with a power combiner and connect the oscilloscope to Pin 7 or Pin 14 of the MC13122. Adjust R17 so the blanking starts at the beginning of the audio pulse and R19 so the audio blanking is just long enough to suppress the audio pulse. The audio blanking time should not be made longer than necessary because it will be more noticeable in the normal program. The effectiveness of the blanker can be determined in field testing by connecting a switch from Pin 2 of the MC13027 to ground and bringing it outside the radio.

Figures 10 to 19 refer to the performance of the Application Circuit of Figure 6.

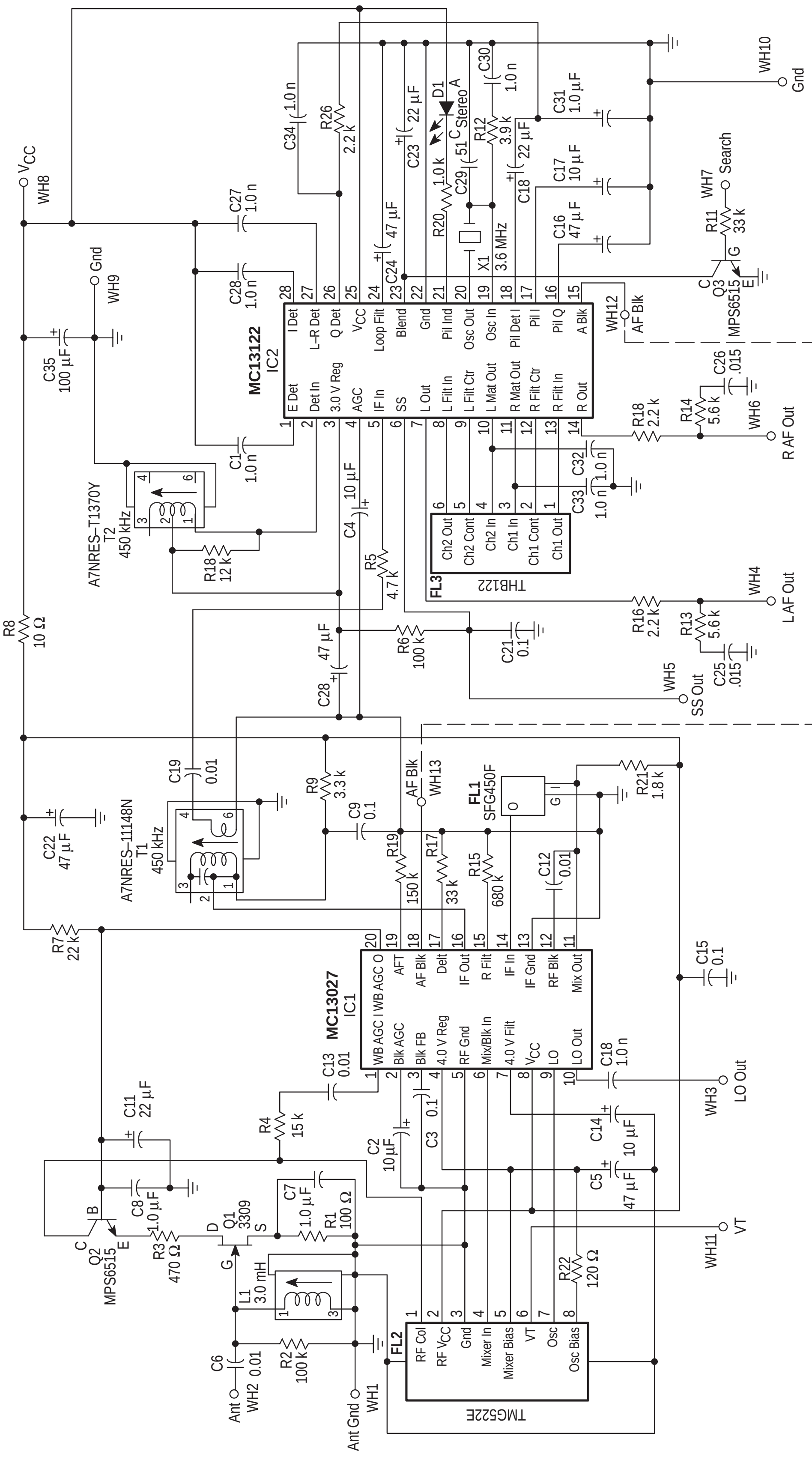


Figure 6. AMAX Chipset Application Circuit

Figure 7. RF Pin Diode

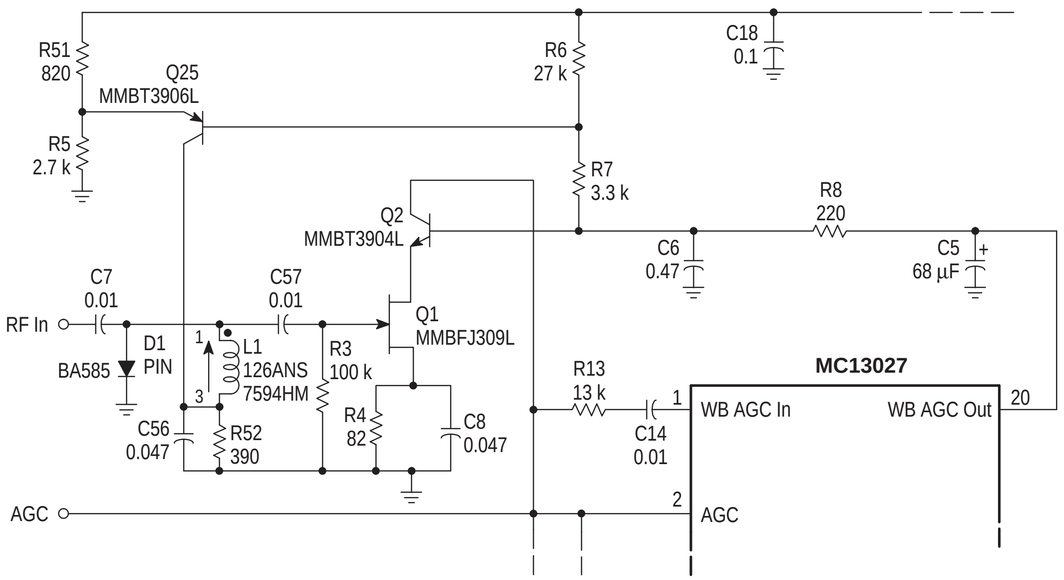


Figure 8. MC13027/MC13122 Discrete RF and Notch Filters

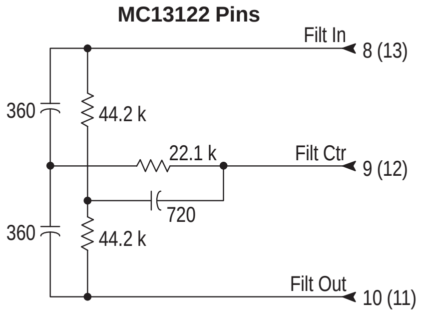


Figure 9. Overall Selectivity of a Typical Receiver versus Filter Control Voltage

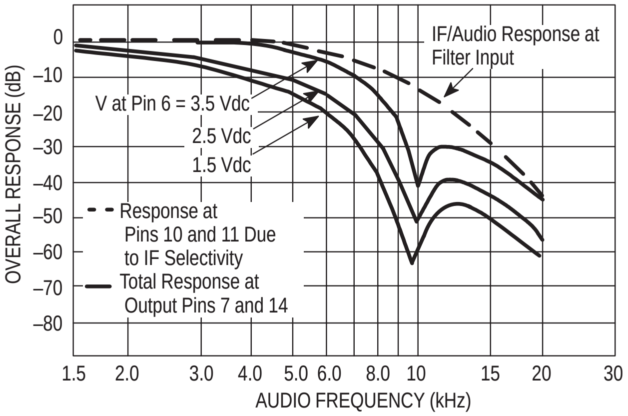
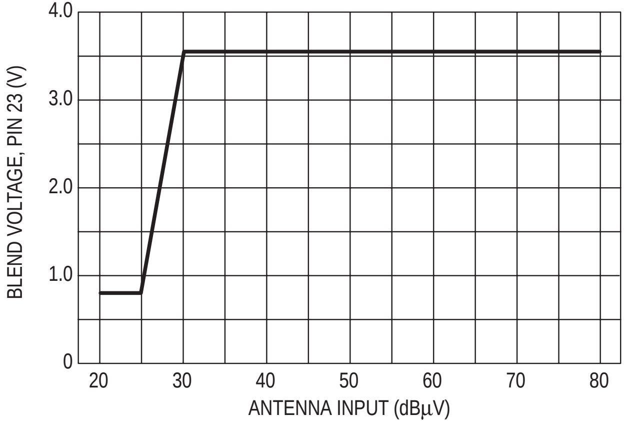
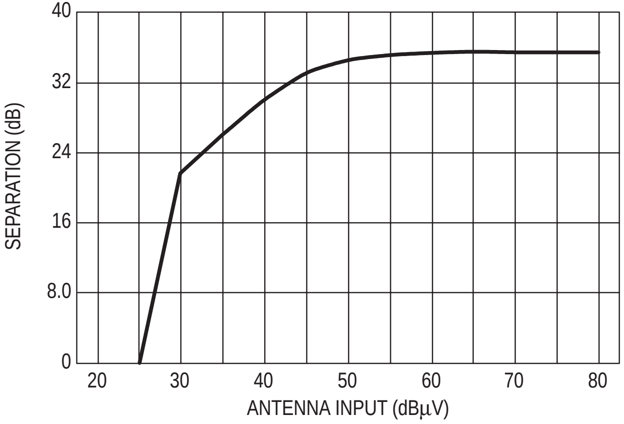


Figure 10. Blend Voltage versus RF Input Level



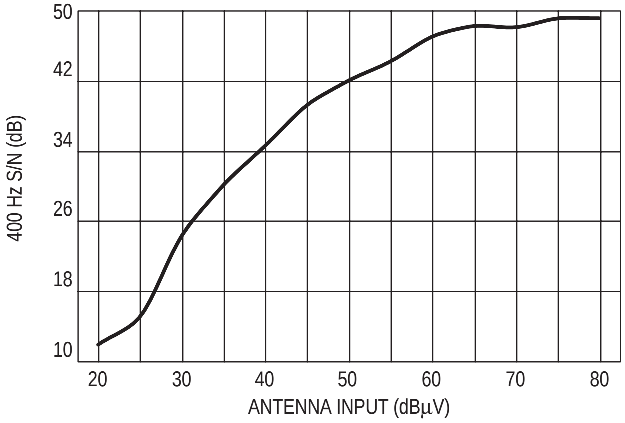
NOTE: The graphs on this page were made using the 15/60 pF dummy antenna and the Application Circuit of Figure 6.

Figure 11. Separation versus RF Input Level



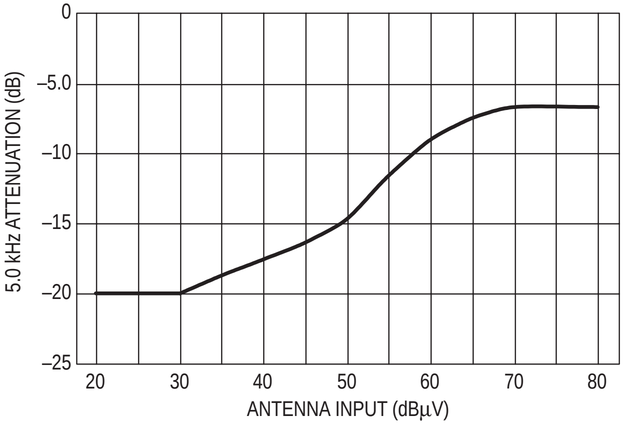
NOTE: The radio stays in mono until the stereo signal is sufficiently large and then makes a smooth transition to stereo. This is similar to FM receivers with variable blend.

Figure 12. Signal to Noise versus RF Input Level



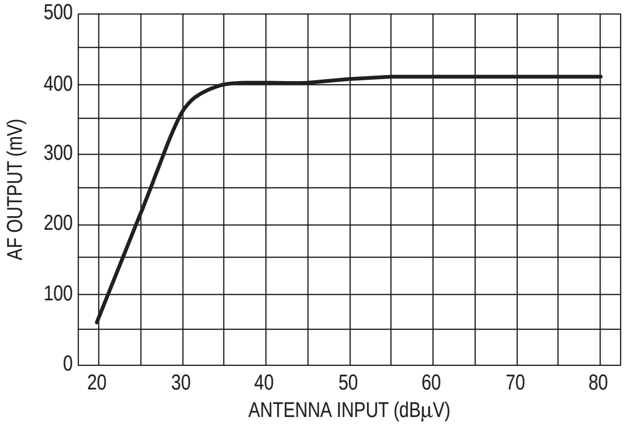
NOTE: The slightly abrupt change at around 25 dBµV is due to the decoder switching into stereo.

Figure 13. 5.0 kHz Attentuation versus RF Input Level



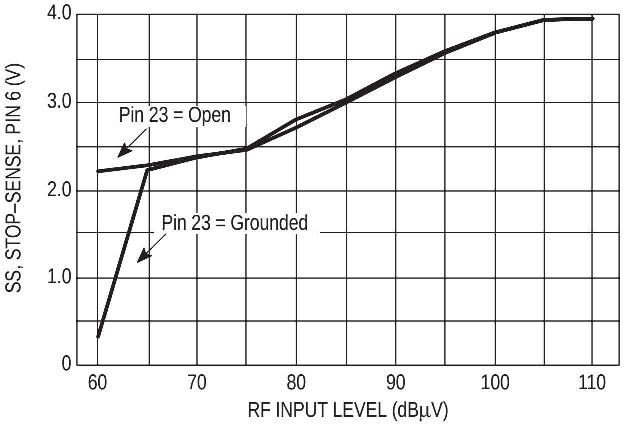
NOTE: This curve shows the effect of the variable audio bandwidth control of the MC13122. It is due to the variable loading of the IF coil and the variable 10 kHz notch filter in the output.

Figure 14. Audio Output Level versus RF Input Level



NOTE: All the curves of performance versus RF input level were generated using the car radio receiver circuit shown in Figure 6. Using a 15/60 pF dummy antenna input and a 50% L only stereo signal.

Figure 15. Stop–Sense Voltage versus RF Input Level



NOTE: This measurement was made on the MC13122 alone with a 10 k series input resistor. It will enable the designer to determine the stop–sense level if the gain of receiver RF section is known. Note that if Pin 23 is held low, the SS voltage on Pin 6 rises from about 0.3 to 2.2 V over a small change in RF level. This can be used to generate a very reliable stop signal. If Pin 23 is not held low, the SS voltage starts out at 2.2 V and rises slowly to a maximum of around 4.0 V.

Figure 16. Audio Blanking Delay versus R17

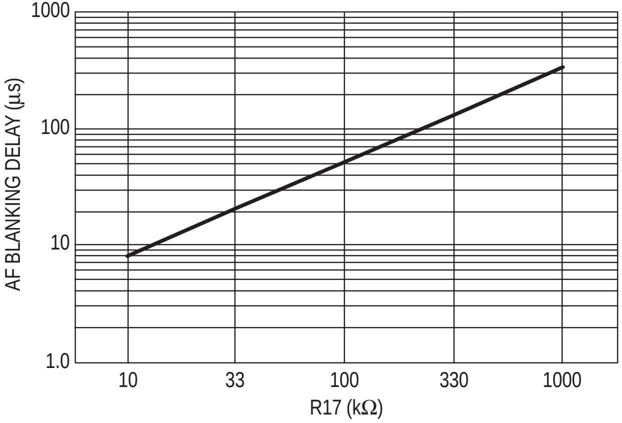


Figure 17. RF Blanking Time versus R15

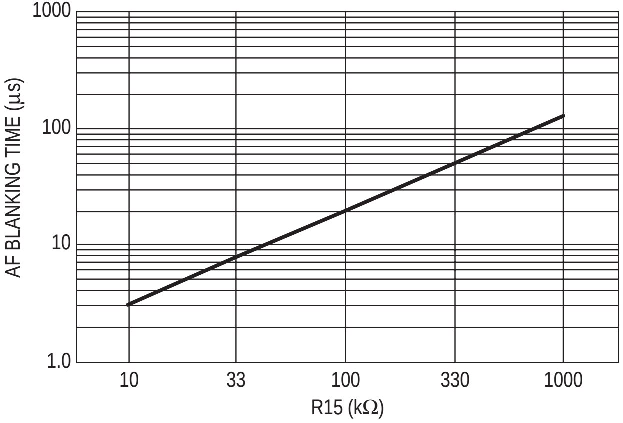


Figure 18. Audio Blanking Time versus R19

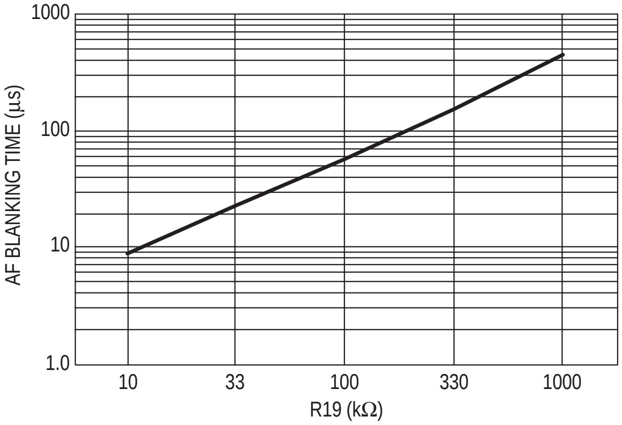
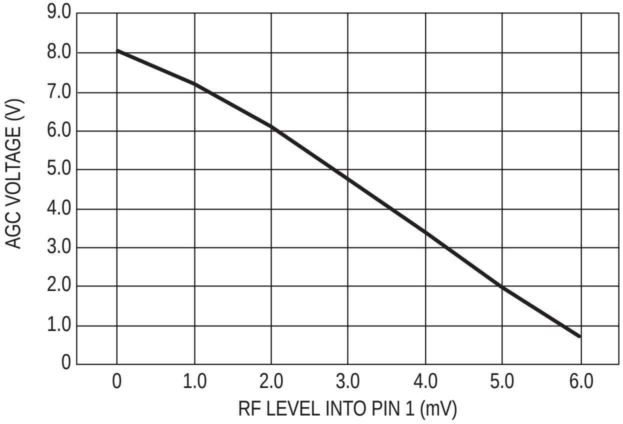


Figure 19. WB AGC Output Voltage (Pin 20) versus RF Input Level



NOTE: This was measured by applying an RF signal through a capacitor directly to Pin 1. The input resistance is 15 k, so the desired threshold can be increased by adding a resistor in series with the input.

AMAX STEREO CHIPSET

The RF Module

In the early development phase of this AMAX Stereo Chipset, Motorola worked with TOKO America Inc. to develop an RF tuning module. Part number TMG522E was assigned and is available from TOKO now. This module provides the “tracked” tuning elements for the RF (T1 and T2 and associated capacitors and varicaps) and the VCO (T3 et al). Some radio designers may prefer to develop their own tuning system using discrete coils and components, but the TOKO approach offers good performance, compactness and ease of application. Motorola recommends that every designer use this approach at least for initial system development and evaluation.

As refinement of the application progressed, it was found that a modification of the TMG522E was needed which would reduce the amount of VCO leakage into the Mixer through the power supply connections. This modification is described below. Motorola will work with TOKO to develop a new part number incorporating this change. In the meantime, it is necessary that the user perform these simple changes, because the radio circuits throughout this data sheet assume this modified design.

Modifying the TMG522E

Referring to Figures 20 and 21, there are three simple steps to the modification:

1. Cut the thin copper trace from Pin 2 to Pin 5 as shown.
2. Cut the thin copper trace from Pin 8 to the bottom of the 120 Ω resistor. Removal of the resistor is optional.
3. Connect a wire from Pin 5 to the top of the 120 Ω resistor (or the upper pad for the resistor).

Figure 20. TMG522E Schematic

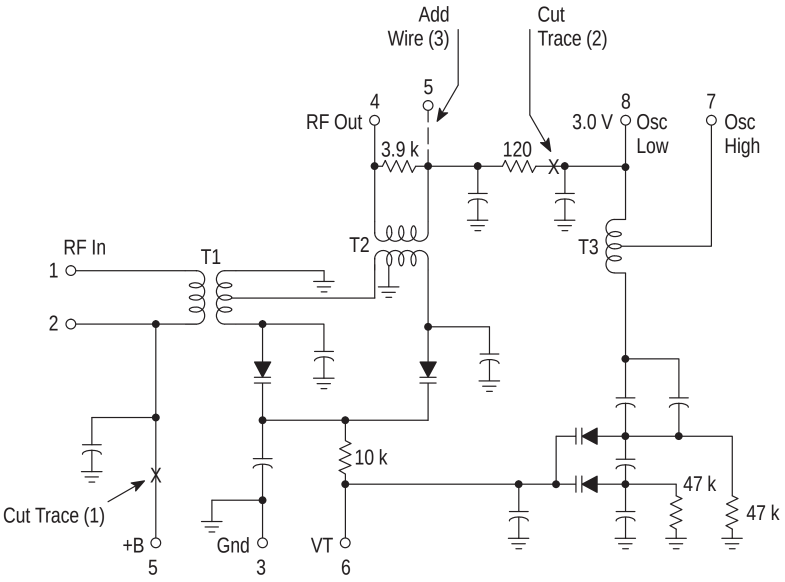


Figure 21. TMG522E Physical Modifications

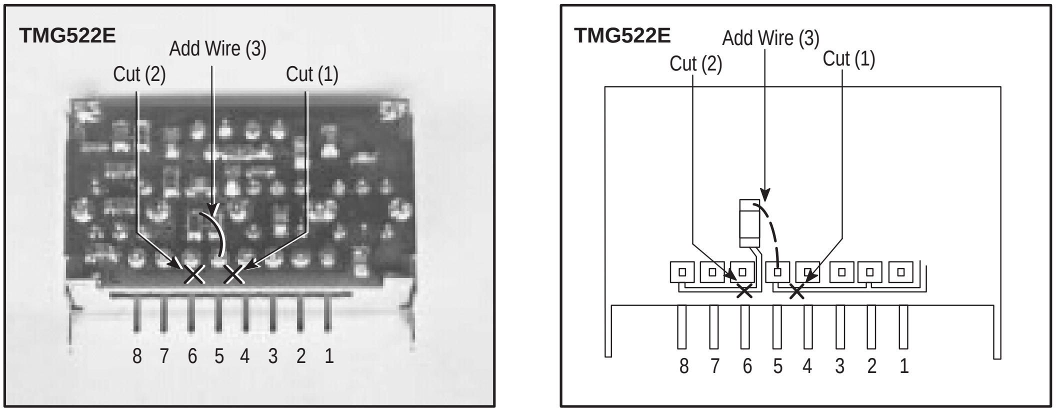


Figure 22. AMAX Chipset Printed Circuit Board
(Top View)

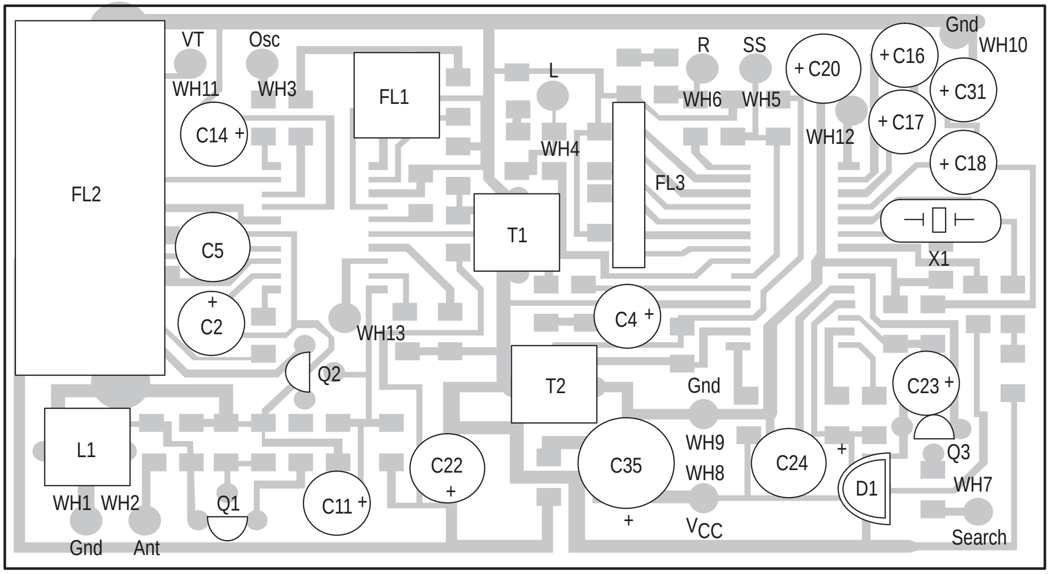


Figure 23. AMAX Chipset Printed Circuit Board
(Bottom View)

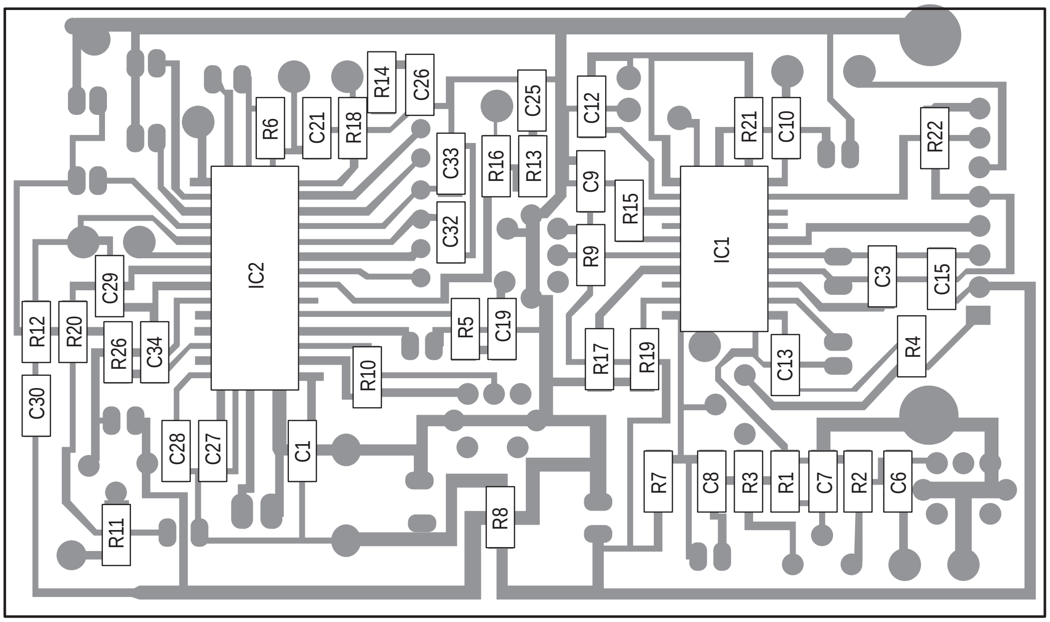
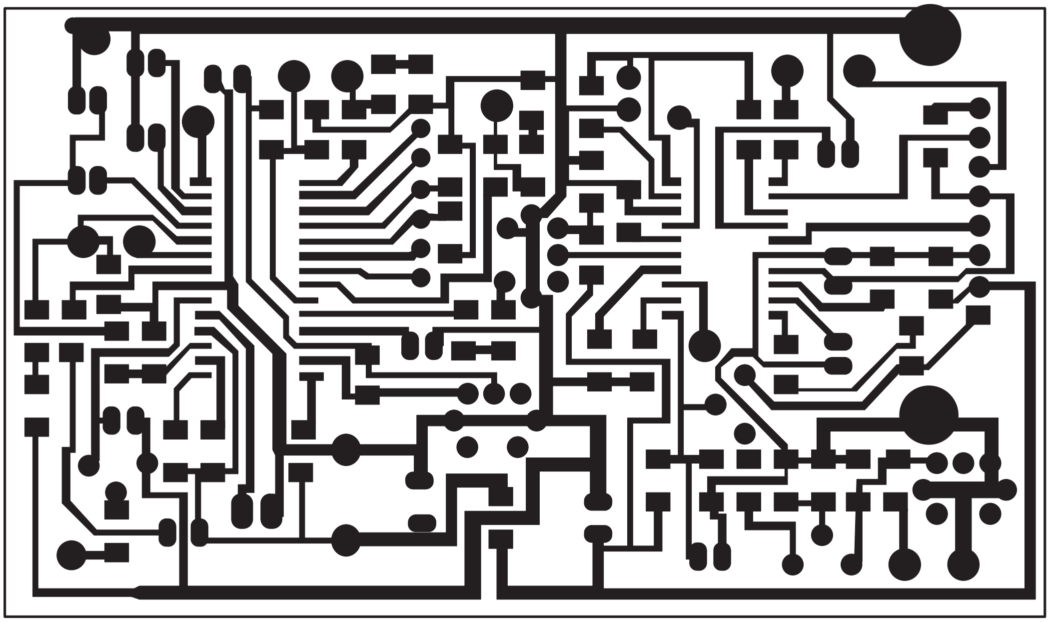


Figure 24. AMAX Chipset Printed Circuit Board

(Copper View)



MOTOROLA

MC13028A

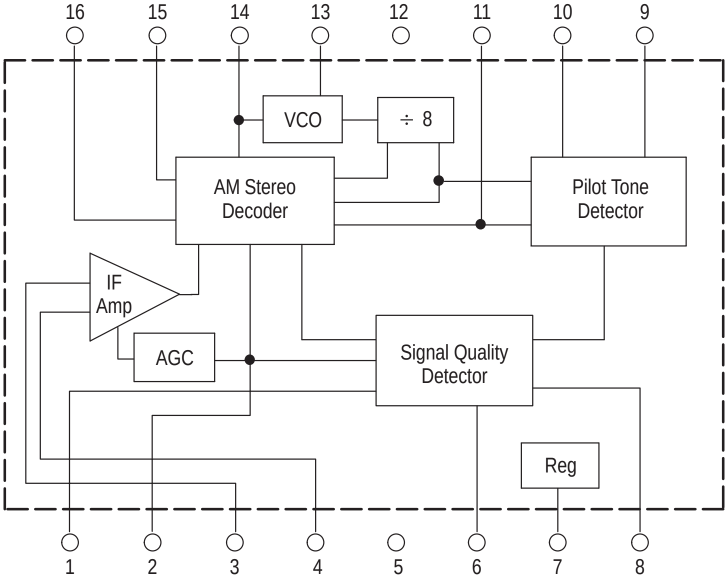
Advanced Wide Voltage IF and C-QUAM® AM Stereo Decoder

The MC13028A is a third generation C–QUAM stereo decoder targeted for use in low voltage, low cost AM/FM E.T.R. radio applications. Advanced features include a signal quality detector that analyzes signal strength, signal to noise ratio, and stereo pilot tone before switching to the stereo mode. A “blend function” much like FM stereo has been added to improve the transition from mono to stereo. The audio output level is adjustable to allow easy interface with a variety of AM/FM tuner chips. The external components have been minimized to keep the total system cost low.

- Adjustable Audio Output Level
- Stereo Blend Function
- Stereo Threshold Adjustment
- Operation from 2.2 V to 12 V Supply
- Precision Pilot Tone Detector
- Forced Mono Function
- Single Pinout VCO
- IF Amplifier with IF AGC Circuit
- VCO Shutdown Mode at Weak Signal Condition

The purchase of the Motorola C–QUAM® AM Stereo Decoder does not carry with such purchase any license by implication, estoppel or otherwise, under any patent rights of Motorola or others covering any combination of this decoder with other elements including use in a radio receiver. Upon application by an interested party, licenses are available from Motorola on its patents applicable to AM Stereo radio receivers.

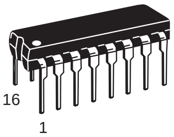
Representative Block Diagram



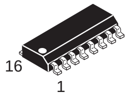
This device contains 679 active transistors.

C–QUAM AM STEREO ADVANCED WIDE VOLTAGE IF and DECODER for E.T.R. RADIOS

SEMICONDUCTOR TECHNICAL DATA

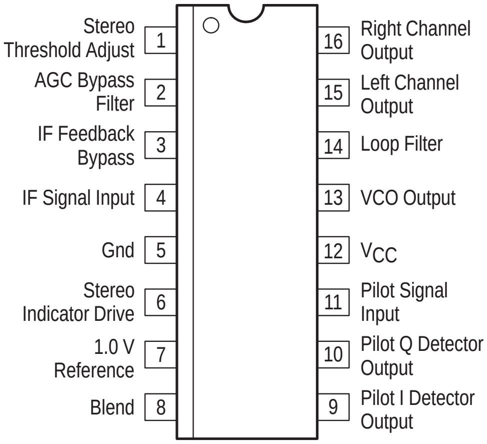


P SUFFIX
PLASTIC PACKAGE
CASE 648



D SUFFIX
PLASTIC PACKAGE
CASE 751B
(SO–16)

PIN CONNECTIONS



ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC13028AD	T_A = –25° to +70°C	SO–16
MC13028AP		DIP–16

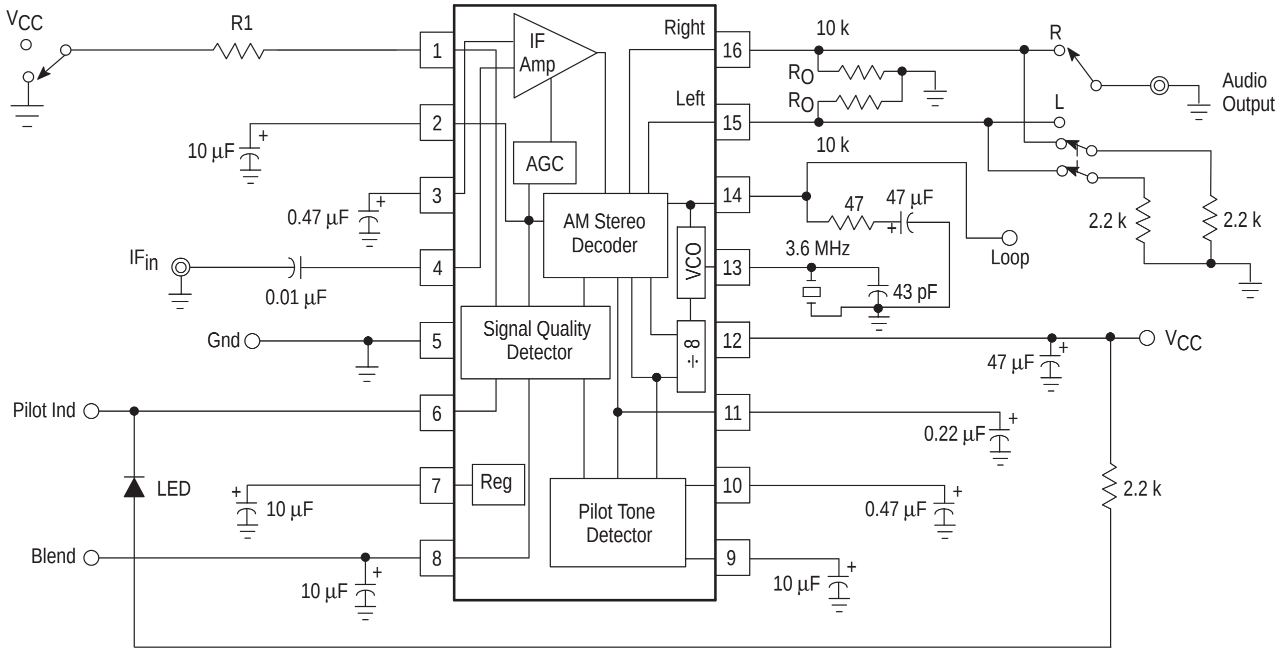
MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Input Voltage	V_{CC}	14	Vdc
Operating Junction Temperature	T_J	150	°C
Operating Ambient Temperature	T_A	–25 to +70	°C
Storage Temperature Range	T_{stg}	–55 to +150	°C
LED Indicator Current	I_{LED}	10	mA

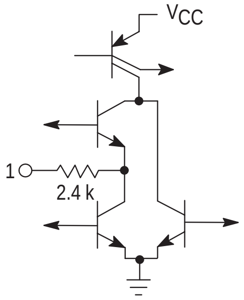
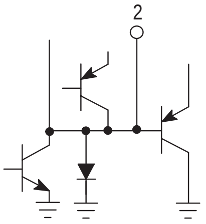
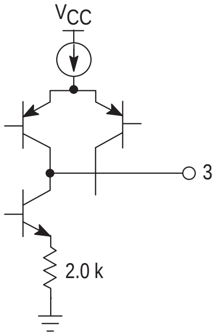
ELECTRICAL CHARACTERISTICS (V_{CC} = 8.0 Vdc, T_A = 25°C, Input Signal Level = 74 dBµV, Modulation = 1.0 kHz @ 50% Modulation, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Supply Current Drain	I_{CC}				mA
V_{CC} = 2.2 V		–	9.0	11	
V_{CC} = 8.0 V		–	11	–	
Audio Output Level, L+R, Mono Modulation	V_{out}				mVrms
R_O = 1.8 k, V_{CC} = 2.2 V, Input 55 dBµV		22	33	44	
R_O = 10 k, V_{CC} = 8.0 V, Input 50 dBµV		150	200	250	
Input 40 dBµV		80	130	180	
Input 31 dBµV		–	50	–	
Audio Output Level, L or R Only, Stereo Modulation	V_{out}				mVrms
R_O = 1.8 k, V_{CC} = 2.2 V, 55 dBµV Input		35	80	106	
R_O = 10 k, V_{CC} = 8.0 V		340	460	580	
Output THD					%
50% Stereo, L or R Only	THD1	–	0.6	1.8	
50% Mono, L+R	THD2	–	0.3	0.6	
90% Mono, L+R, Input 86 dBµV	THD3	–	–	1.5	
Channel Separation 50% L or R Only	L or R	23	35	–	dB
Decoder Input Sensitivity V_{out} = –10 dB	V_{in}	–	33	–	dBµV
Force to Mono Mode, (Pin 10)	–	0.25	0.3	–	Vdc
Stereo Threshold Adjust (Pin 1)	S_{TA}				dBµV
Pin 1 Open		–	50	55	
R1 = 15 k (Gnd)		–	55	–	
R1 = 680 k (V_{CC})		–	48	–	
Signal to Noise Ratio, R_O = 10 k	S/N				dB
50% Stereo, L or R Only		40	62	–	
50% Mono, L+R		40	59	–	
Input Impedance	R_{in}	–	10	–	kΩ
(Reference Specification)	C_{in}	–	8.0	–	pF
Maximum Input Signal Level for THD ≤ 1.5%	–	–	–	86	dBµV
Blend Voltage	Bl				Vdc
Mono Mode		0.7	–	0.9	
Stereo Mode		1.20	1.30	1.35	
Out of Lock		–	0.12	0.2	
VCO Lock Range	OSC_{tun}	–	±2.5	–	kHz
AGC Range	AGC_{rng}	–	44	–	dB
Channel Balance	C–B	–1.0	–	1.0	dB
Pilot Sensitivity	–	–	2.5	4.0	%

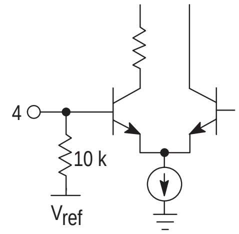
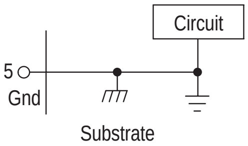
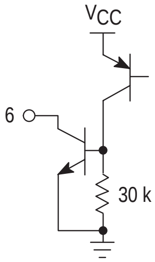
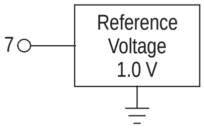
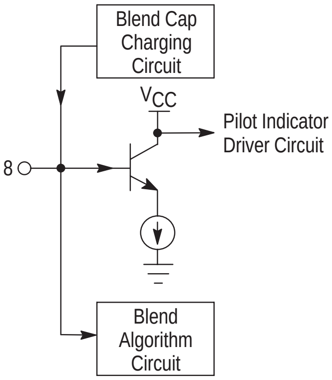
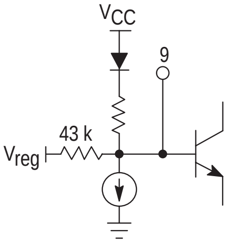
Standard Test Circuit



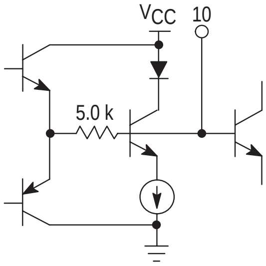
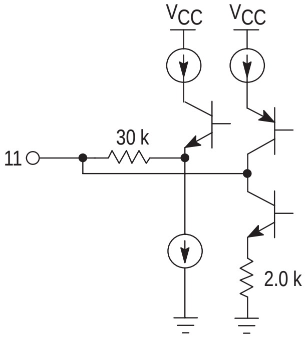
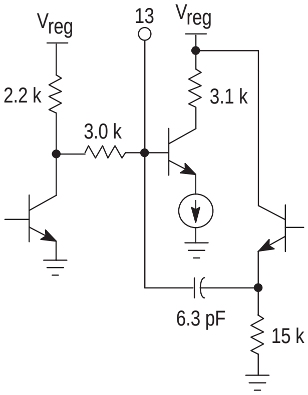
PIN FUNCTION DESCRIPTION

Pin	Symbol	Internal Equivalent Circuit	Description/External Circuit Requirements
1	S_{TA}		**Stereo Threshold Adjustment Pin** The function of this circuit is to provide the freedom to achieve a desired value of incoming IF signal level which will cause full stereo operation of the decoder. The level can be determined by the value of R1, a resistor from Pin 1 that can be connected to either V_{CC} or to ground. This resistor may also be omitted in some designs (Pin 1 left open). The approximate dc level with the pin left open is 0.6 Vdc.
2	AGC_{cap}		**AGC Filter Bypass Capacitor** An electrolytic capacitor is used as a bypass filter and it sets the time constant for the AGC circuit action. The recommended capacitor value is 10 µF from Pin 2 to ground. The dc level at this pin varies as shown in the curve in Figure 13, AGC Voltage versus Input Level.
3	IF_{FBcap}		**IF Amplifier Feedback Capacitor** A capacitor which is specified to have a low ESR at 450 kHz is normally used at Pin 3. The value recommended for this capacitor is 0.47 µF from Pin 3 to ground. This component forms a low pass filter which has a corner frequency around 30 kHz.

PIN FUNCTION DESCRIPTION

Pin	Symbol	Internal Equivalent Circuit	Description/External Circuit Requirements
4	IF_{in}		**IF Amplifier Input** Pin 4 is the IF input pin. The typical input impedance at this pin is 10 k. The input should be ac coupled through a 0.01 µF capacitor.
5	Gnd		**Supply Ground** In the PCB layout, the ground pin should be connected to the chassis ground directly. This pin is the internal circuit ground and the silicon substrate ground.
6	S_{IND}		**Stereo Indicator Driver** This driver circuit is intended to light an LED or other indicator when the decoder receives the proper input signals and switches into the stereo mode. The maximum amount of current that the circuit can sink is 10 mA. A current limiting resistor is applied externally to control LED brightness versus total power supply current.
7	V_{Ref}		**Regulated Voltage, 1.0 V** An electrolytic capacitor used as a bypass filter is recommended from Pin 7 to ground. The capacitor value should be 10 µF.
8	CAP_{Blend}		**Blend Capacitor** The value of the capacitor on this pin will effect the time constant of the decoder blend function. The recommended value is 10 µF from Pin 8 to ground. The dc level at Pin 8 is internally generated in response to input signal level and signal quality. This pin is a key indicator of the operational state of the IC (see text Functional Description). It is recommended to discharge the blend capacitor externally when changing stations.
9	I_{Pilot}		**Pilot I Detector Output** The Pilot I Detector output requires a 10 µF electrolytic capacitor to ground. The value of this capacitor sets the pilot acquisition time. The dc level at Pin 9 is approximately 1.0 Vdc, unlocked, and 1.1 to 2.4 Vdc in the locked condition.

PIN FUNCTION DESCRIPTION

Pin	Symbol	Internal Equivalent Circuit	Description/External Circuit Requirements
10	Q_{Pilot}		**Pilot Q Detector Output** This pin is connected to the Pilot Q detector and requires a 0.47 µF capacitor to ground to filter the error line voltage at the PLL pilot tone detector. If the value of this capacitor is made too large, the decoder may be prevented from coming back into stereo after a signal drop out has been experienced in the field. The force to mono function is also accomplished at this pin by pulling the dc voltage level at the pin below 1.0 V.
11	$PILOT_{fil}$		**Pilot Signal Input** A capacitor to ground forms a filter for the pilot input signal. The recommended value of the capacitor is 0.22 µF. The dc level at Pin 11 is approximately 1.0 Vdc.
12	V_{CC}		**Supply Voltage (V_{CC})** The operating supply voltage range is from 1.8 Vdc to 12 Vdc.
13	OSC_{in}		**Oscillator Input** The oscillator pin requires a ceramic resonator and parallel capacitor connected to ground. The recommended source for the ceramic resonator is Murata, part number CSA 3.60MGF108. A 43 pF NPO capacitor is in parallel with the resonator. The dc level at Pin 13 is approximately 1.1 Vdc.

PIN FUNCTION DESCRIPTION

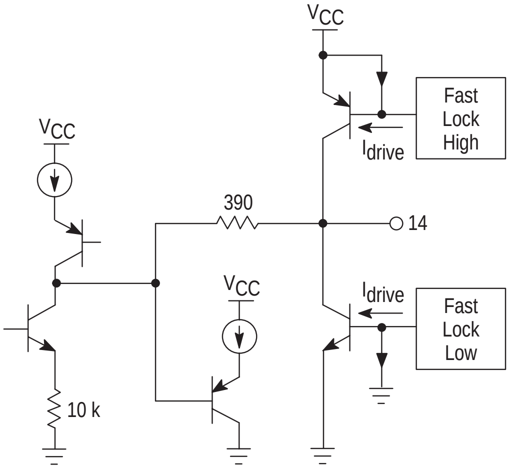
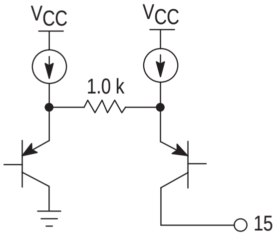
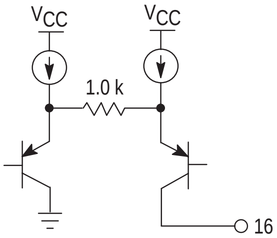
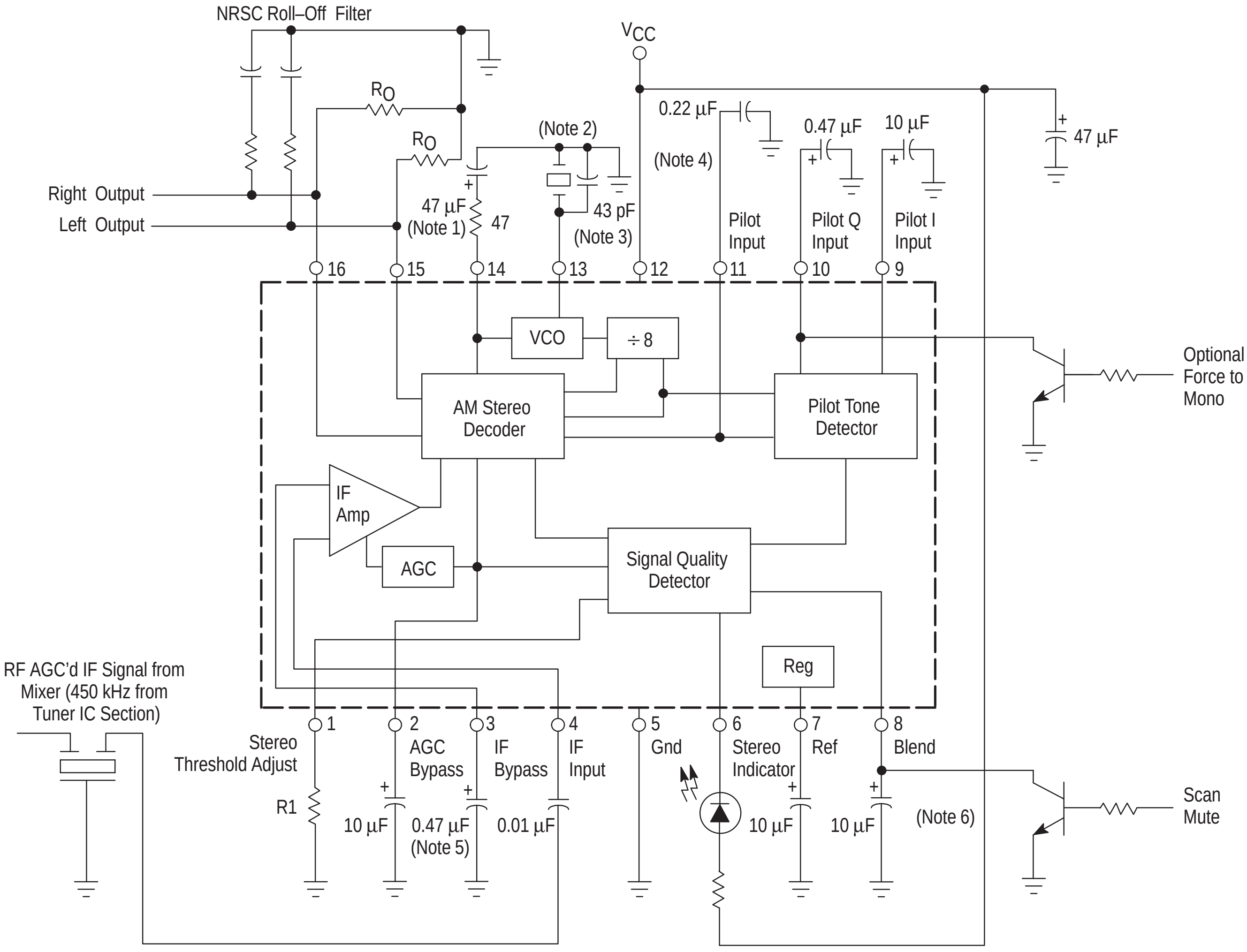
Pin	Symbol	Internal Equivalent Circuit	Description/External Circuit Requirements
14	$LOOP_{Filter}$		**Loop Filter** A capacitor which forms the loop filter is connected from Pin 14 to ground. The recommended value is 47 µF in series with 47 Ω. This capacitor should be of good construction quality so it will have a very low specification for leakage current in order to prevent stereo distortion. The 47 Ω resistor in series with the capacitor controls the PLL corner frequency response, keeping the response shape critically damped and not peaked up. The dc level at Pin 14 is approximately 0.6 Vdc in the locked condition.
15	$LEFT_{out}$		**Left Channel Audio Output** This is the left channel audio output pin from which the IC can provide 1.3 μA_{pp} drive current for each percent of mono modulation. A resistor to ground sets the level of the audio output. For example, *100%* (mono mod) x 1.3 μA_{pp} (IC drive per % mod) = 130 μA_{pp} flowing through the load resistor. (For a 2.2 k load, 286 mV_{pp} is then the output signal voltage.) When dealing with stereo signals, multiply the mod level by 2; i.e. *50%* (left only mod) x 2 (stereo factor) x 1.3 μA_{pp} (IC drive per % mod) = 130 μA_{pp} flowing through the load resistor.
16	$RIGHT_{out}$		**Right Channel Audio Output** This is the right channel audio output pin. A resistor to ground sets the level of the audio output. See the explanation under the Left Channel Audio Output description above.

Figure 1. Typical Circuit for E.T.R. Applications



NOTES:
1. The 47 µF capacitor is recommended to be a low leakage type capacitor. Leakage current due to this capacitor causes increase in stereo distortion and decreased separation performance.
2. The recommended source for this part is Murata Products. CSA3.60MGF108. The location of this part should be carefully considered during the layout of the decoder circuit. This part should not be near the audio signal paths, the 25 Hz pilot filter lines, or the V_{CC} high current lines, and the ceramic element ground line should be direct to the chassis ground lead in order to avoid any oscillator inter–modulation.
3. The 43 pF capacitor is recommended to be a NPO type ceramic part. Changing the value of this capacitor alters the lock range of the decoder PLL.
4. The tolerance on the value of the 0.22 µF capacitor should be within ±20% for the full design temperature range of operation. Any reduction in the value of this capacitor due to temperature excursions will reduce the pilot tone circuit sensitivity.
5. The 0.47 µF capacitor is recommended to be a low ESR type capacitor, (less than 1.5 Ω) in order to avoid increased audio output distortions under weak input signal conditions with higher modulation levels.
6. The scan/mute function is located on the Blend pin at Pin 8. To provide this function, Pin 8 should be pulled down below 0.3 V until the decoder and the synthesizer have both locked to a new station.

FUNCTIONAL DESCRIPTION

Introduction

The MC13028A is designed as a low voltage, low cost decoder for the C–QUAM AM Stereo technology and is completely compatible with existing monaural AM transmissions. The IC requires relatively few, inexpensive external parts to produce a full featured C–QUAM AM Stereo implementation. The layout is straightforward and should produce excellent stereo performance. This device performs the function of IF amplification, AGC, modulation detection, pilot tone detection, signal quality inspection, and left and right audio output matrix operation. The IC is targeted for use in portable and home AM Stereo radio applications.

A simple overview follows which traces the path of the input signal information to the MC13028A all the way to the audio output pins of the decoder IC.

From the appropriate pin of an AM IC, the IF amplifier circuit of the MC13028A receives its input at Pin 4 as a 450 kHz, typically modulated C–QUAM signal. The input signal level for stereo operation can vary from 47 dBμV to about 90 dBμV. A specific threshold level between these limits can be designed into a receiver by the choice of the resistor value for R1 connected to Pin 1. This IC design incorporates feedback in the IF circuit section which provides excellent dc balance in the IF amplifier. This balanced condition also guarantees excellent monophonic performance from the decoder. An IF feedback filter at Pin 3 is formed by a 0.47 μF low leakage capacitor. It is used to filter out the unwanted audio which is present on the IF amplifier feedback line at higher modulation levels under weak input RF signal conditions. Elimination of the unwanted signal helps to decrease the amount of distortion in the audio output of the stereo decoder under these particular input conditions. An AGC circuit controls the level of IF signal which is subsequently fed to the detector circuits. An AGC bypass capacitor is connected to Pin 2 and forms a single pole low pass filter. The value of this part also sets the time constant for the AGC circuit action.

The amplified C–QUAM IF signal is fed simultaneously to the envelope detector circuit, and to a C–QUAM converter circuit. The envelope detector provides the L+R (mono) signal output which is fed to the stereo matrix. In the converter circuit, the C–QUAM signal is restored to a Quam signal. This is accomplished by dividing the C–QUAM IF signal by the demodulated cos ϕ term. The cos ϕ term is derived from the phase modulated IF signal in an active feedback loop. Cosine ϕ is detected by comparing the envelope detector and the in–phase detector outputs in the high speed comparator/feedback loop. Cosine ϕ is extracted from the I detector output and is actively transferred through feedback to the output of the comparator. The output of the comparator is in turn fed to the control input of the divider, thus closing the feedback loop of the converter circuit. In this process, the cos ϕ term is removed from the divider IF output, thus allowing direct detection of the L–R by the quadrature detector. The audio outputs from both the envelope and the L–R detectors are first filtered to minimize the second harmonic of the IF signal. Then they are fed into a matrix circuit where the Left channel and the Right channel outputs can be extracted at Pins 15 and 16. (The outputs from the I and Q detectors are also filtered similarly.) At this time, a stereo indicator driver circuit, which can sink up to 10 mA, is also enabled. The stereo output will occur if the input IF signal is: larger than the stereo threshold level, not too noisy, and if a proper pilot tone is present. If these three conditions are not met, the blend circuit will begin to force monaural operation at that time.

A blend circuit is included in this design because conditions occur during field use that can cause input signal strength fluctuation, strong unwanted co–channel or power line interference, and/or multi–path or re–radiation. When these aberrant conditions occur, rapid switching between stereo and mono might occur, or the stereo quality might be degraded enough to sound displeasing. Since these conditions could be annoying to the normal listener, the stereo information is blended towards a monaural output. This circuit action creates a condition for listening where these aberrant effects are better tolerated by the consumer.

Intentional mono operation is a feature sometimes required in receiver designs. There are several ways in which to accomplish this feat. First, a resistor from Pin 10 to ground can be switched into the circuit. A value of 1.0 k is adequate as is shown in the schematic in Figure 18. A second method to force the decoder into mono is simply to shunt Pin 10 to ground through an NPN transistor (collector to Pin 10, emitter to ground), where the base lead is held electrically “high” to initiate the action.

A third method to force a mono condition upon the decoder is to shunt Pin 8 of the decoder to ground through an NPN transistor as described above. Effectively, this operation discharges the blend capacitor (10 μF), and the blend function takes over internally forcing the decoder into mono. This third method does not necessarily require extra specific parts for the forced mono function as the first two examples do. The reason for this is that most electronically tuned receiver designs require an audio muting function during turn on/turn off, tuning/scanning, or band switching (FM to AM). When the muting function is designed into an AM Stereo receiver, it also should include a blend capacitor reset (discharge) function which is accomplished in this case by the use of an NPN transistor shunting Pin 8 to ground, (thus making the addition of a forced mono function almost “free”). The purpose of the blend reset during muting is to re–initialize the decoder back into the “fast lock” mode from which stereo operation can be attained much quicker after any of the interruptive activities mentioned earlier, (i.e. turn on, tuning, etc.).

The VCO in this IC is a phase shift oscillator type design that operates with a ceramic resonator at eight times the IF frequency, or 3.60 MHz. With IF input levels below the stereo threshold level, the oscillator is not operational. This feature helps to eliminate audio tweets under low level, noisy input conditions.

The phase locked loop (PLL) in the MC13028A is locked to the L–R signal. This insures good stereo distortion performance at the higher levels of left only or right only modulations. Under normal operating conditions, the PLL remains locked because of the current flow capability of the loop driver circuit. This high gain, high impedance circuit performs optimally when the current flow is balanced. The balanced condition is enhanced by the loop driver filter circuit connected between Pin 14 and ground. The filter circuit consists of a 47 Ω resistor in series with a 47 μF capacitor. The 47 Ω resistor is to set the Fast Lock rate. It is recommended that the capacitor be a very low leakage type electrolytic, or a tantalum composition part because any significant amount of leakage current flowing through the capacitor will unbalance the loop driver circuit and result in less than optimum stereo performance, see Figures 10 and 11.

The pilot tone detector circuit is fed internally from the Q detector output signal. The circuit input employs a low pass filter at Pin 11 that is designed to prevent the pilot tone detector input from being overloaded by higher levels of L–R modulation. The filter is formed by a 0.22 μF capacitor and the input impedance of the first amplifier. A pilot I detector circuit employs a capacitor to ground at Pin 9 to operate in conjunction with an internal resistor to create an RC integration time. The value of the capacitor determines the amount of time required to produce a stereo indication. This amount must include the time it takes to check for the presence of detector falsing due to noise or interference, station retuning by the customer, and pilot dropout in the presence of heavy interference. The pilot Q detector utilizes a filter on its pilot tone PLL error line at Pin 10. This capacitor to ground (usually 0.47 μF) is present to filter any low frequency L–R information that may be present on the error line. If the value of this capacitor is allowed to be too small, L–R modulation ripple on the error line may get large enough to cause stereo dropout. If the capacitor value is made too large, the pilot tone may be prevented from being reacquired if it is somehow lost due to fluctuating field conditions.

A 1.0 V reference level is created internally from the V_{CC} source to the IC. This regulated line is used extensively by circuits throughout the MC13028A design. An electrolytic capacitor from Pin 7 to ground is used as a filter for the reference voltage.

DISCUSSION OF GRAPHS AND FIGURES

If the general recommendations put forth in this application guide are followed, excellent stereo performance should result.

The curves in Figures 2 through 7 depict the separation and the distortion performance in stereo for 30%, 50%, and 65% single channel modulations respectively. The data for these figures were collected under the conditions of V_{CC} = 8.0 V and R_O = 10 k in both the left and the right channels as applied to the application circuit of Figure 1. A very precise laboratory generator was used to produce the AM Stereo test signal of 450 kHz at 70 dBμV fed to Pin 4. An NRSC post detection filter was not present at the time of these measurements. The audio separation shows an average performance at 30% and 50% modulations of –45 dB in the frequency range of 2.0 kHz to 5.0 kHz. The corresponding audio distortions under these conditions are about 0.28% at 30% modulation, and about 0.41% at 50% modulation.

Figure 6 shows that the typical separation at 65% modulation in the 2.0 kHz to 5.0 kHz region is about –37 dB, and the corresponding audio distortion shown in Figure 7 is about 1.0%. The performance level of these sinusoidal signals is somewhat less than those discussed in the previous paragraph due to the internal operation of the clamping circuits. In the field, the transmitters at AM Stereo radio stations are not usually permitted to modulate single channel levels past 70%. Therefore these conditions do not occur very often during normal broadcast material.

The roll–off at both the low and high frequencies of the 30% single channel driven responses is due to the fact that a post detection bandpass filter of 60 Hz to 10 kHz was used in the measurement of the data, while a post detection filter of 2.0 Hz to 20 kHz was used for the collection of data in the 50% and 65% modulation examples. The tighter bandwidth was used while collecting the performance data at 30% modulation levels in order to assure that the distortion measurement was indicative of the true distortion products measured near the noise floor and thus not encumbered by residual noise and hum levels which would erroneously add to the magnitude of the harmonic distortion data. Note in Figure 8 the traces of noise response for the four different bandwidths of post detection filtering. It can be seen that the noise floors improve steadily with increasing levels of incoming 450 kHz as the value of the lower corner frequency of the filter is increased. Data for the stereo noise floors was collected with the decoder in the forced stereo mode.

Figure 2. Single Channel Separation at 30% Modulation

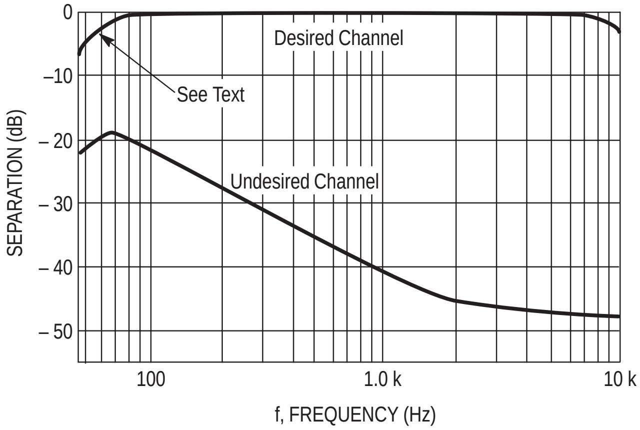


Figure 3. Single Channel Distortion at 30% Modulation

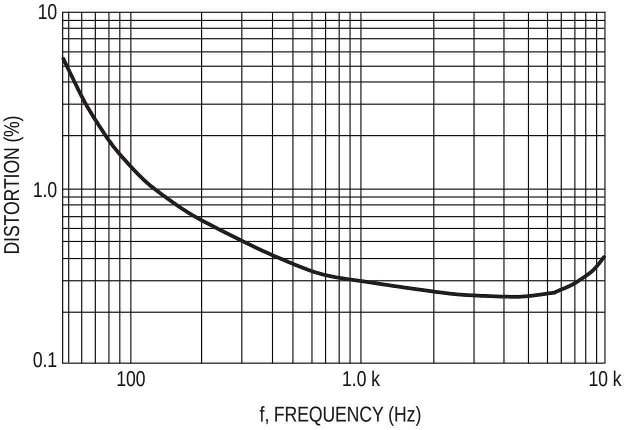


Figure 4. Single Channel Separation at 50% Modulation

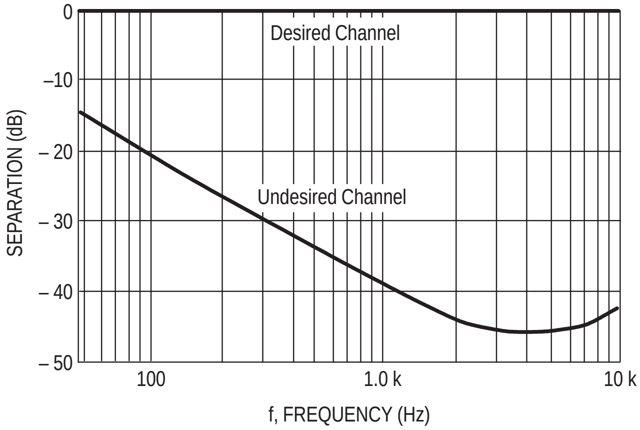


Figure 5. Single Channel Distortion at 50% Modulation

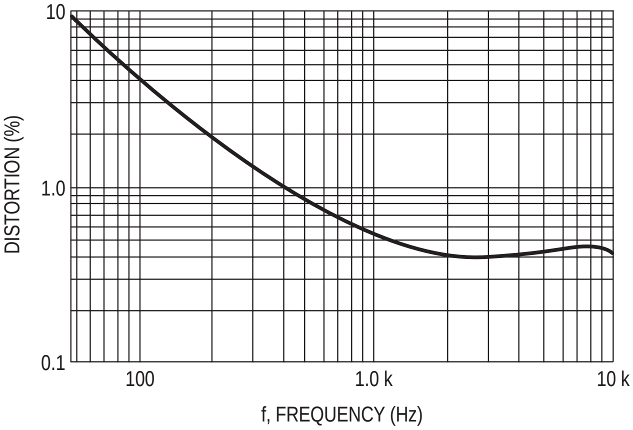


Figure 6. Single Channel Separation at 65% Modulation

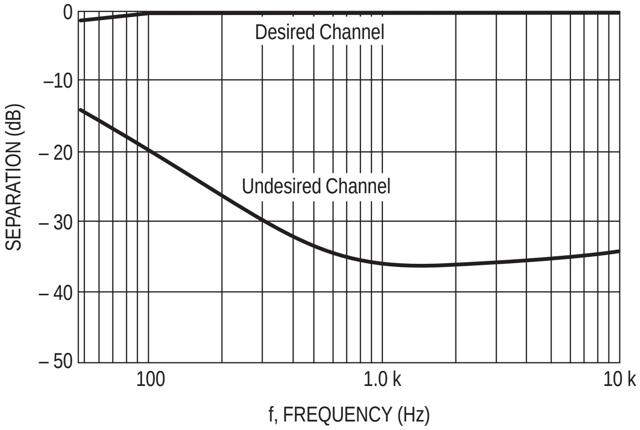


Figure 7. Single Channel Distortion at 65% Modulation

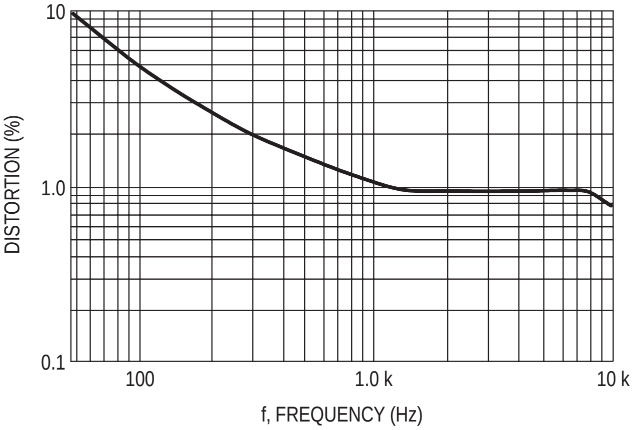


Figure 8. Stereo Noise and Stereo Composite Distortion when Mono Transmitted

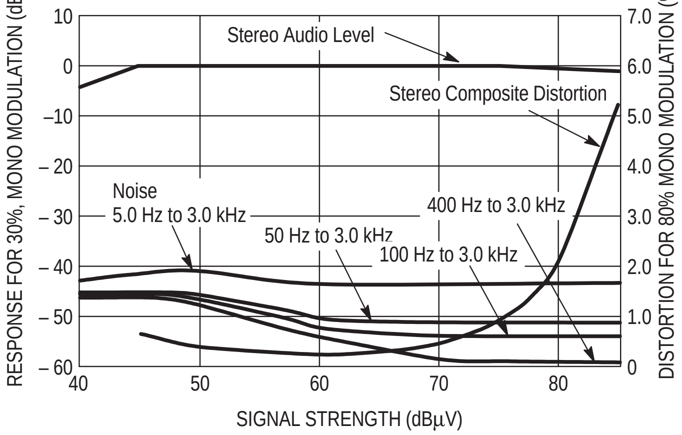


Figure 9. R1 versus Stereo Threshold Point

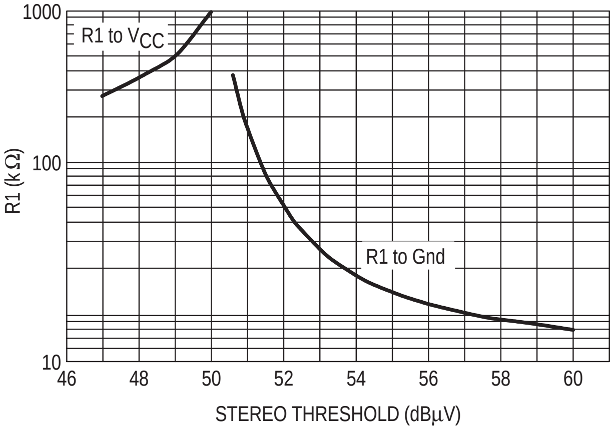


Figure 10. Decoder Separation versus Filter Capacitor (Pin 14) Leakage Current

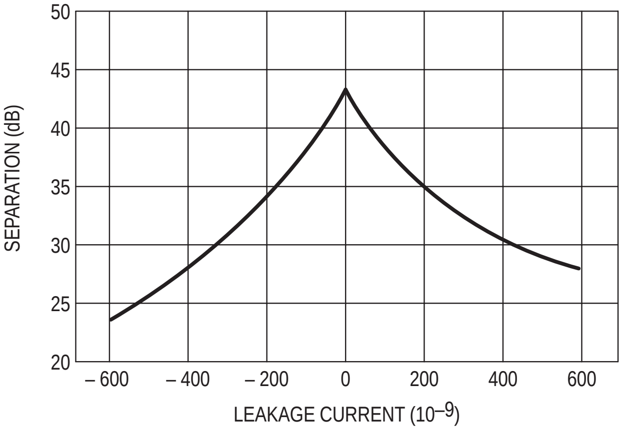


Figure 11. Decoder Distortion versus Filter Capacitor (Pin 14) Leakage Current

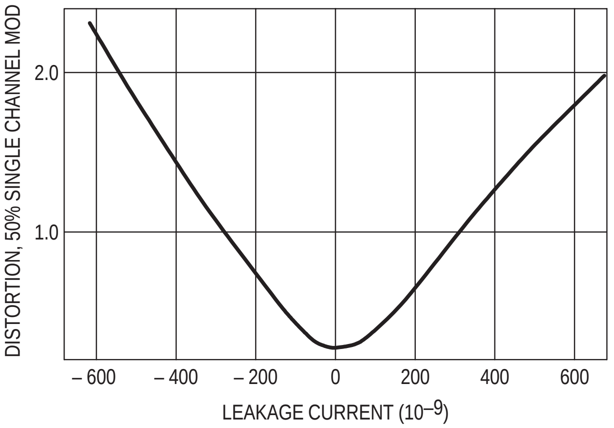


Figure 12. Low Frequency Corner of PLL Response

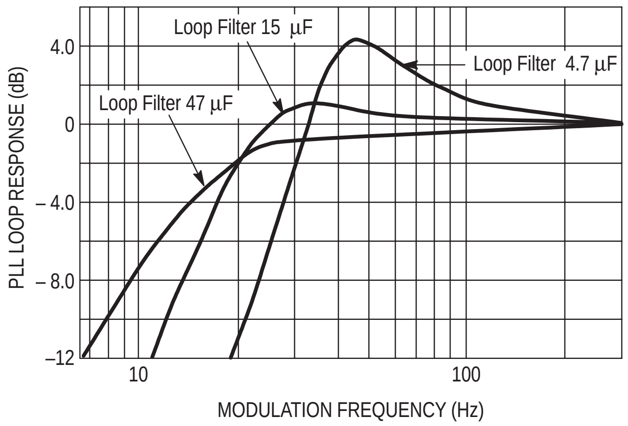


Figure 13. AGC Voltage versus Input Signal Level

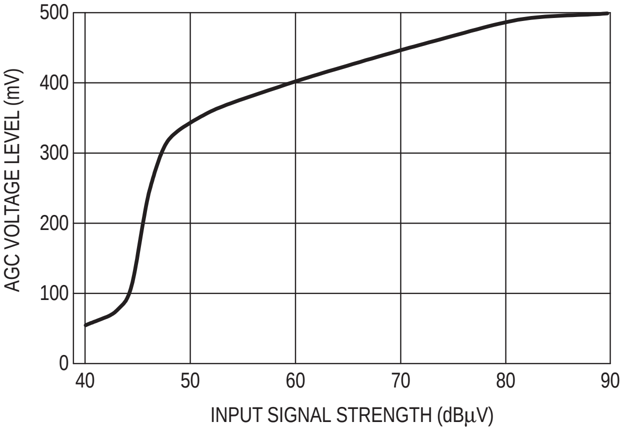


Figure 9 presents more detailed information with respect to the value of resistor R1 at Pin 1 versus the desired incoming signal level for stereo threshold.

Figures 10 and 11, discussed briefly in the Pin Function Description Section, show the importance of using a quality component at Pin 14 to ground. It can be seen that an electrolytic capacitor leakage current of 600 nA can unbalance the PLL to the point where stereo performance may degrade to only 25 dB of separation with a corresponding 2.0% distortion at 50% modulation levels.

The value of the capacitor connected to Pin 14 (47 µF) is also a factor in the determination of the low frequency corner of the PLL circuit response. Three traces of PLL response appear in Figure 12 where they have been plotted for three different values of loop filter capacitor. The recommended value of 47 µF provides the best response shape in this particular circuit set–up where a Murata Products CSA3.60MGF108 part is used.

Figure 13 presents the response of the AGC voltage versus decoder input signal level. This is a typical response when the IC is used as shown in the application schematic of Figure 1. The trace begins approximately at the point of decoder sensitivity, and rises rapidly until reaching the area of stereo sensitivity, approximately 50 dBµV. Thereafter, the circuit responds in a linear fashion for the next 30 dB of input signal increase.

Figures 14 through 17 inclusively depict the V_{CC} ripple rejection performance for the MC13028A under mono and stereo conditions for nominal and for low values of V_{CC}. It should be noted that this data was collected without any V_{CC} filtering. As one might expect, the ripple rejection is better in mono than in stereo. When the decoder operates in stereo, the VCO is functional, thus the decoder becomes more susceptible to audio ripple on the V_{CC} line. Under normal operating conditions, with the recommended value of 47 µF at Pin 12 and 10 µF at Pin 7, a V_{CC} ripple reading will be virtually the same as measuring the noise floor of the IC.

AM STEREO TUNER / FM STEREO IF

Description of Application

This application combines a Sanyo LA1832M with the Motorola MC13028A AM Stereo decoder IC. The LA1832 provides an FM IF, FM multiplex detection, AM tuning, and the AM IF functions. The MC13028A provides the AM Stereo detection as well as Left and Right audio outputs. An MC145151 synthesizer provides the frequency control of the local oscillator contained within the LA1832. Frequency selection is by means of a switch array attached to the synthesizer. The application circuit is shown in Figure 18.

Circuit Board Description

The copper side layout and the component locations are shown in Figure 19. The view is from the plating side of the board, with the components shown in hidden view. Several jumper wires are placed on the component side of the board to complete the circuit. Posts are provided for electrical connections to the circuit. The circuit board has been scaled to fit the page, however, the dimensions provide the true size.

Circuit Description

The Sanyo data sheet for the LA1832 should be consulted for an understanding of the FM detection and multiplex decoding.

Special Parts

The following information provides circuit function, part number, and the manufacturer’s name for special parts identified by their schematic symbol. Where the part is not limited to a single source, a description sufficient to select a part is given.

U1	IC – AM Stereo Decoder MC13028AD by Motorola
U2	IC – AM/FM IF and Multiplex Tuner LA1832M by Sanyo
U3	IC – Frequency Synthesizer MC145151DW2 by Motorola
T1	AM IF Coil A7NRES–11148N by TOKO
F1	AM IF Ceramic Filter SFG450F by Murata
F2	FM IF Detector Resonator CDA10.7MG46A by Murata
F3	FM Multiplex Decoder Resonator CSB456F15 by Murata
F4	AM Tuner Block BL–70 by Korin Giken
X1	10.24 MHz Crystal, Fundamental Mode, AT Cut, 18 pF Load Cap, 35 Ω maximum series R. HC–18/U Holder
X2	3.6 MHz AM Stereo Decoder Resonator CSA3.60MGF108 by Murata
S5	8 SPST DIP Switch

Figure 14. Mono V_{CC} Ripple Rejection

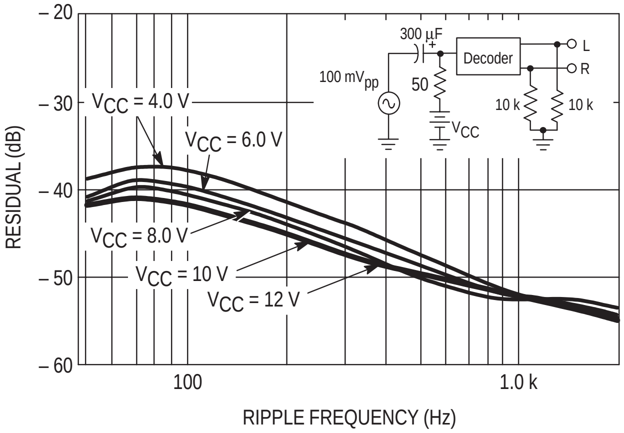


Figure 15. Mono Low Voltage V_{CC} Ripple Rejection

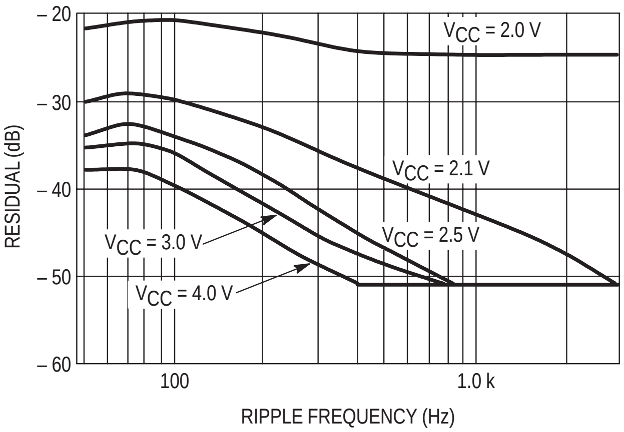


Figure 16. Stereo V_{CC} Ripple Rejection

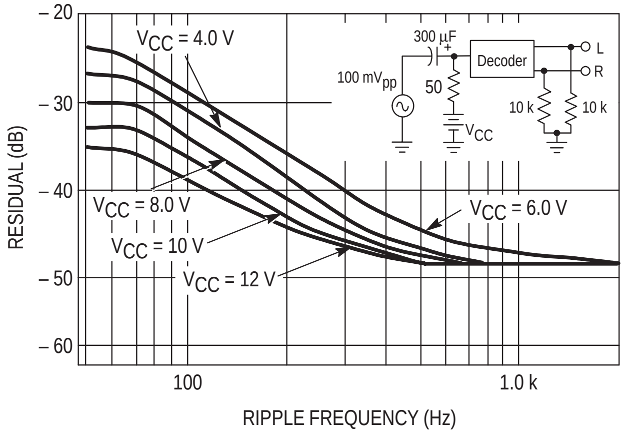


Figure 17. Stereo Low Voltage V_{CC} Ripple Rejection

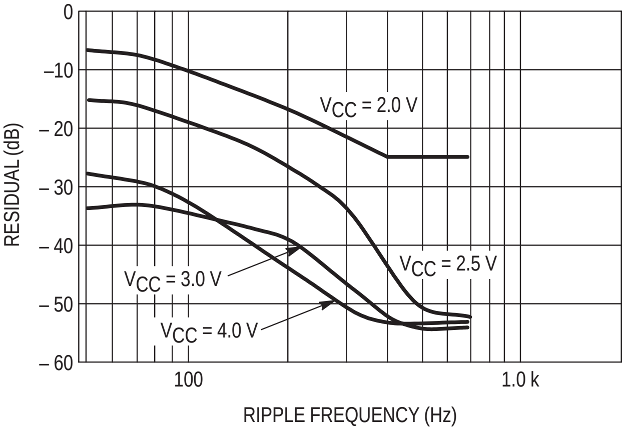


Figure 18. MC13028A Decoder IC Application

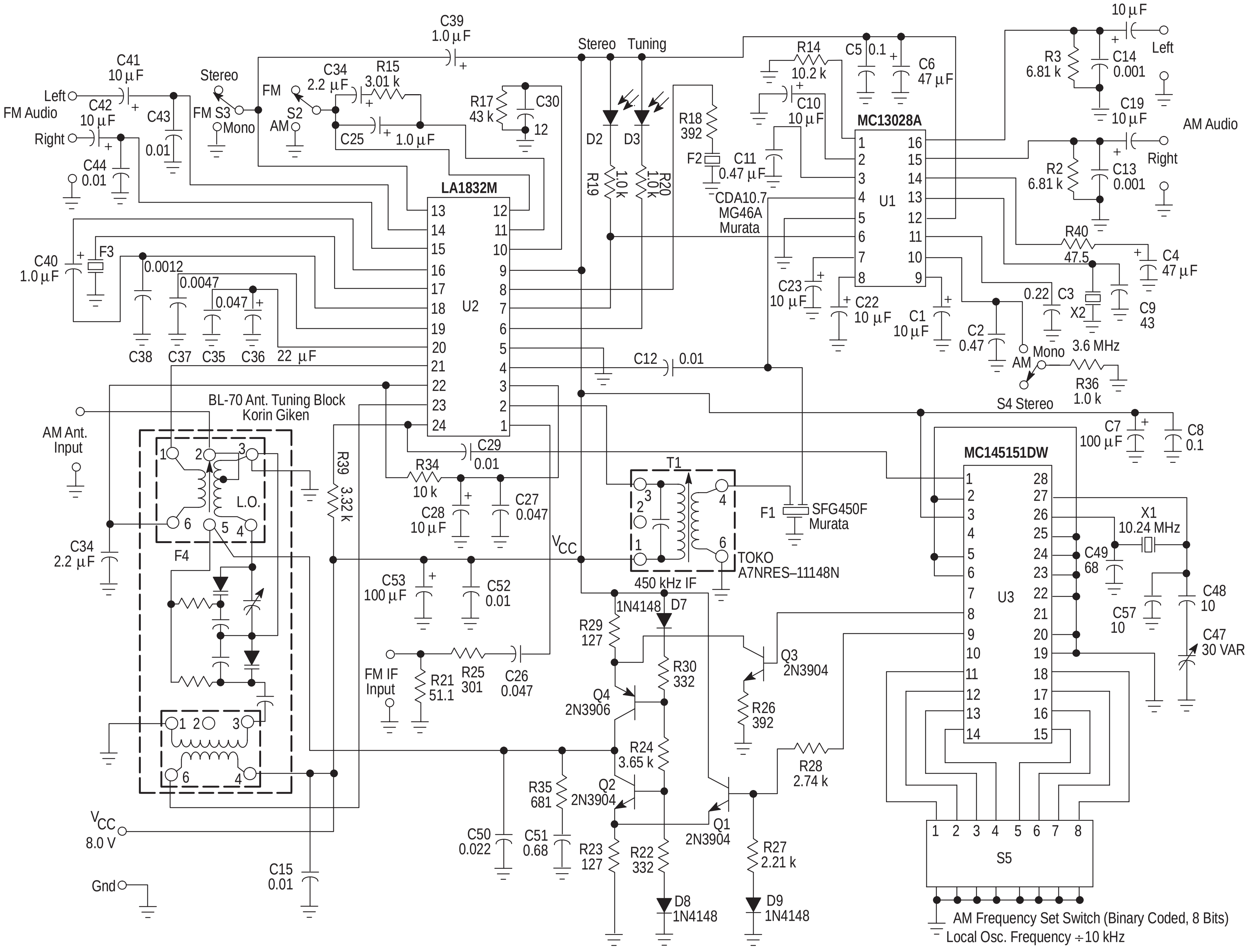
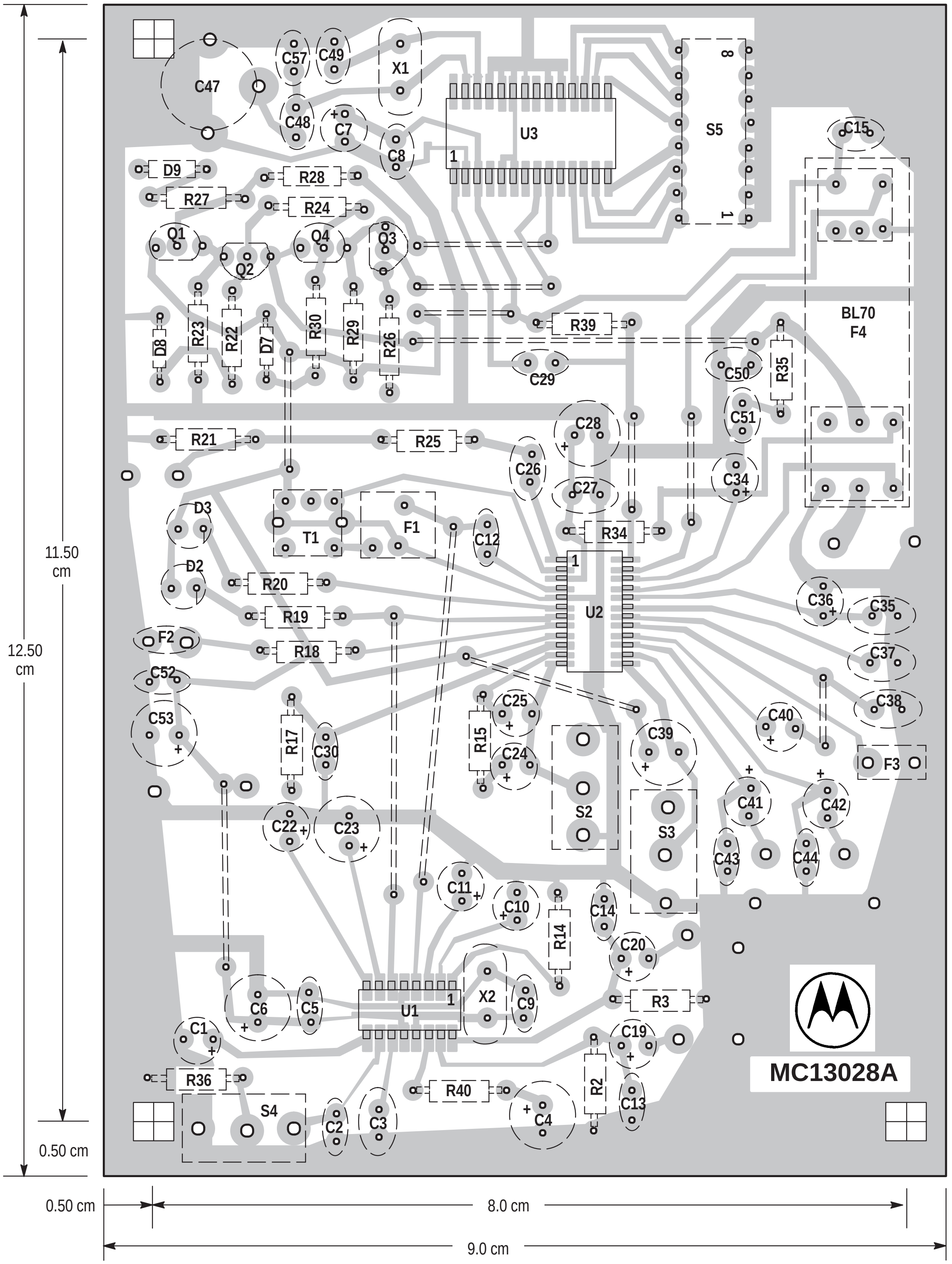


Figure 19. MC13028A Decoder IC Application Circuit Board



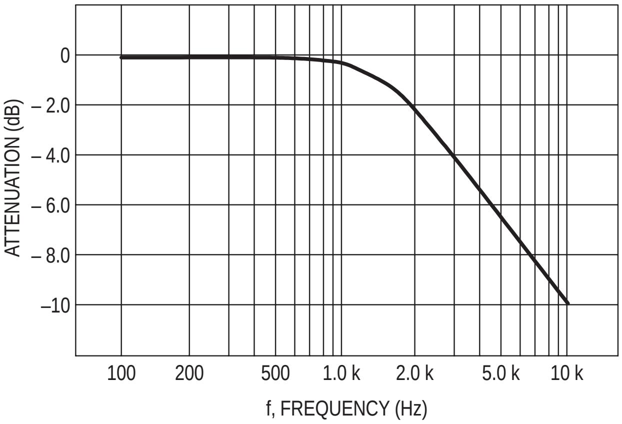
The LA1832 tuner IC (U2) is set for AM operation by switch S2 connecting Pin 12 to ground. An AM Stereo signal source is applied to Pin 2 of the RF coil contained within the BL–70 tuning block. That coil applies the signal to Pin 21 of U2. The L.O. coil is connected from Pin 23 to V_{CC}. The secondary is tuned by a varactor which is controlled by a dc voltage output from the synthesizer circuit. The reactance of this oscillator tank is coupled back to Pin 23. It is through this reactance that the frequency of the L.O. is determined. A buffered output from the L.O. emerges at Pin 24. This signal is routed to Pin 1 of the synthesizer (U3), thus completing the frequency control loop.

The mixer output at Pin 2 is applied to the IF coil T1. Coil T1 provides the correct impedance to drive the ceramic bandpass filter F1. The IF signal returns to U2 through Pin 4, and also to the input, Pin 4 of the AM Stereo decoder (U1). The ceramic filter F1 is designed to operate into a load resistance of 2.0 kΩ. This load is provided at Pin 4 of U2.

The stereo outputs exit from Pins 15 and 16 of U1. The design amplitudes of the audio outputs will vary according to the values used for the resistors to ground at Pins 15 and 16 of the decoder, (labeled R_O in the Electrical Characteristics Table and the Test Circuit on page 2 and 3, and in Figure 1, and called R2 and R3 in Figure 18). While the values chosen for R_O are left to the discretion of the designer, the numbers chosen in this data sheet are reflective of those required to set the general industry standard levels of audio outputs in receiver designs.

Pins 15 and 16 are also good locations for the insertion of simple RC filters that are used to comply with the United States NRSC requirement for the shape of the overall receiver audio response. The following curve, Figure 20, shows the response of this U.S. standard.

Figure 20. NRSC De–Emphasis Curve for the United States



There are many design factors that affect the shape of the receiver response, and they must all be considered when trying to approximate the NRSC de–emphasis response. The mixer output transformer (IF coil, T1), and ceramic filter probably have the greatest contribution to the frequency response. The ceramic filter can be tailored from its rated response by the choice of transformer impedance and bandwidth. When designing an overall audio response shape, the response of the speakers or earphones should also be considered.

Component Values.

The Pin Function Description table gives specific information on the choice of components to be used at each pin of U1. A similar section in the Sanyo LA1832 data sheet should be consulted as to the components to be used with U2.

Tuning

The frequency to which the test circuit will tune is set by the eight binary switches contained in the S5 assembly, numbered from 1 to 8. Number 1 connects to Pin 11 of U3 and number 8 connects to Pin 18. The other switches connect to the pins in between and in order. Each individual switch is a SPST type.

To tune to a specific RF frequency, a computation must be made in order to ascertain the divide ratio to input to the synthesizer via the switch array. The divide ratio is simply the eight digit binary equivalent number for the local oscillator frequency divided by 10 kHz. The local oscillator frequency is the desired RF frequency plus 450 kHz, the IF frequency. Any local oscillator value within the AM band can be represented by a binary number. Each binary bit represents a switch setting where a “1” is an open switch and a “0” is a closed switch. The most significant bit represents switch 8 which is connected to Pin 18.

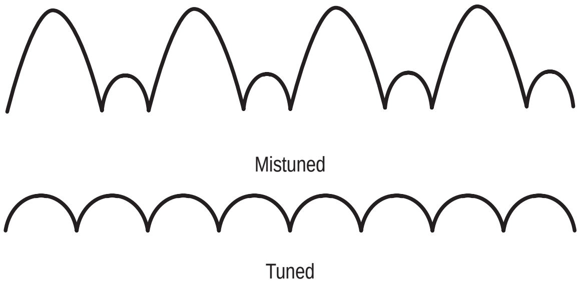
To illustrate, consider the setting for an input frequency of 1070 kHz. (This frequency was used to test the circuit board as described further on.) The local oscillator frequency is 1070 kHz plus 450 kHz which equals 1520 kHz. Dividing by 10 kHz yields the number 152. The binary number for 152 is 10011000. Thus the switches are set to:

Switch	Position	Number
8	Open	1
7	Closed	0
6	Closed	0
5	Open	1
4	Open	1
3	Closed	0
2	Closed	0
1	Closed	0

Circuit Adjustments

The FM circuit requires no adjustment. The AM L.O. must be able to tune from 980 to 2150 kHz to cover the broadcast range. Adjust the core of the L.O. coil if needed in order to be able to cover this range. The AM RF coil and trimmer can be adjusted for best signal after connection to the loop antenna. The coil is adjusted near the low end of the band, and the trimmer is adjusted at the top of the band. The IF coil, T1, is first adjusted for maximum signal out of the filter, F1. This is a “coarse” adjustment. The final “fine tune” adjustment occurs after the following conditions are met. From an AM Stereo generator with the pilot tone off, feed the decoder an input signal of approximately 70 dBμV that is modulated with an 80% L–R audio signal at 3.0 kHz. While monitoring either the left or the right output from the decoder on an oscilloscope, precisely fine tune the IF coil for a minimum residual signal, see the following diagram. If there is no sideband tilt in the system, this adjustment should hold for both channels. Otherwise, the best compromise adjustment for both channels should be used.

Figure 21. Decoder Signal Output for Mistuned and Tuned Condition with Input Signal of 80% L–R at 3.0 kHz



AM Circuit Test

The connections for test are as shown in Figure 22. A 50 Ω resistor is placed on the AM antenna input. The AM Stereo generator is connected to the AM antenna input. Measurements of audio level in mono mode are made with an audio voltmeter connected through a FET probe (pilot signal “off”). Measurements of audio level and distortion in stereo mode (pilot signal “on”) are made using a pilot rejection filter ahead of the distortion analyzer or the audio meter. The pilot rejection filter has a rejection ratio that should exceed 20 to 25 dB. Typical data is shown in Figures 23–26. Figures 23 and 24 were read on the left channel in mono mode. Figures 25–26 were in stereo mode.

Figure 22. MC13028A/LA1832 Application Circuit Board Test Setup

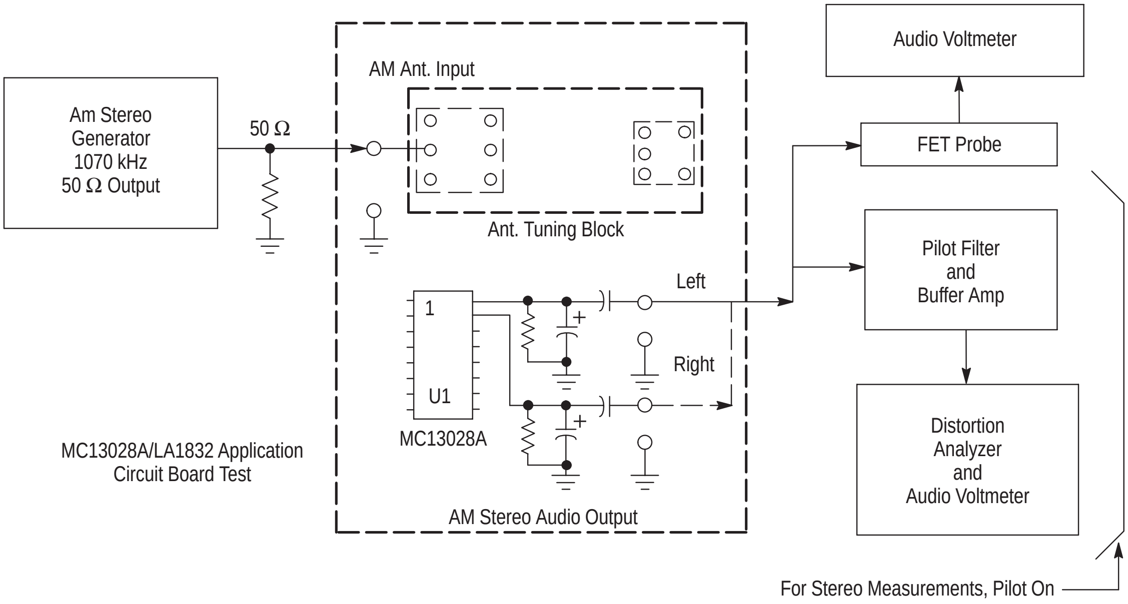


Figure 23. Left AM Output at 30% Modulation

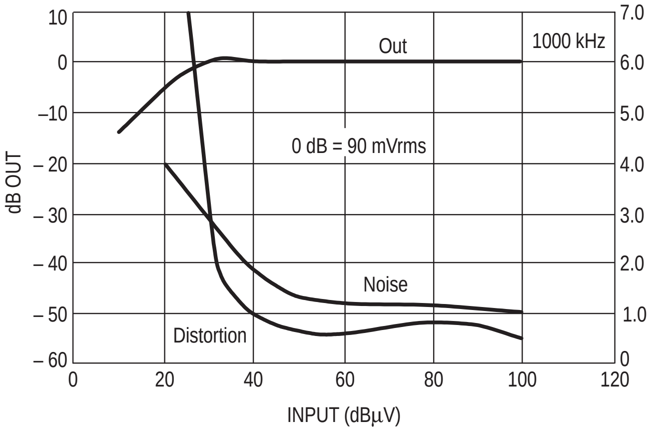


Figure 24. Left AM Output at 80% Modulation

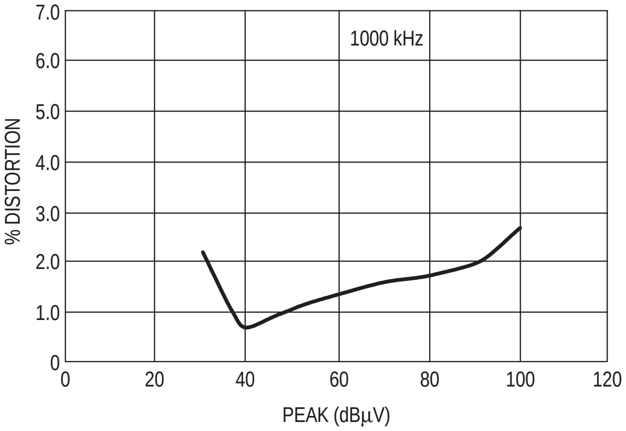


Figure 25. AM Output Right Channel Only Modulated at 50%

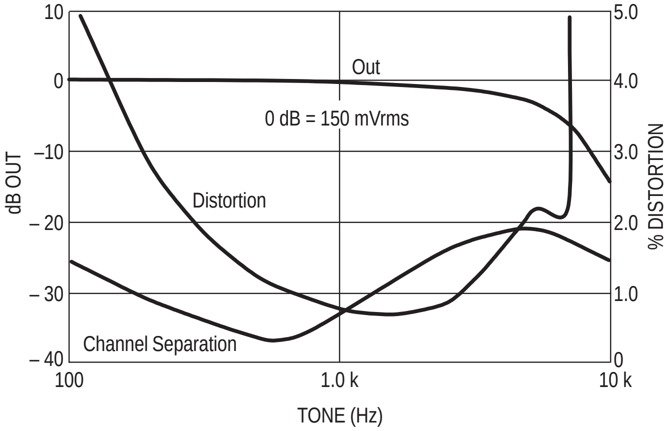
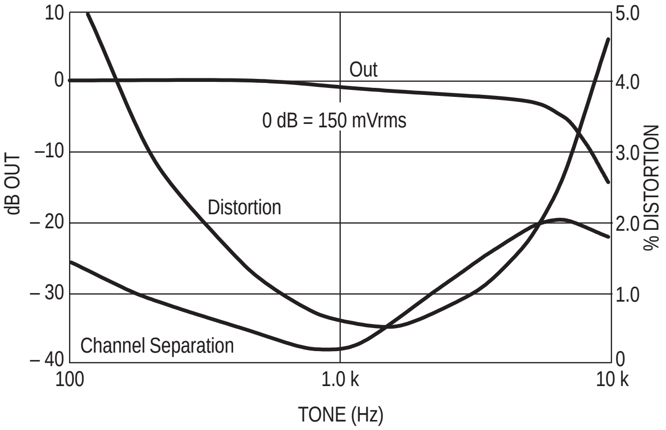


Figure 26. AM Output Left Channel Only Modulated at 50%



MOTOROLA

MC13029A

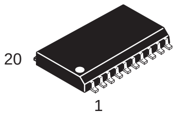
Advance Information

Advanced Medium Voltage IF and C-QUAM® AM Stereo Decoder with FM Amplifier and AM/FM Internal Switch

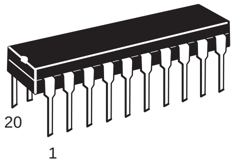
C–QUAM AM STEREO ADVANCED MEDIUM VOLTAGE IF AND DECODER FOR E.T.R. RADIOS

The MC13029A is a third generation C–QUAM stereo decoder targeted for use in medium voltage, CD/Cassette, Mini–Component, and Hi–Fi AM/FM Electronically Tuned radio applications. Advanced features include a signal quality detector that analyzes signal strength, signal to noise ratio, and stereo pilot tone before switching to the stereo mode. A “blend function” has been added to improve the transition from both mono to stereo and stereo to mono. The audio output level is adjustable to allow easy interface with a variety of AM/FM tuner chips. The IC further includes an AM/FM switch, an audio mute and internal high pass filtering on AM. The external components have been minimized to keep the total system cost low.

- Operation From 4.0 to 12 V Supply
- IF Amplifier with IF AGC Circuit
- Single Pin–Out, Temperature Compensated VCO
- VCO Shut Down Mode at Weak Signal Condition
- Precision Pilot Tone Detector
- Stereo Blend Function
- Forced Mono Function
- Adjustable Audio Output Level
- AM/FM Switch
- Separate AM De–Emphasis
- Mute Function
- Internal AM High Pass Filters

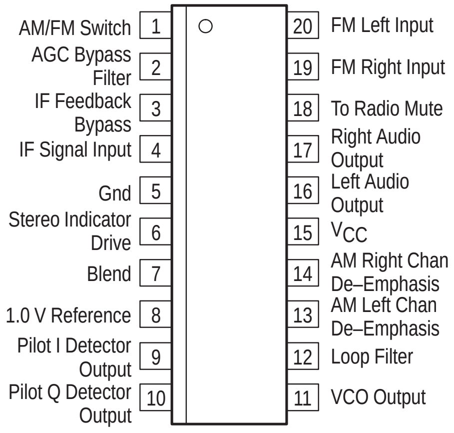


DW SUFFIX
PLASTIC PACKAGE
CASE 751D
(SO–20)



H SUFFIX
PLASTIC PACKAGE
CASE 738

PIN CONNECTIONS



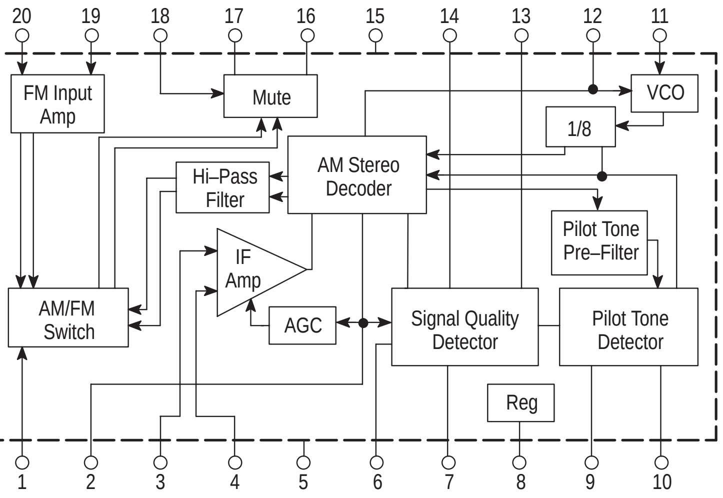
(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC13029ADW	T_A = – 25° to +70°C	SO–20
MC13029AH		DIP–20

The purchase of the Motorola C–QUAM® AM Stereo Decoder does not carry with such purchase any license by implication, estoppel or otherwise, under any patent rights of Motorola or others covering any combination of this decoder with other elements including use in a radio receiver. Upon application by an interested party, licenses are available from Motorola on its patents applicable to AM Stereo radio receivers.

Simplified Block Diagram



This device contains 909 active transistors.

MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Input Voltage	V_{CC}	14	Vdc
Operating Junction Temperature	T_J	150	°C
Operating Ambient Temperature	T_A	–25 to +70	°C
Storage Temperature Range	T_{stg}	–55 to +150	°C
LED Indicator Current	I_{LED}	10	mA

NOTE: ESD data available upon request.

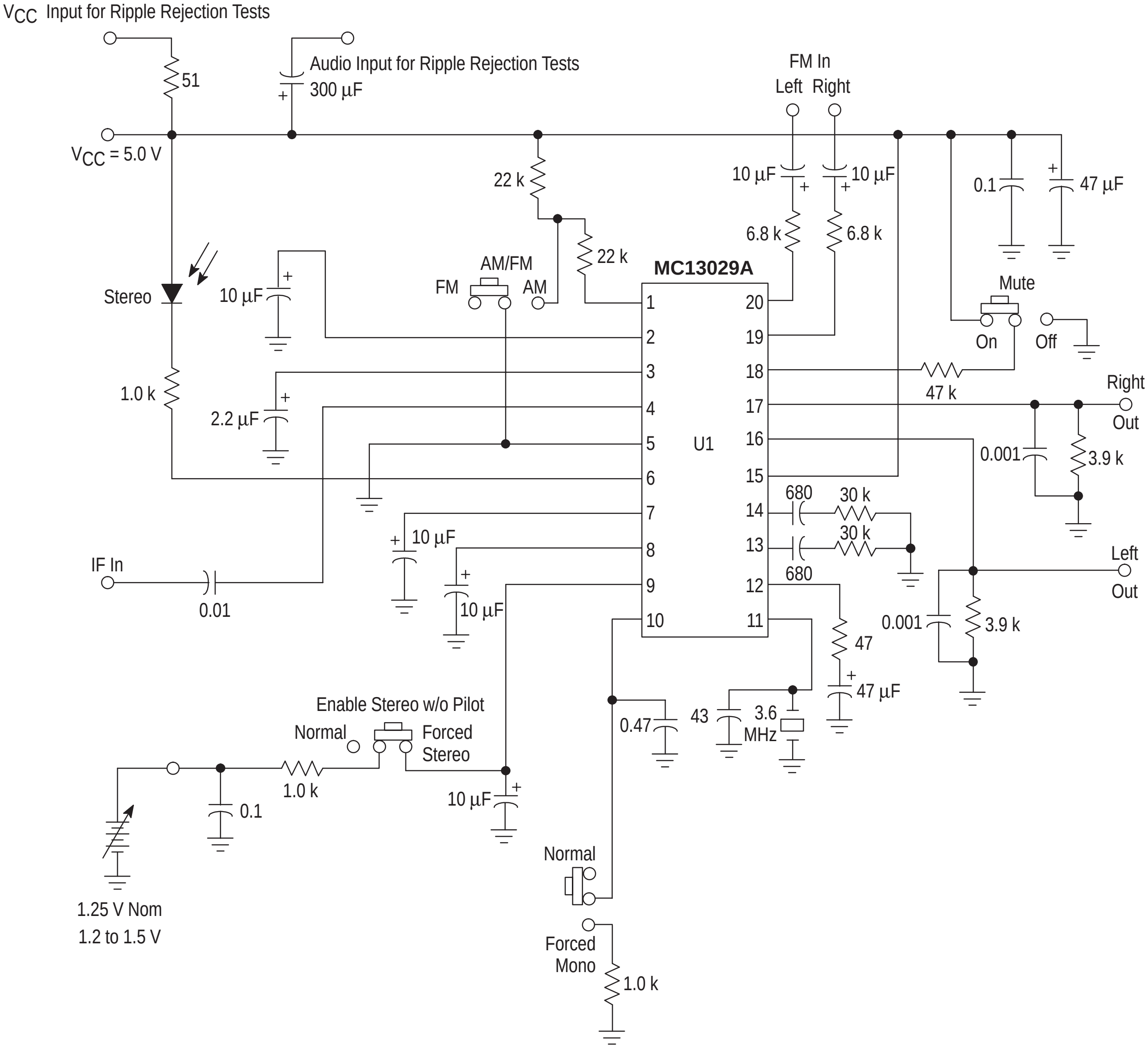
ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 Vdc, T_A = 25°C, Input Signal Level = 74 dBμV, Modulating Signal = 1.0 kHz @ 50% Modulation, Test Circuit of Figure 1, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Supply Current Drain	I_{CC}				mA
V_{CC} = 12 V		–	12	–	
V_{CC} = 5.0 V		9.0	11	13	
Audio Output Level, L+R, Mono Modulation R_O = 3.9 k	V_{out}	50	80	110	mVrms
Audio Output Level, L only or R Only, Stereo Modulation R_O = 3.9 k	V_{out}	110	170	260	mVrms
Output THD					%
Stereo, L or R Only	THD1	–	0.6	1.8	
Mono, L+R	THD2	–	0.1	0.6	
Channel Separation, L or R Only	R or L	23	35	–	dB
Decoder Input Sensitivity, V_{out} = –10 dB	V_{in}	–	33	–	dBμV
Force to Mono Mode, at Pin 10	–	0.25	0.3	–	Vdc
Signal to Noise Ratio	S/N				dB
Stereo, 50%, L or R Only, 1.0 kHz		40	59	–	
Mono, 50%, L+R, 1.0 kHz		40	62	–	
Input Impedance	R_{in}	–	10	–	kΩ
(Reference Specification)	C_{in}	–	8.0	–	pF
Blend Voltage	Bl				Vdc
Mono Mode		0.7	–	0.9	
Stereo Mode		1.2	1.30	1.4	
Out of Lock		–	0.12	0.2	
VCO Lock Range	OSC_{tun}	–	±2.5	–	kHz
AGC Range	AGC_{rng}	–	44	–	dB
Channel Balance	C–B	–1.2	–	1.2	dB
Pilot Sensitivity	–	–	–	4.0	%

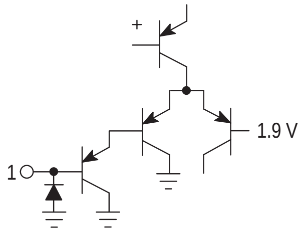
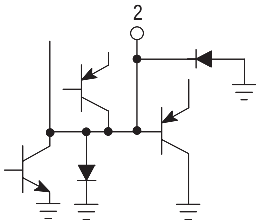
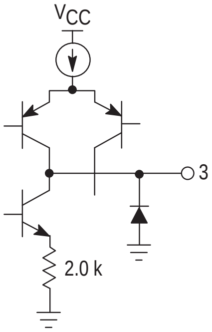
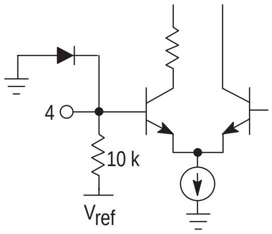
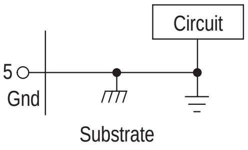
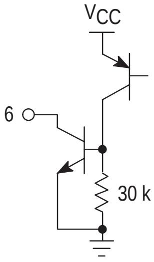
FM AUDIO SWITCH ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 Vdc, T_A = 25°C, Signal = 1.0 kHz.)

Characteristic	Symbol	Min	Typ	Max	Unit
FM Switch Nominal Audio Input V_{CC} = 5.0 V	V_{in}	200	–	500	mV_{pp}
Signal to Noise Ratio (FM Audio Input = 200 mVrms)	S/N	–	80	–	dB
Channel Separation, L or R Only	R or L	–	>60	–	dB
Output THD					%
FM Audio Input = 200 mVrms	THD1	–	0.01	–	
FM Audio Input = 500 mVrms	THD2	–	–	2.0	
AM/FM Switch Input (Pin 1)	–				Vdc
AM Mode		–	–	0.5	
FM Mode		2.6	–	–	
Mute Threshold (Pin 18)	–				Vdc
Mute On		2.6	–	–	
Mute Off		–	–	0.5	

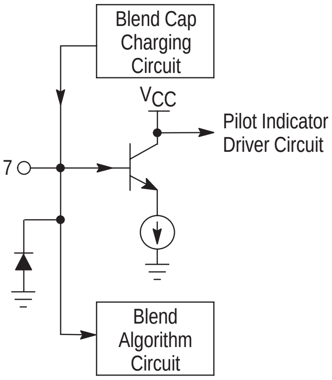
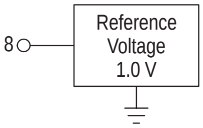
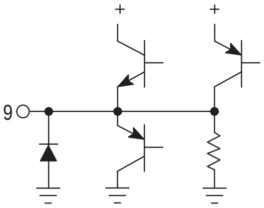
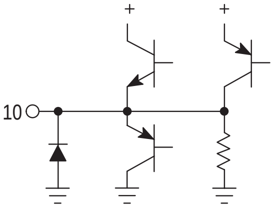
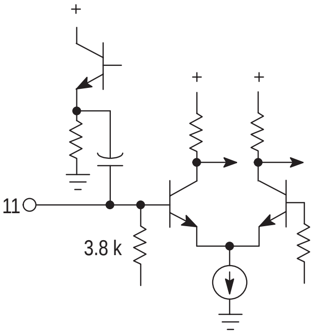
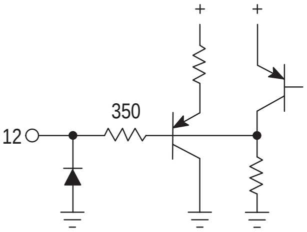
Figure 1. Test Circuit



PIN FUNCTION DESCRIPTION

Pin	Symbol	Internal Equivalent Circuit	Description/External Circuit Requirements
1	AM/FM		**AM/FM Mode Switch** The dc level applied to this pin will determine whether the AM or FM audio is switched to output Pins 16 and 17. A voltage greater than 1.2 V will cause the FM audio to be output.
2	AGC_{cap}		**AGC Filter Bypass Capacitor** An electrolytic capacitor is used as a bypass filter and it sets the time constant for the AGC circuit action. The recommended capacitor value is 10 μF from Pin 2 to ground. The dc level at this pin varies as shown in the curve in Figure 13. AGC Voltage versus Input Level.
3	IF_{FBcap}		**IF Amplifier Feedback Capacitor** A capacitor which is specified to have a low ESR at 450 kHz is normally used at Pin 3. The value recommended for this capacitor is 0.47 μF from Pin 3 to ground. This component forms a low pass filter which has a corner frequency around 30 kHz.
4	IF_{in}		**IF Amplifier Input** Pin 4 is the IF input pin. The typical input impedance at this pin is 10 k. The input should be ac coupled through a 0.01 μF capacitor.
5	Gnd		**Supply Ground** In the PCB layout, the ground pin should be connected to the chassis ground directly. This pin is the internal circuit ground and the silicon substrate ground.
6	S_{IND}		**Stereo Indicator Driver** This driver circuit is intended to light an LED or other indicator when the decoder receives the proper input signals and switches into the stereo mode. The maximum amount of current that the circuit can sink is 10 mA. A current limiting resistor is applied externally to control LED brightness versus total power supply current.

PIN FUNCTION DESCRIPTION (continued)

Pin	Symbol	Internal Equivalent Circuit	Description/External Circuit Requirements
7	$\text{CAP}_{\text{Blend}}$		**Blend Capacitor** The value of the capacitor on this pin will effect the time constant of the decoder blend function. The recommended value is 10 µF from Pin 7 to ground. The dc level at Pin 7 is internally generated in response to input signal level and signal quality. This pin is a key indicator of the operational state of the IC (see text Functional Description). It is recommended to discharge the Blend Capacitor externally when changing stations.
8	V_{ref}		**Regulated Voltage, 1.0 V** An electrolytic capacitor used as a bypass filter is recommended from Pin 8 to ground. The capacitor value should be 10 µF.
9	I_{Pilot}		**Pilot I Detector Output** The Pilot I Detector Output requires a 10 µF electrolytic capacitor to ground. The value of this capacitor sets the pilot acquisition time. The dc level at Pin 9 is approximately 1.0 Vdc, unlocked, and 1.1 to 2.4 Vdc in the locked condition.
10	Q_{Pilot}		**Pilot Q Detector Output** This pin is connected to the Pilot Q Detector and requires a 0.47 µF capacitor to ground to filter the error line voltage at the PLL pilot tone detector. If the value of this capacitor is made too large, the decoder may be prevented from coming back into stereo after a signal dropout has been experienced in the field. The force to mono function is also accomplished at this pin by pulling the dc voltage level at the pin below 1.0 V.
11	OSC_{in}		**Oscillator Input** The Oscillator pin requires a ceramic resonator and parallel capacitor connected to ground. The recommended source for the ceramic resonator is Murata, part number CSA 3.60MGF108. A 43 pF NPO capacitor is in parallel with the resonator. The dc level at Pin 11 is approximately 1.1 Vdc.
12	$\text{LOOP}_{\text{Filter}}$		**Loop Filter** A capacitor which forms the Loop Filter is connected from Pin 12 to ground. The recommended value is 47 µF in series with 47 Ω. This capacitor should be of good construction quality so it will have a very low specification for leakage current in order to prevent stereo distortion. The 47 Ω resistor in series with the capacitor controls fast lock rate. The dc level at Pin 12 is approximately 0.6 Vdc in the locked condition.

PIN FUNCTION DESCRIPTION (continued)

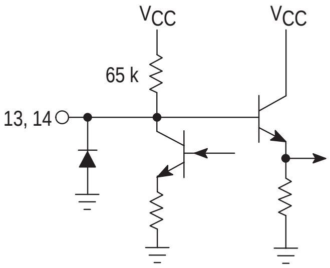
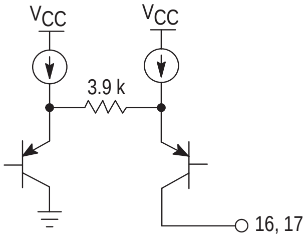
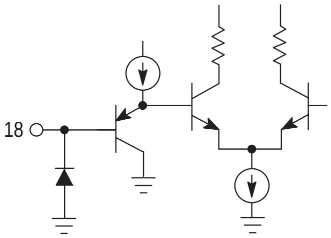
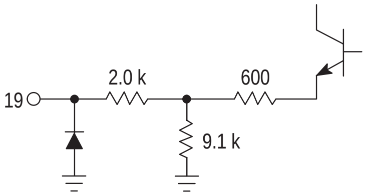
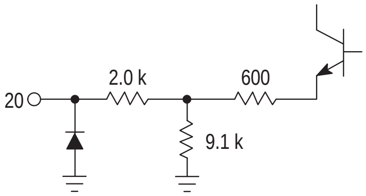
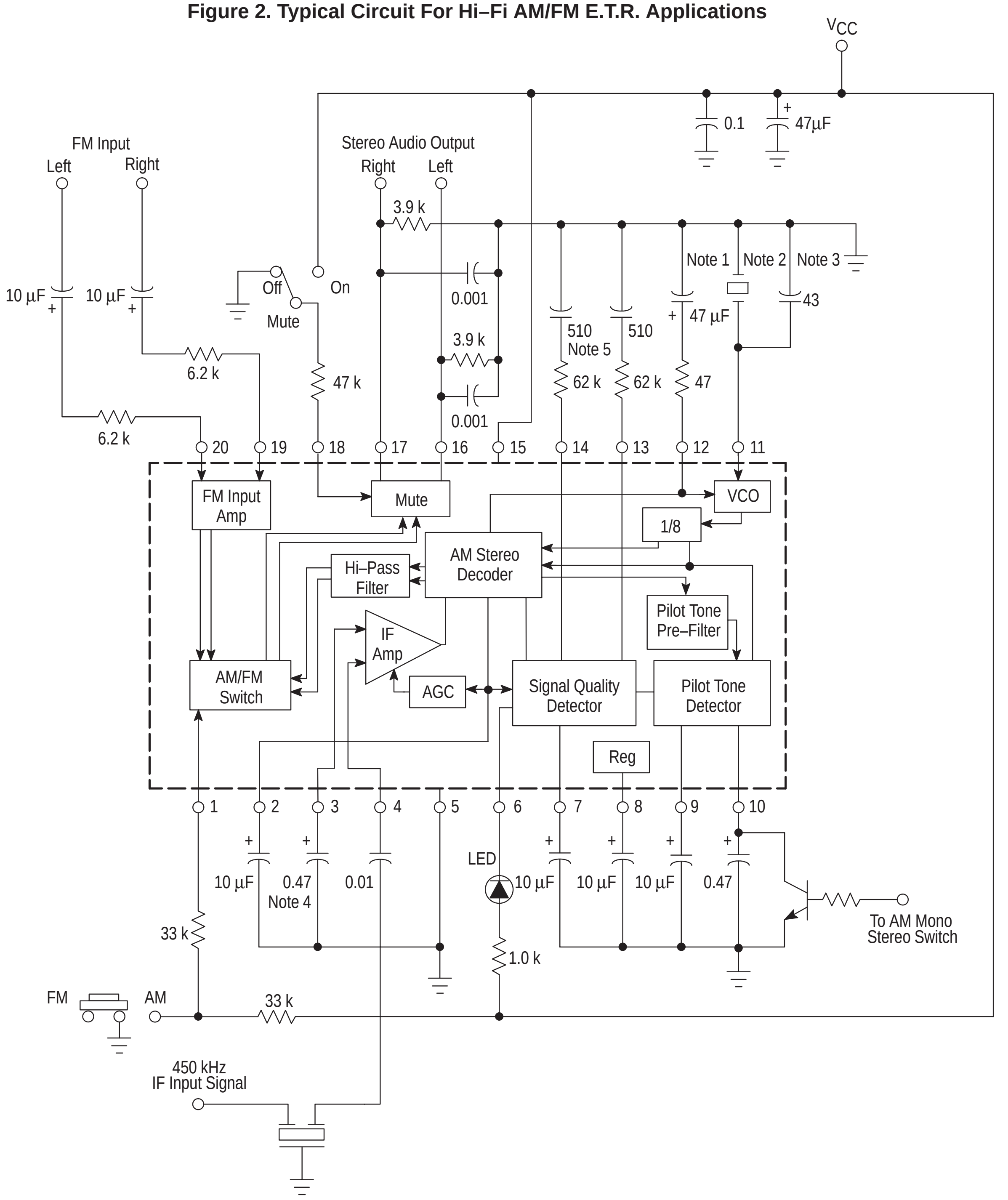
Pin	Symbol	Internal Equivalent Circuit	Description/External Circuit Requirements
13 14	DE–L DE–R		**AM De–Emphasis, Left Channel/Right Channel** An RC network attached at this pin can be used to add de–emphasis to the AM tone response. The AM tone response is primarily shaped by the IF filter. Additional roll–off may be applied here.
15	V_{CC}		**Supply Voltage (V_{CC})** The operating supply voltage range is from 4.0 Vdc to 12 Vdc.
16 17	LEFT_{out} $\text{RIGHT}_{\text{out}}$		**Audio Output** Output is approximately 1.3 μA_{pp} drive current for each percent of mono modulation. A resistor to ground sets the voltage level of the audio output.
18	Mute		**Mute Input** A dc voltage exceeding 1.5 V applied to this pin will cause a shutting down of the left and right channel outputs at Pins 16 and 17.
19	FM–R		**FM Audio Right Channel Input** The audio output from the FM detector is input at this pin. The dc level applied at Pin 1, the AM/FM Mode Switch, then determines whether this audio, or that from the AM channel will be output at Pin 17. An external series resistor between this pin and the FM detector is used to set the FM audio levels at the output Pin 17.
20	FM–L		**FM Audio Left Channel Input** The audio output from the FM detector is input at this pin. The dc level applied at Pin 1, the AM/FM Mode Switch, then determines whether this audio or that from the AM channel will be output at Pin 16. An external series resistor, between this pin and the FM detector, is used to set the FM audio levels at the output Pin 16.

Figure 2. Typical Circuit For Hi–Fi AM/FM E.T.R. Applications



NOTES:
1. This part is recommended to be a low leakage type capacitor. Leakage current due to this capacitor causes increase in stereo distortion and poor separation performance.
2. The recommended source for this part is Murata Products, CSA3.60MGF108. The location of this part should be carefully considered during the layout of the decoder circuit. This part should not be near the audio signal paths, the 25 Hz pilot filter lines, or the V_{CC} high current lines, and the ceramic element ground line should be direct to the chassis ground lead in order to avoid any oscillator inter–modulation.
3. This capacitor is recommended to be an NPO type ceramic part. Changing the value of this capacitor alters the lock range of the decoder PLL.
4. This part is recommended to be a low ESR type capacitor, (less than 1.5 Ω) in order to avoid increased audio output distortions under weak input signal conditions with higher modulation levels.
5. Component values for this stage of the NRSC filter will vary from receiver manufacturer to manufacturer due to the additive nature of the particular response slopes of the frequency selective parts, (RF and IF coils, and the ceramic IF filter) within a radio design. Since these responses may vary somewhat in each custom design, the filters at Pins 13 and 14 are included to provide any remaining response roll–off that might be necessary to comply with the overall NRSC frequency standard.

FUNCTIONAL DESCRIPTION

Introduction

The MC13029A is designed as a medium voltage decoder for the C–QUAM AM Stereo technology and is completely compatible with existing monaural AM transmissions. The IC requires relatively few, inexpensive external parts to produce a multi–featured C–QUAM AM Stereo implementation. The layout is straightforward and should produce excellent stereo performance results. This device performs the function of IF amplification, AGC, modulation detection, pilot tone detection, signal quality inspection, blend, left and right channel FM input amplification, muting, AM and FM switching function, and amplified left and right audio output levels which are adjustable. The IC is targeted for use in CD/Radio/Cassette, Mini–Component, and Hi–Fi AM/FM E.T.R. AM Stereo radio applications.

From the output of a ceramic IF filter and through a coupling capacitor, the IF amplifier circuit of the MC13029A receives its input at Pin 4 as a 450 kHz, typically modulated C–QUAM signal. The input signal level for stereo operation can vary from 50 dBμV to about 90 dBμV. This IC design incorporates feedback in the IF circuit section which provides excellent dc balance in the IF amplifier. This balanced condition also guarantees excellent monophonic performance from the decoder. An IF feedback filter at Pin 3 is formed by a 0.47 μF, low leakage, low ESR capacitor. It is used to filter out the 450 kHz signal which is present on the IF amplifier feedback line. An AGC circuit controls the level of IF signal which is subsequently fed to the detector circuits. An AGC bypass capacitor is connected to Pin 2 and forms a single pole, low pass filter. The value of this part also sets the time constant for the AGC circuit action.

The amplified C–QUAM IF signal is fed simultaneously to the envelope detector circuit, and to a C–QUAM converter circuit. The envelope detector provides the L+R (mono) signal output which is fed to the stereo matrix. In the converter circuit, the C–QUAM signal is changed into a Quam signal when it is divided by the cos ϕ term. The Quam IF signal is then fed into the I detector, the L–R detector, and the Q detector circuits. The outputs of the Envelope detector and the I detector circuits feed back into a comparator circuit which looks at both signals and uses the differences to create the cos ϕ signal. The Quam IF signal fed to the L–R and the Q detectors is multiplied by a 450 kHz signal that is phased 90° from the one in the I detector circuit. This quadrature relationship is necessary in order to detect the L–R (or stereo) audio information from the Quam signal. The audio outputs from both the Envelope and the L–R detectors are first filtered to minimize the harmonics of the IF signal that are created in the mixing process. (The outputs from the I and Q detectors are also filtered similarly.) Then they are fed into a matrix circuit where the Left channel and the Right channel outputs are extracted and fed into a high pass filter block. Here the audio signals are conditioned so they can be fed to an output amplifier which, if left unmuted, delivers the left and the right output at Pins 16 and 17. At this time, a stereo output will occur if the input IF signal is: a.) larger than the stereo threshold level, b.) not too noisy, and c.) a proper pilot tone is present. At Pin 6, the stereo indicator driver circuit, which can sink up to 10 mA, is also enabled.

After turn on or tune in, if the input signal level threshold for stereo operation is not exceeded, or if the incoming signal is too noisy, the blend circuit, at Pin 7, (even in the presence of a pilot signal) will hold the decoder in the monaural mode. A blend circuit is included in this design because of the effects of conditions which occur during field use that can cause input signal strength fluctuation, strong unwanted co–channel or power line interference, and/or multi–path or re–radiation. When these aberrant conditions occur, rapid switching between stereo and mono might occur, or the stereo quality might be degraded. Since these effects could be annoying to the listener, the stereo information is blended towards a monaural output. This creates a condition for listening where the aberrant effects are more tolerable.

Intentional mono operation is a feature sometimes required in receiver designs. There are several ways in which to accomplish this. First, a 10 k resistor from Pin 10 to ground can be switched into the circuit, as is shown in Figure 18. A second method is to shunt Pin 10 to ground through an NPN transistor as shown in Figure 2.

A third method to force a mono condition on the decoder is to shunt Pin 7 of the decoder to ground through an NPN transistor. This discharges the blend capacitor (10 μF), and the blend function internally forces the decoder into mono. This third method does not necessarily require extra parts as most electronically tuned receiver designs require an audio muting function during turn on/turn off, tuning/scanning, or band switching (FM to AM). When the muting function is designed into an AM Stereo receiver, it also should include a blend capacitor reset (discharge) function. The purpose of the blend reset during muting is to re–initialize the decoder back into the “fast lock” mode from which stereo operation can be attained much quicker after any of the interruptive activities mentioned earlier, (i.e. turn on, tuning, etc.).

The VCO in this IC is a phase shift oscillator type that operates with a ceramic resonator at eight times the IF frequency, or 3.60 MHz. With IF input levels below the stereo threshold level, the oscillator is not operational. This feature helps to eliminate audio tweets under low level, noisy input conditions.

The phase locked loop (PLL) in the MC13029A is locked to the L–R signal. This insures good stereo distortion performance at the higher levels of Left only or Right only modulations. Under normal operating conditions, the PLL remains locked because of the current capability of the loop driver circuit. This high gain, high impedance circuit is filtered by a 47 Ω resistor in series with a 47 μF capacitor from Pin 12 to ground. It is recommended that the capacitor be a very low leakage type electrolytic (less than 200 μA), or a tantalum part. Any significant leakage through the capacitor will unbalance the loop driver circuit and result in less than optimum stereo performance, see Figures 10 and 11.

The pilot tone detector circuit is fed internally by a signal from the Q detector output and is filtered by an internal, 50 Hz low pass pilot pre–filter. This filter is designed to prevent the pilot tone detector input from being overloaded by higher levels of L–R audio modulation. A pilot I detector circuit employs a capacitor to ground at Pin 9 to operate in conjunction with an internal resistor to create an RC integration time. The value of the capacitor affects the amount of time required to produce a stereo indication. The minimal time period must be long enough to include the time it takes for the circuit to check for detector falsing due to noise or interference, station re–tuning by the customer, and pilot drop–out in the presence of heavy interference. The pilot Q detector incorporates a filter on its pilot tone PLL error line at Pin 10. This capacitor to ground (usually 0.47 µF) is utilized to filter any low frequency information that may be present on the error line. If the value of this capacitor is allowed to be too small, the level of interference near the pilot tone frequency of 25 Hz may become large enough to cause stereo drop–out. If the capacitor value is made too large, the pilot tone may be prevented from being re–acquired if it is somehow lost due to fluctuating field conditions.

A 1.0 V reference level is created within the IC. This regulated line is used extensively by circuits throughout the MC13029A design. An electrolytic capacitor from Pin 8 to ground is used as a filter for the reference voltage.

At Pin 1, the MC13029A provides a function which allows the user to switch between AM and FM audio signals. The actual switching is controlled by dc level with a low for AM and a high for FM audio output.

The level of the audio output at Pins 16 and 17 can be set by the value of a resistor to ground at these pins. The output pins are connected to the collectors of PNP audio output amplifiers. At strong signal, these amplifiers can supply about 1.3 μA_{pp} of drive current for each percentage of mono modulation present. In other words, for a 100% LTR signal, 130 μA_{pp} will flow through the load. Thus, the value of resistor to ground will determine the peak–to–peak output.

The MC13029A IC provides a true mute function, controlled at Pin 18. A dc level of about 2.6 Vdc is sufficient to ensure muting of the audio outputs at Pins 16 and 17. This feature is useful when tuning in a different radio station, and the designer may also choose to utilize muting when switching between AM and FM.

The FM input audio signals are fed through series external resistors to Pins 19 and 20. Since AM broadcasters normally use heavy audio processing, the value of these resistors is chosen so that the audio output levels of FM are approximately 2.0 dB higher than the audio output levels of AM for the same modulation levels. Under these conditions, there will be only minimal volume differences perceived by the consumer when the MC13029A is switched between AM and FM outputs.

In order to comply with the FCC ruling on the NRSC AM audio response, a connection for de–emphasis circuitry in the MC13029A is provided at Pins 13 and 14 for left and right AM channels respectively. Typically, a series R–C network to ground will provide sufficient additional response shaping to the overall AM response so that the NRSC standard shape can be achieved. The values of these de–emphasis components will vary from design to design. The AM RF and IF coil responses, ceramic filter response and NRSC circuit response all contribute in an additiive manner to the shape of the overall AM audio responses at the IC output pins.

DISCUSSION OF GRAPHS AND FIGURES

The curves in Figures 3 through 8 depict the separation and the distortion performance in stereo for 30%, 50% and 65% single channel modulations respectively. The data for these figures was collected under the conditions of V_{CC} = 8.0 V and R_O = 3.9 k in both the left and the right channels as recommended in the application circuit of Figure 2. A very precise laboratory generator was used to produce the AM Stereo test signal of 450 kHz at 75 dBμV fed to Pin 4. An NRSC post detection filter was not used. The audio separation shows an average performance at 30% and 50% modulations of –38 dB in the frequency range of 1.0 to 5.0 kHz. The corresponding audio distortions are about 0.3% at 30% modulation and about 0.4% or better at 50% modulation.

Figure 7 shows that the typical separation performance at 65% modulation in the 1.0 to 5.0 kHz region is about –35 dB, and the corresponding audio distortion shown in Figure 8 is about 0.9% or better. The performance level of these sinusoidal signals is somewhat less than those discussed in the previous paragraph due to the internal operation of the clamping circuits. In the field, the transmitters at AM Stereo radio stations are not usually permitted to modulate single channel levels past 70%.

Note the –3.0 dB of roll–off at 80 Hz in the output responses of this decoder. These are the top traces (Desired Channel) in Figures 3, 5 and 7. That roll–off appears by design as a feature to help minimize switching transients present when between AM and FM. This roll–off also provides additional attenuation of pilot tone residuals in the detected audio.

The graphs in Figure 9 show the traces of noise response for four different bandwidths of post detection filtering, measured with respect to 30% mono modulation. It can be seen that the noise floors improve steadily with increasing levels of incoming 450 kHz as the value of the lower corner frequency of the filter is increased. Data for the stereo noise floors was collected with the decoder in the forced stereo mode. The upper trace in Figure 9, labeled Audio Level, shows the response, of the 30% mono signal transmitted, as it appears at the decoder output. The change in response level around 55 dBmV shows the characteristic of the total decoder gain at lower signal inputs.

Figures 10 and 11, discussed briefly in the Function Description Section, show the importance of using a quality component at Pin 12 to ground. It can be seen that an electrolytic capacitor leakage current of 600 nA can unbalance the PLL to the point where stereo performance may degrade to only 25 dB of separation with a corresponding 2.0% distortion at 50% modulation levels.

The value of the capacitor connected to Pin 12 (47 μF) is also a factor in the determination of the low frequency corner of the PLL circuit response. PLL responses appear in Figure 12, plotted for three different values of loop filter capacitor. The recommended value of 47 μF provides the best response shape in this circuit where a Murata Products CSA3.60MGF108 part is used.

Figure 13 presents the response of the AGC voltage versus decoder input signal level in the application schematic of Figure 2. The trace begins approximately at the point of decoder sensitivity, and rises until reaching the area of stereo sensitivity. Thereafter, the circuit responds in a near linear fashion for the next 35 dB of input signal increase.

Figures 14 through 17 depict the V_{CC} ripple rejection performance for the MC13029A under mono and stereo conditions for maximum and for no NRSC filtering. It should be noted that this data was collected without any V_{CC} filtering. As one might expect, the ripple rejection is excellent during mono conditions with approximately 45 dB of 50 Hz to 100 Hz ripple rejection at the high level of NRSC filtering. Under stereo operation, the rejection is the same or better in the 6.0 to 12 V range of operation, as can be seen in Figure 16. When the decoder operates in stereo, the VCO is functional, thus the decoder becomes more susceptible to audio ripple on the V_{CC} line. Under normal operating conditions, with the recommended value of 47 μF at Pin 15 and 10 μF at Pin 8, a V_{CC} ripple reading will be virtually the same as measuring the noise floor of the IC.

Figure 3. Single Channel Separation at 30% Modulation

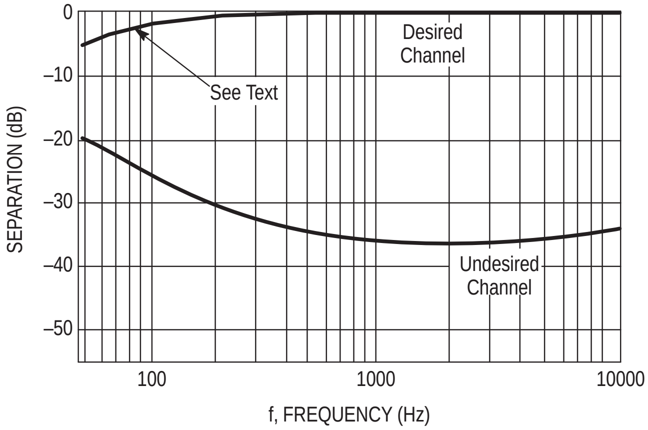


Figure 4. Single Channel Distortion at 30% Modulation

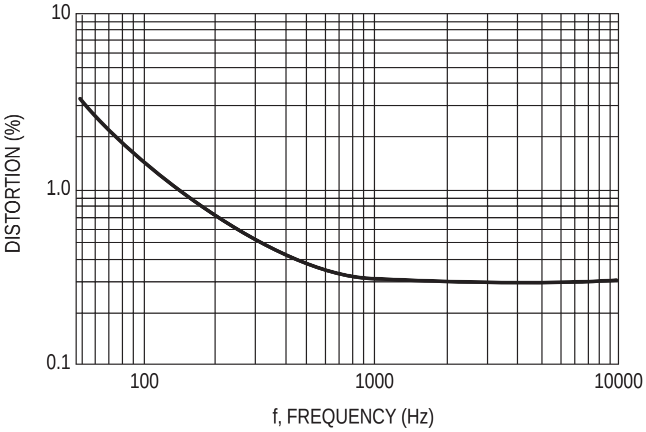


Figure 5. Signal Channel Separation at 50% Modulation

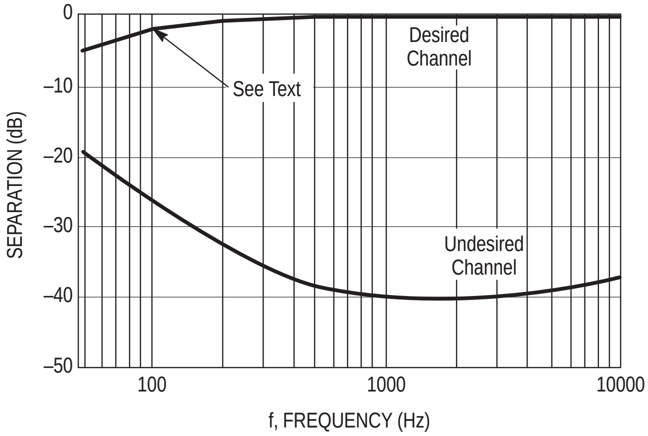


Figure 6. Single Channel Distortion at 50% Modulation

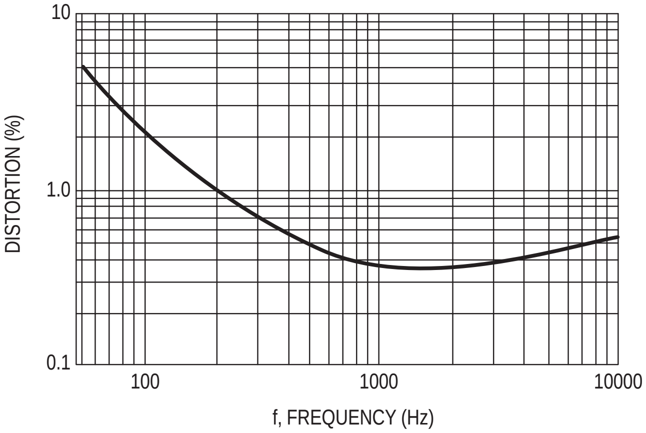


Figure 7. Single Channel Separation at 65% Modulation

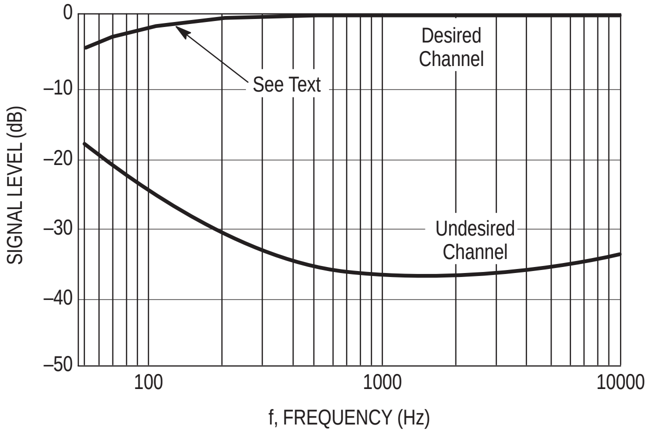


Figure 8. Single Channel Distortion at 65% Modulation

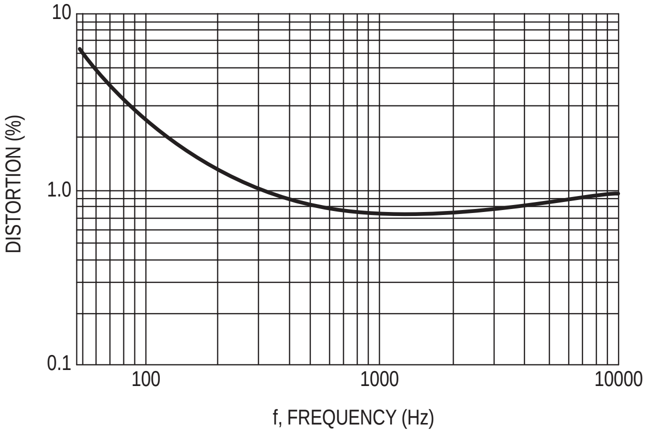


Figure 9. Stereo Noise in Various Bandwidths when Mono Transmitted

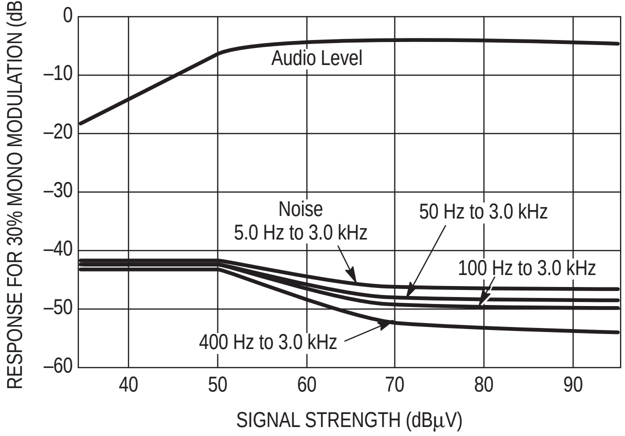


Figure 10. Decoder Separation versus Filter Capacitor (Pin 12) Leakage Current

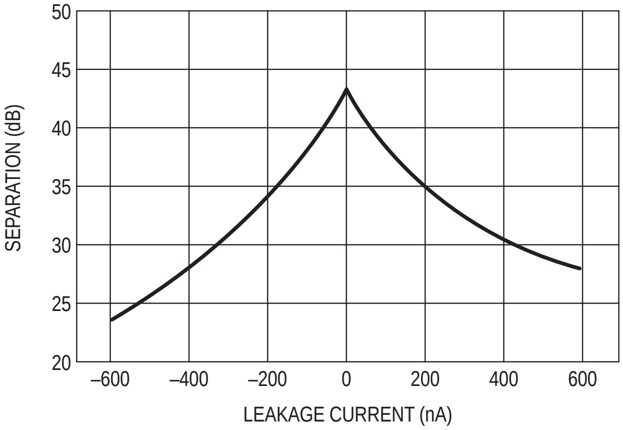


Figure 11. Decoder Distortion versus Filter Capacitor (Pin 12) Leakage Current

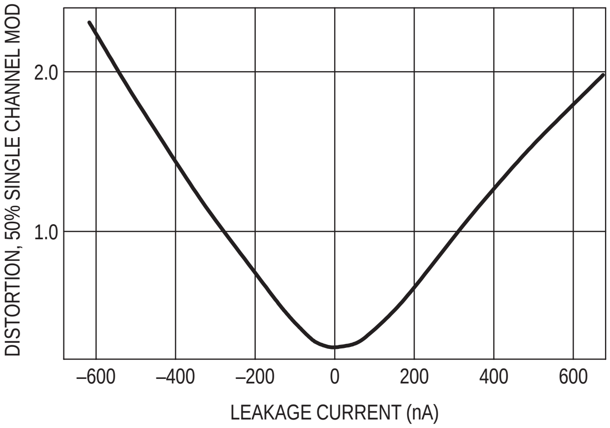


Figure 12. Low Frequency Corner of PLL Response

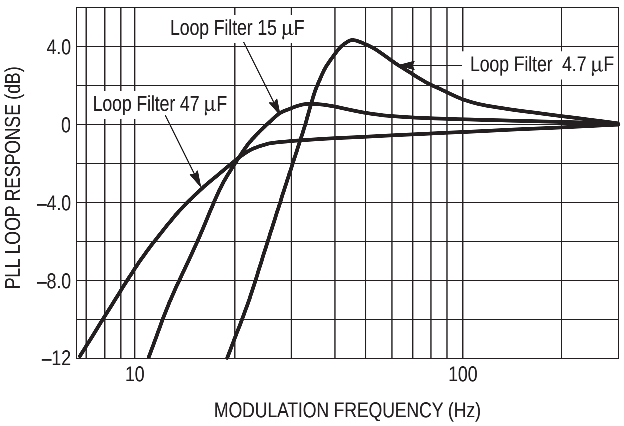
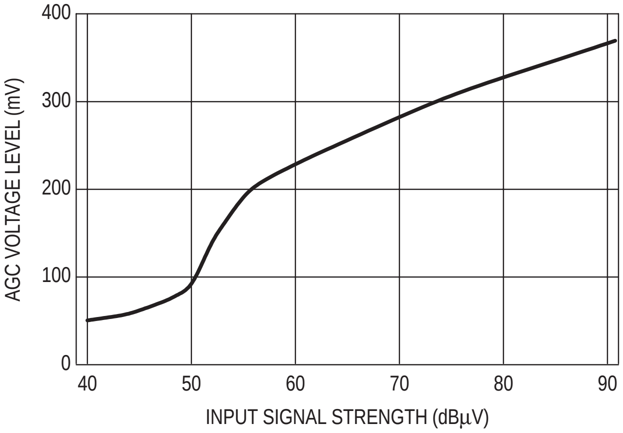


Figure 13. AGC Voltage versus Input Signal Level



AM STEREO TUNER/FM STEREO IF

Description of Application

The MC13029A AM Stereo Decoder is combined with a Sanyo LA1832 Tuner. The combination results in an AM stereo tuner, along with an FM IF and FM stereo detector. The MC13029A provides the means to switch the left and right channel audio between the AM and FM. A MC145151 synthesizer controls the L.O. contained within the LA1832. The circuit schematic is shown in Figure 18.

Circuit Board Description

The copper side layout and component locations are shown in Figure 19. The dimensions in the figure give the true size of the circuit board. With the exception of U2 and U3, all components and jumpers are mounted on the side of the board, away from the viewer.

Special Parts

Table 1 provides the circuit function, part number, and the manufacturer's name for special parts. The parts are identified by their schematic symbol. Where the part is not limited to a single source, a description sufficient to select a part is given.

Table 1

U1	IC–AM Stereo Decoder, MC13029A, Motorola
U2	IC–AM/FM IF and Multiplex Decoder, LA1832M, Sanyo
U3	IC–Frequency Synthesizer, MC145151DW2, Motorola
T1	AM IF Coil, A7NRES–11148N, TOKO
F1	AM IF Ceramic Filter, SFG450F, Murata
F2	FM Detector Resonator, CDA10.7MG43, Murata
F3	FM Multiplex Decoder Resonator, CSB456F15, Murata
F4	AM Tuner Block, BL–70, Korin Giken
X1	10.24 MHz Crystal, Fundamental Mode, AT Cut, 18 pF Load Cap, 35 Ω Max Series R, HC18/U Holder
X2	3.6 MHz AM Stereo Decoder Resonator, CSA3.60F103, Murata
S5	8 Section SPST DIP Switch

Figure 14. Mono V_{CC} Ripple Rejection with No NRSC Filter

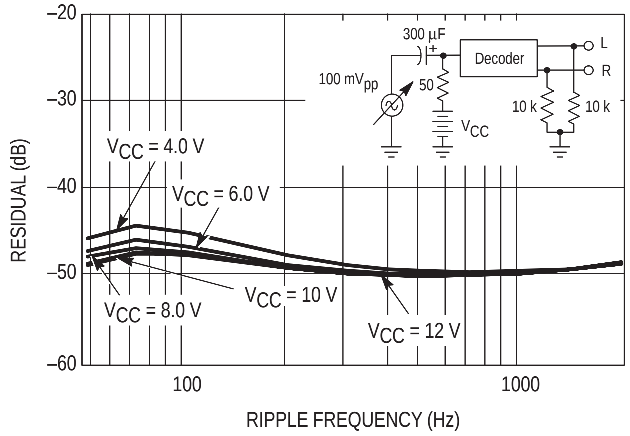


Figure 15. Mono V_{CC} Ripple Rejection with Maximum NRSC Filter

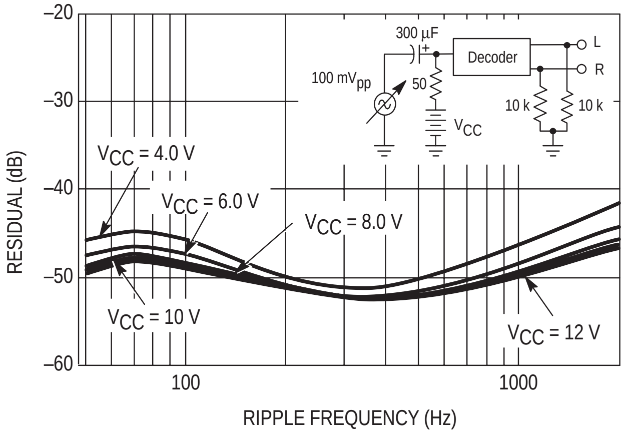


Figure 16. Stereo V_{CC} Ripple Rejection with No NRSC Filter

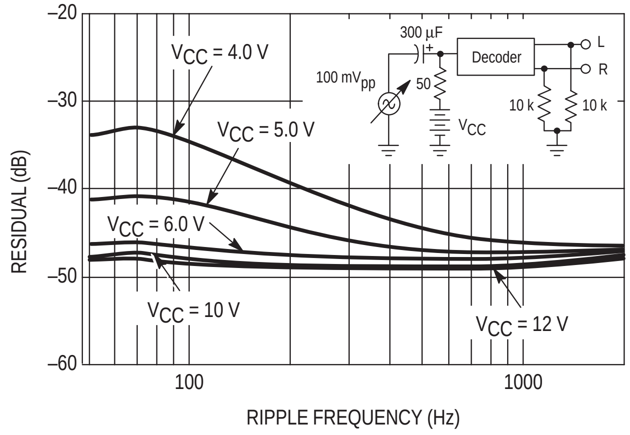


Figure 17. Stereo V_{CC} Ripple Rejection with Maximum NRSC Filter

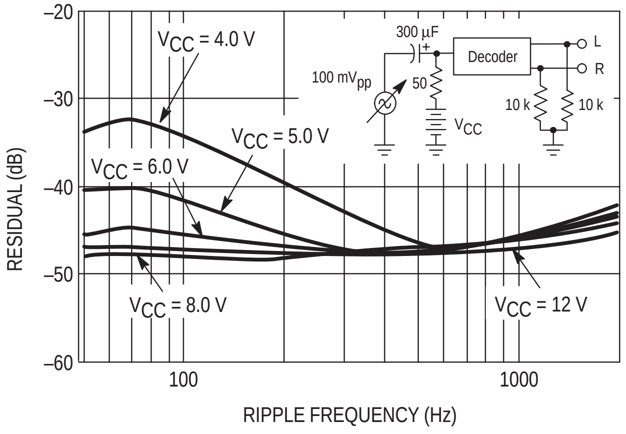


Figure 18. MC13029A Decoder IC Application

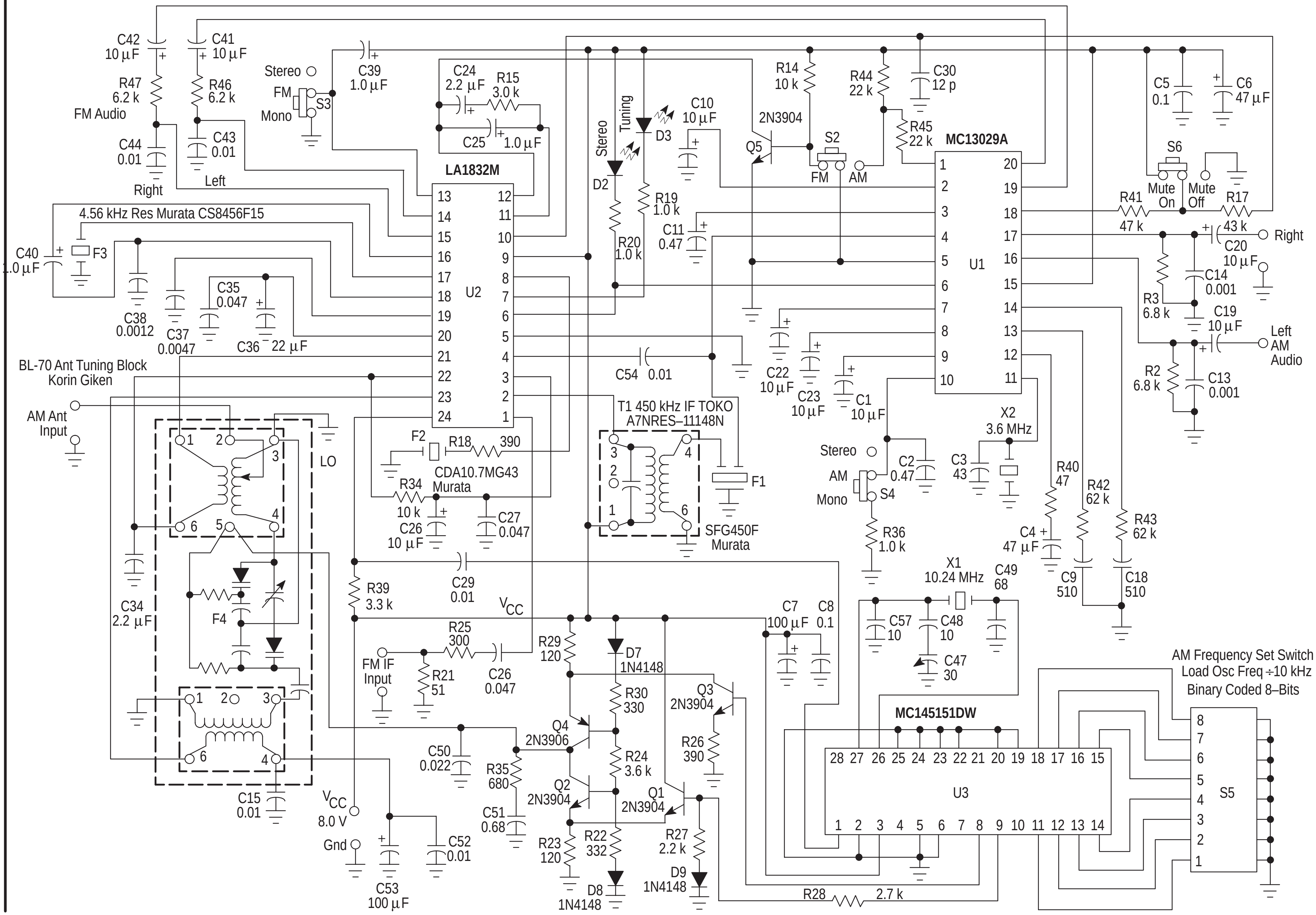
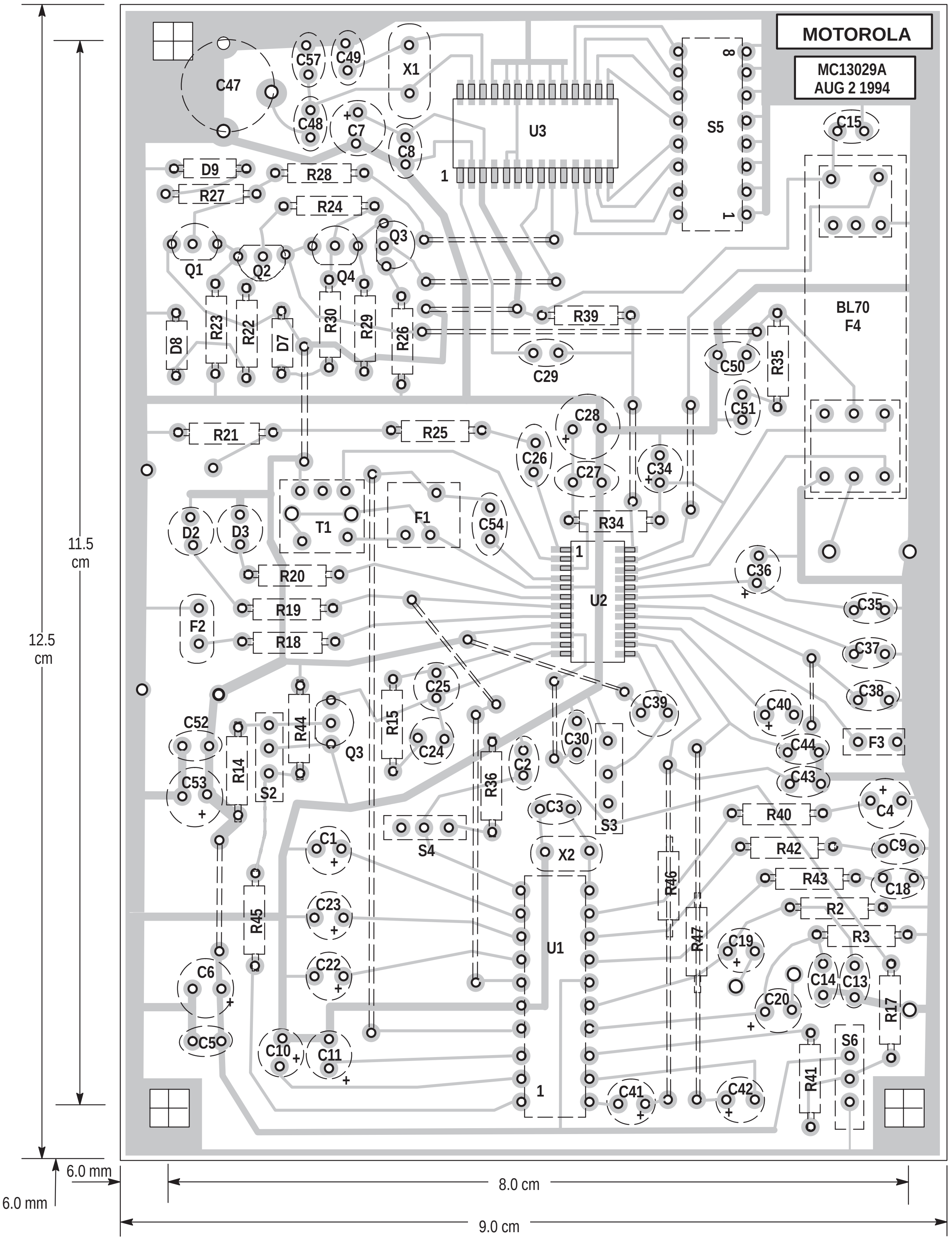


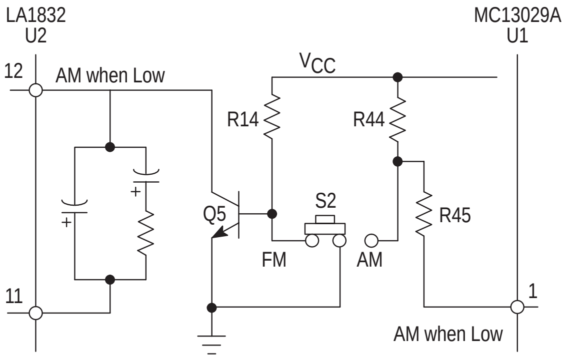
Figure 19. MC13029A Application Circuit Board
Shown 1 1/2 Times Actual Size



CIRCUIT DESCRIPTION

To set the circuit to AM mode, Pin 12 of U2 must be pulled to ground, as is Pin 1 of U1. This operation is shown in Figure 20. Pin 12 of U2 must be isolated by a high impedance when in FM mode. To allow switch S2 to accomplish the switching of both ICs, the transistor Q5 performs the switching of Pin 12 of U2.

Figure 20. AM/FM Switch

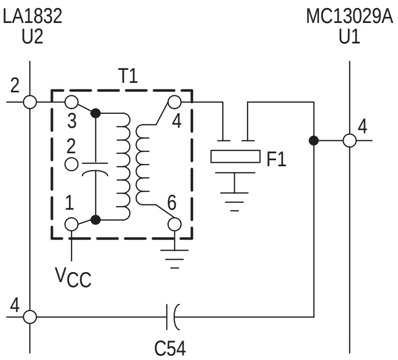


The AM local oscillator is contained in U2 with the L.O. coil located within the tuning block F4, and the coil connected to Pin 23 of U2. See Figure 18. The secondary of the coil is tuned by a varacter contained in F4, and controlled by the synthesizer IC U3. A buffer amplifier outputs the L.O. frequency from U2 Pin 24, This sample of the L.O. frequency is input to Pin 1 of the synthesizer IC U3.

The station signal is applied from a loop antenna (not shown in Figure 18) to the primary of the RF coil contained within the tuning block F4. The primary is tuned by a varactor located within F4, and controlled by the synthesizer U3. The coil secondary applies the signal to Pin 21 of U2 along with a bias voltage from Pin 22 of U2.

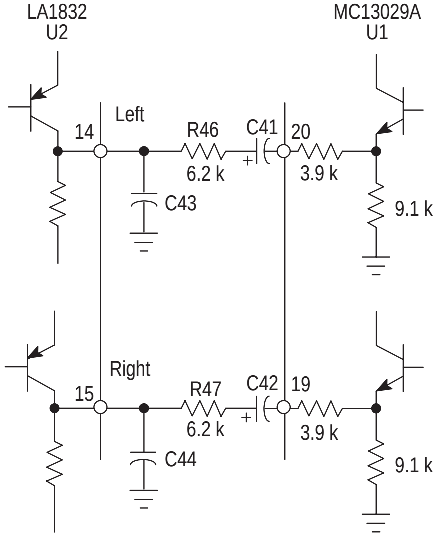
The 450 kHz IF signal from the mixer is output from Pin 2 of U2. Refer to Figure 21. The IF signal is applied through the IF coil T1 to the ceramic band pass filter F1. The signal is then applied to Pin 4 of the tuner IC, U2 and to Pin 4 of the decoder, U1. C54 is necessary to provide dc isolation between Pin 4 of U2 and Pin 4 of U1.

Figure 21. IF Connection



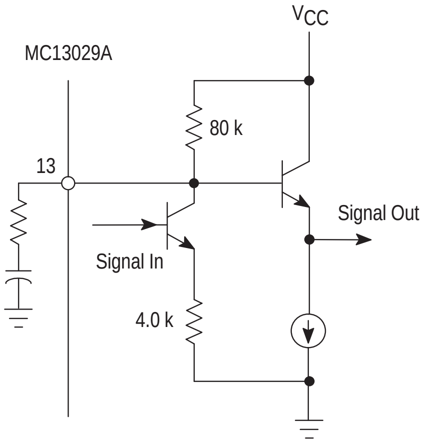
Switching of the audio between AM and FM modes takes place in the decoder IC, U1. The FM audio is conducted from the tuner IC, U2 to the decoder as shown in Figure 22. R46 and R47 provide for the desired balance in audio levels between AM and FM modes. FM de–emphasis is provided by the capacitors C43 and C44. The output impedance of the tuner at Pins 14 and 15 is 5.0 k. The series resistance R46 and R47 in combination with the input resistance at Pins 19 and 20 of U1 bring the effective resistance down to approximately 4.0 k. For a 50 µs de–emphasis, a capacitance value of 0.012 µF would be used for C43 and C44.

Figure 22. FM Audio Connection Tuner to Decoder



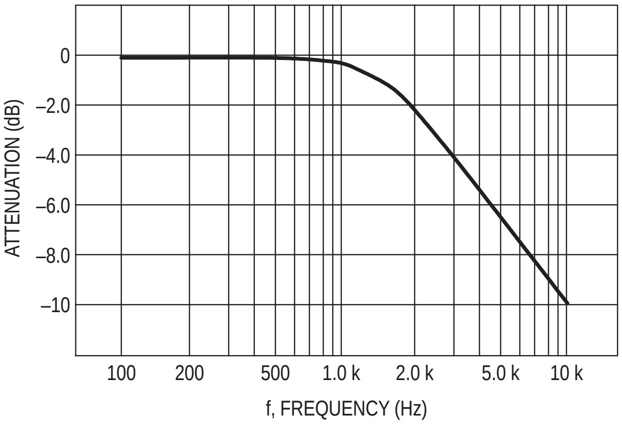
Provision for the application of AM de–emphasis is at Pins 13 (left) and 14 (right) of the decoder U1. This is shown in Figure 23. The tone response in AM mode is primarily set by the IF bandpass filter F1. This response is shown in Figure 28.

Figure 23. AM De–Emphasis Left Channel Shown



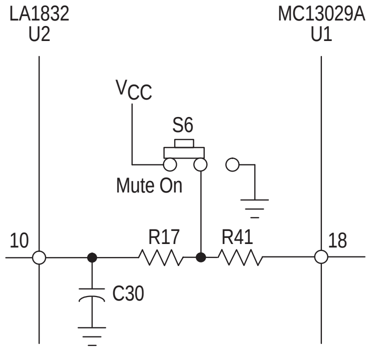
The NRSC recommended tone response is as shown in Figure 24. The tones falling within the IF filter bandpass can be contoured to this response by RC networks at Pins 13 and 14 of the decoder, U1.

Figure 24. NRSC De–Emphasis Curve for the United States



For muting, Pin 10 of U2 and Pin 18 of U1 must be pulled high. This is done by switch S6 as is shown in Figure 25.

Figure 25. Mute Switching



The AM can be forced to mono by pulling Pin 10 of U1 to ground. This is done by switch S4. Refer to Figure 18. The FM can be forced to mono by pulling Pin 13 of U2 to ground. This is accomplished by switch S3.

Component Choice

The pin function section of this data sheet gives the information to select the proper components to be used with the MC13029A decoder. A similar section in the LA1832 data sheet provides the information to choose the components for the tuner.

Tuning

The frequency to which the AM tuner will tune is set by the eight switches contained in the S5 assembly. S5 consists of eight SPST switches. The switches are numbered from 1 to 8. Switch 8 connects to Pin 18 of the synthesizer, U3.

To tune each frequency, the switches are set to a pattern corresponding to that frequency. The pattern is derived from a binary number, equal to the local oscillator frequency divided by 10 kHz.

As an example, consider tuning to 1070 kHz. The local oscillator is 1070 kHz + 450 kHz or 1520 kHz. 1520 kHz/10 kHz is 152. The binary equivalent of 152 is 10011000. The 1 represents an open switch. The 0 represents a closed switch. The left most bit of the binary number is switch 8. Switch 8 is set open. Switch 7 is set closed. This process is continued for all eight bits of the binary number. Table 2 summarizes the switch settings for 1070 kHz.

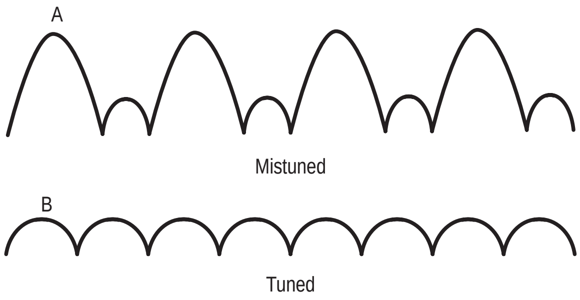
Table 2

Switch	Number	Position
8	1	Open
7	0	Closed
6	0	Closed
5	1	Open
4	1	Open
3	0	Closed
2	0	Closed
1	0	Closed

Circuit Adjustments

The FM circuit requires no adjustments. The AM L.O. must be able to tune from 990 to 2050 kHz to cover the broadcast range. Adjust the core of the L.O. coil, if needed, to be able to cover this range. The AM RF coil and trimmer can be adjusted for best signal after connection to the loop antenna. The coil is adjusted near the low end of the band, and the trimmer is adjusted at the top of the band. The IF coil T1 is first adjusted for maximum signal out of the filter F1. Final adjustment is shown in Figure 26.

Figure 26. Decoder Signal Output for Mistuned and Tuned Condition with Input Signal of 80% L–R and 3.0 kHz



Apply an AM Stereo signal modulated with a 3.0 kHz tone at 80% L–R. Set the pilot tone off. Observe either the left or right channel audio. When T1 is properly adjusted, the waveform should appear as waveform B shown in Figure 26. Adjust T1 as required. If the waveform can only be adjusted to appear as waveform A, then adjust for least amplitude and equal amplitudes on both the left and right channels.

AM Circuit Test

The connections for test are as shown in Figure 27. A 50 Ω resistor is placed on the AM antenna input. The AM Stereo generator is connected to the AM antenna input. Measurements of audio level are made with an audio voltmeter with a high input impedance (1.0 MΩ). Measurements of distortion in stereo mode are made using a 400 Hz high pass filter ahead of the distortion analyzer. Typical data is shown in Figures 28 through 34.

Figure 27. Test Circuit

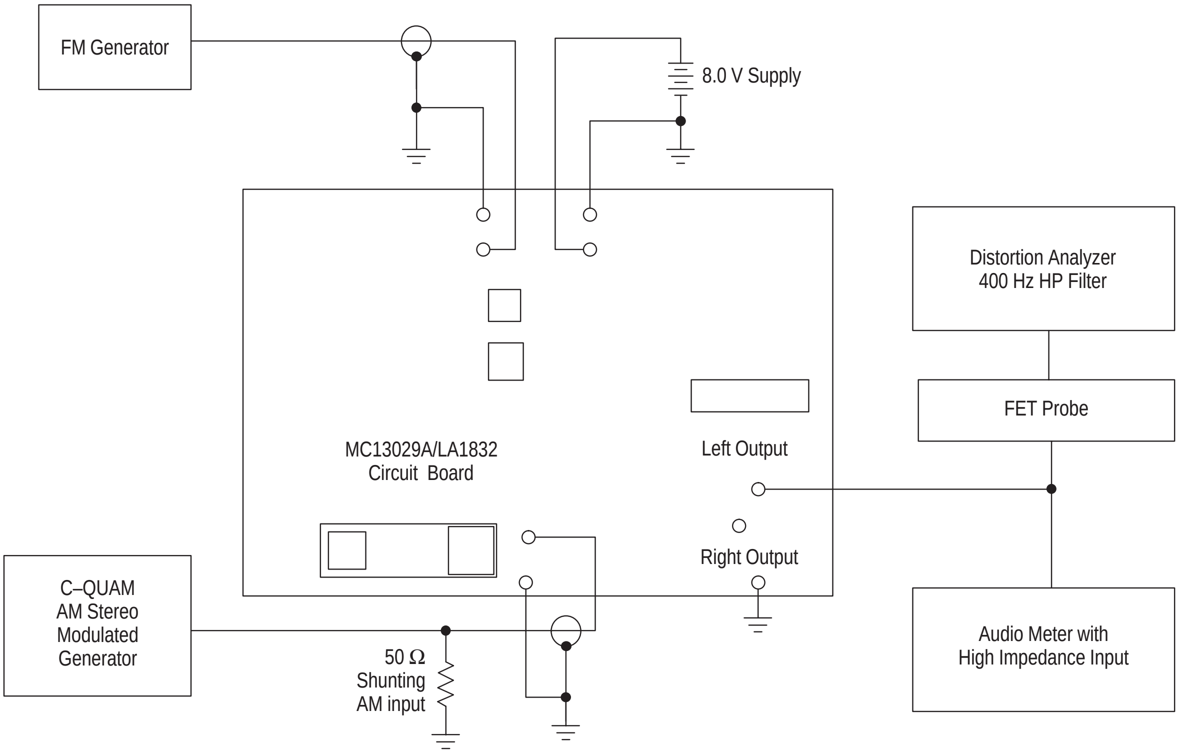


Figure 28. Tone Response without De–Emphasis Set by IF Bypass

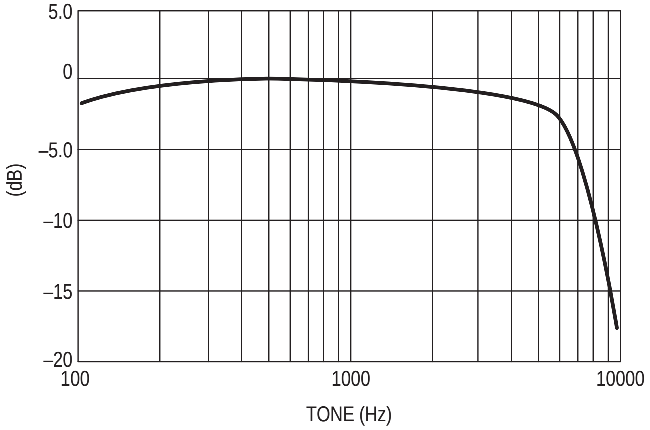
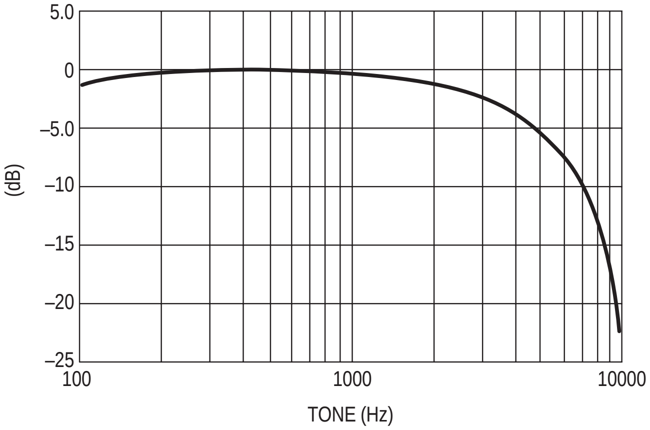


Figure 29. Tone Response with De–Emphasis



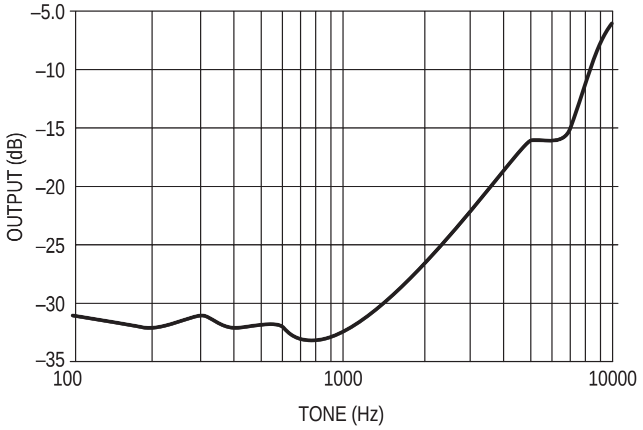


Figure 30. Single Channel Separation at 50% Modulation

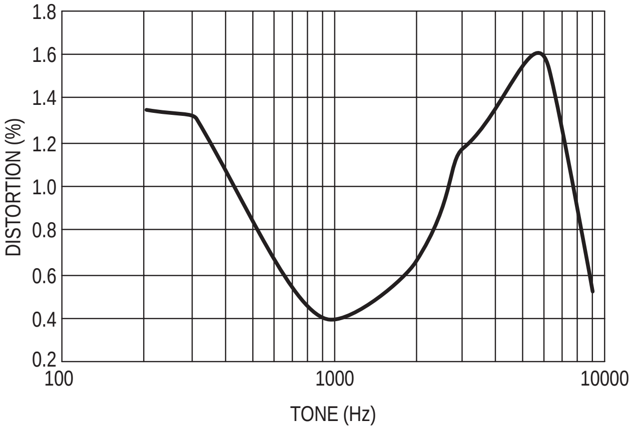


Figure 31. Single Channel Distortion at 50% Modulation

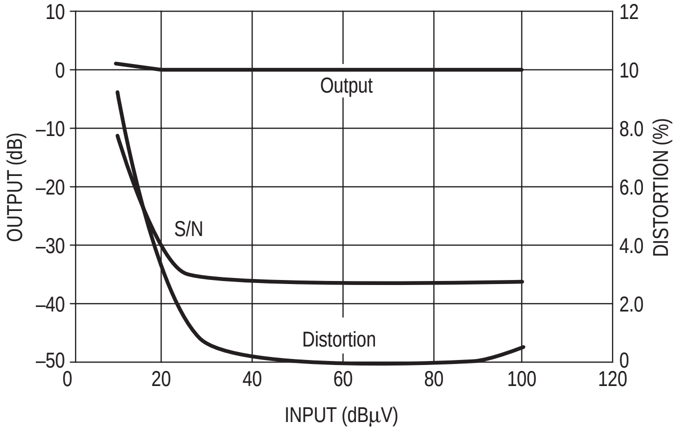


Figure 32. Mono Characteristics at 30% Modulation

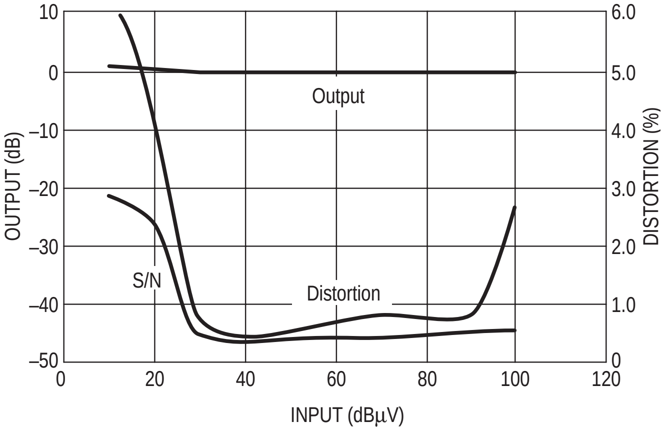


Figure 33. Mono Characteristics at 80% Modulation

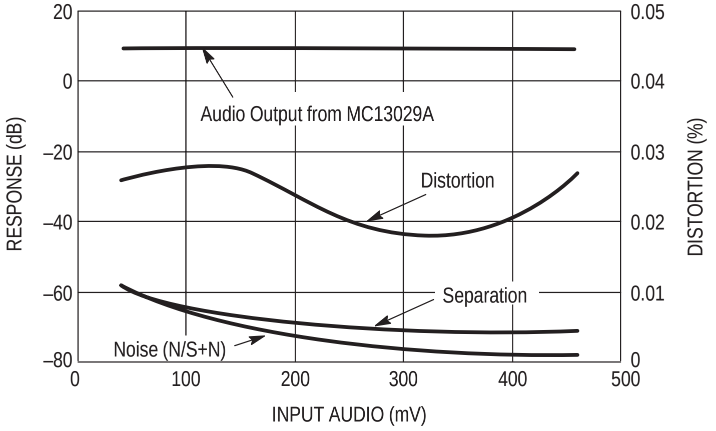


Figure 34. AM/FM Audio Switch Performance of Left FM Channel with 1.0 kHz Audio Tone

MOTOROLA

MC13030

Advance Information

Dual Conversion AM Receiver

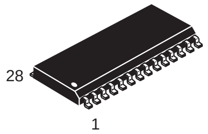
The MC13030 is a dual conversion AM receiver designed for car radio applications. It includes a high dynamic range first mixer, local oscillator, second mixer and second oscillator, and a high gain AGC'd IF and detector. Also included is a signal strength output, two delayed RF AGC outputs for a cascode FET/bipolar RF amplifier and diode attenuator, a buffered IF output stage and a first local oscillator output buffer for driving a synthesizer. Frequency range of the first mixer and oscillator is 100 kHz to 50 MHz.

Applications include single band and multi–band car radio receivers, and shortwave receivers.

- Operation from 7.5 to 9.0 Vdc
- First Mixer, 3rd Order Intercept = 20 dBm
- Buffered First Oscillator Output
- Second Mixer, 3rd Order Intercept = +5.0 dBm
- No Internal Beats Between 1st and 2nd Oscillator Harmonics
- Signal Strength Output
- Limited 2nd IF Output for Frequency Counter Station Detector
- Adjustable IF Output Station Detector Level
- Adjustable RF AGC Threshold for Both Mixer Inputs
- Two Delayed AGC Outputs for Cascode RF Stage and Diode Attenuator

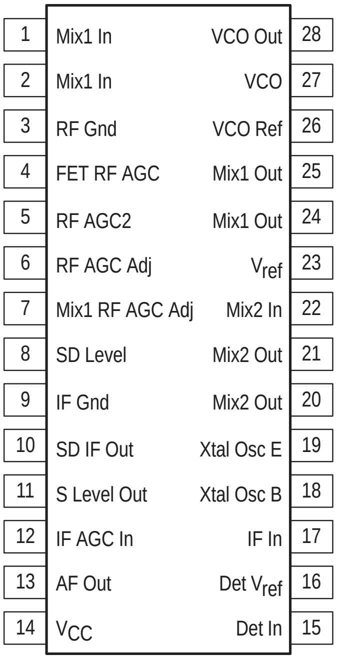
DUAL CONVERSION AM RECEIVER

SEMICONDUCTOR TECHNICAL DATA



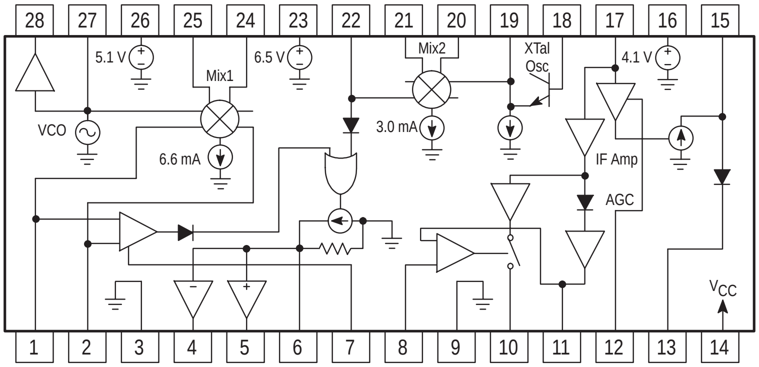
DW SUFFIX
PLASTIC PACKAGE
CASE 751F

PIN CONNECTIONS



(Top View)

Representative Block Diagram



This device contains 335 active transistors.

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC13030DW	T_A = –40° to +85°C	SOIC–28

MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply	V_{CC}	10	V
Operating Temperature	T_A	–40 to +85	°C
Storage Temperature	T_{stg}	–65 to +150	°C
Junction Temperature	T_J	150	°C

NOTE: ESD data available upon request.

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC} = 8.0 V, unless otherwise noted.)

Characteristic	Condition/Pin	Symbol	Min	Typ	Max	Unit
Power Supply Voltage	–	V_{CC}	7.5	8.0	9.0	V
Power Supply Current	V_{CC} = 8.0 V	I_{CC}	26	32	44	mA
Detector Output Level	V_{in} = 1.0 mV, 30% Mod.	V13	160	200	240	mVrms
Audio S/N Ratio	V_{in} = 1.0 mV, 30% Mod.	S/N	48	52	–	dB
Audio THD	V_{in} = 1.0 mV, 30% Mod. V_{in} = 1.0 mV, 80% Mod. V_{in} = 2.0 mV, 80% Mod.	THD	– – –	0.3 0.3 0.4	1.0 1.0 1.5	%
Signal Strength Output	V_{in} = 0 to 2.0 V	V11	0	–	5.2	V
VCO Buffer Output	–	V28	178	224	282	mV
SD Output Level	V_{in} = 1.0 mV, V11 > V8	V10	2.3	2.7	3.3	Vpp

MIXER1

Input Resistance	1 or 2 to Gnd	–	–	10	–	kΩ
Third Order Intercept Point	1 or 2	IP3	–	127	–	dBμV
Conversion Transconductance	1 or 2 to 24 + 25	g_c	–	2.2	–	mS
Total Collector Current	24 + 25	I_C	–	4.6	–	mA
Input IF Rejection	1 or 2	–	–	45	–	dB

MIXER2

Input Resistance	22	–	–	2.4	–	kΩ
Third Order Intercept Point	22	IP3	–	112	–	dBμV
Conversion Transconductance	22 to 20 + 21	g_c	–	4.6	–	mS
Total Collector Current	20 + 21	I_C	–	3.0	–	mA

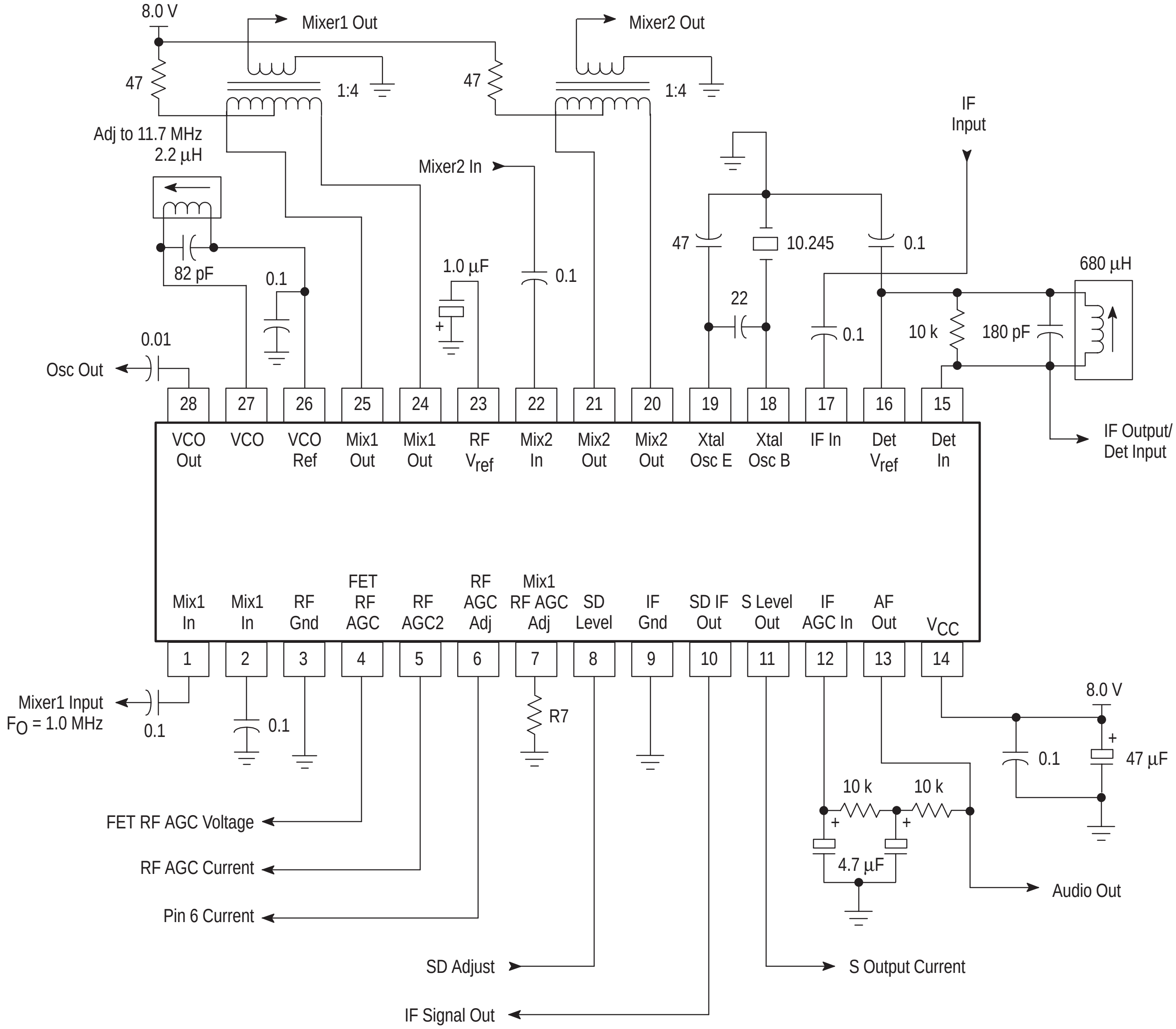
VCO

Minimum Oscillator Coil Parallel Impedance	27 to 26	R_P	–	3.0	–	kΩ
Buffer Output Level	28	V_O	–	224	–	mVrms
Stray Capacitance	27	C_S	–	7.0	–	pF

IF AMPLIFIER

Input Resistance	17	R_{in}	–	2.0	–	kΩ
Transconductance	17 to 15	g_m	–	28	–	mS
Maximum Input Level	17	V_{in}	–	125	–	mVrms
Minimum Detector Coil Parallel Impedance	17 to 15	R_L	–	15	–	kΩ
RF Output Level	15, V_{in} = 1.0 mV	–	–	2.0	–	Vpp
Audio Output Impedance	13	R_{out}	–	120	–	Ω
Audio Output Level	13 @ 30% Mod.	V_{out}	–	200	–	mVrms

Figure 1. Test Circuit



NOTES:
1. The transformers used for at the output of the mixers are wideband 1:4 impedance ratio. The secondary load is the 50 Ω input of the spectrum analyzer, so the impedance across the collectors of the mixer output is 200 Ω.
2. Since the VCO frequency is not critical for this measurement, a fixed tuned oscillator tuned to 11.7 MHz is used. This gives an input frequency of 1.0 MHz.
3. The detector coil is loaded with a 10 k resistor to reduce the tuned circuit Q and to present a 10 kΩ load to the IF output for determination of IF transconductance.
4. The RF AGC current, S output current and Pin 6 current are measured by connecting a current measuring meter to these pins, so they are effectively shorted to ground.
5. SD adjust is adjusted by connecting a power supply or potentiometer and voltmeter to Pin 8.

FUNCTIONAL DESCRIPTION

The MC13030 contains all the necessary active circuits for an AM car radio or shortwave receiver.

The first mixer is a multiplier with emitter resistors in the lower, signal input transistors to give a high dynamic range. It is internally connected to the first oscillator (VCO). The input pins are 1 and 2. The input can be to either Pins 1 or 2, or balanced. These pins are internally biased, so a dc path between them is allowable but not necessary. The mixer outputs are open collectors on Pins 25 and 26. They are normally connected to a tuned transformer.

The first oscillator on Pin 27 is a negative resistance type with automatic level control. The level is low so the signal does not modulate the tuning diode capacitance and cause distortion. Pin 26 is the reference voltage for the oscillator coil. This reference is also the supply for the mixer circuits. The upper bases of the mixer are 0.7 V below this reference.

The second mixer is similar to the first, but it is single–ended input on Pin 22. Its outputs are open collectors on Pins 20 and 21 which are connected to a tuned transformer. The dynamic range of this mixer is less than the first. It is also connected internally to an oscillator which is normally crystal controlled. The oscillator is a standard Colpitts type with the emitter on Pin 19 and the base on Pin 18.

The IF amplifier input is Pin 17. The AGC operates on the input stage to obtain maximum dynamic range and minimum distortion. The IF output, Pin 15, is a current source.

Therefore, its gain is determined by the load impedance connected between Pins 15 and 16. Pin 16 is a voltage reference for the output. The output is internally connected to the AM detector, and Pin 13 is the detector output. This detector also provides the AGC signal for the IF amplifier. An RC filter from Pin 13 to 12 removes the audio, leaving a dc level proportional to the carrier level for AGC.

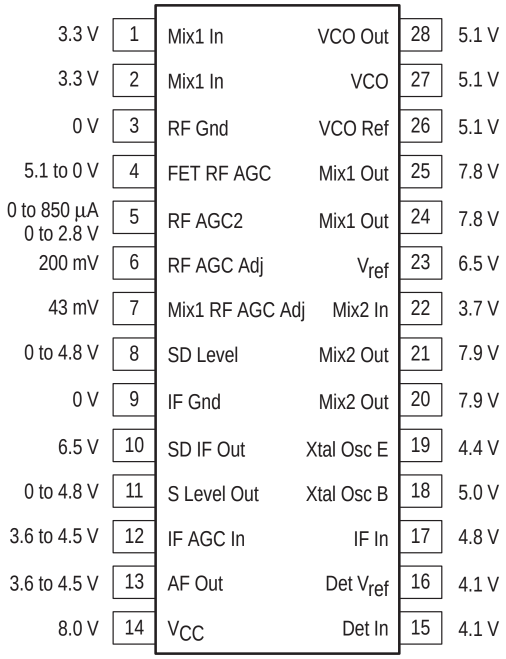
Pin 11 provides a current proportional to signal strength. It is a current source so a resistor must be connected from Pin 11 to ground to select the desired dc voltage range. The current is proportional to the signal level at Pin 17, the IF amplifier input.

A high–gain limiting amplifier is used to derive the station detect (SD) signal output on Pin 10; this output is present only if it is turned on by the voltage on Pin 8. If the voltage on Pin 8 is less than the voltage on Pin 11, the output on Pin 10 is "on". The station detector IF output on Pin 10 is used with synthesizers which have a frequency counting signal detector.

The RF AGC outputs on Pins 4 and 5 are controlled by the signal levels at Mixer1 or Mixer2. Bypass capacitors are required on Pins 6 and 4 to remove audio signals from the AGC outputs. Pin 4 is designed to control the NPN transistor in series with the RF amplifier FET. The voltage on Pin 4 is 5.1 V with no input signal and decreases with increasing input signal. Pin 5 is designed to control an additional AGC circuit at the antenna input. The voltage on Pin 5 is at 0 V with no input signal and increases with increasing input signals. The voltage on Pin 5 does not increase until the voltage on Pin 4 has decreased to about 1.3 V. In most cases, Pin 5 is used to drive a diode shunt. Maximum output current is about 850 µA.

The RF AGC sensitivity is about 40 mVrms input to Mixer1 or about 2.0 mVrms input to Mixer2 at 1.0 MHz. The AGC sensitivity for both mixers can be decreased by adding a resistor from Pin 6 to ground. There is also an additional amplifier between Mixer1 and its AGC rectifier. The gain of this amplifier and AGC sensitivity for Mixer1 can be increased by adding a resistor from Pin 7 to ground. Therefore, the desired AGC sensitivity for both mixers can be achieved by changing the resistors on Pins 6 and 7.

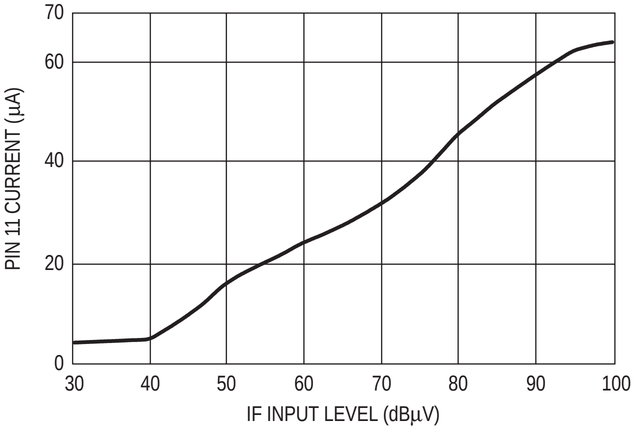
Figure 2. Pin Connections and DC Voltages



S Out versus IF Input:

The S output current at Pin 11 is provided by two collectors, one a PNP source and the other a sink to ground. The desired S output voltage can be selected using the curve of Figure 3 and calculating the value of the required resistor.

Figure 3. S Output Current versus IF Input Level



RF FET AGC versus Mixer1 and Mixer2 Input Level:

Figures 4 and 5 are generated with no external resistance on Pins 4 or 6, so they represent the minimum RF AGC sensitivity of Mixer1 and Mixer2.

Figure 4. RF AGC Voltage versus Mixer1 Input

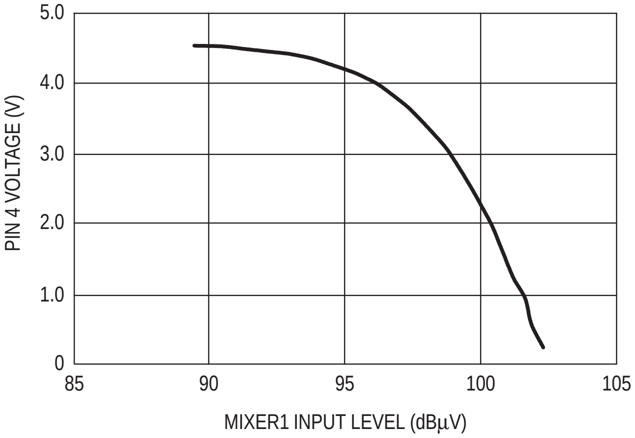
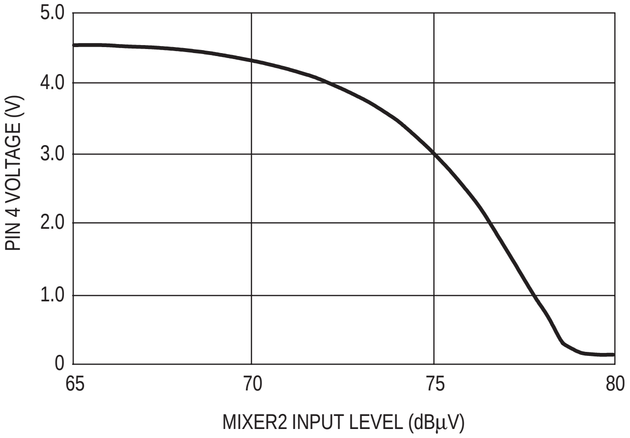


Figure 5. RF AGC Voltage versus Mixer2 Input



Pin 6 Current versus Mixer1 and Mixer2 Input Level:

The internal resistance from Pin 6 to ground is 39 k. The RF AGC voltage on Pin 4 is 2.0 V when the voltage on Pin 6 is 1.2 V. Therefore, the desired AGC thresholds for either mixer can be set with these curves. The design steps are described in the design notes.

Figure 6. Pin 6 Current versus Mixer1 Input Level

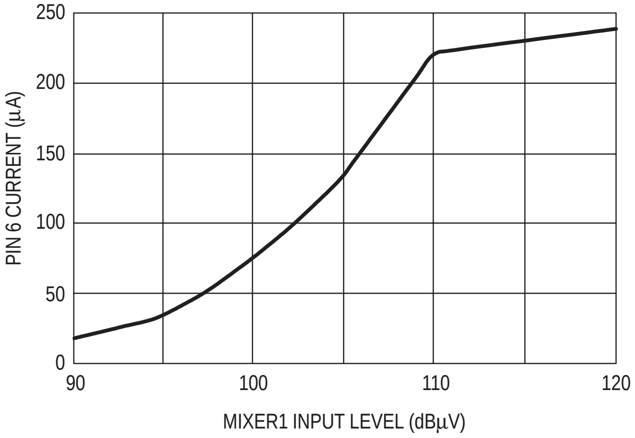
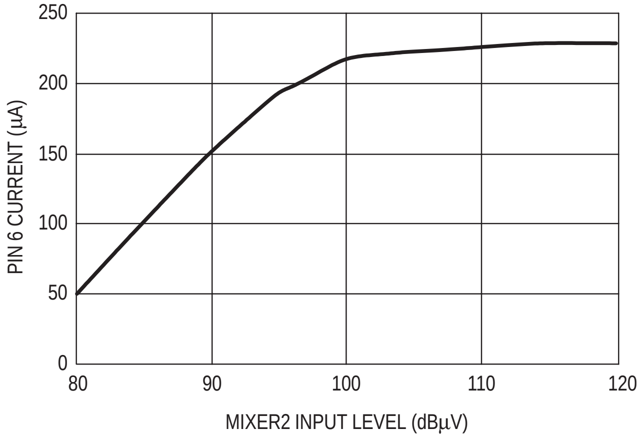


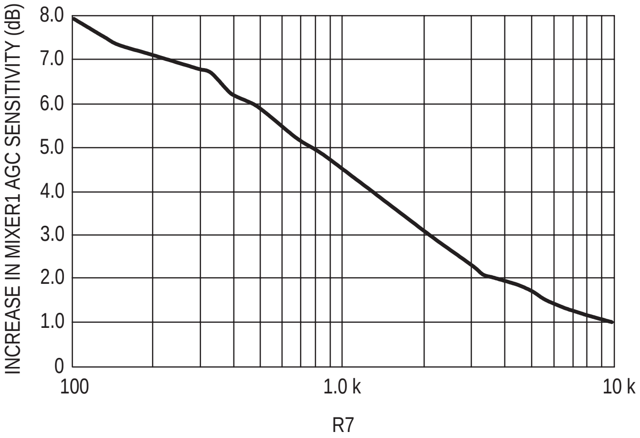
Figure 7. Pin 6 Current versus Mixer2 Input Level



Mixer1 AGC Gain Increase versus R7:

Adding a resistor from Pin 7 to ground increases the AGC sensitivity of Mixer1. The range of increase in dB can be found from this curve. This is useful after setting up the AGC threshold of Mixer2.

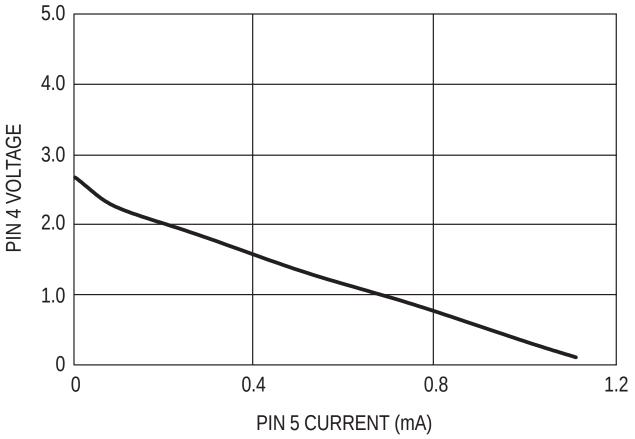
Figure 8. Mixer1 AGC Gain Increase versus R7



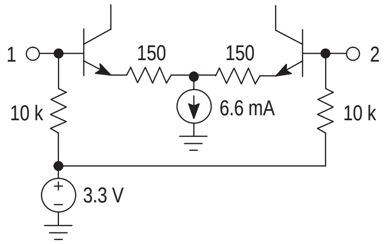
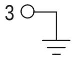
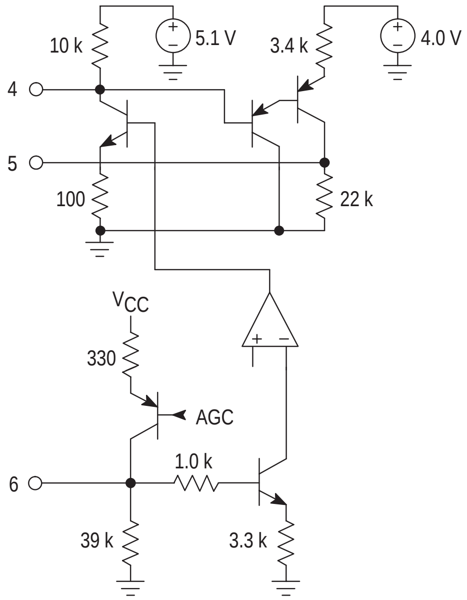
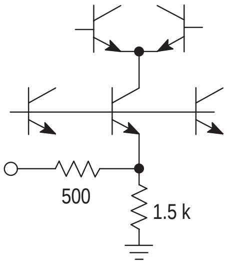
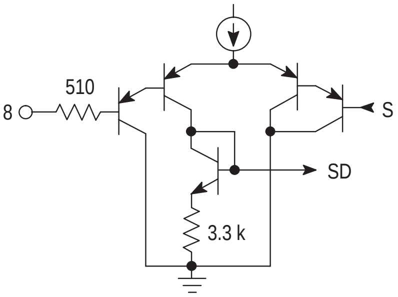
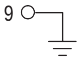
Pin 5 Current versus Pin 4 Voltage:

All the curves give Pin 4 AGC voltage versus some other input level. This curve can be used to determine the auxiliary AGC current from Pin 5 at a given Pin 4 voltage.

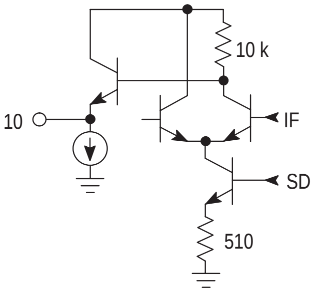
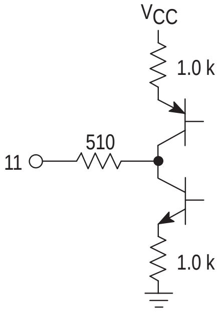
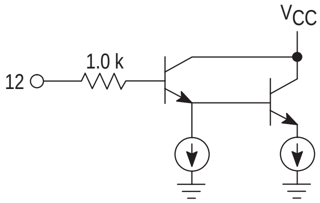
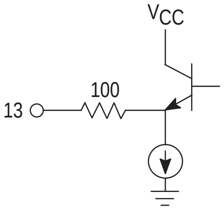
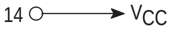
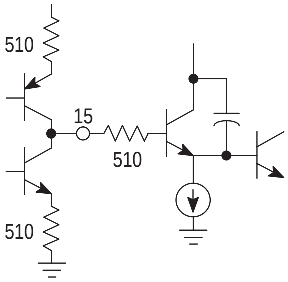
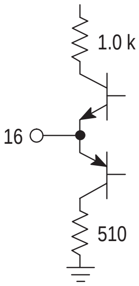
Figure 9. Pin 5 Current versus Pin 4 Voltage



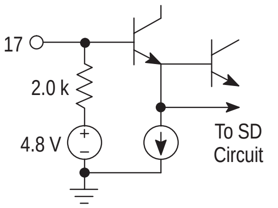
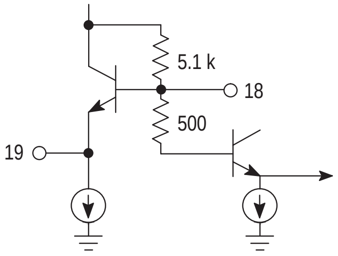
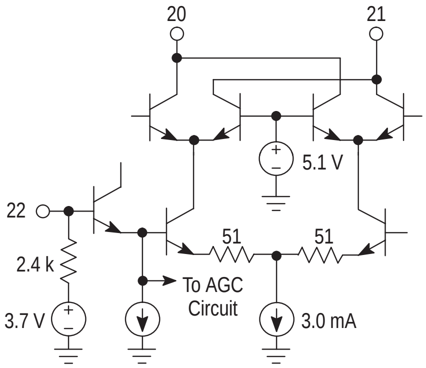
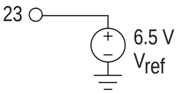
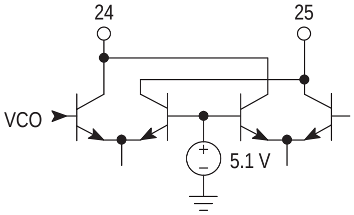
PIN FUNCTION DESCRIPTION

Pin No.	Internal Equivalent Circuit	Description
1, 2	 	**Mixer1 Input** Pins 1 and 2 are equivalent. In the application circuit, 2 is grounded with a capacitor and 1 is the input. If a load resistor is needed for the input filter, it can be placed across Pins 1 and 2. Input impedance for each pin is 10 k. IP3 (third order intercept) at the input is 20 dBm (127 dBμ). To guarantee –50 dB IM3, the input level should not be greater than 3.5 dBm (103 dBμ) (150 mVrms).
3	 	**RF Ground** This should be connected to the ground used for the RF circuits.
4	 	**FET RF AGC Output** This is the AGC for the cascode transistor connected to the RF amplifier FET. The no–signal voltage is 5.1 V. The voltage decreases with increasing input signals. A bypass capacitor and electrolytic capacitor must be added to filter out RF signals on the transistor and audio signals in the AGC signal. See Figures 4 and 5.
5		**RF AGC2 Output** The voltage on this pin starts at 0 and increases with increasing input signals. It is normally used to turn on diodes or a transistor connected across the antenna input and is AGC delayed until Pin 6 reaches 2.7 V. If the voltage on Pin 5 decreases below 2.0 V, the voltage on this pin will decrease from 3.1 down to about 1.5 V. The maximum output current is about 850 μA.
6		**RF AGC Adjust** An electrolytic capacitor of 1.0 μF must be connected to prevent audio modulation of the AGC circuits. If there is no resistor on this pin, the RF AGC starts at an input level to Mixer1 ≈ 40 mVrms or Mixer2 ≈ 2.0 mVrms. Connecting a resistor from Pin 6 to ground increases RF levels required for AGC to start. It should be used to set the desired AGC level of Mixer2. If a resistor is not connected to Pin 6, unwanted RF signals will cause the AGC to start at a very low level, and desired signals may be suppressed.
7	 	**Mixer1 RF Level Adjust** A resistor from Pin 7 to ground will increase the gain of an amplifier from the input of Mixer1 to the AGC circuit. It can be used to set the RF AGC level of Mixer1. The minimum value of R7 is about 680 Ω.
8	 	**Station Detector Signal Level Adjust** A voltage on Pin 8 will set the desired signal strength at which the SD IF Out on Pin 10 appears. The other input to this comparator is the S (signal strength) signal. If Pin 8 is grounded, a square wave of the 2nd IF (usually 450 of 455 kHz) is present with very small input levels. This output could also be used to drive an FM detector if desired.
9	 	**IF Ground** Pin 9 is the ground for the IF section.

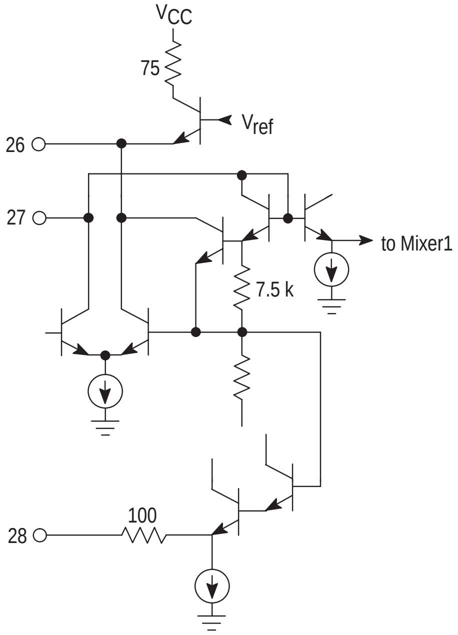
PIN FUNCTION DESCRIPTION (continued)

Pin No.	Internal Equivalent Circuit	Description
10		**Station Detector IF Output** This output is "on" when V11 > V8. The output is an amplified and limited 2nd IF signal. The signal level is ≈ 250 mVpp when it is 100% "on".
11		**S Level Output** This is a dc current proportional to IF input level. With a load resistor of 75 k, the dc voltage is 0 to 5.1 V.
12		**IF AGC In** The IF gain is controlled by the dc voltage on this pin. It is normally connected to Pin 13 through an RC network to filter out the audio signal on Pin 13. The IF gain is maximum when V13 ≈ 3.6 V. When V13 increases, the IF gain decreases.
13		**Audio Output** The dc voltage on Pin 13 is ≈ 3.6 V with no input signal and increases to ≈ 4.5 V at minimum IF gain. A nonpolarized electrolytic capacitor may be required to couple to the audio circuits if the audio amplifier dc bias voltage is between these voltages.
14		**Supply Voltage** The nominal operating voltage is 8.0 V.
15		**IF Amplifier Output and Detector Input** The detector coil must be connected between Pin 15 and 16. The IF amplifier output is a current source, the IF amplifier is a transconductance amplifier; the gain is determined by the impedance between Pins 15 and 16. The IF amplifier g_m ≈ 0.028 mho. If a wide bandwidth IF is desired, the detector coil can be connected between Pins 15 and 16 without a tap and then loaded with a resistor across the coil.
16		**Detector Reference Voltage** One side of the detector coil is connected to this pin. It should be bypassed with a 0.1 µF capacitor.

PIN FUNCTION DESCRIPTION (continued)

Pin No.	Internal Equivalent Circuit	Description
17		**IF Input** The IF input impedance is 2.0 k to match most ceramic 455 or 450 kHz filters. For a ceramic filter requiring a 1.5 k load, a 5.6 k resistor in series with a 0.01 µF capacitor should be connected from Pin 17 to ground.
18		**Crystal Oscillator Base** The crystal oscillator is a simple Colpitts type, operating at a low current. The crystal should operate at 10.250 MHz for 450 kHz IF or 10.245 MHz for 455 kHz IF with a 20 pF load capacitance. The oscillator signal to the second mixer is coupled from Pin 18 through an emitter follower. If a synthesizer such as the Motorola MC145170 with a 15 bit programmable R counter is used, the 10.245 MHz crystal can be connected to the synthesizer, and a 200 mVpp oscillator signal from the synthesizer can be capacitively coupled to Pin 18, so only one crystal is needed.
19		**Crystal Oscillator Emitter** The capacitive divider from Pin 18 is connected as shown in the application circuits of Figures 10, 11, 12.
20, 21		**Mixer2 Output** The maximum AC collector voltage is about 5.8 Vpp or 2.0 Vrms. The mixer conversion transconductance g_C = 0.0046 mho. The load impedance should be selected so the mixer output does not overload before the input.
22		**Mixer2 Input** The input impedance is 2.4 k. A series R–C network from Pin 22 to ground or a resistor from the filter to Pin 22 can be used to properly match the filter. In most cases, a 10.7 MHz crystal filter can be connected to Pin 22 directly without any additional components. IP3 (third order intercept) at the input is 5.0 dBm (112 dBµ). To guarantee –50 dB IM3, the input level should not be greater than –20 dBm (87 dBµ) (22.7 mVrms).
23		**V_{ref}** This is the main reference voltage for most of the circuits in the IC and should be bypassed with a 1.0 µF capacitor.
24, 25		**Mixer1 Output** The maximum collector voltage is about 5.8 Vpp or 2.0 Vrms. The mixer conversion transconductance g_C = 0.0022. The load impedance should be selected so the mixer output does not overload before the input.

PIN FUNCTION DESCRIPTION (continued)

Pin No.	Internal Equivalent Circuit	Description
26		**VCO Reference** The first oscillator coil is connected from Pin 26 to 27. Pin 26 must be bypassed to ground with a capacitor which has a low impedance at the oscillator frequency. This capacitor also will reduce the phase noise of the VCO.
27		**VCO** The VCO is a negative resistance type and has an internal level control circuit so a tapped coil or one with a secondary is not needed. The level is fixed at 0.8 Vpp so the oscillator signal does not modulate the tuning diode, thus keeping the distortion low. The oscillator stray capacitance is ≈ 12 pF and the tuned circuit impedance should be greater than 3.0 k to guarantee oscillation. Oscillator range is up to 45 MHz so it can be used for SW receivers.
28		**VCO Out** The output level is 240 mVrms (108 dBμ), high enough to drive any CMOS synthesizer.

AM CAR RADIO DESIGN NOTES

The MC13030 AM Radio IC is intended for dual conversion AM radios. In most cases, the 1st IF frequency (F_{IF1}) is upconverted above the highest input frequency. The first oscillator (VCO) is tuned by a synthesizer and operates at $F_{in} + F_{IF1}$. For the 530 to 1700 kHz AM band with a 10.7 MHz first IF, the VCO goes from 11.23 to 12.40 MHz. Therefore, F_{max}/F_{min} for VCO is only 1.104, so one low–cost tuning diode can be used. Since the required tuning voltage range can be made less than 5.0 V, it may also be possible to drive the tuning diode directly or from the phase detector of the synthesizer IC, such as the Motorola MC145170, operating from 5.0 V, without using a buffer amplifier or transistor.

If the VCO is above the incoming frequency, the image frequency of the first mixer is at $f_{OSC} + F_{IF1}$. For the AM broadcast receiver, it is around 22 MHz, so a simple LPF can be used between the RF stage and Mixer1 input. However, if a LPF is used, an additional coil is still needed to supply the collector voltage of the RF amplifier. For this reason, a BPF filter was used in the application circuit instead, since it uses the same number of coils and gives better performance. It is simply a lowpass to bandpass conversion. The lowpass filter is designed to have a cutoff frequency equal to the desired bandwidth. In this case, it would be 1700 – 530 kHz = 1170 kHz. Then, it is transformed to be resonant at 949 kHz, the geometric mean of the end frequencies: $\sqrt{1700 \times 530} = 949$ kHz.

A balanced–to–unbalanced transformer is required at the output of both mixers. The first one is designed so that Mixer1 has enough gain to overcome the loss of the 10.7 MHz filter and so that the output of the mixer will not overload before the input. The primary impedance of the transformer is relatively low, and it may be difficult to control with commonly available 7.0 mm transformers because the number of primary turns is quite small. It would also require a large tuning capacitance. A better solution is to tune the secondary with a small capacitance and then use a capacitive divider to match the tuned circuit to the filter. This allows one transformer to be used for either a ceramic or crystal filter. The capacitors can be adjusted to match the filter. The recommended coil is made this way.

If the formula: $P_{in} = \text{IP3} - \text{DR}/2$ is used, the maximum input level to the mixer can be calculated for a desired dynamic range.

IP3 = 3rd order intercept level in dB (dBm or dBμ)

DR = dynamic range in dB between the desired signals and 3rd order intermodulation products

P_{in} = input level in dBm or dBμ

The RF AGC level can then be adjusted so that P_{in} does not exceed this level.

Whether or not a narrow bandwidth crystal or wide bandwidth ceramic filter is used between the first and second mixers depends on the receiver requirements. It is possible to achieve about 50 dB adjacent channel and IM rejection with a ceramic filter because of the wide dynamic range of the mixers. If more than this is required, a crystal filter should be used. If a crystal filter is used, a lower cost CFU type of 455 kHz second IF filter can be used. If a ceramic filter is used, a CFW type filter should be used because there is no RF section selectivity in this type of radio.

Since the wideband AGC system is quite sensitive, it can be set to eliminate all spurious responses present at the receiver output. However, the RF AGC will sometimes eliminate or reduce the level of desired signals if there is a strong signal somewhere in the bandpass of the RF circuit.

The second mixer is designed like the first and requires a balanced output. Since its load impedance is higher, the transformer can be designed to be tuned on the primary or secondary, but, like with the one for the first mixer, if the secondary is tuned, the tap can be adjusted for the impedance of the 455 kHz filter. Wideband filters usually have a higher terminating resistance than the narrowband ones. The recommended coil is made this way.

The IF amplifier is basically a transconductance amplifier because the output is a current source. The output is also internally connected to a high impedance AM detector. g_m for the IF amplifier is ≈ 0.028 mho. The voltage gain will be the detector coil impedance x 0.028. This can be designed to give the desired audio output level for a given RF input level. If it is set too high, the receiver may oscillate with no input signal. The application circuit was designed for a relatively narrow bandwidth, so a tapped detector coil is used to get the desired gain. If a wide bandwidth receiver is desired, the detector coil can be untapped, and a resistor can be added across the coil to get the desired Q.

The detector output on Pin 13 is a low impedance. It supplies the IF AGC signal to Pin 12, so the audio must be filtered out. The time constant of this filter is up to the designer. The main requirement is usually the allowable audio distortion at 100 Hz, 80% modulation. If the time constant is made too long, the audio level will be slow to correct when changing stations.

The Signal Strength (S) output is dependent only on the IF amplifier input level. Its maximum voltage is about 5.0 V with a 75 k load resistor. The range can be reduced by using a lower value for the resistor on Pin 11. The S signal will stop increasing when the RF AGC circuits become active, so if the RF AGC threshold is set too low, or there is too much loss from the Mixer2 output to the IF input, the maximum S signal will be reduced. The desired load resistor on Pin 11 (R11) can be determined using the curve of Pin 11 current versus IF input.

Setting the RF AGC threshold is probably the most difficult because a trade–off between allowable interference and suppression of desired signals must be made.

First select the values for both mixers:

d. Using the formula P_{in} = IP3 – DR/2
Select the desired dynamic range and calculate the maximum input levels for both mixers. Remember that all levels must be in dB, dBμV or dBm. Let DR = 50 dB. IP3 for Mixer2 = 112 dBμV. Therefore, P_{inmax} = 87 dBμV. IP3 for Mixer1 = 127 dBμV. Therefore, P_{inmax} = 102 dBμV.

e. First, adjust the resistor from Pin 6 to ground to give the desired maximum input level to Mixer2. From the curve of Pin 6 current versus Mixer2 input level, R6 = 1.2/110 μA = 11 k. R_{int} = 39 k, so R_{6ext} = 15 k.

f. From the curve of Pin 6 current versus Mixer1 input level, determine how much more gain would be required in the Mixer1 AGC circuit to achieve the desired dynamic range for Mixer1. From the curve of Relative Sensitivity versus R7 determine the value of R7. Alternatively, R7 can be adjusted to give the desired maximum input level to Mixer1.

The resulting R7 may be too small to set the AGC threshold of Mixer1 as low as desired. Also, if R7 is less than 680 Ω, the AGC sensitivity for the Mixer1 input falls off at higher frequencies, so in these cases, the resistor from Pin 6 to ground must be reduced to achieve the desired level because the overload of Mixer1 provides the most important spurious response rejection. However, if the AGC level is set too high, the IF in signal may become too large and the IF amplifier can overload with strong signals. The values used in the application are more conservative.

The gain from the antenna input to the point being measured are shown on the AM radio application. These are helpful when calculating audio sensitivity and troubleshooting a new radio.

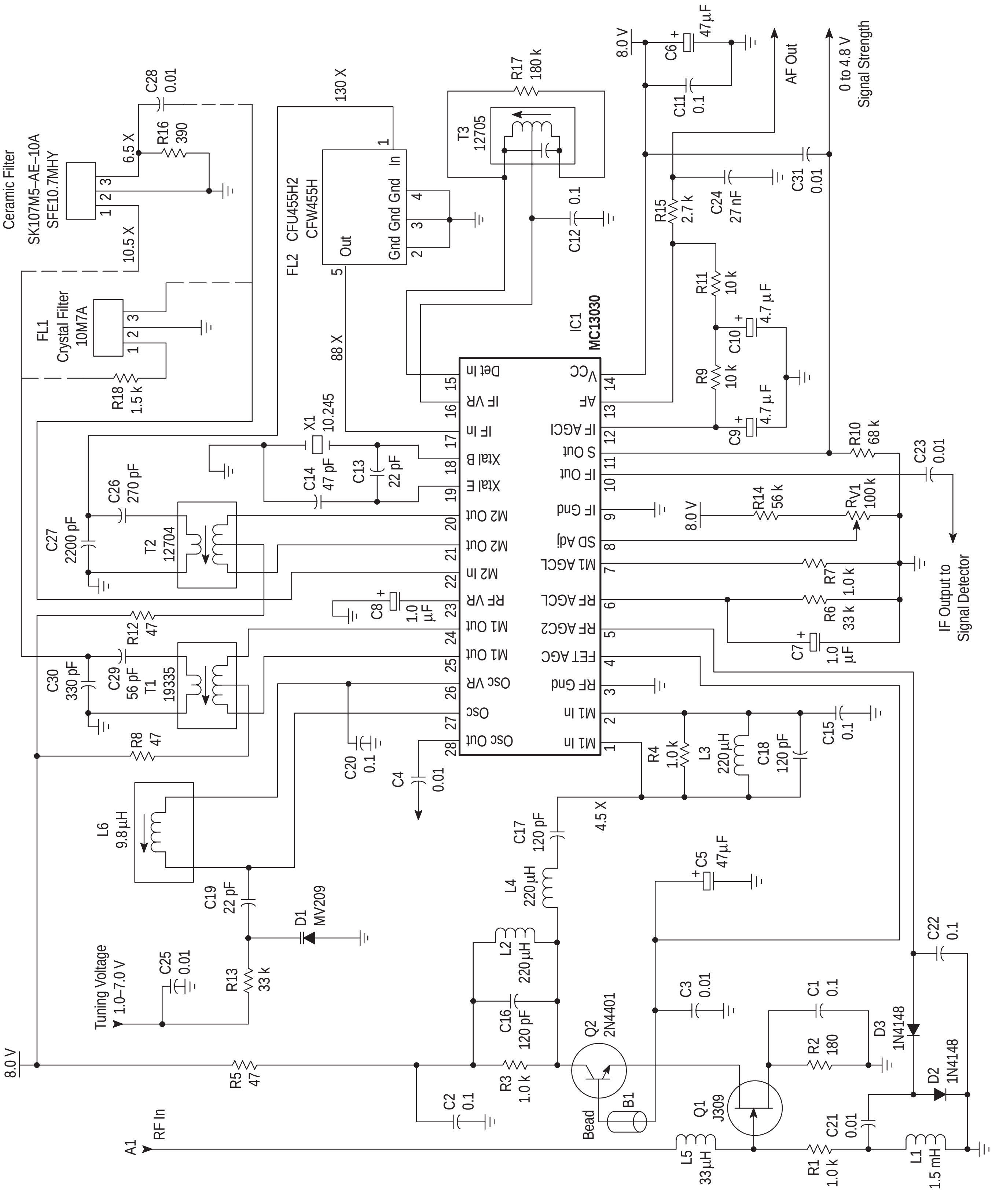


Figure 10. AM Radio Application

SW RADIO DESIGN NOTES

The shortwave receiver was designed to cover from 5.0 to 10 MHz. This MC13030 radio has better performance than most receivers because of the high dynamic range and spurious rejection of the mixers.

The RF stage bandpass filter for this radio is the same type as the one used for the car radio, but the series tuned section was scaled down in impedance to reduce the inductance of the coil.

Since most SW receivers include an SSB and CW mode, the detector coil could have a secondary winding to supply the second IF signal to this section.

The capacitors C10 and C23 have been reduced from those in the AM radio so that the AGC system can follow variations in signal level due to fading.

CB RADIO DESIGN NOTES

The RF stage bandpass filter for this radio consists of a tuned input and a double tuned interstage filter. For lower cost radios, a single tuned interstage filter could be used.

The schematic also shows a crystal 10.7 MHz 1st IF filter, but a ceramic or coil filter could also be used. An intermodulation rejection of 50 dB can be obtained with a ceramic 1st IF filter.

A bipolar transistor is shown for the RF stage. A dual gate CMOS FET could also be used with G2 connected to the AGC voltage on Pin 4. A PIN diode is recommended for D2.

COIL DATA

T1 – Toko A119ANS–19335UH

T2 – Toko A7MNS–12704UH

T3 – Toko A7MCS–12705Y

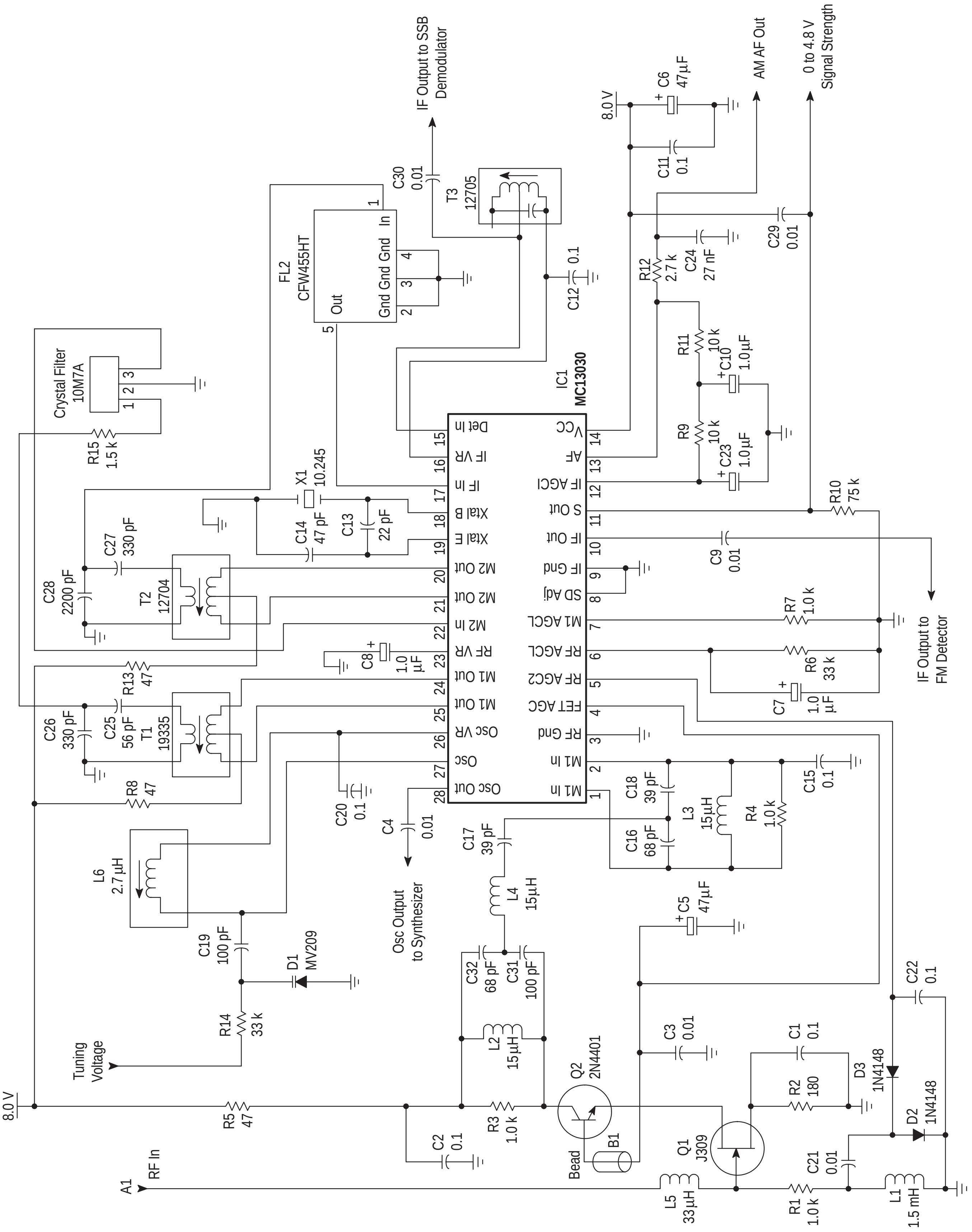


Figure 11. 5 to 10 MHz Radio Application

Figure 12. CB Radio Application

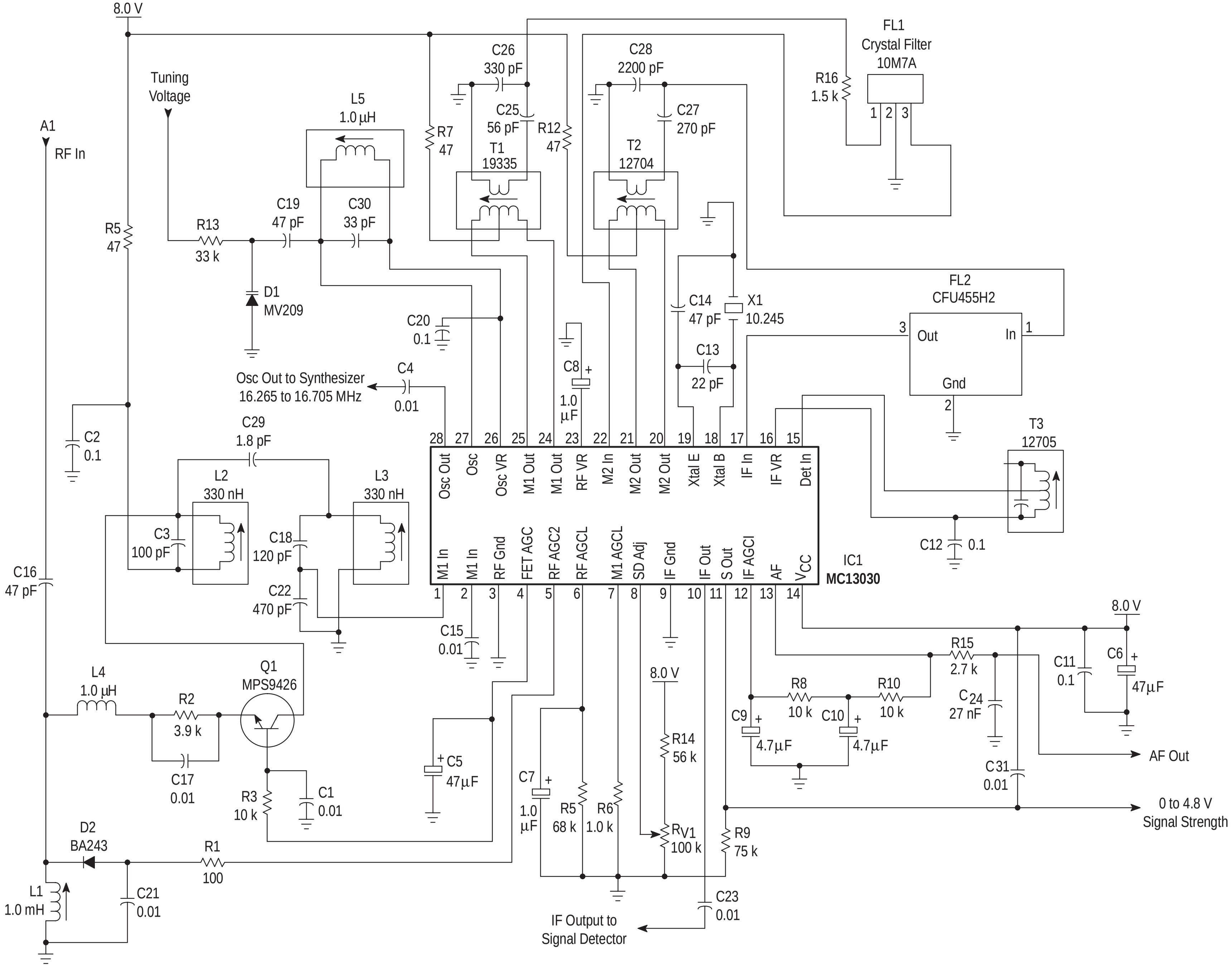
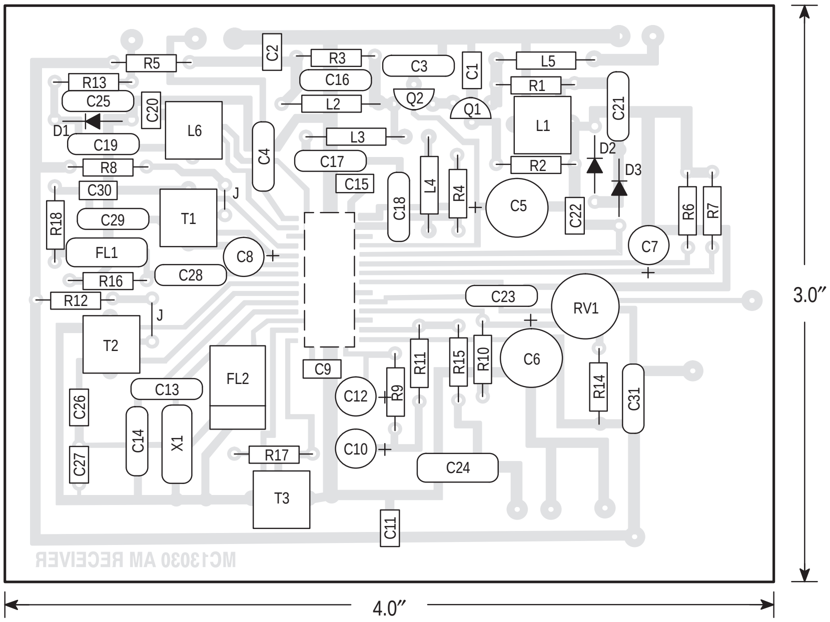
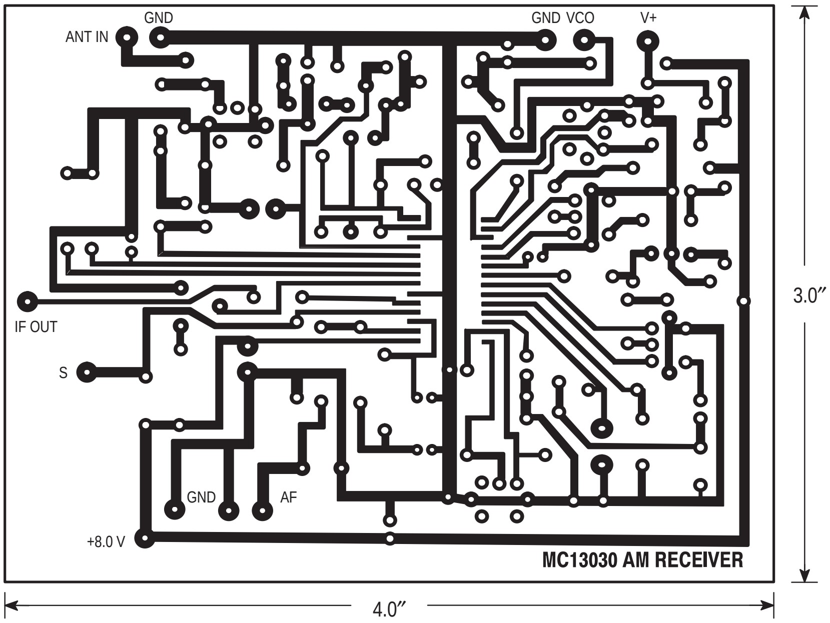


Figure 13. Printed Circuit Board



(Top View)

NOTE: J = Jumper



(Bottom View)

MOTOROLA

MC13060

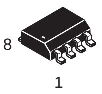
Mini-Watt Audio Output

This device is a rugged and versatile power amplifier in a remarkable plastic power package.

- Supply Voltages from 6.0 Vdc to 35 Vdc
- 2.0 W Output @ 70°C Ambient on PC Board with Good Copper Ground Plane
- Self Protecting Thermal Shutdown
- Easy to Apply, Few Components
- Gain Externally Determined
- Output is Independent of Supply Voltage Over a Wide Range

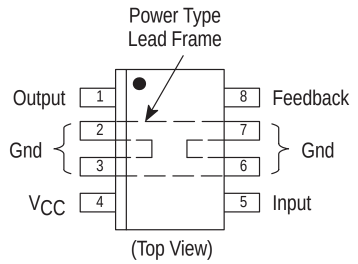
MINI–WATT AUDIO OUTPUT

SEMICONDUCTOR TECHNICAL DATA



D SUFFIX
PLASTIC PACKAGE
CASE 751
(SOP–8)

PIN CONNECTIONS



ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC13060D	T_A = – 40 to +85°C	SOP–8

Figure 1. Simplified Application

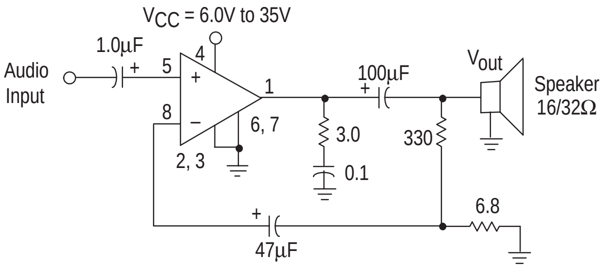
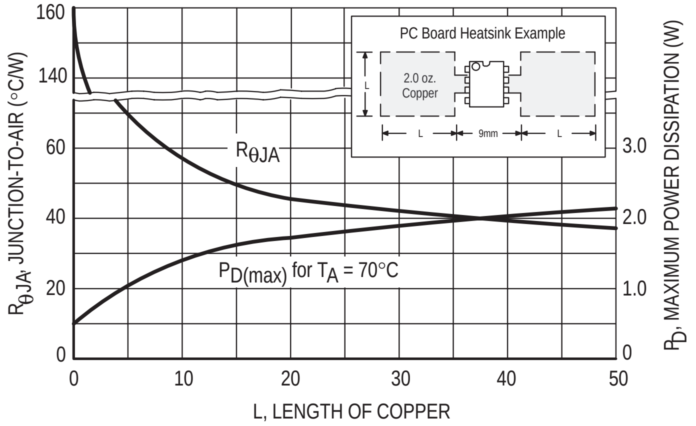


Figure 2. Thermal Resistance & Maximum Power Dissipation versus PC Board Copper



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	35	V
Audio Input, Pin 5		1.0	V_{pp}
Thermal Resistance, Junction to Air	$R_{\theta JA}$	160	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	25	°C/W
Junction Temperature	T_J	150	°C
Operating Ambient Temperature Range	T_A	–40 to +85	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

ELECTRICAL CHARACTERISTICS (TA = 25°C, circuit of Figure 3, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
AUDIO SECTION					
Power Supply Current, No Signal	I_{CC}	–	13	–	mAdc
Gain	A_o	–	50	–	V/V
Distortion at 62.5 mW Output, 1.0 kHz	THD	–	0.2	1.0	%
Distortion at 900 mW Output, 1.0 kHz	THD	–	0.5	3.0	%
Quiescent Output Voltage, No Signal	$V_{Pin\ 1}$	–	8.4	–	Vdc
Input Bias	$V_{Pin\ 5}$, $V_{Pin\ 8}$	–	0.7	–	Vdc
Input Resistance	R_{in}, Pin 5	–	28	–	kΩ
Output Noise (50 Hz to 15 kHz) Input 50 Ω	V_{out}	–	0.5	4.0	mVrms

GENERAL DESCRIPTION

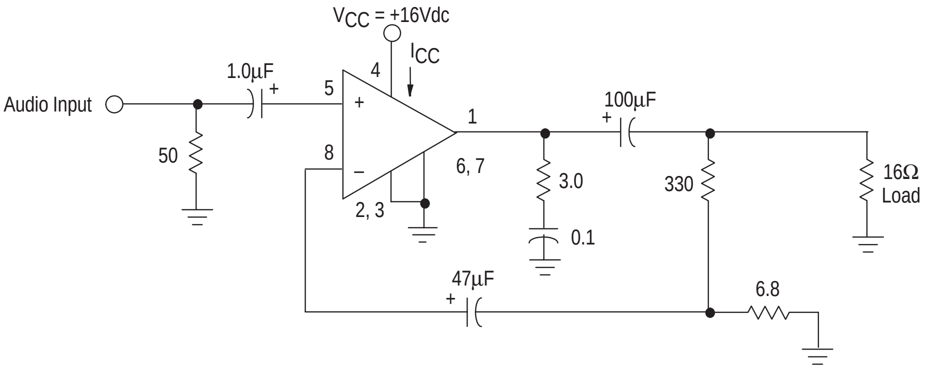
The MC13060 is a quasi–complementary audio power amplifier, mounted in the SOP 8 (power SOIC package). It is well suited to a variety of 1.0 W and 2.0 W applications in radio, TV, intercom, and other speaker driving tasks. It requires the usual external components for high frequency stability and for gain adjustment.

The output signal voltage and the power supply drain current are very linearly related, as shown in Figure 5. Both are quite constant over wide variation of the power supply voltage (above minimum V_{CC} for clipping, of course). The amplifier can best be described as a voltage source with about 1.0 A_{pp} capability. On a good heatsink, it can deliver over 2.0 W at 70°C ambient.

The MC13060 will automatically go into shutdown at a die temperature of about 150°C, effectively protecting itself, even on fairly stiff power supplies. This eliminates the need for decoupling the power supply, which degrades performance and requires extra components.

Input Pins 5 and 8 are internally biased at 0.7 Vdc and should not be driven below ground.

Figure 3. Test Circuit



All Curves Taken in the Test Circuit of Figure 3, Unless Otherwise Noted.

Figure 4. Quiescent Supply Current and Output Voltage versus Supply Voltage

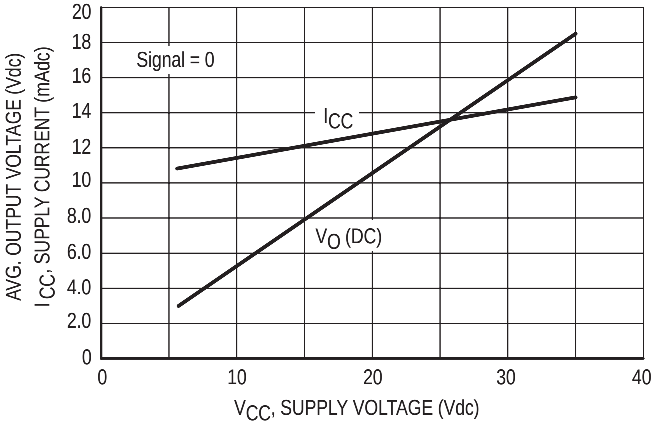


Figure 5. Supply Current versus Output

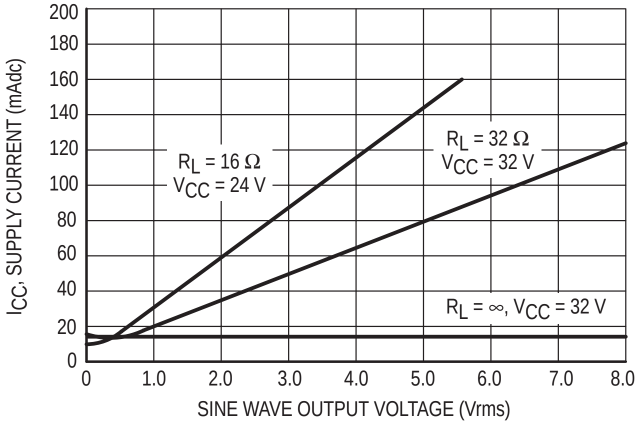


Figure 6. Distortion and Gain versus Frequency

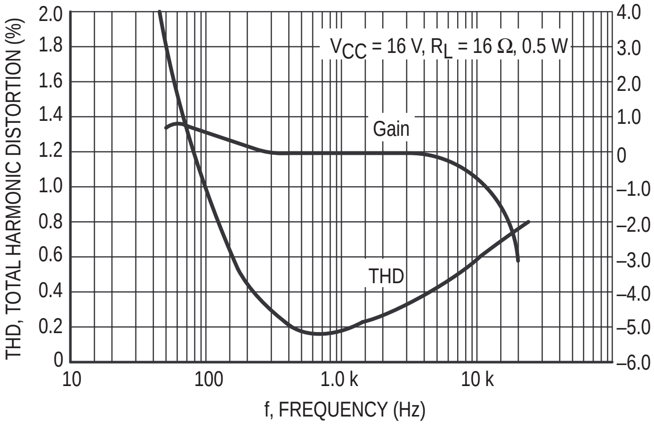


Figure 7. Distortion versus Power Output

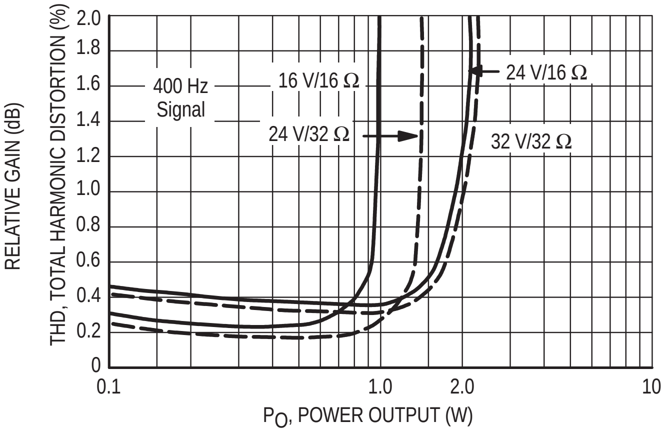


Figure 8. Dissipation versus Output Power

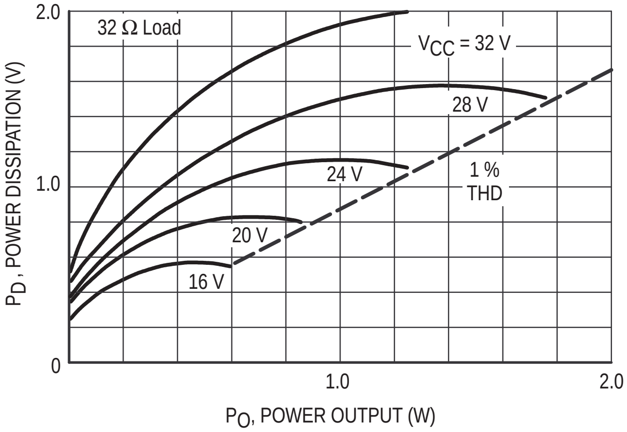


Figure 9. Dissipation versus Output Power

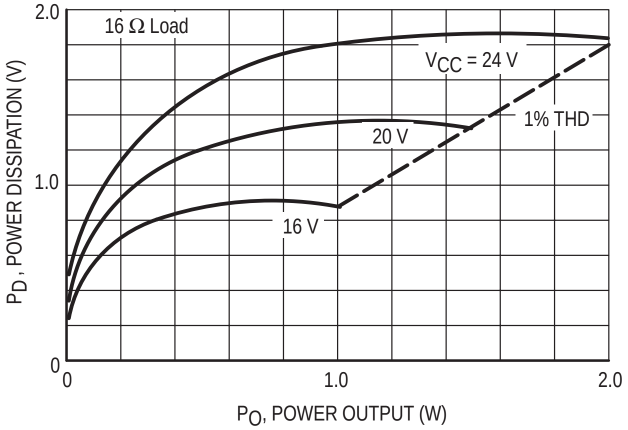
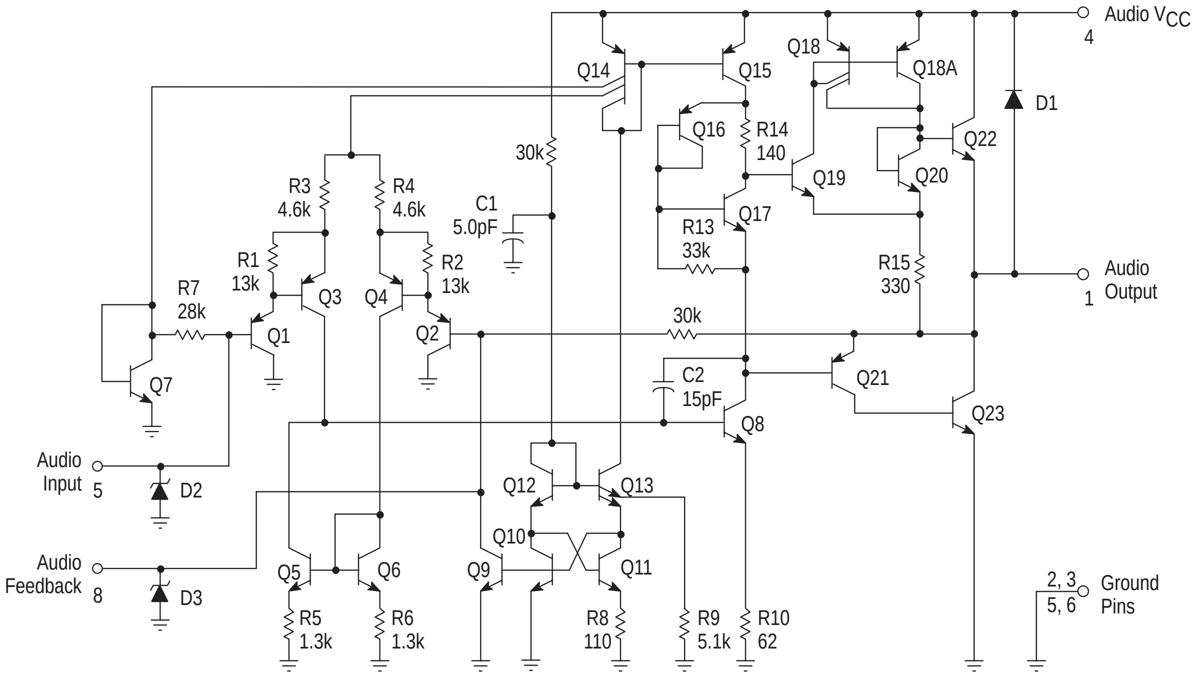


Figure 10. Representative Schematic Diagram



MC13077

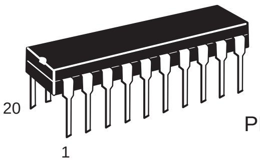
Advanced PAL/NTSC Encoder

ADVANCED
PAL/NTSC ENCODER

SEMICONDUCTOR
TECHNICAL DATA

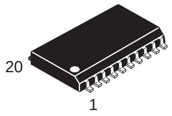
The MC13077 is a high quality RGB/YUV to NTSC/PAL encoder with Composite Video and S–Video outputs. The IC integrates the color difference and luma matrix circuitry, chroma modulators, subcarrier oscillator, and logic circuitry to encode component video into a composite video signal compatible with the NTSC/PAL standards. The IC operates off a standard +5.0 V supply and typically requires less than 75 mA, making it useful in PC environments. The high degree of integration saves board space and cost, as only passive external components are required for operation. The IC is manufactured using Motorola's MOSAIC™ process and is available in a 20 pin DIP or SOIC package.

- Single 5.0 V Supply
- Composite Output
- S–Video Outputs
- PAL/NTSC Switchable
- PAL Squarewave Output
- PAL Sequence Resettable
- Internal/External Burst Flag
- Digitally Determined Modulator Axes
- Subcarrier Reference Drive Selectable



P SUFFIX
PLASTIC PACKAGE
CASE 738

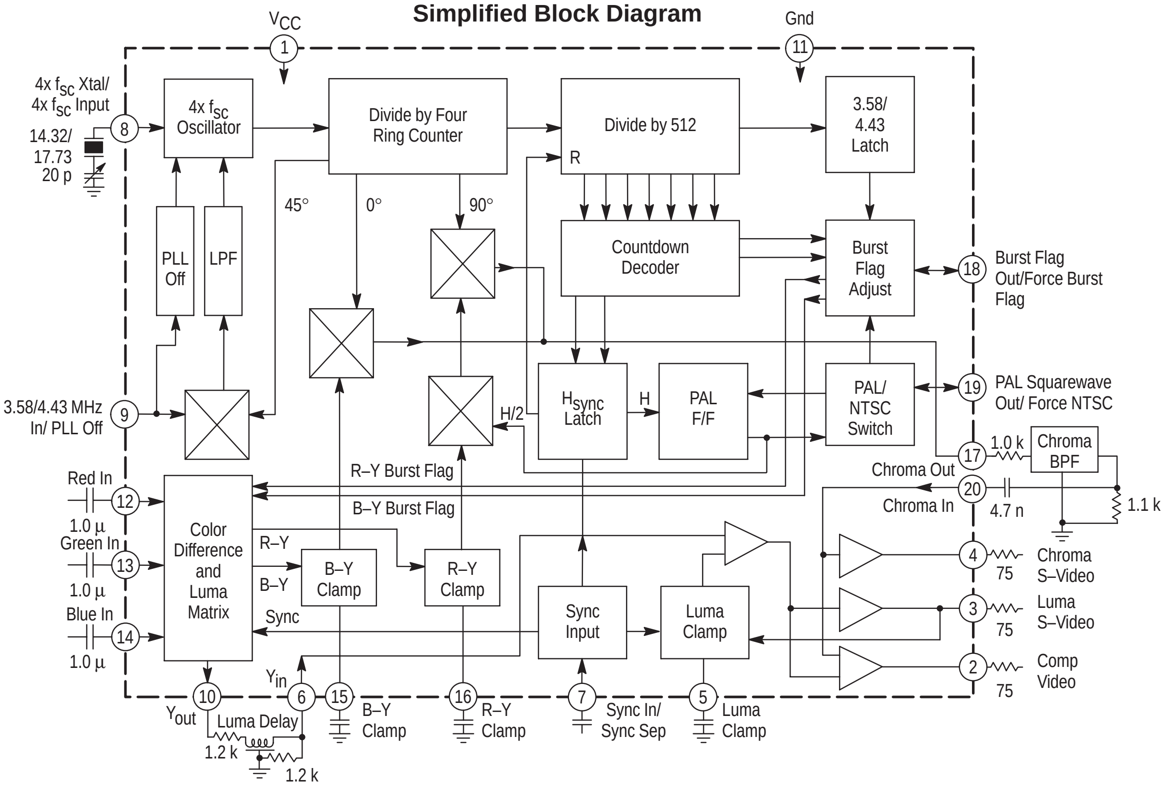
DW SUFFIX
PLASTIC PACKAGE
CASE 751D
(SO–20L)



ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC13077DW	T_A = 0° to +70°C	SO–20L
MC13077P		Plastic DIP

Simplified Block Diagram



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	6.0	V
Storage Temperature	T_{stg}	– 65 to +150	°C
Operating Junction Temperature	T_J	+150	°C
Operating Ambient Temperature	T_A	0 to + 70	°C

RECOMMENDED OPERATING CONDITIONS

Characteristic	Min	Typ	Max	Unit
Supply Voltage	4.5	5.0	5.5	Vdc
Sync Input Threshold Equivalent (See Figure 2)	–	1.4	–	Vdc
Pulse Width	–	4.5 – 5.5	–	µs
R, G, B Input (Amplitude for 100% Saturated Video)	–	0.7	–	Vpp
R–Y Input Amplitude at Pin 16 (for 100% Saturated Video)	–	490	–	mVpp
B–Y Input Amplitude at Pin 15 (for 100% Saturated Video)	–	350	–	
Y Input Amplitude (without sync) at Pins 12, 13, 14 (for 100% Saturated Video)	–	700	–	
Y Input Amplitude (with sync) at Delay Line	–	1.0	–	Vpp
External 4x Subcarrier Input to Pin 8 (If crystal is not used)	–	300	–	mVpp
External Subcarrier Input to Pin 9	–	0.10 to 3.0	–	Vpp
Lock Range (with 4x Subcarrier Crystal specified) at Subcarrier Frequency	–	± 400	–	Hz
Burst Flag Input Threshold (Pin 18)	–	2.5	–	Vdc
NTSC/PAL Select (Pin 19)				Vdc
PAL Switching Amplitude: High	–	4.0	–	
Low	–	1.1	–	
NTSC Select Threshold	–	0.4	–	

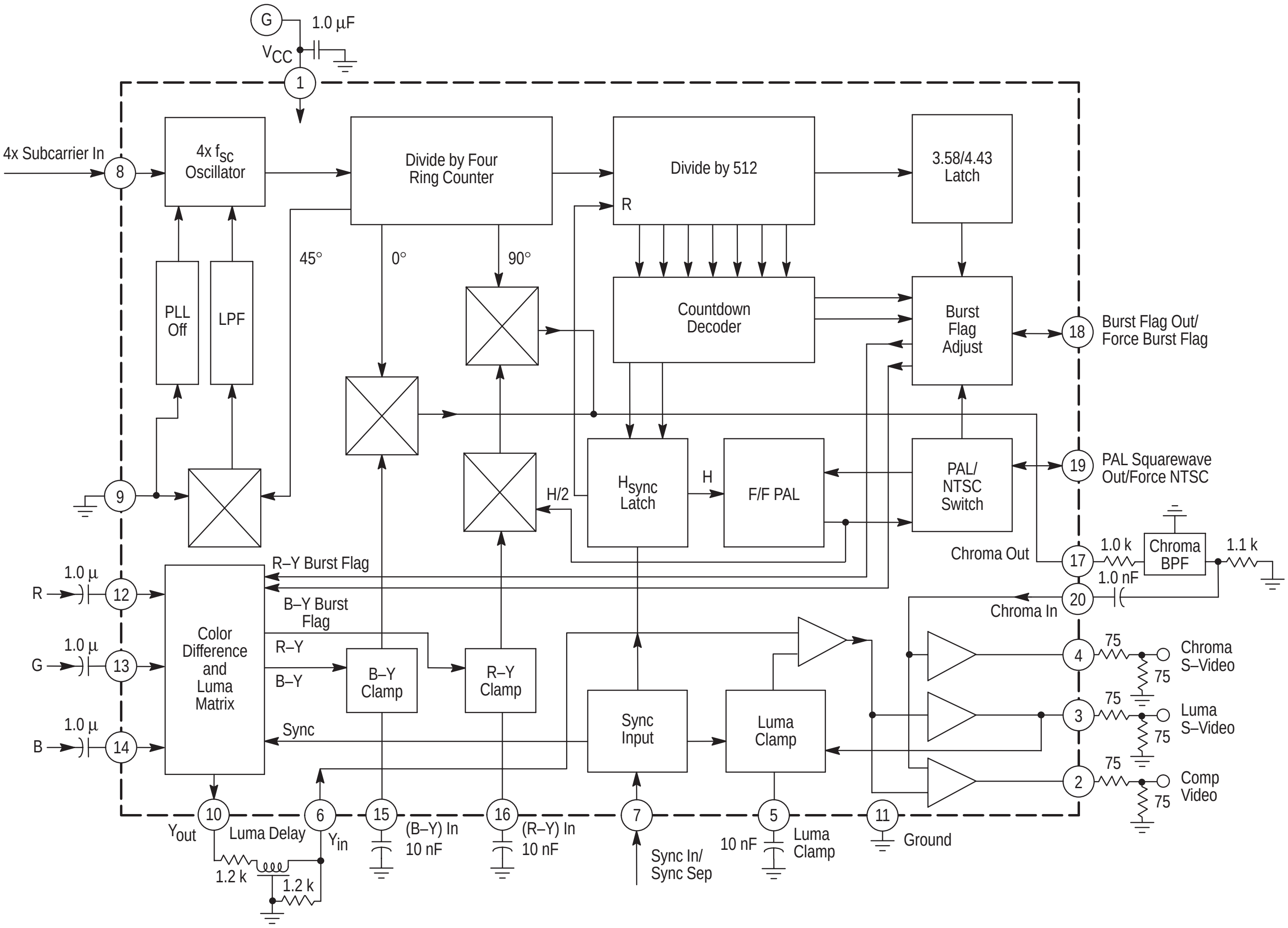
ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0 Vdc, test circuit of Figure 1.)

Characteristic	Pin	Min	Typ	Max	Unit
Supply Current (150 Ω Load on Output Pins)	1	55	70	85	mA
Color Burst Amplitude	2 & 4 (@ 75 Ω load)	250	300	350	mVpp
Line–to–Line Burst Amplitude Deviation		–	7.0	25	mV
Start after leading edge of Sync: NTSC (3.579 MHz)		–	5.0 to 5.3	–	µs
PAL (4.43 MHz)		–	5.4 to 5.6	–	
Duration: NTSC (3.579 MHz)		–	9	–	Cycles
PAL (4.43 MHz)		–	10	–	
PAL Burst Phase: Line n		125	135	145	Degrees
Line n+1		215	225	235	
NTSC Burst Phase		170	180	190	
Subcarrier Leakage in Black	2 & 4 (@ 75 Ω load)	–	–	25	mV
White (100% white)		–	–	65	
Composite Video Output (100% saturated output)	2 (@ 75 Ω load)				
Sync Amplitude		240	281	320	mVpp
Line–to–Line Sync Amplitude Deviation (PAL)		–	7.0	–	mV
Luminance Amplitude Error		–	–	10	%
Line–to–Line Luminance Amplitude Deviation (PAL)		–	3.0	–	mVpp
Chrominance Amplitude Error		–	–	10	%
Line–to–Line Chroma Amplitude Deviation (PAL)		–	< 14	–	mVpp
Chrominance Phase Error		–	–	10	Degrees
Line–to–Line Chrominance Phase Error (PAL)		–	< 5.0	–	
Black Level (RGB at Black during Blanking Intervals)		–	500	–	mV
Sync Tip Clamp Level above Ground		120	200	280	

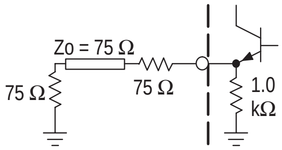
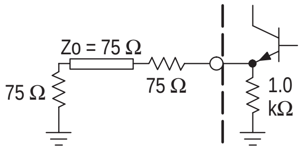
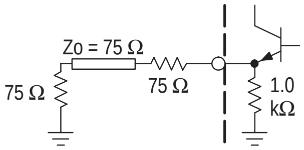
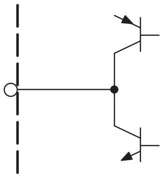
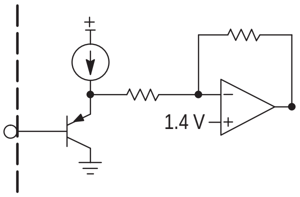
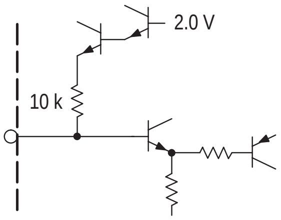
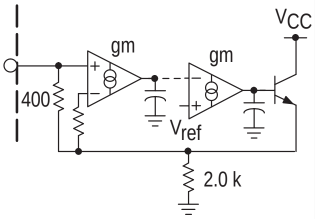
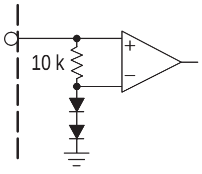
ELECTRICAL CHARACTERISTICS (continued) (T_A = 25°C, V_{CC} = 5.0 Vdc)

Characteristic	Pin	Min	Typ	Max	Unit
Luma S–Video Output					
Sync Amplitude	3 (@ 75 Ω load)	240	281	320	mVpp
Line–to–Line Sync Amplitude Deviation (PAL)		–	7.0	–	mV
Luminance Amplitude Error		–	–	10	%
Line–to–Line Luminance Amplitude Deviation (PAL)		–	3.0	–	mVpp
Black Level		–	500	–	mV
Sync Tip Clamp Level above Ground		120	200	280	
Chroma S–Video Output					
Chrominance Amplitude Error	4 (@ 75 Ω load)	–	–	10	%
Line–to–Line Chrominance Amplitude Deviation (PAL)		–	< 14	–	mVpp
Chrominance Phase Error		–	–	10	Degrees
Black Level		–	500	–	mV

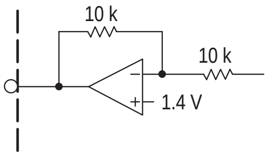
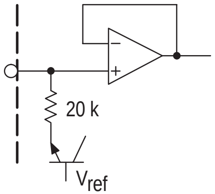
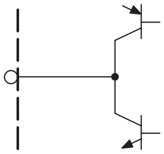
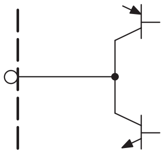
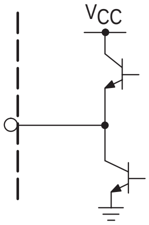
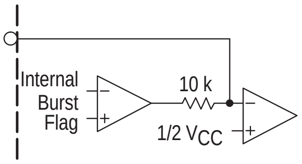
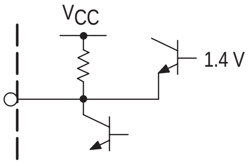
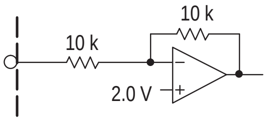
Figure 1. Test Circuit



PIN DESCRIPTIONS

Pin	Symbol	Internal Equivalent Schematic	Description	Expected Waveforms
1	V_{CC}		Supply Voltage	+ 5.0 Vdc ±10%
2	Comp Video		Composite Video output. The external 75 Ω series resistor determines the impedance of the output. The output will drive a 75 Ω load through a 75 Ω coax.	1.0 Vpp (75% Color Saturation), 1.23 Vpp (100% Color Saturation) at the 75 Ω load.
3	Luma S–Video		Luminance S–Video output. The external 75 Ω series resistor determines the impedance of the output. The output will drive a 75 Ω load through a 75 Ω coax.	1.0 Vpp with sync (100% output) at the 75 Ω load.
4	Chroma S–Video		Chrominance S–Video output. The external 75 Ω series resistor determines the impedance of the output. The output will drive a 75 Ω load through a 75 Ω coax.	885 mVpp (100% output) when at the 75 Ω load.
5	Luma Clamp		Luminance Output Clamp storage capacitor. A 0.01 µF capacitor should be connected from this pin to ground.	3.4 Vdc.
6	Y_{In}		Luminance input from the delay line. The delayed Luma from Pin 10 is applied at this pin.	500 mVpp of Composite Luma when 100% saturated RGB inputs are applied.
7	Sync In/ Sync Sep		Composite Sync input. Negative going sync should be applied at this pin. The input has a threshold of 1.4 V.	The peak voltage may not exceed V_{CC}. Minimum voltage should not be less than 0 V. See Figure 2 for input requirements.
8	4x f_{SC} Xtal /4x f_{SC} In		Four times Subcarrier Frequency Crystal Oscillator pin. This pin provides for the connection of the oscillator resonant element. Pin may also be driven directly with a 4x subcarrier signal.	300 to 600 mVpp 4x subcarrier input if the pin is being externally driven. Approximately 40 mVpp, if a crystal is being used.
9	3.58/ 4.43 MHz In/PLL Off		External Subcarrier Input. This pin provides an input to a Phase Detector and PLL and allows phase–lock of the 4x oscillator to an external subcarrier reference. To disable the PLL, this pin should be grounded. 400 Hz of pull–in and lock–in range is possible with a crystal.	0.10 to 3.0 Vpp (AC coupled) of subcarrier to phase–lock 4x oscillator or grounded to disable the PLL.

PIN DESCRIPTIONS (continued)

Pin	Symbol	Internal Equivalent Schematic	Description	Expected Waveforms
10	Y_{Out}		Luminance Delay Line Drive Output. A delay should be inserted between this pin and Pin 6 to match the delay incurred by the Chroma.	1.0 Vpp with sync (100% saturated Color Bar output).
11	Gnd		Ground	Ground
12	Red_{In}		Red Video input.	0.7 Vpp AC coupled (100% Color Bars).
13	$Green_{In}$	See Pin 12	Green Video input.	0.7 Vpp AC coupled (100% Color Bars).
14	$Blue_{In}$	See Pin 12	Blue Video input.	0.7 Vpp AC coupled (100% Color Bars).
15	B–Y Clamp		B–Y Clamp storage capacitor. A 0.01 µF capacitor should be connected from this pin to ground, unless the pin is used as an input.	If not used as an input the pin is clamped during sync to 2.4 Vdc. Can be used as a B–Y input (AC coupled, 350 mVpp, 100% color saturation). Burst Flag, if disabled at Pin 18, must be inserted here with the following signal levels; –170 mV (NTSC), –121 mV (PAL).
16	R–Y Clamp		R–Y Clamp storage capacitor. A 0.01 µF capacitor should be connected from this pin to ground, unless the pin is used as an input.	If not used as an input the pin is clamped during sync to 2.4 Vdc. Can be used as a R–Y input (AC coupled, 490 mVpp, 100% color saturation). Burst Flag, if disabled at Pin 18, must be inserted here with the following signal level; +121 mV for PAL.
17	Chroma Out		Chroma Bandpass Drive Output.	2.8 Vpp (100% Color Bars)
18	Burst Flag Out/Force Burst Flag		Burst Flag Output Disable and Force pin. If left unconnected, internally generated color burst will appear at Pins 2 and 4. Burst Flag will appear at this pin (18). If grounded, the Burst Flag will be disabled. If externally driven from another source of burst flag, the internal flags will be overriden.	1.8 Vpp burst flag pulses if unconnected.
19	PAL Square–wave Out/Force NTSC		PAL/NTSC system switch. If grounded, the MC13077 will encode NTSC, and if left open, PAL.	In PAL mode, a PAL squarewave appears at this pin, the phase of which can be reset by momentarily forcing the pin to ground during the high state of the squarewave.
20	Chroma In		Chroma Bandpass input. Output from chroma bandpass filter should be applied at this pin.	1.4 Vpp (100% Color Bars) with bandpass filter and 1.0 kΩ matching resistors.

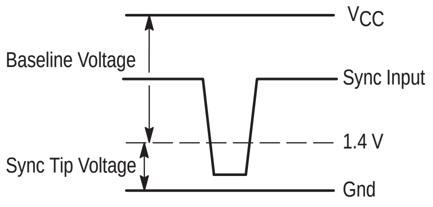
FUNCTIONAL DESCRIPTION

Composite Sync Input

Other than the component video inputs to be encoded, only Composite Sync is required for encoding the components into a composite signal compatible with either the NTSC or PAL standard. The Composite Sync input is used internally for determining which standard to encode to, for driving the black level clamps, and to set the timing of the composite sync in the outputs.

The Composite Sync/Sync Separator input was designed to accept AC or DC coupled inputs making it possible to drive the sync input from a variety of sources. An interesting note is that composite video can also be used for sync input. The threshold of the sync input is 1.4 Vdc. Figure 2 shows the requirements for sync input.

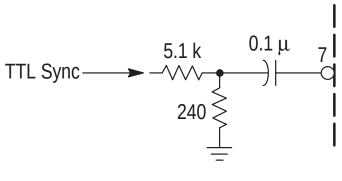
Figure 2. Sync Input Amplitude Requirements



Both serrated and block vertical sync can be used for NTSC applications. PAL applications require a serrated vertical sync. The serrations at the horizontal rate trigger the PAL flip–flop to generate the swinging burst.

Even though the sync input of the MC13077 is well suited for TTL interface, some functions of the IC are susceptible to the high energy present in such signals and may be disturbed. This disturbance may take the form of a noise spike in the video outputs and/or a disturbance of the 4x oscillator resulting in an incorrect encoding of the chroma information. Therefore, it is recommended that if TTL or other fast–edged inputs are going to be used for the sync input, then either the amplitude and/or the edge speed of the sync input pulse should be reduced. 300 mVpp of sync without a reduction of edge speed has to be shown to produce disturbance free operation. Also, a sync input of 4.0 Vpp and edge rates of 225 ns have been shown to produce similar results. Figure 3 shows a recommended coupling circuit for TTL type composite sync.

Figure 3. TTL Sync Input Circuit



Luma and Color Difference Clamps

Clamping for the MC13077 occurs once every horizontal line during sync. The absence of color creates a color difference component voltage of zero, this null is used to generate a reference voltage for black in the video outputs. The clamp capacitors at Pins 5, 15 and 16 are used to store the reference voltage during the line period.

RGB Inputs

To encode RGB, the component video inputs (Pins 12, 13, 14) are applied to the Luma (Y) and color difference (R–Y, B–Y) matrix. The color difference signals are then conditioned by Sallen–key low pass filters (f–3dB = 4.0 MHz). The inputs are designed so that 700 mVpp RGB provides 100% color saturation.

The first color difference component (R–Y) is created by matrixing the RGB components with the following weights:

$$R–Y = 0.70R – 0.59G – 0.11B \quad (1)$$

The second color difference signal (B–Y) is created in a similar fashion by the equation:

$$B–Y = 0.89B – 0.59G – 0.30R \quad (2)$$

These two components then receive burst flag before being modulated by the color subcarrier to create composite chroma.

The luma is also the result of a weighted matrixing of the RGB components. The components and corresponding weights are:

$$Y = 0.30R + 0.59G + 0.11B \quad (3)$$

Composite sync is then added to the result of Equation 3 to create composite luma.

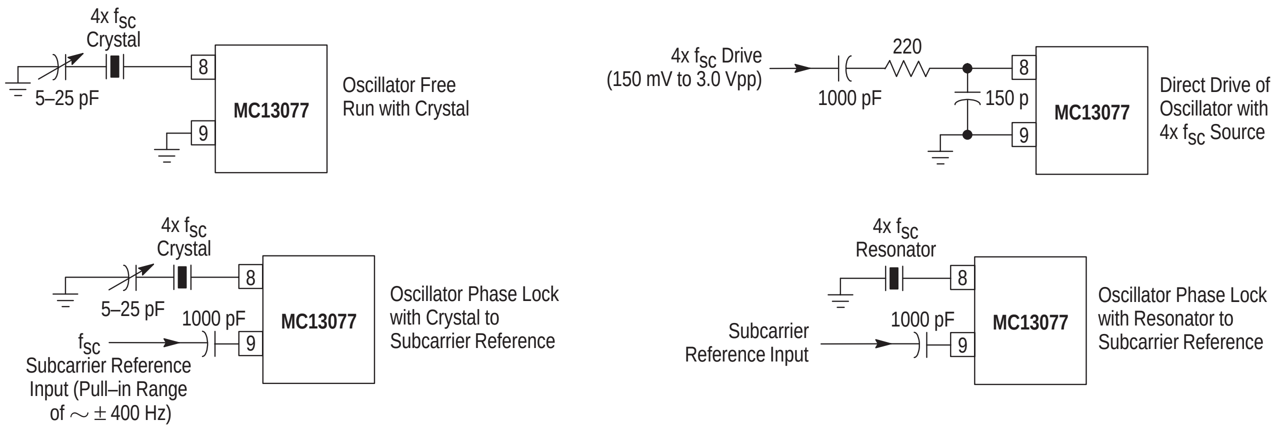
The luma information thus created must be eventually recombined with the chroma information. However, since the chroma information created by Equations 1 and 2 is filtered internally before being modulated then bandlimited externally, the resultant encoded chroma experiences a group delay that is the sum of the delay imposed by the internal and external filtering. So, the composite luma is output at Pin 10 so that an external delay can be inserted in the path to match the delay incurred by the composite chroma. The delayed composite luma is then input back into the MC13077 at Pin 6.

Color Difference Inputs

If the MC13077 is intended to encode color difference signals (YUV or Y, R–Y, B–Y), it becomes necessary to bypass the color difference and luma matrix circuitry. This can be accomplished by inputing directly to the color modulators the color difference signals. 491 mVpp and 349 mVpp should be input to the R–Y and B–Y Clamp pins (Pin 16 and Pin 15) respectively, to achieve 100% color saturation in the composite video output. The luma information can be input in two ways. The luma can be input directly into the RGB inputs (700 mVpp without sync), or through the delay line (1.0 Vpp with sync, sync tip–to–peak white) in which case the RGB inputs should be cap–coupled to ground. In either case, composite sync still needs to be input to the MC13077 at Pin 7 (see Figures 11, 12 and 13).

If the R–Y and B–Y inputs also have burst flag, it can also be input along with the color difference signals at these pins. Of course, now since the color difference modulator pre–filtering is circumvented, the delay for the luma information should be matched only to the delay of the bandpass filter.

Figure 4. Versatility of the 4x f_{SC} Oscillator



4X Subcarrier Oscillator

To encode the color difference components, an accurate and reliable subcarrier source is required. The MC13077 has an on–chip single pin oscillator that will free–run with a 4x f_{SC} crystal, phase–lock to an external subcarrier reference with a 4x f_{SC} crystal or resonator, or be driven externally from a 4x f_{SC} source. If the 4x f_{SC} oscillator is going to be free run, the subcarrier input (Pin 9) should be grounded. If the 4x f_{SC} oscillator is going to be phase–locked to an external subcarrier source, the external reference should be capacitor–coupled to Pin 9. If the 4x f_{SC} oscillator is going to be driven externally, Pin 8 should be driven from a network that increases the impedance of the source at frequencies capable of producing off–frequency oscillations. The 4x f_{SC} subcarrier source, thus being defined, makes it possible to produce accurate quadrature subcarriers for the modulators. The 4x source is internally divided by a ring counter to produce the quadrature subcarrier signals. These signals in turn are provided to the color difference modulators to produce the modulated chroma. The oscillator was designed so that if a crystal is chosen as the resonant element of the 4x oscillator, the crystal specifications would be common. Crystal specifications for an adequate crystal are shown in 1

Table 1. Crystal Specifications

Frequency: 14.31818 MHz (NTSC) 17.734475 MHz (PAL)
Mode: Fundamental
Frequency Tolerance (@25°C), 40 ppm
Frequency Tolerance df/dfo (0° – 70°C), 40 ppm
Load Capacitance: 20 pF
ESR: 50 Ω
C1(Internal Series Capacitance), 15 mpF

This crystal is a common variety and is specified as a parallel resonant.

Burst Flag Decoding

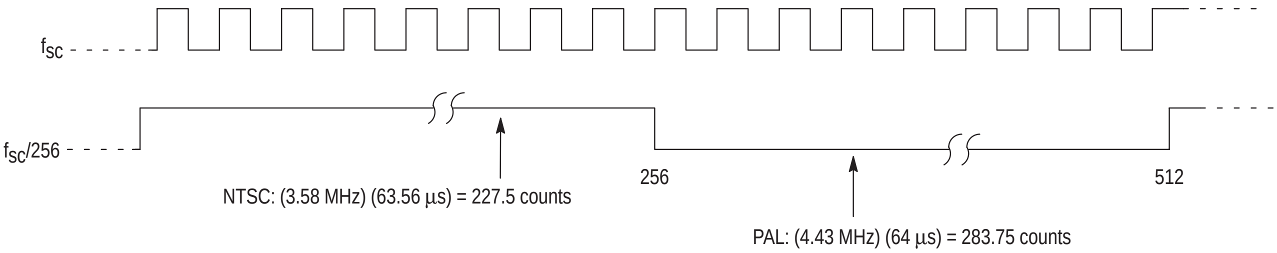
In order to encode to either NTSC or PAL compatibility, the MC13077 must first determine which is the intended standard. The MC13077 accomplishes this with an internal decode using the sync input and the output of the divide by 4 ring counter. Internally, the Sync separator circuitry provides an output that is sampled by the subcarrier signal from the ring counter. The result is an internal sync representative of externally input sync but synchronized to the internal subcarrier signal. This signal provides a reset for an internal 9–bit counter that provides divisions of the subcarrier signal from the ring counter at powers of 2 (i.e. 2^1, 2^2, 2^3,...2^9 = 512). The eighth bit of the counter gives the output, $f_{SC} \div 256$. The decision to provide burst gate timing for PAL or NTSC is based upon the state of this output after one period of the horizontal sync. Figure 5 shows the relationship between the clock and the eighth bit of the counter.

Triggering of the burst PAL flip–flop due to equalizing pulses is also inhibited by the decode circuitry. This is done by counting out beyond a half line interval before generating burst flag.

If the MC13077 is encoding 525/60 component video to NTSC and the MC13077 is generating the burst flag, the start of burst will occur 18 counts after the leading edge of sync has been sampled, and will continue until nine cycles of burst have occurred. Since the reset pulse of the 9–bit counter has a resolution of $1.0/f_{SC}$, this implies that the start of burst will occur 5.17 ± 0.1397 µs after the leading edge of sync and also that the start (and end) of burst may differ by as much as 279.4 ns from line–to–line. If the MC13077 is encoding 625/50 to PAL, the subcarrier frequency will be 4.43361875 MHz and that implies a resolution of 225.5 ns for the burst position. For PAL encoding, 24 counts of the subcarrier are necessary before burst is initiated. So ten cycles of subcarrier will occur 5.53 ± 0.1128 µs after the leading edge of sync. After the timing of the burst gate is selected, the burst gate envelope is added to the color difference components.

Another alternative to the internal determination of burst flag is the external input of burst flag. This allows the user to externally define the exact timing and duration of color burst. If external burst flag is available, it can be inserted at Pin 18. The threshold level is nominally $V_{CC}/2$ and the input should not exceed V_{CC}. Burst will begin when the leading edge of the burst flag input exceeds $V_{CC}/2$ and will stop when it falls below $V_{CC}/2$. If it is desired to disable the burst flag, Pin 18 can be pulled low. It is also possible to insert burst flag with the R–Y and B–Y components. This is done at the clamp pins with the respective color difference inputs with the internal burst flag generation disabled (Pin 18 grounded).

Figure 5. Relationship Showing the Counts of a 3.58 MHz Clock versus a 4.43 MHz Clock at the End of a Horizontal Period



Chroma Band Limiting and Luma Delay

Once the color difference and burst flag envelopes have been modulated, the two components are internally summed and applied to an output buffer that will drive the external bandpass circuitry before entering the chip again at Pin 20. The sum of the color difference modulators produces an output that is high in harmonic content. For this reason, and to reduce the possibility of cross color, a chroma bandpass transformer is used to band–limit the chroma. Suggested bandpass filters and specifications for NTSC and PAL are shown in Figure 7a and 7b. For each of these filters, approximately 300 ns of group delay is experienced by the filtered chroma. There is also an internal delay on the order of 100 ns due to internal filtering that must be considered. Thus a 400 ns luma delay line is used to equalize the timing of the luma and the chroma. Suitable 400 ns delay lines are the TOKO H321LNP–1436PBAB and the TDK DL122401D–1533. The delay of the luma channel is inserted between Pins 10 and 6. Pin 10 is the buffered output of the luma from the RGB matrix. This output is capable of driving the external passive delay line with no external gain or buffering required.

Figure 7a. Group Delay and Magnitude Response of the TOKO Bandpass Filter Intended for NTSC Applications

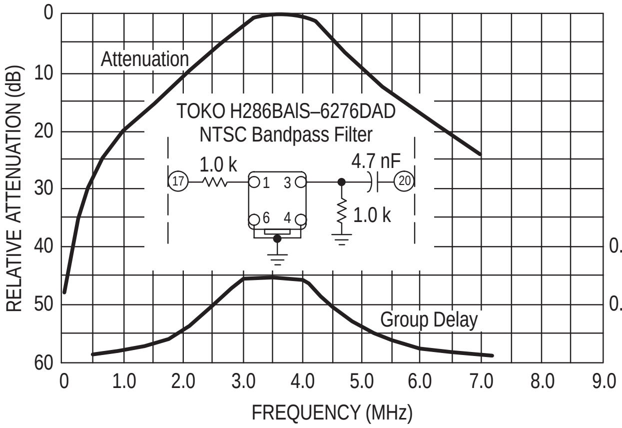
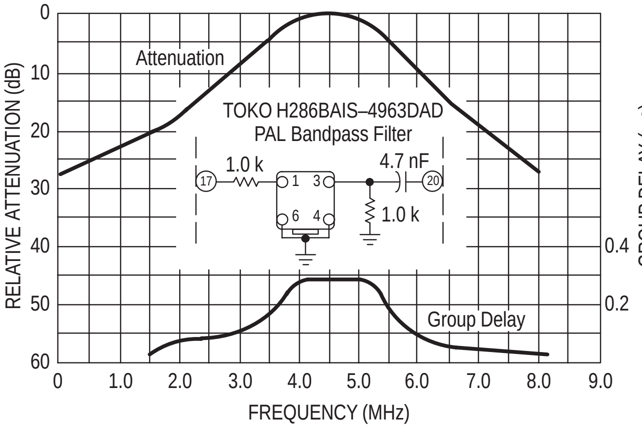


Figure 7b. Group Delay and Magnitude Response of the TOKO Bandpass Filter Intended for PAL Applications



Characteristics of TOKO Bandpass Filter (H286BAIS – 6276DAD)

Frequency (MHz)	**Attenuation** (dB)	**Group Delay** (µs)
2.0	8.0 (min)	0.12
2.8	3.0 ± 3.0	0.25
3.58	Ins. Loss 3.5 (max)	0.290 ± 0.030
4.3	3.0 ± 3.0	0.24
6.2	15 (min)	0.05

Characteristics of TOKO Bandpass Filter (H286BAIS – 4963DAD)

Frequency (MHz)	**Attenuation** (dB)	**Group Delay** (µs)
2.50	10 (min)	0.075
3.73	3.0 ± 3.0	0.24
4.43	Ins Loss 2.0 (max)	0.295 ± 0.035
5.13	3.0 ± 3.0	0.24
6.50	12 (min)	0.05

Chroma Encoding

Modulation of the color difference components is performed by two double–balanced mixers that are driven from quadrature signals provided by an internal ring counter. The quadrature signals are derived from a ring counter that is driven by the 4x oscillator, and which makes highly accurate quadrature angles possible.

If PAL encoding is selected, negative burst flag envelope is provided to both B–Y and R–Y components equally, then the R–Y envelope phase is switched positive and negative from line–to–line to provide the PAL alternating burst phase characteristic. An internal flip–flop that provides the internal $f_H/2$ switching is enabled by opening the connection at Pin 19. If enabled, the pin will exhibit the internally generated half line frequency squarewave. If it is desired to reverse the sense of the PAL swinging burst, it can be done at this pin by pulling Pin 19 low when the squarewave is high. The component envelopes with the proper PAL burst phase are then modulated to produce the composite chroma.

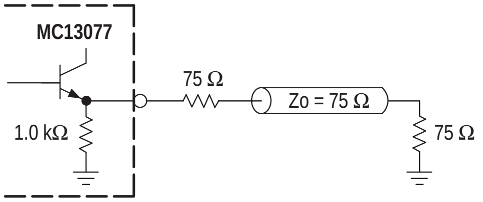
If the MC13077 is encoding to NTSC, only the B–Y color difference component is provided a negative burst flag. This envelope when modulated results in the characteristic –180° phase difference between the color burst and the subcarrier for the B–Y component. Pin 19 should be grounded for NTSC operation to disable the PAL flip–flop.

Video Outputs

After being filtered, the composite chroma is recombined with the composite luma information for the Composite Video output. The composite chroma and composite luma components are also kept separate and buffered for the chroma S–Video and luma S–Video outputs. The video outputs are provided with low impedance emitter–follower stages and, therefore, require an external 75 Ω impedance determining series resistor (see Figure 7). The outputs are designed to drive a 75 Ω load through the external 75 Ω series resistor.

The Composite Video output will provide 1.23 Vpp of video (sync tip–to–peak chroma) for 100% saturated video at the 75 Ω load. Luma S–Video will be 1.0 Vpp (sync tip–to–peak white) at the 75 Ω load and the Chroma S–Video output will provide 885 mVpp at the 75 Ω load.

Figure 7. Composite S–Luma and S–Chroma Video Outputs



APPLICATIONS INFORMATION

Figures 8 through 13 are application examples showing the versatility of the MC13077.

Figure 8. Standard Encoder Application with RGB Inputs and Phase–Locked Subcarrier

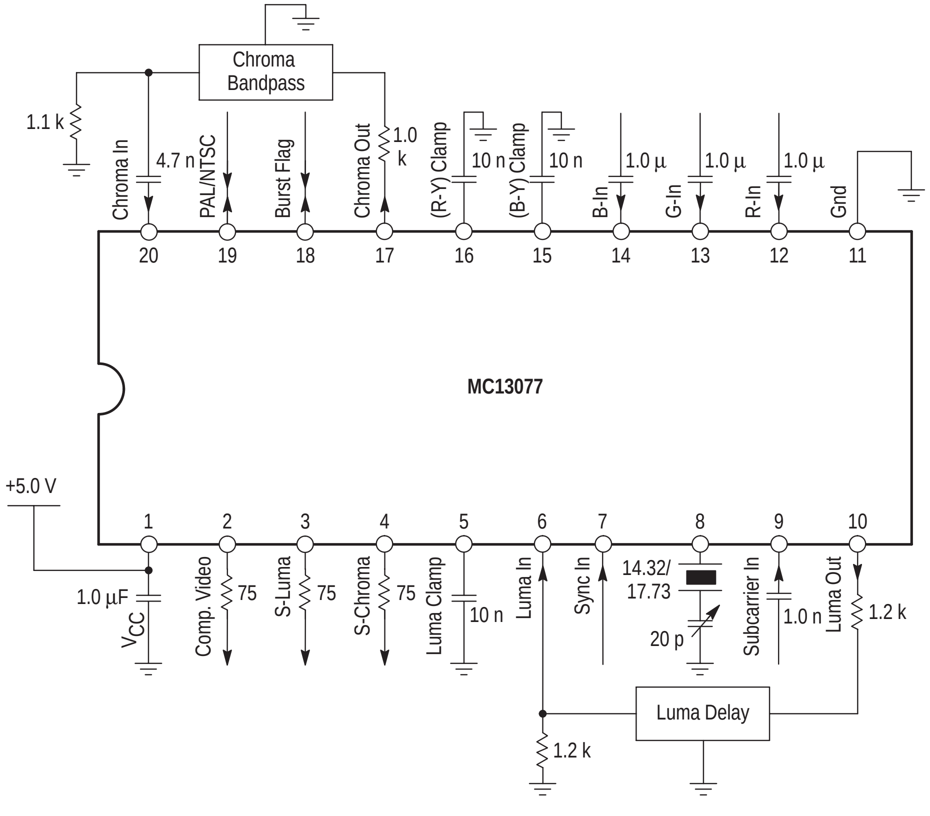


Figure 9. Encoder with RGB Inputs and Unlocked Subcarrier

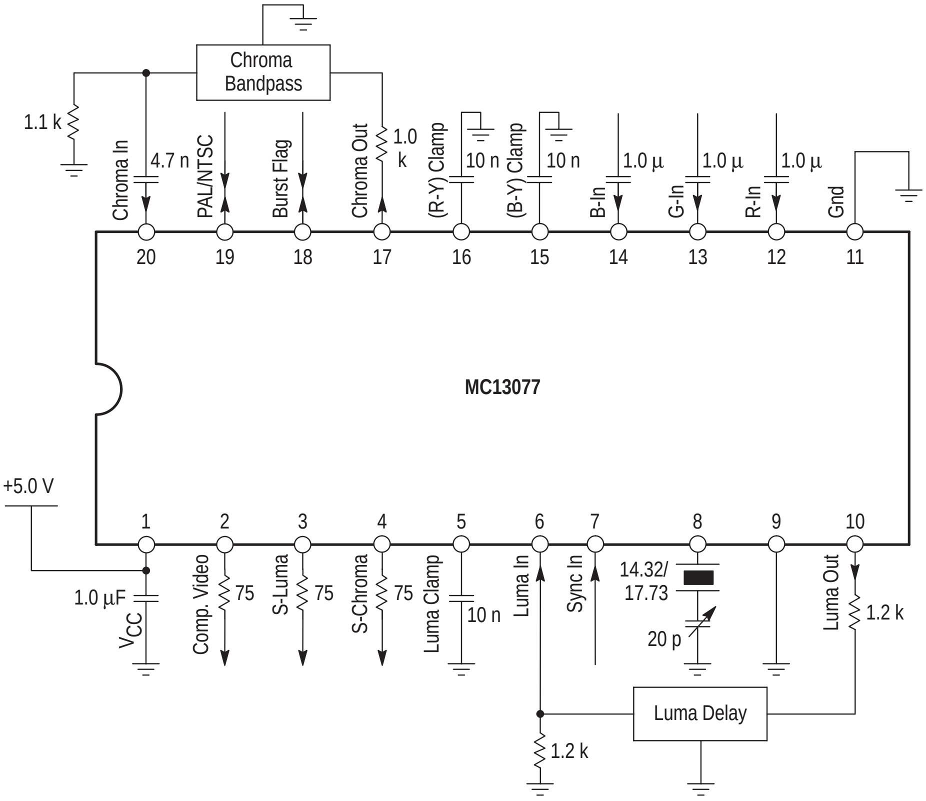


Figure 10. Encoder with RGB Inputs and 4x Subcarrier Drive

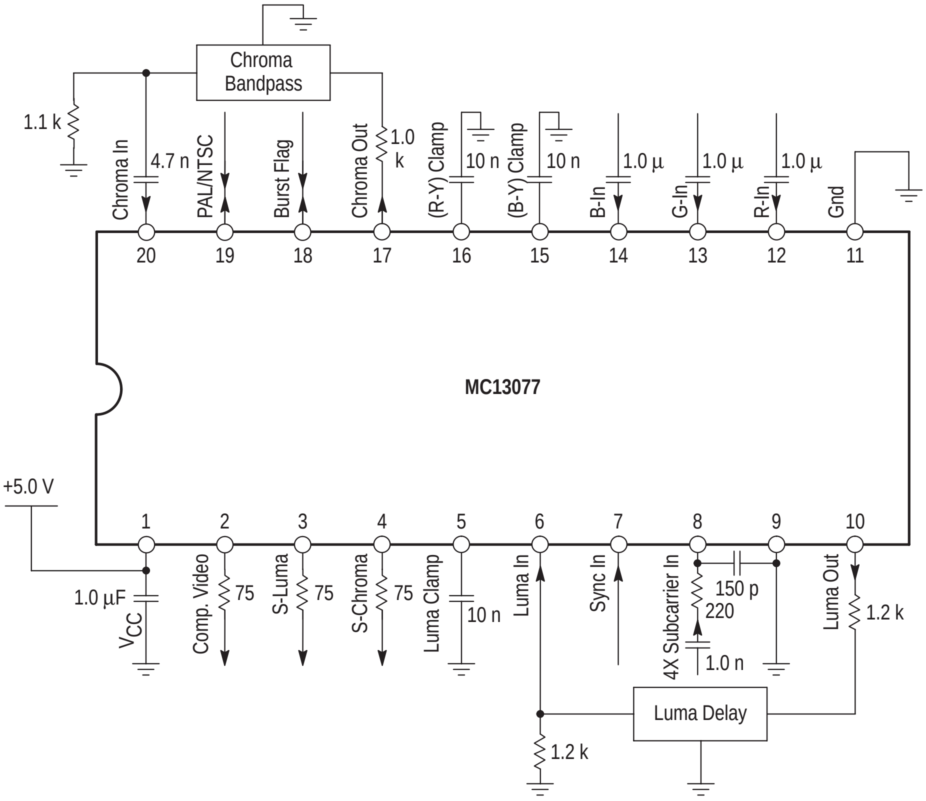


Figure 11. Encoder with Luma and Color Difference Inputs Using Phase–Locked Subcarrier

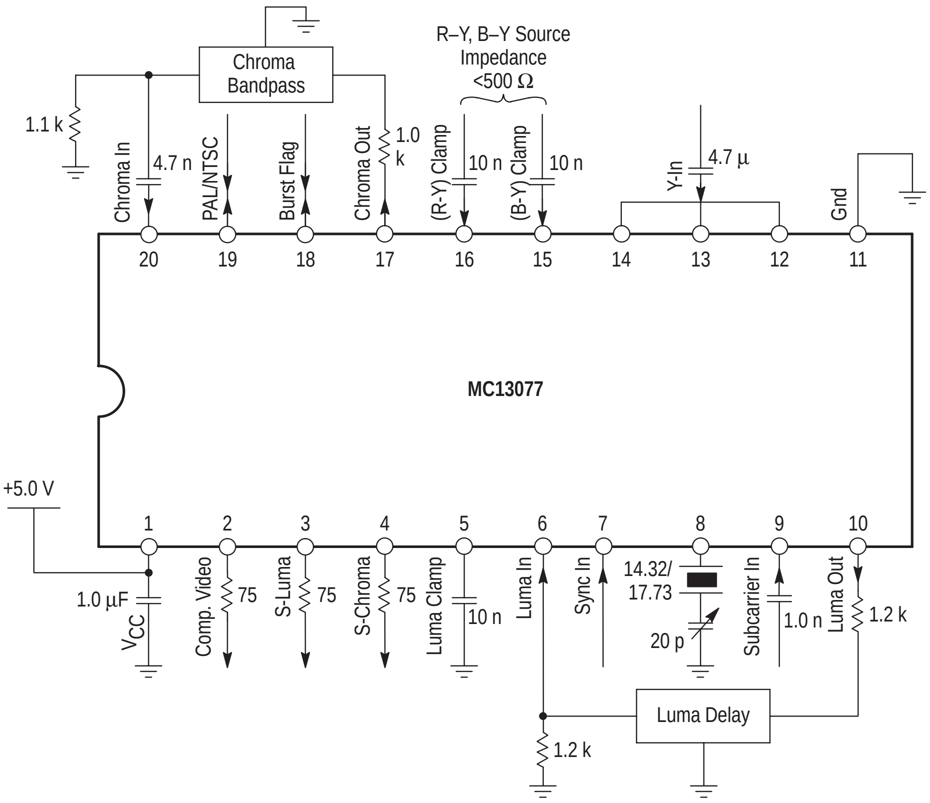


Figure 12. Encoder with Composite Luma and Color Difference Inputs Using Phase–Locked Subcarrier

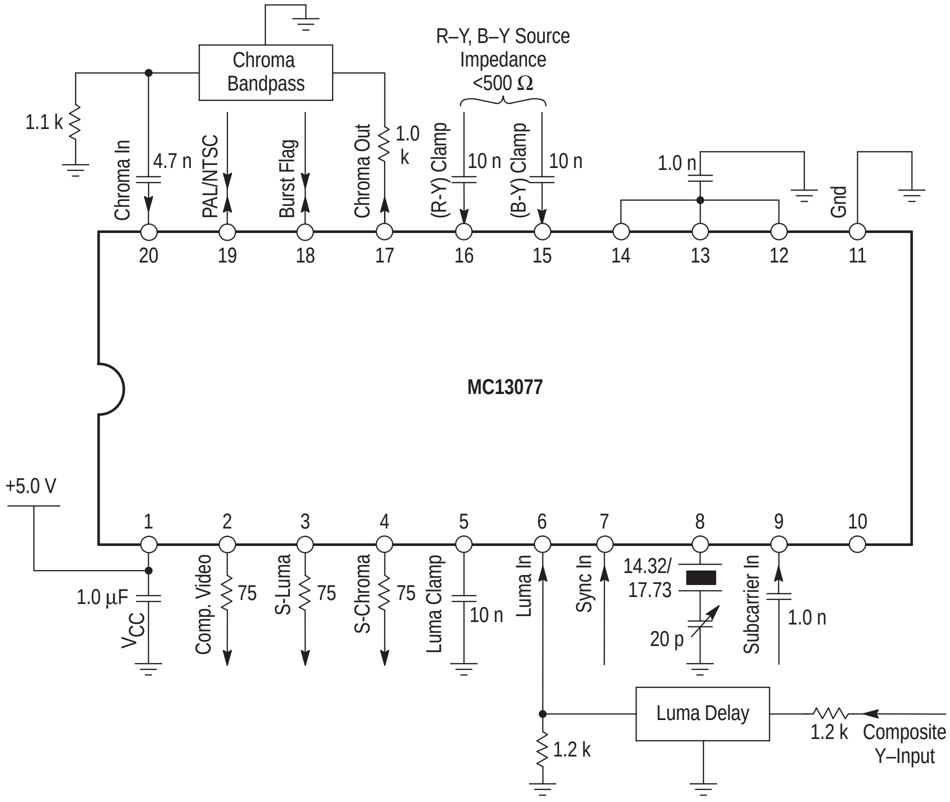
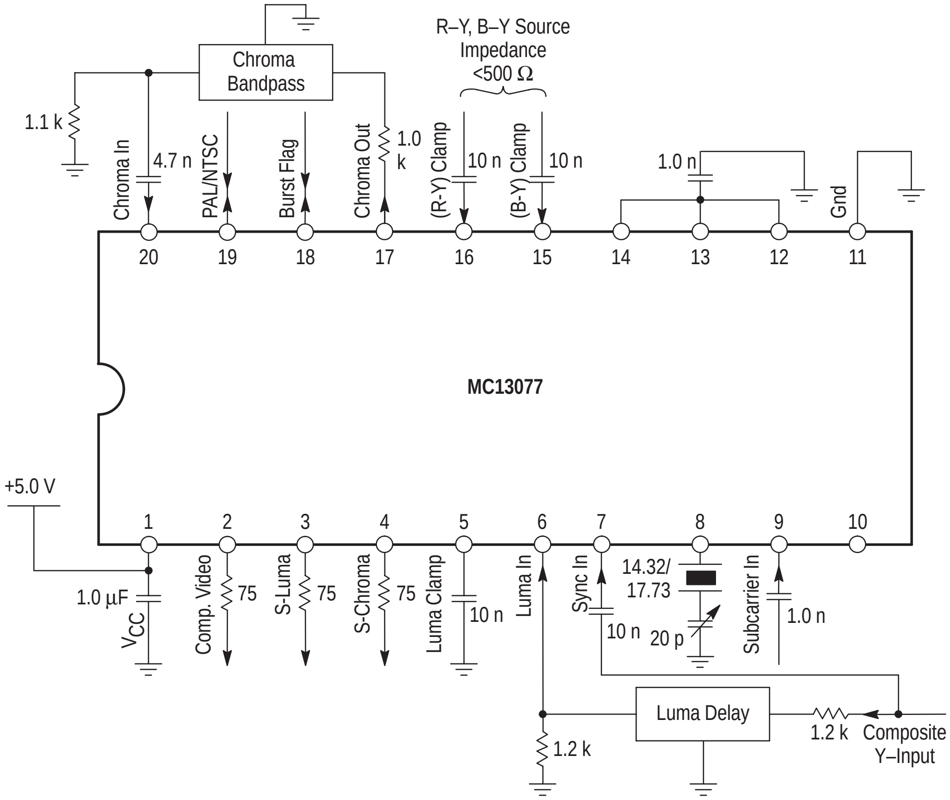


Figure 13. Encoder with Composite Luma and Color Difference Inputs Using the Sync Separator and Having Phase–Locked Subcarrier



Recommended Vendors

Bandpass Filters and Delay Lines

TOKO America Inc.
1250 Feehanville Drive
Mt. Prospect, IL 60056

(708) 297–0070
(708) 699–7864 (fax)

Delay Lines

TDK Corp. of America
1600 Feehanville Drive
Mt. Prospect, IL 60056

(708) 803–6100

Crystals

Fox Electronics
5570 Enterprise Pkwy
Ft. Myers, FL 33905

(813) 693–0099

Standard Crystal Corporation
9940 E. Baldwin Place
El Monte, CA 91731

(818) 443–2121

MOTOROLA

MC13081X

Advance Information

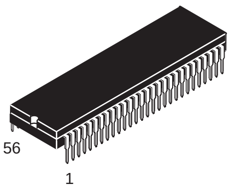
Multimode Color Monitor Horizontal, Vertical, and Video Combination Processor

MULTIMODE COLOR MONITOR PROCESSOR

SEMICONDUCTOR TECHNICAL DATA

The MC13081X includes all the signal processing functions for a scan frequency agile and multiple sync system analog RGB monitor and includes the following functions:

- Automatic Horizontal Frequency Tracking of All Commonly Used Personal Computers, Continuously Adaptable from 30 kHz to 64 kHz
- Sync–on–Green Detection
- Vertical Timebase Operates from 45 to 100 Hz
- Vertical and Horizontal Sync Polarity Detection with Outputs for Mode Switching
- Video Pre–Amplifiers Typical Rise/Fall Time of 5.0 ns at 3.0 Vpp Output Voltage Swing
- Overall Contrast Control and Independent RGB Gain Controls

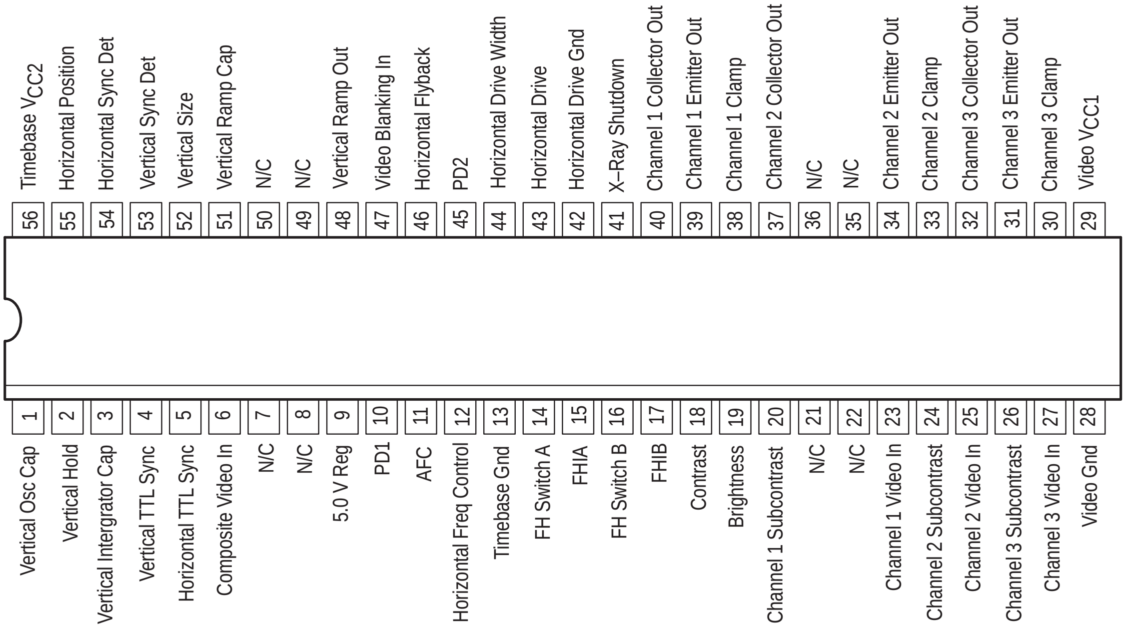


B SUFFIX
PLASTIC SDIP PACKAGE
CASE 859

ORDERING INFORMATION

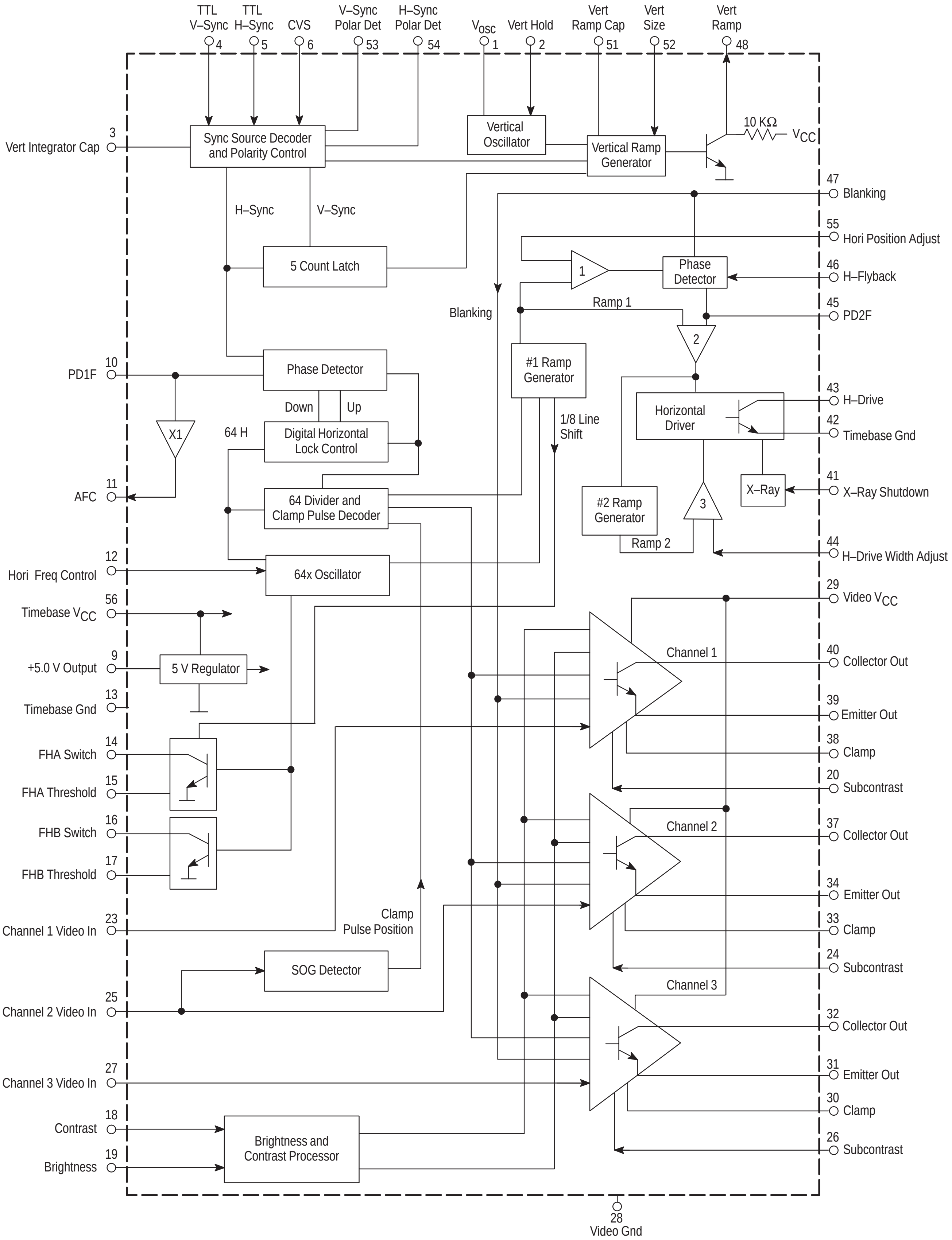
Device	Operating Temperature Range	Package
MC13081XB	T_A = 0° to +70°C	Plastic SDIP

PIN CONNECTIONS



(Top View)

Figure 1. Block Diagram



This device contains 1074 active transistors.

MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted.)

Rating	Pin	Value	Unit
Power Supply Voltage Video Section V_{CC1} Timebase Section V_{CC2}	 29 56	 –0.5, +10 –0.5, +10	Vdc
Brightness, Contrast, Horizontal Flyback Input, Frequency Switch when Off	19, 18, 46, 14, 16	0 to V_{CC}	Vdc
X–Ray Shutdown	41	–0.5, +0.9	Vdc
Subcontrast RGB Controls	20, 24, 26	0 to +2.0	Vdc
Horizontal Drive Width, Horizontal Position	44, 55	0 to +5.0	Vdc
Voltage on Horizontal Drive when Off, Vertical TTL Sync Input, Horizontal TTL Sync Input, Composite Video Sync Input, Video Amplifier Output Collectors	43, 4, 5, 6, 32, 37, 40	–0.5 to V_{CC} + 0.5	Vdc
Current into Horizontal Drive when On	43	100	mA
Current into Frequency Switch when On	14, 16	30	mA
Video Amplifier Inputs	23, 25, 27	–0.5, + 5.0	Vdc
Video Amplifier Output Current (Total for the Three Channels)	40, 39, 37, 34, 32, 31	120	mA
Storage Temperature	–	–65 to +150	°C
Junction Temperature	–	+150	°C

NOTE: ESD data available upon request.

RECOMMENDED OPERATING CONDITIONS

Characteristic	Pin	Min	Typ	Max	Unit
Power Supply Voltage Video Section V_{CC1} Timebase Section V_{CC2}	 29 56	 7.6 7.6	 8.0 8.0	 8.4 8.4	Vdc
Power Supply Voltage Difference, $V_{CC2} – V_{CC1}$	–	–0.3	0	0.8	Vdc
Internal 5.0 V Regulator Output Current	9	–20	–	0	mA
Contrast Control	18	0	–	5.0	Vdc
Brightness Control	19	0	–	5.0	Vdc
Subcontrast Control	20, 24, 26	0	–	2.0	Vdc
Horizontal Drive Width Adjust	44	0	–	5.0	Vdc
Horizontal Position Adjust	55	1.0	–	4.0	Vdc
Horizontal Flyback Signal Amplitude	46	0.7	5.0	8.0	V
Horizontal Flyback Signal DC Input Voltage Level	46	–0.2	0	–	Vdc
Voltage on Horizontal Drive Collector when “Off”	43	0	–	V_{CC}	V
Current into Horizontal Drive Collector when “On”	43	0	–	40	mA
Voltage on Horizontal Drive Emitter W.R.T. Circuit Ground	42	–0.3	0	2.0	Vdc
Blanking Input Signal Amplitude	47	1.5	–	4.0	V
Voltage on FH Switches when “Off”	14, 16	0	–	8.0	Vdc
Current into each FH Switch when “On”	14, 16	0	–	20	mA
X–Ray Shutdown	41	0	–	0.7	Vdc
Composite Video Sync Input	6	1.0	–	2.0	Vpp
Vertical Sync Frequency	–	45	–	100	Hz
Horizontal Sync Frequency	–	30	–	64	kHz
Vertical Sync Pulse Width	–	–	70	–	µs
Horizontal Sync Pulse Width	–	–	1.0	–	µs

RECOMMENDED OPERATING CONDITIONS (continued)

Characteristic	Pin	Min	Typ	Max	Unit
Video Signal Amplitude (with 75 Ω Termination)	23, 25, 27	0.5	0.7	1.2	Vpp
Voltage on Video Amplifier Collector	32, 37, 40	4.5	–	V_{CC}	Vdc
Current Through Video Collector–Emitter	40, 39, 37 34, 32, 31	0	–	40	mA
Vertical Hold Set Resistance, R9 + VR2 (Figure 2)	2	–	10	–	kΩ
Vertical Size Set Resistance, R10 + VR3 (Figure 2)	52	–	220	–	kΩ
Vertical Linearity Set Resistance, R12 + VR4 (Figure 2)	51	–	1000	–	kΩ
Operating Ambient Temperature	–	0	25	70	°C
FH Switches Set Resistance	15, 17	See Application Section 5			–
Vertical TTL Sync Input	4	TTL Voltage Level			Vdc
Horizontal TTL Sync Input	5	TTL Voltage Level			Vdc

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC} = 8.0 Vdc)

Characteristic	Condition	Pin	Min	Typ	Max	Unit
POWER SUPPLIES						
Supply Current Total Consumption	–	29, 56	70	85	110	mA
5.0 V Regulator		9				
Output Voltage	Load Current (I_B) = 0 mA		4.75	5.0	5.25	Vdc
Line Regulation	7.6 V < V_{CC} < 8.4 V, I_B = 0 mA		–	25	–	mV
Load Regulation	–10 mA < I_B < 0 mA		–	100	–	mV
Temperature Coefficient			–	–0.3	–	mV/°C
Thermal Resistance, Junction–to–Ambient	–	–	–	59	–	°C/W
HORIZONTAL PROCESSING						
Horizontal Oscillator Frequency Range	–	43	30	–	64	kHz
Horizontal Oscillator Free Running Frequency @ I12 = 240 µA	Sink 240 µA from Pin 12 with Resistor R5 Opened	43	29	31	33	kHz
Horizontal Sync Detector Output/+V_E Sync	–	54	–	0	–	Vdc
Horizontal Sync Detector Output/–V_E Sync	–	54	–	3.6	–	Vdc
Horizontal Sync Input	–	5				
Input Impedance			–	22	0	kΩ
Input Level – Low			0	–	0.8	Vdc
Input Level – High			2.4	–	5.0	Vdc
Composite Video Sync Input	–	6				
Input Impedance			–	1.0	–	kΩ
Internal Bias Level			–	1.55	–	Vdc
Minimum Input Amplitude			0.1	–	–	Vpp
Short Term Horizontal Pull–In Range	Time < 5.0 ms	–	–	±5.0	–	%FH
Long Term Horizontal Pull–In Range	Time > 500 ms	–	30	–	64	kHz
Horizontal Frequency Control (Current Transfer Constant)	Current Flowing Out of Pin 12	12	115	122	129	Hz/µA
Horizontal Free Running Frequency Change versus Temperature	Pin 11 is Opened	–	–	300	–	ppm/°C
FH Switch Threshold Pins	–	15, 17				
Output Current			–	I12/2	–	µA
Threshold			–	5.0	–	V
Hysteresis			0	–	200	mV
FH Switch Voltage when “On”	I = 10 mA	14, 16	–	–	200	mVdc

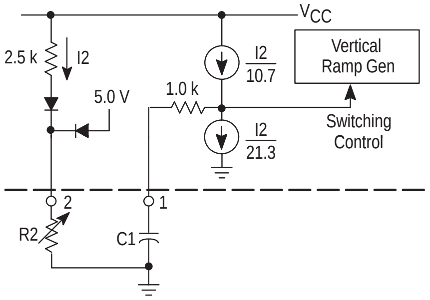
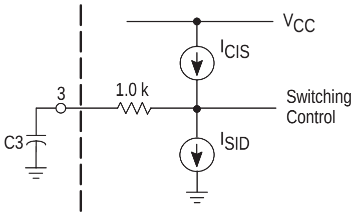
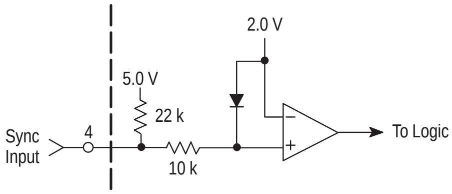
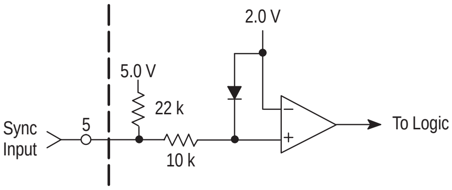
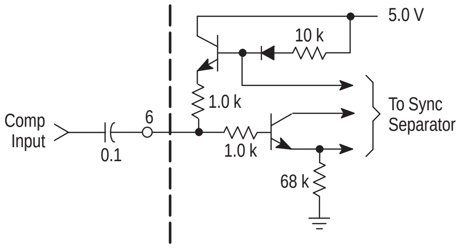
ELECTRICAL CHARACTERISTICS (continued) (T_A = 25°C, V_{CC} = 8.0 Vdc)

Characteristic	Condition	Pin	Min	Typ	Max	Unit
HORIZONTAL DRIVE						
Horizontal Position Adjust	0 < V55 < 5.0 V,	55				
Range	FH = 30 k – 56 kHz		–	10	–	%
Input Impedance	See Application Section 7		–	31	–	kΩ
Horizontal Drive Width Adjust	FH = 35 kHz, 0 < V44 < 5.0 V	44				
Range			2:1	–	1:2	%
Input Impedance			–	30	–	kΩ
Horizontal Flyback	See Application Section 4	46				
Threshold	Input Signal Should Not Fall		–	0.7	–	V
Input Amplitude	Below –0.2 V		0	–	8.0	V
Input Impedance			–	10	–	kΩ
Horizontal Drive		43				
Output Low	I_{sink} = 40 mA		0	–	0.3	Vdc
Output High	V43 = V_{CC}		–	–	100	µA
Time Delay from Flyback to Video Output Blanking	See Application Section 7	–	–	250	–	ns
Time Delay from Blanking to Video Output Blanking	See Application Section 7	–	–	400	–	ns
X–Ray Shutdown Activate Voltage	See Application Section 11	41	0.4	0.58	0.7	Vdc
Temperature Coefficient of X–Ray Threshold Voltage	–	41	–	–2.3	–	mV/°C
Horizontal Jitter	30 kHz < FH < 56 kHz	43	–	3.0	–	ns
VERTICAL PROCESSING						
Vertical Ramp Frequency	–	48	45	–	100	Hz
Vertical Ramp	FV = 50 Hz,	48				
Amplitude	R12 + VR4 = 820 kΩ		–	3.0	–	Vpp
Minimum Peak	R10 + VR3 =120 kΩ,		–	1.9	–	V
Maximum Peak	C6 = C7 = 1.0 µF		–	3.4	–	V
Output Current			–	2.0	–	mA
Non–Linearity			–	0.45	1.0	%
Vertical Ramp Free Running Temperature Drift	FV = 50 Hz	48	–	0.01	–	Hz/°C
Vertical Ramp Free Running Drift with V_{CC}	FV = 50 Hz	48	–	0.5	–	Hz/V
Vertical Ramp Discharge Rate (Retrace)	FV = 50 Hz	48	–	9.5	–	V/ms
Vertical Sync Detector Output/+V_E Sync		53	–	0	–	Vdc
Vertical Sync Detector Output/–V_E Sync		53	–	3.6	–	Vdc
Vertical Sync Input	–	4				
Input Impedance			–	22	–	kΩ
Input Level – Low			0	–	0.8	Vdc
Input Level – High			2.4	–	5.0	Vdc
VIDEO AMPLIFIERS						
Input Impedance	–	23, 25,27	100	–	–	kΩ
Internal DC Bias Voltage			–	2.4	–	Vdc
Output Signal Amplitude	V_{in} = 0.7 Vpp, V18 = 5.0 V	39, 34, 31	–	3.6	–	Vpp
Voltage Gain	V20 = V24 = V26 = 0 V		–	5.1	–	V/V
Contrast Control	V18 = 0 to 5.0 V; V20, 24, 26 = 0 V	18	–	20	–	dB
Subcontrast Control	V20, 24, 26 = 2.0 to 0 V; V18 = 5.0 V	20, 24, 26	1:2.5	–	–	–
Brightness Control	V19 = 0 to 5.0 V, Measure Pin 39, 34, 31 DC Level	19	–	±0.5	–	Vdc

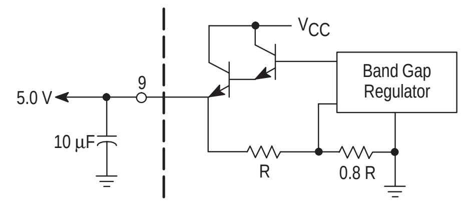
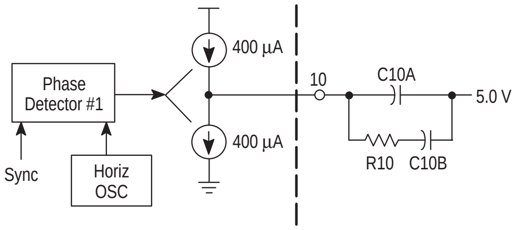
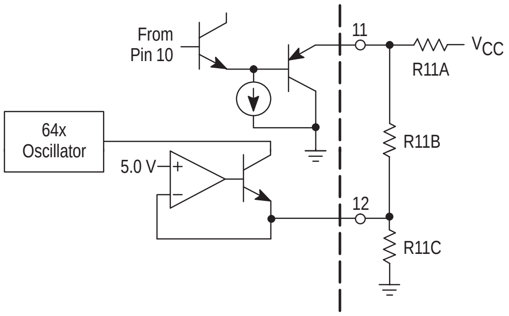
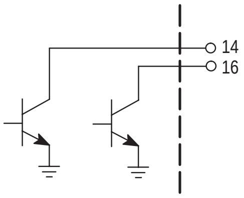
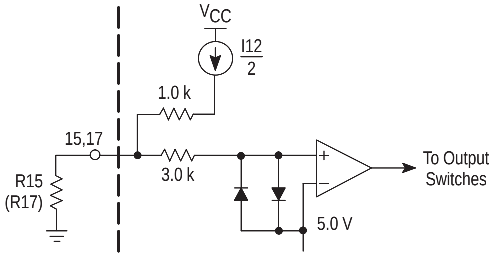
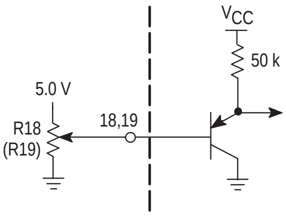
ELECTRICAL CHARACTERISTICS (continued) (T_A = 25°C, V_{CC} = 8.0 Vdc)

Characteristic	Condition	Pin	Min	Typ	Max	Unit
VIDEO AMPLIFIERS						
Emitter DC Level		39, 34, 31				Vdc
Minimum Brightness	V19 = 0 V		–	1.0	–	
Nominal Brightness	V19 = 2.5 V		1.25	1.5	1.75	
Maximum Brightness	V19 = 5.0 V		–	2.0	–	
Crosstalk, Amplifier to Amplifier	Frequency = 10 MHz	39, 34, 31	–	34	–	dB
Output Rise Time	V_{in} = 0.7 Vpp; V_{out} = 3.0 Vpp	39, 34, 31	–	5.0	–	ns
Output Fall Time			–	5.0	–	

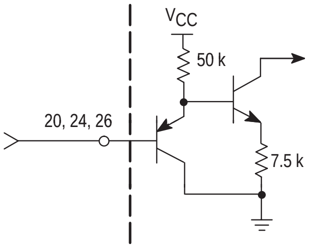
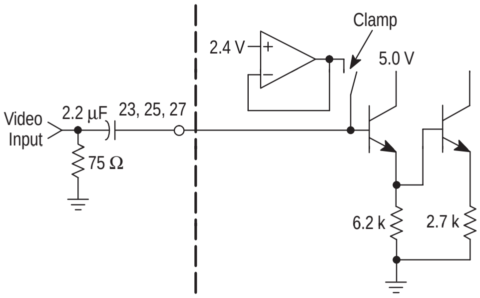
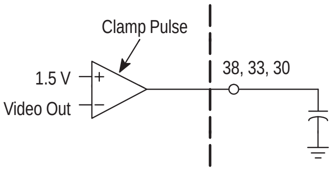
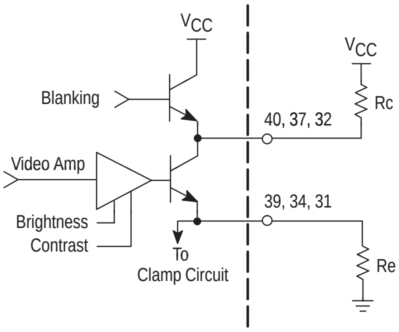
PIN FUNCTION DESCRIPTION

Pin	Name	Equivalent Internal Circuit	Description
1	Vertical Oscillator Capacitor		This capacitor should be 100 nF film type to give good temperature stability.
2	Vertical Hold Control		The potentiometer at Pin 2 adjusts the free running frequency of the oscillator. It should normally be set for about 55 Hz with no vertical signal input such that it will lock to 60 Hz.
3	Vertical Integrator Capacitor		The capacitor on this pin integrates the sync pulses with a long time constant. C3 is typically 0.01 µF.
4	Vertical TTL Sync		Vertical TTL Sync input. The input threshold voltage at this pin is 2.0 V.
5	Horizontal TTL Sync		Composite or Horizontal TTL Sync input. The input threshold voltage at this pin is 2.0 V.
6	Composite Video Input		This pin requires a coupling of min 100 nF. The composite sync input should consist of $-V_E$ sync signal only with amplitude > 500 mVpp. The source impedance of the sync signal should be <1.0 kΩ. Sync information at Pin 5 will override this pin, but signals at Pin 4 will not. Minimum pulse width is 2.0 µs.
7, 8	N/C		These two pins are internally connected to each other, and nothing else.

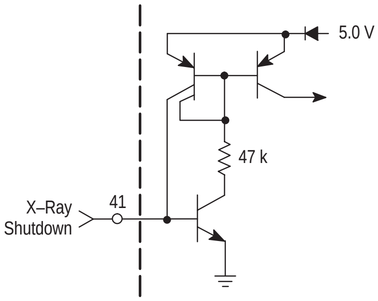
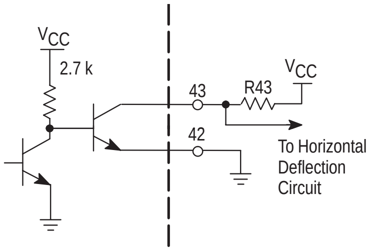
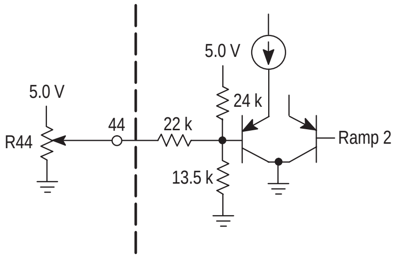
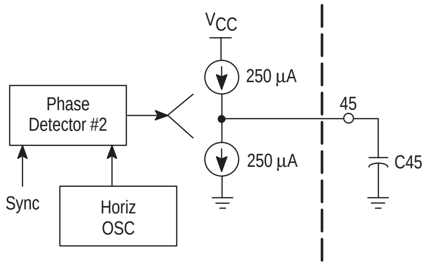
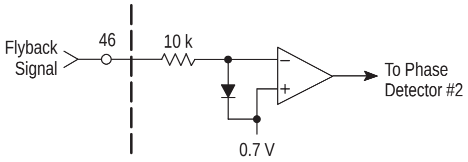
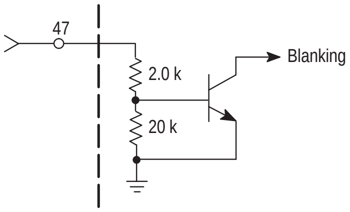
PIN FUNCTION DESCRIPTION (continued)

Pin	Name	Equivalent Internal Circuit	Description
9	5.0 V Regulator Output		5.0 V (±5%) regulator. Minimum 10 µF capacitor is required for noise filtering and compensation. Up to 20 mA can be supplied to external circuitry. It can source but not sink current. Output impedance is ≈ 10 Ω. This 5.0 V regulator is recommended for use as a reference only.
10	Phase Detector 1 Filter		External components at this pin will determine the PLL gain and phase characteristics. The capacitors should be non–polarized. The voltage at this pin nominally ranges from 1.5 V to 5.0 V with corresponding horizontal frequency from 25 kHz to 68 kHz.
11	Automatic Frequency Control		Pin 11 is a buffered equivalent of Pin 10, and ranges from a minimum of 1.5 V at horizontal high frequency to near 5.0 V at low frequency. Pin 11 can sink a maximum of 1.0 mA, but cannot source current.
12	Horizontal Frequency Range		The current out of Pin 12 determines the horizontal frequency by a current transfer constant of ≈ 122 Hz/µA. Pin 12 is internally maintained at 5.0 V.
13	Timebase Ground		Ground for the timebase section. Connect to a clean, low impedance ground.
14, 16	FH Switch A, B		Pin 14 (Switch A), and Pin 16 (Switch B) are open collector NPN switches to ground. Each switch is "on" when the horizontal frequency is higher than the set points set by resistors at Pins 15 and 17, respectively. Maximum voltage is 8.0 V, and maximum sink current is 20 mA.
15, 17	FH Switch A, B Threshold Setting		Pin 15 and Pin 17 are current mirror at 1/2 of Pin 12 current. External resistors at these pins set the horizontal frequency at which Pins 14 and 16 will switch, respectively. The threshold voltage is 5.0 V.
18	Contrast Control		The input control range is from 0 to 5.0 V. An increase of voltage increases contrast.
19	Brightness Control		The input control range is from 0 to 5.0 V. An increase of voltage increases brightness.

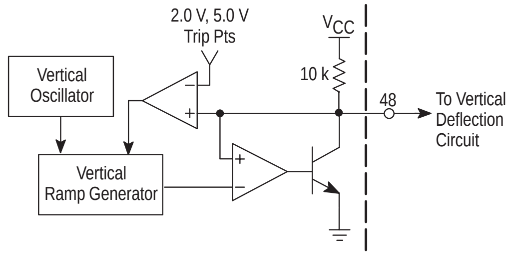
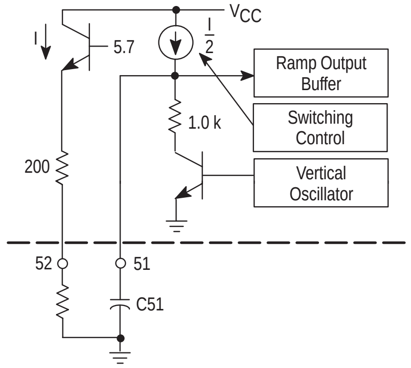
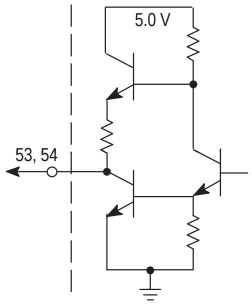
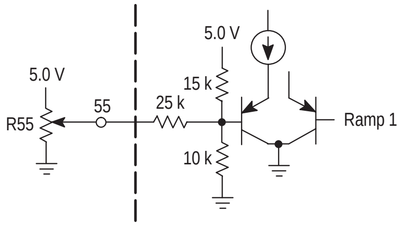
PIN FUNCTION DESCRIPTION (continued)

Pin	Name	Equivalent Internal Circuit	Description
 20 24 26	Subcontrast Control Channel 1 Channel 2 Channel 3		Subcontrast controls the gain of each video channel. 0 V for maximum gain, and 2.0 V for minimum gain.
21, 22	N/C		These two pins are internally connected to each other, and nothing else.
 23 25 27	Video Inputs Channel 1 Channel 2 Channel 3		The input coupling capacitor is used for input clamp storage. The maximum source impedance is 100 Ω. Polarity of the input video signal is positive. Amplitude should be nominally 0.7 Vpp.
28	Video Ground		Ground for the video section (video amplifiers, contrast and brightness controls, subcontrast, and video reference voltage). Noise from the timebase section, and other digital circuits, should not be allowed to produce ground bounce at this pin.
29	Video V_{CC1}		Connected to a 8.0, V ±5%, dc supply. Decoupling is required at this pin.
 38 33 30	Video Clamp Channel 1 Channel 2 Channel 3		Normally a 100 nF capacitor is connected to each of these pins.
  39 34 31 40 37 32	Video Emitter Output Channel 1 Channel 2 Channel 3 Video Collector Output Channel 1 Channel 2 Channel 3		Pins 39, 34, and 31 are the emitter outputs of the three video amplifier, and have an internal 33 Ω resistor. The emitter dc voltage is controlled by the brightness control. The current through each collector and emitter should not exceed 40 mA.
35, 36	N/C		These two pins are internally connected to each other, and nothing else.

PIN FUNCTION DESCRIPTION (continued)

Pin	Name	Equivalent Internal Circuit	Description
41	X–Ray Shutdown		If the voltage at this pin is > 0.58 V, the horizontal driver device (Pins 42 and 43) will be “on” until power is removed, or the voltage on this pin is taken below 0.4 V.
42	Horizontal Drive Ground		This emitter pin must be connected externally to a low impedance ground. Pin 43 is an open collector pin and normally is pulled up by a resistor to V_{CC}. Maximum current through Pins 42 and 43 must be less than 40 mA.
43	Horizontal Drive		
44	Horizontal Drive Width		Varying the voltage at this pin will change the horizontal drive duty cycle. As the voltage of this pin is increased, the “on” time at Pin 43 is decreased. Input impedance is ≈ 30 kΩ.
45	Secondary Phase Detector Filter		Typically a 10 to 100 nF decoupling capacitor is connected to this pin.
46	Horizontal Flyback		The flyback signal should be a $+V_E$ pulse of peak voltage 8.0 V. The internal switching voltage is 0.7 V and it controls the secondary PLL Input impedance is ≈ 10 kΩ
47	Video Blanking Input		The video blanking signal should be positive pulse in the range of 1.5 to 4.0 V.

PIN FUNCTION DESCRIPTION (continued)

Pin	Name	Equivalent Internal Circuit	Description
48	Vertical Ramp Output		This ramp signal drives the external vertical output devices. Voltage ramps from 2.0 V to less than 5.0 V, depending on frequency and components at Pins 51 and 52. Loading on this pin must be > 30 kΩ to avoid distorting or clipping the ramp.
49, 50	N/C		These two pins are internally connected to each other, and nothing else.
51	Vertical Ramp Capacitor		The slope of the output ramp is determined by the components at Pins 51 and 52. The resistor at Pin 52 sets the charging current of the capacitor, and therfore the vertical height of the picture. The linearity of the ramp can be modified by external feedback.
52	Vertical Size Control		
53	Vertical Sync Polarity Detector		The output goes low when the vertical sync input polarity is positive. It goes high when the vertical sync input polarity is negative.
54	Horizontal Sync Polarity Detector		The output goes low when the horizontal sync input polarity is positive. It goes high when the horizontal sync input polarity is negative.
55	Horizontal Position Control		Varying the voltage at this pin will change the horizontal position of the picture. Input impedance is ≈ 31 kΩ.
56	Timebase V_{CC2}		Connected to a 8.0 V, ±5%, dc supply. Decoupling is required at this pin.

APPLICATION INFORMATION

The MC13081X is an integrated multisync color monitor processor. It combines horizontal/vertical deflection processing circuitry and video pre–amplifiers into a single device.

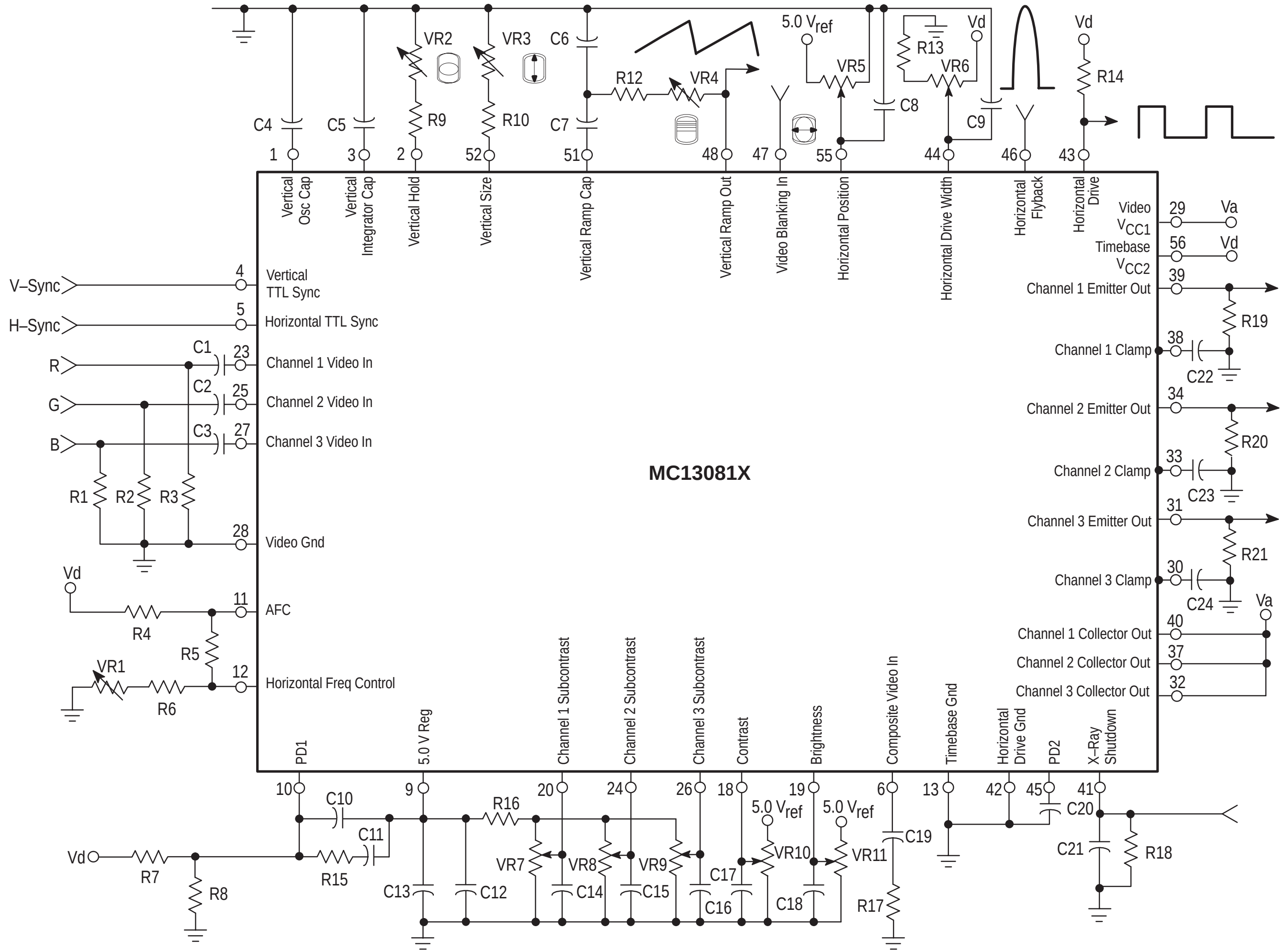
The overall timebase section consists of two parts: horizontal and vertical. The horizontal timebase can be operated from 30 kHz to 64 kHz, and can be driven from TTL separate sync, composite sync, or a composite video signal. There are two PLLs which ensure proper timing throughout the whole system. The first PLL provides line locking of the horizontal sync signal with the built–in oscillator, while the second one maintains fixed timing with the horizontal flyback signal such that a stable display can be achieved.

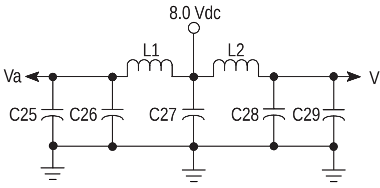
The vertical timebase section operates from 45 Hz to 100 Hz, and can receive various sync signals as the horizontal one does. This section consists of an oscillator and a ramp generator. Adjustments include linearity, ramp amplitude, and minimum free running frequency in the absence of sync signal.

The video section has three 70 MHz bandwidth pre–amplifiers. The outputs of these amplifiers are uncommitted collector/emitter facilitating cascode configuration with subsequent stages. Controls include brightness and contrast. In addition, the voltage gain of each amplifier can be adjusted individually which provides flexibility in adjusting color correctness. Blanking and clamping signals are provided to the amplifiers internally from the timebase section. Additionally, a blanking signal can also be supplied externally.

Separate power supply and ground pins are provided to the timebase and video section in order to minimize the cross interference between these two sections.

Figure 2. Application Circuit





R1–R3,R17	75 Ω
R4–R6	15 kΩ
R7	3.9 MΩ
R8	6.8 MΩ
R9	8.2 kΩ
R10	220 kΩ
R12	220 kΩ
R13	2.2 kΩ
R14	470 Ω
R15	5.6 kΩ
R16	5.1 kΩ
R18	10 kΩ
R19–R21	330 Ω

C1–C3	2.2 µF
C4,C6–C9,C13–C19,C22–C24,C29	100 nF
C5,C20	10 nF
C10	1.0 nF
C11	100 nF
C12	22 µF
C21	10 nF
C27	100 µF
C26,C28	47 µF
C30,C31	1.0 µF

L1	50 µH
L2	50 µH
VR1,VR5–VR11	10 kΩ
VR2	5.0 kΩ
VR3	200 kΩ
VR4	1.0 MΩ

The following describes a step–by–step procedure in using the MC13801 for a typical multisync color monitor chassis; component notations refer to Figure 2.

1. Horizontal Frequency Range Resistor Network (Pins 11, 12)

F_{Hm} = Minimum Horizontal Frequency
F_{Hx} = Maximum Horizontal Frequency
Oscillator Transfer Constant = 122 Hz/µA

$$R5 = \frac{6.35 \text{ x } 10^8}{F_{Hx} - F_{Hm}}$$

$$R6 = \frac{5}{\dfrac{F_{Hx}}{122 \text{ x } 10^6} - \dfrac{3.5}{R5}}$$

$$R4 \leq \frac{V_{CC} - 6.0}{1.5} \text{ x } R5 \text{ and } \frac{V_{CC} - 1.5}{R4} < 1.0 \text{ mA}$$

For most applications, R4 = R5 provides the required results.

NOTE: In order to compensate device/component tolerance, a potentiometer is recommended in series with R6, as VR1.

2. Horizontal Frequency Range Phase Detector Filter Network (Pin 10)

Typical values are:
C10 = 1.0 nF
C11 = 100 nF
R15 = 5.6 k
C11 ≥ 100 x C10

NOTE: C10 and C11 should have less than 1.0 µA leakage.

3. Horizontal Free Running Frequency

The voltage at Pin 10 will be buffered to Pin 11, and hence control the internal oscillator. In the absence of horizontal sync signal, the free running horizontal frequency will vary between preset minimum and maximum horizontal frequency values.

If an undetermined free running frequency value is not desired, a large impedance resistor can be used to pull Pin 10 to V_{CC} or Gnd, and the free running frequency will be equal to F_{Hm} or F_{Hx}, respectively.

The free running frequency can also be set to any value within the horizontal frequency range by using a voltage divider, as R7 and R8 indicate.

$$V11 = V_D \text{ x } \frac{R7}{R7 + R8}$$

$$I12 = \frac{V11}{R6 + VR1} - \frac{V11 - 5}{5}$$

$$\text{Free Running Frequency} = I12 \text{ µA x } \frac{122 \text{ Hz}}{\text{µA}}$$

The above formula provides the ratio of R7 and R8. The values chosen should be similar to those shown in Figure 2.

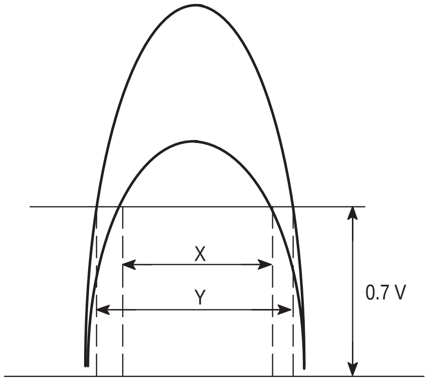
4. Horizontal Flyback Input (Pin 46)

The horizontal flyback signal not only provides proper timing reference for the horizontal drive output, but also supplies the necessary blanking for the video outputs.

There are two precautions for the flyback input. First, the signal should have a zero volt reference, and second, the peak value should be as near to V_{CC} as possible.

The threshold voltage for Pin 46 is 0.7 V. The blanking period depends on the amplitude, as shown in Figure 3 (X and Y, respectively). A larger amplitude provides better consistency and control of the blanking period.

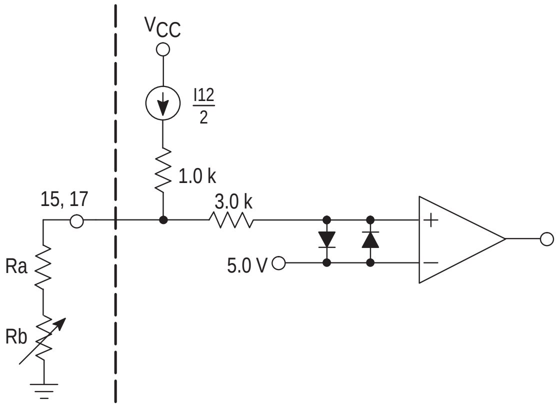
Figure 3. Voltage for Flyback



5. Frequency Switch (Pin 14 to 17)

There are two frequency switches available for screen size compensation for different timing standards. Each switch will turn on at the switch frequency set with its external resistor. See Figure 4.

Figure 4. FH Switches



The switch frequency is calculated as follow:

$$SF = \text{Switch Frequency} \qquad SF = \frac{5 \text{ x } 2 \text{ x } 122 \text{ x } 10^6}{Ra + Rb}$$

In considering the ratio of Ra to Rb, the following parameters, and their tolerances, need to be clarified:

1. I_{osc}	±10%
2. 5.0 V_{ref}	±5%
3. V_{hys}	±5%
4. Ra, Rb	±?%

Internally, the lock–in horizontal frequency will build up a current reference, and half of this current reference is used for setting up a voltage and then compared with the internal 5.0 V_{ref}. Looking at the four parameters above, the first three are IC related, while the last item depends on the external component tolerance.

By adding up the first three items, the value of Ra and Rb should be chosen to compensate for about 20% of system tolerance.

Therefore, if Ra is chosen to be 70% of the calculated value (Ra + Rb), Rb should be 60% of (Ra + Rb). That means, the overall adjustment is about 70% to 130%, which provides additional ±10% margin.

During normal operation, the frequency switch will switch “off” when the pin voltage falls 60 mV below the 5.0 V reference voltage (≈ 4.94 V), and will switch “on” when the pin voltage rises to 40 mV above the 5.0 V reference (≈ 5.04 V).

An Example: Require Trip Point @ 35 kHz

$$I12 = \frac{35 \times 10^3}{122}\ \mu A$$

$$\text{Trip Point Reference Current} = \frac{I12}{2}$$

$$= \frac{35\ k}{122 \times 2}\ \mu A$$

$$Ra + Rb = \frac{5.0\ V}{\frac{35\ k}{122 \times 2}\ \mu A}$$

$$= 34857\ \Omega$$

$$\text{Hysteresis @ 35 kHz} = \frac{5.04 - 4.94\ V}{34857\ \Omega} \times \frac{122\ Hz}{\mu A}$$

$$\approx 350\ Hz$$

From above, Ra + Rb = 34857 Ω

Select Ra = 24 k, and Rb = 20 k Trim Pot

The Temperature Coefficient of the potentiometer can also be considered. If the value of the potentiometer and Ra vary by 1% (for example) over temperature, the error would be:

$$5 \times \left\{\frac{1}{34857 \times 0.99} - \frac{1}{34857 \times 1.01}\right\} \times \frac{122\ Hz}{\mu A}$$

$$\approx 350\ Hz$$

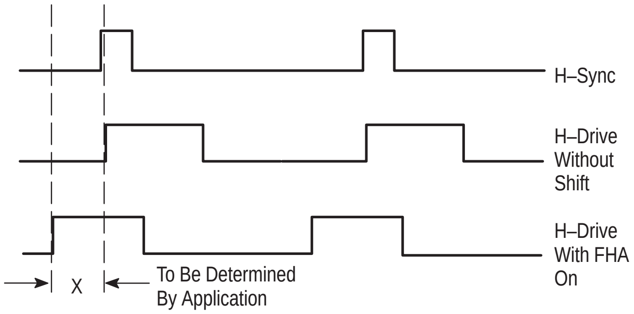
6. Horizontal Position Compensation for Selected Scan Frequency in Using FHA Switch

Refering to Figure1 (block diagram), there is an output from the FHA switch to the horizontal drive output. When the FHA switch is switched on, at a specified horizontal frequency, there is a 1/8th horizontal line shift of H–Ramp1. Referring to Figures 5 and 9, a shift of H–Ramp1 will result in a shift of the H–Drive output timing with respect to flyback input.

The exact H–Drive output shift will be determined by the PD2 voltage (Pin 45), which is generated by the flyback input and the internal Comp1 output. That is related to the H–Drive output transistor storage time.

This function is particularly useful for high frequency scan rates. The higher the frequency, the more significant the storage time becomes, compared to the horizontal scan time.

Figure 5.



7. Proper Horizontal Phase Control

The horizontal adjustment range depends on the phase angle between the H–Sync signal and the horizontal flyback input. In reality, the actual adjustment range is a combination of horizontal frequency, front porch/back porch timing, flyback pulse width, and horizontal output transistor storage time. The following paragraph conveys the concept for normal operation.

There are two clamping situations for video signals. In case 1, separate VTTL and HTTL sync are provided, the video signal is clamped at sync tip, and the dc voltage built up is used for black level reference. In this instance, the clamp pulse has the same pulse width as H–Sync, and nearly the same position. This clamp pulse is blanked out internally. In order to allow the video output to complete the blanking action during horizontal retrace, the horizontal phase should not be over–adjusted. See Figure 6 for a pictorial perception. Accordingly, the total horizontal position adjustment range is calculated as the sum of Δt1 and Δt2.

Should the phase of horizontal flyback/H–Sync move further left or right from the normal adjustment range, the black level reference voltage will be restored, and consequently a slightly brighter than screen dark region will be observed on–screen. See Figure 7 for pictorial explanation.

$$\text{Horizontal Blanking Time} = FP_{time} + \text{Sync Width} + BP_{time} = T_{HB}$$

Criterion for Normal Operation:

$$|\Delta t1| < \frac{T_{HB}}{2} \qquad |\Delta t2| < \frac{T_{HB}}{2}$$

In other words, the left/right 0.7 V threshold flyback reference should be within the H–Sync pulse (shaded area of Figure 6).

Figure 6. Horizontal Position Adjustment at Normal Operation

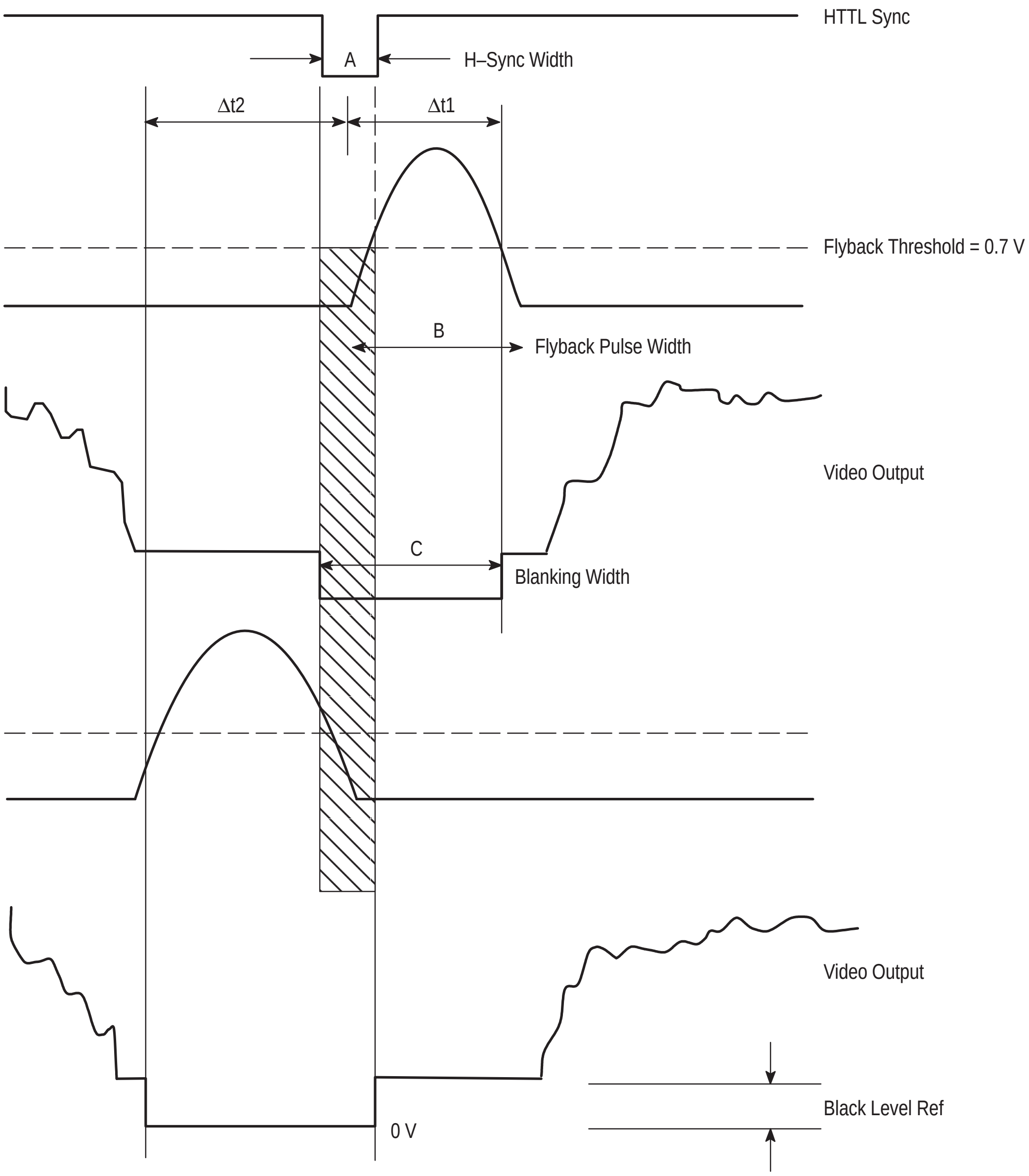
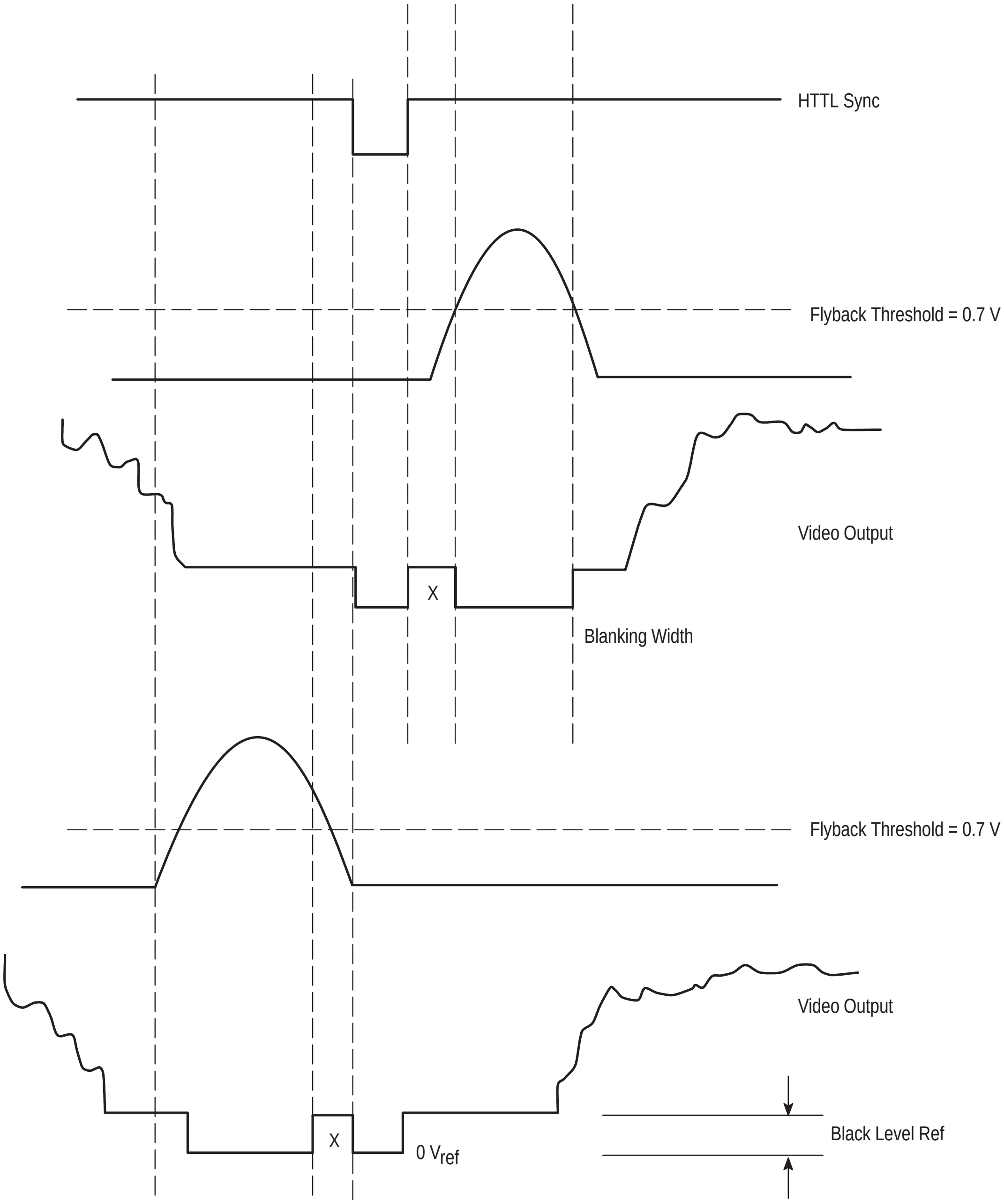
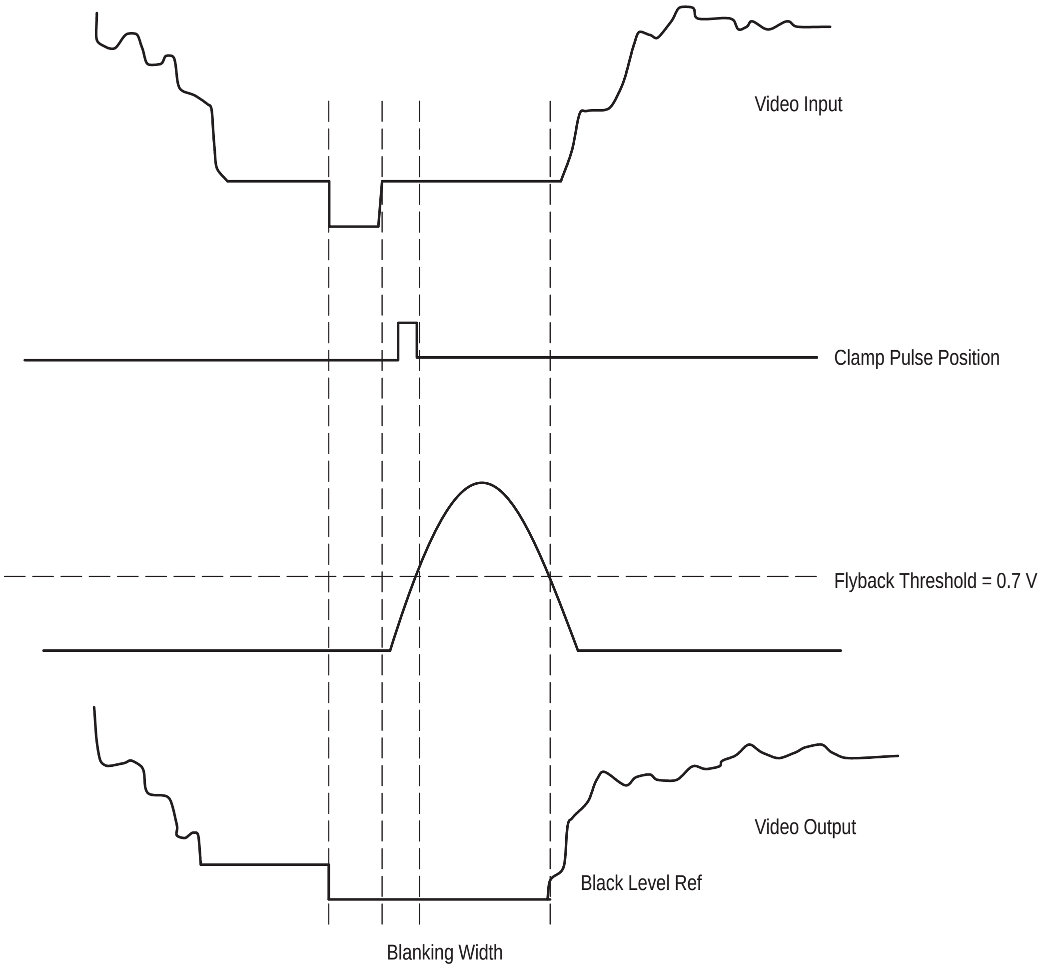


Figure 7. Horizontal Position Adjustment at Overscan Operation



NOTE: Region X will appear as bright vertical stripe.

Figure 8.



In case 2, composite sync is used instead of VTTL and HTTL sync, the clamp pulse is located at the backporch of the video signal, and the width of the clamp pulse is calculated as follows:

$$\text{Clamp Pulse Width} = \frac{1}{64 \text{ x Line Frequency}} \text{ x } 3$$

Blanking Width = Sync Width + Clamp Pulse Width
+ Flyback Threshold (0.7 V) (See Figure 8)

From the above diagram, it can be seen that the horizontal position adjustment is basically the same as case 1 except slightly wider with the addition of clamp pulse blanking.

8. Horizontal Timing Relationship for Phase Detector 2

The following paragraphs explain the PLL2 mechanism. Figure 9 portrays the timing signals of various parts of the IC.

In using the H–Sync pulse, which is generated from PLL1, a horizontal ramp 1 signal is created. H–Ramp1 starts at 1/4th line before H–Sync and the ramping slope is directly proportional to horizontal frequency. The lower tip of this ramp is at approximately 1.2 V, and the amplitude is about 4.2 V. By adjusting the dc bias to the H–Phase control, a pulse waveform is derived from this H–Ramp1.

A phase detector is used to compare the phase between the pulse generated above, and the incoming flyback pulse. An integrating capacitor is applied to generate a dc voltage. This dc voltage, PD2F output, is used to slice the H–Ramp1 signal in order to generate Comp2 output pulse.

A second ramp signal, H–Ramp2, is triggered from this Comp2 output. By applying a dc voltage (H–Width control) to H–Ramp2, the Comp3 output pulses are generated.

The H–Drive output is formed by the rising edge of Comp2 output and the rising edge of Comp3 output.

It can be seen from Figure 9, if the H–Phase control is over or under driven, it will reach the upper/lower tip of H–Ramp1, and thus PLL2 will be disturbed.

Figure 9. Horizontal Timing for PLL2 Internal Sections

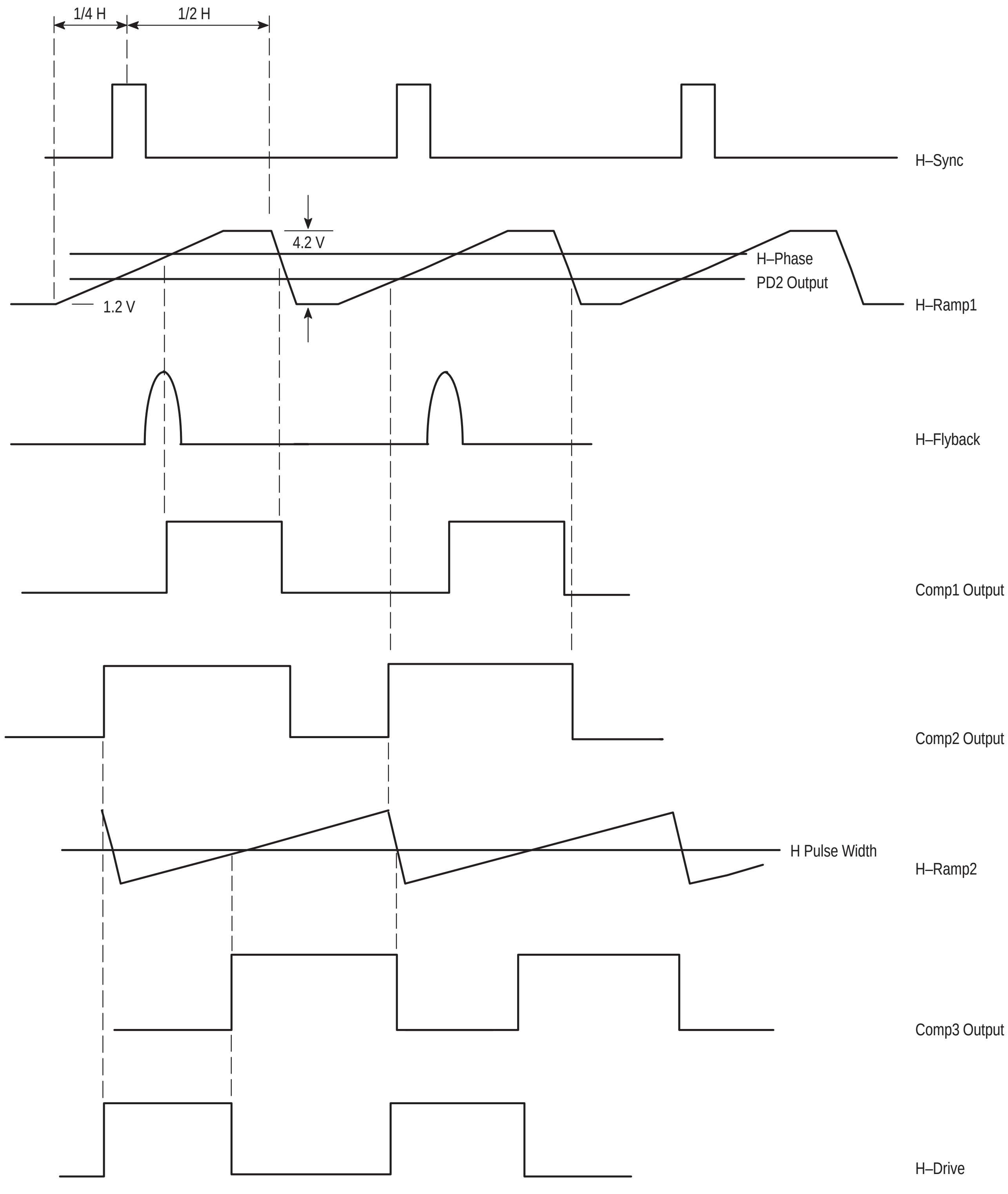
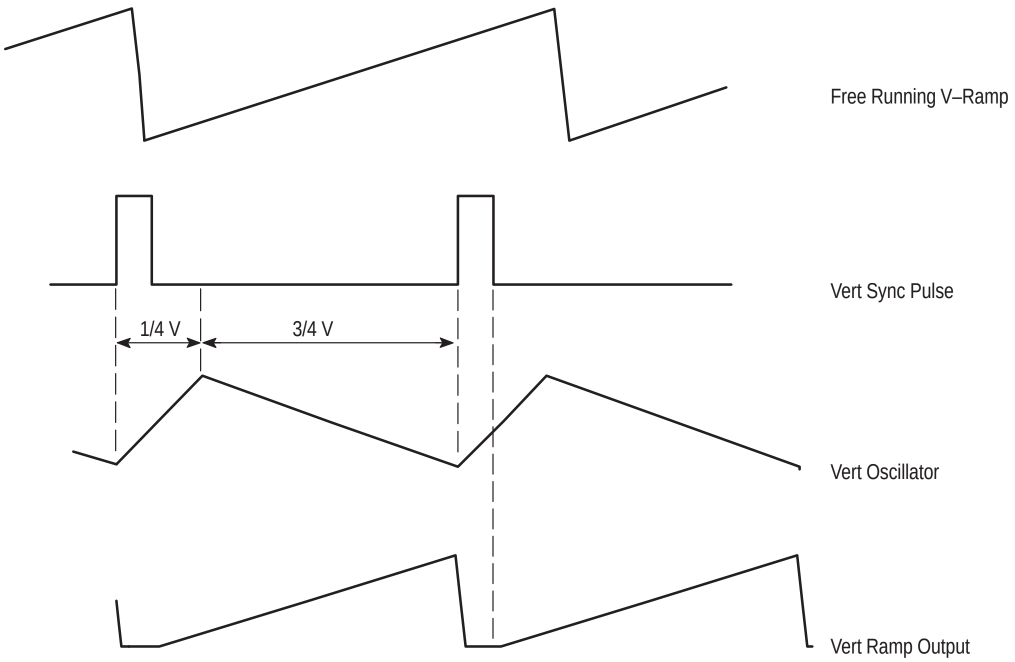


Figure 10. Vertical Section



9. Vertical Frequency Range (Pins 48, 51, 52)

The MC13081X vertical oscillator is an injection–lock type. The device can handle vertical frequency from 45 Hz to 100 Hz.

The internal ramp generator will generate a ramp output in the absence of a V–Sync signal. Upon receiving an external vertical sync pulse, the ramp up portion is forced to retrace, and therefore, the vertical ramp output is synchronized with incoming V–Sync.

The slope of the Vertical Ramp output is directly proportional to the current flowing out of Pin 52. Half of this current is used to charge up the Vertical Ramp Capacitor. As the charging current is increased, so does the ramp slope. External feedback can be provided from Pin 48 to Pins 51 and 52 for linearity adjustment.

10. Vertical Free Running Frequency (Pins 1, 2)

The purpose of the vertical oscillator is to maintain a vertical ramp to the deflection circuitry in the event the vertical sync is not present. Because of the injection–lock type, the free running frequency must be lower than the system’s lowest vertical frequency.

While various combinations of C4 and R9 can produce a given frequency, it is recommended C4 be 0.1 µF in order to obtain practical values for R9. The free running frequency should be set at about 10% lower than the minimum operating vertical frequency (54 Hz for a 60 Hz system).

R9 is then calculated from:

$$R9 = \frac{V_{CC} - 1.4}{96 \text{ x } C4 \text{ x } FV} - 2.5 \text{ k}$$

Connecting a potentiometer, (VR2) provides “Vertical Hold” adjustment.

11. X–Ray Shutdown Protection (Pin 41)

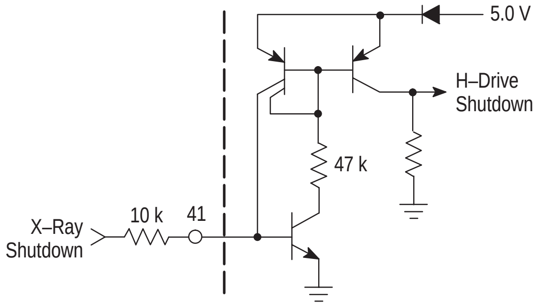
The X–Ray input (Pin 41) permits shutting off the horizontal drive, usually by external circuitry which monitors faults within the high voltage supply, such as excess anode current. This input is activated by taking it above ≈ 0.6 V which causes the drive transistor at Pin 43 to be turned on (low) permanently by an internal latch.

An external resistor must be connected to Pin 41 to limit the input current, and to assist with the latching action (see Figure 11). 10 kΩ is a typical value, but the value can be chosen based on the specifies of the driving circuit. The external resistor reduces the sensitivity of Pin 41 to noise and transients which may otherwise result in false latches.

To resume normal operation (after correction of the fault), lower Pin 41 below 0.4 V. If the external circuit’s normal operation does not take it below 0.4 V, but does take it below 0.6 V, then recycle V_{CC} “off”–“on”. If the pin is not used, it must be connected to ground.

The minimum holding current to keep the latch on is ≈ 70 µA, while the minimum turn–on current is ≈ 0.4 µA.

Figure 11. X–Ray Shutdown Circuit



MOTOROLA

MC13280AY
MC13281A/B

80/100 MHz VIDEO PROCESSOR

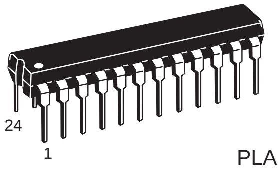
Advance Information

80/100 MHz Video Processor

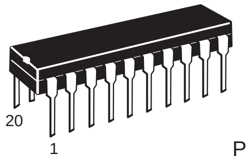
The MC13280AY and MC13281A/B are three channel wideband amplifiers designed for use as a video pre–amplifier in high resolution RGB color monitors.

Features:

- 4.0 Vpp Output Swing
- 3.5 ns Rise/Fall Time, 100 MHz Bandwidth (MC13281A/B)
- 4.3 ns Rise/Fall Time, 80 MHz Bandwidth (MC13280AY)
- Subcontrast Controls for Each Channel
- Main Contrast Control
- Blanking and Clamping Inputs
- Packages: NDIP–24 and NDIP–20
- A Single PC Board Pattern Can Accept the MC13281A and the MC13282A (Video Amplifier with OSD)



P SUFFIX
PLASTIC PACKAGE
CASE 724

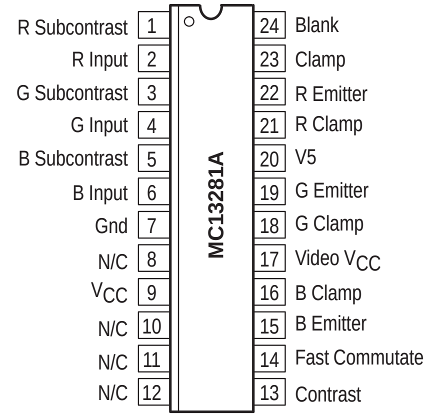


P SUFFIX
PLASTIC PACKAGE
CASE 738

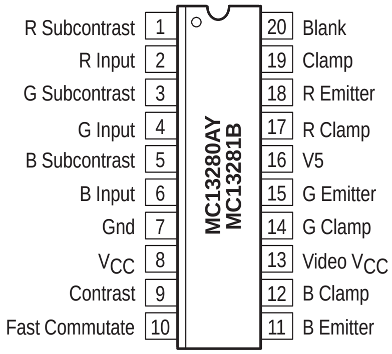
ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC13280AYP	T_A = 0° to +70°C	Plastic DIP
MC13281AP		Plastic DIP
MC13281BP		Plastic DIP

PIN CONNECTIONS



(Top View)



(Top View)

ABSOLUTE MAXIMUM RATINGS

Rating	Pin	Value	Unit
Power Supply Voltage	V_{CC} Video V_{CC}	–0.5, 10 –0.5, 10	Vdc
Voltage at Video Amplifier Inputs	2, 4, 6	–0.5, +5.0	Vdc
Collector–Emitter Current (Three Channels)	Video V_{CC}	120	mA
Storage Temperature	–	–65 to +150	°C
Junction Temperature	–	150	°C

NOTES: 1. Devices should not be operated at these limits. Refer to “Recommended Operating Conditions” section for actual device operation.
2. ESD data available upon request.

RECOMMENDED OPERATING CONDITIONS

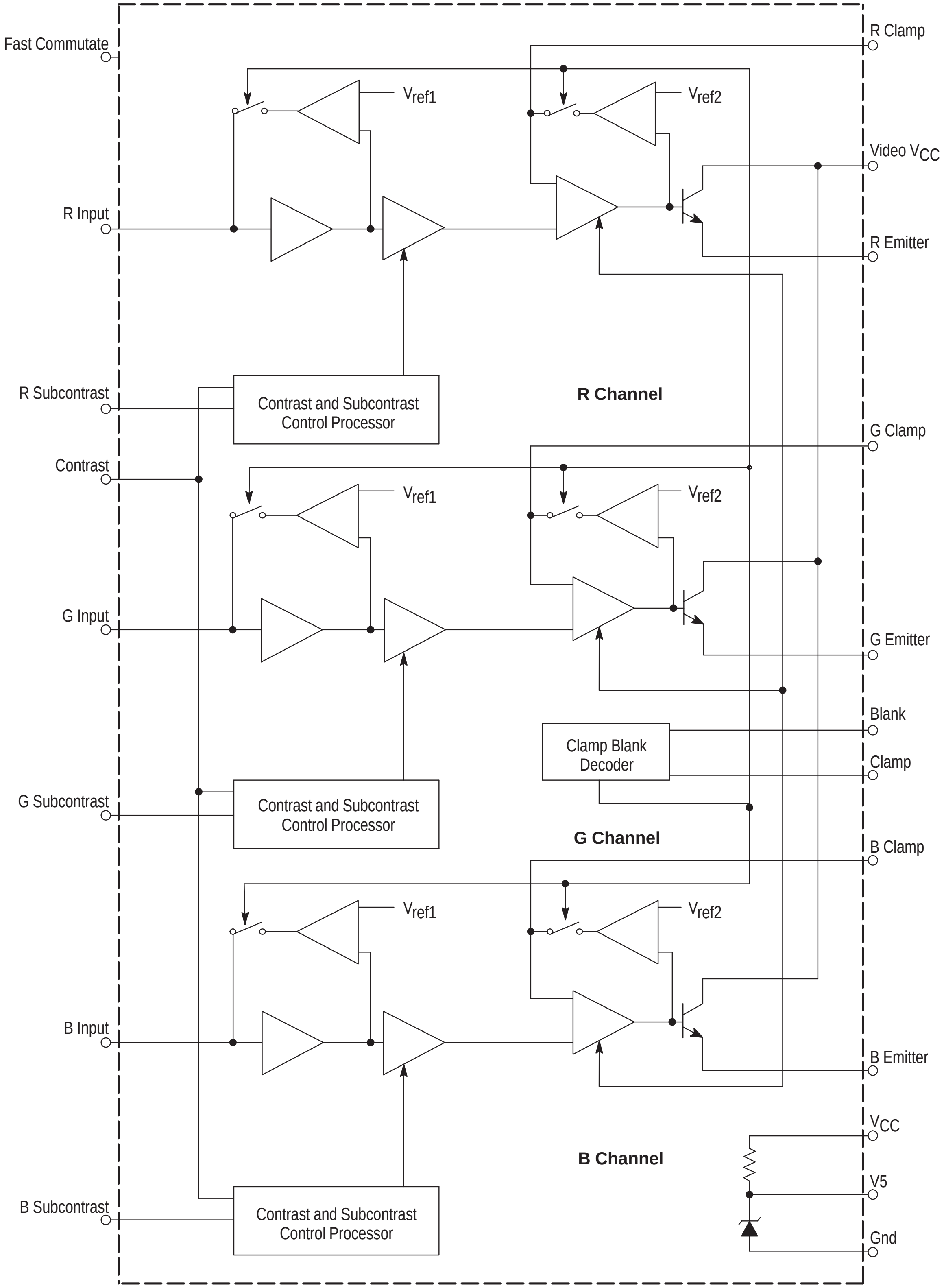
Characteristic	Pin	Min	Typ	Max	Unit
Power Supply Voltage	V_{CC}, Video V_{CC}	7.6	8.0	8.4	Vdc
Contrast Control	Contrast	0	–	5.0	Vdc
Subcontrast Control	1, 3, 5	0	–	5.0	Vdc
Blanking Input Signal Amplitude	Blank	0	–	5.0	V
Clamping Input Signal Amplitude	Clamp	0	–	5.0	V
Video Signal Amplitude (with 75 Ω Termination)	2, 4, 6	–	0.7	1.0	Vpp
Collector–Emitter Current (Total for Three Channels)	Video V_{CC}	0	–	50	mA
Clamp Pulse Width	Clamp	500	–	–	ns
Operating Ambient Temperature	–	0	–	70	°C

ELECTRICAL CHARACTERISTICS (Refer to Test Circuit Figure 1, T_A = 25°C, V_{CC} = 8.0 Vdc.)

Characteristic	Condition	Pin	Min	Typ	Max	Unit
Input Impedance	–	2, 4, 6	100	–	–	kΩ
Internal DC Bias Voltage			–	2.4	–	Vdc
Output Signal Amplitude	V2, V4, V6 = 0.7 Vpp V1, V3, V5 = 5.0 V Contrast = 5.0 V	R, G, B Emitters	3.6	4.0	–	Vpp
Voltage Gain			–	5.6	–	V/V
Contrast Control	Contrast = 5.0 to 0 V V1, V3, V5 = 5.0 V	Contrast	–	–26	–	dB
Subcontrast Control	V1, V3, V5 = 5.0 to 0 V Contrast = 5.0 V	1, 3, 5	–	–26	–	dB
Emitter DC Level	–	–	1.0	1.2	1.4	Vdc
Blanking Input Threshold	–	Blank	–	1.25	–	V
Clamping Input Threshold	–	Clamp	–	3.75	–	V
Video Rise Time	V2, V4, V6 = 0.7 Vpp V_{out} = 4.0 Vpp R_L > 300 Ω, C_L < 5.0 pF	R, G, B Emitters				ns
MC13280AY			–	4.3	–	
MC13281A/B			–	3.5	–	
Video Fall Time	V2, V4, V6 = 0.7 Vpp V_{out} = 4.0 Vpp R_L > 300 Ω, C_L < 5.0 pF	R, G, B Emitters				ns
MC13280AY			–	4.3	–	
MC13281A/B			–	3.5	–	
Video Bandwidth	V2, V4, V6 = 0.7 Vpp V1, V3, V5, Contrast = 5.0 V R_L > 300 Ω, C_L < 5.0 pF	R, G, B Emitters				MHz
MC13280AY			–	80	–	
MC13281A/B			–	100	–	
Power Supply Current	V_{CC}, Video V_{CC} = 8.0 V	–	–	70	–	mA

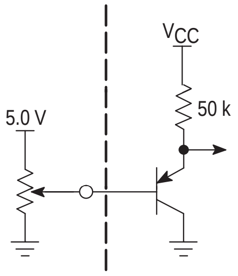
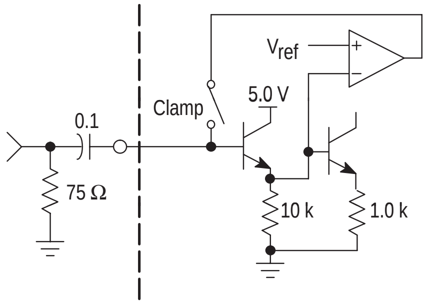
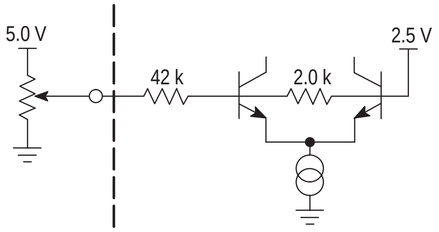
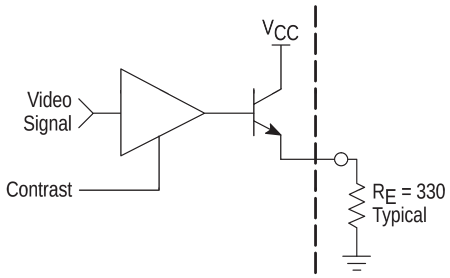
NOTE: It is recommended to use a double sided PCB layout for high frequency measurement (e.g., rise/fall time, bandwidth).

Figure 1. Internal Block Diagram

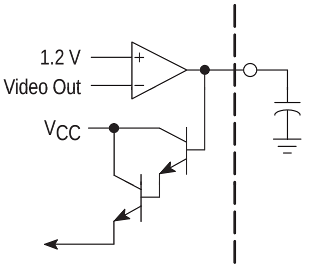
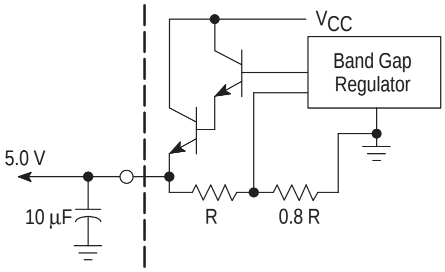
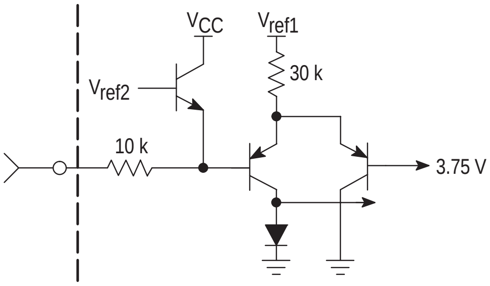
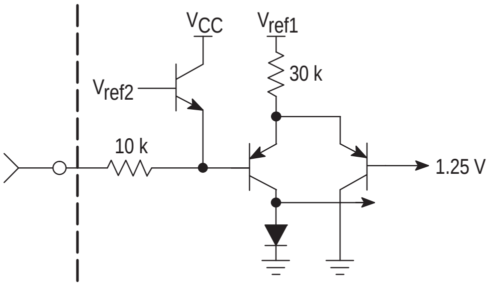


This device contains 272 active transistors.

PIN FUNCTION DESCRIPTION

MC13280AY MC13281B Pin	MC13281A Pin	Name	Equivalent Internal Circuit	Description
1	1	R Subcontrast Control		These pins provides a maximum of 26 dB attenuation to vary the gain of each video amplifier separately. Input voltage is from 0 to 5.0 V. Increasing the voltage will increase the contrast level.
3	3	G Subcontrast Control		
5	5	B Subcontrast Control		
2	2	R Input		The input coupling capacitor is used for input clamping storage. The maximum source impedance is 100 Ω. Input polarity of the video signal is positive. Nominal 0.7 Vpp input signal is recommended (maximum 1.0 Vpp).
4	4	G Input		
6	6	B Input		
7	7	Ground		Ground pin. Connect to a clean, solid ground.
N/A	8	N/C		Connected to ground.
	10	N/C		
	11	N/C		
	12	N/C		
8	9	V_{CC}		Connect to 8.0 Vdc supply, ±5%. Decoupling is required at this pin.
9	13	Contrast		Overall Contrast Control for the three channels. The input range is 0 V to 5.0 V. An increase of voltage increases the contrast.
10	14	Fast Commutate		Must be connected to ground.
11	15	B Emitter Output		The video outputs are configured as emitter–followers with a driving capability of about 15 mA each. The dc voltage at these three emitters is set to 1.2 V (black level). The dc current through the output stage is determined by the emitter resistors (typically 330 Ω).
15	19	G Emitter Output		
18	22	R Emitter Output		

PIN FUNCTION DESCRIPTION (continued)

MC13280AY MC13281B Pin	MC13281A Pin	Name	Equivalent Internal Circuit	Description
12	16	B Clamp Capacitor		A 100 nF capacitor is connected to each of these pins. The capacitor is used for video output dc restoration.
14	18	G Clamp Capacitor		
17	21	R Clamp Capacitor		
13	17	Video V$_{CC}$		Connect to 8.0 V dc supply, ±5%. The V$_{CC}$ is for the video output stage. It is internally connected to the collectors of the output transistors.
16	20	5.0 V$_{ref}$ (V5)		5.0 V regulator. Minimum 10 µF capacitor is required for noise filtering and compensation. It can source up to 20 mA but not sink current. Output impedance is ≈ 10 Ω. Recommended for use as a voltage reference only.
19	23	Clamp		This pin is used for video clamping. The threshold clamping level is 3.75 V.
20	24	Blank		This pin is used for video blanking. The threshold blanking level is 1.25 V.

FUNCTIONAL DESCRIPTION

The MC13280AY and MC13281A/B are composed of three video amplifiers, clamping and blanking circuitry with contrast and subcontrast controls. Each video amplifier is designed to have a –3.0 dB bandwidth of 100 MHz (MC13281, 80 MHz for the MC13280) with a gain of up to about 5.6 V/V, or 15 dB.

Video Input

The video input stages are high impedance and designed to accept a maximum signal of 1.0 Vpp with 75 Ω termination (typically) provided externally. During the clamping period, a current is provided to the input capacitor by the clamping circuit which brings the input to a proper dc level (nominal 2.0 V). The blanking and clamping signals are to be provided externally, with their thresholds at 1.25 V and 3.75 V, respectively.

Video Output

The video output stages are configured as emitter–followers, with a driving capability of about 15 mA for each channel. The dc voltage at these three emitters is set to 1.2 V (black level). The dc current through each output stage is determined by the emitter resistor (typically 330 Ω).

Contrast Control

The contrast control varies the gain of three video amplifiers from a minimum of 0.3 V/V to a maximum of 5.6 V/V when all subcontrast levels are set to 5.0 V.

Subcontrast Control

Each subcontrast control provides a maximum of 26 dB attenuation on each video amplifier separately.

Clamp Pulse Input

The clamping pulse is provided externally, and the pulse width must be no less than 500 ns.

Blank Pulse Input

The blanking pulse is used to blank the video signal during the horizontal sync period, or used as a control pin for video mute function.

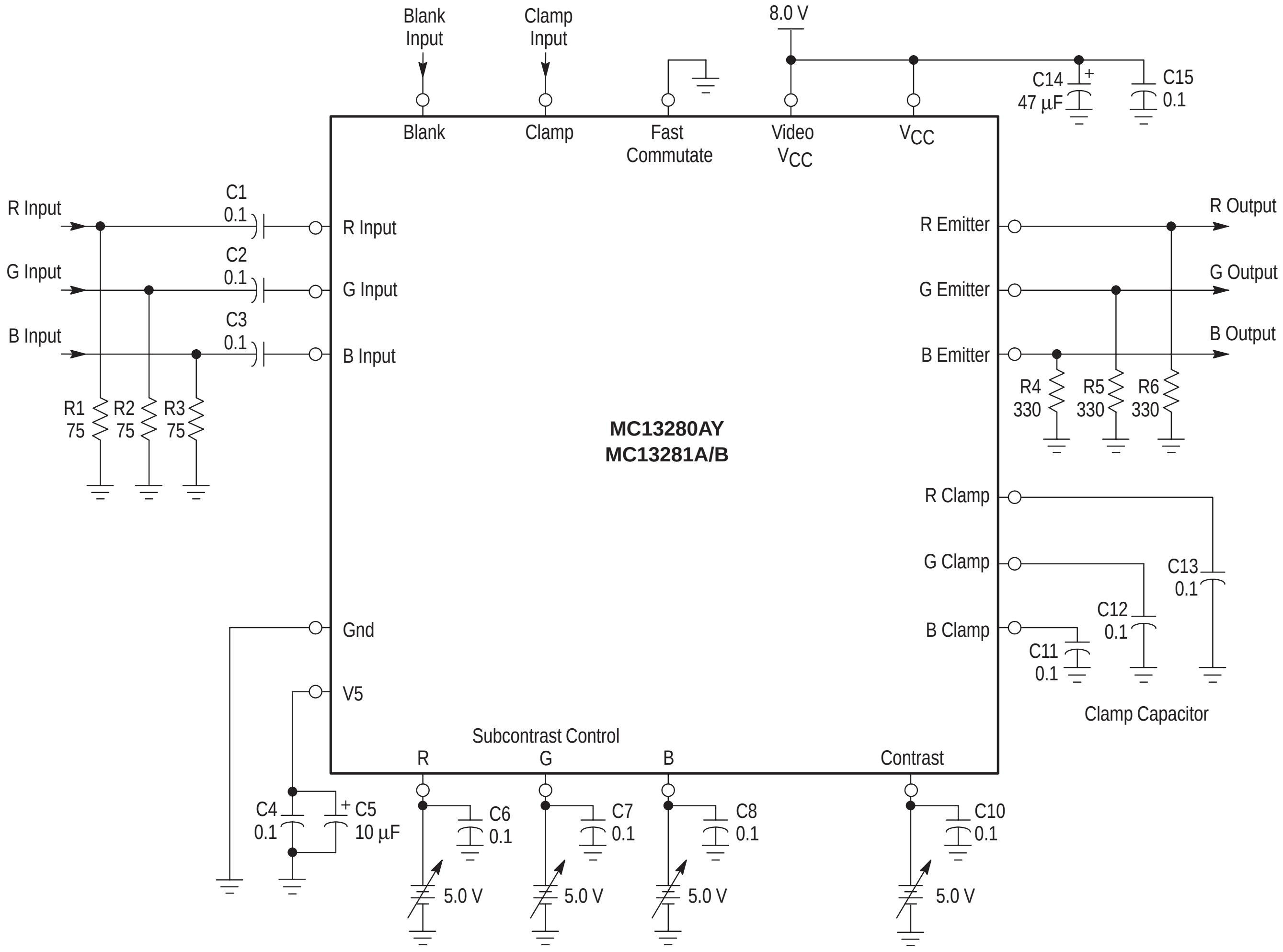
Fast Commutate

This pin should be connected to ground.

Power Supplies

V_{CC} and Video V_{CC} supplies are to be 8.0 V ±5%.

Figure 2. Test Circuit



APPLICATION INFORMATION

PCB Layout

Care should be taken in the PCB layout to minimize the noise effects. The most sensitive pins are V_{CC}, Video V_{CC}, V5 and Clamp. It is strongly recommended to make a ground plane and connect V_{CC}/Video V_{CC} and ground traces, to the power supply directly. Separate power supply traces should be used for V_{CC} and Video V_{CC} and decoupling capacitors should be connected as close as possible to the device. Multi–layer ceramic and tantalum capacitors are recommended. V5 is designed as a 5.0 V voltage reference for contrast, and RGB subcontrast controls, so the same precautions for V_{CC} should also be applied at this pin. The Clamp capacitors should be connected to ground close to IC's ground pin, or power supply ground. The copper trace of video signal inputs and outputs should be as short as possible and separated by ground traces to avoid any RGB cross–interference. A double sided PCB should be used to optimize the device's performance.

RGB Input and Output

The RGB output stages are designed as emitter–followers to drive the CRT driver circuitry directly. The emitter resistors used are 330 Ω (typically) and the driving current is 15 mA maximum for each channel. The loading impedance connected to the output stages should be greater than 330 Ω and less than 5.0 pF for optimum performance (e.g., rise/fall time, bandwidth, etc.). Decreasing the resistive load will reduce the rise/fall time by increasing the driving current, but the output stage may be damaged due to increasing power dissipation at the same time. The frequency response is affected by the loading capacitance. The typical value is 3.0 to 5.0 pF. Figure 3 shows a typical interface with a video output driver. For high resolution color monitor application, it is recommended to use coaxial cable or shielded cable for input signal connections.

Clamp and Blank Input

The clamp input is normally (except for Sync–on–Green) connected to a positive horizontal sync pulse and has a threshold level of 3.75 V. It is used as a timing reference for the dc restoration process, so it cannot be an open circuit. If Sync–on–Green timing mode is used, the clamping pulse should be located at the horizontal back porch period instead of horizontal sync. Otherwise, the black level will be clamped at the wrong dc level.

The blank input is used as a video mute, or horizontal blanking control pin, and is normally connected to a blanking pulse generated from the flyback or MCU. The threshold level is 1.25 V. The blanking pulse width should be equal to the flyback retrace period to make sure that the video signal is blanked properly during retrace. It is necessary to limit the amplitude and avoid any negative undershoot if the flyback pulse is used. The blanking input pin cannot accept a negative voltage. This pin should be grounded if it is not used.

Figure 3. Interfacing with Video Output Drivers

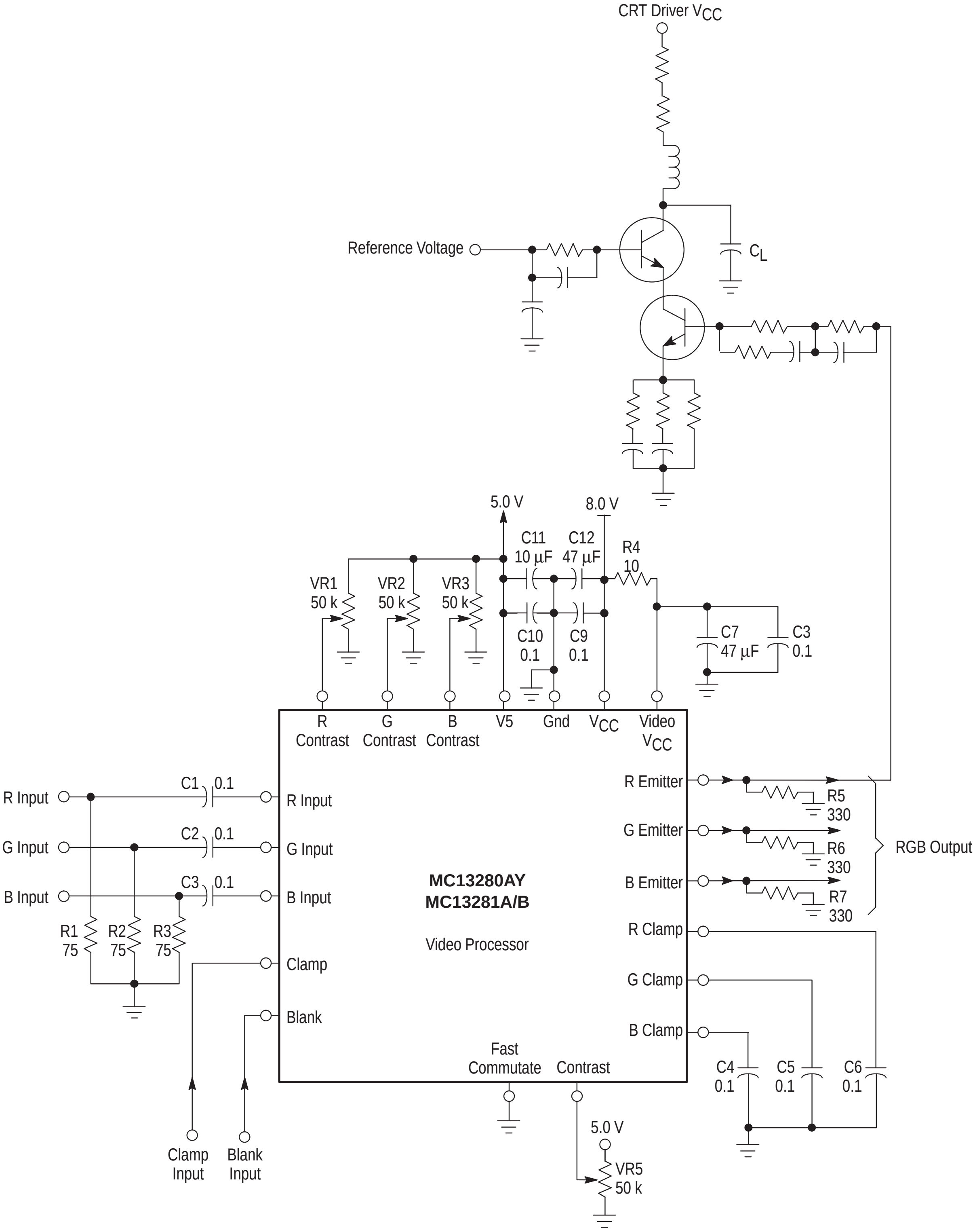


Figure 4. RGB In/Out Linearity

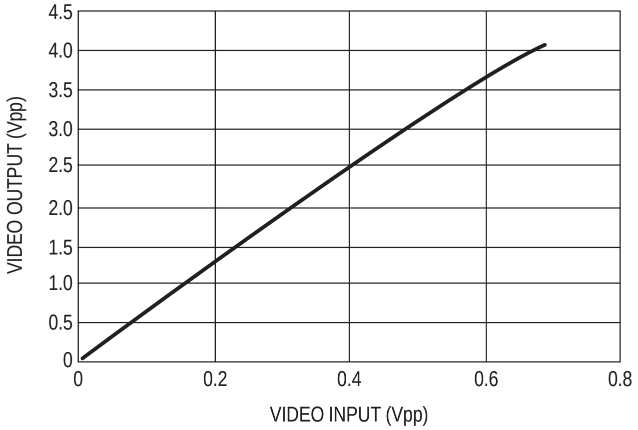


Figure 5. Contrast Control

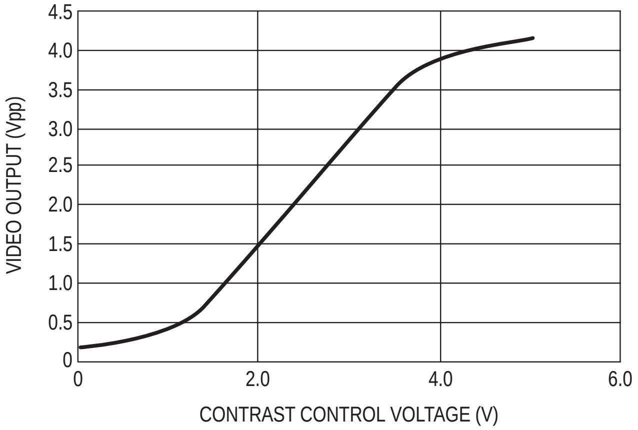


Figure 6. Subcontrast Control

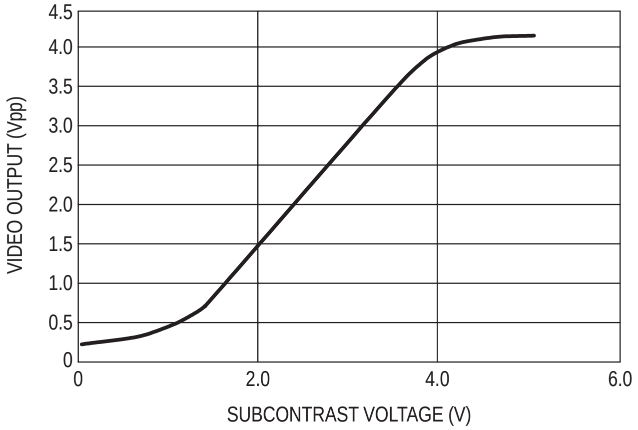


Figure 7. Crosstalk From Green to Red and Blue Channels

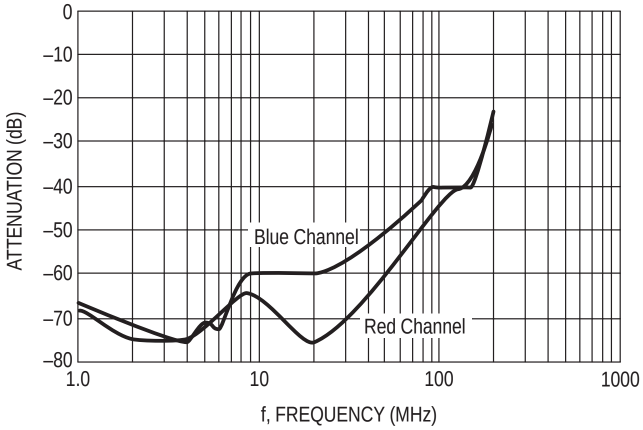
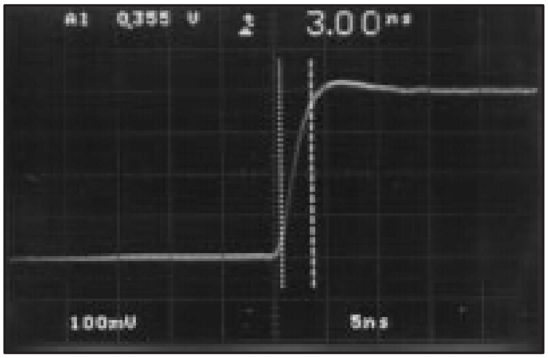
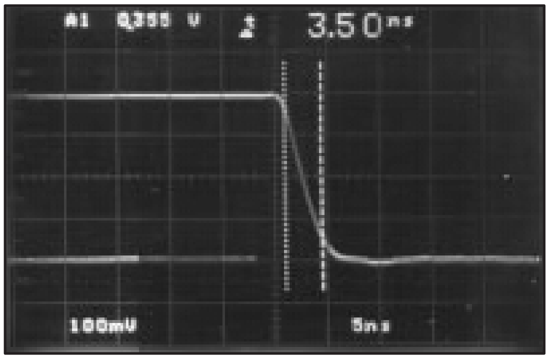


Figure 8. Rise Time for MC13281B



100 mV/DIV
5.0 ns/DIV
10x PROBE

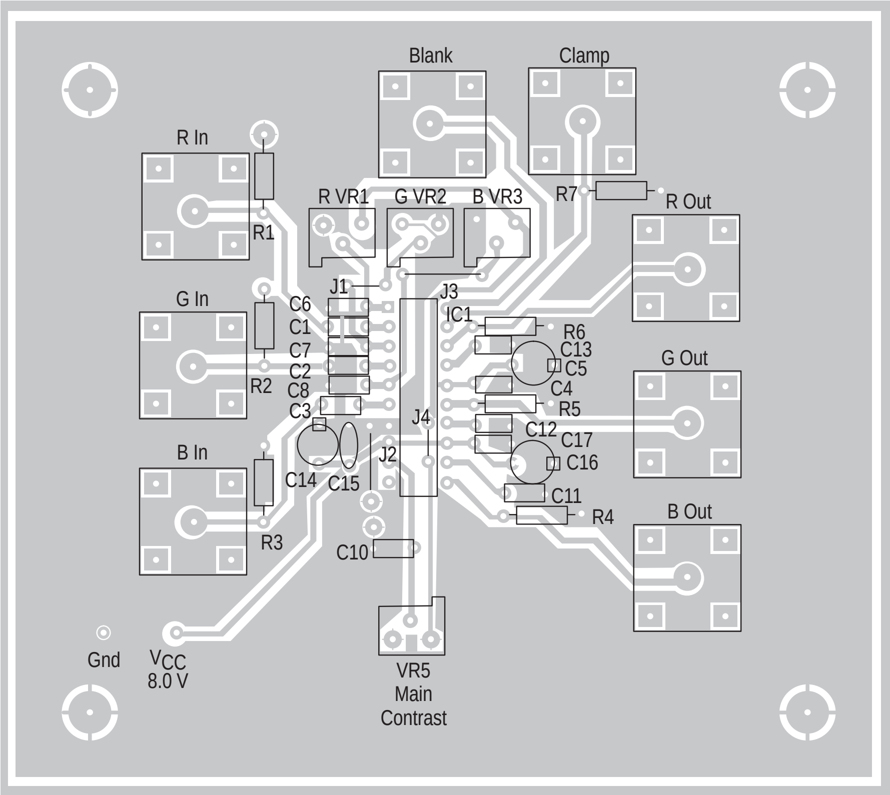
Figure 9. Fall Time for MC13281B



100 mV/DIV
5.0 ns/DIV
10x PROBE

NOTE: Recommend to use a double sided PCB without any socket for rise/fall time measurements, using an input pulse with 1.5 ns rise/fall time and an active probe with 1.7 pF capacitance loading.

Figure 10. Single Sided PCB Layout (Component Side) for MC13280AY, MC13281B



NOTE: J = Jumper

MOTOROLA

MC13282A

Advance Information

100 MHz Video Processor with OSD Interface

The MC13282A is a three channel wideband amplifier designed for use as a video pre–amp in high resolution RGB color monitors.

Features:

- 4.0 Vpp Output with 100 MHz Bandwidth
- 3.5 ns Rise/Fall Time
- Subcontrast Control for Each Channel
- Blanking and Clamping Inputs
- Contrast Control
- OSD Interface with 50 MHz Bandwidth
- OSD Contrast Control
- Package: NDIP–24

ABSOLUTE MAXIMUM RATINGS

Rating	Pin	Value	Unit
Power Supply Voltage – V_{CC}	9	–0.5, 10	Vdc
Power Supply Voltage – Video V_{CC}	17	–0.5, 10	Vdc
Voltage at Video Amplifier Inputs	2, 4, 6, 8, 10, 12	–0.5, +5.0	Vdc
Collector–Emitter Current (Three Channels)	17	120	mA
Storage Temperature	–	–65 to +150	°C
Junction Temperature	–	150	°C

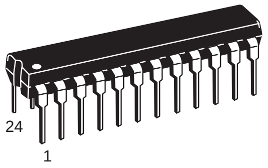
NOTES: 1. Devices should not be operated at these limits. Refer to “Recommended Operating Conditions” section for actual device operation.
2. ESD data available upon request.

RECOMMENDED OPERATING CONDITIONS

Characteristic	Pin	Min	Typ	Max	Unit
Power Supply Voltage	9, 17	7.6	8.0	8.4	Vdc
Contrast Control	13	0	–	5.0	Vdc
Subcontrast Control	1, 3, 5	0	–	5.0	Vdc
Blanking Input Signal Amplitude	24	0	–	5.0	V
Clamping Input Signal Amplitude	23	0	–	5.0	V
Video Signal Amplitude (with 75 Ω Termination)	2, 4, 6	–	0.7	1.0	Vpp
OSD Signal Input	8, 10, 12	–	TTL	–	V
Collector–Emitter Current (Total for Three Channels)	17	0	–	50	mA
Clamping Pulse Width	23	500	–	–	ns
Operating Ambient Temperature	–	0	–	70	°C

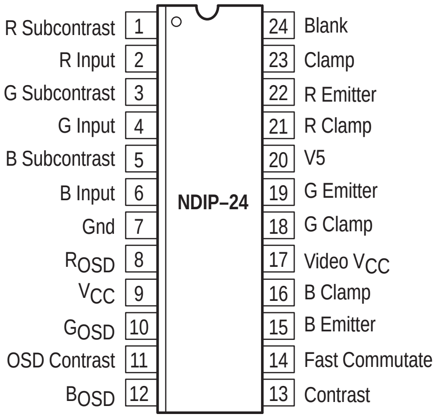
100 MHz VIDEO PROCESSOR WITH OSD INTERFACE

SEMICONDUCTOR TECHNICAL DATA



P SUFFIX
PLASTIC PACKAGE
CASE 724

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

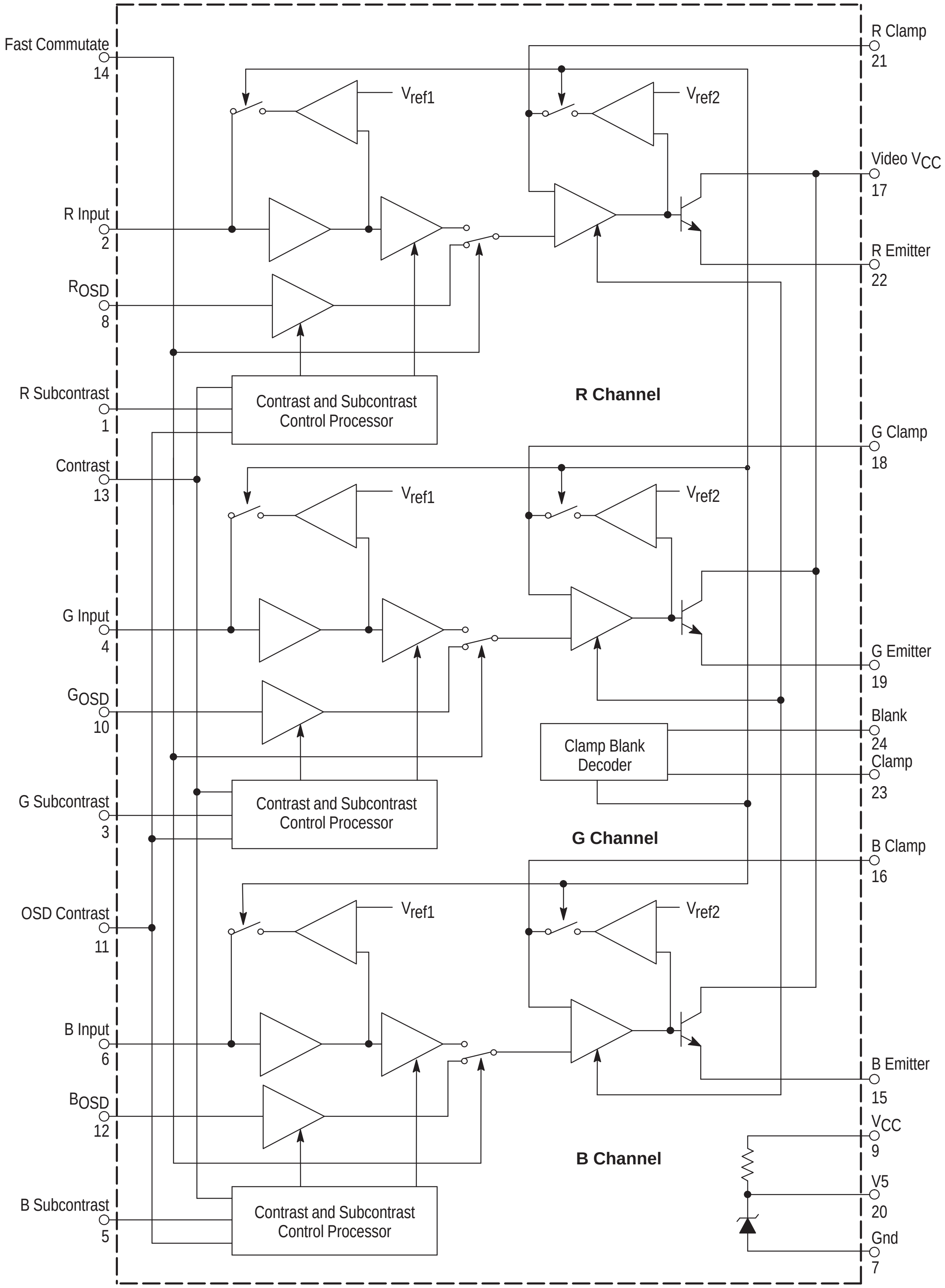
Device	Operating Temperature Range	Package
MC13282AP	T_A = 0° to +70°C	Plastic DIP

ELECTRICAL CHARACTERISTICS (Refer to Test Circuit Figure 1, T_A = 25°C, V_{CC} = 8.0 Vdc.)

Characteristic	Condition	Pin	Min	Typ	Max	Unit
Input Impedance	–	2, 4, 6	100	–	–	kΩ
Internal DC Bias Voltage			–	2.4	–	Vdc
Output Signal Amplitude	V2, V4, V6 = 0.7 Vpp V1, V3, V5, V13 = 5.0 V V14 = 0 V	15, 19, 22	3.6	4.0	–	Vpp
Voltage Gain			–	5.6	–	V/V
Contrast Control	V13 = 5.0 to 0 V V1, V3, V5 = 5.0 V	13	–	–26	–	dB
Subcontrast Control	V1, V3, V5 = 5.0 to 0 V V13 = 5.0 V	1, 3, 5	–	–26	–	dB
Emitter DC Level	–	15, 19, 22	1.0	1.2	1.4	Vdc
Blanking Input Threshold	–	24	–	1.25	–	V
Clamping Input Threshold	–	23	–	3.75	–	V
Video Rise Time	V2, V4, V6 = 0.7 Vpp V_{out} = 4.0 Vpp R_L > 300 Ω, C_L < 5.0 pF	15, 19, 22	–	3.5	–	ns
Video Fall Time			–	3.5	–	
Video Bandwidth	V2, V4, V6 = 0.7 Vpp V1, V3, V5, V13 = 5.0 V V14 = 0 V R_L > 300 Ω, C_L < 5.0 pF	15, 19, 22	–	100	–	MHz
OSD Rise Time	V8, V10, V12 = TTL Level V11 = 5.0 V, V14 = 5.0 V	15, 19, 22	–	7.0	–	ns
OSD Fall Time			–	7.0	–	
OSD Bandwidth	V8, V10, V12 = TTL Level V11 = 5.0 V, V14 = 5.0 V	15, 19, 22	–	50	–	MHz
OSD Propagation Delay	–	–	–	17	–	ns
Power Supply Current	V_{CC}, Video V_{CC} = 8.0 V	9, 17	–	70	–	mA

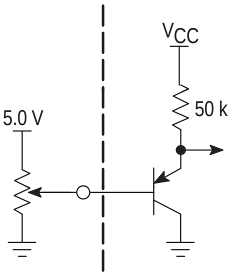
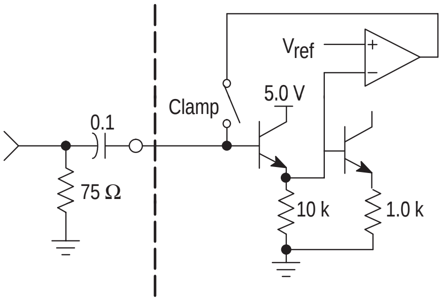
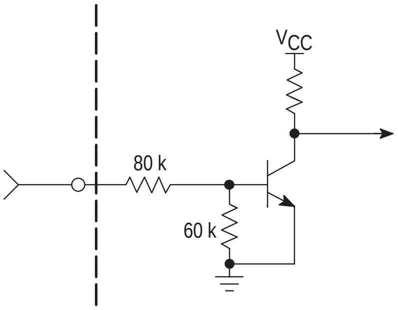
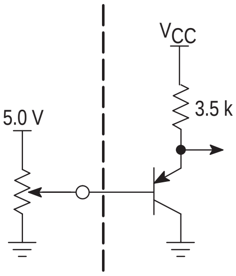
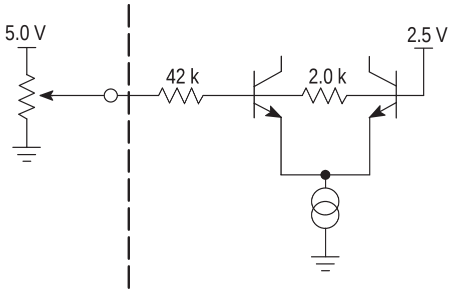
NOTE: It is recommended to use a double sided PCB layout for high frequency measurement (e.g., rise/fall time, bandwidth).

Figure 1. Internal Block Diagram

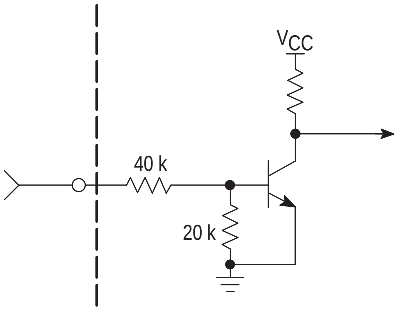
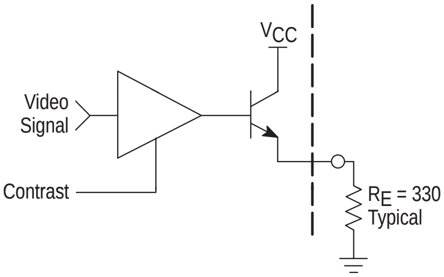
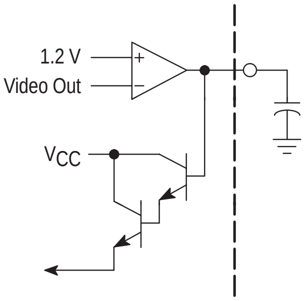
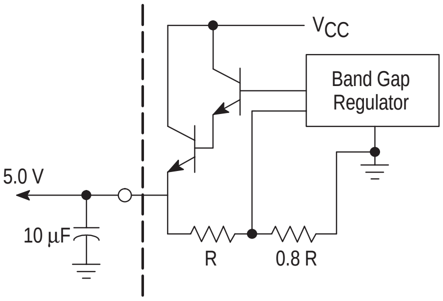


This device contains 272 active transistors.

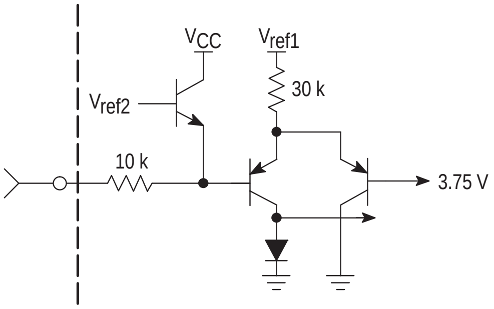
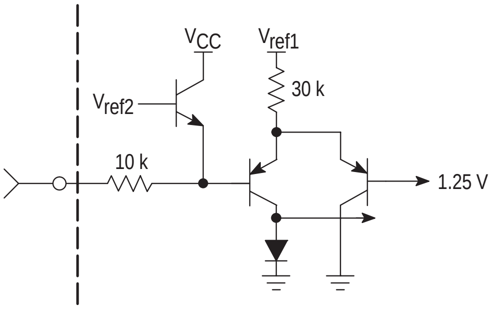
PIN FUNCTION DESCRIPTION

Pin	Name	Equivalent Internal Circuit	Description
1 3 5	R Subcontrast Control G Subcontrast Control B Subcontrast Control		These pin provides a maximum of 26 dB attenuation to vary the gain of each video amplifier separately. Input voltage is from 0 to 5.0 V. Increasing the voltage will increase the contrast level.
2 4 6	R Input G Input B Input		The input coupling capacitor is used for input clamping storage. The maximum source impedance is 100 Ω. Input polarity of the video signal is positive. Nominal 0.7 Vpp input signal is recommended (maximum 1.0 Vpp).
7	Ground		Ground pin. Connect to a clean, solid ground.
8 10 12	R_{OSD} Input G_{OSD} Input B_{OSD} Input		These inputs are standard TTL level.
9	V_{CC}		Connect to 8.0 Vdc supply, ±5%. Decoupling is required at this pin.
11	OSD Contrast		On Screen Display contrast control. Input voltage is from 0 to 5.0 V. Increasing the voltage will increase the contrast of the OSD signal.
13	Contrast		Overall Contrast Control for the three channels. The input range is 0 V to 5.0 V. An increase of voltage increases the contrast.

PIN FUNCTION DESCRIPTION (continued)

Pin	Name	Equivalent Internal Circuit	Description
14	Fast Commutate		This pin is used in conjunction with the RGB OSD inputs. It is a high speed switch used for overlaying text on picture. A logic low selects Pins 2, 4, 6. A logic high selects Pins 8, 10, 12.
15 19 22	B Emitter Output G Emitter Output R Emitter Output		The video outputs are configured as emitter–followers with a driving capability of about 15 mA each. The dc voltage at these three emitters is set to 1.2 V (black level). The dc current through the output stage is determined by the emitter resistors (typically 330 Ω).
16 18 21	B Clamp Capacitor G Clamp Capacitor R Clamp Capacitor		A 100 nF capacitor is connected to each of these pins. The capacitor is used for video output dc restoration.
17	Video V_{CC}		Connect to 8.0 V dc supply, ±5%. This V_{CC} is for the video output stage. It is internally connected to the collectors of the output transistors.
20	5.0 V_{ref} (V5)		5.0 V regulator. Minimum 10 µF capacitor is required for noise filtering and compensation. It can source up to 20 mA but not sink current. Output impedance is ≈ 10 Ω. Recommended for use as a voltage reference only.

PIN FUNCTION DESCRIPTION (continued)

Pin	Name	Equivalent Internal Circuit	Description
23	Clamp		This pin is used for video clamping. The threshold clamping level is 3.75 V.
24	Blank		This pin is used for video blanking. The threshold blanking level is 1.25 V.

FUNCTIONAL DESCRIPTION

The MC13282A is composed of three video amplifiers, clamping and blanking circuitry with contrast and subcontrast controls and OSD interface. Each video amplifier is designed to have a –3.0 dB bandwidth of 100 MHz with a gain of up to about 5.6 V/V, or 15 dB.

Video Input

The video input stages are high impedance and designed to accept a maximum signal of 1.0 Vpp with 75 Ω termination (typically) provided externally. During the clamping period, a current is provided to the input capacitor by the clamping circuit which brings the input to a proper dc level (nominal 2.0 V). The blanking and clamping signals are to be provided externally, with their thresholds sitting at 1.25 V and 3.75 V, respectively.

Video Output

The video output stages are configured as emitter–followers, with a driving capability of about 15 mA for each channel. The dc voltage at these three emitters is set to 1.2 V (black level). The dc current through each output stage is determined by the emitter resistor (typically 330 Ω).

Contrast Control

The contrast control varies the gain of three video amplifiers from a minimum of 0.3 V/V to a maximum of 5.6 V/V when all subcontrast levels are set to 5.0 V.

Subcontrast Control

Each subcontrast control provides a maximum of 26 dB attenuation on each video amplifier separately.

OSD Interface

The three OSD inputs are TTL compatible and have a typical bandwidth of 50 MHz. A fast commutate pin is provided to select either the video or the OSD inputs as the source for the outputs. OSD contrast control is also provided to set the amount of gain required when OSD inputs are selected.

Clamp Pulse Input

The clamping pulse is provided externally, and the pulse width must be no less than 500 ns.

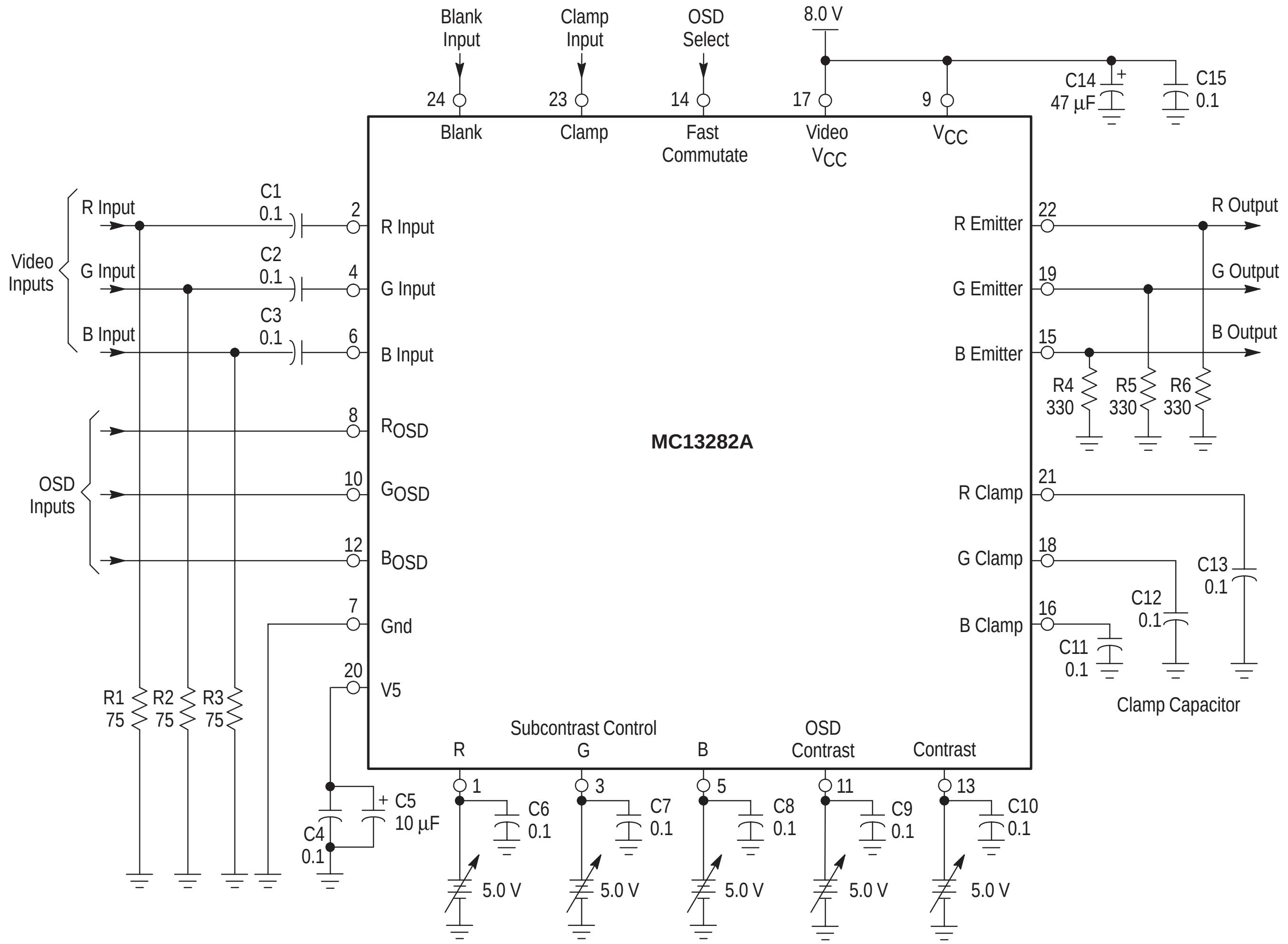
Blank Pulse Input

The blanking pulse is used to blank the video signal during the horizontal sync period, or used as a control pin for video mute function.

Power Supplies

V_{CC} and Video V_{CC} supplies are to be 8.0 V ±5%.

Figure 2. Test Circuit



APPLICATION INFORMATION

PCB Layout

Care should be taken in the PCB layout to minimize the noise effects. The most sensitive pins are V_{CC} (9), Video V_{CC} (17), V5 (20), Clamp (16, 18, 21). It is strongly recommended to make a ground plane and connect V_{CC}/Video V_{CC} and ground traces to the power supply directly. Separate power supply traces, should be used for V_{CC} and Video V_{CC} and decoupling capacitors should be connected as close as possible to the device. Multi–layer ceramic and tantalum capacitors are recommended. Pin 20 (V5) is designed as a 5.0 V voltage reference for contrast, RGB subcontrast and OSD contrast controls, so the same precaution for V_{CC} should be also applied at this pin. The Clamp capacitors at Pins 16,18 and 21 should be connected to ground close to IC's ground Pin 7 or power supply ground. The copper trace of the video signal inputs and outputs should be as short as possible and separated by ground traces to avoid any RGB cross–interference. A double sided PCB should be used to optimize the device's performance.

RGB Input and Output

The RGB output stages are designed as emitter–followers to drive the CRT driver circuitry directly. The emitter resistors used is 330 Ω (typically) and the driving current is 15 mA maximum for each channel. The loading impedance connected to the output stages should be greater than 330 Ω and less than 5.0 pF for optimum performance (e.g., rise/fall time, bandwidth, etc.). Decreasing the resistive load will reduce the rise/fall time by increasing the driving current, but the output stage may be damaged due to increasing power dissipation at the same time. The frequency response is affected by the loading capacitance. The typical value is 3.0 to 5.0 pF. Figure 4 shows a typical interface with a video output driver. For a high resolution color monitor application, it is recommended to use coaxial cable or shielded cable for input signal connections.

Clamp and Blank Input

The clamp input is normally (except for Sync–on–Green) connected to a positive horizontal sync pulse, and has a threshold level of 3.75 V. It is used as a timing reference for the dc restoration process, so it cannot be left open. If Sync–on–Green timing mode is used, the clamping pulse should be located at horizontal back porch period instead of horizontal sync tip. Otherwise, the black level will be clamped at an incorrect voltage.

The blank input is used as a video mute, or horizontal blanking control, and is normally connected to a blanking pulse generated from the flyback or from an MCU. The threshold level of 1.25 V. The blanking pulse width should be equal to the flyback retrace period to make sure that the video signal is blanked properly during retrace. It is necessary to limit the amplitude, and avoid any negative undershoots if the flyback pulse is used. This Blanking input pin cannot accept a negative voltage. This pin should be grounded if it is not used.

OSD interface

Figure 3 show a typical application with an OSD device (MC141540). The MC141540 OSD and FC outputs are TTL compatible, and therefore interface directly with MC13282A. Level shifting circuitry is not needed. The MC141540 is a digital device, controlled by an MCU. Therefore, separate power supply runs to the MC141540 and to the MC13282A are recommended. Care should be taken in the PC board layout to prevent digital noise from entering the analog portions of MC13282A.

Normally the OSD switching is done during the active video time. It is recommended that the Fast Commutate pin not be activated during the horizontal sync time.

Figure 3. Interfacing with OSD Device

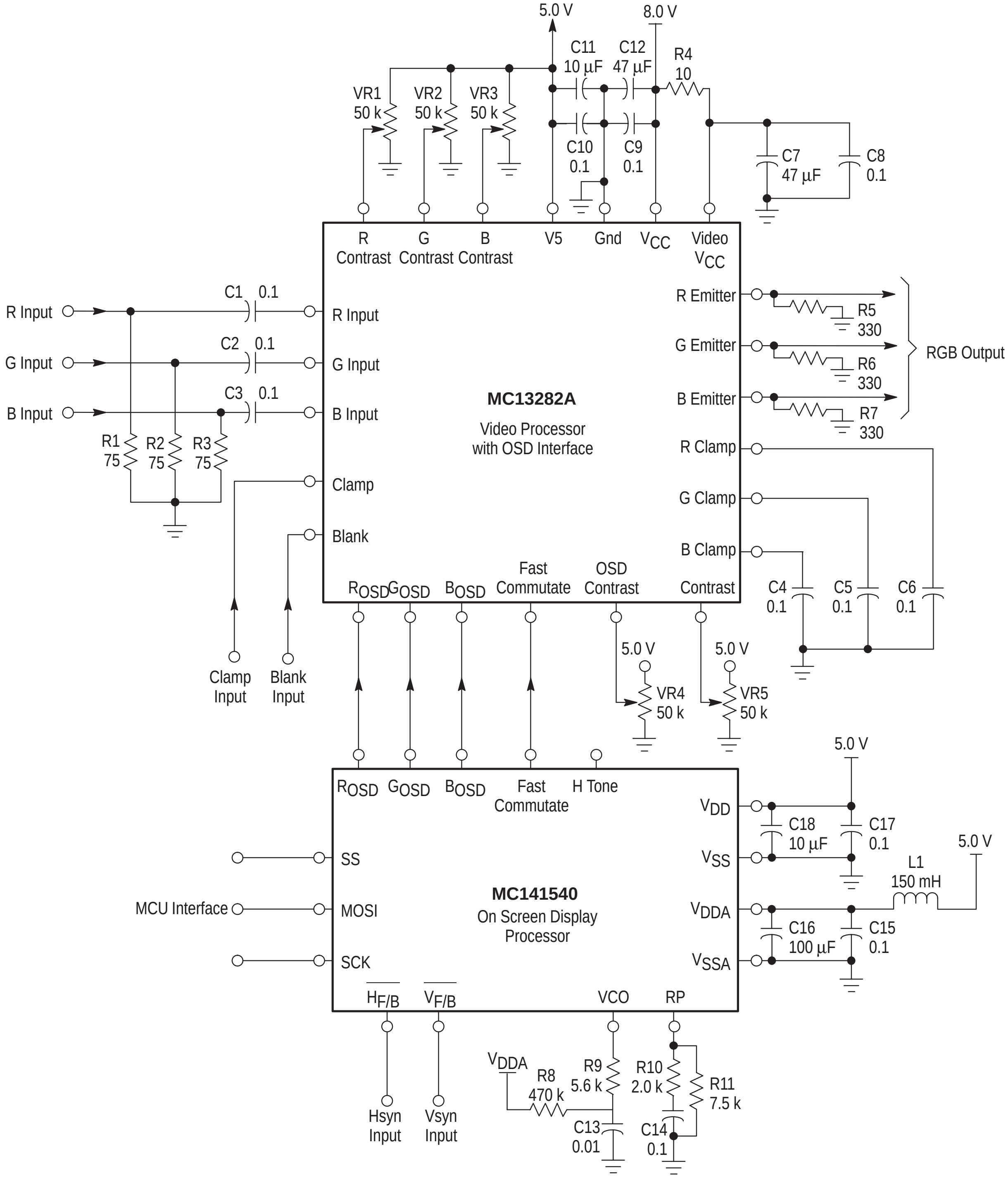


Figure 4. Interfacing with Video Output Drivers

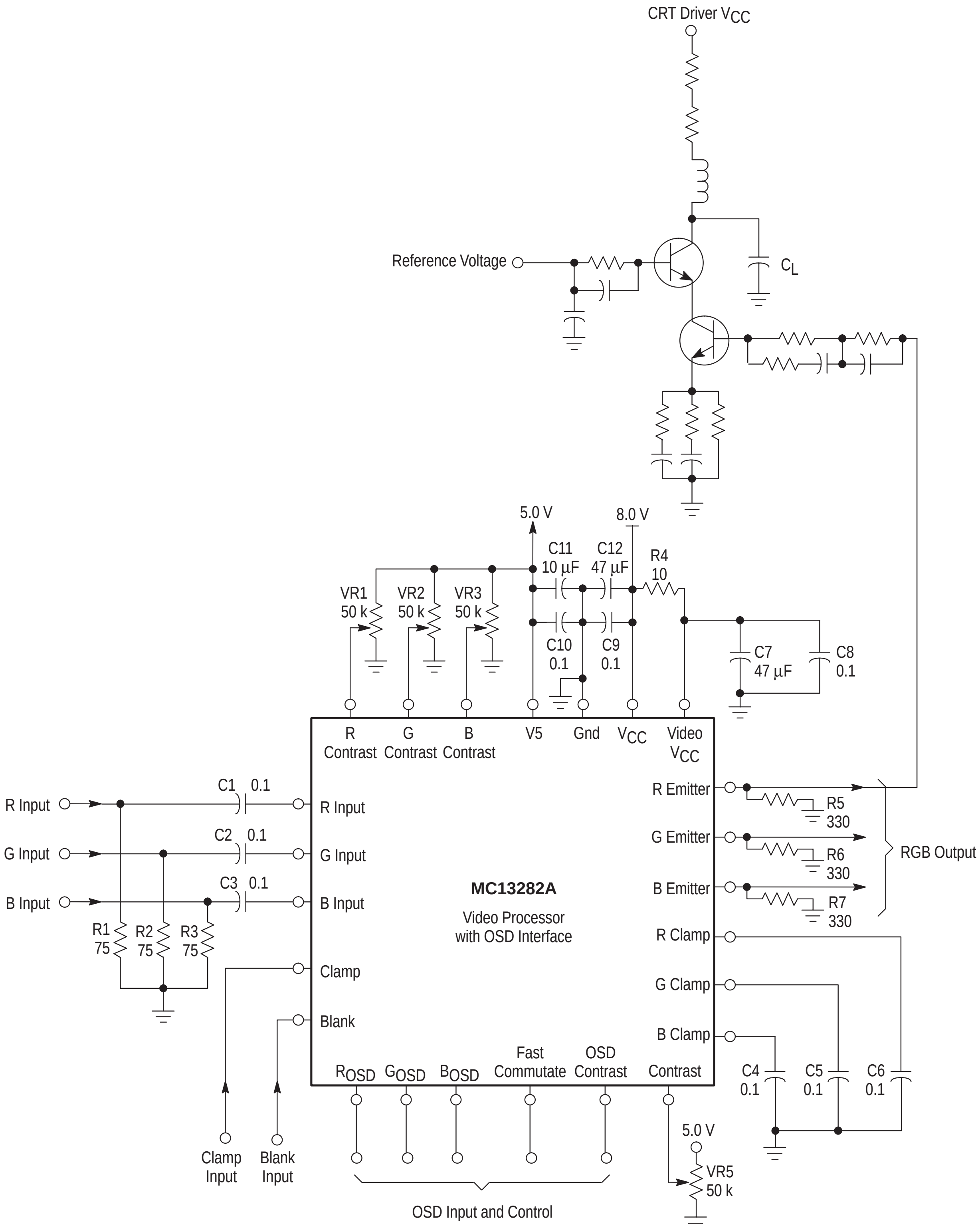


Figure 5. RGB In/Out Linearity

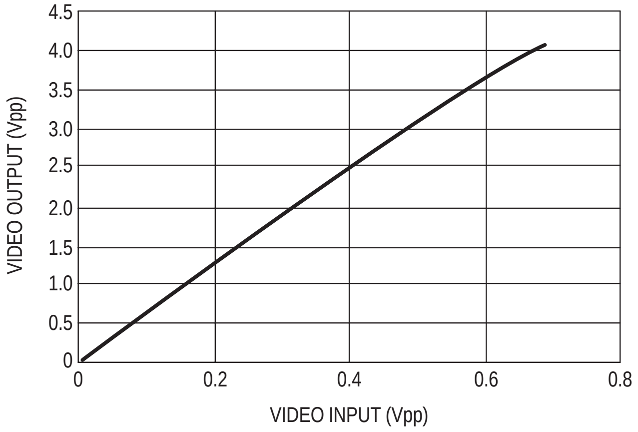


Figure 6. Color Contrast

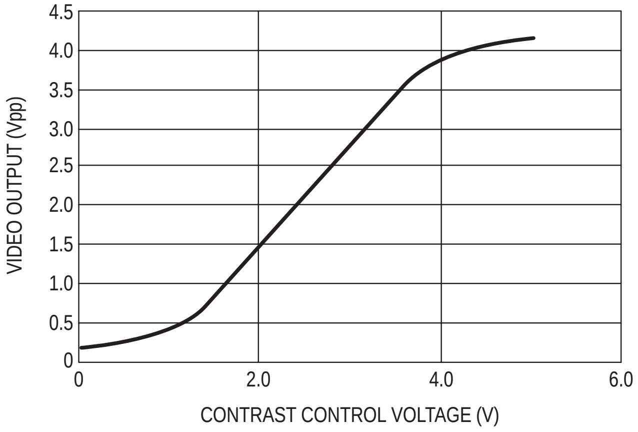


Figure 7. Subcontrast Control

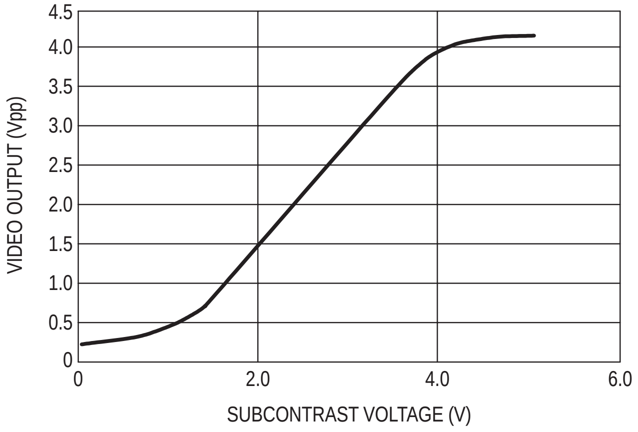


Figure 8. OSD Contrast Control

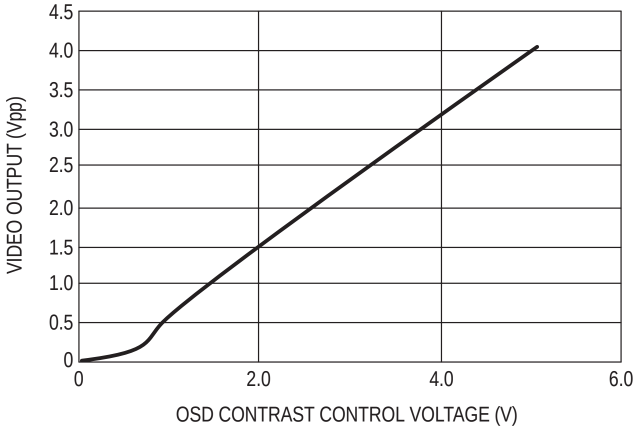


Figure 9. Crosstalk From Green to Red and Blue Channels

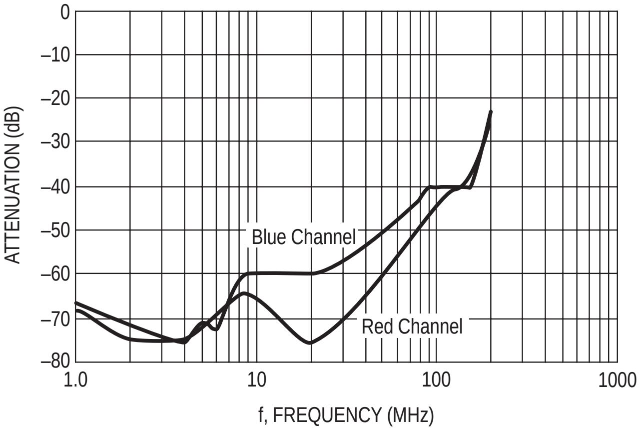
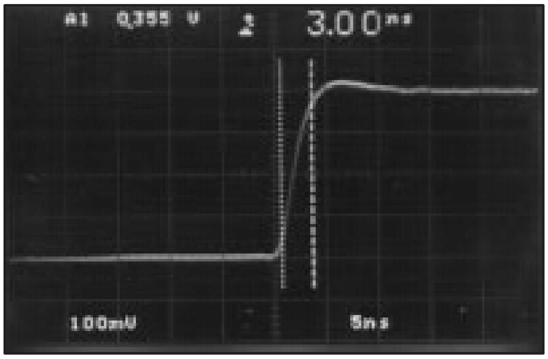
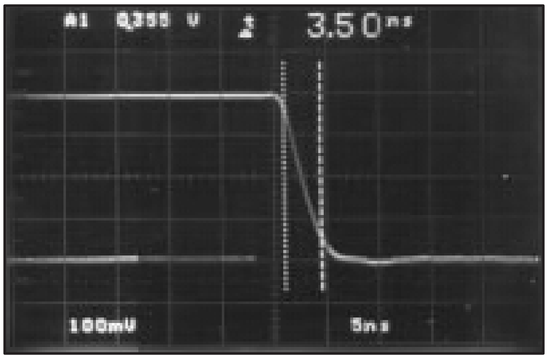


Figure 10. Rise Time



100 mV/DIV
5.0 ns/DIV
10x PROBE

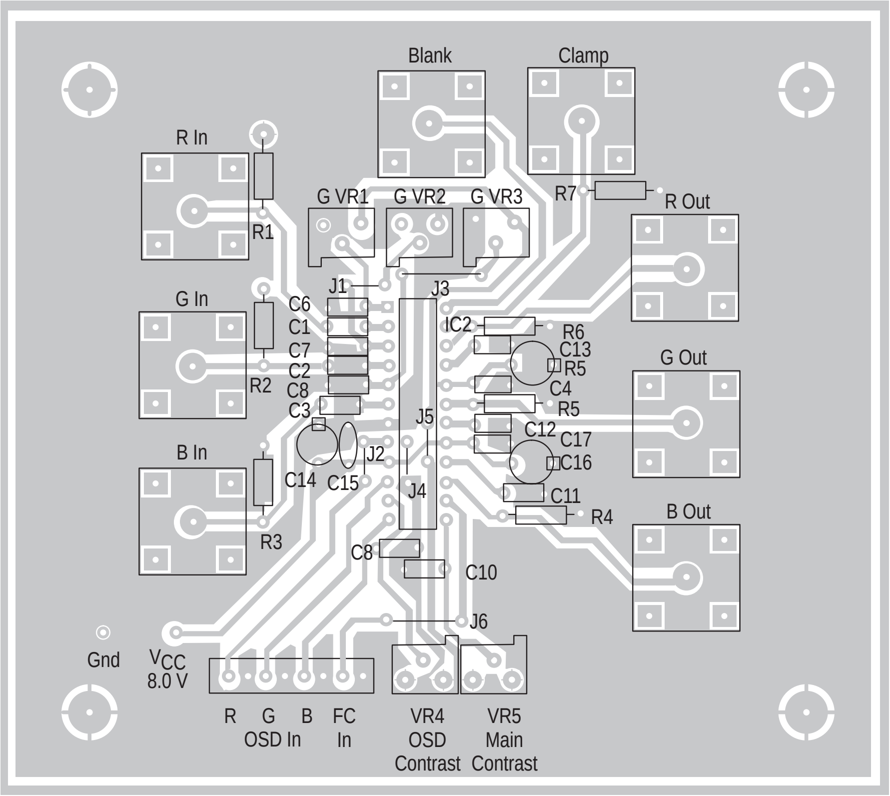
Figure 11. Fall Time



100 mV/DIV
5.0 ns/DIV
10x PROBE

NOTE: Recommended to use a double sided PCB without any socket for rise/fall time measurements, using an input pulse with 1.5 ns rise/fall time and an active probe with 1.7 pF capacitance loading.

Figure 12. Single Sided PCB Layout (Component Side)



NOTE: J = Jumper

MOTOROLA

MC13283

Product Preview

130 MHz Video Processor with OSD Interface

The MC13283 is a three channel wideband amplifier designed for use as a video pre–amp in high resolution RGB color monitors.

Features:

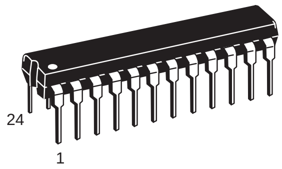
- 4.0 Vpp Output with 130 MHz Bandwidth
- 2.6 ns Rise and 3.2 ns Fall Time
- Subcontrast Control for Each Channel
- Blanking and Clamping Inputs
- Contrast Control
- OSD Interface with 85 MHz Bandwidth
- OSD Contrast Control
- Package: NDIP–24

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC13283P	T_A = 0° to +70°C	Plastic DIP

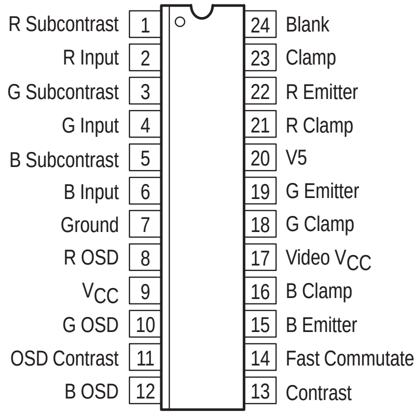
130 MHz VIDEO PROCESSOR WITH OSD INTERFACE

SEMICONDUCTOR TECHNICAL DATA



P SUFFIX
PLASTIC PACKAGE
CASE 724
(NDIP–24)

PIN CONNECTIONS



(Top View)

MOTOROLA

MC34119

Low Power Audio Amplifier

The MC34119 is a low power audio amplifier intergrated circuit intended (primarily) for telephone applications, such as in speakerphones. It provides differential speaker outputs to maximize output swing at low supply voltages (2.0 V minimum). Coupling capacitors to the speaker are not required. Open loop gain is 80 dB, and the closed loop gain is set with two external resistors. A Chip Disable pin permits powering down and/or muting the input signal. The MC34119 is available in standard 8–pin DIP, SOIC package, and TSSOP package.

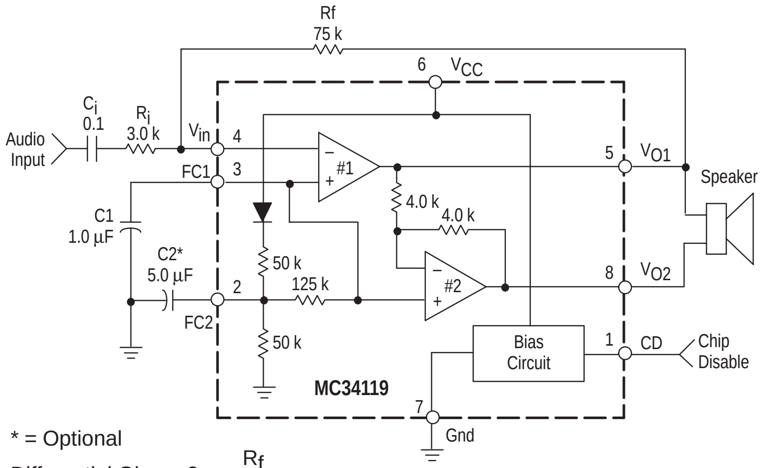
- Wide Operating Supply Voltage Range (2.0 V to 16 V), Allows Telephone Line Powered Applications
- Low Quiescent Supply Current (2.7 mA Typ) for Battery Powered Applications
- Chip Disable Input to Power Down the IC
- Low Power–Down Quiescent Current (65 µA Typ)
- Drives a Wide Range of Speaker Loads (8.0 Ω and Up)
- Output Power Exceeds 250 mW with 32 Ω Speaker
- Low Total Harmonic Distortion (0.5% Typ)
- Gain Adjustable from <0 dB to >46 dB for Voice Band
- Requires Few External Components

MAXIMUM RATINGS

Rating	Value	Unit
Supply Voltage	–1.0 to +18	Vdc
Maximum Output Current at V_{O1}, V_{O2}	±250	mA
Maximum Voltage @ V_{in}, FC1, FC2, CD Applied Output Voltage to V_{O1}, V_{O2} when disabled	–1.0, V_{CC} + 1.0 –1.0, V_{CC} + 1.0	Vdc
Junction Temperature	–55, +140	°C

NOTE: ESD data available upon request.

Block Diagram and Simplified Application



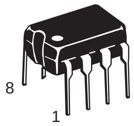
* = Optional

Differential Gian = $2 \times \frac{R_f}{R_i}$

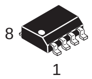
This device contains 45 active transistors.

LOW POWER AUDIO AMPLIFIER

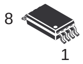
SEMICONDUCTOR TECHNICAL DATA



P SUFFIX
PLASTIC PACKAGE
CASE 626

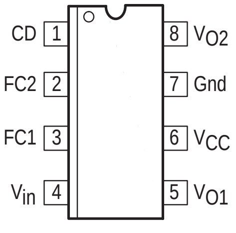


D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)



DTB SUFFIX
PLASTIC PACKAGE
CASE 948J
(TSSOP)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC34119P	T_A = –20° to +70°C	Plastic DIP
MC34119D		SO–8
MC34119DTB		TSSOP

RECOMMENDED OPERATING CONDITIONS

Characteristics	Symbol	Min	Max	Unit
Supply Voltage Voltage @ CD (Pin 1)	V_{CC} V_{CD}	+2.0 0	+16 V_{CC}	Vdc Vdc
Load Impedance	R_L	8.0	–	Ω
Peak Load Current	I_L	–	±200	mA
Differential Gain (5.0 kHz Bandwidth)	AVD	0	46	dB
Ambient Temperature	T_A	–20	+70	°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
AMPLIFIERS (AC CHARACTERISTICS)					
AC Input Resistance (@ V_{In})	r_i	–	>30	–	MΩ
Open Loop Gain (Amplifier #1, f < 100 Hz)	A_{VOL1}	80	–	–	dB
Closed Loop Gain (Amplifier #2, V_{CC} = 6.0 V, f = 1.0 kHz, R_L = 32 Ω)	A_{V2}	–0.35	0	+0.35	dB
Gain Bandwidth Product	GBW	–	1.5	–	MHz
Output Power; V_{CC} = 3.0 V, R_L = 16 Ω, THD ≤ 10% V_{CC} = 6.0 V, R_L = 32 Ω, THD ≤ 10% V_{CC} = 12 V, R_L = 100 Ω, THD ≤ 10%	 P_{Out3} P_{Out6} P_{Out12}	 55 250 400	 – – –	 – – –	mW
Total Harmonic Distortion (f = 1.0 kHz) (V_{CC} = 6.0 V, R_L = 32 Ω, P_{out} = 125 mW) (V_{CC} ≥ 3.0 V, R_L = 8.0 Ω, P_{out} = 20 mW) (V_{CC} ≥ 12 V, R_L = 32 Ω, P_{out} = 200 mW)	THD	 – – –	 0.5 0.5 0.6	 1.0 – –	%
Power Supply Rejection (V_{CC} = 6.0 V, ΔV_{CC} = 3.0 V) (C1 = ∞, C2 = 0.01 µF) (C1 = 0.1 µF, C2 = 0, f = 1.0 kHz) (C1 = 1.0 µF, C2 = 5.0 µF, f = 1.0 kHz)	PSRR	 50 – –	 – 12 52	 – – –	dB
Differential Muting (V_{CC} = 6.0 V, 1.0 kHz ≤ f ≤ 20 kHz, CD = 2.0 V)	GMT	–	>70	–	dB
AMPLIFIERS (DC CHARACTERISTICS)					
Output DC Level @ V_{O1}, V_{O2}, V_{CC} = 3.0 V, R_L = 16 (R_f = 75 k) V_{CC} = 6.0 V V_{CC} = 12 V	$V_{O(3)}$ $V_{O(6)}$ $V_{O(12)}$	1.0 – –	1.15 2.65 5.65	1.25 – –	Vdc
Output Level High (I_{out} = –75 mA, 2.0 V ≤ V_{CC} ≤ 16 V) Low (I_{out} = 75 mA, 2.0 V ≤ V_{CC} ≤ 16 V)	 V_{OH} V_{OL}	 – –	 V_{CC} – 1.0 0.16	 – –	Vdc
Output DC Offset Voltage (V_{O1}–V_{O2}) (V_{CC} = 6.0 V, R_f = 75 kΩ, R_L = 32 Ω)	ΔV_O	 –30	 0	 +30	mV
Input Bias Current @ V_{in} (V_{CC} = 6.0 V)	I_{IB}	–	–100	–200	nA
Equivalent Resistance @ FC1 (V_{CC} = 6.0 V) @ FC2 (V_{CC} = 6.0 V)	 R_{FC1} R_{FC2}	 100 18	 150 25	 220 40	kΩ
CHIP DISABLE (Pin 1)					
Input Voltage Low High	 V_{IL} V_{IH}	 – 2.0	 – –	 0.8 –	Vdc
Input Resistance (V_{CC} = V_{CD} = 16 V)	R_{CD}	50	90	175	kΩ
POWER SUPPLY					
Power Supply Current (V_{CC} = 3.0 V, R_L = ∞, CD = 0.8 V) (V_{CC}= 16 V, R_L = ∞, CD = 0.8 V) (V_{CC} = 3.0 V, R_L = ∞, CD = 2.0 V)	 I_{CC3} I_{CC16} I_{CCD}	 – – –	 2.7 3.3 65	 4.0 5.0 100	 mA mA µA

NOTE: Currents into a pin are positive, currents out of a pin are negative.

PIN FUNCTION DESCRIPTION

Symbol	Pin	Description
CD	1	Chip Disable – Digital input. A Logic “0” (<0.8 V) sets normal operation. A logic “1” (≥2.0 V) sets the power down mode. Input impedance is nominally 90 kΩ .
FC2	2	A capacitor at this pin increases power supply rejection, and affects turn–on time. This pin can be left open if the capacitor at FC1 is sufficient.
FC1	3	Analog ground for the amplifiers. A 1.0 µF capacitor at this pin (with a 5.0 µF capacitor at Pin 2) provides (typically) 52 dB of power supply rejection. Turn–on time of the circuit is affected by the capacitor on this pin. This pin can be used as an alternate input.
V_{in}	4	Amplifier input. The input capacitor and resistor set low frequency rolloff and input impedance. The feedback resistor is connected to this pin and V_{O1}.
V_{O1}	5	Amplifier Output #1. The dc level is ≈ (V_{CC} – 0.7 V)/2.
V_{CC}	6	DC supply voltage (+2.0 V to +16 V) is applied to this pin.
GND	7	Ground pin for the entire circuit.
V_{O2}	8	Amplifier Output #2. This signal is equal in amplitude, but 180° out–of–phase with that at V_{O1}. The dc level is ≈ (V_{CC} – 0.7 V)/2.

TYPICAL TEMPERATURE PERFORMANCE (–20° C < T_A < +70°C)

Function	Typical Change	Units
Input Bias Current (@ V_{in})	±40	pA/°C
Total Harmonic Distortion (V_{CC} = 6.0 V, R_L = 32 Ω. P_{out} = 125 mW, f = 1.0 kHz)	+0.003	%/°C
Power Supply Current		µA/°C
(V_{CC} = 3.0 V, R_L = ∞, CD = 0 V)	–2.5	
(V_{CC} = 3.0 V, R_L = ∞, CD = 2.0 V)	–0.03	

DESIGN GUIDELINES

General

The MC34119 is a low power audio amplifier capable of low voltage operation (V_{CC} = 2.0 V minimum) such as that encountered in line–powered speakerphones. The circuit provides a differential output ($V_{O1}–V_{O2}$) to the speaker to maximize the available voltage swing at low voltages. The differential gain is set by two external resistors. Pins FC1 and FC2 allow controlling the amount of power supply and noise rejection, as well as providing alternate inputs to the amplifiers. The CD pin permits powering down the IC for muting purposes and to conserve power.

Amplifiers

Referring to the block diagram, the internal configuration consists of two identical operational amplifiers. Amplifier #1 has an open loop gain of ≥80 dB (at f ≤ 100 Hz), and the closed loop gain is set by external resistor R_f and R_i. The amplifier is unity gain stable, and has a unity gain frequency of approximately 1.5 MHz. In order to adequately cover the telephone voice band (300 Hz to 3400 Hz), a maximum closed loop gain of 46 is recommended. Amplifier #2 is internally set to a gain of – 1.0 (0 dB).

The outputs of both amplifiers are capable of sourcing and sinking a peak current of 200 mA. The outputs can typically swing to within ≈0.4 V above ground, and to within ≈1.3 V below V_{CC}, at the maximum current. See Figures 18 and 19 for V_{OH} and V_{OL} curves.

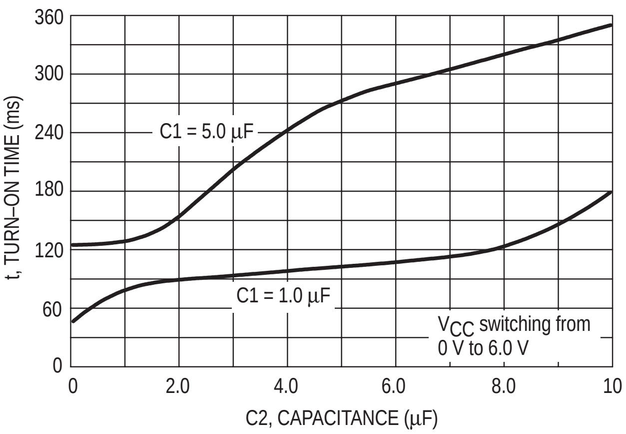
The output dc offset voltage ($V_{O1}–V_{O2}$) is primarily a function of the feedback resistor (R_f), and secondarily due to the amplifiers' input offset voltages. The input offset voltage of the two amplifiers will generally be similar for a particular IC, and therefore nearly cancel each other at the outputs. Amplifier #1's bias current, however, flows out of V_{in} (Pin 4) and through R_f, forcing V_{O1} to shift negative by an amount equal to [$R_f \times I_{IB}$]. V_{O2} is shifted positive an equal amount. The output offset voltage, specified in the Electrical Characteristics, is measured with the feedback resistor shown in the Typical Application Circuit, and therefore takes into account the bias current as well as internal offset voltages of the amplifiers. The bias current is constant with respect to V_{CC}.

FC1 and FC2

Power supply rejection is provided by the capacitors (C1 and C2 in the Typical Application Circuit) at FC1 and FC2. C2 is somewhat dominant at low frequencies, while C1 is dominant at high frequencies, as shown in the graphs of Figures 4 to 7. The required values of C1 and C2 depend on the conditions of each application. A line powered speakerphone, for example, will require more filtering than a circuit powered by a well regulated power supply. The amount of rejection is a function of the capacitors, and the equivalent impedance looking into FC1 and FC2 (listed in the Electrical Characteristics as R_{FC1} and R_{FC2}).

In addition to providing filtering, C1 and C2 also affect the turn–on time of the circuit at power–up, since the two capacitors must charge up through the internal 50 k and 125 kΩ resistors. The graph of Figure 1 indicates the turn–on time upon application of V_{CC} of +6.0 V. The turn–on time is ≈60% longer for V_{CC} = 3.0 V, and ≈20% less for V_{CC} = 9.0 V. Turn–off time is <10 µs upon removal of V_{CC}.

Figure 1. Turn–On Time versus C1, C2 at Power–On



Chip Disable

The Chip Disable (Pin 1) can be used to power down the IC to conserve power, or for muting, or both. When at a Logic "0" (0 V to 0.8 V), the MC34119 is enabled for normal operation. When Pin 1 is at a Logic "1" (2.0 V to V_{CC} V), the IC is disabled. If Pin 1 is open, that is equivalent to a Logic "0," although good design practice dictates that an input should never be left open. Input impedance at Pin 1 is a nominal 90 kΩ. The power supply current (when disabled) is shown in Figure 15.

Muting, defined as the change in differential gain from normal operation to muted operation, is in excess of 70 dB. The turn–off time of the audio output, from the application of the CD signal, is <2.0 µs, and turn on–time is 12 ms–15 ms. Both times are independent of C1, C2, and V_{CC}.

When the MC34119 is disabled, the voltages at FC1 and FC2 do not change as they are powered from V_{CC}. The outputs, V_{O1} and V_{O2}, change to a high impedance condition, removing the signal from the speaker. If signals from other sources are to be applied to the outputs (while disabled), they must be within the range of V_{CC} and Ground.

Power Dissipation

Figures 8 to 10 indicate the device dissipation (within the IC) for various combinations of V_{CC}, R_L, and load power. The maximum power which can safely be dissipated within the MC34119 is found from the following equation:

$$P_D = (140°C – T_A)/\theta_{JA}$$

where T_A is the ambient temperature; and θ_{JA} is the package thermal resistance (100°C/W for the standard DIP package, and 180°C/W for the surface mount package.)

The power dissipated within the MC34119, in a given application, is found from the following equation:

$$P_D = (V_{CC} \times I_{CC}) + (I_{RMS} \times V_{CC}) – (R_L \times I_{RMS}^2)$$

where I_{CC} is obtained from Figure 15; and I_{RMS} is the RMS current at the load; and R_L is the load resistance.

Figures 8 to 10, along with Figures 11 to 13 (distortion curves), and a peak working load current of ±200 mA, define the operating range for the MC34119. The operating range is further defined in terms of allowable load power in Figure 14 for loads of 8.0 Ω, 16 Ω and 32 Ω. The left (ascending) portion of each of the three curves is defined by the power level at which 10% distortion occurs. The center flat portion of each curve is defined by the maximum output current capability of the MC34119. The right (descending) portion of each curve is defined by the maximum internal power dissipation of the IC at 25°C. At higher ambient temperatures, the maximum load power must be reduced according to the above equations. Operating the device beyond the current and junction temperature limits will degrade long term reliability.

Layout Considerations

Normally a snubber is not needed at the output of the MC34119, unlike many other audio amplifiers. However, the PC board layout, stray capacitances, and the manner in which the speaker wires are configured, may dictate otherwise. Generally, the speaker wires should be twisted tightly, and not more than a few inches in length.

Figure 2. Amplifier #1 Open Loop Gain and Phase

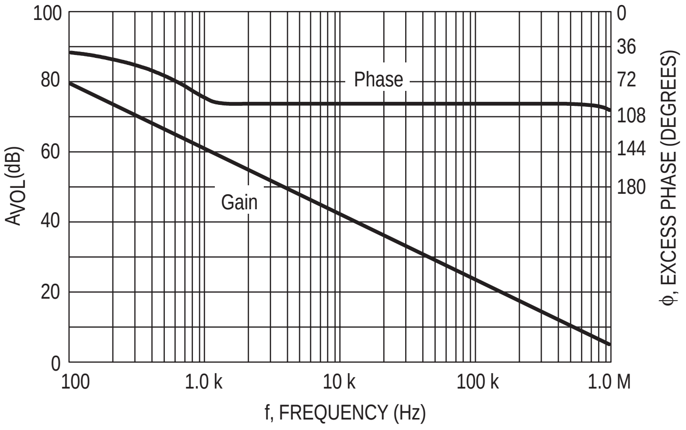


Figure 3. Differential Gain versus Frequency

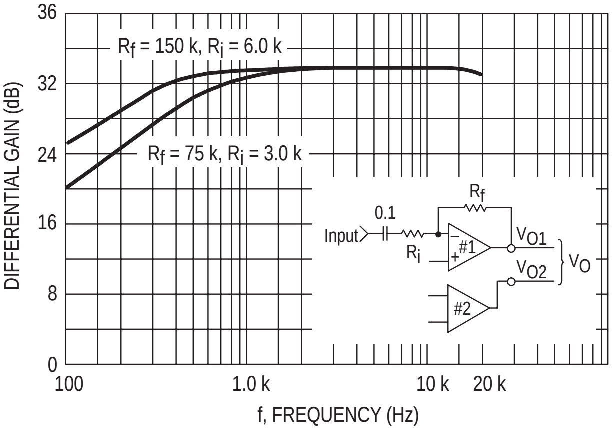


Figure 4. Power Supply Rejection versus Frequency (C2 = 10 µF)

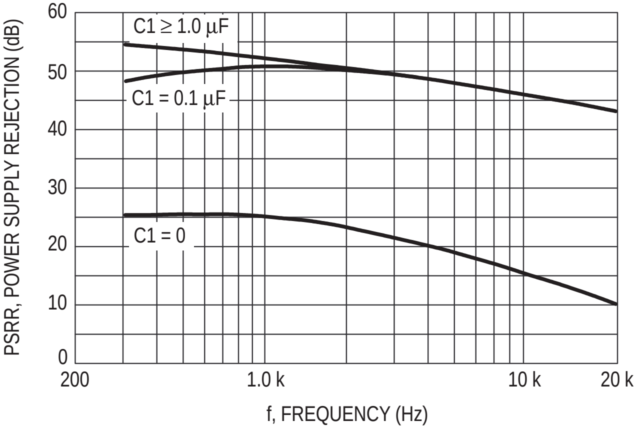


Figure 5. Power Supply Rejection versus Frequency (C2 = 5.0 µF)

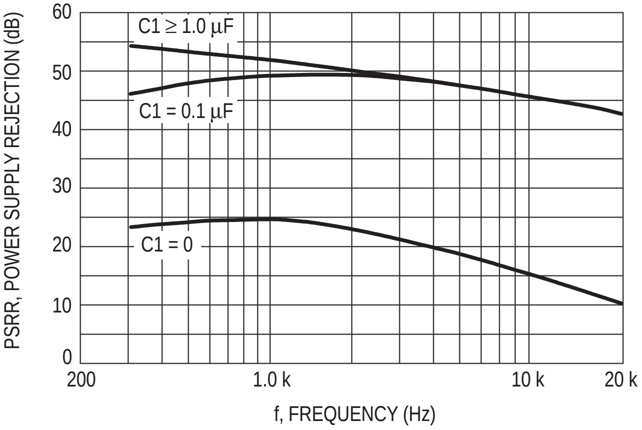


Figure 6. Power Supply Rejection versus Frequency (C2 = 1.0 µF)

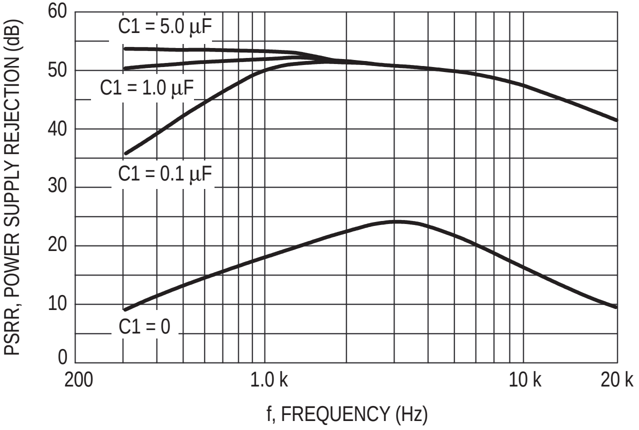


Figure 7. Power Supply Rejection versus Frequency (C2 = 0)

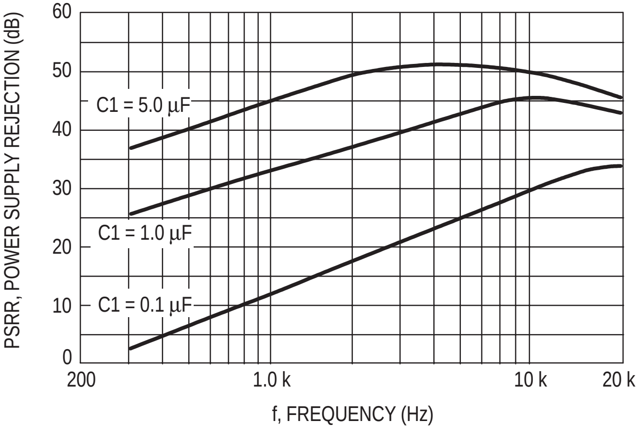


Figure 8. Device Dissipation, 8.0 Ω Load

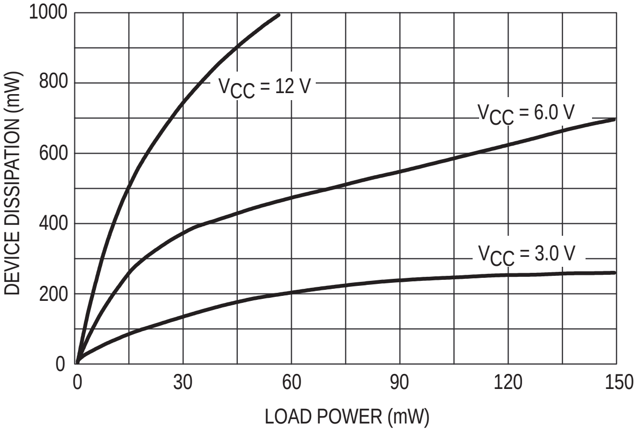


Figure 9. Device Dissipation, 16 Ω Load

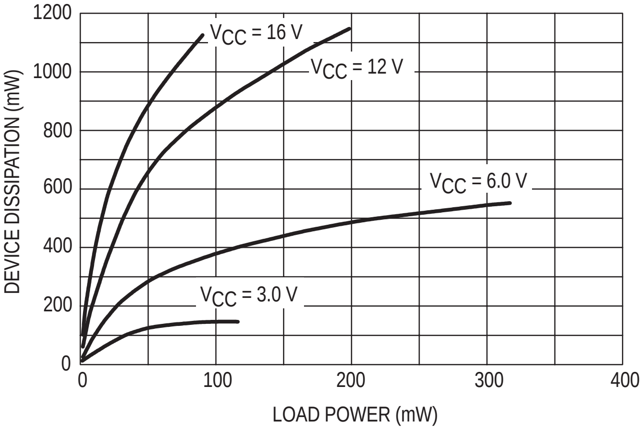


Figure 10. Device Dissipation, 32 Ω Load

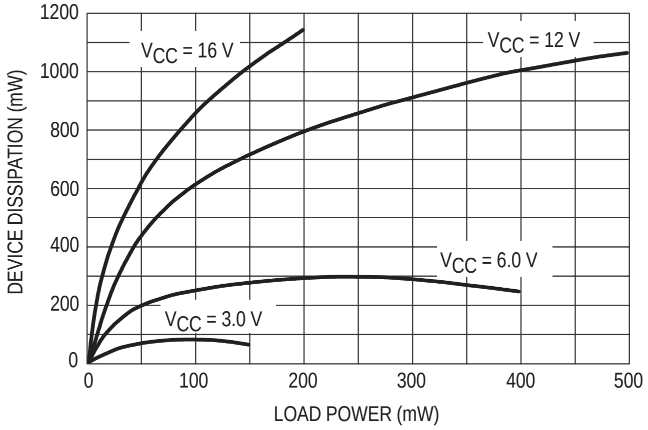


Figure 11. Distortion versus Power

(f = 1.0 kHz, AVD = 34 dB)

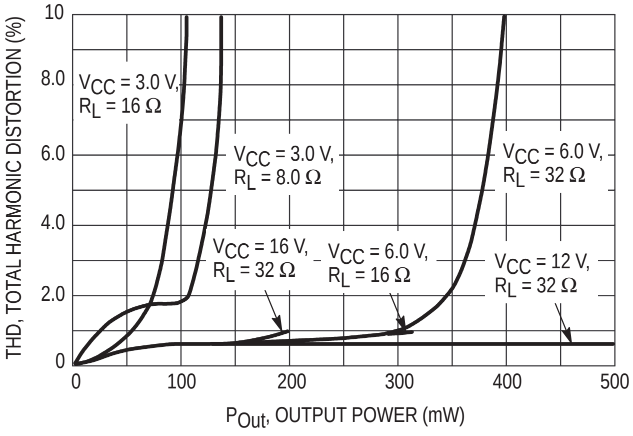


Figure 12. Distortion versus Power

(f = 3.0 kHz, AVD = 34 dB)

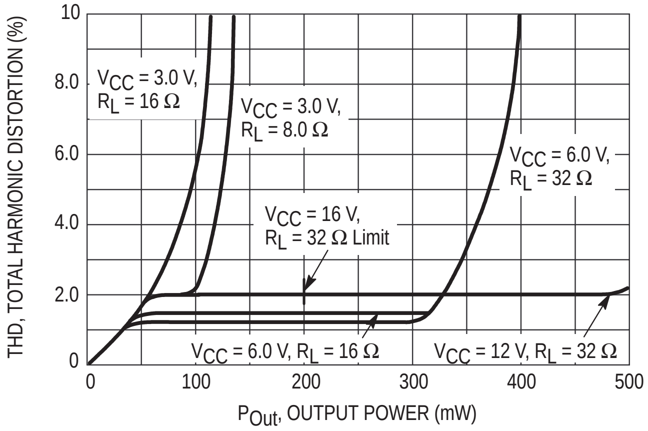


Figure 13. Distortion versus Power

(f = 1, 3.0 kHz, AVD = 12 dB)

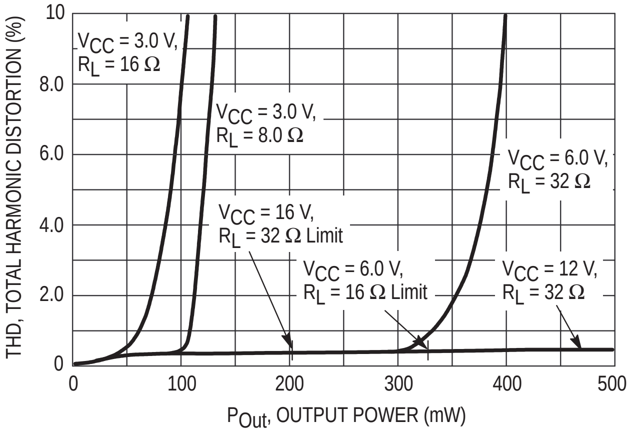


Figure 14. Maximum Allowable Load Power

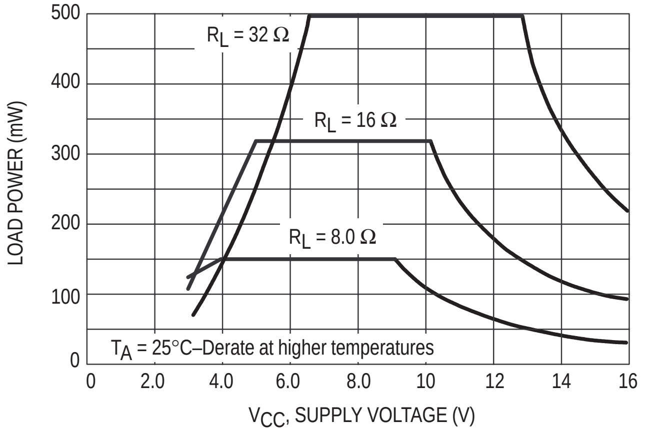


Figure 15. Power Supply Current

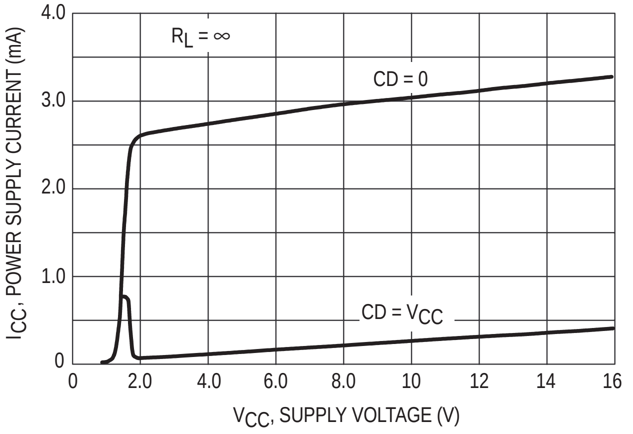


Figure 16. Small Signal Response

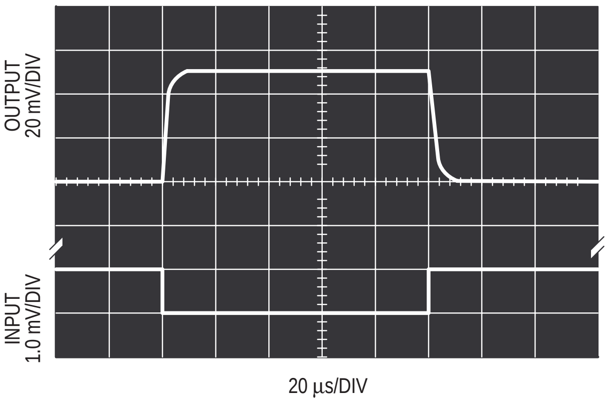


Figure 17. Large Signal Response

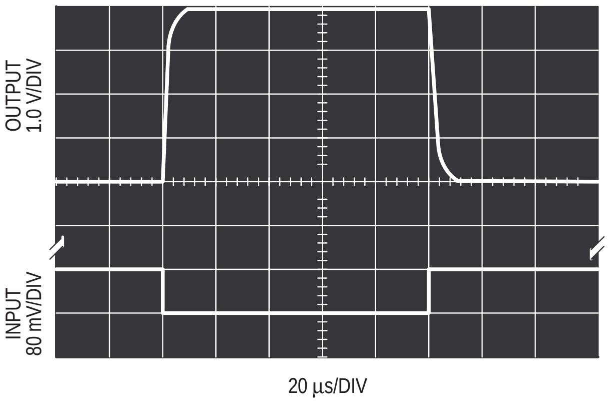


Figure 18. $V_{CC}–V_{OH}$ @ V_{O1}, V_{O2} versus Load Current

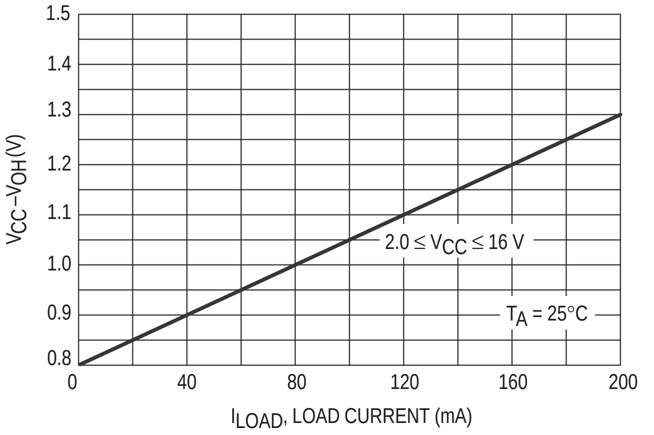


Figure 19. V_{OL} @ V_{O1}, V_{O2} versus Load Current

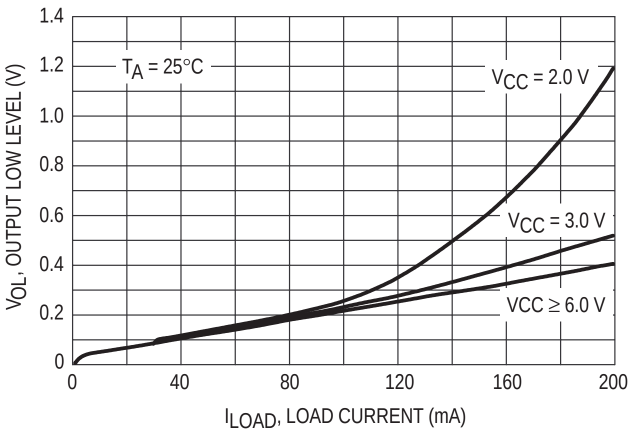


Figure 20. Input Characteristics @ CD (Pin 1)

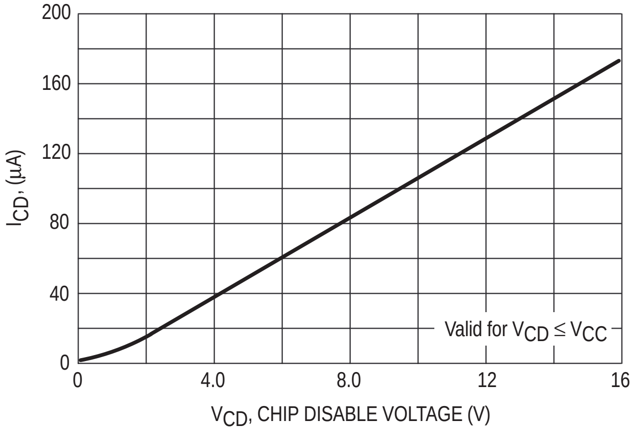
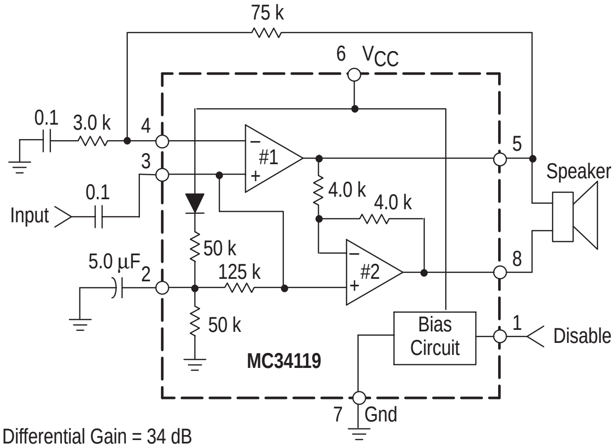


Figure 21. Audio Amplifier with High Input Impedance



Differential Gain = 34 dB
Frequency Response: See Figure 3
Input Impedance ≈ 125 kΩ
PSRR ≈ 50 dB

Figure 22. Audio Amplifier with Bass Suppression

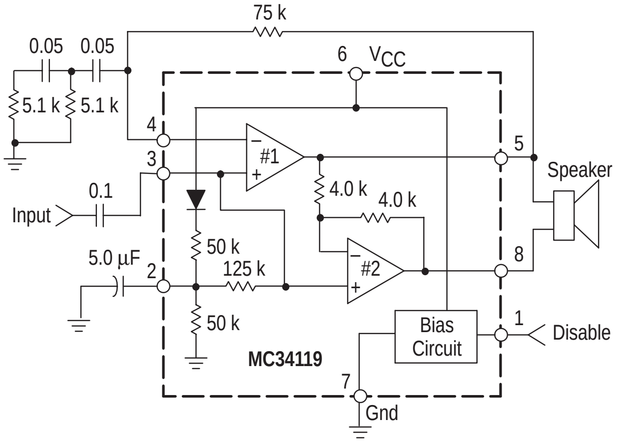


Figure 23. Frequency Response of Figure 22

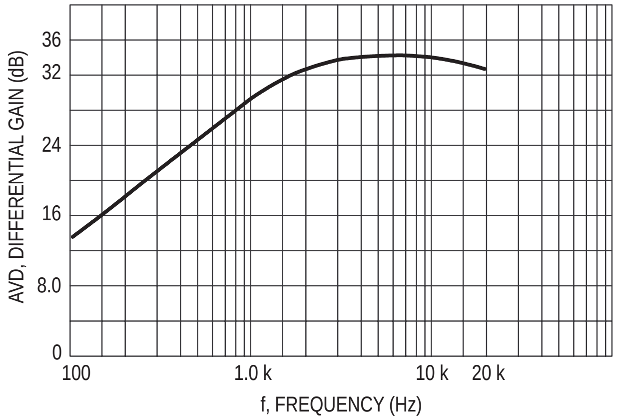


Figure 24. Audio Amplifier with Bandpass

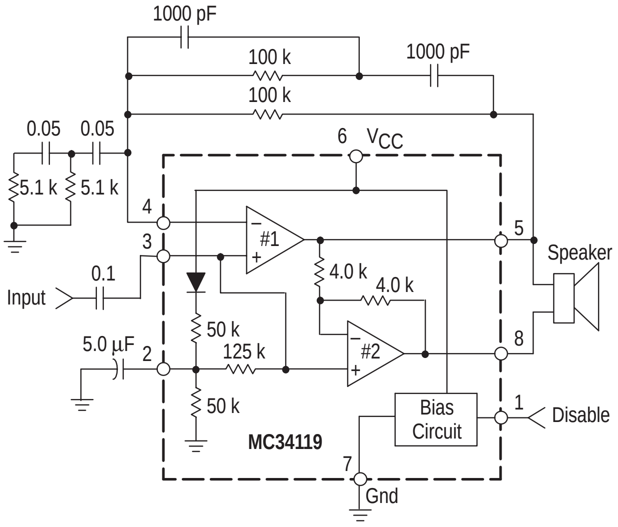


Figure 25. Frequency Response of Figure 24

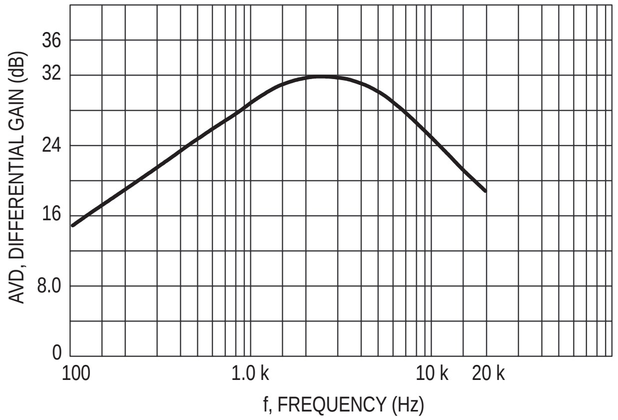
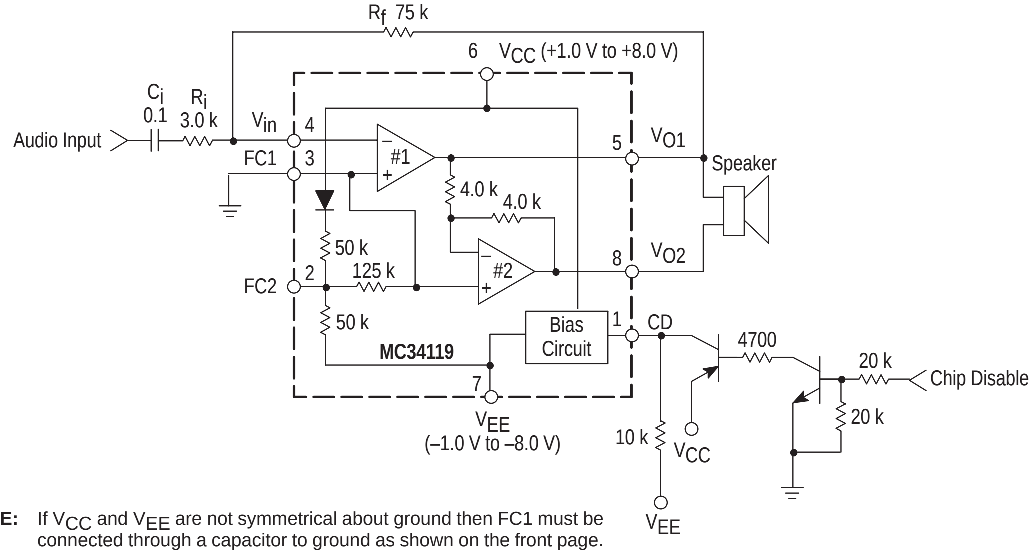


Figure 26. Split Supply Operation



NOTE: If V_{CC} and V_{EE} are not symmetrical about ground then FC1 must be connected through a capacitor to ground as shown on the front page.

MOTOROLA

MC44002
MC44007

Advance Information

Chroma 4 Multistandard Video Processor

The MC44002/7 is a highly advanced circuit which performs most of the basic functions required for a color TV. All of its advanced features are under processor control via an I^{2}C bus, enabling potentiometer controls to be removed completely. In this way the component count may be reduced dramatically, allowing significant cost savings together with the possibility of implementing sophisticated automatic test routines. Using the MC44002/7, TV manufacturers will be able to build a standard chassis for anywhere in the world. Additional features include 4 selectable matrix modes (primarily for NTSC), fast beam current limiting and 16:9 display.

- Operation from a Single 5.0 V Supply; Typical Current Consumption Only 120 mA
- Full PAL/SECAM/NTSC Capability (4 Matrix Modes)
- Dual Composite Video or S-VHS Inputs
- All Chroma/Luma Channel Filtering, and Luma Delay Line Are Integrated Using Sampled Data Filters Requiring No External Components
- Filters Automatically Commutate with Change of Standard
- Chroma Delay Line is Realized with a 16 Pin Companion Device, the MC44140
- RGB Drives Incorporate Contrast and Brightness Controls and Auto Gray Scale
- Switched RGB Inputs with Separate Saturation Control
- Auxiliary Y, R-Y, B-Y Inputs
- Line Timebase Featuring H-Phase Control, Time Constant and Switchable Phase Detector Gain
- Vertical Timebase Incorporating Vertical Geometry Corrections
- 16:9 Display Mode Capability
- E-W Parabola Drive Incorporating Horizontal Geometry Corrections
- Beam Current Monitor with Breathing Compensation
- Analog Contrast Control, Allowing Fast Beam Current Limitation
- MC44007 Decoders PAL/NTSC Only

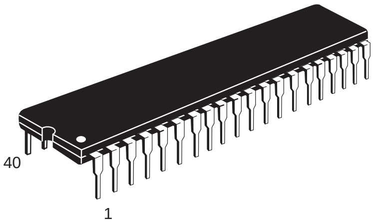
MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted.)

Rating	Pin	Symbol	Value	Unit
Supply Voltage	35	V_{CC}	6.0	Vdc
Operating Ambient Temperature	–	T_A	0 to + 70	°C
Storage Temperature	–	T_{stg}	– 65 to +150	°C
Junction Temperature	–	T_J	+150	°C
Drive Output Sink Current	12	I_{12}	2.0	mA
Applied Voltage Range: Feedback Anode Current All Other Pins	 20 9 –	 V_{20} V_9 V_i	 0 to +8.0 – 2.0 to V_{CC} 0 to V_{CC}	Vdc
ESD				V

NOTE: ESD data available upon request.

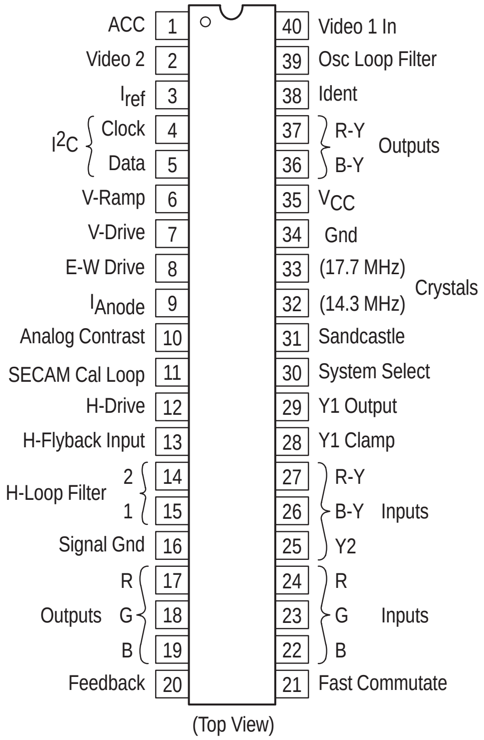
CHROMA 4
VIDEO PROCESSOR

SEMICONDUCTOR
TECHNICAL DATA



P SUFFIX
PLASTIC PACKAGE
CASE 711

PIN CONNECTIONS



ORDERING INFORMATION

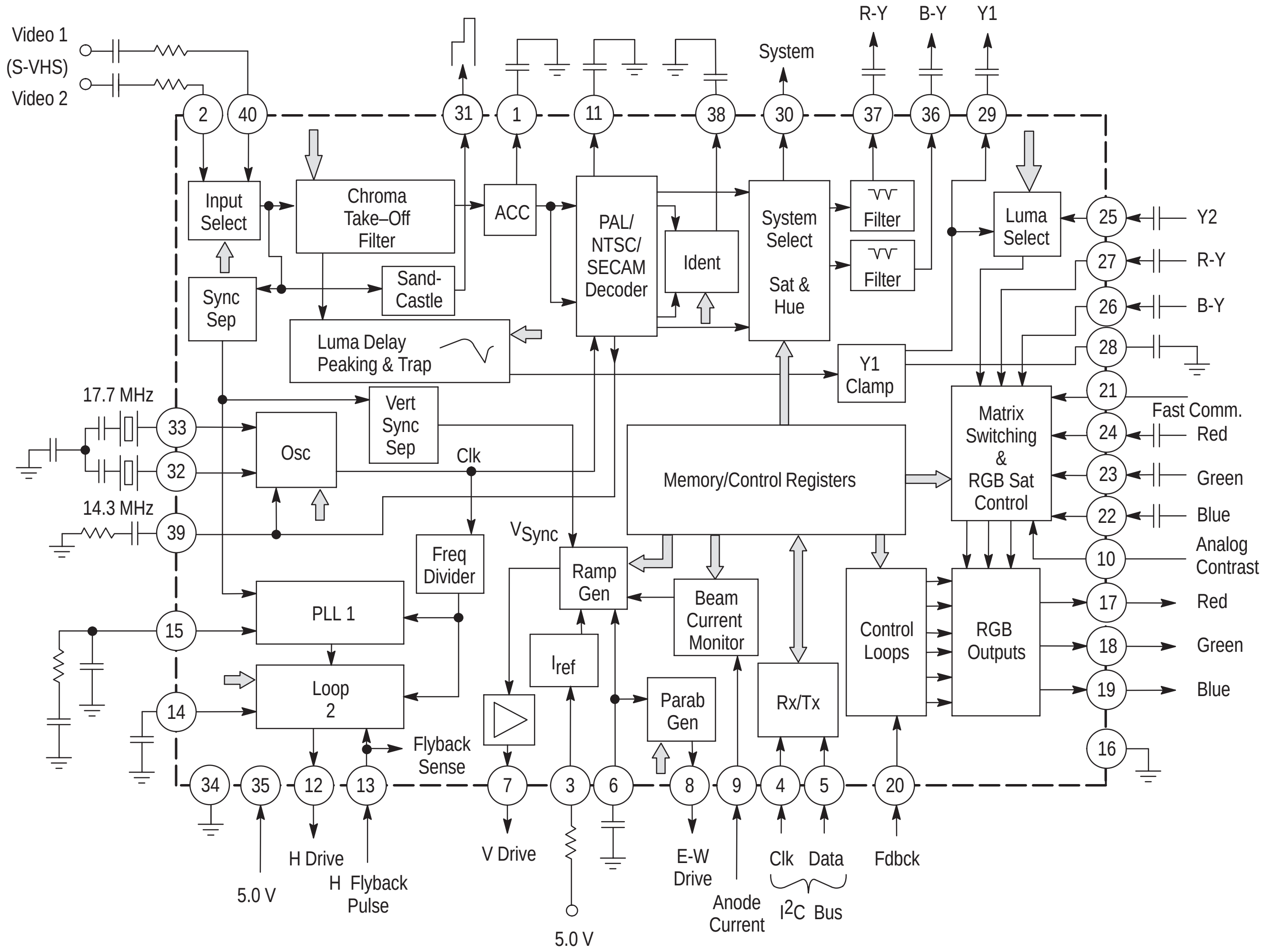
Device	Operating Temperature Range	Package
MC44002P	T_A = 0° to +70°C	Plastic DIP
MC44007P		Plastic DIP

MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted.)

Rating	Pin	Symbol	Value	Unit
Human Body Model	–	–	±2000	
Machine Model	–	–	±200	

NOTE: ESD data available upon request.

Simplified Block Diagram



This device contains 6,245 active transistors.

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 Vdc, I_3 = 70 µA, T_A = 25°C, unless otherwise noted.)

Characteristic	Pin	Min	Typ	Max	Unit
Supply Voltage	35	4.75	5.0	5.25	V
Operating Current	35	90	120	180	mA
Reference Current, Input Voltage	3	1.0	1.3	1.6	V
Thermal Resistance, Junction–to–Ambient	–	–	56	–	°C/W

NOTES:
Composite Video Input Signal Level = 1.0 Vpp
Black-to-White = 0.Vpp7 , Syn-to-Black = 0.3 Vpp
PAL/NTSC = 75% color bars; Burst = 300 mVpp
SECAM = 75% color bars
Horizontal Timebase started (subaddress 00)
Vertical Breathing control set to 00; V9 = 0 V
All other analog controls set to midrange 32
Video Peaking “P1, P2, P3” bits high

TEST CONDITIONS (unless otherwise noted.)

V_{CC} = 5.0 V I_{ref} = 70 µA T_A = 25°C
Video Composite Input = 1.0 Vpp – Black–to–White = 0.7 Vpp – Black–to–Sync = 0.3 Vpp
Horizontal Timebase Started (Reg. 00)
Vertical Breathing Control Set to 00
Pin 9 = 0 V Pin 10 = 5.0 V
PAL/NTSC = 75% Color Bars –Burst = 300 mVpp SECAM = 75% Color Bars (MC44002 only)
All Analog Controls Set to Midpoint (32)
Luma Peaking at Min. (P1 – P3 = 111)

Control Bits Setup

Name	Value	Function Status
V1/V2	1	Video Input 1 Selected
H EN	0	Horizontal Drive Enabled
BRI EN	1	“Bright” Sample “On”
$\overline{\text{HGAIN1}}$	0	Horizontal Phase Detector Gain Reduced by 3 Enabled
YX EN	0	Luma Matrix Disabled
Y1 EN	1	Luma from Filters “On”
D EN	0	RGB Inputs Enabled
XS	0	Pin 33 Crystal Enabled
TEST	1	Outputs Sampled Once/Field
FSI	0	50 Hz Field Rate
T3	1	Low Pass Filter Enabled
VD1	1	4:3 Display Mode
2xFh	0	Horizontal Drive at 1xFh
NORM	0	Horizontal Reference Divider for 17.7 MHz
HGAIN2	1	Horizontal Phase Detector Gain Reduced by 2 Enabled
INTSEL	1	Long Vertical Time Constant
Y2 EN	0	External Luma Input “Off”
SSD	0	SECAM Mode Select Enabled
CALKIL	1	Horizontal Calibration Loop Enabled
BAI	1	Vertical Blanking for 625 Lines
S–VHS	1	Composite Video Input

ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Pin	Min	Typ	Max	Unit
BUS REQUIREMENTS						
Maximum Output Low Voltage I_{sink} = 1.0 mA, Device in “Read” Mode	$V_{OL(max)}$	5	–	0.7	–	V
Maximum Sink Current V_{OL} = 0.7 V, Device in “Read” Mode	$I_{sink(max)}$	5	–	1.0	–	mA
Minimum Input High Voltage	$V_{IH(min)}$	5	–	3.0	–	V
Maximum Input Low Voltage	$V_{IL(max)}$	5	–	1.5	–	V
Maximum Rise Time Between V_{IH} and V_{IL} Levels	$t_{r(max)}$	4, 5	–	1.0	–	μs
SCL Clock Frequency	f_{SCL}	4	–	–	100	kHz
HORIZONTAL TIMEBASE						
Free–Running Frequency (Calibration Mode)	–	31				kHz
17.734475 MHz Crystal. “NORM” Bit = 0; “H EN” Bit = 1 (Horizontal Drive Disabled)			15.39	15.625	15.85	
14.31818 MHz Crystal. “NORM” Bit = 1; “H EN” Bit = 1 (Horizontal Drive Disabled)			15.42	15.75	15.98	
H–Loop 1 (Pin 15 Current Forced to ± 20 μA)	–	12				kHz
Minimum Frequency			13.85	14.25	14.65	
Maximum Frequency			16.05	16.55	17.05	
Frequency Range			–	2.3	–	
VCO Control Gain	–	12, 15	1.9	2.4	2.9	kHz/V
Phase Detector Gain “HGAIN1” Bit = 1; “HGAIN2” Bit = 0	–	15	18	27	39	μA/μs
Phase Detector Gain Reduction Factor	–	15				–
“HGAIN1“ Bit Switched from 1 to 0			2.5	3.0	3.5	
“HGAIN2“ Bit Switched from 0 to 1			1.75	2.0	2.25	
Line Drive Output Saturation Voltage I12 = 1.0 mA	–	12	–	0.25	0.5	V
Horizontal Drive Pulse Low Defined by Internal Counter, Deflection Transistor “Off”, Period is 64 μs	–	12	–	27	–	μs
Horizontal Flyback Input Resistance V13 = 2.0 V	–	13	–	50	–	kΩ
Horizontal Flyback Clamping Voltages	–	13				V
I13 = 500 μA			–	5.7	–	
I13 = –50 μA			–	–0.5	–	
Horizontal Flyback Threshold Current Should be Externally Limited to 500 μA Peak by an External Resistor	–	13	30	–	–	μA
Horizontal Phase Control Range Flyback Duration: 12 μs	–	12	8.0	–	12	μs
External Delay Compensation From Horizontal Drive to Center of Flyback Pulse. Flyback Duration: 12 μs	–	12, 13	6.0	–	18	μs
VERTICAL TIMEBASE (All Values are Related to Pin 3 Reference Current)						
Vertical Drive Amplitude (4:3 Display)	–	7				V
(00)			1.15	1.33	1.5	
(32)			1.55	1.75	1.95	
(63)			1.95	2.18	2.4	
C6 = 82 nF, Assuming Zero Tolerance Capacitance, “VDI” Set to “1”						
Vertical Drive Amplitude Control Range (4:3 Display) C6 = 82 nF, Assuming Zero Tolerance Capacitance, “VDI” Set to “1”, Vertical Amplitude Varied from (00) to (63)	–	7	0.75	0.85	1.0	V

ELECTRICAL CHARACTERISTICS (continued)

Parameter	Symbol	Pin	Min	Typ	Max	Unit
VERTICAL TIMEBASE (All Values are Related to Pin 3 Reference Current)						
Ramp Amplitude Ratio Between 4:3 and 16:9 Display Modes Vertical Amplitude = (32)	–	7	0.7	0.8	0.9	–
Maximum Ramp Amplitude Change With 525/625 Mode Change	–	7	–	2.0	–	%
Vertical Ramp Low Voltage (4:3 Display) Pin 6 Voltage Set to 0 V, “VDI” Set to “1”, Vertical Position = (00)	–	7	–	0.65	–	V
Vertical Ramp Low Voltage (16:9 Display) Pin 6 Voltage Set to 0 V, “VDI” Set to “0”, Vertical Position = (00), Measured After 16:9 Holding Period	–	7	–	0.85	–	V
Vertical Ramp High Voltage Pin 6 Open, “VDI” Set to “0” or “1”, Vertical Position = (63)	–	7	–	4.15	–	V
Vertical Ramp Position Control Range Versus Vertical Ramp Voltage at Vertical Position (32), Measured at V_m, “VDI” Set to “0” or “1”, Vertical Position Varied from (00) to (63)	–	7	±0.5	±0.75	±1.0	V
Vertical Ramp Clamping Duration (t_c) Defined by Internal Counter	–	7	–	512	–	µs
Maximum Output Source Current	–	7	1.0	–	–	mA
Maximum Output Sink Current	–	7	200	–	–	µA
Vertical Linearity	–	7				–
(00)			–	0.8	–	
(63)			–	1.1	–	
Change in Ramp current as Pin 9 Current Varied from 0 to 6.4 µA	–	6				µA
Vertical Breathing Correction = (63)			0.15	0.75	1.3	
Vertical Breathing Correction = (00)			–	0	–	
Gain V7/V6	–	6, 7	0.9	0.95	1.0	V/V
E–W CORRECTION (V6(b) = 0.2 V, V6(m) = 1.1 V, V6(e) = 2.0 V)						
Horizontal Amplitude	–	8				µA
(00)			0	0.2	20	
(63)			150	300	–	
Corner Correction = (00), Tilt = (32), Parabola Amplitude = (00), Measured at T_m.						
Parabola Amplitude	–	8				µA
(00)			0	0.2	10	
(63)			100	250	–	
Corner Correction = (00), Horizontal Amplitude = (32), Tilt = (32), Measured at T_b, T_m and T_e.						
Corner Correction	–	8				µA
(00)			0	0.2	10	
(63)			–	–150	–30	
Horizontal Amplitude = (63), Parabola Amplitude = (00), Tilt = (32), Measured at T_b, T_m and T_e.						
Parabola Tilt	–	8				–
(00)			–	1.9	–	
(63)			–	–1.9	–	
Corner Correction = (00), Horizontal Amplitude = (32), Parabola Amplitude = (32), Measured at T_b, T_m and T_e.						
E–W Drive Output Voltage	–	8	1.0	–	V_{CC}	V

ELECTRICAL CHARACTERISTICS (continued)

Parameter	Symbol	Pin	Min	Typ	Max	Unit
E–W CORRECTION (V6(b) = 0.2 V, V6(m) = 1.1 V, V6(e) = 2.0 V)						
E–W DACs Differential Non–Linearity Error At Minor Transitions: Steps 0–1: 1–2; 3–4; 7–8; 15–16. At Major Transition: Step 31–32	–	8	 –1.0 –2.0	 – –	 1.0 1.0	LSB
SYNC SEPARATOR						
Sync Amplitude to Operate the Device From Black to Sync, Black Picture, Standard Timing Specifications on Sync Signal	–	2, 40 22, 23, 24, 25	100 –	– 160	– –	mV
Vertical Sync Separator Delay Time: t_d “INTSEL” = 0 “INTSEL” = 1 From Vertical Sync Pulse to Vertical Ramp Reset	–	2, 40	 – –	 36 68	 – –	µs
Vertical Sync Window	–	2, 40, 22, 23, 24, 25	448	–	740	Half Lines
COMPOSITE VIDEO PROCESSING (All measurements in NORMAL mode, unless otherwise noted.)						
Composite Video Input Amplitude Load Impedance 75 Ω, Less than 5% Distortion	–	2, 40	0.7	1.0	1.4	Vpp
Video 1/Video 2 Input Crosstalk @ f = (2.0 MHz), Measured on Y1 Output	–	29	–	–	–40	dB
Variable Input LPF Cut–Off Frequency 17.7 MHz Crystal Selected 14.3 MHz Crystal Selected	–	29	 – –	 6.0 4.85	 – –	MHz
Chroma Subcarrier Rejection PAL 4.43 MHz (17.7 MHz Crystal Selected) NTSC 3.58 MHz (14.3 MHz Crystal Selected) SECAM (F_OR and F_OB) (17.7 MHz Crystal Selected)	–	29	 25 25 18	 30 30 20	 – – –	dB
Y1 Output Resistance	–	29	–	–	300	Ω
Y1 Bandwidth (–3.0 dB) PAL Minimum Peaking, “T3” Set to 1 (Input LPF “On”) SECAM Minimum Peaking, “T3” Set to 0 (Input LPF “Off”)	–	29	 2.5 2.5	 3.0 3.0	 – –	MHz
Luma Peaking Range Measured at 3.0 MHz, 17.7 MHz Crystal Selected	–	29	6.0	8.5	–	dB
Luma Gain (@ 100 kHz)	–	2, 40, 29	0.9	1.1	1.3	V/V
Overshoot Peaking at Step 3 (100)	–	29	–	5.0	–	%
Source Impedance	–	2, 40	0	–	1.5	kΩ
Luma Delay Range PAL/SECAM (17.7 MHz Crystal Selected) NTSC 3.58 (14.3 MHz Crystal Selected)	–	29	 – –	 280 350	 – –	ns
Video In to Luma Out Delay Difference Between PAL and SECAM (MC44002 only) Luma Delay Minimum: (D1 D2 D3) = (0 0 0), Green to Magenta Transition, “T3” Set to 1 in PAL, to 0 in SECAM	–	29, 40	–	260	–	ns
PAL/NTSC DECODER						
Chroma Output Variation For a Burst Input Varied from 60 mV to 600 mV	–	36, 37	–	–	3.0	dB
Color Kill Attenuation Referred to Standard Color Video Input, Monochrome Mode Selected	–	36, 37	40	–	–	dB

ELECTRICAL CHARACTERISTICS (continued)

Parameter	Symbol	Pin	Min	Typ	Max	Unit
PAL/NTSC DECODER						
Color Difference Output Distortion @ 1.5 V Output Signal	–	36, 37	–	–	5.0	%
Residual Chroma Subcarrier Rejection PAL NTSC Referred to Video Input	–	36, 37	 40 40	 – –	 – –	dB
Oscillator Pull–In Range PAL NTSC Referred to Nominal Subcarrier Frequency, with Ideal Xtal	–	32, 33	 ±350 ±400	 – –	 – –	Hz
R–Y, B–Y Channel Separation	–	36, 37	30	–	–	dB
B–Y/R–Y Amplitude Ratio At Standard Color Bars Signal	–	36, 37	–	1.3	–	V/V
B–Y/R–Y Amplitude Ratio Spread At Standard Color Bars Signal	–	36, 37	–2.0	–	2.0	dB
Minimum Burst Level for “ACC Active” Flag “On” Standard Set to PAL or NTSC, Increasing Burst Level Steps	–	2, 40	–	10	20	mVpp
Minimum Burst Level for “PAL Identified” Flag “On” Standard Set to PAL or NTSC, Increasing Burst Level Steps	–	2, 40	–	5.0	20	mVpp
Maximum Burst Level for “ACC Active” Flag “Off” Standard Set to PAL or NTSC, Decreasing Burst Level Steps	–	2, 40	–	5.0	–	mVpp
Maximum Burst Level for “PAL Identified” Flag “Off” Standard Set to PAL or NTSC, Decreasing Burst Level Steps	–	2, 40	–	1.0	–	mVpp
(B–Y) Color Difference Output Levels Relative to 75% Color Bars	–	36	0.7	1.1	1.5	V
Hue DAC Control Range Hue Control Register Varying from (00) to (63)	–	36, 37	±20	–	–	Deg
Chroma to Luma Delay PAL NTSC Measured on (B–Y) Output, Luma Delay Set to Minimum: (D1 D2 D3) = (0 0 0), Green to Magenta Transition, “T3” Set to 1	–	29, 36	 – –	 80 100	 – –	ns
DELAY LINE CONTROL SIGNALS						
System Select PAL NTSC SECAM (MC44002 only) EXTERNAL	–	30	 – 1.4 2.75 3.7	 75 1.65 3.0 4.0	 400 1.9 3.25 4.3	 mV V V V
Sandcastle Level 1 Level 2 Level 3 Level 4 See Figure 4	–	31	 3.7 2.75 1..3 –	 4.0 2.95 1.55 75	 4.3 3.15 1.8 –	 V V V mV
Sandcastle t1 t2 See Figure 4, Values Defined by Internal Counter	–	31	 5.0 4.0	 6.0 5.0	 7.0 6.0	µs

ELECTRICAL CHARACTERISTICS (continued)

Parameter	Symbol	Pin	Min	Typ	Max	Unit
S–VHS VIDEO PROCESSING (S–VHS Set to 0, “T3” Set to 0)						
Y1 Bandwidth Luma Peaking Set to Minimum	–	29	3.2	3.5	–	MHz
Minimum Burst Level for “ACC Active” Flag “On” Standard Set to PAL or NTSC, Increasing Burst Level Steps	–	2, 40	–	10	20	mVpp
Minimum Burst Level for “PAL Identified” Flag “On” Standard Set to PAL or NTSC, Increasing Burst Level Steps	–	2, 40	–	5.0	20	mVpp
Maximum Burst Level for “ACC Active” Flag “Off” Standard Set to PAL or NTSC, Decreasing Burst Level Steps	–	2, 40	–	5.0	–	mVpp
Maximum Burst Level for “PAL Identified” Flag “Off” Standard Set to PAL or NTSC, Decreasing Burst Level Steps	–	2, 40	–	1.0	–	mVpp
Video In to Luma Out Delay Difference Between S–VHS and Normal Mode Luma Delay Minimum in Normal Mode, Set to Step 6 in S–VHS Mode, Green to Magenta Transition, “T3” Set to 1 in Normal Mode, to 0 in S–VHS Mode	–	2, 40, 29	–	310	–	ns
Chroma to Luma Delay Difference Between S–VHS and Normal Mode Measured on (B–Y) Output, Luma Delay Minimum in Normal Mode, Set to Step 6 in S–VHS Mode, Green to Magenta Transition, “T3” Set to 1 in Normal Mode, to 0 in S–VHS Mode	–	29, 36, 2, 40	–	60	–	ns
SECAM DECODER (MC44002 ONLY)						
Minimum Subcarrier Level for “SECAM Identified” Flag Measured at f_oR	–	2, 40	–	10	20	mVpp
Color Kill Attenuation Monochrome Mode Selected Referred to Color Difference Output Signal with SECAM Selected and Identified	–	36, 37	40	50	–	dB
Color Difference Zero Level Error Relative to 75% Color Bars, Difference Between Signal Measured at t1 and Active Black Level (Black Bar)	–	36, 37	–	±1.0	±3.0	%
Color Difference Output Distortion Subcarrier Level at f_oR = 20–400 mV @ 1.5 V Output Signal	–	36, 37	–	–	5.0	%
Transient Response (B–Y) (R–Y) Generator Rise Time – 600 ns (B–Y), Green to Magenta Transition, Measured Between 10% and 90% Levels	–	 36 37	 – –	 650 750	 800 900	ns
B–Y/R–Y Amplitude Ratio Ratio Spread Relative to 75% Color Bars	–	36, 37	 – –2.0	 1.3 –	 – 2.0	 V/V dB
Residual Carrier and Harmonics (4.0 to 13.5 MHz) At Standard Color Bars Signal	–	36, 37	–	–	1.0	%
(B–Y) Color Difference Output Levels Relative to 75% Color Bars	–	36	–	1.1	–	V
PAL/SECAM Color Difference Ratio Nominal Input Signals	–	36	0.8	1.0	1.2	–

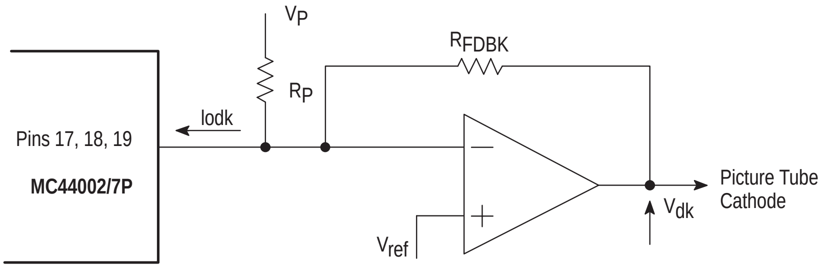
ELECTRICAL CHARACTERISTICS (continued)

Parameter	Symbol	Pin	Min	Typ	Max	Unit
SECAM DECODER (MC44002 ONLY)						
Chroma to Luma Delay Luma Delay Set to Minimum: (D1 D2 D3) = (0 0 0), Green to Magenta Transition, “T3” Set to 0	–	29, 36	–	420	–	ns
Patterning Full Screen 75% Color Frequency, 500 kHz Low Pass Filter, Relative to Black to Color Output Signal	–	36	–	–	5.0	%
Line to Line Luma Levels Difference Full Screen 75% Yellow Color Frequency, Relative to Black to Yellow Output Signal	–	29	–	–	1.5	%
Chroma to Luma Delay Difference Between PAL and SECAM Measured on (B–Y) Output, Luma Delay Set to Minimum: (D1 D2 D3) = (0 0 0), Green to Magenta Transition, “T3” Set to 0 in SECAM, to 1 in PAL	–	29, 36	–	340	–	ns
COLOR DIFFERENCE STAGES						
RGB Input Amplitude Black to Peak (Less than 5% Distortion at RGB Outputs)	–	22, 23, 24	500	700	1000	mVpp
Fast Commutate	–	21				V
Low Level			–	–	0.5	
High Level			1.0	–	–	
Y2 Input Amplitude (Less than 5% Distortion at RGB Outputs)	–	25	0.7	1.0	1.4	Vpp
Color Difference Input Amplitude (Less than 5% Distortion at RGB Outputs)	–	26, 27	–	–	1.8	Vpp
Y2/Y1 Crosstalk Measured at RGB Outputs, Measured at f = (2.0 MHz)	–	25, 29	–	–40	–30	dB
RGB to Y Crosstalk Measured at RGB Outputs, Measured at f = (2.0 MHz)	–	22, 23, 24, 25, 29	–	–40	–30	dB
RGB Transconductance Bandwidth (@ –1.0 dB)	–	24, 17, 23, 18, 22, 19	6.5	–	–	MHz
Gain Reduction in ACL Mode Pin 10 Voltage Varying from 0 to 5.0 v	–	10, 17, 18, 19	–	12.5	–	dB
Gain Reduction Sensitivity in ACL Mode Pin 10 Voltage Varying from 2.0 to 2.5 V	–	10, 17, 18, 19	–	20	–	dB/V
Demodulation Angles and Amplitudes	–	–				Deg
Mode A Rm			–	0.562	–	
Ra			–	90	–	
Gm			–	0.344	–	
Ga			–	237	–	
Mode B Rm			–	0.9	–	
Ra			–	100	–	
Gm			–	0.3	–	
Ga			–	236	–	
Mode C Rm			–	0.9	–	
Ra			–	106	–	
Gm			–	0.3	–	
Ga			–	240	–	
Mode D Rm			–	0.91	–	
Ra			–	106	–	
Gm			–	0.31	–	
Ga			–	246	–	
Definitions: Rm/Gm = Module, Ra/Ga = Argument						

ELECTRICAL CHARACTERISTICS (continued)

Parameter	Symbol	Pin	Min	Typ	Max	Unit
RGB OUTPUT STAGES						
Low Dark Sample Output Current	–	17, 18, 19				mA
Red			–	–	3.15	
Green			–	–	3.15	
Blue			–	–	3.15	
Dark Sample Cathode Current 5.0 to 15 µA, DC DAC Set to Full Scale, See Figure 1						
High Dark Sample Output Current	–	17, 18, 19				mA
Red			3.95	–	–	
Green			3.95	–	–	
Blue			3.95	–	–	
Dark Sample Cathode Current 5.0 to 15 µA, DC DAC Set to Zero, See Figure 1						
Blanking Output Current	–	17, 18, 19	6.0	–	–	mA
Maximum Y to RGB Output Transconductance Gain DAC Set to Full Scale	–	17, 18, 19	6.0	7.0	8.0	mA/V
Brightness	–	–				V
(00)			–	30	–	
(63)			–	–20	–	
Wrt Dark Sample Cathode Voltage, High Voltage Output Stage Transimpedance 39 kΩ, Dark Sample Cathode Current 15 µA, Dark Sample Cathode Voltage 140 V						
RGB Dark Sample Current Intensity Range RGB Intensity DACs Varying from (00) to (63)	–	20	15	20	–	dB
Bright to Dark Sample Current Ratio	–	20	8.0	9.5	11	µA/µA
Leakage Loop	–	20				µA
Sink Current			20	–	–	
Source Current			5.0	–	–	
Average Beam Current Detection Level	–	9				V
Excess Flag			0.9	1.0	1.1	
Overload Flag			–1.3	–1.2	–1.1	
Peak Beam Current Detection Level	–	20	6.5	6.8	7.1	V

Figure 1. Example of Output Circuitry



V_p, V_{ref}, R_{FDBK} and R_p values will determine the exact operating point.

For example, let us take:
$V_p = 5.0$ V $R_{FDBK} = 39$ kΩ
$V_{ref} = 3.6$ V
$R_p = 6.8$ kΩ

The formula giving the Dark Cathode Voltage with above circuit is: $V_{dk} = V_{ref} + R_{FDBK}*(V_{ref} – V_p + Iodk*R_p) / R_p$

With above application, component values and Iodk specifications, all 3 cathodes on all devices will always have a range of at least 120 V to 150 V.

By changing the values of V_p, V_{ref} and R_p, the cathode voltage range may be shifted up or down as required.

Figure 2. Vertical Waveforms

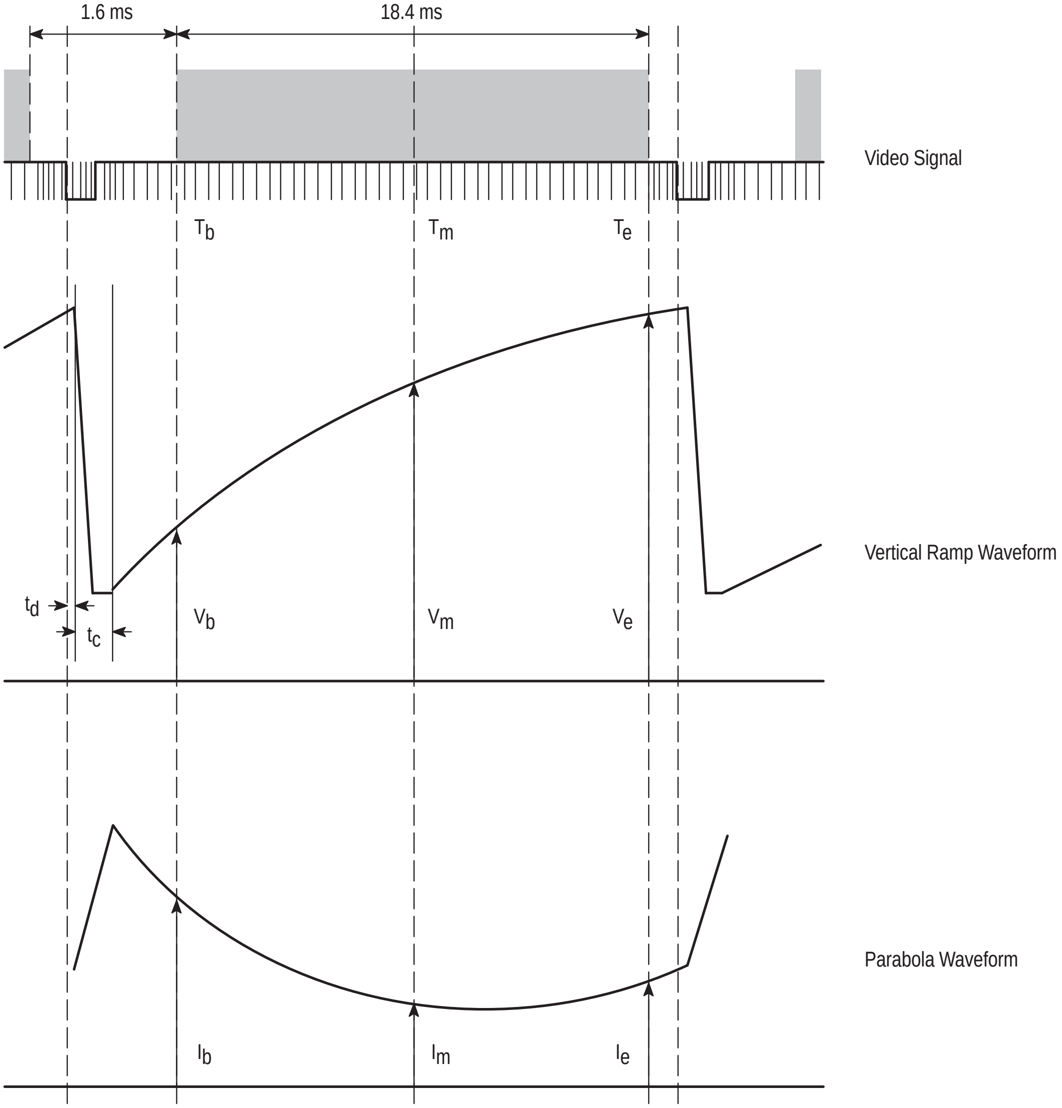
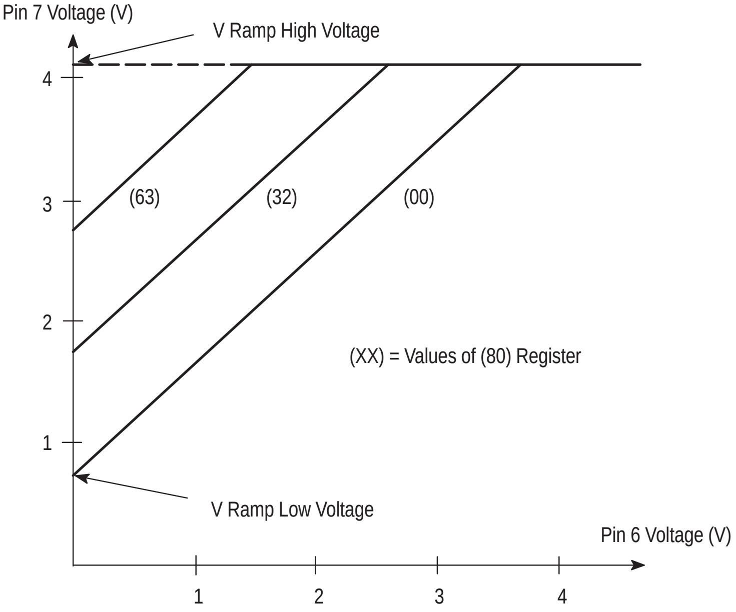


Figure 3. Vertical Ramp Positions (V7 versus V6)



Definitions

$$\text{Parabola Amplitude} = \frac{(i_b + i_e)}{2} - i_m$$

$$\text{Parabola Tilt} = \frac{(i_e - i_b)}{\text{Parabola Amplitude}}$$

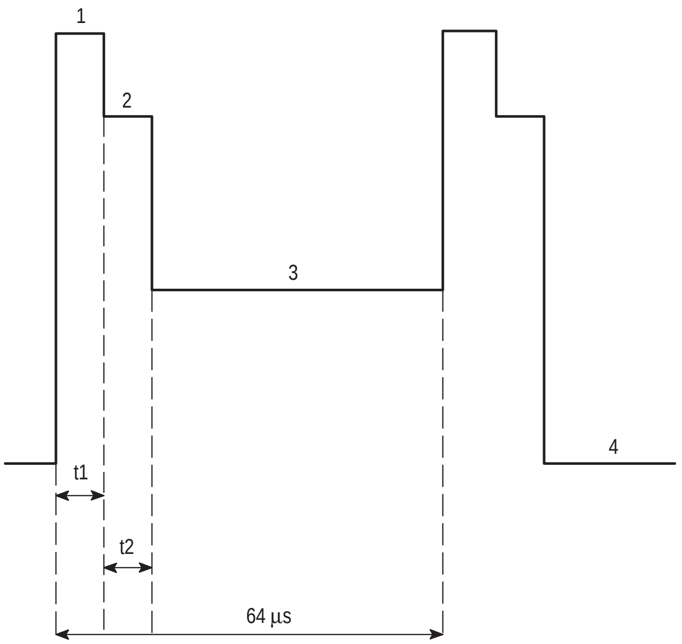
$$\text{Horizontal Amplitude} = i_m$$

$$\text{Vertical Amplitude} = V_e - V_b$$

$$\text{Vertical Linearity} = \frac{(V_e - V_m)}{V_m - V_b}$$

Corner correction is calculated in the same way as Parabola Amplitude.

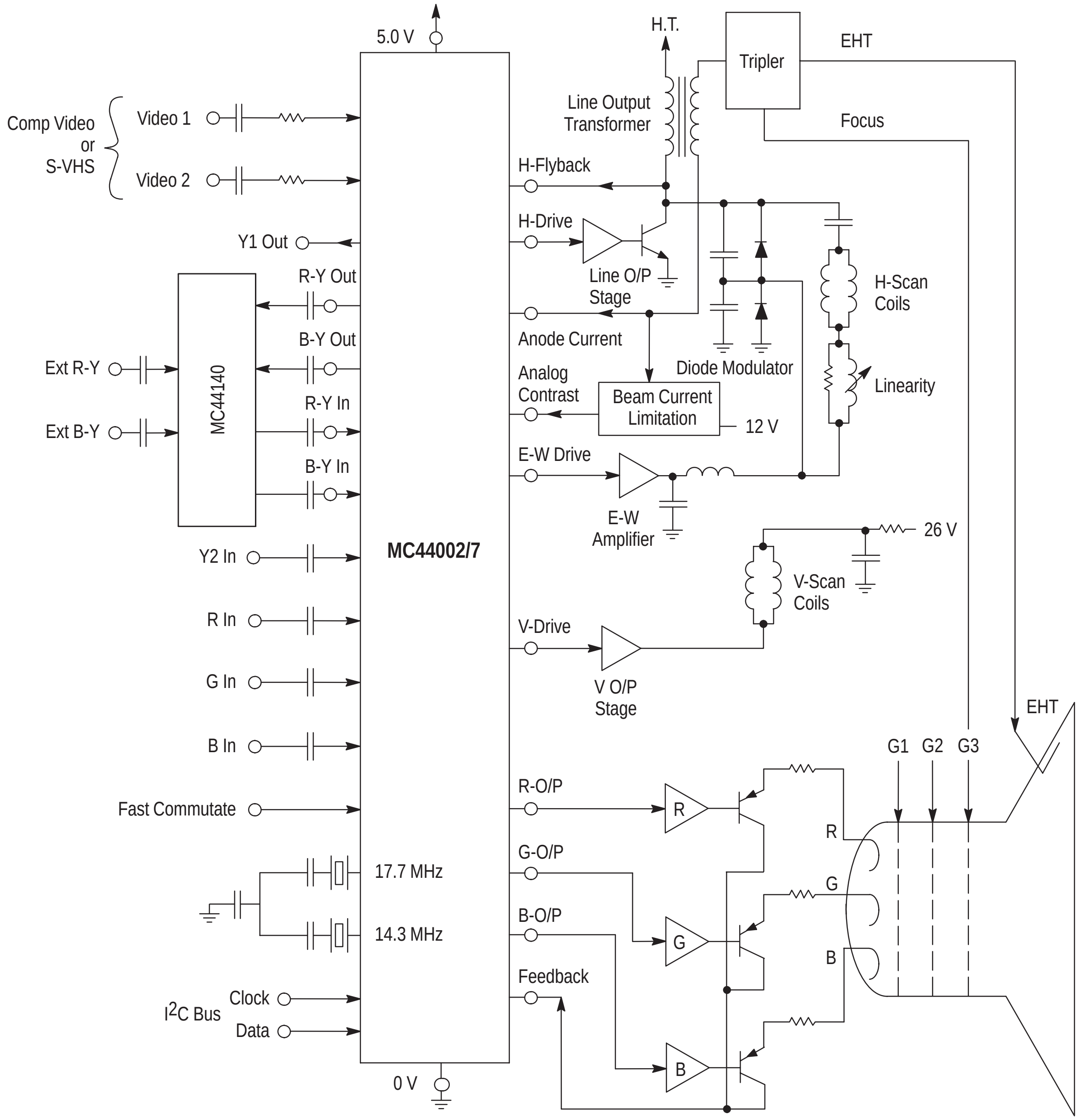
Figure 4. Sandcastle Output (Pin 31)



GENERAL DESCRIPTION OF THE CHROMA 4 SYSTEM

Figure 5 shows a simplified block diagram representation of the basic system using the MC44002/7 and its companion device the MC44140 chroma delay line. The MC44002/7 has been designed to carry out all the processing of video signals, display controls and timebase functions. There are two video inputs which can be used for normal composite video or separate Y and C inputs. In either case, the inputs are interchangeable and selection is made via the I^2C bus. The video is decoded within the MC44002/7 and involves separation, filtering, delay of the luminance part of the signal and demodulation of the chroma into color difference signals. The luminance (called Y1) together with the demodulated R-Y and B-Y are all then brought out from the IC. The color difference signals then enter the MC44140 which performs color correction in PAL and the delay line function in SECAM. Corrected color difference signals then re-enter the MC44002/7.

Figure 5. Connection to TV Chassis



The next stage is called the color difference stage where a number of control functions are carried out together with matrixing of the components to derive RGB signals. At this point a number of auxiliary signals may also be switched in, again all under MCU control. External RGB (text) and Fast Commutate enter here; also an external luminance (Y2) may be used instead of Y1. External R-Y and B-Y are switched in via the delay line circuit to save pins on the main device. The Y2 and External R-Y, B-Y will obviously be of considerable benefit from the system point of view for use with external decoders.

The final stage of video processing is the RGB outputs which drive the high voltage amplifiers connected to the tube cathodes. These outputs are controlled by a sophisticated digital servo-loop which is maintained and stabilized by a sequentially sampled beam current feedback system. Automatic gray scale control is featured as a part of this system.

Both horizontal and vertical timebases are incorporated into the MC44002/7 and control is via the I^{2}C bus. The horizontal timebase employs a dual loop system of a PLL and variable phase shifter, and the vertical uses a countdown system. For the vertical, a field rate sawtooth is available which is used to drive an external power amplifier with flyback generator (usually a single IC). The line output consists of a pulse which drives a conventional line output stage in the normal way. The line flyback pulse is sensed and used by the second loop for horizontal phase shift.

Where E-W correction is required, a parabola waveform is available for this which, with the addition of a power amplifier, can be used with a diode modulator type line output stage for dynamic width and E-W control. The bottom of the EHT overwinding is returned to the MC44002/7 and is used for anode current monitoring.

Fast beam current limitation is also made possible by the use of an analog contrast control.

A much more detailed description of each stage of the MC44002/7 will be found in the next section. Information on the delay line is to be found in its own data sheet.

Introduction

The following information describes the basic operation of the MC44002/7 IC together with the MC44140 chroma delay line. The MC44002/7 is a highly advanced circuit which performs all the video processing, timebase and display functions needed for a modern color TV. The device employs analog circuitry but with the difference that all its advanced features are under processor control, enabling external filtering and potentiometer adjustments to be removed completely. Sophisticated feedback control techniques have been used throughout the design to ensure stable operating conditions and the absence of drift with age.

The IC described herein is one of a new generation of TV circuits, which make use of a serial data bus to carry out control functions. Its revolutionary design concept permits a level of integration and degree of flexibility never achieved before. The MC44002/7 consists of a single bipolar VLSI chip which uses a high density, high frequency, low voltage process called MOSAIC 1.5. Contained within this single 40 pin package is all the circuitry needed for the video signal processing, horizontal and vertical timebases and CRT display control for today's color TV. Furthermore, all the user controls and manufacturer's set-up adjustments are under the control of the processor I^{2}C bus, eliminating the need for potentiometer controls. The MC44002/7 offers an enormous variety of different options configurable in software, to cater to virtually any video standard or circumstance commonly met. The decoder section offers full multistandard capability, able to handle PAL, SECAM (MC44002 only) and NTSC standards with 4 matrix modes available. Practically all the filtering is carried out onboard the IC by means of sampled data filters, and requires no external components or adjustment.

Digital Interface

One of the most important features of MC44002/7 is the use of processor control to replace external potentiometer and filter adjustments. Great flexibility is possible using processor control, as each user can configure the software to suit their individual application. The circuit operates on a bidirectional serial data bus, based on the well known I^{2}C bus. This system is rapidly becoming a world standard for the control of consumer equipment.

I^{2}C Bus

It is not within the scope of this data sheet to describe in detail the functioning of the I^{2}C bus. Basically, the I^{2}C bus is a two-wire bidirectional system consisting of a clock and a serial data stream. The write cycle consists of 3 bytes of data and 3 acknowledge bits. The first byte is the Chip Address, the second the Sub-address to identify the location in the memory, and the third byte is the data. When the address' Read/Write bit is high, the second and third bytes are used to transmit status flags back to the MCU.

Figure 6 shows a block diagram of the MC44002/7 Bus Interface/Decoder. To begin with, the start bit is recognized by means of the data going low during CLK high. This causes the Counter and all the latches to be reset. For a write operation, the Write address ($88) is read into the Shift Register. If the correct address is identified, the Chip Address Latch is set and at CLK 9 an acknowledge is sent.

The second byte is now read into the Shift Register and is used to select the Sub-address. At CLK 18 a Sub-address Enable is sent to the memory to allow the Data in the register to be changed. Also, at CLK 18 another acknowledge is sent.

The third byte is now read into the Shift Register and the Data bussed into the memory. The Data in the Sub-address location already selected is then altered. A third acknowledge is sent at CLK 27 to complete the cycle.

A Read address ($89) indicates that the MCU wants to read the MC44002/7 status flags. In this instance, the Read/Write Latch is set, causing the Memory Enable and Subaddress Enable to be inhibited, and the flags to be written onto the data line. Two of the status flags are permanently wired one-high and one-low (O.K. and Fault), to provide a check on the communication medium between the MC44002/7 and the MCU.

At start-up the Counter is automatically reset and the Data for each Sub-address is read in from the MCU. Only after the entire memory contents have been transmitted, is Data 00 sent to register 00 to start the Horizontal Drive.

The MC44002/7 needs the full 27 clock cycles, or a stop condition, to properly release the I^{2}C bus.

Figure 6. I^{2}C Bus Interface and Decoder

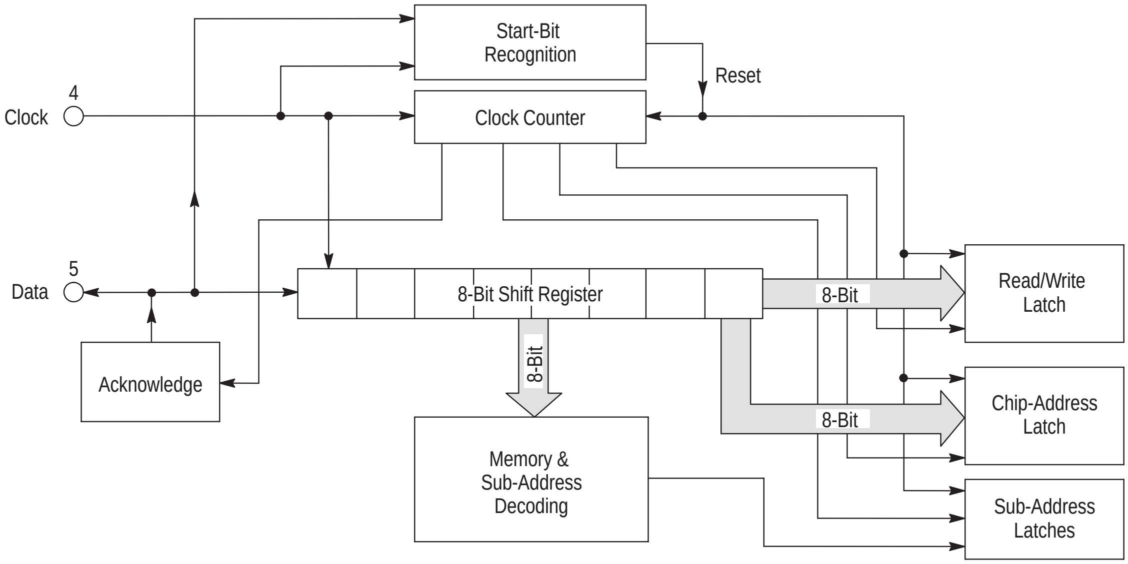
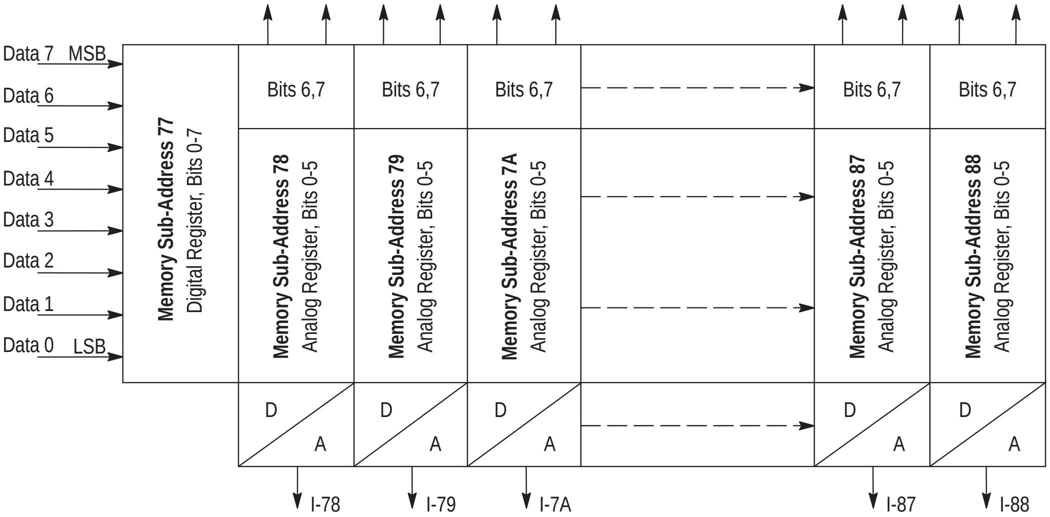


Figure 7. MC44002/7 Memory Map



Memory

Figure 7 shows a diagram of the MC44002/7 Memory Map. It has 18 bytes of memory which are located at hex sub-addresses 77 to 88. Sub-address 77 is used to set up the vertical timebase mode of the IC and for S-VHS switching, and consists of 8 separate data bits. The remaining 17 bytes use the least significant 6-bits as an analog control register. The contents of each are D/A converted, providing an analog control current which is distributed to the appropriate part of the circuit. Bits 6 and 7 are used singularly for switching control functions.

Chroma Decoder

The main function of this section is to decode the incoming composite video, which may be in any of the PAL, NTSC or SECAM (MC44002 only) Standards, and to retrieve the luminance and color difference signals. In addition, the signal filtering and luma delay line functions are carried out in this section by means of sampled data filters.

The entire decoder section operates in sampled data mode using clocks generated by external crystals. The oscillator, which is phase-locked in the usual way for PAL/NTSC modes, provides the clock function for the whole circuit. The crystals are selected by the MCU by means of a control bit (XS). Only crystals appropriate to the standards which are going to be received need to be fitted. A 17.7 MHz crystal (4x PAL subcarrier) is used for PAL and SECAM systems (50 Hz, 625 lines); and 14.3 MHz (4x NTSC subcarrier) for the NTSC system (60 Hz, 525 lines). Nearly all the filters, together with the luma delay line and peaking, have been integrated, requiring no external components or any adjustment. The filter characteristics are entirely determined by the clocks and by capacitor ratios, and are thus completely independent of variations in the manufacturing process. The PAL/NTSC subcarrier PLL and ACC loop filters have not been integrated in order to facilitate testing. These filters consist of fixed external components.

Figure 8 is a block diagram of the main features of the chroma decoder. Selection is first made between the Video 1 and Video 2 inputs. These may be either normal composite video or separate luma and chroma which may enter the IC at either pin. Commands from the MCU are used to route the signals through the appropriate delay and filter sections.

In PAL/NTSC, a variable low pass filter, which can be software bypassed (control bit T3), is then used to compensate for IF filtering and the Q of the external sound traps. Filter response is controlled by means of control bits T1 and T2. It is not recommended to use this filter in SECAM or in S–VHS, as luma–chroma delays will not be optimized. Next, the video enters the luma path. The PAL/NTSC or SECAM chroma signals are separated out by transversal high pass filters. In SECAM mode, the chroma trap frequency is dynamically steered to follow the instantaneous frequency of the chroma.

Then, another transversal filter provides luma peaking, which is also active in S–VHS mode. The high frequency luma may be peaked (at about 3.0 MHz with the 17.7 MHz crystal, and 2.4 MHz with the 14.3 MHz crystal) in 7 steps up to a maximum of 8.5 dB, by a control word from the MCU.

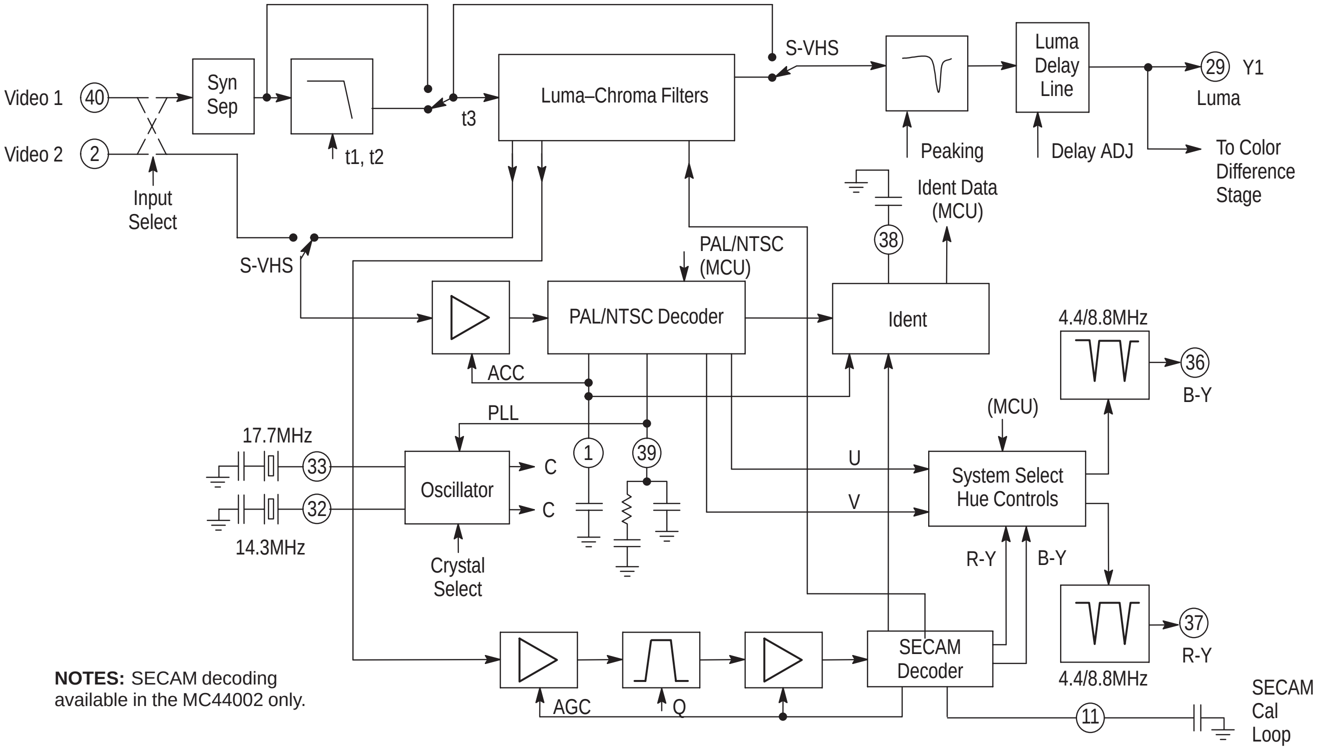
Another control word is used to trim the delay in the luma channel. Five steps of 56 ns (70 ns with the 14.3 MHz crystal) are possible, giving a total programmable delay of 280 ns. Steps 6 and 7 are used in S–VHS mode. The resulting processed luma signal then proceeds to the color difference section after being low–pass filtered by an active filter to remove components of the crystal frequency, and twice that frequency. The luma component (Y1) is made available at Pin 29 for use with auxiliary external functions, as well as testing.

When in the S–VHS mode, the S–VHS control bit controls the signal paths. The luma signal bypasses the first section of the luma channel, which contains the chroma trap. The S–VHS chroma is passed directly to the PAL/NTSC decoder without further filtering.

As all the delay and filter responses are determined by the crystal, they automatically commute to the new standard when the crystal is changed over. Thus, when the 14.3 MHz clock is being used, the chroma trap moves to 3.58 MHz.

The filtered PAL/NTSC and SECAM chroma signals are decoded by their respective circuits. The PAL/NTSC decoder employs a conventional design, using ACC action for gain control and the common double balanced multipliers to retrieve the color difference signals. The SECAM decoder is discussed in a separate subsection.

Figure 8. Chroma Decoder



NOTES: SECAM decoding available in the MC44002 only.

The actual decision as to a signal's identity is made by the MCU based on data provided by 3 flags returned to it, namely: ACC Active, PAL Identified, and SECAM Identified.

Control bits SSA–SSD must be sent to set the decoder to the correct standard.

This allows a maximum of flexibility, since the software may be written to accommodate many different sets of circumstances. For example, channel information could be taken into account if certain channels always carry signals in the same standard. Alternatively, if one standard is never going to be received, the software can be adapted to this circumstance. If none of the flags are on, color killing can be implemented by the MCU. This occurs if the net Ident Signal is too low, or if the ACC circuit is inactive due to too low a signal level.

The demodulated color difference signals now enter the Hue control section, where selection is made between PAL/NTSC and SECAM outputs. The Hue control is simply realized by altering the amplitudes of both color difference signals together. Hue control is only a requirement in NTSC mode and would not normally be used for other standards. The function is usually carried out prior to demodulation of the chroma by shifting the phase of the subcarrier reference, causing decoding to take place along different axes. In the MC44002/7, Hue control is performed on the already demodulated color difference signals. A proportion of the R-Y signal is added or subtracted to the B-Y signal and vice-versa. This has the same effect as altering the reference phase. If desired, the MC44002/7 can apply the Hue control to simple PAL signals.

After manipulation by the Saturation and Hue controls, the color difference signals are finally filtered to reduce any remaining subcarrier and multiplier products. Before leaving the chip at Pins 36 and 37, the signals are blanked during line and frame intervals. The 64 µs chroma delay line is carried out by a companion device, the MC44140.

SECAM Decoder (MC44002 only)

The SECAM signal from the high-pass filter enters tightly controlled AGC amplifiers wrapped around a cloche filter which is a sampled recursive type, with the AGC derived from a signal squarer. Next, the signal is blanked during the calibration gate period and a reference 4.43 MHz is inserted during this time. The SECAM signal is then passed through a limiter.

The frequency demodulator function is carried out by a frequency-locked-loop (F.L.L.). This consists of three components: a tracking filter, a phase detector and a loop filter. The center frequency of the tracking filter depends on three factors: internal R-C product, ADJUST voltage, and TUNING voltage. The tracking filter is dynamically tuned by the TUNING feedback from the loop-filter forming the F.L.L. The ADJUST control calibrates the F.L.L. and compensates for variations in the R-C product. After the F.L.L., the color difference signals are passed to another block where several functions are carried out. The signals are de-emphasized and outputs are provided to the Ident section. Another function of this section is to generate the I_{COMP} signal used for calibrating the F.L.L. This signal is blanked during the H-IG period to ensure that (R-Y) and (B-Y) output signals have a clean dc level for clamping purposes.

In addition, components are added to compensate for the R-C product, and tuning offsets are introduced during the active lines for F0R/F0B.

Calibration of the F.L.L. takes place during every field blanking interval, starting from field retrace and ending just before the SECAM vertical Ident sequence (bottles). The calibration current I_{CAL} is derived from I_{COMP} during the calibration gate (CAL) and integrated by an external capacitor on Pin 11. The resulting voltage V_{EXT} is then transformed to generate the ADJUST control voltage removing from the loop range most of the variations due to internal RC products and temperature.

Color Difference Stages

This stage accepts luminance and color difference signals, together with external R,G,B and Fast Commutation inputs and carries out various functions on them, including clamping, blanking, switching and matrixing. The outputs, consisting of processed R,G,B signals, are then passed to the Auto Gray Scale section.

A block diagram of this stage is shown in Figure 10. The Y2, R-Y, B-Y together with R, G and B are all external inputs to the chip. The Y1 signal comes from the decoder section. Each of the signals is back-porch clamped and then blanked. The Y2 and R,G,B inputs have their own simple sync separators, the output from which may be used as the primary synchronization for the chip by means of commands from the MCU.

The Fast Commutation is an active high input used to drive a high speed switch; for switching between the Y and color difference inputs and the R,G,B (text) inputs.

After blanking, the Y1 and Y2 channels go to the Luma Selector which is controlled by means of 2 bits from the MCU. From here the selected luma signal goes to the RGB matrix. The two color difference signals pass through the saturation control. From here they go to a matrix in which G-Y is generated from the R-Y and B-Y, and lastly, to another matrix where Y is added to the three color difference signals to derive R,G,B.

Control bits (via the I^2C bus) allow the matrix coefficients to be adjusted in order to suit different requirements, particularly in NTSC. Table 1 shows the theoretical demodulation angles and amplitudes and the corresponding matrix coefficient values for each of the 4 selectable modes. (The A mode corresponds to the standard PAL/SECAM/NTSC mode). Although primarily intended for NTSC, this feature can also act on PAL/SECAM or external RGB signals.

The R,G,B inputs may take one of two different paths. They may either go straight to the output without further processing, or via a separate matrix and the saturation control. The path taken is controlled in software. When the latter route is selected, the R,G,B signals undergo a matrix operation to derive Y. From this, R-Y and B-Y are easily derived by subtraction from R and B; the derived color difference signals are then subjected to saturation control. This extra circuitry allows another feature to be added to the TV set, namely the ability to adjust the color saturation of the RGB inputs. After the saturation control the derived signals are processed as before.

Table 1. Matrix Modes Coefficients

	A	B	C	C
RR	1.0	1.577	1.539	1.556
RB	0	–0.156	–0.248	–0.251
GR	–0.513	–0.443	–0.462	–0.504
GB	–0.187	–0.168	–0.150	–0.125
BB	1.0	1.0	1.0	1.0
BR	0	0	0	0
Rm	0.562	0.9	0.9	0.91
Gm	0.344	0.3	0.3	0.31
Ra	90	100	106	106
Ga	237	236	240	246

NOTE: BB = Gain of $(B_{out}/(B–Y)_{in})$ = 1 (reference). BR = Gain of $(B_{out}/(R–Y)_{in})$ = 0 (theoretically).

Figure 9. SECAM Decoder (MC44002 only)

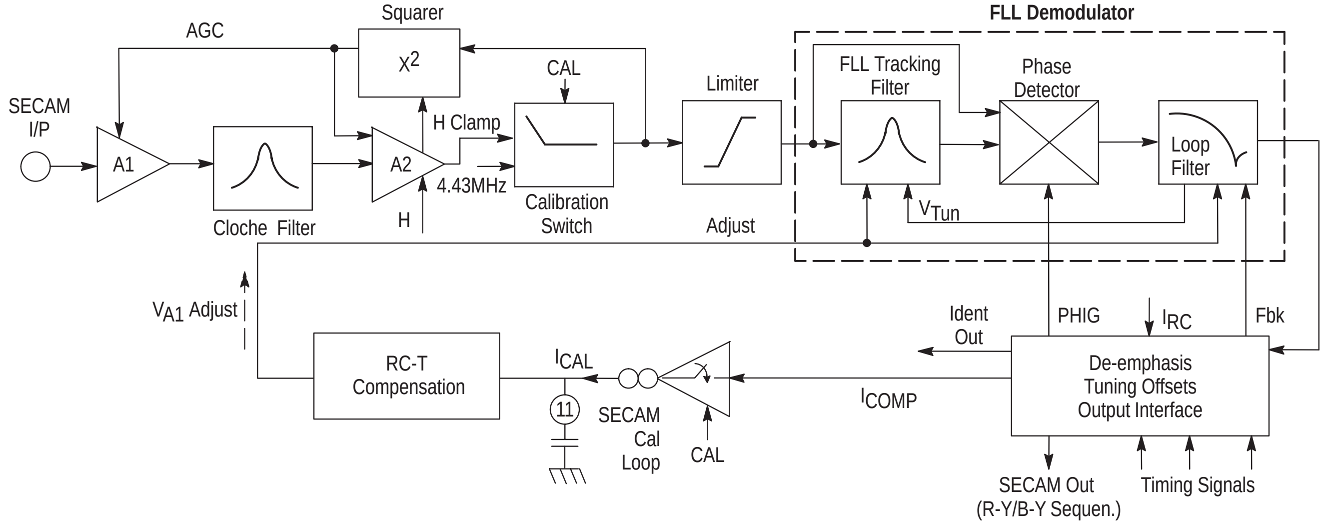
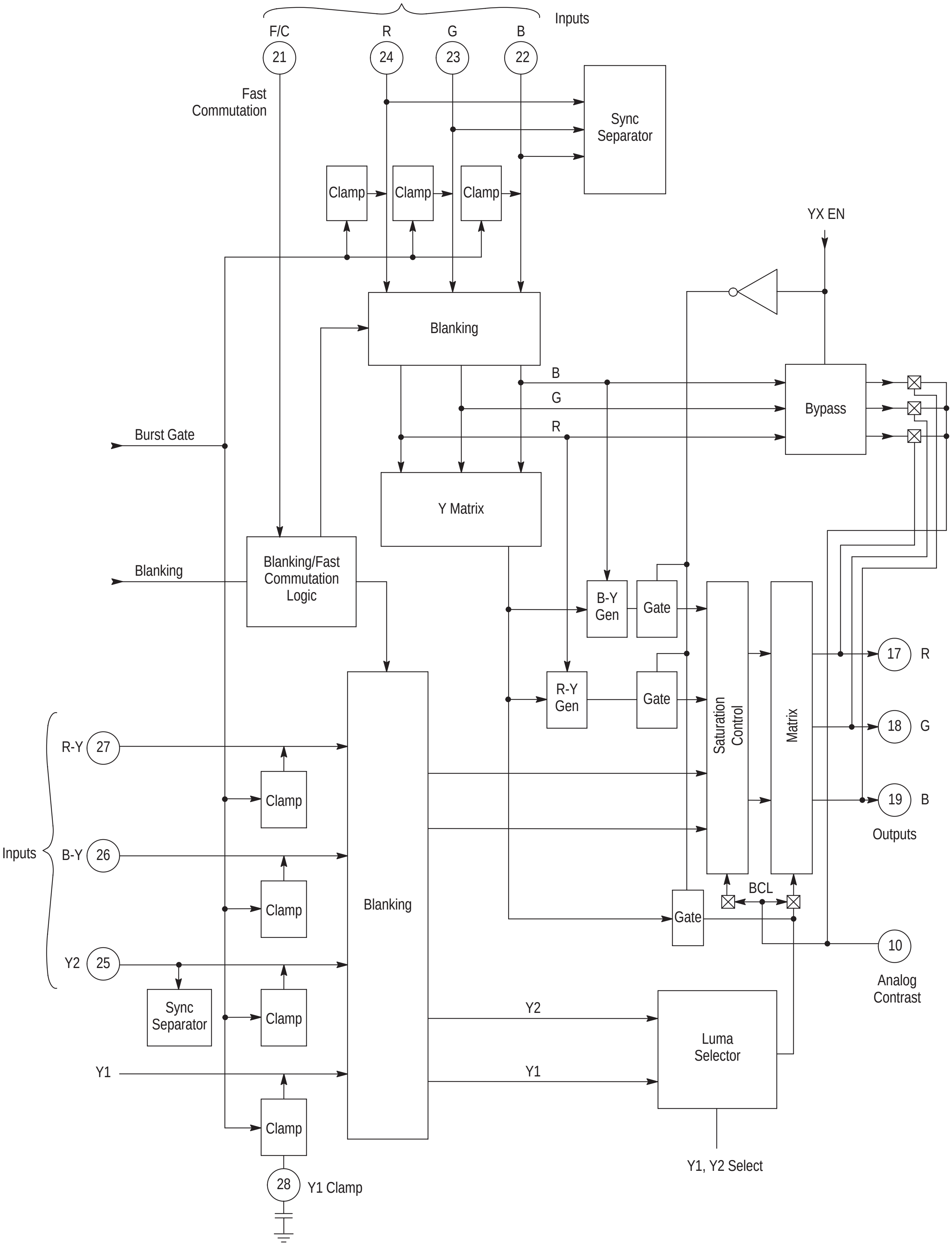


Figure 10. Color Difference Stages



In order to implement automatic beam current limiting (BCL), the possibility of fast contrast reduction has been added. For normal operation, the Contrast control is achieved by auto grey scale output loops and is I^2C bus controlled (see Section 4). In the case of excess beam current, this control is not fast enough to protect the tube and power supply stages. It is now possible, by acting on the Pin 10 voltage, to reduce the contrast about 12 dB by reducing the luma gain and saturation. In the case of direct RGB mode, the RGB gains are also reduced.

Figure 11. Typical Contrast Reduction

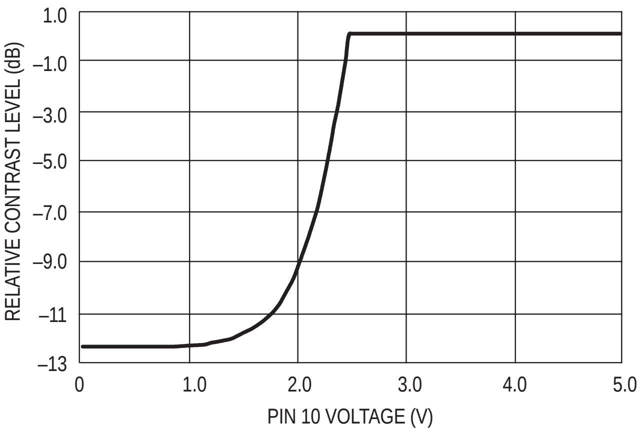
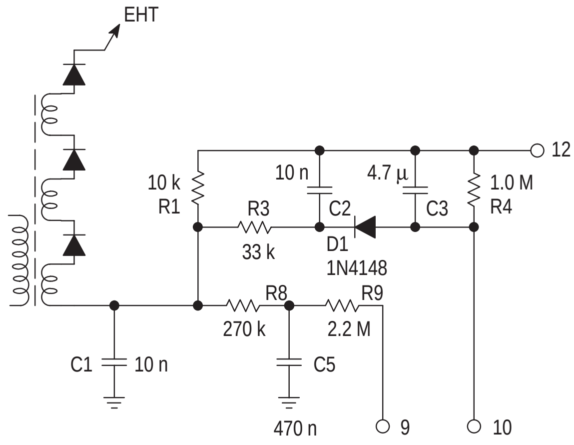


Figure 11 is showing the typical analog CONTRAST reduction possible as a function of the voltage on Pin 10. Two solutions are possible for obtaining the BCL function:

1st solution: A measure of the average and/or peak beam current is applied to Pin 10, which causes a reduction of the RGB drive levels to the high voltage video amplifiers. In this case, no software control is required, but variations in color balance and saturation may be observed. A typical application is shown in Figure 12.

2nd solution: The beam current flags are read and acted on by the MCU, which reduces the I^2C bus CONTRAST control to maintain the average beam current below the desired level. In the case of rapid and extreme beam current changes (black to white picture at high contrast level), the circuit of Figure 12 may be used as a fast aging protection while the MCU is reducing the CONTRAST through I^2C bus. The average of this method is to make any color balance/saturation variation only transient.

Figure 12. Automatic Beam Current Limiter Application

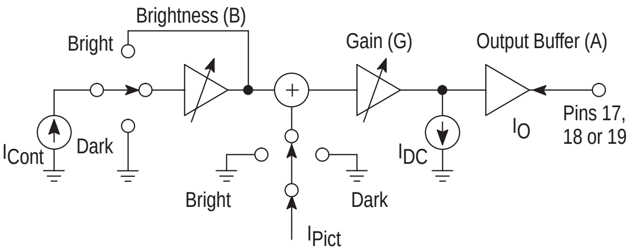


Auto Gray Scale Control Loops

This section supplies current drives to the RGB cathode amplifiers and receives a signal feedback from them, proportional to the combined cathode currents. The current feedback is used to establish a set of feedback loops to control the dc level of the cathode voltage (cut–off), and gain of the signal at the cathode (white balance). There are three loops to control the dark currents dark loops and another three to control the gains bright loops. The system uses 3 lines at the end of the vertical suppression period and just before the beginning of the picture for sampling the cathode current (i.e., one line for red, one for green and one for blue). The first half of reach line is used for adjusting the gain of the channel and is usually called the “bright” adjustment period. The second half of the line is used for adjusting the dc level of the channel and is called the “dark” adjustment.

The theoretical circuit diagram for one channel is shown in Figure 13 along with the basic equations. The dc level (Idc) and gain (G) are both controlled by 7 bit DACs which receive data directly from latches in which the required values are stored between sampling periods.

Figure 13. Bright/Dark Current Control



Picture Output Current: $I_{O(Pict)} = A \times [\, I_{DC} = G \times ((B \times I_{Cont}) + I_{Pict})]$
Dark Sample Output Current: $I_{O(dk)} = A \times I_{DC}$
Bright Sample Output Current: $I_{O(br)} = I_{O(dk)} - A \times G \times I_{Cont}$
Black Level Output Current: $I_{O(bk)} = I_{O(dk)} - B \times A \times G \times I_{Cont}$
$= I_{O(dk)} \times B \times [I_{O(dk)} - I_{O(br)}]$

A block diagram of the complete system is illustrated in Figure 16. Data words from the MCU which represent the RGB color temperatures selected at the factory, are stored in Latches 1,2,3 and D/A converted by DAC1,2,3 to reference currents. During the bright adjustment period, a reference current pulse, whose amplitude depends on the Contrast setting, is output to the cathode of the tube. The gain control is adjusted to bring the feedback current to the same value as the bright reference current, which is defined by the color intensity setting of the output considered. The currents must match each other. If not, a current will flow in resistor R producing an error voltage. This is then buffered into comparators Comp1, 2 and is compared with voltage references V_{ref1} and V_{ref2}. If the error voltage is greater than V_{ref1}, Comp1 causes the counter to count up. If the error voltage is less than V_{ref2}, Comp2 sends a count-down command. In this way, a “deadband” is set up to prevent the outputs from continuously changing. With the color intensity DAC set to about 32_d, the bright cathode current is 100 µA (10 times the dark current).

During Load the contents of the counter are loaded into Latch 6 (for red dc) and then D/A converted. The resulting dc current is then applied as an offset to the red output amplifier, completing the loop. During the dark adjustment period, the same intensity data is used but divided by a common factor (typically 10). A black level reference pulse is applied and the feedback loop adjusts the dc levels of the cathode to obtain a set of cathode currents equal to the dark reference currents

(10 μA). Therefore, the image color will always be adjusted to match the dark level color, i.e. grey scale tracking is ensured.

The Load/Backload sequencer is used to control which latch is being addressed at any given time by means of the timing signals input to it. The backload command sends the data from the appropriate latch to the Up/Down Counter, ready to be modified if necessary.

The Brightness control is affected by simply changing the dc pedestal of all three drives by the same amount, and does not form part of the feedback loop. The Contrast is adjusted to a set of values dependent on the level of the bright pulse applied during the set–up period. This level is set by a control word from the MCU. Once the loops have stabilized under normal working conditions, they may be deactivated by means of a control bit from the MCU. When, however, any change is made to either contrast or RGB intensity, the loops must be reactivated. For normal operation, it is not necessary to deactivate the bright loops.

Increasing the RGB intensity values will cause the Black–to–White cathode voltage amplitude to increase for a given Contrast setting. The White balance can therefore be set by adjusting the relative values of R, G and B intensity. An extra loop has been included via Latch 4 and DAC 4, which operates during the field flyback time to compensate for offsets within the loop. This has the effect of counteracting any input offset from the Buffer/Amp and will also compensate for cathode leakage should this be needed.

A second output of the reference currents from the RGB DACs are used to compare with preset limits, to ensure that the loops are working within their range of control. Should the limits be exceeded in either direction, flags are returned to the MCU to request that the G2 control be adjusted up or down as appropriate. Once set–up, the servo loops maintain the same conditions throughout the life of the TV.

Horizontal Timebase

The horizontal timebase consists of a PLL which locks up to the incoming horizontal sync, and a phase detector and shifter whose purpose is to maintain the H-Drive in phase with the line flyback pulse.

Because of on-chip component tolerances, the free-running oscillator frequency cannot be set more accurately than ± 40%; this range would be too much for the line output stage to cope with. For this reason the free-running frequency is calibrated periodically by other means. During startup and whenever there is a channel change, the phase detector is disconnected from the VCO for 2 lines during the blanking interval. A block diagram of the line timebase is given in Figure 14. The calibration loop consists of a frequency comparator driving an Up/Down Counter. The count is D/A converted to give a dc bias which is used to correct a 1.0 MHz VCO. The 1.0 MHz is divided by 64 to give line frequency and this is returned to the frequency comparator. This compares Fh from the VCO with a reference derived from dividing down the subcarrier frequency. Any difference in frequency will result in an output from the comparator, causing the counter to count up or down; and thus closing the loop. Since the horizontal oscillator is quite stable, this calibration does not need to be carried out very often. After switch–on, the calibration loop need only be enabled when the timebase goes out of lock.

A Coincidence Detector looks at the PLL Fh and compares it with the incoming H-sync. If they are not in lock, a flag is returned to the MCU. To allow for use with VCRs, the gain of the phase detector may be switched by means of commands from the MCU (bits HGAIN1 and HGAIN2). The gain of the phase detector is switched to the maximum value at the end of the vertical sync pulse and then reduced to the selected value after about 11 lines. This allows the horizontal timebase to rapidly compensate any horizontal phase jump (e.g. with a VCR) during the vertical blanking period, thus avoiding bending at the top of the picture.

Twice line frequency is output from the PLL which may be divided by either 1 or 2 depending on the command of the MCU. The x2 Fh will be used with Feature Boxes. The phase of the Fh and flyback pulses are compared in a phase detector, whose output drives a phase shifter. A 6-bit control word and D/A converter are used to apply an offset to the phase detector giving a horizontal phase shift control.

The presence of the horizontal flyback pulse is detected; if it is missing a warning flag is sent back to the MCU which can take appropriate action.

Vertical Timebase

The vertical timebase consists of two sections; a digital section which includes a vertical sync separator and standard recognition; and an analog section which generates a vertical ramp which may be modified under MCU control to allow for geometrical adjustments. A parabola is also generated and may be used for pin-cushion (E-W) correction and width control (see Figure 15).

In the digital section, the MC44002/7 uses a video sync separator which works using feedback, such that the threshold level of a comparator (slice level) is always maintained at the center of the sync pulse. Sync from any of the auxiliary inputs may also be used. The composite sync is fed to a vertical sync separator, where vertical sync is derived. This consists of a comparator, up/down counter and decoder. The counter counts up when sync is high, and down when sync is low. The output of the decoder is compared with a threshold level, the threshold only being reached with a high count during the broad pulses in the field interval.

When “Auto Countdown” is selected, the vertical timebase in fact starts off in the “Injection Lock” mode. This means that the timebase locks immediately to the first signal received, in exactly the same way as an old type injection locked timebase. A coincidence detector looks for counts of the right number (525 e.g.), and causes a 4 bit counter to count up. When there are 8 consecutive coincidences, the vertical countdown is engaged, and the MSB of the counter is brought out to set the flag. Similarly, non–coincidence, which will occur if synchronizing pulses are missing or in the wrong place, or if there is noise on the signals, causes the counter to count down. When the count goes back to zero, after 8 noncoincidences, the timebase automatically reverts to “Injection Lock” mode.

If it is known that lock will be lost (e.g., channel change), it is possible to jump straight into Injection Lock mode and not have to wait for the 8 consecutive non-coincidences. In this way the new channel will be captured rapidly. Once locked on to the new channel, “auto countdown” is then reselected by the MCU.

Under some conditions such as some VCRs in Search mode, it is possible to get signals having an incorrect number of lines, meaning that the countdown flag will go off because of successive non-coincidences. In these circumstances, if “auto countdown” is selected, the timebase will automatically lock to the signal in the Injection Lock mode. The fact that the flag is effectively saying that the vertical timebase is out of lock need not be a cause for major concern, since the horizontal timebase will still be locked to the signal, and has its own flag – "Horizontal out of lock". The vertical countdown and horizontal lock flags both perform an independent test for the presence of a valid signal. A logical OR function can be performed on the two flags, such that if either are present then by definition a valid signal is present.

The vertical oscillator has end-stops set at two line-count decodes as given below:

50 x 625 / 740 = 42.2 Hz (min)
50 x 625 / 448 = 69.8 Hz (max)

These figures assume that the horizontal timebase is running at 15,625 Hz. When the vertical timebase is in Injection Lock mode, the line counter reset is inhibited so that it ignores any sync pulses before a count of 448 is reached. This prevents any possible attempted synchronization in the middle of the picture. If the count reaches 740 lines, then there is an automatic reset which effectively sets the lower frequency limit. The choice of these limits is a compromise between a wide window for rapid signal capture and a narrow window for good noise immunity.

It is also possible to run the timebase in 2.0 V mode as there are decodes for 100 Hz (2 x 50 Hz) operation with upper and lower limits in proportion. This is, of course, intended to be used in conjunction with field and frame memory stores. The similar decodes which would be necessary to allow 120 Hz (2 x 60 Hz) operation have not, for the present, been implemented. Finally, the timebase can be forced into a count of either 625 or 525 by commands from the MCU; in this mode the input signal, if present, is ignored completely. If there is no signal present save for noise, then this feature can be used to obtain a stable raster.

In the analog section, an adjustable current source is used to charge an external capacitor at Pin 6 to generate a vertical ramp. The amplitude of the ramp is varied according to the current source (Height), and is automatically adapted when the 525 standard is recognized by multiplying by 1.2. The Linearity control is achieved by squaring the ramp and either adding or subtracting a portion of it to the main linear current. In addition, a correction current, depending on the level of anode current, is applied in the sense of oppose a change of picture height with EHT (Breathing).

The final ramp with corrections added is then passed to a driver/amplifier and is output at Pin 7. The vertical ramp can be used to drive a separate vertical deflection power circuit with local feedback control. Vertical "S" Correction will then be made using fixed components within the feedback loop of the power op amp. The vertical position can be adjusted under MCU control – this is achieved by varying the dc output level at Pin 7. The vertical amplitude can be reduced to 75% of its original value (bit VDI) to make possible the display of a 16:9 picture on a 4:3 screen.

The reference ramp is squared to provide a pin-cushion correction parabola, developed across an external resistor at Pin 8. The parabola itself is squared, giving an independent fourth order term (Corner Correction) whose level can also be varied; this is then added as a further modifying term to the E-W output. This latter correction is used for obtaining good corner geometry with flat-square tubes. A variable dc current is added to the parabola to effect a width control. Using a suitable power amplifier and a diode-modulator in the line output stage, the parabola may be used for E-W correction and dynamic width control. A further control is provided to shift the center point of the parabola up and down the screen (Parabola Tilt).

All of the vertical and horizontal signals are adjustable via 6-bit words from the MCU, and stored in latches. The adjustment controls available are:

Vertical Amplitude/Linearity/Breathing Correction/Position
Parabola (E-W) Amplitude/Horizontal Amplitude/
Corner Correction, and Parabola Tilt

The Anode Current Sense at Pin 9 is also used as a beam current monitor. Two thresholds may be set, by the manufacturer, using external components. The first threshold sets a flag to the processor if beam current becomes excessive. The MCU could, e.g., reduce brightness and/or contrast to alleviate the condition. The second threshold sets a flag warning of an overload condition where the CRT phosphor could be damaged. If such a condition were to arise, the processor would be programmed to shut down the PSU.

The vertical blanking lines may be selected by means of a bit from the MCU for either the 525 or 625 standard. The interlace may also be suppressed again under the control of the processor (bits ICI, IFI).

Figure 14. Horizontal Timebase

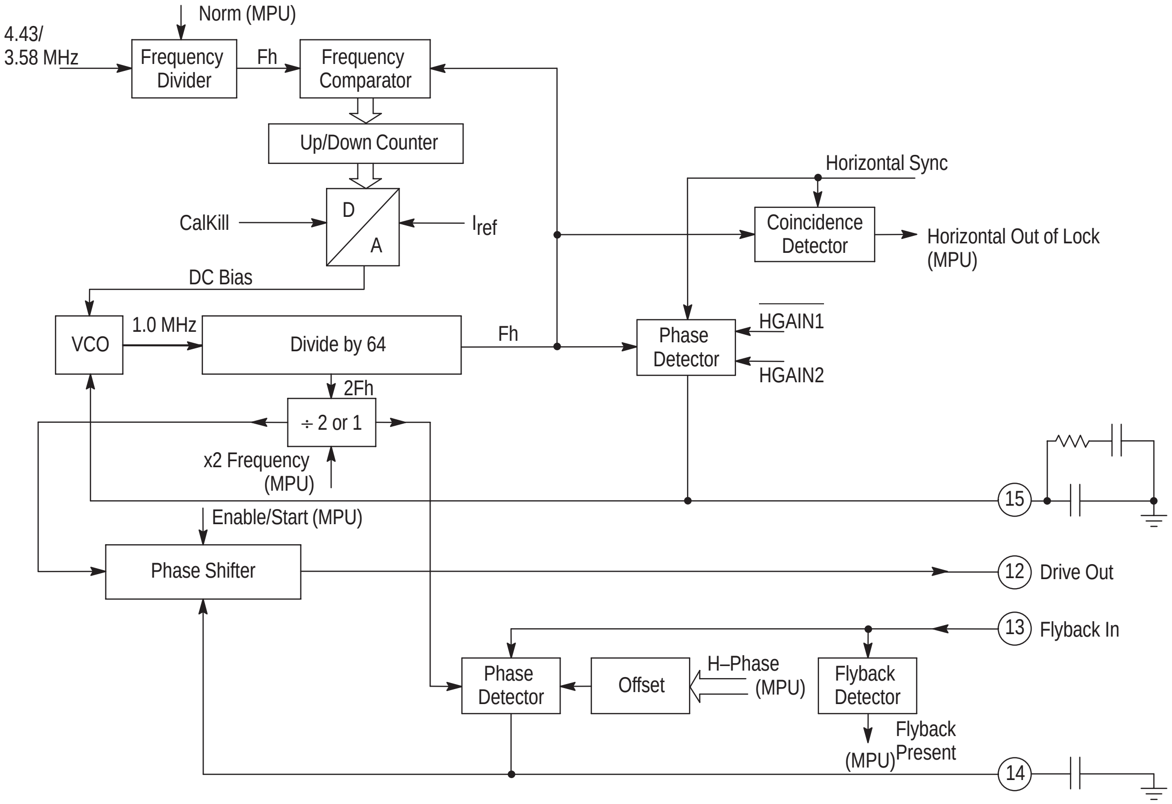


Figure 15. Vertical Timebase

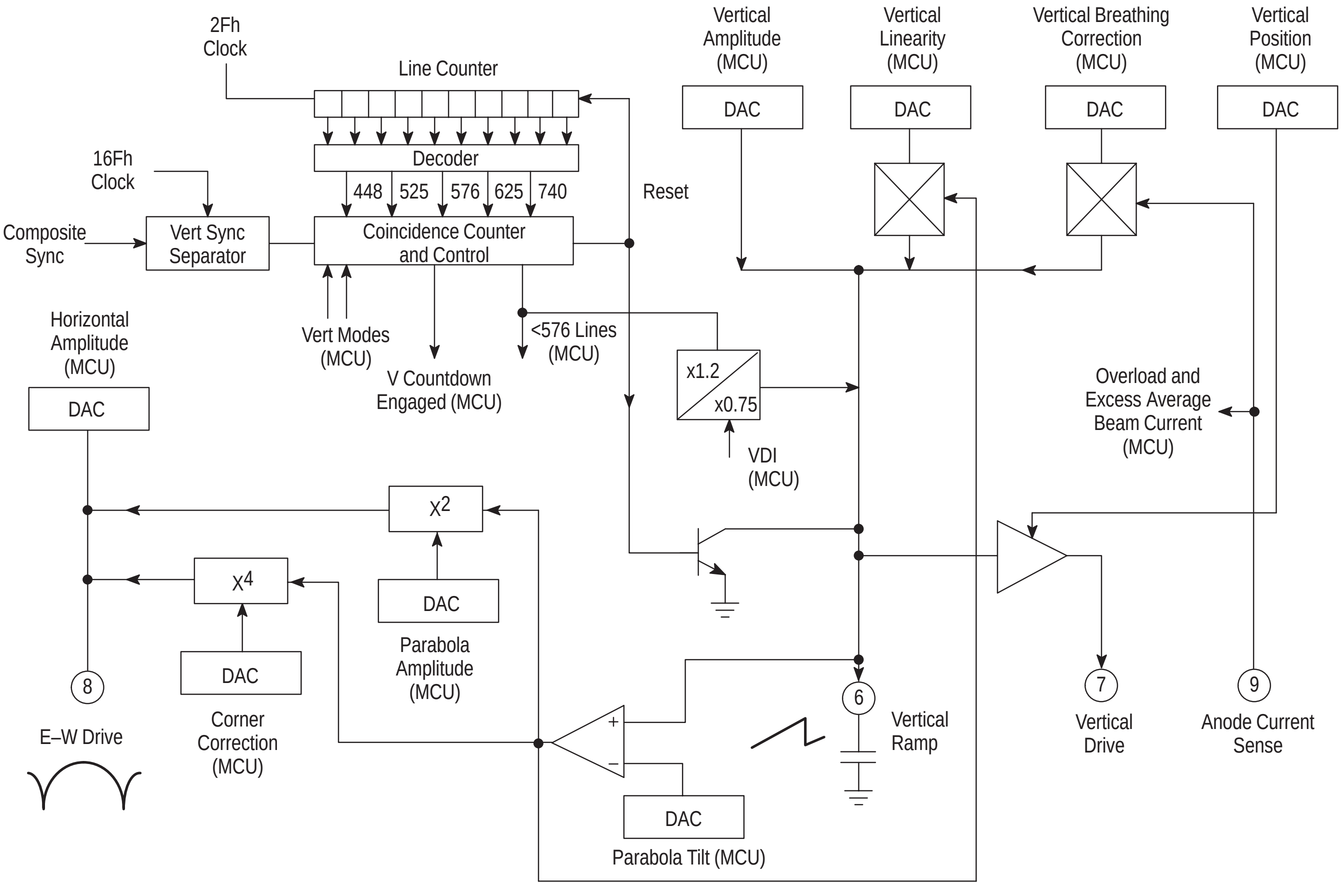
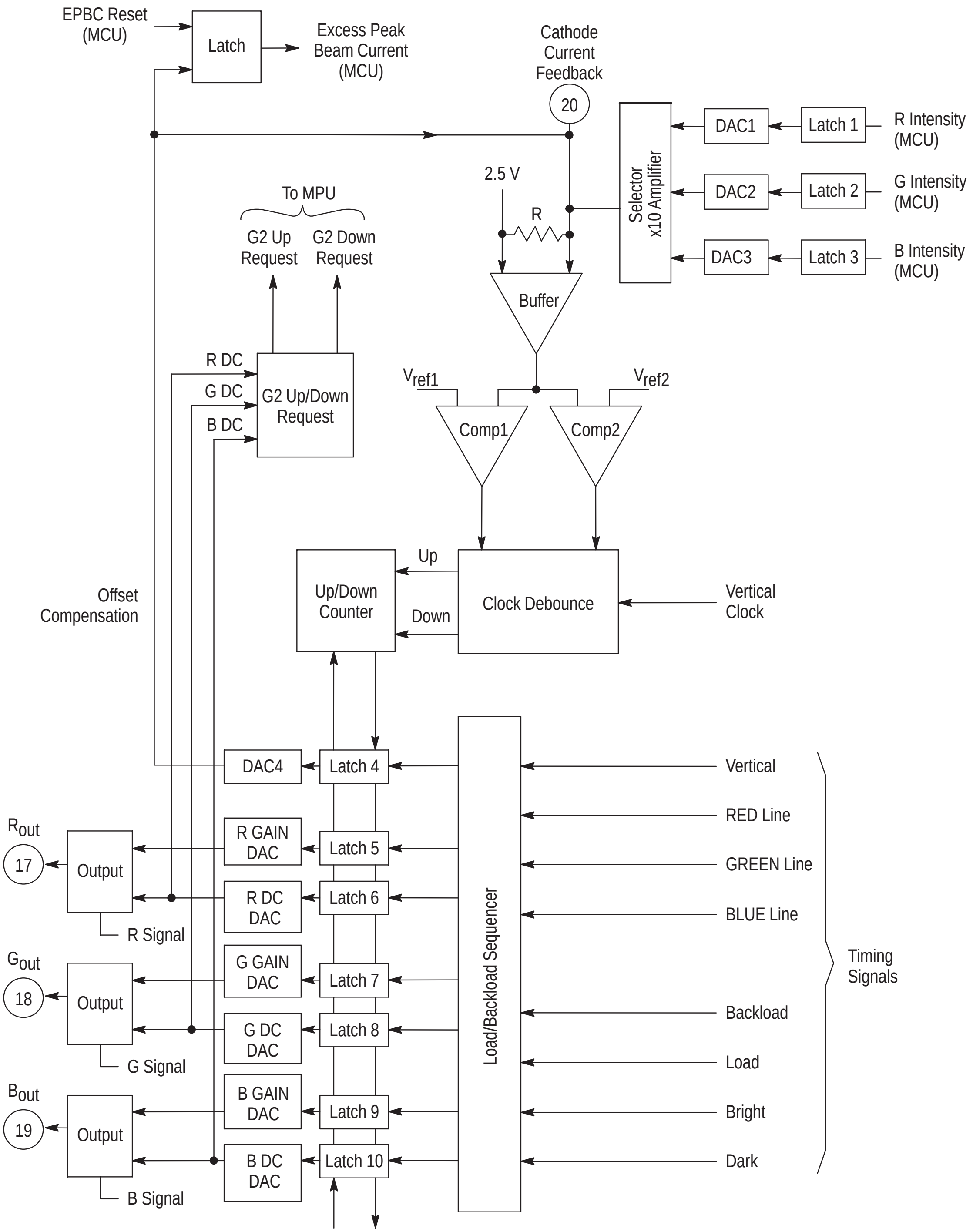


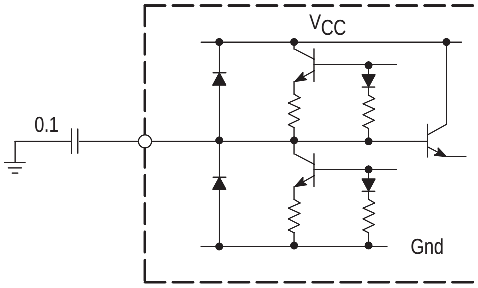
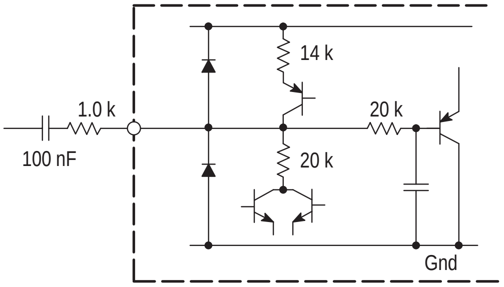
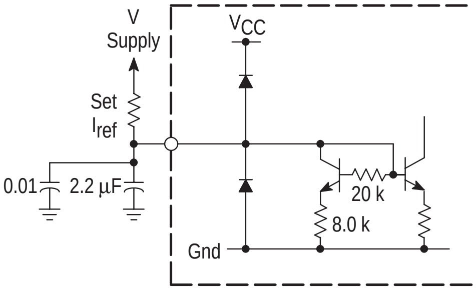
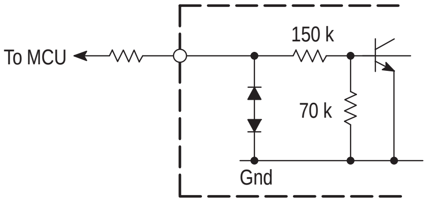
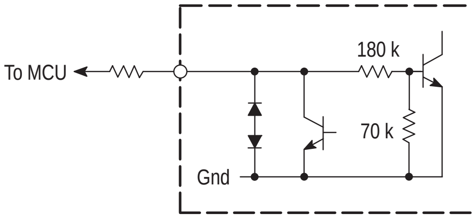
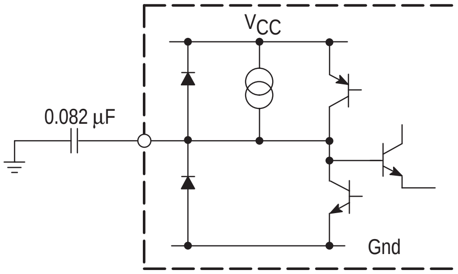
Figure 16. Auto Gray Scale Control Loops



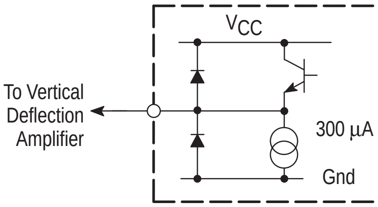
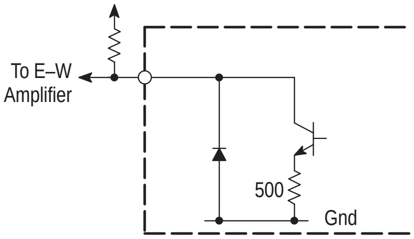
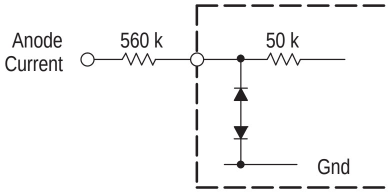
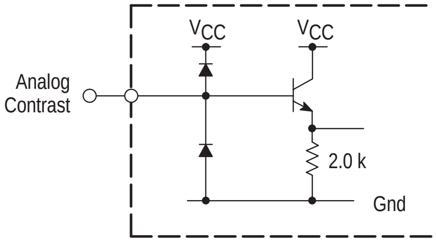
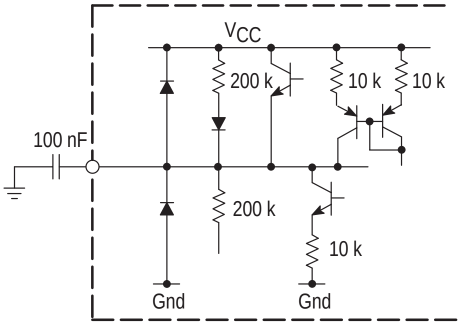
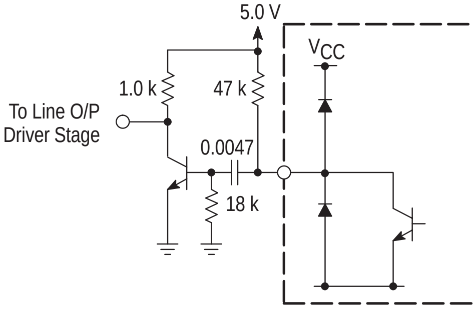
PIN FUNCTION AND EXTERNAL CIRCUIT REQUIREMENTS

The following section describes the purpose and function of each of the 40 pins on the MC44002/7. There is also an explanation of the external circuit component requirements for a practical application; a diagram of the small signal circuit will be found in Figure 17. One of the primary design aims for the MC44002/7 was to use the minimum number of external components, and where these are necessary, to employ low cost and easily obtainable standard types. Thus for example, as all the video signal filtering is carried out on the IC, there are no coils required whatsoever. The most common requirement is for ac coupling capacitors which are far too big to be integrated onto the chip. The time constants on certain pins are deliberately determined by external components to facilitate testing and for fine tuning the performance.

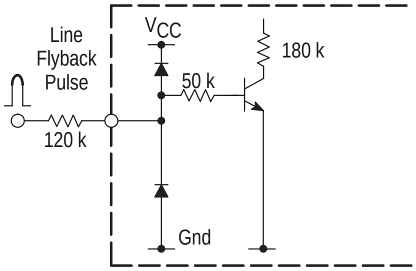
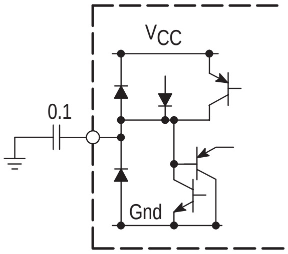
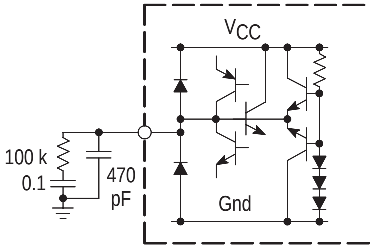
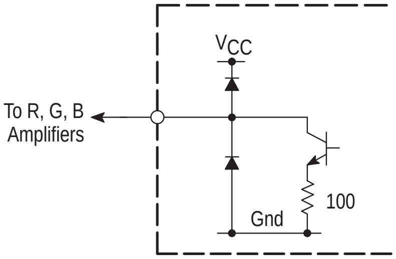
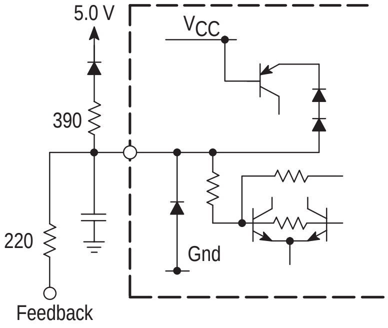
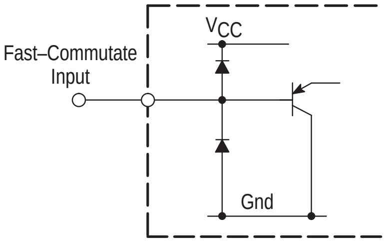
PIN FUNCTION DESCRIPTION

Pin	Equivalent Internal Circuit	Description
1		**ACC** External Filter used by ACC section. A single capacitor, that does not have a critical value, typically 0.01 µF, filters the feedback loop of the chroma automatic gain control amplifier.
2 40		**Video Input 1 (Pin 40) and 2 (Pin 2)** Video inputs (Pin 2 = Video 2; Pin 40 = Video1); Intended for a nominal 1.0 Vpp input level of composite video. Separate luma and chroma components may also be used with these input pins for S–VHS. The external circuit requirement is for a coupling capacitor of 0.01 µF and a series resistance not exceeding 1.0 kΩ. The input selection and adaptation for Y and C is carried out in software.
3		**Reference Current** Master reference current used throughout the IC. This is programmed by means of an external pull–up resistor, as on–board resistors are not sufficiently accurate. The designated current is 70 µA. This pin should be very well de–coupled to ground to avoid picking up interference from the nearby I^2C bus inputs. Nominal voltage at the pin is 1.3 V.
4		**I^2C Clock** I^2C bus clock input. This input can be taken straight into the IC, but in a real TV application it may be prudent to fit a series current limiting resistor near the pin in case of flash–over. A single pull–up resistor to 5.0 V is required. Although its value is associated with the µP, taking into account system capacitance at high data rates, a value of 4.7 kΩ, giving optimal performance, is recommended.
5		**I^2C Data** I^2C data input. Comments above for Pin 4 also apply to this pin.
6		**Vertical Ramp** A current is used to charge an external capacitor connected to this pin, developing a voltage sawtooth with a field period. The capacitor value determines the ramp amplitude. 82 nF is the more convenient value for symmetrical, linearity and parabola tilt adjustments.

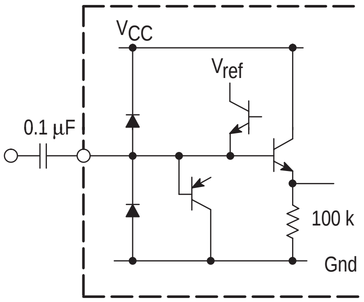
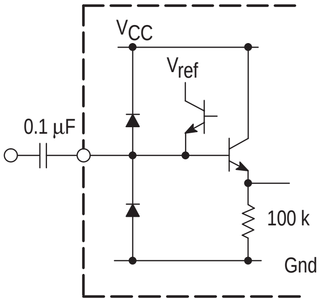
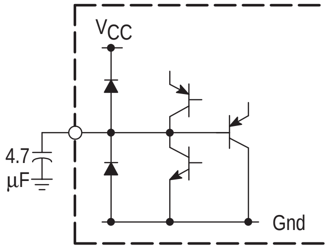
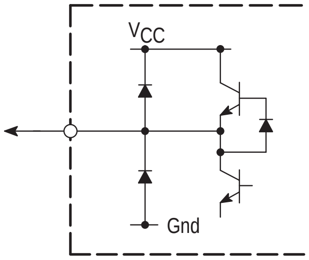
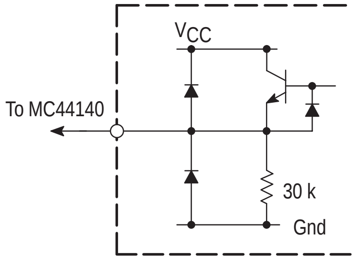
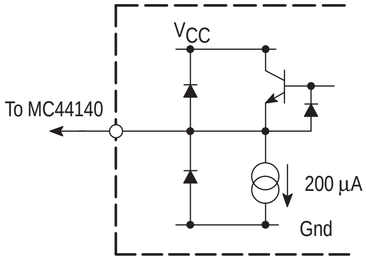
PIN FUNCTION DESCRIPTION (continued)

Pin	Equivalent Internal Circuit	Description
7		**Vertical Drive** The sawtooth derived on Pin 6 is used to drive an external power amplifier vertical output stage. The amplitude, linearity and position of the output ramp are adjustable via the MCU.
8		**Parabola (E–W) Drive** An inverted parabolic waveform derived by squaring the vertical ramp is used to drive an external power amplifier. In sets fitted with a diode modulator type line output stage, this provides width control and pin–cushion correction. The parabola is squared again to give a fourth order correction term required for flat square tubes. The E–W amplitude, dc level, tilt and corner correction are all adjustable by means of the MCU. This is a current output and may be used, for example, to drive the virtual ground of an external power amplifier
9		**Anode Current** Used as an anode current monitor whose purpose is to: (1) Provide E.H.T. compensation (anti–breathing) for the vertical ramp; and (2) provide warning of excessive and overload beam current conditions. The pin is connected via about 560 kΩ series resistor to the bottom of the E.H.T. overwinding. Therefore, increasing beam current will pull the voltage on this pin more negative. This change is sensed within the chip and used to apply a correction to the ramp and parabola amplitudes. With large beam currents, thresholds at $+V_{be}$ and $-2.0\ V_{be}$ set off warning flags to the MCU, which then has to take the appropriate action. The anode current levels at which these thresholds are reached are set up using fixed external resistors.
10		**Anode Contrast** This pin is used as an Analog Contrast monitor, allowing fast Beam Current Limiting (BCL). The fast BCL is controlled by Pin 10 voltage, which decreases with the contrast reduction (see typical curve). Above 2.5 V on the pin, the contrast remains maximum. Below 2.5, the contrast is reduced by about 12 dB, which is reached at about 1.0 V.
11		**SECAM Calibration Loop** This pin is used for the storage capacitor of the analog SECAM calibration loop (typically 100 nF). The capacitor is required regardless of whether or not SECAM will be decoded.
12		**Horizontal Drive Output** Horizontal drive pulses having an approximately even mark–to–space ratio emerge from this pin. This is an open–collector output which can sink up to 10 mA. However, taking this much current is not recommended since there is no separate ground pin available which may be connected near the line output stage; noise could be injected into the signal ground on the IC. Therefore, with a transformer driven line output stage, this output has been designed to be used with an extra external transistor inverter between the IC and the line driver. The transistor is open during the period when the line deflection transistor should be conducting.

PIN FUNCTION DESCRIPTION (continued)

Pin	Equivalent Internal Circuit	Description
13		**Horizontal Flyback Input** Flyback sensing input taken from the line output transformer. These pulses are used by the 2nd horizontal loop for H–Phase control. A positive going pulse from 0 to 5.0 V amplitude is needed for correct operation. The internal impedance of the pin is about 50 kΩ and an external attenuating series resistor of around 120 kΩ will also be needed.
14		**Horizontal Loop 2 Filter** Components at this pin filter the output of the phase detector in the 2nd horizontal loop. A simple external filter consisting of a 0.1 µF capacitor is required.
15		**Horizontal Loop 1 Filter** Horizontal PLL loop time constant. Components at this pin filter the output of the phase detector is in the 1st horizontal loop. The value of RC time constant is selected with external components to give a smooth recovery after the field interval disturbance and to ensure optimum performances in the presence of noise.
17 18 19		**RGB Outputs** The R, G and B drives are current rather than voltage due to the limited headroom available with the 5.0 V supply line. The outputs themselves consist of open–collector transistors and these are used to drive the virtual ground point of the high voltage cathode amplifiers
20		**Feedback** Current feedback sense derived from the video output amplifiers. The currents from all three guns are summed together as each is driven sequentially with know current pulses during the field interval. This feedback is then compared with internally set–up references. A low value ceramic capacitor to ground may be fitted close to this pin to help stabilize the control loops. A secondary function of this pin is for peak beam current limiting. When the feedback voltage during picture time becomes too great (i.e. too high beam current), a threshold at V_{CC} + 3.0 V_{be} is exceeded at which time a flag is sent to the MCU. The MCU then has to carry out the function of peak beam limiter by e.g. reducing contrast until the flag goes off. The threshold current is set externally with a fixed resistor value.
21		**Fast Commutate** A very fast active high switch (transition time 10 ns) used with text on the RGB inputs, for overlaying text on picture. This hardware switch may be enabled and disabled in software.

PIN FUNCTION DESCRIPTION (continued)

Pin	Equivalent Internal Circuit	Description
22 23 24		**RGB Inputs** These external input signals to the color difference stages are ac coupled into the IC via 0.1 µF capacitors. They have a clamp and sync separator. The inputs should be driven from a source of less than 1.0 kΩ output impedance with 700 mVpp signal levels.
25		**Y2 Input** Auxiliary external input to MC44002/7 which can be used in conjunction with auxiliary color difference inputs and/or as a sync input. The pin should be driven from a source of less than 1.0 kΩ output impedance with 700 mVpp luminance signal. The signal must be ac coupled via an external 0.1 µF coupling capacitor. Internal clamp and sync separator are provided.
26 27		**B–Y and R–Y Inputs** Corrected color difference inputs from the MC44140. The signals are ac coupled via 0.1 µF capacitors and are clamped internally. The inputs should be driven from a source of less than 1.0 kΩ output impedance.
28		**YI Clamp** External capacitor used by the circuit which clamps the Y1 signal output on Pin 29. A typical value is 4.7 µF.
29		**YI Output** The luminance, after passing through the filter and delay line/peaking sections, is made available on this pin. It is also routed internally to the color difference stages.
30		**System Select** A multilevel dc output controlled in software, which is used by the MC44140 for system selection. Please refer to separate functional description of the MC44140 chroma delay line.
31		**Sandcastle** A special multilevel timing pulse derived in the MC44002/7 for use by the MC44140. Please refer to separate function description of the MC44140 chroma delay line.

PIN FUNCTION DESCRIPTION (continued)

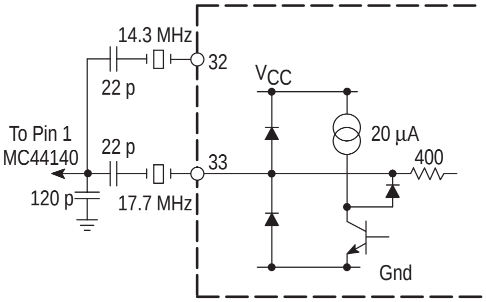
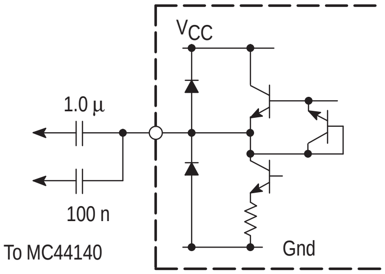
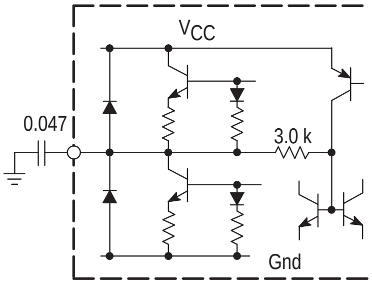
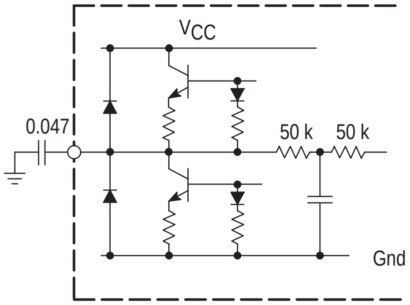
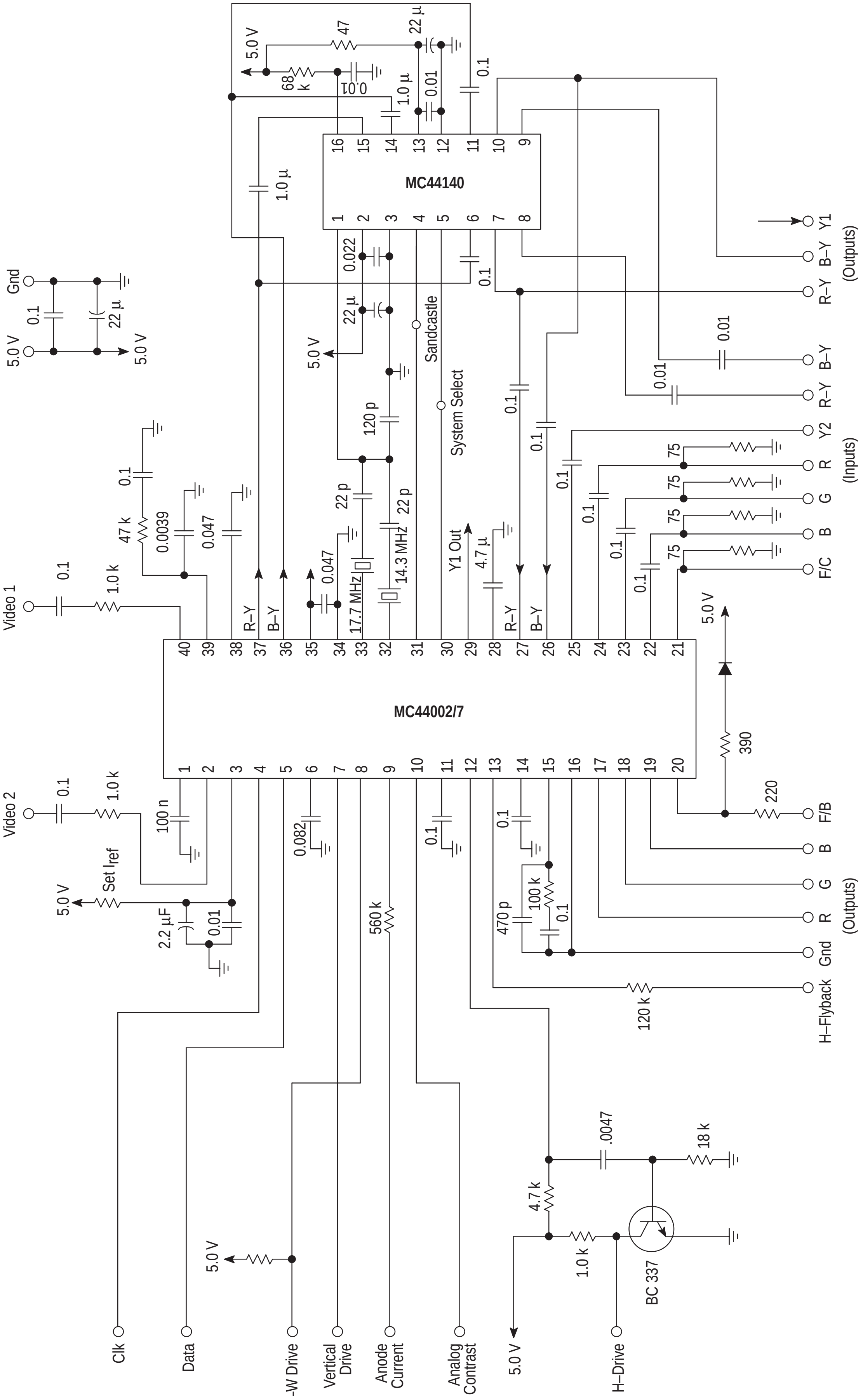
Pin	Equivalent Internal Circuit	Description
32 33		**Crystals (Respectively 14.3 MHz and 17.7 MHz)** Drive for externally fitted crystal clock reference for PAL, SECAM or NTSC. Four times F_{SC} is used. If the NTSC system is not going to be received, the 14.3 MHz crystal may be omitted. The crystal is parallel driven from a single pin and it requires a series load capacitance of appropriate value (usually 20 to 30 pF). Only crystals intended for VCO use should be fitted. The reference frequency is divided down in a capacitor chain to provide about 50 mV of clock reference for the MC44140. Positions for Pins 32 and 33 are selected by software.
34 35		**5.0 V Supply (35) and Ground (34)** Supply line, nominally 5.0 V, requiring about 120 mA. The actual voltage should be in the range of 4.75 to 5.25 V for usable results. It is recommended to decouple the supply line using a small ceramic capacitor mounted close to the supply and ground pins.
36 37		**B–Y and R–Y Outputs** Demodulated color difference outputs. These signals are ac coupled to the MC44140 for correction and delay with PAL and SECAM respectively. Signal level of about 1.4 Vpp may be expected on B–Y output when using a standard 75% color bars input video signal.
38		**Identification** External filter used by R–Y identification circuit. The filter normally consists of a single capacitor whose value is a compromise between rapid identification and noise rejection. Experience has shown that 0.047 µF is a suitable value.
39		**Oscillator Loop Filter** External time constant for chroma PLL. The crystal reference oscillator is phase locked to the incoming burst in PAL and NTSC. A low value ceramic capacitor, for good noise immunity, is normally placed in parallel with a much longer RC time constant. The PLL pull–in range is reduced when the time constant on the pin is made bigger, allowing this function to be optimized by the user.

Figure 17. Typical Application Circuit



SOFTWARE CONTROL FUNCTIONS

General Description

As already related in the circuit description, the MC44002/7 has a memory of 18 bytes. All, except Sub-address 77 and 7F, use the 6 least significant bits as an analog control register with D/A converters (64 steps) within the memory section. The remaining bits are controlled individually for switching numerous functions. Table 2 gives a listing of all the memory registers and control bits. An explanation of the function of the 16 DACs is given below.

Vertical Amplitude – Changes the amplitude of the vertical ramp available on Pin 7.

Vertical Breathing Correction – A correction is applied to the vertical ramp amplitude in a sense opposite to the picture expansion and contraction produced by changes in beam current. This register alters the sensitivity of the beam current sensing and hence the size of correction applied for a given change in beam current.

Parabola Amplitude – Changes the amplitude of the E-W output parabola developed across an external pull-up resistor at Pin 8.

Parabola Tilt – Shifts the point of inflection of the E-W parabola from side to side along the time axis. Also known as *keystone correction*.

Vertical Linearity – The vertical ramp is multiplied by itself to give a squared term, a part of which is either added or subtracted to the linear ramp as determined by this register.

Corner Correction – An independent 4th order term which is subtracted from the E-W parabola to achieve correct geometry with flat square tubes.

Horizontal Amplitude – A variable dc offset applied to the E-W output parabola on Pin 8.

Vertical Position – Adjust the dc level of the vertical ramp on Pin 7, allowing vertical centering control.

Horizontal Phase Control – Applies a variable phase offset to the horizontal drive pulse at Pin 15 providing for a picture centering control.

B, G, R Intensity – These controls set up the current reference pulses used when sampling the beam current during field interval. The data is fixed by the TV manufacturer when setting up the White balance and the CRT for correct Gray Scale tracking.

(All the above registers are for use during the test and setting up procedures; the remaining 4 registers are also user controls.)

Contrast – During bright sample time during the field interval, this control varies the level of the current pulses injected into the R,G,B channels, so altering the picture contrast.

Brightness – A variable current pedestal which is added to the three drives during active picture time.

Saturation – A variable gain control for the two color difference signals.

Hue – Achieved by mixing a portion of one color difference signal into the other.

Individually Adjustable Control Bits – These consist of bits 7 and 6 of registers 77 through 88, as well as bits 0 to 5 of register 77 and bits 0 to 3 of register 7F. Some of these are used individually to control single functions requiring just on/off switching; and some are arranged into 2 or 3-bit words (e.g., luma peaking). A list of control words and truth tables for these may be found in Table 3.

CA1, CB1 – Used to change the mode of operation of the vertical timebase to either injection lock or auto countdown, or to force it into 525 or 625 lines. Just prior to changing channel, the vertical timebase can be switched to injection lock mode and when a new channel is captured, the timebase is switched back to auto mode. In this way there is no delay in locking onto the new channel and hence no picture roll. If there is no valid signal being received, the display can be stabilized by forcing the timebase into 525 or 625 lines.

IC1, IF1 – These bits are used to suppress the field interlace, which can be scanned in the nearest even or odd half line.

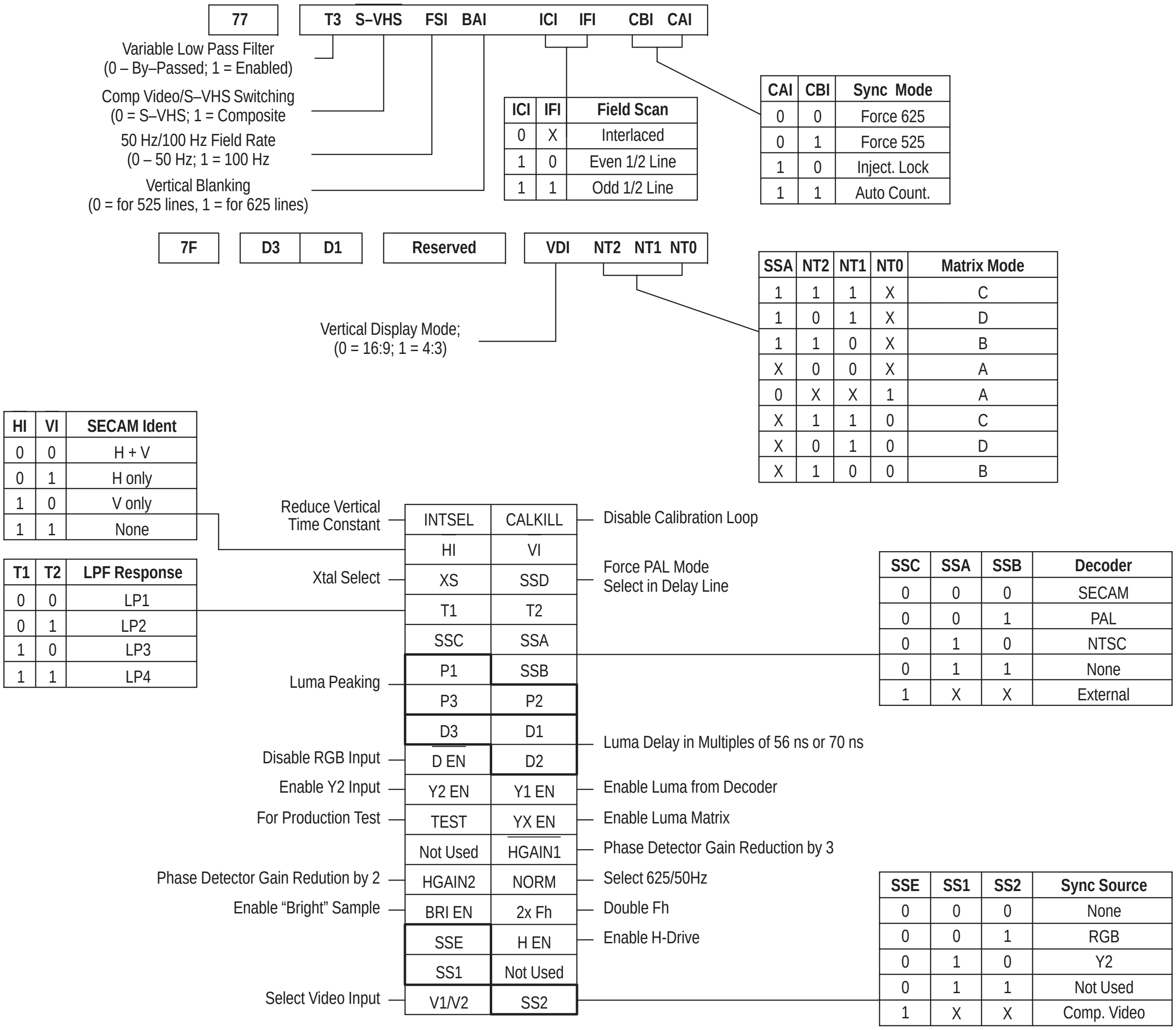
HI, VI – Selects the type of SECAM ident when operating in this mode. Either vertical ident bursts or horizontal ident can be selected individually, or ident can be taken from a combination of the two. In certain transmissions the vertical SECAM identification is not present (and sometimes replaced by other signals), so it is strongly recommended that only the horizontal identification be used. These bits must both be set to 1 when SECAM is not decoded (MC44002 and MC44007).

SSA, SSB, SSC – Used to set the color decoder and the dc level of the System Select output from the MC44002/7, Pin 30. This output is used by the MC44140 delay line in turn for changing between PAL, NTSC, SECAM and external modes of operation. In effect, the MC44140 is being controlled by the I^2C bus via the MC44002/7.

Table 2a. Register Memory Map

HEX Sub-address	MSB	Data Byte						LSB
77	T3	$\overline{\text{S-VHS}}$	FSI	BAI	ICI	IFI	CBI	CAI
78	INTSEL	CALKILL	Vertical Amplitude					
79	$\overline{\text{HI}}$	$\overline{\text{VI}}$	Vertical Breathing Correction					
7A	XS	SSD	Parabola Amplitude					
7B	T1	T2	Parabola Tilt					
7C	SSC	SSA	Vertical Linearity					
7D	P1	SSB	Corner Correction					
7E	P3	P2	Horizontal Amplitude					
7F	D3	D1	Reserved		VDI	NT2	NT1	NT0
80	$\overline{\text{D EN}}$	D2	Vertical Position					
81	Y2 EN	Y1 EN	Horizontal Phase Control					
82	$\overline{\text{TEST}}$	YX EN	Blue Intensity					
83	Not Used	$\overline{\text{HGAIN1}}$	Green Intensity					
84	HGAIN2	NORM	Red Intensity					
85	BRI EN	2x Fh	Contrast					
86	SSE	H EN	Brightness					
87	SS1	Not Used	Saturation					
88	V1/V2	SS2	Hue					
00		Dummy – If H EN, then starts H timebase						
FF		Dummy – Resets peak beam limit flag						

Table 2b. Register Memory Map



ICI	IFI	Field Scan
0	X	Interlaced
1	0	Even 1/2 Line
1	1	Odd 1/2 Line

CAI	CBI	Sync Mode
0	0	Force 625
0	1	Force 525
1	0	Inject. Lock
1	1	Auto Count.

SSA	NT2	NT1	NT0	Matrix Mode
1	1	1	X	C
1	0	1	X	D
1	1	0	X	B
X	0	0	X	A
0	X	X	1	A
X	1	1	0	C
X	0	1	0	D
X	1	0	0	B

HI	VI	SECAM Ident
0	0	H + V
0	1	H only
1	0	V only
1	1	None

T1	T2	LPF Response
0	0	LP1
0	1	LP2
1	0	LP3
1	1	LP4

SSC	SSA	SSB	Decoder
0	0	0	SECAM
0	0	1	PAL
0	1	0	NTSC
0	1	1	None
1	X	X	External

SSE	SS1	SS2	Sync Source
0	0	0	None
0	0	1	RGB
0	1	0	Y2
0	1	1	Not Used
1	X	X	Comp. Video

NOTES: SECAM decoding is selectable in the MC44002 only. $\overline{\text{HI}}$ and VI must be set to 1,1 in non–SECAM applications.

Table 3. Control Bit Truth Tables

CAI	CBI	Sync Mode
0	0	Force 625
0	1	Force 525
1	0	Injection Lock
1	1	Auto Countdown

ICI	IFI	Field Scan
0	X	Interlaced
1	0	Even Up 1/2 Line
1	1	Odd Up 1/2 Line

$\overline{\text{HI}}$	$\overline{\text{VI}}$	SECAM Ident
0	0	H + V
0	1	H only
1	0	V only
1	1	None

T1	T2	LPF Response
0	0	LP1
0	1	LP2
1	0	LP3
1	1	LP4

SSC	SSA	SSB	Color Diff. Source
0	0	0	SECAM
0	0	1	PAL
0	1	0	NTSC
0	1	1	None
1	X	X	External

SSE	SS1	SS2	Sync Source
0	0	0	None
0	0	1	RGB
0	1	0	Y2
0	1	1	Not Used
1	X	X	Comp. Video

P2	P1	P3	Luma Peak (dB) @ 3.0 MHz *
0	0	0	8.5
0	0	1	8.0
0	1	0	7.2
0	1	1	6.3
1	0	0	5.4
1	0	1	3.8
1	1	0	2.3
1	1	1	0.0

* Value shown for 17.7 MHz crystal.
Peak Frequency is ≈ 2.2 MHz when using 14.3 MHz crystal.

SSA	NT2	NT1	NT0	Matrix Mode
0	0	0	X	A
0	0	1	0	D
0	0	1	1	A
0	1	0	0	B
0	1	0	1	A
0	1	1	0	C
0	1	1	1	A
1	0	0	X	A
1	0	1	X	D
1	1	0	X	B
1	1	1	X	C

$\overline{\text{HGAIN1}}$	HGAIN2	H–Phase Detector Gain
0	0	Divide by 3 (Sync Window Enabled)
0	1	Divide by 6 (Sync Window Enabled)
1	0	High (Sync Window Disabled)
1	1	Divide by 2 (Sync Window Disabled)

D1	D2	D3	PAL (T3 = 1)	NTSC (T3 = 1)	SECAM (T3 = 0)	S–VHS (T3 = 0)
0	0	0	780 ns	940 ns	1050 ns	N/A
0	0	1	836 ns	1010 ns	1106 ns	N/A
0	1	0	892 ns	1080 ns	1162 ns	N/A
0	1	1	948 ns	1150 ns	1218 ns	N/A
1	0	0	1004 ns	1220 ns	1274 ns	N/A
1	0	1	1060 ns	1290 ns	1330 ns	N/A
1	1	0	N/A	N/A	N/A	480 ns
1	1	1	N/A	N/A	N/A	480 ns

SSE, SS1, SS2 – These 3 bits select the signal input from which the timebase synchronization is taken. The composite video input has a high quality sync separator which has been designed to cope with noise and interference on the video; the RGB and Y2 inputs have simple single sync separators which may also be used for synchronization.

T1, T2 – The bits are used to modify the response of the variable Low Pass Filter placed at the composite video inputs (for PAL/NTSC signals) in order to compensate for IF filtering and the Q of external sound traps.

P1, P2, P3 – These 3 bits are used to adjust the Luma peaking value. The amount of peaking indicated is with respect to the gain at the minimum peaking value (P1, P2, P3 = 111).

D1, D2, D3 – These 3 bits are used to adjust the Luma delay. The indicated delay is that from the video inputs (Pins 2 and 40) to the Y1 output. The amount of delay depends on the composite video standard used if S–VHS is selected.

NT0, NT1, NT2 – These 3 bits are used in conjunction with SSA for the selection of the matrix coefficients mode.

HGAIN1, HGAIN2 – These 2 bits are used to set the gain of the horizontal phase detector. The high gain position is used to acquire lock and for operation with a VCR. Setting HGAIN1 to 0 also enables a horizontal sync window. The low gain position is used for off–the–air signals.

The remaining control bits are used singularly and are listed as follows:

T3 – When high, this bit enables the variable Low Pass Filter at the video inputs. For optimum performance, T3 must be set to 0 in S–VHS and SECAM modes, and to 1 in PAL and NTSC. The filter response is set with bits T1, T2.

S-VHS – Set to 1 for normal composite video input to Pin 2 or 40. In this mode, the luma–chroma separator is active. Set to 0 for S–VHS (Y/C) operation at those pins. In this mode, luma is to be applied to the selected video input (with bit V1/V2), and chroma is to be applied to the other input. The luma–chroma separator is bypassed.

FSI – Selects either 50 Hz or 100 Hz field rate. When bit is low, 50 Hz operation is selected. No usable with NTSC.

BAI – This bit selects the number of blanked lines for either 525 or 625 line standards.

INTSEL – The vertical sync separator operates by starting a counter counting up at the beginning of each sync pulse, a field pulse being recognized only if the counter counts up to a sufficiently high value. The control bit INTSEL is used in taking the decision as to when a vertical sync pulse has been detected. When low, the pulse is detected after 36 µs; when high after 68 µs. This may find application with anti-copy techniques used with some VCRs, which rely on a modified or corrupted field sync to allow a TV with a short time constant to display a stable picture. However, a VCR having a longer time constant will be unable to lock to the vertical.

CALKILL – Enables or disables the horizontal calibration loop. The loop is normally enabled only during startup for some seconds and when there is no signal present. The loop may be disabled so long as the horizontal timebase is locked to an incoming signal.

XS – Is used to change between the two external crystal positions (Pins 32 and 33).

SSD – Forces system select to PAL level. Can be used to override SECAM mode in the delay line. When low, SECAM mode is enabled (MC44002 only).

VDI – Either 4:3 or 16:9 display mode can be chosen using this bit. When low, the 16:9 mode is enabled.

D EN – Enables or disables the RGB Fast Commutation switch for the RGB inputs. When low, RGB inputs are enabled.

Y1 EN – Switches Y1 through to the color difference stage.

Y2 EN – Switches Y2 through to the color difference stage.

Test – When bit is low, enables continuous sampling by the RGB output control loops throughout the entire field period. Used only for testing the IC.

YX EN – Enables the luma matrix allowing saturation control in the color difference stage.

Norm – Alters the division ratio for the reference frequency used by the horizontal calibration loop. Always used when changing between 14.3 MHz and 17.7 MHz crystals.

BRI EN – Used to switch on or off the “bright” sampling pulses used by the RGB output loops. This feature was originally introduced to prevent any backscatter from these three bright lines in the field interval from getting into the picture. Must be enabled when adjusting intensity Contrast or Red, Green and Blue.

2x Fh – Line drive output is either standard 15.625 kHz (15.750 kHz) or at double this rate.

H EN – Control bit enables horizontal drive pulse. This is normally done automatically after the values stored in the MCU nonvolatile memory have been read into the MC44002/7 memory.

V1/V2 – To select between Video Inputs 1 and 2.

Table 4. Control Bit Functions

Bits	Bit Low	Bit High
T3	Variable Input LPF By–Passed	Variable Input LPF Enabled
$\overline{\text{S–VHS}}$	S–VHS Mode Enabled	Composite Video Mode Enabled
FSI	50 Hz Field Rate Selected	100 Hz Field Rate Selected
BAI	Vertical Blanking for 525 Lines	Vertical Blanking for 625 Lines
INTSEL	Short Vertical Time–Constant	Long Vertical Time–Constant
CALKILL	H Calibration Loop Enabled	H Calibration Loop Disabled
XS	17.7 MHz Crystal (Pin 33) Selected	14.3 MHz Crystal (Pin 32) Selected
SSD	System Select Active	System Select Forced to PAL
$\overline{\text{D EN}}$	RGB Inputs Enabled	RGB Inputs Disabled
Y2 EN	External Luma Input Switched “Off”	External Luma Input Switched “On”
Y1 EN	Luma from Filters Switched “Off”	Luma from Filters Switched “On”
$\overline{\text{TEST}}$	Video Outputs Sampled Continuously	Video Outputs Sampled Once per Field
YX EN	Disable Luma Matrix (RGB Saturation Control)	Enable Luma Matrix (RGB Saturation Control)
$\overline{\text{HGAIN1}}$	H–Phase Detector Gain Division by 3 Enabled	H–Phase Detector Gain Division by 3 Disabled
HGAIN2	H–Phase Detector Gain Division by 2 Disabled	H–Phase Detector Gain Division by 2 Enabled
NORM	H–Reference Divider Ratio for 17.7 MHz Crystal	H–Reference Divider Ratio for 14.3 MHz Crystal
BRI EN	“Bright” Sample Switched “Off”	“Bright” Sample Switched “On”
2 x fH	H–Drive : 1 x fH	H–Drive : 2 x fH
H EN	H–Drive Enabled	H–Drive Disabled
VDI	16:9 Display Mode Enabled	4:3 Display Mode Enabled
V1/V2	Video Input 2 (Pin 2) Selected	Video Input 1 (Pin 40) Selected

FLAGS RETURNED BY THE MC44002/7

When the Address Read/Write bit is high the last two bytes of I^2C data are read by the MCU as status flags; a listing of these may be found in Table 5. The MC44002/7 is designed to be part of a closed-loop system with the MCU; these flags are the feedback mechanism which allow the MCU to interact with the MC44002/7.

A brief description of each of the flags, its significance and possible uses are given below.

Table 5. Flags Returned

Clock #	Flag (Bit High)
10	Horizontal Flyback Present
11	Horizontal Drive Enabled
12	Horizontal Out Of Lock
13	Excess Average Beam Current
14	Less Than 576 Lines
15	Vertical Countdown Engaged
16	Overload Average Beam Current
17	Reserved
18	(Acknowledge)
19	Grid 2 Voltage Up Request
20	Grid 2 Voltage Down Request
21	OK
22	Fault
23	ACC Active
24	PAL Identified
25	SECAM Identified (MC44002 only)
26	Excess Peak Beam Current
27	(Acknowledge)

Horizontal Flyback Present – A sense of the horizontal flyback is taken via a current limiting series resistor from one of the flyback transformer secondaries to Pin 13. This is used for the H-phase shift control, but the presence of the pulse is also flagged to the MCU. Should the flag be missing after the chassis has been started up, then the MCU would have to shut down the set immediately.

Horizontal Drive Enabled – Indicates that the horizontal drive pulse output at Pin 15 has been enabled. This occurs after the stored values in the nonvolatile memory have been transferred to the MC44002/7 memory.

Horizontal Out of Lock – This flag is high when no valid signal is being received by the MC44002/7. Possible action in this case would be to change the phase detector gain and time constant bits to ensure rapid capture and locking to a new signal.

Excess Average Beam Current – This is one of two threshold levels which are determined by an external component network connected to the beam current sensing at Pin 9. This flag indicates an excess of beam current. A typical application of this flag in conjunction with “Overload Average Beam Current” flag is for the software controlled Automatic Beam Current Limiting. When this flag is “on”, it is recommended that the software prevent increases to the Contrast setting.

Less Than 576 Lines – Output from the line counter in the vertical timebase. If there is a count of less than 576 this is indicative of a 525 line system being received. If the flag is low then a 625 line system is being received. This information can be used as part of an automatic system selection software.

Vertical Countdown Engaged – The vertical timebase is based on a countdown system. The timebase starts in Injection Lock mode and when vertical retrace is initiated a 4-bit counter is set to zero. A coincidence detector looks for counts of 625 lines. In Auto mode each coincidence causes the counter to count up. When eight consecutive coincidences are detected, the countdown is engaged. The MSB of the counter is used to set this flag to the processor.

Overload Average Beam Current – This is the second threshold level which is set by the external component network on Pin 9. The flag warns of an overload in anode current which should be lowered by reducing the Contrast.

Grid 2 Voltage Up/Down Requests – These flags indicate when the RGB output loops are about to go out of the control range necessary for correct gray scale tracking. These 2 flags are used during factory adjustment.

OK and Fault – These two flags are included as a check on the communication line between the MCU and MC44002/7. The OK flag is permanently wired high and Fault is permanently wired low. The MCU can use these flags to verify that the data received is valid.

ACC Active – This flag is high when there is a sufficient level of burst present in PAL and NTSC modes during the video back porch period. The flag goes low when the level of burst falls below a set threshold or if the signal becomes too noisy. The flag is used to implement a software color killer in PAL and NTSC and is also available for system identification purposes. Since in SECAM there is line carrier present during the gating period, it is quite likely that the ACC will be on, or will flicker on and off in this mode.

*** PAL Identified** – Recognizes the line-by-line swinging phase characteristic of the PAL burst. When this flag is on together with the ACC flag, this is positive identification for a PAL signal.

*** SECAM Identified** – Senses the changing line-by-line reference frequencies (Fo1 and Fo2) present during the back porch period of the SECAM signal. This flag alone provides identification that SECAM is being received (MC44002 only).

Excess Peak Beam Current – A voltage threshold is set on the beam current feedback on Pin 20, which is also used for the RGB output loops for current sampling. When the threshold is reached, the flag is set, indicating too high a peak beam current which may be in only a part of the screen. The response of the MCU might be to reduce the contrast of the picture. This flag, together with the Excess Average Beam Current flag, performs the function of beam limiting. The exact way in which this is handled is left to the discretion of the user who will have their own requirements, which may be incorporated by the way in which the software is written.

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* These two flags are set in opposition to one another such that they can never both be on at the same time. This has been done to try to prevent misidentification from occurring. Often it is very difficult to distinguish between PAL and SECAM especially when broadcast material has been transcoded, sometimes badly, leaving e.g. large amounts of SECAM carrier in a transcoded PAL signal (also often with noise). With this method the strongest influence will win out making a misidentification much less likely.

APPENDIX A – SYSTEM IDENTIFICATION TABLE

The table below can be used for color standard selection between the normal PAL (I, BG), SECAM (L, BG) and NTSC (3.58 MHz – M) standards. Detecting the hybrid VCR standard (525 lines with 4.4 MHz chrominance) would entail switching back to the 17.7 MHz crystal in the event of there being no flag present with the 14.3 MHz crystal. The MC44002/7 could also be used for the PAL M and N standards that are used in some parts of South America, but because the subcarrier frequencies differ by some kHz from the normal, crystals with a different center frequency would be required.

Table 6. System Identification

Flags from the MC44002/7				Crystal (MHz)	Standard Selected By MCU
<576 Lines	ACC On	PAL	SECAM		
0	0	0	0	17.7	Kill
0	0	0	1	17.7	SECAM
0	0	1	0	17.7	Kill
0	0	1	1	17.7	I^2C Bus Error
0	1	0	0	17.7	Kill
0	1	0	1	17.7	SECAM
0	1	1	0	17.7	PAL
0	1	1	1	17.7	I^2C Bus Error
1	0	0	0	14.3	NTSC Kill
1	0	0	1	14.3	NTSC Kill
1	0	1	0	14.3	NTSC Kill
1	0	1	1	14.3	I^2C Bus Error
1	1	0	0	14.3	NTSC
1	1	0	1	14.3	NTSC
1	1	1	0	14.3	NTSC
1	1	1	1	14.3	I^2C Bus Error

APPENDIX B – I2C BUS AND RGB CONTROL LOOPS WITH MC44002/7

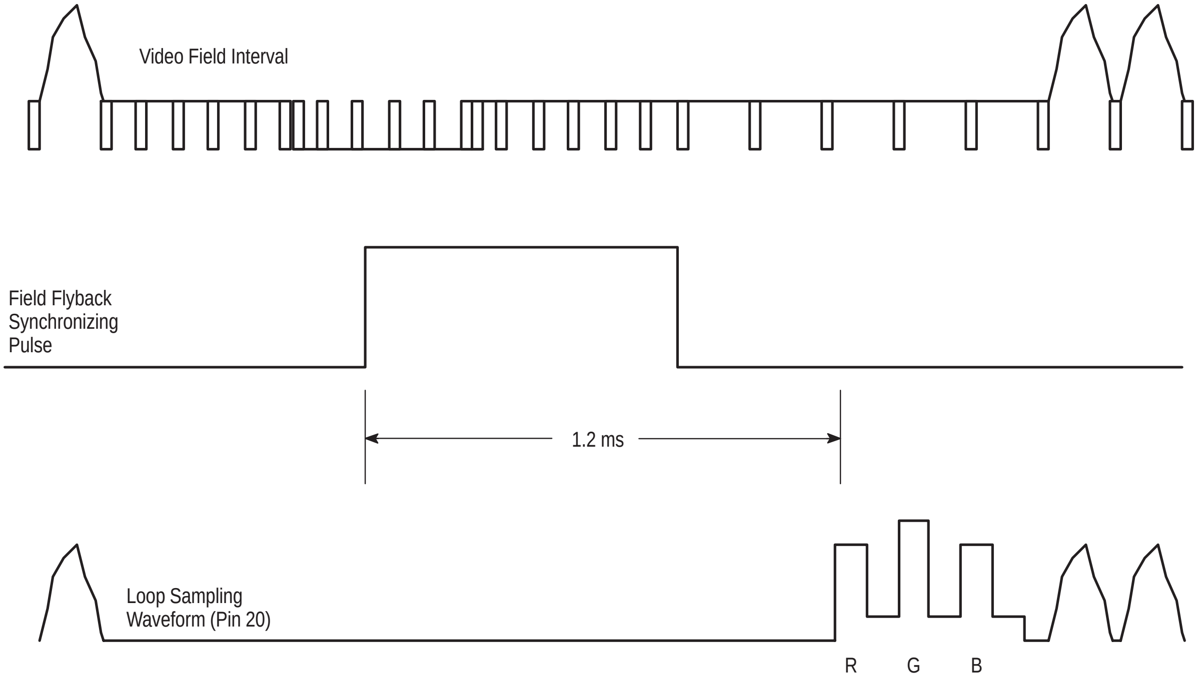
The RGB drive DACs cannot be buffered on account of the chip area that this would take up. This factor has considerable implications on the way that the I2C data is written into the MC44002/7 memory. If the data for Brightness, Contrast, Saturation and Hue are transmitted at just any time, a disturbance will be visible on the screen.

To overcome this difficulty, a method synchronizing the MCU to write data only during the field interval has been developed. This represents something of a limitation, but has to be used only for the 4 user controls.

Another characteristic of the MC44002/7 is that the Contrast control function is carried out within the RGB sampling loops. If data is written into the registers during the time when the RGB loops are taking their samples, then the situation arises where data is being sampled and changed at the same time. Hence, the loops will inevitably go unstable. When this happens, the brightness is seen to vary uncontrollably while the Contrast is changed. The effect has been described as “loop bounce”.

The timing diagram below show the exact situation.

From the start of the field flyback pulse to the beginning of the RGB sampling, approximately 1.2 ms is available to write the I2C data. Therefore, with a reasonable safety margin, the write time should be limited to only about 1.0 ms. This should not present any serious difficulty since only the data byte has to be transmitted during this time, and then only for the 4 user controls.



APPENDIX C – A SUGGESTED METHOD FOR OUTPUT LOOPS ADJUSTMENT

As described in section 4, the MC44002/7 output loops stage automatically adjust the dc level of the cathode voltage (cut–off) and the gain of the signal at the cathode (white balance). These automatic adjustments replace the conventional manual adjustments. The only adjustment that must be carried out, either by hand or automatically using an "intelligent screwdriver", is for the G2 voltage.

As the G2 voltage is varied, the automatic output loops of the MC44002/7 will adjust the cathode voltage of the dark sample level to always obtain the correct dark cathode current. However, if the G2 voltage is adjusted too high or too low, one or more of the DAC's controlling the dc level will reach the end of their range and the cathode voltage on the channel will not be correctly adjusted. In order to inform the operator or machine adjusting the G2 voltage that the control range has been exceeded, the G2–Up Request or G2–Down Request flags will be set. These flags are set when any one of the dc–DAC's approaches the end of its range. The threshold for setting the flags lies typically between 15 and 20% of the range from the actual end. Therefore, when a flag is set, the output loops can still operate correctly. As the gain of the picture tube varies very little with the G2 voltage, flags are not provided for the gain–DAC's.

In order to fix a procedure for setting the G2 voltage it is necessary to consider several points:

– On a given sample, the output currents from the three channels corresponding to the dark level are all different. The range of each DAC is about 2.4 mA and varies little from one channel to another and from one device to another. For reasons of stability and control range we recommend that the feedback resistor of the high–voltage video amplifier be 39 kΩ. this means that the dark cathode voltage range of each channel is about 94 V (i.e. 39 kΩ x 2.4 mA), but the absolute value of the cathode voltage can vary.

– In a typical application the actual cut–off voltage (i.e. zero cathode current) lies about 10–15 V higher than the dark cathode current (10 µA).

– When the beam–current in the picture tube increases, the G2 voltage tends to decrease. With the output loops of the MC44002/7, the cathode voltage is lowered automatically to compensate, but this effect would normally cause the values in the dc–DAC's to fall, using up their useful control range. as high beam current is associated to high contrast, in the MC44002/7 the dc output current (and therefore the cathode voltage) is reduced directly as the contrast setting is increased. In this way as contrast is increased, leading to higher beam current and lower G2 voltage, the dc–DAC's do not move much, thus saving range.

– A picture tube can have a difference in cut–off voltage between guns of up to about 30 V and it is not generally possible to identify in a particular type and make of tube which gun has the lowest and which gun has the highest cut–off voltage. Also, it is generally recommended by the tube manufacturer to set the cut–off voltage of the highest gun to a certain value which gives optimum focus performance.

– As the picture tube ages, the cathode cut–off voltage falls. It is therefore best to set the G2 voltage when the tube is new to give the highest possible cathode cut–off voltage.

Taking into account the above points, it is recommended that the G2 voltage be set up in the following way:

1) Display a black picture with the brightness control to minimum. (This give minimum beam current and no drop in G2 voltage.)

2) Set he contrast to maximum. (This causes the dc output current to be forced to a lower level and the output loops to compensate by moving towards the top of their range.)

3) Now adjust the G2 voltage so that the G2 Down Request flag is just turned off. (All the dc–DAC's are towards the top of their range and the highest one is just at the level to switch on the flag. Lowering the contrast setting, increasing the beam current or aging of the tube will cause the output loops to reduce the values in the dc–DAC's, but the available range will be a maximum.)

4) With a white picture and contrast set to give the maximum allowable beam current, check that the G2 Up Request flag is still off. (This is just to check that the G2 voltage is not falling too much at high beam current, but this step is not absolutely necessary.)

It is not recommended adjusting the G2 voltage to reach a specific value of cathode cut–off or dark voltage. The reason for this is that tolerances of the picture tube, high voltage video amplifier and the MC44002/7 itself will cause the dc–DACs to be set anywhere in their range and perhaps near the bottom end, leaving no margin for aging and G2 voltage drop.

MOTOROLA

MC44011

Advance Information

Bus Controlled Multistandard Video Processor

The Motorola MC44011, a member of the MC44000 Chroma 4 family, is designed to provide RGB or YUV outputs from a variety of inputs. The inputs can be composite video (two inputs), S–VHS, RGB, and color difference (R–Y, B–Y). The composite video can be PAL and/or NTSC as the MC44011 is capable of decoding both systems. Additionally, R–Y and B–Y outputs and inputs are provided for use with a delay line where needed. Sync separators are provided at all video inputs.

In addition, the MC44011 provides a sampling clock output for use by a subsequent triple A/D converter system which digitizes the RGB/YUV outputs. The sampling clock (6.0 to 40 MHz) is phase–locked to the horizontal frequency.

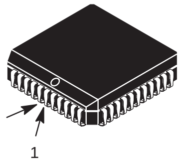
Additional outputs include composite sync, vertical sync, field identification, luma, burst gate, and horizontal frequency.

Control of the MC44011, and reading of status flags, is via an I^2C bus.

- Accepts NTSC and PAL Composite Video, S–VHS, RGB, and R–Y, B–Y
- Includes Luma and Chroma Filters, Luma Delay Lines, and Sound Traps
- Digitally Controlled via I^2C Bus
- R–Y, B–Y Inputs for Alternate Signal Source
- Line–Locked Sampling Clock for A/D Converters
- Burst Gate, Composite Sync, Vertical Sync and Field Identification Outputs
- RGB/YUV Outputs can Provide 3.0 Vpp for A/D Inputs
- Overlay Capability
- Single Power Supply: 5.0 V, ±5%, 550 mW (Typical)
- 44 Pin PLCC and QFP Packages

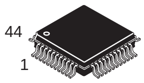
BUS CONTROLLED MULTISTANDARD VIDEO PROCESSOR

SEMICONDUCTOR TECHNICAL DATA



FN SUFFIX
PLASTIC PACKAGE
CASE 777
(PLCC)

FB SUFFIX
PLASTIC PACKAGE
CASE 824E
(QFP)



ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC44011FN	T_A = 0° to +70°C	PLCC–44
MC44011FB		QFP

Representative Block Diagram

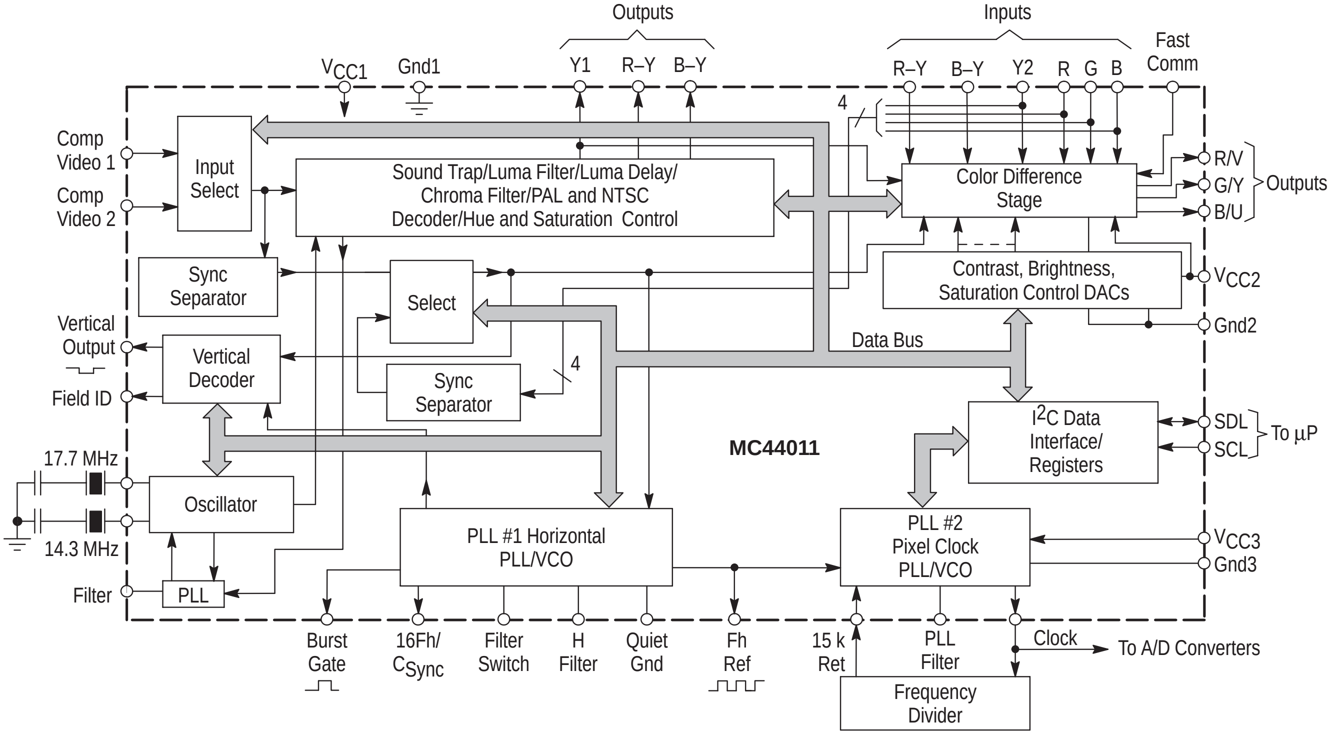
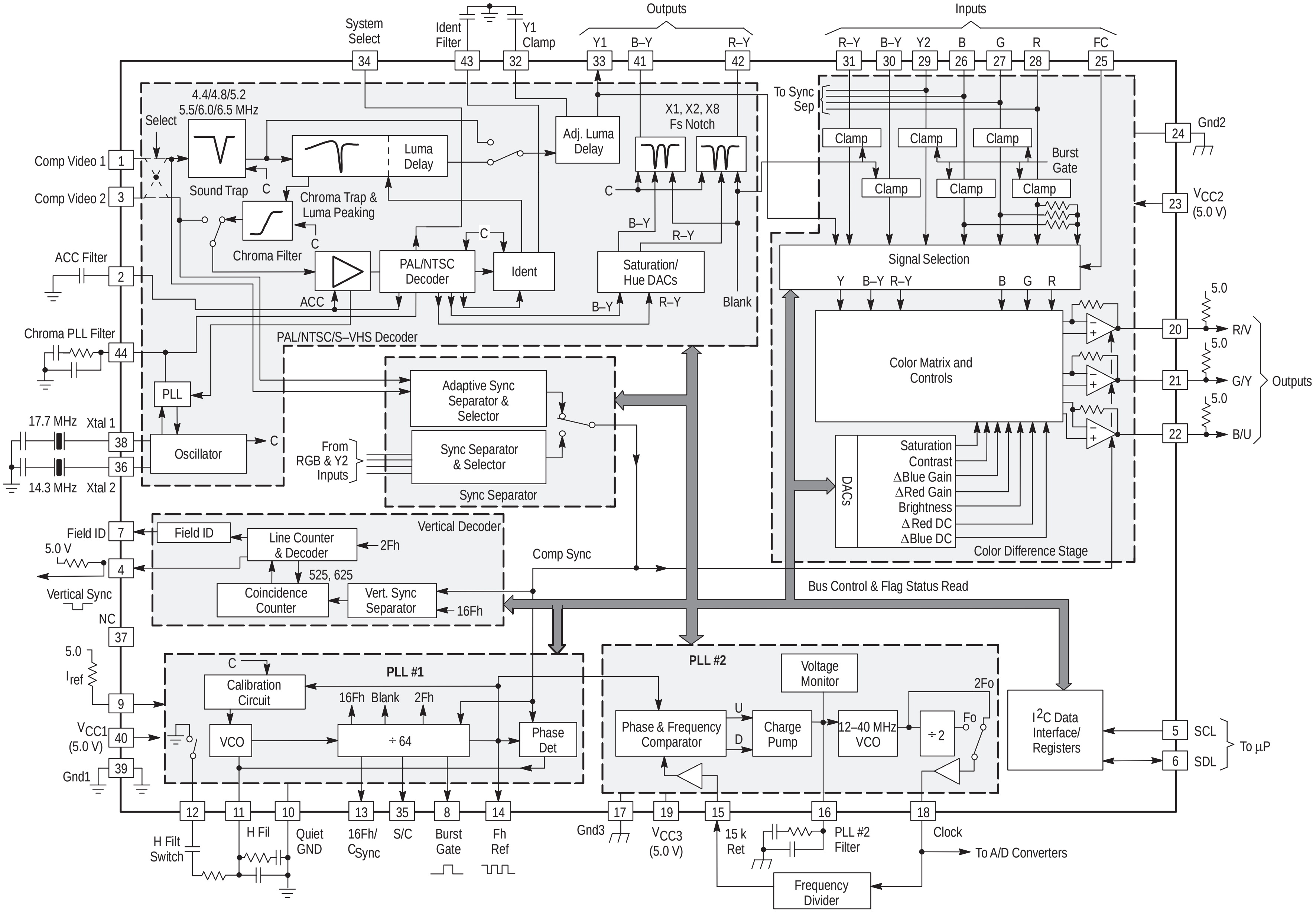


Figure 1. Representative Block Diagram



ELECTRICAL CHARACTERISTICS (The tested electrical characteristics are based on the conditions shown in Table 1 and 2. Composite Video input signal = 1.0 Vpp, composed of: 0.7 Vpp Black–to–White; 0.3 Vpp Sync–to–Black; 0.3 Vpp Color Burst. $V_{CC1} = V_{CC2} = V_{CC3} = 5.0$ V, $I_{ref} = 32$ µA (Pin 9), unless otherwise noted.)

Table 1. Control Bit Test Settings

Control Bit	Name	Value	Function
$77–7	S–VHS–Y	0	Composite Video input selected.
$77–6	S–VHS–C	0	Composite Video input selected.
$77–5	FSI	0	50 Hz Field Rate selected.
$77–4	$\overline{\text{L2 GATE}}$	0	PLL #2 Gating enabled.
$77–3	$\overline{\text{BLCP}}$	0	Clamp Pulse Gating enabled.
$77–2	$\overline{\text{L1 GATE}}$	0	Vertical Gating enabled.
$77–1, 0	CB1, CA1	1,1	Vertical section Auto–Countdown mode
$78–7	36/68 µs	0	Time from beginning of Line 4 to Vertical Sync is 36 µs.
$78–6	CalKill	0	Horizontal Calibration Loop enabled.
$79–7, 6	HI, VI	1,1	Normal
$7A–7	Xtal	–	0 = 17.7 MHz crystal selected, 1 = 14.3 MHz crystal selected.
$7A–6	SSD	0	Normal
$7B–7, 6	T1, T2	1,1	Sound Trap Notch filter set to 5.5 MHz (with 17.7 MHz crystal).
$7C–7	SSC	0	Permits PAL and NTSC selection.
$7C–6, $7D–6	SSA, SSB	–	0, 1 = PAL decoding, 1,0 = NTSC decoding
$7D–7, $7E–7, 6	P1, P3, P2	1, 1, 1	Sets Luma Peaking at 0 dB.
$7F–7, 6, $80–6	D3, D1, D2	0, 0, 0	Set Luma Delay to minimum
$80–7	$\overline{\text{RGB EN}}$	0	Fast Commutate input can enable RGB inputs.
$81–7	Y2 EN	0	Y2 input (Pin 29) deselected
$81–6	Y1 EN	1	Y1 luma path from PAL/NTSC decoder selected.
$82–7	YUV EN	0	RGB output mode selected
$82–6	YX EN	0	Disable luma matrix from RGB inputs.
$83–7	L2 Gain	0	Set PLL #2 Phase/Frequency detector gain high.
$83–6	L1 Gain	1	Set PLL #1 Phase Detector gain high.
$84–7	H Switch	0	Set Horizontal Phase Detector filter switch open.
$84–6	525/625	–	0 = 625 lines (PAL), 1 = 525 lines (NTSC)
$85–7	$F_{osc} \div 2$	0	Select direct VCO output from PLL #2.
$85–6	C_{Sync}	0	16 Fh output selected at Pin 13.
$86–7	V_{in} Sync	1	Composite Video inputs (Pin 1 or 3) Sync Source selected.
$86–6	H EN	0	Enabled Horizontal Timebase.
$87–7	Y2 Sync	0	Y2 sync source not selected.
$88–7	V2/V1	1	Select Video 1 input (Pin 1).
$88–6	RGB Sync	0	RGB inputs Sync Source not selected.

Table 2. DAC Test Settings

DAC	Value	Function	DAC	Value	Function
$78	32	R–Y/B–Y Gain	$82	32	Red Contrast Trim
$79	32	Sub Carrier Phase	$83	32	Blue Brightness Trim
$7D	00	Blue Output DC Bias	$84	32	Main Brightness
$7E	00	Red Output DC Bias	$85	32	Red Brightness Trim
$7F	63	Pixel Clock VCO Gain	$86	32	Saturation (Color Diff.)
$80	32	Blue Contrast Trim	$87	16	Saturation (Decoder)
$81	32	Main Contrast	$88	32	Hue

NOTE: Currents out of a pin are designated –, and those into a pin are designated +.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC1} V_{CC2} V_{CC3}	–0.5 to +6.0 –0.5 to +6.0 –0.5 to +6.0	Vdc
Power Supply Difference (Between any two V_{CC} pins)	–	±0.5	Vdc
Input Voltage: Video 1, 2, SCL, SDL 15 kHz Return R–Y, B–Y, Y2, RGB, FC	V_{in}	–0.5, V_{CC1} +0.5 –0.5, V_{CC3} +0.5 –0.5, V_{CC2} +0.5	Vdc
Junction Temperature (Storage and Operating)	T_J	–65 to +150	°C

NOTES: 1. Devices should not be operated at these limits. The “Recommended Operating Conditions” table provides for actual device operation.

2. ESD data available upon request.

RECOMMENDED OPERATING CONDITIONS

Characteristics	Symbol	Min	Typ	Max	Unit
Power Supply Voltage	$V_{CC1, 2, 3}$	4.75	5.0	5.25	Vdc
Power Supply Difference (Between any two V_{CC} pins)	ΔV_{CC}	–0.5	0	0.5	Vdc
Input Voltage: Video 1, 2 (Sync–White)	V_{in}	0.7	1.0	1.4	Vpp
Chroma (S–VHS Mode)		–	–	1.2	
Y2		0.7	1.0	1.4	
RGB		0.5	0.7	1.0	
R–Y, B–Y (Pins 30, 31)		0	–	1.8	
15 kHz Return		0	–	V_{CC3}	Vdc
SCL, SDL		0	–	V_{CC1}	
FC		0	–	V_{CC2}	
Burst Signal		30	280	560	mVpp
Sync Amplitude		60	300	V_{CC1}	mVpp
Output Load Impedance to Ground: RGB (Pull–Up = 390 Ω)	RL_{RGB}	1.0	–	∞	kΩ
B–Y, R–Y	RL_{CD}	10	–	∞	
Y1	RL_{Y1}	1.0	–	∞	
Pull–Up Resistance at Vertical Sync (Pin 4)	R_{VS}	1.0	10	–	kΩ
Source Impedance: Video 1, 2	–	0	–	1.0	kΩ
Pins 26 to 31		0	–	1.0	
Pixel Clock Frequency (Pin 18, see PLL #2 Electrical Characteristic)	f_{px}	–	2.0 to 45	–	MHz
15 kHz Return Pulse Width (Low Time)	PW_{15k}	0.2	–	45	µs
I^2C Clock Frequency	f_{I^2C}	–	–	100	kHz
Reference Current (Pin 9)	I_{ref}	–	32	–	µA
Operating Ambient Temperature	T_A	0	–	70	°C

NOTE: All limits are not necessarily functional concurrently.

ELECTRICAL CHARACTERISTICS (T$_A$ = 25°C, V_{CC1} = V_{CC2} = V_{CC3} = 5.0 V, unless otherwise noted.)

Characteristics	Min	Typ	Max	Unit
POWER SUPPLIES				
Power Supply Current (V_{CC} = 5.0 V) Pin 40	75	95	115	mA
Pin 23	6.0	9.0	12	
Pin 19	3.5	6.0	8.0	
Total	85	110	135	

ELECTRICAL CHARACTERISTICS (continued) (T_A = 25°C, V_{CC1} = V_{CC2} = V_{CC3} = 5.0 V, unless otherwise noted.)

Characteristics	Min	Typ	Max	Unit
PAL/NTSC/S–VHS DECODER				
Video 1, 2 Inputs				
Crosstalk Rejection, f = 1.0 MHz (Measured at Y1 output, Luma Peaking = 0 dB, $77–7 = 1)	20	40	–	dB
DC Level: @ Selected Input	–	2.8	–	Vdc
@ Unselected Input	–	0.7	–	
Clamp Current	–30	–20	–10	µA
Sound Trap Rejection (See Figures 14 to 23)				
With 17.7 MHz Crystal: @ 6.5 MHz (T1, T2 = 00)	15	30	–	dB
@ 6.0 MHz (T1, T2 = 10)	15	30	–	
@ 5.5 MHz (T1, T2 = 11)	10	43	–	
@ 5.74 MHz (T1, T2 = 01)	15	26	–	
With 14.3 MHz Crystal: @ 4.44 MHz (T1, T2 = 11)	–	35	–	
R–Y, B–Y Outputs (Pins 41, 42)				
Output Amplitude (with 100% Saturated Color Bars)				
Saturation (DAC 87) = 00	–	<1.0	–	mVpp
Saturation (DAC 87) = 16	–	1.6	–	Vpp
Saturation (DAC 87) = 63	1.8	3.0	–	
DC Level During Blanking	–	2.4	–	Vdc
Hue Control – Minimum Phase (DAC 88 = 00)	–	–30	–	Deg
– Maximum Phase (DAC 88 = 63)	–	30	–	
Nominal Saturation (with respect to Y1 Output, Note 1)	–	100	–	%
R–Y/B–Y Ratio: Balance (DAC 78) = 63	1.35	1.69	2.06	V/V
Balance (DAC 78) = 32	0.98	1.27	1.58	
Balance (DAC 78) = 00	0.60	0.77	0.96	
Output Amplitude Variation as Burst is varied from 80 mVpp to 600 mVpp	–	3.0	–	dB
Color Kill Attenuation ($7C–7, 6 and $7D–6 = 011)	–	40	–	dB
Crosstalk with respect to Y1 Output (@ 1.0 MHz)	–27	–20	–	
Chroma Subcarrier Residual				
(Measured at Y1 Output, with 17.7 MHz Crystal)				
f = Subcarrier	–	25	60	mVpp
2nd Harmonic Residual	–	4.0	12	
4th Harmonic Residual	–	12	30	
(Measured at R–Y, B–Y Outputs, with 17.7 or 14.3 MHz Crystal)				
f = Subcarrier	–	5.0	20	
2nd Harmonic Residual	–	5.0	20	
4th Harmonic Residual	–	15	50	
Y1 Luma Output (Pin 33)				
Clamp Level	0.4	1.1	1.8	Vdc
Output Impedance	–	300	–	Ω
Composite Video Mode ($77–6, 7 = 00)				
Output Level versus Input Level				
Delay = 000, Peaking = 111, f = 100 kHz	1.0	1.1	1.2	V/V
Delay = Min–to–Max, Peaking = Min–to–Max	–	1.1	–	
–3.0 dB Bandwidth (17.7 MHz Crystal, PAL Decoding selected, Sound trap at 6.5 MHz, Peaking off)	–	2.8	–	MHz
Peaking Range ($7D–7, $7E–6/7 = 000 to 111, @ 3.0 MHz, with 17.7 MHz Crystal, Sound trap at 6.5 MHz)	5.0	8.0	10	dB
Overshoot with Minimum Peaking	–	0	–	%
Differential Non–linearity (Measured with Staircase)	–	2.0	–	%
Delay (Pin 1 or 3 to 33)				
With 14.3 MHz Crystal: Minimum	–	690	–	ns
Maximum	–	1040	–	
With 17.7 MHz Crystal: Minimum	–	594	–	
Maximum	–	876	–	

NOTE: 1. This spec indicates a correct output amplitude at Pins 41 and 42, with respect to Y1 output. For standard color bar inputs, the output amplitude is between 1.5 and 1.7 Vpp, with the settings in Tables 1 and 2.

ELECTRICAL CHARACTERISTICS (continued) (T_A = 25°C, V_{CC1} = V_{CC2} = V_{CC3} = 5.0 V, unless otherwise noted.)

Characteristics	Min	Typ	Max	Unit
PAL/NTSC/S–VHS DECODER				
S–VHS Mode ($77–6, 7 = 11)				
Output Level versus Input Level (Delay = Min–to–Max)	1.0	1.1	1.2	V/V
–3.0 dB Bandwidth (17.7 MHz crystal, PAL Decoding selected, Sound trap at 6.5 MHz)	–	4.5	–	MHz
Y/C Crosstalk Rejection	20	40	–	dB
Delay (Luma input to Pin 33)				
14.3 MHz Crystal: Minimum	–	395	–	ns
Maximum	–	745	–	
17.7 MHz Crystal: Minimum	–	350	–	
Maximum	–	632	–	
Crystal Oscillator				
PLL Pull–in range with respect to Subcarrier Frequency				
(Burst Level ≥ 30 mVpp): with 17.7 MHz Crystal	–	±350	–	Hz
with 14.3 MHz Crystal	–	±300	–	
$4f_{SC}$ Filter (Pin 44) DC Voltage				
@ 14.3 MHz	–	2.4	–	Vdc
@ 17.7 MHz	–	3.5	–	
No Burst present	–	1.3	–	
DC Voltages				Vdc
System Select (Pin 34)				
NTSC Mode (SSA = 1, SSB = 0, SSC = 0, SSD = 0)	1.5	1.75	2.0	
PAL Mode (SSA = 0, SSB = 1, SSC = 0, SSD = 0)	0	0.075	0.4	
Color Kill Mode (SSA = 1, SSB = 1, SSC = 0, SSD = 0)	–	0.075	–	
External Mode (SSA = X, SSB = X, SSC = 1, SSD = 0)	3.7	4.0	4.3	
Ident Filter (Pin 43)				
NTSC Mode	–	1.6	–	
PAL Mode	1.2	1.5	1.8	
No Burst present	–	0.2	–	
ACC Filter (Pin 2)				
No Burst present	–	0.25	–	
Threshold for ACC Flag on	0.8	1.2	1.6	
Burst = 50 mVpp	–	1.4	–	
Burst = 280 mVpp	–	1.7	–	
System Select Output Impedance	–	40	100	kΩ
COLOR DIFFERENCE SECTION				
RGB/YUV Outputs				
Output Swing, Black–to–White (DAC $81 = 63)	2.0	3.0	–	Vpp
THD (RGB Inputs to RGB Outputs @ 1.0 MHz, 0.7 Vpp)	–	0.5	2.0	%
–3.0 dB Bandwidth	–	6.0	–	MHz
Clamp Level				
RGB Outputs ($7D, 7E = 00)	–	1.4	–	Vdc
UV Outputs ($7D, 7E = 32)	–	2.3	–	
Red, Blue Clamp Level Change (DACs $7D, 7E varied from 00 to 63)	0.85	1.8	2.4	
Crosstalk Rejection				
Among RGB Outputs @ 1.0 MHz	20	40	–	dB
Y1 to Y2	20	40	–	
From RGB Outputs to Y1 or Y2	20	40	–	
Input Black Clamp Voltage at Y2, B–Y, R–Y, and RGB	2.4	3.0	3.6	Vdc
Fast Commutate Input (Pin 25)				
Switching Threshold Voltage	–	0.5	–	Vdc
Input Current @ V_{in} = 0 V	–	–7.5	–	µA
Input Current @ V_{in} = 5.0 V	–	0	–	
Timing: Input Low–to–High (RGB Enable)	–	50	–	ns
Input High–to–Low (RGB Disable)	–	90	–	

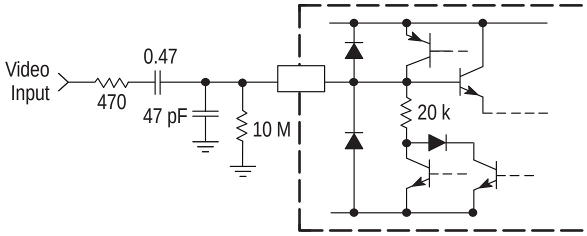
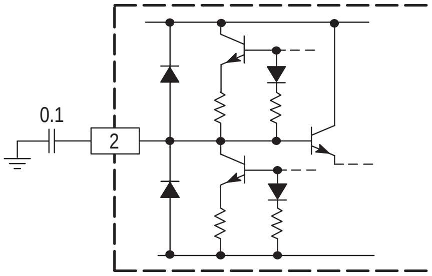
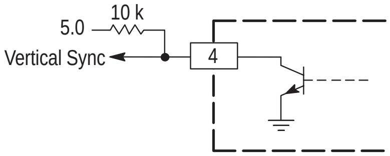
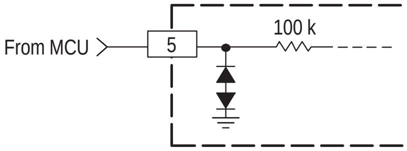
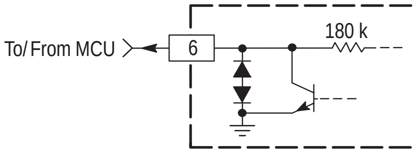
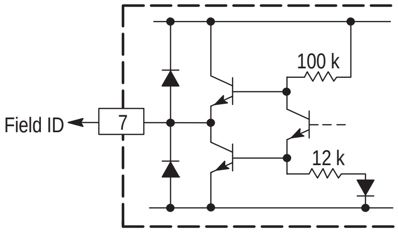
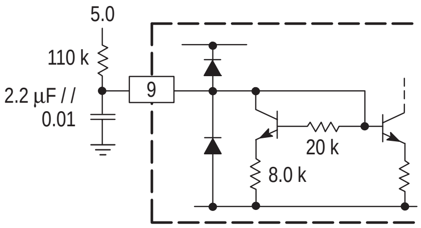
ELECTRICAL CHARACTERISTICS (continued) (T_A = 25°C, V_{CC1} = V_{CC2} = V_{CC3} = 5.0 V, unless otherwise noted.)

Characteristics	Min	Typ	Max	Unit
COLOR DIFFERENCE SECTION				
Contrast (Gain)				V/V
Y1 to RGB (DAC $81 = 32, DAC $86 = 00)	1.9	2.4	3.0	
Y2 to RGB (DAC $81 = 32, DAC $86 = 00)	1.8	2.3	2.8	
Green In (Pin 27) to Green Out (Pin 21) with YX Enabled ($82–6 = 1, DAC $81 and DAC $86 = 32)	1.8	2.3	2.4	
Red–to–Green and Blue–to–Green Gain Ratio	0.8	1.0	1.2	
RGB Input to RGB Output with YX Not Enabled ($82–6 = 0, DAC $81 and DAC $86 = 32)	2.0	2.6	3.2	
Ratio (DAC $81 = 00 versus 32)	–	0.2	0.4	
Ratio (DAC $81 = 63 versus 32)	1.5	2.0	2.5	
Red and Blue Trim Control (DACs $80, 82 varied from 00 to 63)	±5.0	±30	±60	%
Saturation (Average of R, G, B saturation levels with respect to Luma)				
Inputs at Pins 29 to 31 (DAC $86 = 32)	50	90	130	%
Ratio (DAC $86 = 00 versus 32)	–	–	5	
Ratio (DAC $86 = 63 versus 32)	150	170	190	
Inputs at Pins 26 to 28 (DAC $86 = 32, $82–6 = 1)	70	125	180	
Brightness				
Black Level Range (Brightness = 00 to 63 with respect to Brightness setting of 32)	±0.3	±0.5	±0.7	Vdc
Red and Blue Trim Control (DACs $83, 85 varied from 00 to 63)	±0.05	±0.3	±0.6	
Color Coefficients				
G–Y Matrix Coefficient versus B–Y	–0.21	–0.19	–0.17	
G–Y Matrix Coefficient versus R–Y	–0.56	–0.51	–0.46	
YX Matrix (Inputs at Pins 26 to 28, $82–6 = 1):				
Y versus R	0.28	0.30	0.32	
Y versus G	0.57	0.59	0.61	
Y versus B	0.09	0.11	0.13	
HORIZONTAL TIME BASE SECTION (PLL #1)				
Free–Running Period (Calibration mode in effect, Bit $86–6 = 1)				
17.7 MHz Crystal selected ($84–6 = 0)	62.5	64.0	65.5	µs
14.3 MHz Crystal selected ($84–6 = 1)	62.5	63.5	65.5	
VCO minimum period (Pin 11 Voltage at 1.2 V)	56	59.5	62	µs
VCO maximum period (Pin 11 Voltage at 2.8 V)	66	69.5	72	
VCO Control Gain factor	5.0	8.5	12	µs/V
Phase Detector Current				
High Gain ($83–6 = 1)	15	50	85	µA
Low Gain–to–High Gain Current Ratio	0.32	0.38	0.44	µA/µA
Noise Gate Width ($77–2 = 0, Low Gain, see Figure 26)	–	16	–	µs
Horizontal Filter Switch (Pin 12)				
Saturation Voltage (I_{12} = 20 µA)	–	10	100	mV
Dynamic Impendance ($84–7 = 1)	–	<5.0	–	kΩ
Parallel Resistance ($84–7 = 0)	0.6	1.0	–	MΩ
Pins 8, 13, 14 Output Level				
High (I_O = –40 µA)	2.4	4.5	–	Vdc
Low (I_O = 800 µA)	–	0.1	0.8	
Burst Gate (Pin 8) Timing (See Figures 25, 27)				µs
Rising edge from Sync leading edge (Pins 1, 3)	4.4	5.6	6.8	
Rising edge from Sync center (Pins 26 to 29)	–	2.5	–	
Pulse Width	3.0	3.5	4.0	
16Fh Output (Pin 13) Timing (Bit $85–6 = 0) (See Figures 25, 27)				
Rising edge from Fh rising edge	–	1.3	–	µs
Duty Cycle	–	50	–	%
Composite Sync Output (Pin 13) Timing (Bit $85–6 = 1)				µs
Input Sync center to Output Sync center (Pins 1, 3)	–	0.95	–	
Input Sync center to Output Sync center (Pins 26 to 29)	–	0.4	–	

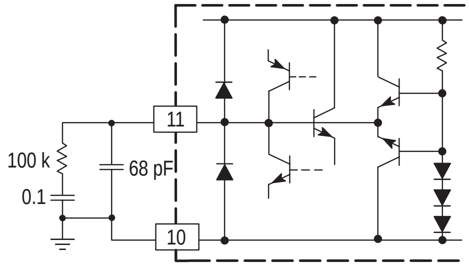
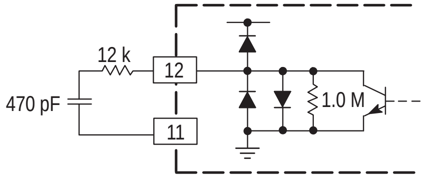
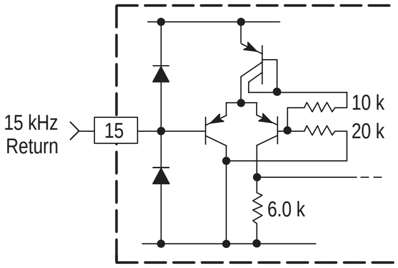
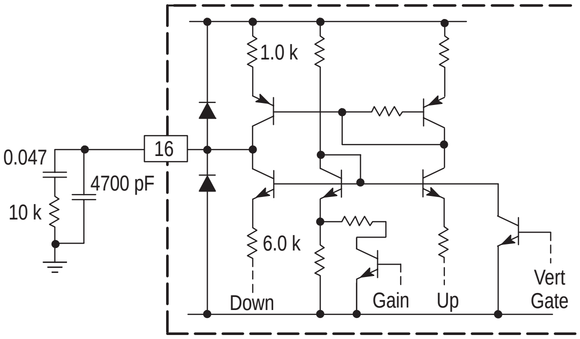
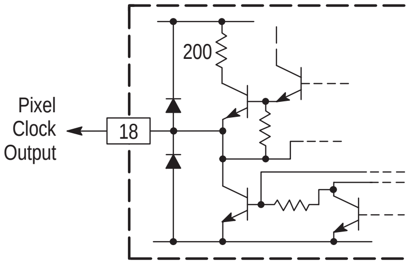
ELECTRICAL CHARACTERISTICS (continued) (T_A = 25°C, V_{CC1} = V_{CC2} = V_{CC3} = 5.0 V, unless otherwise noted.)

Characteristics	Min	Typ	Max	Unit
HORIZONTAL TIME BASE SECTION (PLL #1)				
Fh Reference (Pin 14) Timing (See Figures 25, 27)				
Rising edge from Sync center (Pins 1, 3)	–	1.3	–	µs
Rising edge from Sync center (Pins 26 to 29)	–	650	–	ns
Duty cycle	–	50	–	%
Sandcastle Output (Pin 35, see Figures 25, 27)				Vdc
Output Voltage – Level 1	3.7	4.0	4.3	
Output Voltage – Level 2	2.8	3.0	3.2	
Output Voltage – Level 3	–	1.55	–	
Output Voltage – Level 4	–	0.07	–	
Rising edge from Sync center (Pins 1, 3)	–	–2.6	–	µs
Rising edge from Sync center (Pins 26 to 29)	–	–3.3	–	
High Time	–	6.0	–	
Level 2 Time	–	5.0	–	
Reference Voltage @ Pin 9 (I_{ref} = 32 µA)	1.0	1.2	1.4	Vdc
PHASE–LOCKED PIXEL CLOCK SECTION (PLL #2)				
VCO Frequency @ Pin 18				MHz
Minimum (Pin 16 = 1.6 V, $85–7 = 1)	–	2.0	4.0	
Maximum (Pin 16 = 4.0 V, $85–7= 0)	30	45	60	
VCO Up (Flag 19) Threshold Voltage @ Pin 16	1.5	1.7	1.9	Vdc
VCO Down (Flag 20) Threshold Voltage @ Pin 16	3.1	3.3	3.5	
VCO Control Voltage Range @ Pin 16	1.2	–	3.8	Vdc
VCO Control Gain factor ($7FDAC = 00, $85–7 = 0)	4.0	8.0	12	MHz/V
Charge Pump Current (Pin 16)	25	50	75	µA
High Gain ($83–7 = 0)				
Current Ratio	0.3	0.4	0.5	µA/µA
Low Gain–to–High Gain				
Pixel Clock Output (Pin 18) (Load = 3 FAST TTL loads + 10 pF)				
Output Voltage – High	–	3.9	–	Vdc
Output Voltage – Low	–	0.15	–	
Rise Time @ 50 MHz	–	7.0	–	ns
Rise Time @ 9.0 MHz	–	17	–	
Fall Time @ 50 MHz	–	5.0	–	
Fall Time @ 9.0 MHz	–	8.0	–	
15 kHz Return (Pin 15)				
Input Threshold Voltage	–	1.5	–	Vdc
Falling edge from Fh rising edge	–	60	–	ns
Minimum Input Low Time	200	–	–	
VERTICAL DECODER				
Vertical Frequency Range	43.3	–	122	Hz
Vertical Sync Output				
Saturation Voltage (I_O = 800 µA)	–	0.1	0.8	V
Leakage Current @ 5.0 V (Output high)	–	–	40	µA
Timing from Sync polarity reversal to Pin 4 falling edge (See Figures 33, 34)				µs
($78–7 = 0)	32	36	40	
($78–7 = 1)	62	68	74	
Vertical Sync Pulse Width (Pin 4, NTSC or PAL)	490	500	510	µs
Field Ident (Pin 7) Output Voltage – High (I_O = –40 µA)	2.4	4.5	–	Vdc
Output Voltage – Low (I_O = 800 µA)	–	0.1	0.8	
Timing	–	Fig. 33, 34	–	
HORIZONTAL SYNC SEPARATOR				
Sync Slicing Levels (Pins 1, 3)	–	120	–	mV
From Black Level (Pins 26 to 29)	–	150	–	

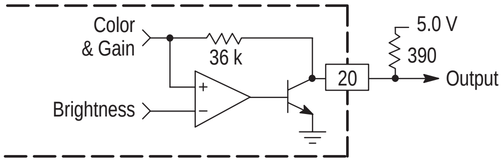
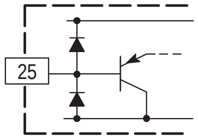
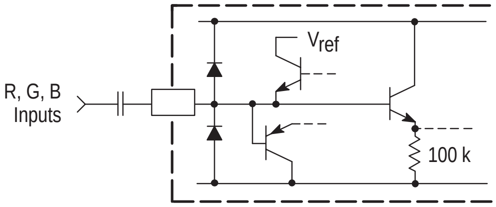
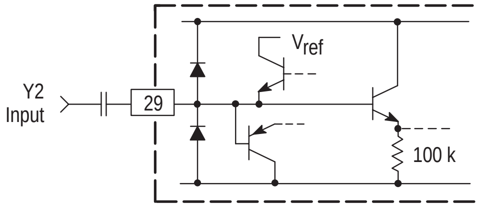
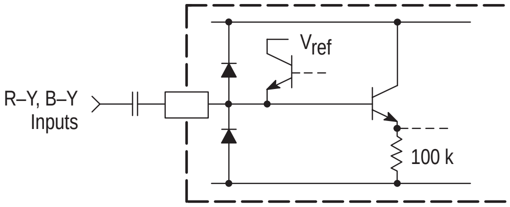
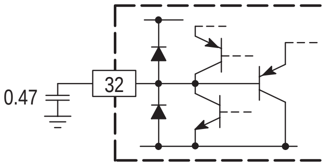
PIN FUNCTION DESCRIPTION

FB QFP Pin	FN PLCC Pin	Representative Circuitry (Pin numbers refer to PLCC package)	Description (Pin numbers refer to PLCC package)
39, 41	1, 3		**Video Input 1 & 2** – Video 1 (Pin 1) and Video 2 (Pin 3) are composite video inputs. Either can be NTSC or PAL. Input impedance is high, termination must be external. Also used for the luma and chroma components of an S–VHS signal. Selection of these inputs is done by software. External components protect against ESD and noise.
40	2		**ACC Filter** – A 0.1 µF capacitor at this pin filters the feedback loop of the chroma automatic gain control amplifier. Input chroma burst amplitude can be between 30 and 600 mVpp.
42	4		**Vertical Sync Output** – An open collector output requiring an external pull–up. Output is an active low pulse, 500 µs wide, occurring each field. Timing of this pulse depends on Bit $78–7.
43	5		**SCL** – Clock for the I^2C bus interface. See Appendix C for specifications. Maximum frequency is 100 kHz.
44	6		**SDL** – Bidirectional data line for the I^2C bus interface. As an output, it is an open collector. (Write Address $8A, Read Address $8B)
1	7		**Field ID** – TTL level output indicating Field 1 or Field 2. Polarity depends on state of Bit $78–7 (Vertical Sync Delay). See Table 11 and Figure 33 and 34.
2	8	(Same as Pin 7)	**Burst Gate** – TTL level output used for external clamps, as well as internally. Pulse is active high, ≈ 3.5 µs wide, with the rising edge ≈ 3.0 µs after center of selected incoming sync pulse.
3	9		**Reference Current Input** – Current supplied to this pin, typically 32 µA from 5.0 V through a 110 kΩ resistor, is the reference current for the calibration circuit. Noise filtering should be done at the pin. Voltage at this pin is typically 1.2 V.
4	10	(See power distribution diagram at the end of this section.)	**Quiet Ground** – Ground for the horizontal PLL filter (PLL #1) at Pin 11.

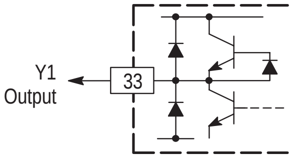
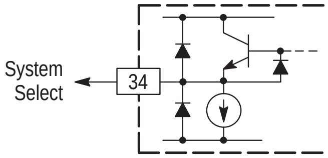
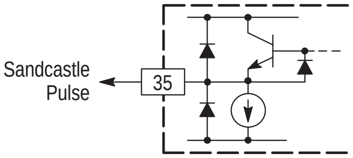
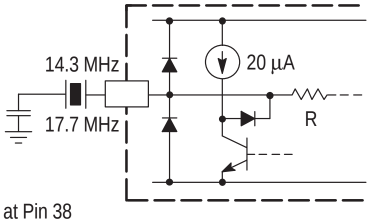
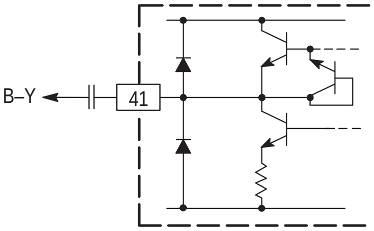
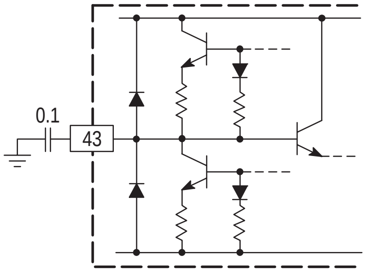
PIN FUNCTION DESCRIPTION (continued)

FB QFP	FN PLCC	Representative Circuitry (Pin numbers refer to PLCC package)	Description (Pin numbers refer to PLCC package)
Pin			
5	11		**H Filter** – Components at this pin filter the output of the phase detector of PLL #1. This PLL becomes phase–locked to the selected incoming horizontal sync. External component values are valid for NTSC and PAL systems.
6	12		**H Filter Switch** – An internal switch–to–ground which permits altering the filtering action of the components at Pin 11.
7	13	(Same as Pin 7)	**16 Fh/C$_{Sync}$** – A TTL level output from PLL #1. This pin provides either a square wave equal to Fh x 16 (≈ 250 kHz), or composite sync, depending on the setting of Bit $85–6.
8	14	(Same as Pin 7)	**Fh Reference** – A TTL square wave output which is phase–locked to the selected incoming horizontal sync. The rising edge occurs ≈ 1.3 µs after sync center.
9	15		**15 kHz Return** – This TTL input receives the output of an external frequency divider which is part of PLL #2 (Pixel Clock PLL). This signal will be phase and frequency–locked to the Fh signal at Pin 14. If PLL #2 is not used, this pin should be connected to a 5.0 V supply.
10	16		**PLL #2 Filter** – Components at this pin filter the output of the phase detector of PLL 2. This PLL becomes phase–locked to the Fh signal at Pin 14. Recommended values for filter components are shown. External components should be connected to ground at Pin 17. If PLL #2 is not used, this pin should be grounded.
11	17	(See power distribution diagram at the end of this section.)	**Gnd3** – Ground for the high frequency PLL #2. Signals at Pins 15 to 19 should be referenced to this ground.
12	18		**Pixel Clock Outpu**t – Sampling clock output (TTL) for external A/D converters, and for the external frequency divider. Frequency range at this pin is 6.0 to 40 MHz.

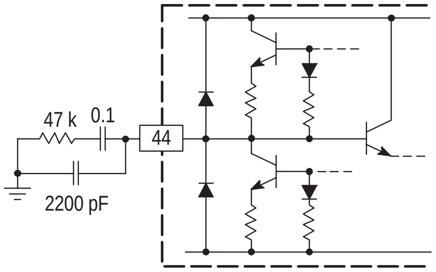
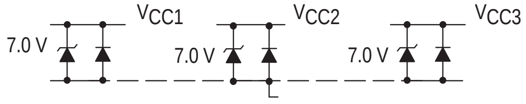
PIN FUNCTION DESCRIPTION (continued)

FB	FN	Representative Circuitry (Pin numbers refer to PLCC package)	Description (Pin numbers refer to PLCC package)
QFP	PLCC		
Pin			
13	19	(See power distribution diagram at the end of this section.)	**V_{CC3}** – A 5.0 V supply (±5%), for the high frequency PLL #2. Decoupling must be provided from this pin to Pin 17. Ripple on this pin will affect pixel clock jitter.
14	20		**R/V Output** – Red (in RGB mode), or R–Y (in YUV mode), output from the color difference stage. A pull–up (390 Ω) to 5.0 V is required. Blank level is ≈ 1.4 Vdc. Maximum amplitude is ≈ 3.0 Vpp, black–to–white.
15	21	(Same as Pin 20)	**G/Y Output** – Green (in RGB mode), or Y (in YUV mode), output from the color difference stage (same as Pin 20).
16	22	(Same as Pin 20)	**B/U Output** – Blue (in RGB mode), or B–Y (in YUV mode), output from the color difference stage (same as Pin 20).
17	23	(See power distribution diagram at the end of this section.)	**V_{CC2}** – A 5.0 V supply (±5%), for the color difference stage. Decoupling must be provided from this pin to Pin 24.
18	24	(See power distribution diagram at the end of this section.)	**Gnd2** – Ground for the color difference stage. Signals at Pins 20 to 31 should be referenced to this pin.
19	25		**FC** – Fast Commutate switch. Taking this pin high (TTL level) connects the RGB inputs (Pins 26 to 28) to the RGB outputs (Pins 20 to 22), permitting an overlay function. The switch can be disabled in software (Bit $80–7).
20, 21, 22	26, 27, 28		**Blue (26), Green (27), Red (28) Inputs** – Inputs to the color difference stage. Designed to accept standard analog video levels, these input pins have a clamp and sync separator. They are selected with Pin 25 or in software (Bit $80–7).
23	29		**Y2 Input** – Luma #2/Composite sync input. This luma input to the color difference stage is used in conjunction with auxiliary color difference inputs, and/or as a sync input. Clamp and sync separator are provided.
24, 25	30, 31		**B–Y (30), R–Y (31) Inputs** – Inputs to the color difference stage. Designed for standard color difference levels, these inputs can be capacitor coupled from the color difference outputs, from a delay line, or an auxiliary signal source. Input clamp is provided.
26	32		**Y1 Clamp** – A 0.47 µF capacitor at this pin provides clamping for the Luma #1 output.

PIN FUNCTION DESCRIPTION (continued)

FB QFP Pin	FN PLCC Pin	Representative Circuitry (Pin numbers refer to PLCC package)	Description (Pin numbers refer to PLCC package)
27	33		**Y1 Output** – Luma #1 output. This output from the PAL/NTSC/S–VHS decoder is the luma component of the decoded composite video at Pin 1 or 3. It is internally directed to the color difference stage.
28	34		**System Select** – A multi–level dc output which indicates the color decoding system to which the PAL/NTSC detector is set by the software. This output is used by the MC44140 chroma delay line.
29	35		**Sandcastle Pulse** – A multi–level timing pulse output used by the MC44140 chroma delay line. This pulse encompasses the horizontal sync and burst time.
30, 32	36, 38	 R = 400 Ω at Pin 38 R = 300 Ω at Pin 36	**Xtal 2 (36), Xtal 1 (38)** – Designed for connection of 4x subcarrier color crystals. Selection is done in software. The selected frequency is used by the PAL/NTSC detector; system identifier; all notches and traps; delay lines; and the horizontal calibration circuit. The crystal frequency should be: 14.3 MHz at Pin 36 for NTSC, 17.7 MHz at Pin 38 for PAL. (See Table 17 for crystal specifications)
31	37		**No Connect** – This pin is to be left open.
33	39	(See power distribution diagram at the end of this section.)	**Ground 1** – Ground for all sections except PLL #2 and the color difference stage.
34	40	(See power distribution diagram at the end of this section.)	**V_{CC1}** – A 5.0 V (±5%), supply to all sections except PLL #2 and the color difference stage.
35	41		**B–Y Output** – Output from the PAL/NTSC decoder, it is typically capacitor–coupled to a delay line or to the B–Y input. This pin is clamped, and filtered at the color subcarrier frequency, 2x, and 8x that frequency.
36	42	(Same as Pin 41)	**R–Y Output** – Output from the PAL/NTSC decoder.
37	43		**Ident Filter** – A 0.1 µF capacitor filters the system identification circuit in the NTSC/PAL decoder.

PIN FUNCTION DESCRIPTION (continued)

FB	FN	Representative Circuitry (Pin numbers refer to PLCC package)	Description (Pin numbers refer to PLCC package)
QFP	PLCC		
Pin			
38	44		**Crystal PLL Filter** – Components at this pin filter the PLL for the crystal chroma oscillator circuit.
4, 11, 13, 17, 18, 33, 34	10, 17, 19, 23, 24, 39, 40	 (Dashed lines indicate substrate connection.)	**Power Distribution** – The three V_{CC} pins must be externally connected to 5.0 V (±5%) supply. The four grounds must be externally tied together, preferably to a ground plane.

Luma Frequency Response (14.3 MHz) Crystal, (4.5 MHz) Sound Trap

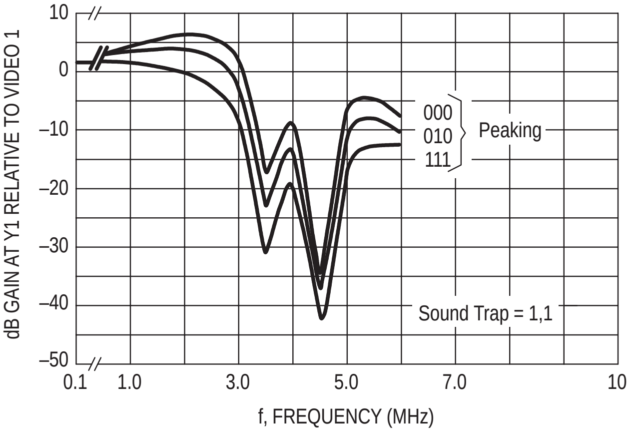


Figure 2. Composite Video Mode

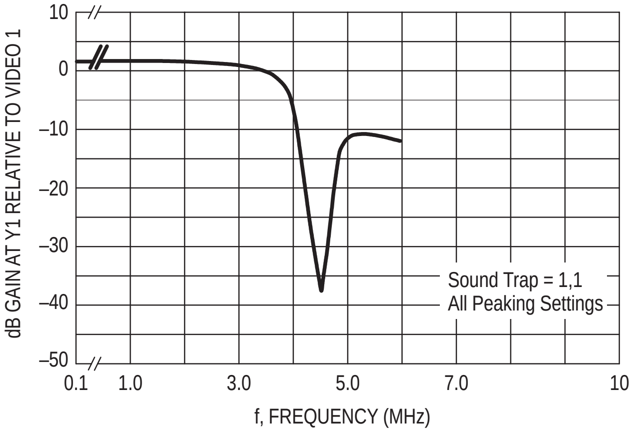


Figure 3. S–VHS Mode

Luma Frequency Response (17.7 MHz) Crystal, (5.5 MHz) Sound Trap

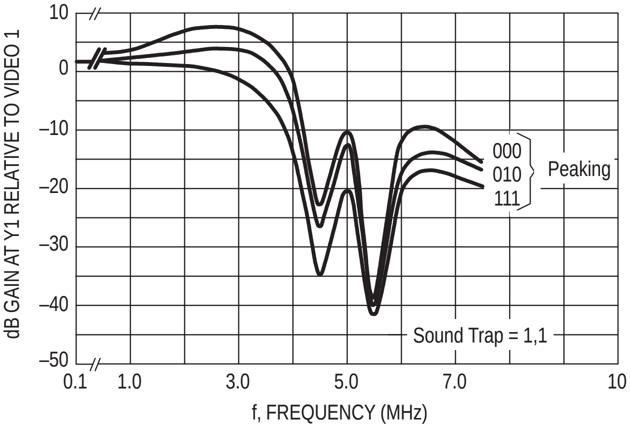


Figure 4. Composite Video Mode

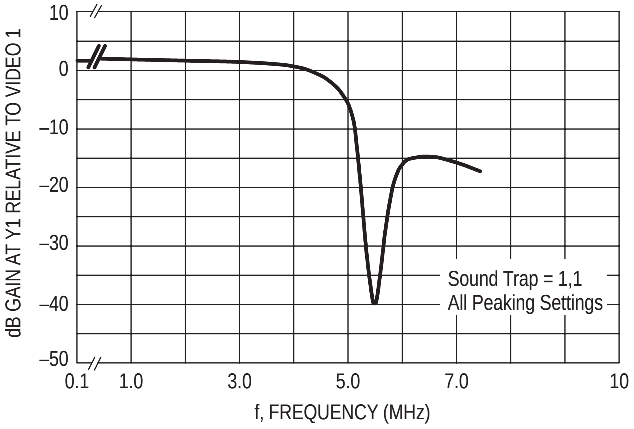


Figure 5. S–VHS Mode

Luma Frequency Response (17.7 MHz) Crystal, (5.5/5.75 MHz) Sound Trap

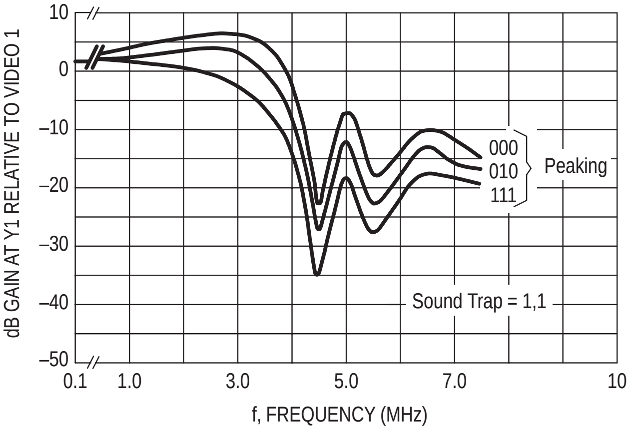


Figure 6. Composite Video Mode

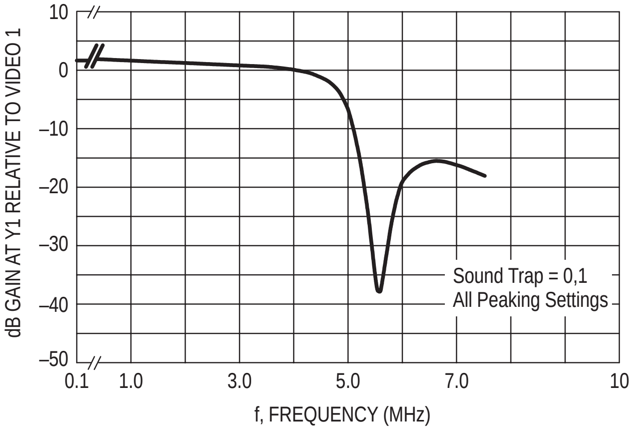


Figure 7. S–VHS Mode

Luma Frequency Response (17.7 MHz) Crystal, (6.0 MHz) Sound Trap

Figure 8. Composite Video Mode

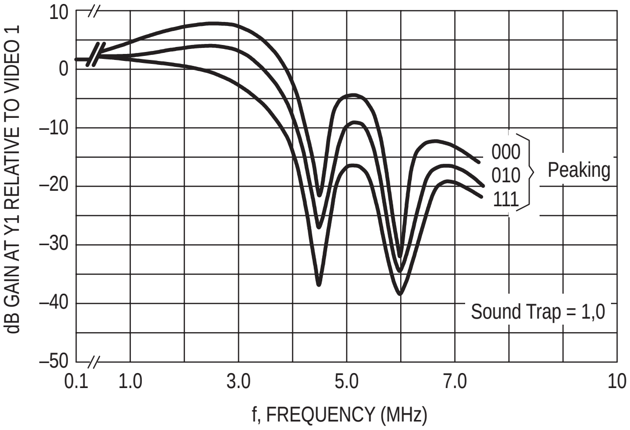
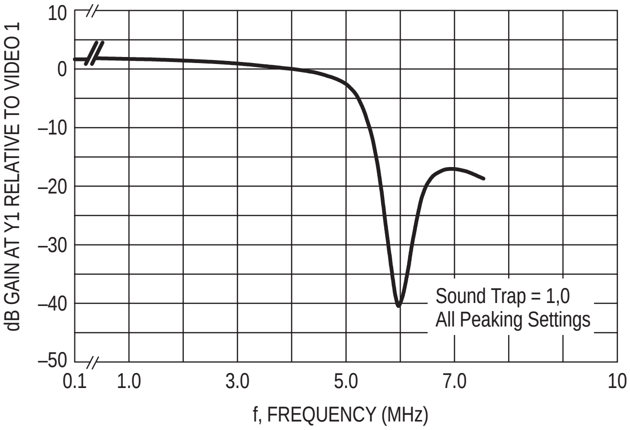


Figure 9. S–VHS Mode



Luma Frequency Response (17.7 MHz) Crystal, (6.5 MHz) Sound Trap

Figure 10. Composite Video Mode

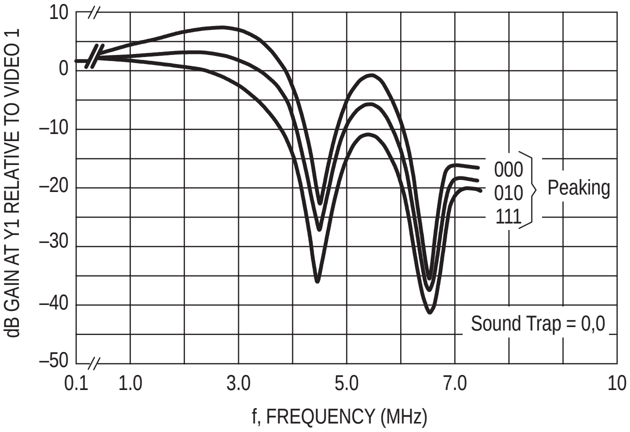


Figure 11. S–VHS Mode

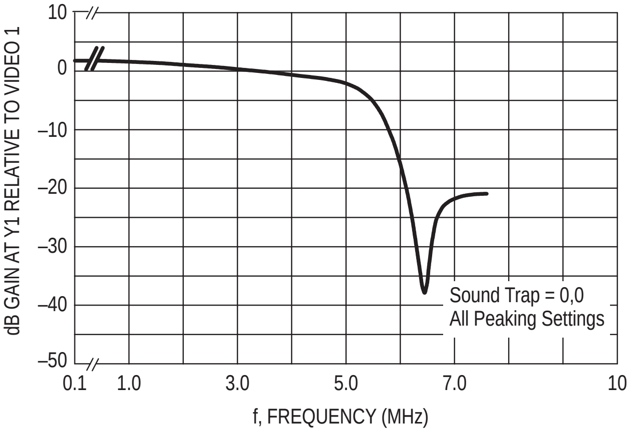


Figure 12. (3.58 MHz) Chroma Notch

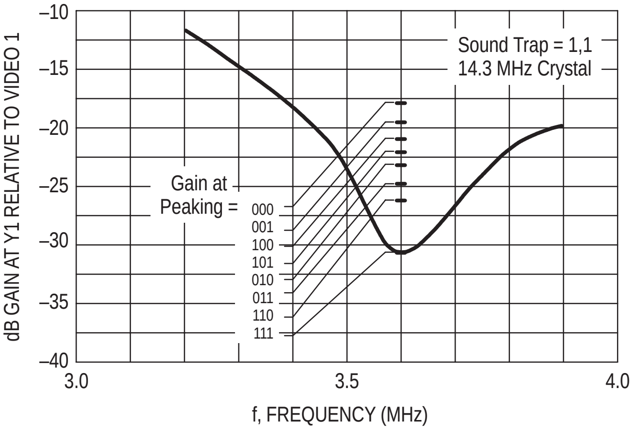
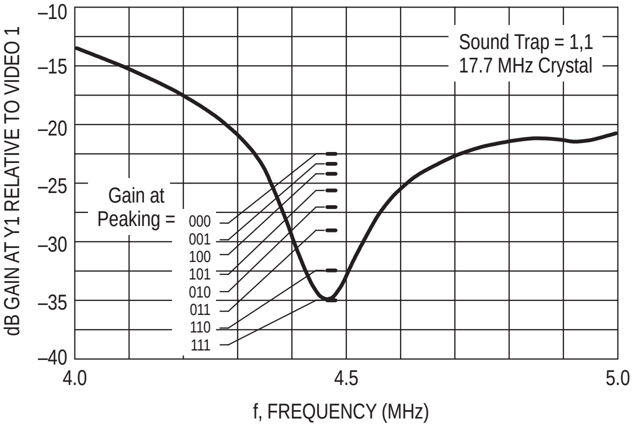


Figure 13. (4.43 MHz) Chroma Notch



(4.5 MHz) Sound Trap

Figure 14. Composite Video Mode

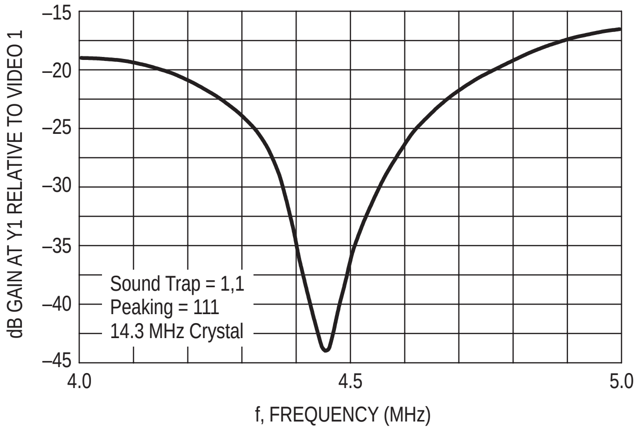
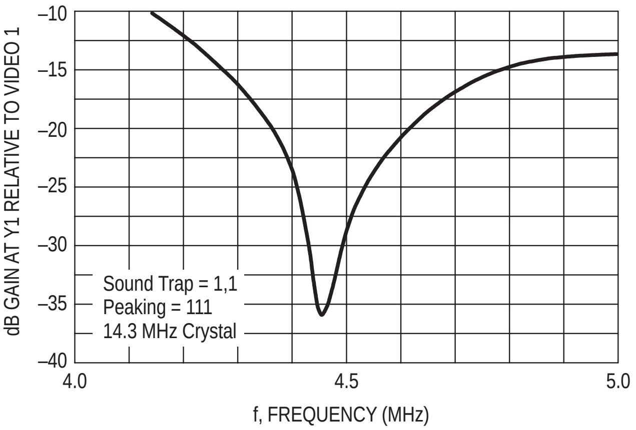


Figure 15. S–VHS Mode



(5.5 MHz) Sound Trap

Figure 16. Composite Video Mode

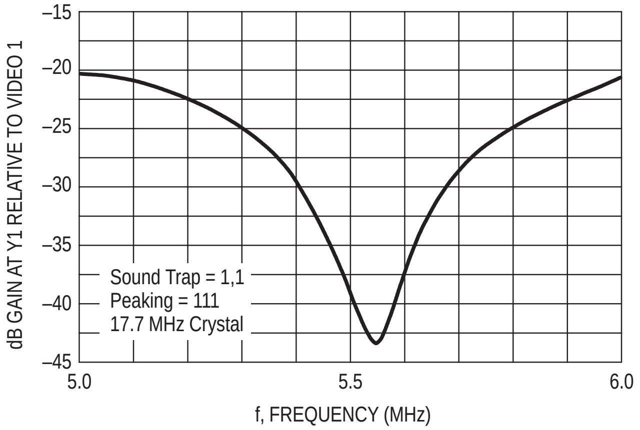
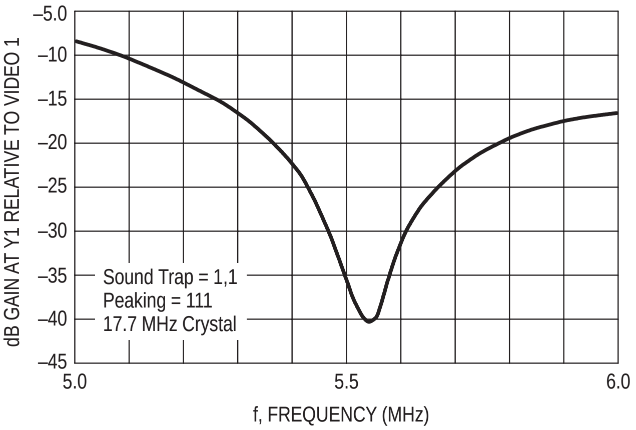


Figure 17. S–VHS Mode



(5.5 + 5.75 MHz) Sound Trap

Figure 18. Composite Video Mode

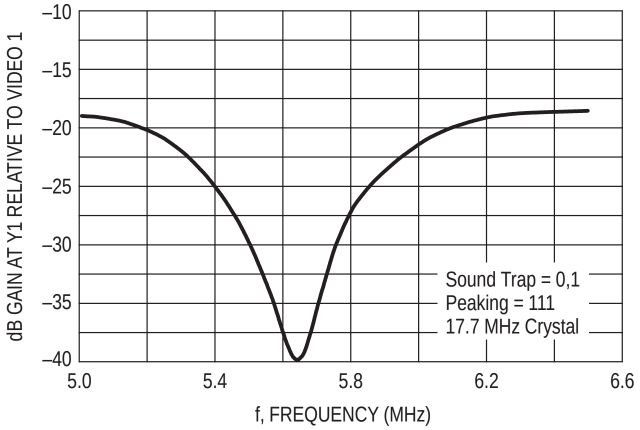
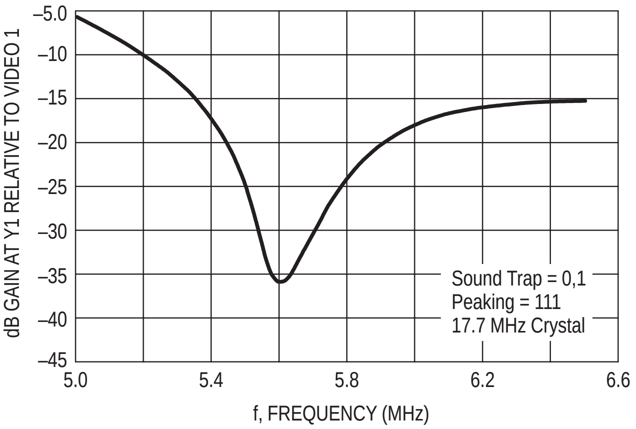


Figure 19. S–VHS Mode



(6.0 MHz) Sound Trap

Figure 20. Composite Video Mode

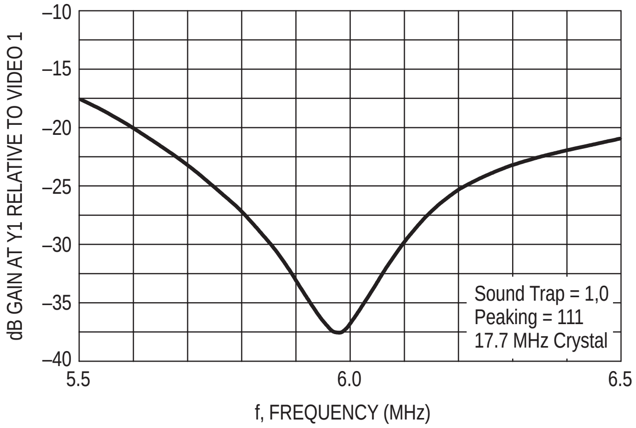
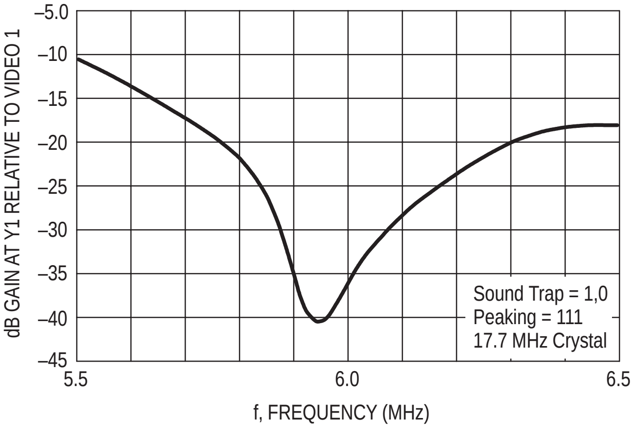


Figure 21. S–VHS Mode



(6.5 MHz) Sound Trap

Figure 22. Composite Video Mode

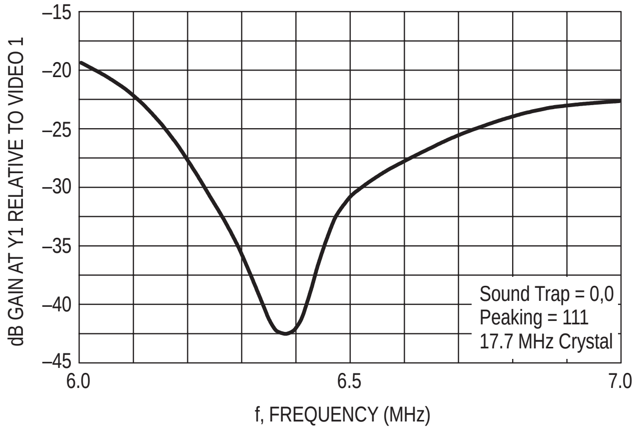


Figure 23. S–VHS Mode

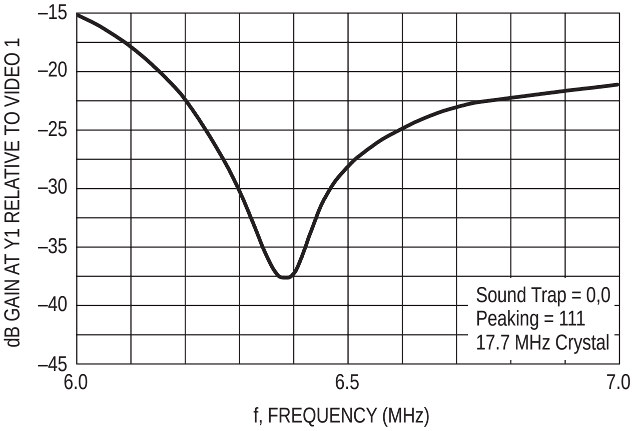


Figure 24. FC Input Current

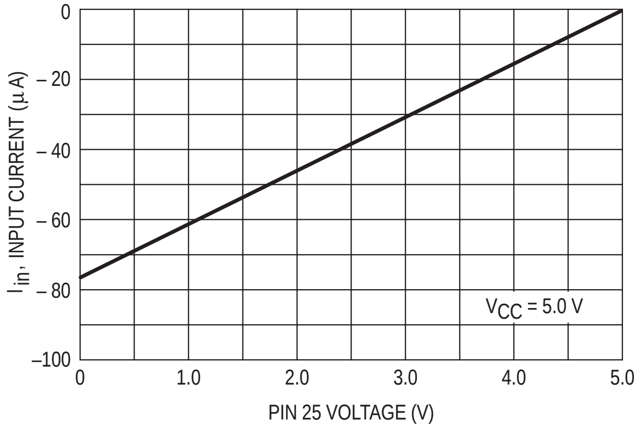
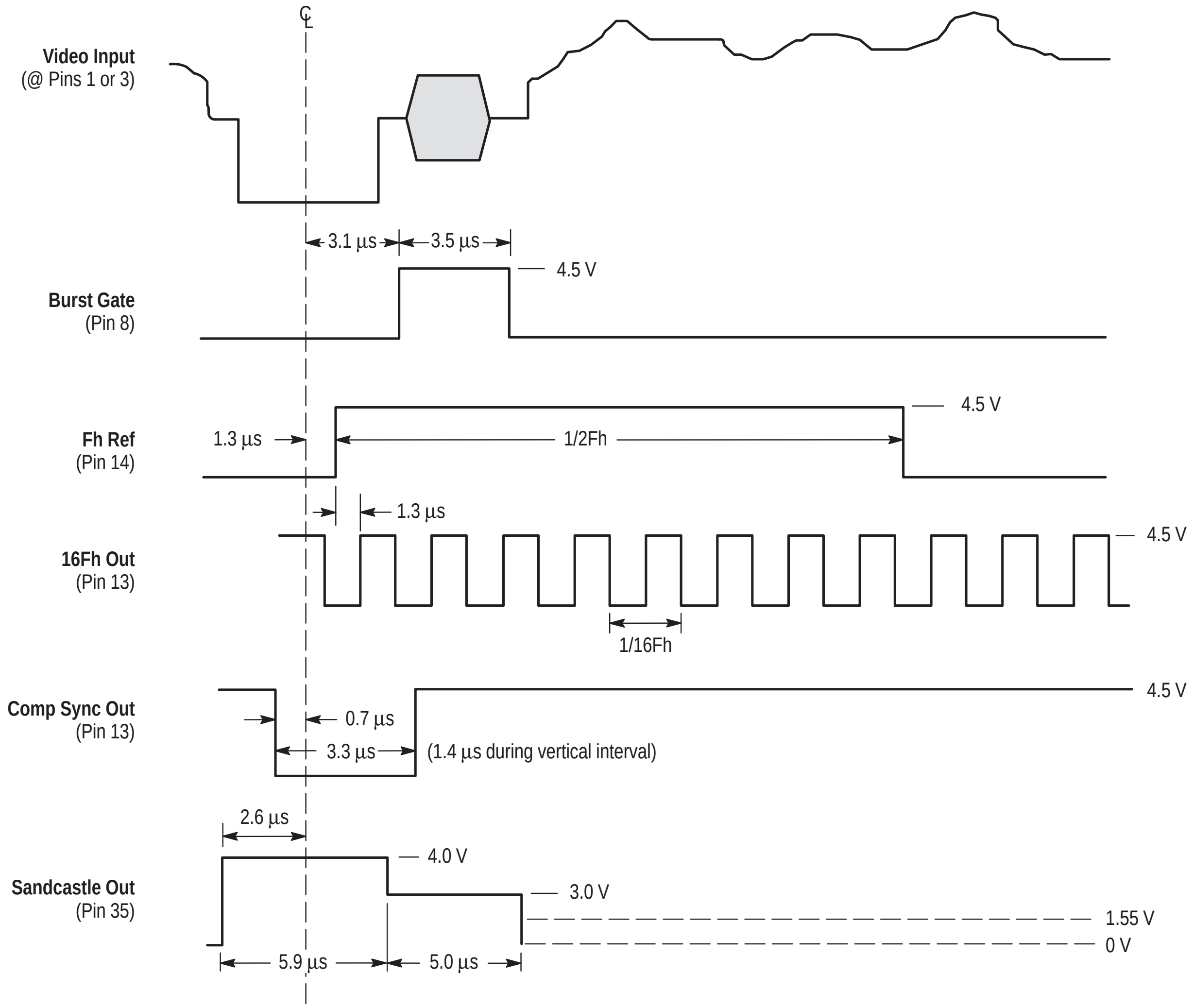


Figure 25. Horizontal PLL1 Timing/Composite Video Inputs



NOTE: In above waveforms, all timing is referenced to the **center** of the incoming Sync Pulse at Pin 1 or 3.
Above timings based on a 4.6 µs wide sync pulse.
Lower two levels of Sandcastle output alternate, based on video system in effect.
All timings are nominal, and apply to both PAL and NTSC signals.

Figure 26. Horizontal PLL1 Noise Gate and Filter Pin

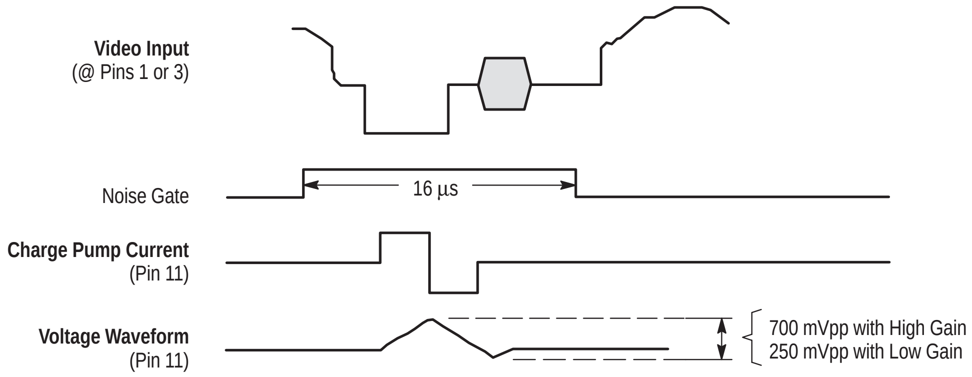
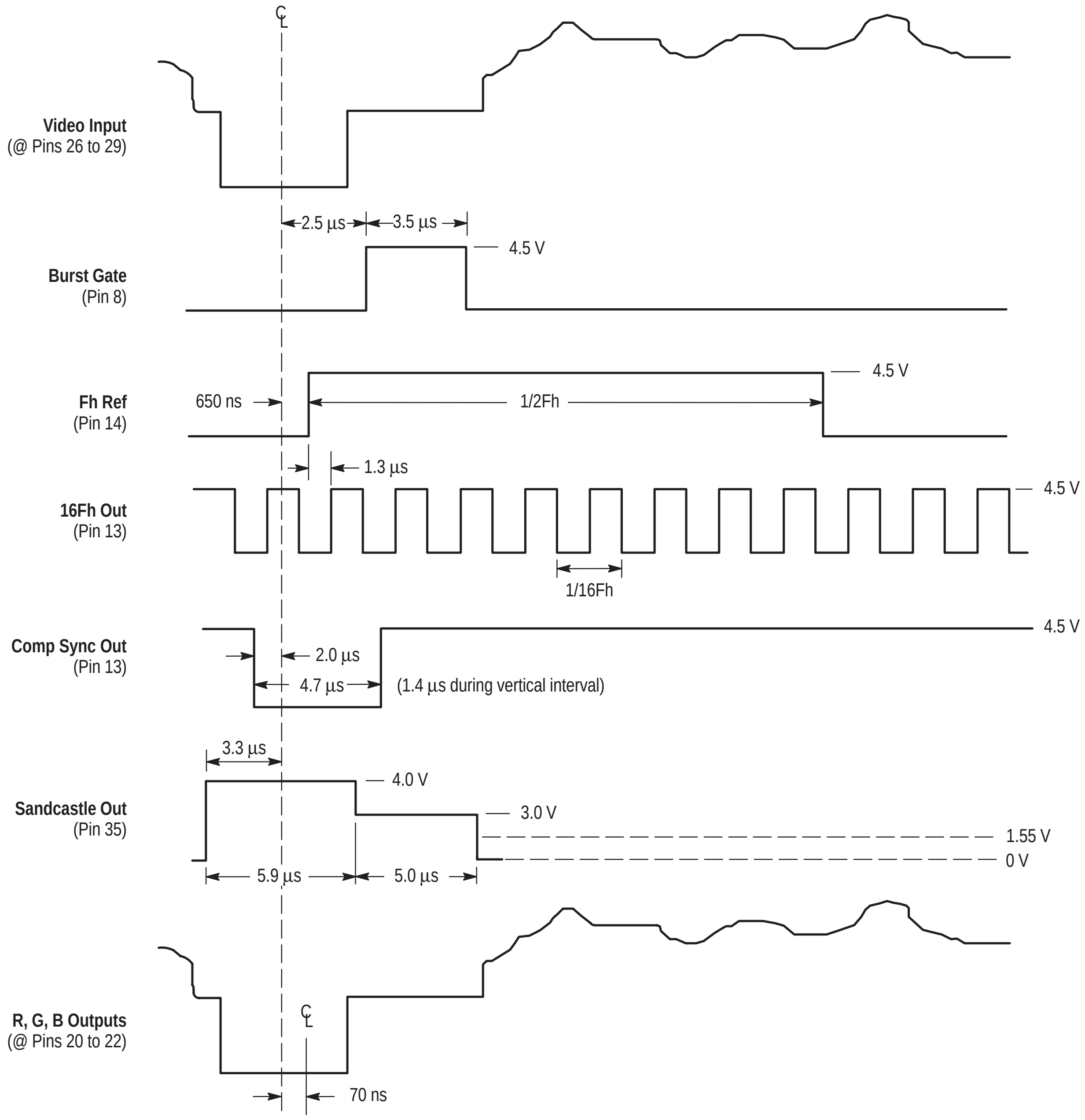


Figure 27. Horizontal PLL1 Timing/R, G, B and Y2 Inputs



NOTE: In above waveforms, all timing is referenced to the **center** of the incoming Sync Pulse at Pin 26 to 28, or 29.
Above timings based on a 4.6 µs wide sync pulse.
Lower two levels of Sandcastle output alternate, based on video system in effect.

Figure 28. System Timing/Video Inputs to RGB Outputs

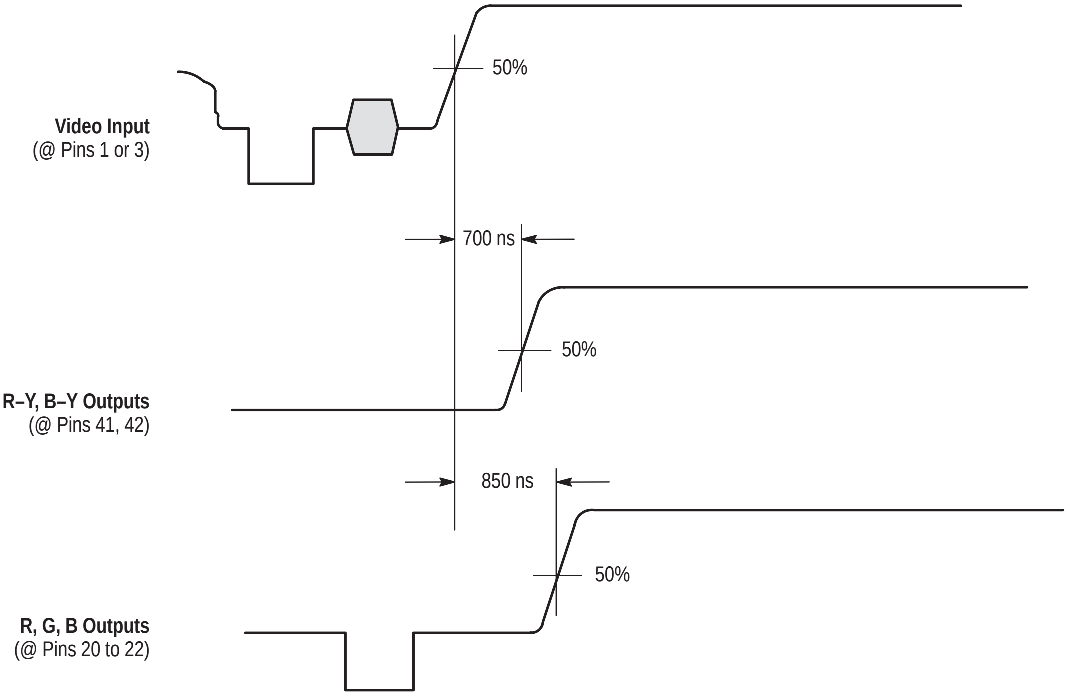


Figure 29. Fast Commutate Timing

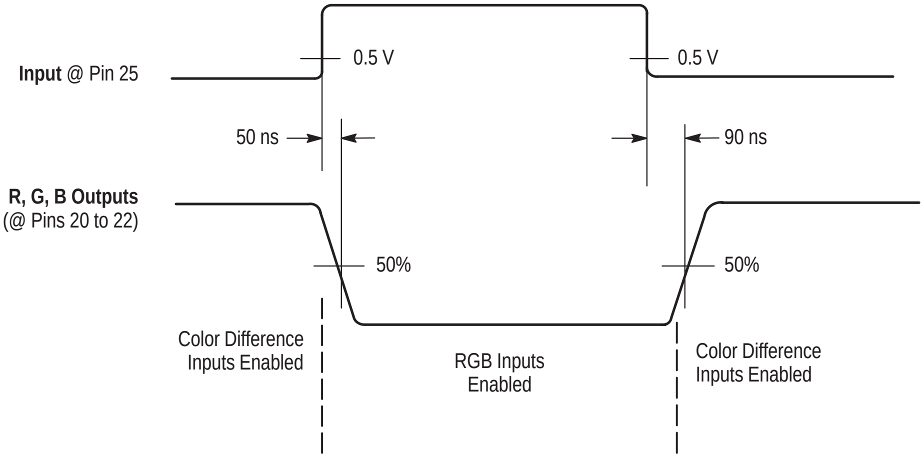


Figure 30. Horizontal Outputs versus Fields (NTSC System)

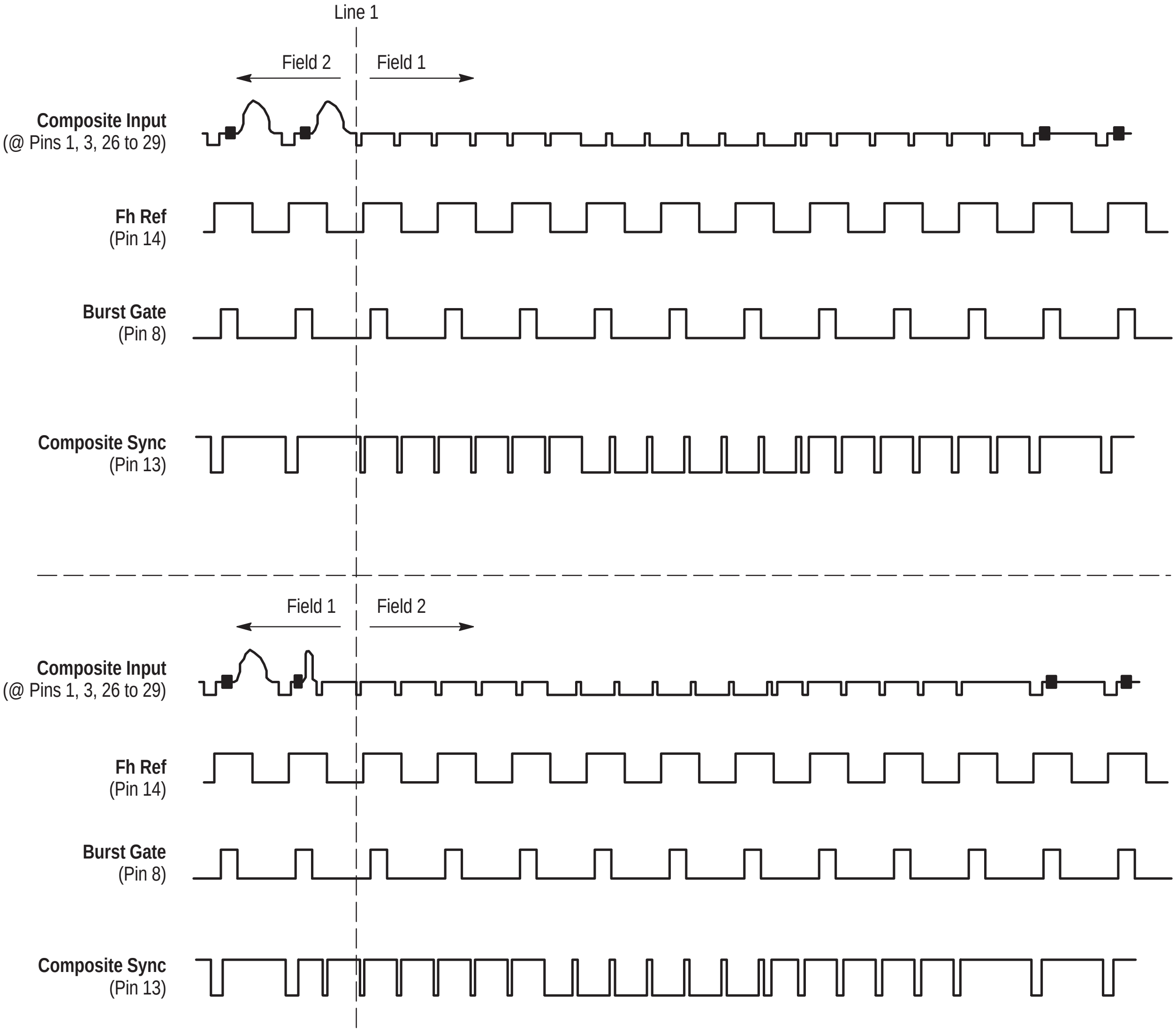


Figure 31. Horizontal Outputs versus Fields (PAL System)

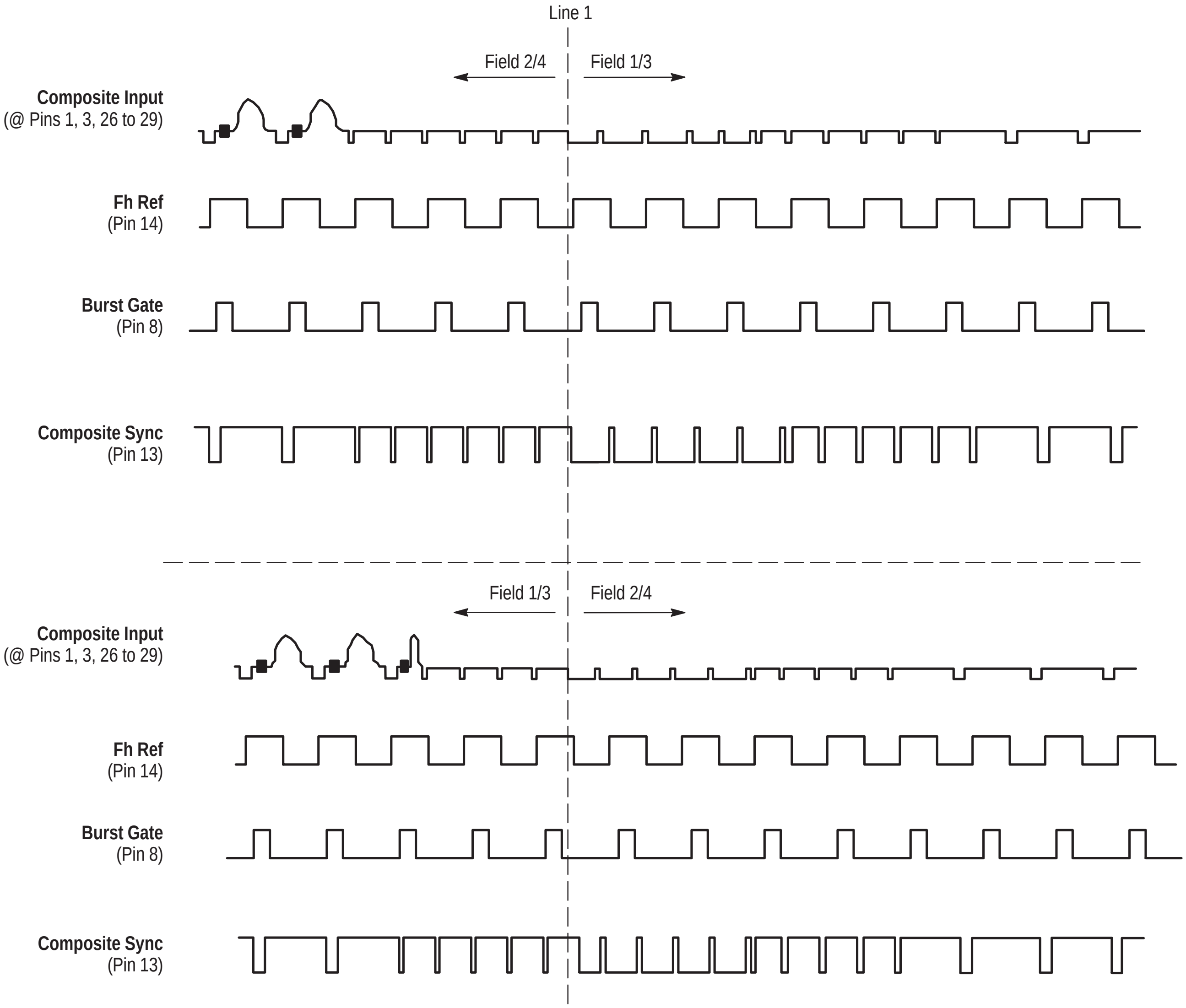


Figure 32. Horizontal PLL2 Timing

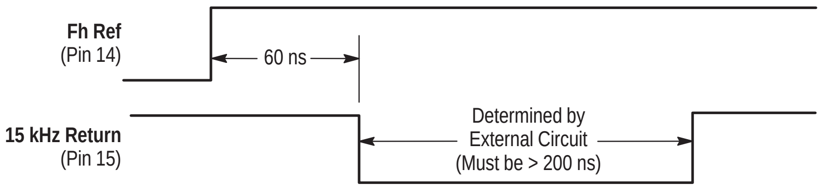


Figure 33. Vertical Timing (NTSC System)

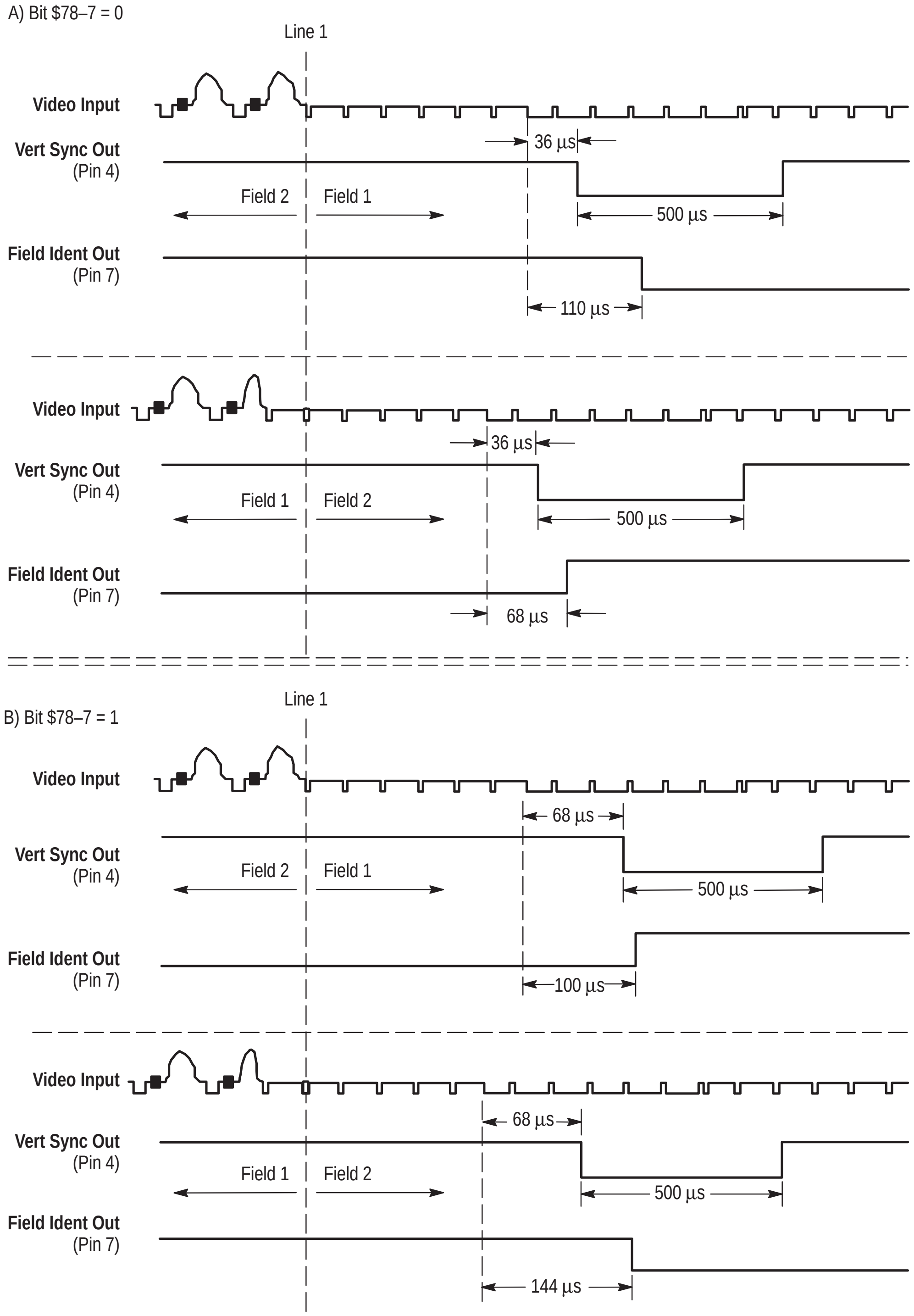
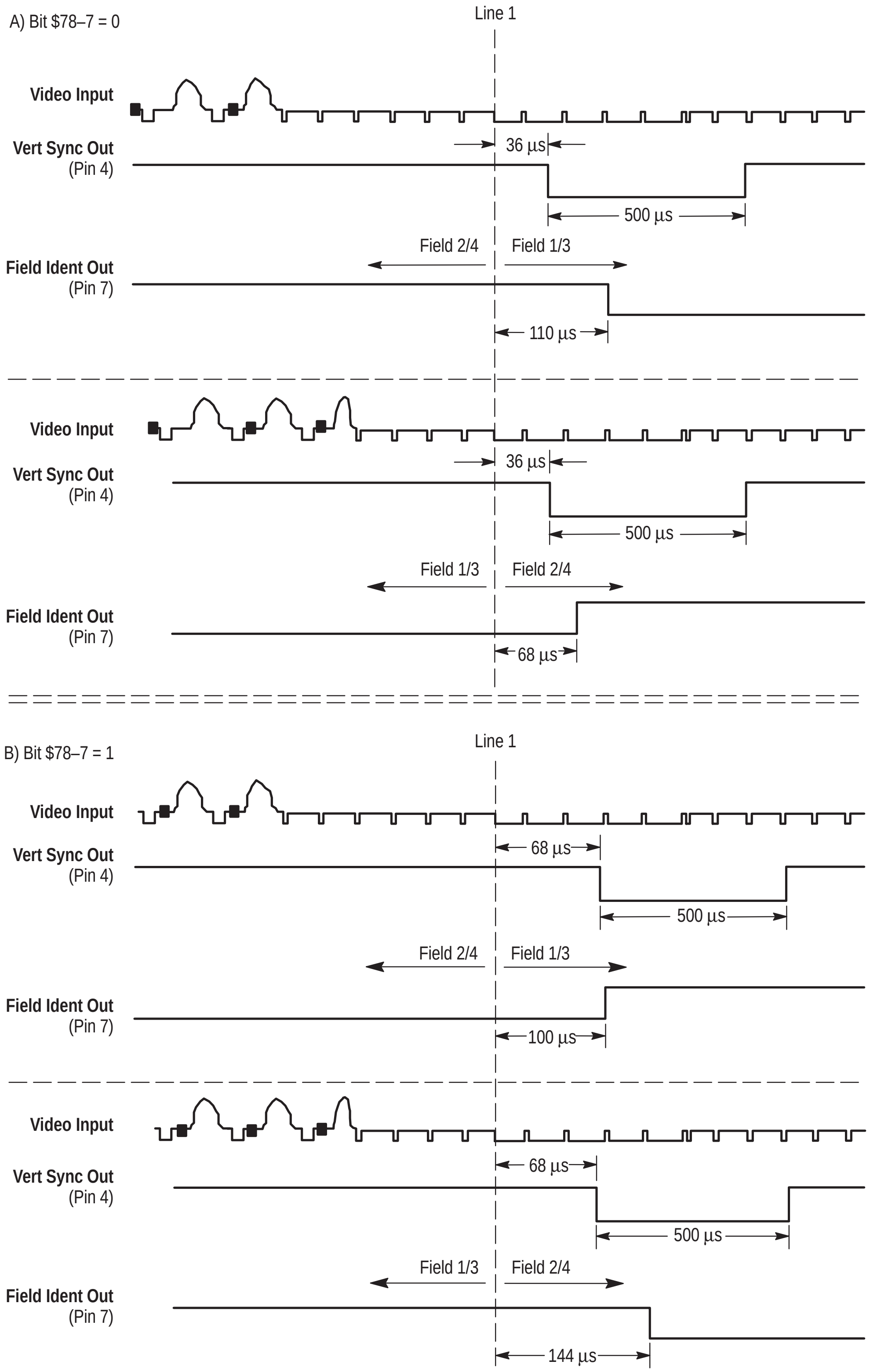


Figure 34. Vertical Timing (PAL System)



FUNCTIONAL DESCRIPTION

Introduction

The MC44011, a member of the MC44000 Chroma 4 family, is a composite video decoder which has been tailored for applications involving multimedia, picture–in–picture, and frame storage (although not limited to those applications). The first stage of the MC44011 provides color difference signals (R–Y, B–Y, and Y) from one of two (selectable) composite video inputs, which are designed to receive PAL, NTSC, and S–VHS (Y,C) signals. The second stage provides either RGB or YUV outputs from the first stage's signals, or from a separate (internally selectable) set of RGB inputs, permitting an overlay function to be performed. Adjustments can be made to saturation; hue; brightness; contrast; brightness balance; contrast balance; U and V bias; subcarrier phase; and color difference gain ratio.

The above mentioned video decoding sections provide the necessary luma/delay function, as well as all necessary filters for sound traps, luma/chroma separation, luma peaking, and subcarrier rejection. External tank circuits and luma delay lines are not needed. For PAL applications, the MC44140 chroma delay line provides the necessary line–by–line corrections to the color difference signals required by that system.

The MC44011 provides a pixel clock to set the sampling rate of external A/D converters. This pixel clock, and other horizontal frequency related output signals, are phase–locked to the incoming sync. The VCO's gain is adjustable for optimum performance. The MC44011 also provides vertical sync and field identification (Field 1, Field 2) outputs.

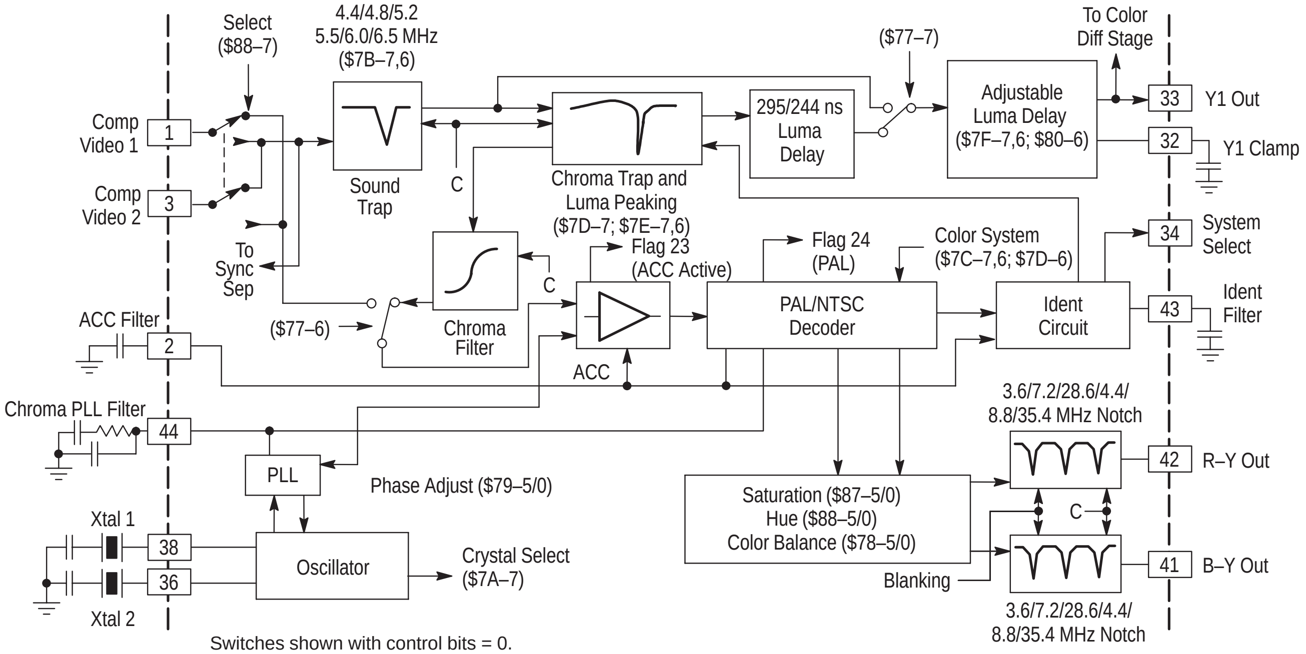
Selection of the various inputs, outputs, and functions, as well as the adjustments, is done by means of a two–wire I^{2}C interface. The basic procedure requires the microprocessor system to read the internal flags of the MC44011, and then set the internal registers appropriately. This I^{2}C interface eliminates the need for manual controls (potentiometers) and external switches. All of the external components for the MC44011, except for the two crystals, are standard value resistors and capacitors, and can be non–precision.

(The DACs mentioned in the following description are 6–bits wide. The settings mentioned for them are given in decimal values of 00 to 63. These are not hex values.)

PAL/NTSC/S–VHS Decoder

A block diagram of this decoder section is shown in Figure 35. This section's function is to take the incoming composite video (at Pins 1 or 3), separate it into luma and chroma information, determine if the signal is PAL or NTSC (for the flags), and then provide color difference and luma signals at the outputs. If the input is S–VHS, the luma/chroma separation is bypassed, but the other functions are still in effect.

Figure 35. PAL/NTSC/S–VHS Decoder Block Diagram



Switches shown with control bits = 0.

Inputs

The inputs at Pins 1 and 3 are high impedance inputs designed to accept standard 1.0 Vpp positive video signals (with negative going sync). The inputs are to be capacitor–coupled so as not to upset the internal dc bias. When normal composite video is applied, the desired input is selected by Bit $88–7. Bits $77–6 and $77–7 must be set to 0 so that their switches are as shown in Figure 35. The selected signal passes through the sound trap, and is then separated by the chroma trap and the chroma (high pass) filter.

When S–VHS signals (Y,C) are applied to the two inputs, Bit $88–7 is used to direct the luma information to the sound trap, and the chroma information to the ACC circuit (Bit $77–6 must be set to a Logic 1). Bit $77–7 is normally set to a Logic 1 in this mode to bypass the first luma delay line and the chroma trap, but it can be left 0 if the additional delay is desired.

Sound Trap

The sound trap will filter out any residual sound subcarrier at the frequency selected by control bits T1 and T2 according to Table 3. The accuracy of the notch frequency is directly related to the selected crystal frequency.

Table 3. Sound Trap Frequency

Crystal Frequency	T1 ($7B–7)	T1 ($7B–6)	Notch Frequency
17.73 MHZ	0	0	6.5 MHz
	0	1	5.5 + 5.75 MHz
	1	0	6.0 MHz
	1	1	5.5 MHz
14.32 MHz	0	0	5.25 MHz
	0	1	4.44 + 4.64 MHz
	1	0	4.84 MHz
	1	1	4.44 MHz

Code 01 (for T1, T2) is used to widen the band rejection where stereo is in use. Typical rejection is 30 dB.

ACC and PAL/NTSC Decoder

The chroma filter bandpass characteristics (3.58 or 4.43 MHz) is determined by the selected crystal. The output of the chroma filter is sent to the ACC circuit which detects the burst signal, and provides automatic gain control once the crystal oscillator has achieved phase lock–up to the burst. The dc voltage at Pin 2 is ≈ 1.5 to 2.0 V. This will occur if the burst amplitude exceeds 30 mVpp, and if the correct crystal is selected (Bit $7A–7). A 17.734472 MHz crystal is required for PAL, and a 14.31818 MHz crystal is required for NTSC. When Flag 23 is high, it indicates that the crystal's PLL has locked up, and the ACC circuit is active, providing automatic gain control. A small amount of phase adjustment (≈ ±5°) of the crystal PLL, for color correction, can be made with control DAC $79–5/0. Pin 2 is the filter for the ACC loop, and Pin 44 is the filter for the crystal oscillator PLL.

The PAL/NTSC decoder then determines if the signal is PAL or NTSC by looking for the alternating phase characteristic of the PAL burst. When Flag 24 is high, PAL has been detected. Bits SSA, SSB, SSC, and SSD (Table 4) must then be sent to the decoder to set the appropriate decoding method.

Table 4. Color System Select

SSA ($7C–6)	SSB ($7D–6)	SSC ($7C–7)	SSD ($7A–6)	Color System
0	0	0	0	Not Used
0	1	0	0	PAL
1	0	0	0	NTSC
1	1	0	0	Color Kill
X	X	1	0	External

Upon receiving the SSA to SSD bits, the decoder provides the correct color difference signals, and with the Identification circuit, provides the correct level at the System Select output (Pin 34). This output is used by the MC44140 delay line.

The color kill setting (SSA = SSB = 1) should be used when the ACC flag is 0, when the color system cannot be properly determined, or when it is desired to have a black–and–white output (the ACC circuit and flag will still function if the input signal has a burst signal). The "External" setting (SSC = 1) is used when an external (alternate) source of color difference signals are applied to the MC44140 delay line. (See Miscellaneous Applications Information for more details.)

Color Difference Controls and Outputs

The color difference signals (R–Y, B–Y) from the PAL/NTSC decoder are directed to the saturation, hue and color balance controls, and then through a series of notch filters before being output at Pins 41 and 42. Blanking and clamping are applied to these outputs.

The saturation control DAC($87–5/0) varies the amplitude of the two signals from 0 Vpp (DAC setting = 00), to a maximum of ≈ 1.8 Vpp (at a DAC setting of 63). The maximum amplitude (without clipping) is ≈ 1.5 Vpp, but a nominal setting is ≈ 1.3 Vpp at a DAC setting of 15.

The hue control ($88–5/0) varies the relative amplitude of the two signals to provide a hue adjustment. The nominal setting for this DAC is 32.

The color balance control ($78–5/0) provides a fine adjustment of the relative amplitude of the two outputs. This provides for a more accurate color setting, particularly when NTSC signals are decoded. The nominal setting for this DAC is 32, and should be adjusted before the hue control is adjusted.

The notch filters provide filtering at the color burst frequency, and at 2x and 8x that frequency. Additionally, blanking and clamping (derived from the horizontal PLL) are applied to the signals at this stage. The nominal output dc level is ≈ 2.0 to 2.5 Vdc, and the load applied to these outputs should be >10 kΩ. Sync is not present on these outputs.

Luma Peaking, Delay Line, and Y1 Output

When composite video is applied, the luma information extracted in the chroma trap is then applied to a stage which allows peaking at ≈ 3.0 MHz with the 17.7 MHz crystal (≈ 2.2 MHz with the 14.3 MHz crystal). The amount of peaking at Y1 is with respect to the gain at the minimum peaking value (P1, P2, P3 = 111), and is adjustable with Bits $7D–7, and $7E–7,6 according to Table 5.

The luma delay lines allow for adjustment of that delay so as to correspond to the chroma delay through this section. Table 6 indicates the amount of delay using the D1–D3 bits ($7F–7,6, and $80–6). The delay indicated is the total delay from Pin 1 or 3 to the Y1 output at Pin 33. The amount of delay depends on whether Composite Video is applied, or YC signals (S–VHS) are applied.

The output impedance at Y1 is ≈ 300 Ω, and the black level clamp is at ≈ 1.1 V. Sync is present on this output. Y1 is also internally routed to the color difference stage.

Table 5. Luma Peaking

P1 ($7D–7)	P2 ($7E–6)	P3 ($7E–7)	Y1 Peaking
0	0	0	9.5 dB
0	0	1	8.5
1	0	0	7.7
1	0	1	6.5
0	1	0	5.3
0	1	1	3.8
1	1	0	2.2
1	1	1	0

17.7 MHz Crystal, 6.5 MHz Sound Trap, Composite Video Mode

Table 6. Luma Delay

D1 ($7F–6)	D2 ($80–6)	D3 ($7F–7)	14.3 MHz Crystal		17.7 MHz Crystal	
			Comp. Video ($77–7 = 0)	S–VHS ($77–7 = 1)	Composite Video ($77–7 = 0)	S–VHS ($77–7 = 1)
0	0	0	690 ns	395 ns	594 ns	350 ns
0	0	1	760	465	650	406
0	1	0	830	535	707	463
0	1	1	900	605	763	519
1	0	0	970	675	819	575
1	0	1	1040	745	876	632
1	1	0	970	675	819	575
1	1	1	1040	745	876	632

Color Difference Stage and RGB/YUV Outputs

A block diagram of this section is shown in Figure 36. This section’s function is to take the color difference input signals (Pins 30, 31), or the RGB inputs (Pins 26 to 28), and output the information at Pins 20 to 22 as either RGB or YUV.

The inputs (on the left side of Figure 36) are analog RGB, or color difference signals (R–Y and B–Y) with Y1 or Y2 as the luma component. Pin 25 (Fast Commutate) is a logic level input, used in conjunction with $\overline{\text{RGB EN}}$ (Bit $80–7), to select the RGB inputs or the color difference inputs. The outputs (Pins 20 to 22) are either RGB or YUV, selected with Bit $82–7. The bit numbers adjacent to the various switches and gates indicate the bits used to control those functions. Table 7 indicates the modes of operation.

Table 7. Color Difference Input/Output Selection

FC	$\overline{\text{RGB EN}}$ $80–7	YX EN $82–6	YUV EN $82–7	Function
1	0	0	0	RGB inputs, RGB outputs, no saturation control
1	0	1	0	RGB inputs, RGB outputs, with saturation control
1	0	1	1	RGB inputs, YUV outputs, with saturation control
1	0	0	1	Not usable
FC Low and/or RGB EN Hi		X	0	R–Y, B–Y inputs, RGB outputs. Y1 or Y2 must be selected
FC Low and/or RGB EN Hi		X	1	R–Y, B–Y inputs, YUV outputs. Y1 or Y2 must be selected

In addition to Table 7, the following guidelines apply:

a. To select the RGB inputs, both FC must be high and RGB EN must be low. Therefore, the RGB inputs can be selected either by the I^2C bus by leaving FC permanently high, or by the FC input by leaving Bit $80–7 permanently low. For overlay functions, where high speed, well controlled switching is necessary, the FC pin must be the controlling input.

b. When the R–Y, B–Y inputs are selected, either Y1 or Y2 must be selected, and the other must be deselected. The YX input is automatically disabled in this mode.

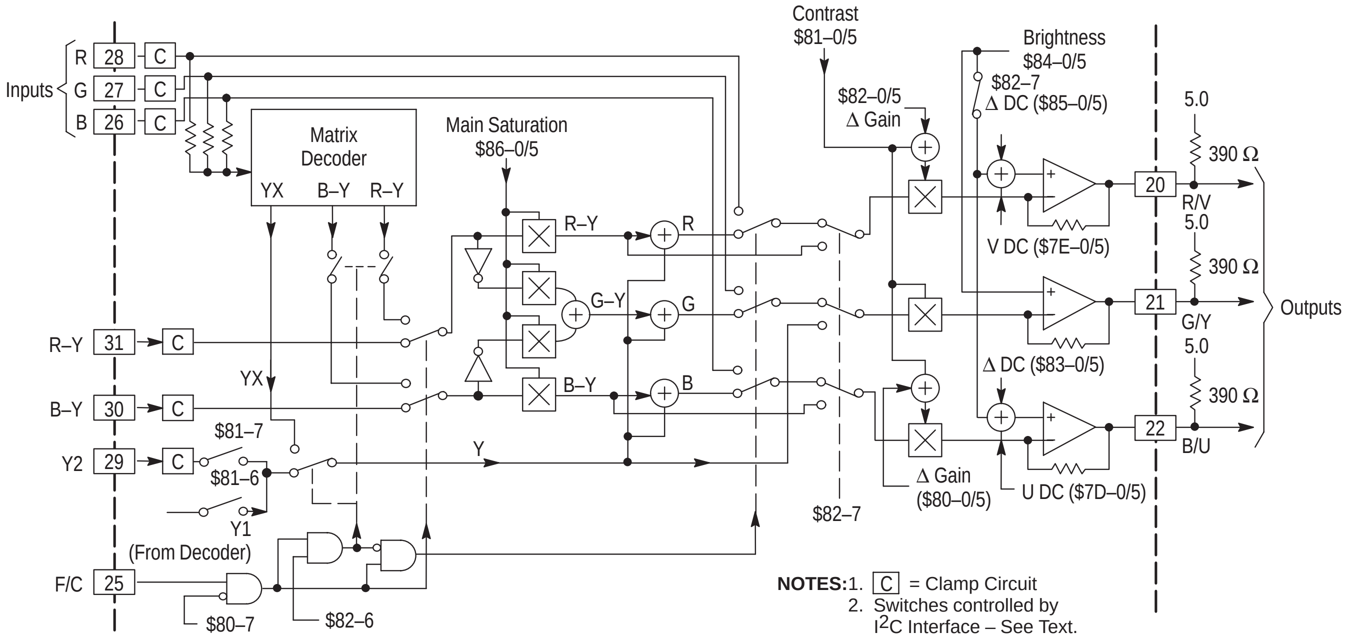
c. In applications where the color difference inputs are obtained from the NTSC/PAL decoder (from a composite video signal), Y1 is used. The Y2 input is normally used where alternately sourced color difference signals are applied, either through the MC44140 delay line, or through other external switching to Pins 30 and 31.

In Figure 36, the bit numbers followed by "–0/5" indicate DAC operated controls (contrast, brightness, etc.), which are controlled by the I^2C bus. The DACs have 6–bit resolution, allowing 64 adjustment steps. Table 8 provides guidelines on the DAC operation.

Table 8. DAC Operation – Color Difference Section

Function	Bits	RGB Outputs ($82–7 = 0)	YUV Outputs ($82–7 = 1)
Brightness	$84–0/5	Affects dc black and maximum levels of the three outputs, but not the clamp level, nor the amplitude.	Affects dc black and white levels of the Y output only, but not the clamp level, nor the amplitude.
Δ DC – Red Δ DC – Blue	$85–0/5 $83–0/5	Fine tune the Red and Blue brightness levels.	Allows a small amount of color tint control (not to be confused with hue).
Contrast	$81–0/5	Provides gain adjustment (black–to–white) of the three outputs.	Provides gain adjustment of the three outputs.
Δ Gain – Red Δ Gain – Blue	$82–0/5 $80–0/5	Fine tune the Red and Blue contrast levels.	Fine tune of the U and V gain levels.
V DC U DC	$7E–0/5 $7D–0/5	Must be set to 00.	Should nominally be set to 32. This sets the dc level of the U and V outputs at ≈ mid–scale.
Main Saturation	$86–0/5	Affects color saturation, except when the RGB inputs bypass this section (YX EN = 0).	Affects color saturation levels of the UV outputs. Does not affect the Y output.

Figure 36. Color Difference Stage and Outputs



NOTES: 1. C = Clamp Circuit
2. Switches controlled by I^2C Interface – See Text.

The RGB and Y2 inputs are designed to accept standard 1.0 Vpp analog video signals. They are not designed for TTL level signals. The color difference inputs are designed to accept signals ranging up to 1.8 Vpp. All signals are to be capacitor–coupled as clamping is provided internally. Input impedance at these six pins is high.

For applications involving externally supplied color difference signals, sync can be supplied on the luma input (Y2), or it can be supplied separately at the RGB inputs. Where the color difference signals are obtained from the NTSC/PAL decoder, sync is provided to this section on the internal Y1 signal. See Sync Separator section for more details on injecting sync into the MC44011.

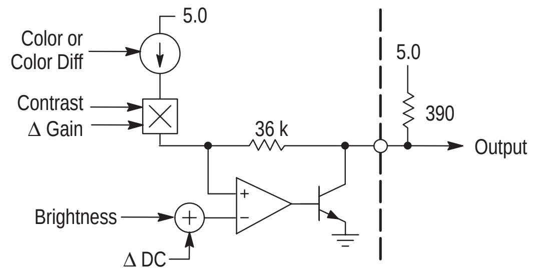
Sync is present on all three outputs in the RGB mode, and on the Y output only (Pin 21) in the YUV mode.

The Fast Commutate input (FC, Pin 25) is a logic level input with a threshold at ≈ 0.5 V. Input impedance is ≈ 67 kΩ, and the graph of Figure 24 shows the input current requirements. Propagation delay from the FC pin to the RGB/YUV outputs is ≈ 50 ns when enabling the RGB inputs, and ≈ 90 ns when disabling the inputs. (See Figure 29 Fast Commutate Timing diagram.) If Pin 25 is open, that is equivalent to a Logic 1, although good design practices dictate that inputs should never be left open. The voltage on this pin should not be allowed to go more than 0.5 V above V_{CC2} or below ground.

The three outputs (Pins 20 to 22) are open–collector, requiring an external pull–up. A representative schematic is shown in Figure 37.

The output amplitude can be varied from 100 mVpp to 3.0 Vpp by use of the contrast and saturation controls. Any output load to ground should be kept larger than 1.0 kΩ. In the RGB mode, DACs $7D and $7E should be set to 00, which results in clamping levels of ≈ 1.4 Vdc. In the YUV mode, DACs $7D and $7E should be set to 00, which results in clamping levels of ≈ 1.4 Vdc. In the YUV mode, the DACs should be set to 32 to bias the U and V outputs to ≈ 2.3 V. The Y output clamp will remain at ≈ 1.4 V in the YUV mode.

Figure 37. Output Stage



Horizontal PLL (PLL1)

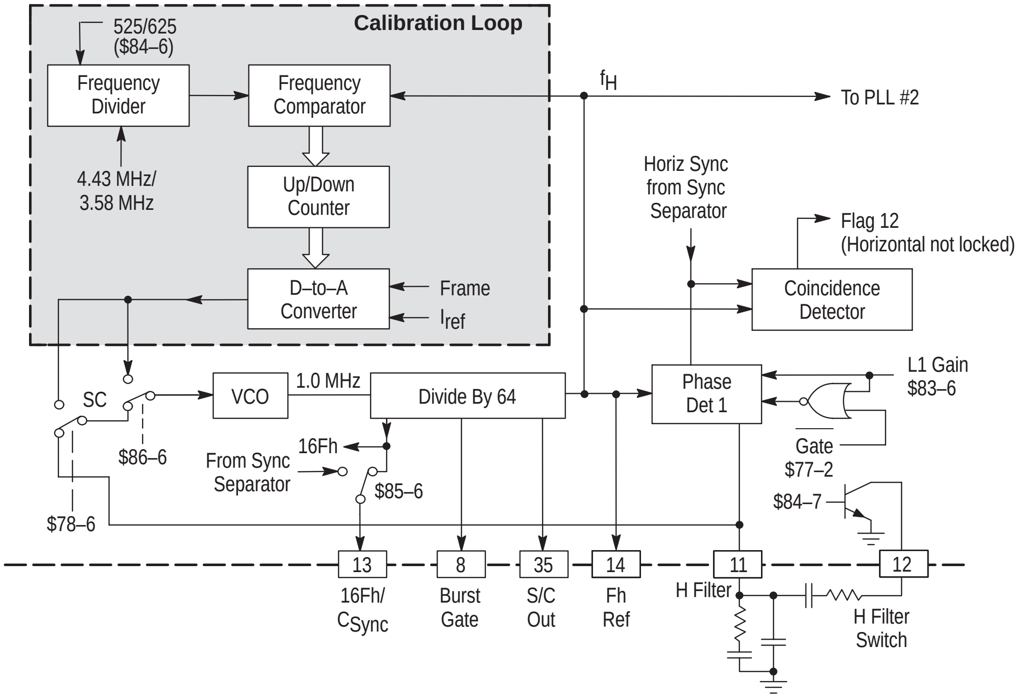
PLL1 (shown in Figure 38) provides several outputs which are phase–locked to the incoming horizontal sync. In normal operation, the two switches at the left side of Figure 38 are as shown, and (usually) the transistor at Pin 12 is off.

The phase detector compares the incoming sync (from the sync separator) to the frequency from the ÷ 64 block. The phase detector's output, filtered at Pin 11, controls the VCO to set the correct frequency (≈ 1.0 MHz) so that the output of the ÷ 64 is equal to the incoming horizontal frequency.

The line–locked outputs are:

1) **Fh Ref** (Pin 14) – A square wave, TTL levels, at the horizontal frequency, and phase–locked to the sync source according to the timing diagram of Figures 25 and 27.
2) **Burst Gate** (Pin 8) – This is a positive going pulse, TTL levels, coincident with the burst signal. See the timing diagram of Figures 25 and 27.

Figure 38. Horizontal PLL (PLL1)



3) **Sandcastle Output** (Pin 35) – This is a multilevel output, at the horizontal frequency, used by the MC44140 delay line. See the timing diagram of Figures 25 and 27.

4) **16Fh/C$_{Sync}$** (Pin 13) – This is a dual purpose output, TTL levels, user selectable. When Bit $85–6 is set to 0, Pin 13 is a square wave at 16x the horizontal frequency (250 kHz for PAL, ≈ 252 kHz for NTSC). When Bit $85–6 is set to 1, Pin 13 is negative composite sync, derived from the internal sync separator. See the timing diagram of Figures 25 and 27.

The first three outputs mentioned above, and Pin 13 when set to 16Fh, are consistent, and do not change duty cycle or wave shape during the vertical sync interval. These four outputs will also be present regardless of the presence of a video signal at the selected input.

When Pin 13 is set to C$_{Sync}$ output, it follows the incoming composite sync format. If there is no video signal present at the selected input, this output will be a steady logic high.

Loading on these pins should not be less than 2.0 kΩ to either ground or 5.0 V.

Pin 11 is the filter for the PLL, and requires the components shown in Figure 38, and with the values shown in the application circuit of Figure 42. Pin 12 is a switch which allows the filtering characteristics at Pin 11 to be changed. Switching in the additional components (set $84–7 = 1) increases the filter time constant, permitting better performance in the presence of noisy signals.

The gain of the phase detector may be set high or low, depending on the jitter content of the incoming horizontal frequency, by using Bit $83–6. Broadcast signals usually have a very stable horizontal frequency, in which case the low gain setting ($83–6 = 0) should be used. When the video source is, for example, a VCR, the high gain setting may be preferable to minimize instability artifacts which may show up on the screen.

The gating function ($77–2) provides additional control where the stability of the incoming horizontal frequency is in question. With this bit set to 0, gating is in effect, causing the phase detector to not respond to the incoming sync pulses during the vertical interval. This reduces disturbances in this PLL due to the half–line pulses and their change in polarity. The gating may be disabled by setting this bit to 1 where the timing of the incoming sync is known to be stable. The gating cannot be enabled if the phase detector gain is set high ($83–6 = 1).

Calibration Loop

The calibration loop (upper left portion of Figure 38) maintains a near correct frequency of this PLL in the absence of incoming sync signals. This feature minimizes re–adjustment and lock time when sync signals are re–applied. The calibration loop is similar to the PLL function, receiving one frequency from the crystal (either 4.43 MHz or 3.58 MHz) divided down to a frequency similar to the standard horizontal frequency. Bit $84–6 is used to set the frequency divider to the correct ratio, depending on which crystal is selected (see Table 9). The output of the frequency comparator operates an up/down counter, which in turn sets the D–to–A converter to drive the VCO through switch Sc. The resulting frequency at the output of the divide–by–64 block is then fed to the frequency comparator to complete the loop.

When a sync signal is not present at Phase Detector #1, and at the Coincidence Detector, as indicated by the coincidence detector’s output (Flag 12), Bit $78–6 should be set to 0. This will cause the switch (Sc) to transfer to the D–to–A converter for two lines (lines 4, 5) in each vertical field, and will maintain the PLL1 at a frequency near the standard horizontal frequency (between 14 to 16 kHz). When lock to an incoming sync is established, Bit $78–6 may be set to 1, disabling the periodic recalibration function, or it may be left set to 0.

If a more accurate horizontal frequency is desired in the absence of an input signal, Bit $86–6. can be set to 1 (and Bit $84–6 set according to Table 9). This holds the horizontal frequency to ≈ 15.7 kHz. In this mode, Flag 12 will stay 0, as the PLL will not be able to lock–up to a newly applied external signal. To reset the system, set $86–6 to 0, write $00 to register $00, and then check Flag 12 to determine when the loop locks to an incoming signal.

Table 9. Calibration Loop

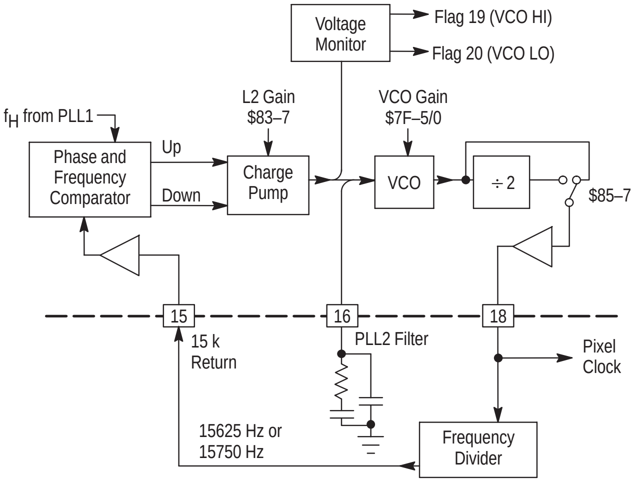
Crystal	Set Bit $84–6 to
14.3 MHz	1
17.7 MHz	0

On initial power up, Bit $86–6 (PLL1 EN) is automatically set to 1, engaging the calibration loop continuously. This condition will remain until this bit is set to 0, and $00 is written to register $00, as part of the initialization routine.

Pixel Clock PLL (PLL2)

The second PLL, depicted in Figure 39, generates a high frequency clock which is phase–locked to the horizontal frequency.

Figure 39. Pixel Clock PLL (PLL2)



The phase and frequency comparator receive inputs from PLL1 (f_H, the horizontal frequency), and the frequency returned from the external divider. Any difference between these two signals causes the Up or Down output to change the charge pump's timing. The charge pump output is composed of two equal current sources which alternately source and sink current to the filter at Pin 16. The voltage at Pin 16 (which is the input to the VCO) is therefore determined by the relative timing of those two current sources, and the filter characteristics. A coarse control of the loop gain is set with Bit $83–7. Low gain is obtained by setting this bit to a 1, which sets the charge pump's output current sources to ≈ ±20 µA. Setting this bit to 0 sets the current sources to ≈ ±50 µA, or high gain.

Depending on the output frequency desired, and whether or not a 50–50 square wave is needed at the pixel clock, the ÷ 2 may be engaged (Bit $85–7). Generally, the ÷ 2 should not be engaged for high frequencies, and should be engaged for low frequencies, so as to keep the VCO's input voltage in a comfortable range (between 1.7 and 3.3 V). If the input voltage is outside this range, Flag 19 or 20 will switch high, indicating the need to fine tune the VCO's gain (control DAC $7F). The usable adjustment range for this DAC is 00 to ≈ 50. Settings of 51 to 62 will generally produce non–square wave outputs, and can be unstable. A setting of 63 will shut off the VCO, which should be done if the pixel clock is not used. When not used, Pin 18 will be at a constant low level.

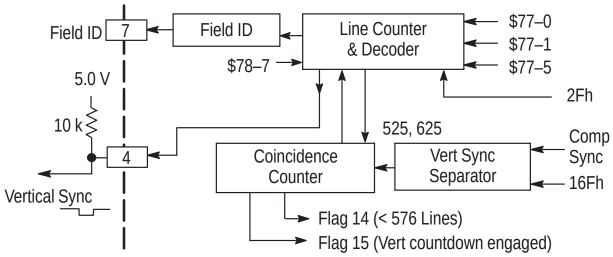
The pixel clock frequency is equal to the horizontal frequency (f_H) x the frequency divider ratio. The frequency divider can be made up of programmable counters (e.g., MC74F161A Applications Information), or it can be integrated into another device (e.g., an ASIC). The returned signal to Pin 15 must be TTL/CMOS logic levels, and must have a low time of > 200 ns. The phase comparator will phase–lock the falling edge of the returned signal with the rising edge of the f_H signal at Pin 14 (see Figure 32).

Vertical Decoder

The vertical decoder section, depicted in Figure 40, provides a vertical sync pulse and a field identification signal, as well as flags which indicate if vertical lockup has occurred, and if the number of horizontal lines per frame is greater or less than 576.

Inputs to this section consists of the composite sync from the sync separator, and horizontal related signals from the horizontal PLL (PLL1).

Figure 40. Vertical Decoder



The sync output (Pin 4) is an active low signal which starts after the horizontal half–line sync pulses change polarity (see Figures 33 and 34). The pulse width is nominally 500 µs for both PAL and NTSC signals. The position of this sync pulse's leading edge can be altered slightly with Bit $78–7, but this does not change the pulse width. Since the pulse width is generated digitally by counters, it will not vary with temperature, supply voltage, or manufacturing distribution. The sync output is an open–collector NPN output, requiring an external pull–up resistor. Minimum value for the pull–up is 1.0 kΩ, with 10 kΩ recommended for most applications.

Flag 14 (< 576 lines) is derived from the counter which compares the number of horizontal lines in each frame with a preset value of 576. This flag can be used externally to help determine whether PAL or NTSC signals are being provided to the MC44011. Flag 15 (Vertical countdown engaged) indicates that the vertical decoder has locked–up to the incoming composite sync information for eight consecutive fields (CB1, CA1 = 11).

The operation of the vertical decoder is controlled by Bits $77–0 and $77–1, according to Table 10.

Table 10. Vertical Decoder Mode

CB1 ($77–1)	CA1 ($77–0)	Vertical Sync Mode
0	0	Force 625
1	0	Force 525
0	1	Injection Lock
1	1	Auto–Count

The Injection Lock mode has a quicker response time, but less noise immunity, than the Auto–Count mode, and is normally used when attempting to lock–up to a new signal (such as when changing video input selection). Flag 15 will not switch high when in this mode. The Auto–Count mode, having a higher noise immunity, should be set once the horizontal PLL is locked–up (by reading Flag 12), and then Flag 15 should be checked after 8 fields for vertical lock–up.

The modes designated Force 525 and Force 625 can be used for those cases where it is desired to force the vertical sync pulse to occur twice every 525 or 625 lines, regardless of the incoming signal. In either of these modes, the MC44011's vertical section will not lock–up to the vertical sync information contained in the incoming composite video signal. If there is no incoming video signal, the vertical sync will still occur every 525 or 625 lines generated by the horizontal PLL. Flag 14 will indicate the number of lines selected, and Flag 15 will be a steady high.

Bit $77–5 (FSI) is used only in the PAL mode to select the vertical sync output rate. With this bit set to 0, the vertical sync pulses will be synchronized with the composite vertical sync input (every 20 ms). With this bit set to 1, the MC44011 will add a second vertical output sync pulse 10 ms after the one occurring at the vertical interval, giving a vertical sync rate of 100 Hz.

The Field ID output (Pin 7) indicates which field is being processed when interlaced signals are applied, but the polarity depends on Bit $78–7. Table 11 indicates Pin 7 output. When non–interlaced signals are being processed, Pin 7 will be a constant high level when $78–7 is set to 1, and will be a constant low level when $78–7 is set to a 0. Loading on Pin 7 should not be less than 2.0 kΩ to either ground or 5.0 V. Figures 33 and 34 indicate the timing.

Table 11. Field ID Output

36/68 μs ($78–7)	Field	Field ID (Pin 7)
1	1	High
1	2	Low
0	1	Low
0	2	High

Sync Separator

The sync separator block provides composite sync information to the horizontal PLL, and to various other blocks within the MC44011 from one of several sources. It also provides composite sync output at Pin 13 when Bit $85–6 = 1. The sync source is selectable via the I^2C bus according to Table 12.

Table 12. Sync Source

V_{in} Sync ($86–7)	Y2 Sync ($87–7)	RGB Sync ($88–6)	Sync Source
0	0	0	None
0	0	1	RGB (Pins 26–28)
0	1	0	Y2 (Pin 29)
1	X	X	Comp. Video (Pins 1, 3)

Setting Bit $86–7 to a 1 overrides the other bits, thereby deriving the sync from the composite video input (either Pin 1 or 3) selected by Bit $88–7.

When RGB is selected, sync information on Pins 26 to 28 is used. Sync may be applied to all three inputs, or to any one with the other two ac grounded. If RGB signals are applied to these pins, sync may be present on any one or all three.

When Y2 is selected, sync information on Pin 29 is used. The sync amplitude applied to any of the above pins must be greater than 100 mV, and it must be capacitor coupled.

This system allows a certain amount of flexibility in using the MC44011, in that if the sync information is not present as part of the applied video signals, sync may be applied to another input. In other words, the input selected for the sync information need not be the same as the input selected for the video information.

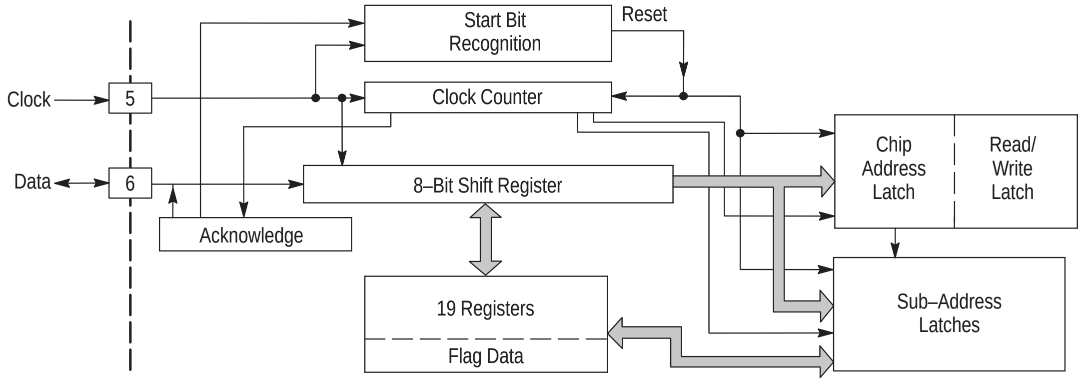
SOFTWARE CONTROL OF THE MC44011

I^2C Interface

Communication to and from the MC44011 follows the I^2C interface arrangement and protocol defined by Philips Corporation. In simple terms, I^2C is a two line, multimaster bidirectional bus for data transfer. See Appendix C for a description of the I^2C requirements and operation. Although an I^2C system can be multimaster, the MC44011 never functions as a master.

The MC44011 has a write address of $8A, and a flag read address of $8B. It requires that an external microprocessor read the internal flags, and then set the appropriate registers. The MC44011 does not do any automatic internal switching when applied video signals are changed. A block diagram of the I^2C interface is shown in Figure 41. Since writing to the MC44011's registers can momentarily create jitter and other undesirable artifacts on the screen, writing should be done only during vertical retrace (before line 20). Reading of flags, however, can be done anytime.

Figure 41. I^2C Bus Interface and Decoder



Write to Control Registers

Writing should be done only during vertical retrace. A write cycle consists of three bytes (with three acknowledge bits):

1) The first byte is always the write address for the MC44011 ($8A).
2) The second byte defines the sub–address register (within the MC44011) to be operated on ($77 through $88, and $00).
3) The third byte is the data for that register.

Communication begins when a start bit (data taken low while clock is high), initiated by the master, is detected, generating an internal reset. The first byte is then entered, and if the address is correct ($8A), an acknowledge is generated by the MC44011, which tells the master to continue the communication. The second byte is then entered, followed by an acknowledge. The third byte is the operative data which is directed to the designated register, followed by a third acknowledge.

Sub–Address Registers

The sub–addresses of the 19 registers are at $77 through $88, and $00. Fourteen of the registers use Bits 0–5 to operate DACs which provide the analog adjustments. Most of the other bits are used to set/reset functions, and to select appropriate inputs/outputs. Table 13 indicates the assignments of the registers.

Table 13. Sub–Address Register Assignments

Sub–Address	7	6	5	4	3	2	1	0
$77	S–VHS Y	S–VHS C	FSI	$\overline{\text{L2 GATE}}$	$\overline{\text{BLCP}}$	$\overline{\text{L1 GATE}}$	CBI	CAI
$78	36/38 μs	Cal Kill	(R–Y)/(B–Y) adjust DAC					
$79	HI	VI	Subcarrier balance DAC					
$7A	Xtal	SSD						
$7B	T1	T2						
$7C	SSC	SSA						
$7D	P1	SSB	Blue bias for YUV operation DAC					
$7E	P3	P2	Red bias for YUV operation DAC					
$7F	D3	D1	Pixel Clock VCO Gain adjust DAC					
$80	$\overline{\text{RGB EN}}$	D2	Blue Contrast trim DAC					
$81	Y2 EN	Y1 EN	Main Contrast DAC					
$82	YUV EN	YX EN	Red Contrast trim DAC					
$83	L2 Gain	L1 Gain	Blue Brightness trim DAC					
$84	H Switch	525/625	Main Brightness DAC					
$85	PClk/2	C Sync	Red Brightness trim DAC					
$86	V_{in} Sync	$\overline{\text{PLL1 En}}$	Main Saturation DAC (Color Difference section)					
$87	Y2 Sync	0	(R–Y)/(B–Y) Saturation balance DAC (Decoder section)					
$88	V2/V1	RGB Sync	Hue DAC					
$00	Set to $00 to start Horizontal Loop if $88–6 = 0							

Table 14 is a brief explanation of the individual control bits. A more detailed explanation of the functions is found in the block diagram description of the text (within the Functional Description section). Table 15 provides an explanation of the DACs. Each DAC is 6 bits wide, allowing 64 adjustment steps. The proper sequence and control of the bits and DACs, to achieve various system functions, is described in the Applications Information section.

Table 14. Control Bit Description

Control Bit	Name	Description
$77–7	S–VHS–Y	Set to 0 for normal Composite Video inputs at V1 and/or V2 (Pins 1, 3). Set to 1 for S–VHS (YC) operation. When 1, the Y–input at the selected video input (V1 or V2, selected by Bit $88–7) bypasses the initial luma delay line, and associated luma/chroma filters and peaking. The signal passes through the second luma delay, adjustable with Bits D1–D3. Luma is output at Pin 33.
$77–6	S–VHS–C	Set to 0 for normal Composite Video inputs at V1 and/or V2 (Pins 1, 3). Set to 1 for S–VHS (YC) operation. When 1, the chroma input at the non–selected video input (V1 or V2 by Bit $88–7) is directed to the ACC loop and PAL/NTSC detector. Color difference signals are then output at Pins 41 and 42.
$77–5	FSI	Set to 0 for a Vertical Sync output rate of 50 Hz. Set to 1 for 100 Hz. Useable in PAL systems only.
$77–4	$\overline{\text{L2 GATE}}$	When set to 0, the pixel clock charge pump (PLL2) operation is inhibited during the Vertical Retrace to minimize momentary instabilities. When set to 1, PLL2 operation is not inhibited.
$77–3	$\overline{\text{BLCP}}$ $\overline{\text{GATE}}$	When 0, Vertical Gating of the black level clamp pulse during the Vertical Retrace occurs to minimize momentary instabilities. The Vertical Gating can be inhibited by setting this bit to 1.
$77–2	$\overline{\text{L1 GATE}}$	When set to 0, the horizontal PLL's phase detector (PLL1) operation is inhibited during the Vertical Retrace to minimize momentary instabilities. When set to 1, the phase detector is not inhibited. If PLL1 gain is high (Bit $83–6 = 1), gating cannot be enabled.
$77–1, 0	CB1, CA1	Sets the Vertical Timebase operating method according to Table 10.
$78–7	36/68 µs	When 0, the time delay from the sync polarity reversal within the Composite Sync to the leading edge of the Vertical Sync output (Pin 4) is 36 µs. When 1, the time delay is 68 µs. (See Figure 33 and 34).
$78–6	CalKill	When 0, the Horizontal Calibration Loop is enabled for two lines (lines 4 and 5) in each field. When 1, the Calibration Loop is not engaged. Upon power–up, this bit is ineffective (Calibration Loop is enabled) until bit $86–6 is set to 0, and register $00 is set to $00.
$79–7	HI	This bit is not used in the MC44011, and must be set to 1.
$79–6	VI	This bit is not used in the MC44011, and must be set to 1.
$7A–7	Xtal	When 0, the crystal at Pin 38 (17.7 MHz) is selected. When 1, the crystal at Pin 36 (14.3 MHz) is selected.
$7A–6	SSD	This bit is not used in the MC44011, and must be set to 0.
$7B–7, 6	T1, T2	Used to set the Sound Trap Notch filter frequency according to Table 3.
$7C–7, 6 $7D–6	SSC, SSA, SSB	Sets the NTSC/PAL decoder to the correct system according to Table 4.
$7D–7 $7E–7, 6	P1, P2, P3	Sets the Luma Peaking in the decoder section according to Table 5. (See text).
$7F–7, 6 $80–6	D3, D1, D2	Sets the Luma Delay in the decoder section according to Table 6. (See text).
$80–7	$\overline{\text{RGB EN}}$	When 0, permits the RGB inputs (Pins 26 to 28) to be selected with the Fast Commutate (FC) input (Pin 25). When 1, the FC input is disabled, preventing the RGB inputs from being selected. When the RGB inputs are selected, the Color Difference inputs (Pins 30, 31) are deselected.
$81–7	Y2 EN	When 1, the Y2 Luma input (Pin 29) is selected. When 0, it is deselected.
$81–6	Y1 EN	When 1, the Y1 Luma Signal (provided by the decoder section to the color difference section) is selected. When 0, it is deselected.
$82–7	YUV EN	When 0, Pins 20 to 22 provide RGB output signals. When 1, those pins provide YUV output signals.
$82–6	YX EN	Effective only when the RGB inputs are selected. When 0, the RGB inputs (Pins 26 to 28) are directed to the RGB outputs (Pins 20 to 22) via the Contrast and Brightness controls. When 1, the RGB inputs are directed through the Color Difference Matrix, allowing Saturation control in addition to the Brightness and Contrast controls. See Figure 36.
$83–7	L2 Gain	When 0, the gain of the pixel clock VCO (PLL2) is high (50 µA). When 1, the gain is low (20 µA).
$83–6	L1 Gain	When 0, the Horizontal Phase Detector Gain (PLL1) is low. When 1, the gain is high.
$84–7	H Switch	When 0, Pin 12 is open. When 1, Pin 12 is internally switched to ground, allowing the PLL1 filter operation to be adjusted for noisy signals.
$85–7	PClk/2	When 0, the PLL2 VCO provides the Pixel Clock at Pin 18 directly. When 1, the VCO output is directed through a ÷ 2 stage, and then to Pin 18.

Table 14. Control Bit Description (continued)

Control Bit	Name	Description
$84–6	525/625	This bit sets the division ratio from the crystal for the reference frequency for the Horizontal Calibration Loop. For NTSC systems, set to 1. For PAL systems, set to 0.
$85–6	C Sync	When 0, Pin 13 will provide a square wave of ≈ 250 kHz (16 x Fh). When 1, Pin 13 provides a negative composite sync signal. See Figures 25, 27, 30, 31.
$86–7	V_{in} Sync	When 1, Composite Sync at the selected Video input (Pin 1 or 3) is used for all internal timing. When 0, the Sync source is selected by Bits $87–7 and $88–6. See Table 12.
$86–6	PLL1 Enable	After power up, this bit must be set to 0, and then register $00 set to $00, to enable the Horizontal Loop (PLL1). Setting this bit to a 1 will disable the Horizontal Loop, and engages the Calibration Loop.
$87–7	Y2 Sync	When 1, and $86–7 = $88–6 = 0, Composite Sync at the Y2 input (Pin 29) is used for all internal timing. When 0, the Sync source is selected by Bits $86–7 or $88–6. See Table 12.
$87–6	0	This bit must always be set to 0.
$88–7	V2/V1	When Composite Video is applied, and this bit is 0, the Video 2 input (Pin 3) is directed to the Sound Trap. When 1, the Video 1 input (Pin 1) is selected. In S–VHS applications, when 0, Pin 3 is the Y (luma) input, and Pin 1 is the chroma input. When this bit is 1, Pin 1 is the luma input, and Pin 3 is the chroma input.
$88–6	RGB Sync	When 1, and $86–7 = $87–7 = 0, Composite Sync at any or all of the RGB inputs (Pin 26 to 28) is used for all internal timing. When 0, the sync source is selected by Bits $86–7 or $87–7. See Table 12.

Table 15. Control DAC Description

Control Bits	Description
$78–5/0	This DAC allows for a relative gain adjustment of the R–Y and B–Y outputs (Pins 41, 42) as a means of adjusting the color decoding accuracy. Nominal setting is 32.
$79–5/0	Used to balance out reference errors of the color subcarrier, primarily for NTSC. Nominal setting is 32. Adjustment range is ≈ ±5°.
$7D–5/0	Used to set the U (Pin 22) dc bias level. When in the YUV mode ($82–7 = 1), this setting should nominally be 32. When in RGB mode, set to 00.
$7E–5/0	Used to set the V (Pin 22) dc bias level. When in the YUV mode ($82–7 = 1), this setting should nominally be 32. When in RGB mode, set to 00.
$7F–5/0	Used to fine tune the gain of the Pixel Clock VCO to obtain optimum performance without instabilities. A setting of 63 will shut off the VCO. Setting 50 to 62 provide non–square wave outputs, and can be unstable. As the setting is increased from 00 to 49, the gain is increased. Changing this register does not change the Pixel Clock frequency.
$80–5/0	Used to fine tune the contrast of the Blue output when in RGB mode. In YUV mode this provides a fine tuning of the color, similar to, but not to be confused with, hue.
$81–5/0	Used to adjust the gain of the three outputs. In RGB mode this is the Contrast control.
$82–5/0	Used to fine tune the contrast of the Red output when in RGB mode. In YUV mode this provides a fine tuning of the color, similar to, but not to be confused with, hue.
$83–5/0	Used to fine tune the brightness of the Blue output when in RGB mode. In YUV mode this provides a fine tuning of the color, similar to, but not to be confused with, hue.
$84–5/0	Used to adjust the brightness of the three RGB outputs. In YUV mode this DAC affects only Y output (Pin 21).
$85–5/0	Used to fine tune the brightness of the Red output when in RGB mode. In YUV mode this provides a fine tuning of the color, similar to, but not to be confused with, hue.
$86–5/0	Used to adjust the saturation of the RGB/YUV outputs of the Color Difference section.
$87–5/0	Used to adjust the saturation of the R–Y, B–Y outputs (Pins 41, 42) of the Decoder section.
$88–5/0	Used to adjust the hue of the R–Y, B–Y outputs (Pins 41, 42). Nominal setting is 32.
$00–7/0	This register must be set to 00, after Bit $86–6 is set to 0, to enable the Horizontal Loop (PLL1) after power up, or anytime when Bit $86–6 is set to 0 after having been a 1.

NOTE: The above DACs are 6–bits wide. The settings mentioned above, and in subsequent paragraphs are given in decimal values of 00 to 63. These are not hex values.

Reading Flags

A read cycle need not be restricted to the vertical interval, but may be done anytime. A flag read cycle consists of three bytes (with three acknowledge bits):

- The first byte is always the Read address for the MC44011 ($8B).
- The second and third bytes are the flag data.

Communication begins when a start bit (data taken low while clock is high), initiated by the master (not the MC44011), is detected, generating an internal reset. The first byte (address) is then entered, and if correct, an acknowledge is generated by the MC44011. The flag bits will then exit the MC44011 as two 8 bit bytes at clock cycles 10–17 and 19–26. The master (receiving the data) is expected to generate the acknowledge bits at clocks 18 and 27. The master must then generate the stop bit.

The MC44011 flags must be read on a regular basis to determine the status of the various circuit blocks. The MC44011 does not generate interrupts. It is recommended the flags be read once per field or frame. See Table 16 for a description of the flags.

Table 16. Flag Description

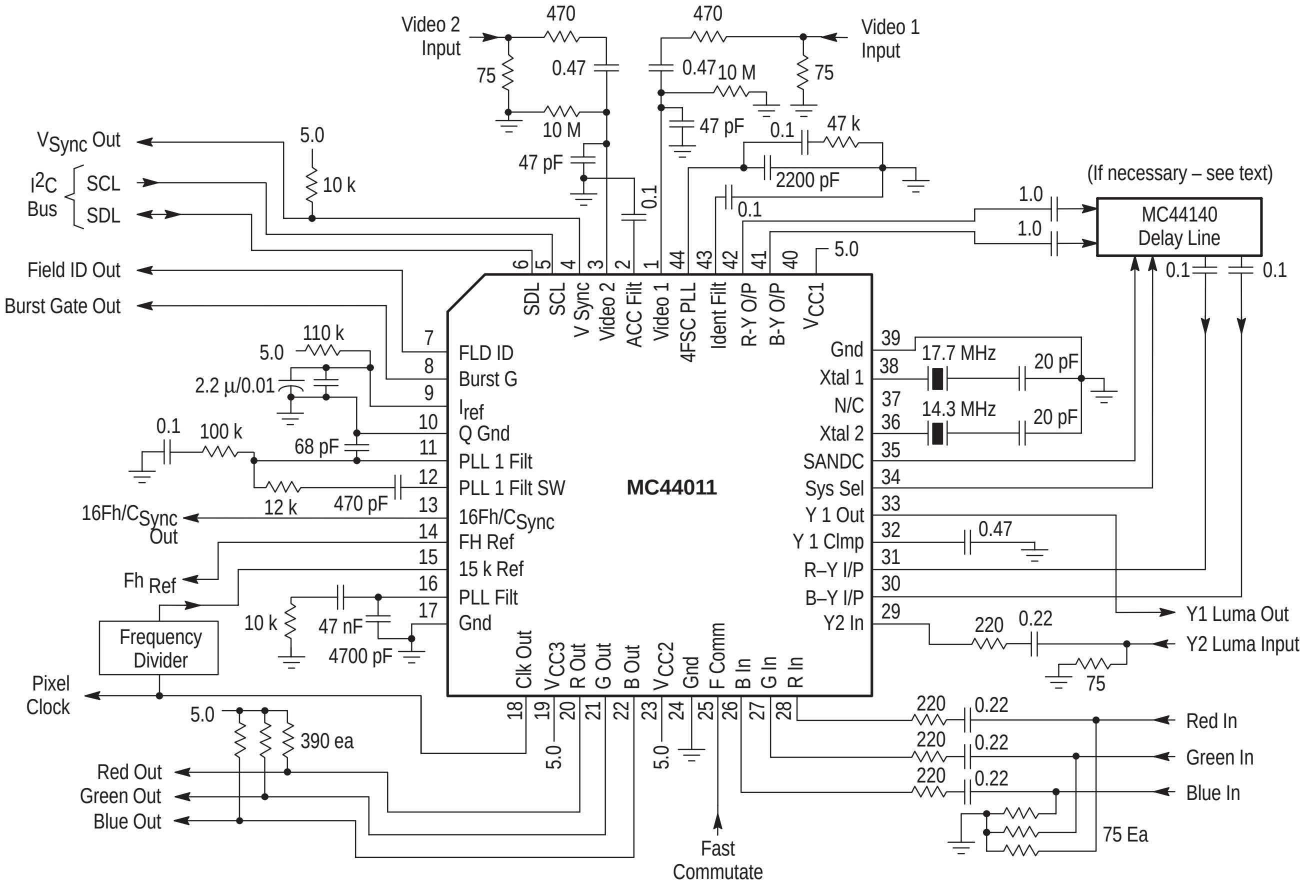
Clock No.	Description (When Flag = 1)
10	Internally set to a Logic 1.
11	Horizontal Loop (PLL1) enabled, indicating the loop can be driven by the incoming sync. This bit will be low upon power up, and will change to a 1 after initialization of control Bit $86–6 and register $00.
12	Horizontal Loop (PLL1) not locked. Lack of incoming sync, or wrong sync source selection, or the wrong horizontal frequency, will cause the Coincidence Detector to indicate a “not locked” condition.
13	Internally set to Logic 0.
14	Less than 576 horizontal lines counted per frame. This flag helps determine the applied video system. When high, a 525 line system (NTSC) is indicated. When low, a 625 line system (PAL) is indicated.
15	Vertical Countdown engaged. When high, this flag indicates the Vertical Countdown section has successfully maintained lock for 8 consecutive fields, indicating therefor a successful vertical lock–up. This flag is low in the Injection Lock mode.
16	Internally set to a Logic 1.
17	Internally set to a Logic 1.
18	(Acknowledge pulse).
19	Pixel clock VCO control voltage too low (< 1.7 V at Pin 16). This indicates the VCO may not function correctly as the control voltage is near one end of its range. The DAC setting at register $7F–5/0 must be increased, and/or the ÷ 2 block must be selected (set $85–7 = 1), to clear this flag.
20	Pixel clock VCO control voltage too high (> 3.3 V at Pin 16). This indicates the VCO may not function correctly as the control voltage is near one end of its range. The DAC setting at register $7F–5/0 must be reduced, and/or the ÷ 2 block must be deselected (set $85–7 = 0) to clear this flag. This flag will be high if the VCO is off (DAC $7F = 63).
21	Internally set to a Logic 1.
22	Internally set to a Logic 0.
23	ACC Loop is active, indicating it is locked up to the color burst signal. The Color Burst amplitude must exceed 30 mVpp, and the correct crystal selected, for lock–up to occur.
24	PAL system identified by the decoder, indicating the decoder recognizes the line–by–line change in the burst phase. When NTSC is applied, this flag is 0.
25	Not used.
26	Internally set to a Logic 0.
27	(Acknowledge pulse).

APPLICATIONS INFORMATION

Design Procedure and PC Board Layout

The external components required by the MC44011 are shown in Figure 42. Except for the crystals, all the components are standard value resistors and capacitors, and can be non–precision. Table 18 describes the external components for each pin.

Figure 42. Basic Functional Circuit



Crystal Specifications and Operation

The crystals used with the MC44011 should comply with Table 17 specifications.

Table 17. Crystal Specifications

Frequency: (4 x Subcarrier)	NTSC (14.31818 MHz) PAL (17.734472 MHz) PAL–M (14.30244 MHz)
Pull–in range:	±1600 Hz (with respect to crystal frequency)
Tolerance:	30 ppm (with fixed load capacitor)
Temperature Coefficient:	50 ppm (with fixed load capacitor)
Operating Mode:	Fundamental series resonance
Load Capacitance:	Nominally 20 pF
Motional Capacitance:	10 to 30 fF
Series Resistance:	< 30 Ω (nominally 10 Ω)

The oscillator output resistance at Pin 36 is nominally 300 Ω for NTSC mode, and 400 Ω at Pin 38 for PAL mode. It is recommended that a stray capacitance (PC board, package pins, etc.) of 4.0 to 5.0 pF be included when selecting a crystal.

The above values for tolerance and temperature coefficent can be increased if a trimmer capacitor is used for the load capacitor.

The crystal PLL filter (Pin 44) voltage is between 1.8 and 3.8 V in normal operation. If the color output of the MC44011 is incorrect, or non–existent (ACC flag off), this voltage should be checked. If it is beyond either of the above limits, the capacitor in series with the crystal should be changed so as to allow the PLL to pull–in the crystal. The capacitor is generally specified by the crystal manufacturer, but should also comply with Table 17 specifications. If no burst is present, Pin 44 voltage will be ≈ 1.3 V.

The selected crystal frequency can be checked by using a scope at the non–selected crystal pin. The signal amplitude is nominally 200 to 400 mVpp. In this way the selected crystal's frequency is not affected by the scope probe.

Table 18. External Components

Pin	Name	Function
1, 3	Video 1, Video 2	Input signals must be capacitor–coupled. The 470 Ω resistors protect the pins from ESD and RFI. The 75 Ω resistors are not required by the MC44011, but depend on the signal source. The 47 pF capacitors filter high frequency noise.
2	ACC Filter	The 0.1 µF ceramic capacitor filters the Automatic Gain circuit.
4	Vert Sync	The pull–up resistor is required for this open–collector output.
5, 6	SCL, SDL	Pull–up resistors are required on each I^2C line since outputs are open–collector. They are typically located at the master device.
7	Field ID	No external components required.
8	Burst Gate	No external components required.
9	I_{ref}	The 110 kΩ resistor provides ≈ 32 µA from the 5.0 V source. This pin must be well filtered to the Quiet Ground (Pin 10).
10	Quiet Gnd	This is the Reference Ground for Pin 9 and the PLL1 Filter.
11	PLL1 Filter	The 100 kΩ resistor, and the 0.1 µF and 68 pF capacitors are the filter network for this PLL. Connect to Pin 10 ground.
12	PLL1 Filt SW	The 12 kΩ resistor and 470 pF capacitor give the filter a longer time constant when Pin 12 is switched in.
13	$16Fh/C_{Sync}$	No external components required.
14	Fh Ref	No external components required.
15	15 k Return	TTL Return signal from external frequency divider.
16	PLL2 Filter	The 10 kΩ resistor and 47 nF and 4.7 nF capacitors are the filter network for this PLL. Connect to Pin 17 ground.
17	Ground	Ground for the Pixel Clock circuit.
18	Clk Out	Pixel Clock output to external frequency divider and triple A/D converter.
19	V_{CC3}	5.0 V supply for the Pixel Clock circuit.
20, 21, 22	R, G, B Out	The 390 Ω pull–up resistors are required for these open–collector outputs. The pull–ups should go to a clean, well filtered 5.0 V supply. These pins cannot drive 75 Ω directly. If required to do so, see text for suggested buffer.
23	V_{CC2}	5.0 V supply for the Color Difference section.
24	Ground	Ground for the Color Difference section.
25	Fast Comm	No external components required. This input *should not* be left open.
26, 27, 28	B, G, R In	Input signals must be capacitor–coupled. The 220 Ω resistors protect the pins from ESD and RFI.
29	Y2 Input	Input signals must be capacitor–coupled. The 220 Ω resistor protects the pin from ESD and RFI. The 75 Ω resistor is not required by the MC44011, but depends on the signal source.
30, 31	B–Y, R–Y In	Input signals must be capacitor–coupled. The MC44140 is required if PAL signals are processed (see text).
32	Y1 Clamp	The 0.1 µF ceramic capacitor provides clamping for the Y1 output.
33	Y1 Out	No external components required. This pin cannot drive 75 Ω directly. If required to do so, see text for suggested buffer.
34, 35	System Sel, Sandcastle	For use by the MC44140 delay line. No other external components required.
36, 38	Xtal 2, Xtal 1	A 17.7 MHz crystal is required (at Pin 38) for PAL signals, and a 14.3 MHz crystal is required (at Pin 36) for NTSC signals. If only one crystal is required, leave the other pin open. The series capacitor depends on the crystal manufacturer. (See Table 17 for crystal specs.)
37	N/C	No external components required.
39	Ground	Ground for Color Decoder section.
40	V_{CC1}	5.0 V supply for the Color Decoder section.
41, 42	B–Y, R–Y Out	The MC44140 is required if PAL signals are processed. Otherwise, capacitor–couple to Pins 30, 31 (see text).
43	Indent Filter	The 0.1 µF ceramic capacitor provides filtering for the Identification circuit.
44	4FSC PLL	The 47 kΩ resistor, and 0.1 µF and 2.2 nF capacitors are the filter network for the crystal PLL. Connect to Pin 39 ground.

Power Supplies and Ground

There are three V_{CC} pins (Pins 19, 23, and 40) which must be connected to a source of 5.0 V, ±5%. Since the three pins are internally connected by diodes, none can be left open, even if a particular section (such as the Pixel Clock Generator) is to be unused. Total current required is ≈ 135 mA (including the RGB output load current). There are four ground pins (Pins 10, 17, 24, and 39) which must be connected together, and preferably connected to a ground plane.

Pins 19 and 17 are the V_{CC} and ground for the Pixel Clock Generator, and the circuitry associated with the Pixel Clock should be referenced to those two pins.

Pins 23 and 24 are the V_{CC} and ground for the Color Difference section, which includes the RGB outputs. The output pull–up resistors should be connected to the V_{CC} at Pin 23.

Pins 40 and 39 are the V_{CC} and ground for the Color Decoder, Sync Separator, Horizontal PLL and the Vertical Decoder. Pin 10 is the Quiet Ground for the horizontal PLL's VCO and filter, and therefore, the components on Pins 9 and 11 should be connected as close as possible to Pin 10.

Bypassing of the power supplies must be done as close as possible to each V_{CC} pin, and at the output pull–up resistors. Recommended bypassing components are a 10 µF tantalum capacitor in parallel with a 0.01 µF ceramic.

Input Signals

The various video inputs, Video 1 and 2, Red In, Green In, Blue In, R–Y, B–Y, and Y2 inputs, are designed to accept standard level analog video waveforms. They are not designed for digital signals. The input impedance of the above pins is high. The need for 75 Ω terminations for those video signals depends on the video source itself. All of the above signals must be capacitor–coupled as clamping is provided internally.

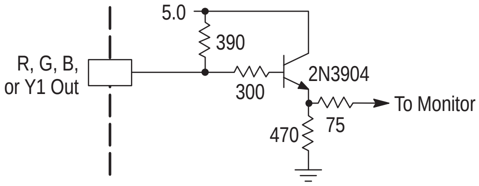
The I^{2}C inputs (SCL, SDL) are designed according to the I^{2}C specifications, which define V_{OL} as between 0 and 1.5 V, and V_{OH} as between 3.0 V to V_{CC}. See Appendix C.

The 15 k Return and Fast Commutate (Pins 15 and 25, respectively) are designed for TTL level signals. If unused, they should not be left open, but connected to 5.0 V, or ground, as appropriate.

Output Signals

The RGB/YUV outputs are open–collector, and require pull–up resistors (typically 390 Ω) to a clean 5.0 V (V_{CC2}). The output impedance is such that the load impedance (to ground) should be >1.5 kΩ. If it is desired to drive a 75 Ω load (e.g., a monitor) from these outputs, a simple buffer (see Figure 43) can be added.

Figure 43. Output Buffer



The Y1 output (Pin 33) has an output impedance of ≈ 300 Ω, and can be used as a monitoring point, or to drive the input of the MC44145 sync separator, or other high impedance loads (minimum load for Y1 is 1.0 kΩ). If it is to be used to drive a 75 Ω load, the buffer shown in Figure 43 can be used, *except the 390 Ω resistor must be deleted*.

The Vertical Sync output (Pin 4) is an open–collector logic level output, and requires a pull–up resistor to 5.0 V. 10 kΩ is recommended, but it can be as low as 1.0 kΩ. The I^{2}C data line (SDL, Pin 6) is also open–collector when it is an output, and can sink a maximum of 3.0 mA. Only one pull–up resistor is required on the SDL line (regardless of the number of devices on that line), and it is typically near the master device. The Field ID, Burst Gate, 16Fh/C_{Sync}, Fh Ref, and Pixel Clock outputs are logic level totem–pole outputs.

PC Board

The PC board layout should be neat and compact, and should preferably have a ground plane. If feasible, a second plane should be provided for the 5.0 V supply, but this is not mandatory. The components at Pins 9 and 11 should be connected to the same ground track which goes to Pin 10. The V_{CC} and ground should be connected as directly as possible to the power supply, and not routed through a maze of digital circuitry before arriving at the MC44011. Since the MC44011 is intended to be used with A/D converters and high speed digital signals, it is expected digital circuitry will be on the same board. Care should be taken in the layout to prevent digital noise from entering the analog portions of the MC44011. The most sensitive pins are Pins 1, 2, 3, 9, 10, 11, 12, 16, and 44, and should be protected from noise.

Initialization and Programming Information

Upon powering up the MC44011, initialization consists of first filling the registers with initial values to set a known condition. Table 19 provides recommended values for the initial settings, although these may be tailored for each application (with the exception of Bits $79–6,7, $7A–6, $86–6, and $87–6). Table 19 settings will set up the MC44011 to the following conditions:

- Composite video input at Video 1 (Pin 1), NTSC, using the crystal at Xtal 2 (Pin 36).
- Y1 enabled, RGB outputs enabled, and Composite Sync at Pin 13
- RGB inputs not enabled (R–Y, B–Y inputs are enabled)
- The Sound Trap at 4.5 MHz
- The Luma Peaking at 0 dB
- The Luma Delay at minimum
- High gain and high noise rejection for the horizontal PLL
- Vertical decoder set to Injection Lock mode
- The Pixel Clock VCO is off

After the registers are initialized, then set Bit $86–6 to 0, and load register $00 with $00. This will enable the horizontal PLL, permitting normal operation.

Table 19. Recommended Initial Settings

Sub–Address	7	6	5	4	3	2	1	0
$77	S–VHS Y = 0	S–VHS C = 0	FSI = 0	$\overline{\text{L2 Gain}}$ = 0	$\overline{\text{BLCP}}$ = 0	$\overline{\text{L1 Gain}}$ = 0	CBI = 0	CAI = 1
$78	36/68 µs = 0	Calkill = 0	(R–Y)/(B–Y) Adjust DAC = 32					
$79	HI = 1	VI = 1	Subcarrier Balance DAC = 32					
$7A	Xtal = 1	SSD = 0	–					
$7B	T1 = 1	T2 = 1	–					
$7C	SSC = 0	SSA = 1	–					
$7D	P1 = 1	SSB = 0	Blue Bias = 00					
$7E	P3 = 1	P2 = 1	Red Bias = 00					
$7F	D3 = 0	D1 = 0	Pixel Clock VCO Gain Adjust = 63					
$80	$\overline{\text{RGB EN}}$ = 1	D2 = 0	Blue Contrast Trim = 32					
$81	Y2 EN = 0	Y1 EN = 1	Main Contrast = 47					
$82	YUV EN = 0	YX EN = 0	Red Contrast Trim = 32					
$83	L2 Gain = 1	L1 Gain = 1	Blue Brightness Trim = 32					
$84	H Switch = 1	525/625 = 1	Main Brightness = 30					
$85	PClk/2 = 1	C_{Sync} = 1	Red Brightness Trim = 32					
$86	V_{in} Sync = 1	$\overline{\text{PLL1 EN}}$ = 1	Main Saturation (Color Difference section) = 32					
$87	Y2 Sync = 0	0	(R–Y)/(B–Y) Saturation Balance (Decoder section) = 15					
$88	V2/V1 = 1	RGB_{Sync} = 0	Hue = 32					

NOTE: These settings are for power–up initialization only. Refer to the text, and Appendix B, for subsequent modifications based on the application.

Then, after selecting the desired input(s) (from Pins 1, 3, or 26 to 31), and based on the applied signals at those inputs, and by reading the flags, the registers are adjusted for the desired and proper mode of operation. A suggested routine for setting modes is given in Appendix B. The “initial values” in the Control DACs table of Appendix B are those in Table 19. The remainder of the flow chart is a recommendation only, and should be tailored for each application.

The monitoring of flags should be done on a regular basis, and it is recommended it be done once per field. See Table 16 (in the Functional Description section) for a summary of the flags. Should any flags change, the following procedures are recommended:

Flag 11 (Horizontal Enabled) – Once enabled by setting Bit $86–6 = 0, this flag should always remain a 1. Should it change to 0, reset $86–6 to 0, and write $00 to register $00 again. If the flag does not return to a 1, this indicates a possible device malfunction.

Flag 12 (Horizontal Out–of–Lock) – When 1, this indicates:

a. the wrong input is selected (Bits $88–7, $81–7, $80–7, and $77–7,6), or;
b. the wrong sync source is selected (Bits $86–7, $87–7, and $88–6), or;
c. the incoming signal is somewhat unstable, as from a VCR tape (change Bit $83–6), and/or;
d. the incoming signal is noisy (change Bit $84–7), or;
e. a loss of the incoming signal with sync.

(It is possible for this flag to flicker when the video signal is from a poor quality tape, or other poor quality source.)

Flag 14 (Less than 576 lines) – This flag, from the vertical decoder, is used to help determine if the signal is PAL or NTSC. Should it change, this indicates the incoming signal has changed format, or possibly one of the items listed under Flag 12 above.

Flag 15 (Vertical Countdown Engaged) – Bits 77–0 and 1 must be set to 1 (after Flag 12 reads 0) for this flag to indicate correctly. Then this flag will change to a 1 after 8 fields of successful synchronization of the internal counters with the incoming signal. To change to a 0 requires 8 consecutive fields of non–synchronization. If this flag changes to 0, this indicates a loss of signal, a change of signal format, or instability in the horizontal PLL.

Flags 19, 20 (VCO Control Voltage Low/High) – These flags are meaningful only if the Pixel Clock Generator is used. If Flag 19 is a 1, the gain of the pixel clock VCO needs to be increased by increasing the value of register $7F, and/or set Bit $85–7 = 1. If Flag 20 is a 1, the value of the register must be decreased, and/or set Bit $85–7 = 0. If the VCO is turned off ($7F = 63), Flag 19 will be 0, and Flag 20 will be 1.

Flag 23 (ACC Active) – If this flag is a 0, it indicates the ACC loop is not active. This will happen if the burst signal is less than 30 mVpp, if the incorrect crystal is selected ($7A–7), if the crystal PLL is not locked, or if the horizontal PLL is not locked.

Flag 24 (PAL Identified) – This flag is a 1 when PAL signals are applied, and a 0 when NTSC signals are applied, or when no burst is present.

It is recommended that the Color Decoder section, and crystal, should be set according to the state of Flags 14, 23, and 24 according to Table 20.

Table 20. Color Standard Selection Table

Flags			Bit Settings				
#14 <576 Lines	#23 ACC Active	#24 PAL Signal	Crystal	SSA ($7C–6)	SSB ($7D–6)	SSC ($7C–7)	System
X	0	X	Either	1	1	0	Color Kill
0	1	0	Either	1	1	0	Color Kill
0	1	1	17.7 MHz	0	1	0	PAL
1	1	0	14.3 MHz	1	0	0	NTSC
1	1	1	(Note 1)	0	1	0	PAL–M

NOTES: 1. PAL–M, used in Brazil and other South American countries, can be decoded by the MC44011, but requires a 14.3024 MHz crystal.
2. SSD ($7A–6) is always set to 0.

MISCELLANEOUS APPLICATIONS INFORMATION

Use of the MC44140 Delay Line

The MC44140 delay line is generally required if PAL signals are to be decoded, so as to average out the line–by–line color information associated with PAL color decoding. If the same single PAL video source is always used in a particular application, the delay line can be eliminated, and any slight phase errors can be corrected with the DAC of register $79–5/0. If, however, various video sources can be used, and/or if the video signal is less than broadcast quality, it is recommended the MC44140 delay line be included.

The MC44140 acts on the color difference signals before they enter the color difference stage of the MC44011. It will, however, pass NTSC signals through without modifications. The MC44011 uses the System Select output (Pin 34) to indicate to the delay line which signals are being processed. The System Select voltage is set when the color decoder is set with Bits SSA, SSB, SSC, SSD. The Sandcastle output (Pin 35) provides the horizontal timing signals to the delay line. In addition, the MC44140 uses the crystal frequency for the internal counters.

The MC44140 is inserted into the circuit between the Color Difference outputs and inputs of the MC44011. In addition, the MC44140 provides pins (Pins 8,9) for inserting an alternate source of color difference signals to the MC44011 by setting the System Select to external (Bit $7C–7 = 1). See Figure 44 for a suggested circuit.

If only NTSC signals are to be processed by the MC44011, the MC44140 is not needed. In this case, connect Pin 42 to Pin 31 with a 0.1 μF capacitor, and similarly connect Pin 41 to Pin 30.

Figure 44. Incorporating the MC44140 Delay Line

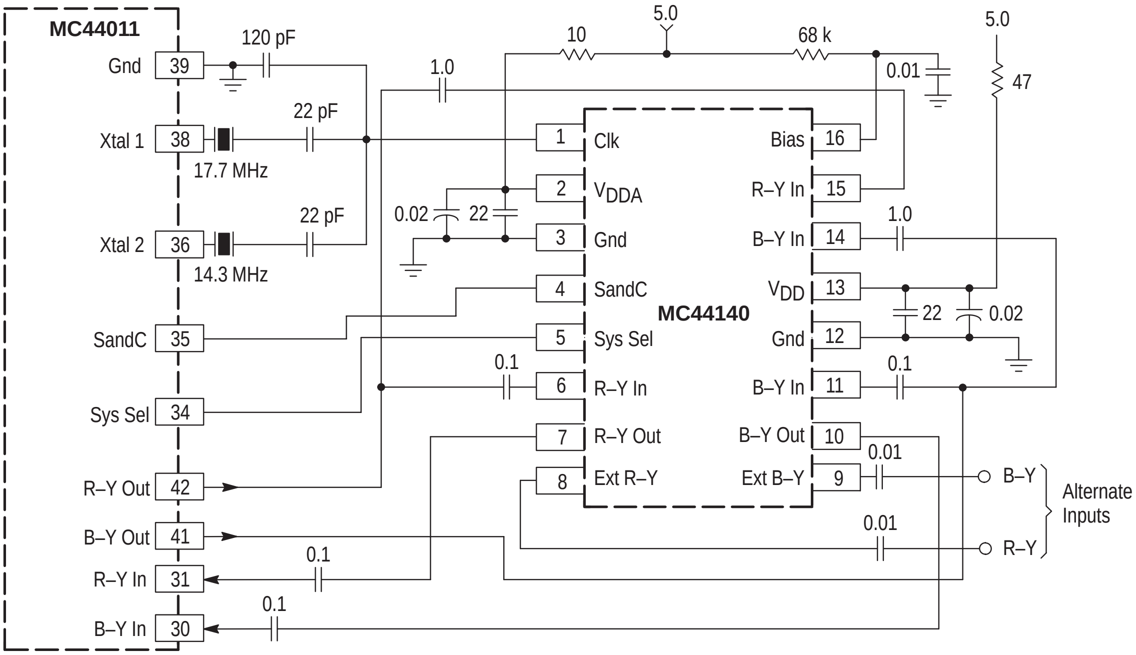
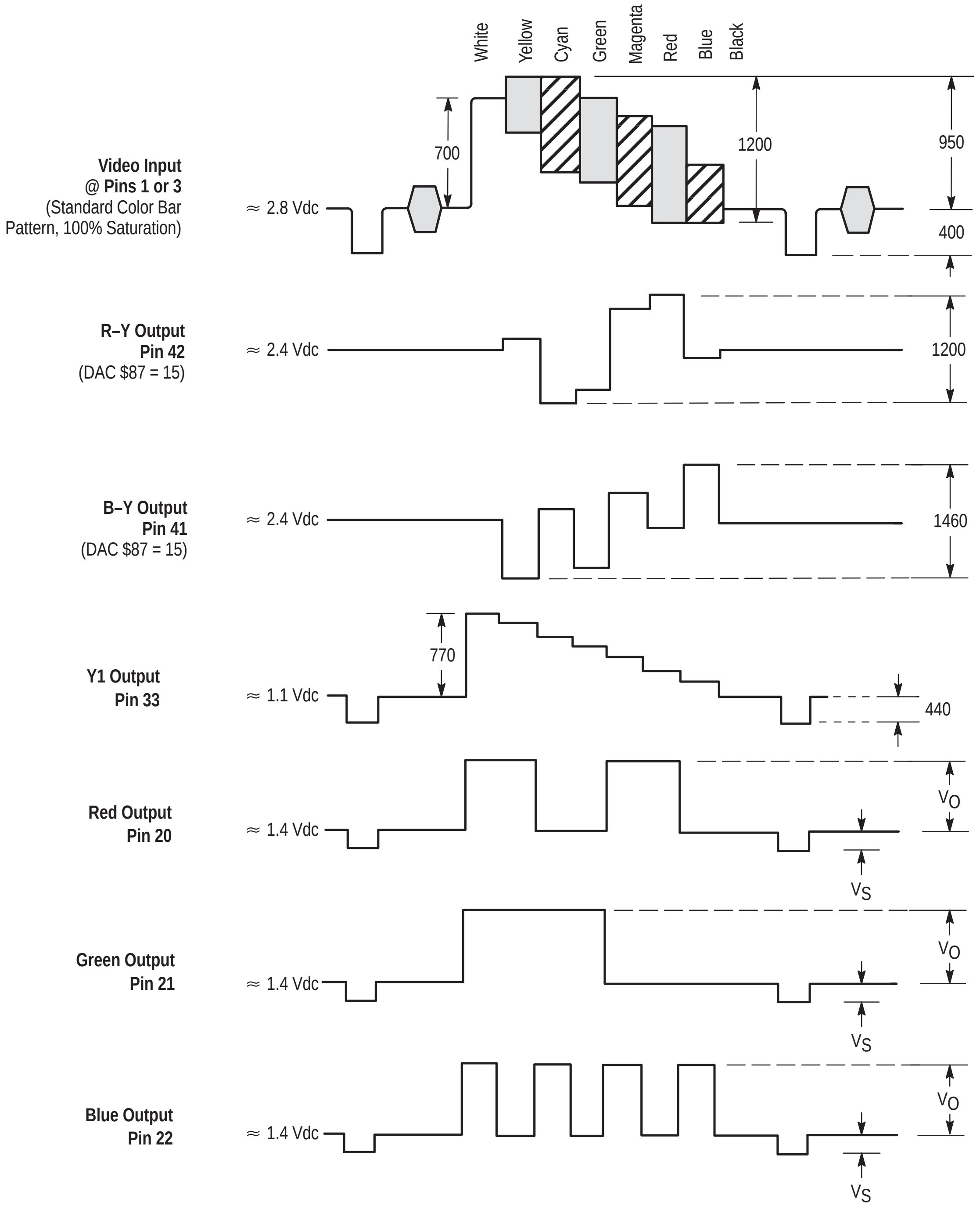


Figure 45. Typical Waveforms



DACs set per Table 19. All amplitudes in milliVolts.
Voltages are nominal, and do not represent guaranteed limits.

DAC 81	V_O	V_S
32	1725	220
47	2360	340
63	3160	440

Use of the MC44145 Pixel Clock Generator

For most applications the Pixel Clock Generator (PLL2) within the MC44011 will be suitable. In those cases, however, where the pixel clock frequency is set to within ±1.0 MHz of the selected crystal frequency (14.3 MHz or 17.7 MHz), or to within ±1.0 MHz of double the selected crystal frequencies, undesirable noise artifacts may be present on the RGB outputs. In these cases the MC44145 should be used to generate the Pixel Clock. The circuitry within the MC44145 duplicates that of the MC44011, but since it is physically removed from the circuitry within the MC44011, the interfering noise is not generated. If the MC44145 is used, the Pixel Clock Generator within the MC44011 should be shut off by setting the DAC of register $7F to 63, eliminating the components at Pin 16, and grounding Pin 16.

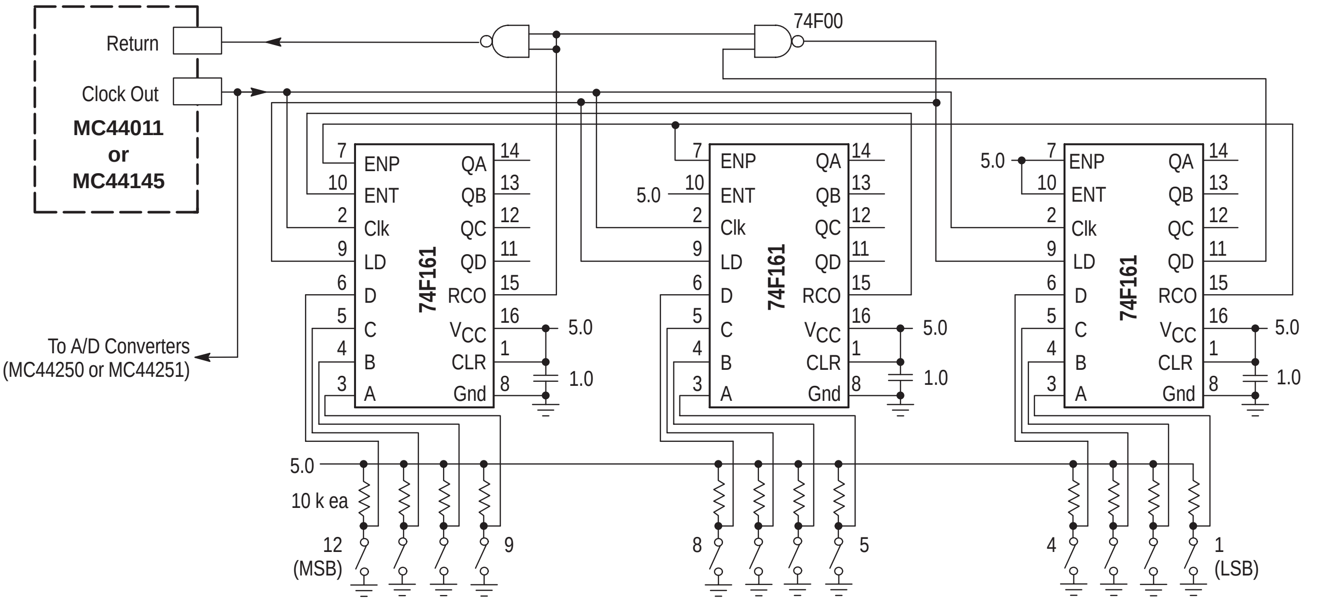
If the desired pixel clock frequency is close to the limits mentioned above, then experimentation may be used to determine the need for the MC44145.

Frequency Divider

The frequency of the Pixel Clock is determined by the horizontal frequency and an external frequency divider. The divider simply divides down the Pixel Clock Frequency so that it equals the horizontal frequency. The PLL within the MC44011 (or the MC44145) compares the horizontal frequency with the returned frequency, and adjusts the internal VCO accordingly, to achieve the proper relationship between the two. The PLL will phase–lock the negative–going edge of the returned signal with the positive–going edge of the Fh signal (Pin 14 of the MC44011). The returned signal must be TTL logic level amplitudes, and have a minimum low time of 200 ns. A suggested circuit for the divider, shown in Figure 46, uses 74F161 programmable binary counters. The 12 switches at the bottom are used to set the division ratio, and hence the Pixel Clock frequency.

The division ratio is determined by dividing the desired clock frequency by the horizontal frequency, and then using the closest whole number. After determining the binary equivalent of that number, close each switch corresponding to a 1, and leave open each switch corresponding to a 0. Alternately, the switches could be deleted, and Pins 3, 4, 5 and 6 of each 74F161 hard–wired to 5.0 V or ground, or controlled by a microprocessor where different pixel clock frequencies are required.

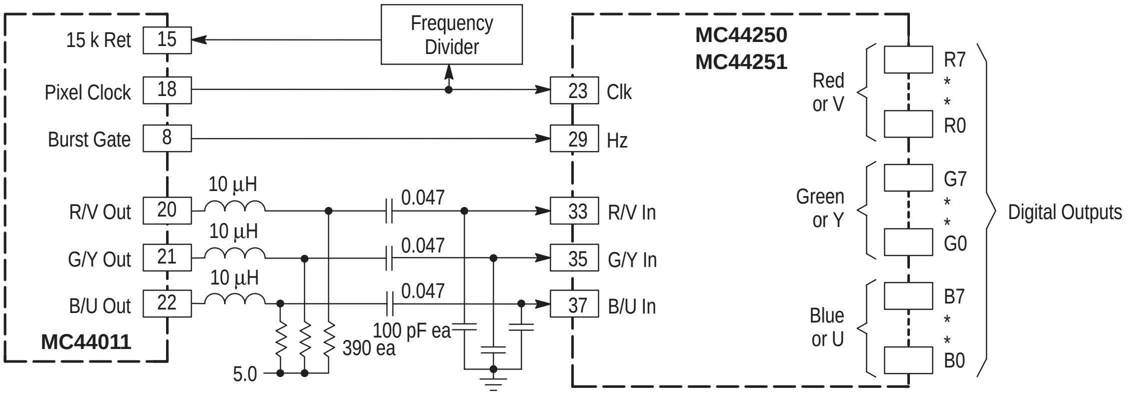
Figure 46. Suggested Frequency Divider



Connecting the MC44011 to the MC44250 or MC44251 A/D Converter

The MC44250 and MC44251 triple A/D converters are designed to accept RGB or YUV inputs, and provide 8–bit equivalents of each. Additionally, the inputs have black level clamps, allowing the input signals to be capacitor–coupled. The simplified schematic of Figure 47 shows the connections between the MC44011 and the MC44250/1, including anti–aliasing filters between the devices. Connection to other A/D converters would be done in a similar manner. Refer to the appropriate data sheet for details.

Figure 47. Connecting to a Triple A/D Converter

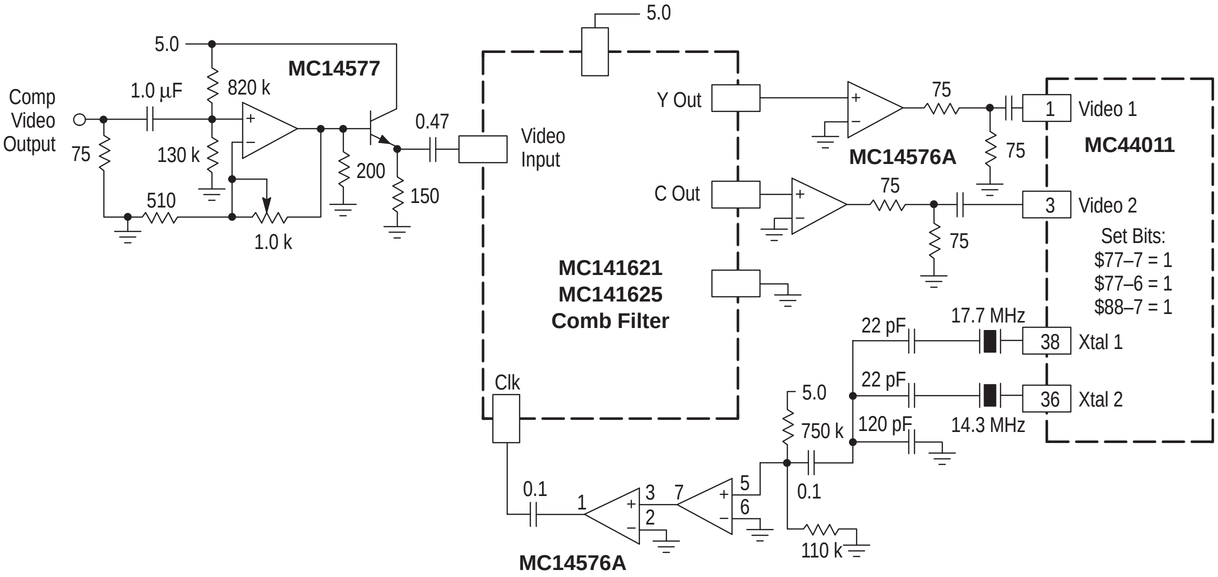


Connecting the MC44011 to the MC141621 or MC141625 NTSC Comb Filter

A comb filter can be used ahead of the MC44011 to enhance picture quality by providing a more accurate separation of the luma and chroma components from the composite video, without sacrificing bandwidth. The usual benefits are reduced dot crawl, and increased color purity.

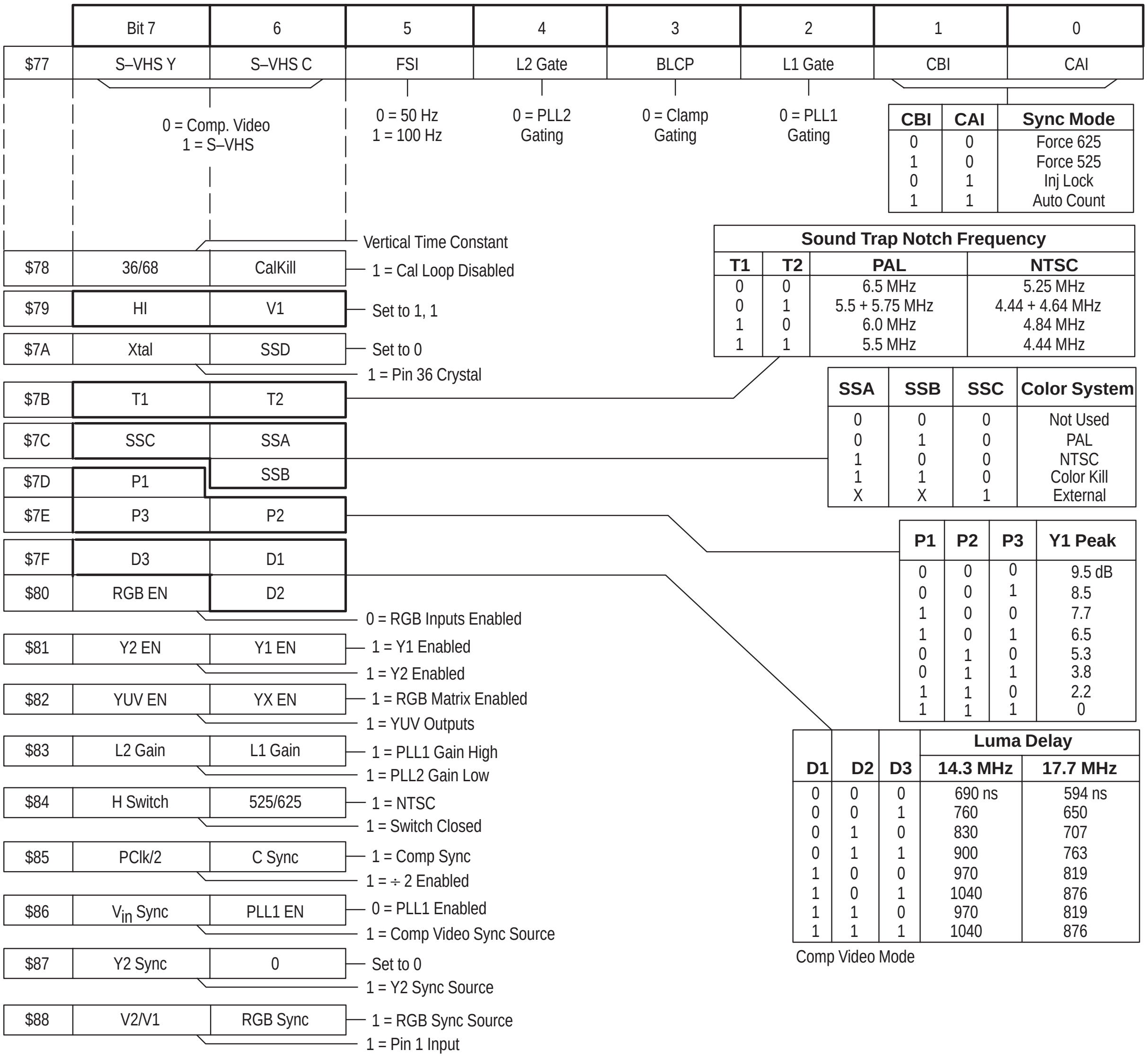
Figure 48 (a simplified schematic) shows the normal mode of implementing the MC141621 (NTSC) or MC141625 (PAL/NTSC) comb filter with the MC44011. The two comb filters can also provide the Y and C signals in digital format. Refer to their data sheets for details. The MC14576A operational amplifiers have an internally set gain of 2.

Figure 48. Implementing the Comb Filter



APPENDIX A

Control Bit Summary



	Bit 7	6	5	4	3	2	1	0
$77	S–VHS Y	S–VHS C	FSI	L2 Gate	BLCP	L1 Gate	CBI	CAI
$78	36/68	CalKill						
$79	HI	V1						
$7A	Xtal	SSD						
$7B	T1	T2						
$7C	SSC	SSA						
$7D	P1	SSB						
$7E	P3	P2						
$7F	D3	D1						
$80	RGB EN	D2						
$81	Y2 EN	Y1 EN						
$82	YUV EN	YX EN						
$83	L2 Gain	L1 Gain						
$84	H Switch	525/625						
$85	PClk/2	C Sync						
$86	V_{in} Sync	PLL1 EN						
$87	Y2 Sync	0						
$88	V2/V1	RGB Sync						

CBI	CAI	Sync Mode
0	0	Force 625
1	0	Force 525
0	1	Inj Lock
1	1	Auto Count

Sound Trap Notch Frequency			
T1	T2	PAL	NTSC
0	0	6.5 MHz	5.25 MHz
0	1	5.5 + 5.75 MHz	4.44 + 4.64 MHz
1	0	6.0 MHz	4.84 MHz
1	1	5.5 MHz	4.44 MHz

SSA	SSB	SSC	Color System
0	0	0	Not Used
0	1	0	PAL
1	0	0	NTSC
1	1	0	Color Kill
X	X	1	External

P1	P2	P3	Y1 Peak
0	0	0	9.5 dB
0	0	1	8.5
1	0	0	7.7
1	0	1	6.5
0	1	0	5.3
0	1	1	3.8
1	1	0	2.2
1	1	1	0

			Luma Delay	
D1	D2	D3	14.3 MHz	17.7 MHz
0	0	0	690 ns	594 ns
0	0	1	760	650
0	1	0	830	707
0	1	1	900	763
1	0	0	970	819
1	0	1	1040	876
1	1	0	970	819
1	1	1	1040	876

Control DACs

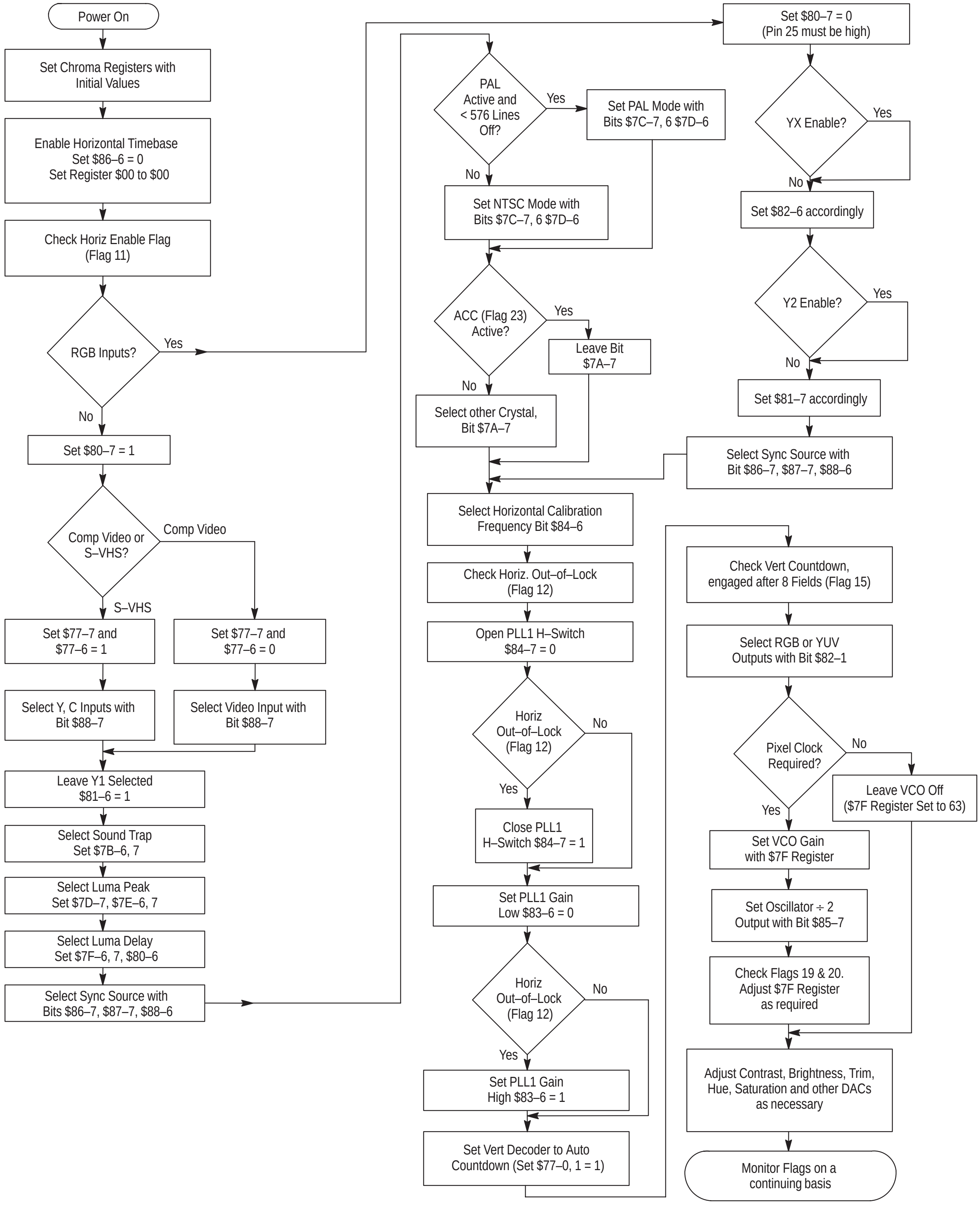
$78	R–Y/B–Y Gain Adjustment	$82	Red Contrast Trim
$79	Subcarrier Phase	$83	Blue Brightness Trim
$7D	Blue DC Bias	$84	Main Brightness
$7E	Red DC Bias	$85	Red Brightness Trim
$7F	Pixel Clock VCO Gain	$86	Saturation (Color Diff Section)
$80	Blue Contrast Trim	$87	Saturation (Decoder)
$81	Main Contrast	$88	Hue

Flags

10	Internally Set to 1	19	Pixel Clock VCO Gain too low
11	Horizontal Loop (PLL1) Enabled	20	Pixel Clock VCO Gain too high
12	Horizontal Loop not Locked	21	Internally Set to 1
13	Internally Set to 0	22	Internally Set to 0
14	Less than 576 Lines	23	ACC Loop Active
15	Vertical Decoder Engaged	24	PAL Signals Detected
16	Internally Set to 1	25	Not Used
17	Internally Set to 1	26	Internally Set to 0

APPENDIX B

Suggested Mode Setting Routine (Simplified)



APPENDIX C

I^{2}C Description

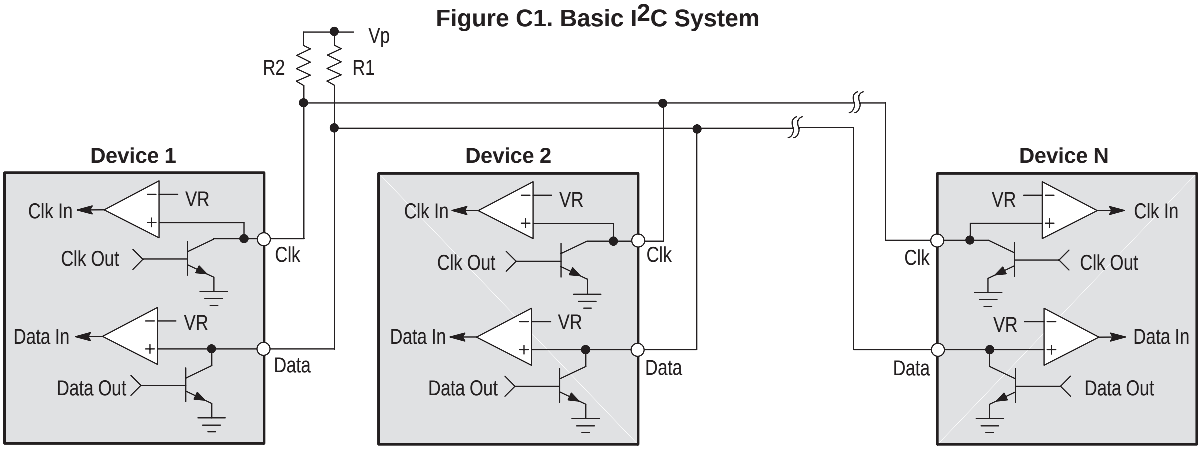
Introduction

The I^{2}C system, a patented and proprietary system developed by Philips Corporation, defines a two–wire communication system. The number of devices in a system is limited only by the system capacitance and data rate. Each device is assigned two unique addresses – one for writing to it, and one for reading from it. Any device may act as a master by initiating a data transfer with any other device (the slave). Data transfer is in 8–bit bytes, and can be in either direction, but not in both directions in one data transfer operation.

Hardware Aspects

The system bus consists of two wires, Clock and Data. All devices must have open–collector (or open–drain) outputs. A single pull–up resistor is required on each line, as shown in Figure C1.

Figure C1. Basic I^{2}C System



Devices such as the MC44011, which never act as a master, need not have the output drive transistor at the Clock pin. Nominal value for R1 and R2 is 10 kΩ, but can be different to account for system capacitance at high data rates. VR is a switching threshold for input signals.

The significant electrical characteristics are as follows:

– Maximum data rate (Clock frequency) is 100 kHz;
– V_{OL} max is 0.4 V when sinking 3.0 mA;
– V_{IL} max is 0.3 x Vp, but at least 1.5 V;
– V_{IH} min is 3.0 V for a 5.0 V system, or 0.7 x Vp for other supply voltages.
– The maximum input current at Clock and Data at V_{OL} max (when they are inputs) is –10 µA;
– The maximum input current at Clock and Data at 0.9 x Vp (when they are inputs) is 10 µA;
– The maximum pin capacitance is 10 pF;
– Maximum bus capacitance is 400 pF.

Data Transfer

Prior to initiating a data transfer, both lines must be high (all drive transistors off). A device which initiates a data transfer assumes the role of the master, and generates a START condition by taking the Data line low while Clock is still high. At this time, all other devices become listeners. The master will supply the clock for the entire sequence.

The master then sends the 8–bit address by operating both the clock and data lines. Data must be stable during the clock's high time, and can change during the clock's low time. The MSB is sent first. The address must end in a 0 if it is a Write operation (data transfer from master–to–slave), and it must end in a 1 if it is a Read operation.

At the 9th Clock Pulse, the master must release the Data line high, and the slave must provide an acknowledge bit by pulling Data low during this clock time. If the master does not receive a proper acknowledge, it can terminate the operation.

After the first acknowledge, the role of the two devices depends on whether it is a Write or a Read operation, but the master always supplies the clock.

– In a Write operation the master is the transmitter, and the slave is the receiver.
– In a Read operation the slave is the transmitter, and the master is the receiver.

The transmitter then sends the next 8–bit byte. At the 18th Clock Pulse (and every 9th clock pulse thereafter), the transmitter releases the Data line, and the receiver acknowledges by pulling Data low. There is no limit to how many bytes may be sent after the address.

When all data is transferred, the Data line must be released by the transmitter so that the master can set the STOP condition. This is done by first pulling Data low (during clock low), then releasing Data high while clock is high. After this, the bus is free for any other device to initiate a new data transfer.

Definitions

Master – The device which initiates a data transfer (regardless of the data direction), generates the clock, and terminates the transfer.

Slave – The device addressed by the master.

Transmitter – The device which supplies data to the bus.

Receiver – The device which receives data from the bus.

Notice that the master is not necessarily the transmitter, and the slave is not necessarily the receiver.

Other

For additional information on the I^{2}C bus specifications; modes of operation; arbitration; and synchronization, contact Philips Corporation.

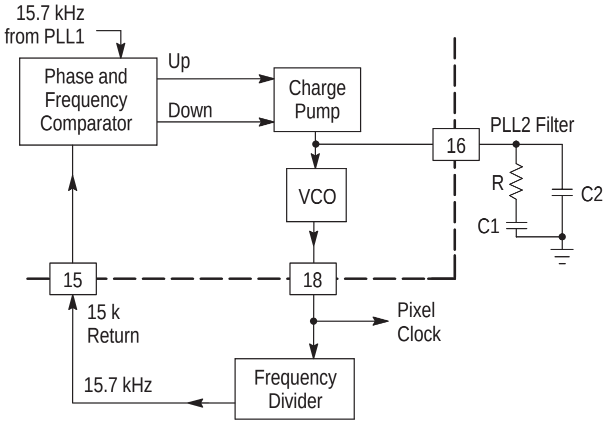
APPENDIX D

PLL Loop Theory

High Frequency Line–Locked Clock Generator

This section is not intended as a complete loop theory, its aim is merely to point out the idiosyncrasies of the loop, and provide the user with enough information for the selection of filter components. For a more in depth explanation, the references at the end of this section may be consulted.

Figure D1. PLL2 Basic Configuration



The following general remarks apply to the loop (PLL2):

- The loop frequency is ≈ 15.7 kHz.
- In spite of the samples nature of the loop, a continuous time approximation is possible if the loop bandwidth is sufficiently small.
- Ripple on V_C (filter pin) is a function of loop bandwidth.
- The loop is a type II, 3rd order. However, since C2 is small, the pole it creates is far removed from the low frequency dominant poles, and the loop can be analyzed as a 2nd order loop.

The following remarks apply to the Phase and Frequency Comparator:

- Phase and frequency sensitive.
- Independent of duty cycle.
- It has 3 allowed states: up, down, and off (high impedance).
- The VCO is always pulled in the right direction during acquisition.
- The Comparator’s gain is higher at or near lock.

The last two remarks imply that only the higher value need be taken into account, as acquisition will be slower but always in the correct direction, whereas the higher gain will come into action as soon as the error reaches 2π.

The following values are selected and defined:
C2 = C1/10 or less, to satisfy the requirement that the effect of C2 on the low frequency response of the loop be minimal, and similar to a 2nd order loop.

ξ = 0.707 (damping factor).
ωi = 15750 x 2p = 98960 rad/sec (input frequency).
τ = RC as the loop filter
K = Ko x Ip x R/(2πN) – the loop gain
K′ = K x τ = $4\xi^2$ (the normalized loop gain)
Ko = 70×10^6 rad/V

Stability analysis with C2 = C1/10 and K′ = 2 (ξ = 0.707) gives a minimum value of 7.5 for the ratio ωi/K. To have some margin, a reasonable value can be 15 to 20 or higher.

Selecting ωi/K = 20 yields,
K = ωi/20 ≈ 5000.

Using the following items:
K′ = 2,
τ = 2/K = 400 µs,
K = Ko x Ip x R/(2πN)
Ip = 20 µA
N = 2000 (average value)

yields a value of 22 kΩ for R. Using a value of 400 µs for τ, C1 calculates to 18 nF, and C2 calculates to 1.8 nF.

With the above values, the loop’s natural frequency (ωn), and loop bandwidth (ω3dB) can be calculated:
$\omega n = \{(Ko/N) \times Ip/(2\pi C)\}^{0.5}$ = 3520 rad/sec.
fn = 3520/2π = 560 Hz.
ω3dB ≈ 2 x ωn = 1120 Hz (valid if ξ = 0.707).

The circuit designer should be cautioned at this point that the above calculated values are not necessarily optimum for every application. Besides the fact that several assumptions were made in the discussion, the equations cannot account for items such as the PC board layout, characteristics of the external divider, and noise from various sources. The above calculated values provide for a functional circuit, which should then be tweaked to obtain minimum jitter at the pixel clock output.

When initially adjusting the filter component values, it is advisable to maintain the same general time constant (400 µs in this example), and the same x10 relationship between C1 and C2.

References:
(1) *Charge–Pump Phase–Lock–Loops* by Floyd M. Gardner, IEEE Transactions on Communications, Vol. com–28, no. 11, Nov. 1980.
(2) *Phaselock Techniques* by Floyd M. Gardner, J. Wiley & Sons, 1979.
(3) *Phase–Locked–Loops* by Roland E. Best, McGraw Hill, 1984.
(4) AN–535, *Phase–Locked–Loop Design Fundamentals*, Motorola.

GLOSSARY

Aspect Ratio – The ratio of the width of a TV screen to the height. In standard TVs, it is 4:3. In HDVT it will likely be 16:9.

Back Porch – The blanking time after the sync signal during which the color burst is inserted.

Blank, Pedestal – The signal level which is either at black, or slightly more negative than black (“blacker–than–black”), and is used to turn off the screen dot during retrace. Also referred to as the *pedestal*.

Brightness – A measure of the dc levels of the luma component. Changing brightness will change the minimum and maximum luma levels together.

Burst – The 8 to 10 cycle sine wave which is inserted in the back porch. It’s frequency is the color subcarrier (3.58 MHz or 4.43 MHz), and is used as a phase reference for the color decoder.

Burst Gate – A signal identifying the time during which the burst signal occurs.

C, Chrominance – The color component of the video signal. The color is determined by the phase of the chrominance component relative to the burst signal.

Clamping – A process which establishes a fixed dc voltage level, usually during the back porch time.

Color Difference Signals – B–Y, R–Y, also designated as U and V.

Color Decoder – A circuit which separates composite video into Red, Blue, and Green, luminance, and sync signals.

Color Encoder – A circuit which combines Red, Blue, and Green, luminance, and sync signals into composite video.

Comb Filter – A multi–bandpass filter which separates the luma and chrominance components from the video signal, without sacrificing bandwidth.

Component Video, YUV – A format whereby the video information is kept as separate luma, R–Y, and B–Y signals *(YUV)*. U is the same as B–Y, and V is the same as R–Y.

Composite Sync – A sync signal which combines horizontal and vertical sync information. The waveform is made up of regularly spaced negative going pulses for the horizontal sync, and then half–line pulses and polarity reversal to indicate the vertical sync and retrace time.

Composite Video – The video signal which consists of sync, back porch, color burst, video information (luma and chroma), and front porch. This is the signal normally broadcast by TV stations.

Contrast – A measure of the difference between minimum and maximum luma amplitudes. Increasing contrast produces a “blacker” black and a “whiter” white.

dB – A power or voltage measurement unit, referred to another power or voltage. It is generally computed as:

10 x log (P1/P2) for power measurements, and
20 x log (V1/V2) for voltage measurements.

Field – One of the two or more equal parts into which a frame is divided in an interlaced system.

Frame – The information which makes up one complete picture. It consists of 525 lines in NTSC systems, and 625 lines in PAL systems. An interlaced system is typically composed of two fields.

Front Porch – The blanking time immediately before the sync signal.

Horizontal Sync – The negative going sync pulses at the beginning of each line. The pulses indicate to the circuit to begin sweeping the dot across the screen.

Hue – A measure of the correctness of the colors on a screen.

Interlaced System – A method of generating a picture on the screen whereby the even number lines are processed, and then the odd number lines are processed, thereby completing a full picture.

IRE – Abbreviation for *International Radio Engineers*, it is the amplitude unit used to define video levels. In standard NTSC signals, blank–to–white is 100 IRE units, and blank–to–sync tip is 40 IRE units. In a 1.0 Vpp signal, one IRE unit is 7.14 mV.

Luma, Y – The brightness component of the video signal. Usually abbreviated “Y”, it defines the shade of gray in a black–and–white TV set. In color systems, it is composed of 0.30 red, 0.59 green and 0.11 blue.

NTSC – *National Television System Committee*. This committee set the color encoding standards and format for television broadcast in the United States.

PAL – *Phase Alternating Line*. A color encoding system in which the burst is alternated 90° each line to help compensate for color errors which may occur during transmission. This system is popular mainly in Europe.

Pixel – The smallest picture element, or dot, on a screen. It is determined by the design of the CRT, as well as the system bandwidth.

R–Y, B–Y – Referred to as *color difference signals*. These are two of the three signals of component video. When combined with Y, the full color and luminance information is available.

Retrace – The rapid movement of the blanked dot from the screen’s right edge to the left edge so it can start scanning a new line. It is also the rapid movement from the lower right corner to the upper left corner during vertical blanking.

RGB – The three main colors *(red, blue, green)* used in the acquiring, and subsequent display of a video signal.

S–VHS – A format whereby the video information is kept as separate luma and chroma signals (Y and C).

Sandcastle – A signal which indicates the horizontal blanking time. It encompasses the front porch, sync, and back porch. Two amplitudes distinguish the front porch + sync time from the back porch.

Saturation – A measure of the intensity of the color on a screen. Also related to its purity.

Sync Separator – A circuit which will detect, and output, the sync signal from a composite video waveform.

Vertical Sync – The synchronizing signal which indicates to the circuitry to drive the dot to the upper left corner of the screen, thereby starting a new field. This signal is derived from the composite sync.

MOTOROLA

MC44030
MC44035

Product Preview

Multistandard Video Signal Processor with Integrated Chroma Delay Line

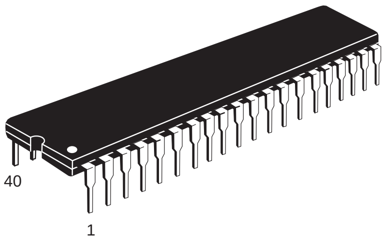
**MULTISTANDARD
VIDEO SIGNAL PROCESSOR
WITH INTEGRATED
CHROMA DELAY LINE**

**SEMICONDUCTOR
TECHNICAL DATA**

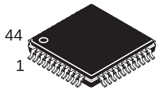
The MC44030/35 is a highly advanced circuit which performs most of the basic functions required for a color TV. All its advanced features are under processor control via I^{2}C bus, enabling potentiometer controls to be removed completely and allowing significant cost savings together with the possibility of implementing sophisticated automatic test routines.

A summary of the features available on the device is given below:

- Operation from a Single 5.0 V Supply; Low Current Consumption (Typically 150 mA)
- PAL/SECAM/NTSC Decoding Capability (4 Matrix Modes Available)
- Integrated Chroma Delay Line
- Dual Composite Video or S–VHS Inputs
- Integrated Luma and Chroma Filters (Including SECAM Cloche Filter)
- Programmable Luma Delay and Peaking
- RGB Drives Including CONTRAST/BRIGHTNESS Controls and Auto Grey–Scale
- External RGB and Fast Commutate Inputs with SATURATION Control Possibility
- Auxiliary Y, R–Y, B–Y Inputs
- Line Timebase Featuring H–PHASE Control and Switchable Phase Detector Gain
- Countdown Type Vertical Timebase Including the Vertical Geometry Corrections
- 16:9 Display Mode Capability
- E–W Parabola Drive Including the Horizontal Geometry Corrections
- Anode Current Monitor with Vertical Breathing Compensation
- Analog Contrast Control, Allowing Fast Beam Current Limitation
- Pin to Pin Compatible with MC44002/7
- MC44035 is the PAL/NTSC Only Version of the MC44030
- Available in DIP and TQFP Packages



P SUFFIX
PLASTIC PACKAGE
CASE 711

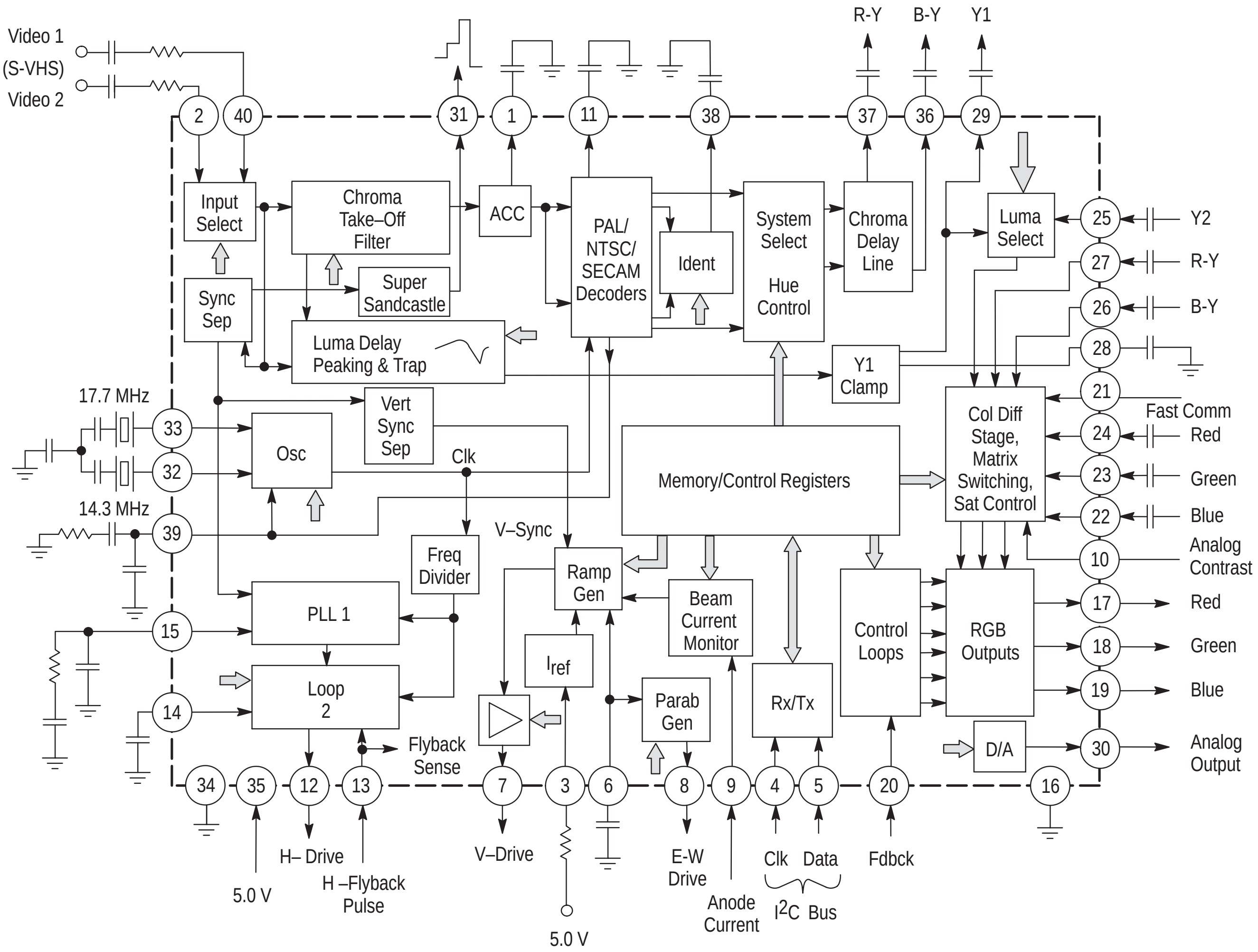


FTB SUFFIX
PLASTIC PACKAGE
CASE 824D
(TQFP–44)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC44030P	T_A = 0° to +70°C	Plastic DIP
MC44030FTB		TQFP–44
MC44035P		Plastic DIP
MC44035FTB		TQFP–44

Simplified Block Diagram



NOTE: Pin numbers shown are for the DIP package.

This device contains 6360 active transistors.

MOTOROLA

MC44144

Subcarrier Phase-Locked Loop

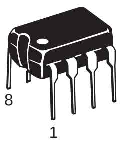
SUBCARRIER PHASE–LOCKED LOOP

SEMICONDUCTOR TECHNICAL DATA

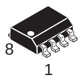
The MC44144 is a gated phase–locked loop intended for, but not restricted to, video applications. The integrated circuit contains a gated phase detector, voltage controlled crystal oscillator, divide–by–4 circuitry, and a video clamp. This device provides a 4X reference frequency output, and a 1X reference frequency output.

The MC44144 is manufactured using Motorola's high density, bipolar MOSAIC™ process.

- 8–Pin DIP or Surface Mount Package
- Gated–Phase Detector
- Single Pin Voltage Controlled Crystal Oscillator
- 1X and 4X Subcarrier Output
- Operates Off of a Standard 5.0 V Supply

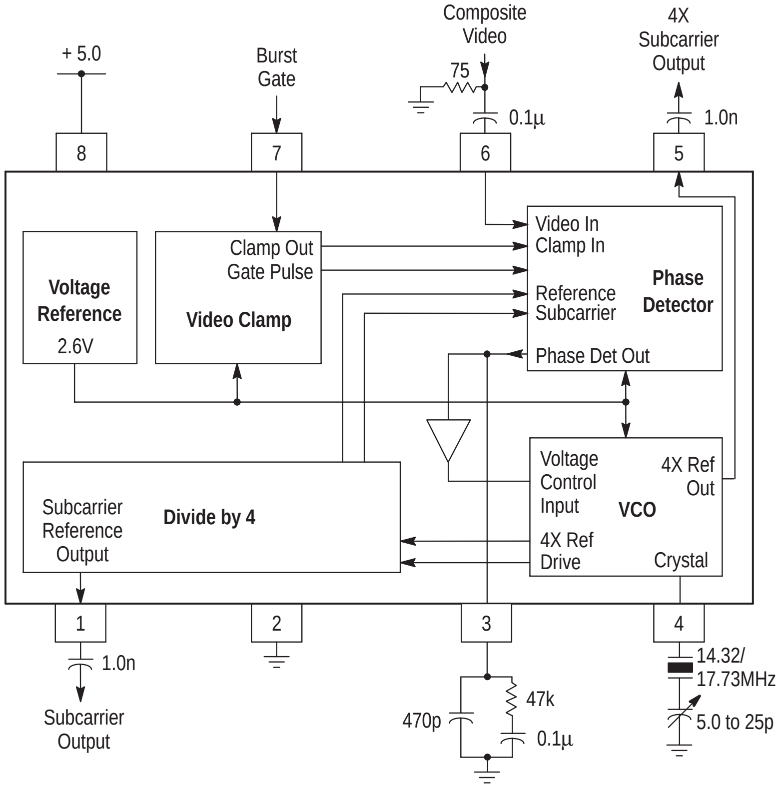


P SUFFIX
PLASTIC PACKAGE
CASE 626

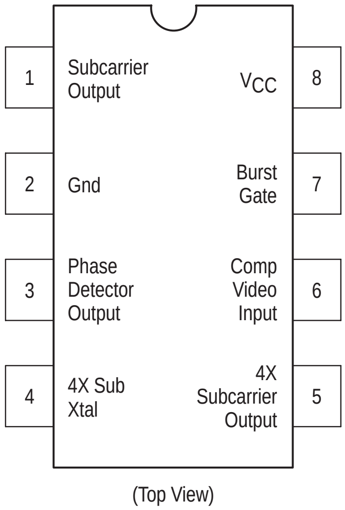


D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

Representative Block Diagram



PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC44144D	T_A = 0° to +70°C	SO–8
MC44144P		Plastic

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	6.0	Vdc
Operating Ambient Temperature	T_A	0° to +70	°C
Storage Temperature Range	T_{stg}	– 65 to +150	°C
Operating Junction Temperature	T_J	+150	°C

RECOMMENDED OPERATING CONDITIONS

Characteristic	Pin	Symbol	Min	Typ	Max	Unit
Supply Voltage	8	V_{CC}	4.5	5.0	5.5	Vdc
Composite Video Input (Note 1) Burst Amplitude to Acquire Lock	6	– 	50	300	1000	mVpp

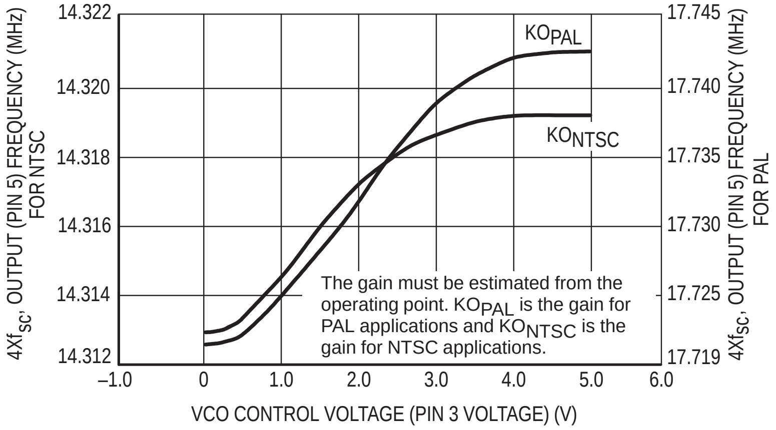
NOTE: 1. Total peak–to–peak voltage of video should not exceed ground or V_{CC}.

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 Vdc, T_A = 25°C)

Characteristic		Pin	Min	Typ	Max	Unit
Operating Current		8	8.0	10	12	mA
Burst Gate Threshold Voltage:	V_{IH}	7	3.0	–	–	Vdc
	V_{IL}		–	–	1.5	
Burst Gate Input Current:	I_{IH} (V_{in} = 5.0 V)		–	–	20	µA
	I_{IL} (V_{in} = 0 V)		–	–	–0.5	
4X Subcarrier		5				
Output Voltage: (14.32 MHz)			400	610	650	mVpp
(17.73 MHz)			–	450	–	
Output Impedance: (14.3 MHz and 17.73 MHz)			–	25	–	Ω
Subcarrier Output						
Output Voltage: (3.58 MHz and 4.43 MHz)			200	300	400	mVpp
Output Impedance: (3.58 MHz and 4.43 MHz)		1	–	200	–	Ω
Phase Angle (Note 1)			–	–60	–	deg
Phase Sensitivity (Notes 1 & 2)			–	3.0	–	Note 2
Static Phase Error (Note 2)		1, 2	–	3	–	deg/100 Hz
Phase–Locked Loop Pull–In Range			–	± 350	–	Hz
Phase–Locked Loop Hold–In Range			–	± 500	–	

NOTES: 1. Referenced to composite video input color burst.
2. See paragraph 1 of the Functional Description text.

Figure 1. Typical VCXO Gain

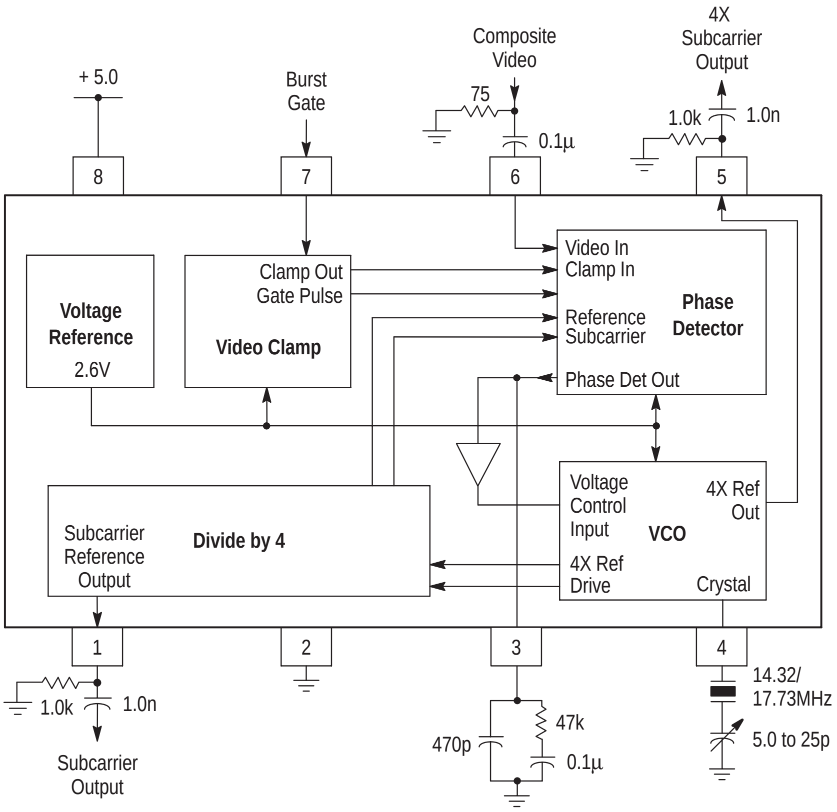


The gain must be estimated from the operating point. KO_{PAL} is the gain for PAL applications and KO_{NTSC} is the gain for NTSC applications.

Table 1. Crystal Specifications

Frequency	14.31818 MHz (NTSC) 17.734475 MHz (PAL)
Mode	Fundamental
Frequency Tolerance @ 25°C df/dfo 0°C – 70°C	40 ppm
Load Capacitance	20 pF
ESR	50 Ω
C1 (Internal Series Capacitance)	15 mpF

Figure 2. Representative Schematic Diagram



FUNCTIONAL DESCRIPTION

The MC44144 is designed to implement the color sync function in a video system. When provided NTSC/PAL composite video or composite chroma and burst gate inputs, the IC will phase–lock a Voltage Controlled Crystal Oscillator (VCXO) to the color burst. Both 4X and 1X subcarrier frequency outputs are provided by the IC. The VCXO operates off of a 4X subcarrier crystal and The VCXO operates off a 4X subcarrier crystal and is capable of at least ± 600 Hz of pull–in. The tradeoff for such a wide pull–in range is a resultant "soft" lock, or a 3° phase shift per 100 Hz *change* in oscillator free–run or input reference frequency.

In addition to providing the gate pulse for the MC44144 phase detector, the Burst Gate input also initiates a clamp pulse that sets up the level of the composite video at the input to the Phase Detector. The start and duration of the Gate Pulse should be timed so that the pulse envelopes the color burst of the video signal, but not so wide as to gate sync or video into the Phase Detector.

The Phase Detector is enabled when the voltage at the Burst Gate input (Pin 7) is above the nominal 2.2 V threshold. While this makes possible the ability to lock to a color burst, it does not exclude the possibility of lock to a constant reference. If a constant source is to be the reference, the Phase Detector can be permanently enabled by holding the voltage on the Phase Detector input pin higher than the threshold voltage.

The phase detector gain must be specified in two ways, for a constant reference and for a burst–locked application. The gain in a constant reference application is specified by the maximum current output with the maximum phase error. For a maximum phase error of $\pi/2$ radians the maximum current available is approximately 200 μA. So the phase detector gain is defined as,

$$KPD = 200/(\pi/2)(\mu A/rad \bullet sec)$$

For a burst–locked application, the Phase Detector is active for only the duration of the color burst. Therefore the phase detector gain must be specified as an average gain over a line period. In this case the phase detector gain for NTSC and for PAL applications is,

$$KPD_{NTSC} = (8/(\pi/2))(\mu A/rad \bullet sec) \text{ and,}$$

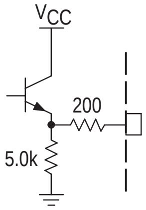
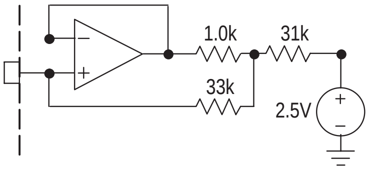
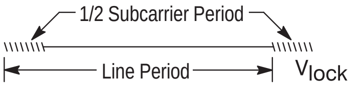
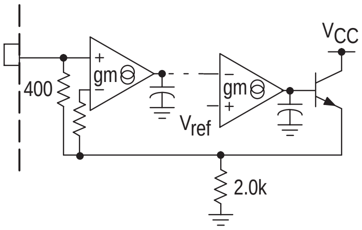
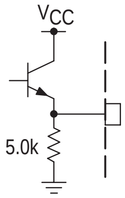
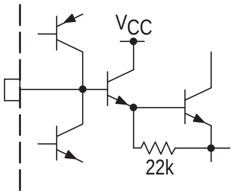
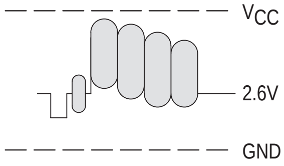
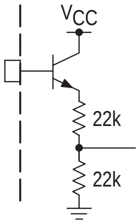
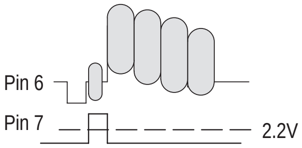
$$KPD_{PAL} = (7/(\pi/2))(\mu A/rad \bullet sec)$$

A suitable filter for both types of applications is shown in the test schematic Figure 2. This same filter also works for both NTSC and PAL applications.

The 4X subcarrier Voltage Controlled Crystal Oscillator (VCXO) uses a design that enables the use of series or parallel resonant types of crystals. Still, layout and crystal positioning are critical as the oscillator frequency is sensitive to shunt capacitance. Care should be taken to keep the crystal close to the IC and crystal switching should be avoided. A suitable parallel type crystal would meet the specifications in Table 1.

A plot showing the VCXO gain is shown in Figure 1. From this plot the gain must be estimated from the operating point. KO_{PAL} is the gain for PAL applications and KO_{NTSC} is the gain for NTSC applications.

PIN FUNCTION DESCRIPTION

Name	Pin	Representative Circuitry	Description	Expected Waveforms
Subcarrier Output	1		Subcarrier Output. A phase–locked reference of the PAL or NTSC color burst is output at this pin.	A 300 mVpp square wave is output. Some high frequency content is present.
Ground	2		Circuit Ground	
Phase Detector Output	3		The error current from the phase detector is output at this pin. A filter circuit should be connected at this pin.	A beat waveform, showing both horizontal period and half the subcarrier period, is present. 
4X Sub Xtal	4		Crystal Oscillator Pin. A 4X subcarrier parallel resonant crystal, in series with a 5.0 to 25 pF trimmer capacitor provides the resonant element for the Voltage Controlled Crystal Oscillator (VCXO).	Approximately 40 mVpp. A scope probe will disturb the frequency of oscillation.
4X Subcarrier Output (or Black Burst)	5		Buffered output from the 4X voltage controlled oscillator.	The sinusoidal $4Xf_{SC}$ oscillator output is available at this pin. The output is nominally: 525 mVpp for NTSC, 425 mVpp for PAL.
Composite Video Input (Black Burst, Continuous Wave, or Composite Chroma can also be applied)	6		Composite Video Input. Color burst from the video present at this pin is used as a reference to phase lock the VCXO. Positive or negative video may be used.	Composite video should be applied at this pin. The color burst amplitude of the input video should be at least 50 mV, but no more than 1000 mV. The waveform at this pin should not exceed ground or V_{CC}. 
Burst Gate Input	7		Input for the phase detector gate pulse. TTL compatible. The threshold is nominally 2.6V.	A positive going gate pulse should be applied at this pin. The Burst Gate input should envelope the color burst. 
V_{CC}	8		Power Supply Pin. 5.0 Vdc should be applied at this pin.	

Linear and TTL Output Buffers

The output buffers of the MC44144 are not designed to any specific logic family. If it is desired, Linear or TTL buffers can be added externally. Figure 3 shows an example of a Linear buffer using an MC3346 Transistor array; virtually any utility transistor can be used. Figure 4 shows a TTL type buffer using an MC74LS04 buffer.

Figure 3. Linear Buffer

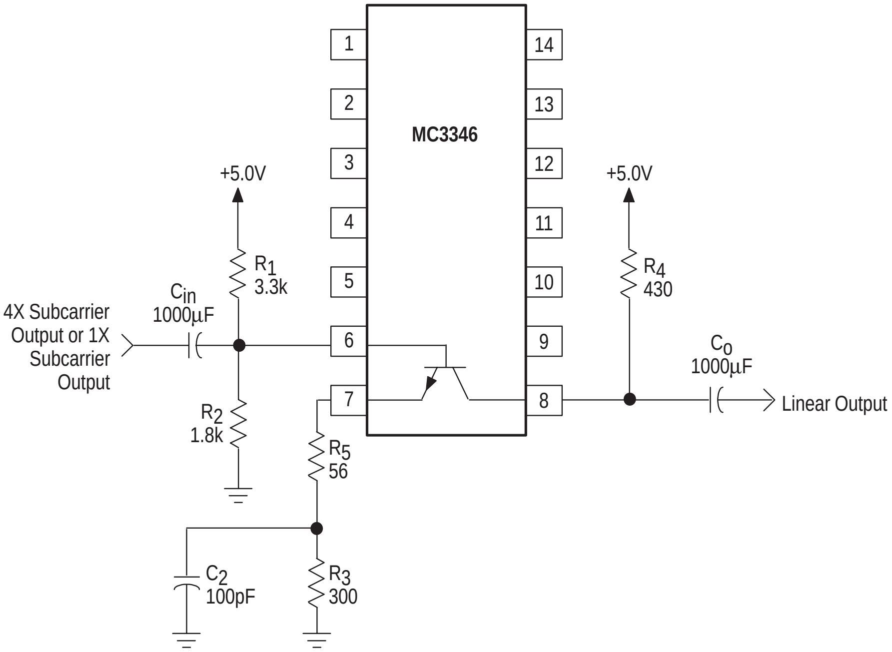
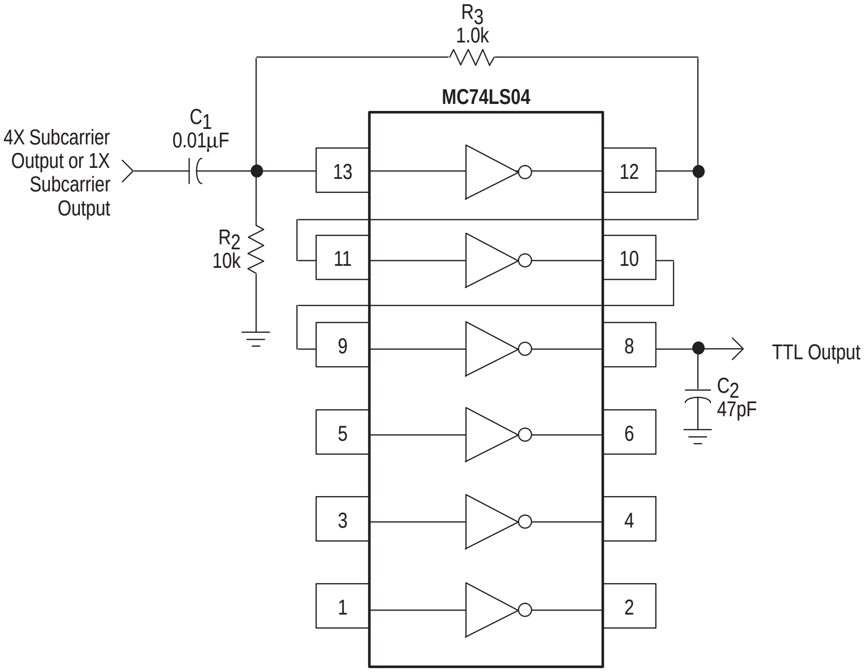


Figure 4. TTL Buffer



MOTOROLA

MC44145

Pixel Clock Generator/ Sync Separator

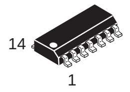
The MC44145, Pixel Clock Generator, is a component of the MC44000 family.

The MC44145 contains a sync separator with composite sync and vertical outputs, and clock generation circuitry for the digitization of any video signal along with the necessary circuitry for clock generation, such as a phase comparator and a divide–by–2 to provide a 50% duty cycle.

The MC44145 is available in a SO–14 package and is fabricated in the Motorola high density, high speed, low voltage, process called MOSAIC 1.5®.

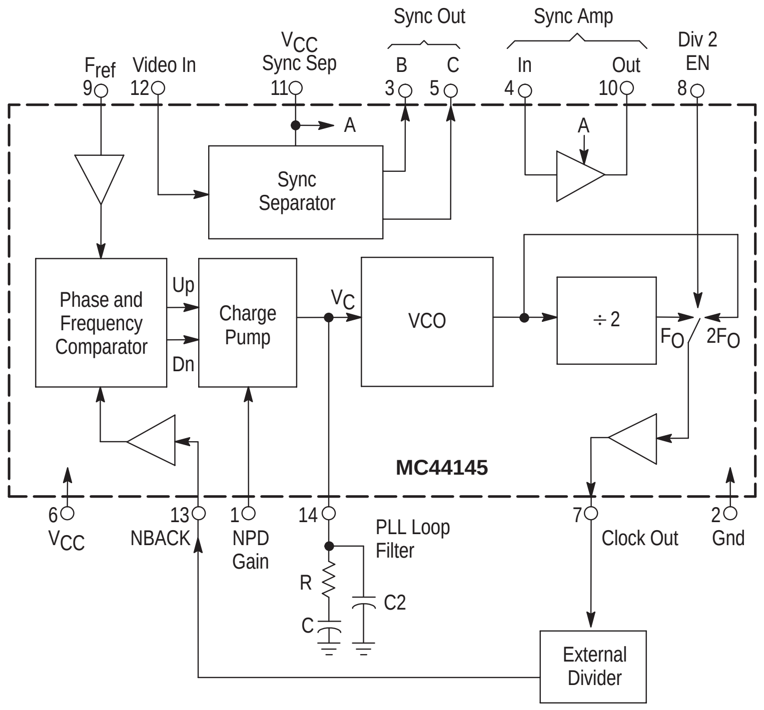
PIXEL CLOCK GENERATOR/ SYNC SEPARATOR

SEMICONDUCTOR TECHNICAL DATA



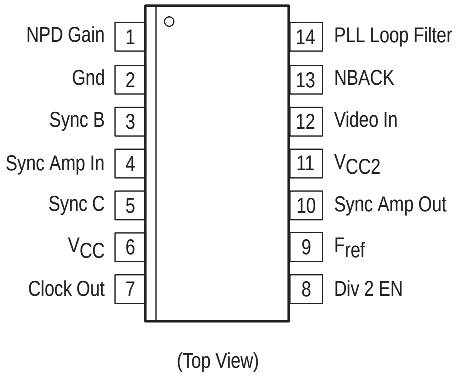
D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO–14)

Representative Block Diagram



This device contains 214 active transistors.

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC44145D	T_A = 0° to +70°C	SO–14

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC} V_{CC2}	6.0 6.0	V
Storage Temperature Range	T_{stg}	–65 to +150	°C
Operating Junction Temperature	T_J	+150	°C

NOTE: ESD data available upon request.

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Pin	Min	Typ	Max	Unit
Supply Voltage	V_{CC} V_{CC2}	6 11	4.75 4.75	5.0 5.0	5.5 5.5	Vdc
Video Input Amplitude (Note 2)	V_{in}	12	0.4	1.0	2.5	Vpp
NBACK Pulse Width	NBACK	13	100	500	–	ns
F_{ref} Pulse Width	F_{ref}	9	100	500	–	ns
Operating Ambient Temperature	T_A	–	0	–	+70	°C

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Note	Pin	Min	Typ	Max	Unit
POWER SUPPLY							
Supply Current (Note 1)	I_{CC}	–	6	–	15.5	–	mA
Supply Current	I_{CC2}	–	11	–	300	–	µA
SYNC SEPARATOR (V_{CC} = 5.0 V; T_A = 25°C, unless otherwise specified.)							
Sync B Output	–	3	3	–	5.0 to 0	–	V
Sync C Output (1.0 mA Source)	–	4	5	–	0 to 3.3	–	V
Slicing Level (S_L)	–	–	12	–	$V_{CC/2}$	–	V
Video Input Sink Current	–	$V_{Pin\ 12} < S_L$	12	–	18	–	µA
Video Input Source Current	–	$V_{Pin\ 12} > S_L$	12	–	1.2	–	µA

NOTES: 1. Operating current for Pin 6 is dependent on the clock frequency (Pin 7). Values given are specified for Pin 14 = 4.0 V.
2. Positive Video.
3. High impedance output.
4. Low impedance output.

ELECTRICAL CHARACTERISTICS (continued)

Characteristic	Note	Pin	Min	Typ	Max	Unit
SYNC SEPARATOR (V_{CC} = 5.0 V; T_A = 25°C, unless otherwise specified.)						
VCO (V_{CC} = 5.0 V; T_A = 25°C, unless otherwise specified, divider disabled.)						
F_{min}	1, 5	7, 8, 14	–	–	10	MHz
F_{max}	1, 4	7, 8, 14	39	42	–	MHz
Control Range	2	14	1.0	–	4.0	V
Transfer Function	1	7, 8, 14	–	14	–	MHz/V
Input Resistance	9	14	0.5	–	–	MΩ
Charge Pump	6 7	1, 14	– –	40 80	– –	µA
Phase Jitter	8	7, 9	–	–	3.0	ns
INPUT BUFFERS (F_{ref} AND NBACK) (T_A = 25°C, unless otherwise specified.)						
Threshold (TTL Compatible)	–	9, 13	–	2.5	–	V
Input Current	–	9, 13	–	–	1.0	µA
OUTPUT BUFFER CLOCK (T_A = 25°C, unless otherwise specified.)						
Sync Amplifier Output High Level	1.0 mA Source	10	2.4	3.0	–	V
Sync Amplifier Output Low Level	1.0 mA Sink	10	–	0.2	0.4	V
Rise Time	11	10	–	–	6.0	ns
Fall Time	11	10	–	–	6.0	ns
Load Capacitance	10	10	–	15	–	pF

NOTES: 1. Internal divider disabled.
2. 0 V stops the oscillator.
3. Divider ÷2 active.
4. V_C = 4.0 V.
5. V_C = 1.0 V.
6. PFD gain low.
7. PFD gain high.
8. VCO alone.
9. V_C = 4.0 V, charge pumps off.
10. 2 LSTTL loads.
11. With cap load 15 pF and between 10 and 90% of 0.4 and 2.4 V.

CIRCUIT DESCRIPTION

Composite Sync Separator

The composite sync separation section is comprised of two blocks, a sync slicer and a sync amplifier, which can be used to extract the vertical sync and composite sync information from a video signal.

The sync separator is an adaptive slicer in which the video signal is slightly integrated and then sliced at a ratio of 4.7 to 64 which corresponds to the sync to horizontal ratio. Two outputs are given, one of high impedance and the other low impedance.

A slicing sync inverting amplifier is also on–chip, allowing one output to be used for composite sync and the other output to be integrated and then sliced using the slicing amplifier to extract the vertical sync information.

Clock Generation

The clock generation is made up of a wide ranging emitter–coupled VCO followed by a switchable ÷2 to provide a 50% duty cycle wherever required, or twice the set frequency if an external divider is used. The clock generator is a PLL subsection; its function is the generation of a high frequency, line locked clock that is used for video sampling and digitizing.

The clock output is a LSTTL–like buffer which has a limited drive capability of two LSTTL loads.

The VCO is driven from a charge pump with selectable current. The charge pump is driven by the phase comparator.

The phase comparator is a type IV “phase and frequency comparator” sequential circuit.

The clock generator, the heart of a PLL, is to be closed by means of an external divider, thus setting the synthesized frequency. This divider could be implemented in discrete logic or be a part of an ASIC subsystem.

Phase and Frequency Comparator

The phase comparator is fed from two input buffers, F_{ref} which expects a reference frequency at line rate and that is rising edge sensitive, and NBACK which comes from the external divider and is falling edge sensitive.

Charge pump current and output divider action are controlled by applying suitable voltage on the appropriate pins (respectively, NPD Gain and Div 2 EN).

PIN FUNCTION DESCRIPTION

Pin	Function	Description
1	NPD Gain	This pin sets the gain of the phase frequency detector by changing the current of the charge pump output (40 µA or 80 µA). Low current with this pin > 2.0 V, high current for < 0.5 V.
2	Ground	Ground connection common to the PLL and sync separator sections.
3	Sync B	High impedance sync output.
4	Sync Amp In	Sync amplifier input.
5	Sync C	Low impedance sync output.
6	V_{CC}	Power connection to the PLL section.
7	Clock Out	VCO clock output. Capable of limited LSTTL drive. It should not be used to drive high capacitive loads, such as long PCB traces or coaxial lines.
8	Div 2 EN	The divider is switched in with this pin > 2.0 V; switched out for < 0.5 V.
9	F_{ref}	Reference frequency input to the phase and frequency comparator. Typically this will be a 15625 (15750) Hz signal. It is rising edge sensitive. Due to the nature of the phase and frequency comparator, no missing pulses are tolerable on this input. In a typical setup, this signal can be provided by the MC44011.
10	Sync Amp Out	Sync amplifier output.
11	V_{CC2}	Power connection to the sync separator and amplifier.
12	Video In	Video signal input to the sync separator.
13	NBACK	Fed by the external clock divider. Sets the multiplication ratio of the loop in multiples of the F_{ref} frequency. Negative edge sensitive.
14	PLL Loop Filter	See loop filter calculations at the end of this document.

NOTE: The two V_{CC} pins are not independent, as they are internally connected by means of the input protection diodes; they must always be both connected to a suitable V_{CC} line.

CIRCUIT OPERATION

Composite Sync Separator

The sync separator is an adaptive slicer. It will output “raw” sync data. Two outputs are given, thus allowing one output to be used for composite sync and the other output to be integrated and then sliced using the inverting slicing amplifier provided. As the input of the slicing amplifier is external, the amplifier may be driven from either sync output, although normally the high impedance output (Sync B) would be recommended.

The positive video input signal required is nominally 1.0 V sync–to–white, but the circuit supports signals above and below this level and also is resistant to a degree of reflections on the signal. Coupling to the sync separator may be achieved by a simple capacitor of 100 nF, but better results may be obtained with a higher value in series with a resistance of 1.0 kΩ.

Clock Generator

The system is best put to use in a dual loop configuration; a first loop locks to line frequency by means of a type I phase detector (multiplier type) which is insensitive to missing pulses. This PLL is then followed by a second loop using the MC44145, performing frequency multiplication. The phase comparator of the MC44145 is frequency and phase sensitive. It is a type IV (sequential type) phase detector, which does not tolerate missing pulses. The dual loop structure makes up a noise insensitive frequency (and phase) locked loop.

The phase and frequency comparator provides two logical outputs, mutually exclusive – up or down – that are used to source or sink current to and from the loop filter. This current can be user–selected to be 40 µA or 80 µA (typical), thus providing some degree of loop gain control.

The VCO is an emitter–coupled multivibrator type, with an on–chip timing capacitor, and has been designed for low phase noise.

The divide–by–2 is included at the output of the VCO, thus allowing for a precise 50% duty cycle, hence the VCO is operating at twice the required frequency. The divider can be bypassed, bringing the VCO output directly to the output buffer.

The external divider must provide a feedback pulse to close the loop; the falling edge of this pulse will be aligned (when the loop is in lock) with the rising edge of the pulse applied to the F_{ref} input. Operation of the phase comparator is insensitive to the duty cycle of both its inputs. The feedback pulse should have a minimum width of 500 ns. This can be guaranteed if it has a length of at least 16 output clock cycles (highest output frequency with the divider disabled).

APPLICATION INFORMATION

Analog video signals out of the MC44011 are sampled and converted to 8–bits digital in the A/D converter (MC44250 series) by means of the clock provided by the MC44145, pixel clock generator (see Figure 1).

The frame store contains the memory, the necessary logic for the memory addressing, as well as the counter to set the frequency multiplication ratio of the line locked clock generator (H. Count).

Figure 1. Application Block Diagram

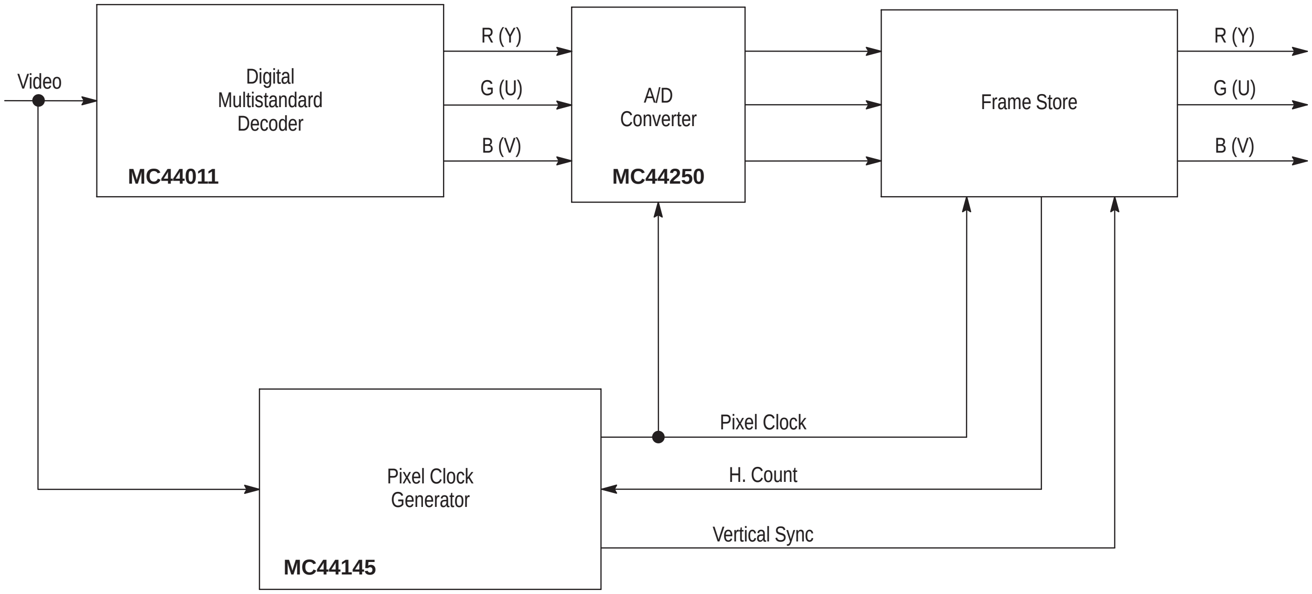


Figure 2.

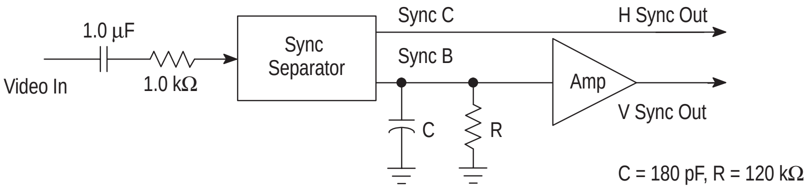


Figure 3. Typical VCO Transfer Characteristics

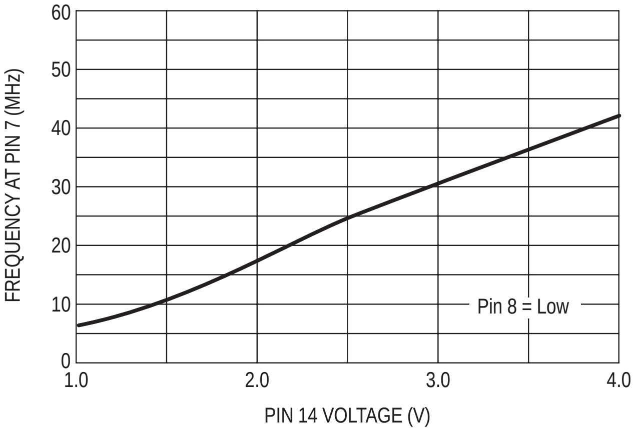
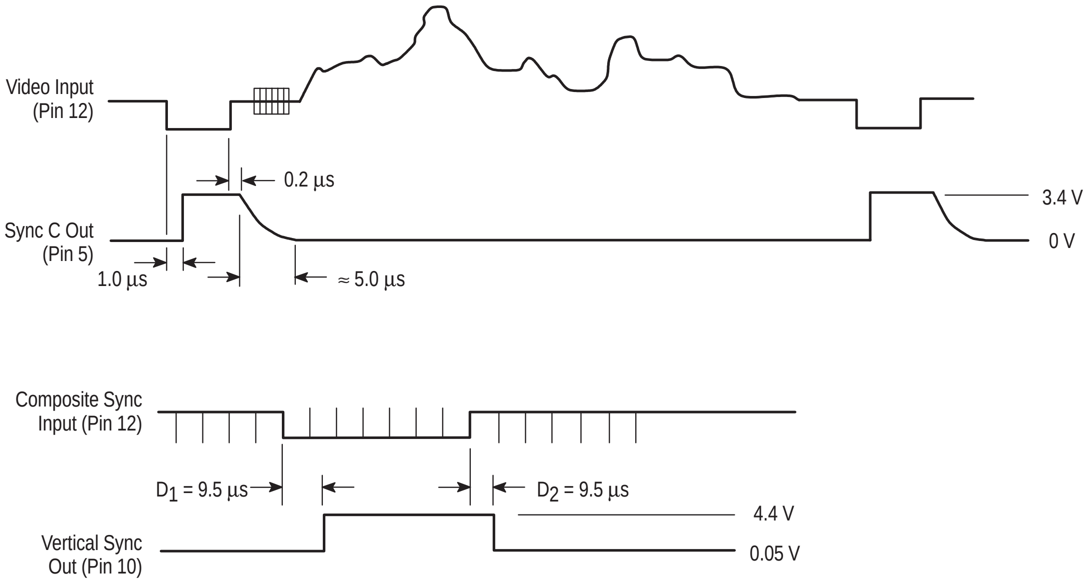


Figure 4. Sync Separator Timing



Note: D_1 and D_2 depend on the value of R and C connected to Pin 3. They are specified here for the values: R = 120 kΩ, and C = 180 pF.

LOOP FILTER CALCULATION

This section is not intended as a complete loop theory; its aim is merely to point out the peculiarities of the loop, and provide the user with enough information for the filter components selection. For a more in–depth covering, the cited reference should be consulted, especially [1].

The following remarks apply to the loop:

- The loop frequency is 15 kHz.
- In spite of the sampled nature of the loop, a continuous time approximation is possible if the loop bandwidth is sufficiently small.
- Ripple on V_C is a function of the loop bandwidth
- The loop is a type II, 3rd order; however, since C2 is small, the pole it creates is far removed from the low frequency dominant poles, and the loop can be analyzed as a 2nd order loop.

These remarks apply to the PFD:

- Phase and frequency sensitive.
- Independent of duty cycle.
- PFD has 3 allowed states: up, down, hi–Z
- The VCO is always pulled in the right direction (during acquisition).
- PFD gain is higher near lock.

The last two remarks imply that only the higher value need be taken into account, as acquisition will be slower, but always in the proper direction, whereas the higher gain will enter the action as soon as the error reaches $\pm 2\pi$.

The following values are selected and defined (see Block Diagram):

C2 = C/10 or less, to satisfy the requirement that the effect of C2 on the low frequency response of the loop be minimal, and similar to a second order loop.

$\zeta = 0.707$ for the damping factor.

$\omega i = 15625 \text{ x } 2\pi$ the input pulsation.

$\tau = RC$ as the loop filter.

$K = Ko \text{ x } Ip \text{ x } R/(2 \text{ x } \pi \text{ x } N)$ the loop gain.

$K' = K \text{ x } \tau = 4\zeta^2$ is the “normalized” loop gain.

$Ko = 57 \text{ x } 10^6$ [rad/Vs] (9.0 MHz/V).

Stability analysis, with C2 = C/10 and $K' = 2$ ($\zeta = 0.707$) gives a minimum value of 7.5 for the ratio $\omega i/K$ and to have some margin, a reasonable value can be 15 to 20 or higher [1].

Selecting $\omega i/K = 20$, gives : $K = \omega i/20 \approx 5000$.

With $K' = 2$, $\tau = 2/K = 400$ µs.

Using $K = Ko \text{ x } Ip \text{ x } R/(2 \text{ x } \pi \text{ x } N)$ and setting $Ip = 60$ µA, and N an average value of 1000, we get R = 9.1 kΩ.

Then for $\tau = 400$ µs, C becomes 47 nF and C2, 4.7 nF.

With these values, the loop natural frequency (ωn) and the loop bandwidth ($\omega 3dB$) can be calculated:

$\omega n = [(Ko/N) \text{ x } Ip/(2\pi C)^{1/2} = 3400$ and

$fn = 3400/2\pi = 540$ Hz.

$\omega 3dB = 2 \text{ x } \omega n = 1080$ Hz (valid if ζ is close to 0.707).

References:

[4] Charge–Pump Phase–Lock Loops, Floyd M. Gardner, IEEE transactions on communications, vol. com–28 no. 11 November 1980
[5] Phaselock Techniques, Floyd M. Gardner, J. Wiley & Sons, 1979
[6] Phase–Locked Loops, Roland E. Best, McGraw–Hill, 1984
[7] Phase–Locked Loop Systems, Motorola

MOTOROLA

MC44353
MC44354
MC44355

**MULTI–STANDARD
AND PAL/NTSC
MODULATOR ICs**

**SEMICONDUCTOR
TECHNICAL DATA**

Product Preview

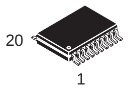
PLL Tuned UHF Audio/Video Modulator ICs for PAL, SECAM and NTSC TV Systems

MC44353 – Multi–Standard Modulator IC
MC44354 – PAL/NTSC Modulator IC
MC44355 – PAL/NTSC Modulator IC with Fixed Video Modulation Index

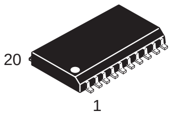
These modulator circuits are intended for use in VCRs, satellite receivers, set–top boxes, video games, etc. An on–chip high speed I^2C compatible bus receiver is included and is used to set the channel, tuned by a PLL over the full range in the UHF bands. The modulator incorporates a sound subcarrier oscillator, using a second PLL to derive 4.5, 5.5, 6.0 and 6.5 MHz carrier frequencies, selectable by the bus.

For the sound, either frequency modulation with pre–emphasis or amplitude modulation (MC44353 only) is possible. A control bit (MC44353 only) is used to select AM sound with positive RF modulation (system L). The level of the sound carrier with respect to the vision carrier and the modulation depth of both sound and vision may be adjusted by means of the bus. In addition, an on–chip video test pattern generator may be switched in with a 1.0 kHz audio test signal.

- UHF Operation (471 MHz to 855 MHz)
- On–Chip Low Power Operational Amplifier for Direct Tuning Voltage Output
- Single–Ended Output for Low Cost and Ease of Interface
- Low External Component Count
- High Speed I^2C Bus Compatible (Min 500 kHz)
- Programmable Video Modulation Depth (8 Steps of 2.5%)
- Programmable Picture/Sound Carriers Ratio and Audio Sensitivity (8 Steps of 1.0 dB)
- Programmable Sound Subcarrier Oscillator (4.5 MHz to 6.5 MHz)
- Video Test Pattern Generator with Sound Test Signal (1.0 kHz)
- V_{CC} Standby Mode (Typ 500 µA)
- Transient Output Inhibit During PLL Lock–Up at Power–On



DTB SUFFIX
PLASTIC PACKAGE
CASE 948E
(TSSOP–20)

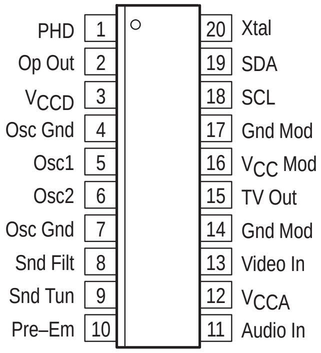


DW SUFFIX
PLASTIC PACKAGE
CASE 751D
(SO–20L)

ORDERING INFORMATION

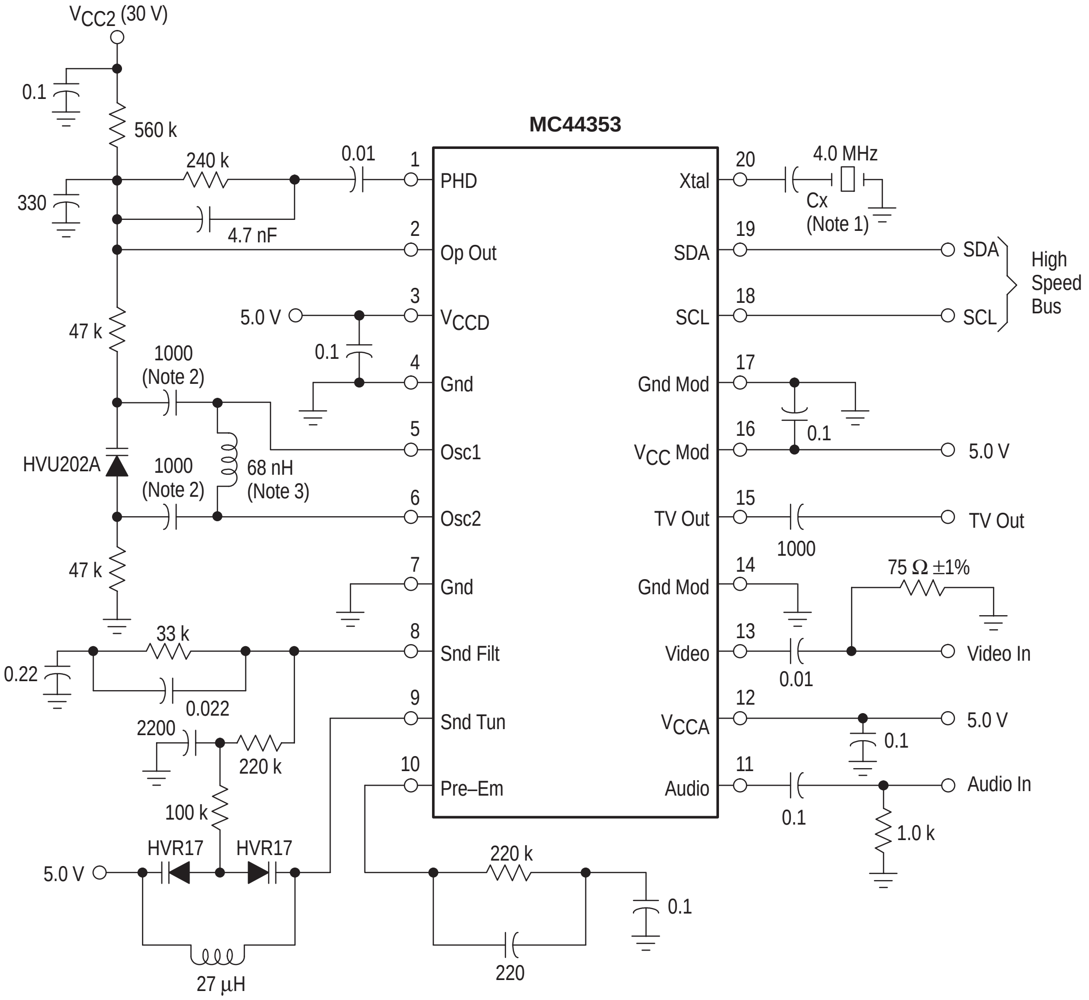
Device	Operating Temperature Range	Package
MC44353DTB	T_A = –20° to +80°C	TSSOP–20
MC44353DW		SO–20L
MC44354DTB		TSSOP–20
MC44354DW		SO–20L
MC44355DTB		TSSOP–20
MC44355DW		SO–20L

PIN CONNECTIONS



(Top View)

Typical Application



NOTES: 1. Cx depends on Crystal Load Capacitance, Crystal resistance < 200 Ω.
2. Tubular 0603 1000 pF capacitors.
3. UHF Coil is a surface mount 0805 Chip Inductor, REF: AVX/KYOCERA – L0805 6R8 DEW ±0.5 nH (@ 450 MHz Q = 43, @ 900 MHz Q = 62 and L = 7.0 nH)

MODULATOR FUNCTIONAL DESCRIPTION

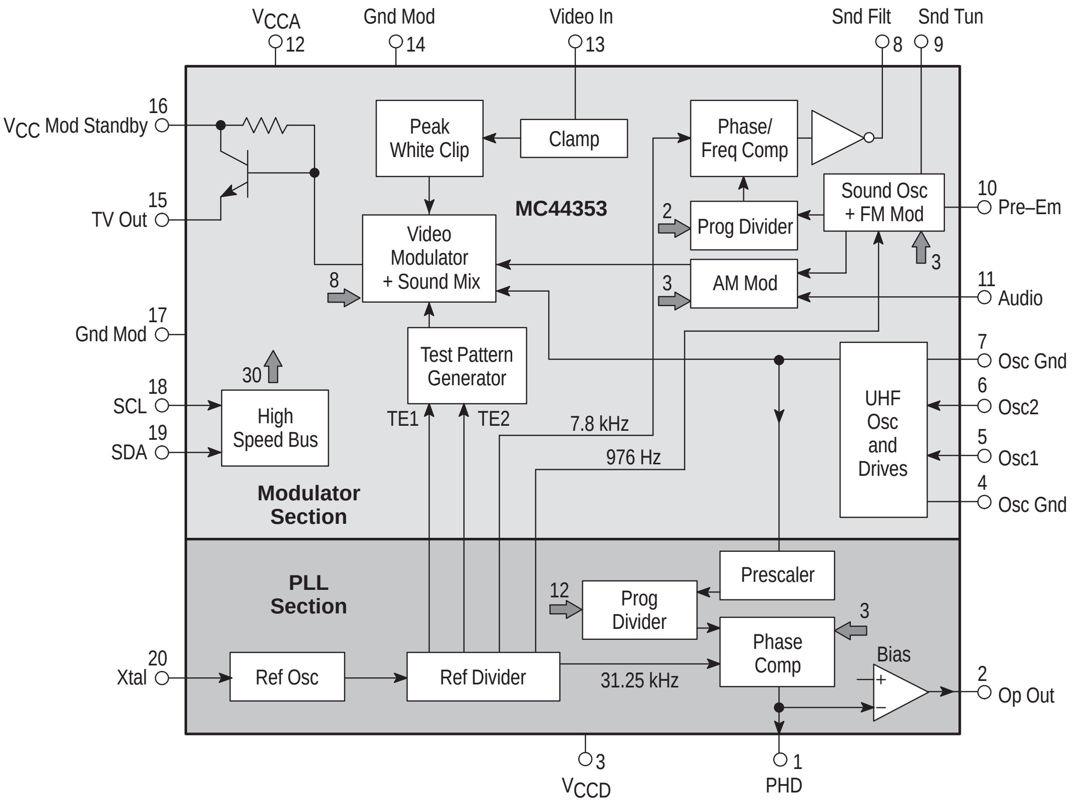
General

The device has two main sections; a PLL section to synthesize the channel frequency of the UHF output and a modulator section which accepts audio and video inputs and modulates the UHF carrier with them.

The channel frequency, sound and picture modulation index and sound/picture carrier ratio are all programmable by means of a high speed I^2C compatible bus. An on–chip video test pattern generator with an audio test signal is also included.

The MC44353 is designed to operate as a multi–standard modulator and can handle the systems B/G, D/K, H, I, L and N with the same external circuit components.

Figure 1. MC44353 Simplified Block Diagram



MOTOROLA

MC44461

Advance Information

Picture-in-Picture (PIP) Controller

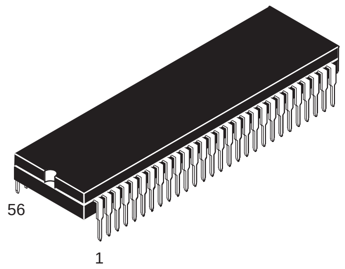
PICTURE–IN–PICTURE (PIP) CONTROLLER

SEMICONDUCTOR TECHNICAL DATA

The MC44461 Picture–in–Picture (PIP) controller is a member of Motorola's low cost PIP family. It is NTSC compatible and contains all the analog signal processing, control logic and memory necessary to provide for the overlay of a small picture from a second non synchronized source onto the main picture of a television. All control and setup of the MC44461 is via a standard two pin I^{2}C bus interface. The device is fabricated using BICMOS technology. It is available in a 56–pin shrink dip (SDIP) package.

The main features of the MC44461 are:

- Two NTSC CVBS Inputs
- Switchable Main and PIP Video Signals
- Single NTSC CVBS Output Allows Simple TV Chassis Integration
- Two PIP Sizes; 1/16 and 1/9 Screen Area
- Freeze Field Feature
- Variable PIP Position in 64–X by 64–Y Steps
- PIP Border with Programmable Color
- Programmable PIP Tint and Saturation Control
- Automatic Main to PIP Contrast Balance
- Vertical Filter
- Integrated 64 k Bit DRAM Memory Resulting in Minimal RFI
- Minimal RFI Allows Simple Low Cost Application into TV
- I^{2}C Bus Control – No External Variable Adjustments Needed
- Operates from a Single 5.0 V Supply
- Economical 56–Pin Shrink DIP Package



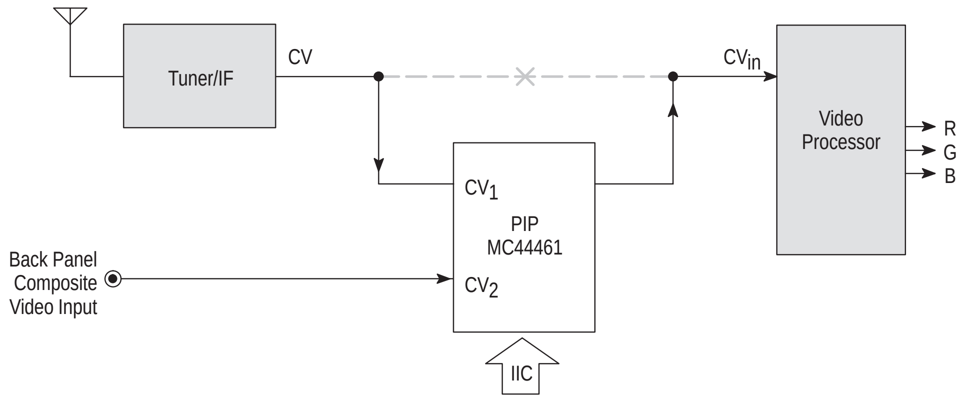
B SUFFIX
PLASTIC PACKAGE
CASE 859
(SDIP)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC44461B	T_J = –65° to +150°C	SDIP

For surface mount package availability, contact your local Motorola sales office or authorized distributor.

Composite Video Simplified System Diagram



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{DD}	–0.5 to +6.0	V
Power Supply Voltage	V_{CC}	–0.5 to +6.0	V
Input Voltage Range	V_{IR}	–0.5, V_{DD} + 0.5	V
Output Current	I_O	160	mA
Power Dissipation Maximum Power Dissipation @ 70°C Thermal Resistance, Junction–to–Air	 P_D $R_{\theta JA}$	 1.3 59	 W °C/W
Junction Temperature (Storage and Operating)	T_J	–65 to +150	°C

NOTE: ESD data available upon request.

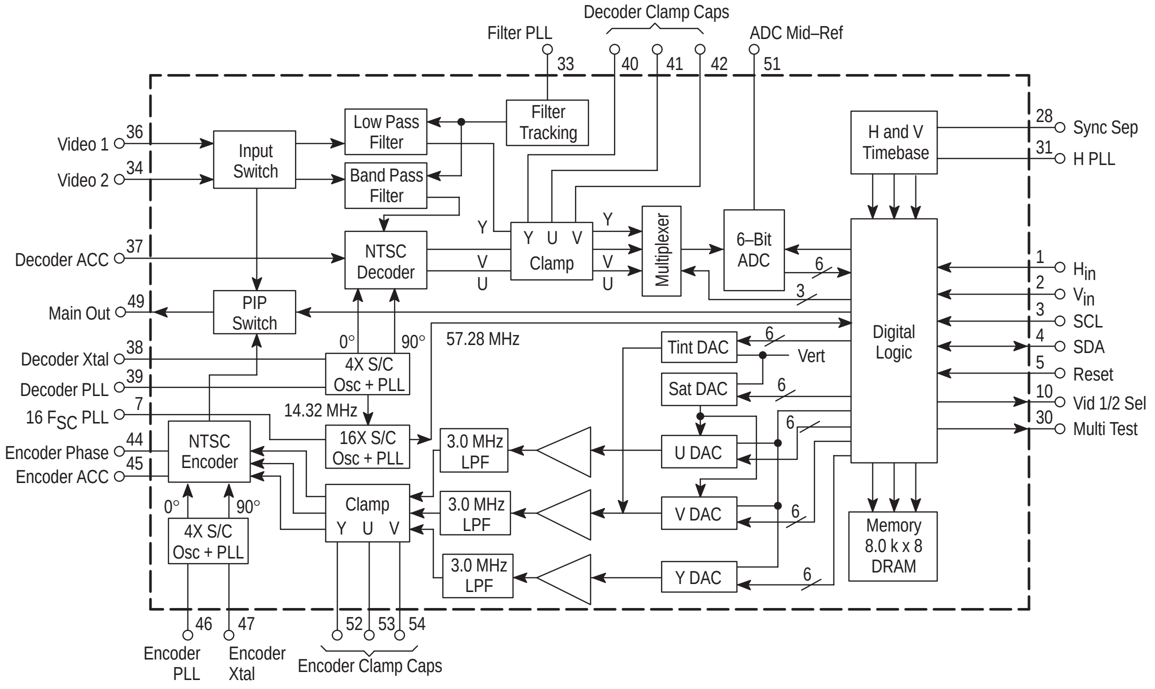
ELECTRICAL CHARACTERISTICS ($V_{CC} = V_{DD} = 5.0$ V, $T_A = 25$°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
POWER SUPPLY					
Total Supply (Pins 8, 15, 43 and 50)	Total I_{Supply}	–	100	160	mA
VIDEO					
Composite Video Input (Pin 34 or 36)	CVi	–	1.0	–	Vpp
Composite Video Output (Pin 49, Unterminated)	–	–	2.0	–	Vpp
Video Output DC Level (Sync Tip)	–	–	1.0	–	Vdc
Video Gain	–	–	6.0	–	dB
Video Frequency Response (Main Video to –1.0 dB)	–	–	10	–	MHz
Color Bar Accuracy	–	–	±4.0	–	deg
Video Crosstalk (@ 75% Color Bars) Main to PIP PIP to Main	–	 – –	 55 55	 – –	dB
Output Impedance	–	–	5.0	–	Ω
HORIZONTAL TIMEBASE					
Free Run HPLL Frequency (Pin 16)	–	–	15734	–	Hz
HPLL Pull–In Range	–	–	±400	–	Hz
HPLL Jitter	–	–	±4.0	–	ns
Burst Gate Timing (from Trailing Edge Hsync, Pin 24)	–	–	1.0	–	µs
Burst Gate Width	–	–	4.0	–	µs
VERTICAL TIMEBASE					
Vertical Countdown Window	–	–	232/296	–	H lines
Vertical Sync Integration Time	–	–	31	–	µs
ANALOG TO DIGITAL CONVERTER					
Resolution	–	–	6	–	Bits
Integral Non–Linearity	–	–	±1	–	LSB
Differential Non–Linearity	–	–	+2/–1	–	LSB
ADC – Y Frequency Response @ –5.0 dB	–	–	1.0	–	MHz
ADC – U, V Frequency Response @ –5.0 dB	–	–	200	–	kHz
Sample Clock Frequency (4/3 F_{SC})	–	–	4.773	–	MHz

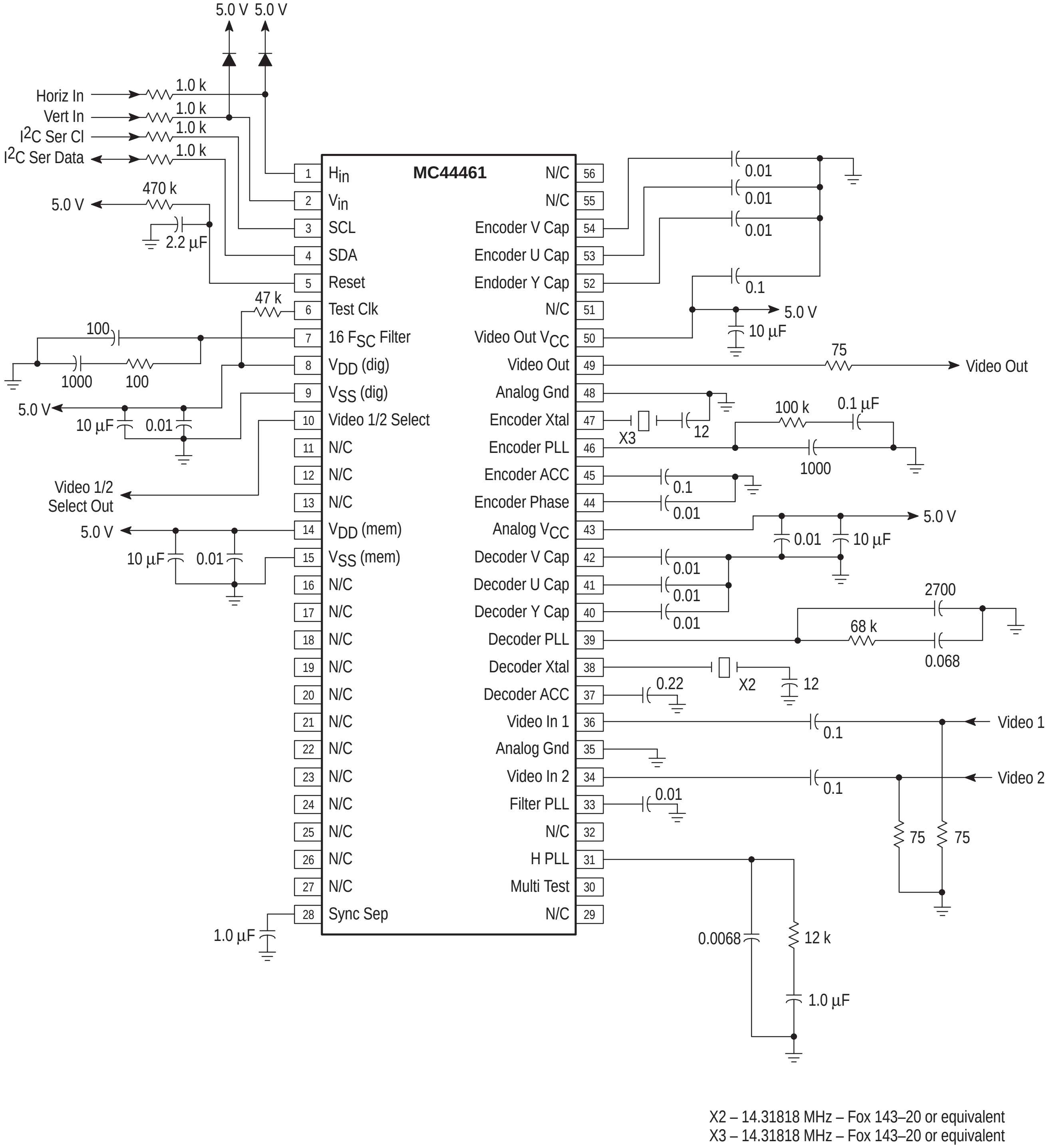
ELECTRICAL CHARACTERISTICS (continued) (V_{CC} = V_{DD} = 5.0 V, T_A = 25°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
DIGITAL TO ANALOG CONVERTER					
Resolution	–	–	–	6	Bits
Integral Non–Linearity	–	–	±1	–	LSB
Differential Non–Linearity	–	–	+2/–1	–	LSB
Tint DAC Control Range (in 64 Steps)	–	–	±10	–	Deg
Saturation DAC Control Range (in 64 steps)	–	–	±6.0	–	dB
NTSC DECODER					
Color Kill Threshold	–	–	–24/–16	–	dB
Threshold Hysteresis	–	–	3.0 ±1.0	–	dB
ACC (Chroma Amplitude Change, +3.0 dB to –12 dB)	–	–	±0.5	–	dB
PIP CHARACTERISTICS					
PIP Size	–				
1/9 Screen Horizontal		–	114	–	pels
1/9 Screen Vertical		–	71	–	lines
1/16 Screen Horizontal		–	84	–	pels
1/16 Screen Vertical		–	53	–	lines
Border Size Horizontal	–	–	3	–	pels
Border Size Vertical	–	–	2	–	lines
Output PEL Clock (4 F_{SC})	–	–	14.318	–	MHz
Position Control Range Horizontal (% of Main Picture), 64 Steps	–	–	100	–	%
Position Control Range Vertical (% of Main Picture), 64 Steps	–	–	100	–	%

Figure 1. Representative Block Diagram



This device contains approximately 500,000 active transistors.

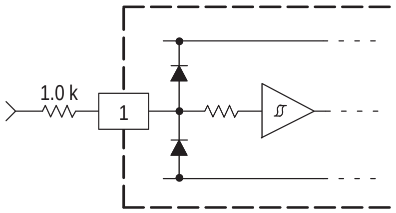
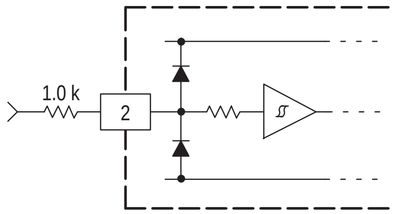
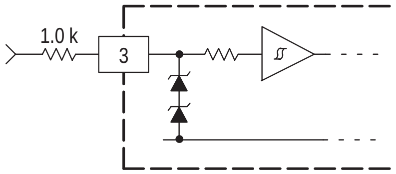
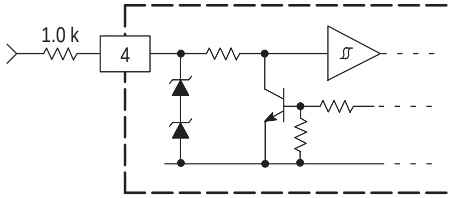
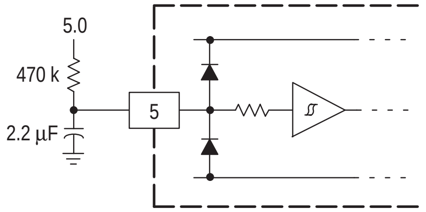
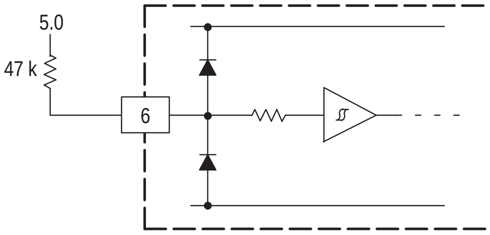
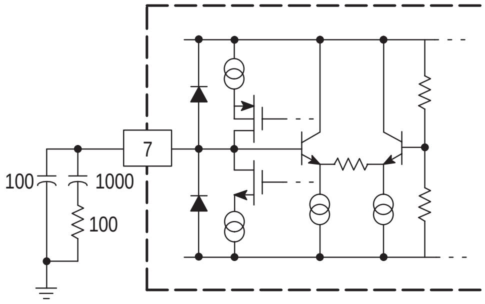


X2 – 14.31818 MHz – Fox 143–20 or equivalent
X3 – 14.31818 MHz – Fox 143–20 or equivalent

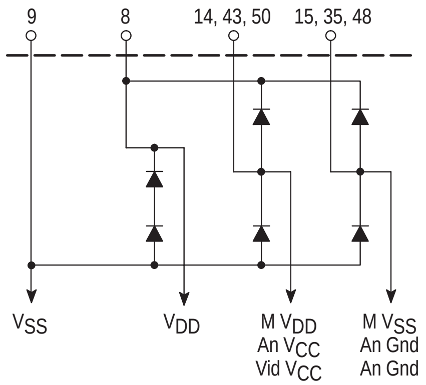
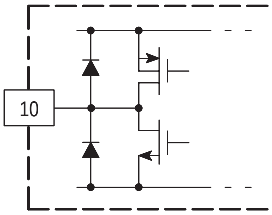
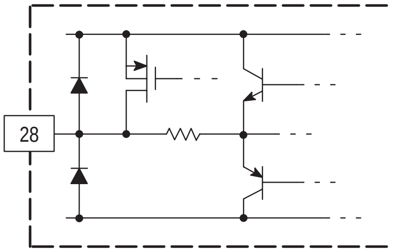
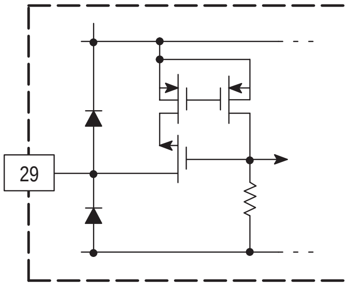
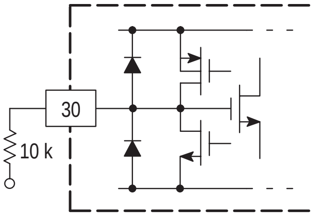
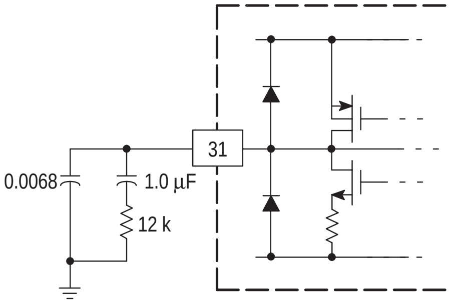
Figure 2. Application Circuit

NOTE: For proper noise isolation, Power Supply Pins 8, 14, 43 and 50 should be bypassed by both high and low frequency capacitors. As a guideline, a 10 µF in parallel with a 0.1 µF at each supply pin is recommended.

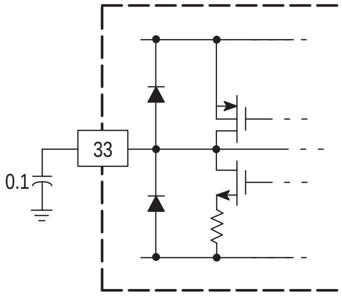
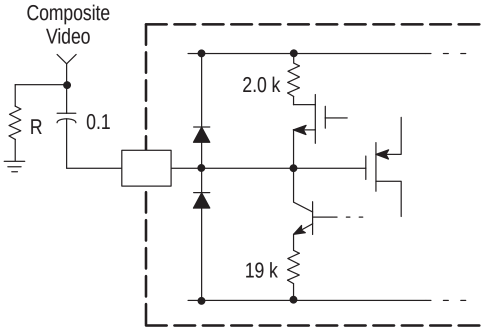
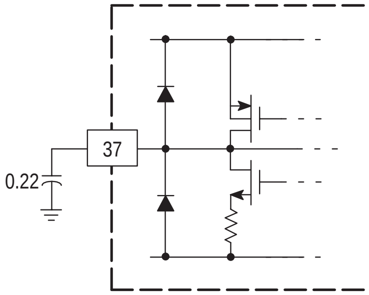
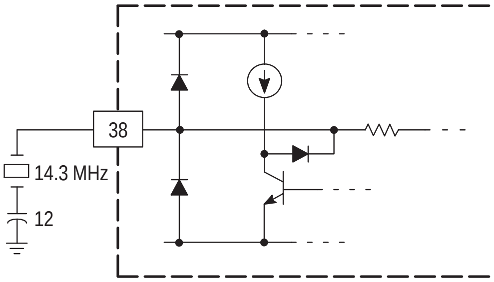
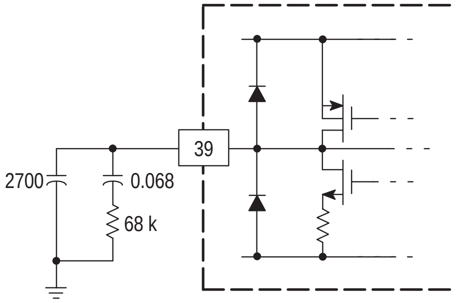
PIN FUNCTION DESCRIPTION

Pin	Equivalent Internal Circuit	Description
1		**Horizontal Reference In (H_{in})** CMOS level pulse synchronous with TV horizontal retrace signal. This pulse may be active high or low since there is a polarity selector bit in an internal control register. *This pulse should begin 0.5 to 0.75 µs after the beginning of the main video H sync period.* Its duty cycle should be less than 50%.
2		**Vertical Reference In (V_{in})** CMOS level pulse synchronous with TV vertical retrace signal. This pulse may be active high or low since there is a polarity selector bit in an internal control register. This pulse should begin during the main video vertical interval and have a duration of at least .5H.
3		**Serial Clock (SCL)** CMOS level I^{2}C Compatible slave only clock input. 100 kHz Maximum frequency. 50% duty cycle. See Figure 4 for timing. See I^{2}C Register Description for internal register descriptions and addresses.
4		**Serial Data (SDA)** CMOS level I^{2}C Compatible slave only data input/output. As an output it is open collector. See Figure 4 for timing. See I^{2}C Register Description for internal register descriptions and addresses.
5		**Reset** The active low, Power On Reset initializes all internal registers to zero and resets the I^{2}C interface. Minimum active low time required for Power On Reset reset is 100 ms.
6		**Test Clock**
7		**PLL Filter** Filter for the 16X S/C PLL which is phase locked to the 4X S/C oscillator.

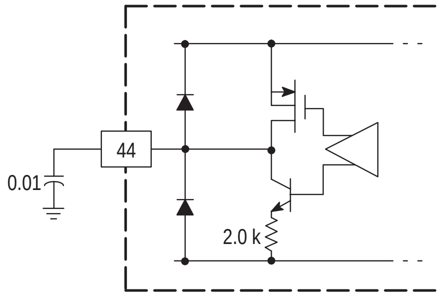
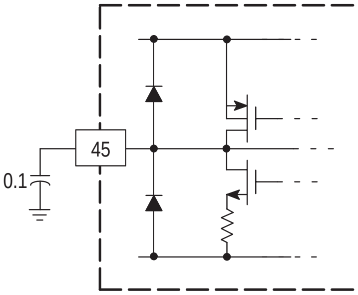
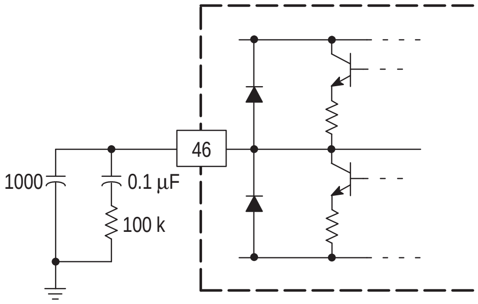
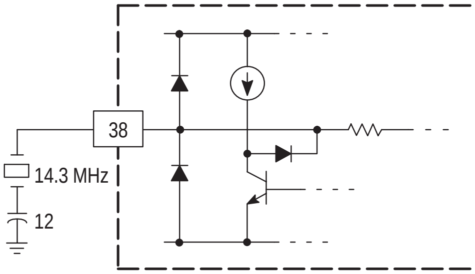
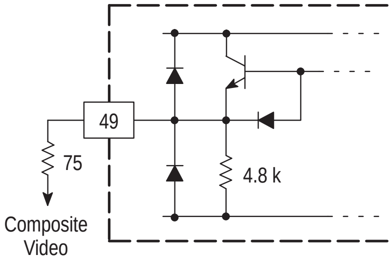
PIN FUNCTION DESCRIPTION (continued)

Pin	Equivalent Internal Circuit	Description
8 14, 43, 50 9 15, 35, 48		**V_{DD}, V_{SS}** The four V_{DD} pins must be externally connected to a 5.0 V (±5%) supply. The four V_{SS} lines must externally connect to their respective V_{DD} bypass return(s) to ensure that no ground disturbances occur in operation. All supplies must be properly bypassed and isolated for the application. Bypass capacitors of 10 µF in parallel with 0.1 µF for each supply are recommended as a general guideline. The 0.1 µF, high frequency bypass capacitors should be placed as close to the power pins as practical.
10		**Video 1/2 Select Output** High output level indicates that Video 1 is selected to be the main picture video. Low output level indicates Video 2 is selected to be the main picture video.
28		**Sync Out** Outputs the video signal selected as the PIP to be filtered and applied to the H and V timebase through the Sync In pin.
29		**Sync In** PIP sync pulses are externally filtered and applied to the H and V timebase to allow H and V synchronization.
30		**Multi Test** Under control of I^2C bus output signals for test and adjustment are provided through this pin.
31		**H PLL** Connection for horizontal timebase PLL filter.

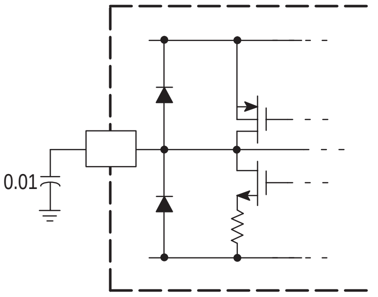
PIN FUNCTION DESCRIPTION (continued)

Pin	Equivalent Internal Circuit	Description
33		**Filter PLL** The on board reference filter produces a phase shift which is measured and applied to an internal filter PLL. This capacitor connected to this pin stores the phase correction voltage for the PLL which sets the 90° phase correction reference for the rest of the on chip filters.
36 and 34		**Video Input 1 and 2** Accepts ac coupled 1.0 Vpp composite video input usually from a source generated inside the TV and an external video source. The series coupling capacitor also functions as the storage capacitor for the clamp voltage for the input circuit. It is necessary to return the input of this capacitor to ground through a dc low impedance to enable this clamp function. R = 50 to 100 Ω is acceptable.
37		**Decoder ACC** The Decoder ACC pin provides access to the internal chroma decoder automatic gain control amplifier. The ACC capacitor filters the feedback loop of this amplifier. During PIP burst gate time a voltage proportional to the burst gate magnitude is stored on the capacitor connected to this pin to compensate for input chroma level variation and provide a constant U and V output level to the A/D conversion stage.
38		**Decoder Crystal** 4X Sub–Carrier crystal used to synchronize the decoding of the PIP UV information prior to A/D conversion, sub–sampling and storage in the field memory. The crystal frequency is 14.31818 MHz.
39		**Decoder PLL** Connection for Decoder PLL filter.

PIN FUNCTION DESCRIPTION (continued)

Pin	Equivalent Internal Circuit	Description
44		**Encoder Phase** Phase difference of the main to encoded burst is sampled and applied to the capacitor connected to this pin to shift the phase of the re–encoded chrominance to match the main.
45		**Encoder ACC** The Encoder ACC pin provides access to the internal chroma reference sample and hold circuit, which stores the sampled value of the main channel chroma burst amplitude on this external ACC capacitor. The ACC amplifier matches the chroma amplitude of the insert picture to that of the main picture.
46		**Encoder PLL** Connection for Encoder PLL filter. See separate discussion for filter values.
47		**Encoder Crystal** 4X Sub–Carrier crystal used to synchronize the encoding of the PIP YUV from the field memory with the main video. The output from this PLL is phase corrected to match the PIP video signal to the main video at the PIP switch. The crystal frequency is 14.31818 MHz.
49		**Video Out** The selected Video 1/2 input is available at the Video Out mixed with the PIP overlay when selected. This signal is a nominal 2.0 V peak–to–peak signal unterminated. This connection is intended to drive an external series 75 Ω load into a 75 Ω termination to ground to provide a 1.0 Vpp signal at the termination.

PIN FUNCTION DESCRIPTION (continued)

Pin	Equivalent Internal Circuit	Description
54, 53, 52, 42, 41, 40		**Encoder and Decoder YUV Caps** During the internal H rate clamping time the YUV reference levels are set by the charge on the capacitors attached to these pins. The nominal value of these capacitors should be 0.01 µF.

SOFTWARE CONTROL OF THE MC44461

Communications to and from the MC44461 follows the I^{2}C interface protocol defined by the Philips Corporation. In simple terms, the I^{2}C is a two line, multi–master, bidirectional bus used for data transfer. Although an I^{2}C system can be multi–master, the MC44461 never functions as a master.

The MC44461 has a write address of $24 and a flag read address of $25. A block diagram of the I^{2}C interface is shown in Figure 3. Writing to the MC44461 registers can cause momentary jitter or other undesirable effects to the TV screen, writing should be done only during the vertical retrace (before line 20).

Write to Control Registers

A write cycle consists of three bytes, with three acknowledge bits.

1) The first byte is always the write address for the MC44461 ($24).

2) The second byte defines the sub–address register, within the MC44461, to be updated; $00 through $0B.

3) The third byte is the data for that register.

The communication begins when a start sequence (data line taken low while the clock line is high) is initiated by the master (MCU) and detected by the MC44461, generating an internal reset. The first byte is then generated, and if the address is correct ($24), an acknowledge is generated by the MC44461, which tells the master to continue to send data. The second byte is then entered, followed by an acknowledge. The third byte is the operative data which is stored in the designated register, followed by the third acknowledge. Writing to multiple registers in a single write operation is permitted in the MC44461. The sub–address is auto–incremented while receiving n – data bytes + Ack, ending with the stop sequence. The sub–address of the 11 registers are at $00 through $0B.

Figure 3. I^{2}C Bus Interface and Decoder

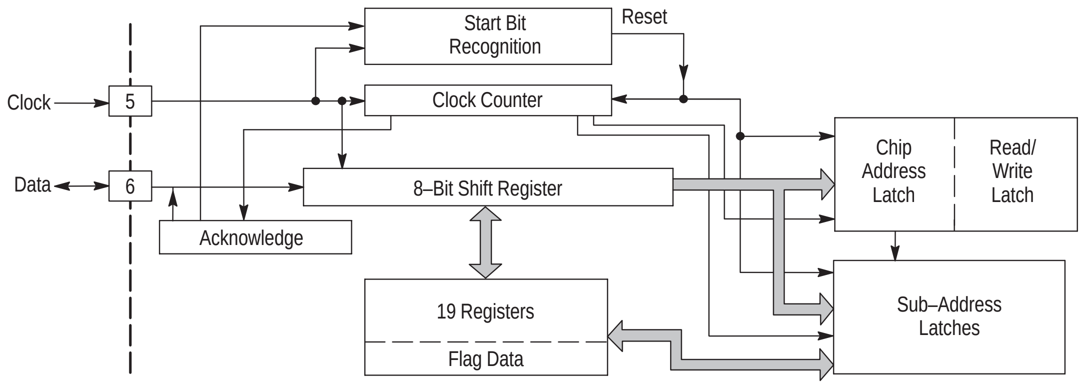
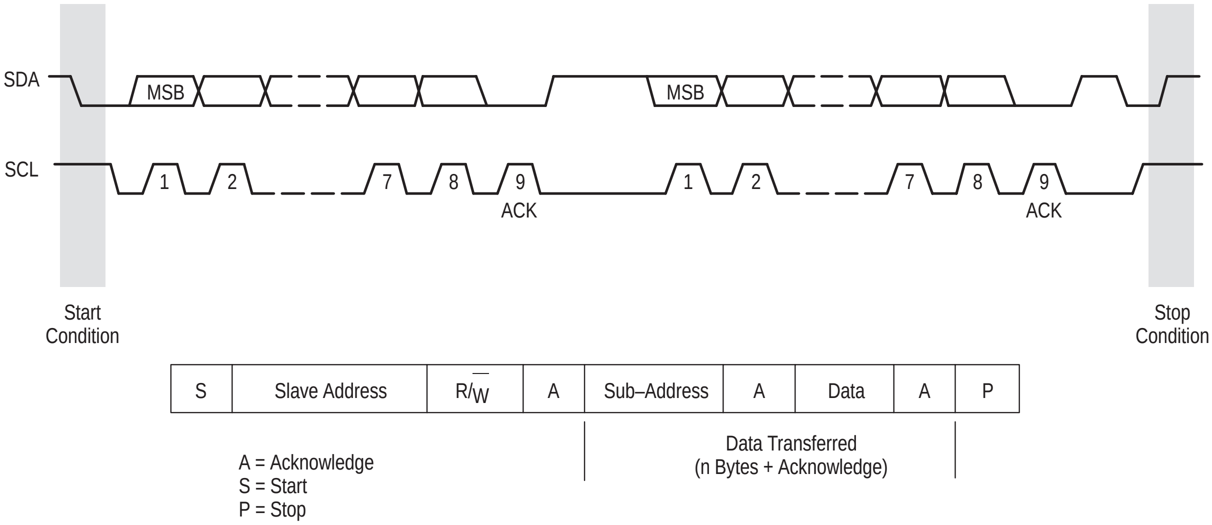


Figure 4. I^{2}C Data Transfer



I^{2}C REGISTER DESCRIPTIONS

Base write address = 24h

Base read address = 25h

Read Register

There are two active bits in the single read byte available from the MC44461 as follows:

Write Vertical Indicator (WVI0) – D7

When 0 indicates that the write operation specified by the last I^{2}C command has been completed.

PIP Sync Detect Bit (PSD0) – D1

When 0 indicates that the PIP video H pulses are present and the horizontal timebase oscillator is within acceptable limits.

Write Registers

Read Start Position/Write Start Position Registers

Sub–address = 00h

Write Raster Position Start Bits (WPS0–2) – D0–D2

Establishes the horizontal beginning of the PIP and its black level measurement gate. This beginning may be varied by approximately 3.0 µs. The position of this pulse may be observed through the Multi Test Pin 30 (See Test Mode Register Sub–address 03h).

Read Raster Position Bits (RPS0–3) – D4–D7

Establishes the clamp gate position for the black level reference for the main picture. This position may be varied by approximately 5.0 µs. The position of this pulse may be observed through the Multi Test Pin 30 (See Test Mode Register Sub–address 03h).

Pip Switch Delay/Vertical Filter Register

Sub–address = 01h

PIP Switch Delay Bits (PSD0–3) – D0–D3

Delays the start of PIP on time relative to the PIP picture. These bits are used to center the PIP border and PIP picture in the horizontal direction.

Vertical Filter Bit (VFON) – D4

When the filter is activated (VFON = 1) a three line weighted average is taken to provide the data stored in the field memory.

Border Color Register

Sub–address = 02h

Border Color Bits (BC0–2) – D0–D2

These Bits control the color of the border. Note that when using one of the saturated border colors it is possible to get objectionable dot crawl at the edge of the border in some TVs unless appropriate comb filtering is used in the TV circuitry.

BC (2:0)	Border Color
000	Black
001	White 70%
010	No Border (clear)
011	No Border (clear)
100	Blue
101	Green
110	Red
111	White

Test Mode/Main Vertical and Horizontal Polarity Register

Sub–address = 03h

Internal Test Mode Register (ITM0–2) – D0–D2

Sets the Multi Test Pin output to provide one of several internal signals for test and production alignment. Also controls the test memory address counter.

ITM (2:0)	Multi–Test I/O and Function
000	Input – Analog Test mode
001	Input – Digital Test mode
010	Output – Sync Detect
011	Output – PIP Switch
100	Output – PIP H Detect
101	Output – PIP V Detect
110	Output – PIP Clamp
111	Output – Main Clamp

Main vertical polarity select bit (MVP0) – D6

Selects polarity of active level of vertical reference input. 0 = positive going, 1 = negative going.

Main horizontal polarity select bit (MHP0) – D7

Selects polarity of active level of horizontal reference input. 0 = positive going, 1 = negative going.

PIP Freeze/PIP Size/Main and PIP Video Source Register

Sub–address = 04h

PIP Freeze Bit (STIL0) – D4

When set to one, the most recently received field is continuously displayed until the freeze bit is cleared.

PIP Size Bit (PSI90) – D5

Switches the PIP size between 1/16 main size (when 0) and 1/9 main size (when 1).

Main Video Source Select Bit (MSEL0) – D6

Selects which video input will be applied to the PIP switch as the main video out.

PIP Video Source Select Bit (PSEL0) – D7

Selects which video input will be applied to the video decoder to provide the PIP video.

MSEL/PSEL	Function
0	Video 1 Input to Main/ Video 1 Input to PIP
1	Video 2 Input to Main/ Video 2 Input to PIP

PIP On/PIP Blank Register

Sub–address = 05h

PIP On Bit (PON0) – D0

When on (1) turns the PIP on.

PIP Blanking Bit (PBL0) – D4

When on (1) sets the PIP to black. If the PIP is off, then it will be black if it is turned on. Overrides all other settings of the PIP control.

PIP X Position Register

Sub–address = 06h

X Position Bits (XPS0–5) – D0–D5

Moves the PIP start position from the left to the right edge of the display in 64 steps. There is protection circuitry to prevent the PIP from interfering with the main picture sync pulses.

PIP Y Position Register

Sub–address = 07h

Y Position Bits (YPS0–5) – D0–D5

Moves the PIP start position from the top to the bottom edge of the display in 64 steps. There is protection circuitry to prevent the PIP from interfering with the main picture sync pulses.

PIP Chroma Level Register

Sub–address = 08h

Chroma (C0–5) – D0–D5

The color of the PIP can be adjusted to suit viewer preference by setting the value stored in these bits. A total of 64 steps varies the color from no color to maximum. This control acts in conjunction with the auto phase control.

PIP Tint Level Register

Sub–address = 09h

Tint (T0–5) – D0–D5

An auto phase control compares the main color burst to the internally generated pseudo color burst so that the tints are matched. In addition to this, the tint of the PIP can be varied ±10° in a total of 64 steps by changing the value of these bits to suit viewer preference.

PIP Luma Delay Register

Sub–address = 0Ah

Y Delay (YDL0–2) – D0–D2

Since the Chroma passes through a bandpass filter and the color decoder, it is delayed with respect to the Luma signal. Therefore, to time match the Luma and Chroma these bits are set to a single value determined to be correct in the application.

Pip Fill/Test Register

Sub–address = 0Ch

PIP Fill Bits (PIPFILL0–1) – D0–D1

May be used to fill the PIP with one of three selectable solid colors

Test Register Bits (INTC0 and MACR0) – D6–D7

Used for production test only.

Function Control of the MC44461

The registers of the MC44461 may be programmed via the I^{2}C bus. At power up, the registers are in an undefined state. The Setup Value given in the Register Table represents a nominal start point. The setup will put a 1/9 size PIP, with white borders, in the lower right corner of the screen.

I^{2}C REGISTER TABLE

Sub–address	Setup Values	Data Bit							
		D7	D6	D5	D4	D3	D2	D1	D0
00h	45h	RPS3	RPS2	RPS1	RPS0	–	WPS2	WPS1	WPS0
01h	1Ah	–	–	–	VFON	PSD3	PSD2	PSD1	PSD0
02h	07h	–	–	–	–	–	BC2	BC1	BC0
03h	02h	MHP0	MVP0	–	–	–	ITM2	ITM1	ITM0
04h	20h	PSEL0	MSEL0	PSI90	STIL0	–	–	–	–
05h	01h	–	–	–	PBL0	–	–	–	PON0
06h	34h	–	–	XPS5	XPS4	XPS3	XPS2	XPS1	XPS0
07h	24h	–	–	YPS5	YPS4	YPS3	YPS2	YPS1	YPS0
08h	20h	–	–	C5	C4	C3	C2	C1	C0
09h	20h	–	–	T5	T4	T3	T2	T1	T0
0Ah	02h	–	–	–	–	–	YDL2	YDL1	YDL0
0Bh	–	–	–	–	–	–	–	–	–
0Ch	00h	–	–	–	–	–	–	–	–

CIRCUIT DESCRIPTION

The MC44461 Picture–in–Picture (PIP) controller is composed of an analog section, logic section and an 8192 x 8–bit DRAM array. A block diagram showing details of all of these sections is shown in the Representative Block Diagram.

The analog section includes an Input Switch, Sync Processor, Filters, PLLs, NTSC Decoder, ADC, DACs, NTSC Encoder and Output Switch. All necessary controls are provided by registers in the logic section. These registers are set by external control through the I^{2}C Bus.

In operation, the MC44461 overlays a single PIP on the main video in either a 1/9th or 1/16th size. In 1/9th, the PIP is 152 samples (114 Y, 19 V, 19 U) by 70 lines and occupies 8094 bytes of the 8192 byte DRAM. The 1/16 size is 112 samples (84 Y, 14 V, 14 U) by 52 lines and occupies 4452 bytes of the DRAM. An extra line of data is stored for each PIP size to allow for interlace disorder correction. The 6:1:1 samples are formatted by the logic section as follows in order to efficiently utilize memory:

Byte 1: Y0(5:0), V(1:0)

Byte 2: Y1(5:0), V(3:2)

Byte 3: Y2(5:0), V(5:4)

Byte 4: Y3(5:0), U(1:0)

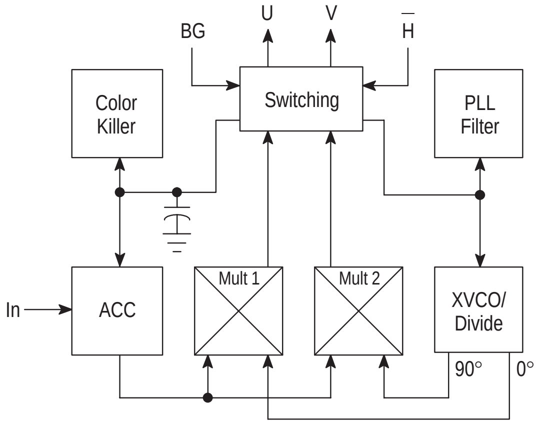
Byte 5: Y4(5:0), U(3:2)

Byte 6: Y5(5:0), U(5:4)

Refer to the block diagram. Both the video inputs are applied to an input switch which is controlled by the I^{2}C bus interface. Either of the inputs is applied to the PIP processing circuitry and either to the main video signal path of the output switch. The signal applied to the PIP processor also provides the vertical sync reference to the PIP processor.

The PIP output from the switch is applied to a 1.0 MHz cutoff low pass GmC biquad filter to extract the luminance signal and a similar bandpass filter to pass chroma to the decoder section. These filters are tracked to a master GmC cell using subcarrier as a reference. A single–ended transconductance stage with relatively large signal handling ability (>2.5 Vpp @ 4.5 V V_{CC}) is used to avoid potential noise problems.

Figure 5. NTSC Decoder



The NTSC Decoder (Figure 5) consists of two multipliers, a voltage controlled 4 X S/C crystal oscillator/divider, Automatic Color Control (ACC) block, Color Kill circuit and necessary switching. During Burst Gate time, the ACC block in the NTSC Decoder is calibrated with respect to burst magnitude by applying the output of multiplier 1 to the reference input of the ACC block. The result is U and V outputs which are 0.6 V ± 0.5 dB for burst amplitudes varying from –12 dB to 3.0 dB. The second multiplier serves as a phase detector during color burst to match the 90 degree output from the XVCO to the 180 degree color burst and feed a correction current to the PLL filter. The phase is correct when the two signals are 90 degrees out of phase.

During the H drive time, the output of the multipliers is fed to the YUV clamp, filtered to 200 KHz and input along with the Y signal to the multiplexer.

The YUV samples are fed through a multiplexer to a single six bit A/D converter. The A/D is a flash type architecture and is capable of digitizing at a 20 MHz sample rate. It is comprised of an internal bandgap source voltage reference, a 64 tap resistor ladder comparator array, a binary encoder and output latches. Once the multiplexer has switched, sufficient time is provided to allow the A/D converter to settle before the reading is latched. The encoder code is determined from the values of any comparators which are not metastable.

The multiplexer and A/D converter receive and convert the YUV data at a $4F_{SC}/3$ rate for a 1/9th size picture or F_{SC} for a 1/16th size picture. The samples are taken in the following way to simplify the control logic:

Y,V,Y,U,Y,V,Y,U

To provide a 6:1:1 format, one of three U and V samples is saved to memory giving a luminance sample rate of $2F_{SC}/3$ for a 1/9th picture and $F_{SC}/2$ for a 1/16 picture. In the vertical direction, one line of every 3 (1/9th picture) or 4 (1/16th picture) are saved. In order to avoid objectionable artifacts, a piece–wise vertical filter is used to take a weighted average on the luminance samples. For three lines (1/9th size) the weight is 1/4 + 1/2 + 1/4 and for four lines (1/16 size) it is 1/4 + 1/4 + 1/4 + 1/4. This filter also delays the luma samples correcting for the longer chroma signal path through the decoder.

Finally the logic incorporates a field generator to determine the current field in order to correct interlace disorders arising from a single field memory.

A separate process runs in the logic section to create the PIP window on the main picture. Control signals are generated and sent to the memory controller to read data from the field memory. Data from the eight bit memory are then de–multiplexed into a six bit YUV format, borders are added, blanking is generated for the video clamps and sent to the Y, U and V DACs. Since the PIP display is based on a data clock, it is important to minimize the main display clock skew on a line by line basis. Skew is minimized in the MC44461 by reclocking the display timebase to the nearest rising or falling edge of a $16F_{SC}$ clock. This produces a maximum line to line skew of approximately 8.0 ns which is not perceptible to the viewer. The PIP write logic also incorporates a field generator for use by the memory controller for interlace disorder correction. Interlace disorder can occur when the line order of the two fields of the PIP image is swapped due to a mismatch with the main picture field or due to an incomplete field being displayed from memory. The main and PIP field generators, along with monitoring, when the PIP read address passes the PIP write address, allows the read address to the memory to be modified to correct for interlace disorder.

The read logic can provide various border colors: black, 75% white (light gray), 50% white (medium gray), red, green, blue or transparent (no border). In a system without an adaptive comb filter, borders which contain no chroma give the best results. Also built into the read logic is a PIP fill mode which allows the PIP window to be filled with either a solid green, blue or red color as an aid in aligning the PIP analog color circuitry.

Because the DAC output video will be referenced during back porch time, the read processor zeroes the luminance value and sets the bipolar U and V values to mid–range during periods outside the PIP window to ensure clamping at correct levels. Since the PIP window is positioned relative to the main picture's vertical and horizontal sync, a safety feature turns off the window if the window encroaches upon the sync period, thus preventing erroneous clamping.

The Y, U and V DACs are all three of the same design. A binary weighted current source is used, split into two, three bit levels. In the three most significant bits, the current sources are cascaded to improve the matching to the three least significant current sources. Analog transmission gates, switched by the bi–phase outputs of the data latches, feed the binary currents to the single ended current mirror. The output current is subsequently clamped and filtered for processing buy the NTSC Encoder.

The outputs of the U and V DACS are buffered and burst flag pulses added to both signals. The U burst flag is fixed to generate a –180° color burst at the modulator output. The V burst flag is variable under the control of an internal register set through the I^2C bus to provide a variable tint. Saturation is controlled by varying a register which sets the reference voltage to the U and V DACs. This is also under I^2C bus control. By oversampling the U and V DACs, it was possible to use identical post–DAC filtering for Y, U and V, thereby reducing the delay inequalities between Y and UV and also simplifying the design. After filtering, the U and V signals are clamped to an internal reference voltage during horizontal blanking periods and fed to the U and V modulators. In the NTSC Decoder, the Y, U and V signals were scaled to use the entire A/D range. Gain through the NTSC Encoder is set to properly match these amplitudes.

The phase of the re–encoded chrominance must match that of the incoming main video signal at the input to the PIP switch, so a separate first order PLL is placed within the loop of the main video signal burst PLL. The first order PLL compares the phase of the main burst with that of the encoded burst and moves the oscillator phase so that they match. A special phase shift circuit allowing a continuous range of 180° was developed to do this.

The amplitude of the re–encoded chrominance signal must also match that of the main video signal. To do this, a synchronous amplitude comparator looks at both burst signals and adjusts the chrominance amplitude in the modulator section of the NTSC encoder. The Y signal from the YDAC is compared to the main video signal at black level during back porch time and clamped to this same black level voltage. The PIP chrominance and luminance are then added together and fed to the PIP output switch through a buffered output.

MOTOROLA

MC44462

Product Preview

Y-C Picture-in-Picture (PIP) Controller

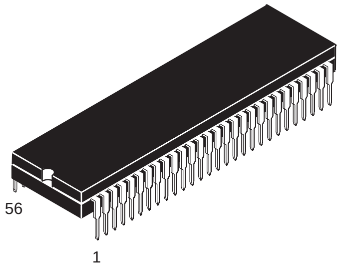
The MC44462 Y–C PIP controller is a low cost member of a family of high performance PIP controllers and video signal processors for television. It is a follow–up to the MC44461 PIP and has a modified input selection to allow higher performance in TV systems which have S–Video inputs on the back panel. The S–Video input is separate luma (luminance) and chroma components. It is NTSC compatible and contains all the analog signal processing, control logic and memory necessary to provide for the overlay of a small picture from a second non synchronized source onto the main picture of a television. All control and setup of the MC44462 is via a standard two pin I^2C bus interface. The device is fabricated using BICMOS technology. It is available in a 56–pin shrink dip (SDIP) package.

The main features of the MC44462 are:

- Switchable PIP Composite Video Signals – Video 1 and Video 2
- S–Video Output Allows High Performance in TV
- Two PIP Sizes; 1/16 and 1/9 Screen Area
- Freeze Field Feature
- Variable PIP Position in 64–X by 64–Y Steps
- PIP Border with Programmable Color
- Programmable PIP Tint and Saturation Control
- Automatic Main to PIP Contrast Balance
- Vertical Filter
- Integrated 64 k Bit DRAM Memory Resulting in Minimal RFI
- Minimal RFI Allows Simple Low Cost Application into TV
- I^2C Bus Control – No External Variable Adjustments Needed
- Operates from a Single 5.0 V Supply
- Economical 56–Pin Shrink DIP Package

Y–C PICTURE–IN–PICTURE (PIP) CONTROLLER

SEMICONDUCTOR TECHNICAL DATA

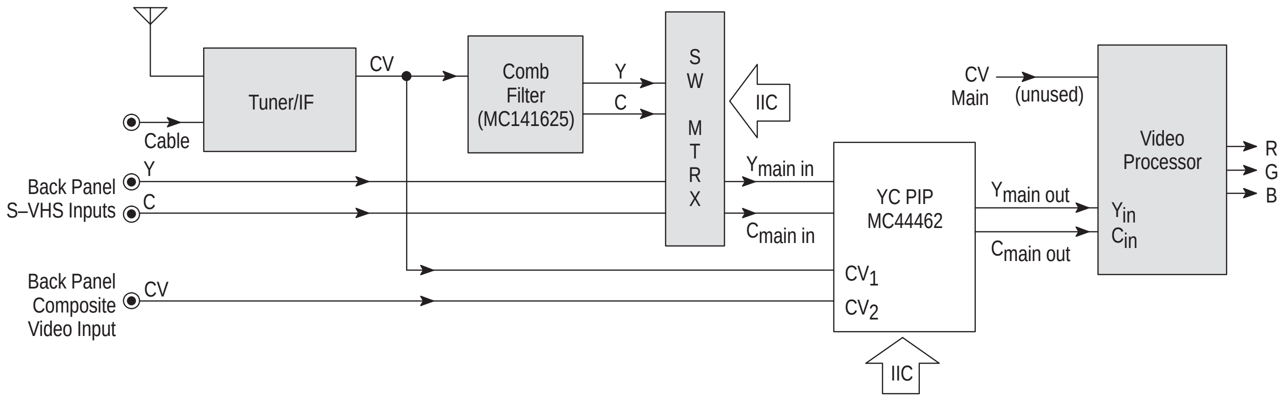


B SUFFIX
PLASTIC PACKAGE
CASE 859
(SDIP)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC44462B	T_J = –65° to +150°C	SDIP

YC–PIP System Diagram



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{DD}	–0.5 to +6.0	V
Power Supply Voltage	V_{CC}	–0.5 to +6.0	V
Input Voltage Range	V_{IR}	–0.5, V_{DD} + 0.5	V
Output Current	I_O	160	mA
Power Dissipation			
Maximum Power Dissipation @ 70°C	P_D	1.3	W
Thermal Resistance, Junction–to–Air	$R_{\theta JA}$	59	°C/W
Junction Temperature (Storage and Operating)	T_J	–65 to +150	°C

NOTE: ESD data available upon request.

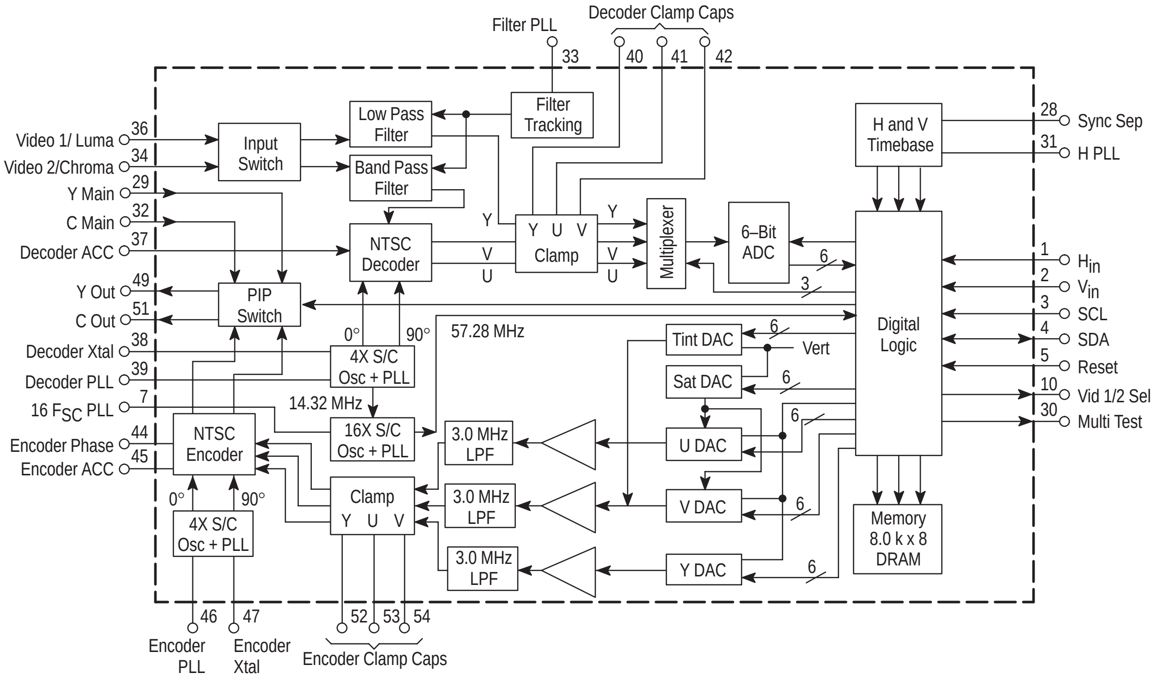
ELECTRICAL CHARACTERISTICS (V_{CC} = V_{DD} = 5.0 V, T_A = 25°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
POWER SUPPLY					
Total Supply (Pins 8, 15, 43 and 50)	Total I_{Supply}	–	100	160	mA
VIDEO					
Composite Video Input (Pin 34 or 36)	CVi	–	1.0	–	Vpp
Luma Output (Pin 49, Unterminated)	–	–	2.0	–	Vpp
Video Output DC Level (Sync Tip)	–	–	1.0	–	Vdc
Video Gain	–	–	6.0	–	dB
Video Frequency Response (Main Video to –1.0 dB)	–	–	10	–	MHz
Color Bar Accuracy	–	–	±4.0	–	deg
Video Crosstalk (@ 75% Color Bars)	–				dB
Main to PIP		–	55	–	
PIP to Main		–	55	–	
Output Impedance	–	–	5.0	–	Ω
HORIZONTAL TIMEBASE					
Free Run HPLL Frequency (Pin 16)	–	–	15734	–	Hz
HPLL Pull–In Range	–	–	±400	–	Hz
HPLL Jitter	–	–	±4.0	–	ns
Burst Gate Timing (from Trailing Edge Hsync, Pin 24)	–	–	1.0	–	µs
Burst Gate Width	–	–	4.0	–	µs
VERTICAL TIMEBASE					
Vertical Countdown Window	–	–	232 – 296	–	H lines
Vertical Sync Integration Time	–	–	31	–	µs
ANALOG TO DIGITAL CONVERTER					
Resolution	–	–	6	–	Bits
Integral Non–Linearity	–	–	±1	–	LSB
Differential Non–Linearity	–	–	+2/–1	–	LSB
ADC – Y Frequency Response @ –5.0 dB	–	–	1.0	–	MHz
ADC – U, V Frequency Response @ –5.0 dB	–	–	200	–	kHz
Sample Clock Frequency (4/3 F_{SC})	–	–	4.773	–	MHz

ELECTRICAL CHARACTERISTICS (continued) (V_{CC} = V_{DD} = 5.0 V, T_A = 25°C, unless otherwise noted.)

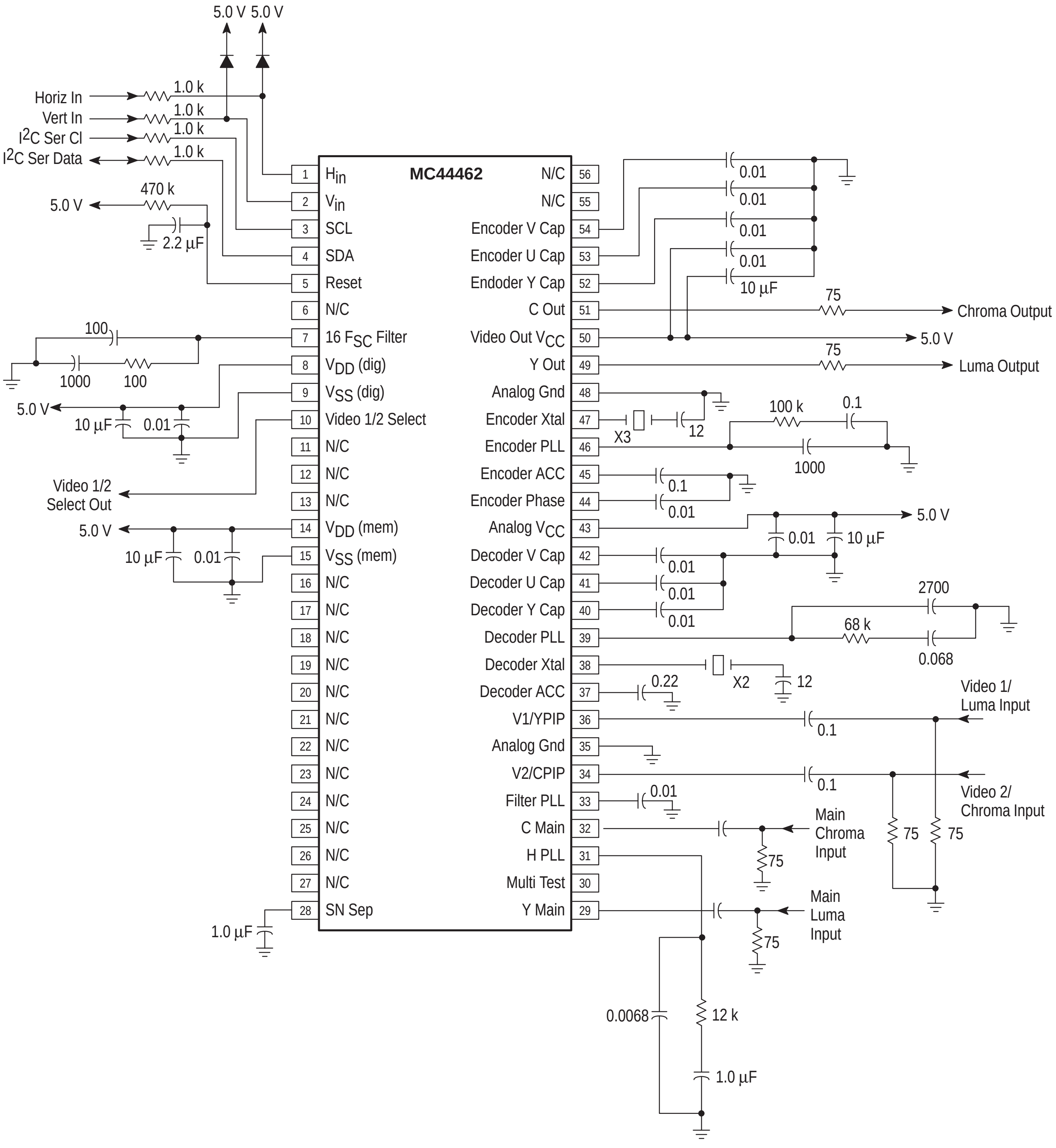
Characteristic	Symbol	Min	Typ	Max	Unit
DIGITAL TO ANALOG CONVERTER					
Resolution	–	–	–	6	Bits
Integral Non–Linearity	–	–	±1	–	LSB
Differential Non–Linearity	–	–	+2/–1	–	LSB
Tint DAC Control Range (in 64 Steps)	–	–	±10	–	Deg
Saturation DAC Control Range (in 64 steps)	–	–	±6.0	–	dB
NTSC DECODER					
Color Kill Threshold	–	–	–24/–16	–	dB
Threshold Hysteresis	–	–	±1.0	–	dB
ACC (Chroma Amplitude Change, +3.0 dB to –12 dB)	–	–	±0.5	–	dB
PIP CHARACTERISTICS					
PIP Size	–				
1/9 Screen Horizontal		–	114	–	pels
1/9 Screen Vertical		–	71	–	lines
1/16 Screen Horizontal		–	84	–	pels
1/16 Screen Vertical		–	53	–	lines
Border Size Horizontal	–	–	3	–	pels
Border Size Vertical	–	–	2	–	lines
Output PEL Clock (4 F_{SC})	–	–	14.318	–	MHz
Position Control Range Horizontal (% of Main Picture), 64 Steps	–	–	100	–	%
Position Control Range Vertical (% of Main Picture), 64 Steps	–	–	100	–	%

Figure 1. Representative Block Diagram



This device contains approximately 500,000 active transistors.

Figure 2. Application Circuit



X2 – 14.31818 MHz – Fox 143–20 or equivalent
X3 – 14.31818 MHz – Fox 143–20 or equivalent

NOTE: For proper noise isolation, Power Supply Pins 8, 14, 43 and 50 should be bypassed by both high and low frequency capacitors. As a guideline, a 10 µF in parallel with a 0.1 µF at each supply pin is recommended.

I^{2}C REGISTER DESCRIPTIONS

Base write address = 24h

Base read address = 25h

Read Register

There are two active bits in the single read byte available from the MC44462 as follows:

Write Vertical Indicator (WVI0) – D7

When 0 indicates that the write operation specified by the last I^{2}C command has been completed.

PIP Sync Detect Bit (PSD0) – D1

When 0 indicates that the PIP video H pulses are present and the horizontal timebase oscillator is within acceptable limits.

Write Registers

Read Start Position/Write Start Position Registers
Sub–address = 00h

Write Raster Position Start Bits (WPS0–2) – D0–D2

Establishes the horizontal beginning of the PIP and its black level measurement gate. This beginning may be varied by approximately 3.0 µs. The position of this pulse may be observed through the Multi Test Pin 30 (See Test Mode Register Sub–address 03h).

Read Raster Position Bits (RPS0–3) – D4–D7

Establishes the clamp gate position for the black level reference for the main picture. This position may be varied by approximately 5.0 µs. The position of this pulse may be observed through the Multi Test Pin 30 (See Test Mode Register Sub–address 03h).

Pip Switch Delay/Vertical Filter Register
Sub–address = 01h

PIP Switch Delay Bits (PSD0–3) – D0–D3

Delays the start of PIP on time relative to the PIP picture. These bits are used to center the PIP border and PIP picture in the horizontal direction.

Vertical Filter Bit (VFON) – D4

When the filter is activated (VFON = 1) a three line weighted average is taken to provide the data stored in the field memory.

Border Color Register
Sub–address = 02h

Border Color Bits (BC0–2) – D0–D2

These Bits control the color of the border. Note that when using one of the saturated border colors it is possible to get objectionable dot crawl at the edge of the border in some TVs unless appropriate comb filtering is used in the TV circuitry.

BC (2:0)	Border Color
000	Black
001	White 70%
010	No Border (clear)
011	No Border (clear)
100	Blue
101	Green
110	Red
111	White

Test Mode/Main Vertical and Horizontal Polarity Register
Sub–address = 03h

Internal Test Mode Register (ITM0–2) – D0–D2

Sets the Multi Test Pin output to provide one of several internal signals for test and production alignment. Also controls the test memory address counter.

ITM (2:0)	Multi–Test I/O and Function
000	Input – Analog Test mode
001	Input – Digital Test mode
010	Output – Sync Detect
011	Output – PIP Switch
100	Output – PIP H Detect
101	Output – PIP V Detect
110	Output – PIP Clamp
111	Output – Main Clamp

Main vertical polarity select bit (MVP0) – D6

Selects polarity of active level of vertical reference input. 0 = positive going, 1 = negative going.

Main horizontal polarity select bit (MHP0) – D7

Selects polarity of active level of horizontal reference input. 0 = positive going, 1 = negative going.

PIP Freeze/PIP Size/Main and PIP Video Source Register
Sub–address = 04h

PIP Freeze Bit (STIL0) – D4

When set to one, the most recently received field is continuously displayed until the freeze bit is cleared.

PIP Size Bit (PSI90) – D5

Switches the PIP size between 1/16 main size (when 0) and 1/9 main size (when 1).

Video Type Select Bit (YCPSEL) – D6

Selects which video type will be applied to the PIP input.

PIP Video Source Select Bit (PSEL0) – D7

Selects which composite video input will be applied to the video decoder to provide the PIP video in CV mode.

PSEL	YCPSEL	Function
0	1	YC Input to PIP
0 1	0	CV$_1$ Input to PIP CV$_2$ Input to PIP

PIP On/PIP Blank Register
Sub–address = 05h

PIP On Bit (PON0) – D0

When on (1) turns the PIP on.

PIP Blanking Bit (PBL0) – D4

When on (1) sets the PIP to black. If the PIP is off, then it will be black if it is turned on. Overrides all other settings of the PIP control.

PIP X Position Register
Sub–address = 06h

X Position Bits (XPS0–5) – D0–D5

Moves the PIP start position from the left to the right edge of the display in 64 steps. There is protection circuitry to prevent the PIP from interfering with the main picture sync pulses.

PIP Y Position Register

Sub–address = 07h

Y Position Bits (YPS0–5) – D0–D5

Moves the PIP start position from the top to the bottom edge of the display in 64 steps. There is protection circuitry to prevent the PIP from interfering with the main picture sync pulses.

PIP Chroma Level Register

Sub–address = 08h

Chroma (C0–5) – D0–D5

The color of the PIP can be adjusted to suit viewer preference by setting the value stored in these bits. A total of 64 steps varies the color from no color to maximum. This control acts in conjunction with the auto phase control.

PIP Tint Level Register

Sub–address = 09h

Tint (T0–5) – D0–D5

An auto phase control compares the main color burst to the internally generated pseudo color burst so that the tints are matched. In addition to this, the tint of the PIP can be varied ±10° in a total of 64 steps by changing the value of these bits to suit viewer preference.

PIP Luma Delay Register

Sub–address = 0Ah

Y Delay (YDL0–2) – D0–D2

Since the Chroma passes through a bandpass filter and the color decoder, it is delayed with respect to the Luma signal. Therefore, to time match the Luma and Chroma these bits are set to a single value determined to be correct in the application.

Pip Fill/Test Register

Sub–address = 0Ch

PIP Fill Bits (PIPFILL0–1) – D0–D1

May be used to fill the PIP with one of three selectable solid colors

Test Register Bits (INTC0 and MACR0) – D6–D7

Used for production test only.

I^{2}C REGISTER TABLE

Sub–address	Data Bit							
	D7	D6	D5	D4	D3	D2	D1	D0
00	RPS3	RPS2	RPS1	RPS0	–	WPS2	WPS1	WPS0
01	–	–	–	VFON	PSD3	PSD2	PSD1	PSD0
02	–	–	–	–	–	BC2	BC1	BC0
03	MHP0	MVP0	–	–	–	ITM2	ITM1	ITM0
04	PSEL0	YCPSEL	PSI90	STIL0	–	–	–	–
05	–	–	–	PBL0	–	–	–	PON0
06	–	–	XPS5	XPS4	XPS3	XPS2	XPS1	XPS0
07	–	–	YPS5	YPS4	YPS3	YPS2	YPS1	YPS0
08	–	–	C5	C4	C3	C2	C1	C0
09	–	–	T5	T4	T3	T2	T1	T0
0A	–	–	–	–	–	YDL2	YDL1	YDL0
0B	–	–	–	–	–	–	–	–
0C	–	–	–	–	–	–	–	–

MOTOROLA

Product Preview

Picture-in-Picture (PIP) Controller

The MC44463 Picture–In–Picture (PIP) controller is a low cost member of a family of high performance PIP controllers and video processors for television. It is a follow–up to the MC44461 PIP, in which two additional modes of operation have been added. A replay mode is provided, which captures several seconds of the main picture for replay in four different speeds. The capture time is programmable in four resolutions (ratio of captured fields to total fields), which trade the number of fields captured to the length of replay time. The second additional mode provides for multiple small picture overlays from a second non–synchronized source. The number of PIP images is 3 for the 1/9 screen area and 4 for the 1/16 screen area. Like the MC44461 this is NTSC compatible, I^2C bus controlled and available in the 56–pin shrink dip (SDIP) package.

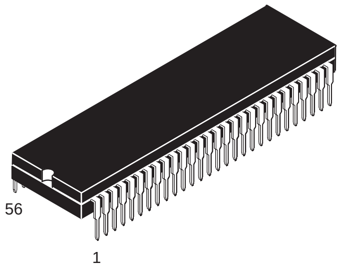
The main features of the MC44463 are:

- Three PIP Functional Modes: Standard Single Active PIP Mode, Up to 8 Seconds of Capture and Replay Mode, and a 3 or 4 Multiple PIP Mode – Vertical Stacked with 1 Active at Any One Time
- 4 Capture Resolutions – 1 out of 10, 1:8, 1:6, 1:4. 4 Playback Speeds = 1 Times Acquire Speed; 1/2; 1/4; 1/8
- Full 2 Frame Store for the Single PIP Removes the Rolling Store/Playback Memory Interference – “Joint Line”
- External Memory for Replay and Multiple Modes: 4 Meg and 16 Meg
- Two NTSC CVBS Inputs – Switchable Main and PIP Video Signals
- Single NTSC CVBS Output Allows Simple TV Chassis Integration
- Two PIP Sizes; 1/16 and 1/9 Screen Area – Freeze Field Feature
- Variable PIP Position in 64–X by 64–Y Steps
- PIP Border with Programmable Color
- Programmable PIP Tint and Saturation Control
- Automatic Main to PIP Contrast Balance
- Vertical Filter
- I^2C Bus Control – No External Variable Adjustments Needed
- Operates from a Single 5.0 V Supply
- Economical 56–Pin Shrink DIP Package

MC44463

REPLAY AND MULTIPLE PICTURE–IN–PICTURE (PIP) CONTROLLER

SEMICONDUCTOR
TECHNICAL DATA

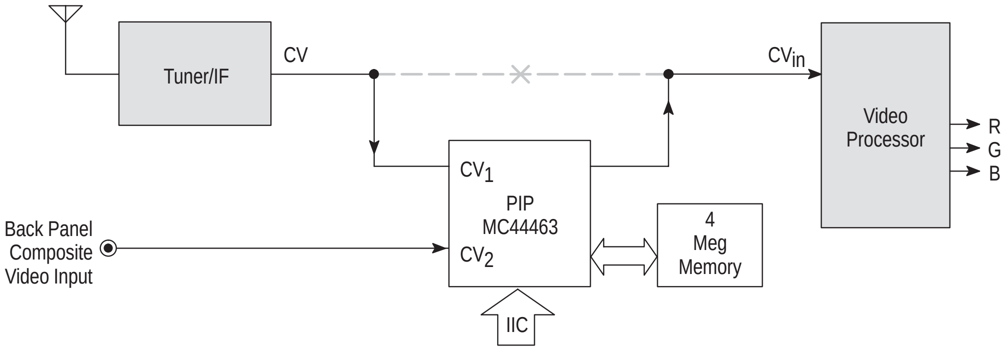


B SUFFIX
PLASTIC PACKAGE
CASE 859
(SDIP)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC44463B	T_J = –65° to +150°C	SDIP

Composite Video Simplified System Diagram



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{DD}	–0.5 to +6.0	V
Power Supply Voltage	V_{CC}	–0.5 to +6.0	V
Input Voltage Range	V_{IR}	–0.5, V_{DD} + 0.5	V
Output Current	I_O	160	mA
Power Dissipation			
Maximum Power Dissipation @ 70°C	P_D	1.3	W
Thermal Resistance, Junction–to–Air	$R_{\theta JA}$	59	°C/W
Junction Temperature (Storage and Operating)	T_J	–65 to +150	°C

NOTE: ESD data available upon request.

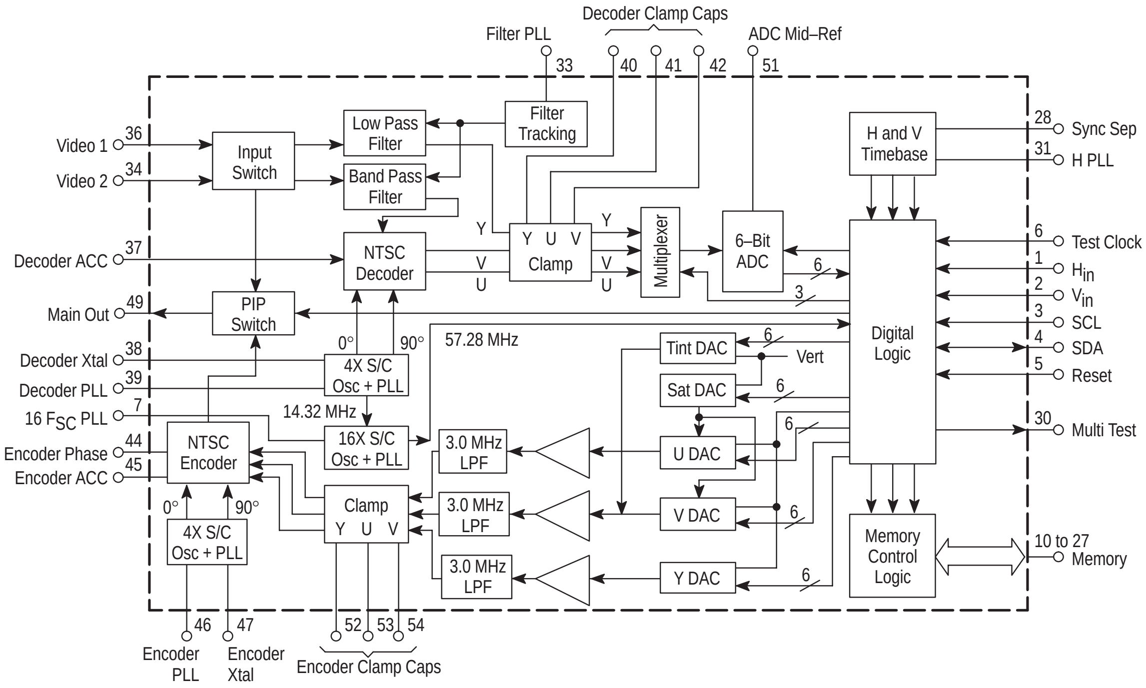
ELECTRICAL CHARACTERISTICS (V_{CC} = V_{DD} = 5.0 V, T_A = 25°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
POWER SUPPLY					
Total Supply (Pins 8, 15, 43 and 50)	Total I_{Supply}	–	110	160	mA
VIDEO					
Composite Video Input (Pin 34 or 36)	CVi	–	1.0	–	Vpp
Composite Video Output (Pin 49, Unterminated)	–	–	2.0	–	Vpp
Video Output DC Level (Sync Tip)	–	–	1.0	–	Vdc
Video Gain	–	–	6.0	–	dB
Video Frequency Response (Main Video to –1.0 dB)	–	–	10	–	MHz
Color Bar Accuracy	–	–	±4.0	–	deg
Video Crosstalk (@ 75% Color Bars)	–				dB
Main to PIP		–	55	–	
PIP to Main		–	55	–	
Output Impedance	–	–	5.0	–	Ω
HORIZONTAL TIMEBASE					
Free Run HPLL Frequency (Pin 16)	–	–	15734	–	Hz
HPLL Pull–In Range	–	–	±400	–	Hz
HPLL Jitter	–	–	±4.0	–	ns
Burst Gate Timing (from Trailing Edge Hsync, Pin 24)	–	–	1.0	–	µs
Burst Gate Width	–	–	4.0	–	µs
VERTICAL TIMEBASE					
Vertical Countdown Window	–	–	232/296	–	H lines
Vertical Sync Integration Time	–	–	31	–	µs
ANALOG TO DIGITAL CONVERTER					
Resolution	–	–	–	6	Bits
Integral Non–Linearity	–	–	±1	–	LSB
Differential Non–Linearity	–	–	+2/–1	–	LSB
ADC – Y Frequency Response @ –5.0 dB	–	–	1.0	–	MHz
ADC – U, V Frequency Response @ –5.0 dB	–	–	200	–	kHz
Sample Clock Frequency (4/3 F_{SC})	–	–	4.773	–	MHz

ELECTRICAL CHARACTERISTICS (continued) (V_{CC} = V_{DD} = 5.0 V, T_A = 25°C, unless otherwise noted.)

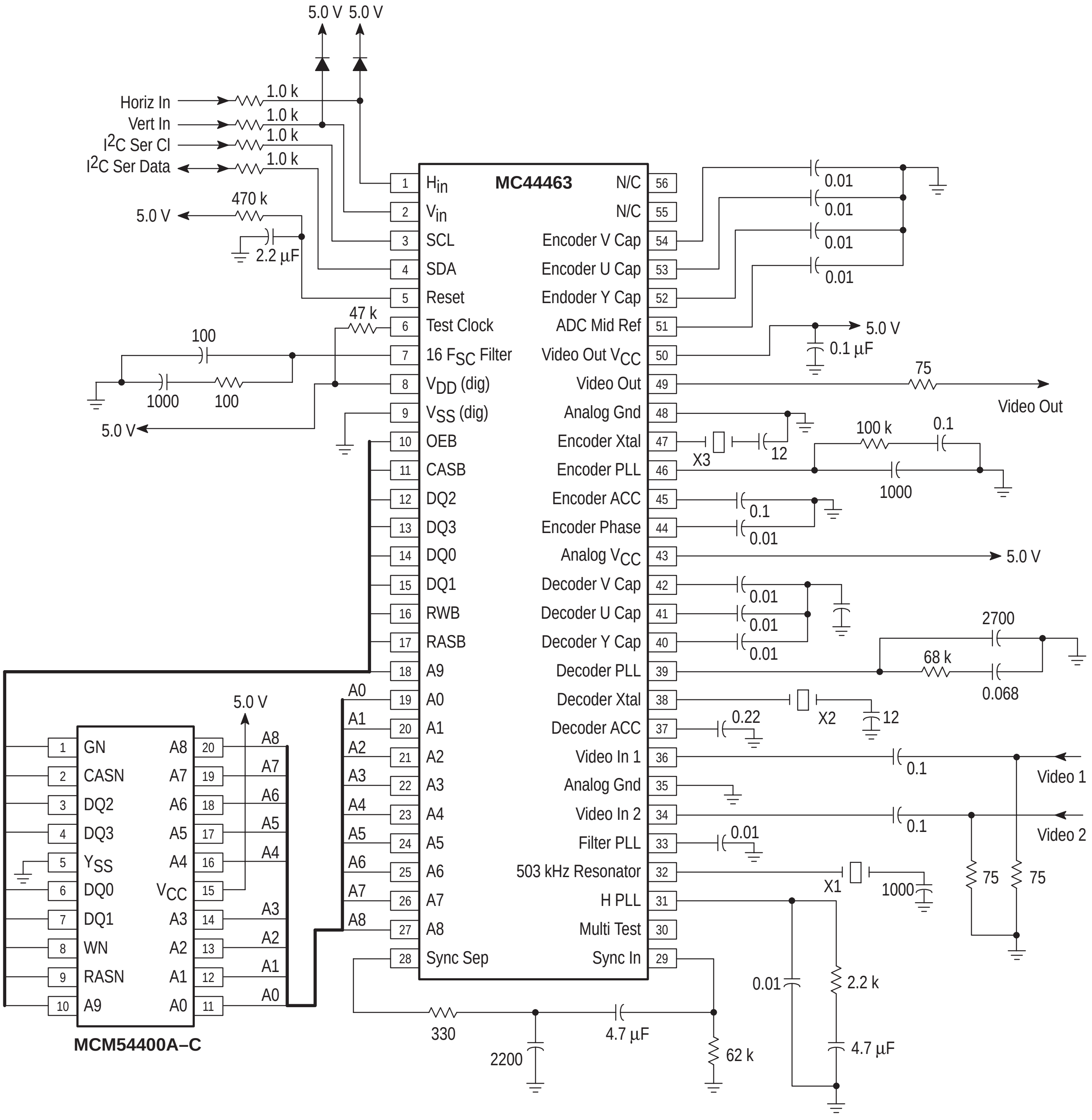
Characteristic	Symbol	Min	Typ	Max	Unit
DIGITAL TO ANALOG CONVERTER					
Resolution	–	–	–	6	Bits
Integral Non–Linearity	–	–	±1	–	LSB
Differential Non–Linearity	–	–	+2/–1	–	LSB
Tint DAC Control Range (in 64 Steps)	–	–	±10	–	Deg
Saturation DAC Control Range (in 64 steps)	–	–	±6.0	–	dB
NTSC DECODER					
Color Kill Threshold	–	–	–24/–16	–	dB
Threshold Hysteresis	–	–	±1.0	–	dB
ACC (Chroma Amplitude Change, +3.0 dB to –12 dB)	–	–	±5.0	–	dB
PIP CHARACTERISTICS					
PIP Size 1/9 Screen Horizontal 1/9 Screen Vertical 1/16 Screen Horizontal 1/16 Screen Vertical	–	 – – – –	 114 71 84 53	 – – – –	 pels lines pels lines
Border Size Horizontal	–	–	3	–	pels
Border Size Vertical	–	–	2	–	lines
Output PEL Clock (4 F_{SC})	–	–	14.318	–	MHz
Position Control Range Horizontal (% of Main Picture), 64 Steps	–	–	100	–	%
Position Control Range Vertical (% of Main Picture), 64 Steps	–	–	100	–	%

Figure 1. Representative Block Diagram



This device contains approximately 300,000 active transistors.

Figure 2. Application Circuit



X1 – 503 kHz – Murata Erie CSB503F2 or equivalent
X2 – 14.31818 MHz – Fox 143–20 or equivalent
X3 – 14.31818 MHz – Fox 143–20 or equivalent

I²C REGISTER DESCRIPTIONS

Base write address = 26h

Base read address = 27h

Read Register

There are two active bits in the single read byte available from the MC44463 as follows:

Write Vertical Indicator (WVI0) – D7

When 0 indicates that the write operation specified by the last I²C command has been completed.

PIP Sync Detect Bit (PSD0) – D1

When 0 indicates that the PIP video H pulses are present and the horizontal timebase oscillator is within acceptable limits.

Write Registers

Read Start Position/Write Start Position Registers

Sub–address = 00h

Write Raster Position Start Bits (WPS0–2) – D0–D2

Establishes the horizontal beginning of the PIP and its black level measurement gate. This beginning may be varied by approximately 3.0 µs. The position of this pulse may be observed through the Multi Test Pin 30 (See Test Mode Register Sub–address 03h).

Read Raster Position Bits (RPS0–3) – D4–D7

Establishes the clamp gate position for the black level reference for the main picture. This position may be varied by approximately 5.0 µs. The position of this pulse may be observed through the Multi Test Pin 30 (See Test Mode Register Sub–address 03h).

Pip Switch Delay/Vertical Filter Register

Sub–address = 01h

PIP Switch Delay Bits (PSD0–3) – D0–D3

Delays the start of PIP on time relative to the PIP picture. These bits are used to center the PIP border and PIP picture in the horizontal direction.

Vertical Filter Bit (VFON) – D4

When the filter is activated (VFON = 1) a three line weighted average is taken to provide the data stored in the field memory.

Border Color Register

Sub–address = 02h

Border Color Bits (BC0–2) – D0–D2

These Bits control the color of the border. Note that when using one of the saturated border colors it is possible to get objectionable dot crawl at the edge of the border in some TVs unless appropriate comb filtering is used in the TV circuitry.

BC (2:0)	Border Color
000	Black
001	White 70%
010	No Border (clear)
011	No Border (clear)
100	Blue
101	Green
110	Red
111	White

Test Mode/Main Vertical and Horizontal Polarity Register

Sub–address = 03h

Internal Test Mode Register (ITM0–2) – D0–D2

Sets the Multi Test Pin output to provide one of several internal signals for test and production alignment. Also controls the test memory address counter.

ITM (2:0)	Multi–Test I/O and Function
000	Input – Analog Test mode
001	Input – Digital Test mode
010	Output – Sync Detect
011	Output – PIP Switch
100	Output – PIP H Detect
101	Output – PIP V Detect
110	Output – PIP Clamp
111	Output – Main Clamp

Main vertical polarity select bit (MVP0) – D6

Selects polarity of active level of vertical reference input. 0 = positive going, 1 = negative going.

Main horizontal polarity select bit (MHP0) – D7

Selects polarity of active level of horizontal reference input. 0 = positive going, 1 = negative going.

PIP Freeze/PIP Size/Main and PIP Video Source Register

Sub–address = 04h

LIVE PIP Select Bits (LIVE_P0–1) – D0–D1

Selects which of the mutliple PIP pictures is the active “live” one.

LIVE_P (1:0)	1/16 Size	1/9 Size
00	Top = LIVE	Top = LIVE
01	2nd from Top = LIVE	2nd from Top = LIVE
10	3rd from Top = LIVE	3rd from Top = LIVE
11	4th from Top = LIVE	3rd from Top = LIVE

PIP Freeze Bit (STIL0) – D4

When set to one, the most recently received field is continuously displayed until the freeze bit is cleared.

PIP Size Bit (PSI90) – D5

Switches the PIP size between 1/16 main size (when 0) and 1/9 main size (when 1).

Main Video Source Select Bit (MSEL0) – D6

Selects which video input will be applied to the PIP switch as the main video out.

PIP Video Source Select Bit (PSEL0) – D7

Selects which video input will be applied to the video decoder to provide the PIP video.

MSEL/PSEL	Function
0	Video 1 Input to Main/ Video 1 Input to PIP
1	Video 2 Input to Main/ Video 2 Input to PIP

PIP On/PIP Blank Register

Sub–address = 05h

PIP On Bits (PON0–3) – D4–D3

When on (1) turns the corresponding PIP display on.

PON (3:0)	1/16 Size	1/9 Size
0000	No PIP	No PIP
0001	Top = On	Top = On
0010	2nd from Top = On	2nd from Top = On
0100	3rd from Top = On	3rd from Top = On
1000	4th from Top = On	3rd from Top = On

PIP Blanking Bits (PBL0–3) – D4–D7

When on (1) sets the corresponding PIP to black. If the individual PIP is off, then it will be black when it is turned on.

PBL (7:4)	Function
0000	PIP Picture Normal
0001	Top = Blanked (Set to Black)
0010	2nd from Top = Blanked (Set to Black)
0100	3rd from Top = Blanked (Set to Black)
1000	4th from Top = Blanked (Set to Black)

PIP X Position Register

Sub–address = 06h

X Position Bits (XPS0–5) – D0–D5

Moves the PIP start position from the left to the right edge of the display in 64 steps. There is protection circuitry to prevent the PIP from interfering with the main picture sync pulses.

PIP Y Position Register

Sub–address = 07h

Y Position Bits (YPS0–5) – D0–D5

Moves the PIP start position from the top to the bottom edge of the display in 64 steps. There is protection circuitry to prevent the PIP from interfering with the main picture sync pulses.

PIP Chroma Level Register

Sub–address = 08h

Chroma (C0–5) – D0–D5

The color of the PIP can be adjusted to suit viewer preference by setting the value stored in these bits. A total of 64 steps varies the color from no color to maximum. This control acts in conjunction with the auto phase control.

PIP Tint Level Register

Sub–address = 09h

Tint (T0–5) – D0–D5

An auto phase control compares the main color burst to the internally generated pseudo color burst so that the tints are matched. In addition to this, the tint of the PIP can be varied ±10° in a total of 64 steps by changing the value of these bits to suit viewer preference.

PIP Luma Delay Register

Sub–address = 0Ah

Y Delay (YDL0–2) – D0–D2

Since the Chroma passes through a bandpass filter and the color decoder, it is delayed with respect to the Luma signal. Therefore, to time match the Luma and Chroma these bits are set to a single value determined to be correct in the application.

PIP Acquire/Playback Register

Sub–address = 0Bh

PIP Acquire Speed Bits (ACQ_SP0–1) – D0–D1

These select the speed of the video acquisition. This is only active when RE_AQ = 1.

ACQ_SP (1:0)	Function
00	Acquire 1 Out of Every 4 Fields
01	Acquire 1 Out of Every 6 Fields
10	Acquire 1 Out of Every 8 Fields
11	Acquire 1 Out of Every 10 Fields

PIP Save/Clear Bit (RE_AQ) –D2

This bit controls the save and clear function for the instant replay. The bit value 1 is only effective when PON0–3 = 0000. (No PIP display.)

RE_AQ (2:2)	Function
0	Save Memory
1	Clear Reacquire

PIP Playback Speed Bits (PB_SP0–1) – D4–D5

These bits control the relative playback speed, to the acquired speed.

PB_SP (5:4)	Function
00	Playback at 1 x ACQ_SP Speed
01	Playback at 1/2 x ACQ_SP Speed
10	Playback at 1/4 x ACQ_SP Speed
11	Playback at 1/8 x ACQ_SP Speed

PIP Playback Control Bit (PB) – D6

This bit controls the start/stop of the instant replay function.

PB (6:6)	Function
0	No Action
1	Instant Replay Activated

PIP Fill/Background/Free Run/Test Register

Sub–address = 0Ch

PIP Fill Bits (PIPFILL0–1) – D0–D1

May be used to fill the PIP with one of three selectable solid colors

PIPFILL (1:0)	Function
00	Normal
01	Red
10	Green
11	Blue

Test Register Bits (INTC0 and MACR0) – D6–D7

When the FRUN is set to 1 the circuitry provides a generated sync and displays a flat field that can be either dark blue or gray determined by the BGND bit.

BGND (2:2)	Function
0	Blue
1	50% White

I^{2}C REGISTER TABLE

Sub–address	Data Bit							
	D7	D6	D5	D4	D3	D2	D1	D0
00	RPS3	RPS2	RPS1	RPS0	–	WPS2	WPS1	WPS0
01	–	–	–	VFON	PSD3	PSD2	PSD1	PSD0
02	–	–	–	–	–	BC2	BC1	BC0
03	MHP0	MVP0	–	–	–	ITM2	ITM1	ITM0
04	PSEL0	MSEL0	PSI90	STIL0	–	–	LIVE_P1	LIVE_P0
05	PBL3	PBL2	PBL1	PBL0	PON3	PON2	PON1	PON0
06	–	–	XPS5	XPS4	XPS3	XPS2	XPS1	XPS0
07	–	–	YPS5	YPS4	YPS3	YPS2	YPS1	YPS0
08	–	–	C5	C4	C3	C2	C1	C0
09	–	–	T5	T4	T3	T2	T1	T0
0A	–	–	–	–	–	YDL2	YDL1	YDL0
0B	–	PB	PB_SP1	PB_SP0	–	RE_AQ	ACQ_SP1	ACQ_SP0
0C	INTC	MACR	FRUN	–	–	BGND	PIPFILL1	PIPFILL0

Function Control of the MC44463

There are three modes of operation; Single PIP, Multiple PIP and Replay. These are enabled by setting specific register bits in the I^{2}C register set.

Single PIP (SPIP) Operation

Register 0Bh : D6 –> 0

Register 05h : D0–D7 –> 01h

Multiple PIP (MPIP) Operation

Register 05h : D0–D3 –> 07h or 0Fh

Register 04h : D0–D1 –> 0 to 3

Register 0Bh : D6 –> 0

Register 0Ch : D5 –> 1, D2 –> 0 or 1 (Optional)

Replay PIP (RPIP) Operation

In sequence, the Capture Ready mode must be first activated, allowing up to 8 seconds of fill memory with the desired video stream. Then the Capture mode must be set, disabling further write to memory. The Capture data may be re–displayed at any time afterword.

Capture Ready

Register 05h : D0–D3 –> 0

Register 0Bh : D6 –> 0, D2 –> 1, D0–D1 –> 0 to 3

Capture

Register 0Bh : D6 –> 1, D2 –> 0, D4–D5 –> 0 to 3

Register 05h: D0 –> 1

MOTOROLA

MC44817/17B

PLL Tuning Circuits with 3-Wire Bus

The MC44817/17B are tuning circuits for TV and VCR tuner applications. They contain on one chip all the functions required for PLL control of a VCO. The integrated circuits also contain a high frequency prescaler and thus can handle frequencies up to 1.3 GHz.

The MC44817 has programmable 512/1024 reference divider while the MC44817B has a fixed reference divider of 1024.

The MC44817/17B are manufactured on a single silicon chip using Motorola's high density bipolar process, MOSAIC™ (Motorola Oxide Self Aligned Implanted Circuits).

- Complete Single Chip System for MPU Control (3–Wire Bus). Data and Clock Inputs are IIC Bus Compatible
- Divide–by–8 Prescaler Accepts Frequencies up to 1.3 GHz
- 15 Bit Programmable Divider Accepts Input Frequencies up to 165 MHz
- Reference Divider: Programmable for Division Ratios 512 and 1024. The MC44817B has a Fixed 1024 Reference Divider
- Tri–State Phase/Frequency Comparator
- Operational Amplifier for Direct Tuning Voltage Output (30 V)
- Four Integrated PNP Band Buffers for 40 mA (V_{CC1} to 14.4 V)
- Output Options for the Reference Frequency and the Programmable Divider
- Bus Protocol for 18 or 19 Bit Transmission
- Extra Protocol for 34 Bit for Test and Further Features
- High Sensitivity Preamplifier
- Circuit to Detect Phase Lock
- Fully ESD Protected

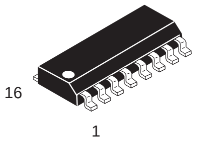
MOSAIC is a trademark of Motorola, Inc.

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC44817D	T_A = –20° to +80°C	SO–16
MC44817BD		

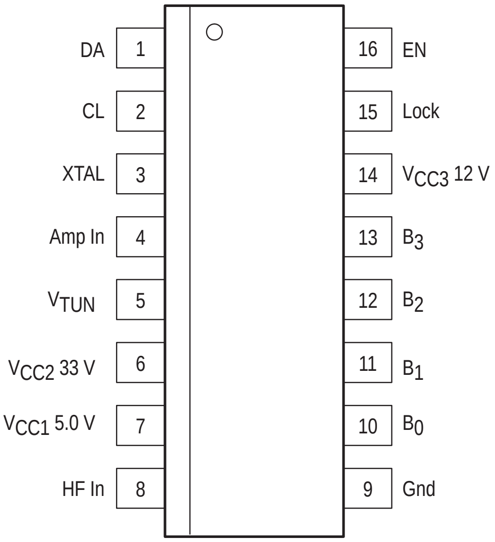
TV AND VCR PLL TUNING CIRCUITS WITH 1.3 GHz PRESCALER AND 3–WIRE BUS

SEMICONDUCTOR TECHNICAL DATA



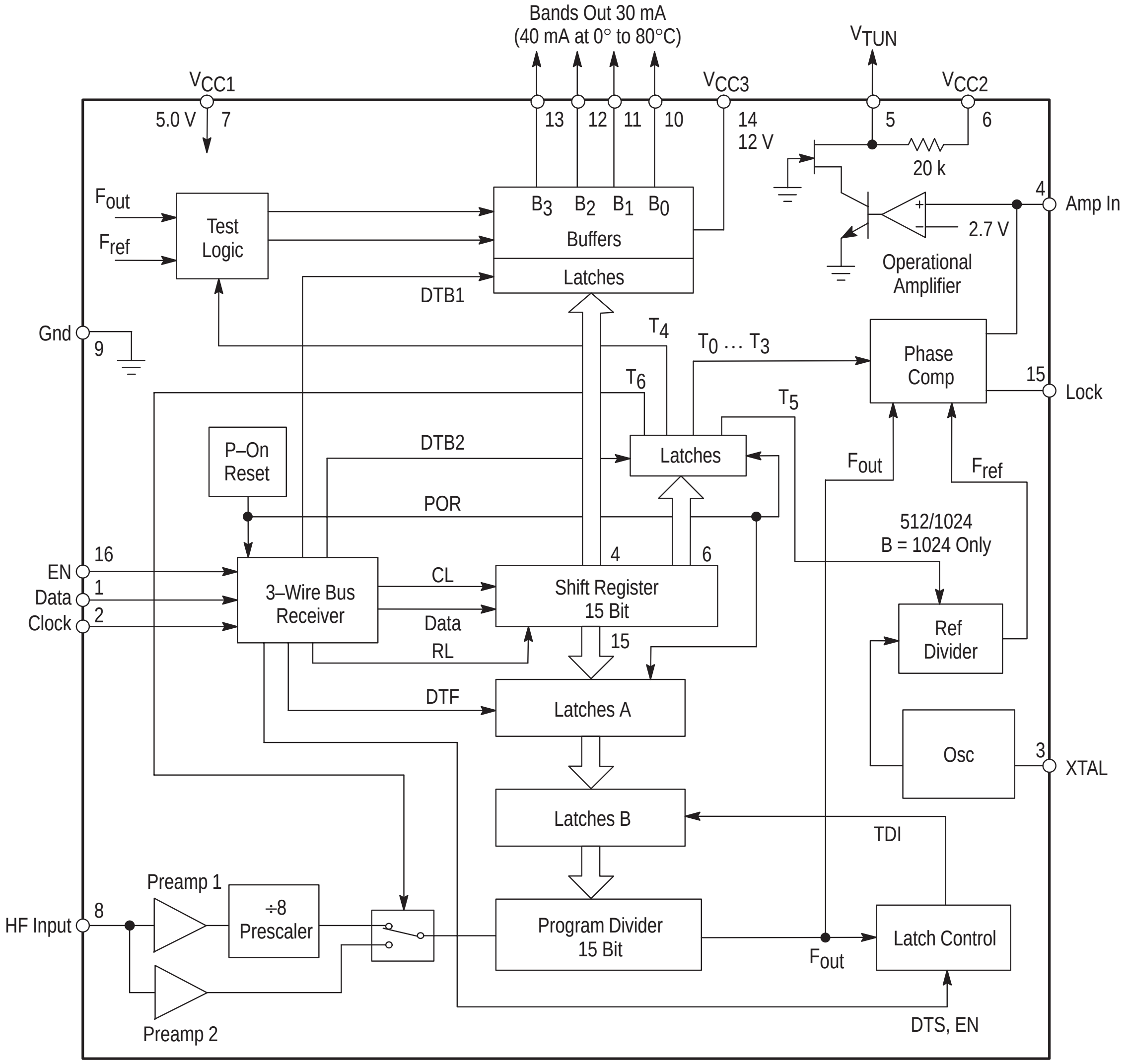
D SUFFIX
PLASTIC PACKAGE
CASE 751B
(SO–16)

PIN CONNECTIONS



(Top View)

Representative Block Diagram



This device contains 3,204 active transistors.

MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted.)

Rating	Pin	Value	Unit
Power Supply Voltage (V_{CC1})	7	6.0	V
Band Buffer “Off” Voltage	10–13	14.4	V
Band Buffer “On” Current	10–13	50	mA
Band Buffer – Short Circuit Duration (0 to V_{CC3}) (Note 2)	10–13	Continuous	–
Operational Amplifier Power Supply Voltage (V_{CC2})	6	40	V
Operational Amplifier Short Circuit Duration (0 to V_{CC2})	5	Continuous	–
Power Supply Voltage (V_{CC3})	14	14.4	V
Storage Temperature	–	–65 to +150	°C
Operating Temperature Range	–	–20 to +80	°C
Band Buffer Operation (Note 1) at 50 mA each Buffer All Buffers “On” Simultaneously	10–13	10	sec
Operational Amplifier Output Voltage	5	V_{CC2}	V
RF Input Level (10 MHz to 1.3 GHz)	–	1.5	Vrms

NOTES: 1. At $V_{CC3} = V_{CC1}$ to 14.4 V and T_A = –20° to +80°C.
2. At $V_{CC3} = V_{CC1}$ to 14.4 V and T_A = –20° to +80°C one buffer “On” only.

ELECTRICAL CHARACTERISTICS (V_{CC1} = 5.0 V, V_{CC2} = 33 V, V_{CC3} = 12 V, T_A = 25°C, unless otherwise noted.)

Characteristic	Pin	Min	Typ	Max	Unit
V_{CC1} Supply Voltage Range	7	4.5	5.0	5.5	V
V_{CC1} Supply Current (V_{CC1} = 5.0 V)	7	–	37	50	mA
V_{CC2} Supply Voltage Range	6	25	–	37	V
V_{CC2} Supply Current (Output Open)	6	–	1.5	3.5	mA
Band Buffer Leakage Current when “Off” at 12 V	10–13	–	0.01	1.0	µA
Band Buffer Saturation Voltage when “On” at 30 mA	10–13	–	0.15	0.3	V
Band Buffer Saturation Voltage when “On” at 40 mA only for 0° to 80°C	10–13	–	0.2	0.5	V
Data/Clock/Enable Current at 0 V	1, 2, 16	–10	–	0	µA
Data/Clock/Enable Current at 5.0 V	1, 2, 16	0	–	1.0	µA
Data/Clock/Enable Input Voltage Low	1, 2, 16	–	–	1.5	V
Data/Clock/Enable Input Voltage High	1, 2, 16	3.0	–	–	V
Clock Frequency Range	2	–	–	100	kHz
Oscillator Frequency Range	3	3.15	3.2	4.05	MHz
Operational Amplifier Internal Reference Voltage	–	2.0	2.75	3.2	V
Operational Amplifier Input Current	4	–15	0	15	nA
DC Open Loop Voltage Gain	–	100	250	–	V/V
Gain Bandwidth Product (CL = 1.0 nF)	–	0.3	–	–	MHz
V_{out} Low, Sinking 50 µA	5	–	0.2	0.4	V
V_{out} High, Sourcing 10 µA, $V_{CC2} – V_{out}$	5	–	0.2	0.5	V
Phase Comparator Tri–State Current	4	–15	0	15	nA
Charge Pump High Current of Phase Comparator	4	30	50	85	µA
Charge Pump Low Current of Phase Comparator	4	10	15	30	µA
V_{CC3} Supply Voltage Range	14	V_{CC1}	–	14.4	V
V_{CC3} Supply Current All Buffers “Off” One Buffer “On” when Open One Buffer “On” at 40 mA	14	 – – –	 0.2 8.0 48	 0.5 13 53	mA

Data Format and Bus Receiver

The circuit is controlled by a 3–wire bus via Data (DA), Clock (CL), and Enable (EN) inputs. The Data and Clock inputs may be shared with other inputs on the IIC–Bus while the Enable is a separate signal. The circuit is compatible with 18 and 19 bit data transmission and also has a mode for 34 bit transmission for test and additional features.

The 3–wire bus receiver receives data for the internal shift register after the positive going edge of the EN–signal. The data is transmitted to the band buffers on the negative going edge of the clock pulse 4 (signal DTB1).

18 and 19 Bit Data Transmission

The programmable divider may receive 14 bit (18 bit transmission) or 15 bit (19 bit transmission). The data is transmitted to the programmable divider (latches A) on the negative going edge of clock pulse 19 or on the negative edge of the EN–signal if EN goes down after the 18th clock pulse (signal DTF). If the programmable divider receives 14 bit, its MSB (bit N_{14}) is internally reset. The reset pulse is generated only if EN goes negative after the 18th clock pulse (signal RL).

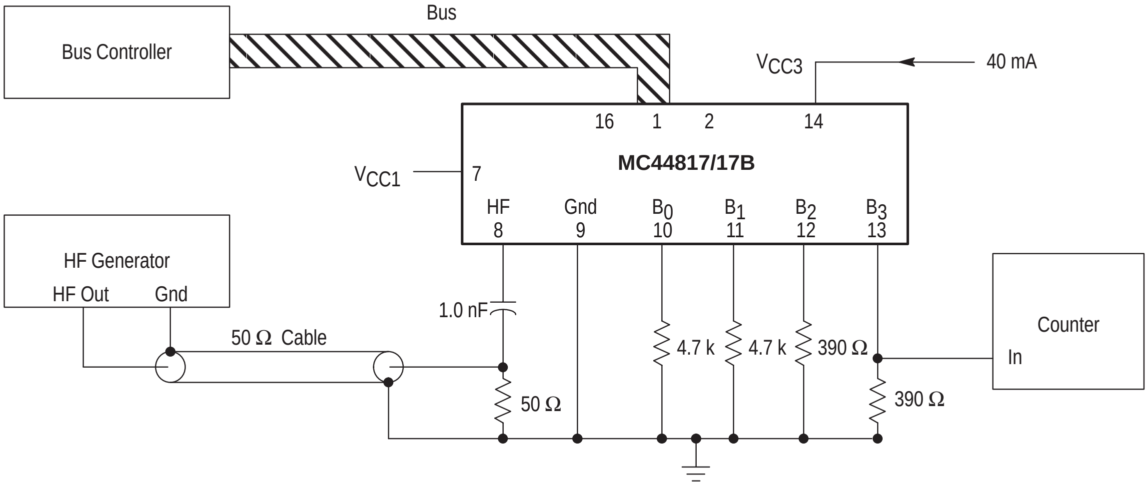
34 Bit Data Transmission
(For Test and Additional Features)

In the test mode, the programmable divider receives 15 bit and the data is transferred to latches A on the negative edge of clock pulse 19 (signal DTF). The information for test is received on clock pulses 20 to 26 and transmitted to the latches on the negative edge of pulse 34 (signal DTB2). These latches have a power–on reset. The power–on reset sets the programmable divider to a counting ratio of 256 or higher and resets the corresponding latches to the test bits T_0 to T_6 (signal POR). The bus receiver is not disturbed if the data format is wrong. Useless bits are ignored. If for example the Enable signal goes low after the clock pulse 9, bits one to four are accepted as valid buffer information and the other bits are ignored. If more than 34 bits are received, bit 35 and the following are ignored.

Lock Detector

The lock–detector output is low in lock. The output goes immediately high when an unlock condition is detected. The output goes low again when the loop is in lock during a complete period of the reference frequency.

Figure 1. HF Sensitivity Test Circuit



Device is in test mode. B_2, B_3 are "On" and B_0, B_1 are "Off".
Sensitivity is level of HF generator on 50 Ω load (without Pin 8 loading).

HF CHARACTERISTICS (See Figure 1)

Characteristic	Pin	Min	Typ	Max	Unit
DC Bias	8	–	1.6	–	V
Input Voltage Range					mVrms
10–80 MHz, Prescaler "Off", $T_6 = 1.0$	8	20	–	315	
80–150 MHz	8	10	–	315	
150–600 MHz	8	5.0	–	315	
600–950 MHz	8	10	–	315	
950–1300 MHz	8	50	–	315	

Figure 2. Typical HF Input Impedance

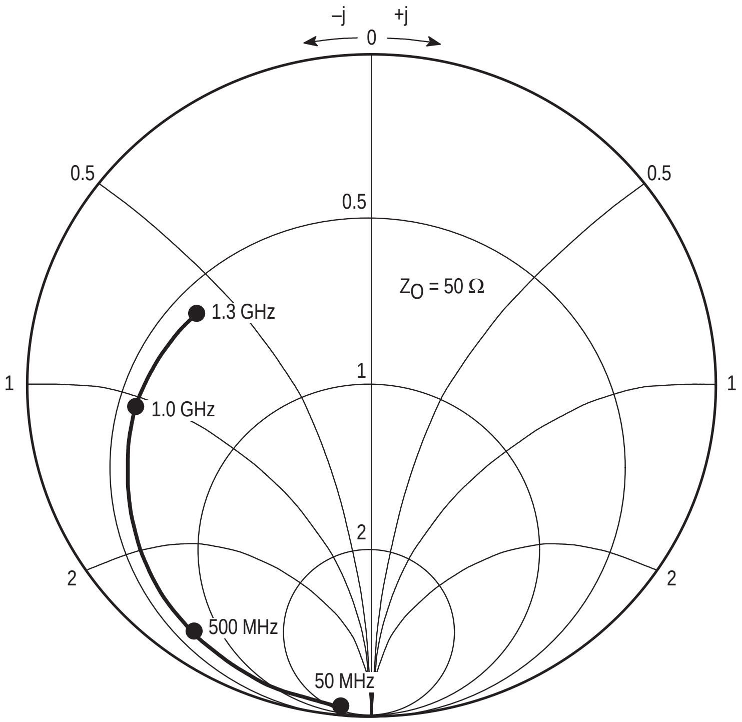
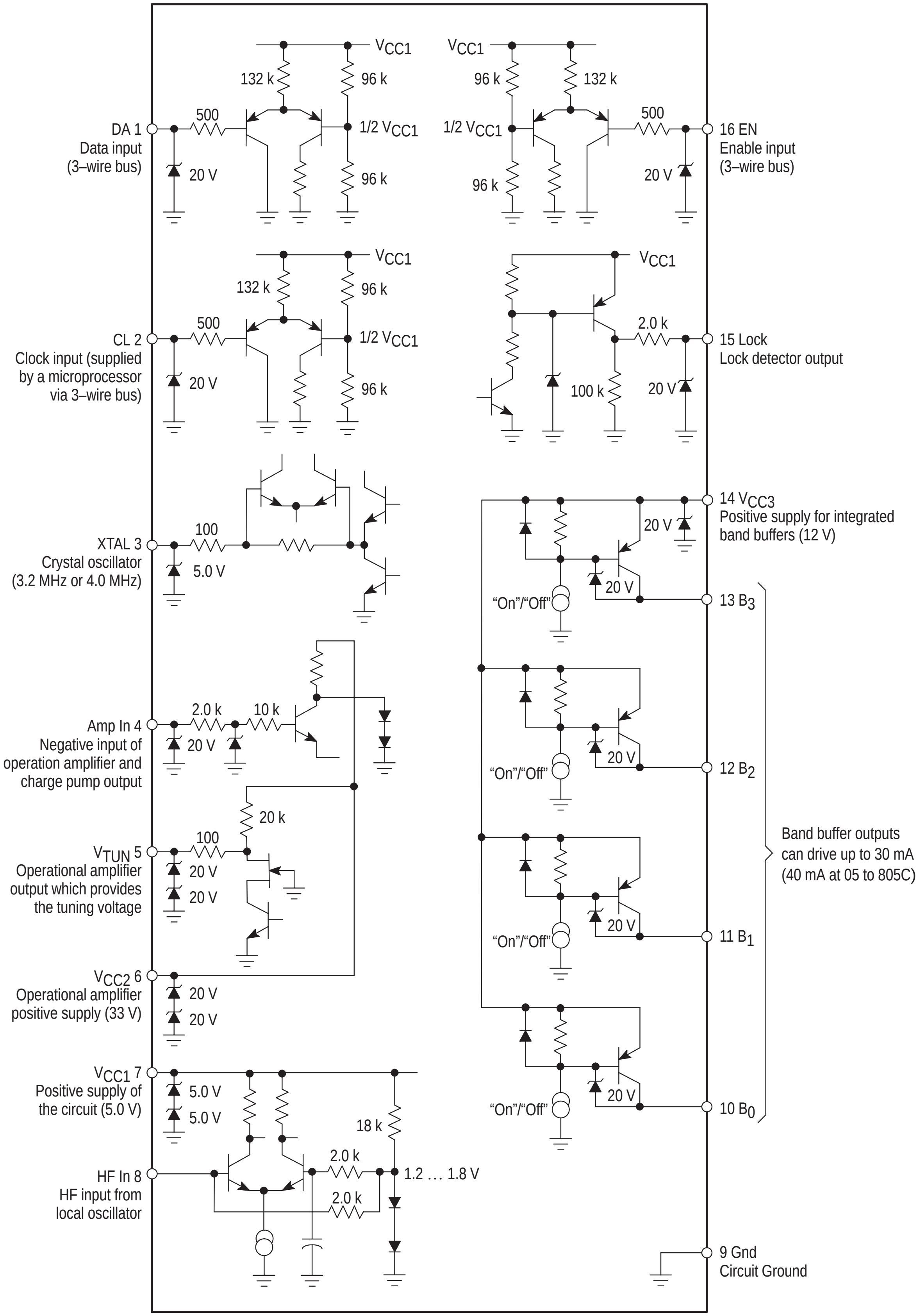
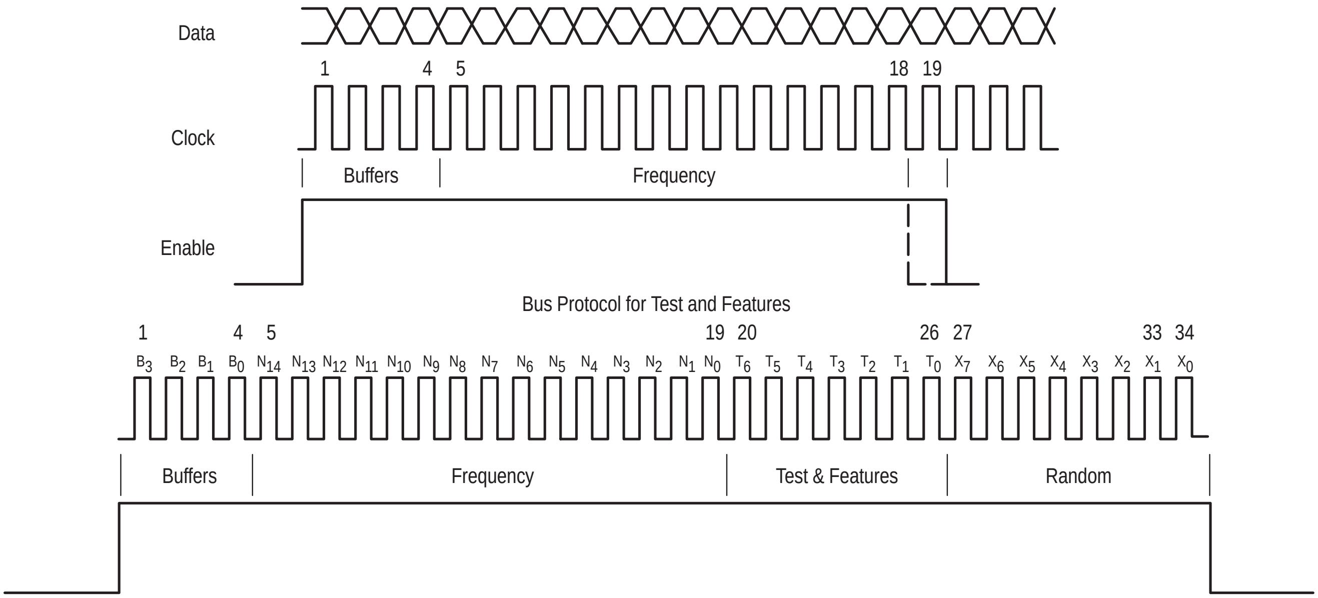


Figure 3. Pin Circuit Schematic



Bus Timing Diagram

Standard Bus Protocol 18 or 19 Bit



Definition of Permissible Bus Protocols

1. Bus Protocol for 18 Bit
   B_3 B_2 B_1 B_0 N_{13} N_{12} N_{11} N_{10} N_9 N_8 N_7 N_6 N_5 N_4 N_3 N_2 N_1 N_0
   Max Counting Ratio 16363
   N_{14} is Reset Internally
2. Bus Protocol for 19 Bit
   B_3 B_2 B_1 B_0 N_{14} N_{13} N_{12} N_{11} N_{10} N_9 N_8 N_7 N_6 N_5 N_4 N_3 N_2 N_1 N_0
   Max Counting Ratio 32767
   - B_0 to B_3: Control of Band Buffers
   - N_0 to N_{14}: Control of Programmable Dividers

   N_{14} = MSB; N_0 = LSB
   Minimum Counting Ratio Always 17
   B_3 = First Shifted Bit
   N_0 = Last Shifted Bit
3. Bus Protocol for Test and Further Features (34 Bit)
   B_3 B_2 B_1 B_0 N_{14}…N_0 T_6 T_5 T_4 T_3 T_2 T_1 T_0 X_7 X_6…X_1 X_0
   - T_0 to T_3: Control the Phase Comparator
   - T_4: Switches Test Signals to the Buffer Outputs
   - T_5: Division Ratio of the Reference Divider
     B Version T_5 = “X”
   - T_6: Bypasses the Prescaler (Note 1)
   - X_0 to X_7: Are Random

   B_3 = First Shifted Bit
   X_0 = Last Shifted Bit

Definition of the Bits for Test and Features

Bit T_0: Defines the Charge Pump Current of the Phase Comparator

T_0 = 0 = 1	Pump Current 50 µA Typical Pump Current 15 µA Typical

Bits T_1 and T_2: Define the Digital Function of the Phase Comparator

T_2	T_1	State	Output Function of Phase Comparator
0	0	1	Normal Operation
0	1	2	High Impedance (Tri–State)
1	0	3	Upper Source “On”, Lower Source “Off”
1	1	4	Lower Source “On”, Upper Source “Off”

NOTE: 1. The phase comparator pulls high if the input frequency is too high and it pulls low when the input frequency is too low. (Inversion by Operational Amplifier) The phase comparator generates a fixed duration offset pulse for each comparison pulse (similar to the MC44802A). This guarantees operation in the linear region. The offset pulse is a positive current pulse (upper source).

Bit T_3: Defines the Offset Pulse of the Phase Comparator

T_3 = 0	Offset Pulse Short (200 ns) Normal Mode
= 1	Offset Pulse Long (350 ns)

Bit T_4: Switches the Internal Frequencies F_{ref} and FBY2 to the Buffer Outputs (B_2, B_3)

T_4 = 0	Normal Operation
= 1	F_{ref} Switched to Buffer Output B_2 FBY2 Switched to Buffer Output B_3

NOTE: Bits B_2 and B_3 have to be one in this case.
F_{ref} is the reference frequency.
FBY2 is the output frequency of the programmable divider, divided by two.

Bit T_5: Defines the Division Ratio of the Reference Divider

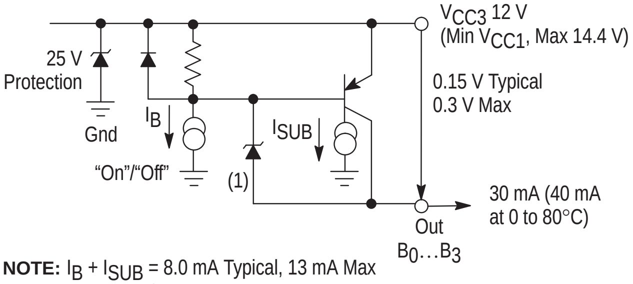
T_5 = 0 = 1	Division Ratio 512 Division Ratio 1024

NOTE: The division ratio of the reference divider can only be programmed in the 34 bit bus protocol.
In the standard bus protocol the division ratio is 512.
(The power–up reset POR sets the division ratio to 512).
On “B–version”, T_5 = “X”. Division ratio 1024 fixed.

Bit T_6: Switches the Prescaler

$T_6 = 0$	Normal Operation, 1.3 GHz
= 1	Low Frequency Operation Preamp. 2 Switched Off, 165 MHz maximum The prescaler is bypassed and the power supply of the prescaler is switched off. Input: 10 MHz minimum, 20 mVrms minimum

Figure 4. Equivalent Circuit of the Integrated Band Buffers



NOTE: $I_B + I_{SUB}$ = 8.0 mA Typical, 13 mA Max
I_B = Base Current
I_{SUB} = Substrate Current of PNP

The Programmable Divider

The programmable divider is a presettable down counter. When it has counted to zero it takes its required division ratio out of the latches B. Latches B are loaded from latches A by means of signal TDI which is synchronous to the programmable divider output signal.

Since latches A receive the data asynchronously with the programmable divider; this double latch scheme is needed to assure correct data transfer to the counter.

The division ratio definition is given by:

$N = 16384 \times N_{14} + 8132 \times N_{13} + \ldots + 4 \times N_2 + 2 \times N_1 + N_0$

Maximum Ratio 32767
(16363 in case of 18 bit bus protocol)
Minimum Ratio 17
$N_0 \ldots N_{14}$ are the different bits for frequency information.

At power–on the whole bus receiver is reset and the programmable divider is set to a counting ratio of N = 256 or higher.

The Prescaler

The prescaler has a preamplifier which guarantees high input sensitivity.

The Phase Comparator

The phase comparator is phase and frequency sensitive and has very low output leakage current in the high impedance state.

The Operational Amplifier

The operational amplifier is designed for very low noise, low input bias current and high power supply rejection. The positive input is biased internally. The operational amplifier needs 28.5 V supply (V_{CC2}) as minimum voltage for a guaranteed maximum tuning voltage of 28 V.

Figure 6 shows a possible filter arrangement. The component values depend very much on the application (tuner characteristic, reference frequency, etc.).

The Oscillator

The oscillator uses a 3.2 to 4.0 MHz crystal tied to ground in series with a capacitor. The crystal operates in the series resonance mode.

The voltage at Pin 3 has low amplitude and low harmonic distortion.

Figure 5. Equivalent Circuit of the Lock Output

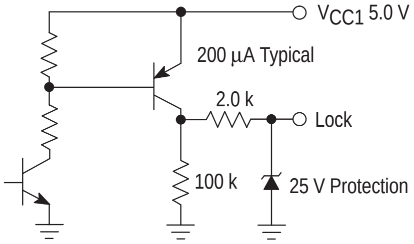
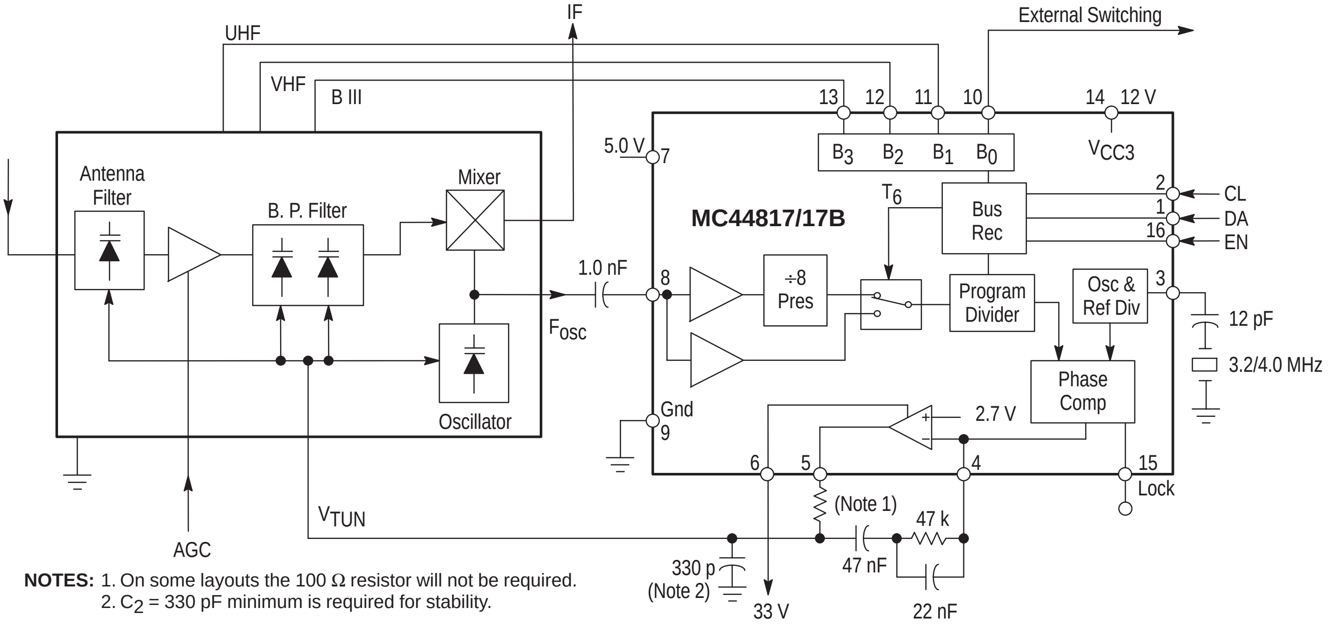


Figure 6. Typical Tuner Application



NOTES: 1. On some layouts the 100 Ω resistor will not be required.
2. C_2 = 330 pF minimum is required for stability.

MC44818

PLL Tuning Circuit with I^{2}C Bus

The MC44818 is a tuning circuit for TV and VCR tuner applications. It contains, on one chip, all the functions required for PLL control of a VCO. This integrated circuit also contains a high frequency prescaler and thus can handle frequencies up to 1.3 GHz. The MC44818 is a pin compatible drop in replacement for the MC44817, where the only difference is the MC44818 has a fixed divide–by–8 prescaler (cannot be bypassed) and the MC44817 uses the three wire bus.

The MC44818 has a programmable 512/1024 reference divider and is manufactured on a single silicon chip using Motorola's high density bipolar process, MOSAIC™ (Motorola Oxide Self Aligned Implanted Circuits).

- Complete Single Chip System for MPU Control (I^{2}C Bus). Data and Clock Inputs are 3–Wire Bus Compatible
- Divide–by–8 Prescaler Accepts Frequencies up to 1.3 GHz
- 15 Bit Programmable Divider Accepts Input Frequencies up to 165 MHz
- Reference Divider: Programmable for Division Ratios 512 and 1024.
- 3–State Phase/Frequency Comparator
- Operational Amplifier for Direct Tuning Voltage Output (30 V)
- Four Integrated PNP Band Buffers for 40 mA (V_{CC1} to 14.4 V)
- Output Options for the Reference Frequency and the Programmable Divider
- High Sensitivity Preamplifier
- Circuit to Detect Phase Lock
- Fully ESD Protected

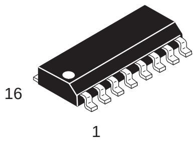
MOSAIC is a trademark of Motorola, Inc.

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC44818D	T_A = –20° to +80°C	SO–16

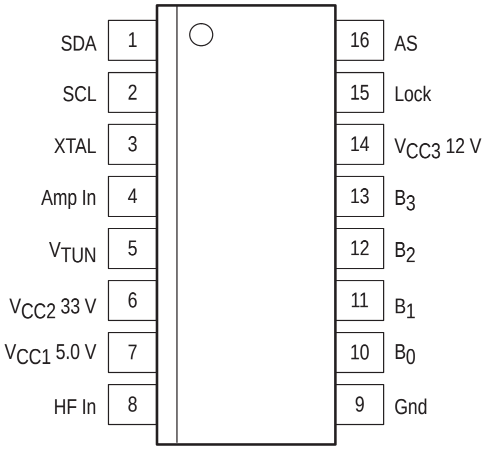
TV AND VCR PLL TUNING CIRCUIT WITH 1.3 GHz PRESCALER AND I^{2}C BUS

SEMICONDUCTOR TECHNICAL DATA



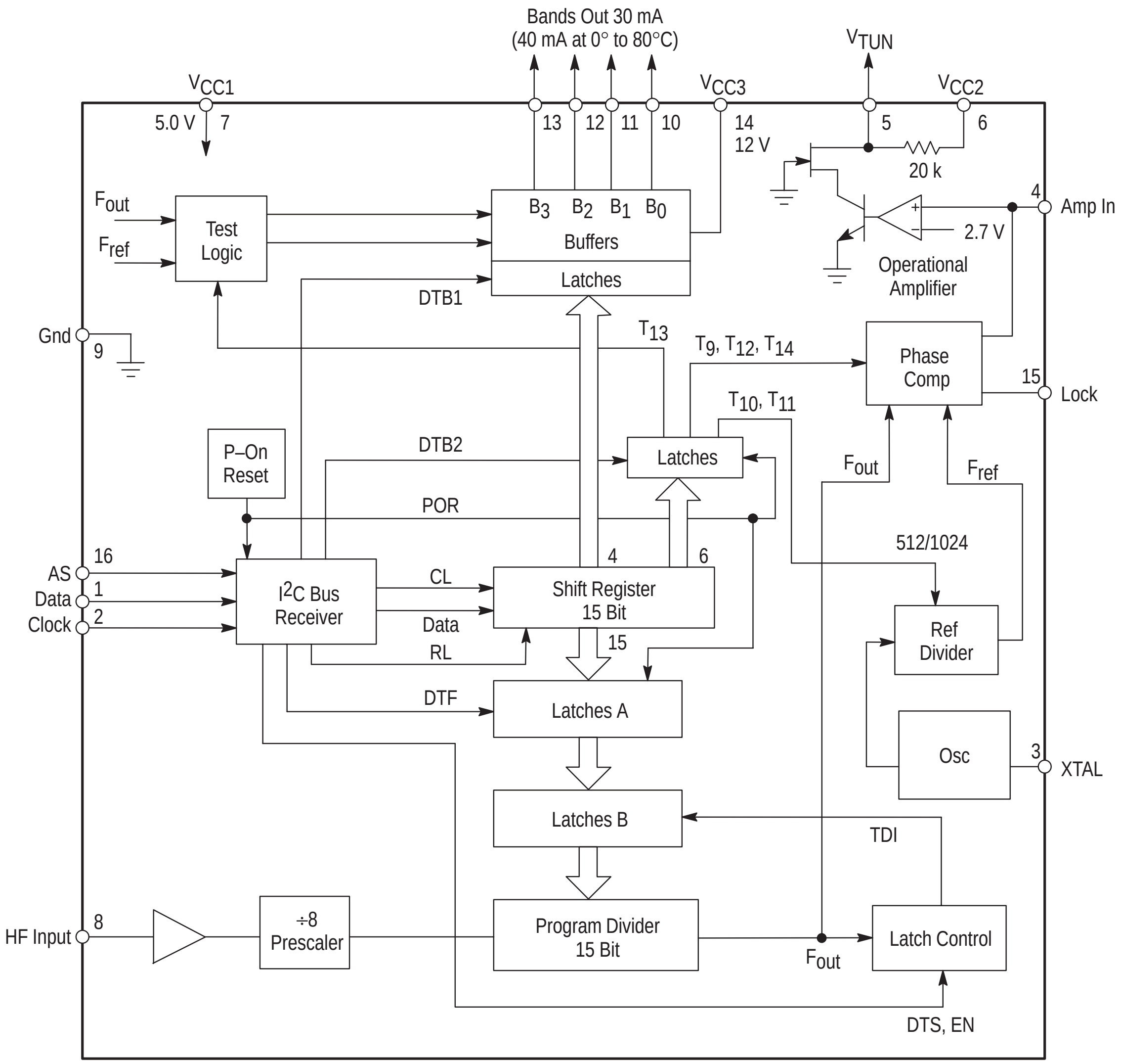
D SUFFIX
PLASTIC PACKAGE
CASE 751B
(SO–16)

PIN CONNECTIONS



(Top View)

Representative Block Diagram



This device contains 3,204 active transistors.

MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted.)

Rating	Pin	Value	Unit
Power Supply Voltage (V_{CC1})	7	6.0	V
Band Buffer “Off” Voltage	10–13	14.4	V
Band Buffer “On” Current	10–13	50	mA
Band Buffer – Short Circuit Duration (0 to V_{CC3}) (Note 2)	10–13	Continuous	–
Operational Amplifier Power Supply Voltage (V_{CC2})	6	40	V
Operational Amplifier Short Circuit Duration (0 to V_{CC2})	5	Continuous	–
Power Supply Voltage (V_{CC3})	14	14.4	V
Storage Temperature	–	–65 to +150	°C
Operating Temperature Range	–	–20 to +80	°C
Band Buffer Operation (Note 1) at 50 mA each Buffer All Buffers “On” Simultaneously	10–13	10	sec
Operational Amplifier Output Voltage	5	V_{CC2}	V
RF Input Level (10 MHz to 1.3 GHz)	–	1.5	Vrms

NOTES: 1. At $V_{CC3} = V_{CC1}$ to 14.4 V and T_A = –20° to +80°C.
2. At $V_{CC3} = V_{CC1}$ to 14.4 V and T_A = –20° to +80°C one buffer “On” only.

ELECTRICAL CHARACTERISTICS (V_{CC1} = 5.0 V, V_{CC2} = 33 V, V_{CC3} = 12 V, T_A = 25°C, unless otherwise noted.)

Characteristic	Pin	Min	Typ	Max	Unit
V_{CC1} Supply Voltage Range	7	4.5	5.0	5.5	V
V_{CC1} Supply Current (V_{CC1} = 5.0 V)	7	–	37	50	mA
V_{CC2} Supply Voltage Range	6	25	–	37	V
V_{CC2} Supply Current (Output Open)	6	–	1.5	2.3	mA
Band Buffer Leakage Current when “Off” at 12 V	10–13	–	0.01	1.0	µA
Band Buffer Saturation Voltage when “On” at 30 mA	10–13	–	0.15	0.3	V
Band Buffer Saturation Voltage when “On” at 40 mA only for 0° to 80°C	10–13	–	0.2	0.5	V
Data/Clock Current at 0 V	1, 2	–10	–	0	µA
Clock Current at 5.0 V	2	0	–	1.0	µA
Data Current at 5.0 V Acknowledge “Off”	1	0	–	1.0	µA
Data Saturation Voltage at 15 mA Acknowledge “On”	1	–	–	1.0	V
Data/Clock Input Voltage Low	1, 2	–	–	1.5	V
Data/Clock Input Voltage High	1, 2	3.0	–	–	V
Clock Frequency Range	2	–	–	100	kHz
Oscillator Frequency Range	3	3.15	3.2	4.05	MHz
Operational Amplifier Internal Reference Voltage	–	2.0	2.75	3.2	V
Operational Amplifier Input Current	4	–15	0	15	nA
DC Open Loop Voltage Gain	–	100	250	–	V/V
Gain Bandwidth Product (C_L = 1.0 nF)	–	0.3	–	–	MHz
V_{out} Low, Sinking 50 µA	5	–	0.2	0.4	V
V_{out} High, Sourcing 10 µA, $V_{CC2} – V_{out}$	5	–	0.2	0.5	V
Phase Detector Current in the High Impedance State	4	–15	0	15	nA
Charge Pump High Current of Phase Comparator	4	30	50	85	µA
Charge Pump Low Current of Phase Comparator	4	10	15	30	µA
V_{CC3} Supply Voltage Range	14	V_{CC1}	–	14.4	V
V_{CC3} Supply Current All Buffers “Off” One Buffer “On” when Open One Buffer “On” at 40 mA	14	 – – –	 0.2 8.0 48	 0.5 13 53	mA

Data Format and Bus Receiver

The circuit receives the information for tuning and control via the I^2C bus. The incoming information, consisting of a chip address byte followed by two or four data bytes, is treated in the I^2C bus receiver. The definition of the permissible bus protocol is shown below:

1_STA CA CO BA STO
2_STA CA FM FL STO
3_STA CA CO BA FM FL STO
4_STA CA FM FL CO BA STO

STA = Start Condition
STO = Stop Condition
CA = Chip Address Byte
CO = Data Byte for Control Information
BA = Band Information
FM = Data Byte for Frequency Information
FL = Data Byte for Frequency Information

Figure 1. Complete Data Transfer Process

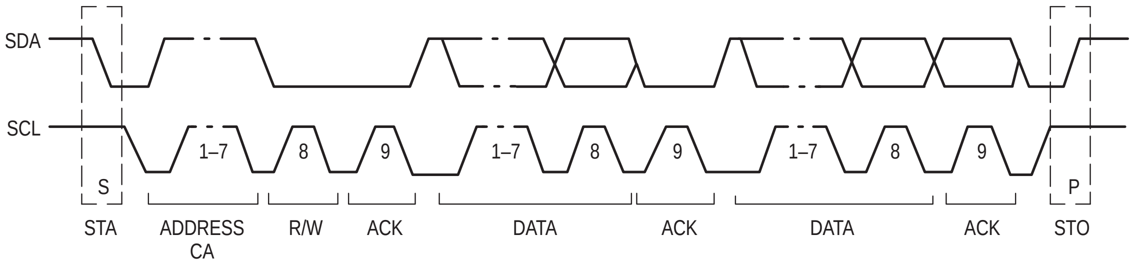


Figure 2 shows the five bytes of information that are needed for circuit operation: there is the chip address, two bytes of control and band information and two bytes of frequency information.

After the chip address, two or four data bytes may be received: if three data bytes are received the third data byte is ignored.

If five or more data bytes are received the fifth and following data bytes are ignored and the last acknowledge pulse is sent at the end of the fourth data byte.

The first and the third data bytes contain a function bit which allows the IC to distinguish between frequency information and control plus band information.

Frequency information is preceeded by a Logic “0”. If the function bit is Logic “1” the two following bytes contain control and band information. The first data byte, shifted after the chip address, may be byte CO or byte FM.

The two permissible bus protocols with five bytes are shown in Figure 2.

Figure 2. Definition of Bytes

CA_Chip Address	1	1	0	0	0	0/1	0/1	0	ACK
CO_Information	①	T_{14}	T_{13}	T_{12}	T_{11}	T_{10}	T_9	T_8	ACK
BA_Band Information	X	X	X	X	B_3	B_2	B_1	B_0	ACK
FM_Frequency Information	⓪	N_{14}	N_{13}	N_{12}	N_{11}	N_{10}	N_9	N_8	ACK
FL_Frequency Information	N_7	N_6	N_5	N_4	N_3	N_2	N_1	N_0	ACK

CA_Chip Address	1	1	0	0	0	0/1	0/1	0	ACK
FM_Frequency Information	⓪	N_{14}	N_{13}	N_{12}	N_{11}	N_{10}	N_9	N_8	ACK
FL_Frequency Information	N_7	N_6	N_5	N_4	N_3	N_2	N_1	N_0	ACK
CO_Information	①	T_{14}	T_{13}	T_{12}	T_{11}	T_{10}	T_9	T_8	ACK
BA_Band Information	X	X	X	X	B_3	B_2	B_1	B_0	ACK

Chip Address

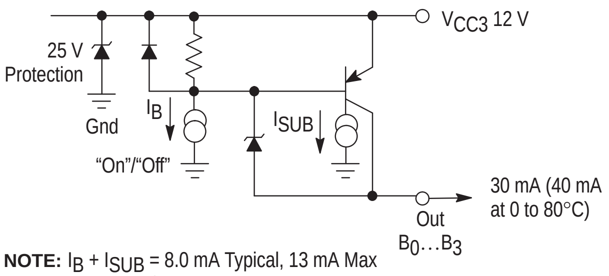
The chip address is programmable by Pin 16 (AS – Address Select).

AS – Pin 16	Address (HEX.)
Gnd to 0.1 V_{CC1}	C0
Open or 0.2 V_{CC1} to 0.3 V_{CC1}	C2
0.4 V_{CC1} to 0.7 V_{CC1}	C4
0.8 V_{CC1} to 1.1 V_{CC1}	C6

Bits B_0, B_1, B_2, B_3: Control the Band Buffers

B_0, B_1, B_2, B_3 = 0 = 1	Buffer “Off” Buffer “On”

Figure 3. Equivalent Circuit of the Integrated Band Buffers



NOTE: $I_B + I_{SUB}$ = 8.0 mA Typical, 13 mA Max
I_B = Base Current
I_{SUB} = Substrate Current of PNP

Bit T_8: Controls the Output of the Operational Amplifier

T_8 = 0	Normal Operation Operational Amplifier Active
= 1	Output State of Operational Amplifier Switched “Off”, Output Pulls High Through 20 k Internal Pull–Up Resistor

Bits T_9, T_{12}: Control the Phase Comparator

T_9	T_{12}	Function
1	0	Normal Operation
1	1	High Impedance
0	0	Upper Source “On” Only
0	1	Lower Source “On” Only

Bits T_{10}, T_{11}: Control the Reference Ratio

T_{10}	T_{11}	Division Ratio
0	0	512
0	1	1024
1	0	1024
1	1	512

Bit T_{13}: Switches the Internal Signals F_{ref} and F_{BY2} to the Band Buffer Outputs (Test)

T_{13} = 0	Normal Operation
= 1	Test Mode F_{ref} Output at B_2 (Pin 12) F_{BY2} Output at B_3 (Pin 13)

Bits B_2 and B_3 have to be “On”, $B_2 = B_3 = 1$ in the test mode.
F_{ref} is the reference frequency.
F_{BY2} is the output frequency of the programmable divider, divided by two.

Bit T_{14}: Controls the Charge Pump Current of the Phase Comparator

$T_{14} = 0$	Pump Current 15 µA Typical
$= 1$	Pump Current 50 µA Typical

The Programmable Divider

The programmable divider is a presettable down counter. When it has counted to zero it takes its required division ratio out of the latches B. Latches B are loaded from latches A by means of signal TDI which is synchronous to the programmable divider output signal.

Since latches A receive the data asynchronously with the programmable divider; this double latch scheme is needed to assure correct data transfer to the counter.

The division ratio definition is given by:

$N = 16384 \times N_{14} + 8192 \times N_{13} + \ldots + 4 \times N_2 + 2 \times N_1 + N_0$

Maximum Ratio 32767

Minimum Ratio 17

$N_0 \ldots N_{14}$ are the different bits for frequency information.

At power "on" the whole bus receiver is reset and the programmable divider is set to a counting ratio of N = 256 or higher.

The Prescaler

The prescaler has a preamplifier which guarantees high input sensitivity.

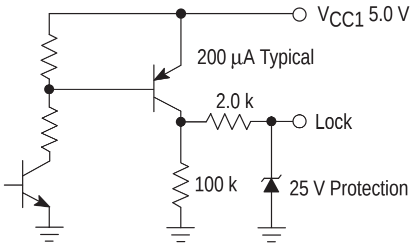
The Phase Comparator

The phase comparator is phase and frequency sensitive and has very low output leakage current in the high impedance state.

Lock Detector

The lock detector output is low in lock. The output goes immediately high when an unlock condition is detected. The output goes low again when the loop is in lock during a complete period of the reference frequency.

Figure 4. Equivalent Circuit of the Lock Output



The Operational Amplifier

The operational amplifier is designed for very low noise, low input bias current and high power supply rejection. The positive input is biased internally. The operational amplifier needs 28.5 V supply (V_{CC2}) as minimum voltage for a guaranteed maximum tuning voltage of 28 V.

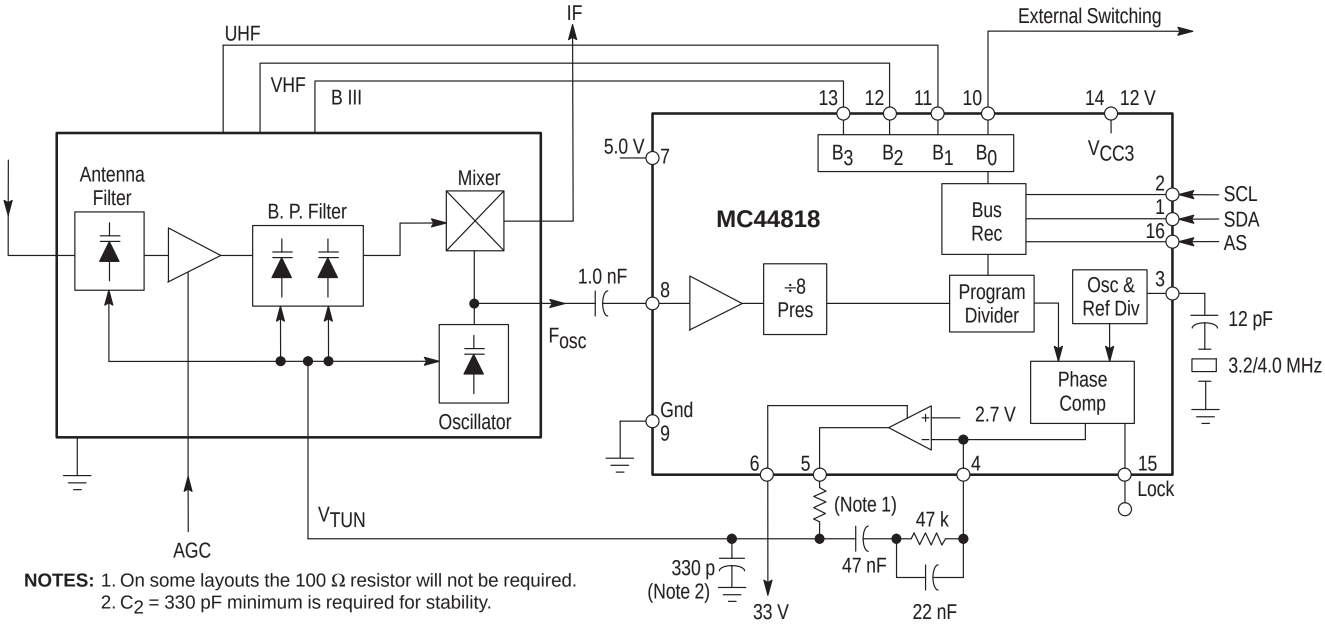
Figure 6 shows a possible filter arrangement. The component values depend very much on the application (tuner characteristic, reference frequency, etc.).

The Oscillator

The oscillator uses a 3.2 to 4.0 MHz crystal tied to ground in series with a capacitor. The crystal operates in the series resonance mode.

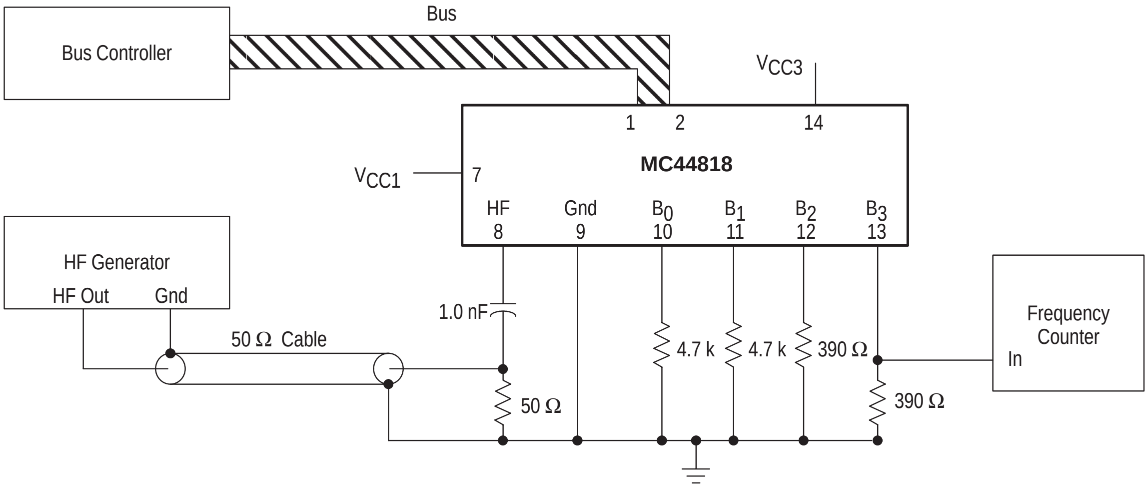
The voltage at Pin 3 has low amplitude and low harmonic distortion.

Figure 5. Typical Tuner Application



NOTES: 1. On some layouts the 100 Ω resistor will not be required.
2. C_2 = 330 pF minimum is required for stability.

Figure 6. HF Sensitivity Test Circuit



Device is in test mode. B_2, B_3 are "On" and B_0, B_1 are "Off".
Sensitivity is level of HF generator on 50 Ω load (without Pin 8 loading).

HF CHARACTERISTICS (See Figure 1)

Characteristic	Pin	Min	Typ	Max	Unit
DC Bias	8	–	1.6	–	V
Input Voltage Range					mVrms
80–150 MHz	8	10	–	315	
150–600 MHz	8	5.0	–	315	
600–950 MHz	8	10	–	315	
950–1300 MHz	8	50	–	315	

Figure 7. Typical HF Input Impedance

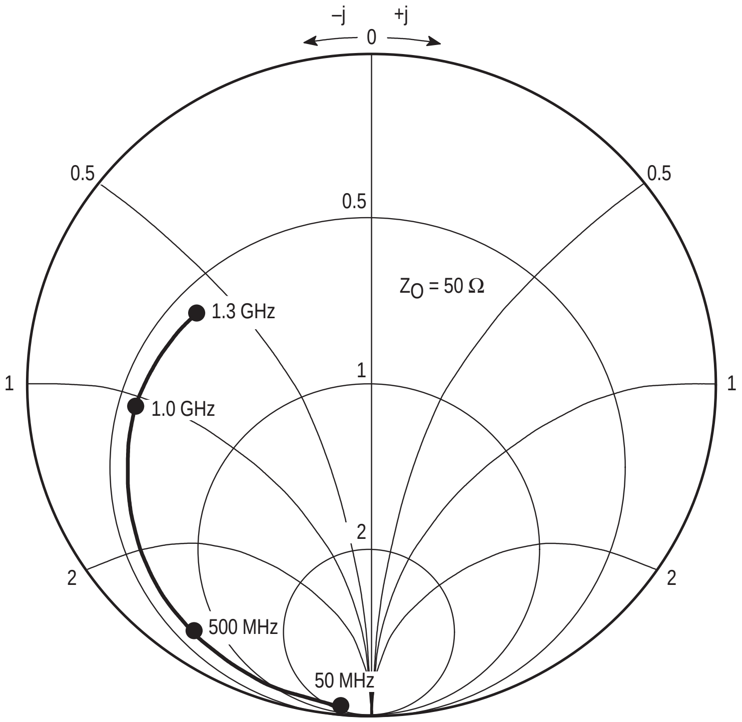
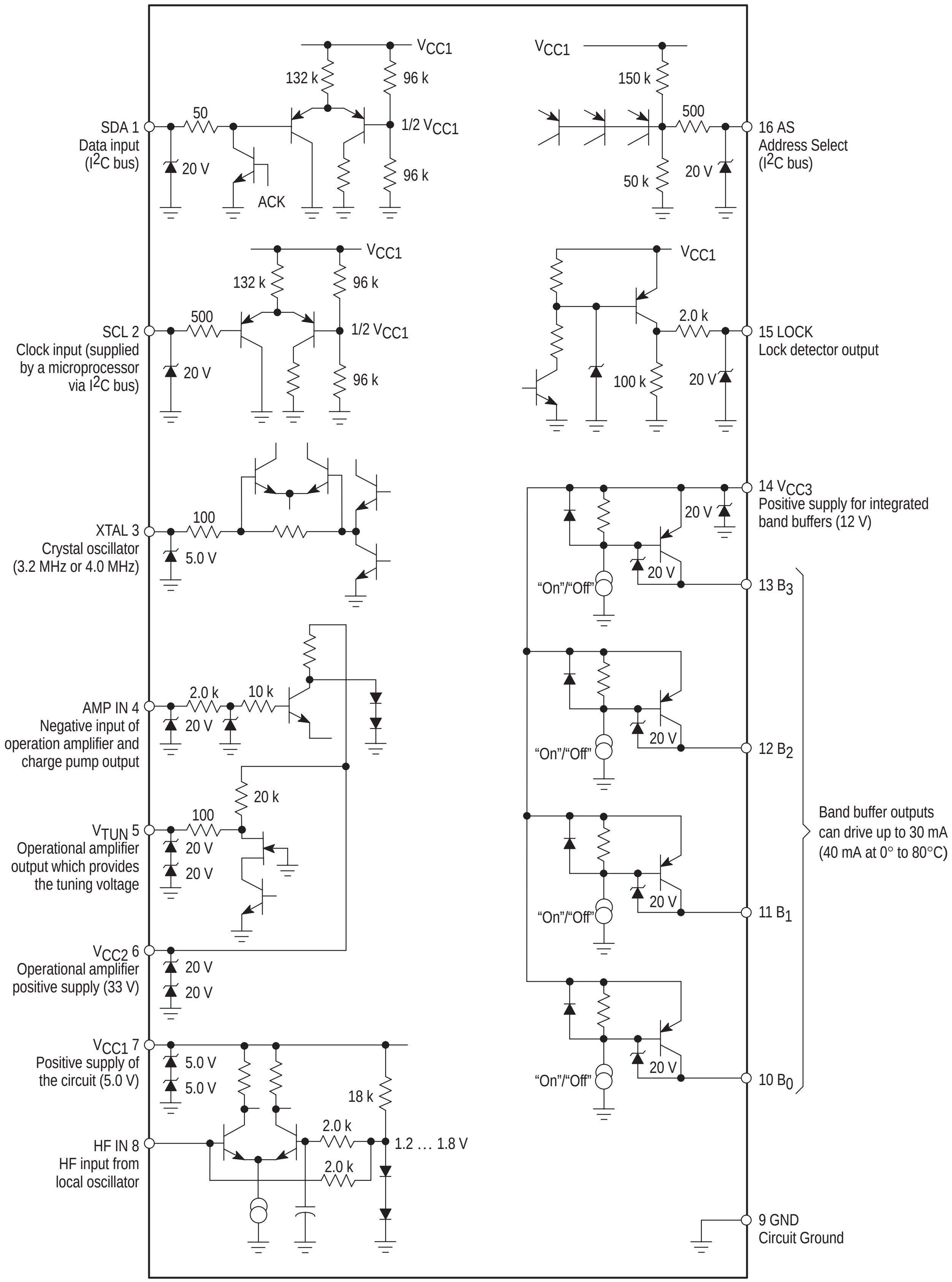


Figure 8. Pin Circuit Schematic



MC44824/25

PLL Tuning Circuits with I^{2}C Bus

The MC44824/25 are tuning circuits for TV and VCR tuner applications. They contain on one chip all the functions required for PLL control of a VCO. The integrated circuits also contain a high frequency prescaler and thus can handle frequencies up to 1.3 GHz.

The MC44824/25 are manufactured on a single silicon chip using Motorola's high density bipolar process, MOSAIC™ (Motorola Oxide Self Aligned Implanted Circuits).

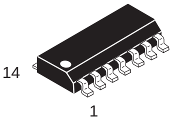
- Complete Single Chip System for MPU Control (I^{2}C Bus). Data and Clock Inputs are 3–Wire Bus Compatible
- Divide–by–8 Prescaler Accepts Frequencies up to 1.3 GHz
- 15 Bit Programmable Divider
- Reference Divider: Programmable for Division Ratios 512 and 1024
- 3–State Phase/Frequency Comparator
- 4 Programmable Chip Addresses
- 3 Output Buffers (MC44824) respectively 5 Output Buffers (MC44825) for 10 mA/15 V
- Operational Amplifier for use with External NPN Transistor
- SO–14 Package for MC44824 and SO–16 for MC44825
- High Sensitivity Preamplifier
- Fully ESD Protected

MOSAIC is a trademark of Motorola, Inc.

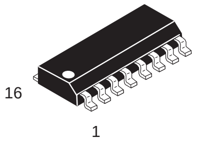
ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC44824D	$T_A = -20° \text{ to } +80°C$	SO–14
MC44825D		SO–16

TV AND VCR PLL TUNING CIRCUITS WITH 1.3 GHz PRESCALER AND I^{2}C BUS



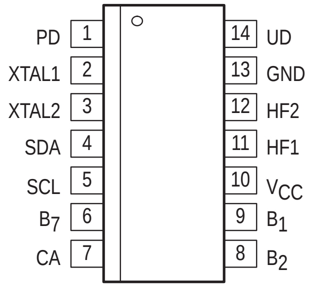
D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO–14)



D SUFFIX
PLASTIC PACKAGE
CASE 751B
(SO–16)

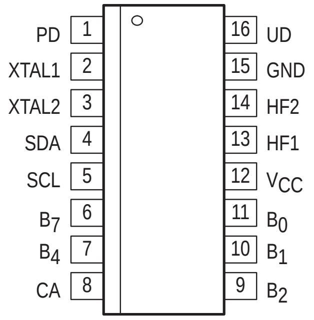
PIN CONNECTIONS

MC44824



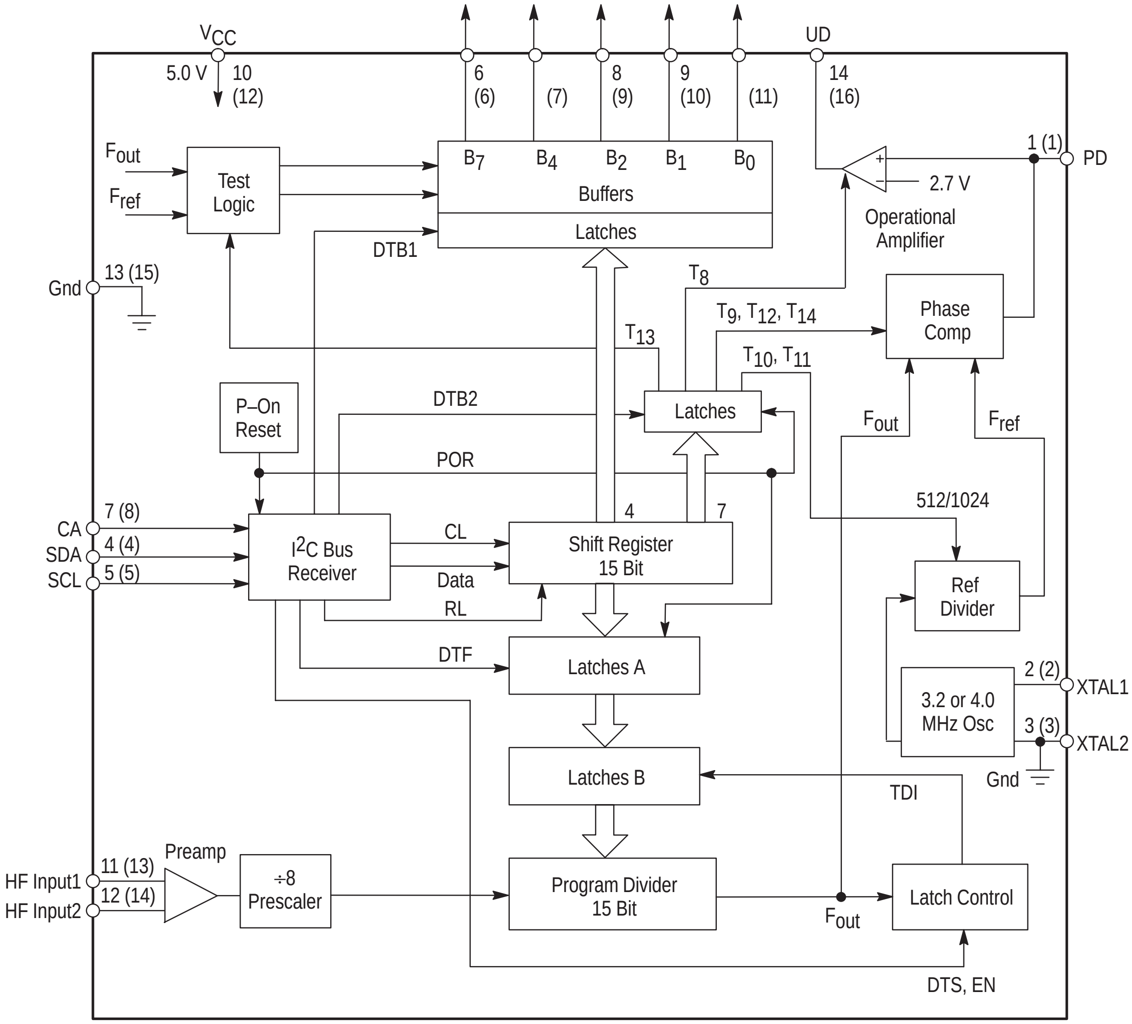
(Top View)

MC44825



(Top View)

Representative Block Diagram



MC44825 Pin Numbers ( )

This device contains 3,204 active transistors.

PIN FUNCTION DESCRIPTION

Pin		Symbol	Description
MC44824	MC44825		
1	1	PD	Input of tuning voltage amplifier
2	2	XTAL1	First crystal input is the active pin at the oscillators
3	3	XTAL2	Second crystal input is the internal ground
4	4	SDA	Data input
5	5	SCL	Clock input of the I^{2}C bus
6, 8, 9	–	B_7, B_2, B_1	Band buffer (open collector) outputs for up to 10 mA
–	6, 7, 9, 10, 11	B_7, B_4, B_2, B_1, B_0	Band buffer (open collector) outputs for up to 10 mA
7	8	CA	Chip address selection pin
10	12	V_{CC}	Supply voltage, typical 5.0 V
11, 12	13, 14	HF1/HF2	Symmetric HF inputs from local oscillator
13	15	GND	Ground
14	16	UD	Output of the tuning voltage amplifier. Needs an external NPN with pull–up resistor to drive the varicaps

MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted.)

Rating	Pin MC44824	Pin MC44825	Value	Unit
Power Supply Voltage (V_{CC})	10	12	6.0	V
Band Buffer “Off” Voltage	6, 8, 9	6, 7, 9, 10, 11	15	V
Band Buffer “On” Current	6, 8, 9	6, 7, 9, 10, 11	15	mA
Storage Temperature	–	–	–65 to +150	°C
Operating Temperature Range	–	–	–20 to +80	°C
RF Input Level (10 MHz to 1.3 GHz)	11, 12	13, 14	1.5	Vrms

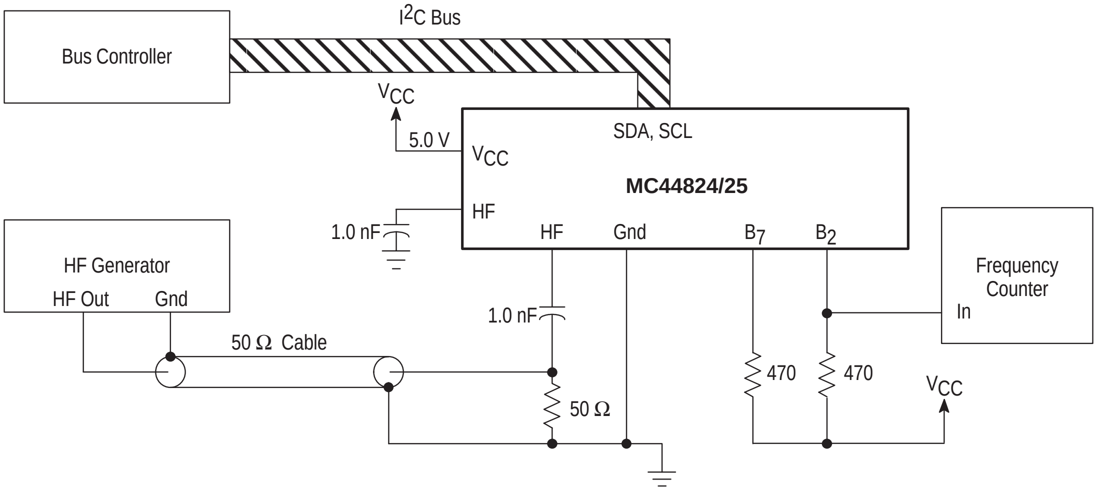
ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C, unless otherwise noted.)

Characteristic	Pin MC44824	Pin MC44825	Min	Typ	Max	Unit
V_{CC} Supply Voltage Range	10	12	4.5	5.0	5.5	V
V_{CC} Supply Current (V_{CC} = 5.0 V)	10	12	–	40	55	mA
Band Buffer Leakage Current when “Off” at 12 V	6, 8, 9	6, 7, 9, 10, 11	–	0.01	1.0	µA
Band Buffer Saturation Voltage when “On” at 10 mA	6, 8, 9	6, 7, 9, 10, 11	–	1.6	1.8	V
Data Saturation Voltage at 15 mA Acknowledge “On”	4	4	–	–	1.0	V
Data/Clock/Enable Current at 0 V	4, 5	4, 5	–10	–	0	µA
Data/Clock/Enable Current at 5.0 V	4, 5	4, 5	0	–	1.0	µA
Data/Clock/Enable Input Voltage Low	4, 5	4, 5	–	–	1.5	V
Data/Clock/Enable Input Voltage High	4, 5	4, 5	3.0	–	–	V
Clock Frequency Range	5	5	–	–	100	kHz
Oscillator Frequency Range	2, 3	2, 3	3.15	3.2	4.05	MHz
Operational Amplifier Input Current	1	1	–15	0	15	nA
Phase Detector Current in High Impedance State	1	1	–15	0	15	nA
Charge Pump Current of Phase Comparator, T_{14} = 0	1	1	30	40	60	µA
Charge Pump Current of Phase Comparator, T_{14} = 1	1	1	100	125	200	µA

HF CHARACTERISTICS (See Figure 1)

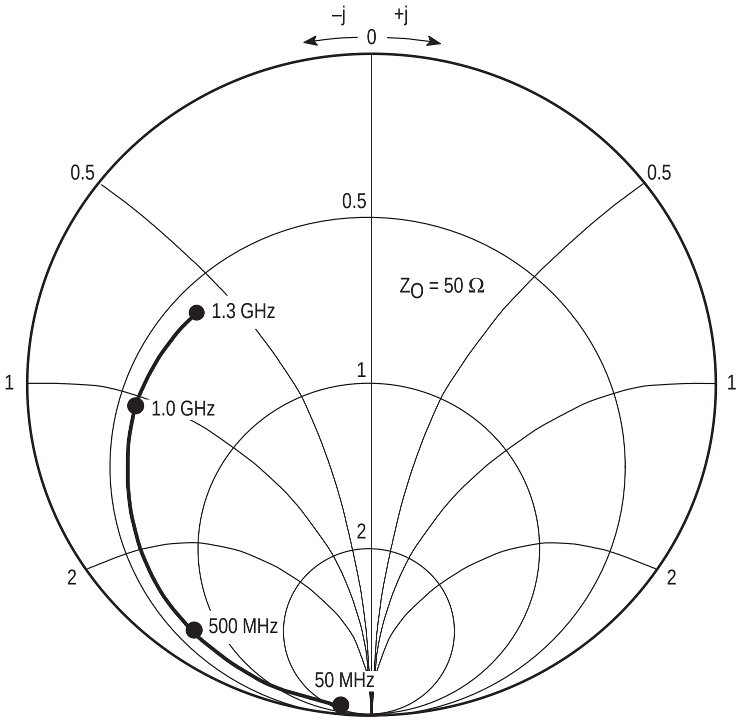
Characteristic	Pin MC44824	Pin MC44825	Min	Typ	Max	Unit
DC Bias	11, 12	13, 14	–	1.6	–	V
Input Voltage Range						mVrms
80–150 MHz	11, 12	13, 14	10	–	315	
150–600 MHz	11, 12	13, 14	5.0	–	315	
600–950 MHz	11, 12	13, 14	10	–	315	
950–1300 MHz	11, 12	13, 14	50	–	315	

Figure 1. HF Sensitivity Test Circuit



Device is in test mode. B_2 and B_7 are “On”.
Sensitivity is level of HF generator on 50 Ω load.

Figure 2. Typical HF Input Impedance



Data Format and Bus Receiver

The circuit receives the information for tuning and control via the I^{2}C bus. The incoming information, consisting of a chip address byte followed by two or four data bytes, is treated in the I^{2}C bus receiver. The definition of the permissible bus protocol is shown below:

1_STA CA CO BA STO
2_STA CA FM FL STO
3_STA CA CO BA FM FL STO
4_STA CA FM FL CO BA STO

STA = Start Condition
STO = Stop Condition
CA = Chip Address Byte
CO = Data Byte for Control Information
BA = Band Information
FM = Data Byte for Frequency Information (MSB’s)
FL = Data Byte for Frequency Information (LSB’s)

Figure 3. Complete Data Transfer Process

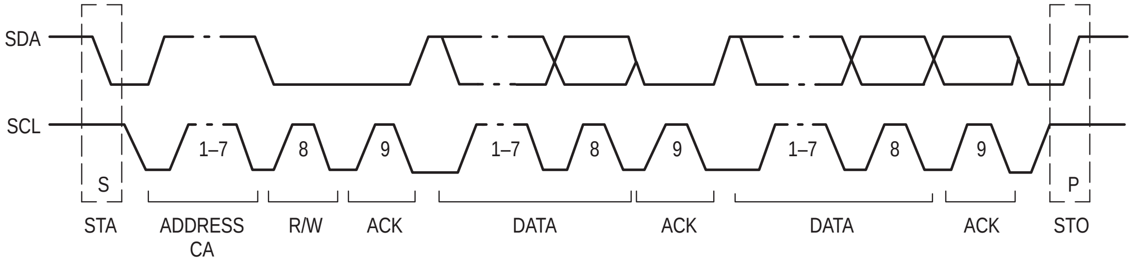


Figure 4 shows the five bytes of information that are needed for circuit operation: there is the chip address, two bytes of control and band information and two bytes of frequency information.

After the chip address, two or four data bytes may be received: if three data bytes are received, the third data byte is ignored.

If five or more data bytes are received, the fifth and following data bytes are ignored and the last acknowledge pulse is sent at the end of the fourth data byte.

The first and the third data bytes contain a function bit which allows the IC to distinguish between frequency information and control plus band information.

Frequency information is preceded by a Logic “0”. If the function bit is Logic “1” the two following bytes contain control and band information. The first data byte, shifted after the chip address, may be byte CO or byte FM.

The two permissible bus protocols with five bytes are shown in Figure 4.

Figure 4. Definition of Bytes

CA_Chip Address	1	1	0	0	0	0/1	0/1	0	ACK
	▨	▨	▨	▨	▨	▨	▨	▨	▨
CO_Information	①	T_{14}	T_{13}	T_{12}	T_{11}	T_{10}	T_9	T_8	ACK
BA_Band Information	B_7	X	X	B_4*	X	B_2	B_1	B_0*	ACK
	▨	▨	▨	▨	▨	▨	▨	▨	▨
FM_Frequency Information	⓪	N_{14}	N_{13}	N_{12}	N_{11}	N_{10}	N_9	N_8	ACK
FL_Frequency Information	N_7	N_6	N_5	N_4	N_3	N_2	N_1	N_0	ACK

CA_Chip Address	1	1	0	0	0	0/1	0/1	0	ACK
	▨	▨	▨	▨	▨	▨	▨	▨	▨
FM_Frequency Information	⓪	N_{14}	N_{13}	N_{12}	N_{11}	N_{10}	N_9	N_8	ACK
FL_Frequency Information	N_7	N_6	N_5	N_4	N_3	N_2	N_1	N_0	ACK
	▨	▨	▨	▨	▨	▨	▨	▨	▨
CO_Information	①	T_{14}	T_{13}	T_{12}	T_{11}	T_{10}	T_9	T_8	ACK
BA_Band Information	B_7	X	X	B_4*	X	B_2	B_1	B_0*	ACK

* B_0 and B_4 are only available on MC44825. On MC44824 this data is random.

Chip Address

The chip address is programmable by Pin 7 (8), CA.

CA – Pin 7 (8)	Address (HEX.)
Gnd to 0.1 V_{CC1}	C0
Open or 0.2 V_{CC1} to 0.3 V_{CC1}	C2
0.4 V_{CC1} to 0.7 V_{CC1}	C4
0.8 V_{CC1} to 1.1 V_{CC1}	C6

Bits B_0, B_1, B_2, B_4, B_7: Control the Band Buffers

B_0, B_1, B_2, B_4, B_7 = 0	Buffer “Off”
= 1	Buffer “On”

Bit T_8: Controls the Output of the Operational Amplifier

T_8 = 0	Normal Operation Operational Amplifier Active
= 1	Output State of Operational Amplifier Switched “Off”, Output Pulls High Through an External Pull–Up Resistor

Bits T_9, T_{12}: Control the Phase Comparator

T_9	T_{12}	Function
1	0	Normal Operation
1	1	High Impedance
0	0	Upper Source “On” Only
0	1	Lower Source “On” Only

Bits T_{10}, T_{11}: Control the Reference Ratio

T_{10}	T_{11}	Division Ratio
0	0	512
0	1	1024
1	0	1024
1	1	512

Bit T_{13}: Switches the Internal Signals F_{ref} and F_{BY2} to the Band Buffer Outputs (Test)

$T_{13} = 0$	Normal Operation
$= 1$	Test Mode F_{ref} Output at B_7 F_{BY2} Output at B_2

Bits B_2 and B_7 have to be “Off”, $B_2 = B_7 = 0$ in the test mode.
F_{ref} is the reference frequency.
F_{BY2} is the output frequency of the programmable divider, divided by two.

Bit T_{14}: Controls the Charge Pump Current of the Phase Comparator

$T_{14} = 0$	Pump Current 40 µA Typical
$= 1$	Pump Current 125 µA Typical

The Band Buffers

BA_Band Information
MC44824 14 Pin version

B_7	X	X	X	X	B_2	B_1	X	ACK

MC44825 16 Pin version

B_7	X	X	B_4	X	B_2	B_1	B_0	ACK

The band buffers are open collector buffers and are active “low” at Bn = 1. They are designed for 10 mA with a typical “On” resistance of 160 Ω. These buffers are designed to withstand relative high output voltage in the “Off” state.

B_2 and B_7 buffers may also be used to output internal IC signals (reference frequency and programmable divider output frequency divided by 2) for test purposes.

The bit B_2 and/or B_7 have to be zero if the buffers are used for these additional functions.

The Programmable Divider

The programmable divider is a presettable down counter. When it has counted to zero it takes its required division ratio out of the latches B. Latches B are loaded from latches A by means of signal TDI which is synchronous to the programmable divider output signal.

Since latches A receive the data asynchronously with the programmable divider, this double latch scheme is needed to assure correct data transfer to the counter.

The division ratio definition is given by:
$N = 16384 \times N_{14} + 8192 \times N_{13} + \ldots + 4 \times N_2 + 2 \times N_1 + N_0$
Maximum Ratio 32767
Minimum Ratio 17

Where $N_0 \ldots N_{14}$ are the different bits for frequency information.

The counter may be used for any ratio between 17 and 32767 and reloads correctly as long as its output frequency does not exceed 1.0 MHz.

The data transfer between latches A and B (signal TDI) is also initiated by any start condition on the I^2C bus.

At power–on, the whole bus receiver is reset and the programmable divider is set to a counting ration of N = 256 or higher.

The first I^2C message must be sent only when the POWER ON RESET is completed.

The Prescaler

The prescaler has a preamplifier which guarantees high input sensitivity.

The Phase Comparator

The phase comparator is phase and frequency sensitive and has very low output leakage current in the high impedance state.

The Tuning Voltage Amplifier

The amplifier is designed for very low noise, low input bias current and high power supply rejection. The positive input is biased internally. The tuning voltage amplifier needs an external NPN with a pull–up resistor to generate the tuning voltage.

The amplifier can be switched “Off” through bit T_8. When bit T_8 is “One”, the amplifier is “Off”. The tuning voltage is then pulled high by the external pull–up resistor.

Figure 5 shows a possible filter arrangement. The component values depend very much on the application (tuner characteristic, reference frequency, etc.).

As a starting point for optimization, the component values in Figure 5 may be used for 7.8125 kHz reference frequency in a multiband TV tuner.

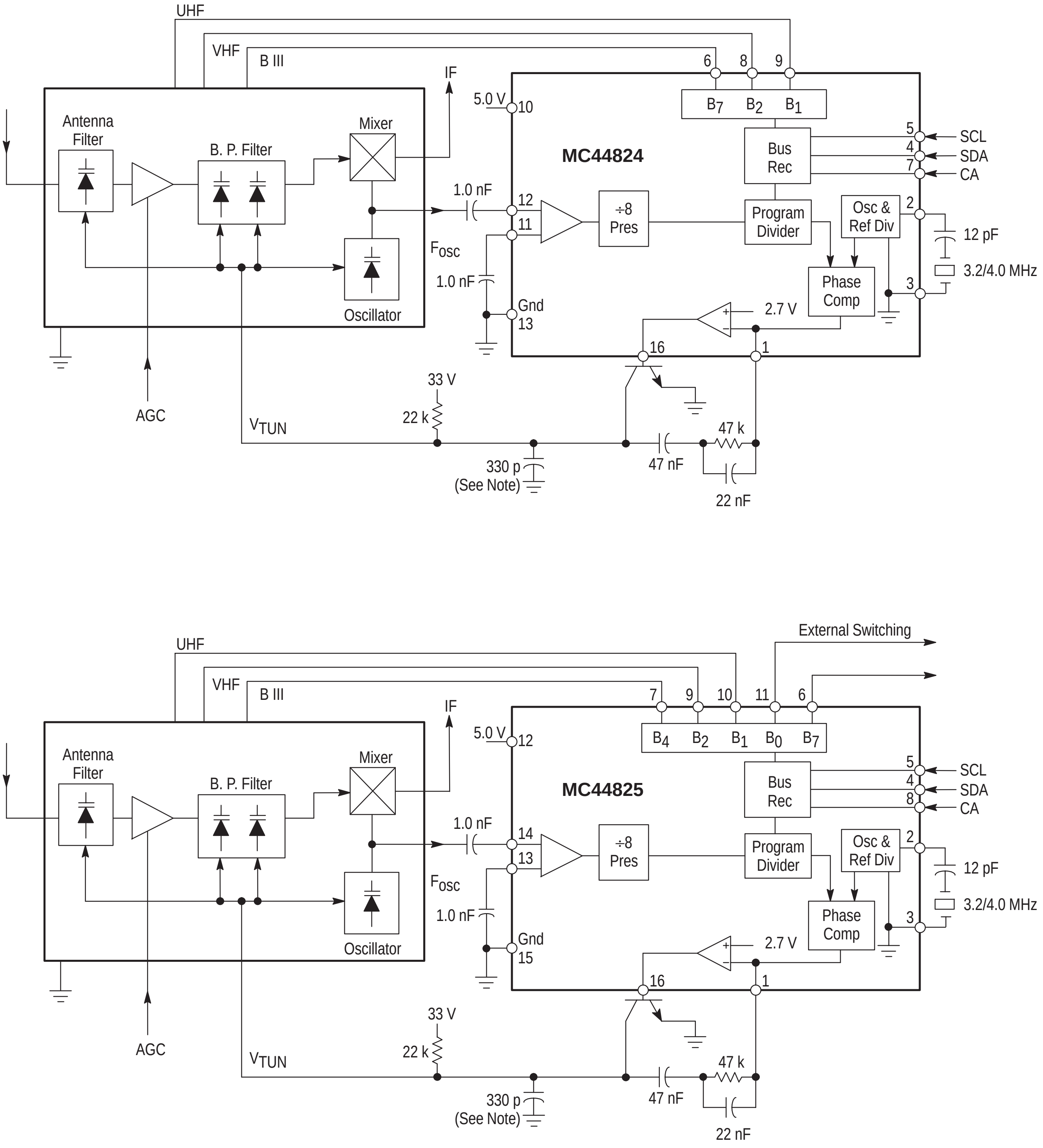
The Oscillator

The oscillator uses a 4.0 MHz crystal tied to ground “or between Pins 2 and 3” through a series capacitor. The crystal oscillates in its series resonance mode.

The voltage at Pin 13 XTAL1, has low amplitude and low harmonic distortion.

Pin XTAL2 is the internal ground of the oscillator; it is connected internally to ground Pin 13 (15).

Figure 5. Typical Tuner Applications



NOTE: C_2 = 330 pF minimum is required for stability.

MOTOROLA

MC44826

PLL Tuning Circuit with I^{2}C Bus

The MC44826 is a tuning circuit for TV and VCR tuner applications. It contains, on one chip, all the functions required for PLL control of a VCO. This integrated circuit also contains a high frequency prescaler and thus can handle frequencies up to 1.3 GHz. The circuit has a band decoder that provides the band switching signal for the mixer/oscillator circuit. The decoder is controlled by the buffer bits or independently by extra bits T_6 and T_7.

The MC44826 has a programmable 512/1024 reference divider and is manufactured on a single silicon chip using Motorola’s high density bipolar process, MOSAIC™ (Motorola Oxide Self Aligned Implanted Circuits).

- Complete Single Chip System for MPU Control (I^{2}C Bus)
- Divide–by–8 Prescaler Accepts Frequencies up to 1.3 GHz
- 15 Bit Programmable Divider
- Reference Divider: Programmable for Division Ratios 512 and 1024
- 3–State Phase/Frequency Comparator
- Operational Amplifier for Direct Tuning Voltage Output (30 V)
- Four Programmable Chip Addresses
- Integrated Band Decoder for the Mixer/Oscillator Circuit
- Band Buffers with Low “On” Voltage (0.4 V Maximum at 15 mA)
- Fully ESD Protected to MIL–STD–883C, Method 3015.7 (2000 V, 1.5 kΩ, 150 pF)

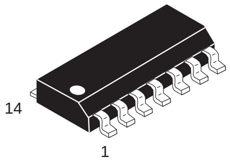
MOSAIC is a trademark of Motorola, Inc.

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC44826D	T_A = –20° to +80°C	SO–14

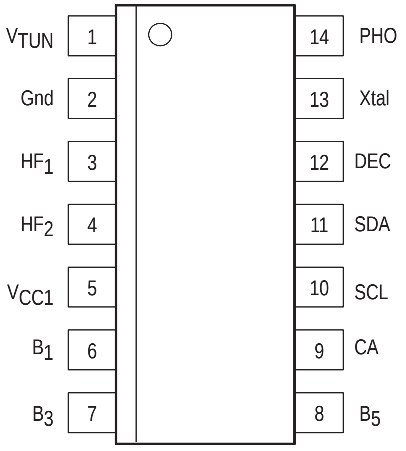
TV AND VCR I^{2}C PLL TUNING CIRCUIT WITH 1.3 GHz PRESCALER AND MIX/OSC DECODER

SEMICONDUCTOR
TECHNICAL DATA



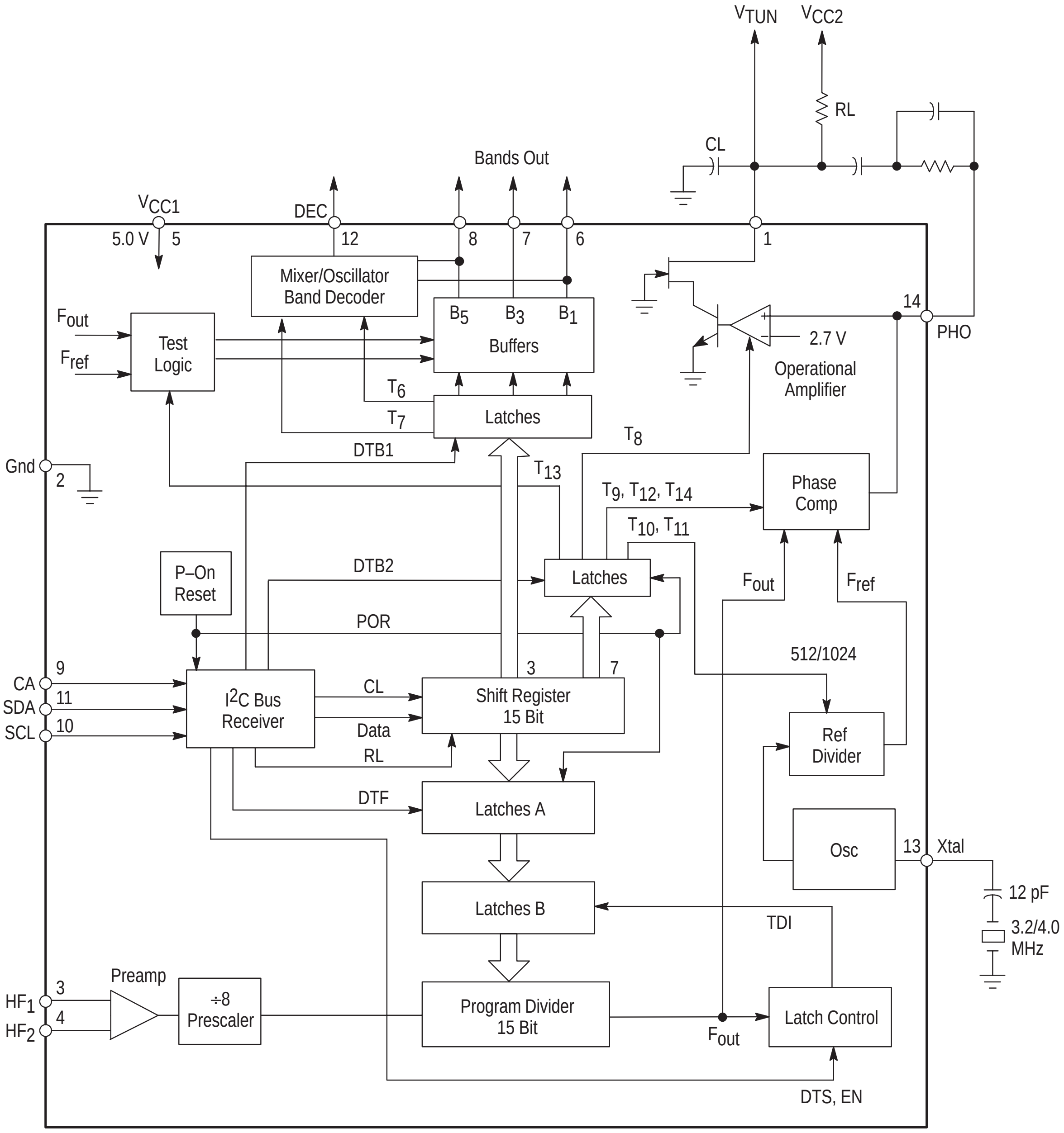
D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO–14)

PIN CONNECTIONS



(Top View)

Representative Block Diagram



This device contains 3,204 active transistors.

MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted.)

Rating	Pin	Value	Unit
Power Supply Voltage (V_{CC1})	5	6.0	V
Band Buffer “Off” Voltage	6, 7, 8	15	V
Band Buffer “On” Current	6, 7, 8	20	mA
Operational Amplifier Power Supply (V_{CC2})	1	40	V
RF Input Level 10 MHz to 1.3 GHz	3, 4	1.5	Vrms
Storage Temperature	–	–65 to +150	°C
Operating Temperature Range	–	–20 to +80	°C
Bus Input Voltage (Positive)	10, 11	7	V
Bus Input Voltage (Negative)	10, 11	–0.5	V

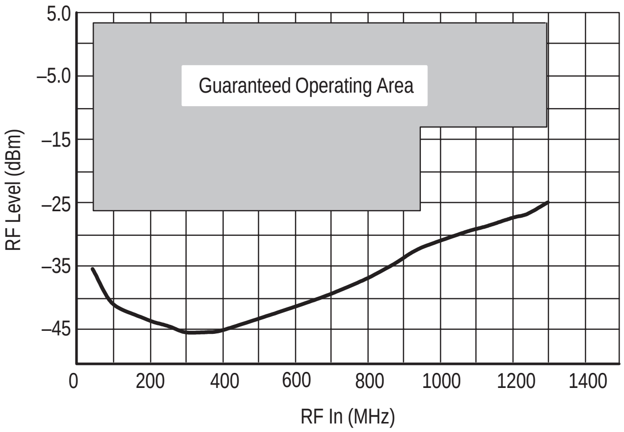
ELECTRICAL CHARACTERISTICS (V_{CC1} = 5.0 V, V_{CC2} = 33 V, T_A = 25°C, unless otherwise noted.)

Characteristic	Pin	Min	Typ	Max	Unit
V_{CC1} Supply Voltage Range	5	4.5	5.0	5.5	V
V_{CC1} Supply Current (V_{CC1} = 5.0 V)	5	25	35	50	mA
Band Buffer Leakage Current when “Off” at 12 V	6, 7, 8	–	0.01	1.0	µA
Band Buffer Saturation Voltage when “On” at 15 mA	6, 7, 8	–	0.2	0.4	V
Data/Clock Current at 0 V (Acknowledge “Off”)	10, 11	–10	–	0	µA
Data/Clock Current at 5.0 V (Acknowledge “Off”)	10, 11	0	–	1.0	µA
Data/Clock Input Voltage Low	10, 11	–	–	1.5	V
Data/Clock Input Voltage High	10, 11	3.0	–	–	V
Data Saturation Voltage at 3.0 mA (Acknowledge “On”)	11	–	0.25	0.4	V
Decoder “High” Level Sourcing 100 µA	12	3.4	–	V_{CC1}	V
Decoder “Medium” Level Sourcing 15 µA	12	1.7	–	2.3	V
Decoder “Low” Level Sinking 20 µA	12	0	–	0.8	V
Clock Frequency Range	10	–	–	100	kHz
Oscillator Frequency Range	13	3.15	3.2	4.05	MHz
Operational Amplifier Internal Reference Voltage	–	2.0	2.75	3.2	V
Operational Amplifier Input Current	14	–15	0	15	nA
DC Open Loop Gain (R_L = 22 kΩ)	14, 1	100	250	1000	V/V
Gain Bandwidth Product (C_L = 0.5 nF)	14, 1	0.3	–	–	MHz
V_{out} Low (R_L = 22 kΩ)	1	–	0.25	0.4	V
Phase Detector Current in High Impedance State	14	–15	0	15	nA
Charge Pump Current of Phase Comparator (T_{14} = 0)	14	30	40	50	µA
Charge Pump Current of Phase Comparator (T_{14} = 1)	14	90	125	150	µA
V_{CC2} Supply Voltage Range	1	25	33	36	V

PIN FUNCTION DESCRIPTION

Pin	Function	Description
1	V_{TUN}/V_{CC2}	Output of the tuning voltage amplifier. Needs an external pull–up resistor to drive the varicaps
2	Gnd	Ground
3, 4	HF_1/ HF_2	Symmetric HF inputs from local oscillator
5	V_{CC1}	Supply voltage. Typical 5.0 V
6, 7, 8	B_1, B_3, B_5	Band buffer outputs
9	CA	Chip address selection pin
10	SCL	Clock input of the I^2C bus
11	SDA	Data input
12	DEC	Band decoder output for the mixer/oscillator circuit
13	Xtal	Crystal input
14	PHO	Input of tuning voltage amplifier

Figure 1. Typical Prescaler Input Sensitivity

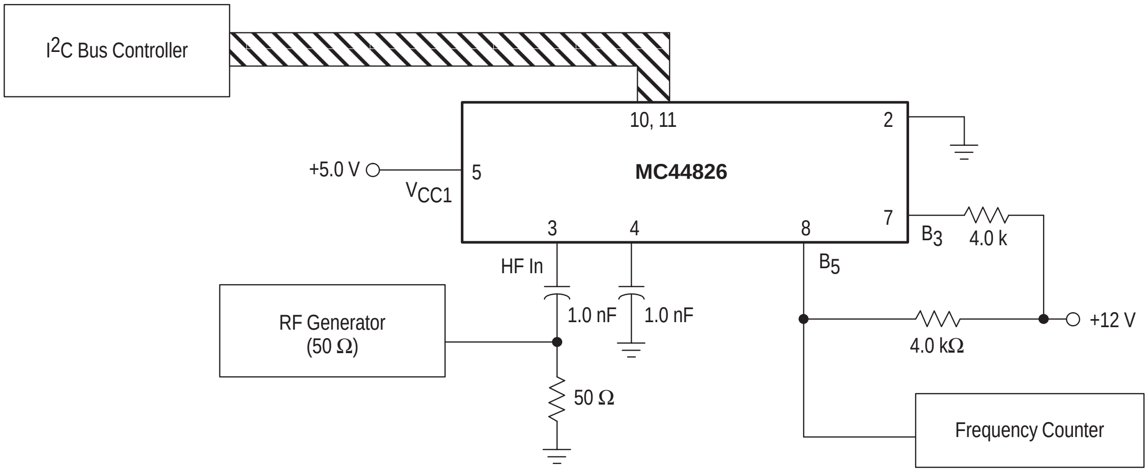


NOTE: V_{CC} = 4.5 to 5.5 V, T_A = – 20° to +80°C

HF CHARACTERISTICS (See Figure 1)

Characteristic	Pin	Min	Typ	Max	Unit
DC Bias	3, 4	–	1.6	–	V
Input Voltage Range					mVrms
50–950 MHz	3, 4	10	–	315	
950–1300 MHz	3, 4	50	–	315	

Figure 2. RF Sensitivity Test Circuit



Device is in test mode, B_5 and B_3 are “On”, B_1 is “Off”.
Sensitivity is the level of the HF generator on 50 Ω load.

Figure 3. Typical HF Input Impedance

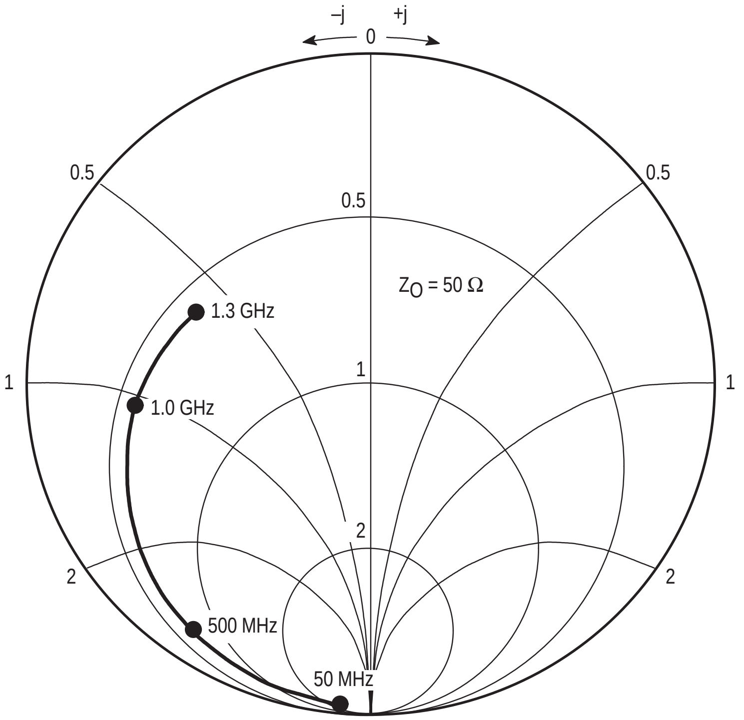
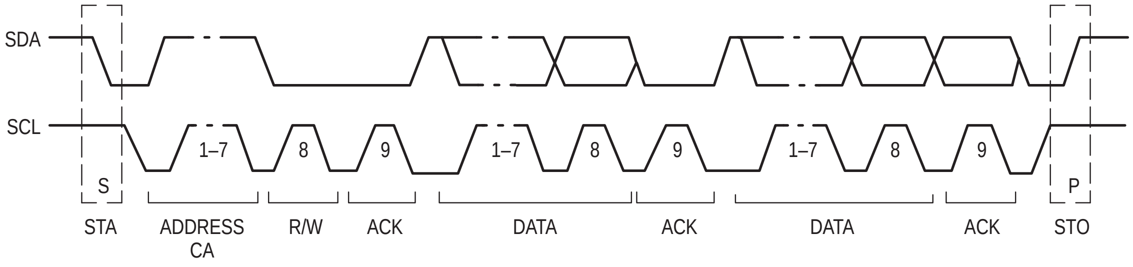


Figure 4. Complete Data Transfer Process



Data Format and Bus Receiver

The circuit receives the information for tuning and control via the I^{2}C bus. The incoming information, consisting of a chip address byte followed by two or four data bytes, is treated in the I^{2}C bus receiver. The definition of the permissible bus protocol is shown below:

1_STA CA CO BA STO
2_STA CA FM FL STO
3_STA CA CO BA FM FL STO
4_STA CA FM FL CO BA STO

STA = Start Condition
STO = Stop Condition
CA = Chip Address Byte
CO = Data Byte for Control Information
BA = Band Information
FM = Data Byte for Frequency Information (MSB's)
FL = Data Byte for Frequency Information (LSB's)

Figure 5 shows the five bytes of information that are needed for circuit operation: there is the chip address, two bytes of control and band information and two bytes of frequency information.

After the chip address, two or four data bytes may be received: if three data bytes are received the third data byte is ignored.

If five or more data bytes are received the fifth and following data bytes are ignored and the last acknowledge pulse is sent at the end of the fourth data byte.

The first and the third data bytes contain a function bit which allows the IC to distinguish between frequency information and control plus band information.

Frequency information is preceded by a Logic "0". If the function bit is Logic "1" the two following bytes contain control and band information. The first data byte, shifted after the chip address, may be byte CO or byte FM.

The two permissible bus protocols with five bytes are shown in Figure 5.

The Data and Clock inputs (Pins 10 and 11) are high impedance when the supply voltage V_{CC1} is between 0 and 5.5 V.

Chip Address

The chip address is programmable by Pin 9 (CA – Address Select).

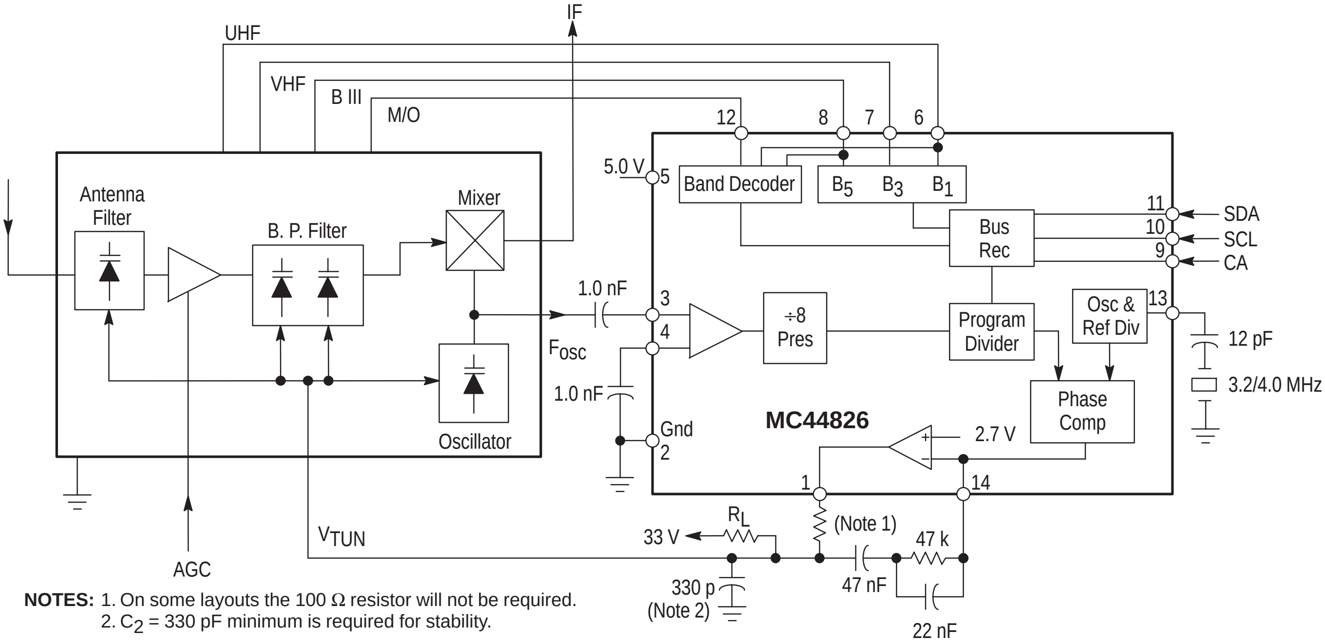
CA – Pin 9	Address (HEX.)
–0.04 V_{CC1} to 0.1 V_{CC1}	C6
Open or 0.2 V_{CC1} to 0.3 V_{CC1}	C4
0.42 V_{CC1} to 0.75 V_{CC1}	C2
0.9 V_{CC1} to 1.2 V_{CC1}	C0

Figure 5. Definition of Bytes

CA_Chip Address	1	1	0	0	0	0/1	0/1	0	ACK
	▨	▨	▨	▨	▨	▨	▨	▨	▨
CO_Information	①	T_{14}	T_{13}	T_{12}	T_{11}	T_{10}	T_9	T_8	ACK
BA_Band Information	T_7	T_6	B_5	X	B_3	X	B_1	X	ACK
	▨	▨	▨	▨	▨	▨	▨	▨	▨
FM_Frequency Information	⓪	N_{14}	N_{13}	N_{12}	N_{11}	N_{10}	N_9	N_8	ACK
FL_Frequency Information	N_7	N_6	N_5	N_4	N_3	N_2	N_1	N_0	ACK

CA_Chip Address	1	1	0	0	0	0/1	0/1	0	ACK
	▨	▨	▨	▨	▨	▨	▨	▨	▨
FM_Frequency Information	⓪	N_{14}	N_{13}	N_{12}	N_{11}	N_{10}	N_9	N_8	ACK
FL_Frequency Information	N_7	N_6	N_5	N_4	N_3	N_2	N_1	N_0	ACK
	▨	▨	▨	▨	▨	▨	▨	▨	▨
CO_Information	①	T_{14}	T_{13}	T_{12}	T_{11}	T_{10}	T_9	T_8	ACK
BA_Band Information	T_7	T_6	B_5	X	B_3	X	B_1	X	ACK

Figure 6. Typical Tuner Application



NOTES: 1. On some layouts the 100 Ω resistor will not be required.
2. C_2 = 330 pF minimum is required for stability.

Bits B_1, B_3, B_5: Control the Band Buffers

B_1, B_3, B_5 = 0 = 1	Buffer "Off" Buffer "On"

Bit T_8: Controls the Output of the Operational Amplifier

T_8 = 0	Normal Operation Operational Amplifier Active
= 1	Output State of Operational Amplifier Switched "Off", Output Pulls High Through the External Pull–Up Resistor R_L

Bits T_9, T_{12}: Control the Phase Comparator

T_9	T_{12}	Function
1	0	Normal Operation
1	1	High Impedance
0	0	Upper Source "On" Only
0	1	Lower Source "On" Only

Bits T_{10}, T_{11}: Control the Reference Divider

T_{10}	T_{11}	Division Ratio
0	0	512
0	1	1024
1	0	1024
1	1	512

Bit T_{13}: Switches the Internal Signals F_{ref} and F_{BY2} to the Band Buffer Outputs (Test)

T_{13} = 0	Normal Operation
= 1	Test Mode F_{ref} Output at B_3 (Pin 7) F_{BY2} Output at B_5 (Pin 8)

Bits B_3 and B_5 have to be "On", $B_3 = B_5 = 1$ in the test mode.
F_{ref} is the reference frequency.
F_{BY2} is the output frequency of the programmable divider, divided by two.

Bit T_{14}: Controls the Charge Pump Current of the Phase Comparator

T_{14} = 0	Pump Current 40 µA Typical
= 1	Normal Operation. Pump Current 125 µA Typical

Bits T_6, T_7: Mixer/Oscillator Band Decoder

The band decoder provides the band switching signal for the mixer/oscillator circuit. The buffer bits control the decoder output. The decoder can be controlled by the buffer bits or independently by the control bits T_6 and T_7 as per the tables below.

T_7	T_6	Decoder Output DEC
0	0	Decoder Output Controlled by Buffer Bits B_1, B_3, B_5
0	1	0 to 0.8 V
1	0	1.8 to 2.1 V
1	1	3.4 V to V_{CC1} (V_{CC1} = 4.5 to 5.5 V)

B_5	B_3	B_1	Decoder Output DEC
0	X	0	1.8 to 2.1 V
0	X	1	0 to 0.8 V
1	X	0	3.4 V to V_{CC1} (V_{CC1} = 4.5 to 5.5 V)
1	X	1	Undefined

BA_Band Information

T_7	T_6	B_5	X	B_3	X	B_1	X	ACK

The band buffers are open collector buffers and are active "low" at Bn = 1. They are designed for 15 mA with a typical "On" voltage of 200 mV. These buffers are designed to withstand relative high output voltage in the "Off" state.

B_3 and B_5 buffers may also be used to output internal IC signals (reference frequency and programmable divider output frequency divided by 2) for test purposes.

The bit B_3 and/or B_5 have to be one if the buffers are used for these additional functions.

The Programmable Divider

The programmable divider is a presettable down counter. When it has counted to zero it takes its required division ratio out of the latches B. Latches B are loaded from latches A by means of signal TDI which is synchronous to the programmable divider output signal.

Since latches A receive the data asynchronously with the programmable divider, this double latch scheme is needed to assure correct data transfer to the counter.

The division ratio definition is given by:

$N = 16384 \times N_{14} + 8192 \times N_{13} + \ldots + 4 \times N_2 + 2 \times N_1 + N_0$

Maximum Ratio 32767

Minimum Ratio 256

Where $N_0 \ldots N_{14}$ are the different bits for frequency information.

The counter may be used for any ratio between 256 and 32767, and reloads correctly as long as its output frequency does not exceed 1.0 MHz.

The data transfer between latches A and B (signal TDI) is also initiated by any start condition on the I^2C bus.

At power–on the whole bus receiver is reset and the bit N_8 of the programmable divider is set to $N_8 = 1$. Thus the programmable divider starts with a division ratio of 256 or higher.

The first I^2C message must be sent only when the POWER ON RESET is completed. Division ratios of $N < 256$ are not allowed.

The Prescaler

The prescaler has a preamplifier which guarantees high input sensitivity.

The Phase Comparator

The phase comparator is phase and frequency sensitive and has very low output leakage current in the high impedance state.

The Tuning Voltage Amplifier

The amplifier is designed for very low noise, low input bias current and high power supply rejection. The positive input is biased internally. The tuning voltage amplifier needs an external pull–up resistor to generate the tuning voltage.

The amplifier can be switched "Off" through bit T_8. When bit T_8 is "One", the amplifier is "Off". The tuning voltage is then pulled high by the external pull–up resistor.

Figure 6 shows a possible filter arrangement. The component values depend very much on the application (tuner characteristic, reference frequency, etc.).

The Oscillator

The oscillator uses a 3.2 or 4.0 MHz crystal tied to ground in series with a capacitor. The crystal operates in its series resonance mode.

The voltage at Pin 13, has low amplitude and low harmonic distortion.

The negative impedance of the crystal input (Pin 13) is about 3.0 kΩ.

MOTOROLA

MC44827

Product Preview

PLL Tuning Circuit with 3-Wire Bus

The MC44827 is a tuning circuit for TV and VCR tuner applications. This device contains on one chip all the functions required for PLL control of a VCO. This integrated circuit also contains a high frequency prescaler and thus can handle frequencies up to 1.3 GHz.

The MC44827 is controlled by a 3–wire bus. It has the same function as the MC44828 which is I^{2}C bus controlled. The MC44827 and MC44828 can replace each other to allow conversion between 3–wire bus and I^{2}C bus control.

The MC44827 is manufactured on a single silicon chip using Motorola's high density bipolar process, MOSAIC™ (Motorola Oxide Self Aligned Implanted Circuits).

The MC44827 has the same features as MC44817 with the following differences:

- Lower Power Consumption, 200 mW Typical
- Improved Prescaler with Higher Margins for Sensitivity and Temperature Range. (A typical device is functional in a temperature range greater than –40 to 100°C.)
- Lock Detector with Push–Pull Output
- No Bypass of Divide–by–8 Prescaler
- TSSOP Package

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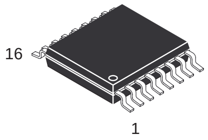
ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC44827DTB	T_J = –20 ° to +80°C	16 Pin TSSOP

PLL TUNING CIRCUIT WITH 1.3 GHz PRESCALER AND 3–WIRE BUS

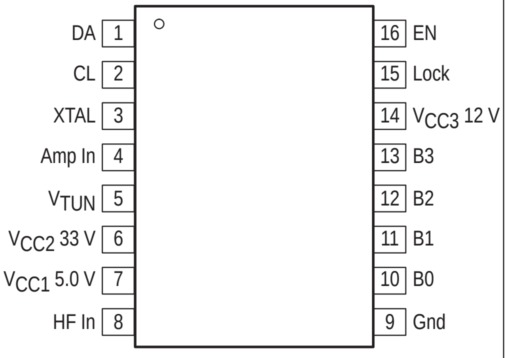
SEMICONDUCTOR TECHNICAL DATA



DTB SUFFIX
PLASTIC PACKAGE
CASE 948F
(TSSOP–16)

PIN CONNECTIONS

16 Pin TSSOP



(Top View)

MOTOROLA

MC44828

Product Preview

PLL Tuning Circuit with I^{2}C Bus

The MC44828 is a tuning circuit for TV and VCR tuner applications. This device contains on one chip all the functions required for PLL control of a VCO. This integrated circuit also contains a high frequency prescaler and thus can handle frequencies up to 1.3 GHz.

The MC44828 is controlled by an I^{2}C bus. It has the same function as the MC44827 which is 3–wire bus controlled. The MC44827 and MC44828 can replace each other to allow conversion between 3–wire bus and I^{2}C bus control.

The MC44828 is manufactured on a single silicon chip using Motorola's high density bipolar process, MOSAIC™ (Motorola Oxide Self Aligned Implanted Circuits).

The MC44828 has the same features as MC44818 with the following differences:

- Lower Power Consumption, 200 mW Typical
- Improved Prescaler with Higher Margins for Sensitivity and Temperature Range. (A typical device is functional in a temperature range greater than –40 to 100°C.)
- Lock Detector with Push–Pull Output
- TSSOP Package

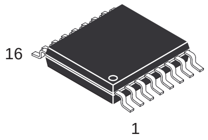
MOSAIC is a trademark of Motorola, Inc.

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC44828DTB	T_J = –20 ° to +80°C	16 Pin TSSOP

PLL TUNING CIRCUIT WITH 1.3 GHz PRESCALER AND I^{2}C BUS

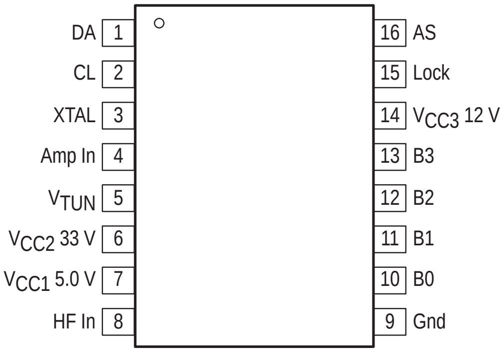
SEMICONDUCTOR
TECHNICAL DATA



DTB SUFFIX
PLASTIC PACKAGE
CASE 948F
(TSSOP–16)

PIN CONNECTIONS

16 Pin TSSOP



(Top View)

MOTOROLA

MC44829

PLL Tuning Circuit with I^{2}C Bus

The MC44829 is a tuning circuit for TV and VCR tuner applications. It contains, on one chip, all the functions required for PLL control of a VCO. This integrated circuit also contains a high frequency prescaler and thus can handle frequencies up to 1.3 GHz. The circuit has a band decoder that provides the band switching signal for the mixer/oscillator circuit. The decoder is controlled by the buffer bits.

The MC44829 has programmable 512/1024 reference dividers and is manufactured on a single silicon chip using Motorola’s high density bipolar process, MOSAIC™ (Motorola Oxide Self Aligned Implanted Circuits).

- Complete Single Chip System for MPU Control (I^{2}C Bus)
- Divide–by–8 Prescaler Accepts Frequencies up to 1.3 GHz
- 15 Bit Programmable Divider
- Reference Divider: Programmable for Division Ratios 512 and 1024
- 3–State Phase/Frequency Comparator
- Operational Amplifier for Direct Tuning Voltage Output (30 V)
- Four Programmable Chip Addresses
- Integrated Band Decoder for the Mixer/Oscillator Circuit
- Band Buffers with Low “On” Voltage (0.4 V Maximum at 5.0 mA)
- Fully ESD Protected to MIL–STD–883C, Method 3015.7 (2000 V, 1.5 kΩ, 150 pF)

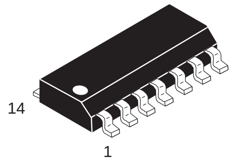
MOSAIC is a trademark of Motorola, Inc.

MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted.)

Rating	Pin	Value	Unit
Power Supply Voltage (V_{CC1})	5	6.0	V
Band Buffer “Off” Voltage	6, 7, 8	15	V
Band Buffer “On” Current	6, 7, 8	10	mA
Operational Amplifier Power Supply (V_{CC2})	1	40	V
RF Input Level 10 MHz to 1.3 GHz	3, 4	1.5	Vrms
Storage Temperature	–	–65 to +150	°C
Operating Temperature Range	–	–20 to +80	°C
Bus Input Voltage (Positive)	10, 11	7.0	V
Bus Input Voltage (Negative)	10, 11	–0.5	V

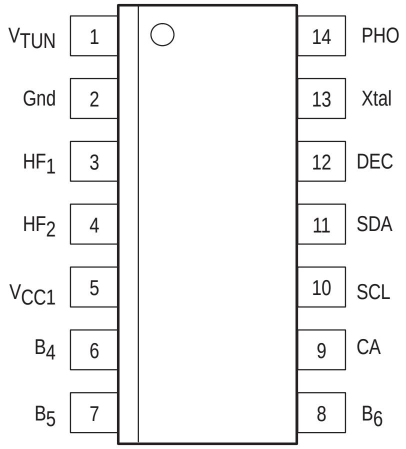
TV AND VCR I^{2}C PLL TUNING CIRCUIT WITH 1.3 GHz PRESCALER AND MIX/OSC DECODER

SEMICONDUCTOR TECHNICAL DATA



D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO–14)

PIN CONNECTIONS

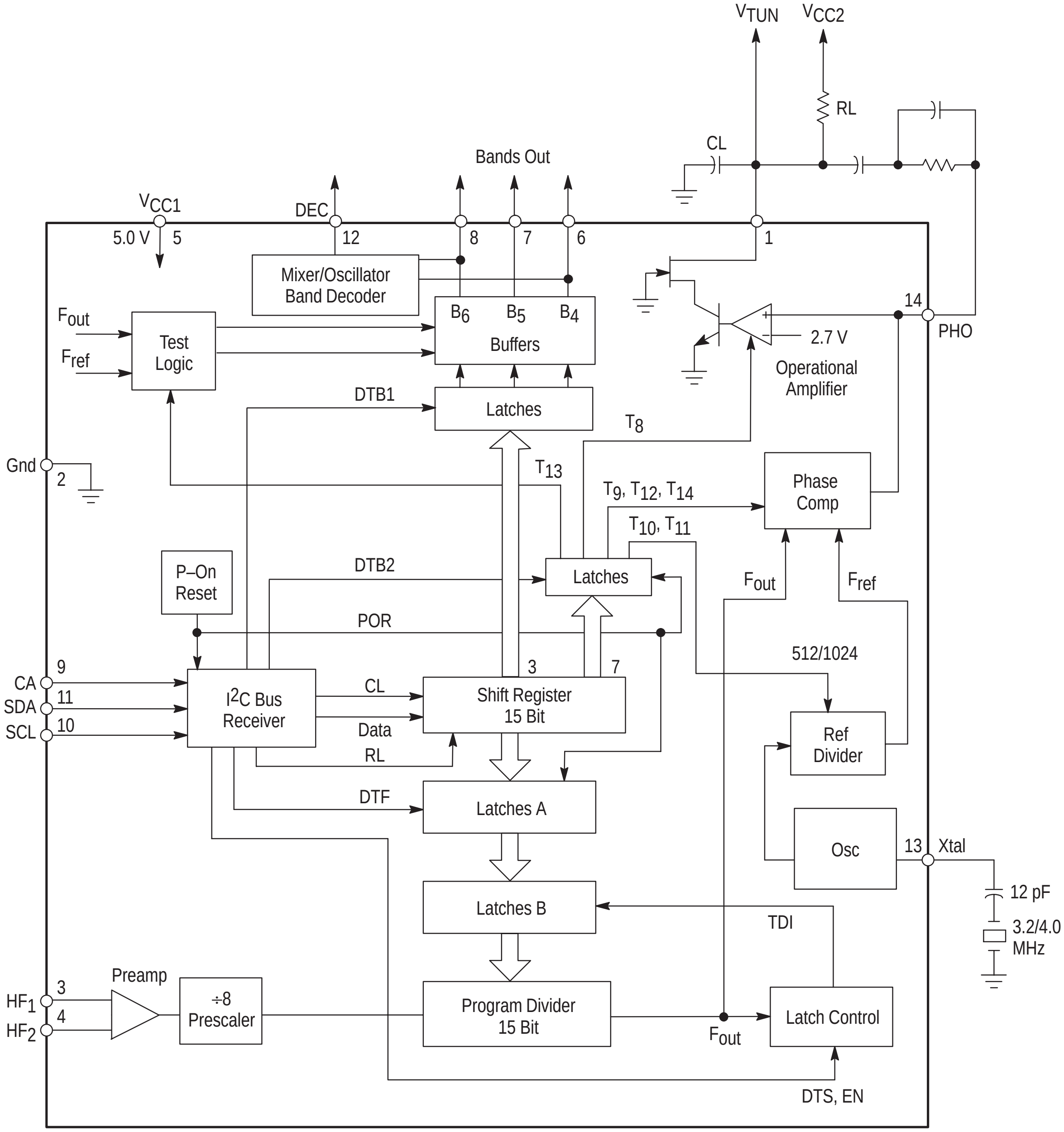


(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC44829D	T_A = –20° to +80°C	SO–14

Representative Block Diagram



This device contains 3,204 active transistors.

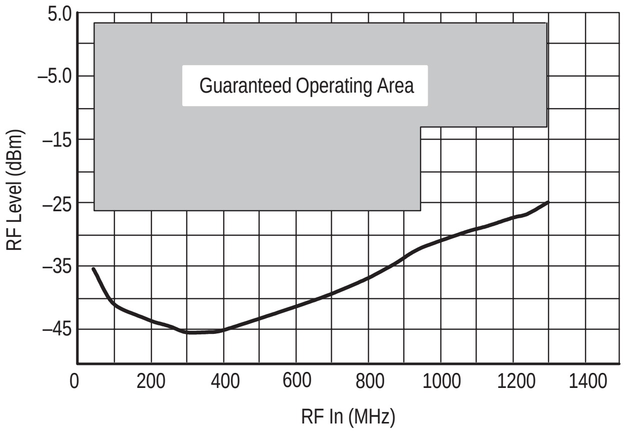
ELECTRICAL CHARACTERISTICS (V_{CC1} = 5.0 V, V_{CC2} = 33 V, T_A = 25°C, unless otherwise noted.)

Characteristic	Pin	Min	Typ	Max	Unit
V_{CC1} Supply Voltage Range	5	4.5	5.0	5.5	V
V_{CC1} Supply Current (V_{CC1} = 5.0 V)	5	25	35	50	mA
Band Buffer Leakage Current when “Off” at 12 V	6, 7, 8	–	0.01	1.0	µA
Band Buffer Saturation Voltage when “On” at 5.0 mA	6, 7, 8	–	0.16	0.4	V
Data/Clock Current at 0 V (Acknowledge “Off”)	10, 11	–10	–	0	µA
Data/Clock Current at 5.0 V (Acknowledge “Off”)	10, 11	0	–	1.0	µA
Data/Clock Input Voltage Low	10, 11	–	–	1.5	V
Data/Clock Input Voltage High	10, 11	3.0	–	–	V
Data Saturation Voltage at 3.0 mA (Acknowledge “On”)	11	–	0.25	0.4	V
Decoder “High” Level Sourcing 100 µA	12	3.4	–	V_{CC1}	V
Decoder “Medium” Level Sourcing 15 µA	12	1.8	–	2.1	V
Decoder “Low” Level Sinking 20 µA	12	0	–	0.8	V
Clock Frequency Range	10	–	–	100	kHz
Oscillator Frequency Range	13	3.15	3.2	4.05	MHz
Operational Amplifier Internal Reference Voltage	–	2.0	2.75	3.2	V
Operational Amplifier Input Current	14	–15	0	15	nA
DC Open Loop Gain (R_L = 22 kΩ)	14, 1	100	250	1000	V/V
Gain Bandwidth Product (C_L = 0.5 nF)	14, 1	0.3	–	–	MHz
V_{out} Low (R_L = 22 kΩ)	1	–	0.45	0.65	V
Phase Detector Tri–State Current	14	–15	0	15	nA
Charge Pump Current of Phase Comparator (T_{14} = 0)	14	30	40	50	µA
Charge Pump Current of Phase Comparator (T_{14} = 1)	14	90	125	150	µA
V_{CC2} Supply Voltage Range	1	25	33	36	V

PIN FUNCTION DESCRIPTION

Pin	Function	Description
1	V_{TUN}/V_{CC2}	Output of the tuning voltage amplifier. Needs an external pull–up resistor to drive the varicaps
2	Gnd	Ground
3, 4	HF_1/ HF_2	Symmetric HF inputs from local oscillator
5	V_{CC1}	Supply voltage. Typical 5.0 V
6, 7, 8	B_4, B_5, B_6	Band buffer outputs
9	CA	Chip address selection pin
10	SCL	Clock input of the I^2C bus
11	SDA	Data input
12	DEC	Band decoder output for the mixer/oscillator circuit
13	Xtal	Crystal input
14	PHO	Input of tuning voltage amplifier

Figure 1. Typical Prescaler Input Sensitivity

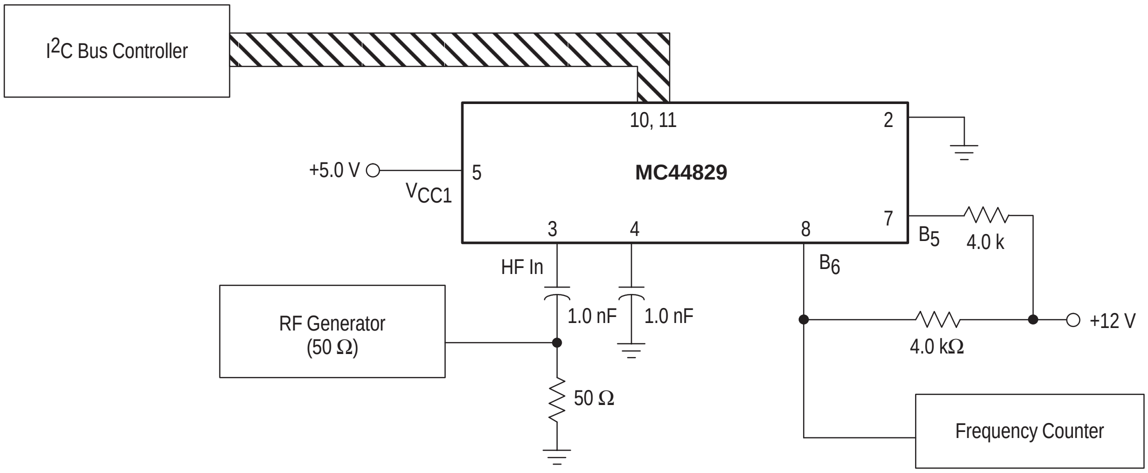


NOTE: V_{CC} = 4.5 to 5.5 V, T_A = – 20° to +80°C

HF CHARACTERISTICS (See Figure 1)

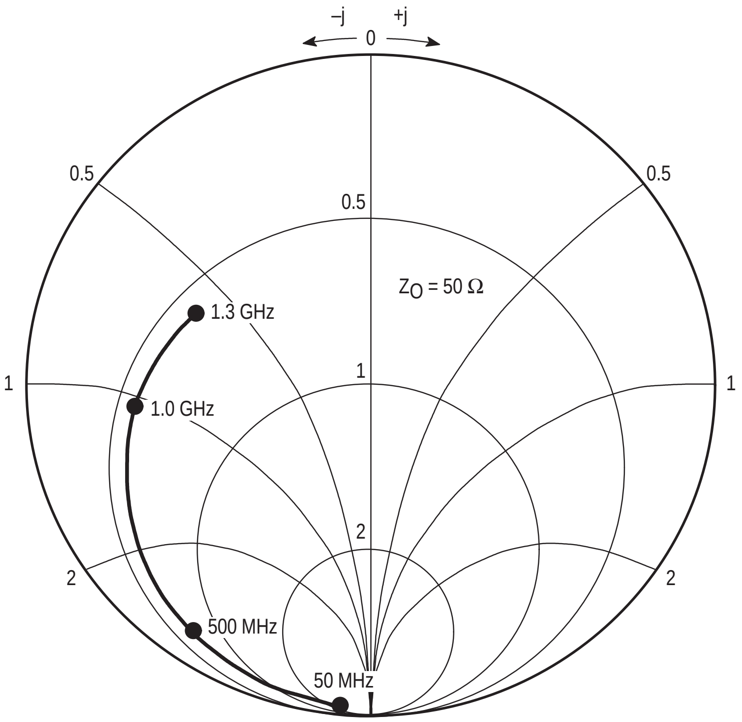
Characteristic	Pin	Min	Typ	Max	Unit
DC Bias	3, 4	–	1.6	–	V
Input Voltage Range					mVrms
50–950 MHz	3, 4	10	–	315	
950–1300 MHz	3, 4	50	–	315	

Figure 2. RF Sensitivity Test Circuit



Device is in test mode, B_5 and B_6 are "On", B_4 is "Off".
Sensitivity is the level of the HF generator of 50 Ω load.

Figure 3. Typical HF Input Impedance



Data Format and Bus Receiver

The circuit receives the information for tuning and control via the I^2C bus. The incoming information, consisting of a chip address byte followed by two or four data bytes, is treated in the I^2C bus receiver. The definition of the permissible bus protocol is shown below:

1_STA CA CO BA STO
2_STA CA FM FL STO
3_STA CA CO BA FM FL STO
4_STA CA FM FL CO BA STO

STA = Start Condition
STO = Stop Condition
CA = Chip Address Byte
CO = Data Byte for Control Information
BA = Band Information
FM = Data Byte for Frequency Information (MSB’s)
FL = Data Byte for Frequency Information (LSB’s)

Figure 4. Complete Data Transfer Process

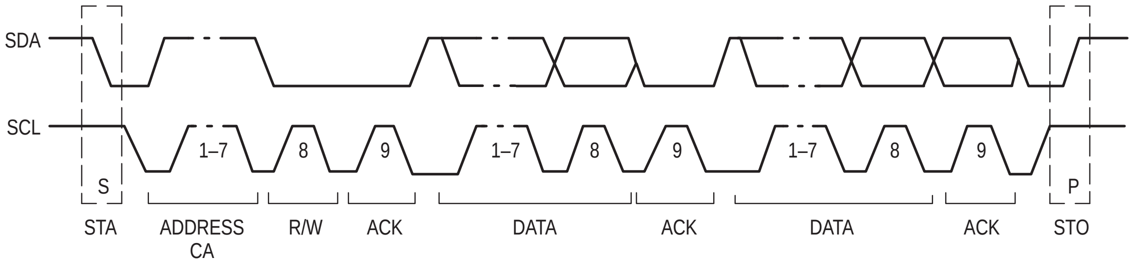


Figure 5 shows the five bytes of information that are needed for circuit operation: there is the chip address, two bytes of control and band information and two bytes of frequency information.

After the chip address, two or four data bytes may be received: if three data bytes are received the third data byte is ignored.

If five or more data bytes are received the fifth and following data bytes are ignored and the last acknowledge pulse is sent at the end of the fourth data byte.

The first and the third data bytes contain a function bit which allows the IC to distinguish between frequency information and control plus band information.

Frequency information is preceded by a Logic “0”. If the function bit is Logic “1” the two following bytes contain control and band information. The first data byte, shifted after the chip address, may be byte CO or byte FM.

The two permissible bus protocols with five bytes are shown in Figure 5.

The Data and Clock inputs (Pins 10 and 11) are high impedance when the supply voltage V_{CC1} is between 0 and 5.5 V.

Chip Address

The chip address is programmable by Pin 9 (CA – Address Select).

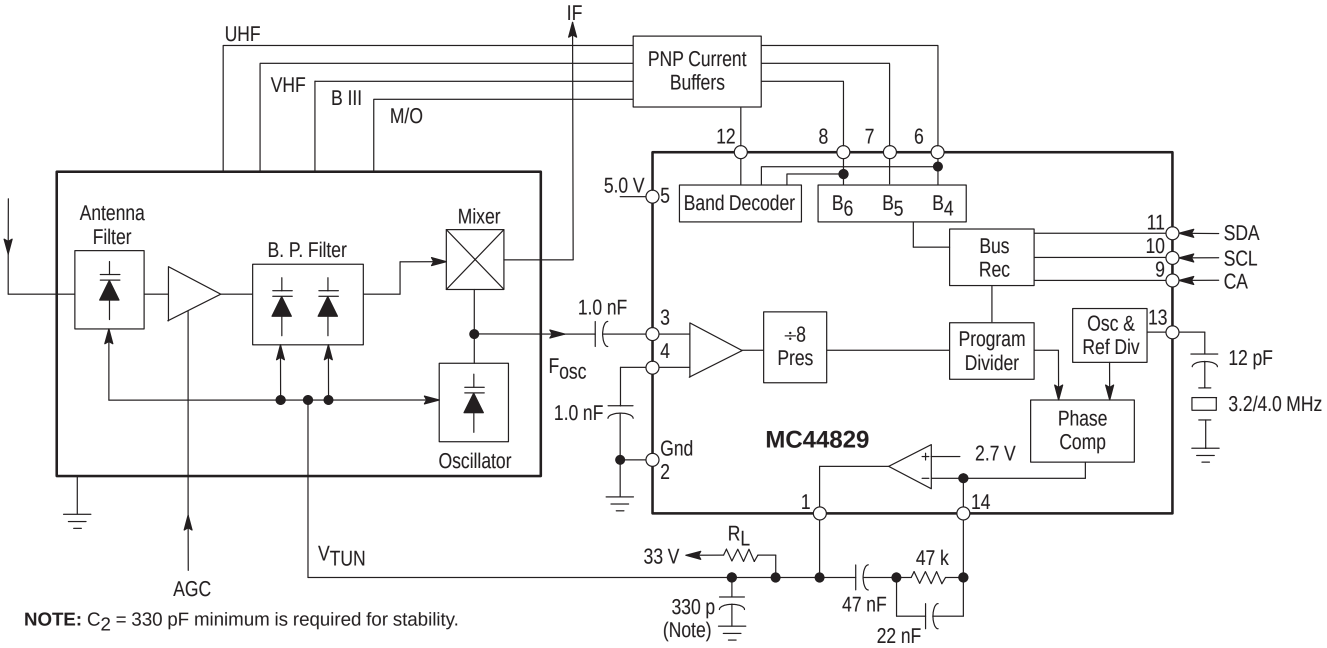
CA – Pin 9	Address (HEX.)
–0.04 V_{CC1} to 0.1 V_{CC1}	C_0
Open or 0.2 V_{CC1} to 0.3 V_{CC1}	C_2
0.42 V_{CC1} to 0.75 V_{CC1}	C_4
0.9 V_{CC1} to 1.2 V_{CC1}	C_6

Figure 5. Definition of Bytes

CA_Chip Address	1	1	0	0	0	0/1	0/1	0	ACK
	▨	▨	▨	▨	▨	▨	▨	▨	▨
CO_Information	①	T_{14}	T_{13}	T_{12}	T_{11}	T_{10}	T_9	T_8	ACK
BA_Band Information	X	B_6	B_5	B_4	X	X	X	X	ACK
	▨	▨	▨	▨	▨	▨	▨	▨	▨
FM_Frequency Information	⓪	N_{14}	N_{13}	N_{12}	N_{11}	N_{10}	N_9	N_8	ACK
FL_Frequency Information	N_7	N_6	N_5	N_4	N_3	N_2	N_1	N_0	ACK

CA_Chip Address	1	1	0	0	0	0/1	0/1	0	ACK
	▨	▨	▨	▨	▨	▨	▨	▨	▨
FM_Frequency Information	⓪	N_{14}	N_{13}	N_{12}	N_{11}	N_{10}	N_9	N_8	ACK
FL_Frequency Information	N_7	N_6	N_5	N_4	N_3	N_2	N_1	N_0	ACK
	▨	▨	▨	▨	▨	▨	▨	▨	▨
CO_Information	①	T_{14}	T_{13}	T_{12}	T_{11}	T_{10}	T_9	T_8	ACK
BA_Band Information	X	B_6	B_5	B_4	X	X	X	X	ACK

Figure 6. Typical Tuner Application



NOTE: C_2 = 330 pF minimum is required for stability.

Bits B_4, B_5, B_6: Control the Band Buffers

B_4, B_5, B_6 = 0	Buffer “Off”
= 1	Buffer “On”

Bit T_8: Controls the Output of the Operational Amplifier

T_8 = 0	Normal Operation Operational Amplifier Active
= 1	Output State of Operational Amplifier Switched “Off”, Output Pulls High Through the External Pull–Up Resistor R_L

Bits T_9, T_{12}: Control the Phase Comparator

T_9	T_{12}	Function
1	0	Normal Operation
1	1	High Impedance (Tri–State)
0	0	Upper Source “On” Only
0	1	Lower Source “On” Only

Bits T_{10}, T_{11}: Control the Reference Divider

T_{10}	T_{11}	Division Ratio
0	0	512
0	1	1024
1	0	1024
1	1	512

Bit T_{13}: Switches the Internal Signals F_{ref} and F_{BY2} to the Band Buffer Outputs (Test)

T_{13} = 0	Normal Operation
= 1	Test Mode F_{ref} Output at B_5 (Pin 7) F_{BY2} Output at B_6 (Pin 8)

Bits B_5 and B_6 have to be “On”, $B_5 = B_6 = 1$ in the test mode.
F_{ref} is the reference frequency.
F_{BY2} is the output frequency of the programmable divider, divided by two.

Bit T_{14}: Controls the Charge Pump Current of the Phase Comparator

T_{14} = 0	Pump Current 40 µA Typical
= 1	Normal Operation. Pump Current 125 µA Typical

Mixer/Oscillator Band Decoder

The band decoder provides the band switching signal for the mixer/oscillator circuit. The buffer bits B_4 and B_6 control the decoder output. B_5 is not decoded. The decoder is controlled by the buffer bits as per the table below.

B_6	B_5	B_4	Decoder Output DEC
0	X	0	Undefined
0	X	1	3.4 V to V_{CC1} (V_{CC1} = 4.5 to 5.5 V)
1	X	0	0 to 0.8 V
1	X	1	1.8 to 2.1 V

BA_Band Information

X	B_6	B_5	B_4	X	X	X	X	ACK

The band buffers are open collector buffers and are active “low” at Bn = 1. They are designed for 5.0 mA with a typical “on” voltage of 160 mV. These buffers are designed to withstand relative high output voltage in the “off” state.

B_5 and B_6 buffers may also be used to output internal IC signals (reference frequency and programmable divider output frequency divided by 2) for test purposes.

The bit B_5 and/or B_6 have to be one if the buffers are used for these additional functions.

The Programmable Divider

The programmable divider is a presettable down counter. When it has counted to zero it takes its required division ratio out of the latches B. Latches B are loaded from latches A by means of signal TDI which is synchronous to the programmable divider output signal.

Since latches A receive the data asynchronously with the programmable divider, this double latch scheme is needed to assure correct data transfer to the counter.

The division ratio definition is given by:

$N = 16384 \times N_{14} + 8132 \times N_{13} + \ldots + 4 \times N_2 + 2 \times N_1 + N_0$

Maximum Ratio 32767

Minimum Ratio 256

Where $N_0 \ldots N_{14}$ are the different bits for frequency information.

The counter may be used for any ratio between 256 and 32767 and reloads correctly as long as its output frequency does not exceed 1.0 MHz.

The data transfer between latches A and B (signal TDI) is also initiated by any start condition on the I^2C bus.

At power "on" the whole bus receiver is reset and the bit N_8 of the programmable divider is set to $N_8 = 1$. Thus the programmable divider starts with a division ratio of 256 or higher.

The first I^2C message must be sent only when the POWER ON RESET is completed. Division ratios of $N < 256$ are not allowed.

The Prescaler

The prescaler has a preamplifier which guarantees high input sensitivity.

The Phase Comparator

The phase comparator is phase and frequency sensitive and has very low output leakage current in the high impedance state.

The Tuning Voltage Amplifier

The amplifier is designed for very low noise, low input bias current and high power supply rejection. The positive input is biased internally. The tuning voltage amplifier needs an external pull–up resistor to generate the tuning voltage.

The amplifier can be switched "off" through bit T_8. When bit T_8 is "One", the amplifier is "Off". The tuning voltage is then pulled high by the external pull–up resistor.

Figure 6 shows a possible filter arrangement. The component values depend very much on the application (tuner characteristic, reference frequency, etc.).

The Oscillator

The oscillator uses a 3.2 or 4.0 MHz crystal tied to ground in series with a capacitor. The crystal operates in its series resonance mode.

The voltage at Pin 13, has low amplitude and low harmonic distortion.

The negative impedance of the crystal input (Pin 13) is about 3.0 kΩ.

MOTOROLA

Advance Information

PLL Tuning Circuit with 1.3 GHz Prescaler and D/A Converters for Automatic Tuner Alignment

The MC44864 is a tuning circuit for TV applications. This device contains a PLL section and a DAC section and is MCU controlled through an I^2C Bus.

The PLL section contains all the functions required to control the VCO of a TV tuner. The IC generates the tuning voltage and the additional control signals, such as band switching voltages.

The D/A section generates three additional varactor voltages to feed all of the varactors of the tuner with individually optimized control voltages (automatic tuner adjustment). The MC44864 is manufactured on a single silicon chip using Motorola's high density bipolar process, MOSIAC™ (Motorola Oxide Self–Aligned Implanted Circuits).

- Complete Single Chip System for MPU Control
- Selectable ÷8 Prescaler Accepts Frequencies up to 1.3 GHz
- 15 Bit Programmable Divider Accepts Input Frequencies up to 165 MHz
- Programmable Reference Divider
- 3–State Phase/Frequency Comparator
- Operational Amplifier for Direct Varactor Control with Low Saturation Voltage
- Four Output Buffers (15 mA)
- Output Options for 62.5 kHz, Reference Frequency and the Programmable Divider
- The HF Input is Symmetrical
- Three 6 Bit DACs for Automatic Tuner Adjustment Allowing Use of Non–Matched Varactors
- Better Tuner Performances Through Optimum Filter Response
- I^2C Bus Controlled
- Four Chip Addresses for the PLL Section
- Four Chip Addresses for the D/A Section
- ESD Protected to MIL–STD–883C, Method 3015.7 (2,000 V, 1.5 kΩ, 150 pF)

MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted.)

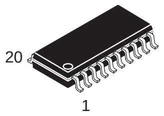
Rating	Pin	Value	Unit
Power Supply Voltage (V_{CC1})	9	6.0	V
Band Buffer "Off" Voltage	14 – 17	15	V
Band Buffer "On" Current	14 – 17	20	mA
Operational Amplifier Power Supply Voltage (V_{CC2})	4	36	V
Operational Amplifier Short Circuit Duration (0 to V_{CC2})	5 – 8	Continuous	S
Storage Temperature	–	–65 to +150	°C
Operating Temperature Range	–	0 to +70	°C

NOTE: ESD data available upon request.

MC44864

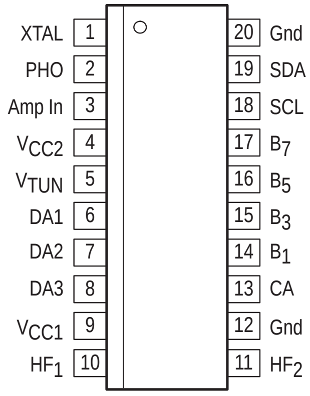
PLL TUNING CIRCUIT WITH 1.3 GHz PRESCALER AND D/A CONVERTERS

SEMICONDUCTOR TECHNICAL DATA



M SUFFIX
PLASTIC PACKAGE
CASE 967
(EIAJ–20)

PIN CONNECTIONS

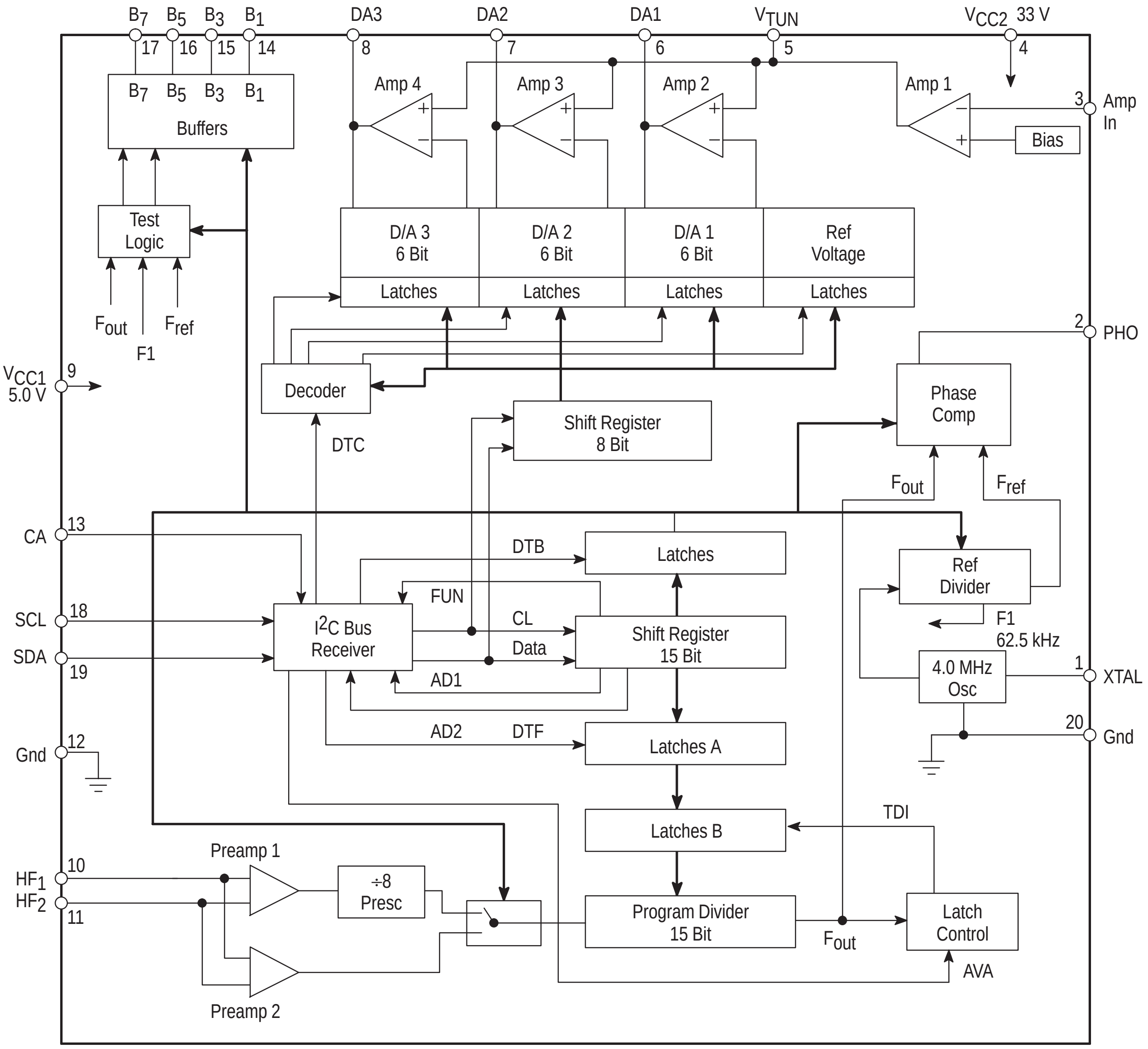


(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC44864M	T_A = 0° to +70°C	EIAJ–20

Representative Block Diagram



This device contains 3,551 active transistors.

ELECTRICAL CHARACTERISTICS (V_{CC1} = 5.0 V, V_{CC2} = 32 V, T_A = 25°C, unless otherwise noted.)

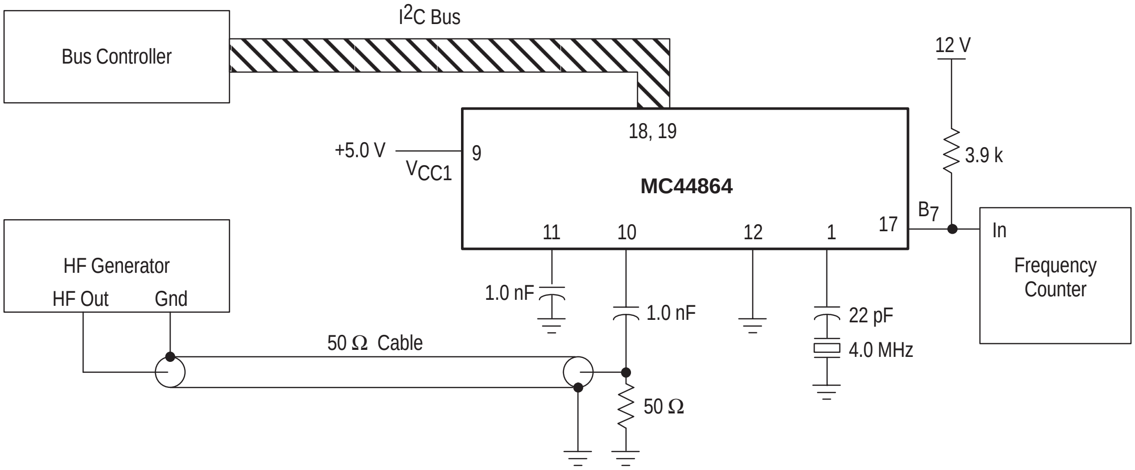
Characteristic	Pin	Min	Typ	Max	Unit
V_{CC1} Supply Voltage Range	9	4.5	5.0	5.5	V
V_{CC1} Supply Current (V_{CC1} = 5.0 V)(1)(2)	9	–	50	70	mA
V_{CC2} Supply Voltage Range	4	25	30	35	V
V_{CC2} Supply Current (Output Open)	4	–	1.3	2.5(4)	mA
Band Buffer Leakage Current when “Off” at 12 V	14 – 17	–	0.01	1.0	µA
Band Buffer Saturation Voltage when “On” at 15 mA	14 – 17	–	1.8	2.0	V
Data/Clock Current at 0 V	18, 19	–10	–	0	µA
Clock Current at 5.0 V	18	0	–	1.0	µA
Data Current at 5.0 V Acknowledge “Off”	19	0	–	1.0	µA
Data Saturation Voltage at 15 mA Acknowledge “On”	19	–	1.2	–	V
Data/Clock Input Voltage Low	18, 19	–	–	1.5	V
Data/Clock Input Voltage High	18, 19	3.0	–	–	V
Clock Frequency Range	18	–	–	100	kHz
Phase Detector Current in High Impedance State	2	–15	–	15	nA
Oscillator Frequency Range	1, 2	3.5	4.0	4.1	MHz
Phase Detector High–State Source Current (@ 1.5 V)	2	–2.5	–	–0.5	mA
Phase Detector Low–State Sink Current (@ 4.0 V)	2	0.5	–	2.5	mA
Operational Amplifier Internal Reference Voltage	–	2.0	2.5	3.0	V
Operational Amplifier Input Current	3	–15	–	15	nA
DC Open Loop Gain	–	2000	–	–	V/V
Gain Bandwidth Product	–	–	0.2	–	MHz
Phase Margin	–	–	50	–	Deg.
V_{out} Low, Sinking 50 µA	6 – 8	–	0.2	0.5	V
V_{out} High, Sourcing 50 µA (V_{CC2} – V_{out} High)	6 – 8	–	–	1.5	V
Tuning Voltage (DC)	5 – 8	–	–	30	V
D/A Converters Step Size(3)	6 – 8	0.5	–	1.5	LSB
D/A Converters Temperature Drift	6 – 8	–	1.0	–	LSB
DAC Offset at V_{TUN} = 2.5 V	–	–50	–	50	mV
DAC Offset at V_{TUN} = 25 V	–	–700	–	700	mV
DAC Voltages (DC)	6 – 8	–	–	33	V

NOTES:
1. When prescaler “Off”, typical supply current is decreased by 10 mA.
2. Band Buffers “Off”, 2.4 mA more when one buffer is on.
3. For definition of the LSB, see Figure 9 in the D/A section.
4. 2.5 mA as long as the analog outputs are not in saturation high, which means V_{TUN}, V_{DAC} (Pins 5, 6, 7, 8) lower than V_{CC2} – 1.5 V. When all outputs are in saturation high the maximum V_{CC2} current is 5.0 mA.

HF CHARACTERISTICS (See Figure 1)

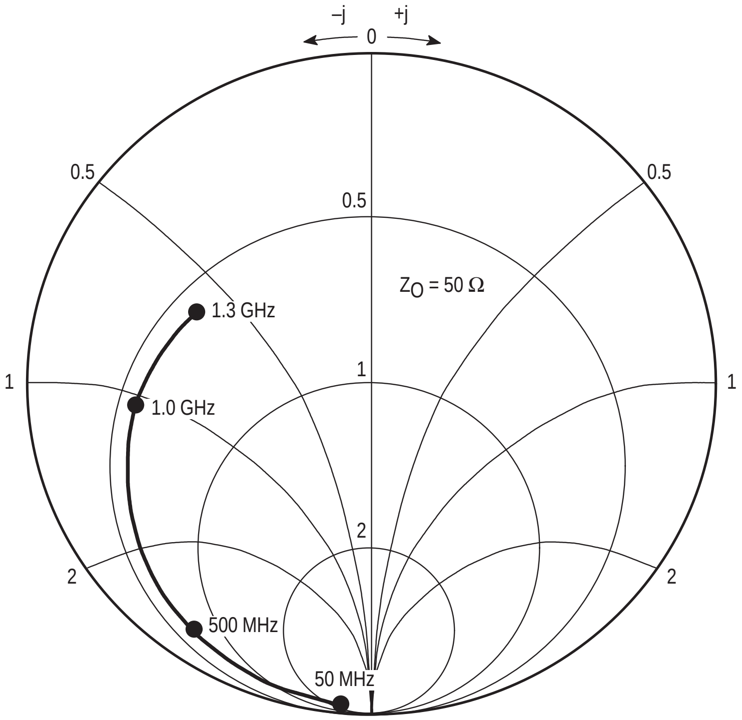
Characteristic	Pin	Min	Typ	Max	Unit
DC Bias	10, 11	–	1.55	–	V
Input Voltage Range					mVrms
10–150 MHz (Prescaler "Off")	10, 11	20	–	315	
80–1000 MHz	10, 11	20	–	315	
1000–1300 MHz	10, 11	50	–	315	

Figure 1. HF Sensitivity Test Circuit



Device is in test mode: B_7 is "On", R_2 = 1 and R_3 = 0 (see Bus section).
Sensitivity is the level of the HF generator on 50 Ω load (without MC44864 load).

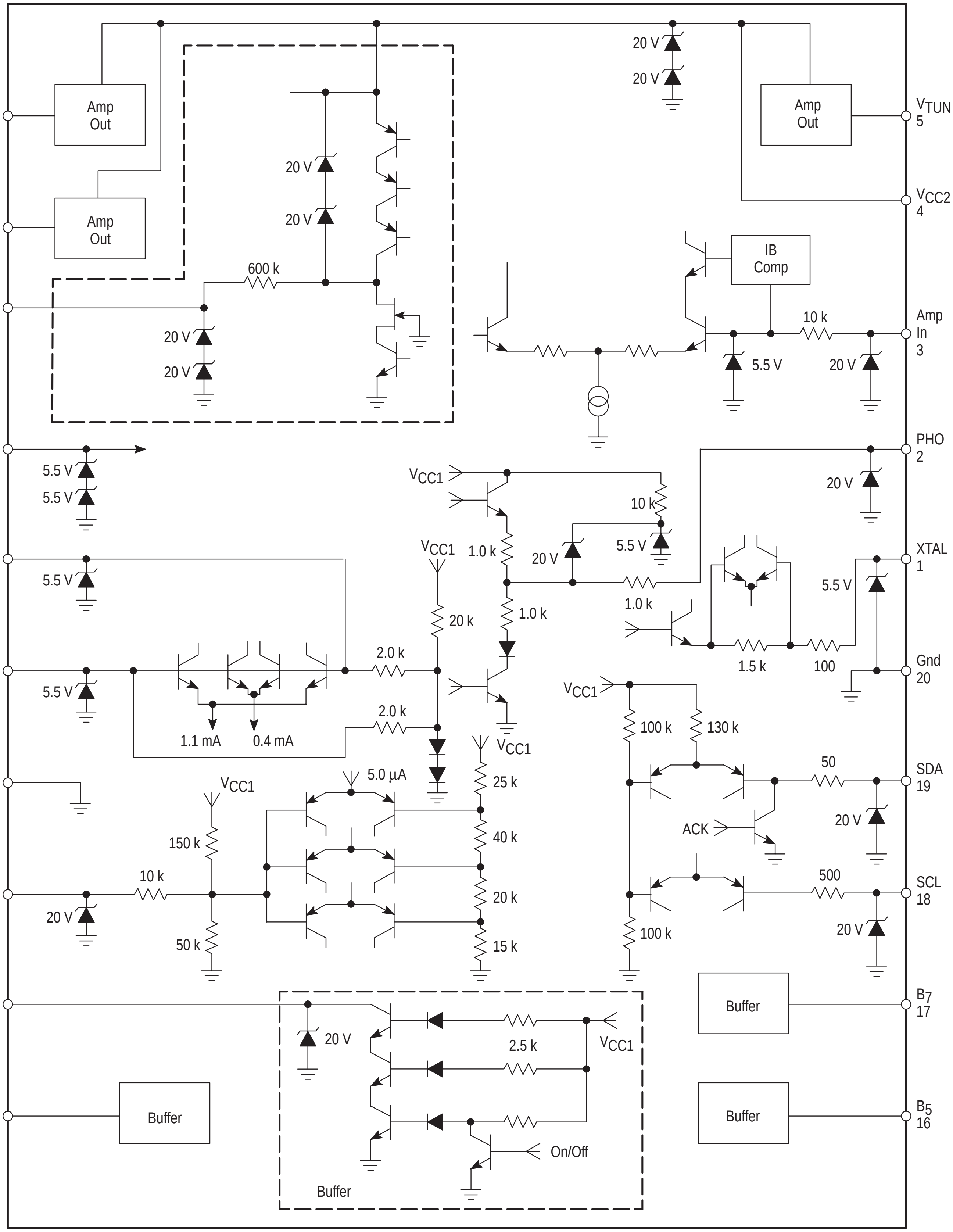
Figure 2. Typical HF Input Impedance



PIN FUNCTION DESCRIPTION

Pin	Symbol	Description
6, 7, 8	DA1, DA2, DA3	D/A output control voltages
9	V_{CC1}	Positive supply of the circuit (except DACs)
10, 11	HF_1, HF_2	HF input from local oscillator
12, 20	Gnd	Ground
13	CA	Chip Address
14, 15, 16, 17	B_1, B_3, B_5, B_7	Band buffer output can drive 15 mA
18	SCL	Clock input (supplied by the microprocessor via Bus)
19	SDA	Data input (bus)
1	XTAL	Crystal oscillator (typically 4.0 MHz)
2	PHO	Phase comparator output
3	Amp In	Negative operational amplifier input
4	V_{CC2}	Operational amplifier positive supply
5	V_{TUN}	Operational amplifier output which provides the tuning voltage

Figure 3. Pin Circuit Schematic



FUNCTIONAL DESCRIPTION

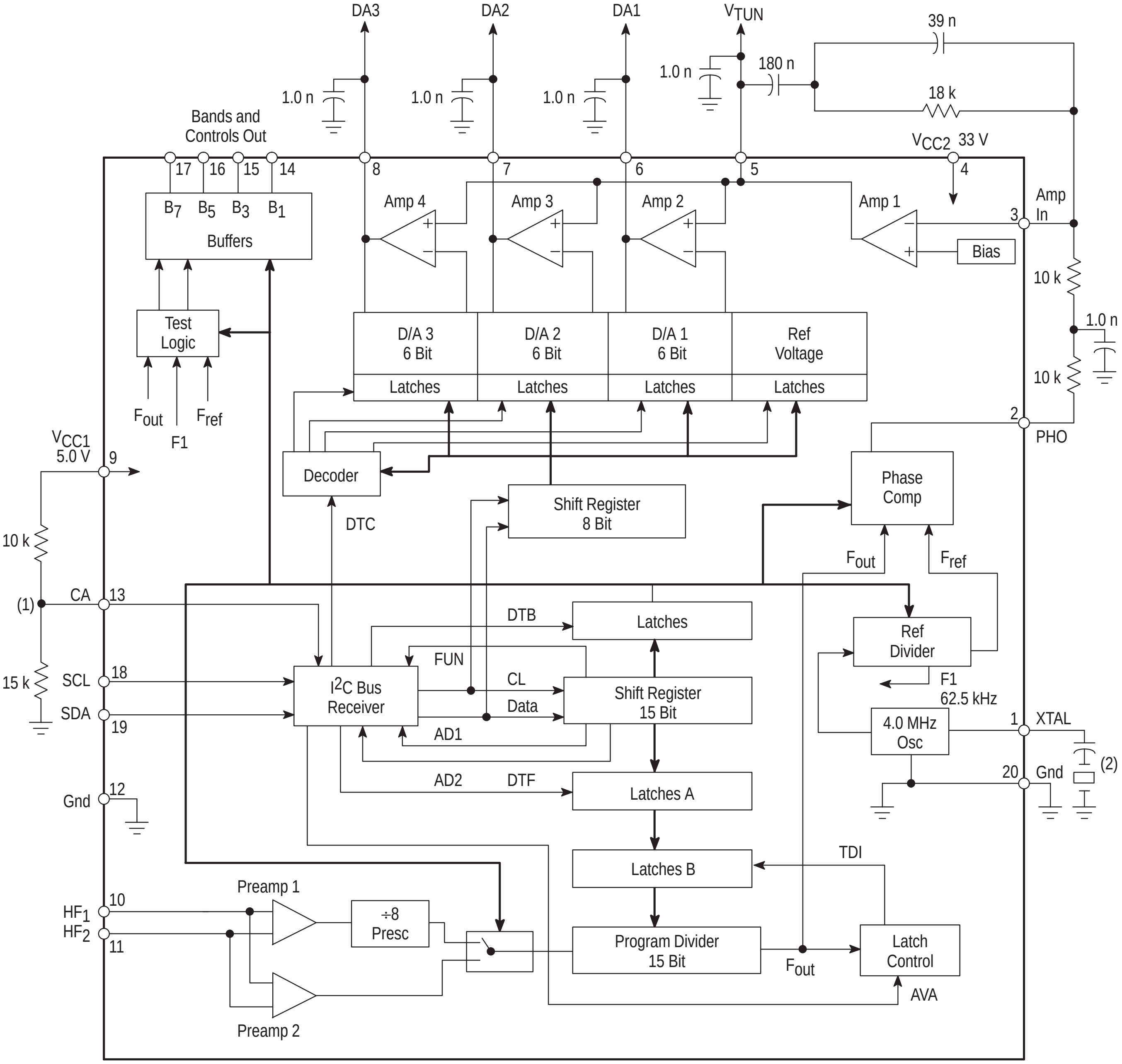
A representative block diagram and a typical system application are shown in Figures 4 and 5. A discussion of the features and function of the internal blocks is given below.

Automatic Tuner Alignment

The circuit generates the tuning voltage through the PLL. The output voltages of the D/A converters are equal to the tuning voltage plus a positive or negative offset of up to 31 steps. During the automatic alignment one first lets the PLL lock to the appropriate frequency and then searches for the optimum value of the other varactor voltages. The digital word for each voltage value is stored in a nonvolatile memory (NVM). Hence, for each frequency point to be adjusted, three times 6 bits of information have to be stored (plus 2 bits for the DAC range).

The information stored in the NVM reflects the characteristic of the individual tuner. For this reason, the NVM is preferably situated inside the tuner and is also controlled by the I^2C Bus.

Figure 4. Block Diagram



NOTES: 1. Pin 13:

Short to V_{CC}	for addresses CC, CE
Resistors ±10%	for addresses C8, CA (values 10 k and 15 k) for test only
Open or 1.0 nF to Gnd	for addresses C4, C6
Short to Gnd	for addresses C0, C2

2. The crystal may be connected to Pin 20 with no connection to external Gnd.

Figure 5. TV Tuner for Automatic Alignment

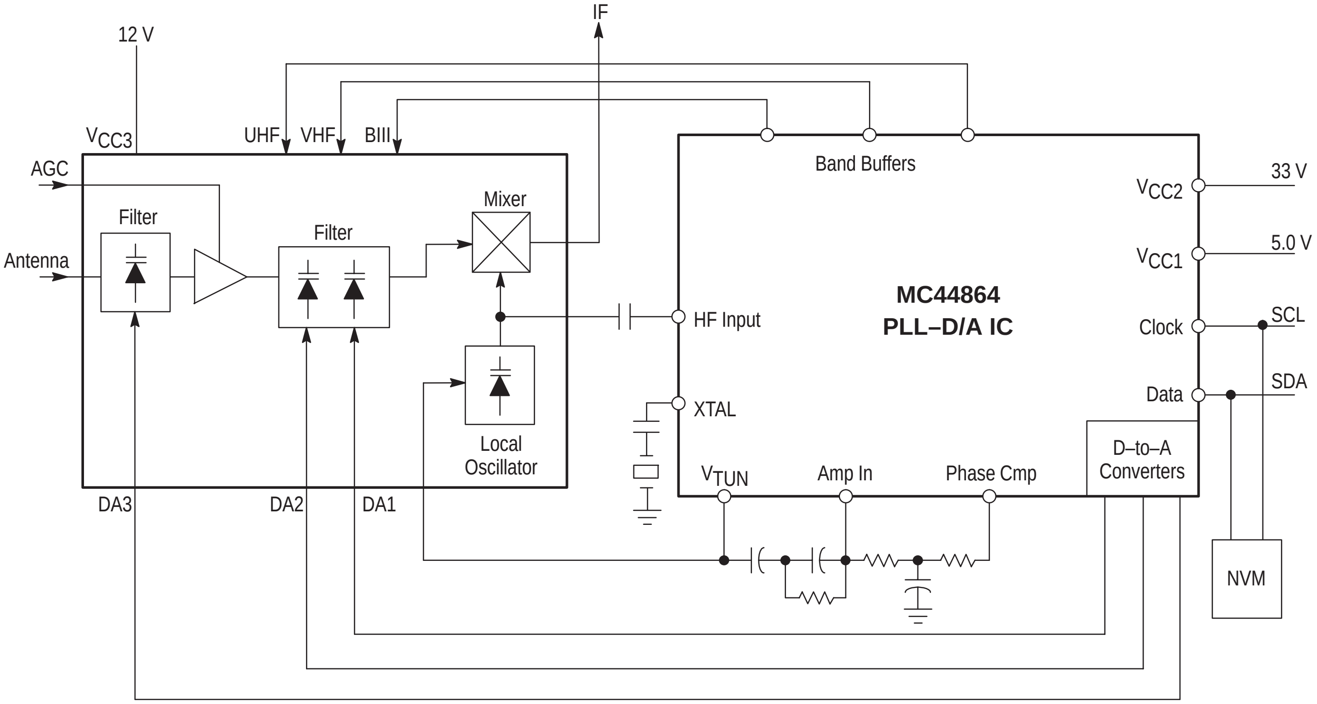


Figure 6. Definition of Bytes

CA1_PLL Chip Address	1	1	0	0	A_3	A_2	A_1	A_0 = 0	ACK
	▨	▨	▨	▨	▨	▨	▨	▨	▨
CO_Control Information	1	R_6	T	P	R_3	R_2	R_1	R_0	ACK
BA_Band Information	B_7	X	B_5	X	B_3	X	B_1	X	ACK
	▨	▨	▨	▨	▨	▨	▨	▨	▨
FM_Frequency Information (with MSB)	0	N_{14}	N_{13}	N_{12}	N_{11}	N_{10}	N_9	N_8	ACK
FL_Frequency Information (with LSB)	N_7	N_6	N_5	N_4	N_3	N_2	N_1	N_0	ACK

Chip Addresses

The chip address is programmable by Pin CA.

The PLL addresses C0, C2, C4, C6 are officially allocated to PLL–IC's.

The addresses C8, CA, CC, CE are not officially allocated. Care has to be taken in the application that no conflict occurs with other devices on the same I^2C Bus when using the addresses C8 to CE.

CA Pin (13)	A_3	A_2	A_1	A_0	Address	Function
–0.04 V_{CC1} to 0.1 V_{CC1}	0	0	0	0	C0	1st PLL
	0	0	1	0	C2	1st DAC
Open or 0.2 V_{CC1}to0.3V_{CC1}	0	1	0	0	C4	2nd PLL
	0	1	1	0	C6	2nd DAC
0.42 V_{CC1} to 0.75 V_{CC1}	1	0	0	0	C8	3rd PLL
	1	0	1	0	CA	3rd DAC
0.9 V_{CC1} to 1.2 V_{CC1}	1	1	0	0	CC	4th PLL
	1	1	1	0	CE	4th DAC

PLL SECTION

Data Format and Bus Receiver

The circuit receives the information for tuning and control via I^2C Bus. The incoming information is treated in the bus receiver. The definition of the permissible bus protocol is shown in the four examples below:

Ex. 1	STA	CA1	CO	BA	STO		
Ex. 2	STA	CA1	FM	FL	STO		
Ex. 3	STA	CA1	CO	BA	FM	FL	STO
Ex. 4	STA	CA1	FM	FL	CO	BA	STO

STA = Start Condition
STO = Stop Condition
CA1 = Chip Address Byte of the PLL Section
CO = Data Byte for Control Information
BA = Band Information
FM = Data Byte for Frequency Information (MSB's)
FL = Data Byte for Frequency Information (LSB's)

Figure 6 shows the five bytes of information that are needed for circuit operation: there is a chip address, two bytes of control and band information and two bytes of frequency information.

After the chip address, two or four data bytes may be received: if three data bytes are received, the third data byte is ignored. If five or more data bytes are received, the fifth and following data bytes are ignored and the last acknowledge pulse is sent at the end of the fourth data byte.

The first and the third data bytes contain a function bit F. If the function bit F= 0, frequency information is acknowledged and if F = 1, control/band information is acknowledged.

If the address is correct (signal AD1) the information is loaded into latches.

A function bit in the first and third data byte is used to pass this data either into the latches of the programmable divider (signal DTF) or into the latches for band and control information (signal DTB). The data transfer to the latches (signals DTF and DTB) is initiated after the 2nd and 4th data bytes.

A second string of latches is used for the data transfer into the programmable divider to inhibit the transfer during the preset operation (signal TDI, signal AVA is an internal “address valid” command).

The switching levels of clock and data (Pins 18 and 19) are 0.5 x V_{CC1}.

The control and band information bits have the following functions.

Bits R_0, R_1: Controls Reference Divider Division Ratio

R_0	R_1	Division Ratio
0	0	2048
1	0	1024
0	1	512
1	1	256

Bits R_2, R_3: Switches Internal Signals to the Buffer Outputs

R_2	R_3	Pin 16	Pin 17
0	0	–	–
0	1	62.5 kHz	–
1	0	F_{ref}	F_{BY2}
1	1	–	–

Bit B_5 has to be “one” when Pin 16 is used to output 62.5 kHz. Bits B_5 and B_7 have to be “one” to output F_{ref} and F_{BY2}. F_{BY2} is the programmable divider output frequency divided by two.

Bits R_2, R_6, T: Controls the Phase Comparator Output Stage

R_2	R_6	T	Output State
0	0	0	Normal Operation
0	0	1	“Off” (High Impedance)
0	1	0	High
0	1	1	Low
1	0	0	Normal Operation
1	0	1	“Off”
1	1	0	Normal Operation
1	1	1	“Off”

The Band Buffers

The band buffers are open collector transistors and are active “low” at Bn = 1. They are designed for 15 mA with typical on–voltage of 1.8 V. These buffers are designed to withstand relative high output voltage in the off–state (15 V).

B_5 and B_7 buffers (Pins 16 and 17) may also be used to output internal IC signals (reference frequency and programmable divider output frequency divided by 2) for test purposes.

Buffer B_5 may also be used to output a 62.5 kHz frequency from an intermediate stage of the reference divider. The bits B_5 and B_7 have to be “one” if the buffers are used for these additional functions.

The Programmable Divider

The programmable divider is a presettable down counter. When it has counted to zero it takes its required division ratio out of the latches B. Latches B are loaded from latches A by means of signal TDI which is synchronous to the programmable divider output signal.

Since latches A receive the data asynchronously with the programmable divider, this double latch scheme is needed to assure correct data transfer to the counter.

The division ratio definition is given by:

$N = 16384 \times N_{14} + 8192 \times N_{13} + \ldots + 4 \times N_2 + 2 \times N_1 + N_0$

Maximum Ratio 32767

Minimum Ratio 256

where $N_0 \ldots N_{14}$ are the different bits for frequency information.

The counter reloads correctly as long as its output frequency does not exceed 1.0 MHz.

Division ratios of < 256 are not allowed. At power–up the counter bit N8 is preset to “1”. All other bits are undetermined. In this way, the counter always starts with a division ratio of 256 or higher.

The data transfer between latches A and B (signal TDI) is also initiated by any start condition on the bus.

At power–on the whole bus receiver is reset and the programmable divider is set to a counting ratio of N = 256 or higher.

The Prescaler

The prescaler has a preamplifier and may be bypassed (Bit P). The signal then passes through preamplifier 2.

The table on the following page shows the frequency ranges which may be synthesized with and without prescaler.

The Phase Comparator

The phase comparator is phase and frequency sensitive and has very low output leakage current in the high impedance state.

The Operational Amplifier

The operational amplifier for the tuning voltage is designed for low noise, low input bias current and high power supply rejection. The positive input is biased internally. The operational amplifier needs 30 V supply (V_{CC2}) as minimum voltage for a guaranteed maximum tuning voltage of 28.5 V.

Figure 4 shows the usual filter arrangement. The component values depend very much on the application (tuner characteristic, reference frequency, etc.).

As a starting point for optimization, the component values in Figure 4 may be used for 7.8125 kHz reference frequency in a multiband TV tuner.

The Oscillator

The oscillator uses a 4.0 MHz crystal tied to ground in series with a capacitor. The crystal operates in the series resonance mode.

The crystal is driven through a 1.6 kΩ resistor on chip.

The voltage at Pin 16 “crystal”, has low amplitude and low harmonic distortion.

The negative resistance of the oscillator at Pin 1 (XTAL) is about 3.0 kΩ.

Input Data		Ref. Divider Div. Ratio	Ref. Freq. Hz(1)	With Int. Prescaler P = 0		Without Prescaler P = 1	
R_0	R_1			Frequency Steps kHz	Max. Input Freq. MHz	Frequency Steps kHz	Max. Imput Freq. MHz
0	0	2048	1953.125	15.625	512	1.953125	64
1	0	1024	3906.25	31.25	1024	3.90625	128
0	1	512	7812.5	62.5	1300(2)	7.8125	165(3)
1	1	256	15625.0	125.0	1300(2)	15.625	165(3)

NOTES: 1. With 4.0 MHz Crystal
2. Limit of Prescaler
3. Limit of Programmable Divider

For satellite tuner applications the circuit may be used with an external /4 prescaler and a reference divider ration of 1024 (R_0 = 1, R_1 = 0). In this way, frequencies up to 4.0 GHz can be synthesized with 125 kHz resolution (4.0 MHz crystal).

The same result can be achieved with an external /32 prescaler when the internal prescaler is bypassed (P = 1).

The Reference Divider

The reference divider of the MC44864 is programmable (Bits R_0 and R_1) for ratios of 2048, 1024, 512 and 256. This feature makes the circuit versatile.

Bit P: Controls the Prescaler

P	Prescaler Function
0	Prescaler Active
1	Prescaler Bypassed Prescaler Power Supply “Off”

Bits B_1, B_3, B_5, B_7: Controls the Band Buffers

B_1, B_3, B_5, B_7 = 0	Buffer “Off”
= 1	Buffer “On”

D/A SECTION

Basic Function

The D/A section has four separate chip addresses from the PLL section. Three D–to–A converters that have a resolution of 6 bits (5 bits plus sign) are on chip. The analog output voltages are dc. The converters are buffered to the analog outputs DA1, DA2 and DA3 by operational amplifiers with an output voltage range that is equal to the tuning voltage range (about 0 to 30 V). The operational amplifiers are arranged such that a positive or negative offset can be generated from the tuning voltage.

Data Format and Bus Protocols

The D–to–A information consists of the D/A chip address (CA2) and four data bytes. The first two bits of the data bytes are used as the function address. Thus the bytes C_1, C_2 and C_3 contain the address for the individual converter and the 6 bits to be converted. Bit D_5 is the sign (log “1” for positive offset, log “0” for negative offset) and the bits D_0 to D_4 determine the number of steps to be made as an offset from the tuning voltage. The bits S_0 and S_1 in the data byte RA define the step size (V_{step}) and the range of the converters (see Figures 8 and 9). The range is the same for all converters.

After the chip address (CA2) is acknowledged, up to four data bytes may be received by the IC. If more than four bytes are received, the fifth and following bytes are ignored and the last acknowledge pulse is sent after the fourth data byte. The data transfer to the converters (signal DTC) is initiated each time a complete data byte is received.

The following shows some examples of the permissible bus protocols of the D–to–A section. The data bytes may be sent to the IC in random order with up to four in one sequence. The same converter may be loaded up to four times as shown in example 6. Below are 6 examples of permissible bus protocols.

Ex. 1	STA	CA2	C1	STO			
Ex. 2	STA	CA2	C1	C2	STO		
Ex. 3	STA	CA2	C1	C2	C3	STO	
Ex. 4	STA	CA2	C1	C2	C3	RA	STO
Ex. 5	STA	CA2	RA	C1	C2	C3	STO
Ex. 6	STA	CA2	C1	C1	C1	C1	STO

STA = Start Condition
STO = Stop Condition
CA2 = Chip Address Byte for D/A Section
C1, C2, C3 = Data Bytes for D/A Converters
RA = Data Byte for Range

Figure 7. Definition of Bytes

CA2_D/A Chip Address	1	1	0	0	A_2	A_1	$A_0 = 0$		ACK
C1_Converter 1	0	0	D_5	D_4	D_3	D_2	D_1	D_0	ACK
C2_Converter 2	0	1	D_5	D_4	D_3	D_2	D_1	D_0	ACK
C3_Converter 3	1	0	D_5	D_4	D_3	D_2	D_1	D_0	ACK
RA_Range Selection	1	1	X	X	X	X	S_1	S_0	ACK

Figure 8. Output Voltage (D/A Converters)

$$V_{DA} = V_{TUN} \pm V_{step}\,(D_0 + 2\,D_1 + 4\,D_2 + 8\,D_3 + 16\,D_4)$$

D_5 = 1 positive sign; D_5 = 0 negative sign

V_{TUN}: Tuning Voltage set by PLL
V_{step}: Voltage Step (LSB) of the D/A Converters

Figure 9. Range Selection of the D/A Converters

Input Data		Typ. Step Size V_{step}	Guaranteed Range 31 Steps
S_0	S_1		
0	0	225 mV	6.25 V
1	0	125 mV	3.40 V
0	1	70 mV	1.90 V
1	1	40 mV	1.05 V

The D/A Converters

The D/A converters convert 5 bit into analog current of which the polarity is switched by the sixth bit. The reference voltage of the converters is programmed by two bits (S_0, S_1 of the RA–byte) to determine the scaling factor. The analog currents are then converted into voltages and added to their respective operational amplifier nominal bias. The resulting voltages at Pins 6, 7 and 8 are the tuning voltages (V_{TUN}, see Figure 4) at Pin 5 plus any offset provided by information in the D/A converters.

If the data bits D_0 to D_4 are all “0”, the three D/A output voltages on Pins 6, 7 and 8 are equal to the tuning voltage (Pin 5) within the DAC offset voltages.

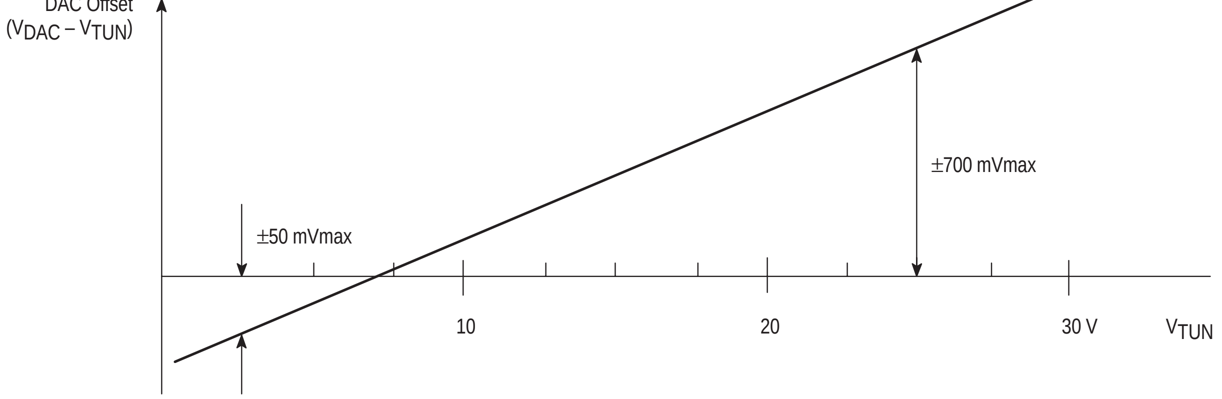
The four amplifiers have the same output characteristics with the maximum output voltage being 1.5 V lower than V_{CC2} in the worst case. The four analog outputs are short–circuit protected. At power–up, the D/A outputs are undetermined.

The D/A converters are guaranteed to be monotonic with a voltage step variation of ±0.5 LSB.

The D/A converters work correctly as long as the PLL loop is active. V_{TUN} is then between 0.3 V and V_{CC2} – 1.5 V. If the loop saturates, the DACs do not work.

The DAC–OFFSET is defined as the difference between the DAC output voltage (with bits D_0 to D_4 = 0) and the tuning voltage (PLL active). The DAC operation is guaranteed from 0.3 V to V_{CC2} – 1.5 V. On typical samples, the DACs will operate down to 0.2 V.

Figure 10. Definition of DAC Offset



Automotive Electronic Circuits

In Brief . . .

Motorola Analog has established itself as a global leader in custom integrated circuits for the automotive market. With multiple design centers located on four continents, global process and assembly sites, and strategically located supply centers, Motorola serves the global automotive market needs. These products are key elements in the rapidly growing engine control, body, navigation, entertainment, and communication electronics portions of modern automobiles. Though Motorola is most active in supplying automotive custom designs, many of yesterday's proprietary custom devices have become standard products of today, available to the broad base manufacturers who support this industry. Today, based on new technologies, Motorola offers a wide array of standard products ranging from rugged high current ''smart'' fuel injector drivers which control and protect the fuel management system through the rigors of the underhood environment, to the latest SMARTMOS™ switches and series transient protectors. Several devices are targeted to support microprocessor housekeeping and data line protection. A wide range of packaging is available including die, flip–chip, and SOICs for high density layouts, to low thermal resistance multi–pin, single–in–line types for high power control ICs.

Automotive Electronic Circuits

Table 1. Voltage Regulators

Function	Features	Suffix/ Package	Device
Low Dropout Voltage Regulator	Positive fixed and adjustable output voltage regulators which maintain regulation with very low input to output voltage differential.	Z/29, T/221A, T/314D, TH/314A, TV/314B, DT/369A, DT–1/369, D2T/936, D2T/936A, D/751	LM2931, C
Low Dropout Dual Regulator	Positive low voltage differential regulator which features dual 5.0 V outputs, with currents in excess of 750 mA (switched) and 10 mA standby, and quiescent current less than 3.0 mA.	T/314D, TH/314A, TV/314B, D2T/936A	LM2935
Automotive Voltage Regulator	Provides load response control, duty cycle limiting, under/overvoltage and phase detection, high side MOSFET field control, voltage regulation in 12 V alternator systems.	DW/751D	MC33092
Low Dropout Voltage Regulator	Positive 5.0 V, 500 mA regulator having on–chip power–up–reset circuit with programmable delay, current limit, and thermal shutdown.	T/314D, TV/314B	MC33267
Low Dropout Voltage Regulator	Positive 3.3 V, 5.0 V, 12 V, 800 mA regulator.	D/751, DT/369A	MC33269

Table 2. Electronic Ignition

Function	Features	Suffix/ Package	Device
Electronic Ignition Circuit	Used in high energy variable dwell electronic ignition systems with variable reluctance sensors. Dwell and spark energy are externally adjustable. “Bumped” die for inverted mounting to substrate.	P/626, D/751, Flip–Chip	MC3334, MCCF3334
Electronic Ignition Circuit	Used in high energy electronic ignition systems requiring differential Hall Sensor control. ‘‘Bumped” die for inverted mounting to substrate.	DW/751G, Flip–Chip	MC33093, MCCF33093
Electronic Ignition Circuit	Used in high energy electronic ignition systems requiring single Hall Sensor control. ‘‘Bumped” die for inverted mounting to substrate.	DW/751G, Flip–Chip	MC33094, MCCF33094
Electronic Ignition Circuit	Used in high energy electronic ignition systems requiring single Hall Sensor control. Dwell feedback for coil variation. ‘‘Bumped” die for inverted mounting to substrate.	DW/751G, Flip–Chip	MC79076, MCCF79076

Table 3. Special Functions

Function	Features	Suffix/ Package	Device
Low Side Protected Switch	Single automotive low side switch having CMOS compatible input, 1.0 A maximum rating, with overcurrent, overvoltage and thermal protection.	T/221A, T–1/314D, DW/751G	MC3392
Low Current High–Side Switch	Drives loads from positive side of power supply and protects against high–voltage transients.	T/314D, DW/751G	MC3399
High–Side TMOS Driver	Designed to drive and protect N–channel power MOSFETs used in high side switching applications. Has internal charge pump, externally programmed timer and fault reporting.	P/626, D/751	MC33091A
MI–Bus Interface Stepper Motor Controller	High noise immunity serial communication using MI–Bus protocol to control relay drivers and motors in harsh environments. Four phase signals drive two phase motors in either half or full–step modes.	DW/751G	MC33192
Quad Fuel Injector Driver	Four low side switches with parallel CMOS compatible input control, $\leq$ 7.0 mA quiescent current, 0.25 Ω $r_{DS(on)}$ at 25°C independent outputs with 3.0 A current limiting and internal 65 V clamps.	T/821D, TV/821C	MC33293A
Octal Serial Output Switch	Eight low side switches having 8–bit serial CMOS compatible input control, serial fault reporting, $\leq$ 4.0 mA quiescent current, independent 0.45 Ω $r_{DS(on)}$ at 25°C outputs with 3.0 A minimum current limiting and internal 55 V clamps.	P/738, DW/751E	MC33298
Integral Alternator Regulator	Control device used in conjunction with a Darlington device to monitor and control the field current in alternator charging systems. ‘‘Bumped” die for inverted mounting to substrate.	D/751A, Flip–Chip	MC33095 MCCF33095
Peripheral Clamping Array	Protects up to six MPU I/O lines against voltage transients.	*/626, D/751	TCF6000
Automotive Direction Indicator	Detects defective lamps and protects against overvoltage in automotive turn–signal applications. Replaces UAA1041B in most applications.	D/751, P/626	MC33193
Automotive Wash Wiper Timer	Standard wiper timer control device that drives a wiper motor relay and can perform the intermittent, afterwash and continuous wiper timer functions.	D/751, P/626	MC33197A
Automotive ISO 9141 Serial Link Driver	Interface between the two–wire asynchronous serial communication interface (SCI) of a microcontroller and a special one–wire care diagnosis system (DIA).	D/751A	MC33199

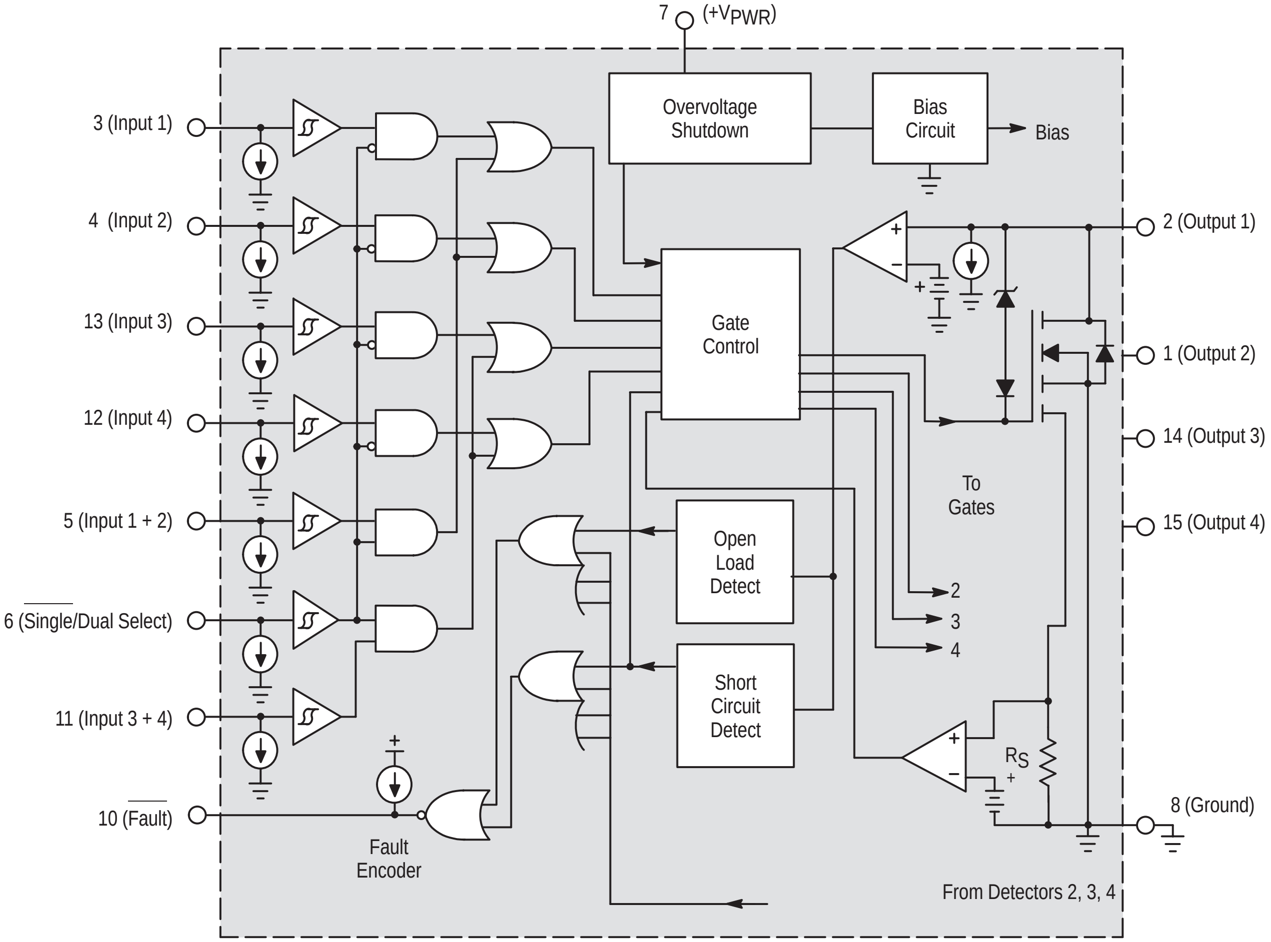
* No Suffix

Quad Fuel Injector Driver

MC33293AT, MC33293ATV

T_J = –40° to +150°C, Case 821D, C

The MC33293AT is a monolithic quad low–side switching device having CMOS logic, bipolar/ CMOS analog circuitry, and DMOS power FETs. All inputs are CMOS compatible. Each independent output is internally clamped to 65 V, current limited to ≥ 3.0 A, and has an $r_{DS(on)}$ of ≤ 0.25 Ω with V_{PWR} ≥ 9.0 V and may be paralleled to lower $r_{DS(on)}$. Fault output reports existence of open loads (outputs “On” or “Off”), shorted loads, and over temperature condition of outputs. A shorted load condition will shut off only the specific output involved while allowing other outputs to operate normally. An overvoltage condition will shut off all outputs for the overvoltage duration. A single/dual mode select pin allows either independent input/output operation or paired output operation.

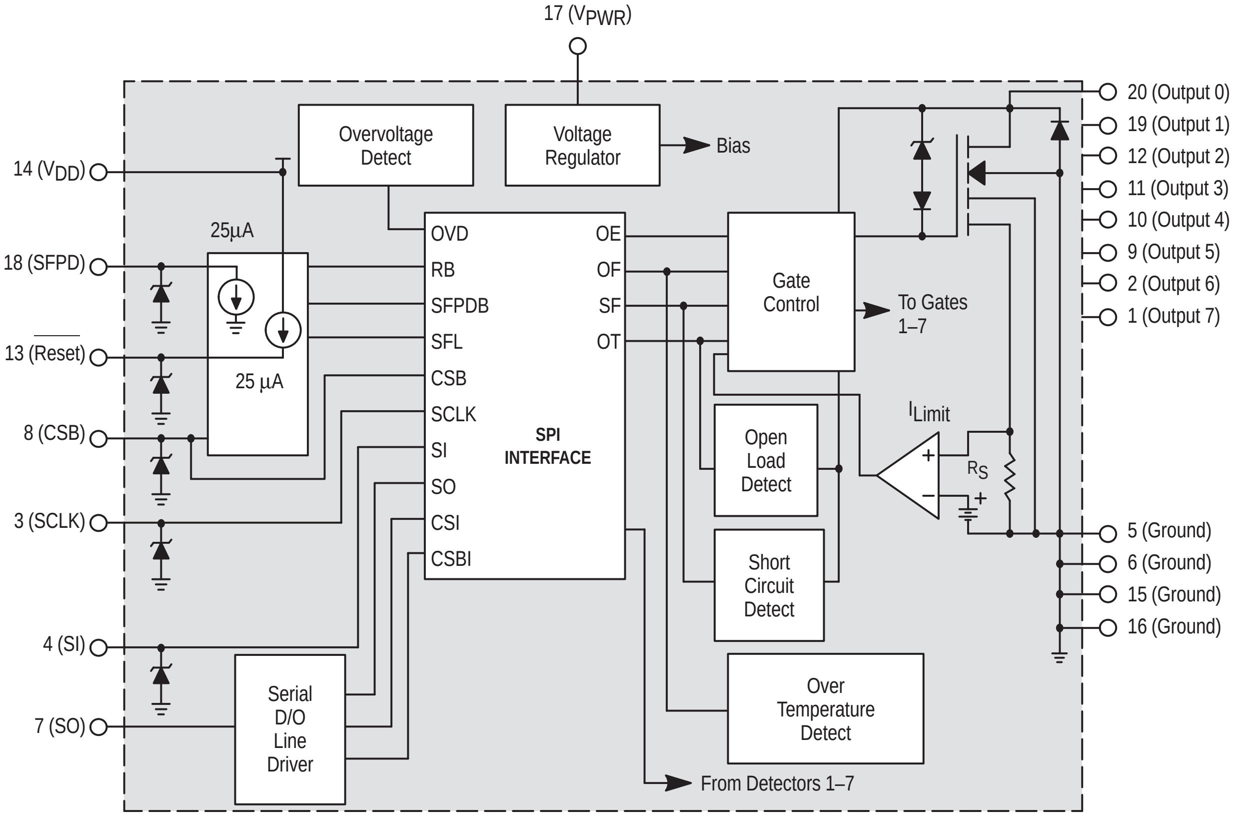


Octal Serial Switch

MC33298P, MC33298DW

T_J = –40° to +150°C, Case 738, 751E

The MC33298 is a monolithic eight output low–side switch with 8–bit serial input control. Incorporates CMOS logic, bipolar/CMOS analog circuitry, and DMOS power FETs. All inputs are CMOS compatible. It is designed to interface to a microcontroller and switch inductive or incandescent loads. Each independent output is internally clamped to 55 V, current limited to ≥ 3.0 A, and has an $r_{DS(on)}$ of ≤ 0.45 Ω with V_{PWR} ≥ 9.0 V. This device has low standby current, cascadable fault status reporting, output diagnostics, and shutdown for each output.



Dual High–Side Switch

MC33143DW

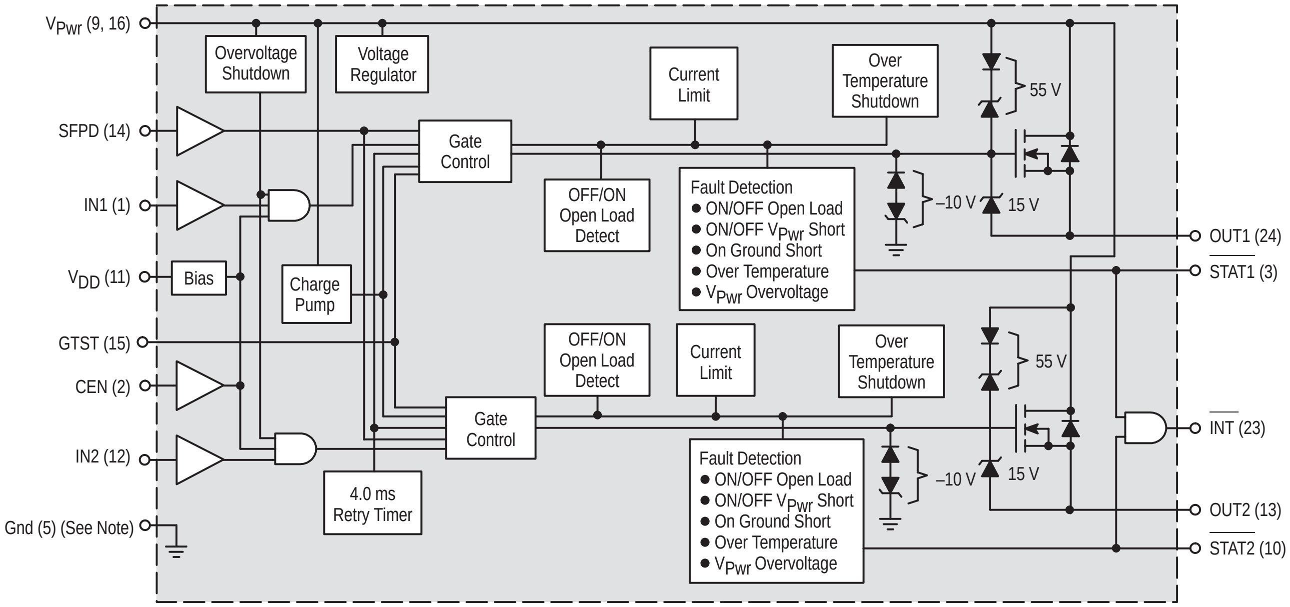
T_A = –40° to +125°C, Case 751E

The MC33143 is a dual high–side switch designed for solenoid control in harsh automotive applications, but is well suited for other environments. The device can also be used to control small motors and relays as well as solenoids. The MC33143 incorporates SMARTMOS™ technology, with CMOS logic, bipolar/MOS analog circuitry, and DMOS power outputs. An internal charge pump is incorporated for efficient gate enhancement of the internal high–side power output devices. The outputs are designed to provide current to low impedance solenoids. The MC33143 provides individual output fault status reporting along with internal Overcurrent and Over Temperature protection. The device also has Overvoltage protection, with automatic recovery, which “globally” disables both outputs for the duration of an Overvoltage condition. Each output has individual Overcurrent and Over Temperature shutdown with automatic retry recovery. Outputs are enabled with a CMOS logic high signal applied to an input to providing true logic control. The outputs, when turned on, provide full supply (battery) voltage across the solenoid coil.

The MC33143 is packaged in an economical 24 pin surface mount power package and specified over an operating voltage of 5.5 V ≤ V_{Pwr} < 26 V for –40°C ≤ T_A ≤ 125°C.

- Designed to Operate Over Wide Supply Voltages of 5.5 V to 26 V
- Dual High–Side Outputs Clamped to –10 V for Driving Inductive Loads
- Internal Charge Pump for Enhanced Gate Drive
- Interfaces Directly to a Microcontroller with Parallel Input Control
- Outputs Current Limited to 3.0 A to 6.0 A for Driving Incandescent Loads
- Chip Enable “Sleep Mode” for Power Conservation
- Individual Output Status Reporting
- Fault Interrupt Output for System Interrupt Use
- Output ON or OFF Open Load Detection
- Overvoltage Detection and Shutdown
- Output Over Temperature Detection and Shutdown with Automatic Retry
- Sustained Current Limit or Immediate Overcurrent Shutdown Output Modes
- Output Short to Ground Detection and Shutdown with Automatic Retry
- Output Short to V_{Pwr} Detection

Simplified Internal Block Diagram



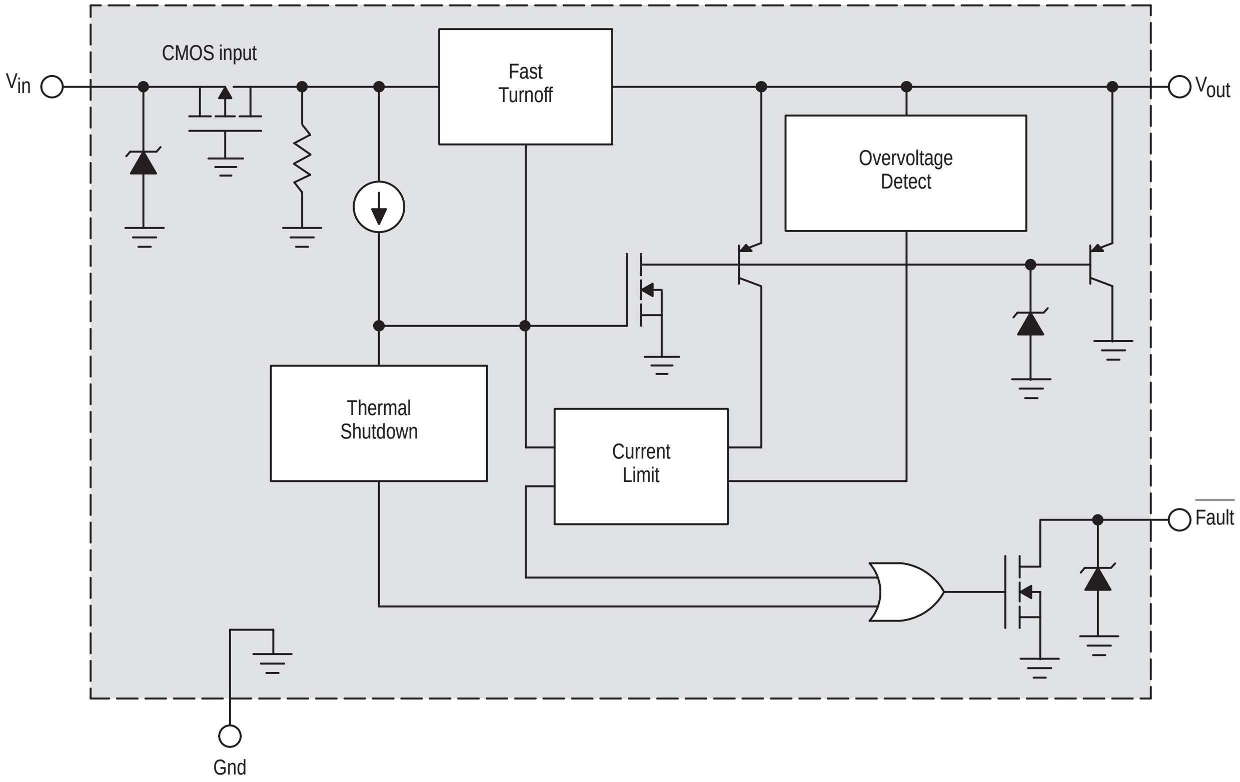
NOTE: Pins 5, 6, 7, 8, 17, 18, 19 and 20 should all be grounded so as to provide electrical as well as thermal heatsinking of the device.

Low Side Protected Switch

MC3392T, T–1, DW

T_J = –40° to +150°C,
Case 221A, 314D, 751G

Single low side protected switch with fault reporting capability. Input is CMOS compatible. Output is short circuit protected to 1.0 A minimum with a unique current fold–back feature. Device has internal output clamp for driving inductive loads with overcurrent, overvoltage, and thermal protection. When driving a moderate load, the MC3392 performs as an extremely high gain, low saturation Darlington transistor having a CMOS input characteristic with added protection features. In some applications, the three terminal version can replace industry standard TIP100/101 NPN power Darlington transistors.

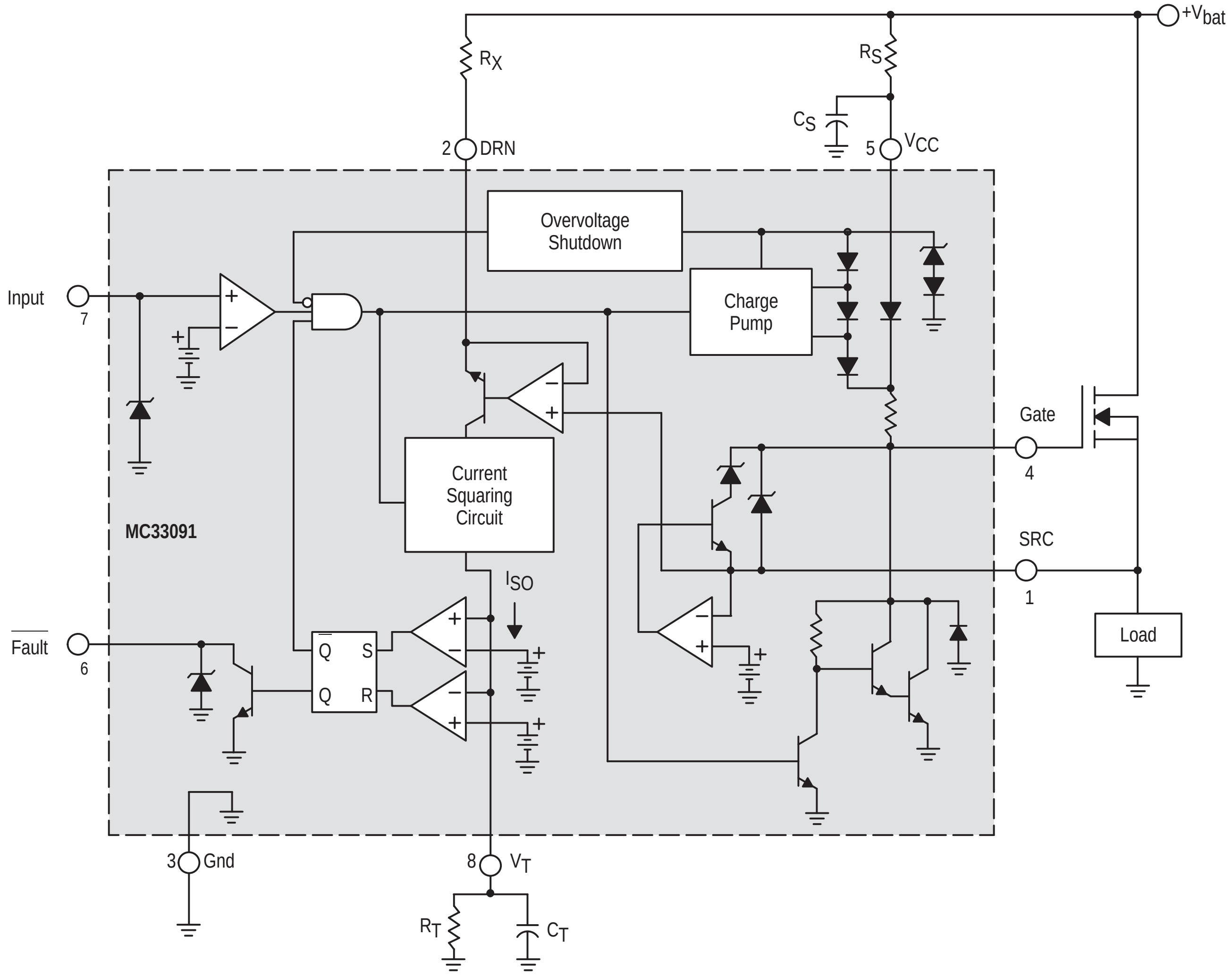


High Side TMOS Driver

MC33091AP, AD

T_J = –40° to +150°C, Case 626, 751

Offers an economical solution to drive and protect N–channel power TMOS devices used in high side switching configurations. Unique device monitors load resulting V_{DS}. TMOS voltage to produce a proportional current used to drive an externally programmed over current timer circuit to protect the TMOS device from shorted load conditions. Timer can be programmed to accommodate driving incandescent loads. Few external components required to drive a wide variety of N–channel TMOS devices. A Fault output is made available through the use of an open collector NPN transistor requiring a single pull–up resistor for operation. Input is CMOS compatible. Device uses ≤ 3.0 µA standby current and has an internal charge pump requiring no external components for operation.

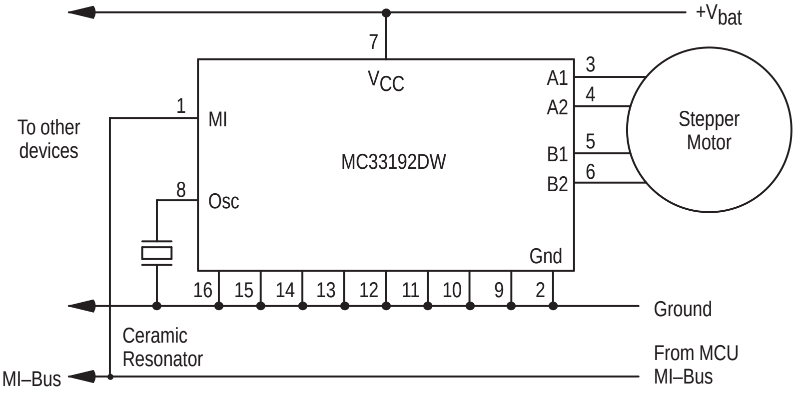


MI–Bus Interface Stepper Motor Controller

MC33192DW

T_J = –40° to +100°C, Case 751G

Intended to control loads in harsh automotive environments using a serial communication bus. Can provide satisfactory real time control of up to eight stepper motors using MI–Bus protocol. Use of MI–Bus offers a noise immune system solution for difficult applications involving relays and motors. The stepper motor controller provides four phase signals to drive two phase motors in either half of full–step modes. Designed to interface to a microprocessor with minimal amount of wiring, affording an economical and versatile system.



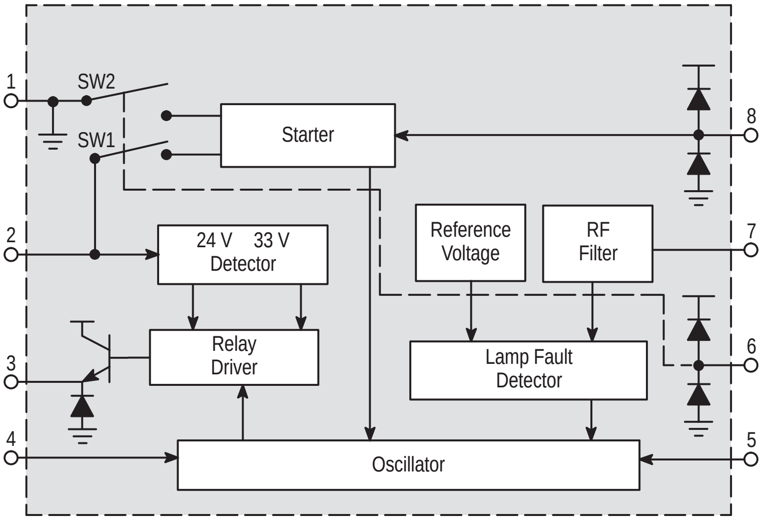
Automotive Direction Indicator

MC33193P, D

T_A = –40° to +125°C, Case 626, 751

The MC33193 is a new generation industry standard UAA1041 “Flasher”. It has been developed for enhanced EMI sensitivity, system reliability, and improved wiring simplification. The MC33193 is pin compatible with the UAA1041 and UAA1041B in the standard application configuration as shown in Figure 9, without lamp short circuit detection and using a 20 mΩ shunt resistor. The MC33193 has a standby mode of operation requiring very low standby supply current and can be directly connected to the vehicle’s battery. It includes a RF filter on the Fault detection pin (Pin 7) for EMI purposes. Fault detection thresholds are reduced relative to those of the UAA1041 allowing a lower shunt resistance value (20 mΩ) to be use.

- Pin Compatible with the UAA1041
- Defective Lamp Detection Threshold
- RF Filter for EMI Purposes
- Load Dump Protection
- Double Battery Capability for Jump Start Protection
- Internal Free Wheeling Diode Protection
- Low Standby Current Mode



Automotive Wash Wiper Timer

MC33197AD

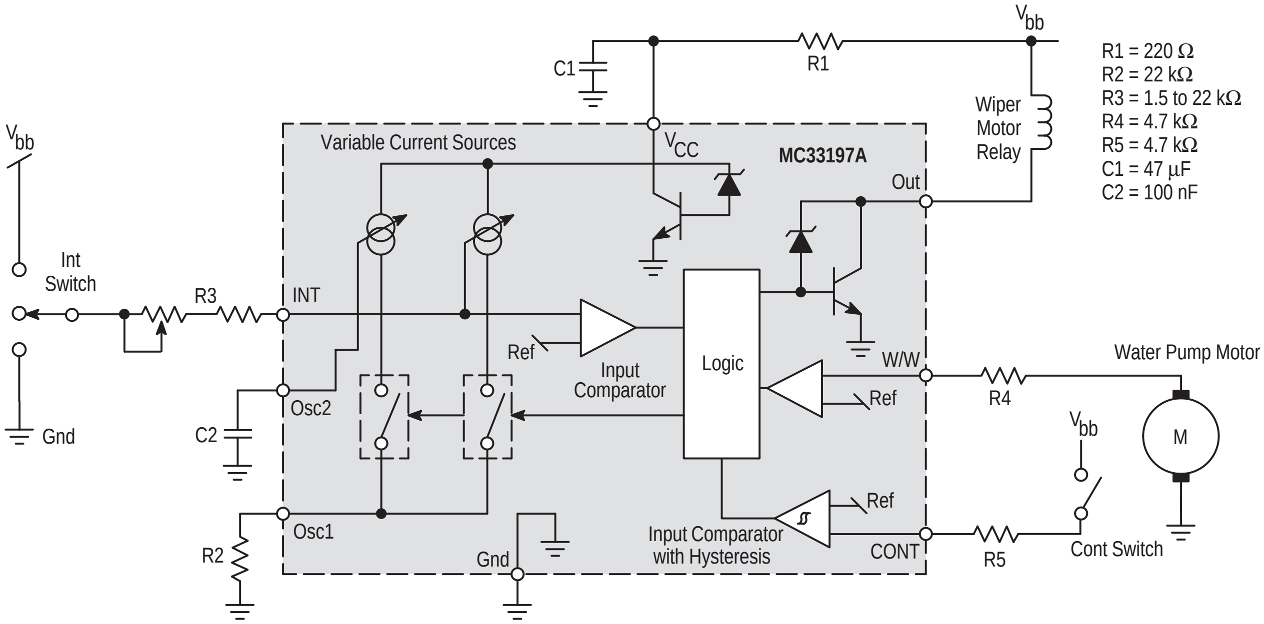
T_A = –40° to +105°C, Case 751

MC33197AP

T_A = –40° to +125°C, Case 626

The MC33197A is a standard wiper timer control device designed for harsh automotive applications. The device can perform the intermittent, after wash, and continuous wiper timer functions. It is designed to directly drive a wiper motor relay. The MC33197A requires very few external components for full system implementation. The intermittent control pin can be switched to ground or V_{bat} to meet a large variety of possible applications. The intermittent timing can be fixed or adjustable via an external resistor. The MC33197A is built using bipolar technology and parametrically specified over the automotive ambient temperature range and 8.0 to 16 V supply voltage. The MC33197A can operate in both front and rear wiper applications.

- Adjustable Time Interval of Less Than 500 ms to More Than 30 s
- Intermittent Control Pin Can Be Switched to Ground or V_{bat}
- Adjustable After Wipe Time
- Priority to Continuous Wipe
- Minimum Number of Timing Components
- Integrated Relay Driver With Free Wheeling Protection Diode
- Operating Voltage Range From 8.0 to 16 V
- For Front Wiper and Rear Wiper Window Applications



Automotive ISO 9141 Serial Link Driver

MC33199D

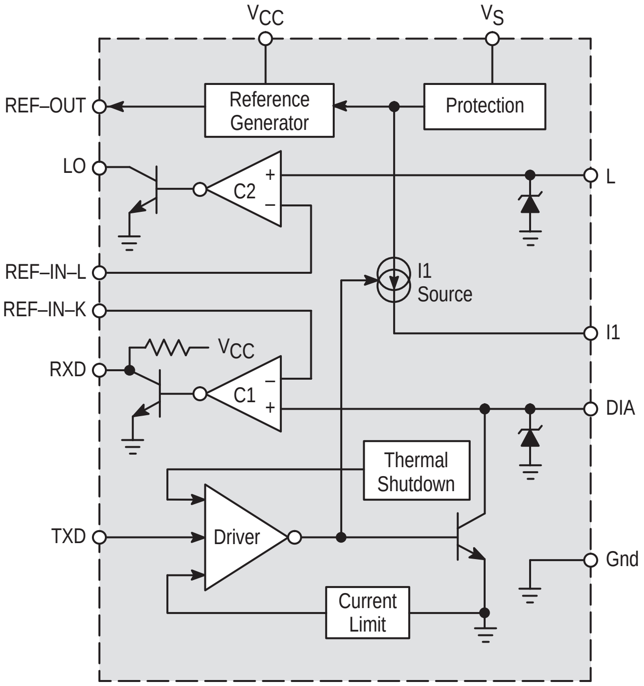
T_A = –40° to +125°C, Case 751A

The MC33199D is a serial interface circuit used in diagnostic applications. It is the interface between the microcontroller and the special K and L Lines of the ISO diagnostic port. The MC33199D has been designed to meet the "Diagnosis System ISO 9141" specification.

The device has a bi–directional bus K Line driver, fully protected against short circuits and over temperature. It also includes the L Line receiver, used during the wake up sequence in the ISO transmission.

The MC33199 has a unique feature which allows transmission baud rate up to 200 k baud.

- Electrically Compatible with Specification "Diagnosis System ISO 9141"
- Transmission Speed Up to 200 k Baud
- Internal Voltage Reference Generator for Line Comparator Thresholds
- TXD, RXD and LO Pins are 5.0 V CMOS Compatible
- High Current Capability of DIA Pin (K Line)
- Short Circuit Protection for the K Line Input
- Over Temperature Shutdown with Hysteresis
- Large Operating Range of Driver Supply Voltage
- Full Operating Temperature Range
- ESD Protected Pins

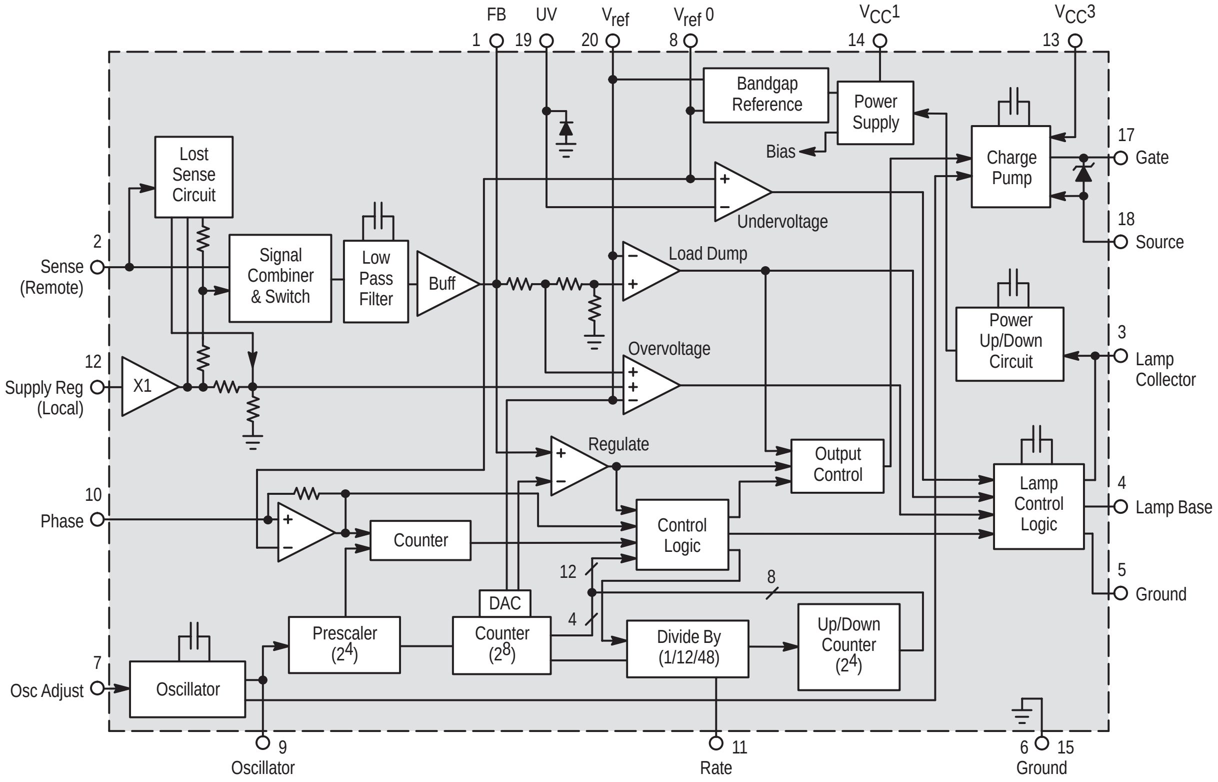


Alternator Voltage Regulator

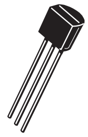
MC33092DW

T_J = –40° to +125°C, Case 751D

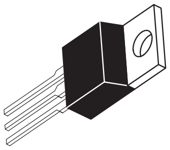
Provides voltage regulation and load response control in diode rectified 12 V alternator charging systems. Provides externally programmed load response control of the alternator output current to eliminate engine speed hunting and vibration due to sudden electrical loads. Monitors and compares the system battery voltage to an externally programmed set point value and pulse width modulates an N–channel MOSFET transistor to control the average alternator field current. In addition, has duty cycle limiting, under/overvoltage and phase detection (broken belt) protective features.



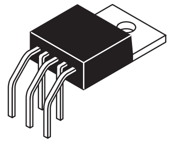
Automotive Electronic Circuits Package Overview



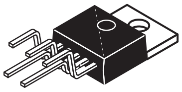
CASE 29
Z SUFFIX



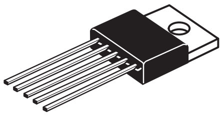
CASE 221A
T SUFFIX



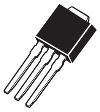
CASE 314A
TH SUFFIX



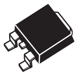
CASE 314B
TV SUFFIX



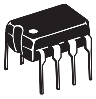
CASE 314D
T, T–1 SUFFIX



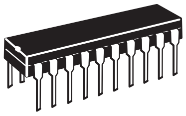
CASE 369
DT–1 SUFFIX



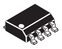
CASE 369A
DT SUFFIX



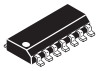
CASE 626
P, NO SUFFIX



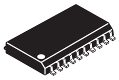
CASE 738
P SUFFIX



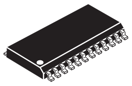
CASE 751
D SUFFIX



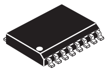
CASE 751A
D SUFFIX



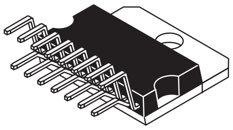
CASE 751D
DW SUFFIX



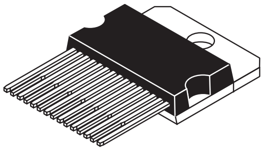
CASE 751E
DW SUFFIX



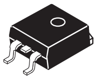
CASE 751G
DW SUFFIX



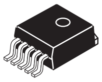
CASE 821C
TV SUFFIX



CASE 821D
T SUFFIX



CASE 936
D2T SUFFIX



CASE 936A
D2T SUFFIX

Device Listing

Voltage Regulators

Device	Function	Page
LM2931 Series	Low Dropout Voltage Regulators	See Chapter 3
MCCF33095, MC33095	Integral Alternator Regulator	10–134

Electronic Ignition

MC3334, MCC3334, MCCF3334	High Energy Ignition Circuit	10–15
MC79076, MCCF79076	Electronic Ignition Control Circuit	10–131
MCCF33093	Ignition Control Flip–Chip	10–132
MCCF33094	Ignition Control Flip–Chip	10–133

Special Functions

MC3392	Low Side Protected Switch	10–19
MC3399	Automotive Half–Amp High–Side Switch	10–28
MC33091A	High–Side TMOS Driver	10–31
MC33092	Alternator Voltage Regulator	10–45
MC33143	Dual High–Side Switch	10–53
MC33192	Mi-Bus Interface Stepper Motor Controller	10–60
MC33193	Automotive Direction Indicator	10–71
MC33197A	Automotive Wash Wiper Timer	10–78
MC33199	Automotive ISO 9141 Serial Link Driver	10–83
MC33293A	Quad Low Side Switch	10–94
MC33298	Octal Serial Switch and Serial Peripheral Interface I/O	10–109
TCA5600/TCF5600	Universal Microprocessor Power Supply/Controllers	See Chapter 3
TCF6000	Peripheral Clamping Array	10–144
UAA1041B	Automotive Direction Indicator	10–148

MC3334
MCC3334
MCCF3334

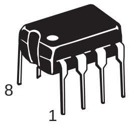
High Energy Ignition Circuit

This device is designed to use the signal from a reluctor type ignition pickup to produce a well controlled output from a power Darlington output transistor.

- Very Low Peripheral Component Count
- No Critical System Resistors
- Wide Supply Voltage Operating Range (4.0 V to 24 V)
- Overvoltage Shutdown (30 V)
- Dwell Automatically Adjusts to Produce Optimum Stored Energy without Waste
- Externally Adjustable Peak Current
- Available in Chip and Flip–Chip Form
- Transient Protected Inputs and Outputs

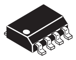
HIGH ENERGY
IGNITION CIRCUIT

SEMICONDUCTOR
TECHNICAL DATA



P SUFFIX
PLASTIC PACKAGE
CASE 626

D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)



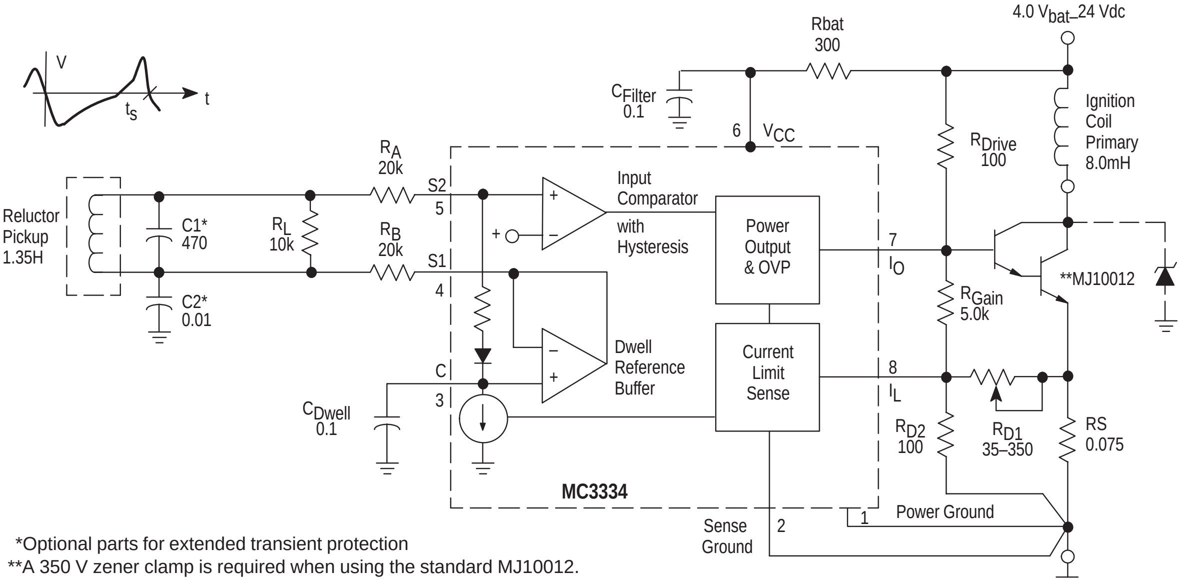
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage–Steady State Transient 300 ms or less	V_{bat}	24 90	V
Output Sink Current–Steady State Transient 300 ms or less	$I_{O(Sink)}$	300 1.0	mA A
Junction Temperature	$T_{J(max)}$	150	°C
Operating Temperature Range	T_A	–40 to +125	°C
Storage Temperature Range	Tstg	–65 to +150	°C
Power Dissipation, Plastic Package, Case 626 Derate above 25°C	P_D	1.25 10	W mW/°C

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC3334P	T_A = – 40° to +125°C	Plastic DIP
MC3334D		SO–8
MCC3334		Chip
MCCF3334		Flip–Chip

Figure 1. Block Diagram and Typical Application

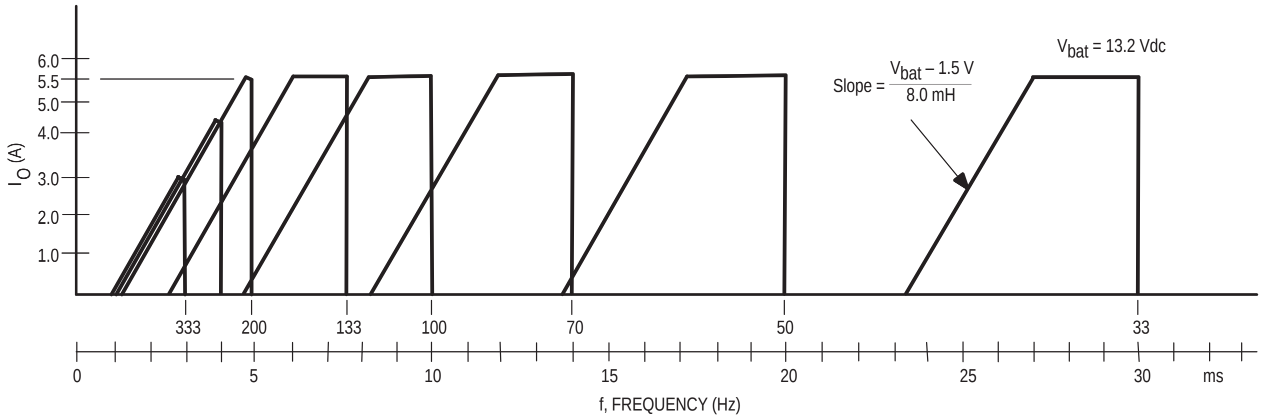


*Optional parts for extended transient protection
**A 350 V zener clamp is required when using the standard MJ10012.
This clamp is not required if a selected version with $V_{CEO(sus)} \geq$ 550 V is used.

ELECTRICAL CHARACTERISTICS (T_A = –40° to +125°C, V_{bat} = 13.2 Vdc, circuit of Figure 1, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Internal Supply Voltage, Pin 6 V_{bat} = 4.0 Vdc 8.0 Vdc 12.0 14.0	V_{CC}	 – – – –	 3.5 7.2 10.4 11.8	 – – – –	Vdc
Ignition Coil Current Peak, Cranking RPM 2.0 Hz to 27 Hz V_{bat} = 4.0 Vdc 6.0 8.0 10.0	$I_{O(pk)}$	 3.0 4.0 4.6 5.1	 3.4 5.2 5.3 5.4	 – – – –	A pk
Ignition Coil Current Peak, Normal RPM Frequency = 33 Hz 133 Hz 200 Hz 267 Hz 333 Hz	$I_{O(pk)}$	 5.1 5.1 4.2 3.4 2.7	 5.5 5.5 5.4 4.4 3.4	 – – – –	A pk
Ignition Coil On–Time, Normal RPM Range Frequency = 33 Hz 133 Hz 200 Hz 267 Hz 333 Hz	t_{on}	 – – – – –	 7.5 5.0 4.0 3.0 2.3	 14.0 5.9 4.6 3.6 2.8	ms
Shutdown Voltage	V_{bat}	25	30	35	Vdc
Input Threshold (Static Test) Turn–on Turn–off	V_{S2}–V_{S1}	 – –	 360 90	 – –	mVdc
Input Threshold Hysteresis	V_{S2}–V_{S1}	75	–	–	mVdc
Input Threshold (Active Operation) Turn–on Turn–off	V_{S2}	 – –	 1.8 1.5	 – –	Vdc
Total Circuit Lag from t_S (Figure 1) until Ignition Coil Current Falls to 10%		–	60	120	µs
Ignition Coil Current Fall Time (90% to 10%)		–	4.0	–	µs
Saturation Voltage IC Output (Pin 7) (R_{DRIVE} = 100 Ω) V_{bat} = 10 Vdc 30 Vdc 50 Vdc	$V_{CE(sat)}$	 – – –	 120 280 540	 – – –	mVdc
Current Limit Reference, Pin 8	V_{ref}	120	160	190	mVdc

Figure 2. Ignition Coil Current versus Frequency/Period



CIRCUIT DESCRIPTION

The MC3334 high energy ignition circuit was designed to serve aftermarket Delco five–terminal ignition applications. This device, driving a high voltage Darlington transistor, offers an ignition system which optimizes spark energy at minimum power dissipation. The IC is pinned–out to permit thick film or printed circuit module design without any crossovers.

The basic function of an ignition circuit is to permit build–up of current in the primary of a spark coil, and then to interrupt the flow at the proper firing time. The resulting flyback action in the ignition coil induces the required high secondary voltage needed for the spark. In the simplest systems, fixed dwell angle produces a fixed duty cycle, which can result in too little stored energy at high RPM, and/or wasted power at low RPM. The MC3334 uses a variable DC voltage reference, stored on C_{Dwell}, and buffered to the bottom end of the reluctor pickup (S1) to vary the duty cycle at the spark coil. At high RPM, the MC3334 holds the output “off” for approximately 1.0 ms to permit full energy discharge from the previous spark; then it switches the output Darlington transistor into full saturation. The current ramps up at a slope dictated by V_{bat} and the coil L. At very high RPM the peak current may be less than desired, but it is limited by the coil itself.

As the RPM decreases, the ignition coil current builds up and would be limited only by series resistance losses. The MC3334 provides adjustable peak current regulation sensed by R_S and set by R_{D1}, in this case at 5.5 A, as shown in Figure 2. As the RPM decreases further, the coil current is held at 5.5 A for a short period. This provides a reserve for sudden acceleration, when discharge may suddenly occur earlier than expected. The peak hold period is about 20% at medium RPM, decreasing to about 10% at very low RPM. (Note: 333 Hz = 5000 RPM for an eight cylinder four stroke engine.) At lower V_{bat}, the “on” period automatically stretches to accommodate the slower current build–up. At very low V_{bat} and low RPM, a common condition during cold starting, the “on” period is nearly the full cycle to permit as much coil current as possible.

The output stage of the IC is designed with an OVP circuit which turns it on at $V_{bat} \approx 30$ V ($V_{CC} \approx 22$ V), holding the output Darlington off. This protects the IC and the Darlington from damage due to load dump or other causes of excessive V_{bat}.

Component Values

Pickup – series resistance = 800 Ω ± 10% @ 25°C
inductance = 1.35 H @ 1.0 kHz @ 15 Vrms

Coil – leakage L = 0.6 mH
primary R = 0.43 Ω ± 5% @ 25°C
primary L = 7.5 mH to 8.5 mH @ 5.0 A

R_L – load resistor for pickup = 10 kΩ ± 20%

R_A, R_B – input buffer resistors provide additional transient protection to the already clamped inputs = 20 k ± 20%

C1, C2 – for reduction of high frequency noise and spark transients induced in pick–up and leads; optional and non–critical

R_{bat} – provides load dump protection (but small enough to allow operation at V_{bat} = 4.0 V) = 300 Ω ± 20%

C_{Filter} – transient filter on V_{CC}, non–critical

C_{Dwell} – stores reference, circuit designed for 0.1 µF ± 20%

R_{Gain} – R_{Gain}/R_{D1} sets the DC gain of the current regulator = 5.0 k ± 20%

R_{D2} – R_{D2}/R_{D1} set up voltage feedback from R_S

R_S – sense resistor (PdAg in thick film techniques) = 0.075 Ω ± 30%

R_{Drive} – low enough to supply drive to the output Darlington, high enough to keep $V_{CE(sat)}$ of the IC below Darlington turn–on during load dump = 100 Ω ± 20%, 5.0 W

R_{D1} – starting with 35 Ω assures less than 5.5 A, increasing as required to set 5.5 A

$$R_{D1} = \frac{I_{O(pk)}\,R_S - V_{ref}}{\dfrac{V_{ref}}{R_{D2}} - \dfrac{1.4}{R_{Gain}}} - (\approx 100\ \Omega)$$

General Layout Notes

The major concern in the substrate design should be to reduce ground resistance problems. The first area of concern is the metallization resistance in the power ground to module ground and the output to the R_{drive} resistor. This resistance directly adds to the $V_{CE(sat)}$ of the IC power device and if not minimized could cause failure in load dump. The second concern is to reference the sense ground as close to the ground end of the sense resistor as possible in order to further remove the sensitivity of ignition coil current to ground I.R. drops.

All versions were designed to provide the same pin–out order viewed from the top (component side) of the board or substrate. This was done to eliminate conductor cross–overs. The standard MC3334 plastic device is numbered in the industry convention, counter–clockwise viewed from the top, or bonding pad side. The MCCF3334 “flip” or “bump” chip is made from reversed artwork, so it is numbered clockwise viewed from its bump side. Since this chip is mounted face down, the resulting assembly still has the same counter–clockwise order viewed from above the component surface. All chips have the same size and bonding pad spacing. See Figure 4 for dimensions.

Figure 3. Internal Schematic

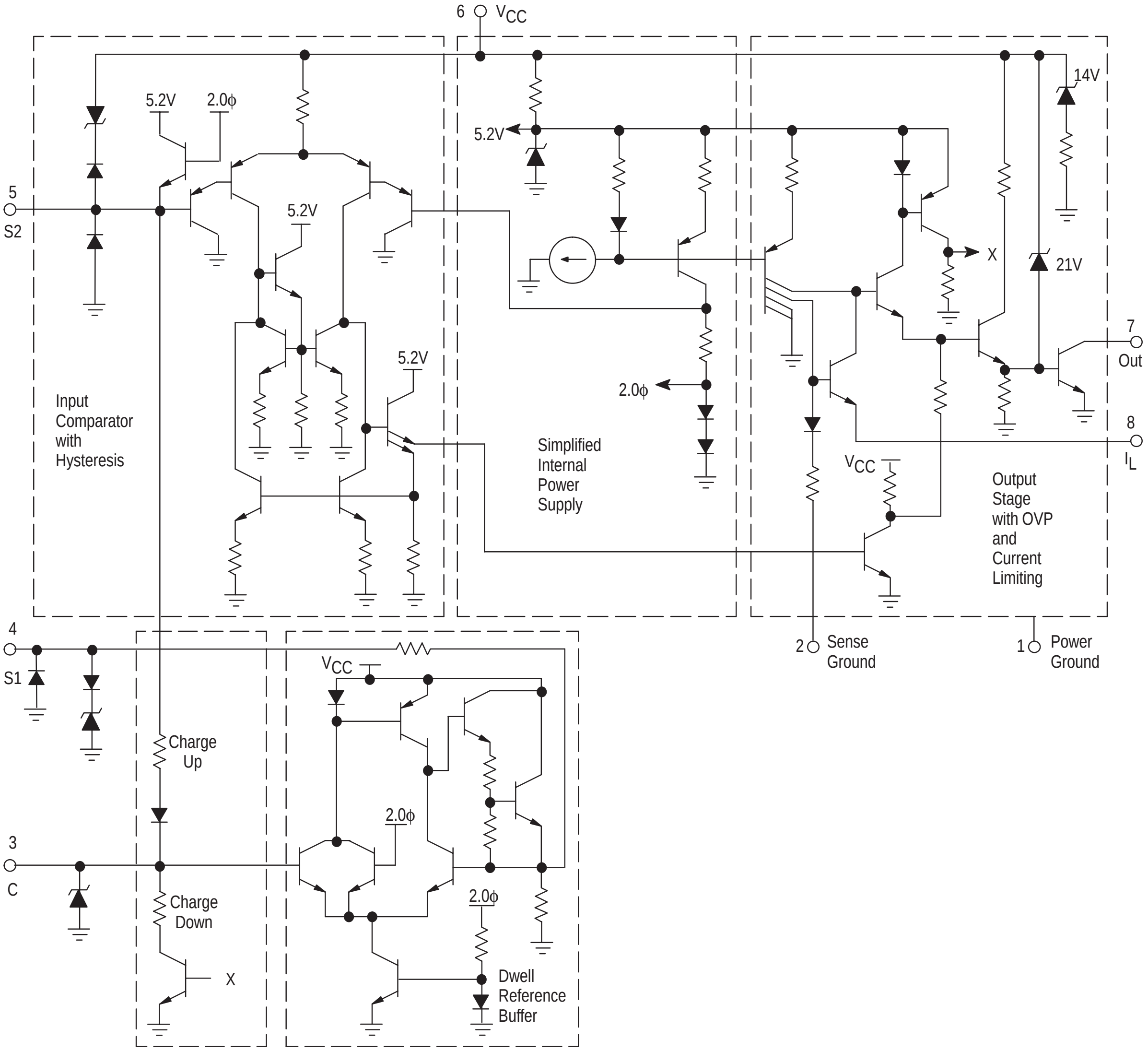
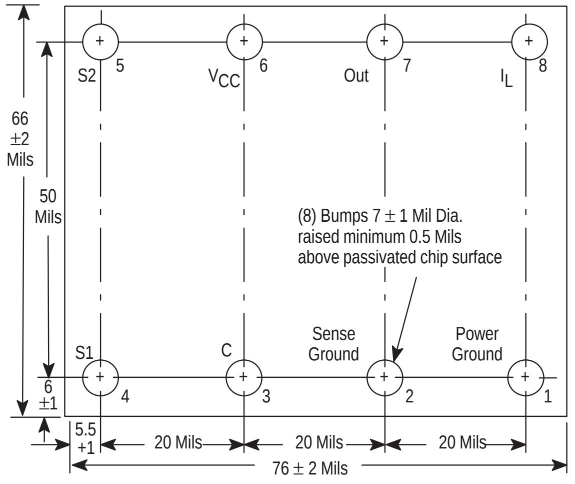


Figure 4. MCCF3334 Ignition Circuit Bump Side View



(8) Bumps 7 ± 1 Mil Dia.
raised minimum 0.5 Mils
above passivated chip surface

MOTOROLA

MC3392

Low Side Protected Switch

The MC3392 is a low side protected switch designed for use in harsh automotive applications which require the capability of handling high voltages attributed to load and field dump transients, in addition to reverse and double battery conditions. The three terminal TO–220 is intended to replace power Darlington transistors in new and existing switching applications when taking into account the CMOS input levels required by the MC3392. It offers improved functionality and ruggedness over power Darlingtons while retaining the same package and pin configuration, and can be used as a replacement in many applications using the industry standard TIP100/101 NPN power Darlington transistor.

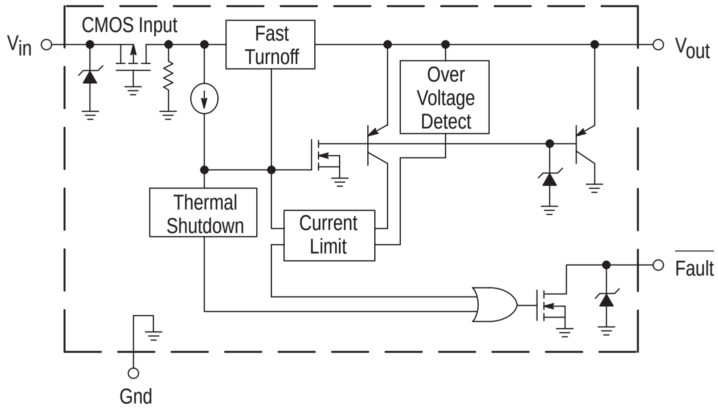
The five–terminal TO–220 has the added feature of having a $\overline{\text{Fault}}$ output (active low) which will indicate the existence of an over temperature, over–voltage or current limit condition, including an output short to ground.

When driving a moderate load, the MC3392 performs as an extremely high gain, low saturation Darlington transistor having CMOS input levels. The primary advantage of the MC3392 over a Darlington transistor is the additional protection afforded the device and load when driving difficult or faulty loads. This device incorporates unique internal current limit and thermal protection circuitry to safeguard itself and the associated load from catastrophic failure.

The MC3392 is available in a three and five–lead TO–220 package; the five–lead having the added diagnostic feature. The full featured MC3392 is also available in a 16 pin wide body SOIC plastic power package.

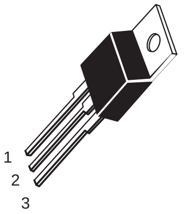
- Designed for Automotive Applications
- Can Be Used as a Replacement for TIP100/101 NPN Power Darlingtons
- Drives Inductive Loads without External Clamp Circuitry
- Withstands Negative and Positive Transient Voltages
- Low ON Voltage
- CMOS Logic Compatible Input
- Over Current, Overvoltage, and Thermal Protection
- Extended Operating Temperature Range
- $\overline{\text{Fault}}$ Output

Simplified Block Diagram



LOW SIDE PROTECTED SWITCH

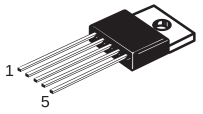
SEMICONDUCTOR TECHNICAL DATA



Pin 1. Input
2. Output
3. Ground

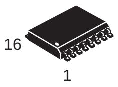
(Heatsink surface connected to Pin 3)

T SUFFIX
PLASTIC PACKAGE
CASE 221A
(TO–220)



Pin 1. $\overline{\text{Input}}$
2. Fault
3. Ground
4. NC
5. Output

T–1 SUFFIX
PLASTIC PACKAGE
CASE 314D
(TO–220)



Pin 1. NC
2. NC
3. NC
4. Output
5. $\overline{\text{Input}}$
6. Fault
7. NC
8. NC
9–16. Ground

DW SUFFIX
PLASTIC PACKAGE
CASE 751G
SOP(8+8)L

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC3392T	T_A = – 40° to +125°C	Plastic Power
MC3392T–1		Plastic Power
MC3392DW		SOP(8+8)L

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage Range	V_{in}	– 0.5 to + 6.5	V
Output Transient Breakdown Voltage – Forward – Reverse	V_{BF} V_{BR}	+ 60 – 80	V
Short Circuit Current	I_{SC}	2.2	A
Output Avalanche Energy (Note 1)	E_{max}	60	mJ
Minimum ESD Voltage Capability (Note 2)	ESD	2000	V
Operating Junction Temperature Internally Limited (Note 3)	T_J	150	°C
Storage Temperature	T_{stg}	– 65 to +150	°C
Operating Ambient Temperature Range	T_A	– 40 to +125	°C
Thermal Resistance (Notes 4, 5)			°C/W
TO–220: Junction–to–Ambient	$R_{\theta JA}$	62.5	
Junction–to–Case	$R_{\theta JC}$	2.5	
SOP: Junction–to–Ambient	$R_{\theta JA}$	118	
Junction–to–Case	$R_{\theta JC}$	59	

NOTES: 1. Capability for both positive and negative repetitive transient pulses.
2. ESD testing performed in accordance with Human Body Model (C_{Zap} = 100 pF, R_{Zap} = 1500 Ω).
3. This device incorporates internal circuit techniques which do not allow the internal junction temperature to reach destructive temperatures.
4. The thermal resistance case is considered to be a point located near the center of the tab and plastic body of the TO–220 or a point on one of the heatsink leads (Pins 9 to 16) of the SOP.
5. The SOP thermal information is based on simulation data.

ELECTRICAL CHARACTERISTICS (Limit values are noted under conditions: – 40°C ≤ T_A ≤ +125°C. Typical denotes calculated mean value derived from 25°C parametric data, unless otherwise noted.)

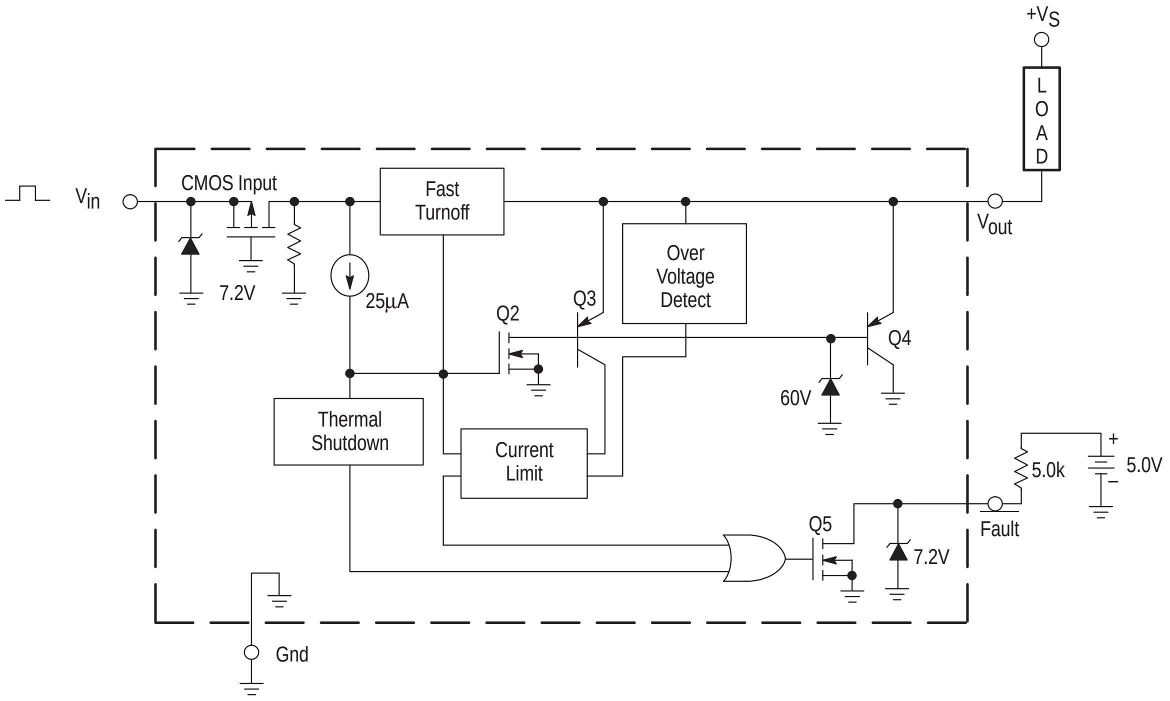
Characteristics	Figure	Symbol	Min	Typ	Max	Unit
Input Control Current	3	I_{in}				µA
V_{in} = 1.0 V			–	0.2	10	
V_{in} = 4.0 V			–	230	350	
V_{in} = 5.0 V			–	260	500	
Input Voltage High (On)	7	V_{IH}	4.0	2.0	–	V
Input Voltage Low (Off)		V_{IL}	–	2.0	1.0	
Output Leakage Current $+V_S$ = 28 V, R_L = 0	4	I_L	–	1.3	100	µA
Output Short Circuit Current $+V_S$ = 14 V, R_L = 0	5	I_{SC}	1.0	1.3	2.2	A
Output On Voltage (V_{in} = 4.0 V, Note 6)	6	V_{OL}				V
I_O = 400 mA			–	0.95	1.1	
I_O = 800 mA			–	1.1	1.8	
Output Clamp Voltage I_O = 100 mA	8	V_{OC}	60	70	80	V
Reverse Leakage Current V_{out} = –13 V	9	I_{BR}	–	–10	– 30	mA
Fault Output Sink Saturation (I_{Sink} = 100 µA, V_{in} = 5.0 V)	10	$V_{DS(sat)}$	–	0.3	0.4	V
Fault Output Off–State Leakage (V_{DS} = 5.0 V)		$I_{DS(leak)}$	–	0.6	100	µA
Turn–On Time 10% to 90% of I_O (400 mA Nominal)	11	t_r	–	3.3	20	µA
Turn–Off Time 90% to 10% of I_O (400 mA Nominal)	12	t_f	–	9.7	25	
Propagation Delay Time Input to Output (Turn–On/Turn–Off, 50%)	–	t_d	–	3.0	10	

NOTE: 6. I_O is defined as the output sink current.

PIN FUNCTION DESCRIPTION

Name	Pin Number			Description
	3–Pin	5–Pin	16–Pin	
V_{in}	1	1	5	CMOS compatible input. Pins 1, 2, 3, 7, 8 no connection on 751G.
V_{out}	2	5	4	Output to load and battery, protected by a 60 V clamp against inductive load transients.
Gnd	3	3	9 to 16	Ground connection.
$\overline{\text{Fault}}$	–	2	6	Fault output pulled low when the IC is operating in a fault state. The open drain output requires a pull–up resistor for normal operation.

Figure 1. Representative Block Diagram



Definition of Currents and Voltages. Positive current flow is defined as conventional current flow into the device. Negative current flow is defined as current flow out of the device. All voltages are referenced to ground. Both currents and voltages are specified as absolute (i.e., –10 V is greater than –1.0 V).

Figure 2. Fault Output Timing Diagram

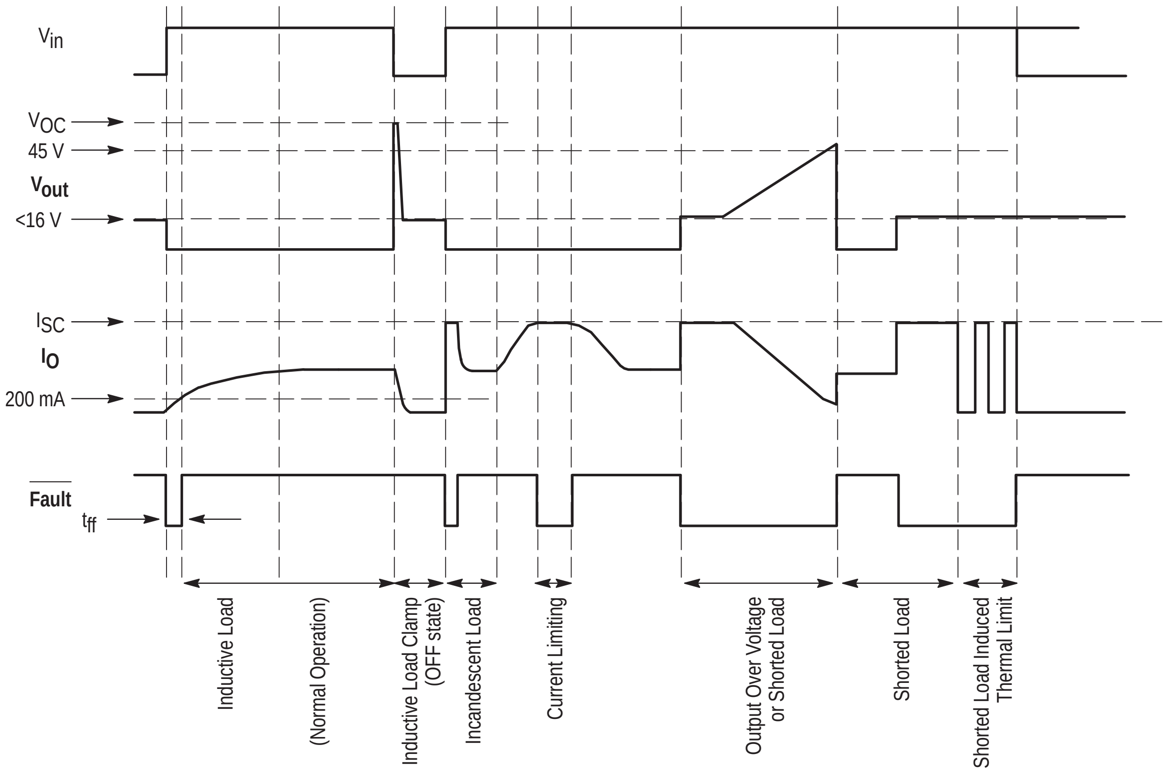


Figure 3. Input Control Current versus Input Voltage

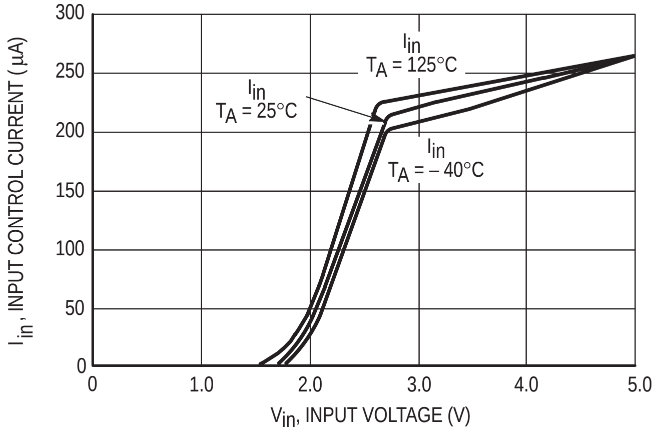


Figure 4. Output Leakage Current versus Temperature

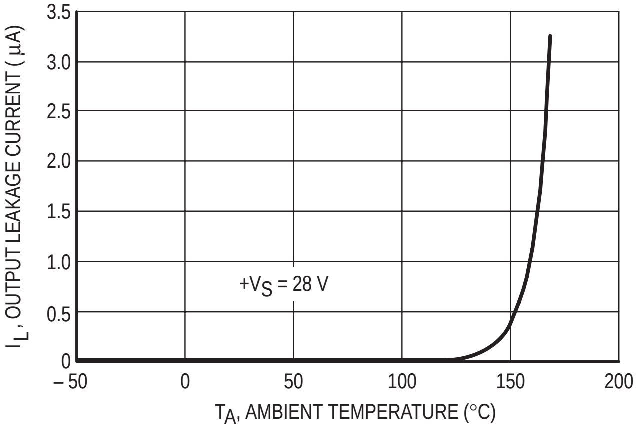


Figure 5. Output Short Circuit Current versus Temperature

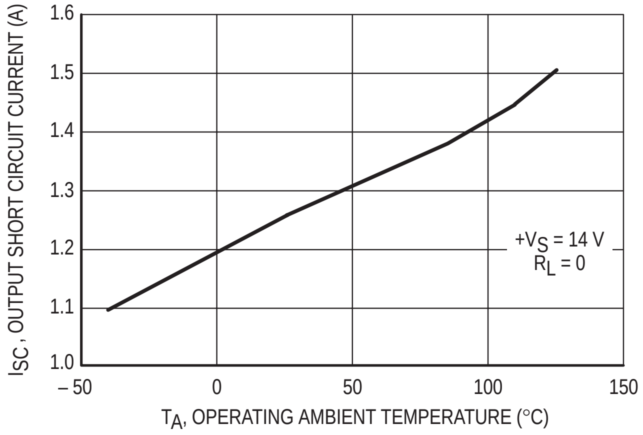


Figure 6. Output On Voltage versus Temperature

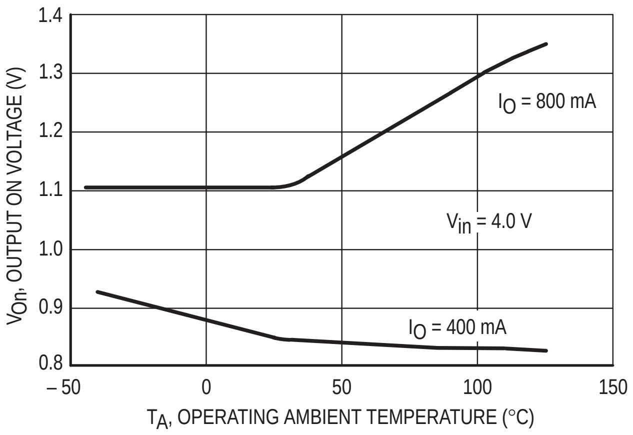


Figure 7. Input Voltage versus Temperature

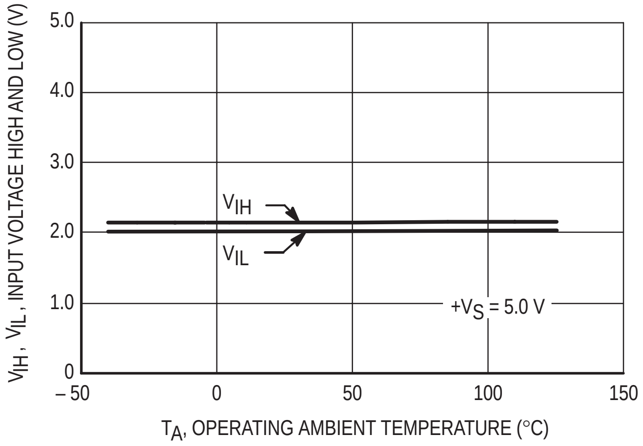


Figure 8. Output Clamp Voltage versus Temperature

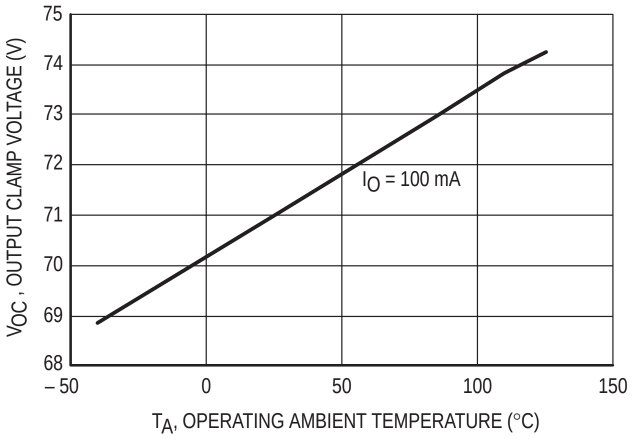


Figure 9. Reverse Breakdown Voltage versus Temperature

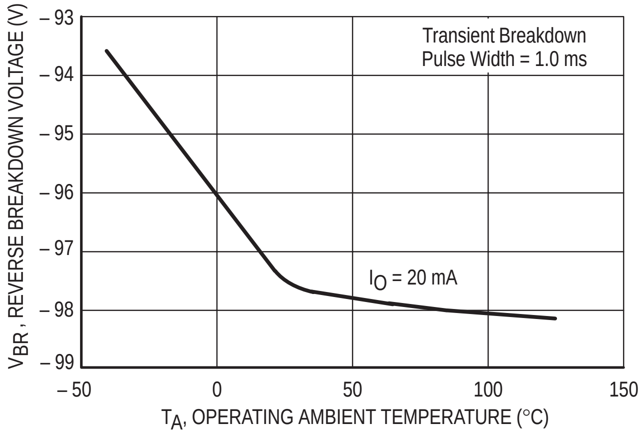


Figure 10. $\overline{\text{Fault}}$ Output Saturation versus Sink Current

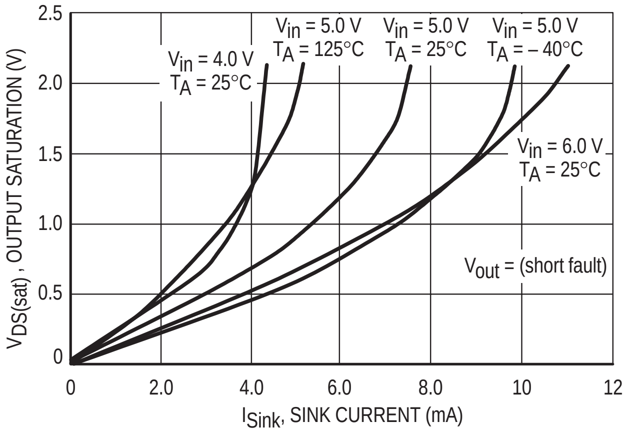


Figure 11. Turn–On Waveform

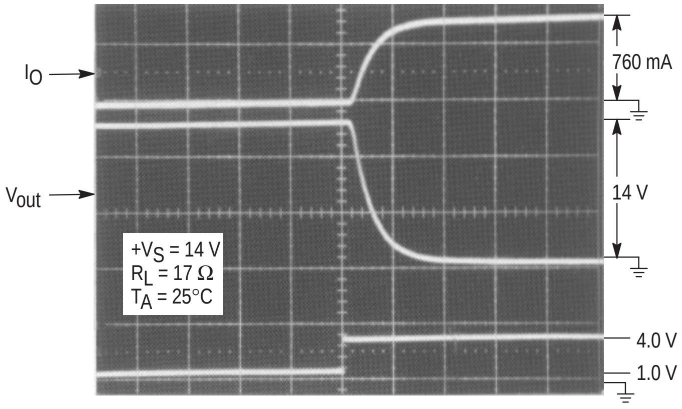


Figure 12. Turn–Off Waveform

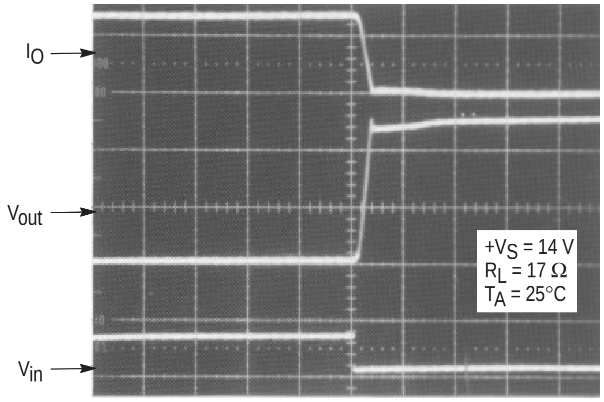


Figure 13. Output Current versus Supply Voltage

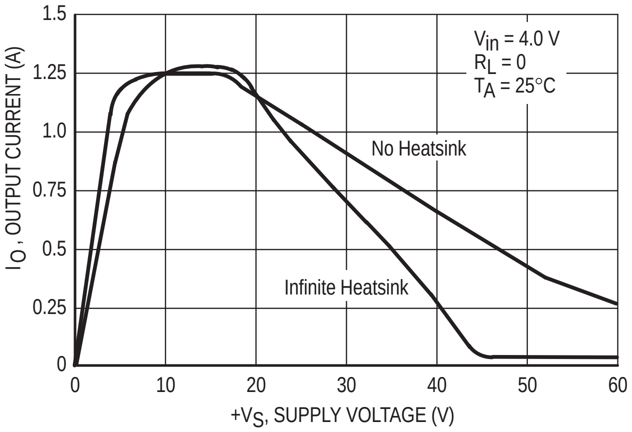
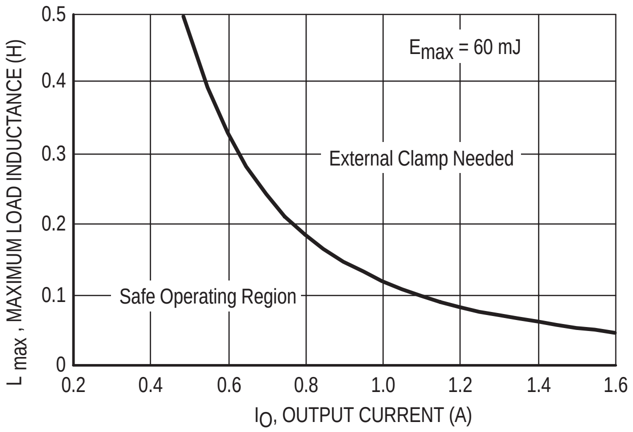


Figure 14. Maximum Load Inductance versus Output Current



TECHNICAL DISCUSSION

Introduction

The MC3392 is a low side protected switch incorporating many features making it ideal for use in harsh automotive applications. The protection circuitry of the MC3392 protects not only itself but also the associated load from destructive voltage transients attributed to load and field dump, as well as reverse and double battery conditions found in automotive applications. The MC3392 is unique in that the protection circuitry is internal and does not require additional external protection components for its operation. This makes the device very cost effective because its application utilizes few external components, thus reducing cost and space requirements needed for the system. The MC3392 is extremely effective when used to drive solenoids, as well as incandescent lamp loads. The following description of the device's operation is in reference to the functional blocks of the Representative Block Diagram shown in Figure 1.

CMOS Input

The input of the MC3392 is CMOS compatible. Input control performs as true logic. When the input (V_{in}) is less than 1.0 V the MC3392 switch is in a high impedance or OFF state. When V_{in} is greater than 4.0 V, is in a low impedance or ON state. The switching threshold of the input is approximately 2.0 V and is graphed in Figure 7. With the input at 4.0 V, the input sink current will be approximately 250 µA. In the ON state, the internal protection circuitry is activated and all of the protection features are available for use. In the OFF state, however, it is important to note that none of the protection features are available, with the exception of the internal inductive load clamp. The input pin is afforded a minimum of 2000 V ESD protection (Human Body Model) by virtue of the 7.2 V zener diode.

Over Temperature Shutdown

Internal Thermal Shutdown Circuitry is provided to protect the MC3392 in the event the Operating Junction Temperature (T_J) exceeds 150°C. Typically, Thermal Shutdown will occur at 160° to 170°C. The thermal shutdown sense element is embedded within the output PNP (Q4) in order to afford very fast thermal coupling of Q4 to the sense element. Any rise in temperature due to the ambient is translated directly to Q4 and the sense element. If the junction temperature rises excessively above 150°C, the Thermal Shutdown circuit will turn ON, quickly pulling the gate of Q2 to ground, which pulls the base of Q4 to ground, turning it OFF. In addition, the Thermal Shutdown circuit simultaneously turns Q5 ON and with a suitable pull–up resistor at the Fault pin reports the presence of a fault (logic low). The output PNP will remain OFF until the junction temperature decreases to within the operating range at which time Thermal Shutdown turns OFF, ceasing to hold the gate of Q2 low, turning Q4 back ON. This process will repeat as long as the thermal over load exists. This mode of operation is a nondestructive safety feature of the device and will correct itself real time when the cause of over temperature is removed. A continued over temperature condition will thermally Pulse Width Modulate (PWM) the output and Fault and may be incorrectly interpreted as an oscillating load if one does not consider the simultaneous performance of the Fault pin.

Current Limit

The MC3392 protects itself against V_{out} to $+V_S$ hard shorts as well as any over current conditions by reducing the magnitude of output current (I_O) to that of the short circuit current limit value (I_{SC}). When the output current monitored by Q3 tries to exceed I_{SC}, the Current Limit circuit lowers the gate voltage of Q2, lowering the base of Q4, causing the load current through Q4 to diminish. Simultaneously, when the load current exceeds I_{SC}, Q5 will turn ON reporting a fault condition. If the output current is allowed to remain excessively high for the degree of heatsinking incorporated, and the junction temperature of the device is allowed to heat beyond 150°C, the Thermal Shutdown circuit will activate and the output will thermally PWM. Again, these modes of operation are safety features of the MC3392 and are not destructive.

Overvoltage Detect

This circuitry protects the MC3392 from V_{out} voltages in excess of 16 V by lowering the output current to a nondestructive value. With increasing V_{out} voltage ($16\ V < V_{out} < 45\ V$) the load current is reduced to below that of I_{SC} and produces a fold back current effect. As V_{out} increases in excess of 16 V, the output current decreases linearly until V_{out} exceeds 45 V. With an infinite heatsink and $V_{out} > 45$ V, I_O will be less than 100 mA. For the other extreme, no heatsink and $V_{out} > 45$ V, I_O can be expected to be less than about 400 mA. This behavior of I_O in relation to V_{out} is shown in Figure 13.

For the infinite heatsink case, the output current initially increases with increased voltage until V_{out} exceeds 16 V, thereafter the behavior is expressed as,

$$I_O = I_{SC}\ [1 – (V_{out} – 16\ V) / 30\ V]$$

Beyond 45 V, I_O is limited to less than 100 mA. Anytime the Overvoltage Detect circuit is activated, the gate of Q5 is pulled low causing Q5 to turn ON to report the fault at the Fault pin.

Inductive Load Clamp

The MC3392 has an internal inductive load clamp for protection against flyback voltages imposed on the output pin in excess of 70 V. The incorporated zener clamp can quickly dissipate up to 60 milli–Joules of inductive flyback energy. Figure 14 shows the maximum inductive load versus load current that the clamp can handle safely. As an example (using Figure 14), if operating the MC3392 to drive a 0.33 H inductor, the maximum load current should be adjusted to 600 mA or less. If the load current is too high for the inductor used, some series resistance can be added to the load to limit the current. If this is not possible, an external clamp must be used to facilitate handling the higher energy. When using an external clamp, the external clamp voltage must be less than 60 V so as to override the internal clamp. The output clamp offers protection for the output when the MC3392 is in the OFF state. During the ON state, other protection features (Overvoltage, Current, and Temperature) are available to protect the output.

Fault Logic

The Fault is comprised of an internal open drain FET requiring an external pull–up resistor. Typically, a 5.0 k pull–up resistor to a +5.0 V supply is satisfactory. The Fault pin is afforded a minimum of 2000 V ESD protection (Human Body Model) by virtue of the 7.2 V zener diode. The Fault will report a fault (logic low state) whenever the MC3392 experiences a fault condition. Conditions producing a fault are: $I_O > 1.3$ A (over current/shorted load); $T_J > 150$°C (over temperature); and $V_{out} > 16$ V (overvoltage).

If the device goes into Thermal Shutdown, caused by environmental overheating (not resulting from another fault condition), the Fault and V_{out} will thermally PWM as the MC3392 repeatedly heats to shut off, cools, and again turns on. If a current limit fault causes the device to go into Thermal Shutdown, the output will oscillate while the Fault remains pulled low. There is no thermal hysteresis designed in to control the PWM effect and this fault mode of operation is not destructive.

Fast Turn–Off

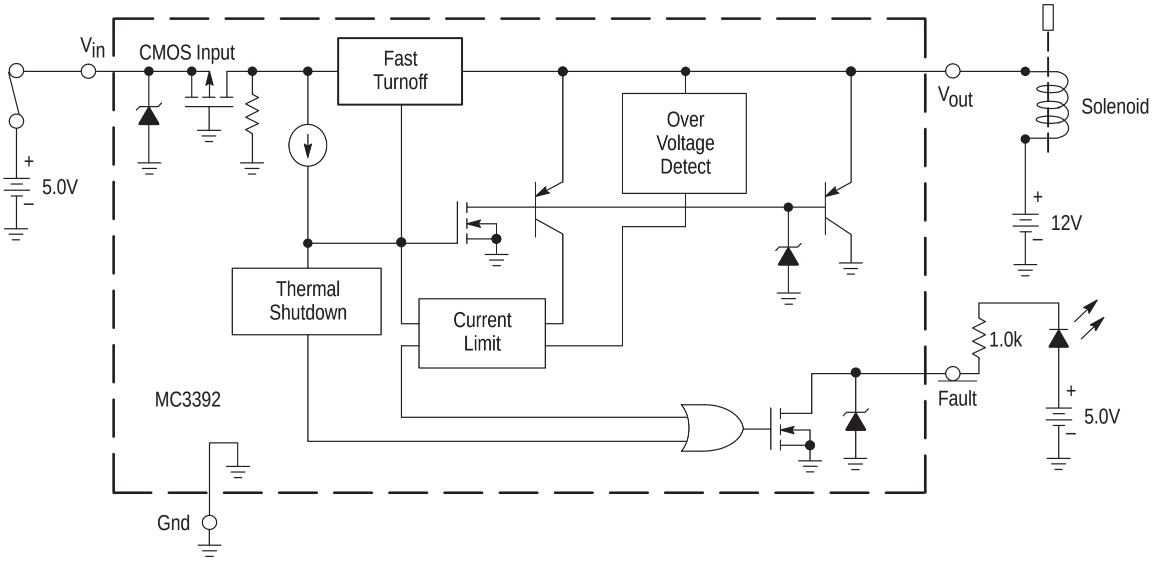
This circuitry enhances the MC3392 turn–off performance. Whenever V_{in} goes to a logic low state, V_{out} is held in an OFF state for approximately 15 µs. During fast turn–off, less than 30 mA of current is allowed to flow producing an abrupt turn–off. This turn–off characteristic can be seen in Figure 12, a photograph of the typical turn–off waveform.

APPLICATIONS INFORMATION

Solenoid Driver

The MC3392 can be used to drive a variety of solenoid applications similar to that of Figure 15. For example; driving a solenoid having an inductance of 73.8 mH and a resistance of 95 Ω from a 12 V supply will cause 240 mA of sink current to flow with the MC3392 in the ON state. The resulting current value is within the normal load current operating region and will not produce a fault. Load current is paramount in any design using the MC3392 and must be less than I_{SC} for acceptable operation. If the load current is greater than I_{SC}, a current limit fault state will exist. Operation in this state is not destructive as the device will turn off if the Junction Temperature (T_J) rises above 150°C. When the Junction Temperature cools below 150°C the device will again turn–on, with a repeat of the cycle. Careful design to acceptable load current limits should be insured for satisfactory operation of an application.

Figure 15. Solenoid Driver

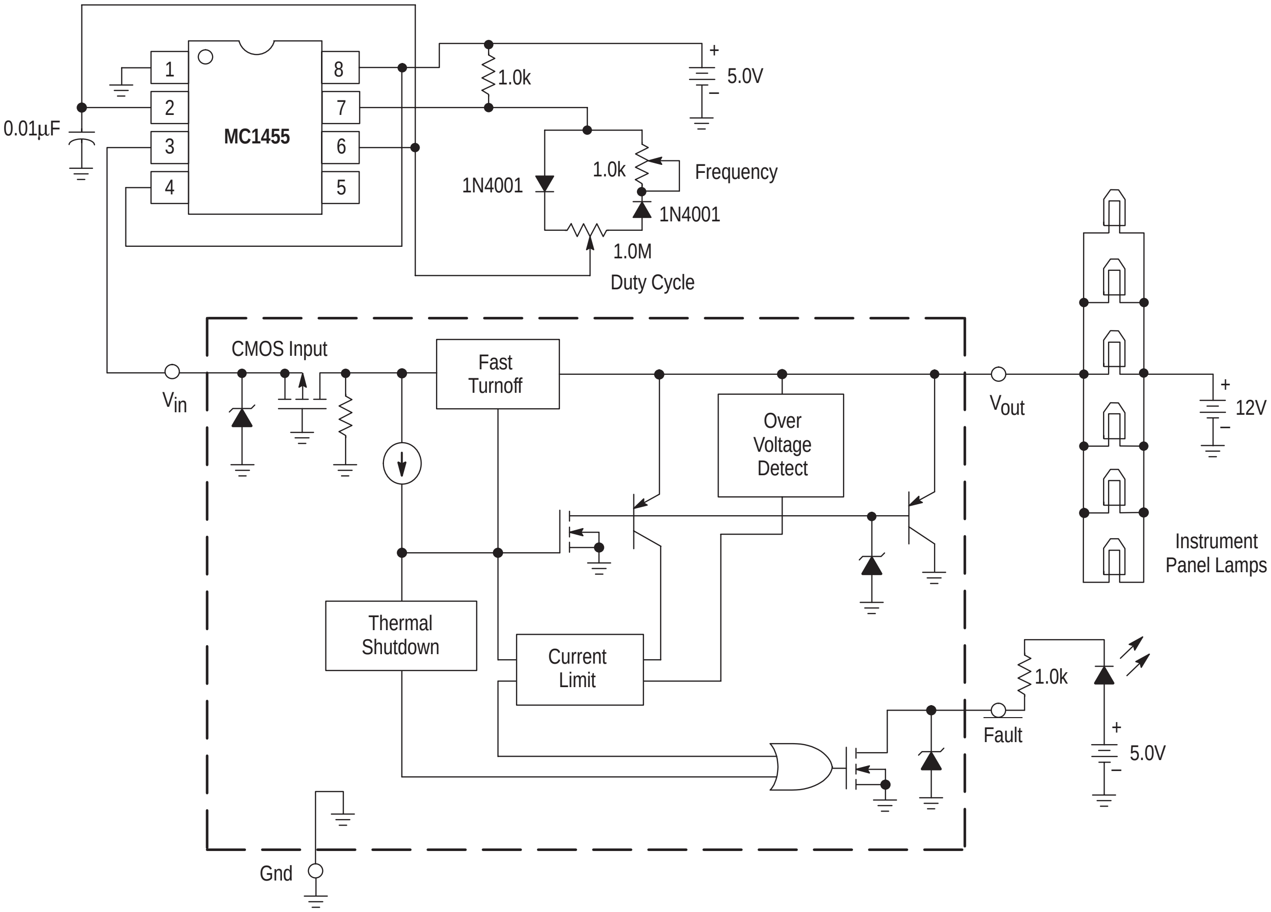


Instrument Panel Lamp Dimmer Control

The MC3392 can be used to control the dimming function associated with instrument panel lamps. The brightness of incandescent lamps can be varied by pulse width modulating the input of the MC3392. The modulating signal for the MC3392 can be obtained directly from a microprocessor or, as in Figure 16, from an MC1455 timer. The MC1455 timer is configured as a free–running clock having both frequency and duty cycle control. The typical timer frequency is approximately 80 Hz when the frequency potentiometer is adjusted to 1.0 k. This frequency was chosen so as to avoid any perceptible lamp flicker. The duty cycle potentiometer controls the duty cycle over a range of approximately 3.0% to 97%; When at 3.0% duty cycle, the lamps are essentially off; When at 97% duty cycle, the lamps are essentially full lit. Six incandescent lamps are shown in this application drawing 720 mA total current. Similar applications can be used to drive a variety of lamp loads. The total load current is the primary factor of consideration when driving lamp loads. The total value of I_O must be less than I_{SC}.

Another convenient aspect of this application is the LED. The LED can be used to denote the existence of a system fault (overvoltage, current limiting, or thermal shutdown).

Figure 16. Instrument Panel Lamp Dimmer Control



MOTOROLA

MC3399

Automotive Half-Amp High-Side Switch

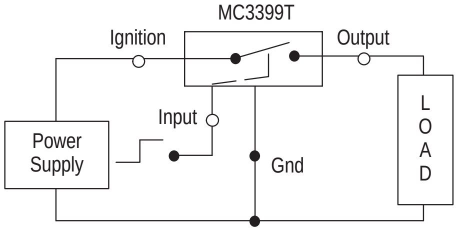
The MC3399 is a High–Side Switch designed to drive loads from the positive side of the power supply. The output is controlled by a TTL compatible input Enable pin. In the “on” state, the device exhibits very low saturation voltages for load currents in excess of 750 mA. The device isolates the load from positive or negative going high voltage transients by abruptly “opening” thus protecting the load from the transient voltage for the duration of the transient. The device automatically re–establishes its original operating state following the transient condition.

The MC3399 is fabricated on a power BIMOS process which combines the best features of Bipolar and MOS technologies. The mixed technology provides higher gain PNP output devices and results in Power Integrated Circuits having substantially reduced quiescent currents.

The device operates over a wide power supply voltage range and can withstand voltage transients (positive or negative) of ±100 V. A rugged PNP output stage along with active clamp circuitry, output current limit and thermal shutdown permit the driving of all types of loads, including inductive. The MC3399 is offered in 5–lead TO–220 and 16–lead SOIC plastic packages to facilitate either “thru–hole” or surface mount use. In addition, it is specified over a wide ambient operating temperature of –40°C to +125°C and is ideally suited for industrial and automotive applications where harsh environments exist.

- Low Switch Voltage Drop
- Load Currents in Excess of 750 mA
- Low Quiescent Current
- Transient Protection Up to ± 100 V
- TTL Compatible Enable Input
- On–Chip Current Limit and Thermal Shutdown Circuitry

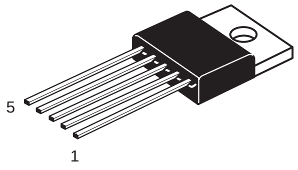
Representative Block Diagram



This device contains 52 active transistors.

AUTOMOTIVE HALF–AMP HIGH–SIDE SWITCH

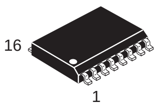
SEMICONDUCTOR TECHNICAL DATA



Pin 1. Ignition
2. Output
3. Output
4. Ground
5. Input

T SUFFIX
PLASTIC PACKAGE
CASE 314D

Pins 2 and 3 connected to package tab.



Pin 1. Ignition
2. N.C.
3. N.C.
4. N.C.
5. Ground
6. N.C.
7. Input
8. N.C.
9. Output
10. Output
11. Output
12. Output
13. Output
14. Output
15. Output
16. Output

DW SUFFIX
PLASTIC PACKAGE
CASE 751G
SOP(8+8)L

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC3399DW	T_A = – 40° to +125°C	SOP(8+8)L
MC3399T		Plastic Power

MAXIMUM RATINGS

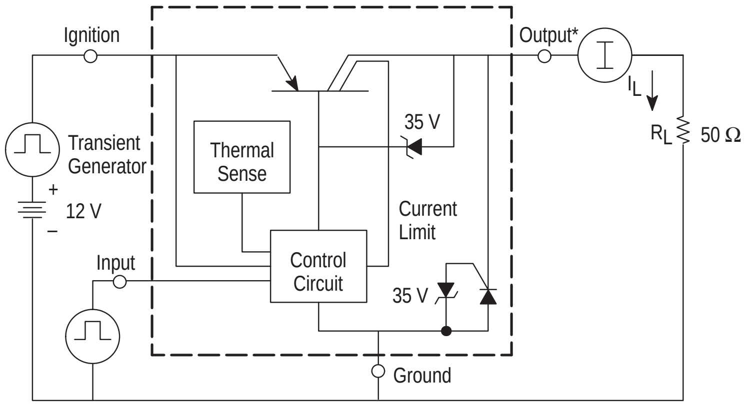
Rating	Symbol	Value	Unit
Ignition Input Voltage (Continuous)	V_{IGN}		Vdc
Forward		25	
Reverse		–16	
Ignition Input Voltage (Transient)	V_{IGN}		V
		±60	
		±100	
Input Voltage	V_{in}	–0.3 to +7.0	V
Output Current	I_O	Internally Limited	A
Thermal Resistance			°C/W
Plastic Power Package (Case 314D)			
Junction–to–Ambient	$R_{\theta JA1}$	65	
Junction–to–Tab	$R_{\theta JT}$	5.0	
SOP(8+8)L Plastic Package (Case 751G)			
Junction–to–Ambient	$R_{\theta JA2}$	138	
Junction–to–Lead 12	$R_{\theta JL}$	52	
Soldering Temperature (for 10 Seconds)	T_{solder}	260	°C
Junction Temperature	T_J	–40 to +150	°C
Storage Temperature	T_{stg}	–65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{IGN} = 12 V, I_L = 150 mA, –40°C ≤ T_A = +125°C, V Input = “1”, unless otherwise noted.)(1)

Characteristic	Symbol	Min	Typ	Max	Unit
Operating Voltage	$V_{IGN(min)}$	4.5	–	–	V
Switch Voltage Drop (Saturation)	$V_{IGN}–V_O$				V
V_{IGN} = 4.5 V I_O = 150 mA, T_A = 25°C		–	0.2	0.5	
I_O = 200 mA, T_A = –40°C		–	0.3	0.5	
I_O = 125 mA, T_A = 125°C		–	0.3	0.5	
V_{IGN} = 12 V I_O = 425 mA, T_A = 25°C		–	0.3	0.7	
I_O = 550 mA, T_A = –40°C		–	0.3	0.7	
V_{IGN} = 16 V I_O = 375 mA, T_A = 125°C		–	0.4	0.7	
Quiescent Current	I_{GND}				mA
V_{IGN} = 12 V I_O = 150 mA, T_A = 25°C		–	12	50	
I_O = 550 mA, T_A = –40°C		–	25	100	
I_O = 300 mA, T_A = 125°C		–	10	50	
Output Current Limit (V_O = 0 V)	I_{SC}	–	1.6	2.5	A
Output Leakage Current (V_{IGN} = 12 V, Input = “0”)	I_{Leak}	–	10	150	µA
Input Voltage				–	V
High Logic State	V_{IH}	2.0	–		
Low Logic State	V_{IL}	–	–	0.8	
Input Current					µA
High Logic State (V_{IH} = 5.5 V)	I_{IH}	–	120	–	
Low Logic State (V_{IL} = 0.4 V)	I_{IL}	–	20	–	
Output Turn–On Delay Time Input = “0” → “1”, T_A = +25°C (Figures 1 and 3)	$t_{DLY(on)}$	–	50	–	µs
Output Turn–Off Delay Time Input = “1” → “0”, T_A = +25°C (Figures 1 and 3)	$t_{DLY(off)}$	–	5.0	–	µs
Overvoltage Shutdown Threshold	$V_{in(OV)}$	26	31	36	V
Output Turn–Off Delay Time (T_A = + 25°C) to Overvoltage Condition, V_{in} stepped from 12 V to 40 V, V ≤ 0.9 V_O (Figures 1 and 3)	t_{DLY}	–	2.0	–	µs
Output Recovery Delay Time (T_A = + 25°C) V_{IGN} stepped from 40 V to 12 V, V ≥ 0.9 V_O (Figures 1 and 3)	t_{RCVY}	–	5.0	–	µs

NOTES: 1. Typical values represent characteristics of operation at T_A = 25°C.

Figure 1. Transient Response Test Circuit



NOTE: * Depending on load current and transient duration, an output capacitor (C_O) of sufficient value may be used to hold up output voltage during the transient, and absorb turn–off delay voltage overshoot.

Figure 2. Timing Diagram

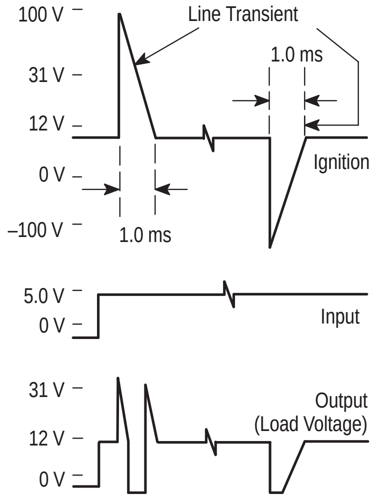


Figure 3. Response Time Diagram

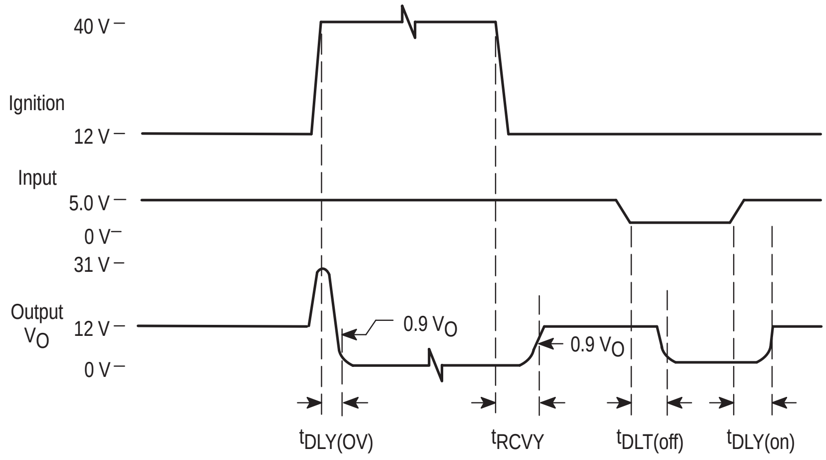


Figure 4. Switch Voltage Drop versus Load Current

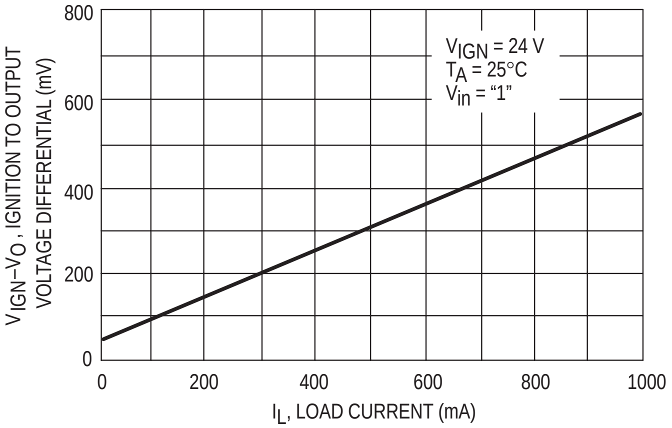
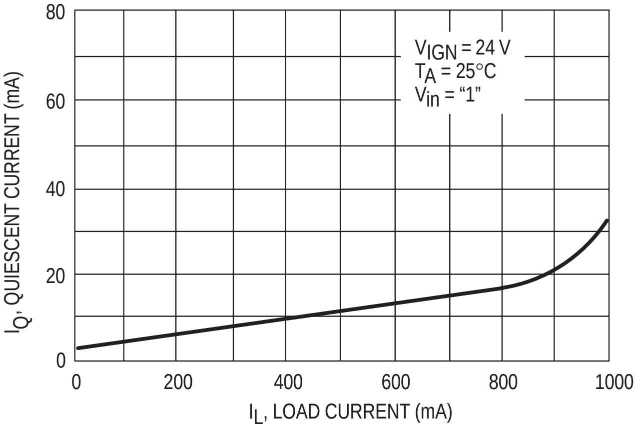


Figure 5. Quiescent Current versus Load Current



MOTOROLA

MC33091A

High-Side TMOS Driver

The MC33091A is a High–Side TMOS Driver designed for use in harsh automotive switching applications requiring the capability of handling high voltages attributed to load and field dump transients, as well as reverse and double battery conditions. Few external components are required to drive a wide variety of N–Channel TMOS devices. The MC33091A, driving an appropriate TMOS device, offers economical system solutions for high–side switching large currents. The MC33091A has CMOS compatible input control, charge pump to drive the TMOS power transistor, basic fault detection circuit, V_{DS} monitoring circuit used to detect a shorted TMOS load, and overcurrent protection timer with associated current squaring circuitry.

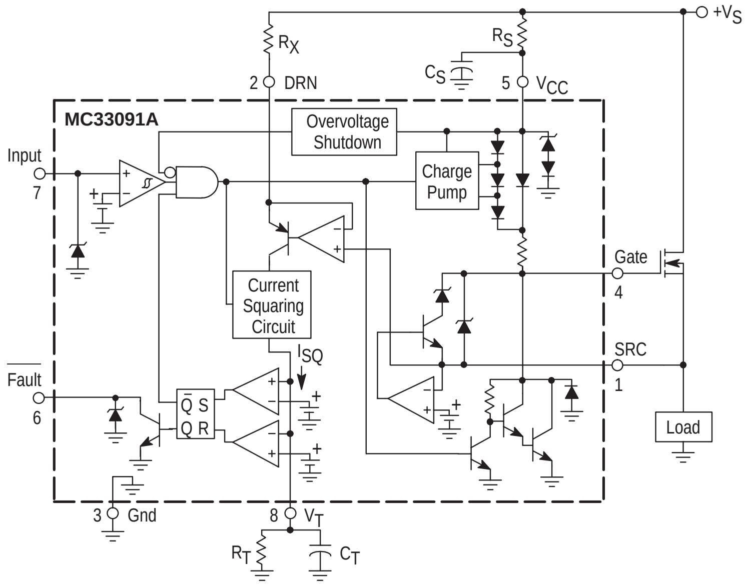
Short circuit protection is made possible by having a unique V_{DS} voltage to current converter drive an externally programmable integrator circuit. This circuit affords fast detection of a shorted load while allowing difficult loads, such as lamps having high in–rush currents, additional time to turn on.

The Fault output is comprised of an open collector NPN transistor requiring a single pull–up resistor for operation. A fault is reported whenever the MOSFET on–current exceeds an externally programmed set level.

The MC33091A is available in the plastic 8–Pin DIP package as well as the plastic 8–Pin surface mount package.

- Designed for Automotive High–Side Driver Applications
- Works with a Wide Variety of N–Channel Power MOSFETs
- Drives Inductive Loads with No External Clamp Circuitry Required
- CMOS Logic Compatible Input Control
- On–Board Charge Pump with No External Components Required
- Shorted Load Detection and Protection
- Forward Overvoltage and Reverse Battery Protection
- Load and Field Dump Protection
- Extended Operating Temperature Range
- Fault Output to Report a MOSFET Overcurrent Condition

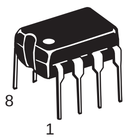
Simplified Block Diagram



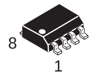
This device contains 54 active transistors.

HIGH–SIDE TMOS DRIVER

SEMICONDUCTOR TECHNICAL DATA

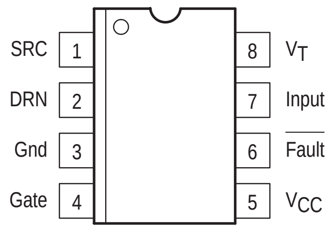


P SUFFIX
PLASTIC PACKAGE
CASE 626



D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

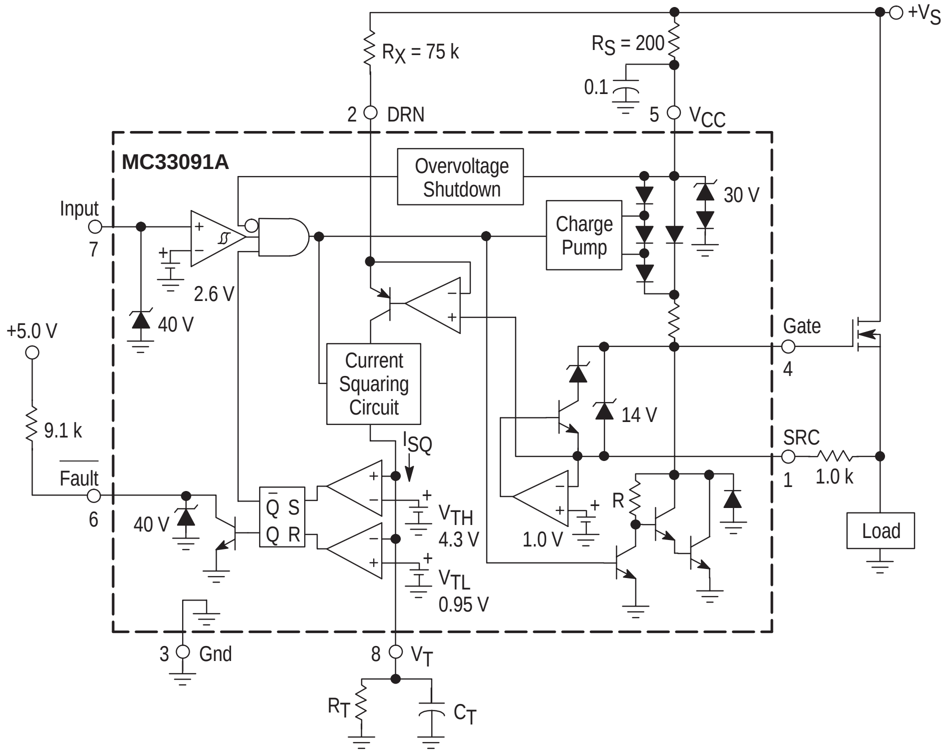
Device	Operating Temperature Range	Package
MC33091AD	T_A = – 40° to +125°C	SO–8
MC33091AP		Plastic DIP

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage (Pin 5) (Note 1) Continuous (Without Activating Clamp)	V_{CC}	–0.7 to 28 7.0 to 28	V
Continuous Supply Clamp Current (Pin 5) DIP Package (Case 626) SO–8 Package (Case 751)	I_C	 10 1.0	mA
Input Control Voltage Range (Pin 7) Continuous	V_{in}	 –0.7 to 28	V
$\overline{\text{Fault}}$ Pull–Up Voltage Range (Pin 6) Continuous	V_{out}	 –0.7 to 28	V
Minimum ESD Voltage Capability (Note 2)	ESD	2000	V
Operating Junction Temperature	T_J	150	°C
Storage Temperature	T_{stg}	–65 to +150	°C
Operating Ambient Temperature Range	T_A	–40 to +125	°C
Thermal Resistance, Junction–to–Ambient DIP Package (Case 626) SO–8 Package (Case 751)	$R_{\theta JA}$	 100 145	°C/W

NOTES: 1. An internal zener diode is incorporated to protect the device from overvoltage transients in excess of 30 V.
2. ESD testing performed in accordance with Human Body Model (C = 100 pF, R = 1500 Ω).

Figure 1. Typical Application



ELECTRICAL CHARACTERISTICS (Values are noted under conditions of 7.0 V ≤ V_{CC} ≤ 24 V, –40°C ≤ T_A ≤ +125°C, unless otherwise noted. Typical values reflect approximate mean at T_A = 25°C at time of device characterization.)

Characteristics	Symbol	Min	Typ	Max	Unit
Supply Current (Note 1)	I_{CC}				
V_{in} = 0 V		–	160	300	µA
V_{in} = 5.0 V (R_X = 100 k)		–	2.5	6.0	mA
Supply Clamp Voltage (Note 2)	V_Z	29	–	35	V
Gate–to–Source Voltage Range (Pin 4)	V_{GS}	8.0	12	15	V
Gate Current (Pin 4)	I_G				µA
$V_G = V_{CC}$		30	–	400	
Gate Saturation Voltage (I_G = 10 µA)	$V_{G(sat)}$	0	1.2	1.4	V
Short Circuit Gate Voltage (Note 4)	I_{GC}	6.4	7.0	7.7	V
Input Control Threshold Voltage (Pin 7)					V
	V_{IL}	–	2.7	1.5	
	V_{IH}	3.5	2.7	–	
Input Control Current (Pin 7) (V_{in} = 5.0 V)	I_{in}	–	100	250	µA
Timer Current Constant (Pin 8)	K				$\mu A/V^2$
(R_X = 100 k, V_T = 0, V_{DS} = 1.0 V) (Note 3)		0.7	1.1	1.5	
Timer (Pin 8)					V
Lower Threshold Voltage	V_{TL}	0.4	0.95	1.2	
Upper Threshold Voltage	V_{TH}	4.3	4.6	5.2	
$\overline{\text{Fault}}$ Sink Current (Pin 6)					
V_F = 5.0 V	I_{OL}	500	–	–	µA
V_F = 0	I_{OH}	–	2.0	100	nA
$\overline{\text{Fault}}$ Saturation Voltage (Pin 6) (I_F = 500 µA)	V_{OL}	–	0.2	0.8	V

NOTES: 1. The total supply current into Pin 2 and Pin 5 with R_X = 100 k (from Pin 2 to supply) and 45 k pull–up resistor from Pin 6 to supply.
2. An internal zener clamp is provided to protect the device from overvoltage transients on the supply line.
3. The timer current constant is the proportionality constant of the voltage to current converter used to monitor the V_{DS} voltage developed across the FET (from Pin 1 to the supply).
4. The gate voltage will be clamped at approximately 7.0 V above the source voltage whenever the source voltage is less than approximately 1.0 V above ground.

Figure 2. Supply Current versus Supply Voltage

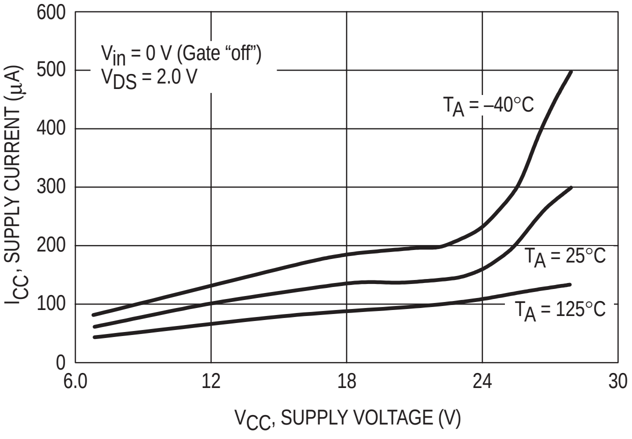


Figure 3. Operating Current versus Supply Voltage

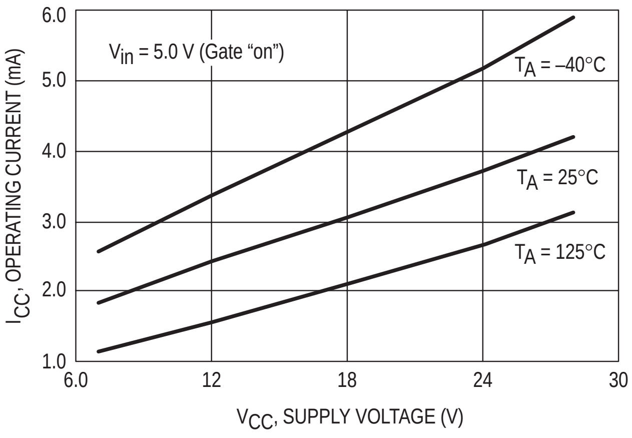


Figure 4. Input Control Current versus Input Control Voltage

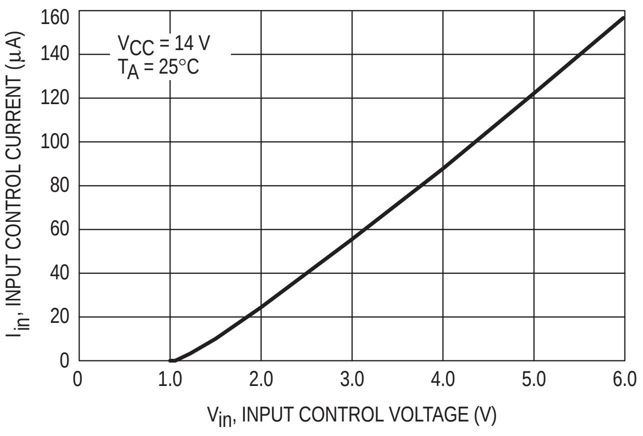


Figure 5. Input Control Current versus Supply Voltage

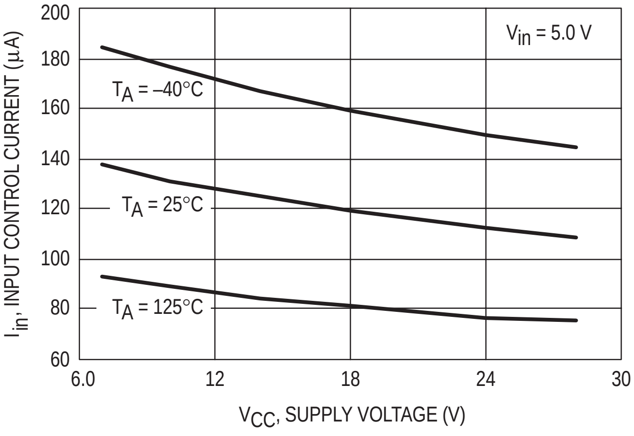


Figure 6. $\overline{\text{Fault}}$ Voltage versus Fault Sink Current

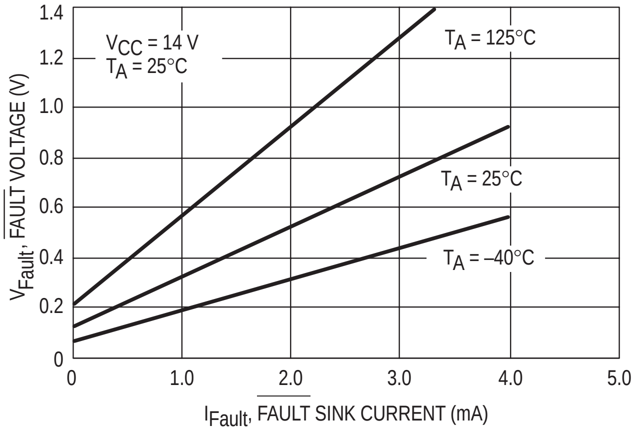


Figure 7. Squaring Constant “K” versus Supply Voltage

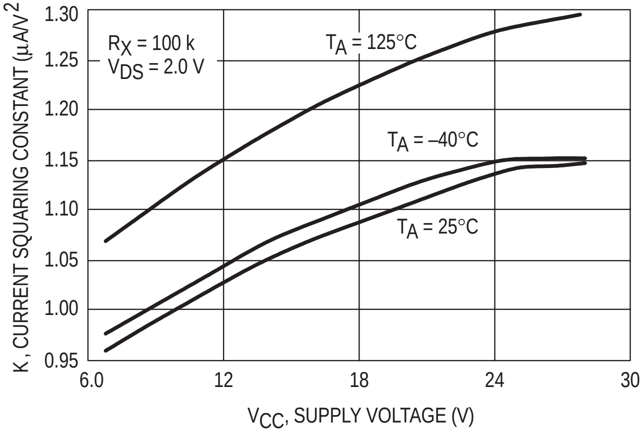


Figure 8. Timer Current versus Drain–to–Source Voltage Squared

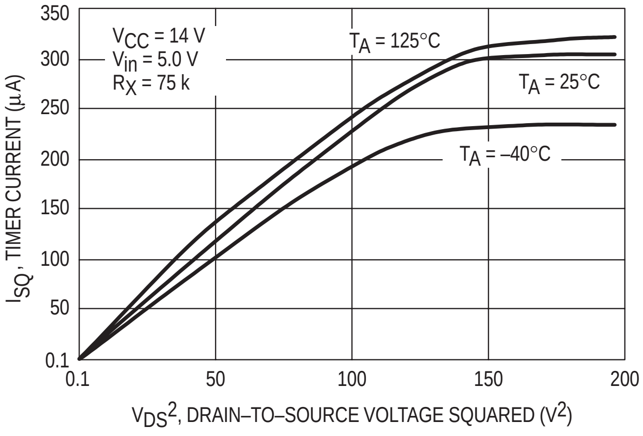


Figure 9. Timer Current versus Drain–to–Source Voltage Squared

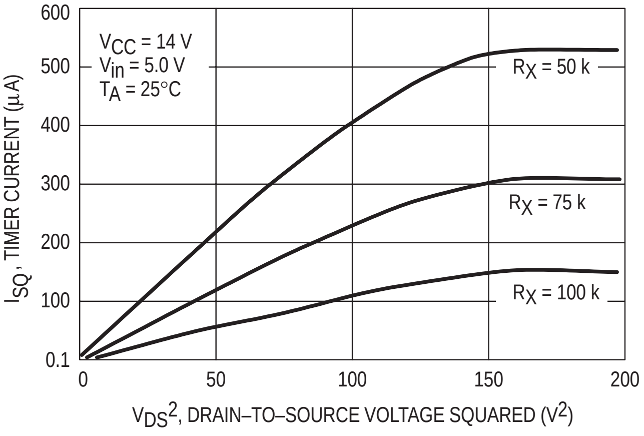


Figure 10. Timer Upper Threshold Voltage versus Temperature

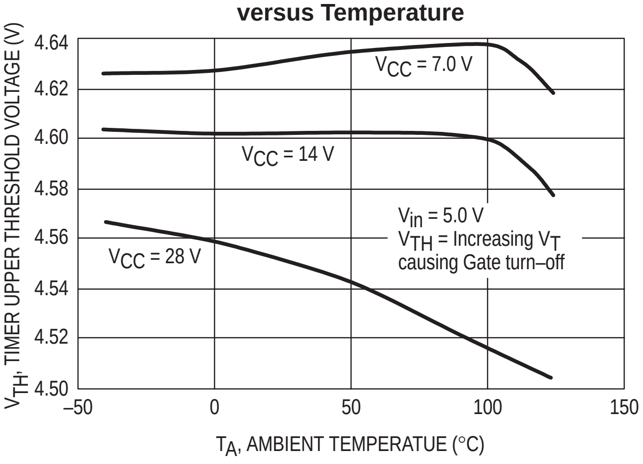


Figure 11. Timer Upper Threshold Voltage versus Supply Voltage

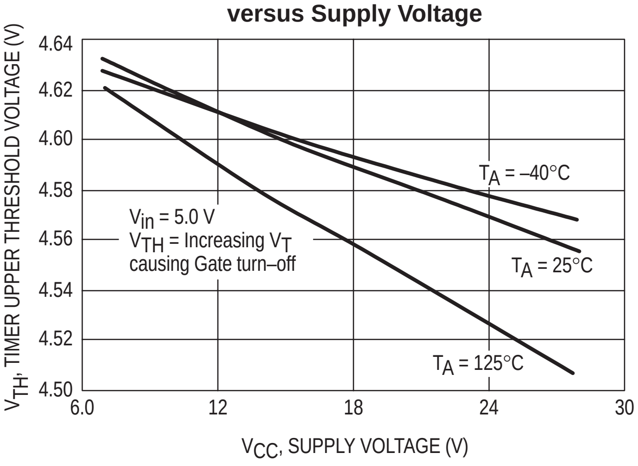


Figure 12. Timer Lower Threshold Voltage versus Temperature

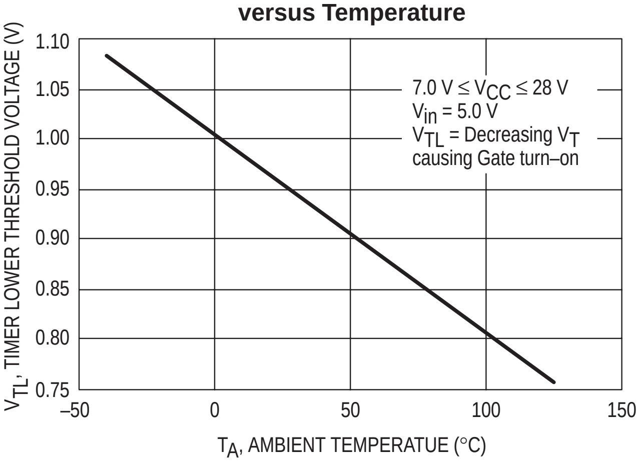


Figure 13. Timer Lower Threshold Voltage versus Supply Voltage

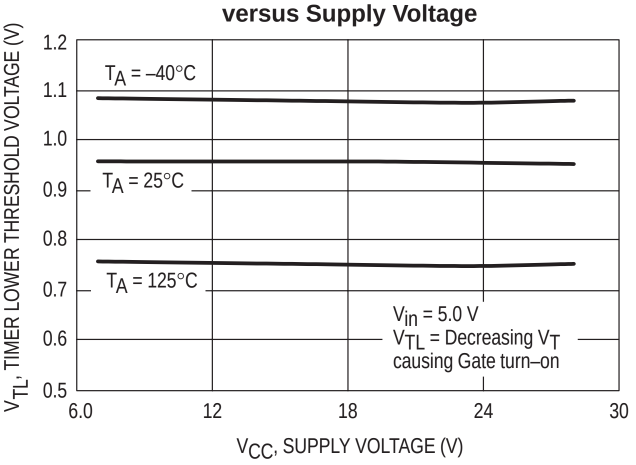


Figure 14. Gate Voltage versus Input Control Voltage

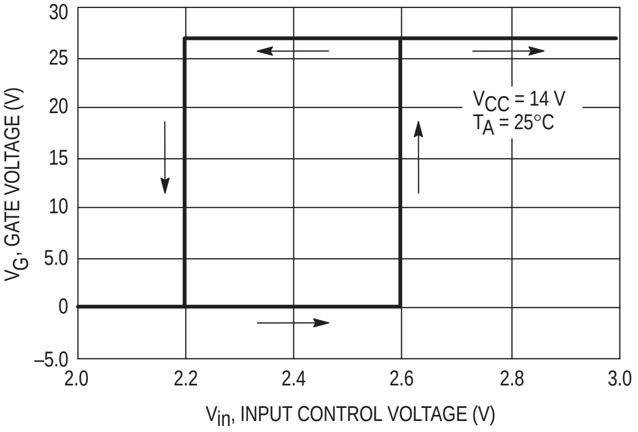


Figure 15. Gate Voltage versus Supply Voltage

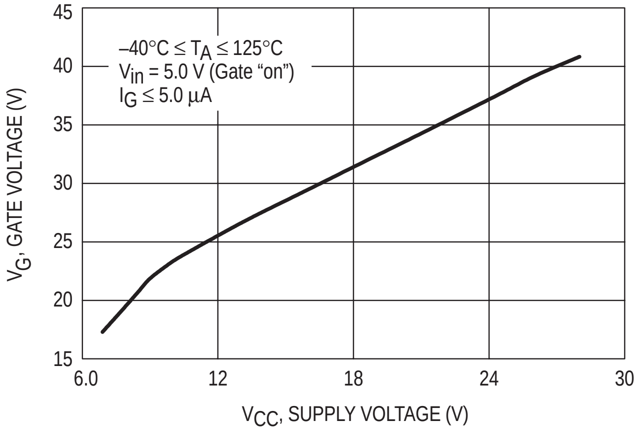


Figure 16. Gate Voltage versus Supply Voltage

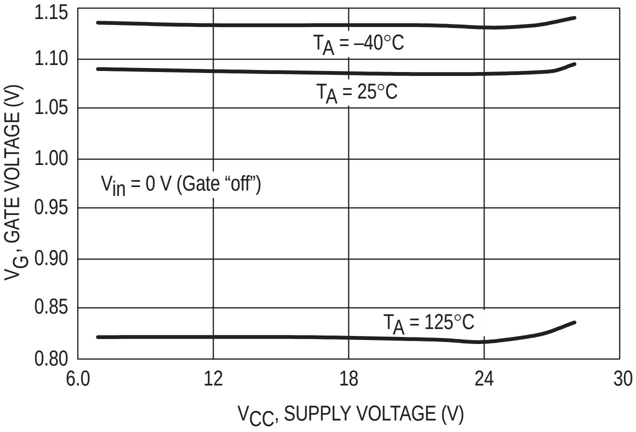


Figure 17. Gate Voltage verus Gate Current

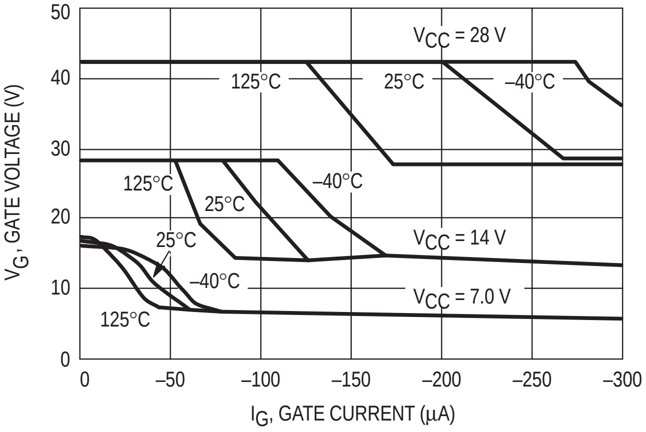


Figure 18. Gate–to–Source Voltage versus Source Voltage

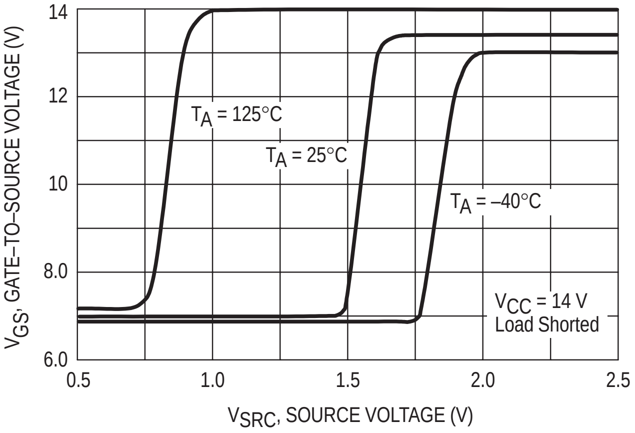


Figure 19. Gate Current versus Supply Voltage

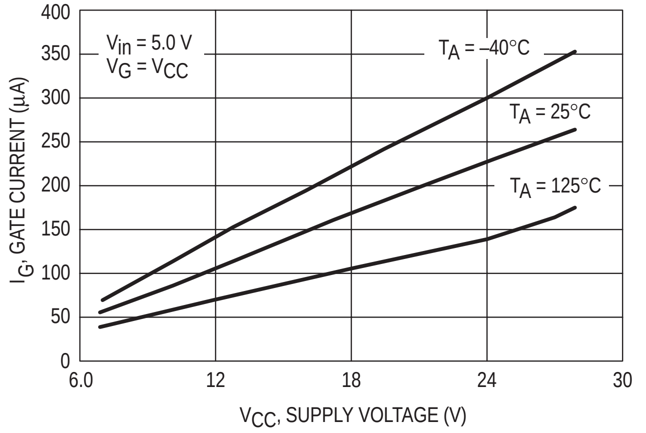


Figure 20. Gate Saturation Voltage versus Gate Current

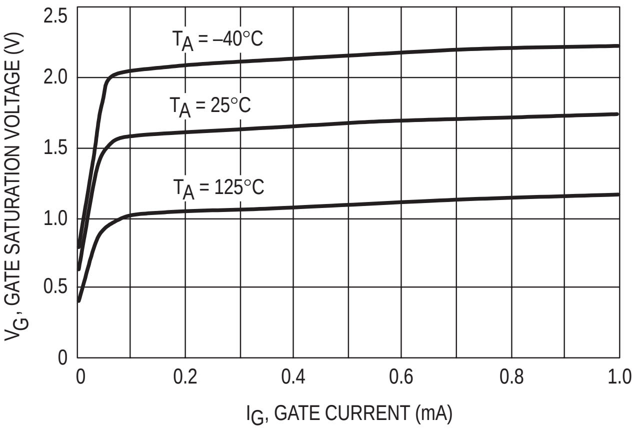


Figure 21. Gate Saturation Voltage versus Gate Current (Expanded Scale)

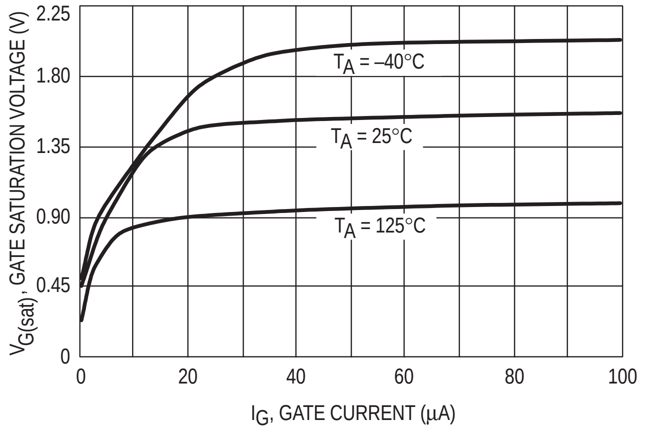


Figure 22. Drain–to–Source Voltage versus External R_T Timer Resistor

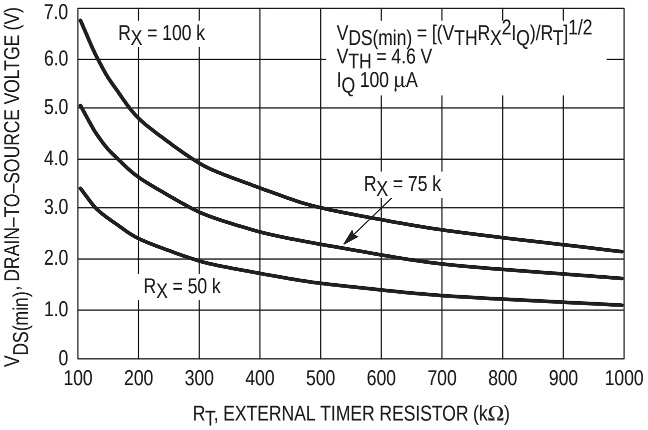


Figure 23. Timer Response versus $V_{DS(min)}/S$ Ratio

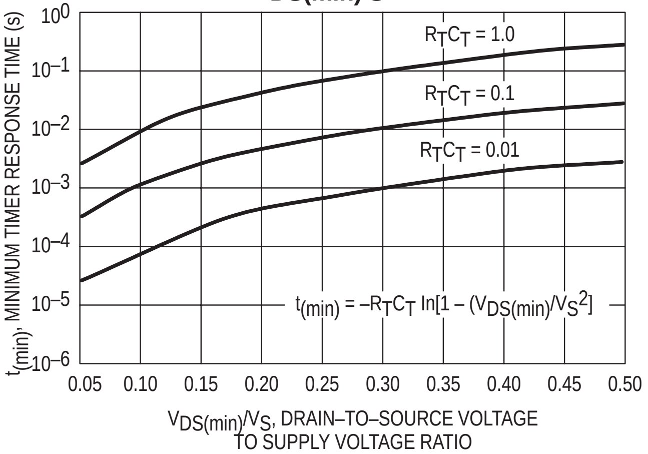


Figure 24. FET Comparison Gate Response

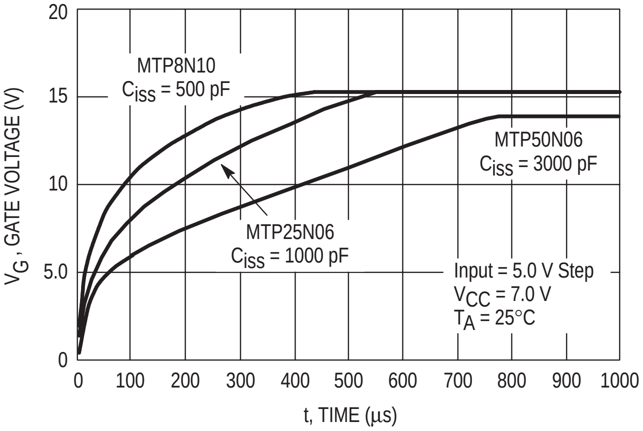


Figure 25. FET Comparison Gate Response

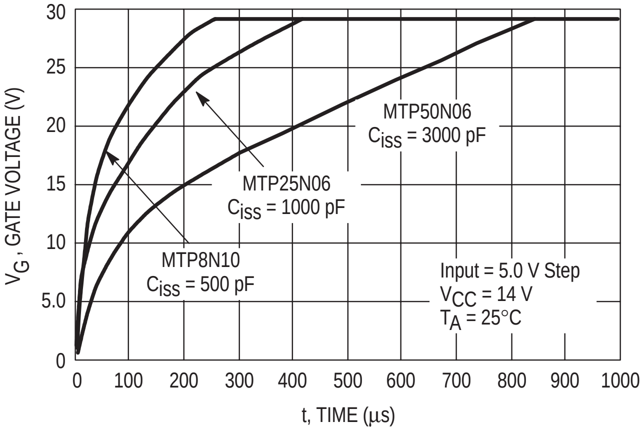


Figure 26. FET Comparison Gate Response

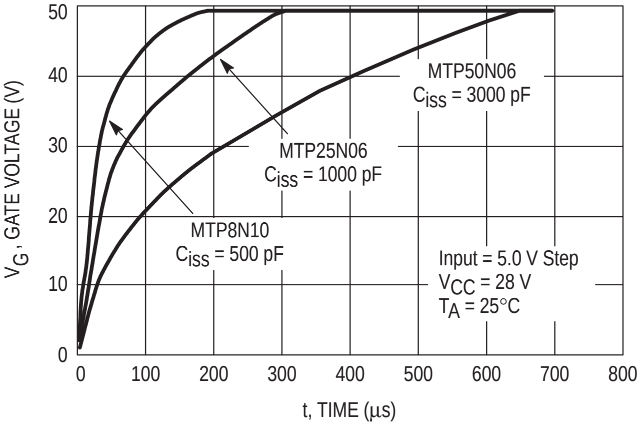


Figure 27. MTP25N06 Gate Response

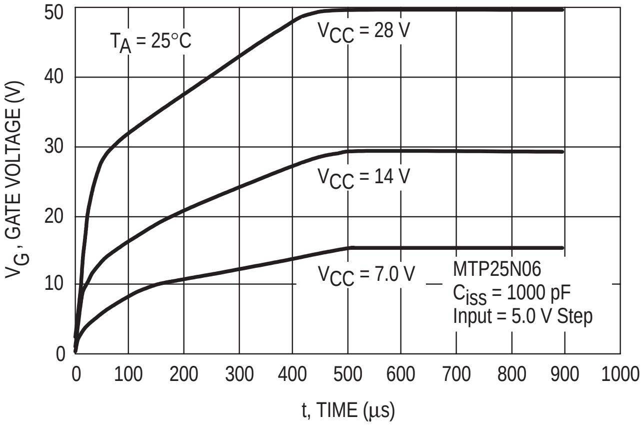
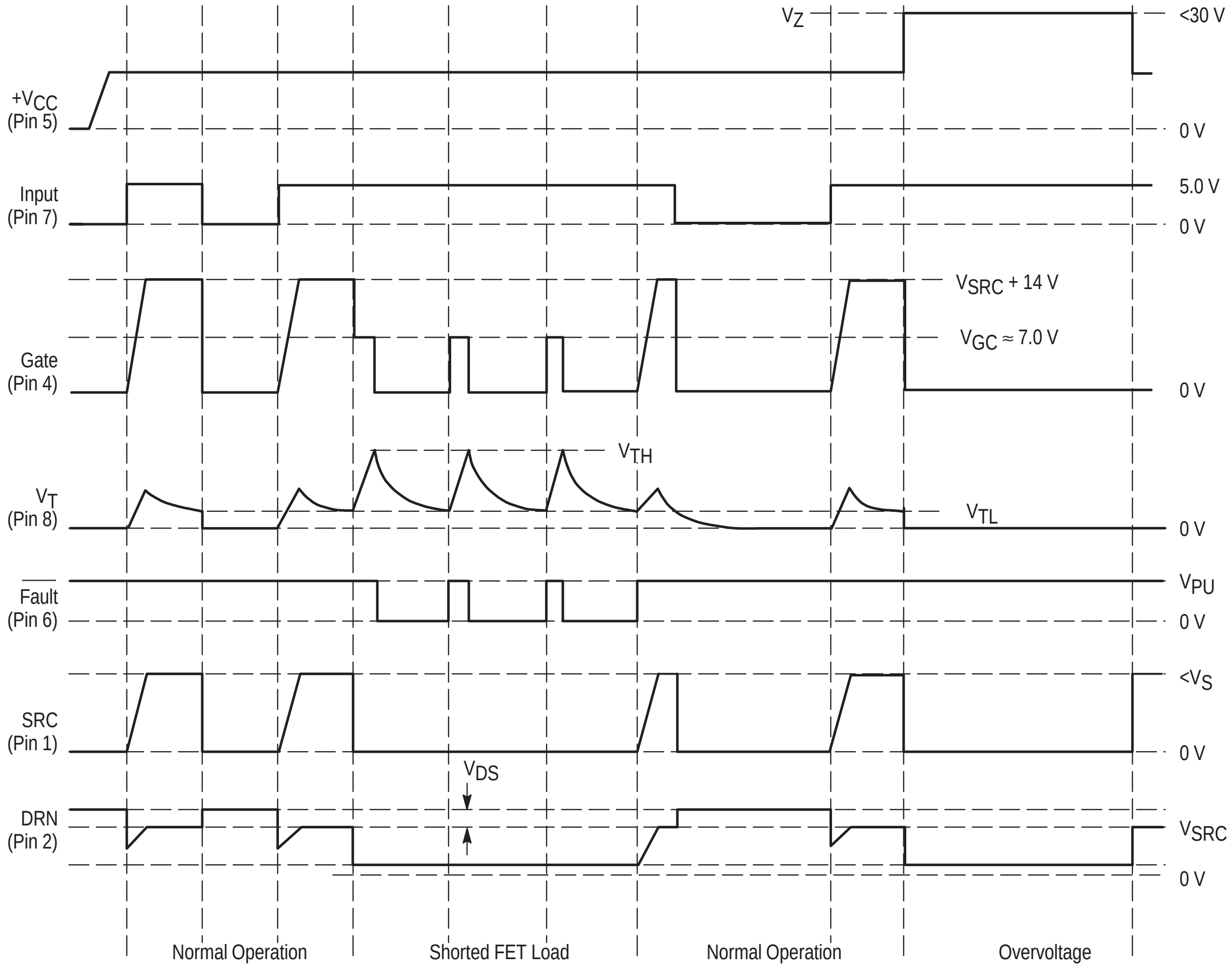


Figure 28. Descriptive Waveform Diagram



FUNCTIONAL DESCRIPTION

Introduction

The MC33091A is designed to drive a wide variety of N–channel TMOS transistors in high–side configured, low frequency switching applications. The MC33091A has an internal charge pump to fully enhance the on–state of the TMOS device. The MC33091A protects the TMOS device from shorts to ground and provides a Fault output to report the presence of an overcurrent condition. The few additional external components required allow tailoring of the application's protection level. The protection scheme of the MC33091A uses an externally programmable, nonlinear timer that disables the TMOS device in the event the drain to source voltage exceeds a specified value for a specified duration. Both the value and duration are externally programmable allowing for flexibility in applications.

Description of Pins

Figure 1 shows a typical application as well as the internal functional blocks of the MC33091A. The discussion to follow references this figure.

Input (Pin 7): The logic levels of the Input are compatible with CMOS logic families. The Input enables the protection and charge pump circuitry. With the Input in a logic low state the MC33091A draws only leakage current of less than 300 µA and in this condition the associated TMOS device will be in the "off" state. When the Input is in a logic high state, the Gate voltage (Pin 4) rise is limited to a maximum of 14 V above SRC (Pin 1), due to an internal clamp diode being used and the TMOS device is enhanced full on.

Fault (Pin 6): The Fault output is comprised of an open collector NPN transistor capable of sinking at least 500 µA when the TMOS gate is disabled due to an overcurrent condition. When the TMOS device experiences an overcurrent condition, the Fault pin is pulled low.

SRC (Pin 1): The SRC pin senses the TMOS source voltage and is the input to the V_{DS} buffer used in conjunction with the DRN pin in monitoring the drain to source voltage developed across the TMOS device. The purpose of the 1.0 k resistor connected to this pin is to protect the SRC input from overvoltage as a result of flyback voltage produced when the TMOS device is used to switch large inductive loads. This resistor can be eliminated when switching noninductive loads.

DRN (Pin 2): The DRN is used in conjunction with the SRC pin and together constitute a V_{DS} monitor of the TMOS drain to source voltage. Feedback from the SRC pin will maintain a voltage across the resistor, R_X, equal to the V_{DS} voltage developed across the TMOS device. The series resistor, R_X, connected between the drain of the TMOS device and DRN of the MC33091A is used in conjunction with the feedback buffer and associated PNP transistor to establish a current proportional to the drain to source voltage, V_{DS}, of the TMOS device. This proportional current, acted upon by the current squaring circuit of the MC33091A, is an important part of the TMOS protection scheme.

V_{CC} (Pin 5): The V_{CC} pin supplies operational power to the MC33091A. An internal 30 V zener clamp connected to this pin provides overvoltage protection of the MC33091A. When the zener is activated, the MC33091A disables the TMOS device only for the duration of the overvoltage but the Fault output (Pin 6) does not change logic states. The Fault pin does not go to a logic low state during the overvoltage duration since this is not an MC33091A device fault, but an external system fault.

Gate (Pin 4): The Gate pin of the MC33091A is the output of the internal charge pump which controls the TMOS device. The charge pump is a voltage tripler and requires no additional external components for operation. When the Input is at a logic low state, the charge pump will be turned off. When the Input is pulled to a logic high state, with no load fault existing, the charge pump turns on and pumps the TMOS gate voltage to at least 8.0 V, typically 10 to 14 V, above V_{CC}. An internal zener clamp is incorporated to limit the Gate to approximately 14 V above the source and prevent rupture of the TMOS gate.

V_T (Pin 8): The Timer pin (V_T) is both an input to the timer window comparators and an output of the current squaring circuit. An external resistor (R_T) and capacitor (C_T) are tied to this node so as to afford programing the characteristics necessary for protection of the TMOS device.

Overcurrent Protection Timer

The MC33091A protection scheme is based on the ability of the MC33091A to constantly sense the voltage drop developed across the TMOS device. A low voltage drop is indicative of normal TMOS "on" operation while a large voltage drop represents the existence of an overcurrent condition. By monitoring the TMOS drain to source voltage (V_{DS}) the MC33091A is able to detect a shorted load and react to disable the TMOS device. The circuit protection scheme is essentially based on a timer whose rate is dependent on the magnitude of V_{DS}. If the drain to source voltage is large (i.e. $V_{DS} = V_{CC}$), the timer will disable the gate drive very quickly. If V_{DS} is only slightly above the normal operating level, the timer will take much longer to disable the gate drive.

Since the power dissipated in the TMOS device is proportional to V_{DS}^2, low V_{DS} conditions can be tolerated for a longer time than high V_{DS} conditions. To enhance the system application, the timer time–out of the MC33091A is inversely proportional to V_{DS}^2. This approach maximizes the TMOS operating range. The timer parameters are completely user programmable through the use of external components affording application usage of a wide variety of TMOS devices. This is intended to model the generation and dissipation of heat within the TMOS device.

The external components R_X, R_T and C_T determine the timer characteristics. Once enabled, the MC33091A will source a current, I_{SQ}, from the timer pin that is proportional to V_{DS}^2 such that:

$$I_{SQ} = KV_{DS}^2 \qquad (1)$$

where: $K = 1/(R_X^2 I_Q)$

I_Q is an internal current source parameter of the MC33091A that has a nominal value of 100 µA and R_X is the external resistor in series with the drain of the TMOS device that establishes the value of the voltage to current proportionality constant. Since the parallel combination of R_T and C_T appear at the timer pin (V_T), the timer pin voltage, V_T, can be written as:

$$V_T(t) = I_{SQ}R_T[1–e^{–t/(R_TC_T)}] \qquad (2)$$

With the Input (Pin 7) in a logic high state and no overcurrent condition exists, the TMOS device will be in the "on" state. If the TMOS device experiences an overcurrent condition, I_{SQ} flowing through R_T will increase causing C_T to charge up, in turn causing the timer voltage, V_T, to exceed the threshold, V_{TH}, of the upper comparator. This sets the latch causing the Q output of the latch to go high (and the Q output to go low), causing the TMOS gate and Fault output (Pin 6) to be pulled low, disabling the TMOS device. Both the current squaring circuit (I_{SQ}) and the charge pump are disabled whenever the Q output of the latch goes low. Using Equation 2, the fault time response for an overcurrent condition can be written as:

$$t = –R_TC_T \ln(1–V_{TH}/I_{SQ}R_T) \qquad (3)$$

Using Equation 1 and substituting for I_{SQ} in Equation 3:

$$t = –R_TC_T \ln[1–(V_{TH}R_X{}^2I_Q)/(V_{DS}{}^2R_T)] \qquad (4)$$

When the timer current (I_{SQ}) is disabled, the attained V_{TH} voltage at Pin 8 decays according to the R_TC_T time constant until the V_{TL} threshold of the lower comparator is reached. At this point the latch is reset and the TMOS gate, charge pump and the current squaring circuit are again enabled, again turning on the TMOS device. The MC33091A will repeatedly duty cycle the TMOS gate in this manner so long as the overcurrent condition exists and the input control signal remains in a high logic state. The Fault output (Pin 6) will likewise duty cycle.

Consider the case where in Equation 4 the term $(V_{TH}R_X{}^2I_Q)$ / $(V_{DS}{}^2R_T) \geq 1$ such that the time period is undefined. Solving for V_{DS} for this case yields the *minimum* drain to source voltage necessary which will *not* allow V_T to charge to the V_{TH} threshold of the upper comparator. In other words, whenever the TMOS on–time period is infinite, *no* TMOS overcurrent condition exists. The minimum drain to source voltage required for uninterrupted continuous TMOS operation is:

$$V_{DS(min)} = [(V_{TH}R_X{}^2I_Q)/R_T]^{1/2} = (V_{TH}/KR_T)^{1/2} \qquad (5)$$

Under *normal* operating steady state TMOS "on" conditions; the values chosen for R_X and R_T should be such that the upper comparator threshold voltage is *never* reached. This insures the TMOS device will always be in operation so long as the $V_{DS(min)}$ is not exceeded.

The minimum time required for the capacitor C_T to charge up to upper comparator threshold voltage occurs when the TMOS device experiences maximum current (I_{max}). This will occur when the load, and in turn the source, are shorted to ground resulting in the full battery voltage (V_S) to appear directly across the TMOS device. This condition causes maximum I_{SQ} current to be produced by the current squaring circuit. The maximum I_{SQ} current experienced is:

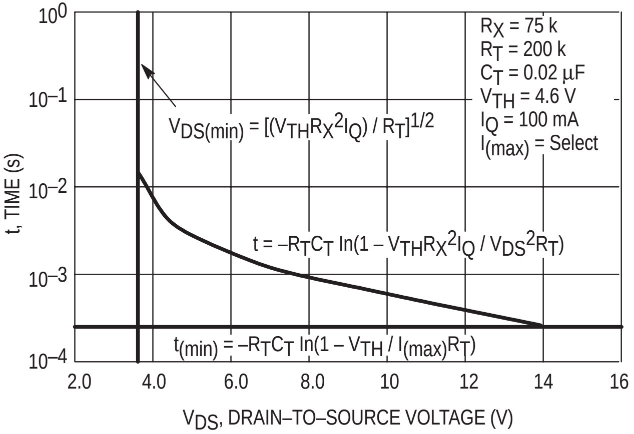
$$I_{SQ(max)} = KV_S{}^2 = (V_S/R_X)^2/I_Q \qquad (6)$$

An expression for the minimum time–out is obtained by substituting I_Q of Equation 6 into Equation 3:

$$t_{(min)} = –R_TC_T \ln[1–V_{TH}/(I_{SQ(max)}R_T)] \qquad (7)$$

Equation 4 is shown graphically along with the asymptotic limits imposed by Equations 5 and 7 in Figure 29.

Figure 29. Theoretical Fault Time versus V_{DS}



When driving incandescent lamp loads, the minimum timer time–out (time required for the V_T voltage to reach V_{TH} threshold of the upper comparator) should be set long enough so as to *not* allow the in–rush current of incandescent lamp to cause a false trigger, yet short enough to afford the TMOS device survival protection against direct shorts under worst case supply and temperature conditions.

TMOS Driver Power Dissipation

Under load short conditions, the MC33091A will duty cycle the TMOS gate. The power dissipation in this mode can be significant. For this reason proper heatsinking of the TMOS device is essential as is the selection of compatible external components so as to protect the TMOS device from destruction. In most cases, the heatsink required to handle the TMOS power dissipation under normal operating conditions will be adequate to insure the device survives a short circuit for an indefinite time under worst case conditions.

The MC33091A can protect the TMOS device under a direct load short condition. If the source voltage is less than about 1.5 V above ground, which will normally be the case in the event of a dead short, the MC33091A will clamp the gate to source voltage at 7.0 V. This action will limit the TMOS current and power dissipated under a direct load short condition.

The data sheet for the particular TMOS device being used will normally reveal the current value, $I_{DS(max)}$, to be expected under a dead short condition. TMOS data sheets normally depict graphs of drain current versus drain to source voltage for various gate to source voltages from which the drain current at 7.0 V V_{GS}, $I_{DS(max)}$, can reasonably be approximated. Using this information, the peak TMOS power dissipation under a dead short condition is approximated to be:

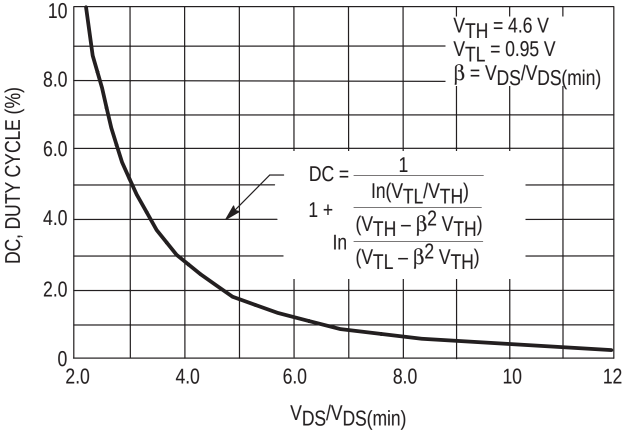
$$P_{D(peak)} = V_{S(max)} I_{DS(max)} \tag{8}$$

The average power is equal to the peak power dissipation multiplied by the duty cycle (DC):

$$P_{D(avg)} = P_{D(peak)} DC \tag{9}$$

As long as the average power, in Equation 9, is less than the maximum power dissipation of the TMOS device under normal conditions, the short circuit protection scheme of the MC33091A will adequately protect the TMOS device. The duty cycle at which the MC33091A controls the gate can be determined by using Figure 30.

Figure 30. MC33091A Duty Cycle versus V_{DS} / $V_{DS(min)}$



As previously discussed, I_{SQ} is externally dependant on the sensed V_{DS} voltage developed across the TMOS device and R_X in accordance with Equations 1 and 2. At the onset of an overload condition, the voltage across C_T will be less than the V_{TH} threshold voltage of the upper comparator with the TMOS device in an "on" state. I_{SQ} current will increase dramatically and the timing capacitor C_T charges toward V_{TH}. When the voltage on C_T reaches the V_{TH} threshold voltage of the upper comparator, the upper comparator output goes high setting the latch output (Q) high, turning on the open collector NPN transistor and pulling the Fault output low. At the same time, I_{SQ} is switched off, allowing C_T to discharge through resistor R_T to V_{TL}, at which time the TMOS device is again switched on. This action is repeated so long as the overload condition exists. The V_{TL} and V_{TH} thresholds are internally set to approximately 0.95 V and 4.6 V respectively.

The charge time (t_c) of C_T can be shown as:

$$t_c = -R_T C_T \ln[1-(V_{TH}-V_{TL})/(I_{SQ} R_T - V_{TL})] \tag{10}$$

The discharge time (t_d) of C_T can be shown as:

$$t_d = -R_T C_T \ln(V_{TL}/V_{TH}) \tag{11}$$

The duty cycle is defined as charge time divided by the charge plus discharge time and represented by:

$$DC = t_c/(t_c+t_d) \tag{12}$$

Substituting Equations 10 and 11 into 12:

$$DC = 1/1+\ln(V_{TL}/V_{TH})/\ln\{(V_{TH}-\beta^2 V_{TH})/(V_{TL}-\beta^2 V_{TH})\} \tag{13}$$

$$\text{where: } \beta = V_{DS}/V_{DS(min)}$$

Notice the duty cycle is dependent *only* on the ratio of the drain to source voltage, V_{DS}, of the TMOS device to the minimum drain to source voltage, $V_{DS(min)}$, allowing uninterrupted continuous TMOS operation as calculated in Equation 5. A graph of Equation 13 is shown in Figure 30 and is valid for any ratio of V_{DS} to $V_{DS(min)}$. Knowing this ratio, the duty cycle can be determined by using Figure 30 or Equation 13 and knowing the duty cycle, the average power dissipation can be calculated by using Equation 9.

If the TMOS device experiences a hard load short to ground a minimum duty cycle will be experienced which can be calculated. When this condition exists, the TMOS device experiences a V_{DS} voltage of V_S which is sensed by the MC33091A. The MC33091A very rapidly charges the timing capacitor C_T to V_{TH} shutting down the TMOS device. This condition produces the minimum duty cycle for the specific system conditions. The minimum duty cycle can be calculated for any valid V_S voltage by substituting the value of V_S used for V_{DS} in Equation 13 and solving for the duty cycle.

Knowing the duty cycle and peak power allows determination of the average power as was pointed out in Equation 9. TMOS data sheets specify the maximum allowable junction temperature and thermal resistance, junction–to–case, at which the device may be operated. Knowing the average power and the device thermal information, proper heatsinking of the TMOS device can be determined.

The duty cycle graph (Figure 30) reveals lower values of $V_{DS(min)}$ produce shorter duty cycles, for given V_{DS} voltages. The minimum duty cycle, being limited to the case where $V_{DS} = V_S$, increases as higher values of V_S are used.

APPLICATION

The following design approach will simplify application of the MC33091A and will insure the components chosen to be optimal for a specific application.

1. Characterize the load impedance and determine the maximum load current possible for the load supply voltage used.

2. Select a TMOS device capable of handling the maximum load current. Though the MC33091A will equally drive our competitors products, it is hoped you will select one of the many TMOS devices listed in Motorola's *Power MOSFET Transistor Data Book*.

3. Determine the maximum steady state V_{DS} voltage the TMOS device will experience under *normal* operating conditions. Typically, this is the maximum load current multiplied by the specified $R_{DS(on)}$ of the TMOS device. Junction temperature considerations should be taken into account for the $R_{DS(on)}$ value since it is significantly temperature dependent. Normally, TMOS data sheets depict the effect of junction temperature on $R_{DS(on)}$ and an $R_{DS(on)}$ value at some considered maximum junction temperature should be used. Various graphs relating to $R_{DS(on)}$ are depicted in Motorola TMOS data sheets. Though Motorola TMOS devices typically specify a maximum allowable junction temperature of 150°C, in a practical sense, the user should strive to keep junction temperature as low as possible so as to enhance the applications long term reliability. The maximum steady state V_{DS} voltage the TMOS device will experience under *normal* operating conditions is thus:

$$V_{DS(norm)} = I_{L(max)}R_{DS(on)} \tag{14}$$

4. Calculate the maximum power dissipation of the TMOS device under *normal* operating conditions:

$$P_{D(max)} = V_{DS(on)}I_{L(max)} \tag{15}$$

5. The calculated maximum power dissipation of the TMOS device dictates the required thermal impedance for the application. Knowing this, the selection of an appropriate heatsink to maintain the junction temperature below the maximum specified by the TMOS manufacture for operation can be made. The required overall thermal impedance is:

$$TR_{JA} = (T_{J(max)} - T_{A(max)})/P_{D(max)} \tag{16}$$

Where $T_{J(max)}$, the maximum allowable junction temperature, is found on the TMOS data sheet and $T_{A(max)}$, the maximum ambient temperature, is dictated by the application itself.

6. The thermal resistance, TR_{JA}, represents the maximum overall or total thermal resistance, from junction to the surrounding ambient, allowable to insure the TMOS manufactures maximum junction temperature will not be exceeded. In general, this overall thermal resistance can be considered as being made up of several separate minor thermal resistance interfaces comprised of TR_{JC}, TR_{CS} and TR_{SA} such that:

$$TR_{JA} = TR_{JC} + TR_{CS} + TR_{SA} \tag{17}$$

Where TR_{JC}, TR_{CS} and TR_{SA} represent the junction–to–case, case–to–heatsink and heatsink–to–ambient thermal resistances respectively. TR_{CS} and TR_{SA} are the only parameters the device user can influence.

The case–to–heatsink thermal resistance, TR_{CS}, is material dependent and can be expressed as:

$$TR_{CS} = \rho \times t/A \tag{18}$$

Where "ρ" is the thermal resistivity of the heatsink material (expressed in °C/Watt/Unit Thickness), "t" is the thickness of heatsink material, and "A" is the contact area of the case–to–heatsink. Heatsink manufactures specify the value of TR_{CS} for standard heatsinks. For nonstandard heatsinks, the user is required to calculate TR_{CS} using some form of the basic Equation 18.

The required heatsink–to–ambient thermal resistance, TR_{SA}, can easily be calculated once the terms of Equation 17 are known. Substituting TR_{JA} of Equation 16 into Equation 17 and solving for TR_{SA} produces:

$$TR_{SA} = (T_{J(max)}–T_{A(max)})/P_{D(max)}–(TR_{JC}+TR_{CS}) \tag{19}$$

Consulting the heatsink manufactures catalog will provide TR_{CS} information for various heatsinks under various mounting conditions so as to allow easy calculation of TR_{SA} in units of °C/W (or when multiplied by the power dissipation produces the heatsink mounting surface temperature rise). Furthermore, heatsink manufactures typically specify for various heatsinks, heatsink efficiency in the form of mounting surface temperature rise above the ambient conditions for various power dissipation levels. The user should insure that the heatsink selected will provide a surface temperature rise somewhat less than the maximum capability of the heatsink so that the device junction temperature will not be exceeded. The user should consult the heatsink manufacturers catalog for this information.

7. Set the value of $V_{DS(min)}$ to something greater than the *normal operating* drain to source voltage, $V_{DS(norm)}$, the TMOS device will experience as calculated in Step 3 above (Equation 14). From a practical standpoint, a value two or three times $V_{DS(norm)}$ expected under normal operation will prove to be a good starting point for $V_{DS(min)}$.

8. Select a value of R_T less than 1.0 MΩ for minimal timing error whose value is compatible with R_X (R_X will be selected in Step 9 below). A recommended starting value to use for R_T would be 470 k. The consideration here is that the input impedance of the threshold comparators are approximately 10 MΩ and if R_T values greater than 1.0 MΩ are used, significant timing errors may be experienced as a result of input bias current variations of the threshold comparators.

9. Select a value of R_X which is compatible with R_T. The value of R_X should be between 50 k and 100 k. Recall in Equation 5 that $V_{DS(min)}$ was determined by the combined selection of R_X and R_T. Low values of R_X will give large values for K ($K = 4.0\ \mu A/V^2$ for $R_X = 50$ k) causing I_{SQ} to be very sensitive to V_{DS} variations (see Equation 1). This is desirable if a minimum V_{DS} trip point is needed in the 1.0 V range since small V_{DS} values will generate measurable currents. However, at high V_{DS} values, TMOS device currents become excessively large and the current squaring function begins to deviate slightly from the predicted value due to high level injection effects occurring in the output PNP of the current squaring circuit. These effects can be seen when I_{SQ} exceeds several hundred microamps. See Figure 22 for graphical aid in the selection of R_T and R_X.

10. Calculate the shorted load average power dissipation for the application using Equations 8 and 9. This involves determining the peak shorted load power dissipation of the TMOS device and gate duty cycle. The duty cycle is based on $V_{DS(min)}$, the value of V_{DS} under shorted conditions (i.e. $V_{S(max)}$).

11. The calculated shorted load average power dissipation of Step 10 should be less than the maximum power dissipation under *normal* operating conditions calculated in Step 4. If this is not the case, there are two options.

Option one is to reduce the thermal resistance of the TMOS device heatsink, in other words, use a larger or better heatsink. This though, is not always practical to do particularly if restricted by size.

Option two is to set $V_{DS(min)}$ to the lowest practical value. If for instance $V_{DS(min)}$ is set to 4.0 V when only 2.0 V are needed, the short circuit duty cycle will be over twice as large, resulting in double the TMOS device power dissipated. Keeping $V_{DS(min)}$ to a minimum, reduces the shorted load average power.

12. Choose a value of C_T. The value of C_T can be determined either by trial and error or by characterizing the V_{DS} waveform for the load and selecting a capacitor value that generates a minimum fault time curve (see Equation 4) that encompasses the V_{DS} versus time waveform. The value of C_T has *no* effect on the duty cycle itself as was pointed out earlier. See Figure 23 for a graphical selection of C_T.

Inductive Loads

The TMOS device is turned off by pulling the gate to near ground potential. Turning off an inductive load will cause the source of the TMOS device to go below ground due to flyback voltage to the point where the TMOS device may become biased on again allowing the inductive energy to be dissipated through the load. An internal 14 V zener diode clamp from the gate to source pin limits how far the source pin can be pulled below ground. For high inductive loads, it may be necessary to have an external 10 k current limiting resistor in series with the source pin to limit the clamp current in the event the source pin is pulled more than 14 V below ground.

Transient Faults

The MC33091A is not able to withstand automotive voltage transients directly. By correctly sizing resistor R_S and capacitor C_S, the MC33091A can withstand load dump and other automotive type transients. The V_{CC} voltage is clamped at approximately 30 V through the use of an internal zener diode.

Under reverse battery conditions, the load will be energized in reverse due to the parasitic body diode inherent in the TMOS device. Under this condition, the drain is grounded and the MC33091A clamps the gate at 0.7 V below the battery potential. This turns the TMOS device on in reverse and minimizes the voltage across the TMOS device resulting in minimal power dissipation. Neither the MC33091A nor the TMOS device will be damaged under such a condition. In addition, if the load can tolerate a reverse polarity, the load will not be damaged. Caution; some sensitive applications may not tolerate a reverse polarity load condition with reverse battery polarity.

There is no protection of the TMOS device during a reverse battery condition if the load itself is already shorted to ground. The MC33091A will not incur damage under this specialized reverse battery condition but the TMOS device may be damaged since there could be significant energy available from the battery to be dissipated in the TMOS device.

The MC33091A will withstand a maximum V_{CC} voltage of 28 V and with the proper TMOS device used, the system can withstand a double battery condition.

Figure 36 depicts a method of protecting the FET from positive transient voltages in excess of the rated FET breakdown voltage. The zener voltage, in this case, should be less than the FET breakdown voltage. The diode, D, is necessary where reverse battery protection of the gate of the FET is required.

EMI Concern

The gate capacitance and thus the size of the TMOS device used will determine the turn–on and turn–off times experienced. In a practical sense, smaller TMOS devices have smaller gate capacitances and give rise to higher slew rates. By way of example, the turn–on of an MPT50N06 TMOS device might be of the order of 80 µs while that of an MPT8N10 might be 10 µs (see Figure 25). The speed of turn–on or turn–off can be calculated by assuming the charge pump to supply approximately 100 µA over the time the gate capacitance will transition a V_{GS} voltage of 0 V to 10 V. In reality, the V_{GS} voltage will be greater than 10 V, but the additional increase in TMOS drain current will be minimal for V_{GS} voltages greater than 10 V.

The charge pump current is sized so that turn–on time need not be of concern in all but the most critical of applications. Where limiting of EMI is of concern, the charge pump of the MC33091A may be slew rate limited by adding an external feedback capacitor from the gate–to–source of the TMOS device for slow down adjustment of both turn–on and turn–off times (see Figure 33). Figures 31 through 35 depict various methods of modifying the turn–on or turn–off times.

Figure 35 depicts a method of using only six external components to decrease turn–off time and clamp the flyback voltage associated with switching inductive loads. $V_{GS(th)}$ used in the critical component selection criteria refers to the gate–to–source threshold voltage of the FET used in the application.

Caution should be exercised when slowing down the switching transition time since doing so can greatly increase the average power dissipation of the TMOS device. The resulting increase in power dissipation should be taken into account when selecting the R_TC_T time constant values in order to protect the TMOS device from any overcurrent condition.

Figure 31. Slow Down FET Turn–On

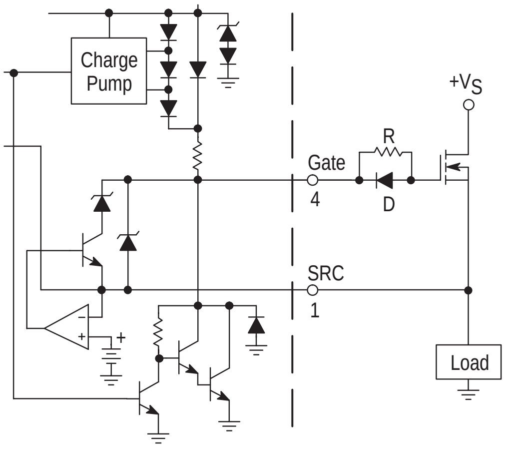


Figure 32. Slow Down FET Turn–Off

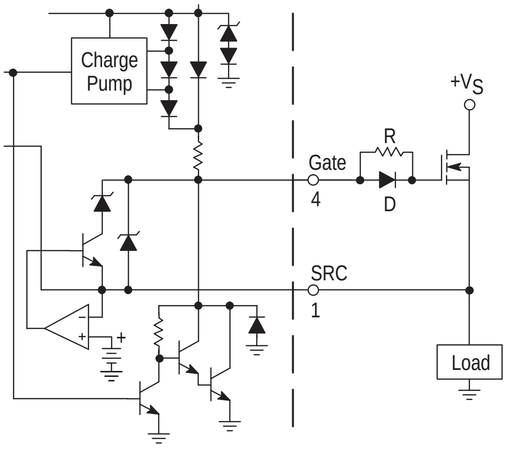


Figure 33. Slow Down Turn–On and Turn–Off of FET

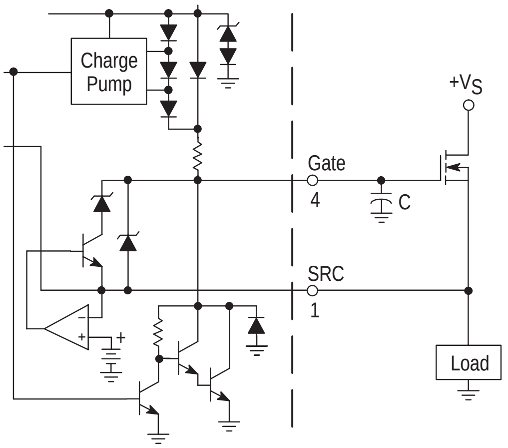


Figure 34. Independent Slow Down Adjustment of FET Turn–On and Turn–Off

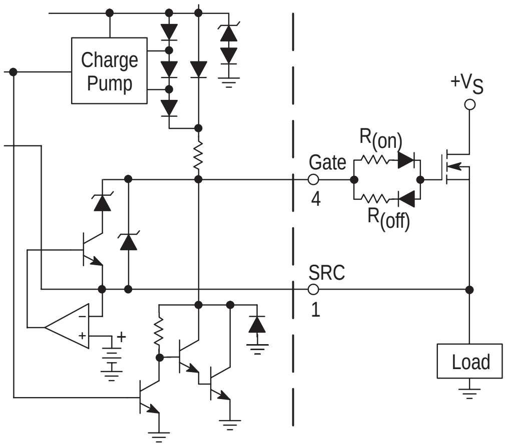


Figure 35. Decreased FET Turn–Off Time with Inductive Flyback Voltage Clamp

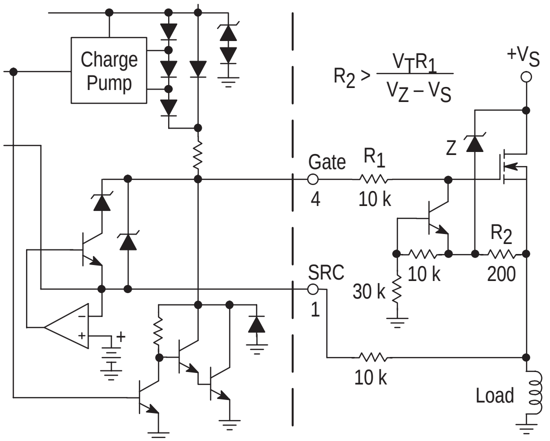
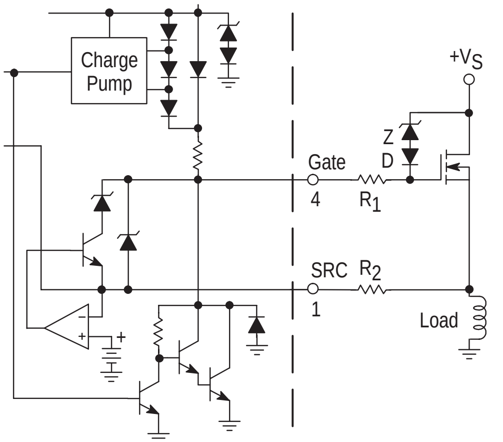


Figure 36. Overvoltage Protection of FET



MC33092

Alternator Voltage Regulator

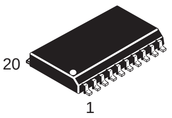
ALTERNATOR VOLTAGE REGULATOR

SEMICONDUCTOR
TECHNICAL DATA

The MC33092 is specifically designed for voltage regulation and Load Response Control (LRC) of diode rectified alternator charging systems, as commonly found in automotive applications. The MC33092 provides load response control of the alternator output current to eliminate engine speed hunting and vibration due to sudden electrical loads which cause abrupt torque loading of the engine at low RPM. Two load response rates are selectable using Pin 11. The timing of the response rates is dependent on the oscillator frequency.

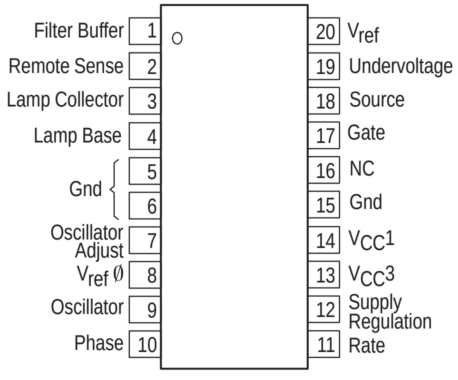
In maintaining system voltage, the MC33092 monitors and compares the system battery voltage to an externally programmed set point value and pulse width modulates an N–channel MOSFET transistor to control the average alternator field current.

- Forced Load Response Control (LRC) with Heavy Load Transitions at Low RPM
- Capable of Regulating Voltage to ± 0.1 V @ 25°C
- Operating Frequency Selectable with One External Resistor
- < 0.1 V Variation over Speed Range of 2000 to 10,000 RPM
- < 0.4 V Variation over 10% to 95% of Maximum Alternator Output
- Maintains Regulation with External Loads as Low as 1.0 A
- Load Dump Protection of Lamp, Field Control Devices, and Loads
- Duty Cycle Limit Protection
- Provides High Side MOSFET Control of a Ground Referenced Field Winding
- Controlled MOSFET and Flyback Diode Recovery Characteristics for Minimum RFI
- < 2.0 mA Standby Current from Battery @ 25°C
- < 3.0 mA Standby Current from Battery Over Temperature Range
- Optional 2.5 or 10 sec. LRC Rate Control (Osc. Freq. = 280 kHz)
- Undervoltage, Overvoltage and Phase Fault (Broken Belt) Detection



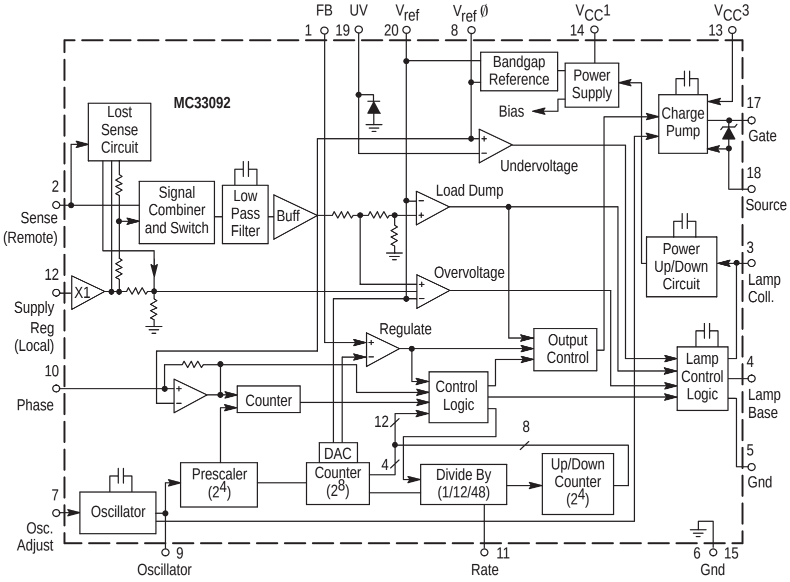
DW SUFFIX
PLASTIC PACKAGE
CASE 751D
(SO–20L)

PIN CONNECTIONS



(Top View)

Simplified Block Diagram



ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC33092DW	T_A = – 40° to +125°C	SO–20L

MAXIMUM RATINGS

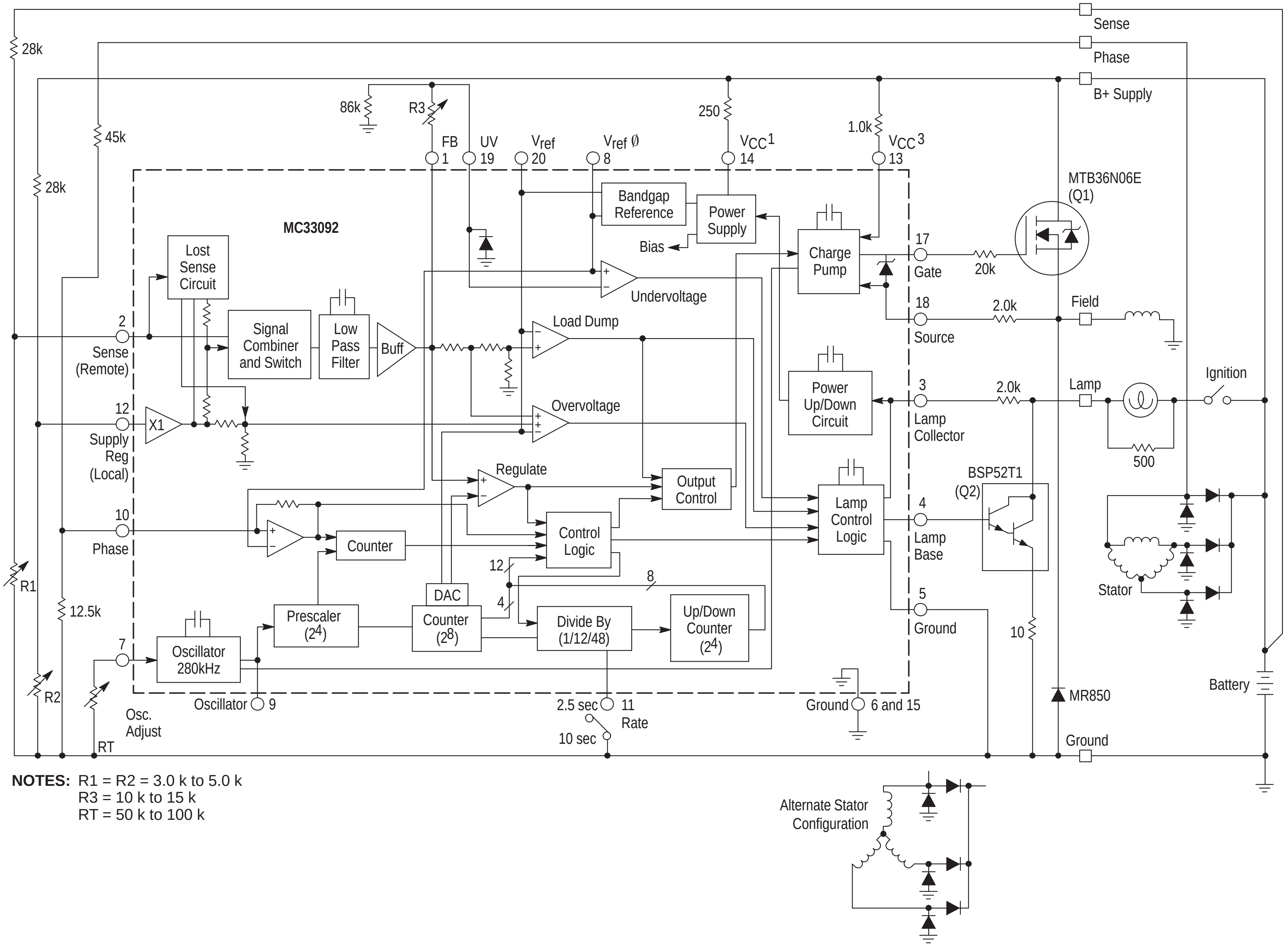
Rating	Symbol	Value	Unit
Power Supply Voltage	V_{bat}	24	V
Load Dump Transient Voltage (Note 1)	$+V_{max}$	40	V
Negative Voltage (Note 2)	$-V_{min}$	– 2.5	V
Power Dissipation and Thermal Characteristics			
Maximum Power Dissipation @ $T_A = 125°C$	P_D	867	mW
Thermal Resistance, Junction–to–Ambient	$R_{\theta JA}$	75	°C/W
Operating Junction Temperature	T_J	+150	°C
Operating Ambient Temperature Range	T_A	– 40 to +125	°C
Storage Temperature Range	T_{stg}	– 45 to +150	°C

ELECTRICAL CHARACTERISTICS (External components per Figure 1, $T_A = 25°C$, unless otherwise noted).

Characteristic	Symbol	Min	Typ	Max	Unit
DC CHARACTERISTICS					
Regulation Voltage (Determined by external resistor divider)	V_{Reg}	–	14.85	–	V
Regulation Voltage Temperature Coefficient	T_C	–13	–11	– 9.0	mV/°C
Suggested Battery Voltage Operating Range	V_{bat}	11.5	14.85	16.5	V
Power Up/Down Threshold Voltage (Pin 3)	V_{Pwr}	0.5	1.2	2.0	V
Standby Current,					
$V_{bat} = 12.8$ V, Ignition off, $T_A = 25°C$	I_{Q1}	–	1.3	2.0	mA
$V_{bat} = 12.8$ V, Ignition off, $-40°C \le T_A \le 125°C$	I_{Q2}	–	–	3.0	mA
Zero Temperature Coefficient Reference Voltage, (Pin 8)	$V_{ref\,\emptyset}$	1.1	1.25	1.4	V
Band Gap Reference Voltage (Pin 20)	V_{ref}	1.7	2.0	2.3	V
Band Gap Reference Temperature Coefficient	TC	–13	–11	– 9.0	mV/°C
Sense Loss Threshold (Pin 2)	$S_{Loss(th)}$	–	0.6	1.0	V
Phase Detection Threshold Voltage (Pin 10)	P_{Th}	1.0	1.25	1.5	V
Phase Rotation Detection Frequency (Pin 10)	P_{Rot}	–	36	–	Hz
Undervoltage Threshold (Pin 19)	V_{UV}	1.0	1.25	1.5	V
Overvoltage Threshold (Pin 2, or Pin 12 if Pin 2 is not used)	V_{OV}	$1.09(V_{ref})$	$1.12(V_{ref})$	$1.16(V_{ref})$	V
Load Dump Threshold (Pin 2, or Pin 12 if Pin 2 is not used)	V_{LD}	$1.33(V_{ref})$	$1.4(V_{ref})$	$1.48(V_{ref})$	V
SWITCHING CHARACTERISTICS					
Fundamental Regulation Output Frequency, (Pin 17) (Clock oscillator frequency divided by 4096)	f	–	68	–	Hz
Suggested Clock Oscillator Frequency Range, (Pin 9) (Determined by external resistor, R_T, see Figure 6)	f_{osc}	205	280	350	kHz
Duty Cycle (Pin 17)					
At Start–up	$Start_{DC}$	27	29	31	%
During Overvoltage Condition	OV_{DC}	3.5	4.7	5.5	%
Low/High RPM Transition Frequency (Pin 10)	LRC_{Freq}	247	273	309	Hz
LRC Duty Cycle Increase Rate					
Low RPM Mode ($LRC_{Freq} < 247$ Hz), Pin 11 = Open (Slow Rate)	LRC_S	8.5	9.5	10.5	%/sec
Low RPM Mode ($LRC_{Freq} < 247$ Hz), Pin 11 = Grounded (Fast Rate)	LRC_F	34	38	42	%/sec
High RPM Mode ($LRC_{Freq} > 309$ Hz), Pin 11 = Don't Care (LRC Mode is disabled)	LRC_H	409	455	501	%/sec

NOTES: 1. 125 ms wide square wave pulse.
2. Maximum time = 2 minutes.

Figure 1. Simplified Application



NOTES: R1 = R2 = 3.0 k to 5.0 k
R3 = 10 k to 15 k
RT = 50 k to 100 k

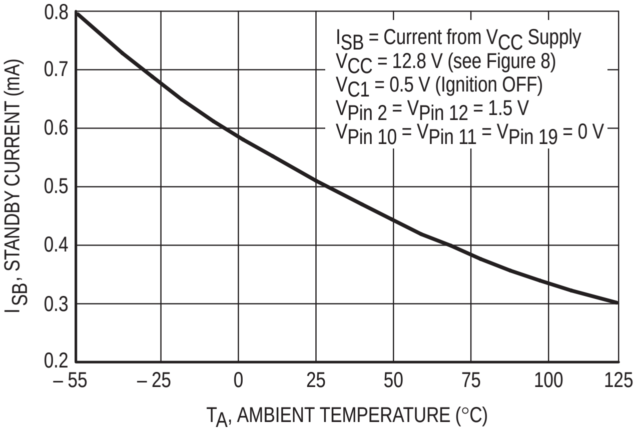


Figure 2. Standby Current versus Temperature

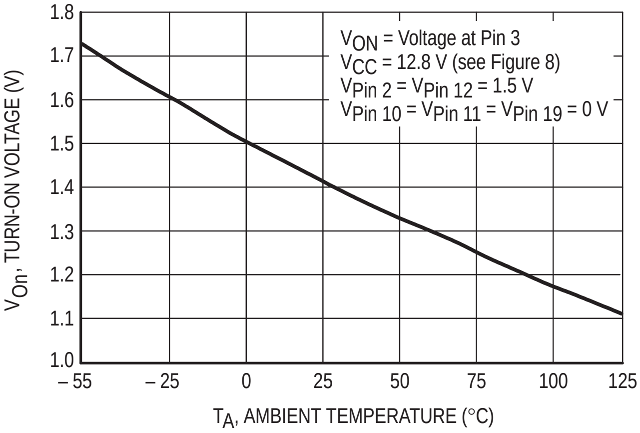


Figure 3. Turn–On Voltage versus Temperature

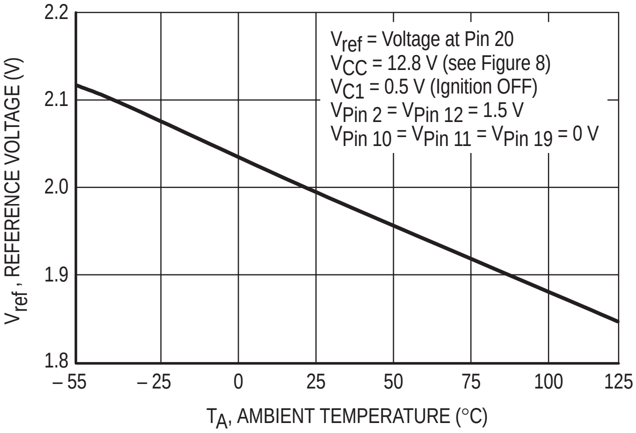


Figure 4. Reference Voltage versus Temperature

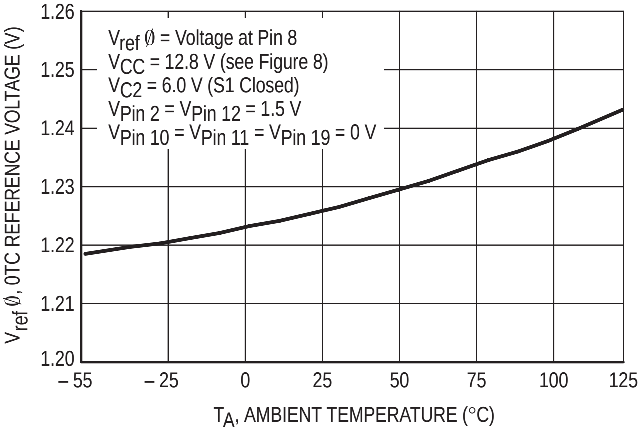


Figure 5. 0TC Reference Voltage versus Temperature

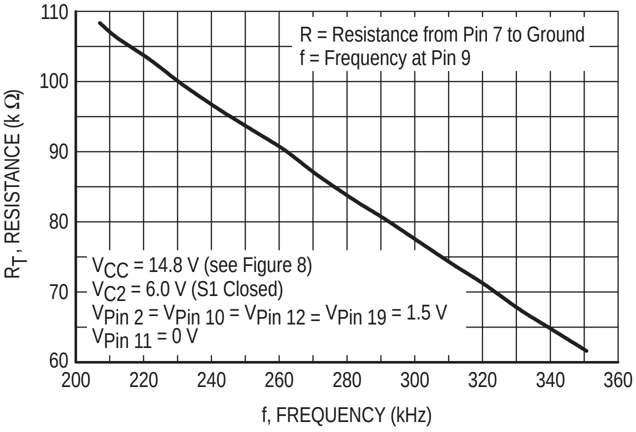


Figure 6. Oscillator Frequency versus Timing Resistor

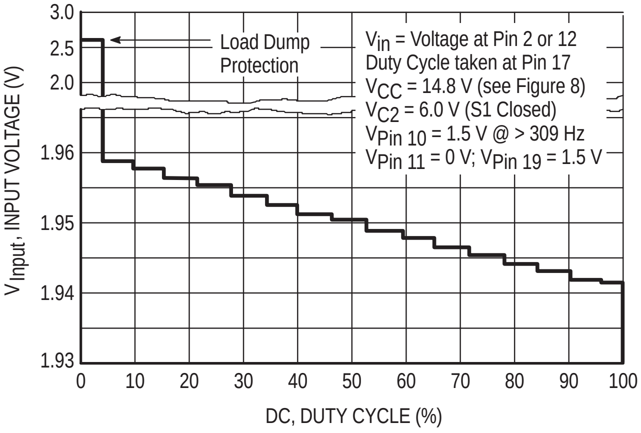
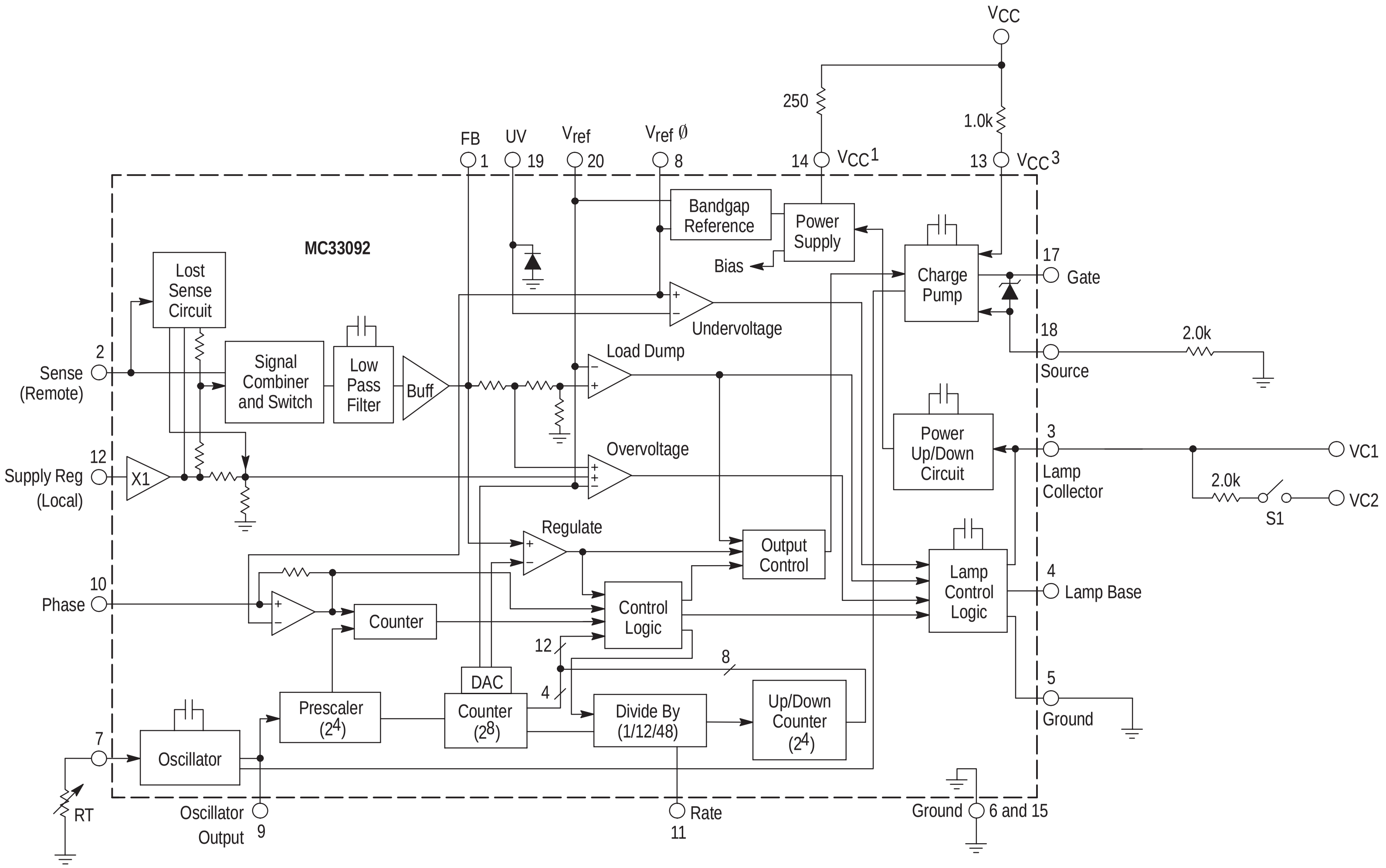


Figure 7. Input Voltage versus Output Duty Cycle

Figure 8. Typical Test Circuit



PIN FUNCTION DESCRIPTION

Pin No.	Function	Description
1	FB	This pin provides a filtered result of the Sense input (if the Sense input is used) or the Supply Regulation input (if the Sense input is not used).
2	Sense	The Sense input is a remote (Kelvin), low current battery voltage reference input used to give an accurate representation of the true battery voltage. This input is also used to monitor overvoltage or load dump conditions.
3	Lamp Collector and Power–Up/Down	This pin connects to the collector of the transistor (Q2) used to drive the fault lamp. It is also used to sense a closed ignition switch (voltage sense) which then turns power on to the IC.
4	Lamp Base	The Lamp Base pin provides base current to the fault lamp drive transistor (Q2).
5	Ground	Grounded to provide a ground return for the fault lamp control logic circuit.
6, 15	Ground	IC ground reference pins.
7	Oscillator Adjust	A resistor to ground on this pin adjusts the internal oscillator frequency (see Figure 6).
8	* $V_{ref\emptyset}$	This is a test point for the 1.1 V to 1.4 V reference voltage. It has a zero temperature coefficient. The reference is used internally for phase signal and undervoltage detection.
9	* Oscillator	Test point for checking the operation of the internal oscillator.
10	Phase	The Phase input detects the existence of a magnetic field rotating within the alternator.
11	Rate	The Rate pin is used to select a slow mode (floating) or fast mode (ground) Load Response Control recovery rate.
12	Supply Regulation	The voltage on the Supply Regulation pin is used as a representation of the alternator output voltage. This input also used to monitor overvoltage or load dump conditions.
13	$V_{CC}3$	Positive supply for the internal Charge Pump.
14	$V_{CC}1$	Positive supply for the entire IC except for the Charge Pump.
15, 6	Ground	Ground reference for the IC.
16	N/C	No connection.
17	Gate	Controls the Gate of the MOSFET used to energize the field winding.
18	Source	Field winding control MOSFET source reference.
19	Undervoltage	If the voltage at this pin goes below 1.0 V, the fault lamp is guaranteed to turn on. The IC will continue to function, but with limited performance.
20	* V_{ref}	Test point for the 1.7 V to 2.3 V Bandgap reference voltage. This voltage has a negative temperature coefficient of approximately –11 mV/°C.

***NOTE:** Pins 8, 9 and 20 are test points only.

APPLICATION CIRCUIT DESCRIPTION

Introduction

The MC33092, designed to operate in a 12 V system, is intended to control the voltage in an automotive system that uses a 3 phase alternator with a rotating field winding. The system shown in Figure 1 includes an alternator with its associated field coil, stator coils and rectifiers, a battery, a lamp and an ignition switch. A tap is connected to one corner of the stator windings and provides an AC signal for rotation (phase) detection.

A unique feature of the MC33092 is the Load Response Control (LRC) circuitry. The LRC circuitry is active when the stator winding AC signal frequency (phase buffer input signal, Pin 10) is lower than the Low/High RPM transition frequency. When active, the LRC circuitry dominates the basic analog control circuitry and slows the alternator response time to sudden increases in load current. This prevents the alternator from placing a sudden, high torque load on the automobile engine when a high current accessory is switched on.

The LRC circuitry is inactive when the stator winding AC signal frequency is higher than the Low/High RPM transition frequency. When the LRC circuitry is inactive, the basic analog control circuitry controls the alternator so it will supply a constant voltage that is independent of the load current.

Both the LRC and analog control circuits control the system voltage by switching ON and OFF the alternator field current using Pulse Width Modulation (PWM). The PWM approach controls the duty cycle and therefore the average field current. The field current is switched ON and OFF at a fixed frequency by a MOSFET (Q1) which is driven directly by the IC. The MC33092 uses a charge pump to drive the MOSFET in a high side configuration for alternators having a grounded field winding.

A fault detector is featured which detects overvoltage, undervoltage, slow rotation or non–rotation (broken alternator belt) conditions and indicates them through a fault lamp drive output (Pin 4).

A Load Dump protection circuit is included. During a load dump condition, the MOSFET gate drive (Pin 17) and the fault lamp drive output are disabled to protect the MOSFET, field winding and lamp.

Power–Up/Down

Power is continuously applied to the MC33092 through $V_{CC}1$ and $V_{CC}3$. A power–up/down condition is determined by the voltage on the Lamp Collector pin (Pin 3). When this voltage is below 0.5 V the IC is guaranteed to be in a low current standby mode. When the voltage at Pin 3 is above 2.0 V, the IC is guaranteed to be fully operational. The power–up voltage is applied to Pin 3 via the ignition switch and fault lamp. In case the fault lamp opens, a 500 Ω bypass resistor should be used to ensure regulator IC power–up.

A power–up reset circuit provides a reset or set condition for all digital counter circuitry. There is also a built–in power–up delay circuit that protects against erratic power–up signals.

Battery and Alternator Output Voltage Sensing

The battery and the alternator output voltage are sensed by the remote (Sense, Pin 2), and the local (Supply Regulator, Pin 12) input buffer pins, respectively, by way of external voltage dividers. The regulated system voltage is determined by the voltage divider resistor values.

Normally the remote pin voltage determines the value at which the battery voltage is regulated. In some cases the remote pin is not used. When this condition ($V_{Pin\ 2} < 0.6$ V typically) exists, a sense loss function allows the local pin voltage to determine the regulated battery voltage with no attenuation of signal. If, however, when the remote pin is used, and the voltage at this pin is approximately 25% less than the voltage at the local sense pin (but greater than 0.6 V, typically), the value at which the battery voltage is regulated is switched to the local sense pin voltage (minus the 25%). The signal combiner/switch controls this transfer function.

Low Pass Filter, DAC & Regulator Comparator

The output of the combiner/switch buffer feeds a low pass filter block to remove high frequency system noise. The filter output is buffered and compared by the regulator comparator to a descending ramp waveform generated by an internal DAC. When the two voltages are approximately equal, the output of the regulator comparator changes state and the gate of the MOSFET is pulled low (turned OFF) by the output control logic for the duration of the output frequency clock cycle. At the beginning of the next output clock cycle, the DAC begins its descending ramp waveform and the MOSFET is turned ON until the regulator comparator output again changes state. This ongoing cycle constitutes the PWM technique used to control the system voltage.

Oscillator

The oscillator block provides the clock pulses for the prescaler–counter chain and the charge control for the charge pump circuit. The oscillator frequency is set by an external resistor from Pin 7 to ground as presented in Figure 6.

The prescaler–counter divides the oscillator frequency by 2^{12} (4096) and feeds it to the output control logic and divider–up/down counter chain. The output control logic uses it as the fundamental regulation output frequency (Pin 17).

Load Response Control

The Load Response Control (LRC) circuit generates a digital control of the regulation function and is active when the stator output AC signal (Pin 10) frequency is lower than the Low/High RPM transition frequency. The LRC circuit takes the output signal of the prescaler–counter chain and with a subsequent divider and up/down counter to provide delay, controls the alternator response time to load increases on the system. The response time is pin programmable to two rates. Pin 11 programs the divider to divide by 12 or divide by 48. If Pin 11 is grounded, the signal fed to the up/down counter is divided by 12 and the response time is 12 times slower than the basic analog response time. If Pin 11 is left floating, the signal to the up/down counter is divided by 48 and the response time is 48 times slower.

The basic analog (LRC not active) and digital duty cycle control (LRC active) are OR'd such that either function will terminate drive to the gate of the MOSFET device with the shortest ON–time, i.e., lower duty cycle dominating.

The digital ON–time is determined by comparing the output of the up/down counter to a continuous counter and decoding when they are equal. This event will terminate drive to the MOSFET. A count direction shift register requires three consecutive clock pulses with a state change on the data input of the register to result in an up/down count direction change. The count will increase for increasing system load up to 100% duty cycle and count down for decreased loading to a minimum of 29% duty cycle. The analog control can provide a minimum duty cycle of 4 to 5%. The initial power–up duty cycle is 29% until the phase comparator input exceeds its input threshold voltage. Also, the IC powers up with the LRC circuit active, i.e., when the Lamp Collector pin exceeds the power–up threshold voltage.

Fault Lamp Indicator

Pins 3 and 4 control the external Darlington transistor (Q2) that drives the fault indicator lamp. A 10 Ω resistor should be placed in series with the transistor’s emitter for current limiting purposes. The fault lamp is energized during any of the following fault conditions: 1) No Phase buffer (Pin 10) input due to slow or no alternator rotation, shorted phase winding, etc.; 2) Phase buffer input AC voltage less than the phase detect threshold; 3) Overvoltage on Pin 2, or Pin 12 if Pin 2 is not used, or 4) Undervoltage on Pin 19 with the phase buffer input signal higher than the Low/High RPM transition frequency.

Phase Buffer Input

A tap is normally connected to one corner of the alternator’s stator winding to provide an AC voltage for rotation detection. This AC signal is fed into the phase buffer input (Pin 10) through a voltage divider. If the frequency of this signal is less than the phase rotation detect frequency (36 Hz, typically), the fault lamp is lit indicating an insufficient alternator rotation and the MOSFET drive (Pin 17) output duty cycle is restricted to approximately 29% maximum. Also, if the peak voltage of the AC signal is less than the phase detect threshold, the fault lamp is lit indicating an insufficient amount of field current and again the MOSFET drive (Pin 17) output duty cycle is restricted to approximately 29% maximum.

Undervoltage, Overvoltage and Load Dump

The low pass filter output feeds an undervoltage comparator through an external voltage divider. The voltage divider can be used to adjust the undervoltage detection level. During an undervoltage condition, the fault lamp will light only if the phase buffer input signal frequency is higher than the Low/High RPM transition frequency. This is to ensure that the undervoltage condition is caused by a true fault and not just by low alternator rotation. To help maintain system voltage regulation during an undervoltage condition, the output duty cycle is automatically increased to 100%. Even though the fault lamp may be energized for an undervoltage condition, the MC33092 will continue to operate but with limited performance.

Through an internal voltage divider, the low pass filter feeds an overvoltage comparator which monitors this output for an overvoltage condition. If the overvoltage threshold is exceeded, the fault lamp is lit and the MOSFET drive (Pin 17) output duty cycle is restricted to approximately 4% maximum.

The internal voltage divider on the input to the load dump comparator has a different ratio than the divider used on the overvoltage comparator. This allows the load dump detect threshold to be higher than the overvoltage threshold even though both comparators are monitoring the same low pass filter output. If the load dump detect threshold is exceeded, the fault lamp and MOSFET drive outputs are disabled to protect the MOSFET, field winding and lamp.

MOTOROLA

MC33143

Advance Information

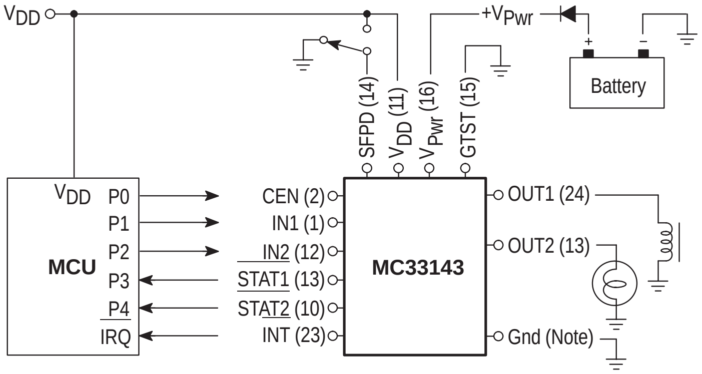
Dual High-Side Switch

The MC33143 is a dual high–side switch designed for solenoid control in harsh automotive applications, but is well suited for other environments. The device can also be used to control small motors and relays as well as solenoids. The MC33143 incorporates SMARTMOS™ technology, with CMOS logic, bipolar/MOS analog circuitry, and DMOS power outputs. An internal charge pump is incorporated for efficient gate enhancement of the internal high–side power output devices. The outputs are designed to provide current to low impedance solenoids. The MC33143 provides individual output fault status reporting along with internal Overcurrent and Over Temperature protection. The device also has Overvoltage protection, with automatic recovery, which “globally” disables both outputs for the duration of an Overvoltage condition. Each output has individual Overcurrent and Over Temperature shutdown with automatic retry recovery. Outputs are enabled with a CMOS logic high signal applied to an input to providing true logic control. The outputs, when turned on, provide full supply (battery) voltage across the solenoid coil.

The MC33143 is packaged in an economical 24 pin surface mount power package and specified over an operating voltage of $5.5\ V \le V_{Pwr} < 26\ V$ for $-40°C \le T_A \le 125°C$.

- Designed to Operate Over Wide Supply Voltages of 5.5 V to 26 V
- Dual High–Side Outputs Clamped to –10 V for Driving Inductive Loads
- Internal Charge Pump for Enhanced Gate Drive
- Interfaces Directly to a Microcontroller with Parallel Input Control
- Outputs Current Limited to 3.0 A to 6.0 A for Driving Incandescent Loads
- Chip Enable “Sleep Mode” for Power Conservation
- Individual Output Status Reporting
- Fault Interrupt Output for System Interrupt Use
- Output ON or OFF Open Load Detection
- Overvoltage Detection and Shutdown
- Output Over Temperature Detection and Shutdown with Automatic Retry
- Sustained Current Limit or Immediate Overcurrent Shutdown Output Modes
- Output Short to Ground Detection and Shutdown with Automatic Retry
- Output Short to V_{Pwr} Detection

Simplified Application

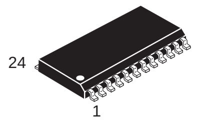


NOTE: Pins 5, 6, 7, 8, 17, 18, 19 and 20 provide electrical ground and heatsinking.

This device contains 889 active transistors.

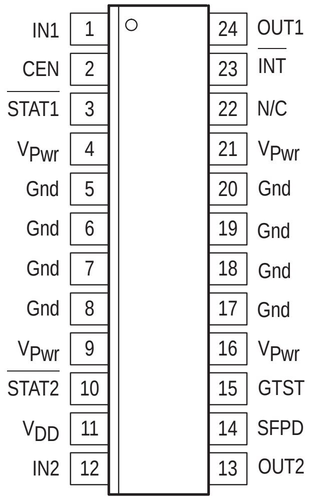
DUAL HIGH–SIDE SWITCH

SEMICONDUCTOR TECHNICAL DATA



DW SUFFIX
PLASTIC PACKAGE
CASE 751E
(SOP (16+4+4)L)

PIN CONNECTIONS

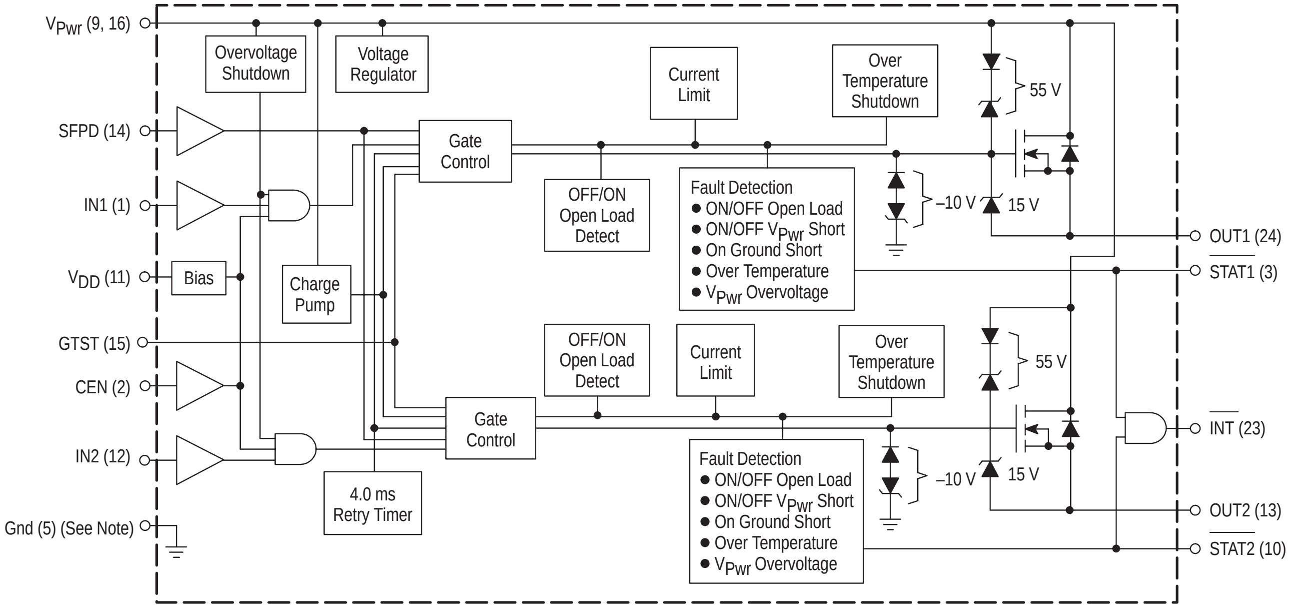


(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC33143DW	T_A = – 40° to +125°C	SOP–24L

Figure 1. Simplified Internal Block Diagram



NOTE: Pins 5, 6, 7, 8, 17, 18, 19 and 20 should all be grounded so as to provide electrical as well as thermal heatsinking of the device.

MAXIMUM RATINGS (All voltages are with respect to ground, unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{Pwr}		V
Steady State Continuous Operation		26	
Negative Transient (Note 1)		–1.5	
Positive Load Dump Transient (Note 2)		60	
Logic Supply Voltage Range	V_{DD}	–0.3 to 7.0	V
Logic Supply Current	I_{DD}	5.0	mA
Input Voltage (Note 3)	V_{in}	–0.3 to 7.0	V
Output Clamp Voltage	V_{Clamp}		V
I_O = –20 mA		–3.0 to –20	
I_O = –200 mA		–5.5 to –20	
Output Current Limit (Note 4)	$I_{O(Lim)}$	–3.0 to –6.0	A
Output Clamp Energy (I_O = –1.0 A)	E_{Clamp}		mJ
T_J = 25°C		300	
T_J = 125°C		100	
ESD (Minimum)			V
Human Body Model (Note 5)	HBM	2000	
Machine Model (Note 6)	MM	200	
Power Dissipation (T_A = 25°C) (Note 7)	P_D	4.2	W
Operating Temperature (Note 8)	T_A	–40 to +125	°C
Operating Junction Temperature	T_J	–40 to +150	°C
Storage Temperature	T_{stg}	–55 to +150	°C
Soldering Temperature (for 10 Seconds)	T_{solder}	270	°C
Thermal Resistance			°C/W
Junction–to–Lead	$R_{\theta JL}$	15	
Junction–to–Ambient	$R_{\theta JA}$	30	

NOTES:
1. Negative transient survival capability for 100 ms time duration.
2. Positive transient survival capability with typical automotive load dump condition; 400 ms time constant decay.
3. All input pins (IN1–2, CEN and SFPD).
4. Each output has independent current limiting.
5. Performed in accordance to HBM; C_{Zap} = 100 pF, R_{Zap} = 1500 Ω.
6. Performed in accordance to MM; C_{Zap} = 100 pF, R_{Zap} = 0 Ω.
7. Derate Power Dissipation 33 mW/°C for temperatures above 25°C.
8. Ambient temperature is given as a practical reference; Maximum junction temperature is the limiting factor.
9. ESD data available upon request.

DC ELECTRICAL CHARACTERISTICS (Characteristics noted under conditions 9.0 V ≤ V_{Pwr} ≤ 17 V, 4.5 V ≤ V_{DD} 5.5 V, –40°C ≤ T_L ≤ 125°C, unless otherwise noted, typical values represent approximate mean at T_L = 25°C.)

Characteristic	Symbol	Min	Typ	Max	Unit
POWER INPUT					
Supply Voltage Range (Operational)	V_{Pwr}	9.0	–	17	V
Supply Current (Note 1)					
Both Outputs ON					
(CEN = IN1 = IN2 = 0.7 x V_{DD}, I_{O1} = I_{O2} = –1.0 A)	I_{Pwr}	0.1	4.2	7.0	mA
Standby (CEN = 0.7 x V_{DD}, IN1 = IN2 = 0.3 x V_{DD}, R_L = 12 Ω)	$I_{Pwr(sby)}$	–	3.9	7.0	mA
“Sleep State” (CEN = IN1 = IN2 = 0.3 x V_{DD}, R_L = 12 Ω)	$I_{Pwr(sleep)}$	–	0.2	300	µA
Logic Supply Voltage Range	V_{DD}	4.5	–	5.5	V
Logic Supply Current	I_{DD}	–	0.43	5.0	
Both Outputs ON (IN1 = IN2 = 0.7 x V_{DD}, I_{O1} = I_{O2} = –1.0 A)					mA
Overvoltage Shutdown (Note 2)	$V_{Pwr(ovsd)}$	30	33.2	38	V
Overvoltage Shutdown Hysteresis	$V_{Pwr(hys)}$	0.3	0.5	1.5	V

NOTES: 1. Supply current when both outputs are ON and during standby are measured in the Ground pin while during “sleep state” is measured in the V_{Pwr} pin.

2. Overvoltage Shutdown causes enabled outputs to be forced OFF; Overvoltage fault is immediately reported.

DC ELECTRICAL CHARACTERISTICS (Characteristics noted under conditions 9.0 V ≤ V_{Pwr} ≤ 17 V, 4.5 V ≤ V_{DD} 5.5 V, –40°C ≤ T_L ≤ 125°C, unless otherwise noted, typical values represent approximate mean at T_L = 25°C.)

Characteristic	Symbol	Min	Typ	Max	Unit
POWER OUTPUT					
Drain–to–Source ON Resistance (Note 1)	$R_{DS(on)}$				Ω
(T_J = 25°C, CEN = IN1 = IN2 = 0.7 x V_{DD})					
I_O = –0.5 A. V_{Pwr} = 5.5 V		–	0.2	0.5	
I_O = –1.0 A. V_{Pwr} = 14 V		–	0.14	0.2	
I_O = –2.0 A. V_{Pwr} = 24 V		–	0.14	0.2	
Drain–to–Source ON Resistance (Note 1)	$R_{DS(on)}$				Ω
(T_J = 125°C, CEN = IN1 = IN2 = 0.7 x V_{DD})					
I_O = –0.5 A. V_{Pwr} = 5.5 V		–	–	1.0	
I_O = –1.0 A. V_{Pwr} = 14 V		–	–	0.38	
I_O = –2.0 A. V_{Pwr} = 24 V		–	–	0.38	
Output Self–Limiting Current (Note 2)	$I_{O(Lim)}$	–3.0	–4.1	–6.0	A
(CEN = IN1 = IN2 = SFPD = 0.7 x V_{DD}, R_L = 0 Ω)					
Output OFF Leakage Current	$I_{O(Lkg)}$	–5.0	–45	–150	µA
(CEN = 0.7 x V_{DD}, IN1 = IN2 = 0.3 x V_{DD})					
Output OFF Open Load Sense Current	$I_{O(Sense)}$	–5.0	–45	–150	µA
(CEN = 0.7 x V_{DD}, IN1 = IN2 = 0.3 x V_{DD})					
Output ON Open Load Detection Current (Note 3)	$I_{O(On)}$				mA
(CEN = IN1 = IN2 = 0.7 x V_{DD})					
T_L = –40°C		–2.0	–145	–200	
T_L = 125°C		–2.0	–181	–200	
Output Clamp Voltage (Note 4)	V_{Clamp}				V
(CEN = 0.7 x V_{DD}, IN1 = IN2 = 0.3 x V_{DD})					
I_O = –20 mA		–9.0	–13.2	–20	
I_O = –200 mA		–9.0	–13.5	–20	
Over Temperature Shutdown Range (Note 5)	T_{Lim}	155	–	185	°C
(CEN = IN1 = IN2 = SFPD = 0.7 x V_{DD})					
Over Temperature Shutdown Hysteresis (Note 6)	$T_{Lim(hys)}$	–	–	15	°C

NOTES: 1. $R_{DS(on)}$ applies to OUT1, OUT2 and is independent of output current.

2. Applies to each output; each output has independent self–limiting source current feature; Over Current and Short–to–Ground defined as condition when output source current exceeds $I_{O(Lim)}$; Device ignores Over Current and Short–to–Ground faults from 0 to t_{ss}.

3. Applies to each output; tested for by ramping I_O from 0 until $\overline{\text{STAT}}$ ≤ 0.7 x V_{DD}; defined as the condition when I_O is outside of $I_{O(on)}$ current window.

4. Applies to each output; each output has independent dynamic output voltage clamping feature.

5. Applies to each output; each output has independent thermal shutdown; parameter is measured by ramping temperature until enabled output is disabled; parameter is established by design but is not production tested; thermal fault is immediately reported.

6. Parameter is established by design but is not production tested.

DC ELECTRICAL CHARACTERISTICS (Characteristics noted under conditions 9.0 V ≤ V_{Pwr} ≤ 17 V, 4.5 V ≤ V_{DD} 5.5 V, –40°C ≤ T_L ≤ 125°C, unless otherwise noted, typical values represent approximate mean at T_L = 25°C.)

Characteristic	Symbol	Min	Typ	Max	Unit
CONTROL INTERFACE					
Input Control					V_{DD}
Logic High (I_O = –0.1 A) (Note 1)	V_{IH}	0.7	0.56	–	
Logic Low (I_O = 0) (Note 2)	V_{IL}	–	0.52	0.3	
Input Logic Voltage Hysteresis (V_{IH} – V_{IL})	V_{hys}	50	250	500	mV
Input Pull–Down Current (0.3 x V_{DD} ≤ V_{in} < 0.7 x V_{DD}) (Note 3)	$I_{in(pd)}$	20	44	100	µA
Chip–Enable Threshold					V_{DD}
Logic Low (Note 4)	$V_{CEN(IL)}$	–	0.5	0.3	
Logic High (Note 5)	$V_{CEN(IH)}$	0.7	0.5	–	
Chip–Enable Hysteresis ($V_{CEN(IH)}$ – $V_{CEN(IL)}$)	$V_{CEN(hys)}$	50	150	500	mV
Chip–Enable Pull–Up Current (CEN = 0.7 x V_{DD})	$I_{\overline{CEN}(pu)}$	–2.0	–16.8	–40	µA
Status Low Voltage (I_{in} = 600 µA) (Note 6)	$V_{\overline{STAT}(low)}$	–	0.07	0.2	V_{DD}
Status Pull–Up Current (Note 7)	$I_{STAT(pu)}$	–20	–44	–100	µA
Interrupt (Note 8)					V_{DD}
Logic High	$\overline{INT}_h$	0.7	–	–	
Logic Low	INT_l	–	–	0.3	

NOTES: 1. Upper logic threshold voltage applies to IN1, IN2, and SFPD and expressed in V_{DD} units
2. Lower logic threshold voltage applies to IN1, IN2, and SFPD and expressed in V_{DD} units.
3. Applies to IN1, IN2, and SFPD.
4. Initially have CEN = 0.7 x V_{DD}, Ramp CEN down from V_{DD} until I_O = 0 and note disabling point.
5. Initially have V_{in} = 0.7 x V_{DD}, Ramp CEN up from ground until I_O = 0.1 A and note enabling point.
6. Applies equally to $\overline{\text{STAT1–2}}$ and INT outputs; Measured threshold voltage by applying an "open" fault to OUT1 or OUT2 while forcing 600 µA of current into STAT1–2 or INT.
7. Measured with no faults on OUT1–2, $V_{\overline{STAT}}$ = $V_{\overline{INT}}$ = 0.8 x V_{DD}.
8. The Interrupt output has an internal active current pull–up.

DC ELECTRICAL CHARACTERISTICS (Characteristics noted under conditions 9.0 V ≤ V_{Pwr} ≤ 17 V, 4.5 V ≤ V_{DD} 5.5 V, –40°C ≤ T_L ≤ 125°C, unless otherwise noted, typical values represent approximate mean at T_L = 25°C.)

Characteristic	Symbol	Min	Typ	Max	Unit
OUTPUT DYNAMICS					
Output Short Sense Time (Note 1)	t_{ss}	30	54	100	µs
Output Short Refresh Time (Note 2)	t_{ref}	3.0	4.1	6.0	ms
Output Open Sense ON Time (Note 3)	$t_{os(on)}$	3.0	6.4	12	ms
Output Propagation Delay					µs
Turn–On (Output Low to High) (Note 4)	t_{dlh}	–	7.2	50	
Turn–Off (Output High to Low) (Note 5)	t_{dhl}	–	40	75	
Output Slew Rate					V/µs
Output Rising (Note 6)	SR_r	0.2	11	10	
Output Falling (Note 7)	SR_f	0.2	2.6	10	

NOTES: 1. CEN = 0.7 x V_{DD}, SFPD = 0.3 x V_{DD}, R_L = 0, Step V_{in} from 0.3 x V_{DD} to 0.7 x V_{DD}; Sense time measured from step until $\overline{\text{STAT}}$ = 0.2 x V_{DD}.
2. CEN = IN1 = IN2 = 0.7 x V_{DD}, R_L = 0; Refresh time measured from output disable until output is re–enabled.
3. R_L = "open", Step V_{in} from ground to 0.7 x V_{DD}, Open sense time measured from step until V_{STAT} ≤ 0.2 x V_{DD}.
4. R_L = 12 Ω, C_L = 0.01 µF, step V_{in} from V_{IL} to V_{IH}; Turn–On propagation measured from V_{in} = 0.5 x V_{DD} until V_{out} = 2.0 V (see Figure 2).
5. R_L = 12 Ω, C_L = 0.01 µF, step V_{in} from V_{IH} to V_{IL}; Turn–Off propagation measured from V_{out} = V_{Pwr} –3.0 V until V_{out} = 2.0 V (see Figure 2).
6. R_L = 12 Ω, C_L = 0.01 µF, step V_{in} from V_{IL} to V_{IH}; Output Slew Rate measured from 2.0 V to V_{Pwr} – 3.0 V (see Figure 2).
7. R_L = 12 Ω, C_L = 0.01 µF, step V_{in} from V_{IH} to V_{IL}; Output Slew Rate measured from V_{Pwr} – 3.0 V to 2.0 V (see Figure 2).

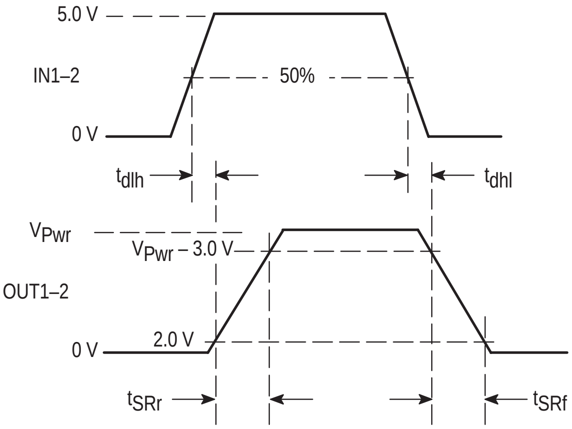


Figure 2. Output Response Waveform

PIN FUNCTION DESCRIPTION

Pin	Symbol	Description
1, 12	IN1, IN2	INput 1 and INput 2 (IN1 and IN2) respectively determine the state of the corresponding output drivers (OUT1 and OUT2) under normal operating conditions. When an input is high, it's corresponding output is active ON, and when low is disabled OFF. IN1 and IN2 have internal active pull–downs which allow a floating input pin to be conservatively interpreted as a logic low, turning Off the output. An unused input should be connected to ground.
2	CEN	Chip Enable (CEN) input pin, when low, disables both outputs (OUT1 and OUT2) and places the device in a "sleep mode" reducing the bias current required from V_{DD} and V_{Pwr}. A falling edge of CEN causes OUT1 and OUT2 to rapidly turn OFF. A falling edge of CEN should precede any V_{DD} shutdown to allow time OUT1 and OUT2 to be disabled. When CEN is low, INTerrupt (INT) and STATus 1 and 2 (STAT1–2) will be tri–stated (high impedance). The CEN pin can also be used for power–on reset and under voltage lockout to disable the outputs for power supply voltages less than 4.5 V. CEN is a dependent input from the system microcontroller unit (MCU) or some other integrated circuit. It has an internal pull–up resistor to V_{DD} affording a floating pin to be interpreted as a logic high. $R_{pull–up}$ is greater than 50 kΩ. If used externally, this pin should be connected to V_{DD}.
3, 10	$\overline{\text{STAT1}}$. $\overline{\text{STAT2}}$	The STATus pins ($\overline{\text{STAT1–2}}$) respectively indicate the presence of faults on OUT1–2. $\overline{\text{STAT1–2}}$ will be logic high during normal operation. A logic low will occur whenever an Open Load, Short–to–Ground, Short–to–Supply (Battery), Thermal Limit, or Overvoltage Shutdown fault condition is experienced on a corresponding output. STAT1–2 are both active low digital drivers. A 10 kΩ resistor between STAT1–2 and the system CPU may improve a Failure Mode Evaluation Analysis (FMEA) score if STAT1–2 are externally shorted to V_{Pwr}. If unused, this pin should be left connected.
4, 9, 16, 21	V_{Pwr}	These pins are connected to the supply and provide load current to the DMOS outputs, are used pumping the DMOS gates, and for Overvoltage shutdown detection of the DMOS. The DMOS outputs will turn ON with 5.5 to 24 V applied to V_{Pwr}. V_{Pwr} is limited to –1.5 V for a maximum duration of 250 ms. A 10 nF de–coupling cap is recommended to be used from V_{Pwr} to Ground.
5, 6, 7, 8, 17, 18, 19, 20	Gnd	These eight pins constitute the circuits ground (Gnd) and also provide heatsinking for the DMOS output transistors. Ground continuity is required for the outputs2 to turn ON.
11	V_{DD}	This pin is to be connected to the 5.0 V logic supply of the system. A 10 nF de–coupling capacitor is recommended from V_{DD} to Gnd.
13, 24	OUT1, OUT2	These pins are connected internally to the DMOS output transistors which source current into the corresponding load. Each output incorporates dynamic clamping to accommodate inductive loads. In addition, each output has independent short to ground detection and protection, current limit detection and protection, thermal limit detection and protection, ON open load and or short to supply (battery) detection. Neither output will turn ON if CEN is logic low. An unused output should be connected to a 10 kΩ load to prevent false fault reporting. A 1.0 nF filter capacitor may be used from OUT to Gnd to provide dV/dt noise filtering.

PIN FUNCTION DESCRIPTION (continued)

Pin	Symbol	Description
14	SFPD	This is a Short Fault Protect Disable (SFPD) input; which when logic high disables the internal current limit timer preventing OUT1–2 from latching OFF when confronted with an overcurrent condition. The condition of SFPD does not affect fault reporting. Current and thermal limit remain active when the SFPD pin is logic high. Having the SFPD pin logic high facilitates the device to drive incandescent lamp loads with peak in–rush currents in excess of three amperes. When SFPD is logic low, an overcurrent demand will latch OFF only the output affected. The device will then automatically begin active re–enabling of the corresponding output affected for the duration of the overcurrent condition. SFPD has an internal active pull–down which affords a floating input pin condition to be conservatively interpreted as a logic low. A 10 kΩ resistor between SFPD and the system CPU may improve the FMEA score if SFPD is externally shorted to OUT2. SFPD should be connected to Gnd or V_{DD} for the desired operating mode and not be left “floating”.
15	GTST	The Gate TeST (GTST) pin is used to stress the devices DMOS gates during testing operations. This pin should normally be connected to ground in the application.
23	$\overline{\text{INT}}$	The INTerrupt pin $\overline{\text{INT}}$ is active logic low and indicates the presence of a fault on either the output. $\overline{\text{INT}}$ can be paralleled with additional fault pins and used as a system CPU interrupt to indicate the presence of a fault. The system CPU can then read STAT1–2 to determine the specific type of fault occurring. INT will be logic high during normal operation. A logic low will result if a fault occurs on either OUT1 or OUT2. INT has an internal active pull–up and requires no external pull–up resistor to be used. The INT output has sufficient current drive capability to afford paralleling of up to five INT pins. A 10 kΩ resistor between INT and the system CPU may improve the FMEA score if INT is externally shorted to OUT1. This pin should be left unconnected if the feature is not used.

Figure 3. Function Table

Device Condition	In	Out	$\overline{\text{STAT}}$	Output Condition	$\overline{\text{STAT}}$ Condition
Normal	Low High	Low High	High High	Normal OFF Normal ON	Normal Normal
Output to Gnd Short	Low	Low	High	Normal OFF	Normal
	High	High/Low	Low	Output in active retry mode. Normal ON when short is removed.	Short fault reported. Fault clears when short is removed.
Open Load	Low	High	Low	Normal OFF	“OFF” open fault reported. Fault clears when load is connected.
	High	High	Low	Normal ON	“ON” open fault reported. Fault clears when load is connected.
Output to V_{Pwr} Short	Low	High	Low	Normal OFF	“OFF” open fault reported. Fault clears when short is removed.
	HIgh	High	Low	Normal ON	“ON” open fault reported. Fault clears when short is removed.
Over Temperature	Low	Low	Low	Normal OFF	Thermal fault reported. Fault clears with no thermal limit.
	High	Low	Low	Output disabled. Output Retries with no thermal limit.	Thermal fault reported. IN low and no thermal limit required to clear the fault.
V_{Pwr} Overvoltage	Low	Low	Low	Normal OFF	Overvoltage fault reported. Fault clears with no overvoltage.
	High	Low	Low	Output disabled. Will reset with no overvoltage.	Overvoltage fault reported. Fault clears with no overvoltage.
“Sleep”/Under Voltage Mode, CEN Low	Low	Low	High–Z	Output disabled.	STAT tri–stated, no faults reported.
	High	Low	High–Z	Output disabled.	STAT tri–stated, no faults reported.

FUNCTIONAL DESCRIPTION

General

The MC33143 is designed as an interface device; between system's electronic control unit and the actuators. It is designed to withstand several abnormal operating conditions, with the capability of reporting it's operating status back to the control unit. The MC33143 will resume normal operation after having experienced 60 V transients on the V_{Pwr} line, output shorts to V_{Pwr}, open loads, output shorts to ground, over current, over temperature, or overvoltage conditions. Status information is available when ever a load experiences any of the faults. In addition, the MC33143 device incorporates internal output transient clamps allowing it to control inductive loads and survive negative voltage spikes without the need of external components.

Power Supply Voltage Requirements

The MC33143 is designed to operate with 5.5 V to 26 V applied to the power supply pin (V_{Pwr}) and 4.5 V to 5.5 V applied to the logic supply pin (V_{DD}). If V_{Pwr} is above the specified Overvoltage Shutdown voltage limit ($V_{Pwr(ovsd)}$) the outputs will be disabled and the status line voltage will transition to a low logic state indicating a fault.

When the CEN voltage is at a low logic state, OUT1 and OUT2 will turn OFF. This provides an under voltage shutdown for V_{Pwr} in the 0 to 4.5 V range. The active low under voltage must be externally provided to the CEN pin.

The MC33143 is designed to survive the loss of V_{Pwr}.

Normal Operations

The MC33143 is considered to be operating normal when the following conditions are met:

8) $5.5\ V \le V_{Pwr} \le 26\ V$.
9) $-40°C \le TJ \le 150°C$.
10) When load currents (I_O) exceed the Output Open "ON" detection current ($I_{O(on)}$) and occur within the Open Sense "ON" time ($t_{os(on)}$) window.
11) When load currents (I_O) are less than the Output Limit Current ($I_{O(Lim)}$) for durations in excess of the Short Sense time (t_{SS}).
12) So long as the output of the device is able to clamp negative voltages produced when switching inductive loads to the specified clamp voltage (V_{Clamp}).

Fault Conditions

Anytime the MC33143 is not operating normal it is said to be operating in a "faulted condition". Fault conditions will result in level changes of the status outputs (STAT1–2) and disable the affected faulted output.

Output Over Current/Short to Ground Faults

For an enabled input, the status line voltage will transition to a low logic level if the output current equals or exceeds the Output Limit current ($I_{O(Lim)}$) for a period of time in excess of the Short Sense time (t_{SS}). Only the affected output will turn off; independent of the corresponding input's condition. The device incorporates an internal short duration Refresh timer (t_{ref}) to mask edge transients due to switching noise. The output will remain off for the short t_{ref} duration and then attempt to re–energize the shorted load. The internal protection circuitry continues to be active during this process. If the short is not removed; the circuitry will sequence and the output will remain off for a another t_{ref} time. This process will continue so long as the output remains shorted and the input remains in a logic high state. If the short is removed from the output, while the input is ON, the MC33143 will return to normal operation and the status line will go to a logic high state after the t_{ref} time–out. The status line will also go to a logic high state on the falling edge of the corresponding input.

Open Load/Short to V_{Pwr} Fault

This condition is commonly referred to as an "ON" open fault. For this fault to be present, the output current of the driver must be at or near zero. Since the MC33143 is a "high–side switch"; It is for this reason a Short to V_{Pwr} fault resembles an Open Load fault, in so far as the MC33143 is concerned. When this fault is present the status line voltage will transition to a low logic level so long as the output current does not exceed the specified Open ON detection current ($I_{O(on)}$) for a duration in excess of the specified Open Sense ON time ($t_{os(on)}$). If the open load or output short to V_{Pwr} condition is removed, and the corresponding input is at a logic high state, the status line voltage will go to a logic high state after the drain current has exceeded $I_{O(on)}$. The ON open fault detection circuit incorporates a voltage comparator which monitors the voltage difference from V_{Pwr} to OUT. When ever the V_{Pwr} to OUT voltage difference falls below 10 mV an ON Open fault is reported. A Short to V_{Pwr} external to any module the MC33143 is in will not be detected as an ON Open fault if the voltage difference from V_{Pwr} to OUT is greater than 10 mV. V_{Pwr} line voltage drops directly impact this detection ability.

Overvoltage Fault

When this fault is present the status line voltage will transition to a logic low state when V_{Pwr} exceeds the specified Overvoltage Shutdown threshold $V_{Pwr(ovsd)}$. This fault produces a "global" response on the part of the MC33143 by turning OFF both outputs independent of input conditions. The outputs will resume normal operation when V_{Pwr} drops the specified Overvoltage Hysteresis $V_{Pwr(hys)}$ value.

Over Temperature Fault

When this fault is present the status line voltage transitions to a low logic level when the junction temperature of either output exceeds the specified Thermal Limit threshold (T_{Lim}). Only the specific faulted output will shutdown independent of the input condition. The other output will continue to operate in a normal fashion unless it also becomes faulted. The thermally faulted output will resume normal operation when the junction temperature drops the specified Over Temperature Shutdown Hysteresis ($T_{Lim(hys)}$) amount.

MOTOROLA

MC33192

MI-Bus Interface Stepper Motor Controller

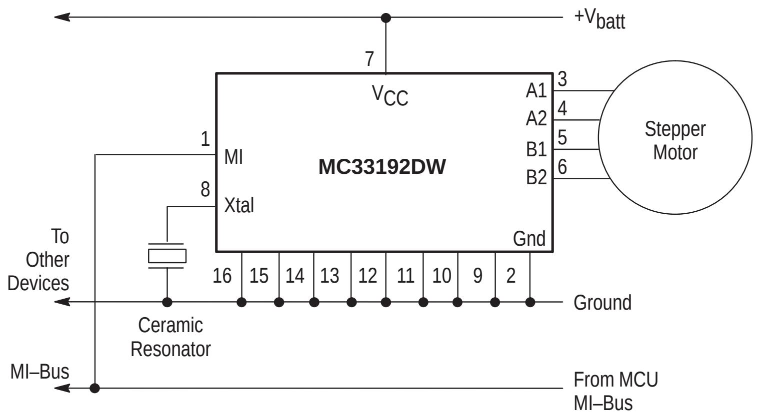
The MC33192 Stepper Motor Controller is intended to control loads in harsh automotive environments using a serial communication bus. The MI–Bus can provide satisfactory real time control of up to eight stepper motors. MI–Bus technology offers a noise immune system solution for difficult control applications involving relay drivers, motor controllers, etc.

The MC33192 stepper motor controller provides four phase signals to drive two phase motors in either half or full step modes. When used with an appropriate Motorola HCMOS microprocessor it provides an economical solution for applications requiring a minimum amount of wiring and optimized system versatility.

The MC33192 is packaged in an economical 16 pin surface mount package and specified at an operating voltage 12 V for – 40°C $\leq T_A \leq$ 100°C.

- Single Wire Open Bus Capability Up to 10 Meters in Length
- Programmable Address Bus System
- Fault Detection of Half–Bridge Drivers and Motor Windings
- Ceramic Resonator For Accurate and Reliable Transmission of Data
- Sub–Multiple of Oscillator End–of–Frame Signal
- MI–Bus Signal Slew Rate Limited to 1.0 V/µs for Minimum RFI
- MI–Bus Error Diagnostics
- Non–Functioning Device Diagnotics
- Over Temperature Detection
- Address Programming Sequence Status
- Load and Double Battery (Jump Start) Protection

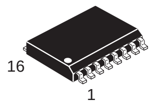
Simplified Application



This device contains 1,528 active transistors.

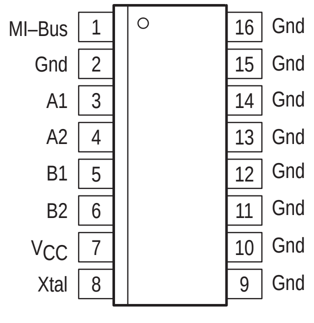
MI–BUS INTERFACE STEPPER MOTOR CONTROLLER

SEMICONDUCTOR TECHNICAL DATA



DW SUFFIX
PLASTIC PACKAGE
CASE 751G
(SO–16L)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC33192DW	T_A = – 40° to +100°C	SO–16L

MAXIMUM RATINGS (All voltages are with respect to ground, unless otherwise noted.)

Rating	Symbol	Value	Limit
Power Supply Voltage Continuous Operation Transient Survival (Note 1)	 V_{CC} V_{LD}	 25 40	V
Digital Input Voltage	V_i	0.3 to V_{CC} + 0.3	V
Output Current (T_A = – 40°C)	I_{OLT}	260	mA
Output Current (T_A = 100°C)	I_{OHT}	150	mA
Storage Temperature	T_{stg}	– 40 to +150	°C
Operating Temperature (Note 2)	T_A	– 40 to +125	°C
Junction Temperature	T_J	– 40 to +150	°C
Power Dissipation (T_A = 100°C)	P_D	0.5	W
Load Dump Transient (Note 3)	V_{LD}	40	V

DC ELECTRICAL CHARACTERISTICS (Characteristics noted under conditions 9.0 V ≤ V_{CC} ≤ 15.5 V, – 40°C ≤ T_A ≤ 100°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Standby Current (V_{CC} = 15.5 V) (Note 4)	I_Q	–	–	12	mA
Output Current (V_{CC} = 15.5 V)	I_O	–	120	–	mA
H–Bridge Saturation Voltage (I_O = 150 mA) (Note 5) T_A = – 40°C T_A = 25°C T_A = 100°C	$V_{O(sat)}$	– – – –	– 1.3 1.2 1.1	– 1.6 1.6 1.6	V
Address Programming Current (T_A = 25°C) (Note 6)	I_{pc}	–	1.2	–	A

CONTROL LOGIC ELECTRICAL CHARACTERISTICS (Characteristics noted under conditions 9.0 V ≤ V_{CC} ≤ 15.5 V, – 40°C ≤ T_A ≤ 100°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Oscillator (Note 7)	f_{cl}		640	–	kHz
Message Time Slot (V_{CC} = 12 V) (Note 8)	t_s	24.8	25	25.2	µs
Urgent Output Disable (V_{CC} = 12 V) (Note 9)	t_{od}	9 x t_s	–	–	µs
Internal MI–Bus Pull–Up Resistor	R_{pu}	6.0	–	20	kΩ
Internal MI–Bus Zener Diode Clamp Voltage	V_{cl}	–	18	–	V
Address Programming Voltage (Note 10)	V_p	10	12	14	V
Program Energize Time	t_{ppw}	200		1000	µs
MI–Bus Slew Rate	$\Delta V/\Delta t$	1.0	1.5	2.0	V/µs
MI–Bus "0" Level Input Voltage Threshold	V_{il}	–	–	1.3	V
MI–Bus "1" Level Input Voltage Threshold	V_{ih}	2.4	–	–	V
MI–Bus "0" Level Output Voltage (I_O = 30 mA)	V_{OL}	–	–	1.0	V
Power–On Reset Time (V_{CC} ≥ 7.5 V)	t_{por}	–	250	–	µs

NOTES:
1. Transient capability is defined as the positive overvoltage transient with 250 ms decay time constant. The detection on an overvoltage condition causes all H–Bridges to be latched "off".
2. Ambient temperature is given as a convience; Maximum junction temperature is the limiting factor.
3. Load Dump is the inductive transient voltage imposed on an automotive battery line as a result of opening the battery connection while the alternator system is producing charge current. The detection on an overvoltage condition causes all H–Bridges to be latched "off".
4. Standby Current is with both H–Bridges "off" (Inh1 = Inh2 = 0).
5. H–Bridge Saturation Voltage is referenced to the positive supply or ground respective of the H–Bridge output being High or Low. Saturation voltage is the voltage drop from the output to the positive supply (with output High) and the voltage drop to ground (with output Low).
6. Address Programming Current is the current encountered when the bus is at 12 V during address programming.
7. A typical application uses an external ceramic resonator crystal having a frequency of 644 kHz. An internal capacitor in parallel with ceramic resonator is used to shift the frequency to the working frequency of 640 kHz. The frequency accuracy of the oscillator is dependant on the capacitor and ceramic resonator tolerance (usually ±1.0%).
8. The Message Time Slot is the time required for one complete device message transfer. The message time is equivalent to a total of 16 periods of the oscillator frequency used.
9. If the MI–Bus becomes shorted to ground, all MC33192 outputs will be disabled after a period of nine time slots ($9t_s$).
10. MI–Bus voltage required for address programming.

GENERAL DESCRIPTION

The MC33192 is a serial stepper motor controller for use in harsh automotive applications using multiplex wiring. The MC33192 provides all the necessary four phase drive signals to control two phase bipolar stepper motors operated in either half or full step modes. Multiple stepper motor controllers can be operated on a real time basis at step frequencies up to 200 Hz using a single microcontroller (MCU). A primary attribute of operation is the utilization of the MI–Bus message media to provide high noise immunity communication ensuring very high operating reliability of motor stepping.

The MC33192 is designed to drive bipolar stepper motors having a winding resistance of 80 Ω at 20°C with a supply voltage of 12 V. It is supplied in a SO–16L plastic package having eight pins, on one side, connected directly to the lead frame thus enhancing the thermal performance to allow a power dissipation of 0.5 W at 120°C ambient temperature.

Multiple Simultaneous Motor Operation

Several motors can be controlled in a serial fashion, one after the other, using the same software time base. The time base determines the step frequency of the motors. A single motor can be operated at a maximum speed of 200 Hz pull–in with a duration of 5.0 ms per step. Three motors can be operated simultaneously using a 68HC05B6 MCU at the same time base (200 Hz) with about 1.7 ms per step. A 68HC11 MCU can control 4 stepper motors with adequate program step time. The step frequency must be decreased to control additional motors. To control eight motors simultaneously would require the motor speed to be decreased to 100 Hz producing about 2.0 ms time duration per step with adequate program time.

MI–Bus General Description

The Motorola Interconnect Bus (MI–Bus) is a serial push–pull communications protocol which efficiently supports distributed real time control while exhibiting a high level of noise immunity.

Under the SAE Vehicle Network categories, the MI–Bus is a Class A bus with a data stream transfer bit rate in excess of 20 kHz and thus inaudible to the human ear. It requires a single wire to carry the control data between the master MCU and its slave devices. The bus can be operated at lengths up to 15 meters.

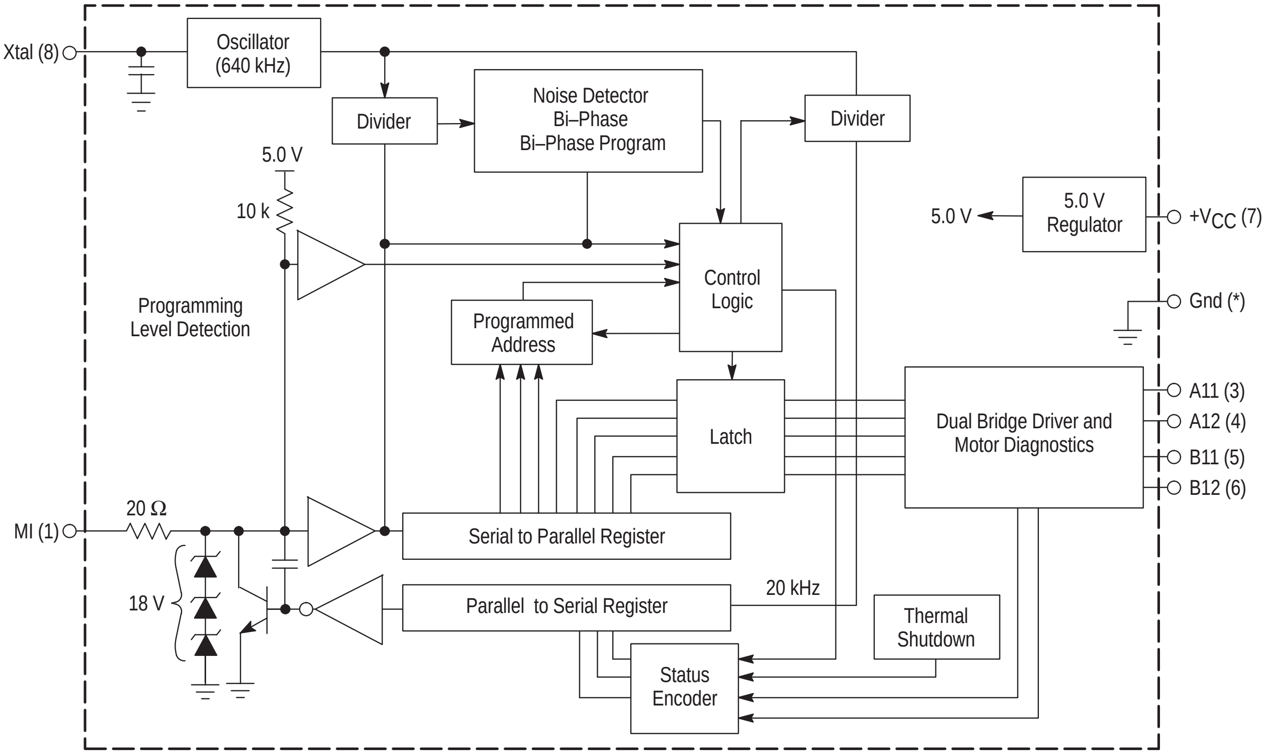
At 20 kHz the time slot used to construct the message (25 µs) can be handled by software using many MCUs available on the market.

The MI–Bus is suitable for medium speed networks requiring very low cost multiplex wiring. Aside from ground, the MI–Bus requires only one signal wire connecting the MCU to multiple slave MC33192 devices with individual control.

A single MI–Bus can accomplish simultaneous automotive system control of Air Conditioning, Head Lamp Levellers, Window Lifts, Sensors, Intelligent Coil Drivers, etc. The MI–Bus has been found to be cost effective in vehicle body electronics by replacing the conventional wiring harness.

Figure 1 shows the internal block diagram of the MC33192 Stepper Motor Controller.

Figure 1. MC33192 Stepper Motor Conroller Block Diagram



NOTE: (*) Pins 2, 9, 10, 11, 12, 13, 14, 15 and 16 are common electrical and heatsink ground pins for the device.

MI–Bus Access Method

The information on the MI–Bus is sent in a fixed message frame format (See Figure 4). The system MCU can take control of the MI–Bus at any time with a start bit which violates the law of Manchester Bi–Phase code by having three consecutive Time Slots ($3t_S$) held constantly at a Logic "0" state.

Push–Pull Communication Sequence

Communication between the system MCU and slave MC33192 devices always use the same message frame organization. The MCU first sends eight serial data bits over the MI–Bus comprised of five control bits followed by three address bits. This communication sequence is called a "Push Field" since it represents command information sent from the MCU. The sequence of the five control data bits follow the order D0, D1, D2, D3 and D4. The three address bits are sent in sequential order A0, A1 and A2 defining a binary address code. The condition of MI–Bus during any of the control bit time windows defines a specific control function as shown in Figure 2. A "Pull Sync" bit is sent at the end of the Push Field, the positive edge of which causes all data sent to the selected device to be latched into the output circuit.

Figure 2. Push Field Data Bits

Bit	Name	Control Function
D4	Inh2	Inhibits H–Bridge 2
D3	Dir2	Establishes Direction of H–Bridge 2 Current
D2	E	Energizes Bridge Coils 1 and 2
D1	Dir1	Establishes Direction of H–Bridge 1 Current
D0	Inh1	Inhibits H–Bridge 1

After the Pull Sync bit is sent, following the Push Field, the MCU listens on the MI–Bus for serial data bits sent back from the previously addressed MC33192 device. This portion of the communication sequence starts the "Pull Field Data" since it represents information pulled from the addressed MC33192 and received by the MCU.

The address selected MC33192 device sends data, in the form of status bits, back to the MCU reporting the devices condition. At the end of the Push Field the MCU outputs a Pull Sync bit which signals the start of the Pull Field. In the Pull Field are three bits (S2, S1 and S0) which report the status of the previously addressed MC33192 according to Figure 3.

Figure 3. Pull Field Status Bits

S2	S1	S0	Status	Comments
0	0	0	Not used	
0	0	1	Free	
0	1	0	No Back EMF	Drivers and/or coils failed
0	1	1	Free	
1	0	0	Normal/OK	
1	0	1	Thermal	Chip temperature > 150°C
1	1	0	Programming	PROM energized
1	1	1	Selection failed	Noise on MI–Bus, failed or disconnected module

The positive edge of the Pull Sync pulse (set by the MCU) causes all Push Field Data sent to the selected MC33192 to be stored in the output latch circuit in time with the strobe pulse. This means the data bits are emitted in real time synchronization with the MCU's machine cycle. The strobe pulse occurs only after the Push Field sequence is validated by the address selected device.

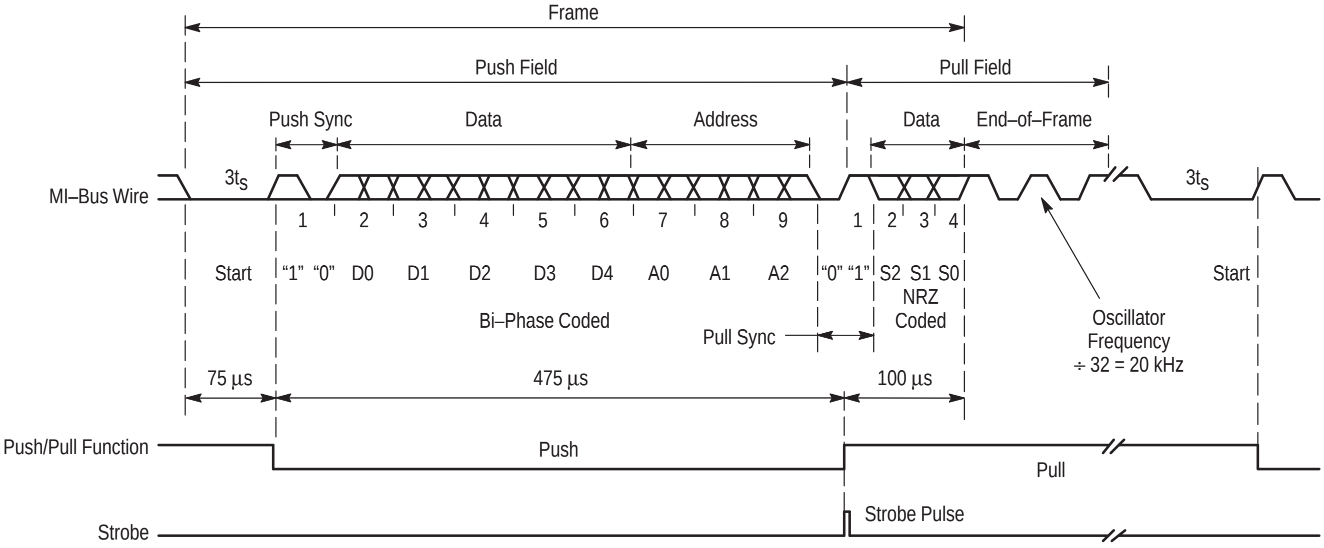
Message Validation

The communication between the MCU and the selected MC33192 device is valid only when the MCU reads (receives) the Pull Field Data having the correct codes (excluding the code "1–1–1" and "0–0–0") followed by an End–of–Frame signal. The frequency of the End–of–Frame signal may be a sub–multiple of the selected devices local oscillator or related to an internal or external analog parameter using a Voltage to Frequency Converter.

Error Detection

An error is detected when the Pull Field contains the code "1–1–1" followed by the End–of–Frame permanently tied to a logic "1" state (internally from 5.0 V through a pull–up resistor). This means the communication between the MCU and the selected device was not obtained.

Figure 4. MI–Bus Timing Diagram



There are four types of system error detections which are not mutually exclusive; These are:

1) Noise Detection

The system MC33192 slave devices receive the Push Field message from the MCU twice for each Time Slot (t_S) of the Bi–Phase Code. A receive error occurs when the two message samples fail to “logic wise” match. Noise and Bi–Phase detection are discussed further under Message Coding.

2) Bi–Phase Detection

The system slave devices receiving the Push Field message from the MCU detect the Bi–Phase Code. A detector error occurs when the two time slots of the Bi–Phase Code do not contain an Exclusive–OR logic function.

3) Field Check

A field error is detected when a fixed–form bit field contains an improper number of bits. A bit error can also be detected by the MCU during the Push Field. The MCU can simultaneously monitor the MI–Bus at the time it is sending data. A bit error is detected if the sent bit value does not match the value which was monitored.

4) Urgent Output Disable

If the MI–Bus becomes shorted to ground, the slave device outputs will be disabled after a period of $9t_S$. The MCU itself can take advantage of this feature to “globally” disable the outputs of all system slave devices by keeping the MI–Bus at a logic “0” level for a duration of $9t_S$ or more. Normal operation is resumed when the MCU sends a “standard” instruction over the MI–Bus.

Basic Stepper Motor Construction and Operation

Stepper motors are constructed with a permanent magnet rotor magnetized with the same number of pole pairs as contained in one stator coil section. Operationally, stepper motors rotate at constant incremental angles by stepping one step every time the current switches discretely in one stator field coil causing the North–South stator field to rotate either clockwise or counter–clockwise causing the permanent magnet rotor to follow (see Figure 5). For simplicity, assume the starting condition of the A1 to A2 stator field to be top to bottom polarized N to S and the B1 to B2 stator field to be left to right polarized N to S. The resulting stator field will produce a vector which points in the direction of position 3. The rotor will, in this case, be in the position shown in Figure 5 (pointing to position 1). This initial condition corresponds to that of step 1 in Figure 6. As the direction of current flow in the B1 to B2 stator field is reversed, the field polarity of the B1 to B2 also reverses and is left to right polarized S to N. This causes the resulting stator field vector to point in the direction of position 4. This in turn causes the N–S rotor to follow and rotate 90° in a clockwise direction and point in the direction of position 2. This condition corresponds to step 2 of Figure 6. Continued clockwise rotor steps will be experienced as the stator field continues to be incrementally rotated as shown in steps 3, 4, 5, etc. of Figure 6. The 90° steps in this simplistic example constitute “full steps”. It is to be noticed that both coils, in the foregoing full step example, were simultaneously energized in one of two directions. It is possible to increment the rotor in 45° “intermediate steps” or “half steps” by alternately energizing only one stator coil at a time in the appropriate direction while turning the other stator coil off. The drive signals for Half Step operation are shown in Figure 7. The Power output stages of the MC33192 consist of two H–Bridges capable of driving two–phase bi–polar permanent magnet motors in either half or full step increment.

Figure 5. Permanent Magnet Stepper Motor

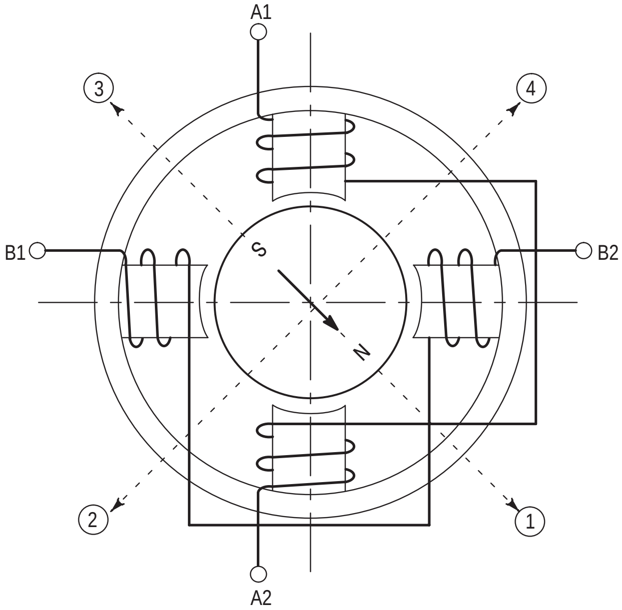


Figure 6. 4–Step “Full Step” Operation

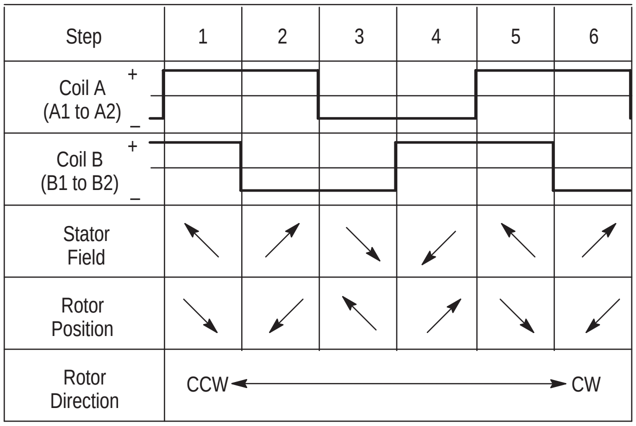
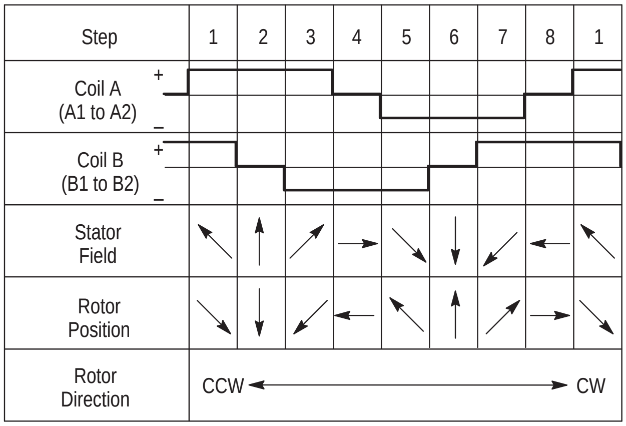


Figure 7. 8–Step “Half Step” Operation



Permanent magnetic stepping motors exhibit the characteristic ability to hold a shaft rotor position with or without a stator coil being energized. Normally the shaft holding ability of the motor with a stator coil energized is referred to as “Holding Torque” while “Residual Torque” or “Detent Torque” refers to the shaft holding ability when a stator coil is not energized. The Holding Torque value is dependent on the interactive magnetic force created by the resulting energized stator fields with that of the permanent magnet rotor. The Residual Torque is a function of the physical size and composition of the permanent magnet rotor material coupled with its intrinsic magnetic attraction for the un–energized stator core material and as a result, the weaker of the two torques.

It is to be noted when using half step operation, only one coil is energized during alternate step periods which produces a somewhat weaker Holding Torque. Holding Torque is maximized when both coils are simultaneously energized. In addition, since each winding and resulting flux conditions are not perfectly matched for each half step, incremental accuracy is not as good as when full stepping.

Two Phase Drive Signals

The DIR1 and DIR2 bits in the Data Frame of the Push Field determine the direction of H–Bridge current flow, and thus the magnetic field polarization of the stator coils, for H–Bridge outputs “A” and “B” respectively. The directional signals DIR1 and DIR2, generated by the MCU, communicate over the MI–Bus to control the two H–Bridge power output stages of the MC33192 to drive two phase bipolar permanent magnet motors. Figure 8 shows the MC33192 truth table to accomplish incremental stepping of the motor in a clockwise or counter–clockwise direction in either half or full step modes. The stator field polarization and rotor position are also shown for reference relative to the basic stepper motor of Figure 5.

Figure 8. Truth Table and Serial Push Field Data Bits For Sequential Stepping

		Push Field Bits											
Step		D0	D1	D2	D3	D4	H–Bridge Outputs				Stator Field (Note 2)	Rotor Position (Note 2)	Direction of Shaft Rotation
Full	Half	Inh1	DIR1	E	DIR2	Inh2	A1	A2	B1	B2			
1	1	1	0	1	0	1	1	0	1	0	↖	↘	CCW ↕ CW
–	2	1	0	1	X	0	1	0	Z	Z	↑	↓	
2	3	1	0	1	1	1	1	0	0	1	↗	↙	
–	4	0	X	1	1	1	Z	Z	0	1	→	←	
3	5	1	1	1	1	1	0	1	0	1	↘	↖	
–	6	1	1	1	X	0	0	1	0	0	↓	↑	
4	7	1	1	1	0	1	0	1	1	0	↙	↗	
–	8	0	X	1	0	1	Z	Z	1	0	←	→	
		0	X	X	X	0	Z	Z	Z	Z			
		1	1	0	1	1	Z	1	Z	1			
		1	0	0	0	1	1	Z	1	Z			
		1	1	0	0	0	Z	1	Z	Z			
		0	0	0	1	1	Z	Z	Z	1			

NOTES: 1. X = Don’t care; Z = High impedance; 1 = High (active “on”) state; 0 = Low (inactive “off”) state.
2. The stator field direction and position of the rotor are shown for explanation purposes and relative to the basic stepper motor shown in Figure 3.
3. DIR1 establishes the direction of current flow in H–Bridge “A”.
4. DIR2 establishes the direction of current flow in H–Bridge “B”.

MI–Bus Interface Description

The MI–Bus Interface shown in Figure 9 is made up of a single NPN transistor (Q1). The two main functions of this NPN transistor are:

1) To drive the MI–Bus during the Push Field with approximately 20 mA of current while also exhibiting low saturation characteristics ($V_{CE(sat)}$).

2) To protect the Input/Output (I/O) pin of the MCU against any Electro–Magnetic Interference (EMI) captured on the bus wire.

Without the NPN transistor, the MCU could be destroyed as a result of receiving excessive EMI energy present on the bus. In addition, the transistor blocks the MCU from receiving EMI signals which could erroneously change the data direction register of the MCU I/O.

The MCU input pin (P_{in}), used to read the Pull Field of the MI–Bus, is protected by two diodes (D2 and D3) and two resistors (R5 and R6). Any transient EMI generated voltage present on the bus is clamped by the two diodes to a windowed voltage value not to be greater than the V_{DD} or less than the V_{SS} supply voltages of the MCU.

MI–Bus Levels

The MI–Bus can have one of two valid logic states, recessive or dominant. The recessive state corresponds to a Logic “1” and is obtained through use of a 10 kΩ pull–up resistor (R9) to 5.0 V. The dominant state corresponds to a Logic “0” which represents a voltage less than 0.3 V and created by the $V_{CE(sat)}$ of Q1.

MI–Bus Overvoltage Protection

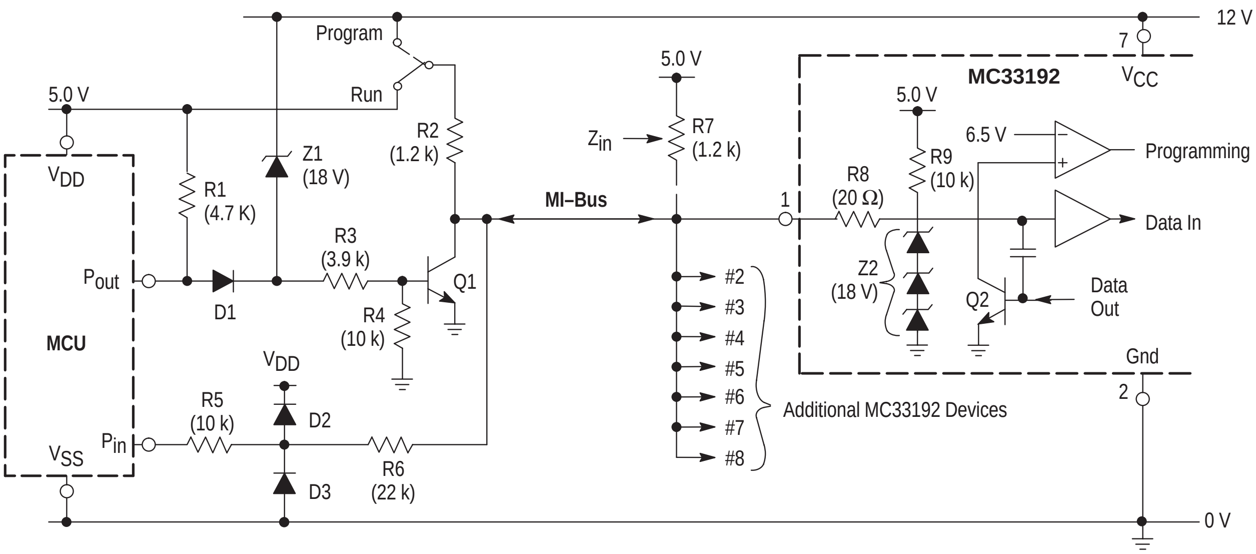
An external zener diode (Z1) is incorporated in the interface circuit so as to protect the MCU output pin (P_{out}) from overvoltages commonly encountered in automotive applications as a result of “Load Dump” and “Jump Start” conditions. Load Dump is defined as the inductive transient generated on the battery line as a result of opening the battery connection while the alternator system is producing charge current. Jump Start overvoltages are the result of paralleling the installed automotive battery, through the use of “jumper cables”, to an external voltage source in excess of the vehicles nominal system voltage. For 12 V automotive systems, it is common for 24 V “jump start” voltages to be used.

When an overvoltage situation (>18 V) exists, due to a load dump or jump start condition, the zener diode (Z1) is activated and supplies base current to turn on the NPN transistor Q1 causing the bus to be pulled to less than 0.3 V producing a Logic “0” on the MI–Bus. After a duration corresponding to $8t_S$ (200 µs) of continuous Logic “0” on the bus all MC33192 devices will disable their outputs. Normal operation is resumed, following the overvoltage, by the MCU sending out a “standard” message instruction.

MI–Bus Termination Network

The MI–Bus is resistively loaded according to the number of MC33192 devices installed on the bus. Each MC33192 has an internal 10 kΩ pull–up resistor to 5.0 V. An external pull–up resistor (R7) is recommended to be used to optimally adjust termination of the bus for a load resistance of 600 Ω.

Figure 9. MI–Bus MCU Interface



MESSAGE CODING

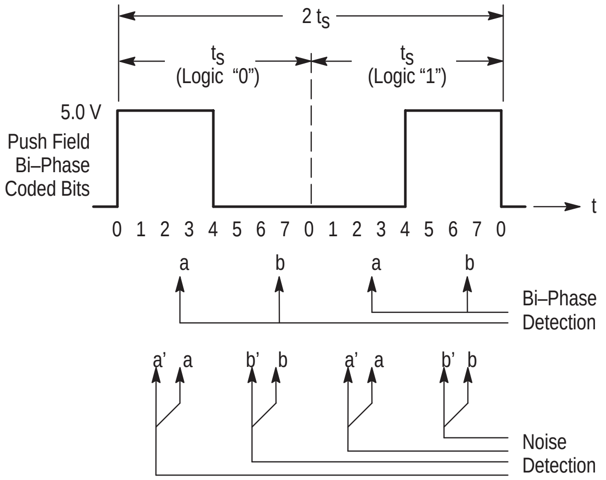
Bi–Phase Coding and Detection

The Manchester Bi–Phase code shown in Figure 10 requires two time slots ($2t_S$) to encode a single data bit. This allows detection of a single error at the time slot level. The logic levels "1" or "0" are determined by the organization of the two time slots. These always have complementary logic levels of either zero volts or plus five volts, which are detected using an Exclusive OR detection circuit during the Push Field sequence. A "1" bit is detected when the first time slot is set to a zero logic state (0 V) followed by the second time slot set to a logic state one (5.0 V). Conversely, a "0" bit is detected when the first time slot is set to the logic state "one" (5.0 V) followed by a second time slot set to a "zero" logic state (0 V). For these two bits are Exclusive–ORs of each other.

The addressed devices receiving the Push Field detect the Bi–Phase code. Bi–Phase detection involves the sampling of the Push Field Bi–Phase code twice (a and b) for each time slot. A code error occurs when the two time slots of the Bi–Phase do not follow a logical Exclusive–OR function (see Figure 10).

Noise monitoring is accomplished by sampling the Push Field Bi–Phase code twice (a and a') and (b and b') during each time slot. A noise error is detected if the two sample values do not have the same logical level.

Figure 10. Noise/Bi–Phase Detection



Each message frame consists of two fields: The Push Field, in which data and addresses are transferred by the MCU to the slave device; and the Pull Field, in which serial data is transferred back to the MCU from the address selected slave device. The message frame is broken down into seven individual field segments as indicated in Figure 4 (Start, Push Field Sync, Push Field Data, Push Field Address, Pull Field Sync, Pull Field Data, and End–of–Frame). The following lists the bit size and function of each of these segments:

1) **Start** is the start of message and consists of three time slots ($3t_S$) having the dominant Logic "0" state of less than 0.3 V. Holding the MI–Bus at ground for three time slots ($3t_S$) marks the beginning of the message frame by violating the law of the Manchester Code.

2) **Push Field Sync** is a single bit which establishes initial timing for the Push Field Data to follow.

3) **Push Field Data** is comprised of five serial data bit fields (D0, D1, D2, D3 and D4) which comprise the instruction set defining the configuration and condition of the two H–Bridge output stages.

4) **Push Field Address** is comprised of three serial data bit fields (A0, A1 and A2) which define the address or name of a MC33192 on the MI–Bus.

5) **Pull Field Sync** is a single bit which establishes the end of the Push Field and the initial start timing for the Pull Field Data to follow.

6) **Pull Field Data** is made up of three serial data bit fields (S2, S1 and S0) which contain the existing status information of an addressed MC33192.

7) **End–of–Frame** field is a signal which communicates to the MCU that the status information sent by the MC33192 is complete.

The Push Field Sync bit, Push Field Data bits, Push Field Address bits, Pull Field Sync bit are all coded by the Manchester Bi–Phase L Code. The Pull Field Data bits are Non–Return to Zero (NRZ) coded. The End–of Frame field is a square wave signal with a frequency of 20 kHz or higher so as to avoid a condition which causes a bus violation.

The Manchester Bi–Phase L code requires two time slots ($2t_S$) to encode a single bit. This allows a single error to be detected during the time slot.

Address Programming involves the use of three instructions. Refer to Figure10.

First Instruction Set the MI–Bus continuously at 12 V. This places the MC33192 in the programming mode. Programming is possible only when the MI–Bus is at 12 V.

Next, the MCU serially enters "Logic Zeros" in all five Push Field Data bit positions (D0, D1, D2, D3 and D4) followed by the designated address value in the Push Field Address positions (A0, A1, & A2).

The MCU now waits 275 µs before starting the second instruction. The total of the Pull time, Delay time, and Bus Violation time (V) of the second instruction (150 µs, 275 µs and 75 µs respectively) will cause the memory cell to be energized for 500 µs. During the first 150 µs of this time, the MCU is checking the Pull Field Data Bits S2, S1 and S0 looking for the **programming code "110"** to indicate complete activation of the memory cell.

Second Instruction (MI–Bus voltage remaining at 12 V)

The MCU repeats the same Push Field instruction as previously sent in the First Instruction; entering all "Logic Zeros" in the Push Field Data positions followed by the designated Push Field Address value in the address positions.

Again, the MCU waits for the Pull, Delay, and Bus violation time while checking the Pull Field Data bits looking for the **programming code "110"** code. The MCU must repeat the initial Push Field Address instruction until a "110" code is received before advancing to the Third Instruction.

Third Instruction The MI–Bus voltage is lowered to 5.0 V.

The MCU serially loads "Logic Zeros" in all five Push Field Data bit positions followed by the programmed address in the Push Field Address positions. The MCU then checks the Pull Field Address status bits looking this time for the

programming OK code "100" indicating the address programming to be executed.

The First and Second Instructions must be repeated until the MCU successfully receives the programming code "100". Address programming is not complete until a "100" OK status is received by the MCU with the MI–Bus voltage at 5.0 V.

Overwrite–Bit Programming involves the use of two instructions. See Figure 11.

First Instruction Have the MI–Bus continuously set at 12 V so as to have the MC33192 in the programming mode. Programming can only be accomplished with the MI–Bus at 12 V.

The MCU serially enters "Logic Zeros" for the Push Field Data bits D0, D1, D2 and D3 and a Logic "1" for D4 bit followed by the programmed address bits A0, A1 and A2.

The MCU now waits 275 µs before starting the second instruction. The total of the Pull time, Delay time, and Bus Violation time (V) of the second instruction (150 µs, 275 µs and 75 µs respectively) will cause the memory cell to be energized for 500 µs. During the first 150 µs of this time, the MCU is checking the Pull Field Data Bits for the status of bits S2, S1 and S0 looking for the **programming code "110"** to indicate complete activation of the memory cell.

Second Instruction (MI–Bus remaining at 12 V)

The MCU repeats the first instruction outlined above until the **programming OK code "100"** is sent back to the MCU from the selected MC33192 indicating the overwrite–bit protection to be programmed. If after eight repeat instructions, the programming code "110" or the OK code "100" is not generated four times in succession, programming of the MC33192 has failed. If this occurs, the Overwrite–Bit Programming sequence should be reviewed and re–started from the beginning.

H–Bridge Output

The H–Bridge output drive circuit and associated diagnostic encoder are shown in Figure 12. The H–Bridge output uses internal diode clamps (D1, D2, D3, D4) to provide transient protection of the output transistors necessary when switching inductive loads associated with stepper motors.

Back EMF Detection

Three different Back EMF currents can occur depending on whether the motor is running or manner in which it is being stopped. Referring to Figure 12; When the Dir1 bit is set to logic 0, the direction of current flow will be from V_{CC} through transistor Q2, Coil A (A1 to A2), and transistor Q4 to ground.

1) **Fast Decay** (when transistors Q1, Q2, Q3 and Q4 are switched off).

When the current flowing in the coil is stopped by setting the Inh1 bit to logic 0, the back EMF current will circulate through the voltage supply (V_{CC}) and diodes D1 and D3. At that time, the voltage developed across the diode D1 is detected by transistor Q6. The generated voltage pulse of Q6 is then encoded and sent, in the Pull–Field, to the microprocessor.

2) **Slow Decay** (Q3 and Q4 are switched off)

When the current flowing in the coil is stopped by setting the E bit to logic 0, the back EMF current will circulate through the diode D1 and transistor Q2 which is already switched on.

3) **When Motor is Running**

The rotational direction of the motor changes whenever the Dir bit state is changed. When the Dir bit is changed from a logic 0 to a logic 1, transistors Q2 and Q4 are switched off and transistors Q1 and Q3 are switched on. At this time, the back EMF current will circulate from ground through diodes D1 and D3 to the voltage supply (V_{CC}). In all cases, the back EMF currents will be detected by transistors Q5 and Q6.

Figure 11. Address Programming Diagram

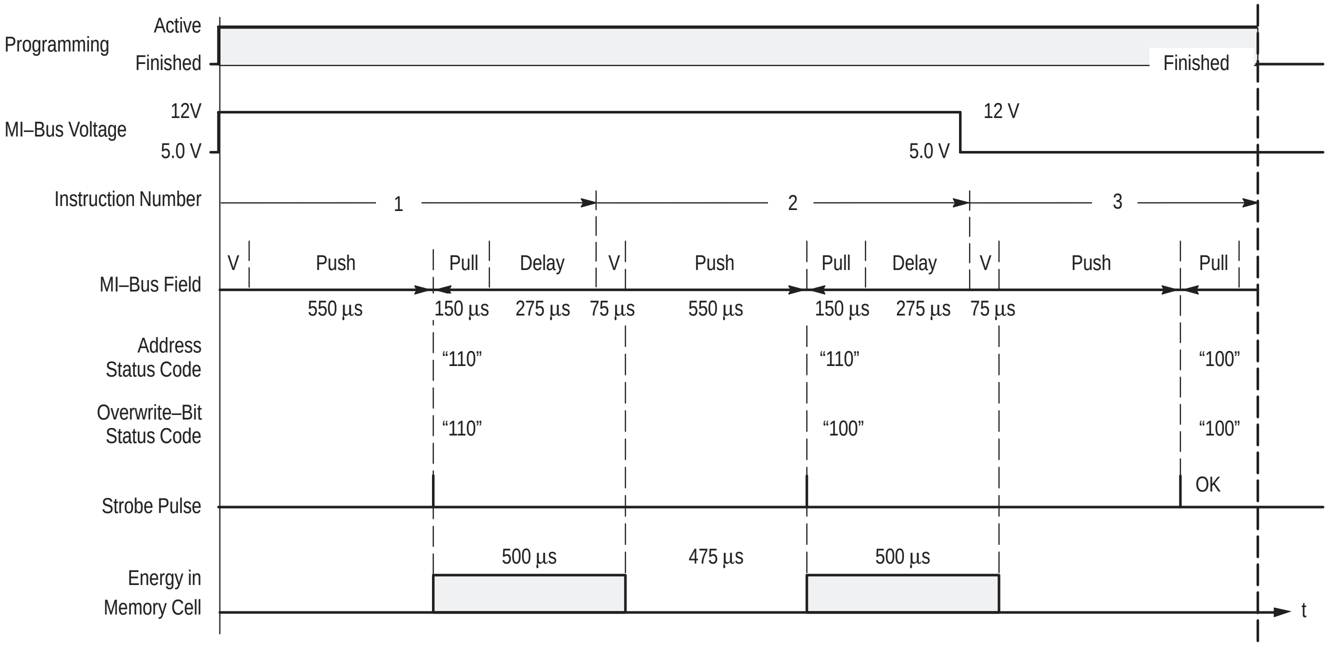
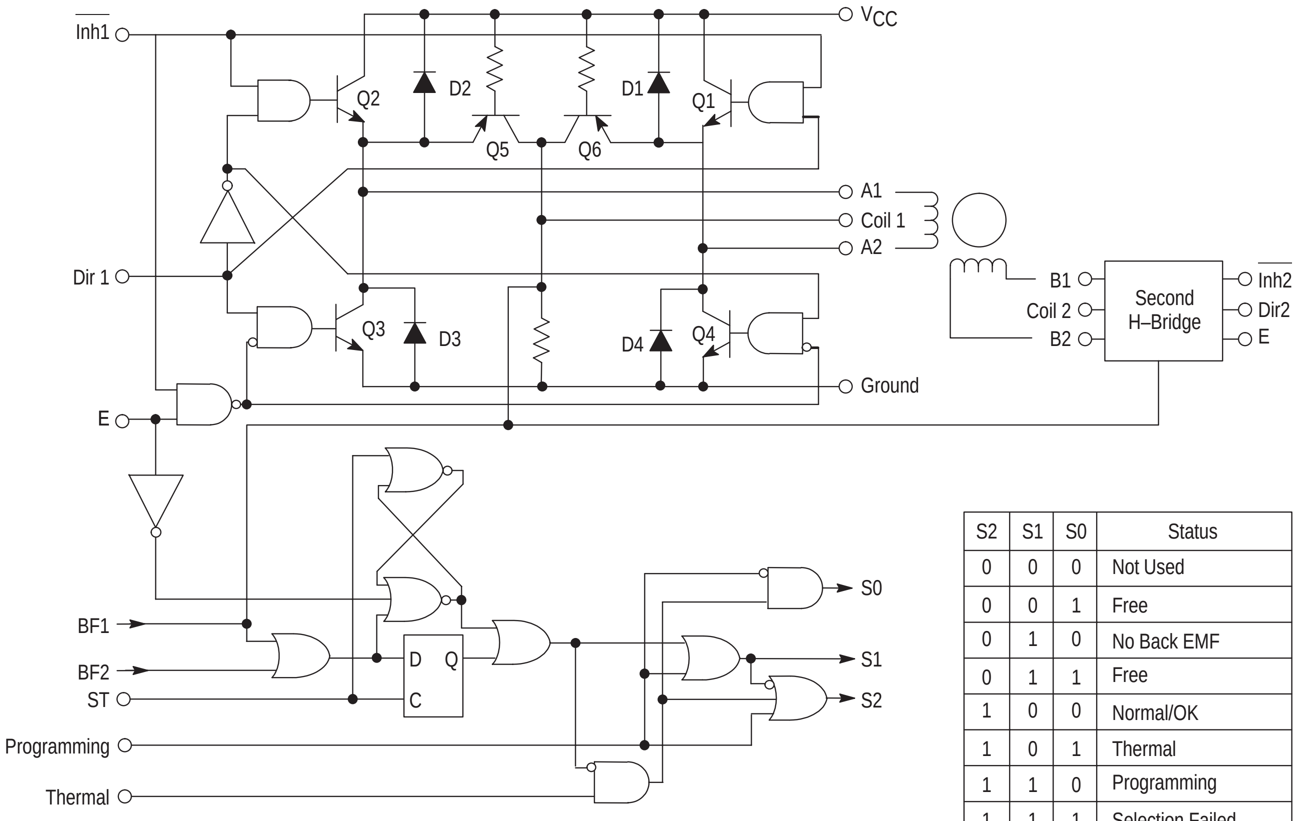
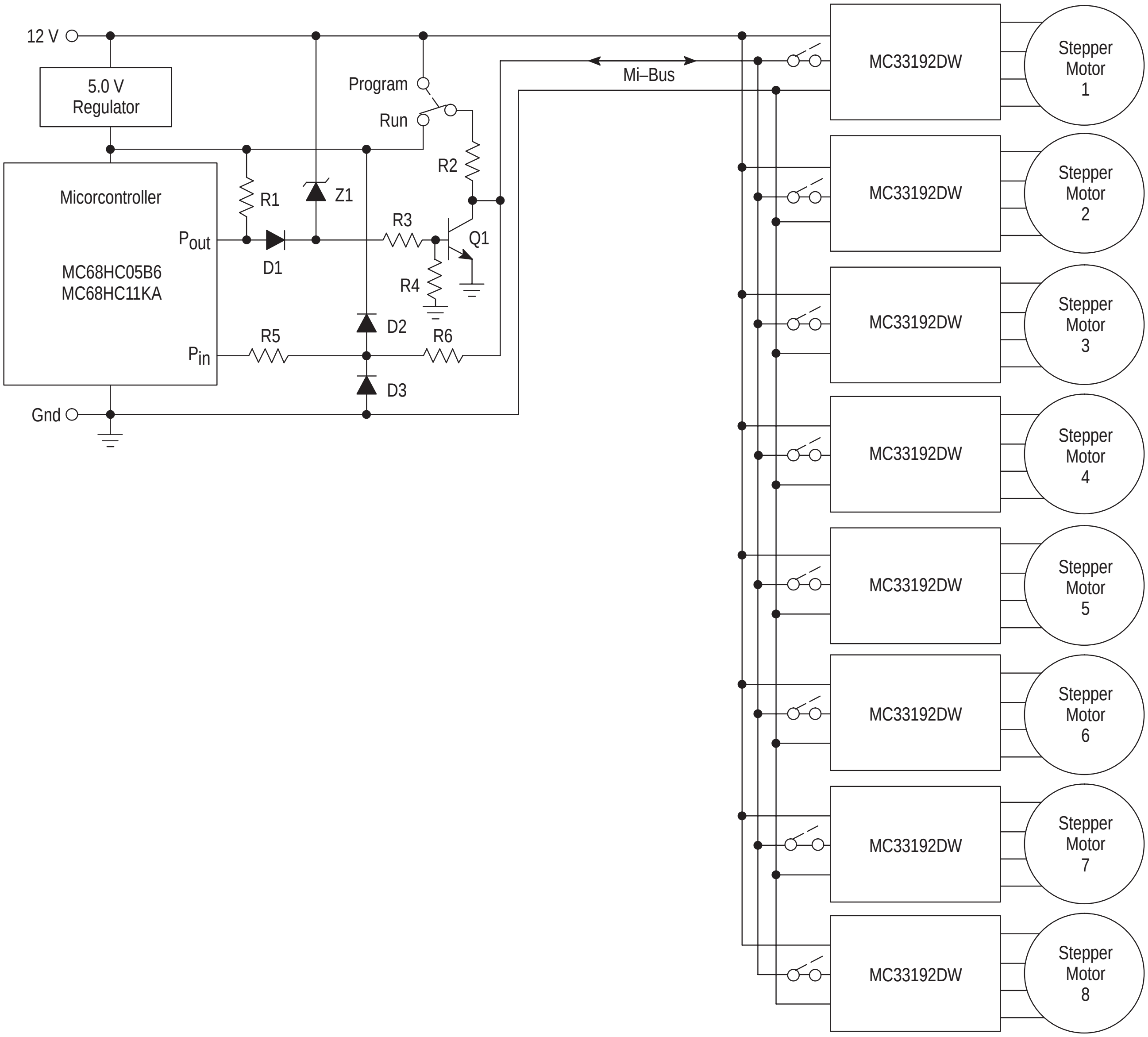


Figure 12. H–Bridge Output Drive Circuit and Diagnostic Encoder



S2	S1	S0	Status
0	0	0	Not Used
0	0	1	Free
0	1	0	No Back EMF
0	1	1	Free
1	0	0	Normal/OK
1	0	1	Thermal
1	1	0	Programming
1	1	1	Selection Failed

Figure 13. Single Wire MI–Bus Control of 8 Stepper Motors



MOTOROLA

MC33193

Advance Information

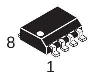
Automotive Direction Indicator

The MC33193 is a new generation industry standard UAA1041 “Flasher”. It has been developed for enhanced EMI sensitivity, system reliability, and improved wiring simplification. The MC33193 is pin compatible with the UAA1041 and UAA1041B in the standard application configuration as shown in Figure 9, without lamp short circuit detection and using a 20 mΩ shunt resistor. The MC33193 has a standby mode of operation requiring very low standby supply current and can be directly connected to the vehicle’s battery. It includes an RF filter on the Fault detection pin (Pin 7) for EMI purposes. Fault detection thresholds are reduced relative to those of the UAA1041, allowing a lower shunt resistance value (20 mΩ) to be used.

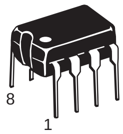
- Pin Compatible with the UAA1041
- Defective Lamp Detection Threshold
- RF Filter for EMI Purposes
- Load Dump Protection
- Double Battery Capability for Jump Start Protection
- Internal Free Wheeling Diode Protection
- Low Standby Current Mode

AUTOMOTIVE DIRECTION INDICATOR

SEMICONDUCTOR TECHNICAL DATA

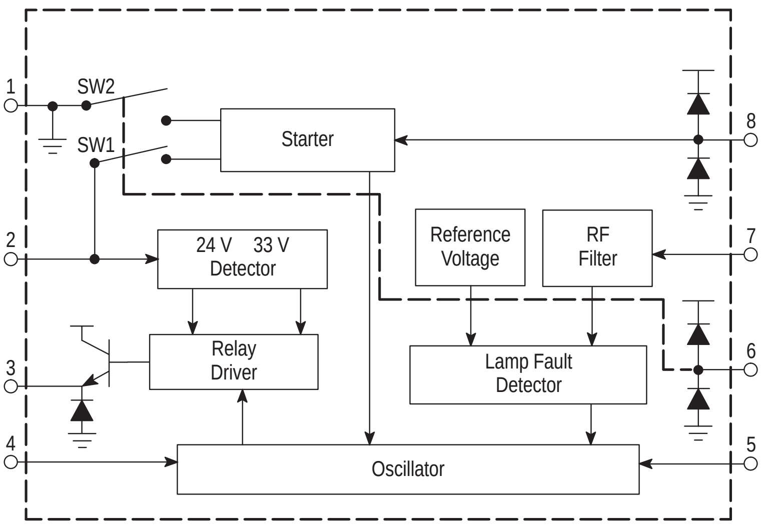


D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)



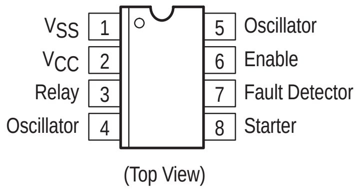
P SUFFIX
PLASTIC PACKAGE
CASE 626

Simplified Block Diagram



This device contains 60 active transistors.

PIN CONNECTIONS



ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC33193D	T_A = –40° to +125°C	SO–8
MC33193P		DIP–8

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Pin 1 Positive Current (Continuous/Pulse)	I1+	150 to 500	mA
Pin 1 Negative Current (Continuous/Pulse)	I1–	–35 to –500	mA
Pin 2 Current (Continuous/Pulse)	I2	±350 to ±1900	mA
Pin 3 Current (Continuous/Pulse)	I3	±300 to ±1400	mA
Pin 8 Current (Continuous/Pulse)	I8	±25 to ±50	mA
ESD (All Pins Except Pin 4 for Negative Pulse)	V_{ESD}	±2000	V
ESD (Pin 4 Negative Pulse)	$V_{ESD4–}$	–1000	V
Junction Temperature	T_J	150	°C
Operation Ambient Temperature Range	T_A	–40 to +125	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

ELECTRICAL CHARACTERISTICS ($–40°C \le T_A \le +125°C$, $8.0 V \le V_{CC} \le 18 V$, unless otherwise noted. Typical values reflect approximate mean at T_A = 25°C, V_{CC} = 14 V at the time of initial device characterization.)

Characteristic	Symbol	Min	Typ	Max	Unit
Battery Voltage Range (Normal Operation)	V_b	8.0	–	18	V
Overvoltage Detector Threshold ($V_{Pin2} – V_{Pin1}$)	V_{ih}	19	20.2	22	V
Clamping Voltage (R2 = 220 Ω)	V_{cl}	27	29.2	34	V
Output Voltage [I = –250 mA ($V_{Pin2} – V_{Pin3}$)]	V_{sat}	–	–	1.5	V
Starter Resistance (R_{st} = R2 + R_{Lamp})	R_{st}	–	3.3	3.6	kΩ
Oscillator Constant (Normal Operation, T_A = 25°C)	K_n	1.3	1.5	1.75	X
Temperature Coefficient of K_n	TC_{Kn}	–	0.001	–	1/°C
Duty Cycle (Normal Operation)	–	45	50	55	%
Oscillator Constant (One 21 W Lamp Defect, T_A = 25°C)	K_f	0.63	0.68	0.73	X
Duty Cycle (One 21 W Lamp Defect)	–	35	40	45	%
Oscillator Constant (T_A = 25°C)	K1 K2	0.167 0.250	0.180 0.270	0.193 0.290	–
Standby Current (Ignition "Off")	I_{CC}	–	2.0	100	µA
Current Consumption (Relay "Off," Enable Pin 6 High)	I_{CC}				mA
V_{bat} = 8.0 V, R3 = 220 Ω, T_A = 25°C		–	1.40	–	
V_{bat} = 13.5 V, R3 = 220 Ω		–	2.16	3.5	
V_{bat} = 18 V, R3 = 220 Ω, T_A = 25°C		–	2.64	–	
Current Consumption (Relay "On")	I_{CC}				mA
V_{bat} = 8.0 V, R3 = 220 Ω, T_A = 25°C		–	1.62	–	
V_{bat} = 13.5 V, R3 = 220 Ω		–	2.06	6.0	
V_{bat} = 18 V, R3 = 220 Ω, T_A = 25°C		–	3.30	–	
Defect Lamp Detector Threshold [R3 = 220 Ω, ($V_{Pin2} – V_{Pin7}$)]	V_S				mV
V_{bat} = 8.0 V, T_A = 25°C		–	43.6	–	
V_{bat} = 13.5 V		46.5	51.0	56	
V_{bat} = 18 V, T_A = 25°C		–	57.0	–	
Temperature Coefficient of V_S	TC_{VS}	–	$0.3 \times 10^{–3}$	–	1/°C

Figure 1. Normal Operation Oscillator Timing Diagram

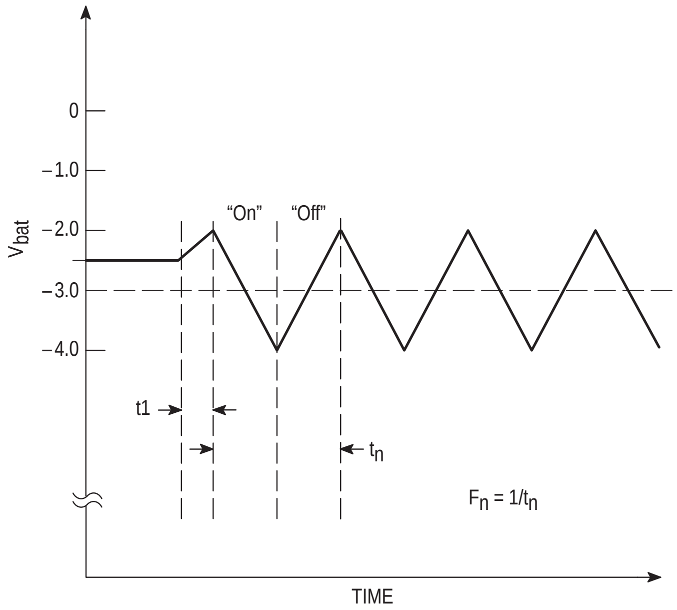
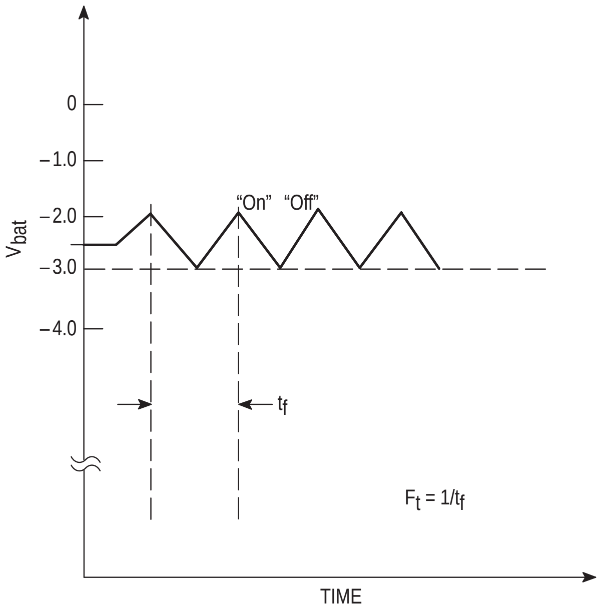


Figure 2. One Defective Lamp Oscillator Timing Diagram



INTRODUCTION

The MC33193 is designed to drive the direction indicator flasher relay. It is a new generation industry standard UAA1041 "Flasher". It consists of the following functions:

- Supply and Protections
- On–Chip Relay Driver
- Oscillator
- Starter Functions
- Lamp Fault Detector with Internal RF Filter
- Standby Mode

Supply and Protection Systems

Pin 1 is connected to ground via resistor R3 which limits the current in the event of any high voltage transients. Pin 2 (V_{CC}) is the positive supply and may be connected directly to the vehicle's battery voltage.

Overvoltage and Double Battery Protection: When the applied V_{CC} to V_{SS} voltage is greater than 22 V, the overvoltage detector circuit turns the relay driver off. Both the device and the lamps are protected if two 12 V batteries are connected in series and used to jump start the vehicle.

Load Dump Overvoltage Protection: A 29 V overvoltage detector protects the circuits against high voltage transients due to load dumps and other low energy spikes. The relay driver is automatically turned on whenever the V_{CC} to V_{SS} voltage is greater than 34 V.

Overvoltage Protection, High Voltage Transients: The Enable and the Starter pins are protected against positive and negative transients by internal on–chip diodes.

On–Chip Relay Driver

The device directly drives the flasher relay. The output structure is an Emitter of an NPN transistor. It contains the free wheeling diode circuitry necessary to protect the device whenever the relay is switched off.

Oscillator

The device uses a sawtooth oscillator (Figure 1).

The frequency is determined by the external components C1 and R1. In the normal operating mode, the flashing frequency is: $F_n = 1/R1*C1*K_n$. With a defective (open) 21 W lamp (Figure 2), the flashing frequency changes to: $F_n = 2.2*F_n$.

The typical first flash delay (the time between the moment when the indicator switch is closed and the first lamp flash occurs) is: t1 = K1*R1*C1

The fault detection delay is from the time relay R1 is on and fault detection is enabled. Where a 21 W lamp opens, the delay is expressed as: t2 = K2*R1*C1

Starter

Pin 8 is connected through a 3.3 kΩ resistor to the flashing lamp. Pin 8 is the input to the Starter function and senses the use of S1 by sensing ground through the lamp (Figures 9 and 10).

Lamp Fault Detector with Internal RF Filter

A Lamp defect is sensed by the lamp fault detector's monitoring of the voltage developed across the external shunt resistor R_S via the RF filter. The R_S voltage drop is compared to a V_{bat} dependent internal reference voltage (V_{ref}) to validate the comparison over the full battery voltage range. A detected fault causes the oscillator to change frequency (Figure 2).

Standby Mode

When the ignition key and warning switches are open; Enable is in a low state and the internal switches, SW1 and SW2, are open and no current passes through the circuit. In this condition, the device's current consumption is zero (I_{CC} = 0). When ignition key and warning switches are closed; Enable is in a high state with SW1 and SW2 being closed and the circuit is powered on.

MAIN DIFFERENCES BETWEEN UAA1041B & MC33193

The MC33193 is pin compatible with the UAA1041.

Supply Current

Supply current is more stable on the MC33193 when the device is in “on” or “off” state. In “on” state the supply current is only 40% higher than when in the “off” state, as compared to a ratio of 3 times for the UAA1041. This results in a lower voltage drop across the ground resistor R3 (see On–Chip Relay Driver).

Short Circuit Detection

The MC33193 has no short circuit detection.

Standby Mode (Pin 6)

The UAA1041 has no standby mode. Pin 6 is used as an Enable/Disable for the short circuit detection.

The MC33193 uses Pin 6 to set the device in standby mode. If Pin 6 is connected to ground, the MC33193 is in the standby mode. In this mode, standby current is very low and Pin 8’s starter resistor R2 and a 2.0 kΩ internal resistor are switched off. As soon as Pin 6 is at a high level (typical threshold = $2V_{be}$) the device becomes active. In the application, the MC33193 can be connected directly to the battery and awakened whenever Pin 6 is connected to the vehicle’s battery by way of a protection resistor and the ignition key switch.

Lamp Defect Detection (Pin 7)

The UAA1041 operates with a 30 mΩ shunt resistor to sense the lamp current. It’s lamp defect detection threshold of Pin 7 is typically 85 mV.

The MC33193 is designed to operate with 20 mΩ shunt resistor and at a reduced threshold of 50 mV. This reduces power generation in the flasher module. In addition, the MC33193 incorporates an RF filter to enhance RFI immunity.

Load Dump and Overvoltage Behavior

The UAA1041 and MC33193 both behave the same in this regard. Both have double battery detection and lamp turn–off protection in the event of a jump start. During load dump, both devices are protected by an internal 30 V zener diode with the relay activated during a load dump.

Relay Driver

Drive capability of both devices is the same. Free wheeling diode protection is internal to both devices. The free wheeling voltage is $2V_{be}$ for the UAA1041 and $3V_{be}$ for the MC33193. This results in a higher clamp voltage across the relay and thus in a faster turn–off. In addition, the lower “on” state supply current is lower on the MC33193 and thus the voltage drop across the ground resistor R3 is reduced. This results in an even higher clamp voltage across the relay.

Oscillator Phase

The oscillator phase is opposite on the MC33193 as compared to the UAA1041. The Oscillator voltage is falling during “on” state and rising during “off” state for the MC33193.

Figure 3. Clamping Voltage versus Temperature

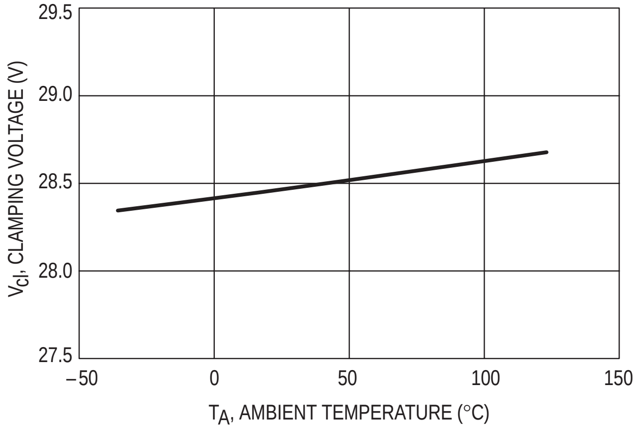


Figure 4. Overvoltage Detection versus Temperature

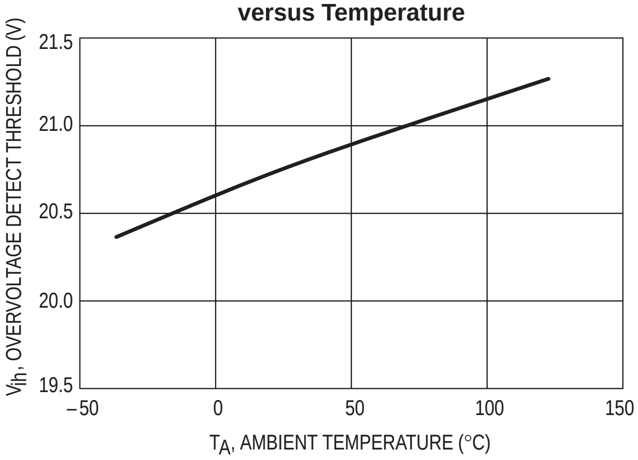


Figure 5. Supply Current versus Temperature

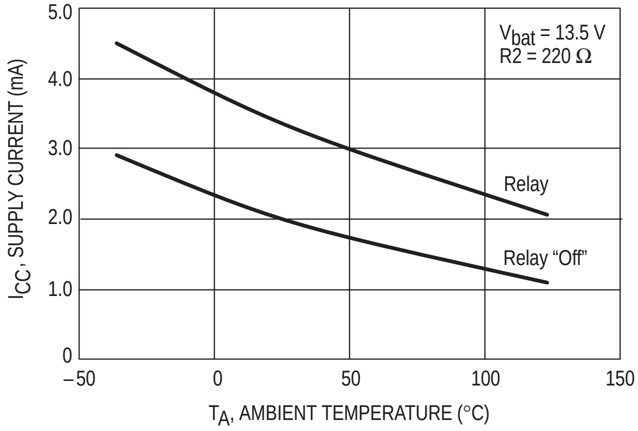


Figure 6. Output Voltage versus Temperature

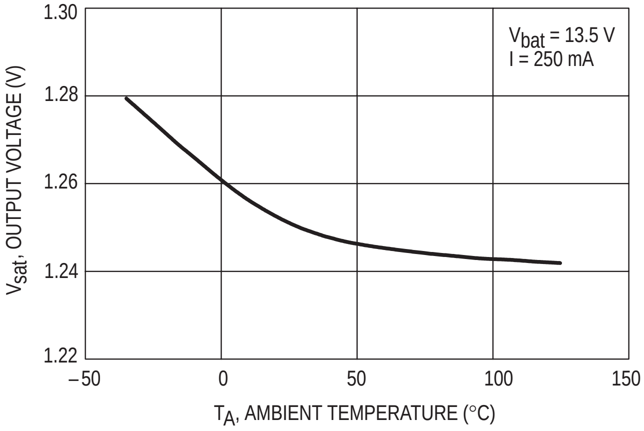


Figure 7. Defect Lamp Detection versus Temperature

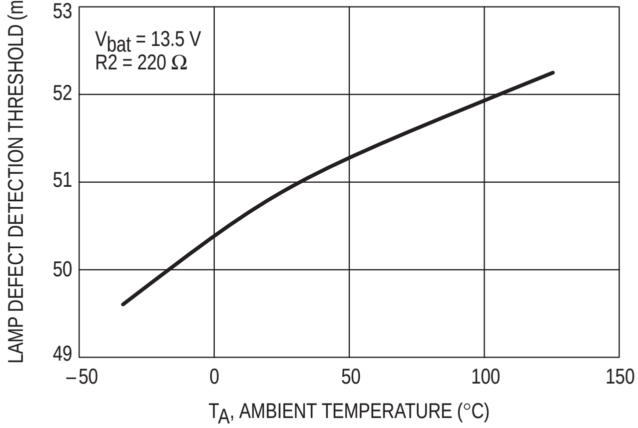


Figure 8. Oscillator Constant versus Temperature

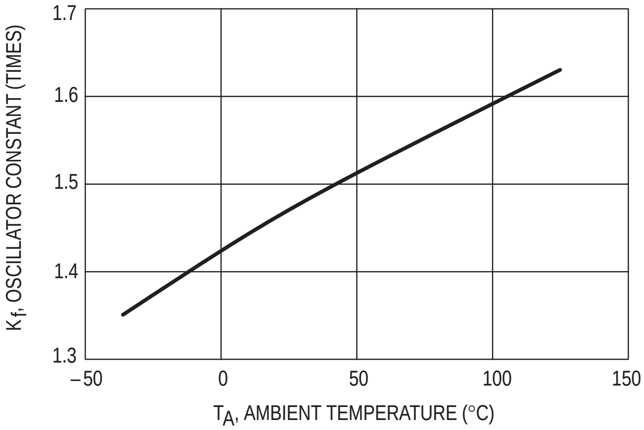
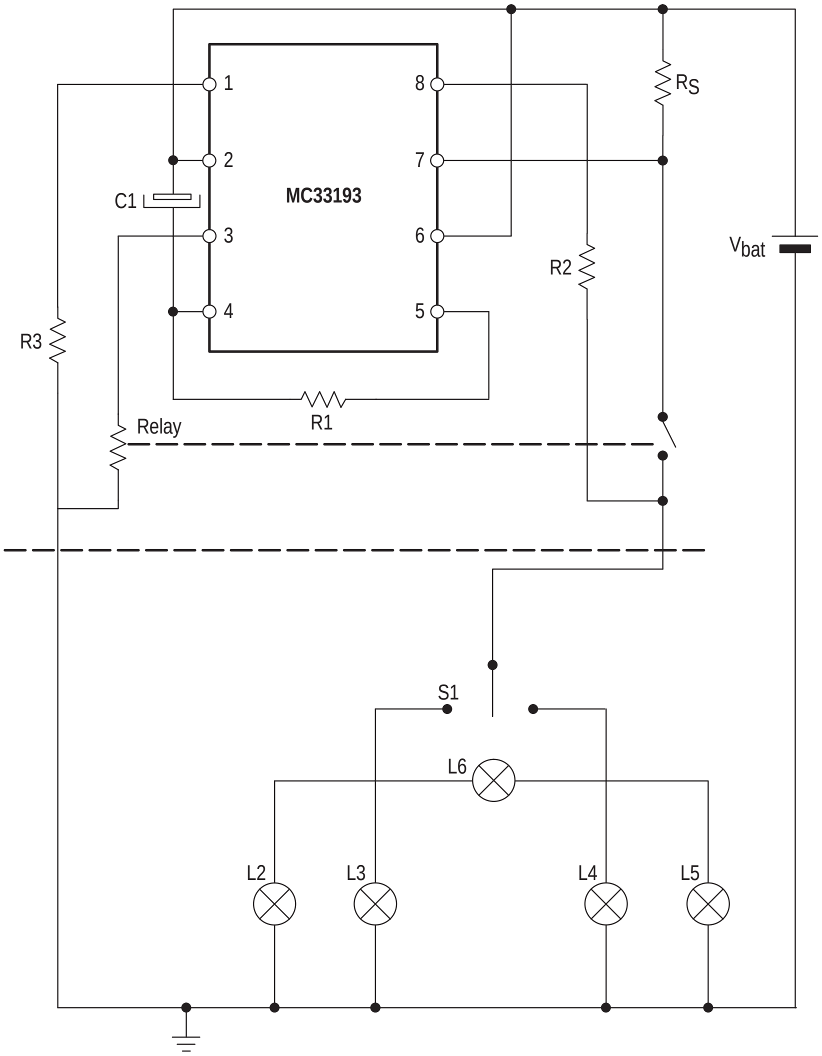


Figure 9. MC33193 Typical Application

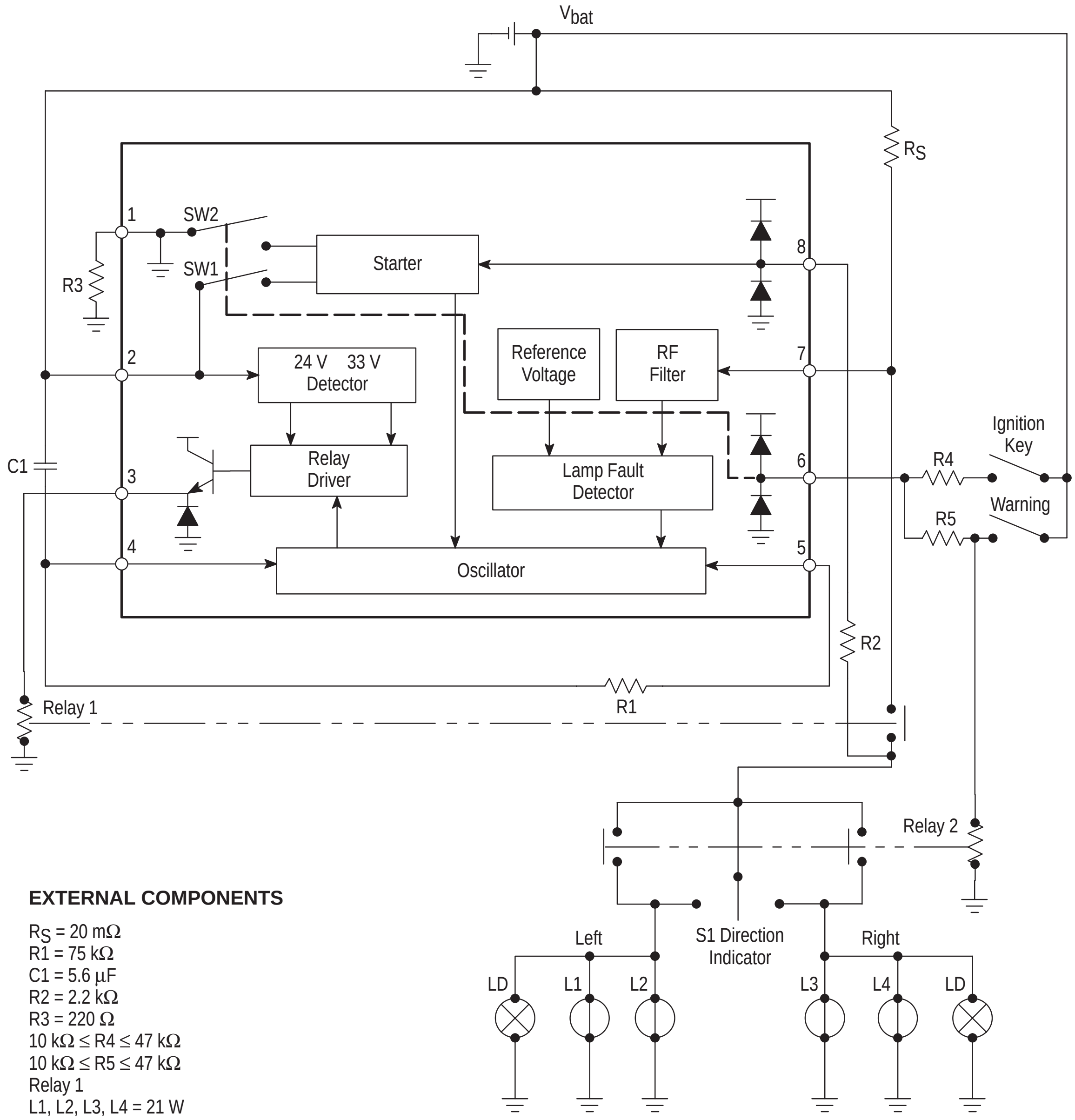


R_S = 20 mΩ
R1 = 75 kΩ
C1 = 5.6 µF
R2 = 3.3 kΩ
R3 = 200 Ω
L2, L3, L4, L5 = 21 W Turn Signal Lamps

Application Information

NOTES:
1. In the above application, the MC33193 is compatible with the UAA1041 and UAA1041B except for the shunt resistor value (R_S = 20 mΩ).
2. The flashing cycle is started by the closing of switch S1.
3. The position of switch S1 is sensed across resistor R2 and R_{Lamp} by the input, Pin 8.

Figure 10. Typical MC33193 Application



EXTERNAL COMPONENTS

R_S = 20 mΩ
R1 = 75 kΩ
C1 = 5.6 µF
R2 = 2.2 kΩ
R3 = 220 Ω
10 kΩ ≤ R4 ≤ 47 kΩ
10 kΩ ≤ R5 ≤ 47 kΩ
Relay 1
L1, L2, L3, L4 = 21 W
L_D = Dashboard Indicator

Application Information

NOTES: 1. The flashing cycle is started by the closing of switch S1.
2. The S1 switch position is sensed across the resistor R2 and R_{Lamp} by the input (Pin 8).
3. If the logic state at Pin 6 is [0], the current through R2 is off.

MOTOROLA

MC33197A

Advance Information

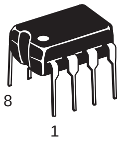
Automotive Wash Wiper Timer

The MC33197A is a standard wiper timer control device designed for harsh automotive applications. The device can perform the intermittent, after wash, and continuous wiper timer functions. It is designed to directly drive a wiper motor relay. The MC33197A requires very few external components for full system implementation. The intermittent control pin can be switched to ground or V_{bat} to meet a large variety of possible applications. The intermittent timing can be fixed or adjustable via an external resistor. The MC33197A is built using bipolar technology and parametrically specified over the automotive ambient temperature range and 8.0 to 16 V supply voltage. The MC33197A can operate in both front and rear wiper applications.

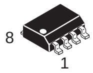
- Adjustable Time Interval of Less Than 500 ms to More Than 30 s
- Intermittent Control Pin Can Be Switched to Ground or V_{bat}
- Adjustable After Wipe Time
- Priority to Continuous Wipe
- Minimum Number of Timing Components
- Integrated Relay Driver With Free Wheeling Protection Diode
- Operating Voltage Range From 8.0 to 16 V
- For Front Wiper and Rear Wiper Window Applications

AUTOMOTIVE WASH WIPER TIMER

SEMICONDUCTOR TECHNICAL DATA



P SUFFIX
PLASTIC PACKAGE
CASE 626



D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

ORDERING INFORMATION

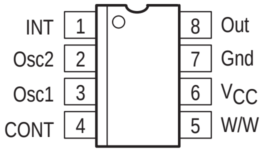
Device	Operating Temperature Range	Package
MC33197AD	T_A = – 40° to +105°C	SO–8
MC33197AP	T_A = – 40° to +125°C	DIP–8

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Continuous Supply Voltage ($V_{Pin\ 6}$)	V_{CC}	16	V
Storage Temperature	T_{stg}	–55 to +150	°C
Thermal Resistance (Junction–to–Ambient) DIP–8 Package SO–8 Package	$R_{\theta JA}$	 100 145	°C/W
Operating Ambient Temperature Range DIP–8 Package SO–8 Package	T_A	 –40 to +125 –40 to +105	°C
Operating Junction Temperature Range	T_J	–40 to +150	°C
Maximum Junction Temperature	$T_{J(max)}$	150	°C

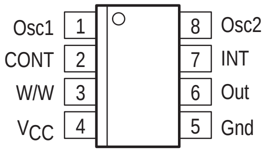
NOTE: ESD data available upon request.

PIN CONNECTIONS



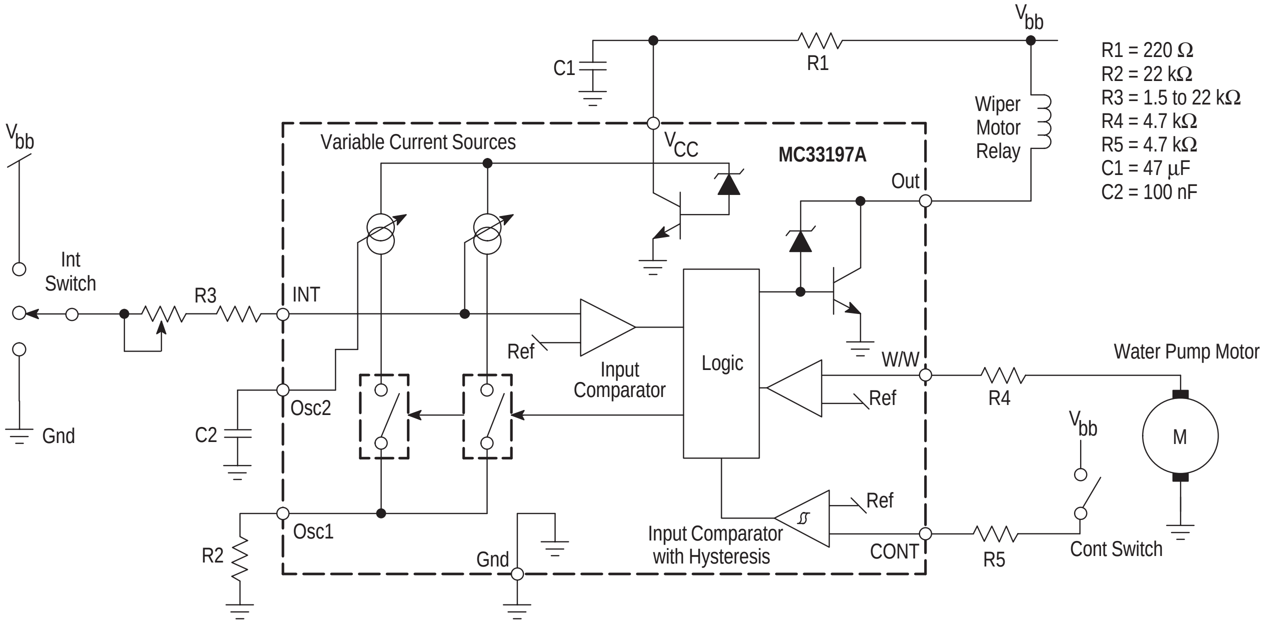
(Top View)

(SO–8)



(Top View)

Representative Block Diagram



This device contains 390 active transistors.

ELECTRICAL CHARACTERISTICS (–40°C ≤ T_A ≤ +125°C, 8.0 V ≤ V_{CC} ≤ 16 V, unless otherwise noted. Typical values reflect approximate mean at T_A = 25°C with V_{CC} = 14 V at the time of initial device characterization.)

Characteristic	Symbol	Min	Typ	Max	Unit
Functional Supply Voltage Range	V_{CCF}	8.0	–	18	V
Operating Supply Voltage Range	V_{CCOP}	8.0	–	16	V
Standby Supply Current (V_{CC} = 16 V, R2 = 68 k)	I_{CC}	–	4.0	5.2	mA
Supply Current INT Active (R3 = 2.5 k)	I_{CC}	–	7.0	8.4	mA
Supply Current Relay "On" (R2 = 68 k)	I_{CC}	–	7.5	11.2	mA
Supply Current INT and Relay "On" (R2 = 68 k, R3 = 2.5 k)	I_{CC}	–	10	14.5	mA
Oscillator Variations with Supply Voltage and Temperature (excluding external component tolerances, C2 = 100 nF polyester capacitor) (Notes 1 & 2) 10 V ≤ V_{bb} ≤ 16 V 8.0 V ≤ V_{bb} ≤ 16 V	K_{osc}	 – –	 10 15	 – –	%
Relay Resistance	R_L	60	–	–	Ω
Output Voltage (I_{out} = 200 mA)	V_{out}	–	0.9	1.5	V
Output Clamp Voltage (I_{out} = 20 mA)	V_{cl}	19.5	–	22	V
Oscillator Period Coefficient (T_A = 25°C) V_{bb} = 13 V (Note 3) V_{bb} = 13 V (INT Connected to Gnd) (Note 4) V_{bb} = 13 V (INT Connected to V_{bat}, R1 = 220 Ω) (Note 4)	 t_{b1} t_{b2g} t_{b2v}	 0.98 15.1 11.5	 1.0 15.5 12.1	 1.03 15.9 12.7	–
CONT Threshold (V_{CC} = 13 V)	V_{ih}	6.0	–	8.5	V
CONT Threshold (V_{CC} = 16 V)	V_{ih}	–	$V_{CC}/2$	–	V

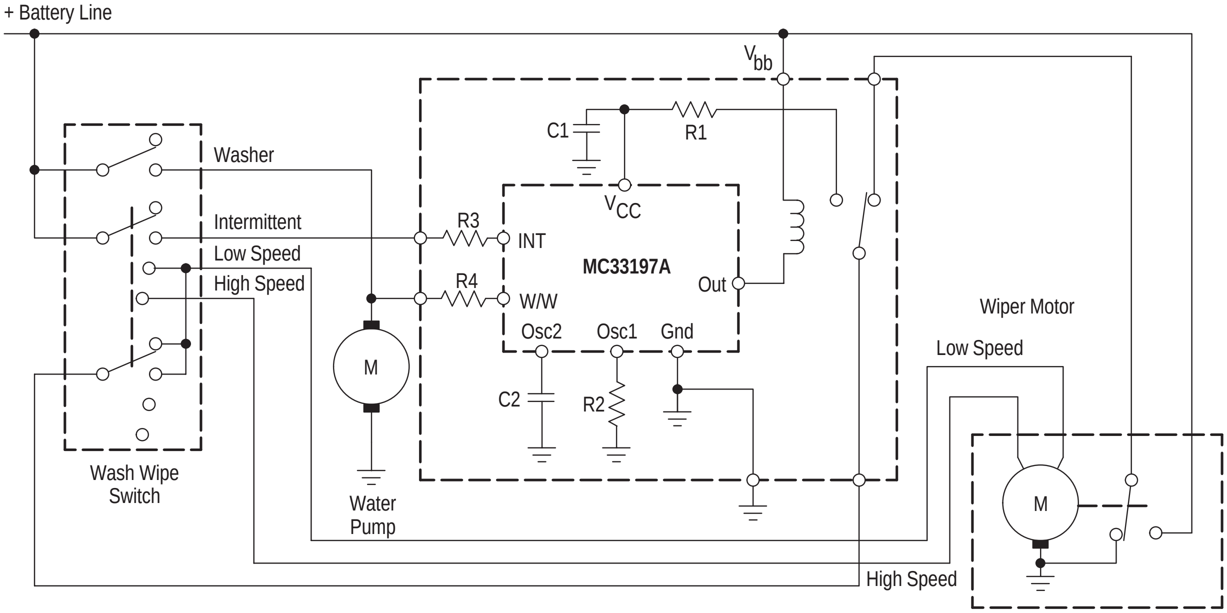
NOTES: 1. The oscillator frequency is defined by the current flowing through the external resistor R2. The voltage at the INT pin is ($V_{CC}/2 – V_{be}$) and hence the current flowing through R3 is different if R3 is connected to V_{bb} or to Gnd because of the voltage drop across resistor R1. This voltage drop causes the oscillator coefficient for t_{b2} to be different for the two cases of INT terminated to Gnd or to V_{bb}. Because of this, the oscillator coefficient is specified with a specific value of R1 whenever INT is connected to V_{bb}. If R1 is changed, the coefficient will change. Also, any extra current through the resistor R1 other than the current used by the device will cause timing deviations in t_{b2} timings (as in the case where two devices are sharing a common R1 resistor).

2. The oscillator stability with temperature is dependent on the temperature coefficients of the external components. If the capacitance value of the external capacitor varies more than 5% over the parametric temperature range, the figures quoted for oscillator variation are not valid.

3. The t_{b1} duration is given by coefficient 4 x R2 x C2 (t_{b1} duration = t_{b1} x 4 x R2 x C2).

4. The t_{b2} duration is given by coefficient x R3 x C2 (t_{b2} duration = t_{b2} x R3 x C2).

Figure 1. Intermittent Wash Wiper Typical Application



This application shows the MC33197A with the external wirings and two speed wiper motor. This application has the Intermittent and Wash Wiper functions.

INTRODUCTION

The MC33197A is a wiper timer control device designed for use in harsh automotive applications. The device can perform the intermittent, after wash, and continuous wiper timer functions.

The MC33197A is designed to directly drive a wiper motor relay. The MC33197A is suitable for both front and rear wiper applications. The MC33197A connects directly to the vehicle's battery voltage (V_{bat}) through a 220 Ω resistor used with a 47 µF de–coupling filter capacitor. The device has an internal oscillator controlled by one of two external resistors (R2 and R3) in addition to one external capacitor (C2), dependent on the application function required. The values of C2 and R2 determine the t_{b1} time base. T_{b1} is used to generate the relay wiper activation during the INT function (T3) and the after wash timing (T2) during the wash wipe mode. The values C2 and R3 determine the t_{b2} time base. The t_{b2} time base is used to generate the pause or intermittent time (T4).

The intermittent wiper function can generate intermittent timing (T4) from less than 500 ms to more than 30 seconds. The intermittent function of the device can be activated by the INT input connected to either ground or V_{bat}. The intermittent timing is externally adjustable by changing the value of resistor R3.

The wash wiper timer function detects the water pump motor's operation. When the pump motor activation is detected, the MC33197A turns the wiper on for the entire duration of the pump motor's activation. When the motor is turned off, it generates an after wash timing (T2) to maintain the wiping action. The W/W pin is connected to the water pump motor through a protection resistor (R4).

The MC33197A also has a continuous function, which activates the wiper relay whenever the CONT input is activated. The CONT input is connected to a switch through a protection resistor (R5). The CONT input comparator has an input threshold of $V_{bb}/2$ with hysteresis.

The device has internal debounce circuitry, based on the oscillator period. This provides filtering of the intermittent (INT) and wash wipe (W/W) input signals (see T1 Debounce Timing paragraph that follows). The device directly drives the wiper motor relay. It internally incorporates a 20 V free wheeling zener diode to protect the device against overvoltage spikes produced when relay is switched off.

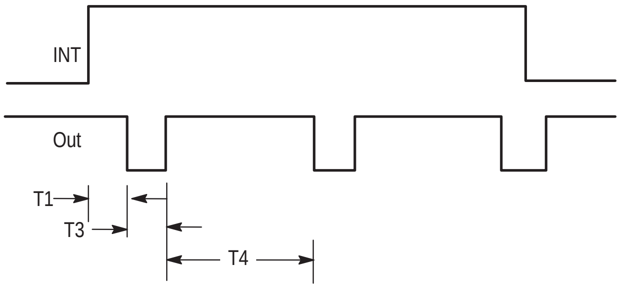
Intermittent Operation

Conditions:

- W/W not connected or connected to ground.
- CONT not connected or connected to ground.
- INT connected to V_{bb} or to ground.

In this configuration, the circuit will respond to the switching of INT to either V_{bb} or ground after a time T1 (see T1 Debounce Timing). If INT is disconnected before the end of T1; no action will be taken. After a time T1, the output will be switched on for a duration, T3 = 16 x 4 x t_{b1} and then switched off for a duration, T4 = 144 x 4 x t_{b2}. This sequence will continue to repeat so long as INT is disconnected from V_{bb} or ground for a time duration greater than T1. If INT is disconnected during the time T3; the output will remain on for the remainder of T3. This is illustrated in the diagram on Figure 2.

Figure 2. Switching Waveform INT Timing



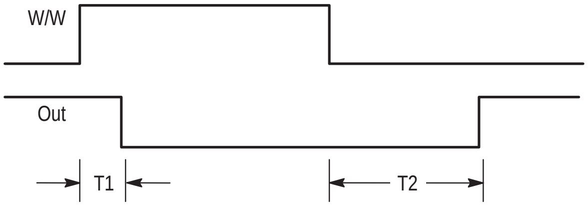
Wash Wipe Operation

Conditions:

- INT disconnected.
- CONT disconnected or connected to ground.

In this condition, the circuit will respond to the switching of W/W to V_{bb} after a time T1 (see T1 Debounce Timing). If W/W is disconnected or connected to ground before the end of T1; no action will be taken. After a time T1; the circuit will perform as shown on Figure 3. The output will turn on and remain on for the duration of W/W. When W/W becomes inactive, the output will remain on for T2 = 96 x 4 x t_{b1}.

Figure 3. Switching Waveform W/W Timing



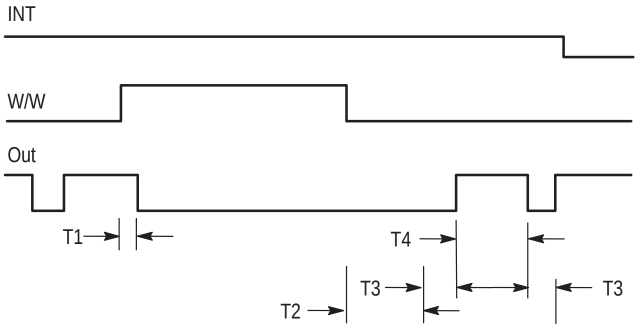
Continuous Operation

In this condition, the circuit responds to the switching of CONT to V_{bb}. If CONT is connected to V_{bb}, the output will turn on regardless of the state of any other input and remain on so long as CONT is active. This command operates directly on the relay output and does not interfere with any other timing. Therefore, the circuit will not be reset to a defined state.

Wash Wiper and Intermittent Operation

If W/W is activated during the time INT is also activated, the circuit will respond to W/W after a time T1 (see T1 Debounce Timing). The output will turn on after T1, and stay on for a time T2 + T3 after W/W is deactivated. Following this, normal operation of INT will occur. This is shown on Figure 4.

Figure 4. Switching Waveform W/W and INT Active



T1 Debounce Timing

The criteria for an input signal to be detected is that it should be active at two successive negative internal clock edges. The inputs are sampled on the negative edge of the internal clock. If two consecutive samples are the same, the input is detected as being in that state. Hence the time T1 from a signal becoming active to the time that the circuit responds can be anytime from 4 x t_{b1} to 2 x 4 x t_{b1} (due to synchronizing the input to the oscillator period) when the oscillator is oscillating with a time base of t_{b1} and 4 x t_{b2} to 2 x 4 x t_{b2}, when the oscillator is oscillating with a time base of t_{b2}.

The following table summarizes all T1 debounce timings:

Condition	Debounce Time
INT Active	4 x t_{b1} to 2 x 4 x t_{b1}
INT Inactive	4 x t_{b1} to 2 x 4 x t_{b1}
W/W Active When INT Inactive	4 x t_{b1} to 2 x 4 x t_{b1}
W/W Active When INT Active During T3	4 x t_{b1} to 2 x 4 x t_{b1}
W/W Active When INT Active During T4	4 x t_{b2} to 2 x 4 x t_{b2}

Two MC33197A Devices Using One Decoupling Resistor and Capacitor

Two devices may be connected to the power source using a common R1 resistor for protection against overvoltages. If this is done it should be noted that the current flowing through R1 is increased and hence the voltage drop across R1 is increased.

Overvoltage Protection

In reference to the Block Diagram and Typical Application, all of the foregoing operational cases require:

R1 ≥ 100 Ω, C1 ≥ 47 µF

R3 ≥ 1.0 kΩ, R4 ≥ 4.7 kΩ, R5 ≥ 4.7 kΩ

The circuit will not operate during the transient conditions. By using the above component values, the circuit will be able to sustain the following overvoltages on V_{bb} without permanent damage:

1. +28 V for 5 minutes
2. –15 V for 5 minutes
3. –16 V cycled off for 1.0 minute
4. +80 V pulse decaying exponentially to 8.0 V in 400 ms repeated 3 times at 1.0 minute intervals.
5. ± 300 V pulse decaying exponentially to 30 V in 300 ms with a maximum energy of 1.0 Joule.
6. ±100 V pulse decaying exponentially to 10 V in 2 ms.

Recommended External Component Values

Below are the recommended component values to ensure the device will operate properly, and that all specified parameters will stay within their tolerances.

R1 should be greater than 100 Ω; recommended value of 220 Ω. R1 can be up to 500 Ω, but in this case the t_{b2v} parameter could be out of it's specified value (see Electrical Characteristics and Note 1). Also, the minimum operating voltage range should be greater than 8.0 V. The following values should be adhered to:

10 kΩ ≤ R2 ≤ 68 kΩ

1.5 kΩ ≤ R3 ≤ 47 kΩ

R4 ≥ 4.7 kΩ

R5 ≥ 4.7 kΩ

C1 ≥ 47 uF

47 nF ≤ C2 ≤ 470 nF

Application Information

The following is an example of timing calculations using the following external components values:

R2 = 22 kΩ, R3 = 2.2 kΩ, C2 = 100 nF (Referring to Block Diagram and Typical Application).

Oscillator Time Base Calculation:

t_{b1} duration = t_{b1} x 4 x R2 x C2 = 1 x 4 x 27e3 x 100e–9 = 10.8 ms

t_{b2} duration_g (INT to Gnd) = t_{b2g} x R3 x C2 = 15.5 x 2.2e3 x 100e–9 = 3.41 ms

t_{b2} duration_v (INT to V_{bb}) = t_{b2v} x R3 x C2 = 12.1 x 2.2e3 x 100e–9 = 2.66 ms

Intermittent timing calculation:

T3 = 16 x 4 x t_{b1} duration = 16 x 4 x 10.8 ms = 691 ms

T4 = 144 x 4 x t_{b2} duration_g = 144 x 4 x 3.41 ms = 1.96 s (INT connected to Gnd)

T4 = 144 x 4 x t_{b2} duration_v = 144 x 4 x 2.66 ms = 1.53 s (INT connected to V_{bb})

Wash wipe timing calculation:

T2 = 96 x 4 x t_{b1} = 96 x 4 x 10.8 ms = 4.15 s

T1 Debounce Time Calculation (see T1 Debounce Timing)

When oscillator is oscillating at t_{b1}:

T1 minimum = 4 x t_{b1} = 4 x 10.8 ms = 43.2 ms

T1 maximum = 2 x 4 x t_{b1} = 2 x 4 x 10.8 ms = 86.4 ms

When oscillator is oscillating at t_{b2}:

T1 minimum (INT connected to Gnd, t_{b2g}) = 4 x t_{b2} = 4 x 3.41 ms = 13.6 ms

T1 maximum (INT connected to Gnd, t_{b2g}) = 2 x 4 x t_{b2} = 2 x 4 x 3.41 ms = 27.3 ms

MOTOROLA

MC33199

Automotive ISO 9141 Serial Link Driver

ISO 9141
SERIAL LINK DRIVER

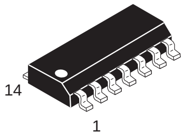
SEMICONDUCTOR
TECHNICAL DATA

The MC33199D is a serial interface circuit used in diagnostic applications. It is the interface between the microcontroller and the special K and L Lines of the ISO diagnostic port. The MC33199D has been designed to meet the “Diagnosis System ISO 9141” specification.

The device has a bi–directional bus K Line driver, fully protected against short circuits and over temperature. It also includes the L Line receiver, used during the wake up sequence in the ISO transmission.

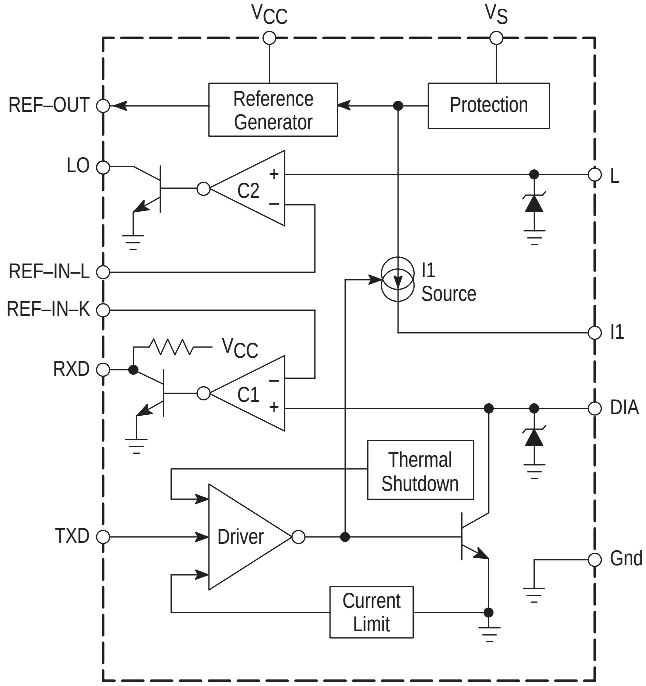
The MC33199 has a unique feature which allows transmission baud rate up to 200 k baud.

- Electrically Compatible with Specification “Diagnosis System ISO 9141”
- Transmission Speed Up to 200 k Baud
- Internal Voltage Reference Generator for Line Comparator Thresholds
- TXD, RXD and LO Pins are 5.0 V CMOS Compatible
- High Current Capability of DIA Pin (K Line)
- Short Circuit Protection for the K Line Input
- Over Temperature Shutdown with Hysteresis
- Large Operating Range of Driver Supply Voltage
- Full Operating Temperature Range
- ESD Protected Pins



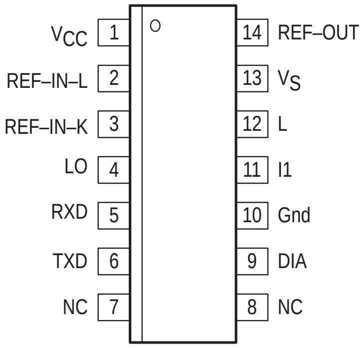
D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO–14)

Simplified Application



This device contains 94 active transistors.

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC33199D	T_A = – 40° to +125°C	SO–14

MAXIMUM RATINGS (Note 1)

Rating	Symbol	Value	Unit
V_S Supply Pin DC Voltage Range Transient Pulse (Note 2)	 V_S V_{pulse}	 –0.5 to +40 –2.0 to +40	V
V_{CC} Supply DC Voltage Range	V_{CC}	–0.3 to +6.0	V
DIA and L Pins (Note 2) DC Voltage Range Transient Pulse (Clamped by Internal Diode) DC Source Current DIA Low Level Sink Current	–	 –0.5 to +40 –2.0 –50 Int. Limit	 V V mA mA
TXD DC Voltage Range	–	–0.3 to V_{CC} + 0.3	V
REF–IN DC Voltage Range $V_S < V_{CC}$ $V_S > V_{CC}$	–	 –0.3 to V_{CC} –0.3 to V_S	V
ESD Voltage Capability (Note 3)	$V_{(ESD)}$	±2000	V

NOTES: 1. The device is compatible with Specification: “Diagnosis System ISO 9141”.
2. See the test circuit (Figure 23). Transient test pulse according to ISO 76371 and DIN 40839; highest test levels.
3. Human Body Model; C = 100 pF, R = 1500 Ω.

THERMAL RATINGS

Rating	Symbol	Value	Unit
Storage Temperature	T_{stg}	–55 to +150	°C
Operating Junction Temperature	T_J	–40 to +150	°C
Thermal Resistance, Junction–to–Ambient	$R_{\theta JA}$	180	°C/W
Maximum Power Dissipation (@ T_A = 105°C)	P_D	250	mW

ELECTRICAL CHARACTERISTICS (– 40°C ≤ T_A ≤ 125°C, 4.5 V ≤ V_{CC} ≤ 5.5 V, 4.5 V ≤ V_S ≤ 20 V, unless otherwise noted. Typical values reflect approximate mean at 25°C, nominal V_{CC} and V_S, at time of device characterization.)

Characteristic	Symbol	Min	Typ	Max	Unit
V_{CC} PIN 1					
V_{CC} Supply Voltage Range	V_{CC}	4.5	–	5.5	V
V_{CC} Supply Current (Note 1)	I_{CC}	0.5	1.0	1.5	mA
REF–IN–L PIN 2 AND REF–IN–K PIN 3					
REF–IN–L and REF–IN–K Input Voltage Range For 0 < V_S < V_{CC} For V_{CC} < V_S < 40 V	V_{inref}	 2.0 2.0	 – –	 V_{CC} – 2.0 V V_S – 1.0 V	V
REF–IN–L and REF–IN–K Inputs Currents	I_{VIN}	–5.0	–	5.0	µA
LO PIN 4					
LO Open Collector Output Low Level Voltage @ I_{out} = 1.0 mA Low Level Voltage @ I_{out} = 4.0 mA	V_{OL}	 – –	 0.34 –	 0.7 0.8	V
RXD PIN 5					
Pull–Up Resistor to V_{CC}	R_{RXD}	1.5	2.0	2.5	kΩ
Low Level Voltage @ I_{out} = 1.0 mA	V_{OL}	–	0.3	0.7	V

NOTES: 1. Measured with TXD = V_{CC}, I1 = V_S, DIA and L high, no load. REF–IN–L and REF–IN–K connected to REF–OUT.
2. 0 < V_{CC} < 5.5 V, 0 < V_S < 40 V, 0 < V_{DIA} < 20 V, TXD high or floating.
3. When an over temperature is detected, the DIA output is forced “off”.
4. 0 < V_{CC} < 5.5 V, 0 < V_S < 40 V, 0 < V_L < 20 V.
5. At static “High” or “Low” level TXD, the current source I1 delivers a current of 3.0 mA (typ). Only during “Low” to “High” transition, does this current increase to a higher value in order to charge the K Line capacitor (CL < 4.0 nF) in a short time (see Figure 3).
6. Measured with TXD = V_{CC}, I1 = V_S, DIA and L high, no load, REF–IN–L and REF–IN–K connected to REF–OUT.

ELECTRICAL CHARACTERISTICS (continued) (– 40°C ≤ T_A ≤ 125°C, 4.5 V ≤ V_{CC} ≤ 5.5 V, 4.5 V ≤ V_S ≤ 20 V, unless otherwise noted. Typical values reflect approximate mean at 25°C, nominal V_{CC} and V_S, at time of device characterization.)

Characteristic	Symbol	Min	Typ	Max	Unit
TXD PIN 6					
High Level Input Voltage	V_{IH}	0.7 V_{CC}	2.8	–	V
Low Level Input Voltage	V_{IL}	–	2.0	0.3 V_{CC}	V
Input Current @ 0 < V_S < 40 V					µA
TXD at High Level	I_H	–200	–	30	
TXD at Low Level	I_L	–600	–	–100	
DIA INPUT/OUTPUT PIN 9					
Low Level Output Voltage @ I = 30 mA	V_{OL}	0	0.35	0.8	V
Drive Current Limit	I_{Lim}	40	–	120	mA
High Level Input Threshold Voltage (REF–IN–K Connected to REF–OUT)	V_{IH}	V_{ref} min + 0.25 V	V_{ref} + 0.325 V	V_{ref} max + 0.4 V	V
Low Level Input Threshold Voltage (REF–IN–K Connected to REF–OUT)	V_{IL}	V_{ref} min – 0.2 V	V_{ref} – 0.125 V	V_{ref} max – 0.05 V	V
Input Hysteresis	V_{Hyst}	300	450	600	mV
Positive Clamp @ 5.0 mA	V_{Cl+}	37	40	44	V
Negative Clamp @ – 5.0 mA	V_{Cl-}	–1.5	–0.6	–0.3	V
Leakage Current (Note 2)	I_{Leak}	4.0	10	16	µA
Over Temperature Shutdown (Note 3)	T_{Lim}	155	–	–	°C
L INPUT PIN 12					
High Level Input Threshold Voltage (REF–IN–L Connected to REF–OUT)	V_{IH}	V_{ref} min + 0.25 V	V_{ref} + 0.325 V	V_{ref} max + 0.4 V	V
Low Level Input Threshold Voltage (REF–IN–L Connected to REF–OUT)	V_{IL}	V_{ref} min – 0.2 V	V_{ref} – 0.125 V	V_{ref} max – 0.05 V	V
Input Hysteresis	V_{Hyst}	300	450	600	mV
Leakage Current (Note 4)	I_{Leak}	4.0	10	16	µA
Positive Clamp @ 5.0 mA	V_{Cl+}	37	40	44	V
Negative Clamp @ – 5.0 mA	V_{Cl-}	–1.5	–0.6	–0.3	V
I1 PIN 11					
Static Source Current	$I1_S$	–4.0	–3.0	–2.0	mA
Static Saturation Voltage ($I1_S$ = – 2.0 mA)	$V_{I1(sat)}$	V_S – 1.2	V_S – 0.8	V_S	V
Dynamic Source Current (Note 5)	$I1_d$	–120	–80	–40	mA
Dynamic Saturation Voltage ($I_{I1(sat)}$ = – 40 mA)	$V_{I1(dsat)}$	V_S – 2.7	V_S – 0.85	V_S	V
VS PIN 13					
V_S Supply Voltage Range	V_S	4.5	–	20	V
V_S Supply Current (Note 6)	I_S	0.5	1.3	2.0	mA

NOTES: 1. Measured with TXD = V_{CC}, I1 = V_S, DIA and L high, no load. REF–IN–L and REF–IN–K connected to REF–OUT.
2. 0 < V_{CC} < 5.5 V, 0 < V_S < 40 V, 0 < V_{DIA} < 20 V, TXD high or floating.
3. When an over temperature is detected, the DIA output is forced “off”.
4. 0 < V_{CC} < 5.5 V, 0 < V_S < 40 V, 0 < V_L < 20 V.
5. At static “High” or “Low” level TXD, the current source I1 delivers a current of 3.0 mA (typ). Only during “Low” to “High” transition, does this current increase to a higher value in order to charge the K Line capacitor (CL < 4.0 nF) in a short time (see Figure 3).
6. Measured with TXD = V_{CC}, I1 = V_S, DIA and L high, no load, REF–IN–L and REF–IN–K connected to REF–OUT.

ELECTRICAL CHARACTERISTICS (continued) (– 40°C ≤ T_A ≤ 125°C, 4.5 V ≤ V_{CC} ≤ 5.5 V, 4.5 V ≤ V_S ≤ 20 V, unless otherwise noted. Typical values reflect approximate mean at 25°C, nominal V_{CC} and V_S, at time of device characterization.)

Characteristic	Symbol	Min	Typ	Max	Unit
REF–OUT PIN 14					
Output Voltage	V_{ref}				V
3.0 < V_S < 5.6 V and I_{RO} = ±10 µA		2.7	–	3.3	
5.6 < V_S < 18 V and I_{RO} = ±10 µA		0.5 x V_S	–	0.56 x V_S	
18 < V_S < 40 V and I_{RO} = ±10 µA		8.5	–	10.8	
Maximum Output Current	I_{out}	–50	–	50	µA
Pull–Up Resistor to V_{CC}	R_{PU}	3.0	8.0	12	kΩ

NOTES:
1. Measured with TXD = V_{CC}, I1 = V_S, DIA and L high, no load. REF–IN–L and REF–IN–K connected to REF–OUT.
2. 0 < V_{CC} < 5.5 V, 0 < V_S < 40 V, 0 < V_{DIA} < 20 V, TXD high or floating.
3. When an over temperature is detected, the DIA output is forced “off”.
4. 0 < V_{CC} < 5.5 V, 0 < V_S < 40 V, 0 < V_L < 20 V.
5. At static “High” or “Low” level TXD, the current source I1 delivers a current of 3.0 mA (typ). Only during “Low” to “High” transition, does this current increase to a higher value in order to charge the K Line capacitor (CL < 4.0 nF) in a short time (see Figure 3).
6. Measured with TXD = V_{CC}, I1 = V_S, DIA and L high, no load, REF–IN–L and REF–IN–K connected to REF–OUT.

DYNAMIC CHARACTERISTICS (– 40°C ≤ T_A ≤ 125°C, 4.5 V ≤ V_{CC} ≤ 5.5 V, 4.5 V ≤ V_S ≤ 20 V, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Transmission Speed	1/t Bit	0	–	200 k	Baud
High or Low Bit Time	t Bit	5.0	–	–	µs
RXD Output					ns
Low to High Transition Delay Time	t_{RDR}	–	–	450	
High to Low Transition Delay Time	t_{RDF}	–	–	450	
LO Output					µs
Low to High Transition Delay Time	t_{LDR}	–	–	2.0	
High to Low Transition Delay Time	t_{LDF}	–	–	2.0	
DIA Output					ns
Low to High Transition Delay Time	t_{DDR}	–	–	650	
High to Low Transition Delay Time	t_{DDF}	–	–	650	
I1 Output (V_S – I1 > 2.7 V)					µs
Rise Time	t_{I1R}	–	–	0.3	
Hold Time	t_{I1F}	1.5	–	4.5	

Figure 1. TXD to DIA AC Characteristic

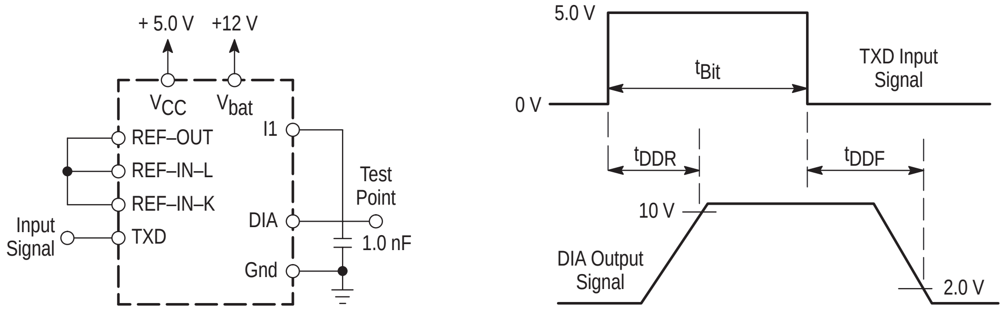


Figure 2. DIA to TXD and L to LO AC Characteristics

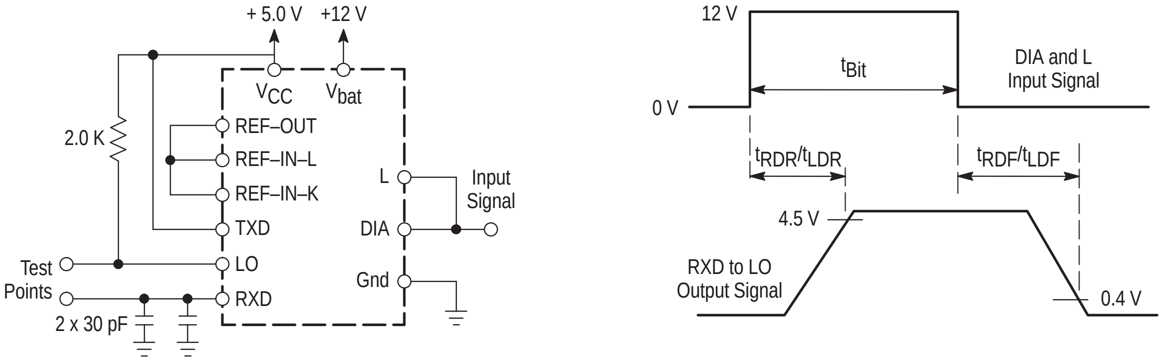
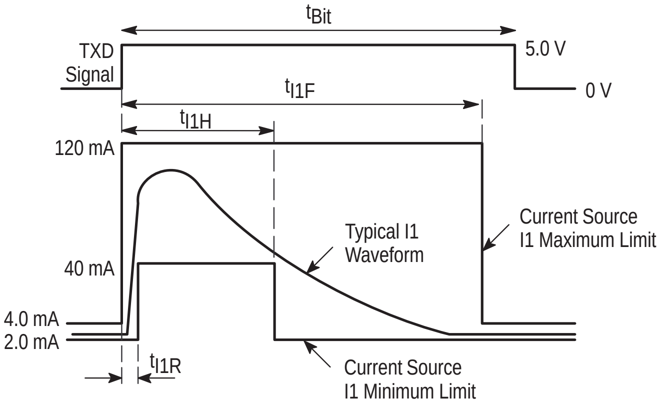


Figure 3. Current Source I1 AC Characteristics



At static “High” or “Low” level TXD, the current source I1 delivers a current of 3.0 mA (typ). Only during “Low” to “High” transition, does this current increase to a higher value in order to charge the K Line capacitor (Cl < 4.0 nF) in a short time.

Figure 4. Current Source I1 and DIA Discharge Current Test Schematic

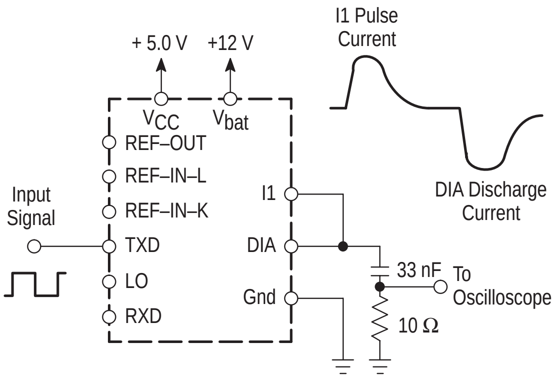


Figure 5. Logic Diagram and Application Schematic

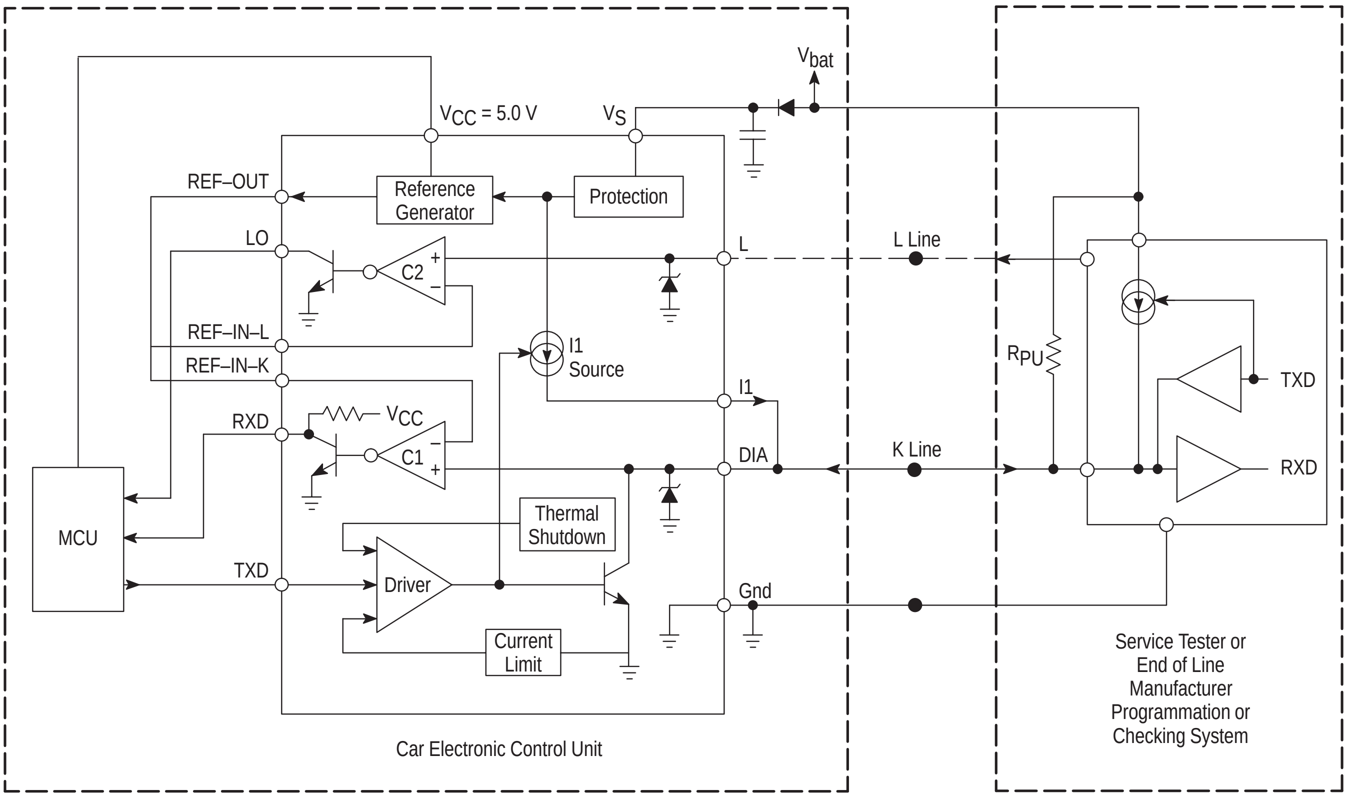


Figure 6. Typical Application with Several ECUs

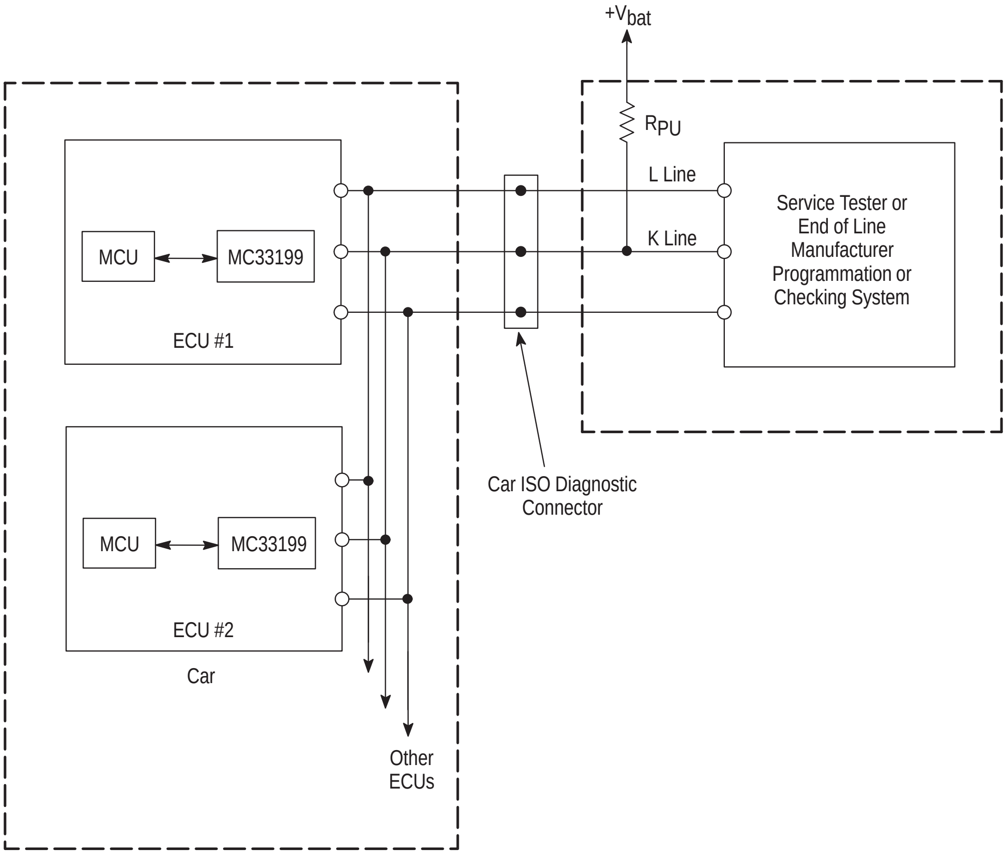


Figure 7. I_{CC} Supply Current versus Temperature

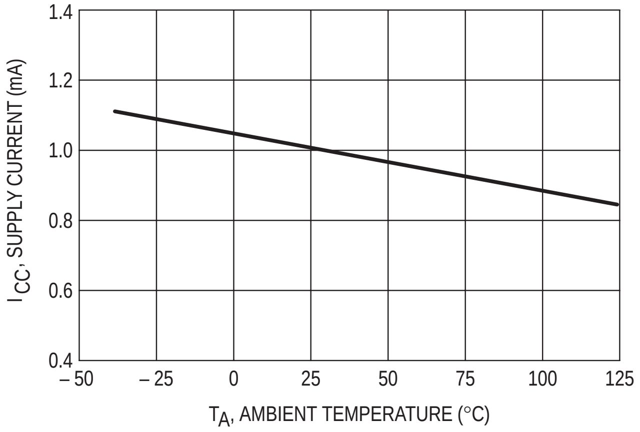


Figure 8. I_S Supply Current versus V_S Supply Voltage

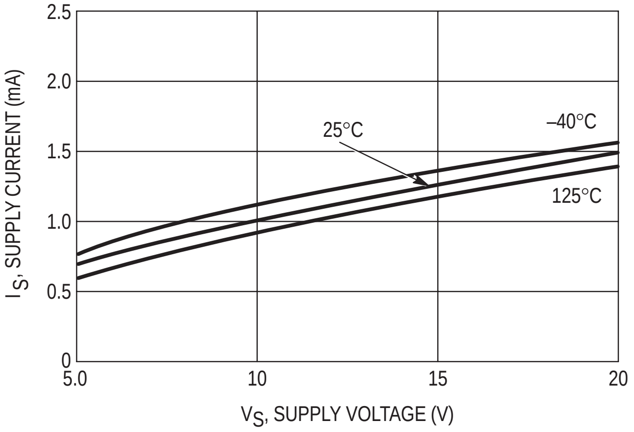


Figure 9. I_S Supply Current versus V_S Supply Voltage

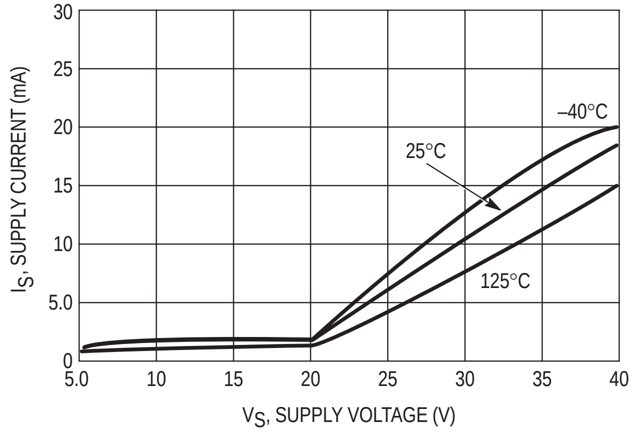


Figure 10. V_S Voltage versus I_S Current

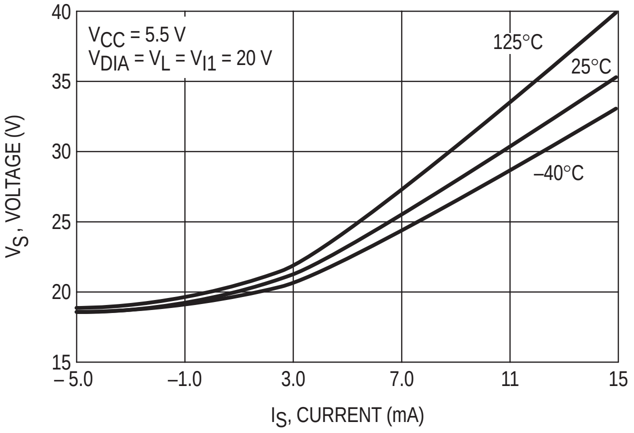


Figure 11. REF–OUT Voltage versus V_S Supply Voltage

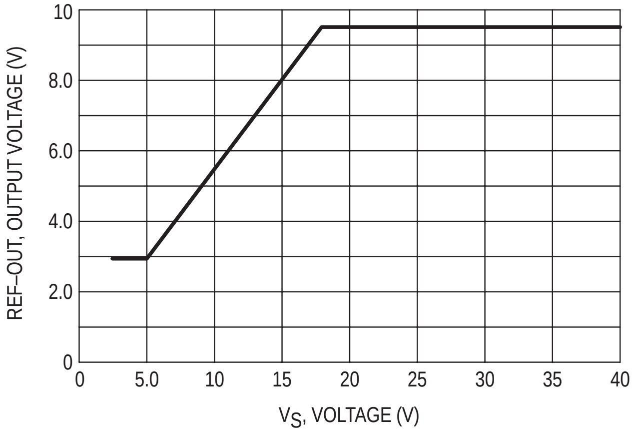


Figure 12. REF–OUT Voltage versus REF–OUT Current

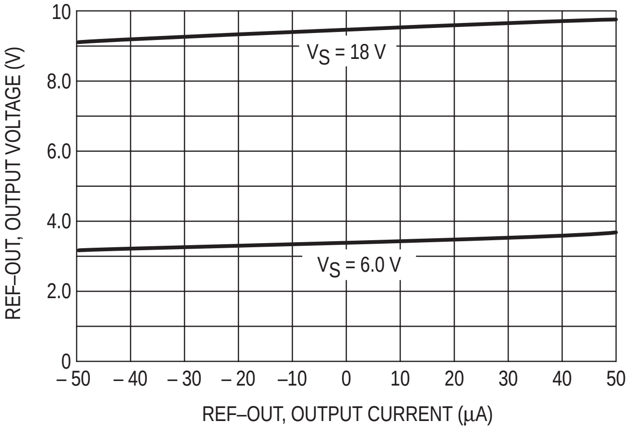


Figure 13. L and DIA Hysteresis versus Ambient Temperature

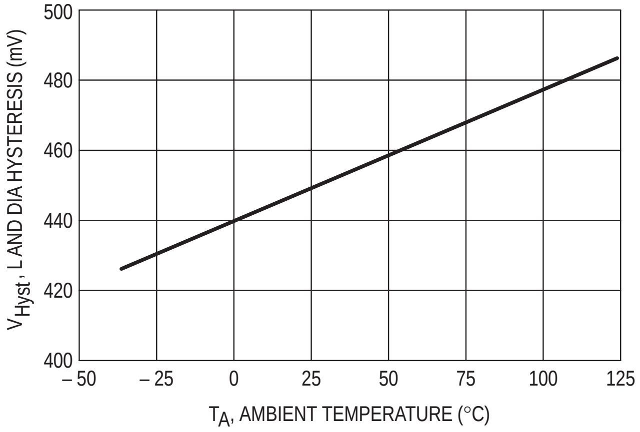


Figure 14. L and DIA Current versus L and DIA Voltage

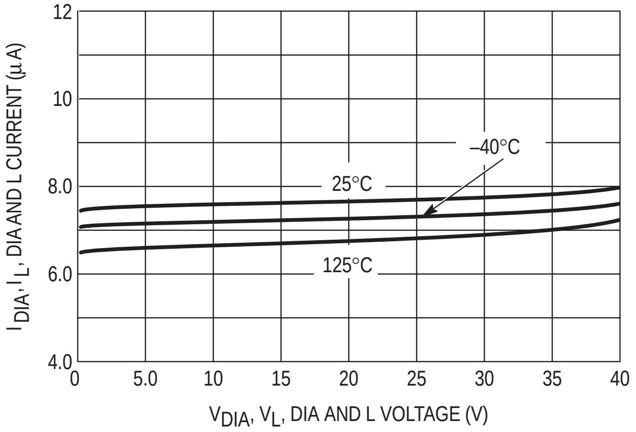


Figure 15. DIA Saturation Voltage versus Temperature

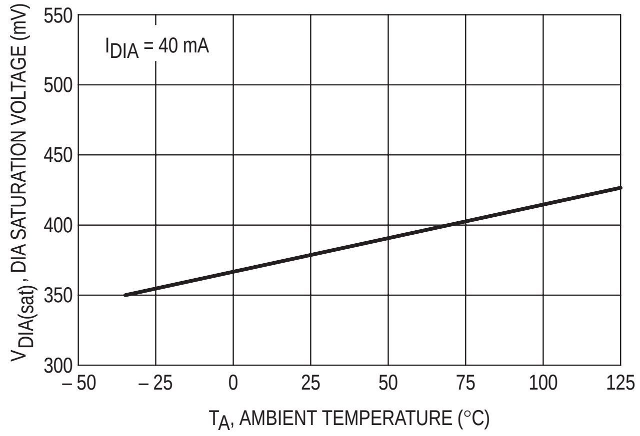


Figure 16. DIA Current Limit versus Temperature

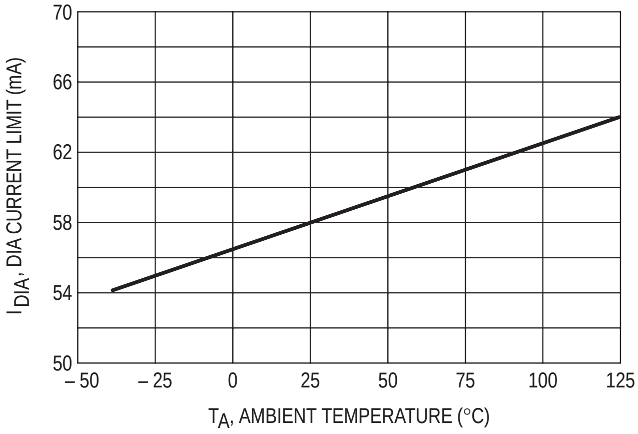


Figure 17. RXD Pull–Up Resistor versus Temperature

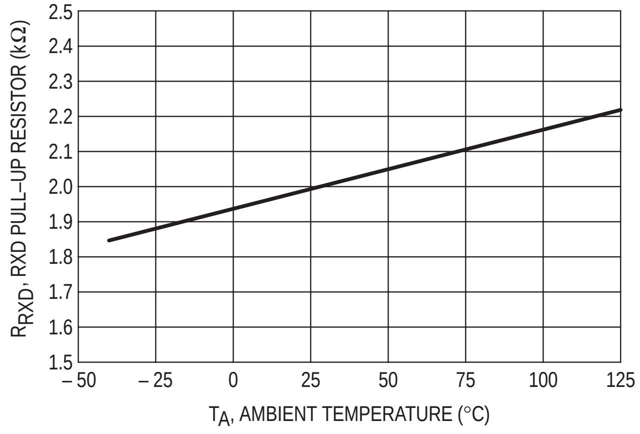


Figure 18. TXD and LO Saturation Voltage versus Temperature

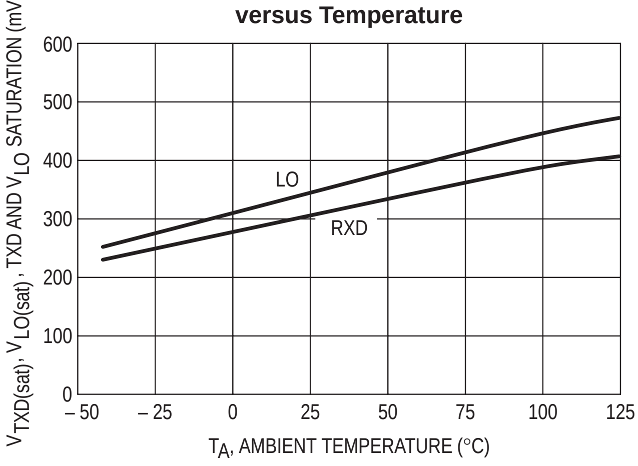


Figure 19. I1 Saturation Voltage versus Temperature

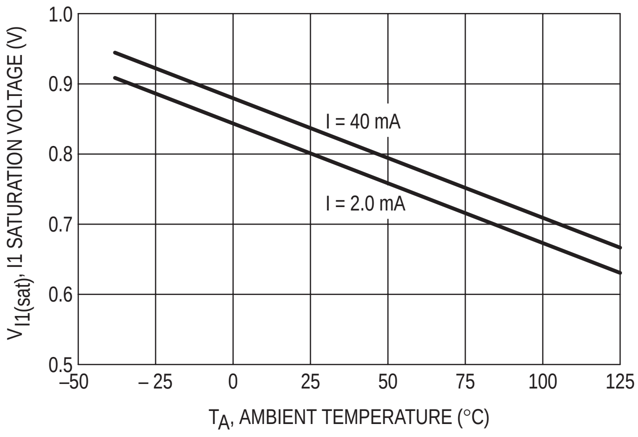


Figure 20. I1 Output DC Current versus Temperature

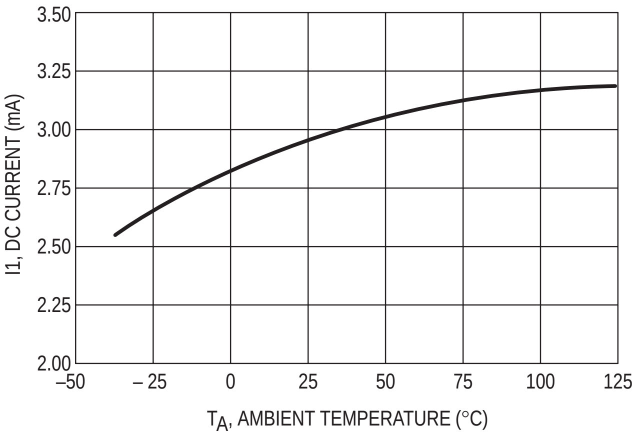


Figure 21. I1 Output Pulse Current versus V_S Supply Voltage

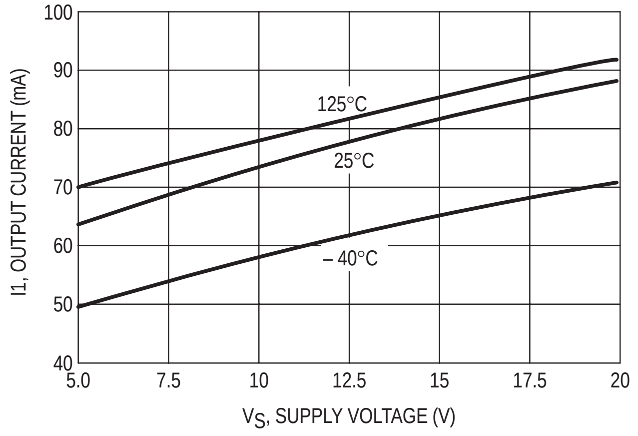


Figure 22. I1 Pulse Current Width versus Temperature

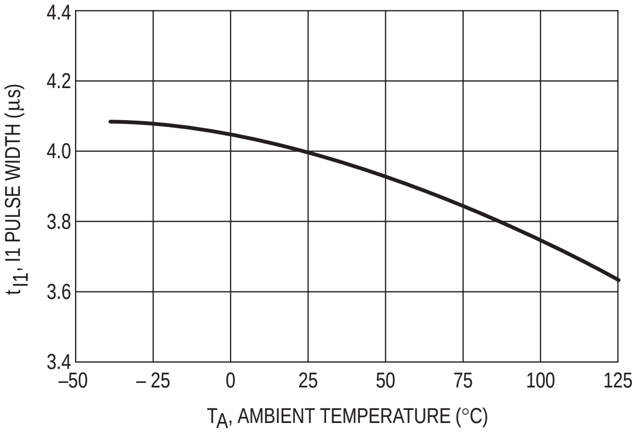
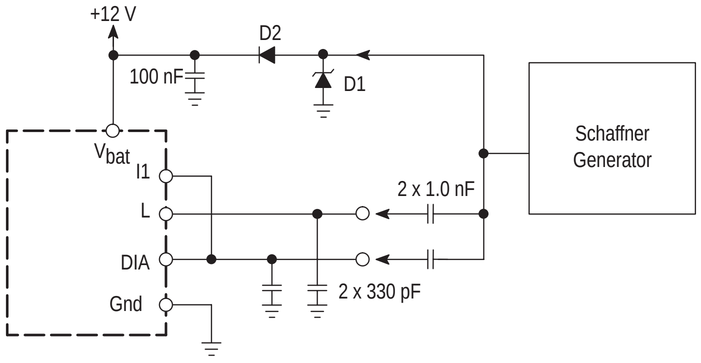


Figure 23. Transient Test Circuit Using Schaffner Generator



Test pulses are directly applied to V_S and via a capacitor of 1.0 nF to DIA and L. The voltage V_S is limited to – 2.0 V/40 V by the transient suppressor diode D1. Pulses can occur simultaneously or separately.

INTRODUCTION

The MC33199 is a serial interface circuit used in diagnostic applications. It is the interface between the microcontroller and the special K and L Lines of the ISO diagnostic port. The MC33199 has been designed to meet the “Diagnosis System ISO 9141” specification.

This product description will detail the functionality of the device (see simplified application). The power supply and reference voltage generator will be discussed followed by the path functions between MCU, K and L Lines. A dedicated paragraph will discuss the special functionality of the I1 pin in it’s ability to accommodate high baud rate transmissions.

Power Supplies and Reference Voltage

The device requires two power supplies to be used; a 5.0 V supply, V_{CC}, which is normally connected to the MCU supply. The device V_{CC} pin is capable of sinking typically 1.0 mA during normal operation. A V_{bat} supply voltage, V_S, is normally tied to the car’s battery voltage. The V_{bat} pin can sustain up to 40 V dc. Care should be taken to provide any additional reverse battery and transient voltage protection in excess of 40 V.

The voltage reference generator is supplied from both V_{CC} and V_{bat} pins. The voltage reference generator provides a reference voltage for the K and L Line comparator thresholds. The reference voltage is dependant on the V_{bat} voltage; it is linear in relation to the V_{bat} voltage for all V_{bat} voltages between 5.6 V and 18 V. Below 5.6 V and over 18 V the reference voltage is clamped (see Figure 11). The REF–OUT pin connects the reference voltage out externally making it available for other application needs. The REF–OUT pin is capable of supplying a current of 50 µA (see Figure 12).

Path Functions Between MCU, K and L Lines

The path function from the MCU to the K Line uses a driver to interface directly with the MCU through the TXD pin. The TXD pin is CMOS compatible. This driver controls the On–Off conduction of the power transistor. When the power transistor is On, it pulls the DIA pin low. This pin is known as K Line in the ISO 9141 specification. The DIA pin structure is open collector and requires an external pull–up resistor for use. Having an open collector without an internal pull–up resistor allows several MC33199 to be connected to the K Line while using a single pull–up resistor for the system (see Figure 6). In order to protect the DIA pin against short circuits to V_{bat}, the MC33199 incorporates an internal current limit (see Figure 16) and thermal shutdown circuit. The current limit feature makes it possible for the device to drive a K Line bus having a large parasitic capacitor value (see Special Functionality of I1 pin below).

The path from the DIA pin, or K Line, to the MCU is done through a comparator. The comparator threshold voltage is connected to REF–IN–K pin. It can be tied to the REF–OUT voltage if a V_{bat} dependant threshold is required in the application. The second input of this comparator is connected internally to DIA pin. The output of this comparator is available at the RXD output pin and normally connects to an MCU I/O port. RXD pin has a 2.0 kΩ internal pull–up resistor.

The path from the L Line, used during a wake–up sequence of the transmission, to the MCU is done through a second comparator. The comparator threshold voltage is connected to REF–IN–L pin. The REF–IN–K pin can be tied to the REF–OUT voltage if a V_{bat} dependant threshold is required in the application. The second input of this comparator is internally connected to L pin. The output of this comparator is available on LO output pin, which is also an open collector structure. The LO pin is normally connected to an MCU I/O port.

The DIA and L pins can sustain up to 40 V dc. Care should be taken to protect these pins from reverse battery and transient voltages exceeding 40 V.

The DIA and L pins both have internal pull–down current sources of typically 7.5 µA (see Figure 14). The L Line exhibits a 10 µA pull–down current. The DIA pin has the same behavior when it is in “off” state, that is when TXD is at logic high level.

Special Functionality of I1 Pin

The MC33199 has a unique feature which accommodates transmission baud rates of up to 200 k baud. In practice, the K Line can be several meters long and have a large parasitic capacitance value. Large parasitic capacitance values will slow down the low to high transition of the K Line and limit the baud rate transmission. For the K Line to go from low to high level, the parasitic capacitor must first be charged, and can only be charged through the pull–up resistor. A low pull–up resistor value would result in fast charge time of the capacitor but also large output currents to be supplied causing a high power dissipation in the driver.

To avoid this problem, the MC33199 incorporates a dynamic current source which is temporarily activated at the low to high transition of the TXD pin when the DIA pin or K Line switches from a low to high level (see Figures 3 and 4).

This current source is available at the I1 pin. The I1 pin has a typical current capability of 80 mA. It is activated for 4.0 µs (see Figures 21 and 22) and is automatically disabled after this time. During this time it will charge the K Line parasitic capacitor. This extra current will quickly increase the K Line voltage up to V_{bat}, resulting in a reduced rise time of the K Line. With this feature, the MC33199 ensures baud rate transmission of up to 200 k baud.

During high to low transitions of the K Line, the parasitic capacitor of the line will be discharged by the output transistor of the DIA pin. In this case, the total current may exceed the internal current limitation of the DIA pin. If so, the current limit circuit will activate, limiting the discharge current to typically 60 mA (see Figures 4 and 16).

If a high baud rate is necessary, the I1 pin should be connected to the DIA as shown in the typical application circuit shown in Figure 5. The I1 pin can be left open, if the I1 functionality and high baud rate are not required for the application.

PIN DESCRIPTION

Pin 1: V_{CC}

Power Supply pin; typically 5.0 V and requiring less than 1.5 mA.

Pin 2: REF–IN–L

Input reference for C2 comparator. This input can be connected directly to REF–OUT with or without a resistor network or to an external reference.

Pin 3: REF–IN–K

Input reference for C1 comparator. This input can be connected directly to REF–OUT with or without a resistor network or to an external reference.

Pin 4: LO

Output of C2 comparator and normally connected to a microcontroller I/O. If L input > (REF–IN–L + Hyst/2); output LO is in high state. If L< (REF–IN–L – Hyst/2); output LO is in low state and the output transistor is "on". This pin is an open collector structure and requires a pull–up resistor to be connected to V_{CC}. Output drive capability of this output is 5.0 mA.

Pin 5: RXD

Receive output normally connected to a microcontroller I/O. If DIA input > (REF–IN–L + Hyst/2); output LO is in high state. If DIA < (REF–IN–L – Hyst/2); output LO is in low state and the output transistor is "on". This pin has an internal pull–up resistor (typically 2.0 kΩ) connected to V_{CC}. Drive capability of this output is 5.0 mA.

Pin 6: TXD

Transmission input normally connected to a microcontroller I/O. This pin controls the DIA output. If TXD is high, the output DIA transistor is in the "off" state. If TXD is low, the DIA output transistor is "on".

Pin 9: DIA

Input/Output Diagnosis Bus line pin. This pin is an open collector structure and is protected against overcurrent and circuit shorts to V_{bat} and V_S. Whenever the open collector transistor turns "on" (TXD low), the Bus line is pulled to ground and the DIA pin current is internally limited to nominal value of 60 mA. The internal power transistor incorporates a thermal shutdown circuit which forces the DIA output "off" in the event of an over temperature condition. The DIA pin is also the C1 comparator input. It is protected against both positive and negative overvoltages by an internal 40 V zener diode. This pin exhibits a constant input current of 7.5 μA.

Pin 10: Gnd

Ground reference for the entire device.

Pin 11: I1

Bus source current pin. It is normally tied to DIA pin and to the Bus line. The current source I1 delivers a nominal current of 3.0 mA at static "High" or "Low" levels of TXD. Only during "Low" to "High" transitions, does this current increase to a higher value so as to charge the key line capacitor (Cl < 4.0 nF) in a short time (see Figures 3 and 4).

Pin 12: L

Input for C2 comparator. This pin is protected against both positive and negative overvoltage by a 40 V zener diode. This L Line is a second independent input. It can be used for wake up sequence in ISO diagnosis or as an additional input bus line. This pin exhibits a constant input current of 7.5 μA.

Pin 13: V_S

12 V typical, or V_{bat} supply pin for the device. This pin is protected against overvoltage transients.

Pin 14: REF–OUT

Internal reference voltage generator output pin. Its value depends on V_S (V_{bat}) values. This output can be directly connected to REF–IN–L and REF–IN–K, or through a resistor network. Maximum current capability is 50 μA.

MOTOROLA

MC33293A

Advance Information

Quad Low Side Switch

The MC33293A is a single monolithic integrated circuit designed for quad low side switching applications. This device was initially conceived as a quad injector driver for use in the harsh automotive environment but is well suited for many other applications. The MC33293A incorporates *SMARTMOS*™ technology having CMOS logic, bipolar and CMOS analog circuitry and DMOS power MOSFETs. All of the device inputs are CMOS compatible. The four output devices are N-channel power MOSFETs. A Fault detect output is provided to flag the existence of open loads (outputs ON or OFF) or shorted loads. If a short circuit is detected, the fault detect circuitry turns off the shorted output, but allows the others to function normally. An overvoltage (V_{PWR}) condition will turn off all outputs for the overvoltage duration. Each output functions independently and has a drain-to-gate diode clamp for inductive flyback voltage protection. A Single/Dual select pin is incorporated to allow either individual output control or control of a pair of outputs from one input.

The MC33293A is parametrically specified over $-40°C \le T_A \le 125°C$ ambient temperature and a $9.0\ V \le V_{PWR} \le 14.5\ V$ supply.

- Designed to Operate with Supply Voltages of 5.5 V to 30 V
- CMOS Compatible Inputs with Active Pull-Downs
- Maximum 5.0 mA Quiescent Current
- $R_{DS(on)}$ of 0.25 Ω Maximum at 25°C, with $V_{PWR} \ge 9.0$ V
- Each Output Clamped to 65 V for Driving Inductive Loads
- Each Output Current Limited at 3.0 A to handle Incandescent Lamp Loads
- Active Low Output Fault Status with Interrogation Capability
- Open Load Detection (Output ON or OFF)
- Capable of Withstanding Reverse Battery
- Overvoltage Shutdown
- Short Circuit Detection and Shutdown with Automatic Retry

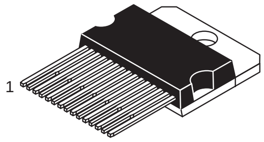
ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC33293AT	T_J = –40° to +150°C	15 Pin SIP
MC33293ATV		

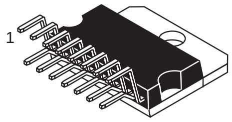
QUAD LOW SIDE SWITCH

($R_{DS(on)}$ = 0.25 Ω Max per Output)

SEMICONDUCTOR TECHNICAL DATA



T SUFFIX
PLASTIC PACKAGE
CASE 821D

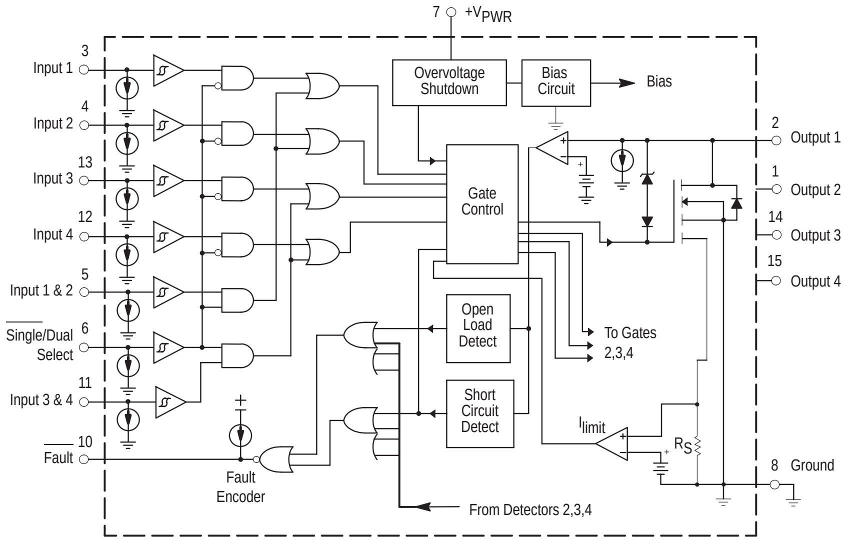


TV SUFFIX
PLASTIC PACKAGE
CASE 821C

PIN CONNECTIONS

Pin 1. Output 2
2. Output 1
3. Input 1
4. Input 2
5. Input 1 & 2
6. Single/Dual
7. V_{PWR}
8. Gnd
9. N/C
10. Fault
11. Input 3 & 4
12. Input 4
13. Input 3
14. Output 3
15. Output 4

Simplified Block Diagram



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
V_{CC} Steady-State Transient Conditions	V_{PWR} $V_{PWR(pk)}$	–13 to 30 –13 to 60	V
Input Pin Voltage	V_{in}	– 0.5 to 7.5	V
ESD Capability Human Body Model (R = 1.5 kΩ, C = 200 pf)	V_{ESD}	2000	V
Lead Current (per Output)	I_{Out}	Internally Limited	A
Single Pulse Clamp Energy @ 25°C, 1.5 A	E_{clamp}	100	mJ
Storage Temperature	T_{stg}	– 55 to +150	°C
Operating Temperature	T_J	– 40 to +150	°C
Lead Temperature (Wave Solder, 10 s)	T_{solder}	260	°C
Power Dissipation @ T_A = 105°C Power Dissipation @ T_A = 125°C Derate for every °C above 25°C	P_D	11.25 6.25 0.25	W W/°C
Thermal Resistance Junction-to-Ambient	$R_{\theta JA}$	35	°C/W
Thermal Resistance Junction-to-Case. Any one O/P	$R_{\theta JC}$	4.0	°C/W

STATIC ELECTRICAL CHARACTERISTICS (9.0 V ≤ V_{PWR} ≤ 14.5 V and – 40°C ≤ T_C ≤ +125°C, unless otherwise noted. Typical values are at 25°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
INPUT					
Turn ON Threshold	$V_{on(th)}$	—	3.4	5.5	V
Operating Voltage Range	V_{PWR}	5.5	—	30	V
Quiescent Power Supply Current (All Inputs off)	I_{PWR}	—	2.2	5.0	mA
Overvoltage Shutdown Range	$V_{PWR(ov)}$	30	35	38	V
Overvoltage Reset Hysteresis	$V_{PWR(hys)}$	2.0	5.0	7.0	V
Input Voltage High (I_{DS} = 1.0 A) Low (I_{DS} = 80 μA)	 V_{IH} V_{IL}	 3.0 —	 2.3 1.6	 — 0.8	V
Input High Hysteresis (I_{DS} = 1.0 A)	$V_{IH(hys)}$	0.4	0.7	—	V
Input Current High (V_{IH} = 3.0 V) Low (V_{IL} = 0.8 V)	 I_{IH} I_{IL}	 — —	 11 11	 50 50	μA
OUTPUT					
Static Drain-Source On-Resistance (I_{DS} = 1.0 A, V_{PWR} = 13 V, T_C = – 40°C to + 25°C) (I_{DS} = 1.0 A, V_{PWR} = 13 V, T_C = +125°C) (I_{DS} = 0.7 A, V_{PWR} = 8.0 V, T_C = + 25°C) (I_{DS} = 0.4 A, V_{PWR} = 5.5 V, T_C = + 25°C)	$RDS_{(on)}$	 — — — —	 0.18 0.28 0.20 0.22	 0.25 0.50 0.40 0.50	Ω
Drain-Source Clamp Voltage (I_{DS} = 20 mA, V_{in} = 0 V, t_{clamp} = 100 μs)	BV_{DSS}	 55	 64	 80	V
Zero Input Voltage Drain Current (V_{DS} = 25 V, V_{PWR} = 14.5 V) (V_{DS} = 58 V, V_{PWR} = 14.5 V)	$I_{DS(off)}$	 10 —	 23 0.06	 80 2.0	 μA mA
Source Drain Diode Forward Voltage (I_{SD} = 1.0 A)	V_{SD}	—	0.62	1.4	V

STATIC ELECTRICAL CHARACTERISTICS (continued) (9.0 V ≤ V_{PWR} ≤ 14.5 V and – 40°C ≤ T_C ≤ +125°C, unless otherwise noted. Typical values are at 25°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
FAULT STATUS OUTPUTT					
Fault Status Pin					V
Low Voltage (V_{PWR} = 14.5 V, I_{stl} = 1.0 mA, open-load on Output 1, 2, 3 or 4. All inputs = 0 V)	V_{stl}	—	0.1	0.4	
High Voltage, (V_{PWR} = 14.5 V, I_{sth} = – 30 µA, Note 1)	V_{sth}	3.0	4.7	5.5	
FAULT DETECTION					
Output Limiting Current (V_{PWR} = 13 V)	$I_{DS(limit)}$	3.0	4.0	6.0	A
Over-Current Detect Voltage Threshold and	$V_{OC(limit)}$	2.4	3.7	5.0	V
Output-Off Open-Load Detect Threshold Voltage	$V_{Ooff(th)}$	2.4	3.7	5.0	
output-on open-load Detect Current	$I_{Oon(th)}$				mA
(V_{PWR} = 13 V, V_{in} = 5.0 V, T_C = – 40°C)		20	80	190	
(V_{PWR} = 13 V, V_{in} = 5.0 V, T_C = + 25°C)		20	75	130	
(V_{PWR} = 13 V, V_{in} = 5.0 V, T_C = +125°C)		20	65	100	

DYNAMIC ELECTRIC CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit
OUTPUT TIMING					
Output Driver Rise Time (V_{CC} = 13 V, R_L = 13 Ω, t_r = Output Voltage change from 90% to 10%, see Figure 2)	t_r	—	2.3	10	µs
Output Driver Fall Time (V_{CC} = 13 V, R_L = 13 Ω, t_f = Output Voltage change from 10% to 90%, see Figure 2)	t_f	—	1.5	10	µs
Output Delay Time (V_{CC} = 13 V, R_L = 13 Ω,					µs
$t_{on(dly)}$ = V_{in} at 3.0 V to V_O at 90%, see Figure 2)	$t_{on(dly)}$	—	3.2	10	
$t_{off(dly)}$ = V_{in} at 1.0 V to V_O at 10%, see Figure 2)	$t_{off(dly)}$	—	5.9	15	
FAULT TIMING					
Over-Current Sense Time (See Figure 5 or 6) (V_{in} = 5.0 V, R_L = 0.05 Ω, V_{PWR} = 14.5 V, over-current duty cycle ≤ 10% t_{oc} = time that V_{Status} is > 1.0 V)	t_{oc}	10	55	250	µs
Over-Current Refresh Time (See Figures 5 or 6) (V_{in} = 5.0 V, R_L = 0.05 Ω, V_{PWR} = 14.5 V, over-current duty cycle ≤ 10% t_{ref} = time that V_{Status} is < 1.0 V)	t_{ref}	1.5	3.6	7.0	ms
Output Open-Load Fault Status Delay Time					ms
(V_{PWR} = 13 V, V_{in} = 5.0 V, open-load on Output, $t_{os(on)}$ = time from V_{in} = 3.0 V to V_{Status} = 1.0 V, see Figure 3)	$t_{os(on)}$	1.0	2.2	4.0	
(V_{PWR} = 13 V, V_{in} = 0 V, open-load on Output, $t_{os(off)}$ = time from V_{in} = 2.5 V to V_{Status} = 1.0 V, see Figure 4)	$t_{os(off)}$	1.0	19	40	µs
Fault Status Reset Delay Time (V_{PWR} = 13 V, V_{in} = 0 V, see Figure 4)	$t_{s(reset)}$	—	2.0	10	µs

NOTE: 1. Negative current signifies current flowing out of device.

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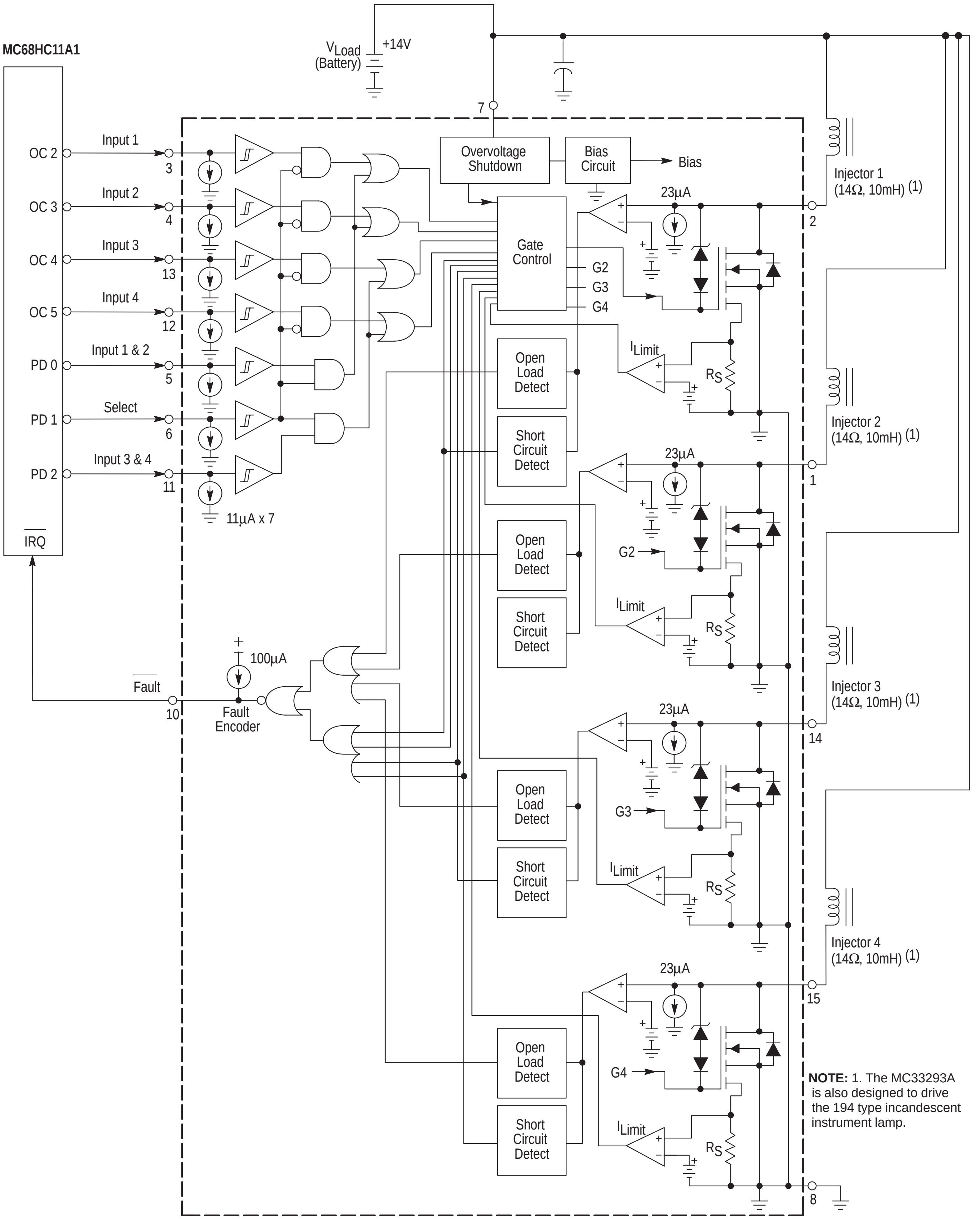
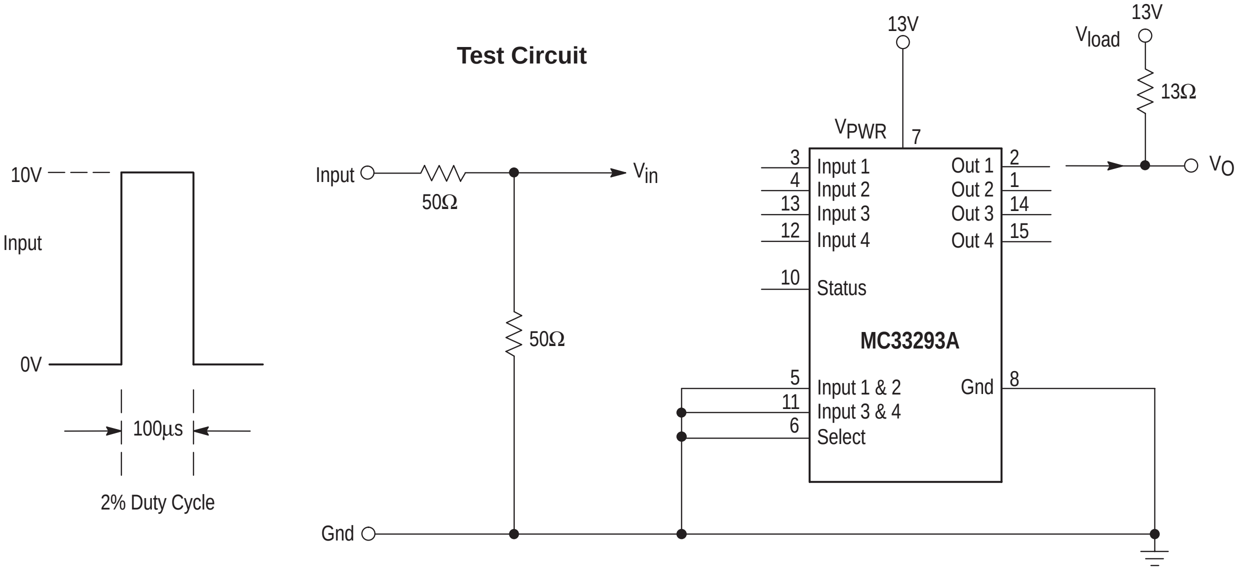
Figure 1. Fuel Injector Application Block Diagram



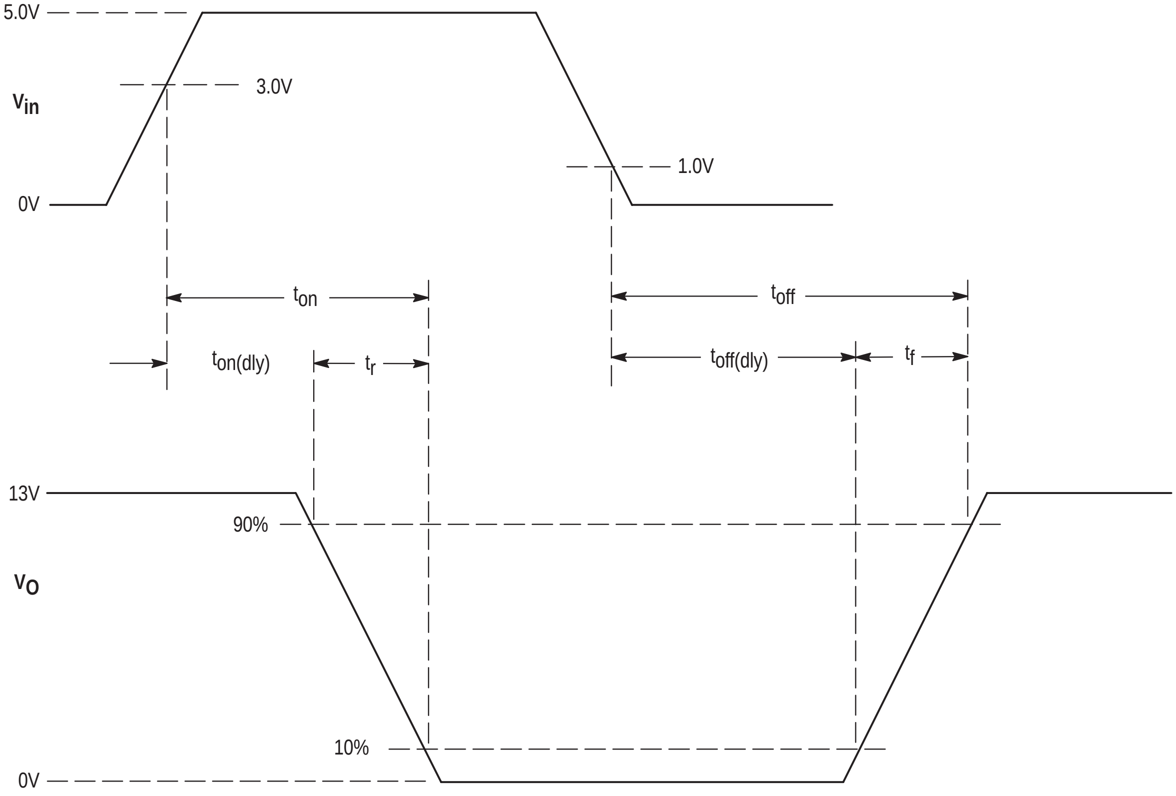
NOTE: 1. The MC33293A is also designed to drive the 194 type incandescent instrument lamp.

Figure 2. Switching Speed Test Circuit and Response Times

Test Circuit



Response Times



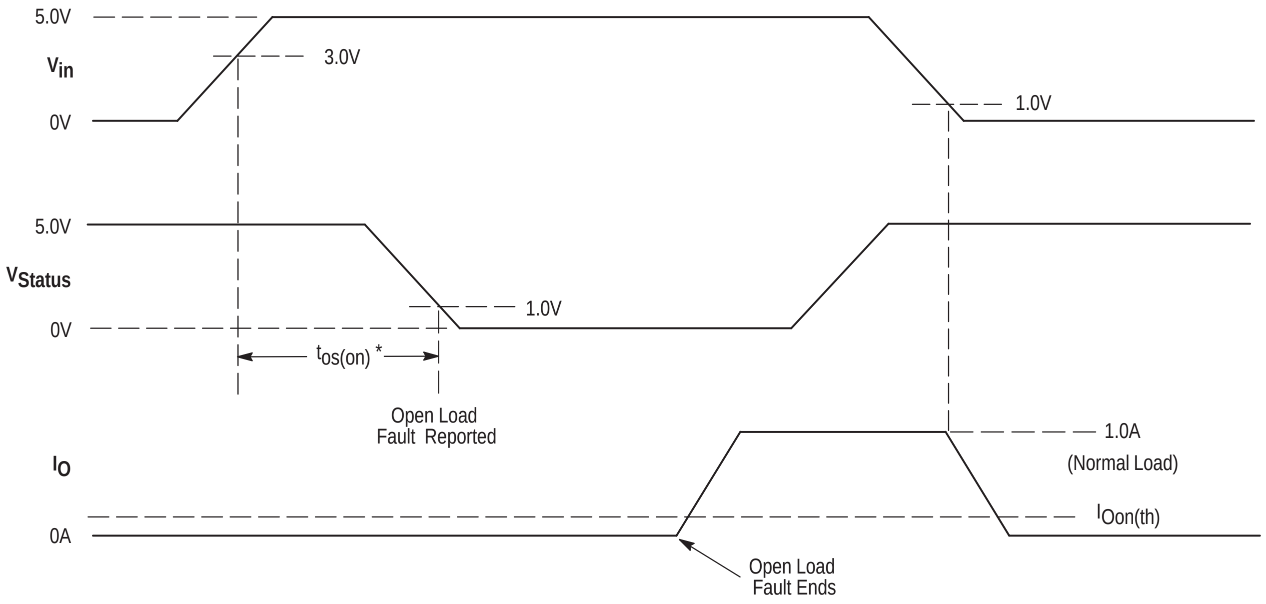


Figure 3. Fault Status Operation with an Output-On, Open-Load Fault

* If the open occurs after the output has been on, the delay time is much less than $t_{os(on)}$.

NOTE: Rise and fall times are exaggerated for emphasis.

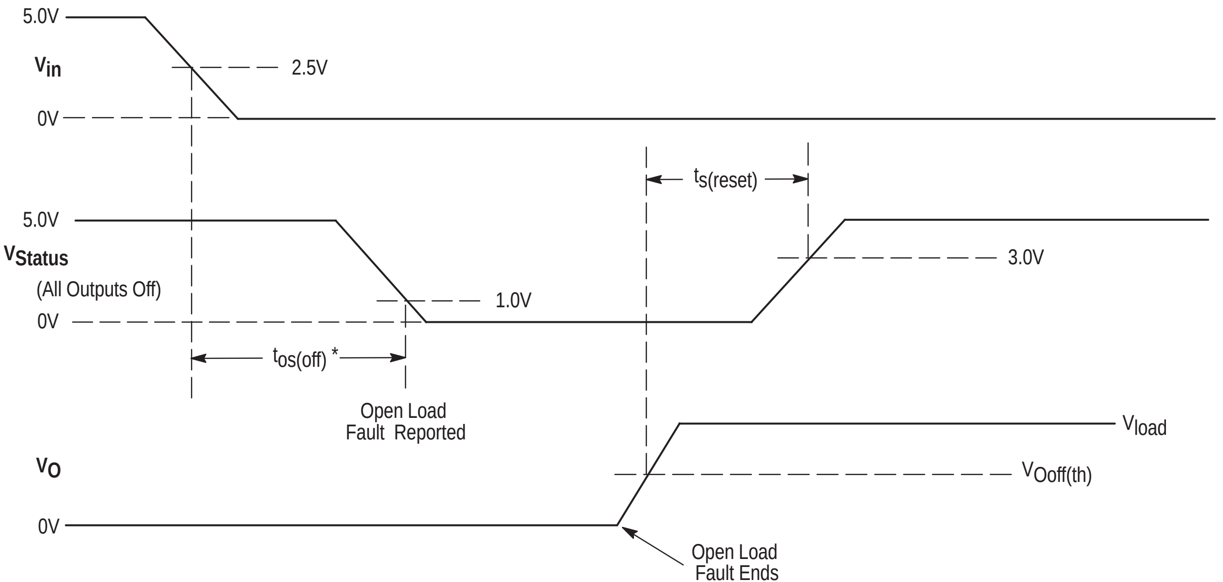
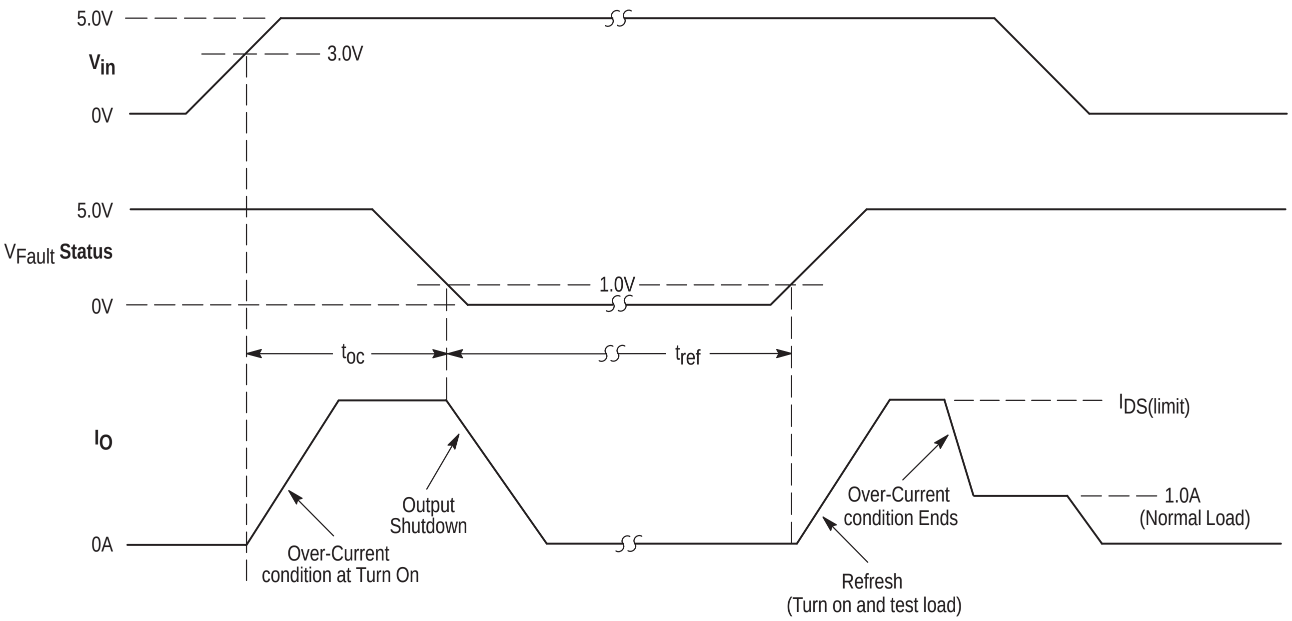


Figure 4. Fault Status Operation with an Output-Off, Open-Load Fault

* If the open occurs after the output has been off, the delay time is much less than $t_{os(off)}$.

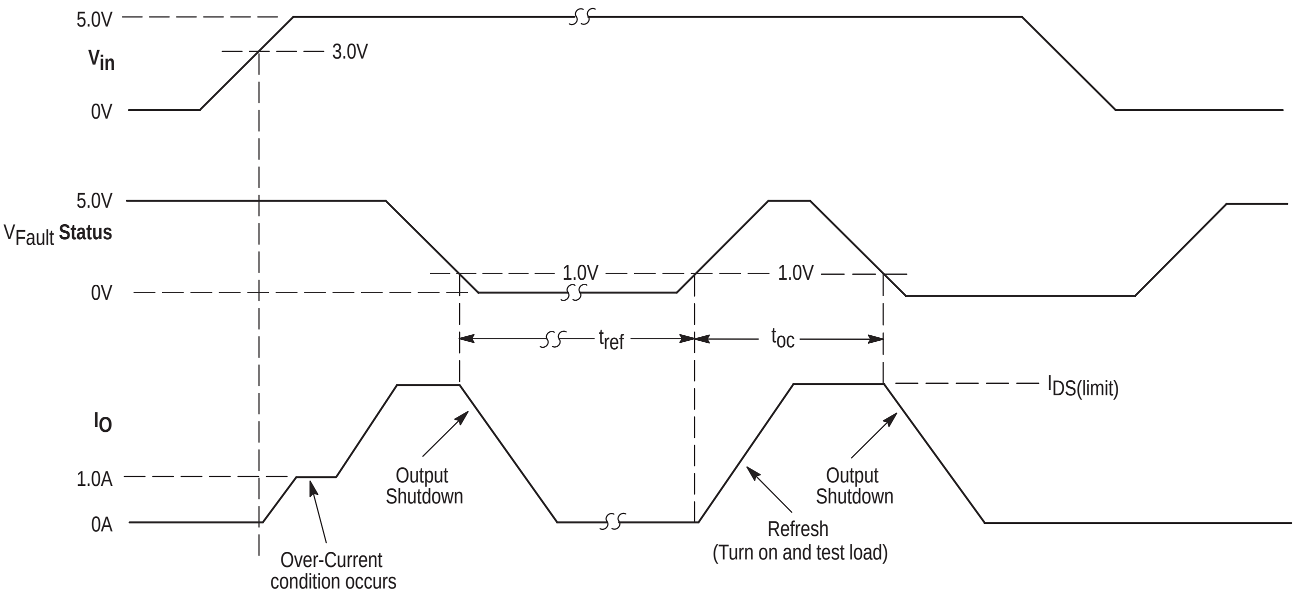
NOTE: Rise and fall times are exaggerated for emphasis.

Figure 5. Fault Status Operation with Turn On into an Over-Current Load



NOTE: Rise and fall times are exaggerated for emphasis.

Figure 6. Fault Status Operation with Over-Current Load after Turn On



NOTE: Rise and fall times are exaggerated for emphasis.

Figure 7. Turn On Threshold Voltage versus Temperature

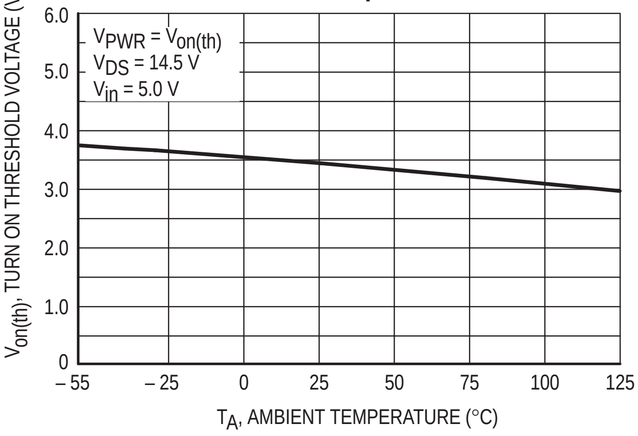


Figure 8. Output On Resistance versus Temperature

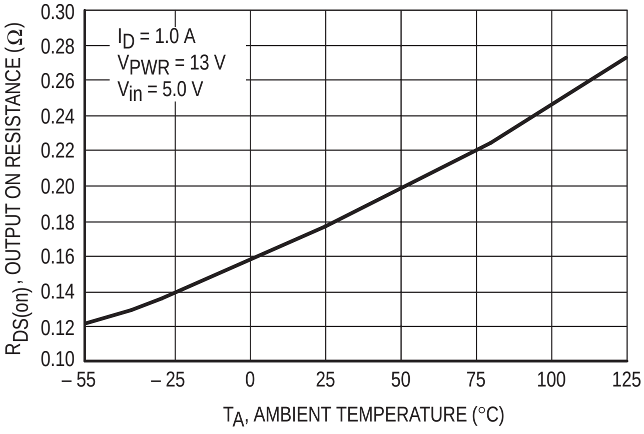


Figure 9. Drain Source Clamp Voltage versus Temperature

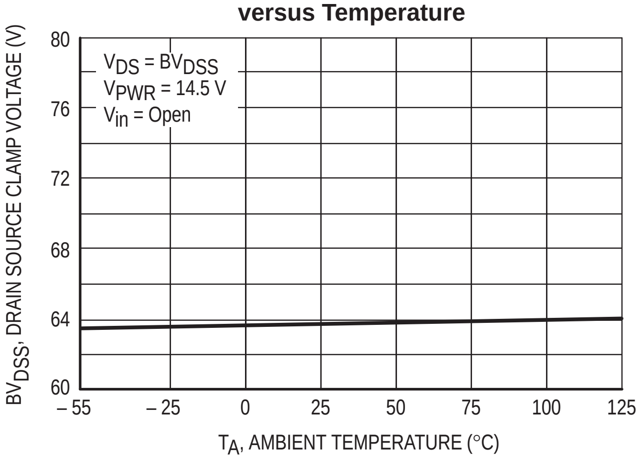


Figure 10. Zero Input Voltage Drain Current versus Temperature

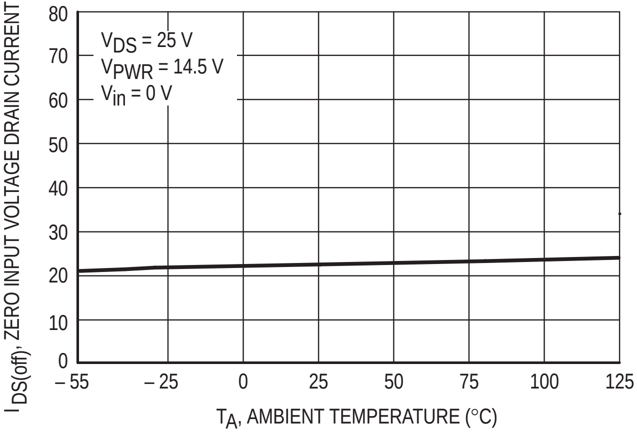


Figure 11. Current Limit versus Temperature

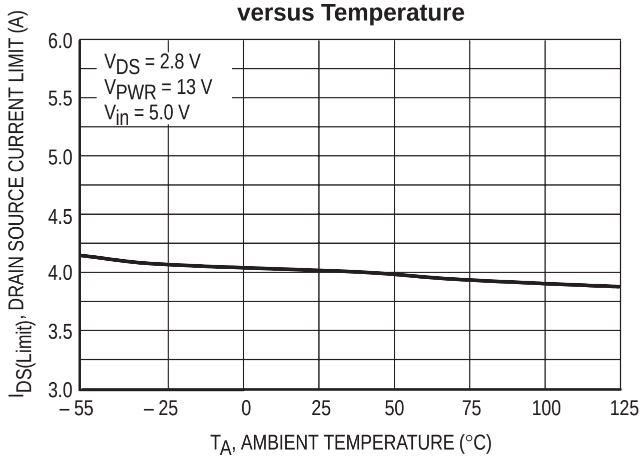
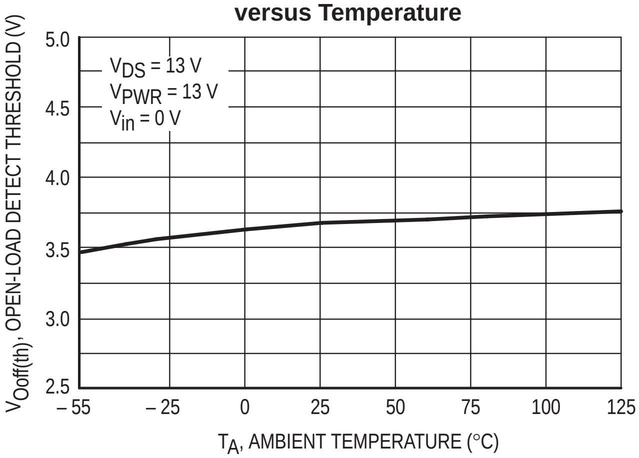


Figure 12. Open-Load Threshold versus Temperature



PIN DESCRIPTION

Pin	Function	Description
1	Output 2	This is one of four open drain power MOSFET output connections. The load is connected from this pin to the positive voltage supply.
2	Output 1	This is one of four open drain power MOSFET output connections. The load is connected from this pin to the positive voltage supply.
3	Input 1	This input controls the turn ON and turn OFF of Output 1 when the $\overline{\text{Single}}$/Dual pin is at a logic low level. It is a CMOS input with an internal active pull-down employed for noise immunity.
4	Input 2	This input controls the turn ON and turn OFF of Output 2 when the $\overline{\text{Single}}$/Dual pin is at a logic low level. It is a CMOS input with an internal active pull-down employed for noise immunity.
5	Input 1 & 2	This input controls the turn ON and turn OFF of Output 1 and Output 2 when the $\overline{\text{Single}}$/Dual select pin is at a logic high level. It is a CMOS input with an internal active pull-down employed for noise immunity.
6	$\overline{\text{Single}}$/Dual Select	This input selects between the single (one input controls one output) mode and the dual (one input controls two outputs) mode of operation.
7	V_{PWR}	The power (voltage and current) to operate the IC is supplied through this pin. The MC33293A is designed to operate over a voltage range of 5.5 V to 30 V.
8	Ground	IC ground reference pin.
9	N/C	No connection.
10	$\overline{\text{Fault}}$	One of three fault conditions, Output-On Open-Load, Output-Off Open-Load or Over-Current are reported at this output. A logic low state signals the existence of a fault condition. This output has an internal active pull-up and does not require an external pull-up resistor.
11	Input 3 & 4	This input controls the turn ON and turn OFF of Output 3 and Output 4 when the $\overline{\text{Single}}$/Dual select pin is at a logic high level. It is a CMOS input with an internal active pull-down employed for noise immunity.
12	Input 4	This input controls the turn ON and turn OFF of Output 4 when the $\overline{\text{Single}}$/Dual pin is at a logic low level. It is a CMOS input with an internal active pull-down employed for noise immunity.
13	Input 3	This input controls the turn ON and turn OFF of Output 3 when the $\overline{\text{Single}}$/Dual pin is at a logic low level. It is a CMOS input with an internal active pull-down employed for noise immunity.
14	Output 3	This is one of four open-drain power MOSFET output connections. The load is connected from this pin to the positive voltage supply.
15	Output 4	This is one of four open-drain power MOSFET output connections. The load is connected from this pin to the positive voltage supply.

CIRCUIT DESCRIPTION

Introduction

The MC33293A is a four output low side switch originally intended for use in automotive applications as a fuel injection driver. This circuit can be used in a variety of applications. It is parametrically specified over a battery voltage range of 9.0 V to 14.5 V, but is designed to operate over a considerably wider range of 5.5 V to 30 V. The design incorporates the use of logic level MOSFETs as output devices which are fully enhanced at a gate voltage of 5.0 V, eliminating the need for internal charge pumps. Each output is identically sized and is *independent* in operation. The efficiency of each output device is such that with as little as 9.0 V of V_{PWR} applied, the $R_{DS(on)}$ is 0.18 Ω typically, at room temperature and increases to only 0.22 Ω as V_{PWR} decreases to 5.5 V.

All inputs of the MC33293A are CMOS and have individual 11 μA internal active pull-downs. This eliminates the need for external pull-down resistors to prevent false switching due to noise on the input control lines. This also ensures that at power-up, no load is turned on before a logic high appears on an input pin. Fault reporting is through the use of an open-drain MOSFET having a 100 μA internal active pull-up.

All inputs incorporate *true logic* (or positive logic). This means that whenever an input is in a logic low state (< 0.8 V) the corresponding output will be in an OFF state. Conversely, whenever an input is in a logic high state (> 3.0 V), the corresponding output will be in an ON state.

$\overline{\text{Single}}$/Dual Select

The $\overline{\text{Single}}$/Dual Select pin can be used to switch between completely independent control and control of the outputs in pairs. Whenever the $\overline{\text{Single}}$/Dual Select pin is in a logic low state, Inputs 1, 2, 3 and 4 control Outputs 1, 2, 3 and 4, respectively. In this mode, only Inputs 1, 2, 3 and 4 can exercise individual control over their respective output. Hence the term “single select” mode of operation. Input 1 & 2 (Pin 5) and Input 3 & 4 (Pin 11) have *no* control whenever the $\overline{\text{Single}}$/Dual Select pin is in a logic low state.

When the Single/Dual Select pin is held at a logic high state, Control Inputs 1, 2, 3 and 4 are turned OFF and can *not* exercise any control over the outputs. In this mode, input control transfers from a single to a dual mode of operation, wherein only Input 1 & 2 and Input 3 & 4 have control of Output 1 plus Output 2, and Output 3 plus Output 4, respectively. Hence the term “Dual Select” mode of operation.

Paralleling Outputs

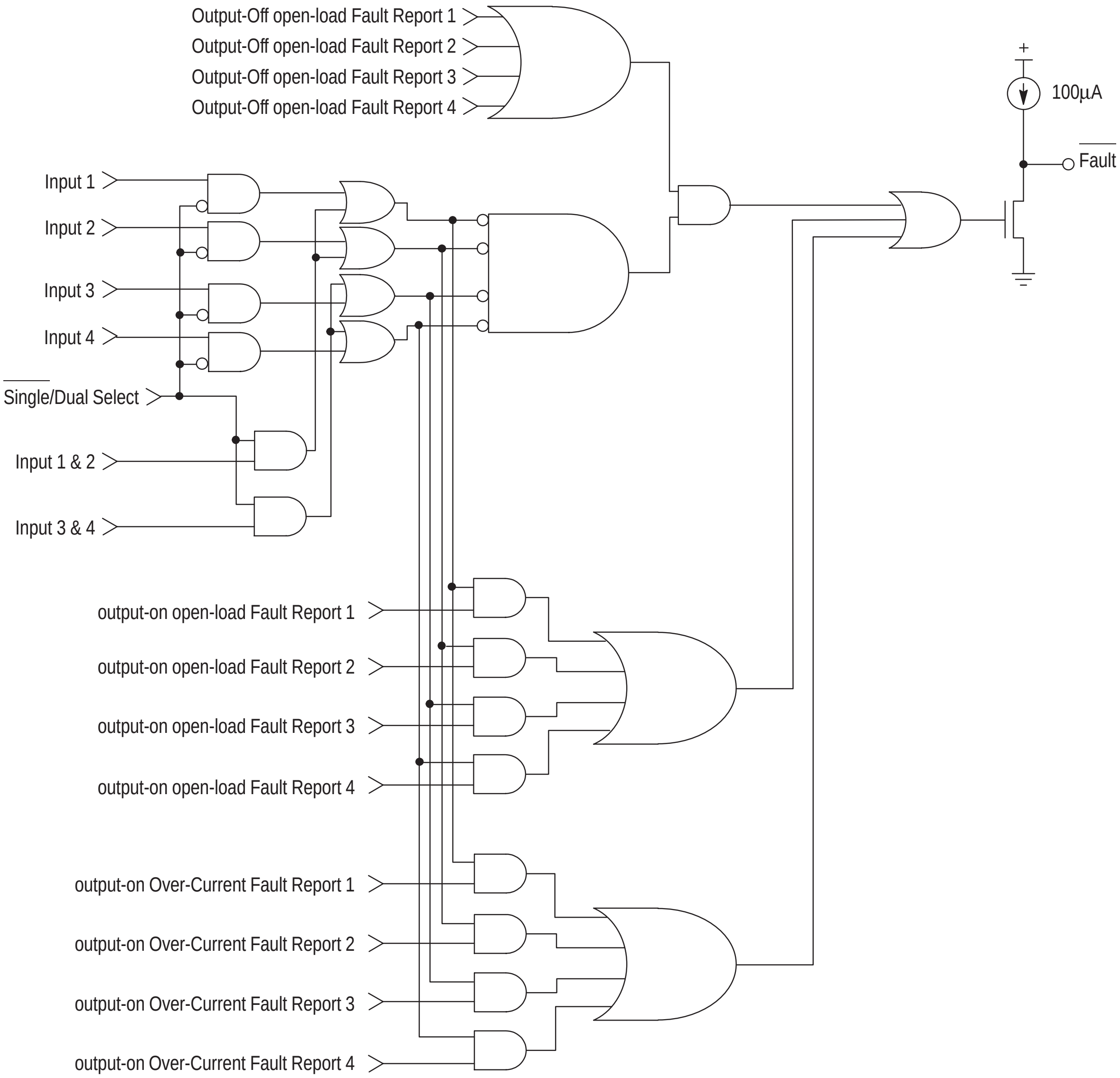
Paralleling outputs may be desirable in the event the application requires a lower $R_{DS(on)}$ or higher current switching capability than a single output. The MC33293A can be operated with all outputs (and therefore all inputs) tied together but modified operation is to be expected. With all inputs tied together and depending on the dual or single select mode used, the paralleled input control current will either be twice (with the dual mode selected) or four times (with the single mode selected) that of any single input. Other expected differences are: $R_{DS(on)}$ will decrease by a factor of four while the Output-On Open-Load Detect current and the Output Limiting current will increase by a factor of four. There will be no change in the Over-Voltage Shutdown Range or the Output-Off Output-On Open-Load Detect Threshold Voltage Range. As always, system level thermal design and verification are important when outputs are paralleled.

FAULT LOGIC OPERATION

General

The Fault Status output (Pin 10) on the MC33293A reports any one of three possible faults from any one of the four outputs. The three possible faults are output-on open-load Fault, output-off open-load Fault and over-current Fault. All faults from any of the four outputs are OR’d together and reported by the single Fault Status output-on Pin 10 (Figure 13).

Figure 13. MC33293A Fault Logic Diagram



Output-On open-load Fault

The MC33293A always checks for an open-load on the outputs whether the outputs are ON or OFF. An output-on open-load Fault is detected if an open-load exists when the output is ON (corresponding input at a logic high state). The output-on open-load Fault detection occurs when the load current is less than the minimum Output-On Open-Load Detect current ($I_{Oon(th)}$), specified in this data sheet. The value of $I_{Oon(th)}$ is, typically, 75 mA at room temperature. See Figure 3.

The minimum load resistance value that the MC33293A will interpret as an output-on open-load ($R_{open(on)}$) is a function of; the Output-On Open-Load Detect current ($I_{Oon(th)}$); the load supply voltage (V_{load}); and the resistance of the output ($R_{DS(on)}$), as shown below.

$$R_{open(on)} = [V_{load} / I_{Oon(th)}] - R_{DS(on)} \approx V_{load} / I_{Oon(th)} \tag{1}$$

Using Equation 1 for the steady state case,

when: $V_{load} = 14\ V$
$R_{DS(on)} = 0.3\ \Omega$
$I_{Oon(th)} = 75\ mA$

an output-on open-load Fault will be detected and reported whenever $R_{load} \geq 187\ \Omega$.

Each output has an output-on open-load fault detect circuit that performs real time load current monitoring. Load current is monitored immediately after any output is turned ON. Since it takes a finite amount of time for load current to begin, the MC33293A detects an output-on open-load Fault from the time the output is turned ON until the load current exceeds the Output-On Open-Load Detect current ($I_{Oon(th)}$). It is important to note that a fault will *not* be reported at the Fault Status output during this short period of time. This is due to the built-in output-on open-load Fault Status Delay Time (t_{oson}), see Figure 3. This delay time is incorporated in the MC33293A to mask the reporting of a false output-on open-load Fault at the Fault Status output. The delay is typically 2.2 ms.

The purpose for the $t_{os(on)}$ delay is to prevent false fault reporting, especially when driving inductive loads. The load inductance causes a current lag when the load is turned ON. The normal current lag of an inductive load could be misinterpreted as an open-load if it weren't for the built-in delay. This delay or masking is accomplished internally with a single timer which resets every time any input switches from a low-to-high logic state. An output-on open-load Fault will be reported by the Fault Status output as a result of turning ON an output having an open-load Fault and the most recent $t_{os(on)}$ is allowed to lapse after switching ON any input.

The time it takes the load current to reach $I_{Oon(th)}$ is a function of the load resistance (R_{load}); load inductance (L_{load}); output on resistance ($R_{DS(on)}$); load supply voltage (V_{load}); and the turn-on time (t_{on}) as shown below. The value of t_{on} is comprised of the low-to-high V_{in} propagation delay time ($t_{on(dly)}$), and the output voltage rise time (t_r). See Figure 2.

$$t_{on(false\ fault)} = -\tau\ \ln [(I_{Oon(th)} - I_{load})/(-I_{load})] + t_{on} \tag{2}$$

where: $\tau = L_{load} / R_{load}$ = time constant (3)

$$I_{load} = V_{load} / [R_{load} + R_{DS(on)}] \tag{4}$$

$$t_{on} = t_{on(dly)} + t_r \tag{5}$$

Using Equation 2 for the transient case,

when: $V_{load} = 14\ V$
$R_{DS(on)} = 0.3\ \Omega$
$L_{load} = 10\ mH$
$R_{load} = 14\ \Omega$
$I_{Oon(th)} = 75\ mA$

an output-on open-load Fault will be detected, but not reported after initial turn ON for a duration of 57 µs + t_{on}.

Output-Off open-load Fault

The MC33293A checks for open-loads on the outputs regardless of an output being on or off. An output-off open-load Fault is detected if an open-load exists when the output is turned OFF (corresponding input at a logic low state). When any one of the four outputs are turned OFF, an independent internal current source tied to each output tries to pull a small amount of zero input voltage drain current ($I_{DS(off)}$, typically 23 µA), through the load. If, while this zero input voltage drain current is being pulled through the load, the output voltage is less than the output-off open-load Detect Threshold Voltage ($V_{Ooff(th)}$, typically 3.7 V), an output-off open-load Fault will be detected.

The zero input voltage drain current could be provided by a large external resistor connected from the output to ground. However, if an external resistor were used to provide this zero input voltage drain current, only "opens" resulting from open-loads or output to ground shorts could be detected. The external resistor could *not* guarantee detection of an open resulting from an output wire bond failure internal to the MC33293A. Because the current source is provided internally, open loads, output to ground shorts, and loss of output wire bonds will all be detected.

The value of load resistance that will be detected as an output-off open-load ($R_{open(off)}$), is a function of the zero input voltage drain current ($I_{DS(off)}$); the load supply voltage (V_{load}); and the output-off open-load Detect Threshold Voltage ($V_{Ooff(th)}$), as shown next by:

$$R_{open(off)} = \frac{[V_{load} - V_{Ooff(th)}]}{I_{DS(off)}} \tag{6}$$

Using Equation 6 for the steady state case,

when: $V_{load} = 14\ V$
$I_{DS(off)} = 23\ \mu A$
$V_{Ooff(th)} = 3.7\ V$

an output-off open-load Fault will be detected and reported whenever $R_L \geq 448\ k\Omega$.

Each output has an output-off open-load fault detect circuit that performs real time output voltage monitoring. Output voltage is monitored immediately after any output is turned off. A finite amount of time is required for output voltage to rise. The MC33293A detects an output-off open-load Fault from when an output is turned off until the output voltage exceeds the output-off open-load Detect Threshold Voltage ($V_{Ooff(th)}$). It is important to note a fault will *not* be reported at the Fault Status output during this rise time. This is due to the built-in output-off open-load Fault Status Delay Time, $t_{os(off)}$, see Figure 4. This delay time is incorporated in the MC33293A to delay the reporting of an output-off open-load Fault at the Fault Status Output. The delay is typically 19 µs.

The purpose for the $t_{os(off)}$ delay is to prevent false fault reporting experienced with capacitance type loads. The load capacitance causes the rise in output voltage to lag even after the load has been turned OFF. The normal voltage lag caused by load capacitance could be misinterpreted as an open-load if it weren't for the built-in delay. This delay, or masking, is accomplished with four separate timers that reset independent of each other when the corresponding input is switched from a high to a low logic state. Internal logic prevents an output-off open-load Fault from being reported at the Fault pin when any input is high. An output-off open-load Fault will be reported at the Fault Status pin after an open load occurs, all inputs not corresponding to the faulted output are low and a time in excess of $t_{os(off)}$ is exceeded after switching OFF the input corresponding to the faulted output.

An important note that bears repeating is that an output-off open-load Fault will not be reported at the Fault Status pin unless all input pins are at a logic low state (Figure 13). This is a Fault Status interrogation feature. It helps in distinguishing between an output-on open-load Fault and an output-on over-current Fault. (Fault Status interrogation is explained in greater detail in a later section).

The time the output voltage takes to reach $V_{Ooff(th)}$ after being turned OFF is $t_{off\ false\ fault}$. It is a function of the load resistance (R_{load}); load inductance (L_{load}); load current (I_{load}); output-on resistance ($R_{DS(on)}$), output capacitance (C_O); load supply voltage (V_{load}); and the turn OFF time (t_{off}). The value of t_{off} is comprised of the V_{in} high-to-low propagation delay time ($t_{off(dly)}$), and the output voltage fall time (t_f).

For the case when:

$$1/2\ L_{load}\ (I_{load})^2 >> 1/2\ C_O\ (V_{Ooff(th)})^2 \qquad (7)$$

$$t_{off\ false\ fault} = [(C_O\ \Delta V)\ /\ I_{load}] + t_{off} \qquad (8)$$

where: $$I_{load} = V_{load}\ /\ [R_{load} + R_{DS(on)}] \qquad (9)$$

$$\Delta V = V_{Ooff(th)} - [I_{load}\ R_{DS(on)}] \qquad (10)$$

$$t_{off} = t_{off(dly)} + t_f \qquad (11)$$

Using Equation 7 for the transient case,

when: $V_{load} = 14$ V
$R_{DS(on)} = 0.3\ \Omega$
$L_{load} = 10$ mH
$R_{load} = 14\ \Omega$
$C_O = 0.001\ \mu F$
$V_{Ooff(th)} = 3.7$ V

an Output-Off open-load Fault will be detected but not reported after initial turn OFF for a duration of 3.5 ns + t_{off}. From Equation 7, the energy stored in the load inductor will be 4.8 mJ. This is much greater than the 68 nJ needed to charge the output capacitance. This allows the use of Equation 8 in determining the false output-off open-load Fault duration following turn OFF because it assures that the output capacitance will be charged by the energy stored in the load inductance.

Over-Current Fault

An over-current (short circuit or current limit) Fault is the detection and reporting of any output over-current condition. An over-current condition is defined as a condition where load current exceeds the internal current limit value (typically 4.0 A). An over-current condition activates the current limit circuit. This circuit then sends an analog signal to the gate control circuit, lowering the voltage on the output transistor's gate. Lowering the gate voltage forces the output transistor to transition from the resistive (fully enhanced) mode of operation to the current limit (between fully enhanced and fully OFF) mode.

The actual detection of an over-current condition does not occur at the initial onset of current limit. The onset of current limit causes the voltage on the affected output to increase. The actual Over-Current detection occurs when the output voltage increases and exceeds the over-current Detect Voltage Threshold ($V_{OC(limit)}$, typically 3.7 V), while the corresponding input signal is in a logic high state.

After detection, the reporting of an over-current Fault at the Fault Status output is delayed by a time equal to the over-current Sense Time (t_{oc}), see Figures 5 and 6. This delay time is typically 55 µs. If the over-current condition no longer exists after the over-current Sense Time has passed, then no fault is reported. The purpose of the Fault reporting delay is to blank any false faults that might be reported due to high inrush current loads such as incandescent lamps. If the over-current condition still exists after the delay time has passed, then a fault will be reported at the Fault Status output and the affected output is turned OFF.

The Over-Current Sense Time is accomplished internally with four separate timers that reset and start independent of each other whenever a corresponding output is turned ON, either due to the corresponding input turning ON or the completion of the over-current Refresh Time (t_{ref}) explained in the next paragraph, (see Figures 5 and 6). An over-current Fault will be reported at the Fault Status output when an over-current condition is detected and a lapse time in excess of t_{oc} is exceeded after turning ON the affected output.

At the same time the over-current Fault is reported, a single internal over-current refresh timer resets, causing *any* over-current outputs to be turned OFF for a duration of t_{ref}, typically 3.6 ms. After a time t_{ref}, the faulted output(s) will be turned ON again to check if the over-current condition still exists. If the over-current condition still exists, the output(s) will be turned OFF again after a time t_{oc}. This periodic retry continues turning ON and OFF over-current loads at a duty cycle of $t_{oc}\ /(t_{oc} + t_{ref})$ with a period of $t_{oc} + t_{ref}$ until either the input is turned OFF or the over-current condition is removed. Any subsequent over-current conditions will reset and restart the t_{ref} timer.

Detection of an over-current condition coincides with, but does not occur until after the onset of current limit. This allows a specific but small current limit range to go undetected. The factors that determine the value of load resistance causing an over-current condition to be detected are: the Output-Load Current Limit [$I_{DS(limit)}$]; load voltage (V_{load}); and the Over-Current Detect Threshold Voltage [$V_{OC(limit)}$] as shown below:

$$R_{load(detect)} = \frac{[V_{load} - V_{OC(limit)}]}{I_{DS(limit)}} \qquad (12)$$

The factors that determine the value of load resistance that will cause the onset of current limit are: $I_{DS(limit)}$, V_{load}, and $R_{DS(on)}$, as shown below.

$$R_{load(limit)} = [V_{load} / I_{DS(limit)}] – R_{DS(on)} \quad (13)$$

For the case when: $V_{load} = 14\ V$
$V_{OC(limit)} = 3.7\ V$
$R_{DS(on)} = 0.3\ \Omega$
$I_{DS(limit)} = 4.0\ A$

an over-current condition will be detected for any load resistance such that $R_{load} \le 2.6\ \Omega$. An undetected current limit condition will occur any time $2.6\ \Omega \le R_{load} \le 3.2\ \Omega$. Notice that the undetected current limit range is quite small.

Fault Interrogation

Even though the MC33293A incorporates a single Fault Status Output pin for reporting three different fault conditions, a real time interrogation routine can be used to determine which one of the three Fault conditions is being reported and which single output is affected.

An important point to note about Fault interrogation is that only one fault on a single output can be interpreted. In other woRDS, if more than one over-current or open-load Fault exists among the four outputs, it is *not* possible to distinguish which outputs have a fault and which do not. It is very unlikely, however, that more than one output will be faulted at the same time.

When a Fault is reported, the first step is to determine if it is an over-current or open-load Fault ($R_{load} \ge 447\ k\Omega$, typical). This is done by taking all the inputs (single or dual) to a logic low state. If the Fault Status resets (changes to a logic high state) after the Fault Status Reset Delay Time ($t_{s(reset)}$, see Figure 4) has lapsed, then an over-current Fault is being reported. If the Fault Status does not reset (remains at a logic low state) after $t_{s(reset)}$ has lapsed, then an open-load Fault ($R_{load} \ge 447\ k\Omega$, typical) is being reported. This type of interrogation is possible because an output-off open-load Fault can only be reported when all the inputs are in a logic low state.

For an over-current Fault, the next step is to determine which single output is affected. After all inputs are turned OFF and the fault status resets, each input is then turned ON then OFF sequentially. A Fault will again be reported when the input to the corresponding Over-Current output is turned ON and $t_{os(on)}$ has lapsed. If the dual input mode is being used, an over-current Fault can only be interrogated down to the two outputs being driven together.

For an open-load Fault ($R_{load} \ge 447\ k\Omega$, typical) interrogation, all inputs are turned OFF and the fault status remains set. Each input is then turned ON and OFF sequentially. The Fault status will remain set when the input to the corresponding faulted output is turned ON and $t_{os(on)}$ has lapsed. If the dual input mode is used, an open-load Fault can only be interrogated down to the two outputs driven together.

From the example following Equation 1, the typical value of $R_{open(on)}$ is 187 Ω. From the example following Equation 6, the typical value of $R_{open(off)}$ is 447 kΩ. Therefore, if the load resistance is between 187 Ω and 447 kΩ typically, an output-on open-load Fault will be reported at the Fault Status output but an output-off open-load Fault will not. This condition is referred to as a *soft open fault*. If a soft open fault exists, it is reported at the Fault Status output the same as an over-current Fault except for the reporting delay time. A soft open fault has a reporting delay time of 2.2 ms typically, and an over-current Fault has a reporting delay time of only 55 µs typically, after the input to the faulted output is turned ON.

Figure 14. Truth Table

	Inputs							Outputs				
Conditions of Outputs	**1**	**2**	**3**	**4**	**$\overline{\text{S}}$/D**	**1 & 2**	**3 & 4**	**1**	**2**	**3**	**4**	**$\overline{\text{Fault}}$**
Non-Faulted Operation	L	L	L	L	L	X	X	H	H	H	H	H
	L	L	L	H	L	X	X	H	H	H	L	H
	L	L	H	L	L	X	X	H	H	L	H	H
	L	L	H	H	L	X	X	H	H	L	L	H
	L	H	L	L	L	X	X	H	L	H	H	H
	L	H	L	H	L	X	X	H	L	H	L	H
	L	H	H	L	L	X	X	H	L	L	H	H
	L	H	H	H	L	X	X	H	L	L	L	H
	H	L	L	L	L	X	X	L	H	H	H	H
	H	L	L	H	L	X	X	L	H	H	L	H
	H	L	H	L	L	X	X	L	H	L	H	H
	H	L	H	H	L	X	X	L	H	L	L	H
	H	H	L	L	L	X	X	L	L	H	H	H
	H	H	L	H	L	X	X	L	L	H	L	H
	H	H	H	L	L	X	X	L	L	L	H	H
	H	H	H	H	L	X	X	L	L	L	L	H
	X	X	X	X	H	L	L	H	H	H	H	H
	X	X	X	X	H	H	L	L	L	H	H	H
	X	X	X	X	H	L	H	H	H	L	L	H
	X	X	X	X	H	H	H	L	L	L	L	H
open-load Fault On Output 1	L	L	L	L	L	X	X	L	H	H	H	L
	H	L	L	L	L	X	X	L	H	H	H	L
	L	H	H	H	L	X	X	L	L	L	L	H*
	H	H	H	H	L	X	X	L	L	L	L	L
	X	X	X	X	H	L	L	L	H	H	H	L
	X	X	X	X	H	H	L	L	L	H	H	L
	X	X	X	X	H	L	H	L	H	L	L	H*
	X	X	X	X	H	H	H	L	L	L	L	L
Over-Current Fault On Output 1	L	L	L	L	L	X	X	H	H	H	H	H
	H	L	L	L	L	X	X	H	H	H	H	L
	L	H	H	H	L	X	X	H	L	L	L	H
	H	H	H	H	L	X	X	H	L	L	L	L
	X	X	X	X	H	L	L	H	H	H	H	H
	X	X	X	X	H	H	L	H	L	H	H	L
	X	X	X	X	H	L	H	H	H	L	L	H
	X	X	X	X	H	H	H	H	L	L	L	L

***NOTE:** All inputs must be a logic low state for an Output-Off open-load Fault to be reported.

MC33298

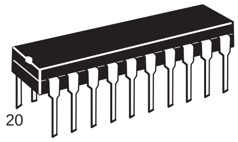
Octal Serial Switch with Serial Peripheral Interface I/O

OCTAL SERIAL SWITCH (SPI Input/Output)

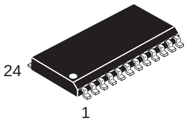
SEMICONDUCTOR TECHNICAL DATA

The MC33298 is an eight output low side power switch with 8 bit serial input control. The MC33298 is a versatile circuit designed for automotive applications, but is well suited for other environments. The MC33298 incorporates SMARTMOS™ technology, with CMOS logic, bipolar/MOS analog circuitry, and DMOS power MOSFETs. The MC33298 interfaces directly with a microcontroller to control various inductive or incandescent loads. The circuit's innovative monitoring and protection features are: very low standby current, cascadable fault reporting, internal 65 V clamp on each output, output specific diagnostics, and independent shutdown of outputs. The MC33298 is parametrically specified over a temperature range of $-40°C \le T_A \le +125°C$ ambient temperature and $9.0\ V \le V_{PWR} \le 16\ V$ supply. The economical 20 pin DIP and SO–24 wide body surface mount plastic packages make the MC33298 very cost effective.

- Designed to Operate Over Wide Supply Voltages of 5.5 V to 26.5 V
- Interfaces Directly to Microprocessor Using SPI Protocol
- SPI Communication for Control and Fault Reporting
- 8–Bit Serial I/O is CMOS Compatible
- 3.0 A Peak Current Outputs with Maximum $R_{DS(on)}$ of 0.45 Ω at 25°C
- Outputs are Current Limited to 3.0 A to 6.0 A for Driving Incandescent Lamp Loads
- Output Voltages Clamped to 65 V During Inductive Switching
- Maximum Sleep Current (I_{PWR}) of 50 µA with $V_{DD} \le 2.0$ V
- Maximum of 4.0 mA I_{DD} During Operation
- Maximum of 2.0 mA I_{PWR} During Operation with All Outputs "On"
- Open Load Detection (Outputs "Off")
- Overvoltage Detection and Shutdown
- Each Output has Independent Over Temperature Detection and Shutdown
- Output Mode Programmable for Sustained Current Limit or Shutdown
- Short Circuit Detect and Shutdown with Automatic Retry for Every Write Cycle
- Serial Operation Guaranteed to 2.0 MHz



P SUFFIX
PLASTIC PACKAGE
CASE 738
DIP (16+2+2)



DW SUFFIX
PLASTIC PACKAGE
CASE 751E
SOP (16+4+4)L

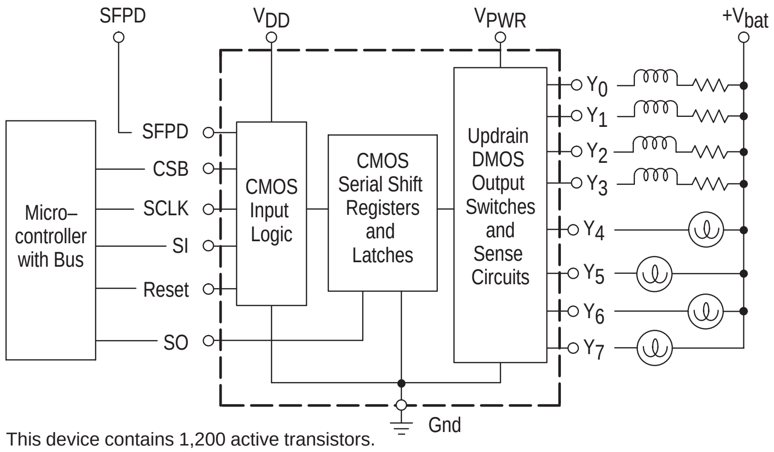
PIN CONNECTIONS

DIP	Function	SOP–24L
1	Output 7	1
2	Output 6	2
3	SCLK	3
4	SI	4
5	Ground	5
6	Ground	6
–	Ground	7
–	Ground	8
7	SO	9
8	CSB	10
9	Output 5	11
10	Output 4	12
11	Output 3	13
12	Output 2	14
13	SFPD	15
14	V_{DD}	16
15	Ground	17
16	Ground	18
–	Ground	19
–	Ground	20
17	V_{PWR}	21
18	Reset	22
19	Output 1	23
20	Output 0	24

ORDERING INFORMATION

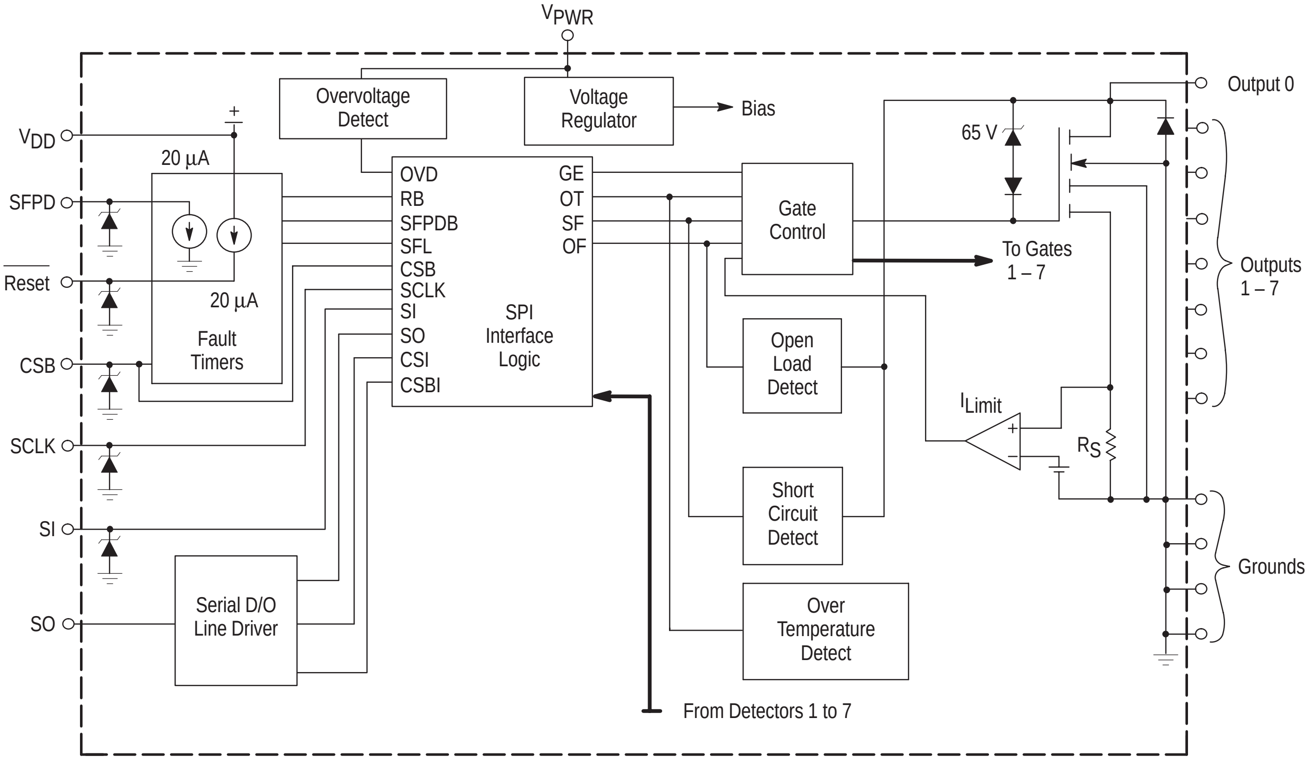
Device	Tested Operating Temperature Range	Package
MC33298P	$T_C = -40°$ to $+125°C$	DIP
MC33298DW		SOP–24L

Simplified Application



This device contains 1,200 active transistors.

Figure 1. Simplified Block Diagram



FAULT OPERATION

SERIAL OUTPUT (SO) PIN REPORTS

Overvoltage	Overvoltage condition reported.
Over Temperature	Fault reported by Serial Output (SO) pin.
Over Current	SO pin reports short to battery/supply or over current condition.
Output “On,” Open Load Fault	Not reported.
Output “Off,” Open Load Fault	SO pin reports output “off” open load condition.

DEVICE SHUTDOWNS

Overvoltage	Total device shutdown at V_{PWR} = 28–36 V. Re–operates when overvoltage is removed with all outputs assuming an off state upon recovery from overvoltage. All device registers are automatically reset (cleared) during shutdown.
Over Temperature	Only the output experiencing an over temperature shuts down.
Over Current	Only the output experiencing an over current condition shuts down at 3.0 A to 6.0 A after a 25 µs to 100 µs delay, with SFPD pin grounded. All outputs will continue to operate in a current limit mode, with no shutdown, if the SPFD pin is at 5.0 V.

MAXIMUM RATINGS (All voltages are with respect to ground, unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage			
Steady–State	$V_{PWR(sus)}$	–1.5 to 26.5	V
Transient Conditions (Note1)	$V_{PWR(pk)}$	–13 to 60	V
Logic Supply Voltage (Note 2)	V_{DD}	– 0.3 to 7.0	V
Input Pin Voltage (Note 3)	V_{IN}	– 0.3 to 7.0	V
Output Clamp Voltage (Note 4)	$V_{OUT(off)}$		V
(2.0 mA ≤ I_{out} ≤ 0.5 A)		50 to 75	
Output Self–Limit Current	$I_{OUT(lim)}$	3.0 to 6.0	A
Continuous Per Output Current (Note 5)	$I_{OUT(cont)}$	1.0	A
ESD Voltage			
Human Body Model (Note 6)	V_{ESD1}	2000	V
Machine Model (Note 7)	V_{ESD2}	200	V
Output Clamp Energy (Note 8)	E_{clamp}		
Repetitive:			
T_J = 25°C		100	mJ
T_J = 125°C		30	mJ
Non–Repetitive:			
T_J = 25°C		2.0	J
T_J = 125°C		0.5	J
Recommended Frequency of SPI Operation (Note 9)	f_{SPI}	2.0	MHz
Storage Temperature	T_{stg}	– 55 to +150	°C
Operating Case Temperature	T_C	– 40 to +125	°C
Operating Junction Temperature	T_J	– 40 to +150	°C
Power Dissipation (T_A = 25°C) (Note 10)	P_D	3.0	W
Soldering Temperature (for 10 seconds)	T_{solder}	260	°C
Thermal Resistance, Junction–to–Ambient (Note 11)	$R_{\theta JA}$		°C/W
Plastic Package, Case 738:			
All Outputs “On” (Note 12)		31	
Single Output “On” (Note 13)		37	
SOP–24 Package, Case 751E:			
All Outputs “On” (Note 12)		34	
Single Output (Note 13)		40	

NOTES:
1. Transient capability with external 100 Ω resistor connected in series with V_{PWR} pin and supply.
2. Exceeding these limits may cause a malfunction or permanent damage to the device.
3. Exceeding voltage limits on SCLK, SI, CSB, SFPD, or Reset pins may cause permanent damage to the device.
4. With output “off.”
5. Continuous output rating so long as maximum junction temperature is not exceeded. (See Figure 21 and 22 for more details).
6. ESD1 testing is performed in accordance with the Human Body Model (C_{Zap} = 100 pF, R_{Zap} = 1500 Ω).
7. ESD2 testing is performed in accordance with the Machine Model (C_{Zap} = 100 pF, R_{Zap} = 0 Ω).
8. Maximum output clamp energy capability at indicated Junction Temperature using single pulse method. See Figure 19 for more details.
9. Guaranteed and production tested for 2.0 MHz SPI operation but has been demonstrated to operate to 8.5 MHz @ 25°C.
10. Maximum power dissipation at indicated junction temperature with no heat sink used. See Figures 20, 21, and 22 for more details.
11. See Figure 20 for Thermal Model.
12. Thermal resistance from Junction–to–Ambient with all outputs “on” and dissipating equal power.
13. Thermal resistance from Junction–to–Ambient with a single output “on.”

STATIC ELECTRICAL CHARACTERISTICS (Characteristics noted under conditions of 4.5 V ≤ V_{DD} ≤ 5.5 V, 9.0 V ≤V_{PWR} ≤ 16 V, – 40°C ≤ T_C ≤ 125°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
POWER INPUT					
Supply Voltage Range Quasi–Functional (Note 1) Full Operational	 $V_{PWR(qf)}$ $V_{PWR(fo)}$	 5.5 9.0	 – –	 9.0 26.5	V
Supply Current (all Outputs “On,” I_{out} = 0.5 A) (Note 2)	$I_{PWR(on)}$	–	1.0	2.0	mA
Sleep State Supply Current (V_{DD} = 0.5 V)	$I_{PWR(ss)}$	–	1.0	50	µA
Sleep State Output Leakage Current (per Output, V_{DD} = 0.5 V)	$I_{OUT(ss)}$	–	–	50	µA
Overvoltage Shutdown	V_{OV}	28	–	36	V
Overvoltage Shutdown Hysteresis	$V_{OV(hys)}$	0.2	–	1.5	V
Logic Supply Voltage	V_{DD}	4.5	–	5.5	V
Logic Supply Current (with any combination of Outputs “On”)	I_{DD}	–	–	4.0	mA
Logic Supply Undervoltage Lockout Threshold (Note 3)	$V_{DD(uvlo)}$	2.0	–	4.5	V
POWER OUTPUT					
Drain–to–Source “On” Resistance (I_{out} = 0.5 A, T_J = 25°C) V_{PWR} = 5.5 V V_{PWR} = 9.0 V V_{PWR} = 13 V	$R_{DS(on)}$	 – – –	 – 0.4 0.35	 1.0 0.5 0.45	Ω
Drain–to–Source “On” Resistance (I_{out} = 0.5 A, T_J = 150°C) V_{PWR} = 5.5 V V_{PWR} = 9.0 V V_{PWR} = 13 V	$R_{DS(on)}$	 – – –	 – 0.75 0.65	 1.8 0.9 0.8	Ω
Output Self–Limiting Current Outputs Programmed “On”, V_{out} = 0.6 V_{DD}	$I_{OUT(lim)}$	 3.0	 4.0	 6.0	A
Output Fault Detect Threshold (Note 4) Output Programmed “Off”	$V_{OUTth(F)}$	 0.6	 0.7	 0.8	V_{DD}
Output “Off” Open Load Detect Current (Note 5) Output Programmed “Off,” V_{out} = 0.6 V_{DD}	I_{OCO}	 30	 50	 100	µA
Output Clamp Voltage 2.0 mA ≤ I_{out} ≤ 200 mA	V_{OK}	 50	 60	 75	V
Output Leakage Current (V_{DD} ≤ 2.0 V) (Note 6)	$I_{OUT(lkg)}$	– 50	0	50	µA
Over Temperature Shutdown (Outputs “Off”) (Note 7)	T_{LIM}	155	170	185	°C
Over Temperature Shutdown Hysteresis (Note 7)	$T_{LIM(hys)}$	–	10	20	°C

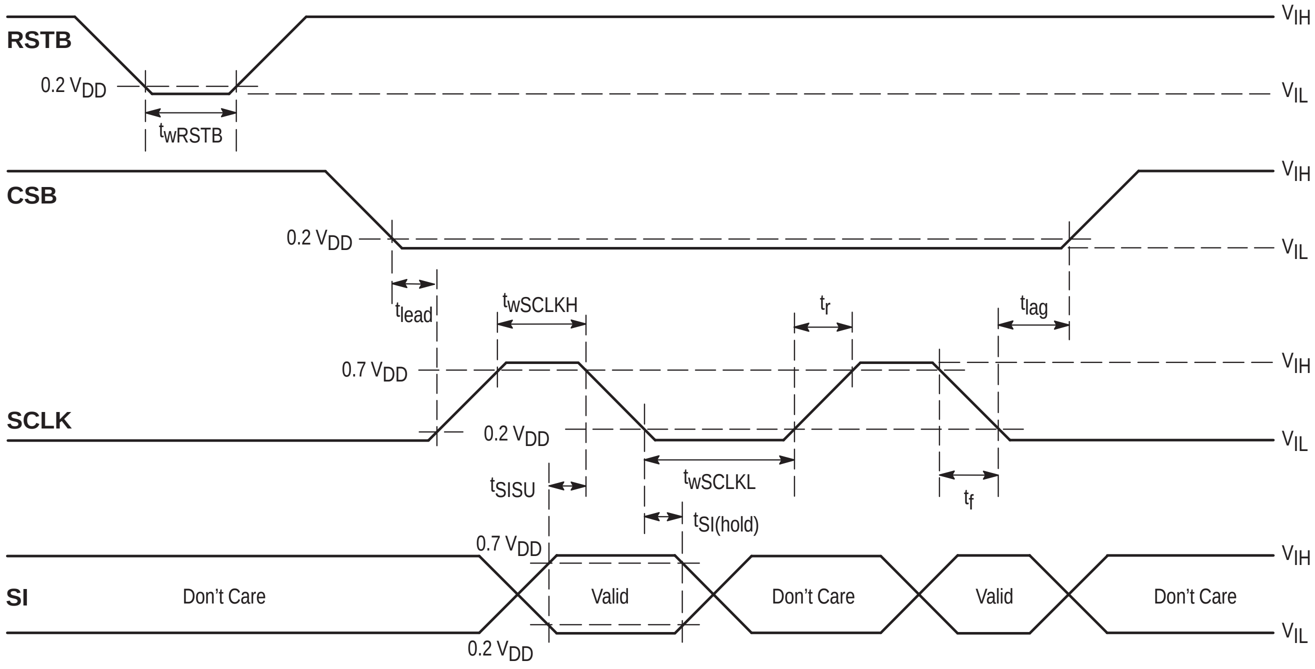
NOTES:
1. SPI inputs and outputs operational; Fault reporting may not be fully operational within this voltage range.
2. Value reflects normal operation (no faults) with all outputs “on.” Each “on” output contributes approximately 20 µA to I_{PWR}. Each output experiencing a “soft short” condition contributes approximately 0.5 mA to I_{PWR}. A “soft short” is defined as any load current causing the output source current to self–limit. A “hard” output short is a very low impedance short to supply.
3. For V_{DD} less than the Undervoltage Lockout Threshold voltage, all data registers are reset and all outputs are disabled.
4. Output fault detect threshold with outputs programmed “off.” Output fault detect thresholds are the same for output opens and shorts.
5. Output “Off” Open Load Detect Current is the current required to flow through the load for the purpose of detecting the existence of an open condition when the specific output is commanded to be “off.”
6. Output leakage current measured with output “off” and at 16 V.
7. This parameter is guaranteed by design but is not production tested.

STATIC ELECTRICAL CHARACTERISTICS (Characteristics noted under conditions of 4.5 V ≤ V_{DD} ≤ 5.5 V, 9.0 V ≤ V_{PWR} ≤ 16 V, – 40°C ≤ T_C ≤ 125°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
DIGITAL INTERFACE					
Input Logic High Voltage (Note 1)	V_{IH}	0.7	–	1.0	V_{DD}
Input Logic Low Voltage (Note 2)	V_{IL}	0.0	–	0.2	V_{DD}
Input Logic Voltage Hysteresis (Note 3)	$V_{I(hys)}$	50	100	500	mV
Input Logic Current (Note 4)	I_{IN}	–10	0	10	µA
Reset Pull–Up Current (Reset = 0.7 V_{DD})	I_{RSTB}	10	22	50	µA
SFPD Pull–Down Current (SFPD = 0.2 V_{DD})	I_{SFPD}	10	22	50	µA
SO High State Output Voltage (I_{OH} = 1.0 mA)	V_{SOH}	V_{DD} –1.0 V	V_{DD} – 0.6 V	–	V
SO Low State Output Voltage (I_{OL} = –1.6 mA)	V_{SOL}	–	0.2	0.4	V
SO Tri–State Leakage Current (CSB = 0.7 V_{DD}, 0 V ≤ V_{SO} ≤ V_{DD})	I_{SOT}	– 10	0	10	µA
Input Capacitance (0 V ≤ V_{DD} ≤ 5.5 V) (Note 5)	C_{IN}	–	–	12	pF
SO Tri–State Capacitance (0 V ≤ V_{DD} ≤ 5.5 V) (Note 6)	C_{SOT}	–	–	20	pF

NOTES: 1. Upper logic threshold voltage range applies to SI, CSB, SCLK, Reset, and SFPD input signals.
2. Lower logic threshold voltage range applies to SI, CSB, SCLK, Reset, and SFPD input signals.
3. Only the SFPD and Reset inputs have hysteresis. This parameter is guaranteed by design but is not production tested.
4. Input current of SCLK, SI, and CSB logic control inputs.
5. Input capacitance of SI, CSB, SCLK, Reset, and SFPD for 0 V ≤ V_{DD} ≤ 5.5 V. This parameter is guaranteed by design, but is not production tested.
6. Tri–state capacitance of SO for 0 V ≤ V_{DD} ≤ 5.5 V. This parameter is guaranteed by design but is not production tested.

Figure 2. Input Timing Switch Characteristics



DYNAMIC ELECTRICAL CHARACTERISTICS (Characteristics noted under conditions of 4.5 V ≤ V_{DD} ≤ 5.5 V, 9.0 V ≤ V_{PWR} ≤ 16 V, – 40°C ≤ T_C ≤ 125°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
POWER OUTPUT TIMING					
Output Rise Time (V_{PWR} = 13 V, R_L = 26 Ω) (Note 1)	t_r	0.4	1.5	20	µs
Output Fall Time (V_{PWR} = 13 V, R_L = 26 Ω) (Note 1)	t_f	0.4	2.5	20	µs
Output Turn “On” Delay Time (V_{PWR} = 13 V, R_L = 26 Ω) (Note 2)	$t_{dly(on)}$	1.0	5.0	15	µs
Output Turn “Off” Delay Time (V_{PWR} = 13 V, R_L = 26 Ω) (Note 3)	$t_{dly(off)}$	1.0	5.0	15	µs
Output Short Fault Disable Report Delay (Note 4) SFPD = 0.2 x V_{DD}	$t_{dly(sf)}$	25	50	100	µs
Output “Off” Fault Report Delay (Note 5) SFPD = 0.2 x V_{DD}	$t_{dly(off)}$	25	50	100	µs

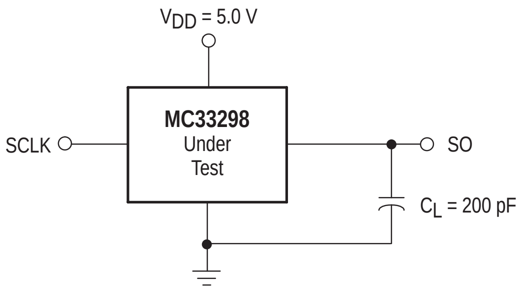
NOTES:
1. Output Rise and Fall time respectively measured across a 26 Ω resistive load at 10% to 90% and 90% to 10% voltage points.
2. Output Turn “On” Delay time measured from rising edge of CSB to 50% of output “off” V_{out} voltage with R_L = 26 Ω resistive load (see Figure 7 and 9).
3. Output Turn “Off” Delay time measured from rising edge of CSB to 50% of output “off” V_{out} voltage with R_L = 26 Ω resistive load (see Figure 7 and 9).
4. Output Short Fault Disable Report Delay measured from rising edge of CSB to I_{out} = 2.0 A point with output “on,” V_{out} = 5.0 V, and SFPD = 0.2 x V_{DD} (see Figure 8 and 10).
5. Output “Off” Fault Report Delay measured from 50% points of rising edge of CSB to rising edge of output (see Figure 9).

DYNAMIC ELECTRICAL CHARACTERISTICS (Characteristics noted under conditions of 4.5 V ≤ V_{DD} ≤ 5.5 V, 9.0 V ≤ V_{PWR} ≤ 16 V, – 40°C ≤ T_C ≤ 125°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
DIGITAL INTERFACE TIMING					
SCLK Clock Period (Note 6)	t_{pSCLK}	500	–	–	ns
SCLK Clock High Time	t_{wSCLKH}	175	–	–	ns
SCLK Clock Low Time	t_{wSCLKL}	175	–	–	ns
Required Low State Duration for Reset (V_{IL} ≤ 0.2 V_{DD}) (Note 1)	t_{wRSTB}	250	50	–	ns
Falling Edge of CSB to Rising Edge of SCLK (Required Setup Time)	t_{lead}	250	50	–	ns
Falling Edge of SCLK to Rising Edge of CSB (Required Setup Time)	t_{lag}	250	50	–	ns
SI to Falling Edge of SCLK (Required Setup Time)	t_{SISU}	125	25	–	ns
Falling Edge of SCLK to SI (Required Hold Time)	$t_{SI(hold)}$	125	25	–	ns
SO Rise Time (C_L = 200 pF)	t_{rSO}	–	25	75	ns
SO Fall Time (C_L = 200 pF)	t_{fSO}	–	25	75	ns
SI, CSB, SCLK Incoming Signal Rise Time (Note 2)	t_{rSI}	–	–	200	ns
SI, CSB, SCLK Incoming Signal Fall TIme (Note 2)	t_{fSI}	–	–	200	ns
Time from Falling Edge of CSB to SO					ns
Low Impedance (Note 3)	$t_{SO(en)}$	–	–	200	
HIgh Impedance (Note 4)	$t_{SO(dis)}$	–	–	200	
Time from Rising Edge of SCLK to SO Data Valid (Note 5) 0.2 V_{DD} ≤ SO ≥ 0.8 V_{DD}, C_L = 200 pF	t_{valid}	–	50	125	ns

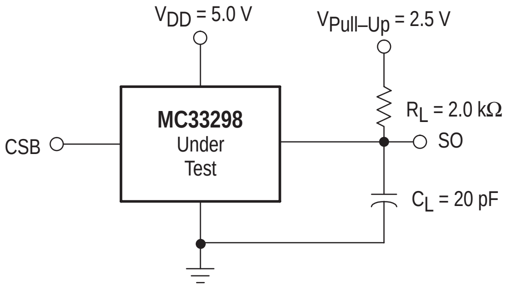
NOTES:
1. Reset Low duration measured with outputs enabled and going to “off” or disabled condition.
2. Rise and Fall time of incoming SI, CSB, and SCLK signals suggested for design consideration to prevent the occurrence of double pulsing.
3. Time required for output status data to be available for use at SO.
4. Time required for output status data to be terminated at SO.
5. Time required to obtain valid data out from SO following the rise of SCLK.
6. Clock period includes 75 ns rise plus 75 ns fall transition time in addition to clock high and low time.

Figure 3. Valid Data Delay Time and Valid Time Test Circuit



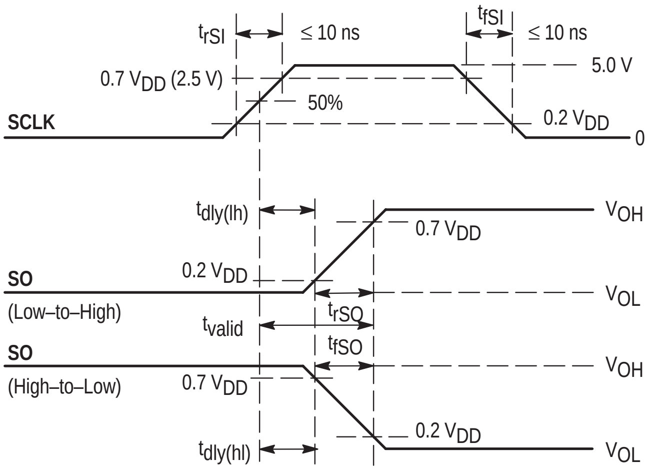
C_L represents the total capacitance of the test fixture and probe.

Figure 4. Enable and Disable Time Test Circuit



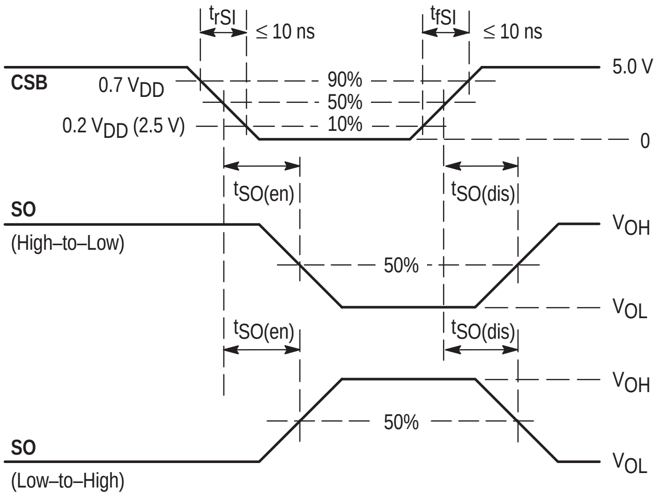
C_L represents the total capacitance of the test fixture and probe.

Figure 5. Vaild Data Delay Time and Valid Time Waveforms



SO (low–to–high) is for an output with internal conditions such that the low–to–high transition of CSB causes the SO output to switch from high–to–low.

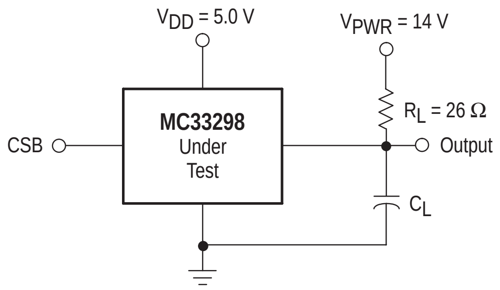
Figure 6. Enable and Disable Time Waveforms



NOTES: 1. SO (high–to–low) waveform is for SO output with internal conditions such that SO output is low except when an output is disabled as a result of detecting a circuit fault with CSB in a High Logic state (e.g., open load).

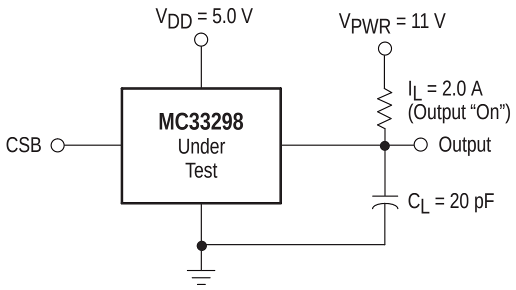
2. SO (low–to–high) waveform is for SO output with internal conditions such that SO output is high except when an output is disabled as a result of detecting a circuit fault with CSB in a High Logic state (e.g., shorted load).

Figure 7. Switching Time Test Circuit



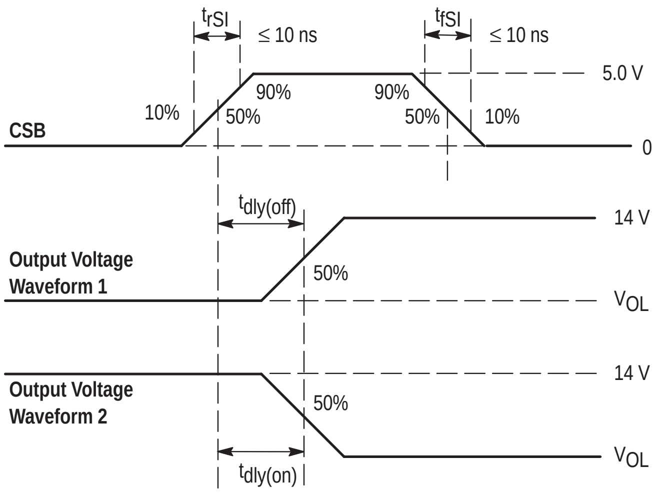
C_L represents the total capacitance of the test fixture and probe.

Figure 8. Output Fault Unlatch Disable Delay Test Circuit



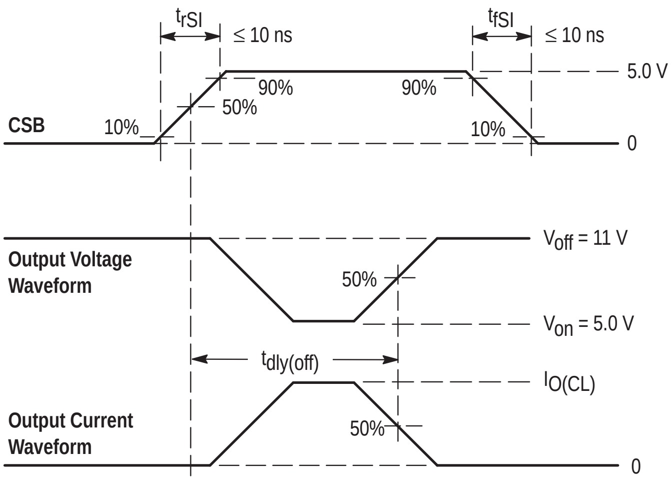
C_L represents the total capacitance of the test fixture and probe.

Figure 9. Turn–On/Off Waveforms



NOTES: 1. $t_{dly(on)}$ and $t_{dly(off)}$ are turn–on and turn–off propagation delay times.
2. Waveform 1 is an output programmed from an “on” to an “off” state.
3. Waveform 2 is an output programmed from an “off” to an “on” state.

Figure 10. Output Fault Unlatch Disable Delay Waveforms



NOTES: 1. $t_{pdly(off)}$ is the output fault unlatch disable propagation delay time required to correctly report an output fault after CSB rises. Represents an output commanded “on” while having an existing output short (overcurrent) to supply.
2. SFPD pin ≤ 0.2 V.

CIRCUIT DESCRIPTION

Introduction

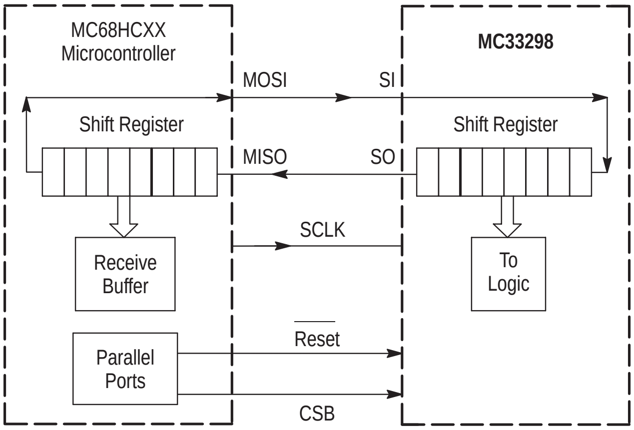
The MC33298 was conceived, specified, designed, and developed for automotive applications. It is an eight output low side power switch having 8–bit serial control. The MC33298 incorporates SMARTMOS™ technology having effective 2.0 µ CMOS logic, bipolar/MOS analog circuitry, and independent state of the art double diffused MOS (DMOS) power output transistors. Many benefits are realized as a direct result of using this mixed technology. A simplified block diagram of the MC33298 is shown in Figure 1.

Where bipolar devices require considerable control current for their operation, structured MOS devices, since they are voltage controlled, require only transient gate charging current affording a significant decrease in power consumption. The CMOS capability of the SMARTMOS™ process allows significant amounts of logic to be economically incorporated into the monolithic design. In addition, bipolar/MOS analog circuits embedded within the updrain power DMOS output transistors monitor and provide fast, independent protection control functions for each individual output. All outputs have internal 65 V at 0.5 A independent output voltage clamps to provide fast inductive turn–off and transient protection.

The MC33298 uses high efficiency updrain power DMOS output transistors exhibiting very low drain to source “on” resistance values ($R_{DS(on)} \leq 0.45\ \Omega$) and dense CMOS control logic. Operational bias currents of less than 4.0 mA (1.0 mA typical) with any combination of outputs “on” are the result of using this mixed technology and would not be possible with bipolar structures. To accomplish a comparable functional feature set using a bipolar structure approach would result in a device requiring hundreds of milliamperes of internal bias and control current. This would represent a very large amount of power to be consumed by the device itself and not available for load use.

In operation the MC33298 functions as an eight output serial switch serving as a microcontroller (MCU) bus expander and buffer with fault management and fault reporting features. In doing so, the device directly relieves the MCU of the fault management functions. The MC33298 directly interfaces to an MCU and operates at system clock serial frequencies in excess of 2.0 MHz using a Synchronous Peripheral Interface (SPI) for control and diagnostic readout. Figure 11 shows the basic SPI configuration between an MCU and one MC33298.

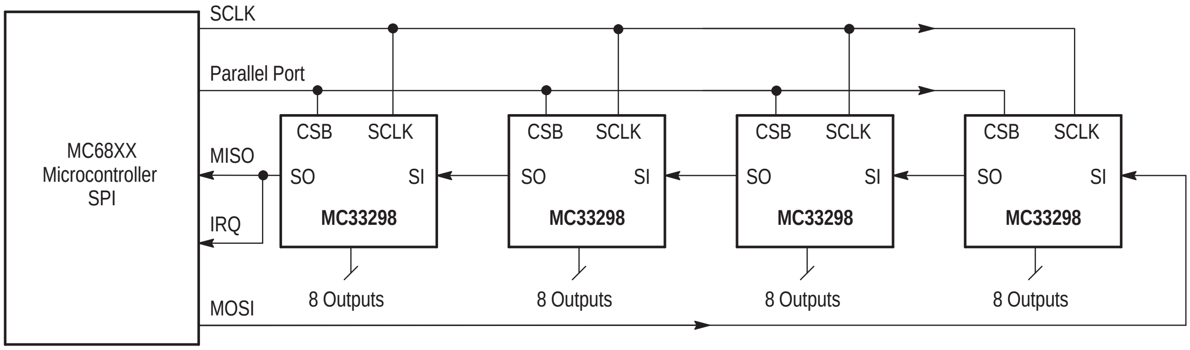
Figure 11. SPI Interface with Microcontroller



The circuit can also be used in a variety of other applications in the computer, telecommunications, and industrial fields. It is parametrically specified over an input “battery”/supply range of 9.0 V to 16 V but is designed to operate over a considerably wider range of 5.5 V to 26.5 V. The design incorporates the use of Logic Level MOSFETs as output devices. These MOSFETs are sufficiently turned “on” with a gate voltage of less than 5.0 V thus eliminating the need for an internal charge pump. Each output is identically sized and independent in operation. The efficiency of each output transistor is such that with as little as 9.0 V supply (V_{PWR}), the maximum $R_{DS(on)}$ of an output at room temperature is 0.45 Ω (0.35 Ω typical) and increases to only 1.0 Ω (0.5 Ω typical) as V_{PWR} is decreased to 5.5 V.

All inputs are compatible with 5.0 V CMOS logic levels and incorporate negative or inverted logic. Whenever an input is programmed to a logic low state (< 1.0 V) the corresponding low side switched output being controlled will be active low and turned “on.” Conversely, whenever an input is programmed to a logic high state (> 3.0 V), the output being controlled will be high and turned “off.”

Figure 12. MC33298 SPI System Daisy Chain



One main advantage of the MC33298 is the serial port which when coupled to an MCU, receives “on”/“off” commands from the MCU and in return transmits the drain status of the device’s output switches. Many devices can be “daisy–chained” together to form a larger system (see Figure 12). Note in this example that only one dedicated MCU parallel port (aside from the required SPI) is needed for chip select to control 32 possible loads.

Multiple MC33298 devices can also be controlled in a parallel input fashion using SPI (see Figure 13). This figure shows a possible 24 loads being controlled by only three dedicated parallel MCU ports used for chip select.

Figure 13. Parallel Input SPI Control

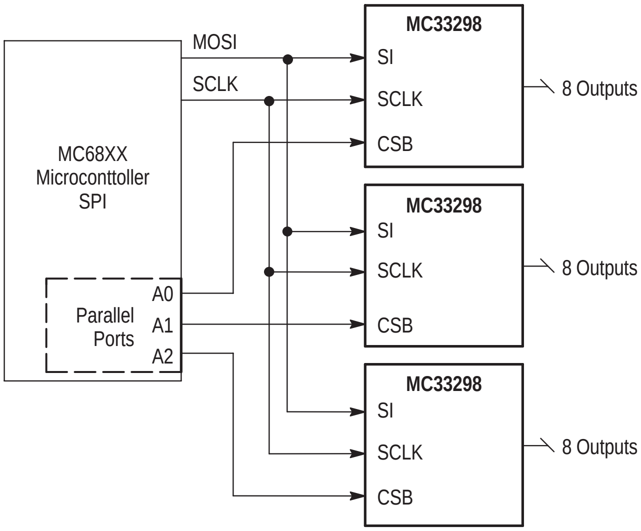


Figure 14 shows a basic method of controlling multiple MC33298 devices using two MCUs. A system can have only one master MCU at any given instant of time and one or more slave MCUs. The master MCU supplies the system clock signal (top MCU designated the master); the lower MCU being the slave. It is possible to have a system with more than one master but not at the same time. Only when the master is not communicating can a slave communicate. MCU master control is switched through the use of the slave select (SS) pin of the MCUs. A master will become a slave when it detects a logic low state on its SS pin.

These basic examples make the MC33298 very attractive for applications where a large number of loads need be controlled efficiently. The popular Synchronous Serial Peripheral Interface (SPI) protocol is incorporated, to this end, to communicate efficiently with the MCU.

SPI System Attributes

The SPI system is flexible enough to communicate directly with numerous standard peripherals and MCUs available from Motorola and other semiconductor manufacturers. SPI reduces the number of pins necessary for input/output (I/O) on the MC33298. It also offers an easy means of expanding the I/O function using few MCU pins. The SPI system of communication consists of the MCU transmitting, and in return, receiving one databit of information per clock cycle.

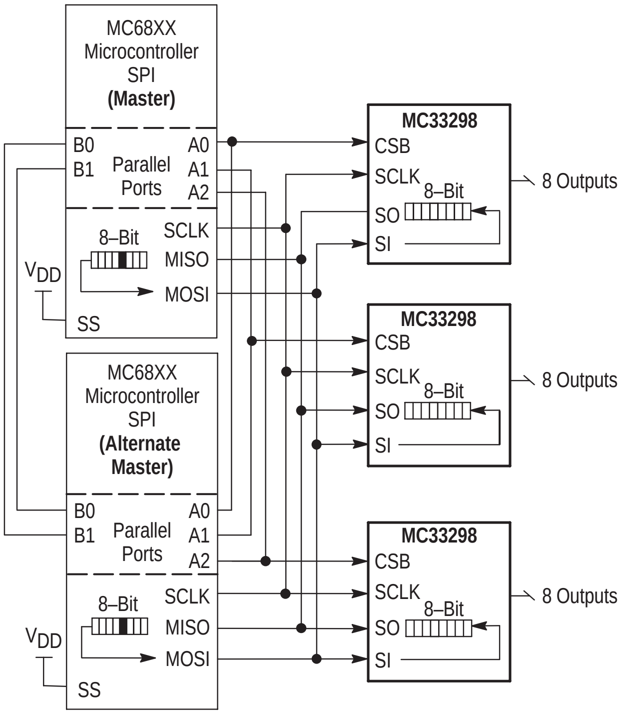
Databits of information are simultaneously transmitted by one pin, Microcontroller Out Serial In (MOSI), and received by another pin, Microcontroller In Serial Out (MISO), of the MCU.

Some features of SPI are:

- Full Duplex, Three–Wire Synchronous Data Transfer
- Each Microcontroller can be a Master or a Slave
- Provides Write Collision Flag Protection
- Provides End of Message Interrupt Flag
- Four I/Os associated with SPI (MOSI, MISO, SCLK, SS)

The only drawbacks to SPI are that an MCU is required for efficient operational control and, in contrast to parallel input control, is slower at performing pulse width modulating (PWM) functions.

Figure 14. Multiple MCU SPI Control



PIN FUNCTION DESCRIPTION

CSB Pin

The system MCU selects the MC33298 to be communicated with through the use of the CSB pin. Whenever the pin is in a logic low state, data can be transferred from the MCU to the MC33298 and vise versa. Clocked–in data from the MCU is transferred from the MC33298 shift register and latched into the power outputs on the rising edge of the CSB signal. On the falling edge of the CSB signal, drain status information is transferred from the power outputs and loaded into the device's shift register. The CSB pin also controls the output driver of the serial output pin. Whenever the CSB pin goes to a logic low state, the SO pin output driver is enabled allowing information to be transferred from the MC33298 to the MCU. To avoid any spurious data, it is essential that the high–to–low transition of the CSB signal occur only when SCLK is in a logic low state.

SCLK Pin

The system clock pin (SCLK) clocks the internal shift registers of the MC33298. The serial input pin (SI) accepts data into the input shift register on the falling edge of the SCLK signal while the serial output pin (SO) shifts data information out of the shift register on the rising edge of the SCLK signal. False clocking of the shift register must be avoided to guarantee validity of data. It is essential that the SCLK pin be in a logic low state whenever chip select bar pin (CSB) makes any transition. For this reason, it is recommended though not necessary, that the SCLK pin be kept in a low logic state as long as the device is not accessed (CSB in logic high state). When CSB is in a logic high state, any signal at the SCLK and SI pin is ignored and SO is tristated (high impedance). See the Data Transfer Timing diagram of Figure 16.

SI Pin

This pin is for the input of serial instruction data. SI information is read in on the falling edge of SCLK. A logic high state present on this pin when the SCLK signal rises will program a specific output "off," and in turn, turns "off" the specific output on the rising edge of the CSB signal. Conversely, a logic low state present on the SI pin will program the output "on," and in turn, turns "on" the specific output on the rising edge of the CSB signal. To program the eight outputs of the MC33298 "on" or "off," an eight bit serial stream of data is required to be entered into the SI pin starting with Output 7, followed by Output 6, Output 5, etc., to Output 0. For each rise of the SCLK signal, with CSB held in a logic low state, a databit instruction ("on" or "off") is loaded into the shift register per the databit SI state. The shift register is full after eight bits of information have been entered. To preserve data integrity, care should be taken to not transition SI as SCLK transitions from a low to high logic state.

SO Pin

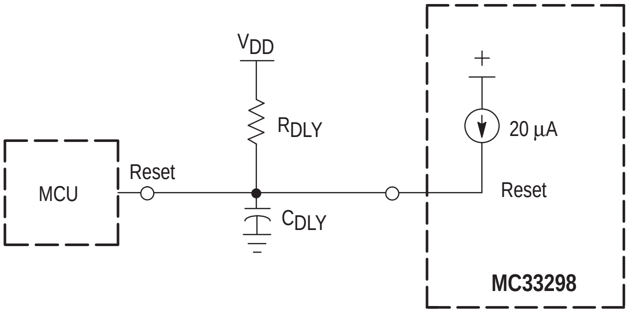
The serial output (SO) pin is the tri–stateable output from the shift register. The SO pin remains in a high impedance state until the CSB pin goes to a logic low state. The SO data reports the drain status, either high or low. The SO pin changes state on the rising edge of SCLK and reads out on the falling edge of SCLK. When an output is "off" and not faulted, the corresponding SO databit is a high state. When an output is "on," and there is no fault, the corresponding databit on the SO pin will be a low logic state. The SI/SO shifting of data follows a first–in–first–out protocol with both input and output words transferring the Most Significant Bit (MSB) first. The SO pin is not affected by the status of the Reset pin.

Reset Pin

The MC33298 Reset pin is active low and used to clear the SPI shift register and in doing so sets all output switches "off." With the device in a system with an MCU; upon initial system power up, the MCU holds the Reset pin of the device in a logic low state ensuring all outputs to be "off" until both the V_{DD} and V_{PWR} pin voltages are adequate for predictable operation. After the MC33298 is reset, the MCU is ready to assert system control with all output switches initially "off." If the V_{PWR} pin of the MC33298 experiences a low voltage, following normal operation, the MCU should pull the Reset pin low so as to shutdown the outputs and clear the input data register. The Reset pin is active low and has an internal pull–up incorporated to ensure operational predictability should the external pull–up of the MCU open circuit. The internal pull–up is only 20 µA to afford safe and easy interfacing to the MCU. The Reset pin of the MC33298 should be pulled to a logic low state for a duration of at least 250 ns to ensure reliable reset.

A simple power "on" reset delay of the system can be programmed through the use of an RC network comprised of a shunt capacitor from the Reset pin to Ground and a resistor to V_{DD} (See Figure 15). Care should be exercised to ensure proper discharge of the capacitor so as to not adversely delay the reset nor damage the MCU should the MCU pull the Reset line low and yet accomplish initialization for turn "on" delay. It may be easier to incorporate delay into the software program and use a parallel port pin of the MCU to control the MC33298 Reset pin.

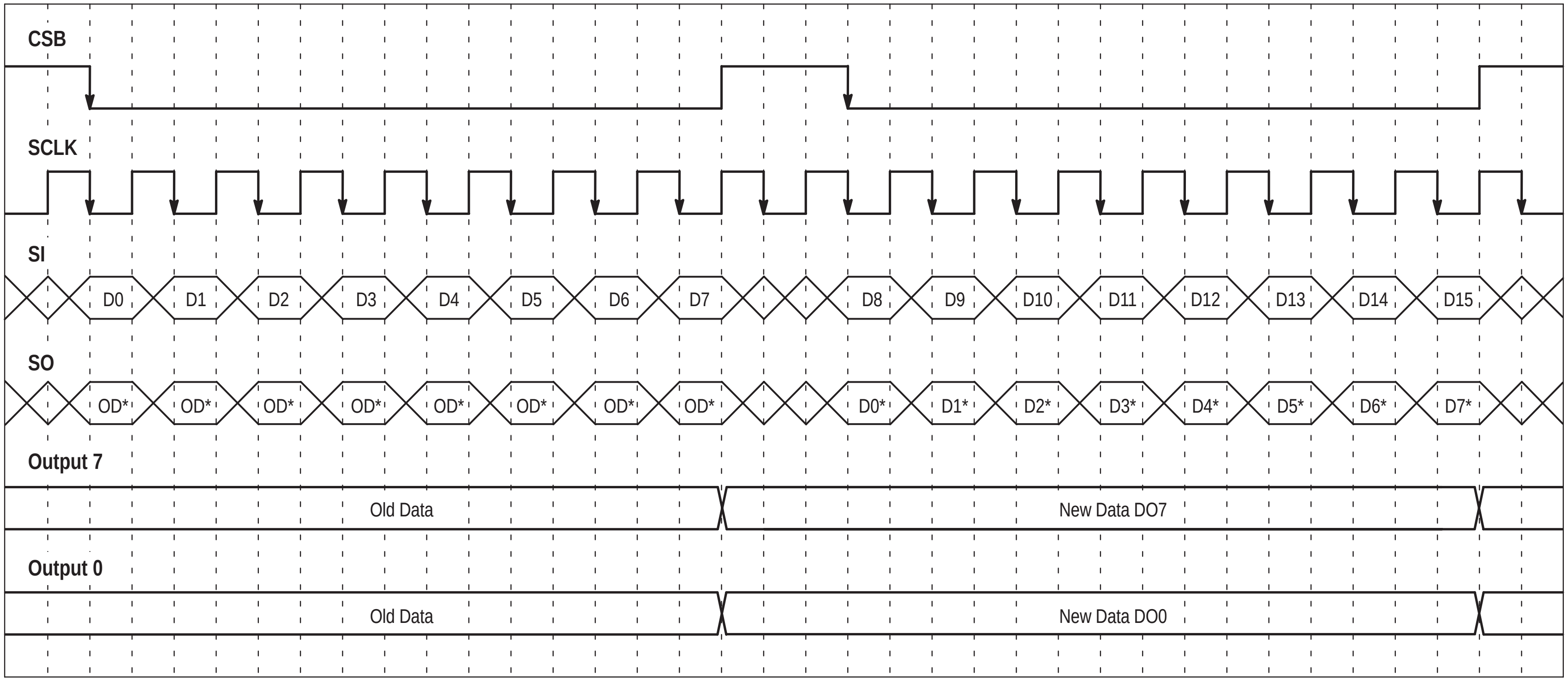
Figure 15. Power "On" Reset



SFPD Pin

The Short Fault Protect Disable (SFPD) pin is used to disable the over current latch–off. This feature allows control of incandescent loads where in–rush currents exceed the device's analog current limits. Essentially the SFPD pin determines whether the MC33298 output(s) will instantly shut down upon sensing an output short or remain "on" in a current limiting mode of operation until the output short is removed or thermal shutdown is reached. If the SFPD pin is tied to V_{DD} = 5.0 V the MC33298 output(s) will remain "on" in a current limited mode of operation upon encountering a load short to supply. If the SFPD pin is grounded, a short circuit will immediately shut down only the output affected. Other outputs not having a fault condition will operate normally. The short circuit operation is addressed in more detail later.

Figure 16. Data Transfer Timing



NOTES: 1. Reset pin is in a logic high state during the above operation.
2. D0, D1, D2, ..., and D15 relate to the ordered entry of program data into the MC33298 with D0/D8 bits (MSB) corresponding to Output 7 and D7/D15 corresponding to Output 0.
3. D0*, D1*, D2*, ..., and D7* relate to the ordered data out of the MC33298 with D0* bit (MSB) corresponding to Output 7.
4. OD* corresponds to Old Databits.
5. For brevity, only DO7 and DO0 are shown which respectively correspond to Output 7 and Output 0.

Data Transfer Timing (General)

CSB High–to–Low	SO pin is enabled. Output Status information transferred to Output Shift Register.
CSB Low–to–High	Data from the Shift Register is transferred to the Output Power Switches.
SO	Will change state on the rising edge of the SCLK pin signal.
SI	Will accept data on the falling edge of the SCLK pin signal.

Power Consumption

The MC33298P has extremely low power consumption in both the operating and standby modes. In the standby or “sleep” mode, with $V_{DD} \le 2.0$ V, the current consumed by the V_{PWR} pin is less than 50 µA. In the operating mode, the current drawn by the V_{DD} pin is less than 4.0 mA (1.0 mA typical) while the current drawn at the V_{PWR} pin is 2.0 mA maximum (1.0 mA typical). During normal operation, turning outputs “on” increases I_{PWR} by only 20 µA per output. Each output experiencing a “soft short” (overcurrent conditions just under the current limit), adds 0.5 mA to the I_{PWR} current.

Paralleling of Outputs

Using MOSFETs as output switches allows the connection of any combination of outputs together. MOSFETs have an inherent positive temperature coefficient thermal feedback which modulates $R_{DS(on)}$ providing balanced current sharing between outputs without destructive operation (bipolar outputs could not be paralleled in this fashion as thermal run–away would likely occur). The device can even be operated with all outputs tied together. This mode of operation may be desirable in the event the application requires lower power dissipation or the added capability of switching higher currents. Performance of parallel operation results in a corresponding decrease in $R_{DS(on)}$ while the Output Off Open Load Detect Currents and the Output Current Limits increase correspondingly (by a factor of eight if all outputs are paralleled). Less than 56 mΩ $R_{DS(on)}$ with current limiting of 24 to 48 A will result if all outputs are paralleled together. There will be no change in the Overvoltage detect or the “Off” Output Threshold Voltage Range. The advantage of paralleling outputs within the same MC33298 affords the existence of minimal $R_{DS(on)}$ and output clamp voltage variation between outputs. Typically, the variation of $R_{DS(on)}$ between outputs of the same device is less than is 0.5%. The variation in clamp voltages (which could affect dynamic current sharing) is less than 5%. Paralleling outputs from two or more devices is possible but not recommended. This is because there is no guarantee that the $R_{DS(on)}$ and clamp voltage of the two devices will match. System level thermal design analysis and verification should be conducted whenever paralleling outputs.

FAULT LOGIC OPERATION

General

The MCU can perform a parity check of the fault logic operation by comparing the command 8–bit word to the status 8–bit word. Assume that after system reset, the MCU first sends an 8–bit command word, Command Word 1, to the MC33298. Each output that is to be turned “on” will have its corresponding databit low. Refer to the Data Transfer Timing diagram of Figure 16. As this word, Command Word 1, is being written into the shift register of the MC33298, a status word is being simultaneously written out and received by the MCU. However, the word being received by the MCU is the status of the previous write word to the MC33298, Status Word 0. If the command word of the MCU is written a second time (Command Word 2 = Command Word 1), the word received by the MCU, Status Word 2, is the status of Command Word 1. The timing diagram shown in Figure 16 depicts this operation. Status Word 2 is then compared with Command Word 1. The MCU will Exclusive OR Status Word 2 with Command Word 1 to determine if the two words are identical. If the two words are identical, no faults exist. The timing between the two write words must be greater than 100 µs to receive proper drain status. The system databus integrity may be tested by writing two like words to the MC33298 within a few microseconds of each other.

Initial System Setup Timing

The MCU can monitor two kinds of faults:

(1) Communication errors on the data bus and

(2) Actual faults of the output loads.

After initial system start up or reset, the MCU will write one word to the MC33298. If the word is repeated within a few microseconds (say 5) of the first word, the word received by the MCU, at the end of the repeated word, serves as a confirmation of data bus integrity (1). At startup, the MC33298 will take 25 to 100 µs before a repeat of the first word can give the actual status of the outputs. Therefore, the first word should be repeated at least 100 µs later to verify the status of the outputs.

The SO of the MC33298 will indicate any one of four faults. The four possible faults are Over Temperature, Output Off Open Fault, Short Fault (overcurrent), and V_{PWR} Overvoltage Fault. All of these faults, with the exception of the Overvoltage Fault, are output specific. Over Temperature Detect, Output Off Open Detect, and Output Short Detect are dedicated to each output separately such that the outputs are independent in operation. A V_{PWR} Overvoltage Detect is of a “global” nature causing all outputs to be turned “off.”

Over Temperature Fault

Patent pending Over Temperature Detect and shutdown circuits are specifically incorporated for each individual output. The shutdown that follows an Over Temperature condition is independent of the system clock or any other logic signal. Each independent output shuts down at 155°C to 185°C. When an output shuts down due to an Over Temperature Fault, no other outputs are affected. The MCU recognizes the fault since the output was commanded to be “on” and the status word indicates that it is “off.” A maximum hysteresis of 20°C ensures an adequate time delay between output turn “off” and recovery. This avoids a very rapid turn “on” and turn “off” of the device around the Over Temperature threshold. When the temperature falls below the recovery level for the Over Temperature Fault, the device will turn “on” only if the Command Word during the next write cycle indicates the output should be turned “on.”

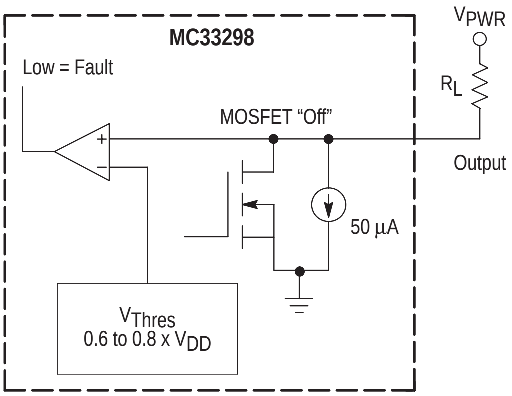
Overvoltage Fault

An Overvoltage condition on the V_{PWR} pin will cause the MC33298 to shut down all outputs until the overvoltage condition is removed and the device is re–programmed by the SPI. The overvoltage threshold on the V_{PWR} pin is specified as 28 V to 36 V with 1.0 V typical hysteresis. Following the overvoltage condition, the next write cycle sends the SO pin the hexadecimal word $FF (all ones) indicating all outputs are turned “off.” In this way, potentially dangerous timing problems are avoided and the MCU reset routine ensures an orderly startup of the loads. The MC33298 does not detect an overvoltage on the V_{DD} pin. Other external circuitry, such as the Motorola MC33161 Universal Voltage Monitor, is necessary to accomplish this function.

Output Off Open Load Fault

An Output Off Open Load Fault is the detection and reporting of an "open" load when the corresponding output is disabled (input in a logic high state). To understand the operation of the Open Load Fault detect circuit, see Figure 17. The Output Off Open Load Fault is detected by comparing the drain voltage of the specific MOSFET output to an internally generated reference. Each output has one dedicated comparator for this purpose.

Figure 17. Output "Off" Open Load Detect



An Output Off Open Load Fault is indicated when the output voltage is less than the Output Threshold Voltage (V_{Thres}) of 0.6 to 0.8 x V_{DD}. Since the MC33298 outputs function as switches, during normal operation, each MOSFET output should either be completely turned "on" or "off." By design the threshold voltage was selected to be between the "on" and "off" voltage of the MOSFET. During normal operation, the "on" state V_{DS} voltage of the MOSFET is less than the threshold voltage and the "off" state V_{DS} voltage is greater than the threshold voltage. This design approach affords using the same threshold comparator for Output Open Load Detect in the "off" state and Short Circuit Detect in the "on" state. See Figure 18 for an understanding of the Short Circuit Detect circuit. With V_{DD} = 5.0 V, an "off" state output voltage of less than 3.0 V will be detected as an Output Off Open Load Fault while voltages greater than 4.0 V will not be detected as a fault.

The MC33298 has an internal pull–down current source of 50 µA, as shown in Figure 17, between the MOSFET drain and ground. This prevents the output from floating up to V_{PWR} if there is an open load or internal wirebond failure. The internal comparator compares the drain voltage with a reference voltage, V_{Thres} (0.6 to 0.8 x V_{DD}). If the output voltage is less than this reference voltage, the MC33298 will declare the condition to be an open load fault.

During steady–state operation, the minimum load resistance (R_L) needed to prevent false fault reporting during normal operation can be found as follows:

$$V_{PWR} = 9.0\text{ V (min)}$$
$$I_{LCO} = 50\ \mu\text{A}$$
$$V_{Thres}\text{ (max)} = (0.8 \times 5.5)\text{V} = 4.4\text{ V}$$

Therefore, the load resistance necessary to prevent false open load fault reporting is (using Ohm's Law) equal to 92 kΩ or less.

During output switching, especially with capacitive loads, a false Output Off Open Load Fault may be triggered. To prevent this false fault from being reported an internal fault filter of 25 to 100 µs is incorporated. The duration for which a false fault may be reported is a function of the load impedance (R_L, C_L, L_L), $R_{DS(on)}$, and C_{out} of the MOSFET as well as the supply voltage, V_{PWR}. The rising edge of CSB triggers a built in fault delay timer which must time out (25 to 100 µs) before the fault comparator is enabled to detect a faulted threshold. The circuit automatically returns to normal operation once the condition causing the Open Load Fault is removed.

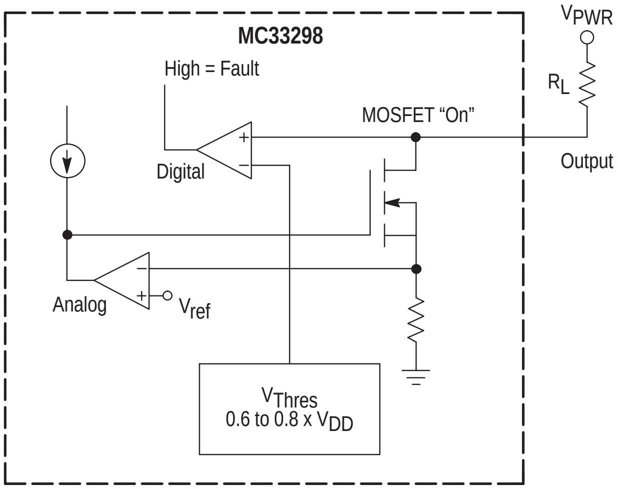
Shorted Load Fault

A shorted load (overcurrent) fault can be caused by any output being shorted directly to supply, or an output experiencing a current greater than the current limit.

There are three safety circuits progressively in operation during load short conditions which afford system protection: 1) The device's output current is monitored in an analog fashion using a SENSEFET™ approach and limited; 2) The device's output current limit threshold is sensed by monitoring the MOSFET drain voltage; and 3) The device's output thermal limit is sensed and when attained causes only the specific faulted output to be latched "off," allowing remaining outputs to operate normally. All three protection mechanisms are incorporated in each output affording robust independent output operation.

The analog current limit circuit is always active and monitors the output drain current. An overcurrent condition causes the gate control circuitry to reduce the gate to source voltage imposed on the output MOSFET which re–establishes the load current in compliance with current limit (3.0 to 6.0 A) range. The time required for the current limit circuitry to act is less than 20 µs. Therefore, currents higher than 3.0 to 6.0 A will never be seen for more than 20 µs (a typical duration is 10 µs). If the current of an output attempts to exceed the predetermined limit of 3.0 to 6.0 A (4.0 A nominal), the V_{DS} voltage will exceed the V_{Thres} voltage and the overcurrent comparator will be tripped as shown in Figure 18.

Figure 18. Short Circuit Detect and Analog Current Limiting Circuit



The status of SFPD will determine whether the MC33298 will shut down or continue to operate in an analog current limited mode until either the short circuit is removed or thermal shutdown is reached.

Grounding the SFPD pin will enable the short fault protection shutdown circuitry. Consider a load short (output short to supply) occurring on an output before, during, and after output turn "on." When the CSB signal rises to the high logic state, the corresponding output is turned "on" and a delay timer activated. The duration of the delay timer is 25 to 100 µs. If the short circuit takes place before the output is turned "on," the delay experienced is the entire 25 to 100 µs followed by shutdown. If the short occurs during the delay time, the shutdown still occurs after the delay time has elapsed. If the short circuit occurs after the delay time, shut– down is immediate (within 20 µs after sensing). The purpose of the delay timer is to prevent false faults from being reported when switching capacitive loads.

If the SFPD pin is at 5.0 V (or V_{DD}), an output will not be disabled when overcurrent is detected. The specific output will, within 5.0 to 10 µs of encountering the short circuit, go into an analog current limited mode. This feature is especially useful when switching incandescent lamp loads, where high in–rush currents experienced during startup last for 10 to 20 ms.

Each output of the MC33298 has its own overcurrent shutdown circuitry. Over temperature faults and the overvoltage faults are not affected by the SFPD pin.

Both load current sensing and output voltage sensing are incorporated for Short Fault detection with actual detection occurring slightly after the onset of current limit. The current limit circuitry incorporates a SENSEFET™ approach to measure the total drain current. This calls for the current through a small number of cells in the power MOSFET to be measured and the result multiplied by a constant to give the total current. Whereas output shutdown circuitry measures the drain to source voltage and shuts down if a threshold (V_{Thres}) is exceeded.

Short Fault detection is accomplished by sensing the output voltage and comparing it to V_{Thres}. The lowest V_{Thres} requires a voltage of 0.6 times 4.5 V (the minimum V_{DD} voltage) or 2.7 V to be sensed. For an enabled output, with $V_{DD} = 5.0 \pm 0.5$ V, an output voltage in excess of 4.4 V will be detected as a "short" while voltages less than 2.7 V will not be detected as "shorts."

Over Current Recovery

If the SFPD pin is in a high logic state, the circuit returns to normal operation automatically after the short circuit is removed (unless thermal shutdown has occurred).

If the SFPD pin is grounded and overcurrent shutdown occurs; removal of the short circuit will result in the output remaining "off" until the next write cycle. If the short circuit is not removed, the output will turn "on" for the delay time (25 to 100 µs) and then turn "off" for every write cycle commanding a turn "on."

SFPD Pin Voltage Selection

Since the voltage condition of the SFPD pin controls the activation of the short fault protection (i.e. shutdown) mode equally for all eight outputs, the load having the longest duration of in–rush current determines what voltage (state) the SFPD pin should be at. Usually if at least one load is, say an incandescent lamp, the in–rush current on that input will be milliseconds in duration. Therefore, setting SFPD at 5.0 V will prevent shutdown of the output due to the in–rush current. The system relies only on the Over Temperature Shutdown to protect the outputs and the loads. The MC33298 was designed to switch GE194 incandescent lamps with the SFPD pin in a grounded state. Considerably larger lamps can be switched with the SFPD pin held in a high logic state.

Sometimes both a delay period greater than 25 to 100 µs (current limiting of the output) followed by an immediate over current shutdown is necessary. This can be accomplished by programming the SFPD pin to 5.0 V for the extended delay period to afford the outputs to remain "on" in a current limited mode and then grounding it to accomplish the immediate shutdown after some period of time. Additional external circuitry is required to implement this type of function. An MCU parallel output port can be devoted to controlling the SFPD voltage during and after the delay period, is often a much better method. In either case, care should be taken to execute the SFPD start–up routine every time start–up or reset occurs.

Undervoltage Shutdown

An undervoltage V_{DD} condition will result in the global shutdown of all outputs. The undervoltage threshold is between 2.5 V and 4.5 V. When V_{DD} goes below the threshold, all outputs are turned "off" and the SO register is reset to indicate the same.

An undervoltage condition at the V_{PWR} pin will not cause output shutdown and reset. When V_{PWR} is between 5.5 V and 9.0 V, the outputs will operate per the command word. However, the status as reported by the serial output (SO) pin may not be accurate. Proper operation at V_{PWR} voltages below 5.5 V cannot be guaranteed.

Deciphering Fault Type

The MC33298 SO pin can be used to understand what kind of system fault has occurred. With eight outputs having open load, over current and over temperature faults, a total of 25 different faults are possible. The SO status word received by the MCU will be compared with the word sent to the MC33298 during the previous write cycle. If the two words are not the same, then the MCU should be programmed to determine which output or outputs are indicating faults. If the command bit for any of the output switches indicating a fault is high, the fault is an open load.

The eight open load faults are therefore the ones most easily detected. Over current and over temperature faults are often related. Turning the affected output switches "off" and waiting for some time should make these faults go away. Over current and over temperature faults can not be differentiated in normal application usage.

One advantage of the synchronous serial output is that multiple faults can be detected with only one pin (SO) being used for fault status indication.

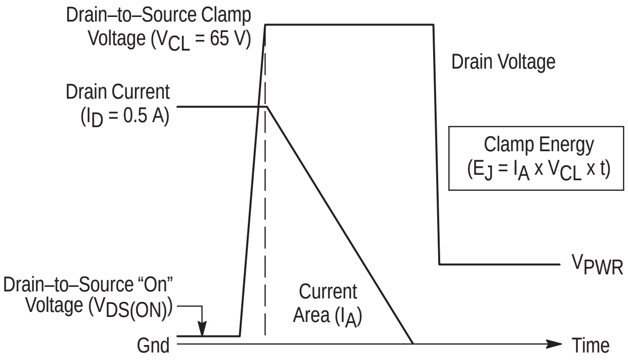
If V_{PWR} experiences an overvoltage condition, all outputs will immediately be turned "off" and remain latched "off." A new command word is required to turn the outputs back "on" following an overvoltage condition.

Output Voltage Clamping

Each output of the MC33298 incorporates an internal voltage clamp to provide fast turn–off and transient protection of the output. Each clamp independently limits the drain to source voltage to 65 V at drain currents of 0.5 A and keeps the output transistors from avalanching by causing the transient energy to be dissipated in the linear mode (see Figure 19). The total energy (E_J) can be calculated by multiplying the current area under the current curve (I_A) during the time the clamp is active and the clamp voltage (V_{CL}).

Characterization of the output clamps, using a single pulse repetitive method at 0.5 A, indicate the maximum energy to be 100 mJ at 25°C and 25 mJ at 125°C per output. Using a single pulse non–repetitive method at 0.5 A the clamps are capable of 2.0 Joules at 25°C and 0.5 Joules at 125°C.

Figure 19. Output Voltage Clamping



THERMAL CHARACTERIZATION

Thermal Model

Logic functions take up a very small area of the die and generate negligible power. In contrast, the output transistors take up most of the die area and are the primary contributors of power generation. The thermal model shown in Figure 20 was developed for the MC33298 mounted on a typical PC board. The model is accurate for both steady state and transient thermal conditions. The components R_{d0}, R_{d1}, R_{d2}, ..., and R_{d7} represent the steady state thermal resistance of the silicon die for transistor outputs 0, 1, 2, ..., and 7, while C_{d0}, C_{d1}, C_{d2}, ..., and C_{d7} represent the corresponding thermal capacitance of the silicon die transistor outputs and plastic. The device area and die thickness determine the values of these specific components.

The thermal impedance of the package from the internal mounting flag to the outside environment is represented by the terms R_{pkg} and C_{pkg}. The steady state thermal resistance of leads and the PC board make up the steady state package thermal resistance, R_{pkg}. The thermal capacitance of the package is made up of the combined capacitance of the flag and the PC board. The mold compound was not modeled as a specific component but is factored into the other overall component values.

The battery voltage in the thermal model represents the ambient temperature the device and PC board are subjected to. The I_{PWR} current source represents the total power dissipation and is calculated by adding up the power dissipation of each individual output transistor. This is easily done by knowing $R_{DS(on)}$ and load current of the individual outputs.

Very satisfactory steady state and transient results have been experienced with this thermal model. Tests indicate the model accuracy to have less than 10% error. Output interaction with an adjacent output is thought to be the main contributor to the thermal inaccuracy. Tests indicate little or no detectable thermal affects caused by distant output transistors which are isolated by one or more other outputs. Tests were conducted with the device mounted on a typical PC board placed horizontally in a 33 cubic inch still air enclosure. The PC board was made of FR4 material measuring 2.5″ by 2.5″, having double–sided circuit traces of 1.0 oz. copper soldered to each device pin. The board temperature was measured with thermal couple soldered to the board surface one inch away from the center of the device. The ambient temperature of the enclosure was measured with a second thermal couple located over the center and one inch distant from device.

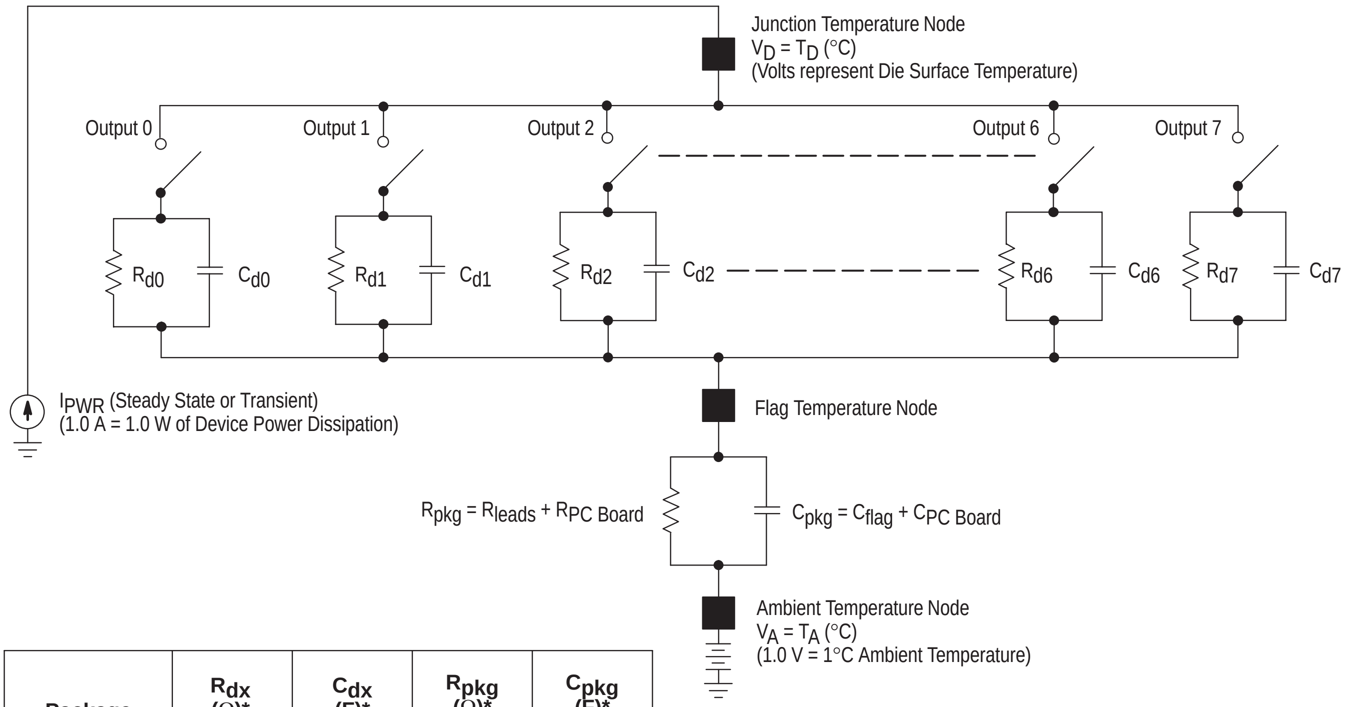
Thermal Performance

Figure 20 shows the worst case thermal component parameters values for the MC33298 in the 20 pin plastic power DIP and the SOP–24 wide body surface mount package. The power DIP package has Pins 5, 6, 15, and 16 connected directly to the lead frame flag. The parameter values indicated take into account adjacent output cell thermal pulling effects as well as different output combinations. The characterization was conducted over power dissipation levels of 0.7 to 17 W. The junction–to–ambient temperature thermal resistance was found to be 37°C/W with a single output active (31°C/W with all outputs dissipating equal power) and in conjunction with this, the thermal resistance from junction to PC board ($R_{junction–board}$) was found to be 27°C/W (board temperature, measured 1″ from device center). In addition, the thermal resistance from junction–to–heatsink lead was found to approximate 10°C/W. Devoting additional PC board metal around the heatsinking pins improved R_{pkg} from 30° to 28°C/W.

The SOP–24 package has Pins 5, 6, 7, 8, 17, 18, 19, and 20 of the package connected directly to the lead frame flag. Characterization was conducted in the same manner as for the DIP package. The junction–to–ambient temperature resistance was found to be 40°C/W with a single output active (34°C/W with all outputs dissipating equal power) and the thermal resistance from junction–to–PC board ($R_{junction–board}$) to be 30°C/W (board temperature, measured 1″ from device center). The junction–to–heatsink lead resistance was found again to approximate 10°C/W. Devoting additional PC board metal around the heatsinking pins for this package improved the R_{pkg} from 33° to 31°C/W.

The total power dissipation available is dependent on the number of outputs enabled at any one time. At 25°C the $R_{DS(on)}$ is 450 mΩ with a coefficient of 6500 ppm/°C. For the junction temperature to remain below 150°C, the maximum available power dissipation must decrease as the ambient temperature increases. Figures 21 and 22 depict the per output limit of current at ambient temperatures necessary for the plastic DIP and SOP packages respectively when one, four, or eight outputs are enabled "on." Figure 23 depicts how the $R_{DS(on)}$ output value is affected by junction temperature.

Figure 20. Thermal Model (Electrical Equivalent)



Package	R_{dx} (Ω)*	C_{dx} (F)*	R_{pkg} (Ω)*	C_{pkg} (F)*
20 Pin DIP	7.0	0.002	30	0.2
SOP–24L	7.0	0.002	33	0.15

* Ω = °C/W, F = W s/°C, I_{PWR} = W, and V_A = °C

Figure 21. Maximum DIP Package Steady State Output Current versus Ambient Temperature

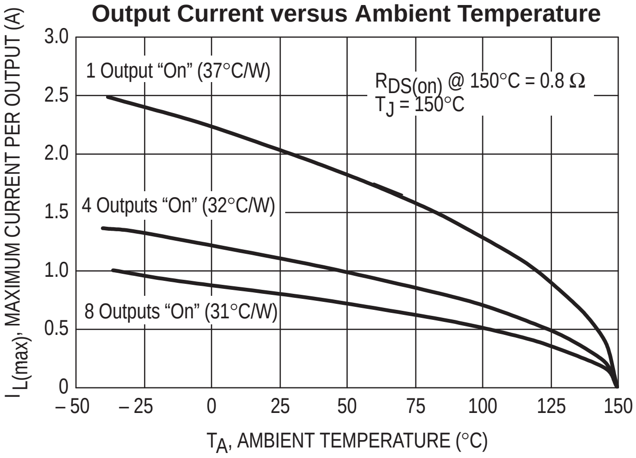


Figure 22. Maximum SOP Package Steady State Ouput Current versus Ambient Temperature

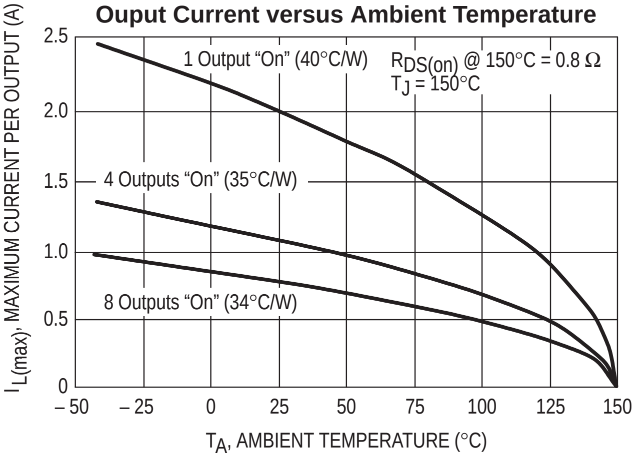
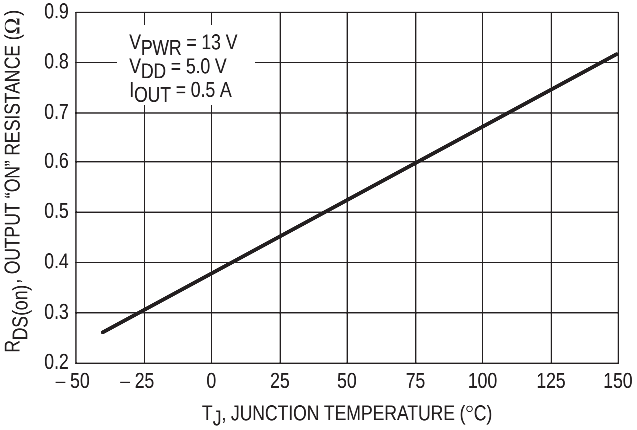


Figure 23. Maximum Output "On" Resistance versus Junction Temperature



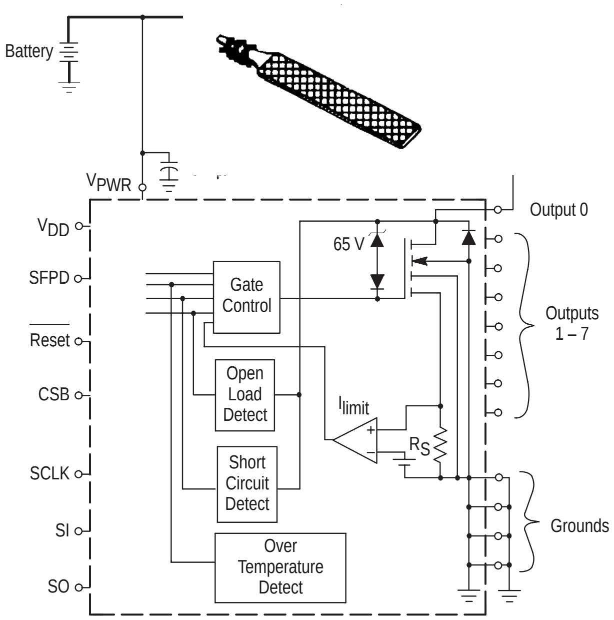
Latch–Up Immunity

Device latch–up caused by substrate injection has been characterized. Latch–up immunity has both a dc and a transient immunity component. DC latch–up immunity results indicate the device to be capable of withstanding in excess of four amps of reverse current out of any of the output transistors while the control logic continues to function normally. The logic control current (I_{DD}) was found to increase by only 0.6 mA with four amps of current being pulled out of an output. Additionally, the I_{PWR} current was found to increase by only 0.15 mA under the same condition. These increases are a result of minority carriers being injected into substrate and subsequently being collected.

The following procedure has been developed to test for transient latch–up immunity and has been applied to this automotive circuit design. Results of transient testing indicate the device to operate properly at output currents greater than 1.5 A. The procedure tests for the device's immunity to intermittent load to battery current connection with the device controlling an inductive load. Appropriately termed "the file test," the battery is connected to a shop file while the lead to the inductive load is dragged across the files surface causing intermittent load opens producing lots of arcs, sparks, and smoke, plus severe transients (see Figure 24). It is during these severe transients that latch–up most likely could occur. The battery voltage used for this test was 18 V and the inductive load was 2.0 mH. These values were found to produce severe transient stresses of the device outputs. All outputs must maintain operation and input control during transient generation to pass "the file test."

The device's input control currents were found to remain stable and were not affected by dc or transient latch–up immunity testing.

Figure 24. Transient Latch–Up Immunity File Test



APPLICATIONS INFORMATION

SIOP Communication

Two common communication protocols used in Motorola's microprocessors are the Serial Peripheral Interface (SPI) and Synchronous Input Output Port (SIOP). SIOP is a subset of the more flexible SPI and the simpler of the two protocols. SIOP is used on many of the MC68HC05 family of microcontrollers. Restrictions of the SIOP protocol include: 1) the SCLK frequency is fixed at one–fourth the internal clock rate and 2) the polarity of the SCLK signal is fixed.

By way of example, the MC68HC05P9 utilizes SIOP protocol and is not directly compatible with the serial input requirements of the MC33298. Specifically, the MC33298 accepts data on the falling edge of SCLK whereas its rising edge triggers data transfer in the SIOP protocol. SCLK is high during SIOP transmissions, which is the opposite of what the MC33298 requires.

Though designed specifically for SPI communication protocol, the MC33298 can easily be adapted to communicate with SIOP protocol through the use of software. The amount of code required to implement SPI in software is relatively small, so the only major drawback is a slower transfer of data. The software routine shown in Table 1 completes a transfer in about 100 µs.

Cost

The bottom line relates to cost. The MC33298 is a very cost effective octal output serial switch for applications typically encountered in the automotive and industrial market segments. To accomplish only the most basic serial switch function the MC33298 offers, using a discrete semiconductor approach, would require the use of at least eight logic level power MOSFETs for the outputs and two shift registers for the I/O plus other miscellaneous "glue" components. Additional circuitry would have to be incorporated to accomplish the protection features offered by the MC33298. Other noteworthy advantages the MC33298 offers are conservation of power and board space, requirement of fewer application components, and enhanced application reliability. The MC33298 is available at a fraction of the cost required for discrete component implementation and represents true value.

The MC33298 represents a cost effective device having advanced performance and features and worthy of consideration.

Table 1. Program to Exercise the MC33298 Using SPI (Having Only SIOP) Protocol

SET LABELS FOR OUTPUT REGISTERS

PORTA	EQU	$0000	;SPI Port ;DO (Data Out), SCLK, CS, RESET, X, FLTOUT, DI (Data In)
PORTB	EQU	$0001	;Normally the SIOP Port. SIOP will be disabled
PORTC	EQU	$0002	;A–D Converter Port
PORTD	EQU	$0003	;Timer Capture Port
DDRA	EQU	$0004	;Data Direction Register for SPI Port
DDRB	EQU	$0005	;Data Direction Register for SCLK, SDI, SDO, 11111
DDRC	EQU	$0006	;Data Direction Register for A–D Converter Port
DDRD	EQU	$0007	;Data Direction Register for PORTD, Timer Capture

DTOUT	EQU	$0080	;Register for the SPI output data. This register will be used for a Serial–to–Parallel transformation.
DATAIN	EQU	$0081	;Input Register for SPI. Also used for a Serial–to–Parallel transformation.
VALUE	EQU	$0082	;Register to store the SPI. Also used for a Serial–to–Parallel transformation.
DATA1	EQU	$0083	;Miscellaneous data register

SCR	EQU	$000A	;Label for SIOP control register, 0 SPE 0 MSTR 0 0 0 0.
SSR	EQU	$000B	;Label for SIOP status register, SPIF DCOL 0 0 0 0 0 0, Read Only Register.
SDR	EQU	$000C	;Label for SIOP data register.

	ORG	$0100	;Program starts at first byte of User ROM.
INIT	RSP		;Reset Stack Pointer to $FF.

INITIALIZE THE DATA REGISTERS AND THEIR DATA DIRECTION BIT REGISTERS

	LDA	#$FE	;Configuration PortA as the SPI Port.
	STA	DDRA	;All but Bit 0 will be outputs.

	LDA	#$FF	
	STA	DDRB	;Configure Register B as an output. SIOP is not used for the MC33298, but is available for another peripheral.
	STA	DDRC	;Configure Register C as an output
	STA	DDRD	;Configure Register D as an output

	LDA	#%00010000	;Initialize the SIOP Control Register.
	STA	SCR	;Disable SIOP by clearing Bit 6.

SELECT THE DESIRED OUTPUTS

TOP	LDA STA	#$55 VALUE	Select outputs of MC33298 to be turned “on.” This instruction is left inside the loop to include changes while running the program. A set bit will cause the associated MC33298 output to be “off.” The value register is uncorrupted by the serial–to–parallel conversion.
	BSET	4,PORTA	;Reset the MC33298.
	BCLR	4,PORTA	;Also establishes a + or – trigger source
	BSET	4,PORTA	;The MC33298 is reset with a logic low.

	BCLR	5,PORTA	;Enable MC33298 by pulling CSB (chip select bar) low. Within the MC33298 the Fault Status is transferred to the MC33298 Serial Register at a falling edge of CSB.

	LDA	VALUE	;Select outputs to be turned “on.”
	STA	DTOUT	;Save Output Word (Value) to check for fault.

SPI TRANSFER LOOP

	LDX	#$07	;Set the number of Read/Shift cycles.

LOOP	ASL	DATAIN	;Shift a Zero into LSB of DATAIN and ASL other bits.
	ASL	DTOUT	;Test value currently in MSB of DTOUT.
	BCS	DOONE	;
	BCLR	7,PORTA	;MSB was Zero, so clear DATA OUT bit.
	JMP	GOON	
DOONE	BSET	7,PORTA	;MSB was One, so set the DATA OUT bit.
GOON	BSET	6,PORTA	;Set the SCLK. Serial Output pin of the MC33298 changes state on the rising edge of the SCLK. Read the next bit coming from the MC33298.

	BRCLR	0,PORTA, WZZER0	;Read the bit and branch if Zero. LSB of DATAIN is already cleared due to the ASL above.
	BSET	0,DATAIN	;Bit was One. Set the next bit in DATAIN.

WZZER0	BCLR	6,PORTA	;Clear SCLK. Falling edge causes the MC33298 to read the next bit from the MCU.
	DECX		
	BPL	LOOP	;Continue to loop eight times until the SPI transfer is complete.

	BSET	5,PORTA	;Transfer control signal to output transistors.

ESTABLISH A BRIEF DELAY

	LDA	#16	
PAUSE	DECA		;3 Clock cycles
	BNE	PAUSE	;3 Clock cycles
	BCLR	5,PORTA	;Transfer output status to Serial Register.
	JSR	FLTCHK	;Jump to Fault Check subroutine.

	JSR	DLY	;Delay 1/T msec

	BSET	5,PORTA	;Deselect the MC33298.
	BRA	TOP	;Return to top of loop.

SUBROUTINE TO CHECK FOR FAULTS

FLTCHK	BCLR	1,PORTA	;CLR the Fault pin.
	LDA	DATAIN	
	CMP	VALUE	;Check for Faults.
	BEQ	NOFLT	;If there is no Fault, continue.
	BSET	1,PORTA	;Activate Fault LED.
NOFLT	RTS		

DELAY SUBROUTINE

DLY	STA	DATA1	;Save Accumulator in RAM.
	LDA	#$04	;Do outer loop 4 times, roughly 4.0 ms.
OUTLP	CLRX		;X used as Inner Loop Count
INNRLP	DECX		;0–FF, FF–FE, … 1–0 256 loops.
	BNE	INNRLP	;6CYC* 256* 1.0 µs/CYC = 1.53 ms
	DECA		;4–3. 3–2, 2–1, 1–0
	BNE	OUTLP	;1545CYC* 4*1.0 µs/CYC = 6.18 ms
	LDA	DATA1	;Recover Accumulator value.
	RTS		;Return from subroutine.

	ORG	$1FF	
	FDB	INIT	

MOTOROLA

MC79076
MCCF79076

Product Preview

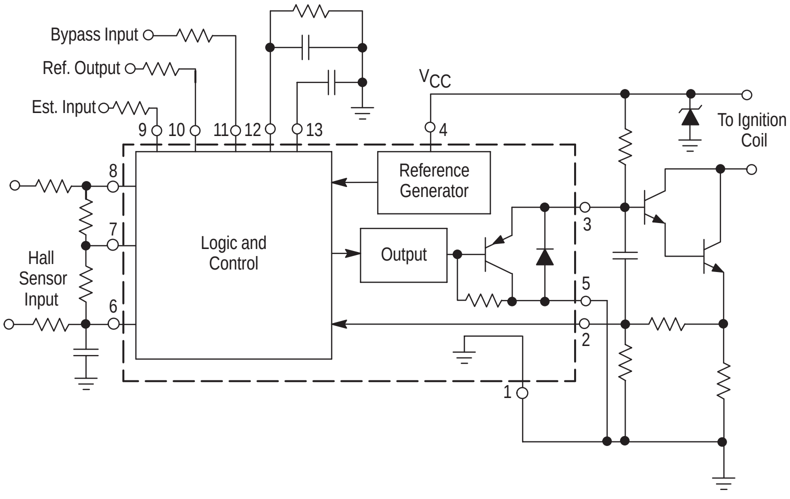
Electronic Ignition Control Circuit

The MCCF79076, in conjunction with an appropriate Motorola Power Darlington Transistor, provides an economical solution for automotive ignition applications. The MCCF79076 offers optimum performance by providing closed loop operation of the Power Darlington in controlling the ignition coil current.

The MCCF79076 incorporates Flip–Chip Technology which involves the formation of solder bumps, rather than traditional wire bonds, to establish mechanical and electrical contact to the semiconductor chip. This process affords a unique device having improved reliability at elevated operating temperatures.

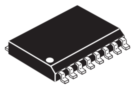
- Solder Bumped for Flip–Chip Assembly
- Ignition Coil Voltage Internally Limited to 375 V
- Coil Current Limiting to 7.5 A
- Output On–Time (Dwell) Control
- Dwell Feedback Control to Sense Coil Variation
- Hall Sensor Input
- – 30°C ≤ T_A ≤ +140°C Ambient Operating Temperature

Simplified Block Diagram and Application Circuit



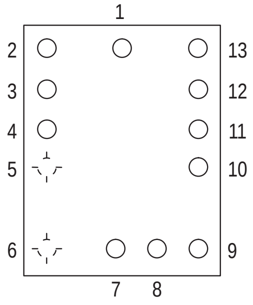
ELECTRONIC IGNITION CONTROL CIRCUIT

SEMICONDUCTOR TECHNICAL DATA



DW SUFFIX
PLASTIC PACKAGE
CASE 751G
(SO–16L)

FLIP–CHIP CONFIGURATION



Top View
(Bump Side)

BUMP CONNECTIONS

1. High Ground
2. Output Current Limit
3. Dwell Output
4. Supply
5. Low Ground
6. Reference Dwell Input
7. Advance Input
8. Bias Voltage
9. Est Input
10. Reference Output
11. Bypass Input
12. 900 RPM Detector
13. Dwell Control

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MCCF79076	T_A = – 30° to +125°C	Flip–Chip
MC79076DW		SO–16L

MOTOROLA

Product Preview

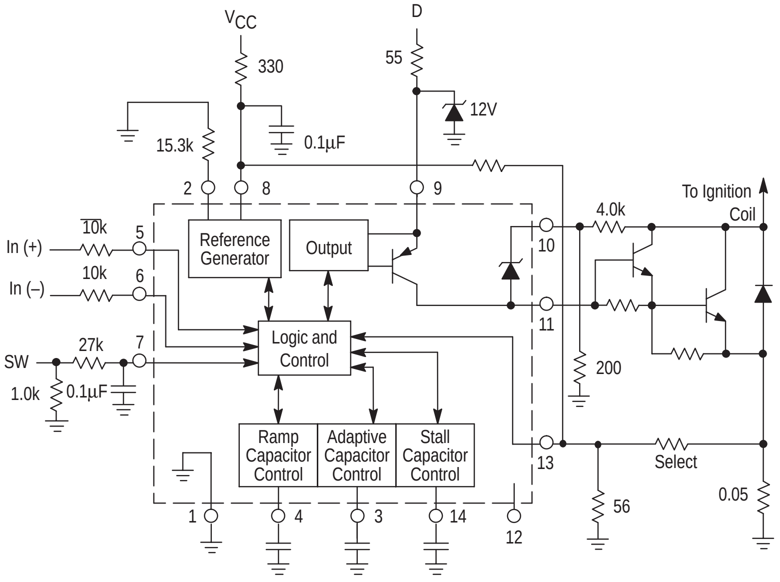
Ignition Control Flip-Chip

Designed for automotive ignition applications. The MCCF33093 provides outstanding control of the ignition coil when used with an appropriate Motorola Power Darlington Transistor. Engine control systems utilizing the MCCF33093 exhibit exceptional fuel efficiency and low exhaust emissions. The MCCF33093 requires a differential Hall Sensor input for proper operation.

The MCCF33093 utilizes Flip-Chip Technology in which solder bumps, rather than traditional wire bonds, are created to establish mechanical and electrical contact to the chip. This process affords a unique device having improved reliability at elevated operating temperatures.

- Solder Bumped for Flip-Chip Assembly
- External Capacitors to Set Device Timing
- Overvoltage Shutdown Protection
- Auto Start-Up Capability Once Overvoltage Condition Ceases
- Allows for Push Start-Up in Automotive Applications
- Ignition Coil Current Limiting
- Ignition Coil Voltage Limiting
- Bandgap Reference for Enhanced Stability Over Temperature
- Negative Edge Filter for Hall Sensor Input Transient Protection
- Hall Sensor Inputs for RPM and Position Sensing
- – 30°C ≤ T_A ≤ +140°C Ambient Operating Temperature

Simplified Block Diagram and Application Circuit

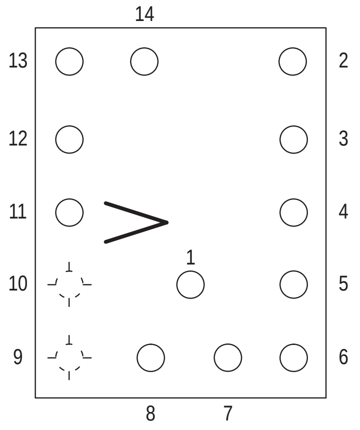


MCCF33093

IGNITION CONTROL FLIP–CHIP

SEMICONDUCTOR TECHNICAL DATA

FLIP-CHIP CONFIGURATION



(Backside View)

0.116 inch x 0.091 inch
Backside orientation marking
indicated by arrow oriented as shown

BUMP CONNECTIONS

1. Ground
2. Master Bias
3. Adaptive Capacitor
4. Ramp Capacitor
5. Positive Hall Input
6. Negative Hall Input
7. Start
8. Supply
9. Distributor Signal
10. Coil
11. Output
12. Process Test
13. Emitter of Darlington
14. Stall Capacitor

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MCCF33093	T_A = –30° to +140°C	Flip–Chip

MOTOROLA

MCCF33094

Product Preview

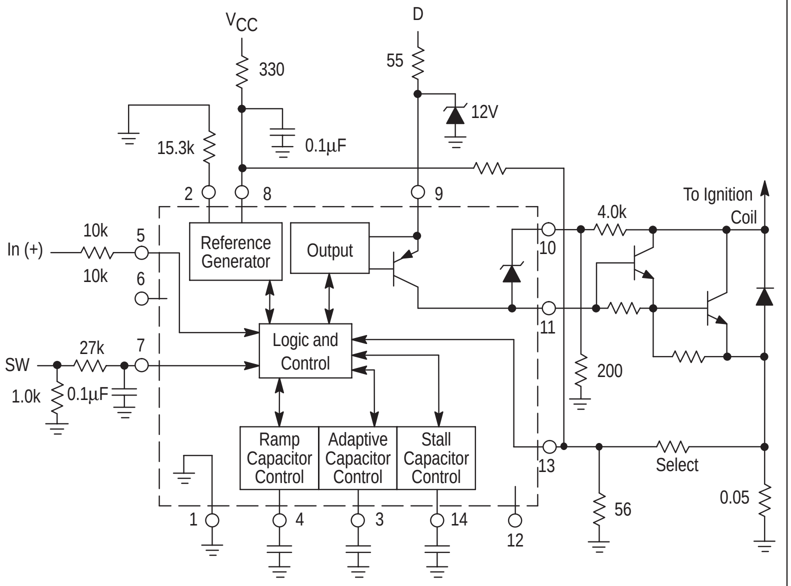
Ignition Control Flip-Chip

Designed for automotive ignition applications. The MCCF33094 provides outstanding control of the ignition coil when used with an appropriate Motorola Power Darlington Transistor. Engine control systems utilizing the MCCF33094 exhibit exceptional fuel efficiency and low exhaust emissions. For proper operation, the MCCF33094 requires a single Hall Sensor input signal, which is compared to an accurate internal reference.

The MCCF33094 utilizes Flip-Chip Technology in which solder bumps, rather than traditional wire bonds, are created to establish mechanical and electrical contact to the chip. This process affords a unique device having improved reliability at elevated operating temperatures.

- Solder Bumped for Flip-Chip Assembly
- External Capacitors to Set Device Timing
- Overvoltage Shutdown Protection
- Auto Start-Up Capability Once Overvoltage Condition Ceases
- Allows for Push Start-Up in Automotive Applications
- Ignition Coil Current Limiting
- Ignition Coil Voltage Limiting
- Bandgap Reference for Enhanced Stability Over Temperature
- Negative Edge Filter for Hall Sensor Input Transient Protection
- Hall Sensor Inputs for RPM and Position Sensing
- – 30°C ≤ T_A ≤ +140°C Ambient Operating Temperature

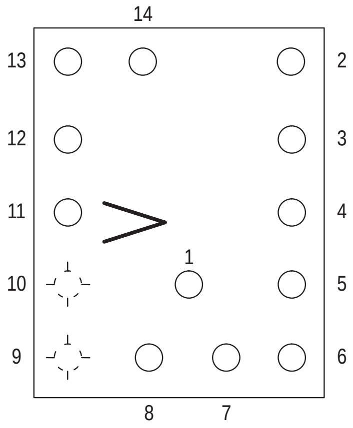
Simplified Block Diagram and Application Circuit



IGNITION CONTROL FLIP–CHIP

SEMICONDUCTOR TECHNICAL DATA

FLIP-CHIP CONFIGURATION



(Backside View)

0.116 inch x 0.091 inch
Backside orientation marking
indicated by arrow oriented as shown

BUMP CONNECTIONS

1. Ground
2. Master Bias
3. Adaptive Capacitor
4. Ramp Capacitor
5. Positive Hall Input
6. N.C.
7. Start
8. Supply
9. Distributor Signal
10. Coil
11. Output
12. Process Test
13. Emitter of Darlington
14. Stall Capacitor

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MCCF33094	T_A = –30° to +140°C	Flip–Chip

MCCF33095
MC33095

Advance Information

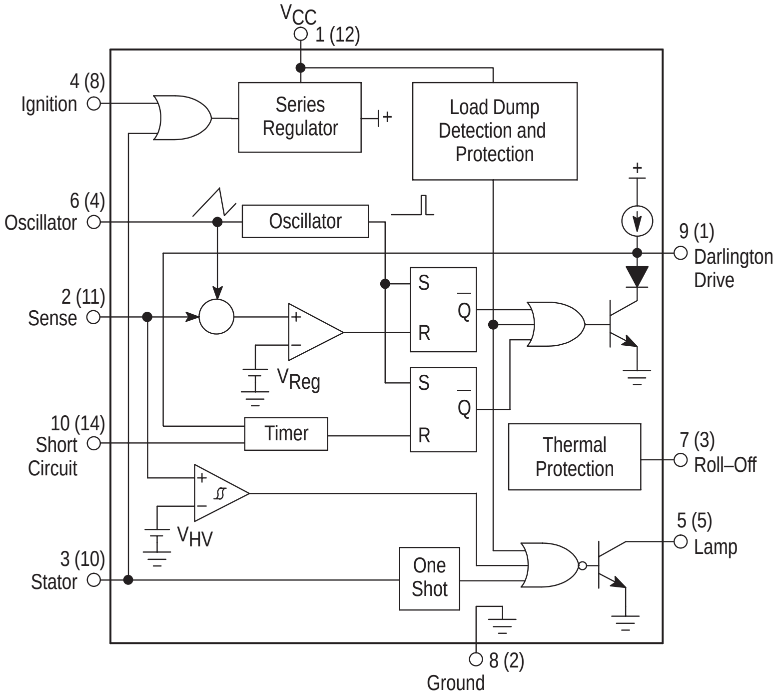
Integral Alternator Regulator

The MCCF33095 (Flip–Chip) and MC33095 (Surface Mount) are regulator control integrated circuits designed for use in automotive 12 V alternator charging systems. Few external components are required for full system implementation. These devices provide control for a broad range of 12 V alternator charging systems when used in conjunction with the appropriate Motorola Power Darlington transistor to control the field current of the specific alternator.

Both versions have internal detection and protection features to withstand extreme electrical variations encountered in harsh automotive environments. Flip–Chip Technology allows the MCCF33095 to operate at higher ambient temperatures than the surface mount version in addition to withstanding severe vibration and thermal shock with a high degree of reliability.

- Constant Frequency with Variable Duty Cycle Operation
- Adjusts System Charging to Compensate for Changes in Ambient Temperature
- Slew Rate Control to Reduce EMI
- Lamp Pin to Indicate Abnormal Operating Conditions
- Shorted Field Protection
- Resumes Normal Operation Once Fault Condition Ceases
- Operation from –40°C to 170°C for Flip–Chip and –40°C to 125°C for SO–14
- Surface Mount or Solder Bump Processed Flip–Chip Assembly Versions

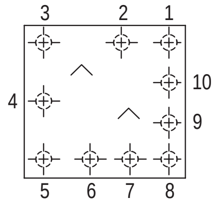
Simplified Block Diagram



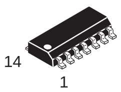
This device contains 145 active transistors.

INTEGRAL ALTERNATOR REGULATOR

SEMICONDUCTOR TECHNICAL DATA



FLIP–CHIP CONFIGURATION
(Backside View)
Back marking is oriented as shown



D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO–14)

Bump	Function	SO–14 (Note 1)
1	V_{CC}	(12)
2	Sense	(11)
3	Stator	(10)
4	Ignition	(8)
5	Lamp	(5)
6	Oscillator	(4)
7	Roll–Off	(3)(Note 2)
8	Ground	(2)
9	Darlington Drive	(1)
10	Short Circuit	(14)

NOTES: 1. No connections to Pins 3, 6, 7, 9 and 13.
2. Connected to ground internal to package.

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MCCF33095	T_A = –40° to +170°C	Flip–Chip
MC33095D	T_A = –40° to +125°C	SO–14

MAXIMUM RATINGS (Notes 1 and 3)

Rating	Symbol	Value	Unit
Steady State V_{CC}, V_{IGN}, V_{STA}	–	9.0 to 24	V
V_{CC} and V_{IGN} Transient	–	80	V
Bump Shear Strength (Flip–Chip)	–	8.0	Grams/Bump
Thermal Characteristics (Thermal Resistance) Junction–to–Substrate (Flip–Chip) Junction–to–Ambient (SO–14)	 $R_{\theta JS}$ $R_{\theta JA}$	 29 145	°C/W
Junction Temperature Flip–Chip SO–14	T_J	 170 150	°C
Operating Ambient Temperature Range Flip–Chip SO–14	T_A	 –40 to +170 –40 to +125	°C

ELECTRICAL CHARACTERISTICS (Limit values are given for –40°C ≤ T_A ≤ 150°C (Flip–Chip), –40°C ≤ T_A ≤ 125°C (SO–14) and typical values represent approximate mean value at T_A = 25°C. Oscillator, Roll–Off, Ground, Short Circuit = 0 V, and 12 V ≤ V_{CC}, Sense, Stator, Ignition ≤ 16 V, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit
SUPPLY (V_{CC})					
Supply Current Disabled (Ignition = 0.5 V, Stator = 5.0 V) Enabled (V_{CC}, Sense = 17 V, Ignition = 1.4 V)	I_{CC}	 –50 0	 0.2 3.9	 300 25	 µA mA
Darlington Drive Overvoltage Disable Threshold (V_{CC}, Ignition, Short Circuit = 19 V to 29 V Ramp, Stator = 10 V) Hysteresis (V_{CC}, Stator, Ignition, Short Circuit = 29 V to 19 V Ramp)	 V_{CODD} V_{CODDH}	 19 –	 26 4.2	 28.5 –	V
Lamp Overvoltage Disable Threshold (V_{CC}, Stator, Ignition, Short Circuit = 19 V to 29 V Ramp) Hysteresis	 V_{COL} V_{COLH}	 19 –	 22.3 0.3	 29.5 –	V
SENSE					
Sense Current (Oscillator = 2.0 V)	I_{SNS}	–10	0.6	10	µA
Calibration Voltage (50% Duty Cycle) (Note 5)	V_R	12.25	14.6	17.5	V
Lamp Comparator Detect Threshold	V_{SCD}	–	16.3	–	V
Proportional Control Range	M_V	50	187.4	350	mV
Lamp Comparator Reset Threshold	V_{HV}	15.4	15.9	16.4	V
Lamp Hysteresis	V_{HYS}	20	416.6	600	mV
STATOR					
Propagation Delay (Lamp–to–High, Stator = 15 V to 6.0 V)	t_{STA}	6.0	59.4	600	ms
Reset Threshold Voltage (Lamp–to–Low, Stator = 5.0 V to 11 V)	V_{IH}	6.0	8.8	11	V
Input Current (Sense = 18 V, Oscillator = 2.0 V)	I_{STA}	–10	1.5	10	µA
LAMP					
Saturation Voltage (Lamp = 14 mA)	V_{OLL}	0	111.8	350	mV
Leakage Current (Sense = 1.0 V, Lamp = 2.5 V)	I_{OHL}	–50	0.8	50	µA
Saturation Voltage (V_{CC}, Sense, Stator, Ignition = 30 V, Lamp = 20 mA)	V_{OOLL}	0	147.4	350	mV

NOTES:
1. V_{CC} applied through a 250 Ω resistor.
2. Sense input applied through a 100 kΩ and 50 kΩ resistor divider to generate one–third V_{bat}.
3. Stator and Ignition inputs applied through a 20 kΩ resistor.
4. Short Circuit input applied through a 30 kΩ resistor.
5. Oscillator pin connected in series with 0.022 µF capacitor to ground.

ELECTRICAL CHARACTERISTICS (continued) (Limit values are given for –40°C ≤ T_A ≤ 150°C (Flip–Chip), –40°C ≤ T_A ≤ 125°C (SO–14) and typical values represent approximate mean value at T_A = 25°C. Oscillator, Roll–Off, Ground, Short Circuit = 0 V, and 12 V ≤ V_{CC}, Sense, Stator, Ignition ≤ 16 V, unless otherwise specified.)

DARLINGTON DRIVE

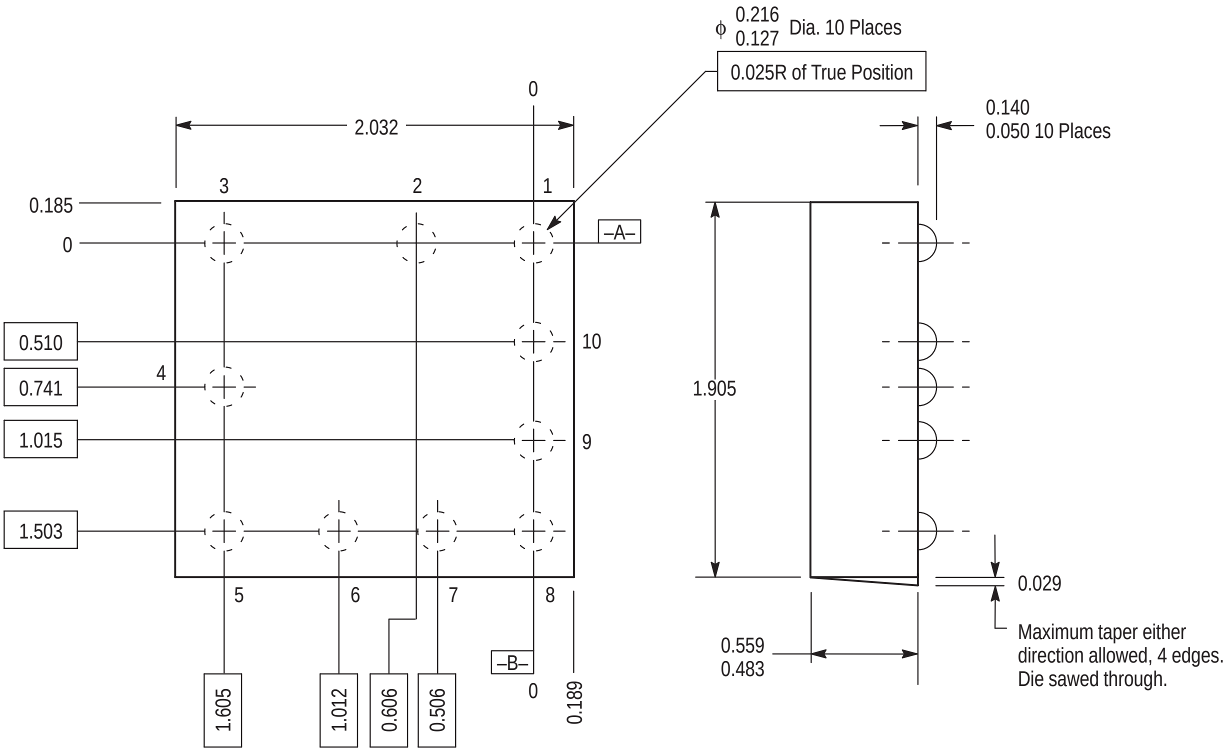
Source Current (Pins V_{CC}, Sense, Ignition = 9.0 V, Darlington Drive = V across Power Darlington)	I_{OHDD}	4.0	7.6	20	mA
Saturation Voltage (Sense = 18 V, Oscillator = 2.0 V, Darlington Drive = –100 μA)	V_{OLDD}	0	300.1	350	mV
Minimum “On” Time (Sense = 18 V) (Note 5)	t_{DD}	200	697.8	700	μs
Frequency (Note 5)	F_{OSC}	75	174.7	325	Hz
Minimum Duty Cycle (Sense = 18 V) (Note 5)	DC_{DD}	4.0	12.2	13	%
Rise Time (10% to 90%) (Note 5)	t_r	10	21.4	50	μs
Fall Time (90% to 10%) (Note 5)	t_f	10	23.7	50	μs

SHORT CIRCUIT

Duty Cycle (Note 5)	DC_{SC}	1.0	1.7	5.0	%
“On” Time (Short Circuit High, Short Circuit = 8.0 V) (Note 5)	PW_{SC}	60	99	660	μs

NOTES: 1. V_{CC} applied through a 250 Ω resistor.
2. Sense input applied through a 100 kΩ and 50 kΩ resistor divider to generate one–third V_{bat}.
3. Stator and Ignition inputs applied through a 20 kΩ resistor.
4. Short Circuit input applied through a 30 kΩ resistor.
5. Oscillator pin connected in series with 0.022 μF capacitor to ground.

Figure 1. Flip–Chip Mechanical Dimensions



NOTES: 1. All dimensions shown indicated in millimeters.
2. ☐ Denotes basic dimension having zero tolerance and describes the theoretical exact location (true position) or contour.

Figure 2. Pins 1, 3 and 4 Field Transient Decay

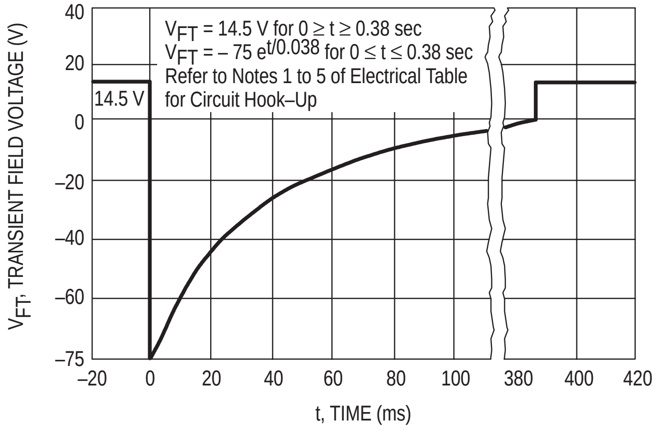


Figure 3. Pins 1 and 4 Load Dump Transient Decay

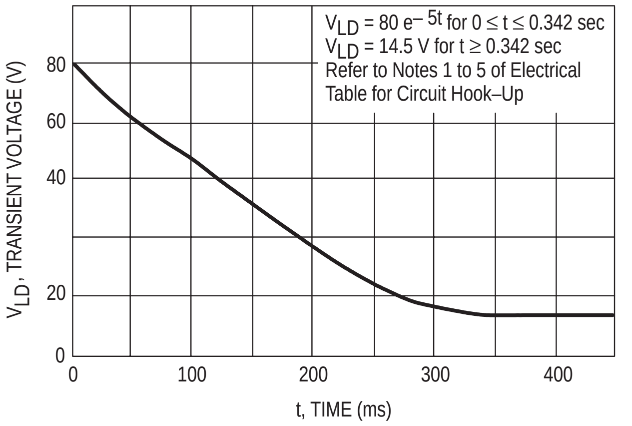


Figure 4. Temperature versus V_{bat} for 50% Duty Cycle

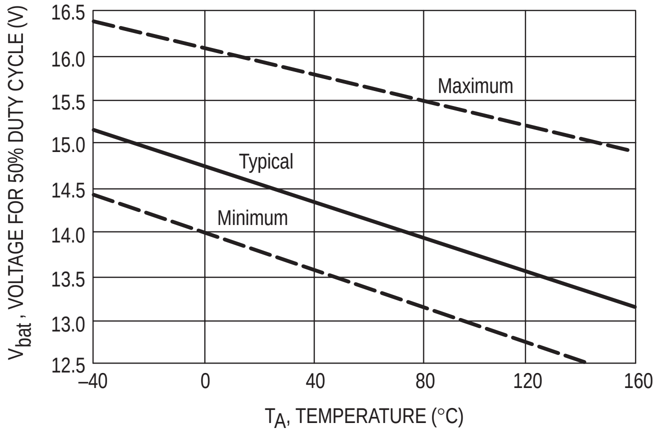


Figure 5. V_{bat} (50% Duty Cycle) versus V_{bat} (Lamp “On”)

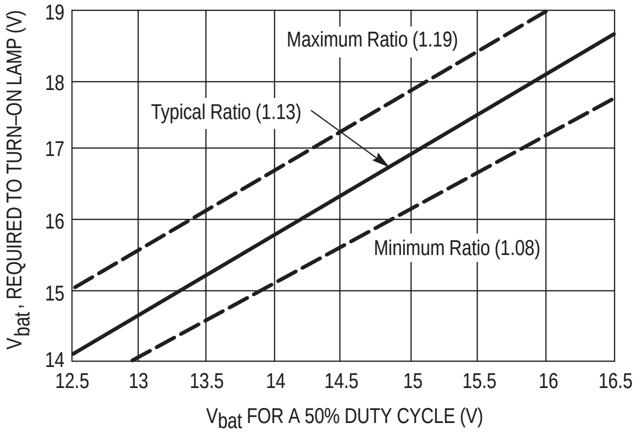


Figure 6. Field Current versus Cycle Time

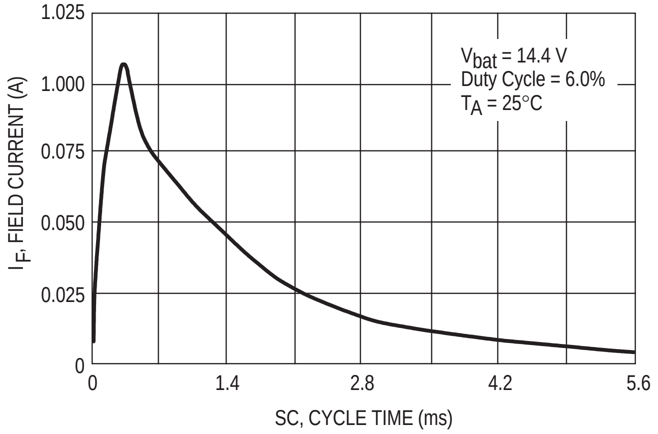


Figure 7. Field Current versus Time

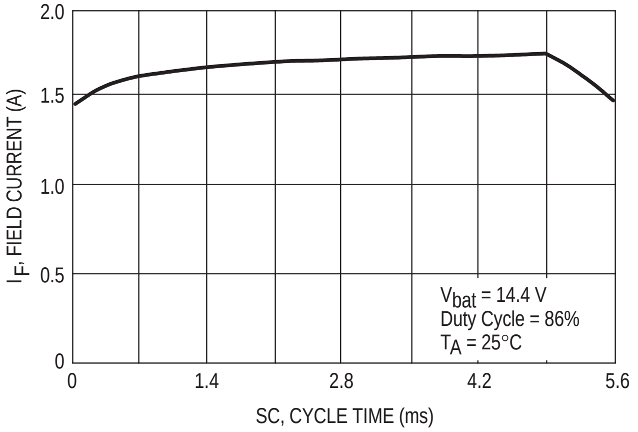
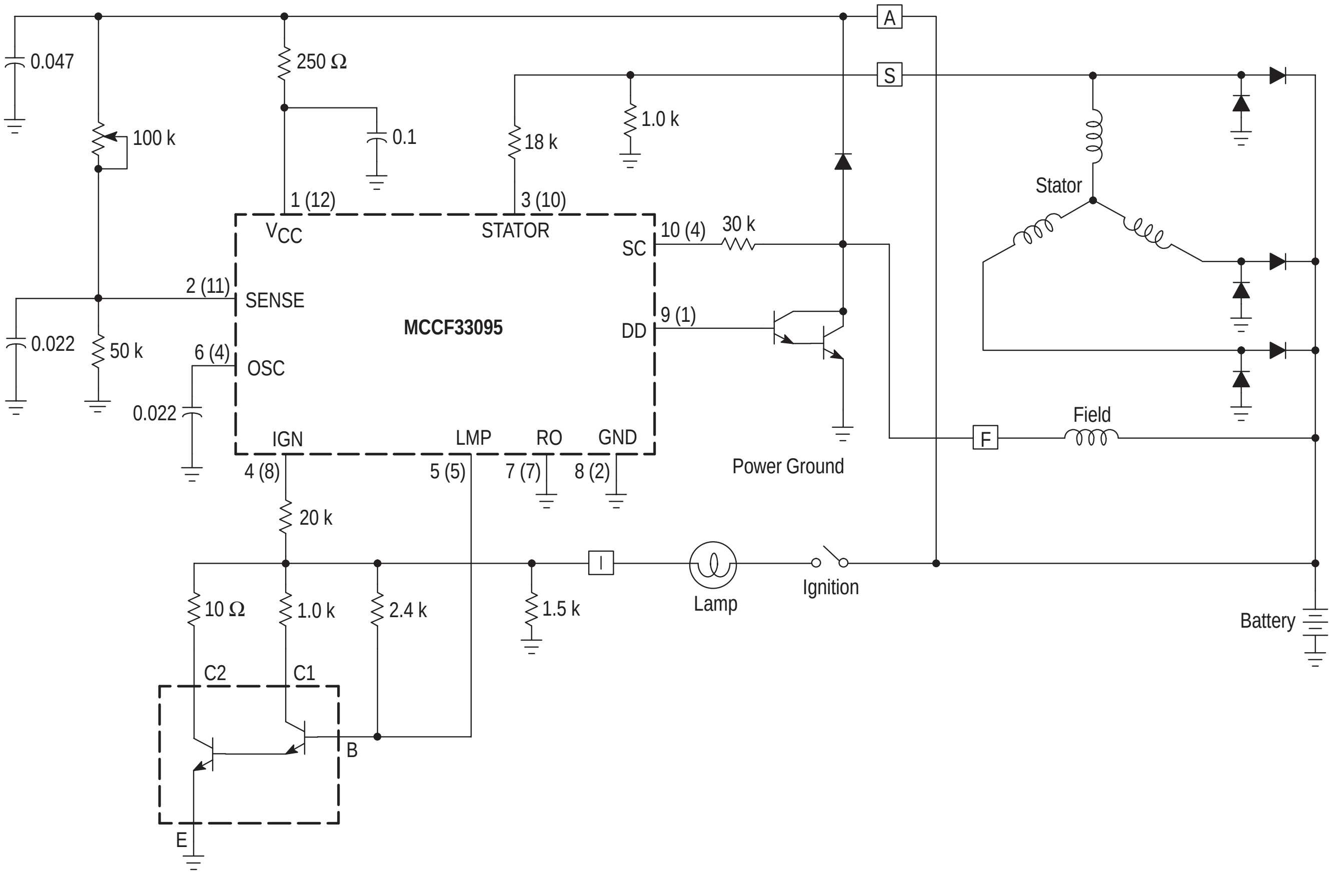


Figure 8. Integral Alternator Regulator System



FUNCTIONAL DESCRIPTION

Introduction

This ignition control circuit was originally designed and offered as an MCCF33095 Flip–Chip for use in 12 V automotive alternator charging systems. The MCCF33095 consists of many protection features which are entailed in a ten pin flip–chip package. The device was subsequently made available in a 14 pin surface mount version (MC33095D). Both versions perform in a similar manner. The Flip–Chip version has an advantage over the surface mount version where minimized space and higher operating ambient temperatures are of major concern. Device operation and application suggestions for both versions are given below.

Oscillator

The oscillator frequency is determined by the value of an external capacitor from the Oscillator pin to ground (see applications circuit). The oscillator frequency in a typical application is approximately 175 Hz, but a range of 50 Hz to 500 Hz can reasonably be used. The waveform generated consists of a positive linear slope followed by relatively fast negative fall (sawtooth). The flip–flops are reset by the falling edge of the sawtooth signal as shown on the logic diagram. The oscillator signal peaks at approximately 3.0 V and provides the timing required for the device.

Ignition

The Ignition input signal enables the device turn–on when the Ignition pin voltage is greater than 1.4 V. This signal normally originates from the ignition switch of automotive systems.

Sense

The Sense pin functions as a voltage sensor. It proportionally senses the battery voltage and determines the amount of time the Darlington transistor is high over the next cycle. A low voltage at the Sense pin will result in a long duty cycle for the Darlington while a high voltage produces a short duty cycle. In the application, proportional control is used to determine the duty cycle. Proportional control is defined as the sense ratio of battery voltage, present on the Sense pin, required to obtain a 20% to 95% duty cycle range in the application. The 20% duty cycle value will correlate to the maximum battery in the application. Normally the sense ratio of battery voltage is an end product trim adjustment.

Lamp

The Lamp output pin functions as a warning indicator for overvoltage and stopped engine or broken belt conditions existing in the system.

Stator

The Stator pin senses the voltage from the stator in the application circuit, and keeps the device powered up while the stator voltage is high. Furthermore, it acts as a sense for a stopped engine or broken belt condition. If this condition is detected, the Stator turns “on” the Lamp.

Power Supply, V_{CC}

The V_{CC} pin powers the entire device and disables all outputs during any overvoltage condition.

Roll–Off

The Roll–Off pin provides thermal protection for the circuit. This capability exists, but has not been characterized and is not tested for at this time. Therefore, it is recommended that this pin be connected to ground. The surface mount version has this pin internally connected to ground.

Darlington Drive

The purpose of the Darlington Drive output pin is to turn on an external power Darlington transistor. The Sense pin voltage determines the duty cycle of the Darlington. The oscillator is set to maintain a minimum duty cycle, except during overvoltage and short circuit conditions.

Short Circuit

The Short Circuit pin monitors the field voltage. When the Darlington Drive and Short Circuit pins are simultaneously high for a duration greater than the slew rate period, a short circuit condition is noted. The detection time required prevents the device from reacting to false shorts. As a result of short circuit detection, the output is disabled. During a short circuit condition, the device automatically retries with a 2% duty cycle (Darlington “on” time). Once the short circuit condition ceases, normal device operation resumes.

Application Notes

A capacitor should be used in parallel with the V_{CC} pin to filter out noise transients on the supply or battery line. Likewise, a capacitor should be used in parallel with the Sense pin to create a dominant closed loop pole. Resistors connected to inputs, as mentioned in Notes 1 through 5 of the Electrical Characteristic table, should be used.

FLIP–CHIP APPLICATION INFORMATION

Introduction

Although the packaging technology known as “flip–chip” has been available for some time, it has seen few applications outside the automotive and computer industries. Present microelectronic trends are demanding smaller chip sizes, reduced manufacturing costs, and improved reliability. Flip–chip technology satisfies all of these needs.

Conventional assembly techniques involve bonding wires to metal pads to make electrical contact to the integrated circuit. Flip–chip assembly requires further processing of the integrated circuit after final nitride deposition to establish robust solder bumps with which to make electrical contact to the circuit. A spatially identical solderable solder bump pattern, normally formed on ceramic material, serves as a substrate host for the flip–chip. The “bumped” flip–chip is aligned to, and temporarily held in place through the use of soldering paste. The aligned flip–chip and substrate host are placed into an oven and the solder reflowed to establish both electrical and mechanical bonding of the flip–chip to the substrate circuit. Use of solder paste not only holds the chip in temporary placement for reflow but also enhances the reflow process to produce highly reliable bonds.

Flip–Chip Benefits

Some of the benefits of flip–chip assembly are:

1) Higher circuit density resulting in approximately one–tenth the footprint required of a conventional plastic encapsulated device.
2) Improved reliability, especially in high temperature applications. This is due, in part, to the absence of wires to corrode or fatigue from extensive thermal cycling.
3) No bond wires are required that might possibly become damaged during assembly.
4) Adaptable for simultaneous assembly of multiple flip–chips, in a hybrid fashion, onto a single ceramic substrate.

The following discussion covers the flip–chip process steps performed by Motorola, and the assembly processing required by the customer, in order to attach the flip–chip onto a ceramic substrate.

MOTOROLA’S FLIP–CHIP PROCESS

Overview

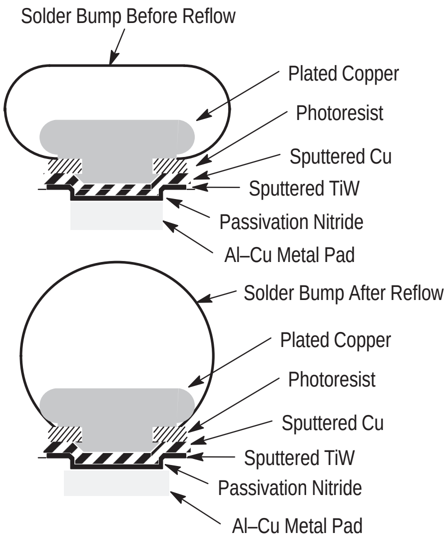
The process steps to develop an integrated circuit flip–chip are identical to that of conventional integrated circuits up to and including the deposition of the final nitride passivation layer on the front surface (circuit side). At this stage all device metal interconnects are present.

The process sequence is as follows:

1) Passivation–nitride photoresist and etch
2) Bimetal sputter (titanium (Ti) and tungsten (W) followed by copper (Cu))
3) Photo mask to define the bump area
4) Copper plate
5) Lead plate
6) Tin plate
7) Photoresist clean to remove all photoresist material
8) Bimetal etchback
9) Reflow for bump formation
10) Final inspection

The diagram below depicts the various layers involved in the bump process.

Figure 9. Plated Bump Structure and Process Flow



Initially, photoresist techniques are used to create openings in the nitride passivation layer exposing the metal pad bias. Ti/W, followed by Cu, are sputtered across the entire wafer surface. The surface is then photo patterned to define the bump areas. The sputtered metals together constitute a base metal for the next two metal depositions.

The Ti/W layer provides excellent intermetallic adhesion between the metal pads and the sputtered copper. In addition, the Ti/W provides a highly reliable interface to absorb mechanical shock and vibrations frequently encountered in automotive applications. The sputtered copper layer creates a platform onto which an electroplated copper layer can be built–up. Layers of Cu, Pb, and Sn are applied by plating onto the void areas of the photoresist material. The photoresist is then removed and the earlier sputtered materials are etched away. The flip–chip wafer is then put into an oven exposing it to a specific ambient temperature which causes the lead and tin to ball–up and form a solder alloy.

IC Solder Bumps

The solder consists of approximately 93% lead and 7% tin. The alloying of lead with tin provides a bump with good ductility and joint adhesion properties. Precise amounts of tin are used in conjunction with lead. Too much tin in relation to lead can cause the solder joints to become brittle and subject to fatigue failure. Motorola has established what it believes to be the optimum material composition necessary in order to achieve high bump reliability.

In the make–up of the flip–chip design, bumps are ideally spaced evenly and symmetrically along each edge of the chip allowing for stress experienced during thermal expansion and vibration to be distributed evenly from bump to bump. The bump dimensions and center–to–center spacing (pitch) are specified by the chip layout and the specific application. The nominal diameter of the bumps is 6.5 mils and the minimum center–to–center pitch is roughly 8.0 mils.

Reflow

The reflow process creates a thermally induced amalgam of the lead and tin. In the melting process, the surface tension is equalized causing the melted solder to uniformly ball up as mentioned earlier.

The ideal reflow oven profile gradually ramps up in temperature to an initial plateau. The purpose of the plateau is to establish a near equilibrium temperature just below that of the solder's melting temperature. Following the preheat, a short time and higher temperature excursion is necessary. This is to ensure adequate melting of the solder materials. The temperature is then ramped down to room temperature.

An atmosphere of hydrogen is used during the reflow heat cycle. The hydrogen provides a reducing atmosphere for the removal of any surface oxides present. The formation or presence of oxides can cause degradation in the bond reliability of the product.

During the flip–chip attachment reflow onto the ceramic substrate host, the created surface tension of the molten solder aids in the alignment of the chip onto the ceramic substrate.

Reliability

Motorola is determined to bring high quality and reliable products to its customers. This is being brought about by increased automation, in–line Statistical Process Control (SPC), bump shear strength testing, thermocycling from – 40° to +140°C, process improvements such as backside laser marking of the silicon chip, and improved copper plating techniques.

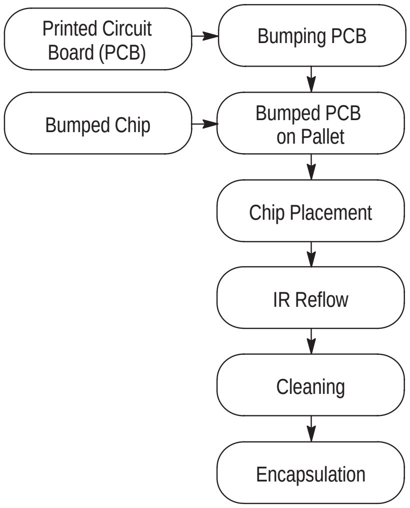
ATTACHING FLIP–CHIPS ONTO CERAMIC SUBSTRATES

Overview

The assembly or process of attaching the flip–chip onto a ceramic substrate is performed by the module fabricator. Prior to actual assembly, the ceramic substrate should undergo several process steps. Care should be exercised to properly orient the flip–chip onto the substrate host in order to accommodate the appropriate solder bumps. Ideally, the flip–chip should be removed from the waffle pack with a pick and place machine utilizing a vacuum pick–up to move the die onto the ceramic substrate. Any other components to be reflow soldered onto the substrate can be placed onto the substrate in a similar manner. Flip–chip assembly onto a ceramic substrate allows for some passive components, such as resistors, to be formed directly into the ceramic substrate circuit pattern itself. With all surface components to be mounted in place on the ceramic substrate, the assembly is moved into the furnace where it undergoes a specified temperature variation to solder all the components onto the ceramic substrate. This is accomplished by melting (reflowing) the substrate solder bumps. The resulting assembly should, after being cooled, be cleaned to remove any flux residues. If the substrate assembly is to be mounted into a module, it is recommended that the cavity of the module be filled with an appropriate silicon gel. The use of a gel coating helps to seal the individual components on the substrate from external moisture. A commonly used gel for this purpose is Dow Corning 562. As a final module assembly step, a cover is recommended to be placed over the ceramic assembly for further protection of the circuit.

It should be pointed out that the commonly used ceramic substrate material, though more expensive than other substrate materials, offers significantly superior thermal properties. By comparison, the use of ceramic material offers 33 times the thermal advantage of the second best material, Ceracom. The common FR–4 epoxy material is 100 times less thermally conductive than ceramic. For applications where dielectric constants are important and/or heat dissipation is not of real importance, other less costly materials can be used. The basic concept of the process is identical for all flip–chip substrates used.

Figure 10. Process Flow Diagram



Ceramic Substrate Preparation

The recommended ceramic substrate is aluminum oxide. These substrates come connected in what is referred to as a card. This is identical to the concept of die or chips on a wafer. Each card usually contains 8 to 16 substrates.

Initially, the ceramic should be precleaned with isopropyl alcohol, followed by freon. The bump pattern is then transferred onto the substrate using a metal stencil technique using a palladium silver conducting paste, such as DuPont 9476, through a #325 mesh. Once the pattern is applied, the substrate is dried for ten minutes at 150°C and then fired for 60 minutes at a temperature increasing to a peak of 850°C for ten additional minutes. Solder paste is then stenciled onto the pads.

A metal etched stencil defining the contact areas is recommended. The use of an etched stencil affords better solder paste control than does a silk screen. The metal stencil affords a deposition of a known amount of solder paste, thereby preventing bridging caused by excess solder usage.

Solder Paste Content

It is recommended that the solder paste consist of 10% tin, 88% lead, and 2% silver alloy. However, 95/3/2 compositions have had successful results.

A rosin based flux, such as RMA (Rosin Mildly Activated) manufactured by Dupont and having spherical particles of 45 to 75 microns, should be used. The tackiness of the solder paste at room temperature helps to hold the flip–chip in place during the pick and place operation. The use of flux:

1) Prevents excess oxidation during reflow.
2) Optimizes the flow of liquid solder through the stencil.
3) Smooths the surface by reducing surface tension, and
4) Enhances the normalization of surface tension upon reflow causing the flip–chip bumps to effectively auto–align themselves to substrate bump pads.

A solder mask can be used for applications requiring high precision as shown in Figures 11a and 11b.

Figure 11a. Before Reflow

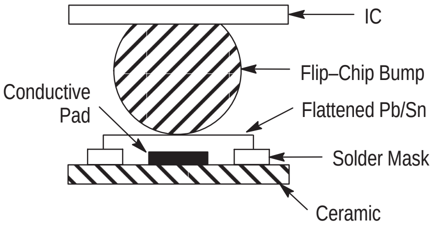
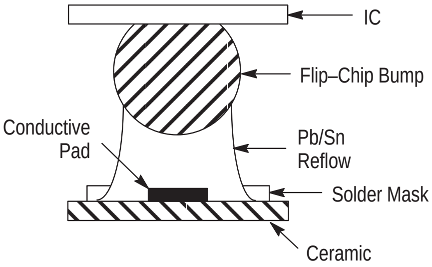


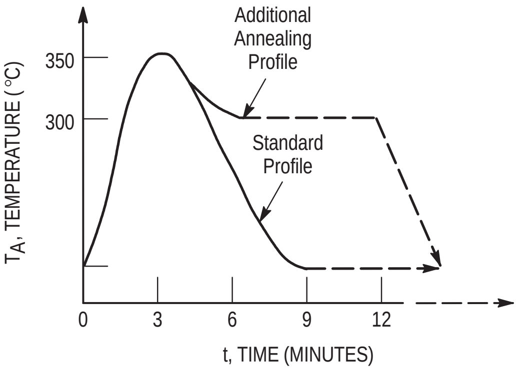
Figure 11b. After Reflow



Oven Profile

After the flip–chip is placed onto the bumped substrate, the substrate and flip–chip are ready for reflow. Initially, the flip–chip is heated to a peak temperature of around 300° to 350°C for five minutes. It is to be noted that the flip–chip bumps have a higher melting temperature than the bumps on the substrate. During assembly reflow, the substrate bumps melt and create a substrate to flip–chip bump bond. After reflow, the assembled part is cooled to room temperature or to some intermediate temperature point for annealing purposes.

Figure 12. Reflow Oven Profile



The oven temperature profile is established primarily to melt the solder while minimizing the alloying of the materials and keeping the flux from boiling away. It should be noted that when the flip–chip is placed onto the substrate, the material is stressed in one direction or another. The use of flux helps to reduce any surface stresses present. A reduction in the surface stress enhances solder wetting which in turn aids in the alignment of the flip–chip to the substrate. Poor solder wetting will produce misalignment as well as inferior bond strengths and reliability.

It is recommended that an inert atmosphere such as nitrogen be used during the reflow process to prevent oxidation.

Final Cleaning

The final cleaning involves removing the remaining flux from the flip–chip assembly. Three possible methods of removing flux are: ultrasonic cleaner, Terpene solvent and DI water, or vapor degreaser. The flux manufacturer should be able to recommend the proper type of vapor degreaser to be used.

Test and Reliability

Both visual inspection and shear strength testing should be performed on packaged flip–chip assemblies.

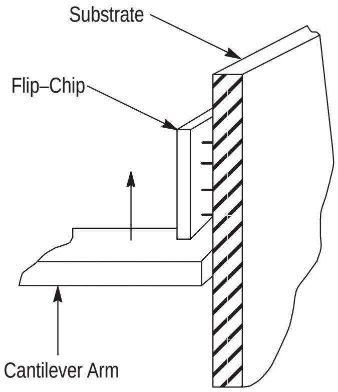
Solder reflow results that exhibit a grainy and dull appearance produce inferior bond shear strengths. Inferior bond shear strengths are visually recognizable by:

1) The presence of old or badly oxidized solder paste.
2) Insufficient amount of solderable material.
3) The contamination of bond pads with grease, oil, etc.

It should be mentioned that many contaminants are transparent and not easily detectable by visual means.

Shear strength testing should meet a 0.8 Newtons/Bump criteria. Shear strength testing should follow thermocycling of the chip from – 40° to +140°C to insure the stability of shear strength over temperature. Figure 13 depicts a test set–up which might possibly be used.

Figure 13. Shear Test Fixture



Aside from physical contamination, flip–chips, like any other chips, should not be handled directly due to the fact that electrostatic discharges can cause permanent damage to the electronic circuit. Flip–chips which do survive an electrostatic discharge can be left in a weakened condition resulting in reduced reliability of the end product. To avoid electrostatic damage of the circuit, assembly personnel should make use of a wrist strap or some other device to provide electrostatic grounding of their body. For the same reason, machinery used to assemble semiconductor circuits should be electrostaticly grounded.

Flip–chips rely primarily on the thermal path established by the bumps to remove heat from the chip as a result of internal circuit operation. Standard Motorola flip–chips have a thermal resistance of approximately 290°C/W/Bump. This figure can be used to estimate the allowed maximum power dissipation of the chip.

Cost and Equipment Manufacturers

The cost of implementing a flip–chip assembly process depends on the specific production requirements and as a result will vary over a broad range. It is possible to implement a small volume laboratory set–up for a few hundred dollars using manual operations. At the other end of the scale one could spend millions setting up a fully automated line incorporating pattern recognization, chip and substrate orientation, reflow, cleaning, and test. The module fabricator will have to make this assessment.

An assembly operator can manually accomplish the pick and place operation using a vacuum probe to pick–up and orient the flip–chip onto the substrate. Furthermore, it is possible to perform the reflow assembly operation using a simple batch process oven fabricated from a laboratory hot plate. However, the use of such process techniques will have questionable impact on the final product's reliability and quality. For this reason, it is highly recommended that the module fabricator seriously consider two major pieces of equipment; a pick and place machine and an infrared solder reflow oven. Both pieces of equipment can vary over a wide cost range depending on the production requirements. A partial list of manufacturers for this equipment is given below.

Pick and Place Machine:
- Universal Instruments Corp.
  Dover Technologies, Inc.
  Binghamton, NY 13902
  (607) 772–7522
- Seiko
  Torrance, CA 90505
  (310) 517–7850
- Laurier Inc.
  Hudson, NH 03051
  (603) 889–8800

Infrared Reflow Oven:
- BTU
  Bellerica, MA 01862
  (508) 667–4111
- Vitronics
  Newmarket, NH 03857
  (603) 659–6550

Additional Applications

Completed ceramic flip–chip sub–assemblies can be stacked one on top of another to produce an overall assembly by making contact connections through bumps. This technology is beginning to emerge in the computer industry where physical module size is of significant importance. Furthermore, this assembly technology, though more complex, is undergoing serious consideration within the automotive industry as well.

Applications requiring small size and high reliability at high ambient temperatures can benefit considerably through the implementation of flip–chip assembly techniques.

TCF6000

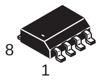
Peripheral Clamping Array

The TCF6000 was designed to protect input/output lines of microprocessor systems against voltage transients.

- Optimized for HMOS System
- Minimal Component Count
- Low Board Space Requirement
- No P.C.B. Track Crossovers Required
- Applications Areas Include Automotive, Industrial, Telecommunications and Consumer Goods

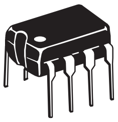
PERIPHERAL CLAMPING ARRAY

SEMICONDUCTOR
TECHNICAL DATA



D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

NO SUFFIX
PLASTIC PACKAGE
CASE 626



PIN CONNECTIONS

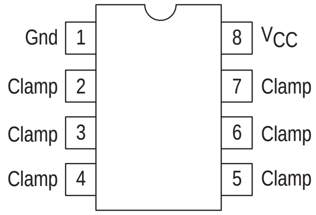
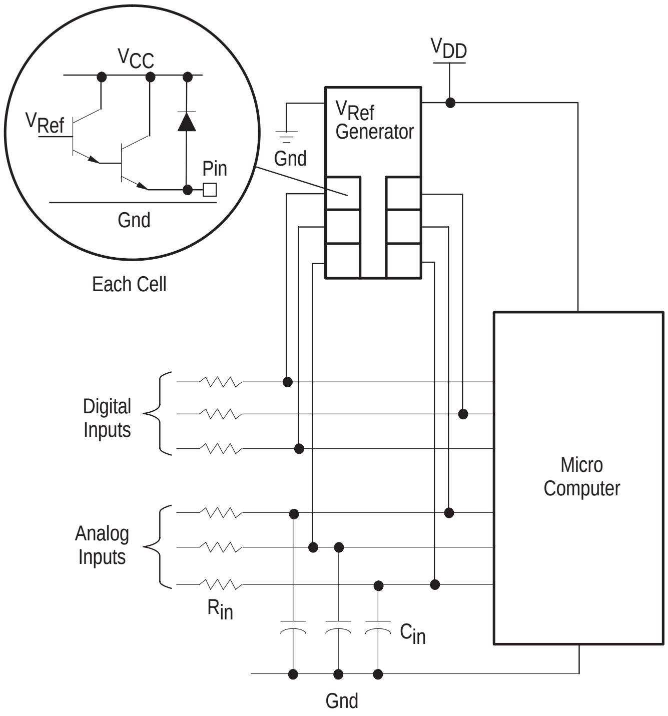


Figure 1. Representative Block Diagram and Simplified Application



ORDERING INFORMATION

Device	Operating Temperature Range	Package
TCF6000D	T_A = – 40° to +85°C	SO–8
TCF6000		Plastic DIP

MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted, Note 1.)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	6.0	V
Supply Current	I_i	300	mA
Clamping Current	I_{IK}	±50	mA
Junction Temperature	T_J	150	°C
Power Dissipation (T_A = + 85°C)	P_D	400	m/W
Thermal Resistance (Junction–Ambient)	θ_{JA}	100	°C/W
Operating Ambient Temperature Range	T_A	–40 to +85	°C
Storage Temperature Range	T_{stg}	–55 to + 150	°C

NOTE: 1. Values beyond which damage may occur.

ELECTRICAL CHARACTERISTICS (T_A = 25°C, 4.5 ≤ V_{CC} ≤ 5.5 V, unless otherwise noted.)

Characteristics	Symbol	Min	Max	Unit
Positive Clamping Voltage (Note 2) (I_{IK} = 10 mA, –40°C ≤ T_A ≤ + 85°C)	$V_{(IK)}$	–	V_{CC} + 1.0	V
Positive Peak Clamping Current	$I_{IK(P)}$	–	20	mA
Negative Peak Clamping Voltage (I_{IK} = –10 mA, –40°C ≤ T_A ≤ + 85°C)	$V_{(IK)}$	–0.3	–	V
Negative Peak Clamping Current	$I_{IK(P)}$	–20	–	mA
Output Leakage Current				μA
(0 V ≤ V_{in} ≤ V_{CC})	I_L	–	1.0	
(0 V ≤ V_{in} ≤ V_{CC}, –40°C ≤ T_A ≤ + 85°C)	I_{LT}	–	5.0	
Channel Crosstalk (A_{CT} = 20 log I_L/I_{IK})	A_{CT}	100	–	dB
Quiescent Current (Package)	I_B	–	2.0	mA

NOTE: 2. The device might not give 100% protection in CMOS applications.

CIRCUIT DESCRIPTION

To ensure the reliable operation of any integrated circuit based electronics system, care has been taken that voltage transients do not reach the device I/O pins. Most NMOS, HMOS and Bipolar integrated circuits are particularly sensitive to negative voltage peaks which can provoke latch–up or otherwise disturb the normal functioning of the circuit, and in extreme cases may destroy the device.

Generally the maximum rating for a negative voltage transients on integral circuits is –0.3 V over the whole temperature range. Classical protection units have consisted of diode/resistor networks as shown in Figures 2a and 2b.

The arrangement in Figure 2a does not, in general, meet the specification and is therefore inadequate.

The problem with the solution shown if Figure 2b lies mainly with the high current drain through the biassing devices R_1 and D_3. A second problem exists if the input line carries an analog signal. When V_{in} is close to the ground potential, currents arising from leakage and mismatch between D_3 and D_2 can be sourced into the input line, thus disturbing the reading.

Figure 2. Classical Protection Circuits

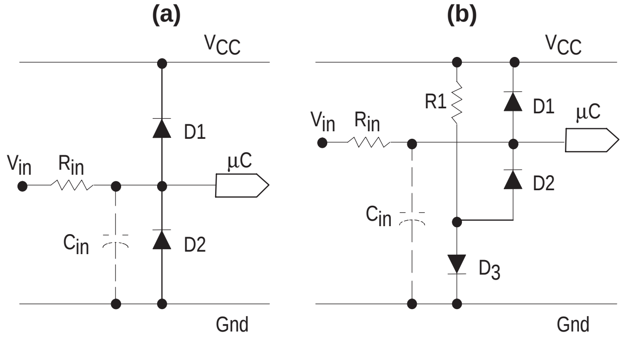
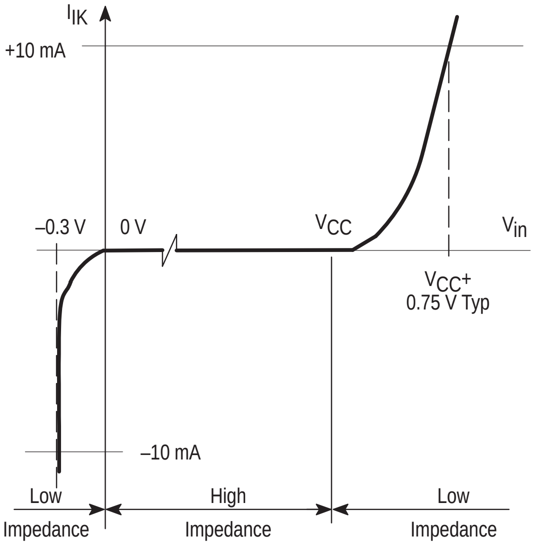


Figure 3 shows the clamping characteristics which are common to each of the six cells in the Peripheral Clamping Array.

As with the classical protection circuits, positive voltage transients are clamped by means of a fast diode to the V_{CC} supply line.

Figure 3. Clamping Characteristics



APPLICATIONS INFORMATION

Figure 4 depicts a typical application in a microcomputer based automotive ignition system.

The TCF6000 is being used not only to protect the system's normal inputs but also the (bidirectional) serial diagnostics port.

The value of the input resistors, R_{in}, is determined by the clamping current and the anticipated value of the spikes.

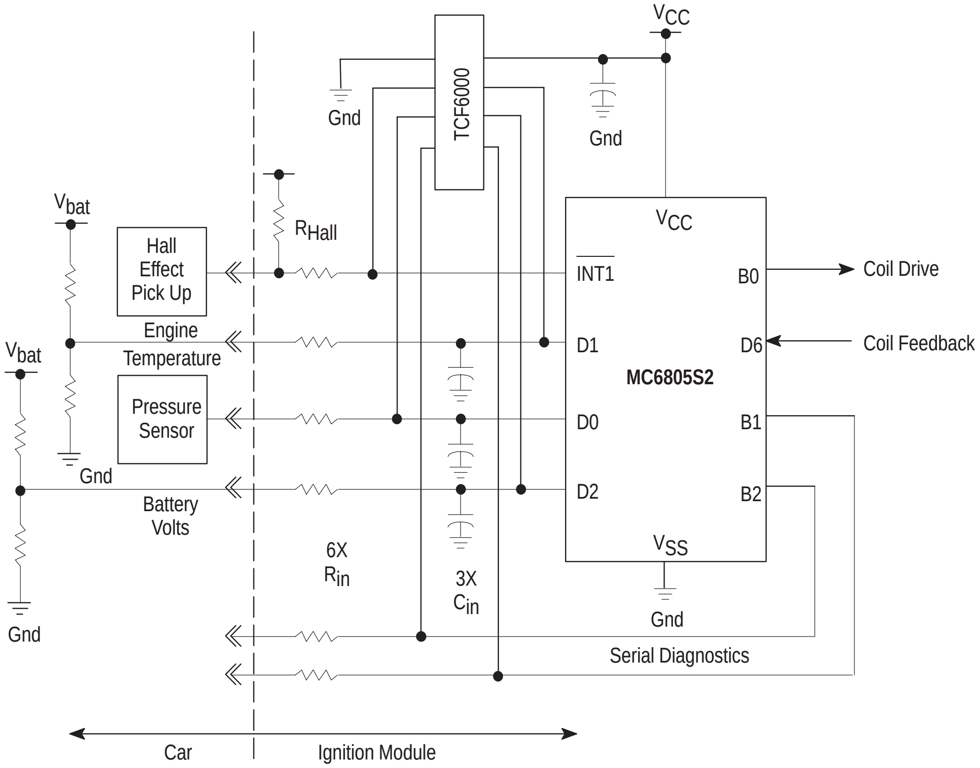
Thus:

$$R_{in} = \frac{V}{I_{IK}}\ \Omega$$

where: V = Peak Volts (V)
I_{IK} = Clamping current (A)
So, taking, V = 300 V typically (SAE J1211)
I_{IK} = 10 mA (recommended)
gives, R_{in} = 30 k

Resistors of this value will not usually cause any problems in MOS systems, but their presence needs to be taken into account by the designer. Their effect will normally need to be compensated for Bipolar systems.

Figure 4. Typical Automotive Application



The use of C_{in} is not mandatory, and is not recommended where the lines to be protected are used for output or for both input and output. For digital input lines, the use of a small capacitor in the range of 50 pF to 220 pF is recommended as this will reduce the rate of rise of voltage seen by the TCF6000 and hence the possibility of overshoot.

In the case of the analog inputs, such as that from the pressure sensor, the capacitor C_{in} is necessary for devices such as the MC6805S2 shown, which present a low impedance during the sampling period. The maximum value for C_{in} is determined by the accuracy required, the time taken to sample the input and the input impedance during that time, while the maximum value is determined by the required frequency response and the value of R_{in}.

Thus for a resistive input A/D connector where:

T_S = Sample time (seconds)
R_D = Device input resistance (Ω)
V_{in} = Input voltage (V)
k = Required accuracy (%)
Q_1 = Charge on capacitor before sampling
Q_2 = Charge on capacitor after sampling
I_D = Device input current (A)

Thus: $Q_1 – Q_2 = \frac{k \times Q_1}{100}$

but, $Q_1 = C_{in} V_{in}$
and, $Q_1 – Q_2 = I_D \bullet T_S$

so that, $I_D T_S = \frac{k \bullet C_{in} – V_{in}}{100}$

and, $C_{in} \text{ (min)} = \frac{I_D \bullet T_S}{V_{in} \bullet k}$ Farad

so, $C_{in} \text{ (min)} = \frac{100 \bullet T_S}{k \bullet R_D}$ Farad

The calculation for a sample and hold type converter is even simpler:

k = Required accuracy (%)
C_H = Hold capacitor (Farad)

$C_{in} \text{ (min)} = \frac{100 \bullet C_H}{k}$ Farad

For the MC6805S2 this comes out at:

$C_{in} \text{ (min)} = \frac{100.25 \text{ pF}}{0.25}$ = 10 nF for 1/4% accuracy

MOTOROLA

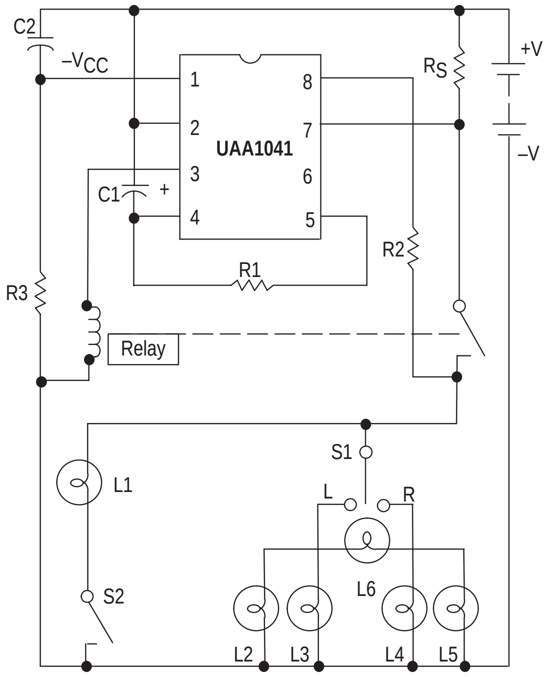
UAA1041B

Automotive Direction Indicator

This device was designed for use in conjunction with a relay in automotive applications. It is also applicable for other warning lamps such as “handbrake ON,” etc.

- Defective Lamp Detection
- Overvoltage Protection
- Short Circuit Detection and Relay Shutdown to Prevent Risk of Fire
- Reverse Battery Connection Protection
- Integrated Suppression Clamp Diode

Figure 1. Typical Automotive System



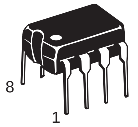
L1: 1.2 W, warning light handbrake ON
L2, L3, L4, L5: 21 W, turn signals

R1 = 75 k
R2 = 3.3 k
R3 = 220 Ω

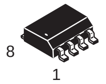
R_S = 30 mΩ
C1 = 5.6 µF
C2 = 0.047 µF

AUTOMOTIVE DIRECTION INDICATOR

SEMICONDUCTOR TECHNICAL DATA

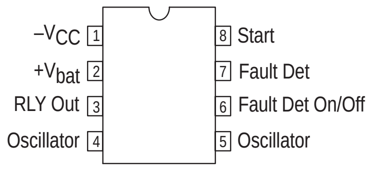


NO SUFFIX
PLASTIC PACKAGE
CASE 626



D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
UAA1041BD	T_A = – 40° to +100°C	SO–8
UAA1041B		Plastic DIP

MAXIMUM RATINGS

Rating	Pin	Value	Unit
Current: Continuous/Pulse*	1	+150/+500	mA
		–35/–500	
	2	±350/1900	
	3	±300/1400	
	8	±25/50	
Junction Temperature	T_J	150	°C
Operating Ambient Temperature Range	T_A	–40 to + 100	°C
Storage Temperature Range	T_{stg}	–65 to + 150	°C
Thermal Resistance, Junction–to–Ambient	$R_{\theta JA}$	100	°C/W (Typ)

* One pulse with an exponential decay and with a time constant of 500 ms.

ELECTRICAL CHARACTERISTICS (T_1 = 25°C)

Characteristics	Symbol	Min	Typ	Max	Unit
Battery Voltage Range (normal operation)	V_B	8.0	–	18	V
Overvoltage Detector Threshold (V_{Pin2}–V_{Pin1})	$D_{th(OV)}$	19	20.2	21.5	V
Clamping Voltage (V_{Pin2}–V_{Pin1})	V_{IK}	29	31.5	34	V
Short Circuit Detector Threshold (V_{Pin2}–V_{Pin7})	$D_{th(SC)}$	0.63	0.7	0.77	V
Output Voltage (I_{relay} = –250 mA) (V_{Pin2}–V_{Pin3})	V_O	–	–	1.5	V
Starter Resistance R_{st} = R_2 + R_{Lamp}	R_{st}	–	–	3.6	kΩ†
Oscillator Constant (normal operation)	Kn	1.4	1.5	1.6	–
Temperature Coefficient of Kn	Kn	–	$–1.5x10^{–3}$	–	1/°C
Duty Cycle (normal operation)	–	45	50	55	%
Oscillator Constant – (1 lamp defect of 21 W)	K_F	0.63	0.68	0.73	–
Duty Cycle (1 lamp defect of 21 W)	–	35	40	45	%
Oscillator Constant	K1	0.167	0.18	0.193	–
	K2	0.25	0.27	0.29	
	K3	0.126	0.13	0.14	
Current Consumption (relay off)	I_{CC}				mA
Pin 1; at V_{Pin2} – V_{Pin1} = 8.0 V		–	–0.9	–	
= 13.5 V		–2.5	–1.6	–1.0	
= 18 V		–	–2.2	–	
Current Consumption (relay on)	–				mA
Pin 1; at V_{Pin2} – V_{Pin1} = 8.0 V		–	–3.8	–	
= 13.5 V		–	–5.6	–	
= 18 V		–	–6.9	–	
Defect Lamp Detector Threshold at $V_{Pin}2$ to V_B = 8.0 V	V_{Pin2}–V_{Pin7}	–	68	–	mV
and R_3 = 220 Ω = 13.5 V	V_{Pin2}–V_{Pin7}	79	85.3	91	
= 18 V	V_{Pin2}–V_{Pin7}	–	100	–	

† See Note 1 of Application Information

CIRCUIT DESCRIPTION

The circuit is designed to drive the direction indicator flasher relay. Figure 2 shows the typical system configuration with the external components. It consists of a network (R1, C1) to determine the oscillator frequency, shunt resistor (R_S) to detect defective bulbs and short circuits in the system, and two current limiting resistors (R_2/R_3) to protect the IC against load dump transients. The circuit can be used either with or without short circuit detection, and features overvoltage, defective lamp and short circuit detection.

The lightbulbs L2, L3, L4, L5 are the turn signal indicators with the dashboard–light L6. When switch S1 is closed, after a time delay of t_1 (in our example t_1 = 75 ms), the relay will be actuated. The corresponding lightbulbs (L2, L3 or L4, L5) will flash at the oscillator frequency, independent of the battery voltage of 8.0 V to 18 V. The flashing cycle stops and the circuit is reset to the initial position when switch S1 is open.

Overvoltage Detection

Senses the battery voltage. When this voltage exceeds 20.2 V (this is the case when two batteries are connected in series), the relay will be turned off to protect the lightbulbs.

Lightbulb Defect Detector

Senses the current through the shunt resistor R_S. When one of the lightbulbs is defective, the failure is indicated by doubling the flashing frequency.

Short Circuit Detector

Detects excessive current (I_{sh} > 25 A) flowing in the shunt resistor R_S. The detection takes place after a time delay of t_3 (t_3 = 55 ms). In this case, the relay will be turned off. The circuit is reset by switching S1 to the off position.

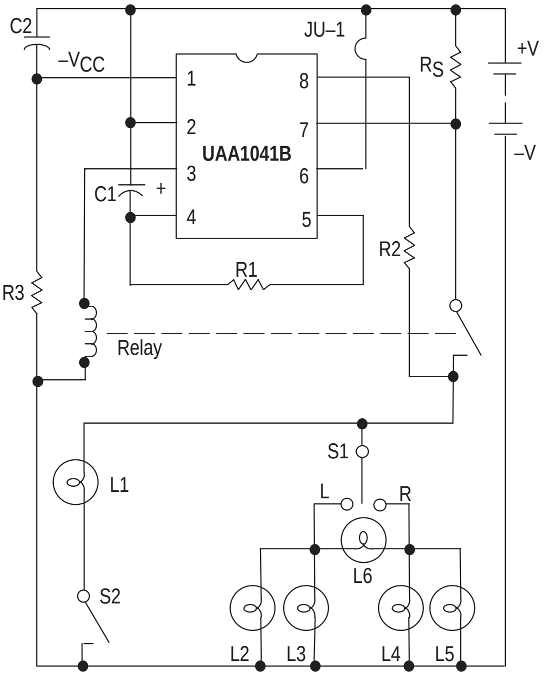
Operation with Short Circuit Detection

Pin 6 has to be left open and a capacitor C_2 has to be connected between Pin 1 and Pin 2.

Operation without Short Circuit Detection

Pin 6 has to be connected to Pin 2, and the use of capacitor C_2 is not necessary. The circuit can also be used for other warning flashers. In this example, when the handbrake is engaged, it is signaled by the light (L1).

Figure 2. Typical System Configuration



PARTS LIST

R1 = 75 kΩ
R2 = 3.3 kΩ
R3 = 220 Ω
R_S = 30 mΩ
Wire Resistor
C1 = 5.6 µF
C2 = 0.047 µF

Relay–Coil Resistance
Range 60 Ω to 800 Ω

Note: Per text connect
jumper JU–1 bypass
short circuit detector
C2 may be deleted also.

APPLICATION INFORMATION

1. The flashing cycle is started by closing S1. The switch position is sensed across resistor R_2 and R_{Lamp} by Input 8.

   $$R_{st} = R_2 + R_{Lamp}.$$

   The condition for the start is: R_{st} < 3.6 kΩ.
   For correct operation, leakage resistance from Pin 8 to ground must be greater than 5.6 kΩ.

2. Flashing frequency: $f_n = \dfrac{1}{R_1C_1K_n}$

3. Flashing frequency in the case of one defective lightbulb of 21 W:

   $$f_F = \frac{1}{R_1C_1K_F} \quad K_n = 2{,}2K_F$$

4. t_1: delay at the moment when S1 is closed and first flash
   $t_1 = K_1R_1C$
5. t_2: defective lightbulb detection delay $t_2 = K_2R_1C_1$
6. t_3: short circuit detection delay $t_3 = K_1R_1C_1$
   In the case of short circuit – it is assumed that the voltage (V_{Pin2}–V_{Pin1}) ≥ 8.0 V. The relay will be turned off after delay t_3. The circuit is reset by switching S1 to the off position.
7. The capacitor C2 is not obligatory when the short circuit detector is not used. In this case Pin 6 has to be connected to Pin 2.
8. When overvoltage is sensed (V_{Pin2} – V_{Pin1}) the relay is turned off to protect the relay and the lightbulbs against excessive currents.

Other Analog Circuits

In Brief . . .

Other analog circuits are provided for special applications with both bipolar and CMOS technologies. These circuits range from the industry standard analog timing circuits and multipliers to specialized CMOS smoke detectors. These products provide key functions in a wide range of applications, including data transmission, commercial smoke detectors, and various industrial controls.

Timing Circuits

These highly stable timers are capable of producing accurate time delays or oscillation. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor. For a stable operation as an oscillator, the free–running frequency and the duty cycle are both accurately controlled with two external resistors and one capacitor. The output structure can source or sink up to 200 mA or drive TTL circuits. Timing intervals from microseconds through hours can be obtained. Additional terminals are provided for triggering or resetting if desired.

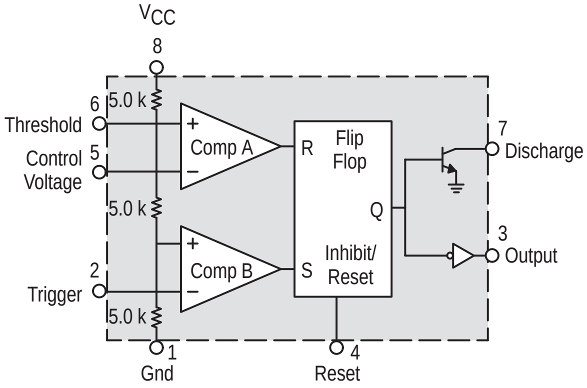
Singles

MC1455P1, D

T_A = 0° to +70°C, Case 626, 751

MC1455BP1, D

T_A = –40° to +85°C, Case 626, 751



Duals

MC3456P

T_A = 0° to +70°C, Case 646

NE556N, D

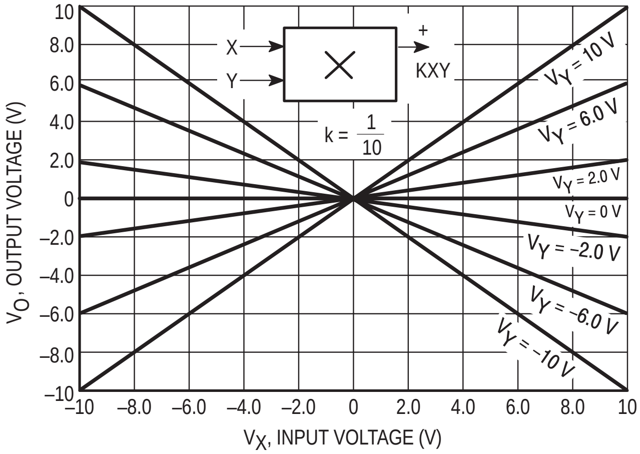
T_A = 0° to +70°C, Case 646, 751A

Multipliers

Linear Four–Quadrant Multipliers

Multipliers are designed for use where the output voltage is a linear product of two input voltages. Typical applications include: multiply, divide, square, root–mean–square, phase detector, frequency doubler, balanced modulator/demodulator, electronic gain control.

Multiplier Transfer Characteristics



MC1494P

T_A = 0° to +70°C, Case 648

This device has all the necessary internal regulation and references. The single–ended output is referenced to ground.

MC1495D, P

T_A = 0° to +70°C, Case 751A, 646

Maximum versatility is assured by allowing the user to select the level shift method.

MC1495BP

T_A = –40° to +125°C, Case 646

Linearity and offset are actually tested over temperature. This is an improved specification over previous versions.

Smoke Detectors (CMOS)

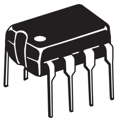
These smoke detector ICs require a minimum number of external components. When smoke is sensed, or a low battery voltage is detected, an alarm is sounded via an external piezoelectric transducer. All devices are designed to comply with UL specifications.

Table 1. Smoke Detectors (CMOS)

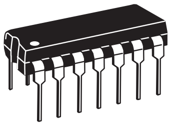
Function	Recommended Power Source	Unique Feature	Low Battery Detector	Piezoelectric Horn Driver	Complies with UL217 and UL268	Device Number	Suffix/ Package
Ionization–Type Smoke Detector	Battery	High Input Impedance FET Comparator	✓	✓	✓	MC14467–1	P1/646
	Line		–	–	✓	MC14578	P/648
Ionization–Type Smoke Detector with Interconnect	Battery		✓	✓	✓	MC14468	
	Line		–	✓	✓	MC14470	
Photoelectric–Type Smoke Detector with Interconnect	Battery	Photo Amplifier	✓	✓	✓	MC145010	P/648, DW/751G
	Line		(1)	✓	✓	MC145011	

(1) Low–supply detector.

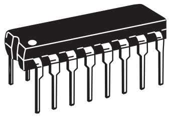
Other Analog Circuits Package Overview



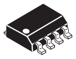
CASE 626
P1 SUFFIX



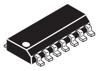
CASE 646
N, P, P1 SUFFIX



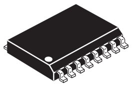
CASE 648
P SUFFIX



CASE 751
D SUFFIX



CASE 751A
D SUFFIX



CASE 751G
DW SUFFIX

Device Listing

Timing Circuits

Multipliers

MC1455, B

MOTOROLA

Timing Circuit

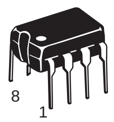
The MC1455 monolithic timing circuit is a highly stable controller capable of producing accurate time delays or oscillation. Additional terminals are provided for triggering or resetting if desired. In the time delay mode, time is precisely controlled by one external resistor and capacitor. For astable operation as an oscillator, the free–running frequency and the duty cycle are both accurately controlled with two external resistors and one capacitor. The circuit may be triggered and reset on falling waveforms, and the output structure can source or sink up to 200 mA or drive MTTL circuits.

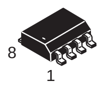
- Direct Replacement for NE555 Timers
- Timing from Microseconds through Hours
- Operates in Both Astable and Monostable Modes
- Adjustable Duty Cycle
- High Current Output Can Source or Sink 200 mA
- Output Can Drive MTTL
- Temperature Stability of 0.005% per °C
- Normally ON or Normally OFF Output

TIMING CIRCUIT

SEMICONDUCTOR
TECHNICAL DATA

P1 SUFFIX
PLASTIC PACKAGE
CASE 626



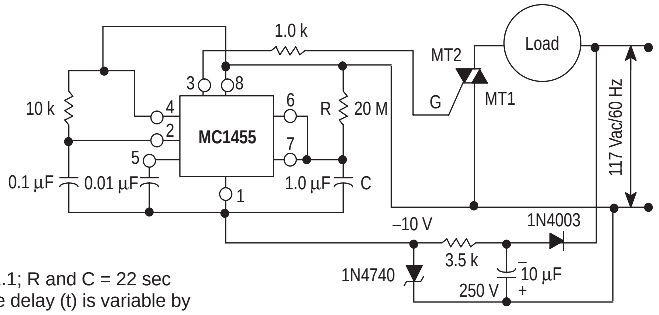


D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC1455P1	T_A = 0° to +70°C	Plastic DIP
MC1455D		SO–8
MC1455BD	T_A = – 40° to +85°C	SO–8
MC1455BP1		Plastic DIP

Figure 1. 22 Second Solid State Time Delay Relay Circuit



t = 1.1; R and C = 22 sec
Time delay (t) is variable by
changing R and C (see Figure 16).

Figure 2. Representative Block Diagram

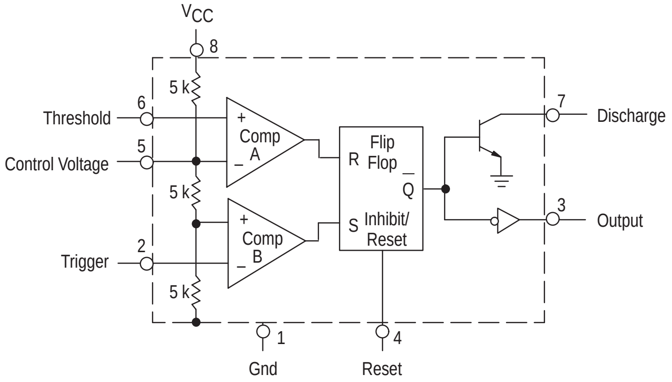
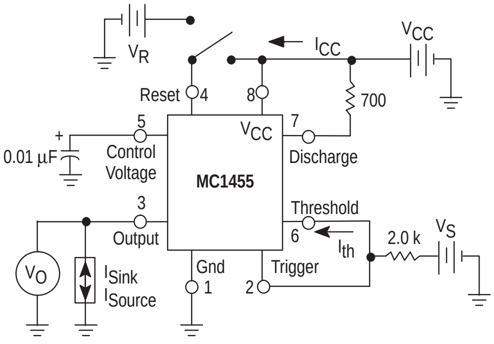


Figure 3. General Test Circuit



Test circuit for measuring DC parameters (to set output and measure parameters):

a) When $V_S \geq 2/3\ V_{CC}$, V_O is low.
b) When $V_S \leq 1/3\ V_{CC}$, V_O is high.
c) When V_O is low, Pin 7 sinks current. To test for Reset, set V_O high, apply Reset voltage, and test for current flowing into Pin 7. When Reset is not in use, it should be tied to V_{CC}.

MAXIMUM RATINGS (T_A = +25°C, unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	+18	Vdc
Discharge Current (Pin 7)	I_7	200	mA
Power Dissipation (Package Limitation)			
P1 Suffix, Plastic Package	P_D	625	mW
Derate above T_A = +25°C		5.0	mW/°C
D Suffix, Plastic Package	P_D	625	mW
Derate above T_A = +25°C		160	°C/W
Operating Temperature Range (Ambient)	T_A		°C
MC1455B		–40 to +85	
MC1455		0 to +70	
Storage Temperature Range	T_{stg}	–65 to +150	°C

ELECTRICAL CHARACTERISTICS (T_A = +25°C, V_{CC} = +5.0 V to +15 V, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Operating Supply Voltage Range	V_{CC}	4.5	–	16	V
Supply Current	I_{CC}				mA
V_{CC} = 5.0 V, $R_L = \infty$		–	3.0	6.0	
V_{CC} = 15 V, $R_L = \infty$, Low State (Note 1)		–	10	15	
Timing Error (R = 1.0 kΩ to 100 kΩ) (Note 2)					
Initial Accuracy C = 0.1 µF		–	1.0	–	%
Drift with Temperature		–	50	–	PPM/°C
Drift with Supply Voltage		–	0.1	–	%/V
Threshold Voltage/Supply Voltage	V_{th}/V_{CC}	–	2/3	–	
Trigger Voltage	V_T				V
V_{CC} = 15 V		–	5.0	–	
V_{CC} = 5.0 V		–	1.67	–	
Trigger Current	I_T	–	0.5	–	µA
Reset Voltage	V_R	0.4	0.7	1.0	V
Reset Current	I_R	–	0.1	–	mA
Threshold Current (Note 3)	I_{th}	–	0.1	0.25	µA
Discharge Leakage Current (Pin 7)	I_{dischg}	–	–	100	nA
Control Voltage Level	V_{CL}				V
V_{CC} = 15 V		9.0	10	11	
V_{CC} = 5.0 V		2.6	3.33	4.0	
Output Voltage Low	V_{OL}				V
I_{Sink} = 10 mA (V_{CC} = 15 V)		–	0.1	0.25	
I_{Sink} = 50 mA (V_{CC} = 15 V)		–	0.4	0.75	
I_{Sink} = 100 mA (V_{CC} = 15 V)		–	2.0	2.5	
I_{Sink} = 200 mA (V_{CC} = 15 V)		–	2.5	–	
I_{Sink} = 8.0 mA (V_{CC} = 5.0 V)		–	–	–	
I_{Sink} = 5.0 mA (V_{CC} = 5.0 V)		–	0.25	0.35	
Output Voltage High	V_{OH}				V
V_{CC} = 15 V (I_{Source} = 200 mA)		–	12.5	–	
V_{CC} = 15 V (I_{Source} = 100 mA)		12.75	13.3	–	
V_{CC} = 5.0 V (I_{Source} = 100 mA)		2.75	3.3	–	
Rise Time Differential Output	t_r	–	100	–	ns
Fall Time Differential Output	t_f	–	100	–	ns

NOTES: 1. Supply current when output is high is typically 1.0 mA less.
2. Tested at V_{CC} = 5.0 V and V_{CC} = 15 V Monostable mode.
3. This will determine the maximum value of $R_A + R_B$ for 15 V operation. The maximum total R = 20 mΩ.

Figure 4. Trigger Pulse Width

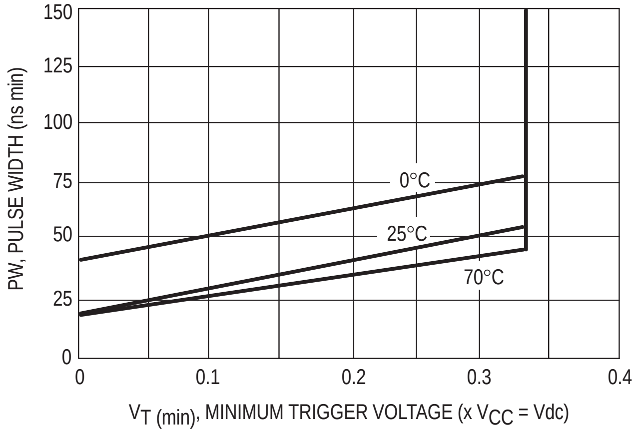


Figure 5. Supply Current

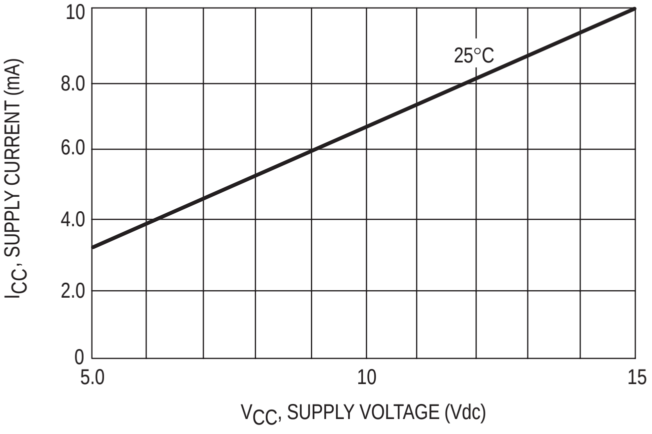


Figure 6. High Output Voltage

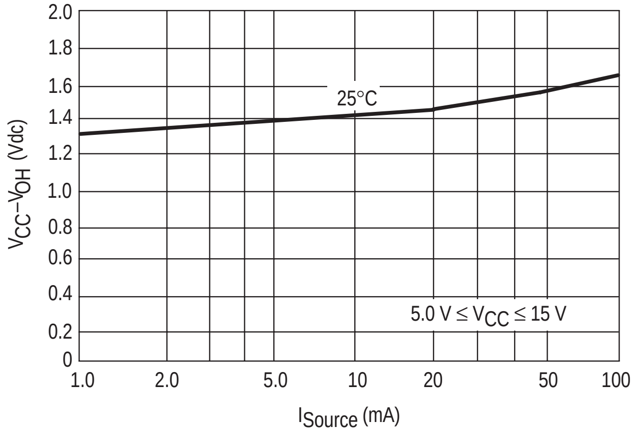


Figure 7. Low Output Voltage @ V_{CC} = 5.0 Vdc

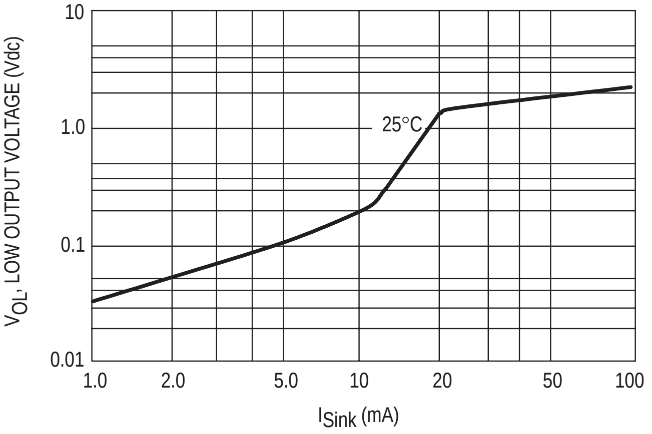


Figure 8. Low Output Voltage @ V_{CC} = 10 Vdc

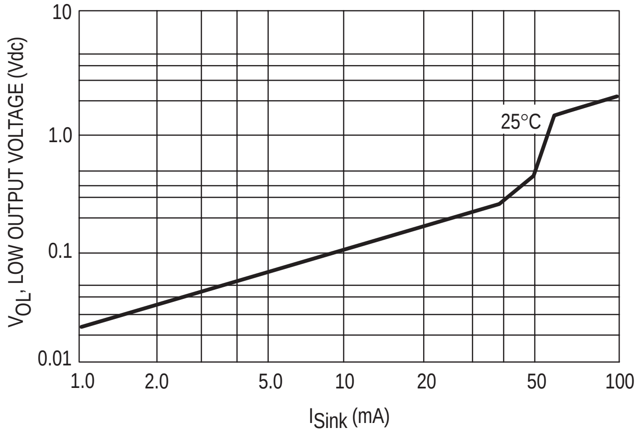
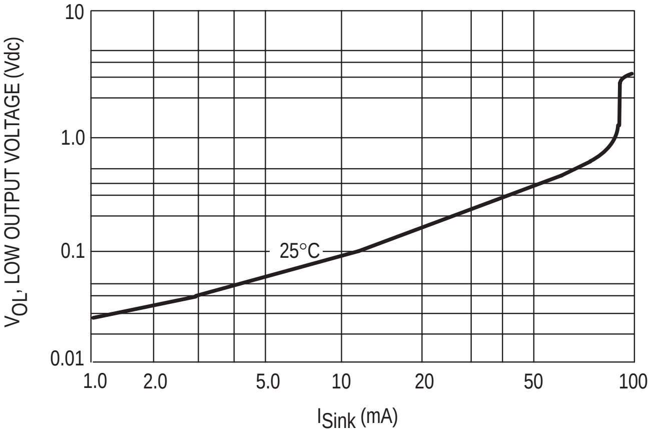


Figure 9. Low Output Voltage @ V_{CC} = 15 Vdc



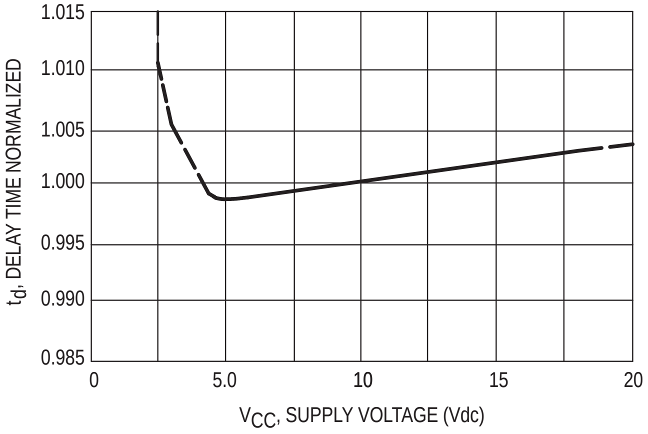


Figure 10. Delay Time versus Supply Voltage

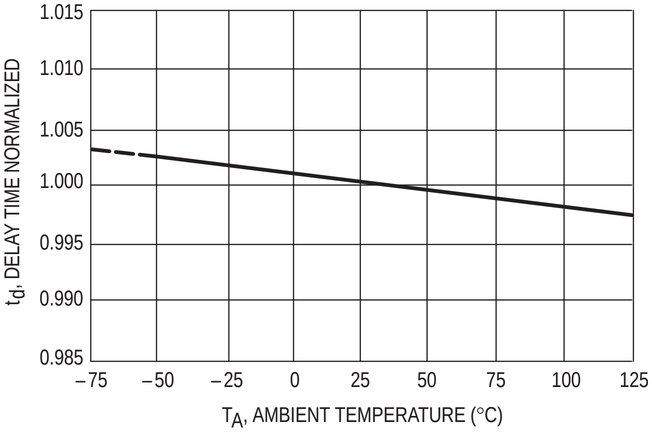


Figure 11. Delay Time versus Temperature

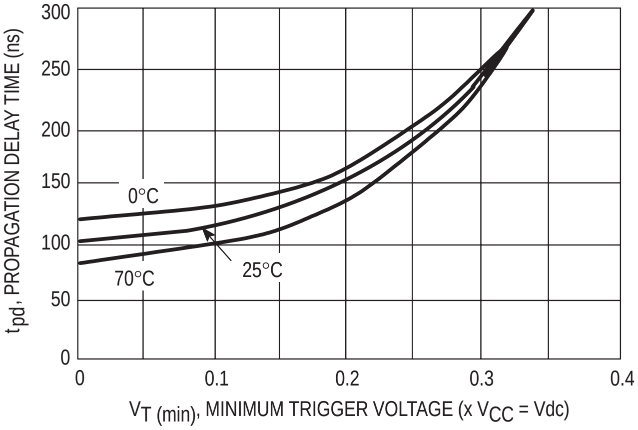
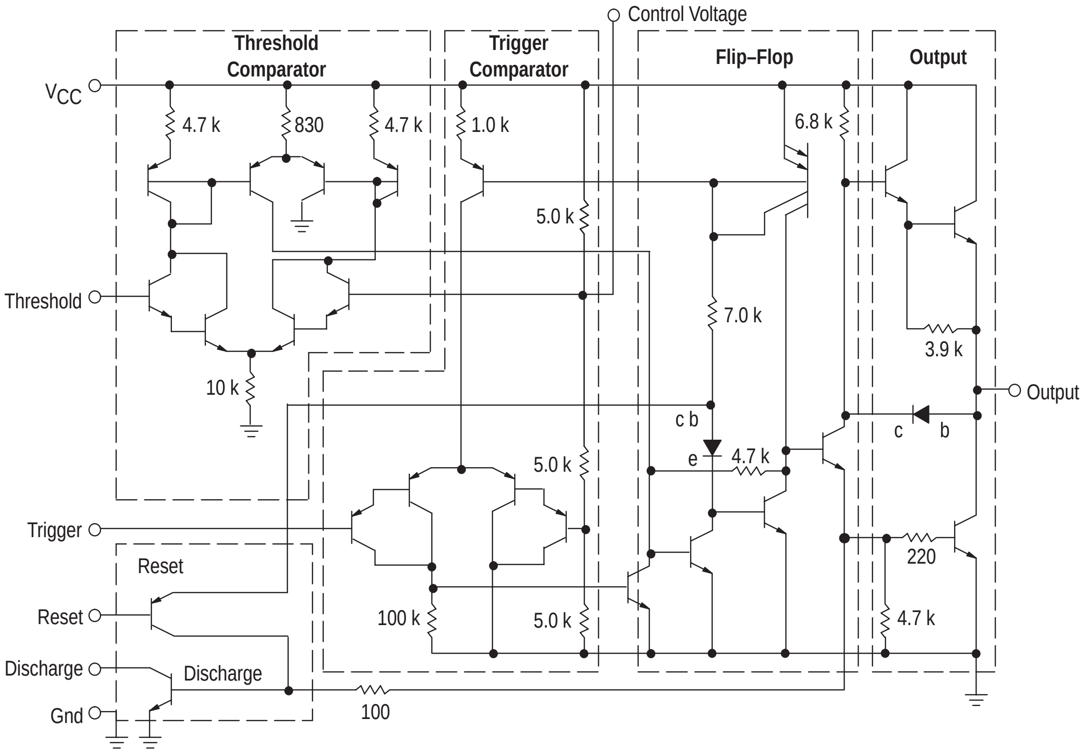


Figure 12. Propagation Delay versus Trigger Voltage

Figure 13. Representative Circuit Schematic



GENERAL OPERATION

The MC1455 is a monolithic timing circuit which uses an external resistor – capacitor network as its timing element. It can be used in both the monostable (one–shot) and astable modes with frequency and duty cycle controlled by the capacitor and resistor values. While the timing is dependent upon the external passive components, the monolithic circuit provides the starting circuit, voltage comparison and other functions needed for a complete timing circuit. Internal to the integrated circuit are two comparators, one for the input signal and the other for capacitor voltage; also a flip–flop and digital output are included. The comparator reference voltages are always a fixed ratio of the supply voltage thus providing output timing independent of supply voltage.

Monostable Mode

In the monostable mode, a capacitor and a single resistor are used for the timing network. Both the threshold terminal and the discharge transistor terminal are connected together in this mode (refer to circuit in Figure 14). When the input voltage to the trigger comparator falls below 1/3 V_{CC}, the comparator output triggers the flip–flop so that its output sets low. This turns the capacitor discharge transistor “off” and drives the digital output to the high state. This condition allows the capacitor to charge at an exponential rate which is set by the RC time constant. When the capacitor voltage reaches 2/3 V_{CC}, the threshold comparator resets the flip–flop. This action discharges the timing capacitor and returns the digital output to the low state. Once the flip–flop has been triggered by an input signal, it cannot be retriggered until the present timing period has been completed. The time that the output is high is given by the equation $t = 1.1\ R_A\ C$. Various combinations of R and C and their associated times are shown in Figure 16. The trigger pulse width must be less than the timing period.

A reset pin is provided to discharge the capacitor, thus interrupting the timing cycle. As long as the reset pin is low, the capacitor discharge transistor is turned “on” and prevents the capacitor from charging. While the reset voltage is applied the digital output will remain the same. The reset pin should be tied to the supply voltage when not in use.

Figure 14. Monostable Circuit

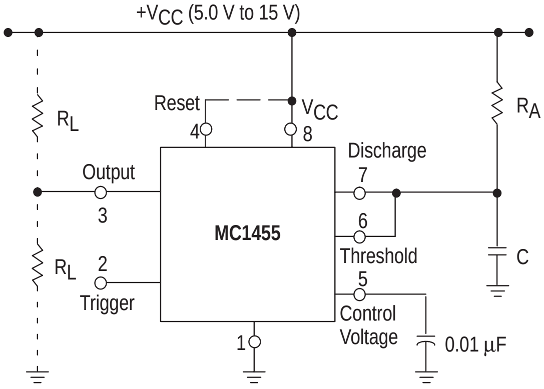
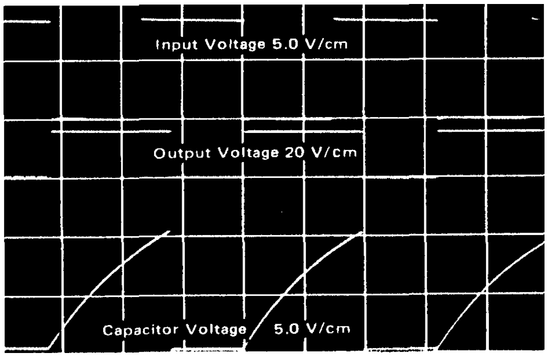


Figure 15. Monostable Waveforms



t = 50 µs/cm
(R_A = 10 kΩ, C = 0.01 µF, R_L = 1.0 kΩ, V_{CC} = 15 V)

Figure 16. Time Delay

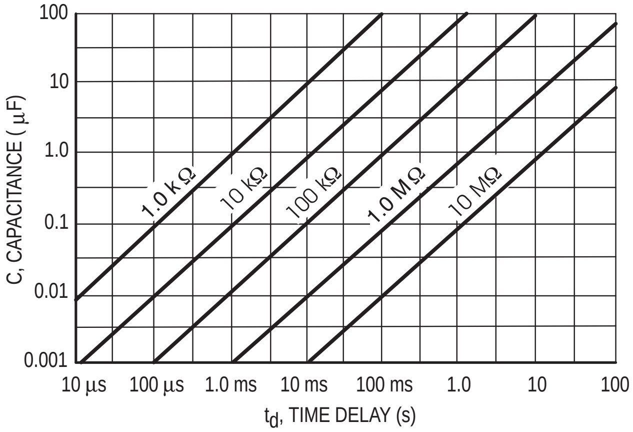


Figure 17. Astable Circuit

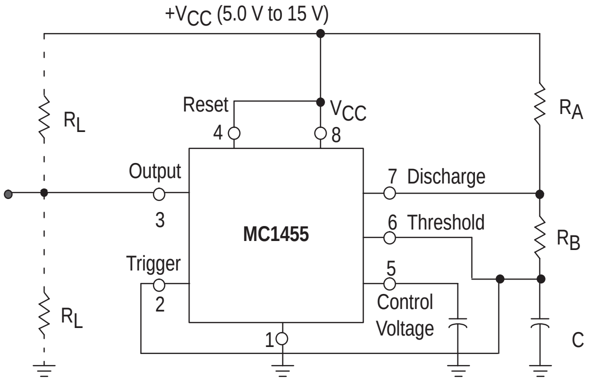
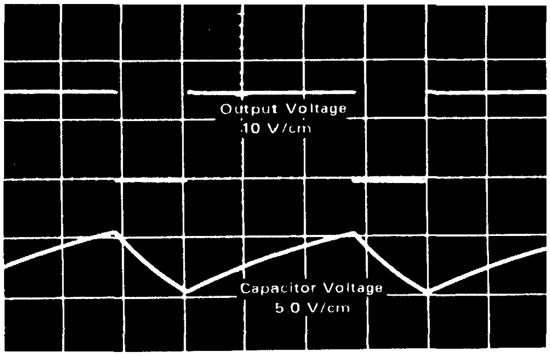


Figure 18. Astable Waveforms



t = 20 µs/cm
(R_A = 5.1 kΩ, C = 0.01 µF, R_L = 1.0 kΩ; R_B = 3.9 kΩ, V_{CC} = 15 V)

Astable Mode

In the astable mode the timer is connected so that it will retrigger itself and cause the capacitor voltage to oscillate between 1/3 V_{CC} and 2/3 V_{CC}. See Figure 17.

The external capacitor changes to 2/3 V_{CC} through R_A and R_B and discharges to 1/3 V_{CC} through R_B. By varying the ratio of these resistors the duty cycle can be varied. The charge and discharge times are independent of the supply voltage.

The charge time (output high) is given by:

$$t_1 = 0.695\ (R_A + R_B)\ C$$

The discharge time (output low) is given by:

$$t_2 = 0.695\ (R_B)\ C$$

Thus the total period is given by:

$$T = t_1 + t_2 = 0.695\ (R_A + 2R_B)\ C$$

The frequency of oscillation is then: $f = \frac{1}{T} = \frac{1.44}{(R_A + 2R_B)\ C}$

and may be easily found as shown in Figure 19.

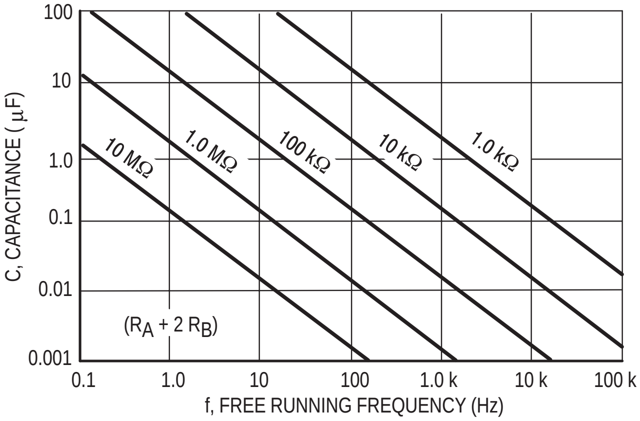
The duty cycle is given by: $DC = \frac{R_B}{R_A + 2R_B}$

To obtain the maximum duty cycle R_A must be as small as possible; but it must also be large enough to limit the discharge current (Pin 7 current) within the maximum rating of the discharge transistor (200 mA).

The minimum value of R_A is given by:

$$R_A \geq \frac{V_{CC}\ (\text{Vdc})}{I7\ (\text{A})} \geq \frac{V_{CC}\ (\text{Vdc})}{0.2}$$

Figure 19. Free Running Frequency



APPLICATIONS INFORMATION

Linear Voltage Ramp

In the monostable mode, the resistor can be replaced by a constant current source to provide a linear ramp voltage. The capacitor still charges from 0 V_{CC} to 2/3 V_{CC}. The linear ramp time is given by:

$$t = \frac{2}{3}\,\frac{V_{CC}}{1}, \quad \text{where } I = \frac{V_{CC} - V_B - V_{BE}}{R_E}$$

If V_B is much larger than V_{BE}, then t can be made independent of V_{CC}.

Missing Pulse Detector

The timer can be used to produce an output when an input pulse fails to occur within the delay of the timer. To accomplish this, set the time delay to be slightly longer than the time between successive input pulses. The timing cycle is then continuously reset by the input pulse train until a change in frequency or a missing pulse allows completion of the timing cycle, causing a change in the output level.

Figure 20. Linear Voltage Sweep Circuit

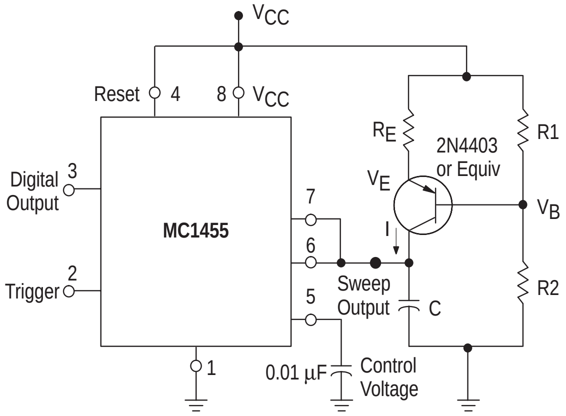


Figure 21. Missing Pulse Detector

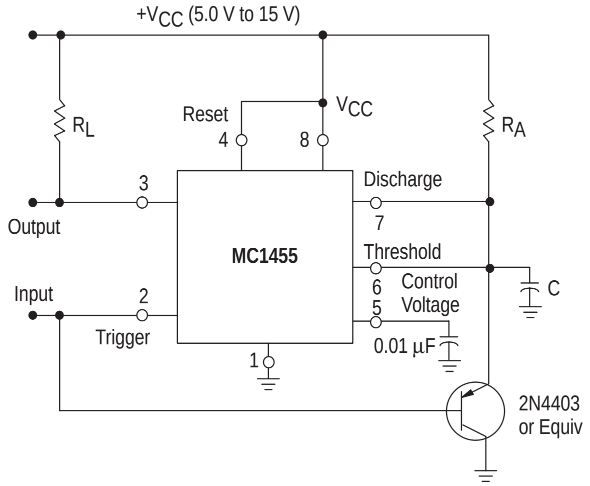
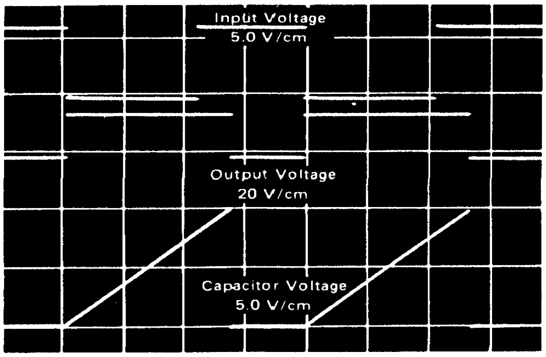


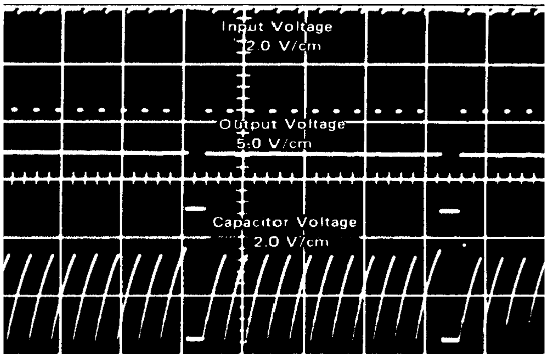
Figure 22. Linear Voltage Ramp Waveforms



t = 100 µs/cm

(R_E = 10 kΩ, R2 = 100 kΩ, R1 = 39 kΩ, C = 0.01 µF, V_{CC} = 15 V)

Figure 23. Missing Pulse Detector Waveforms



t = 500 µs/cm

(R_A = 2.0 kΩ, R_L = 1.0 kΩ, C = 0.01 µF, V_{CC} = 15 V)

Pulse Width Modulation

If the timer is triggered with a continuous pulse train in the monstable mode of operation, the charge time of the capacitor can be varied by changing the control voltage at Pin 5. In this manner, the output pulse width can be modulated by applying a modulating signal that controls the threshold voltage.

Figure 24. Pulse Width Modulator

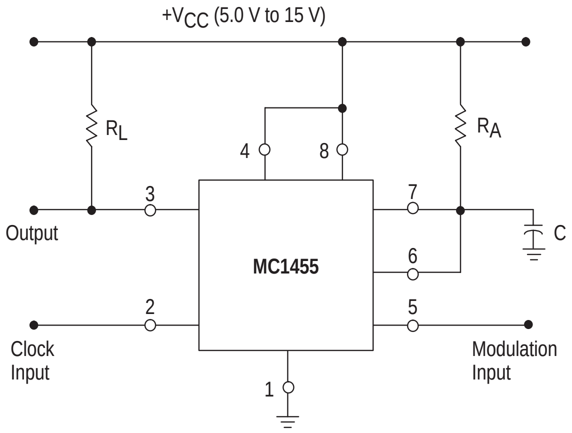
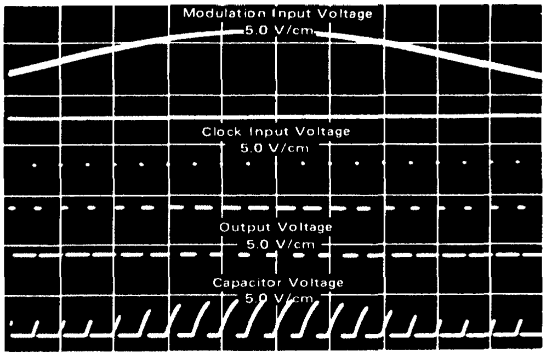


Figure 25. Pulse Width Modulation Waveforms

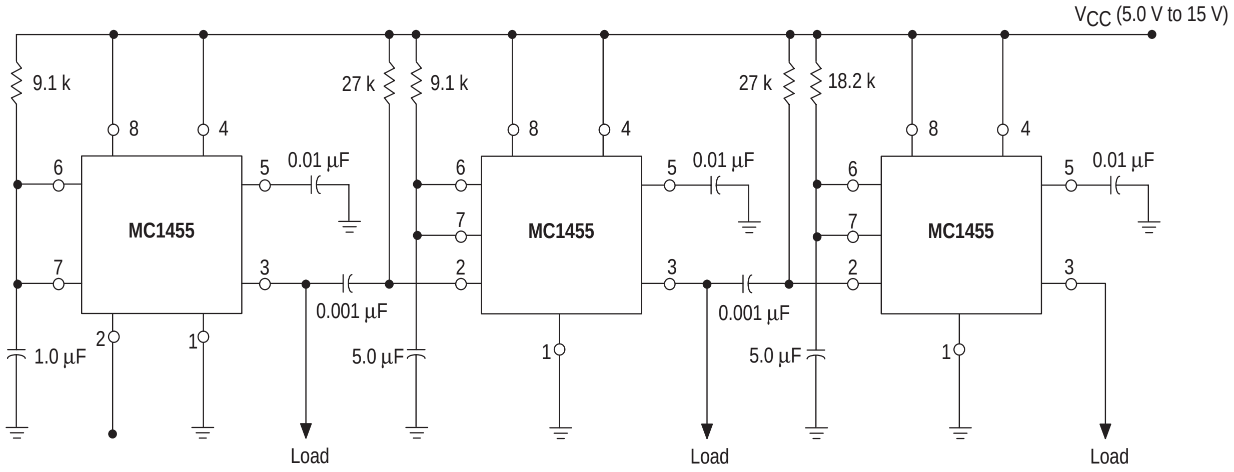


t = 0.5 ms/cm
(R_A = 10 kΩ, C = 0.02 µF, V_{CC} = 15 V)

Test Sequences

Several timers can be connected to drive each other for sequential timing. An example is shown in Figure 26 where the sequence is started by triggering the first timer which runs for 10 ms. The output then switches low momentarily and starts the second timer which runs for 50 ms and so forth.

Figure 26. Sequential Timer



MOTOROLA

MC1494

Linear Four-Quadrant Multiplier

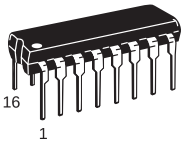
The MC1494 is designed for use where the output voltage is a linear product of two input voltages. Typical applications include: multiply, divide, square root, mean square, phase detector, frequency doubler, balanced modulator/ demodulator, electronic gain control.

The MC1494 is a variable transconductance multiplier with internal level–shift circuitry and voltage regulator. Scale factor, input offsets and output offset are completely adjustable with the use of four external potentiometers. Two complementary regulated voltages are provided to simplify offset adjustment and improve power supply rejection.

- Operates with ±15 V Supplies
- Excellent Linearity: Maximum Error (X or Y) ±1.0 %
- Wide Input Voltage Range: ±10 V
- Adjustable Scale Factor, K (0.1 nominal)
- Single–Ended Output Referenced to Ground
- Simplified Offset Adjust Circuitry
- Frequency Response (3.0 dB Small–Signal): 1.0 MHz
- Power Supply Sensitivity: 30 mV/V typical

LINEAR FOUR–QUADRANT MULTIPLIER INTEGRATED CIRCUIT

SEMICONDUCTOR TECHNICAL DATA



P SUFFIX
PLASTIC PACKAGE
CASE 648C

ORDERING INFORMATION

Device	Tested Operating Temperature Range	Package
MC1494P	T_A = 0° to + 70°C	Plastic DIP

Figure 1. Multiplier Transfer Characteristic

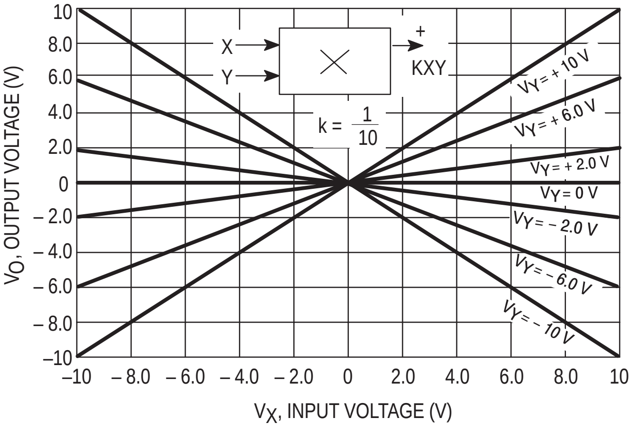
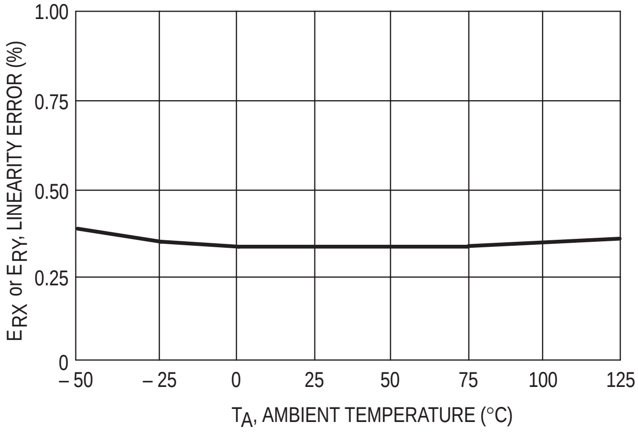


Figure 2. Linearity Error versus Temperature



MAXIMUM RATINGS (T_A = + 25°C, unless otherwise noted.)

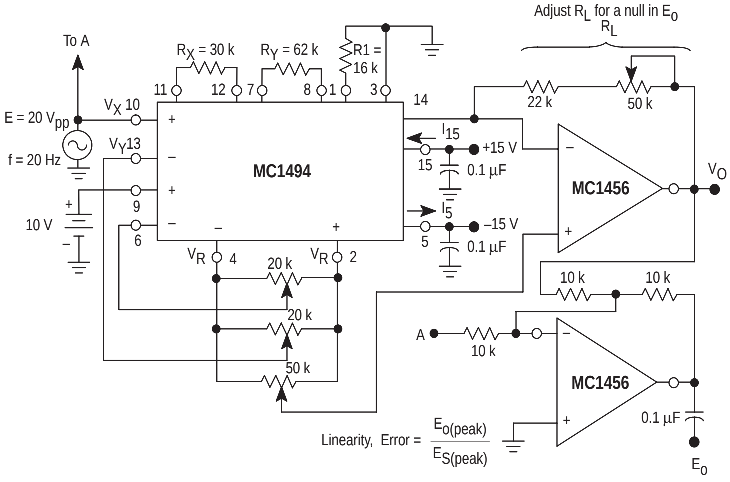
Rating	Symbol	Value	Unit
Power Supply Voltages	± V	± 18	Vdc
Differential Input Signal	$V_9 – V_6$ $V_{10} – V_{13}$	$\pm\lvert 6 + I_1R_Y \rvert < 30$ $\pm\lvert 6 + I_1R_X \rvert < 30$	Vdc
Common Mode Input Voltage $V_{CMY} = V_9 = V_6$ $V_{CMX} = V_{10} = V_{13}$	V_{CMY} V_{CMX}	±11.5 ±11.5	Vdc
Power Dissipation (Package Limitation) T_A = + 25°C Derate above T_A = + 25°C	P_D $1/\theta_{JA}$	1.25 20	W mW/°C
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	– 65 to +150	°C

ELECTRICAL CHARACTERISTICS (±V = ±15 V, T_A = + 25°C, R1 = 16 kΩ, R_X = 30 kΩ, R_Y = 62 kΩ, R_L = 47 kΩ, unless otherwise noted.)

Characteristics	Figure	Symbol	Min	Typ	Max	Unit
Linearity	3	E_{RX} or E_{RY}				%
Output error in percent of full scale						
–10 V < V_X < +10 V (V_Y = ±10 V)						
–10 V < V_Y < +10 V (V_X = ±10 V)						
T_A = +25°C			–	±0.5	±1.0	
$T_A = T_{high}$ or T_{low} (Note 1)			–	–	±1.3	
Input	4, 5, 6					
Voltage Range ($V_X = V_Y = V_{in}$)		V_{in}	±10	–	–	V_{pk}
Resistance (X or Y Input)		R_{in}	–	300	–	MΩ
Offset Voltage (X Input) (Note 1)		$\lvert V_{iox} \rvert$	–	0.2	2.5	V
(Y Input) (Note 1)		$\lvert V_{ioy} \rvert$	–	0.8	2.5	
Bias Current (X or Y Input)		I_b	–	1.0	2.5	µA
Offset Current (X or Y Input)		$\lvert I_{io} \rvert$	–	50	400	nA
Output	5, 6					
Voltage Swing Capability		V_O	±10	–	–	V_{pk}
Impedance		R_O	–	850	–	kΩ
Offset Voltage (Note 1)		$\lvert V_{OO} \rvert$	–	1.2	2.5	V
Offset Current (Note 1)		$\lvert I_{OO} \rvert$	–	25	52	µA
Temperature Stability (Drift)	–					
$T_A = T_{high}$ to T_{low}						
Output Offset (X = 0, Y = 0) Voltage		$\lvert TCV_{OO} \rvert$	–	1.3	–	mV/°C
Current		$\lvert TCI_{OO} \rvert$	–	27	–	nA/°C
X Input Offset (Y = 0)		$\lvert TCV_{iox} \rvert$	–	0.3	–	mV/°C
Y Input Offset (X = 0)		$\lvert TCV_{ioy} \rvert$	–	1.5	–	
Scale Factor		$\lvert TCK \rvert$	–	0.07	–	%/°C
Total DC Accuracy Drift (X = 10, Y = 10)		$\lvert TCE \rvert$	–	0.09	–	
Dynamic Response	7					
Small Signal (3.0 dB)		BW_{3dB} (X)	–	0.8	–	MHz
		BW_{3dB} (Y)	–	1.0	–	
Power Bandwidth (47 k)		P_{BW}	–	440	–	kHz
3° Relative Phase Shift		$f\phi$	–	240	–	
1% Absolute Error		$f\theta$	–	30	–	
Common Mode	8					
Input Swing (X or Y)		CMV	±10.5	–	–	V_{pk}
Gain (X or Y)		A_{CM}	–	– 65	–	dB
Power Supply	9					
Current		I_d+	–	6.0	12	mAdc
		$I_d–$	–	6.5	12	
Quiescent Power Dissipation		P_D	–	185	350	mW
Sensitivity		S+	–	13	100	mV/V
		S–	–	30	200	
Regulated Offset Adjust Voltages	9					
Positive/Negative		V_R+, $V_R–$	3.5	4.3	5.0	Vdc
Temperature Coefficient (V_R+ or $V_R–$)		TCV_R	–	0.03	–	mV/°C
Power Supply Sensitivity (V_R+ or $V_R–$)		S_R+, $S_R–$	–	0.6	–	mV/V

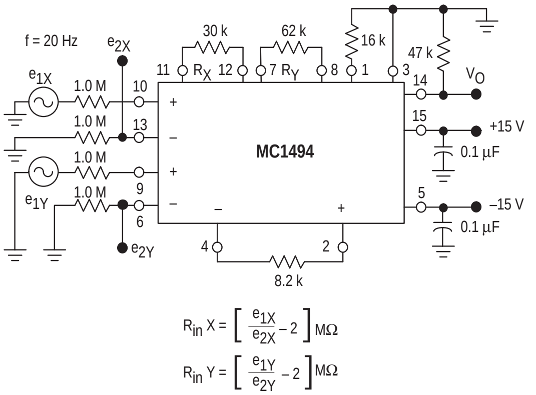
NOTE: 1. Offsets can be adjusted to zero with external potentiomers. T_{High} = +70°C, T_{Low} = 0°C

Figure 3. Linearity



$$\text{Linearity, Error} = \frac{E_{o(peak)}}{E_{S(peak)}}$$

Figure 4. Input Resistance



$$R_{in}\,X = \left[\frac{e_{1X}}{e_{2X}} - 2\right] M\Omega$$

$$R_{in}\,Y = \left[\frac{e_{1Y}}{e_{2Y}} - 2\right] M\Omega$$

Figure 5. Offset Voltages, Gain

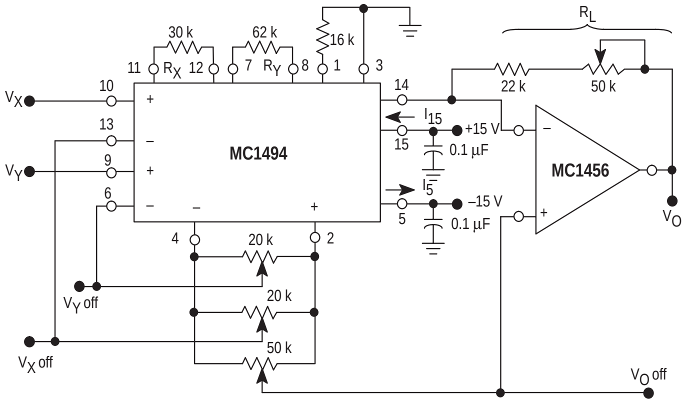


Figure 6. Input Bias Current/Input Offset Current, Output Resistance

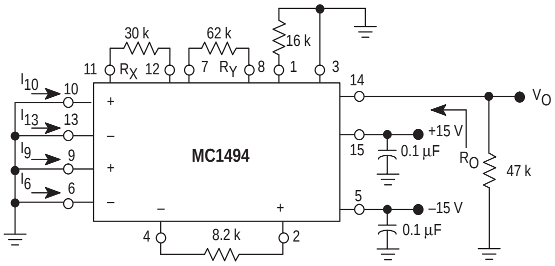


Figure 7. Frequency Response

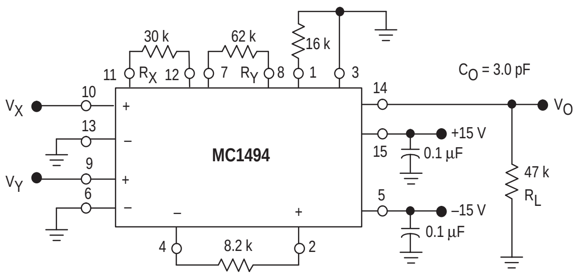


Figure 8. Common Mode

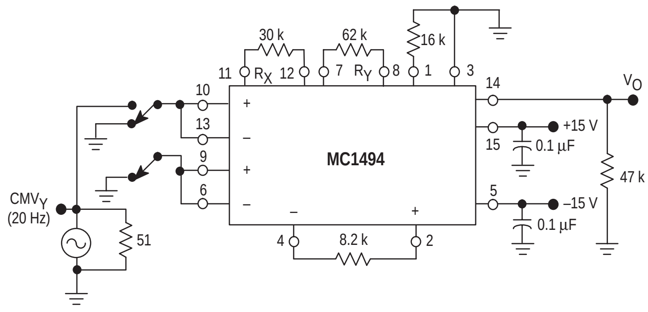


Figure 9. Power Supply Sensitivity

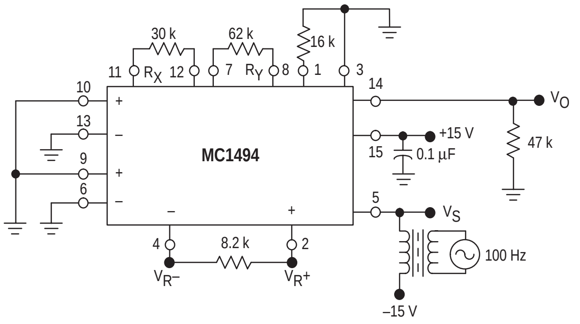


Figure 10. Burn–In

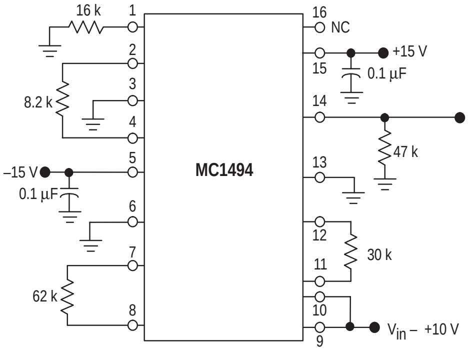


Figure 11. Frequency Response of Y Input versus Load Resistance

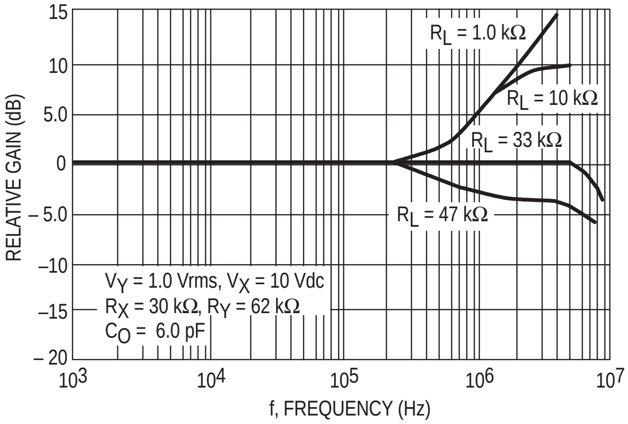


Figure 12. Frequency Response of X Input versus Load Resistance

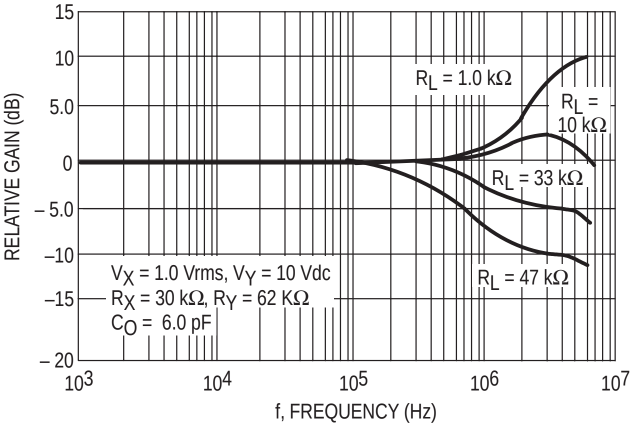


Figure 13. Linearity versus R_X or R_Y with K = 1

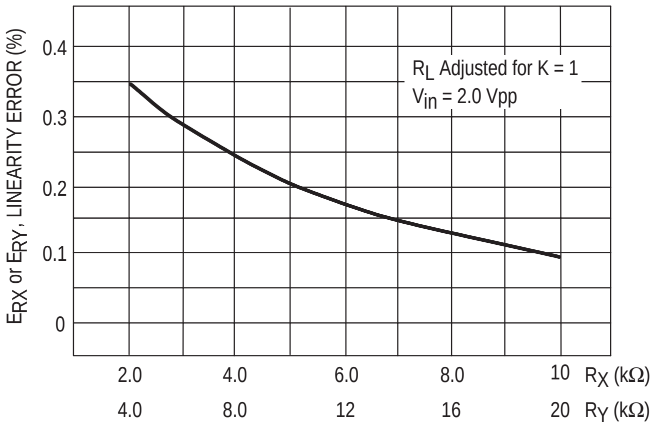


Figure 14. Linearity versus R_X or R_Y with K = 1/10

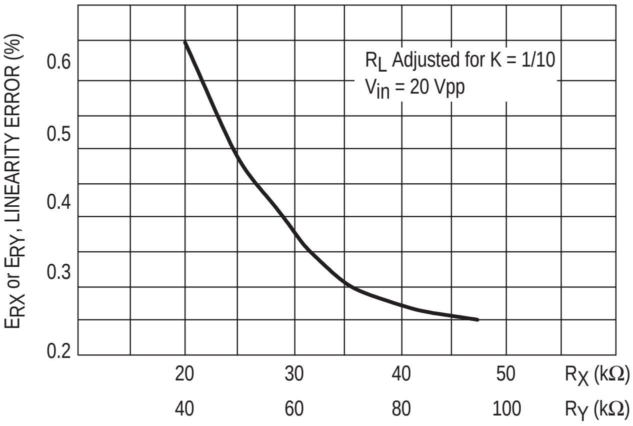


Figure 15. Large Signal Voltage versus Frequency

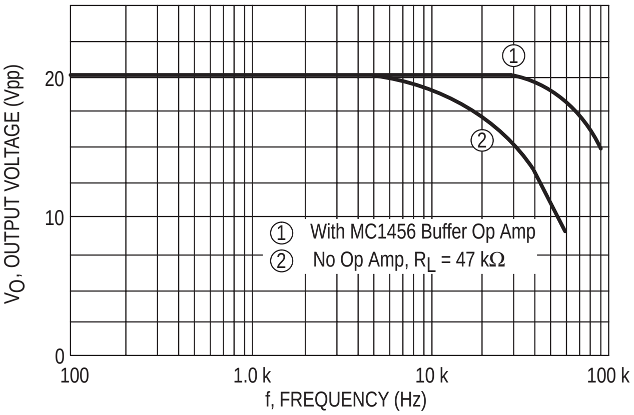
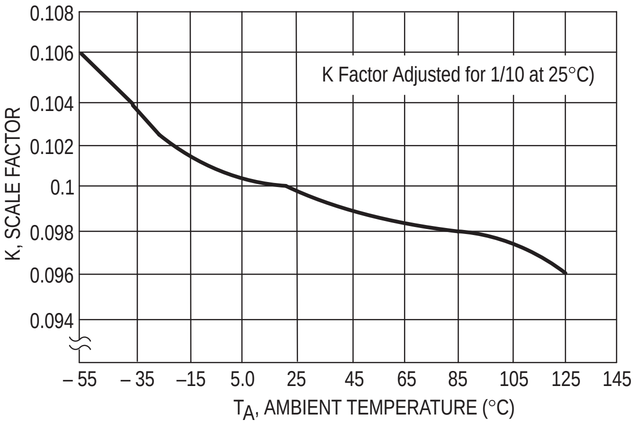


Figure 16. Scale Factor (K) versus Temperature



CIRCUIT DESCRIPTION

Introduction

The MC1494 is a monolithic, four–quadrant multiplier that operates on the principle of variable transconductance. It features a single–ended current output referenced to ground and provides two complementary regulated voltages for use with the offset adjust circuits to virtually eliminate sensitivity of the offset voltage nulls to changes in supply voltages.

As shown in Figure 17, the MC1494 consists of a multiplier proper and associated peripheral circuitry to provide these features.

Regulator

The regulator biases the entire MC1494 circuit making it essentially independent of supply variation. It also provides two convenient regulated supply voltages which can be used in the offset adjust circuitry. The regulated output voltage at Pin 2 is approximately + 4.3 V, while the regulated voltage at Pin 4 is approximately – 4.3 V. For optimum temperature stability of these regulated voltages, it is recommended that $|I_2| = |I_4| = 1.0$ mA (equivalent load of 8.6 kΩ). As will be shown later, there will normally be two 20 kΩ potentiometers and one 50 kΩ potentiometer connected between Pins 2 and 4.

The regulator also establishes a constant current reference that controls all of the constant current sources in the MC1494. Note that all current sources are related to current I_1 which is determined by R1. For best temperatures performance, R1 should be 16 kΩ so that $I_1 \approx 0.5$ mA for all applications.

Multiplier

The multiplier section of the MC1494 (center section of Figure 17) is nearly identical to the MC1495 and is discussed in detail in Application Note AN489, *Analysis and Basic Operation of the MC1495*. The result of this analysis is that the differential output current of the multiplier is given by:

$$I_A - I_B = \Delta I \approx \frac{2V_X\,V_Y}{R_X R_Y I_1}$$

Therefore, the output is proportional to the product of the two input voltages.

Differential Current Converter

This portion of the circuitry converts the differential output current ($I_A - I_B$) of the multiplier to a single–ended output current (I_O); $I_O = I_A - I_B$

$$\text{or} \quad I_O = \frac{2V_X\,V_Y}{R_X R_Y I_1}$$

The output current can be easily converted to an output voltage by placing a load resistor R_L from the output (Pin 14) to ground (Figure 19) or by using an op amp as a current–to–voltage converter (Figure 18). The result in both circuits is that the output voltage is given by:

$$V_O = \frac{2R_L\,V_X\,V_Y}{R_X R_Y I_1} = KV_X V_Y$$

$$\text{where, K (scale factor)} = \frac{2R_L}{R_X R_Y I_1}$$

DC OPERATION

Selection of External Components

For low frequency operation the circuit of Figure 18 is recommended. For this circuit, $R_X = 30$ kΩ, $R_Y = 62$ kΩ, R1 = 16 kΩ and, hence, $I_1 \approx 0.5$ mA. Therefore, to set the scale factor (K) equal to 1/10, the value of R_L can be calculated to be:

$$K = \frac{1}{10} = \frac{2R_L}{R_X R_Y I_1}$$

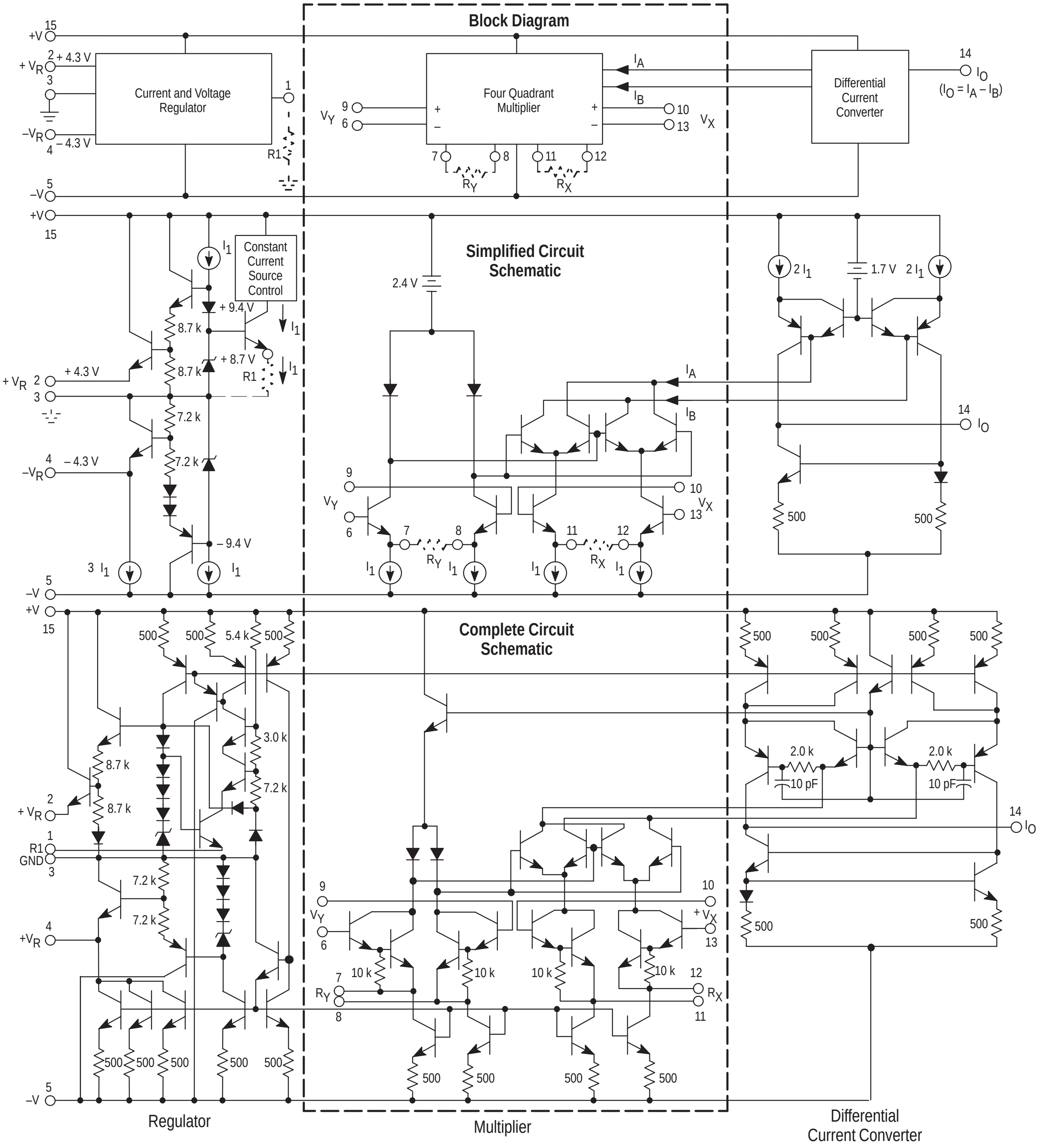
$$\text{or} \quad R_L = \frac{R_X R_Y I_1}{(2)\,(10)} = \frac{(30\text{ k})\,(62\text{ k})\,(0.5\text{ mA})}{20}$$

$$R_L = 46.5\text{ k}$$

Thus, a reasonable accuracy in scale factor can be achieved by making R_L a fixed 47 kΩ resistor. However, if it is desired that the scale factor be exact, R_L can be comprised of a fixed resistor and a potentiometer as shown in Figure 18.

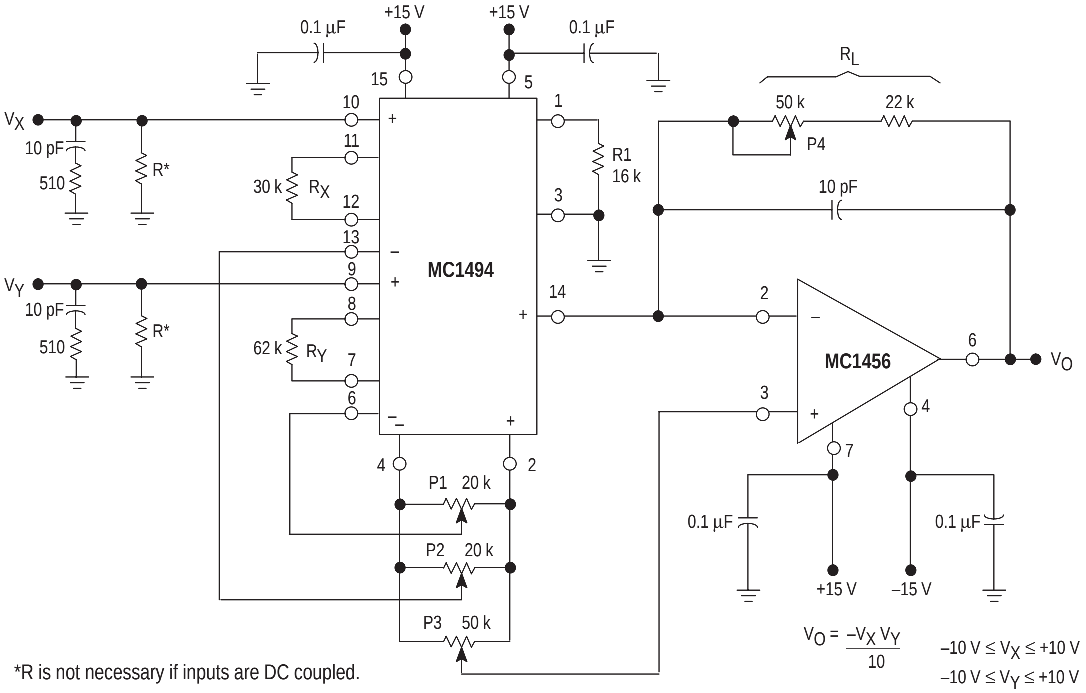
Figure 17. Internal Schematic

(Recommended External Circuitry is Depicted within Dotted Lines)



This device contains 44 active transistors.

Figure 18. Typical Multiplier Connection



*R is not necessary if inputs are DC coupled.

It should be pointed out that there is nothing magic about setting the scale factor to 1/10. This is merely a convenient factor to use if the V_X and V_Y input voltages are expected to be large, say ±10 V. Obviously with $V_X = V_Y = 10$ V and a scale factor of unity, the device could not hope to provide a 100 V output, so the scale factor is set to 1/10 and provides an output scaled down by a factor of ten. For many applications it may be desirable to set K = 1/2 or K = 1 or even K = 100. This can be accomplished by adjusting R_X, R_Y and R_L appropriately.

The selection of R_L is arbitrary and can be chosen after resistors R_X and R_Y are found. Note in Figure 18 that R_Y is 62 kΩ while R_X is 30 kΩ. The reason for this is that the “Y” side of the multiplier exhibits a second order nonlinearity whereas the “X” side exhibits a simple nonlinearity. By making the R_Y resistor approximately twice the value of the R_X resistor, the linearity on both the “X” and “Y” sides are made equal. The selection of the R_X and R_Y resistor values is dependent upon the expected amplitude of V_X and V_Y inputs. To maintain a specified linearity, resistors R_X and R_Y should be selected according to the following equations:

$R_X \ge 3\ V_X$ (max) in kΩ when V_X is in Volts,
$R_Y \ge 6\ V_Y$ (max) in kΩ when V_Y is in Volts.

For example, if the maximum input on the “X” side is ±1.0 V, resistor R_X can be selected to be 3.0 kΩ. If the maximum input on the “Y” side is also ±1.0 V, then resistor R_Y can be selected to be 6.0 kΩ (6.2 kΩ nominal value). If a scale factor of K = 10 is desired, the load resistor is found to be 47 kΩ. In this example, the multiplier provides a gain of 20 dB.

Operational Amplifier Selection

The operational amplifier connection in Figure 18 is a simple but extremely accurate current–to–voltage converter. The output current of the multiplier flows through the feedback resistor R_L to provide a low impedance output voltage from the op amp. Since the offset current and bias currents of the op amp will cause errors in the output voltage, particularly with temperature, one with very low bias and offset currents is recommended. The MC1456 or MC1741 are excellent choices for this application.

Since the MC1494 is capable of operation at much higher frequencies than the op amp, the frequency characteristics of the circuit in Figure 18 will be primarily dependent upon the operational amplifier.

Stability

The current–to–voltage converter mode is a most demanding application for an operational amplifier. Loop gain is at its maximum and the feedback resistor in conjunction with stray or input capacitance at the multiplier output adds additional phase shift. It may therefore be necessary to add (particularly in the case of internally compensated op amps) a small feedback capacitor to reduce loop gain at the higher frequencies. A value of 10 pF in parallel with R_L should be adequate to insure stability over production and temperature variations, etc.

An externally compensated op amp might be employed using slightly heavier compensation than that recommended for unity–gain operation.

Offset Adjustment

The noninverting input of the op amp provides a convenient point to adjust the output offset voltage. By connecting this point to the wiper arm of a potentiometer (P3), the output offset voltage can be adjusted to zero (see Offset and Scale Factor Adjustment Procedure).

The input offset adjustment potentiometers, P1 and P2 will be necessary for most applications where it is desirable to take advantage of the multiplier’s excellent linearity characteristics. Depending upon the particular application, some of the potentiometers can be omitted (see Figures 19, 21, 24, 26 and 27).

Offset and Scale Factor Adjustment Procedure

The adjustment procedure for the circuit of Figure 18 is:

A. X Input Offset
   1. Connect oscillator (1.0 kHz, 5.0 Vpp sinewave) to the ‘‘Y’’ input (Pin 9).
   2. Connect ‘‘X’’ input (Pin 10) to ground.
   3. Adjust X–offset potentiometer, P2 for an AC null at the output.

B. Y Input Offset
   1. Connect oscillator (1.0 kHz, 5.0 Vpp sinewave) to the ‘‘X’’ input (Pin 10).
   2. Connect ‘‘Y’’ input (Pin 9) to ground.
   3. Adjust Y–offset potentiometer, P1 for an AC null at the output.

C. Output Offset
   1. Connect both ‘‘X’’ and ‘‘Y’’ inputs to ground.
   2. Adjust output offset potentiometer, P3 until the output voltage V_O is 0 Vdc.

D. Scale Factor
   1. Apply +10 Vdc to both the ‘‘X’’ and ‘‘Y’’ inputs.
   2. Adjust P4 to achieve –10 V at the output.
   3. Apply –10 Vdc to both ‘‘X’’ and ‘‘Y’’ inputs and check for V_O = –10 V.

E. Repeat steps A through D as necessary.

The ability to accurately adjust the MC1494 is dependent on the offset adjust potentiometers. Potentiometers should be of the “infinite” resolution type rather than wirewound. Fine adjustments in balanced–modulator applications may require two potentiometers to provide “coarse” and “fine” adjustment. Potentiometers should have low temperature coefficients and be free from backlash.

Temperature Stability

While the MC1494 provides excellent performance in itself, overall performance depends to a large degree on the quality of the external components. Previous discussion shows the direct dependence on R_X, R_Y and R_L and indirect dependence on R1 (through I_1). *Any circuit subjected to temperature variations should be evaluated with these effects in mind.*

Bias Currents

The MC1494 multiplier, like most linear ICs, requires a DC bias current into its input terminals. The device cannot be capacitively coupled at the input without regard for this bias current. If inputs V_X and V_Y are able to supply the small bias current (≈ 0.5 µA) resistors R can be omitted (see Figure 18). If the MC1494 is used in an AC mode of operation and capacitive coupling is used the value of resistor R can be any reasonable value up to 100 kΩ. For minimum noise and optimum temperature performance, the value of resistor R should be as low as practical.

Parasitic Oscillation

When long leads are used on the inputs, oscillation may occur. In this event, an RC parasitic suppression network similar to the ones shown in Figure 18 should be connected directly to each input using short leads. The purpose of the network is to reduce the “Q” of the source–tuned circuits which cause the oscillation.

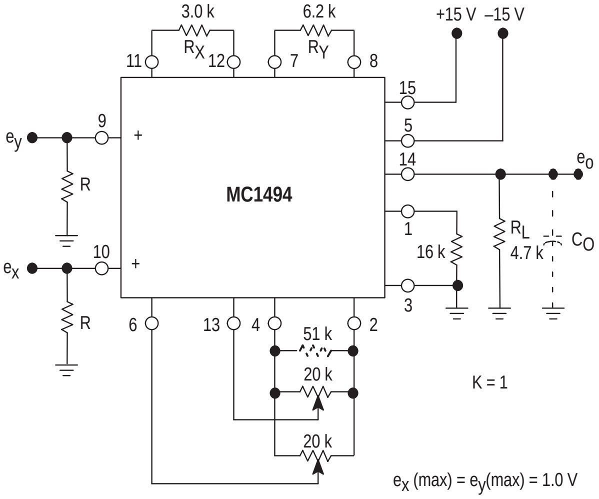
Inability to adjust the circuit to within the specified accuracy may be an indication of oscillation.

AC OPERATION

General

For AC operation, such as balanced modulation, frequency doubler, AGC, etc., the op amp will usually be omitted as well as the output offset adjust potentiometer. The output offset adjust potentiometer is omitted since the output will normally be AC coupled and the DC voltage at the output is of no concern providing it is close enough to zero volts that it will not cause clipping in the output waveform. Figure 19 shows a typical AC multiplier circuit with a scale factor K ≈ 1. Again, resistor R_X and R_Y are chosen as outlined in the previous section, with R_L chosen to provide the required scale factor.

Figure 19. Wideband Multiplier



The offset voltage then existing at the output will be equal to the offset current times the load resistance. The output offset current of the MC1494 is typically 17 µA and 35 µA maximum. Thus, the maximum output offset would be about 160 mV.

Bandwidth

The bandwidth of the MC1494 is primarily determined by two factors. First, the dominant pole will be determined by the load resistor and the stray capacitance at the output terminal. For the circuit shown in Figure 19, assuming a total output capacitance (C_O) of 10 pF, the 3.0 dB bandwidth would be approximately 3.4 MHz. If the load resistor were 47 kΩ, the bandwidth would be approximately 340 kHz.

Secondly, a “zero” is present in the frequency response characteristic for both the “X” and “Y” inputs which causes the output signal to rise in amplitude at a 6.0 dB/octave slope at frequencies beyond the breakpoint of the “zero”. The “zero” is caused by the parasitic and substrate capacitance which is related to resistors R_X and R_Y and the transistors associated with them. The effect of these transmission “zeros” is seen in Figures 11 and 12. The reason for this increase in gain is due to the bypassing of R_X and R_Y at high frequencies. Since the R_Y resistor is approximately twice the value of the R_X resistor, the zero associated with the “Y” input will occur at approximately one octave below the zero associated with “X” input. For R_X = 30 kΩ and R_Y = 62 kΩ, the zeros occur at 1.5 MHz for the “X” input and 700 kHz for the “Y” input. These two measured breakpoints correspond to a shunt capacitance of about 3.5 pF. Thus, for the circuit of

Figure 19, the “X” input zero and “Y” input zero will be at approximately 15 MHz and 7.0 MHz respectively.

It should be noted that the MC1494 multiplies in the time domain, hence, its frequency response is found by means of complex convolution in the frequency (Laplace) domain. This means that if the “X” input does not involve a frequency, it is not necessary to consider the “X” side frequency response in the output product. Likewise, for the “Y” side. Thus, for applications such as a wideband linear AGC amplifier which has a DC voltage as one input, the multiplier frequency response has one zero and one pole. For applications which involve an AC voltage on both the “X” and “Y” side such as a balanced modulator, the product voltage response will have two zeros and one pole, hence, peaking may be present in the output.

From this brief discussion, it is evident that for AC applications; (1) the value of resistors R_X, R_Y and R_L should be kept as small as possible to achieve maximum frequency response, and (2) it is possible to select a load resistor R_L such that the dominant pole (R_L, C_O) cancels the input zero (R_X, 3.5 pF or R_Y, 3.5 pF) to give a flat amplitude characteristic with frequency. This is shown in Figures 11 and 12. Examination of the frequency characteristics of the “X” and “Y” inputs will demonstrate that for wideband amplifier applications, the best tradeoff with frequency response and gain is achieved by using the “Y” input for the AC signal.

For AC applications requiring bandwidths greater than those specified for the MC1494, two other devices are recommended. For modulator–demodulator applications, the MC1496 may be used up to 100 MHz. For wideband multiplier applications, the MC1495 (using small collector loads and AC coupling) can be used.

Slew–Rate

The MC1494 multiplier is not slew–rate limited in the ordinary sense that an op amp is. Since all the signals in the multiplier are currents and not voltages, there is no charging and discharging of stray capacitors and thus no limitations beyond the normal device limitataions. However, it should be noted that the quiescent current in the output transistors is 0.5 mA and thus the maximum rate of change of the output voltage is limited by the output load capacitance by the simple equation:

$$\text{Slew Rate } \frac{\Delta V_O}{\Delta T} = \frac{I_O}{C}$$

Thus, if C_O is 10 pF, the maximum slew rate would be:

$$\frac{\Delta V_O}{\Delta T} = \frac{0.5 \times 10^{-3}}{10 \times 10^{-12}} = 50\ \text{V}/\mu\text{s}$$

This can be improved, if necessary, by the addition of an emitter–follower or other type of buffer.

Phase Vector Error

All multipliers are subject to an error which is known as the phase vector error. This error is a phase error only and does not contribute an amplitude error per se. The phase vector error is best explained by an example. If the “X” input is described in vector notation as;

$$X = A \measuredangle 0^\circ$$

and the “Y” input is described as;

$$Y = B \measuredangle 0^\circ$$

then the output product would be expected to be;

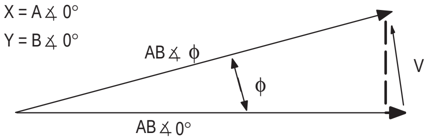
$$V_O = AB \measuredangle 0^\circ \text{ (see Figure 20)}$$

However, due to a relative phase shift between the ‘‘X’’ and ‘‘Y’’ channels, the output product will be given by:

$$V_O = AB \measuredangle \phi$$

Notice that the magnitude is correct but the phase angle of the product is in error. The vector (V) associated with this error is the ‘‘phase vector error’’. The startling fact about the phase vector error is that it occurs and accumulates much more rapidly than the amplitude error associated with frequency response. In fact, a relative phase shift of only 0.57° will result in a 1% phase vector error. For most applications, this error is meaningless. If phase of the output product is not important, then neither is the phase vector error. If phase is important, such as in the case of double sideband modulation or demodulation, then a 1% phase vector error will represent a 1% amplitude error a the phase angle of interest.

Figure 20. Phase Vector Error



Circuit Layout

If wideband operation is desired, careful circuit layout must be observed. Stray capacitance across R_X and R_Y should be avoided to minimize peaking (caused by a zero created by the parallel RC circuit).

DC APPLICATIONS

Squaring Circuit

If the two inputs are connected together, the resultant function is squaring:

$$V_O = KV^2$$

where K is the scale factor (see Figure 21).

However, a more careful look at the multiplier’s defining equation will provide some useful information. The output voltage, without initial offset adjustments is given by:

$$V_O = K(V_X + V_{iox} - V_{X\ off})\ (V_Y + V_{ioy} - V_{Y\ off}) + V_{OO}$$

(Refer to “Definitions” section for an explanation of terms.)

With $V_X = V_Y = V$ (squaring) and defining;

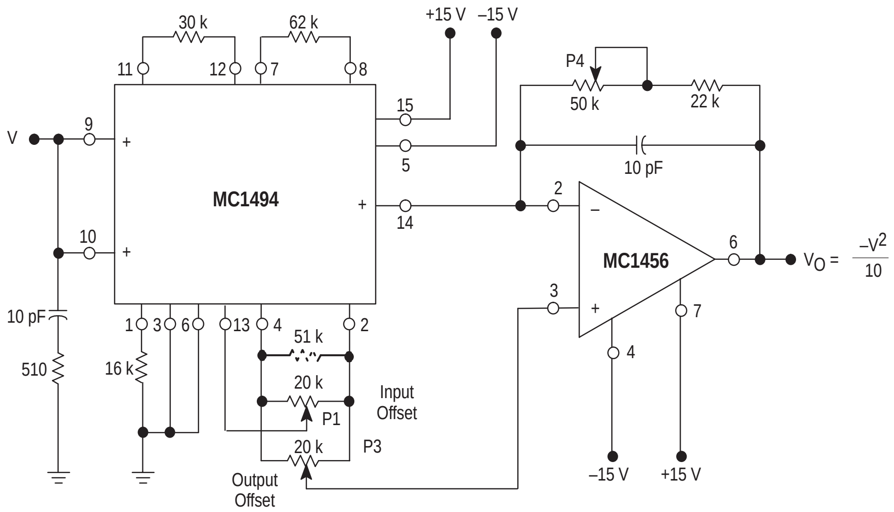
$$\in_x = V_{iox} - V_x \text{ (off)}$$

$$\in_y = V_{ioy} - V_y \text{ (off)}$$

The output voltage equation becomes:

$$V_O = KV_x^2 + KV_x\ (\in_x + \in_y) + K\in_x \in_y + V_{OO}$$

Figure 21. MC1494 Squaring Circuit



This shows that all error terms can be eliminated with only three adjustment potentiometers, eliminating one of the input offset adjustments. For instance, if the "X" input offset adjustment is eliminated, $\in_X$ is determined by the internal offset (V_{ioX}) but $\in_Y$ is adjustable to the extent that the ($\in_X + \in_Y$) term can be zeroed. Then the output offset adjustment is used to adjust the V_{OO} term and thus zero the remaining error terms. An AC procedure for nulling with three adjustments is:

A. AC Procedure:
   1. Connect oscillator (1.0 kHz, 15 Vpp) to input.
   2. Monitor output at 2.0 kHz with tuned voltmeter and adjust P4 for desired gain (Be sure to peak response of voltmeter).
   3. Tune voltmeter to 1.0 kHz and adjust P1 for a minimum output voltage.
   4. Ground input and adjust P3 (output offset) for 0 Vdc out.
   5. Repeat steps 1 through 4 as necessary.

B. DC Procedure:
   1. Set $V_X = V_Y = 0$ V and adjust P3 (output offset potentiometer) such that $V_O = 0$ Vdc.
   2. Set $V_X = V_Y = 1.0$ V and adjust P1 (Y input offset potentiometer) such that the output voltage is – 0.100 V.
   3. Set $V_X = V_Y = 10$ Vdc and adjust P4 (load resistor) such that the output voltage is –10 V.
   4. Set $V_X = V_Y = -10$ Vdc and check that $V_O = -10$ V.
   5. Repeat steps 1 through 4 as necessary.

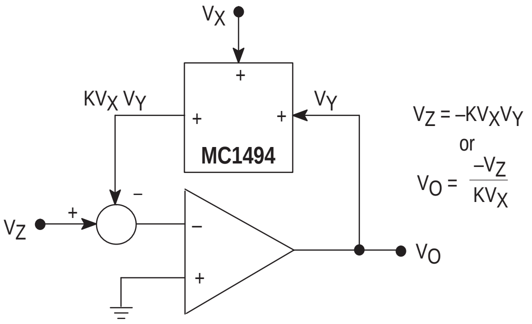
Divide

Divide circuits warrant a special discussion as a result of their special problems. Classic feedback theory teaches that if a multiplier is used as a feedback element in an operational amplifier circuit, the divide function results. Figure 22 illustrates the theoretical simplicity of such an approach and a practical realization is shown in Figure 23.

The characteristic "failure" mode of the divide circuit is latch–up. One way it can occur is if V_X is allowed to go negative, or in some cases, if V_X approaches zero.

Figure 22 illustrates why this is so. For $V_X > 0$ the transfer function through the multiplier is noninverting. Its output is fed to the inverting input of the op amp Thus, operation is in the negative feedback mode and the circuit is DC stable.

Figure 22. Basic Divide Circuit Using Multiplier

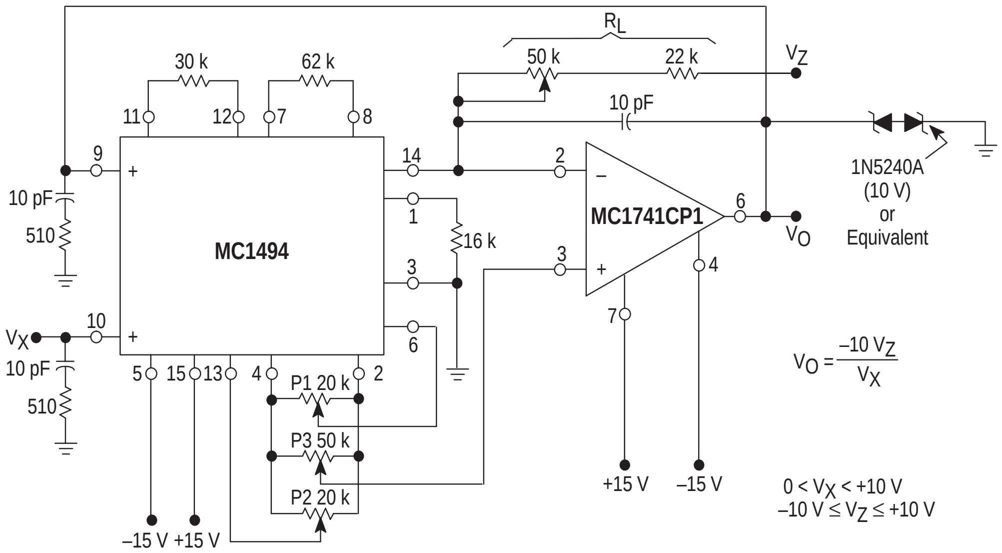


Should V_X change polarity, the transfer function through the multiplier becomes inverting, the amplifier has positive feedback and latch–up results. The problem resulting from V_X being near zero is a result of the transfer through the multiplier being near zero. The op amp is then operating with a very high closed–loop gain and error voltages can thus become effective in causing latch–up.

The other mode of latch–up results from the output voltage of the op amp exceeding the rated common mode input voltage of the multiplier. The input stage of the multiplier becomes saturated, phase reversal results, and the circuit is latched up. The circuit of Figure 23 protects against this happening by clamping the output swing of the op amp to approximately ± 10.7 V. Five percent tolerance, 10 V zeners are used to assure adequate output swing but still limit the output voltage of the op amp from exceeding the common mode input range of the MC1494.

Setting up the divide circuit for reasonably accurate operation is somewhat different from the procedure for the multiplier itself. One approach, however, is to break the feedback loop, null out the multiplier circuit, and then close the loop.

Figure 23. Practical Divide Circuit



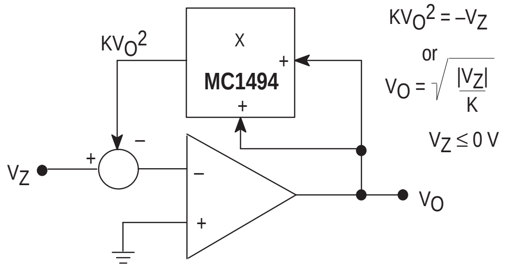
A simpler approach, since it does not involve breaking the loop (thus making it more practical on a production basis), is:

1. Set V_Z = 0 V and adjust the output offset potentiometer (P3) until the output voltage (V_O) remains at some (not necessarily zero) constant value as V_X is varied between +1.0 V and +10 V.
2. Maintain V_Z at 0 V, set V_X at +10 V and adjust the Y input offset potentiometer (P1) until V_O = 0 V.
3. With $V_X = V_Z$, adjust the X input offset potentiometer (P2) until the output voltage remains at some (not necessarily –10 V) constant value as $V_Z = V_X$ is varied between +1.0 V and +10 V.
4. Maintain $V_X = V_Z$ and adjust the scale factor potentiometer (R_L) until the average value of V_O is –10 V as $V_Z = V_X$ is varied between +1.0 V and +10 V.
5. Repeat steps 1 through 4 as necessary to achieve optimum performance.

Users of the divide circuit should be aware that the accuracy to be expected decreases in direct proportion to the denominator voltage. As a result, if V_X is set to 10 V and 0.5% accuracy is available, then 5% accuracy can be expected when V_X is only 1.0 V.

In accordance with an earlier statement, V_X may have only one polarity (positive) while V_Z may be either polarity.

Figure 24. Basic Square Root Circuit



Square Root

A special case of the divide circuit in which the two inputs to the multiplier are connected together results in the square root function as indicated in Figure 24. This circuit too may suffer from latch–up problems similar to those of the divide circuit. Note that only one polarity of input is allowed and diode clamping (see Figure 25) protects against accidental latch–up.

This circuit too, may be adjusted in the closed–loop mode:

1. Set V_Z = –0.01 Vdc and adjust P3 (output offset) for V_O = 0.316 Vdc.
2. Set V_Z to –0.9 Vdc and adjust P2 (“X” adjust) for V_O = +3.0 Vdc.
3. Set V_Z to –10 Vdc and adjust P4 (gain adjust) for V_O = +10 Vdc.
4. Steps 1 through 3 may be repeated as necessary to achieve desired accuracy.

NOTE: Operation near 0 V input may prove very inaccurate, hence, it may not be possible to adjust V_O to zero but rather only to within 100 mV to 400 mV of zero.

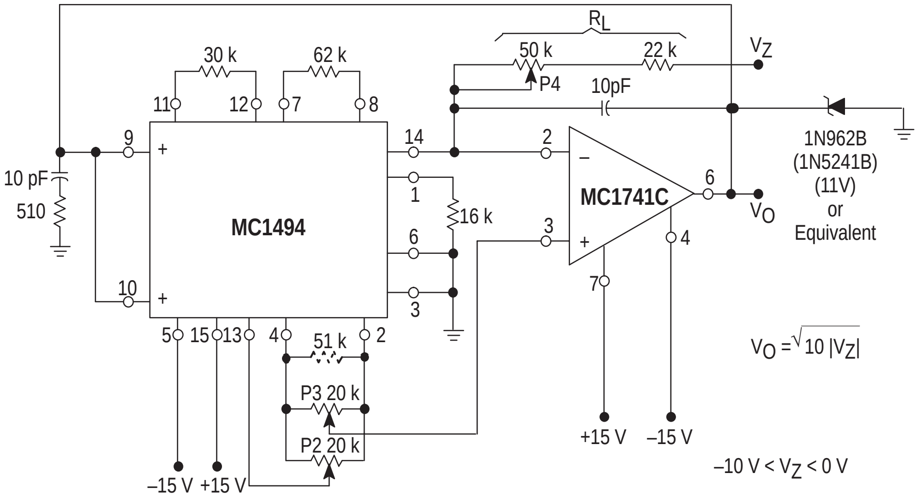
AC APPLICATIONS

Wideband Amplifier with Linear AGC

If one input to the MC1494 is a DC voltage and a signal voltage is applied to the other input, the amplitude of the output signal can be controlled in a linear fashion by varying the DC voltage. Hence, the multiplier can function as a DC coupled, wideband amplifier with linear AGC control.

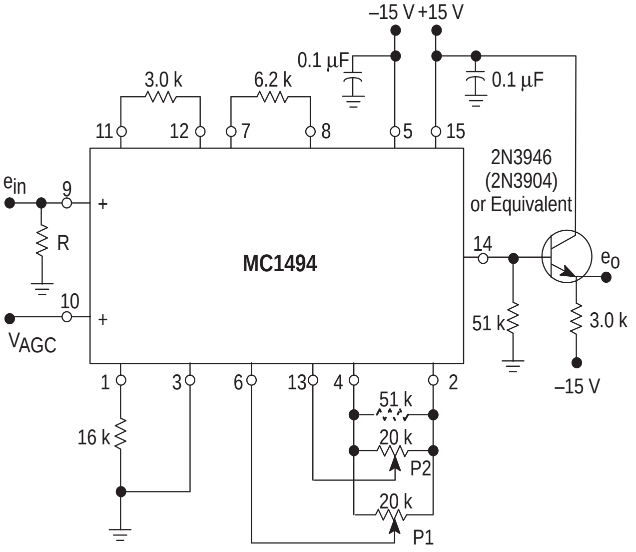
In addition to the advantage of linear AGC control, the multiplier has three other distinct advantages over most other types of AGC systems. First, the AGC dynamic range is theoretically infinite. This stems from the basic fact that with 0 Vdc applied to the AGC, the output will be zero regardless of the input. In practice, the dynamic range is limited by the ability to adjust the input offset adjust potentiometers. By using cermet multi–turn potentiometers, a dynamic range of 80 dB can be obtained. The second advantage of the multiplier is that variation of the AGC voltage has no effect on the signal handling capability of the signal port, nor does it alter the input impedance of the signal port. This feature is particularly important in AGC systems which are phase sensitive. A third advantage of the multiplier is that the output voltage swing capability and output impedance are unchanged with variations in AGC voltage.

Figure 25. Square Root Circuit



The circuit of Figure 26 demonstrates the linear AGC amplifier. The amplifier can handle 1.0 Vrms and exhibits a gain of approximately 20 dB. It is AGC'd through a 60 dB dynamic range with the application of an AGC voltage from 0 Vdc to 1.0 Vdc. The bandwidth of the amplifier is determined by the load resistor and output stray capacitance. For this reason, an emitter–follower buffer has been added to extend the bandwidth in excess of 1.0 MHz.

Figure 26. Wideband Amplifier with Linear AGC



Balanced Modulator

When two–time variant signals are used as inputs, the resulting output is suppressed–carrier double–sideband modulation. In terms of sinusoidal inputs, this can be seen in the following equation:

$$V_O = K(e_1 \cos\omega_m t)\,(e_2 \cos\omega_c t)$$

where ω_m is the modulation frequency and ω_c is the carrier frequency. This equation can be expanded to show the suppressed carrier or balanced modulation:

$$V_O = \frac{Ke_1e_2}{2}\,[\cos(\omega_c+\omega_m)\,t + \cos(\omega_c \pm \omega_m)t]$$

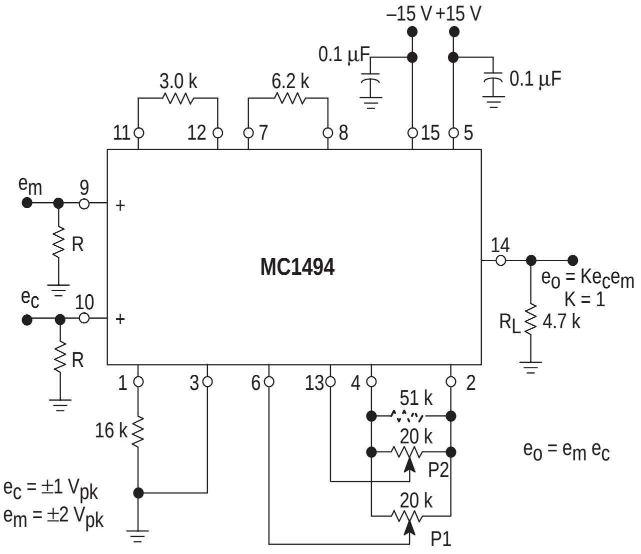
Unlike many modulation schemes, which are nonlinear in nature, the modulation which takes place when using the MC1494 is linear. This means that for two sinusoidal inputs, the output will contain only two frequencies, the sum and difference, as seen in the above equation. There will be no spectrum centered about the second harmonic of the carrier, or any multiple of the carrier. For this reason, the filter requirements of a modulation system are reduced to the minimum. Figure 27 shows the MC1494 configuration to perform this function.

Notice that the resistor values for R_X, R_Y and R_L have been modified. This has been done primarily to increase the bandwidth by lowering the output impedance of the MC1494 and then lowering R_X and R_Y to achieve a gain of 1. The e_c can be as large as 1.0 V peak and e_m as high as 2.0 V peak. No output offset adjust is employed since we are interested only in the AC output components.

The input reisstors (R) are used to supply bias current to the multiplier inputs as well as provide matching input impedance. The output frequency range of this configuration is determined by the 4.7 kΩ output impedance and capacitive loading. Assuming a 6.0 pF load, the small–signal bandwidth is 5.5 MHz.

The circuit of Figure 27 will provide at typical carrier rejection of ≥ 70 dB from 10 kHz to 1.5 MHz.

Figure 27. Balanced Modulator



The adjustment procedure for this circuit is quite simple.

1. Place the carrier signal at Pin 10. With no signal applied to Pin 9, adjust potentiometer P1 such that an AC null is obtained at the output.
2. Place a modulation signal at Pin 9. With no signal applied to Pin 10, adjust potentiometer P2 such that an AC null is obtained at the output.

Again, the ability to make careful adjustment of these offsets will be a function of the type of potentiometers used for P1 and P2. Multiple turn cermet type potentiometers are recommended.

Frequency Doubler

If for Figure 27 both inputs are identical:

$$e_m = e_c = E \cos\omega t$$

then the output is given by,

$$e_o = e_m e_c = E^2 \cos^2 \omega t$$

which reduces to,

$$e_o = \frac{E^2}{2}\,(1 + \cos 2\omega t)$$

This equation states that the output will consist of a DC term equal to one half the peak voltage squared and the second harmonic of the input frequency. Thus, the circuit acts as a frequency doubler. Two facts about this circuit are worthy of note. First, the second harmonic of the input frequency is the only frequency appearing at the output. The fundamental does not appear. Second, if the input is sinusoidal, the output will be sinusoidal and requires *no* filtering.

The circuit of Figure 27 can be used as a frequency doubler with input frequencies in excess of 2.0 MHz.

Amplitude Modulator

The circuit of Figure 27 is also easily used as an amplitude modulator. This is accomplished by simply varying the input offset adjust potentiometer (P1) associated with the mudulation input. This procedure places a DC offset on the modulation input of the multiplier such that the carrier still passes through the multiplier when the modulating signal is zero. The result is amplitude modulation. This is easily seen by examining the basic mathematical expression for amplitude modulation given below. For the case under discussion, with K = 1,

$$e_o = (E + E_m \cos\omega_m t)\,(E_c \cos\omega_c t)$$

where E is the DC input offset adjust voltage. This expression can be written as:

$$e_o = E_o\,[1 + M \cos\omega_c t] \cos\omega_c t$$

where, $E_o = EE_c$

$$\text{and,}\quad M = \frac{E_m}{E} = \text{modulation index.}$$

This is the standard equation for amplitude modulation. From this, it is easy to see that 100% modulation can be achieved by adjusting the input offset adjust voltage to be exactly equal to the peak value of the modulation (E_m). This is done by observing the output waveform and adjusting the input offset potentiometer (P1) until the output exhibits the familiar amplitude modulation waveform.

Phase Detector

If the circuit of Figure 27 has as its inputs two signals of identical frequency, but having a relative phase shift, the output will be a DC signal which is directly proportional to the cosine of phase difference as well as the double frequency term.

$$e_c = E_c \cos\omega_c t$$

$$e_m = E_m \cos(\omega_c t + \phi)$$

$$e_o = e_c e_m = E_c E_m \cos\omega_c t \cos(\omega_c t + \phi)$$

$$\text{or,}\quad e_o = \frac{E_c E_m}{2}\,[\cos\phi + \cos(2\omega_c t + \phi)]$$

The addition of a simple low pass filter to the output (which eliminates the second cosine term) and return of R_L to an offset adjustment potentiometer will result in a DC output voltage which is proportional to the cosine of the phase difference. Hence, the circuit functions as a synchronous detector.

DEFINITION OF SPECIFICATIONS

Because of the unique nature of a multiplier, i.e., two inputs and one output, operating specifications are difficult to define and interpret. Indeed the same specification may be defined in several completely different ways depending upon which manufacturer is doing the defining. In order to clear up some of the mystery, the following definitions and examples are presented.

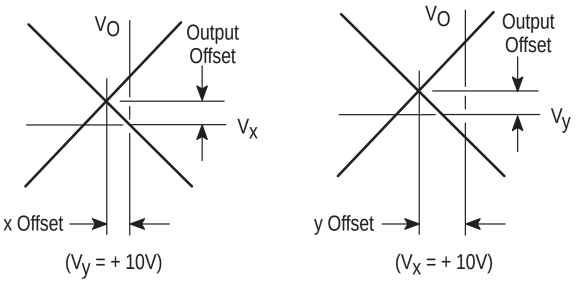
Multiplier Transfer Function – The output of the multiplier may be expressed by the following equation:

$$V_O = K[V_x \pm V_{iox} - V_{x(off)}]\ [V_y \pm V_{ioy} - V_{y(off)}] \pm V_{OO} \quad (1)$$

where, K = scale factor
V_x = “x” input voltage
V_y = “y” input voltage
V_{iox} = “x” input offset voltage
V_{ioy} = “y” input offset voltage
$V_{x(off)}$ = “x” input offset adjust voltage
$V_{y(off)}$ = “y” input offset adjust voltage
V_{OO} = output offset voltage

The voltage transfer characteristic below indicates x, y and output offset voltages.

Figure 28. Offset Voltages



Linearity – Linearity is defined to be the maximum deviation of output voltage from a straight line transfer function. It is expressed as a percentage of full–scale output and is measured for V_x and V_y separately, either using an X–Y plotter (and checking the deviation from a straight line) or by using the method shown in Figure 3. The latter method nulls the output signal with the input signal, resulting in distortion components proportional to the linearity.

Example: 0.35% linearity means

$$V_O = \frac{V_x\,V_y}{10} \pm (0.0035)(10\ V)$$

Input Offset Voltage – The input offset voltage is defined from Equation (1). It is measured for V_x and V_y separately and is defined to be that DC input offset adjust voltage (x or y) that will result in minimum AC output when AC (5.0 Vpp, 1.0 kHz) is applied to the other input (y or x, respectively). From Equation (1) we have:

$$V_O(AC) = K\,[0 \pm V_{iox} - V_{x(off)}]\ [\sin\omega t]$$

adjust $V_{x(off)}$ so that $[\pm V_{iox} - V_{x(off)}] = 0$.

Output Offset Current and Voltage – Output offset current (I_{OO}) is the DC current flowing in the output lead when $V_x = V_y = 0$ and X and Y offset voltages are adjusted to zero.

Output offset voltage (V_{OO}) is:

$$V_{OO} = I_{OO}\,R_L$$

where R_L is the load resistance.

NOTE: Output offset voltage is defined by many manufacturers with all inputs at zero but without adjusting X and Y offset voltages to zero. Thus, it includes input offset terms, an output offset term and a scale factor term.

Scale Factor – Scale factor is the K term in Equation (1). It determines the gain of the multiplier and is expressed approximately by the following equation.

$$K = \frac{2R_L}{R_x R_y I_1}\ \text{, where } R_x \text{ and } R_y >> \frac{kT}{qI_1}$$

and I_1 is the current out of Pin 1.

Total DC Accuracy – The total DC accuracy of a multiplier is defined as error in multiplier output with DC (± 10 Vdc) applied to both inputs. It is expressed as a percent of full scale. Accuracy is not specified for the MC1494 because error terms can be nulled by the user.

Temperature Stability (Drift) – Each term defined above will have a finite drift with temperature. The temperature specifications are obtained by readjusting the multiplier offsets and scale factor at each new temperature (see previous definitions and the adjustment procedure) and noting the change.

Assume inputs are grounded and initial offset voltages have been adjusted to zero. Then output voltage drift is given by:

$$\Delta V_O = \pm\ [K \pm K\,(TCK)\,(\Delta T)]\ [(TCV_{iox})\,(\Delta T)]$$
$$[(TCV_{ioy})\,(\Delta T)] \pm (TCV_{OO})\,(\Delta T)$$

Total DC Accuracy Drift – This is the temperature drift in output voltage with 10 V applied to each input. The output is adjusted to 10 V at T_A = + 25°C. Assuming initial offset voltages have been adjusted to zero at T_A = +25°C, then:

$$V_O = [\,K \pm K\,(TCK)\,(\Delta T)]\ [10 \pm (TCV_{iox})\,(\Delta T)]$$
$$[10 \pm (TCV_{ioy})\,(\Delta T)] \pm (TCV_{OO})\,(\Delta T)$$

Power Supply Rejection – Variation in power supply voltages will cause undesired variation of the output voltage. It is measured by superimposing a 1.0 V, 100 Hz signal on each supply (±15 V) with each input grounded. The resulting change in the output is expressed in mV/V.

Output Voltage Swing – Output voltage swing capability is the maximum output voltage swing (without clipping) into a resistive load. (Note, output offset is adjusted to zero).

If an op amp is used, the multiplier output becomes a virtual ground – the swing is then determined by the scale factor and the op amp selected.

MOTOROLA

MC1495

Wideband Linear Four-Quadrant Multiplier

The MC1495 is designed for use where the output is a linear product of two input voltages. Maximum versatility is assured by allowing the user to select the level shift method. Typical applications include: multiply, divide*, square root*, mean square*, phase detector, frequency doubler, balanced modulator/demodulator, and electronic gain control.

- Wide Bandwidth
- Excellent Linearity:
  2% max Error on X Input, 4% max Error on Y Input Over Temperature
  1% max Error on X Input, 2% max Error on Y Input at + 25°C
- Adjustable Scale Factor, K
- Excellent Temperature Stability
- Wide Input Voltage Range: ± 10 V
- ±15 V Operation

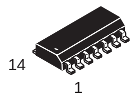
*When used with an operational amplifier.

MAXIMUM RATINGS (T_A = + 25°C, unless otherwise noted.)

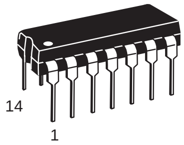
Rating	Symbol	Value	Unit
Applied Voltage (V_2–V_1, V_{14}–V_1, V_1–V_9, V_1–V_{12}, V_1–V_4, V_1–V_8, V_{12}–V_7, V_9–V_7, V_8–V_7, V_4–V_7)	∆V	30	Vdc
Differential Input Signal	V_{12}–V_9 V_4–V_8	± (6+I_{13} R_X) ± (6+I_3 R_Y)	Vdc
Maximum Bias Current	I_3 I_{13}	10 10	mA
Operating Temperature Range MC1495 MC1495B	T_A	 0 to +70 – 40 to +125	°C
Storage Temperature Range	T_{stg}	– 65 to +150	°C

LINEAR
FOUR-QUADRANT
MULTIPLIER

SEMICONDUCTOR
TECHNICAL DATA



D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO-14)



P SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

Device	Tested Operating Temperature Range	Package
MC1495D	T_A = 0° to + 70°C	SO–14
MC1495P		Plastic DIP
MC1495BP	T_A = – 40° to +125°C	Plastic DIP

ELECTRICAL CHARACTERISTICS (+V = + 32 V , –V = –15 V, T_A = + 25°C, I_3 = I_{13} = 1.0 mA, R_X = R_Y = 15 kΩ, R_L = 11 kΩ, unless otherwise noted.)

Characteristics	Figure	Symbol	Min	Typ	Max	Unit
Linearity (Output Error in percent of full scale)	5					%
T_A = + 25°C						
–10 < V_X < +10 (V_Y = ±10 V)		E_{RX}	–	±1.0	±1.0	
–10 < V_Y < +10 (V_X = ±10 V)		E_{RY}	–	± 2.0	± 2.0	
T_A = T_{Low} to T_{High}						
–10 < V_X < +10 (V_Y = ±10 V)		E_{RX}	–	±1.5	± 2.0	
–10 < V_Y < +10 (V_X = ±10 V)		E_{RY}	–	± 3.0	± 4.0	
Square Mode Error (Accuracy in percent of full scale after Offset and Scale Factor adjustment)	5	E_{SQ}				%
T_A = + 25°C			–	± 0.75	–	
T_A = T_{Low} to T_{High}			–	±1.0	–	
Scale Factor (Adjustable) $\left(K = \frac{2R_L}{I_3 R_X R_Y}\right)$	–	K	–	0.1	–	
Input Resistance (f = 20 Hz)	7	R_{inX}	–	30	–	MΩ
		R_{inY}	–	20	–	
Differential Output Resistance (f = 20 Hz)	8	R_O	–	300	–	kΩ
Input Bias Current	6					µA
$I_{bx} = \frac{(I_9 + I_{12})}{2}$, $I_{by} = \frac{(I_4 + I_8)}{2}$ T_A = + 25°C		I_{bx}, I_{by}	–	2.0	8.0	
T_A = T_{Low} to T_{High}			–	2.0	12	
Input Offset Current	6					µA
$\lvert I_9 – I_{12} \rvert$ T_A = + 25°C		$\lvert I_{iox} \rvert$, $\lvert I_{ioy} \rvert$	–	0.4	1.0	
$\lvert I_4 – I_8 \rvert$ T_A = T_{Low} to T_{High}			–	0.4	2.0	
Average Temperature Coefficient of Input Offset Current	6	$\lvert TC_{Iio} \rvert$				nA/°C
T_A = T_{Low} to T_{High}			–	2.5	–	
Output Offset Current T_A = + 25°C	6	$\lvert I_{OO} \rvert$		10	50	µA
$\lvert I_{14} – I_2 \rvert$ T_A = T_{Low} to T_{High}			–	20	100	
Average Temperature Coefficient of Output Offset Current	6	$\lvert TC_{IOO} \rvert$				nA/°C
T_A = T_{Low} to T_{High}			–	20	–	
Frequency Response	9,10					
3.0 dB Bandwidth, R_L = 11 kΩ		$BW_{(3dB)}$	–	3.0	–	MHz
3.0 dB Bandwidth, R_L = 50 Ω (Transconductance Bandwidth)		$TBW_{(3dB)}$	–	80	–	MHz
3° Relative Phase Shift Between V_X and V_Y		fφ	–	750	–	kHz
1% Absolute Error Due to Input-Output Phase Shift		fθ	–	30	–	kHz
Common Mode Input Swing (Either Input)	11	CMV	±10.5	±12	–	Vdc
Common Mode Gain T_A = + 25°C	11	A_{CM}	– 50	– 60	–	dB
(Either Input) T_A = T_{Low} to T_{High}			– 40	– 50	–	
Common Mode Quiescent Output Voltage	12	V_{O1}	–	21	–	Vdc
		V_{O2}	–	21	–	
Differential Output Voltage Swing Capability	9	V_O	–	±14	–	V_{pk}
Power Supply Sensitivity	12	S^+	–	5.0	–	mV/V
		$S^–$	–	10	–	
Power Supply Current	12	I_7	–	6.0	7.0	mA
DC Power Dissipation	12	P_D	–	135	170	mW

NOTES: 1. T_{High} = +70°C for MC1495 = +125°C for MC1495B T_{Low} = 0°C for MC1495 = – 40°C for MC1495B

Figure 1. Multiplier Transfer Characteristic

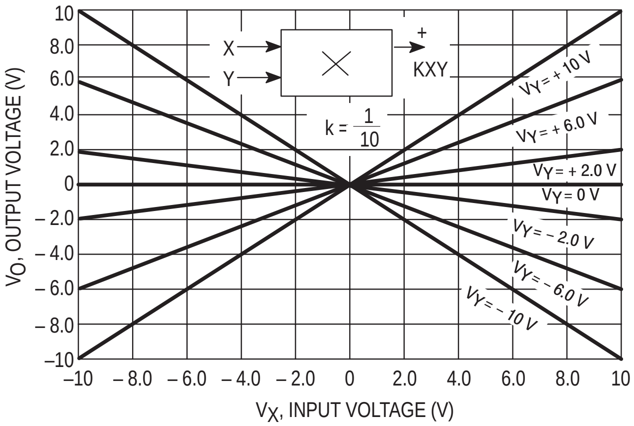


Figure 2. Transconductance Bandwidth

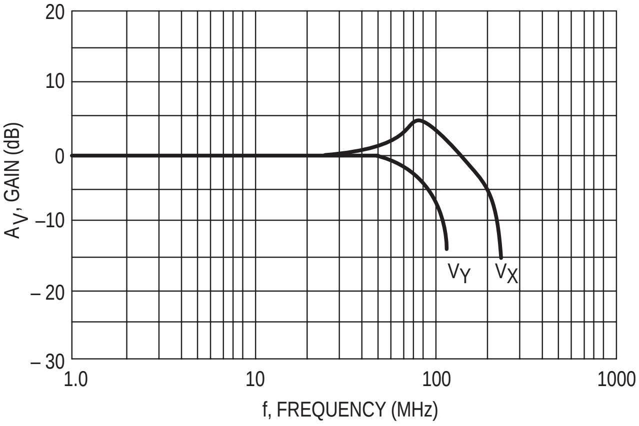
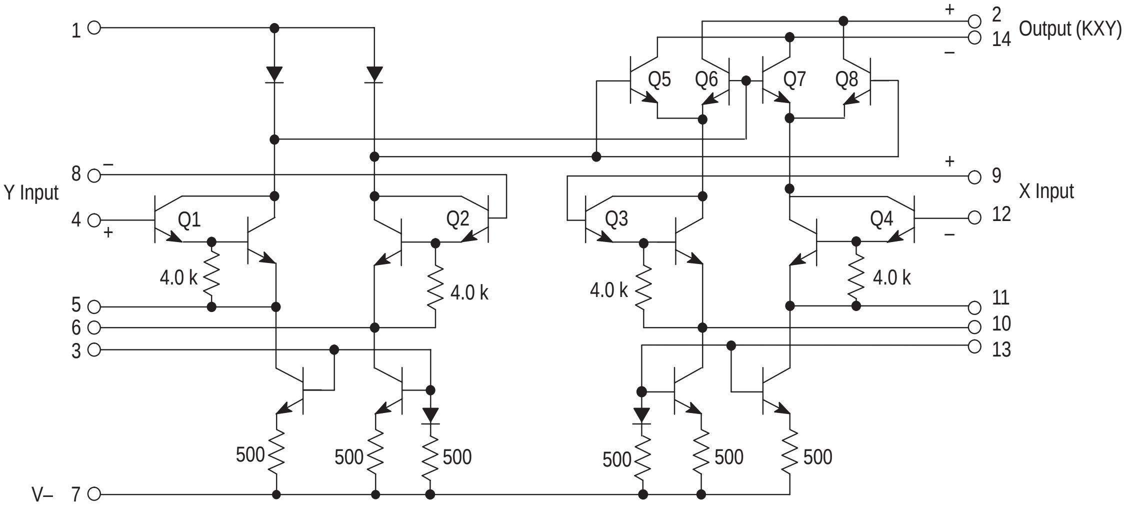
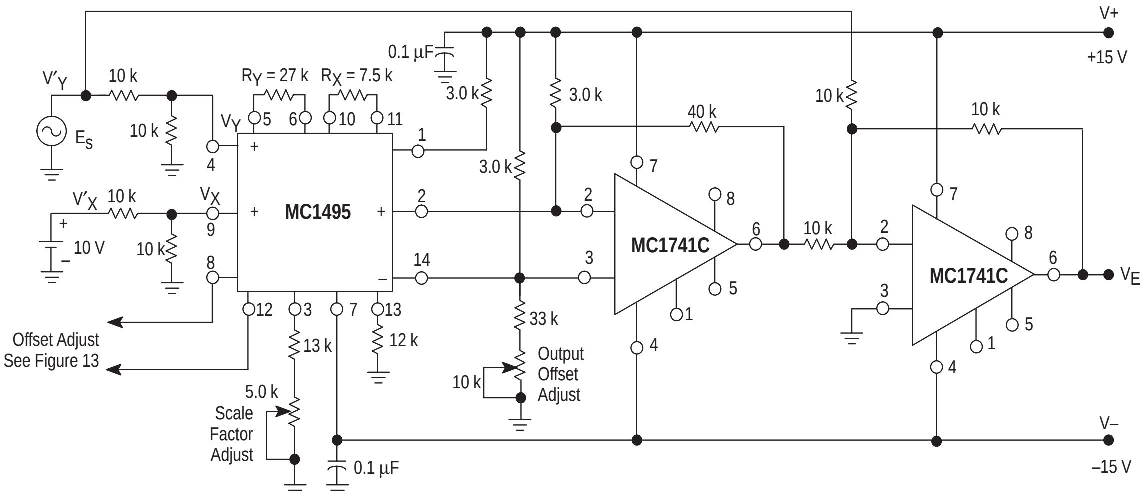


Figure 3. Circuit Schematic



This device contains 16 active transistors.

Figure 4. Linearity (Using Null Technique)



NOTE: Adjust “Scale Factor Adjust” for a null in V_E.This schematic for illustrative purposes only, not specified for test conditions.

Figure 5. Linearity (Using X-Y Plotter Technique)

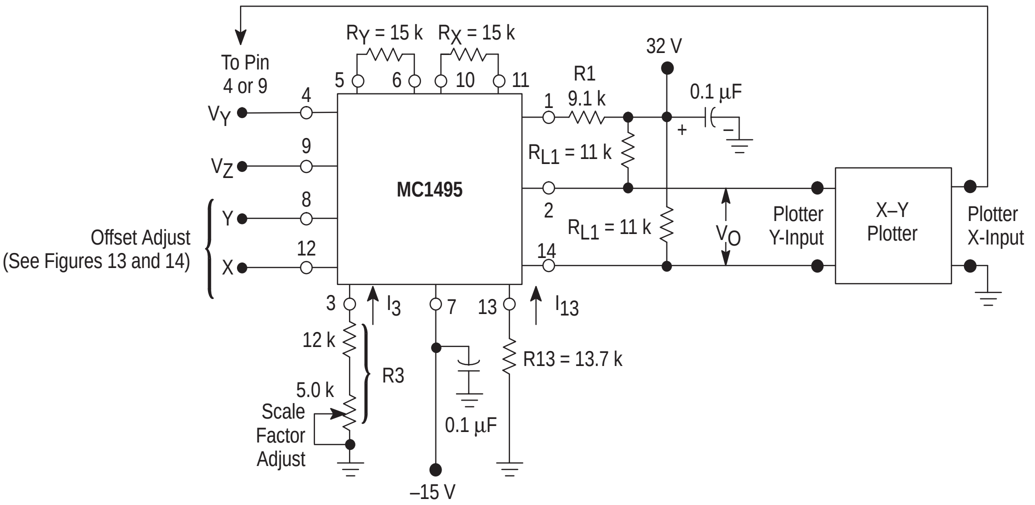


Figure 6. Input and Output Current

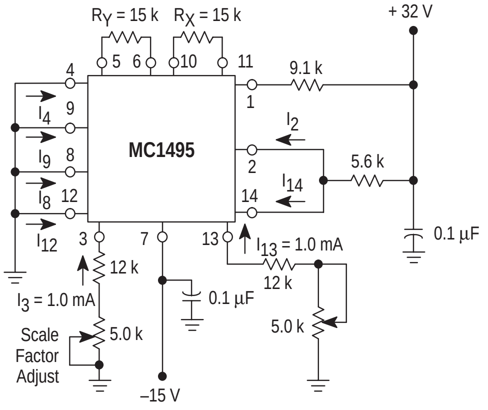
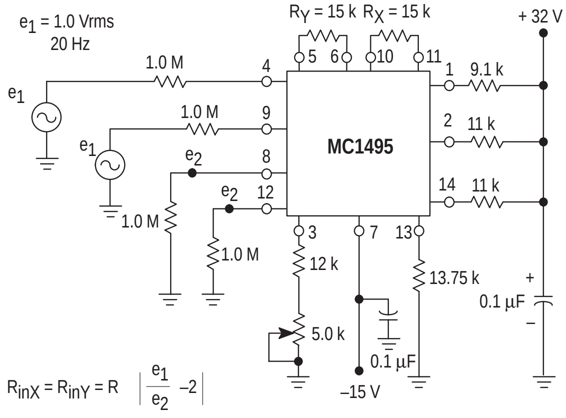
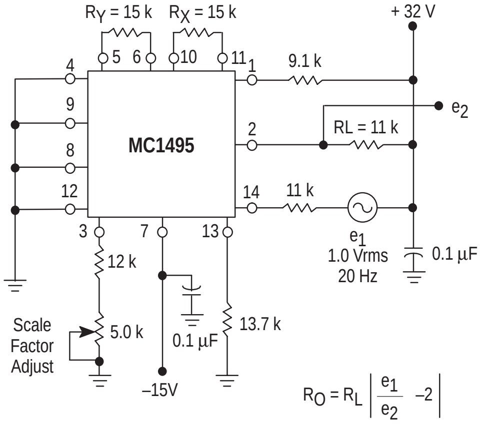


Figure 7. Input Resistance



$$R_{inX} = R_{inY} = R \left| \frac{e_1}{e_2} - 2 \right|$$

Figure 8. Output Resistance



$$R_O = R_L \left| \frac{e_1}{e_2} - 2 \right|$$

Figure 9. Bandwidth (R_L = 11 kΩ)

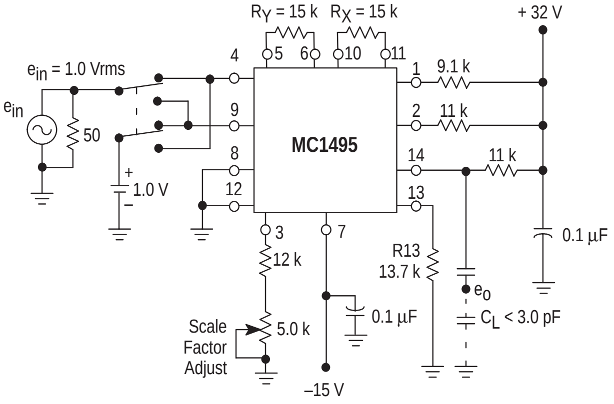


Figure 10. Bandwidth (R_L = 50 Ω)

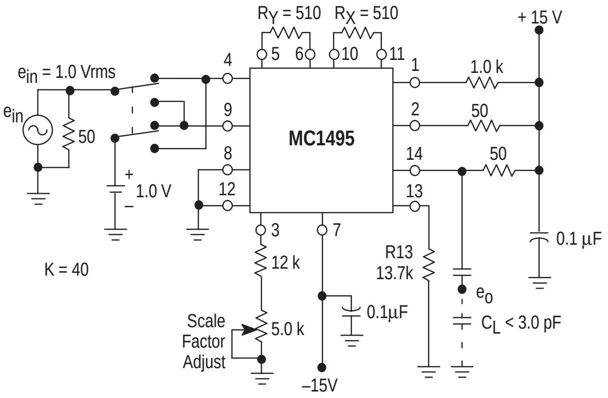


Figure 11. Common Mode Gain and Common Mode Input Swing

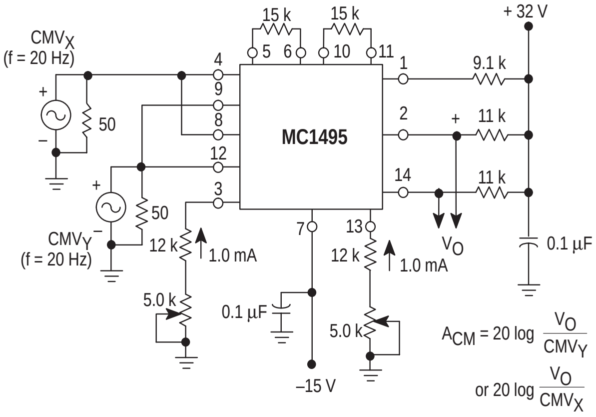


Figure 12. Power Supply Sensitivity

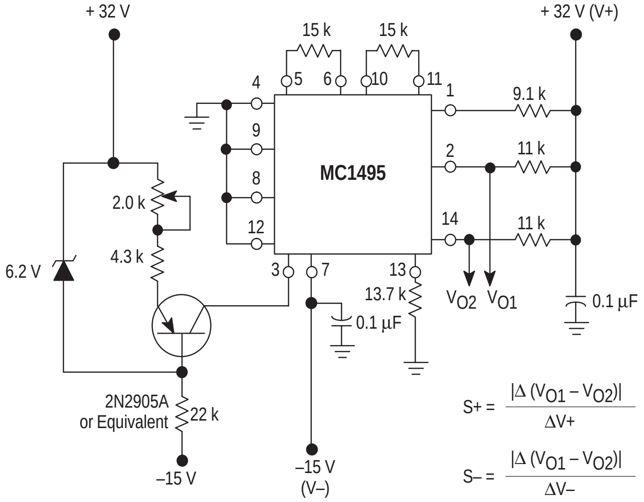
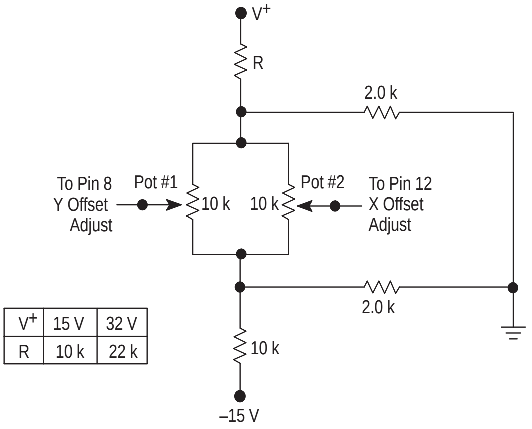
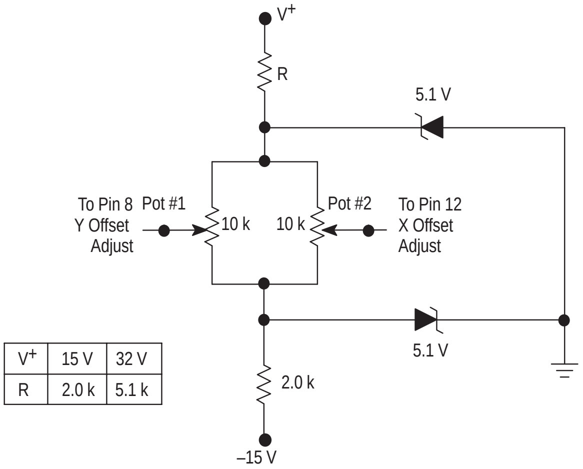


Figure 13. Offset Adjust Circuit



V+	15 V	32 V
R	10 k	22 k

Figure 14. Offset Adjust Circuit (Alternate)



V+	15 V	32 V
R	2.0 k	5.1 k

Figure 15. Linearity versus Temperature

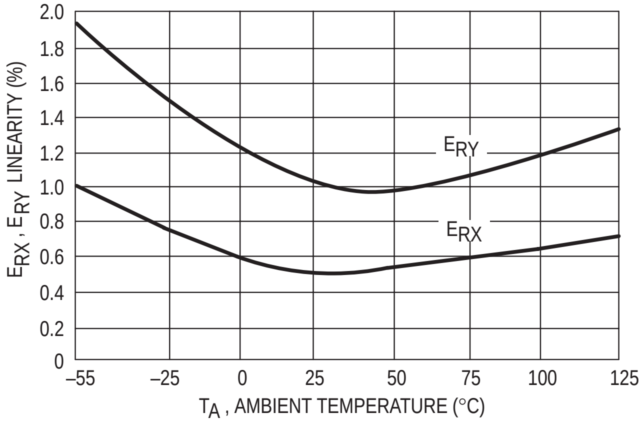


Figure 16. Scale Factor versus Temperature

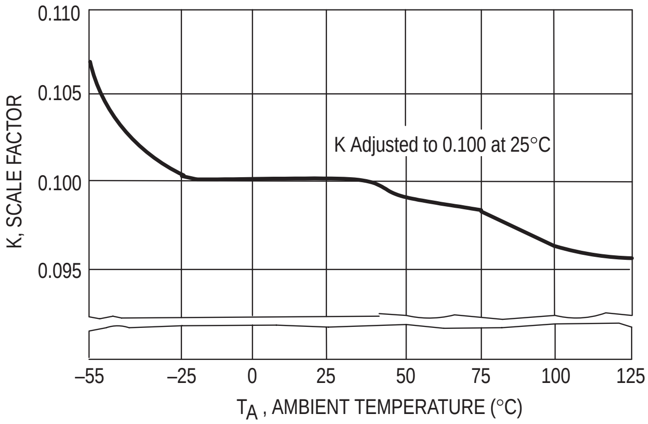


Figure 17. Error Contributed by Input Differential Amplifier

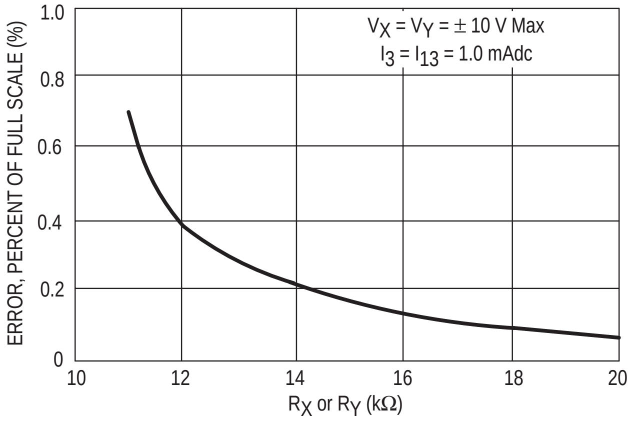


Figure 18. Error Contributed by Input Differential Amplifier

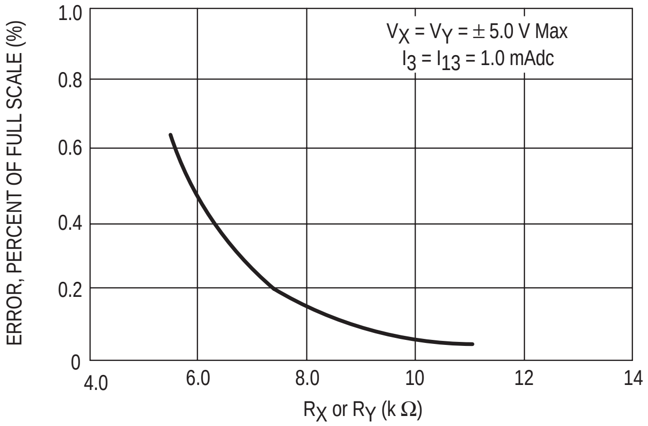
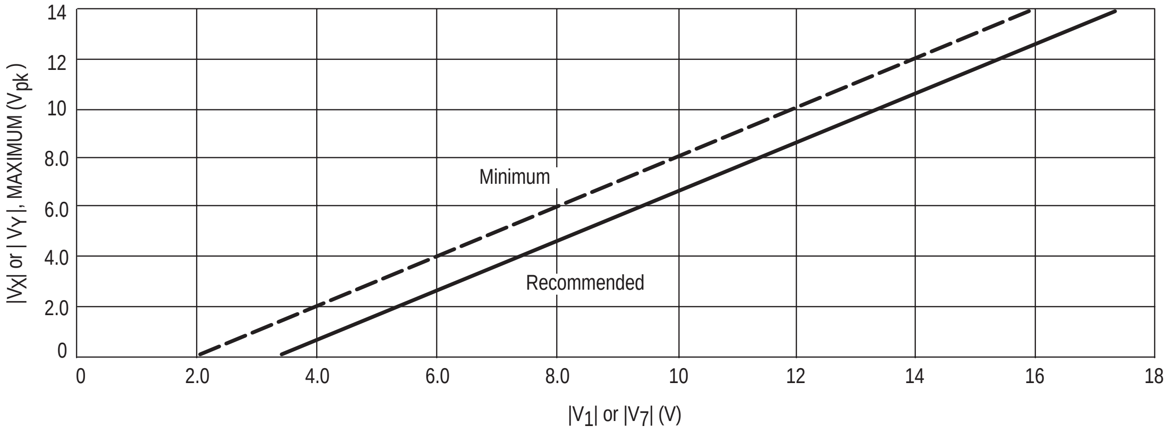


Figure 19. Maximum Allowable Input Voltage versus Voltage at Pin 1 or Pin 7



OPERATION AND APPLICATIONS INFORMATION

Theory of Operation

The MC1495 is a monolithic, four-quadrant multiplier which operates on the principle of variable transconductance. A detailed theory of operation is covered in Application Note AN489, *Analysis and Basic Operation of the MC1595*. The result of this analysis is that the differential output current of the multiplier is given by:

$$I_A - I_B = \Delta I = \frac{2V_X V_Y}{R_X R_Y I_3}$$

where, I_A and I_B are the currents into Pins 14 and 2, respectively, and V_X and V_Y are the X and Y input voltages at the multiplier input terminals.

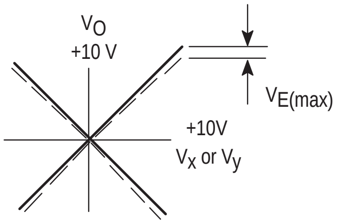
DESIGN CONSIDERATIONS

General

The MC1495 permits the designer to tailor the multiplier to a specific application by proper selection of external components. External components may be selected to optimize a given parameter (e.g. bandwidth) which may in turn restrict another parameter (e.g. maximum output voltage swing). Each important parameter is discussed in detail in the following paragraphs.

Linearity, Output Error, E_{RX} or E_{RY}

Linearity error is defined as the maximum deviation of output voltage from a straight line transfer function. It is expressed as error in percent of full scale (see figure below).



For example, if the maximum deviation, $V_{E(max)}$, is ±100 mV and the full scale output is 10 V, then the percentage error is:

$$E_R = \frac{V_E(max)}{V_O(max)} \times 100 = \frac{100 \times 10^{-3}}{10} \times 100 = \pm 1.0\%.$$

Linearity error may be measured by either of the following methods:

1. Using an X-Y plotter with the circuit shown in Figure 5, obtain plots for X and Y similar to the one shown above.
2. Use the circuit of Figure 4. This method nulls the level shifted output of the multiplier with the original input.The peak output of the null operational amplifier will be equal to the error voltage, $V_{E\ (max)}$.

One source of linearity error can arise from large signal nonlinearity in the X and Y input differential amplifiers. To avoid introducing error from this source, the emitter degeneration resistors R_X and R_Y must be chosen large enough so that nonlinear base-emitter voltage variation can be ignored. Figures 17 and 18 show the error expected from this source as a function of the values of R_X and R_Y with an operating current of 1.0 mA in each side of the differential amplifiers (i.e., $I_3 = I_{13} = 1.0$ mA).

3 dB Bandwidth and Phase Shift

Bandwidth is primarily determined by the load resistors and the stray multiplier output capacitance and/or the operational amplifier used to level shift the output. If wideband operation is desired, low value load resistors and/or a wideband operational amplifier should be used. Stray output capacitance will depend to a large extent on circuit layout.

Phase shift in the multiplier circuit results from two sources: phase shift common to both X and Y channels (due to the load resistor-output capacitance pole mentioned above) and relative phase shift between X and Y channels (due to differences in transadmittance in the X and Y channels). If the input to output phase shift is only 0.6°, the output product of two sine waves will exhibit a vector error of 1%. A 3° relative phase shift between V_X and V_Y results in a vector error of 5%.

Maximum Input Voltage

$V_{X(max)}$, $V_{Y(max)}$ input voltages must be such that:

$$V_{X(max)} < I_{13} R_Y$$

$$V_{Y(max)} < I_3 R_Y$$

Exceeding this value will drive one side of the input amplifier to “cutoff” and cause nonlinear operation.

Current I_3 and I_{13} are chosen at a convenient value (observing power dissipation limitation) between 0.5 mA and 2.0 mA, approximately 1.0 mA. Then R_X and R_Y can be determined by considering the input signal handling requirements.

For $V_{X(max)} = V_{Y(max)} = 10$ V;

$$R_X = R_Y > \frac{10\ \text{V}}{1.0\ \text{mA}} = 10\ \text{k}\Omega.$$

The equation $I_A - I_B = \dfrac{2V_X V_Y}{R_X R_Y I_3}$

is derived from $I_A - I_B = \dfrac{2V_X V_Y}{\left(R_X + \dfrac{2kT}{qI_{13}}\right)\left(R_Y + \dfrac{2kT}{qI_3}\right) I_3}$

with the assumption $R_X \gg \dfrac{2kT}{qI_{13}}$ and $R_Y \gg \dfrac{2kT}{qI_3}$.

At $T_A = +25°C$ and $I_{13} = I_3 = 1.0$ mA,

$$\frac{2kT}{qI_{13}} = \frac{2kT}{qI_3} = 52\ \Omega.$$

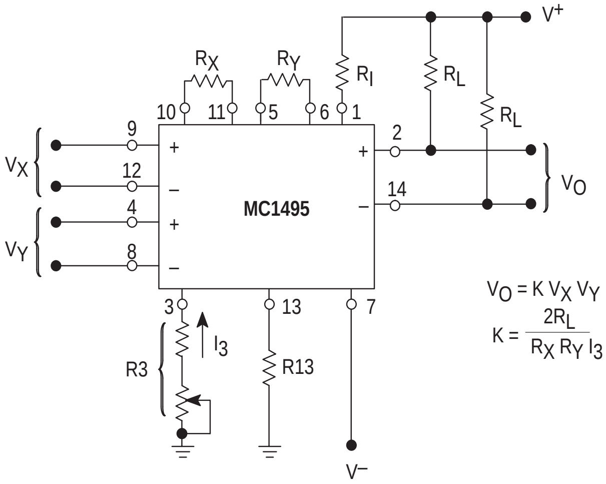
Therefore, with $R_X = R_Y = 10$ kΩ the above assumption is valid. Reference to Figure 19 will indicate limitations of $V_{X(max)}$ or $V_{Y(max)}$ due to V_1 and V_7. Exceeding these limits will cause saturation or “cutoff” of the input transistors. See Step 4 of General Design Procedure for further details.

Maximum Output Voltage Swing

The maximum output voltage swing is dependent upon the factors mentioned below and upon the particular circuit being considered.

For Figure 20 the maximum output swing is dependent upon V^+ for positive swing and upon the voltage at Pin 1 for negative swing. The potential at Pin 1 determines the quiescent level for transistors Q_5, Q_6, Q_7 and Q_8. This potential should be related so that negative swing at Pins 2 or 14 does not saturate those transistors. See General Design Procedure for further information regarding selection of these potentials.

Figure 20. Basic Multiplier



If an operational amplifier is used for level shift, as shown in Figure 21, the output swing (of the multiplier) is greatly reduced. See Section 3 for further details.

GENERAL DESIGN PROCEDURE

Selection of component values is best demonstrated by the following example. Assume resistive dividers are used at the X and Y-inputs to limit the maximum multiplier input to ± 5.0 V [$V_X = V_{Y(max)}$] for a ± 10 V input [$V_{X'} = V_{Y'(max)}$] (see Figure 21). If an overall scale factor of 1/10 is desired,

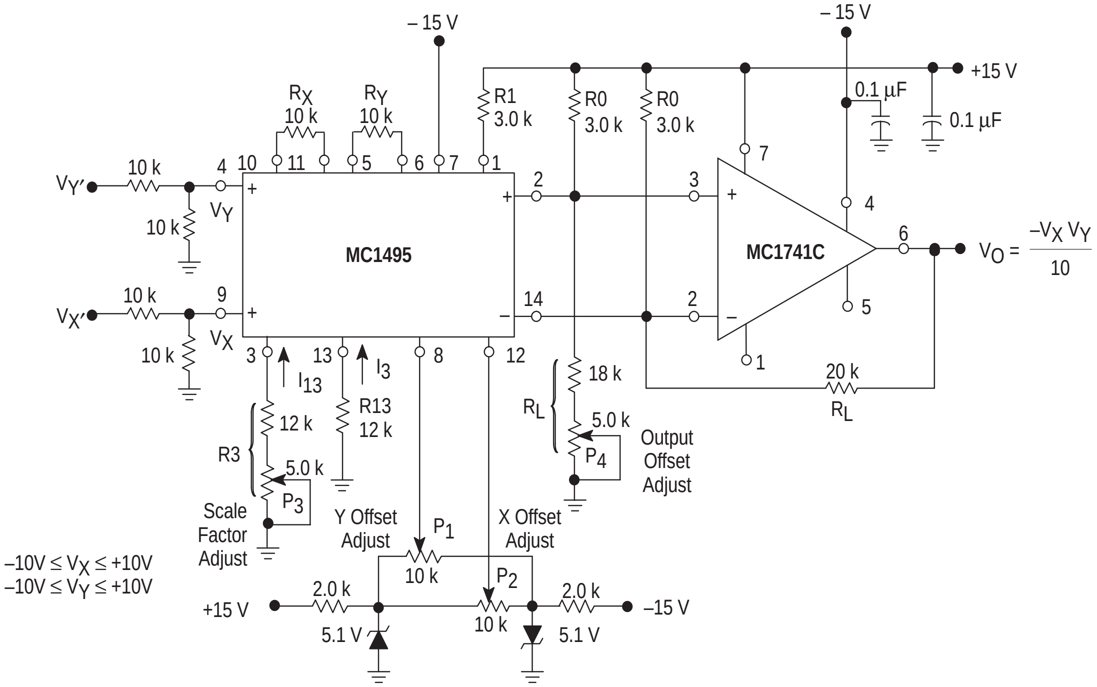
$$\text{then, } V_O = \frac{V_{X'}\,V_{Y'}}{10} = \frac{(2V_X)\,(2V_Y)}{10} = 4/10\ V_X\,V_Y$$

Therefore, K = 4/10 for the multiplier (excluding the divider network).

Step 1. The fist step is to select current I_3 and current I_{13}. There are no restrictions on the selection of either of these currents except the power dissipation of the device. I_3 and I_{13} will normally be 1.0 mA or 2.0 mA. Further, I_3 does not have to be equal to I_{13}, and there is normally no need to make them different. For this example, let

$$I_3 = I_{13} = 1.0\text{ mA.}$$

Figure 21. Multiplier with Operational Amplifier Level Shift



To set currents I_3 and I_{13} to the desired value, it is only necessary to connect a resistor between Pin 13 and ground, and between Pin 3 and ground. From the schematic shown in Figure 3, it can be seen that the resistor values necessary are given by:

$$R13 + 500\ \Omega = \frac{|V-| - 0.7\ V}{I_{13}}$$

$$R3 + 500\ \Omega = \frac{|V-| - 0.7\ V}{I_3}$$

$$\text{Let } V- = -15\ V\text{, then } R13 + 500 = \frac{14.3\ V}{1.0\ mA} \text{ or } R13 = 13.8\ k\Omega$$

Let $R_{13} = 12\ k\Omega$. Similarly, $R_3 = 13.8\ k\Omega$, let $R_3 = 15\ k\Omega$

However, for applications which require an accurate scale factor, the adjustment of R_3 and consequently, I_3, offers a convenient method of making a final trim of the scale factor. For this reason, as shown in Figure 21, resistor R_3 is shown as a fixed resistor in series with a potentiometer.

For applications not requiring an exact scale factor (balanced modulator, frequency doubler, AGC amplifier, etc.) Pins 3 and 13 can be connected together and a single resistor from Pin 3 to ground can be used. In this case, the single resistor would have a value of 1/2 the above calculated value for R_{13}.

Step 2. The next step is to select R_X and R_Y. To insure that the input transistors will always be active, the following conditions should be met:

$$\frac{V_X}{R_X} < I_{13}, \qquad \frac{V_Y}{R_Y} < I_3$$

A good rule of thumb is to make $I_3R_Y \geq 1.5\ V_{Y(max)}$ and $I_{13}R_X \geq 1.5\,V_{X(max)}$. The larger the I_3R_Y and $I_{13}R_X$ product in relation to V_Y and V_X respectively, the more accurate the multiplier will be (see Figures 17 and 18).

Let $R_X = R_Y = 10\ k\Omega$,
then $I_3R_Y = 10\ V$
$I_{13}R_X = 10\ V$

since $V_{X(max)} = V_{Y(max)} = 5.0\ V$, the value of $R_X = R_Y = 10\ k\Omega$ is sufficient.

Step 3. Now that R_X, R_Y and I_3 have been chosen, R_L can be determined:

$$K = \frac{2R_L}{R_X\ R_Y\ I_3} = \frac{4}{10}\ \text{, or } \frac{(2)\ (R_L)}{(10\ k)\ (10\ k)\ (1.0\ mA)} = \frac{4}{10}$$

Thus $R_L = 20\ k\Omega$.

Step 4. To determine what power supply voltage is necessary for this application, attention must be given to the circuit schematic shown in Figure 3. From the circuit schematic it can be seen that in order to maintain transistors Q_1, Q_2, Q_3 and Q_4 in an active region when the maximum input voltages are applied ($V_{X'} = V_{Y'} = 10$ V or $V_X = 5.0$ V, $V_Y = 5.0$ V), their respective collector voltage should be at least a few tenths of a volt higher than the maximum input voltage. It should also be noticed that the collector voltage of transistors Q_3 and Q_4 is at a potential which is two diode-drops below the voltage at Pin 1. Thus, the voltage at Pin 1 should be about 2.0 V higher than the maximum input voltage. Therefore, to handle +5.0 V at the inputs, the voltage at Pin 1 must be at least +7.0 V. Let $V_1 = 9.0$ Vdc.

Since the current flowing into Pin 1 is always equal to $2I_3$, the voltage at Pin 1 can be set by placing a resistor (R_1) from Pin 1 to the positive supply:

$$R_1 = \frac{V^+ - V_1}{2I_3}$$

$$\text{Let } V+ = 15\ V\text{, then } R_1 = \frac{15\ V - 9.0\ V}{(2)\ (1.0\ mA)}$$

$$R_1 = 3.0\ k\Omega.$$

Note that the voltage at the base of transistors Q_5, Q_6, Q_7 and Q_8 is one diode-drop below the voltage at Pin 1. Thus, in order that these transistors stay active, the voltage at Pins 2 and 14 should be approximately halfway between the voltage at Pin 1 and the positive supply voltage. For this example, the voltage at Pins 2 and 14 should be approximately 11 V.

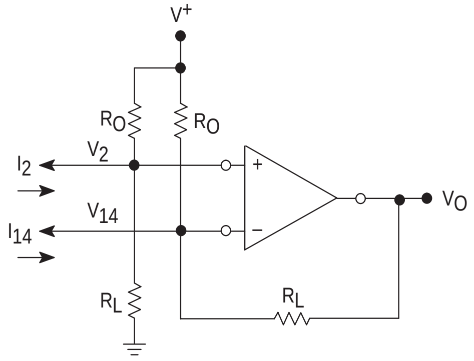
Step 5. For dc applications, such as the multiply, divide and square-root functions, it is usually desirable to convert the differential output to a single-ended output voltage referenced to ground. The circuit shown in Figure 22 performs this function. It can be shown that the output voltage of this circuit is given by:

$$V_O = (I_2 - I_{14})\ R_L$$

$$\text{And since } I_A - I_B = I_2 - I_{14} = \frac{2I_X\ I_Y}{I_3} = \frac{2V_XV_Y}{I_3R_XR_Y}$$

then $V_O = \dfrac{2R_L\ V_X'\ V_Y'}{4R_X\ R_X\ I_3}$ where, $V_X'\ V_Y'$ is the voltage at the input to the voltage dividers.

Figure 22. Level Shift Circuit



The choice of an operational amplifier for this application should have low bias currents, low offset current, and a high common mode input voltage range as well as a high common mode rejection ratio. The MC1456, and MC1741C operational amplifiers meet these requirements.

Referring to Figure 21, the level shift components will be determined. When $V_X = V_Y = 0$, the currents I_2 and I_{14} will be equal to I_{13}. In Step 3, R_L was found to be 20 kΩ and in Step 4, V_2 and V_{14} were found to be approximately 11 V. From this information R_O can be found easily from the following equation (neglecting the operational amplifiers bias current):

$$\frac{V2}{R_L} + I_{13} = \frac{V^+ - V_2}{R_O}$$

And for this example, $\frac{11\ V}{20\ k\Omega} + 1.0\ mA = \frac{15\ V - 11\ V}{R_O}$

Solving for R_O: $R_O = 2.6\ k\Omega$, thus, select $R_O = 3.0\ k\Omega$

For $R_O = 3.0\ k\Omega$, the voltage at Pins 2 and 14 is calculated to be:

$$V_2 = V_{14} = 10.4\ V.$$

The linearity of this circuit (Figure 21) is likely to be as good or better than the circuit of Figure 5. Further improvements are possible as shown in Figure 23 where R_Y has been increased substantially to improve the Y linearity, and R_X decreased somewhat so as not to materially affect the X linearity. This avoids increasing R_L significantly in order to maintain a K of 0.1.

The versatility of the MC1495 allows the user to to optimize its performance for various input and output signal levels.

OFFSET AND SCALE FACTOR ADJUSTMENT

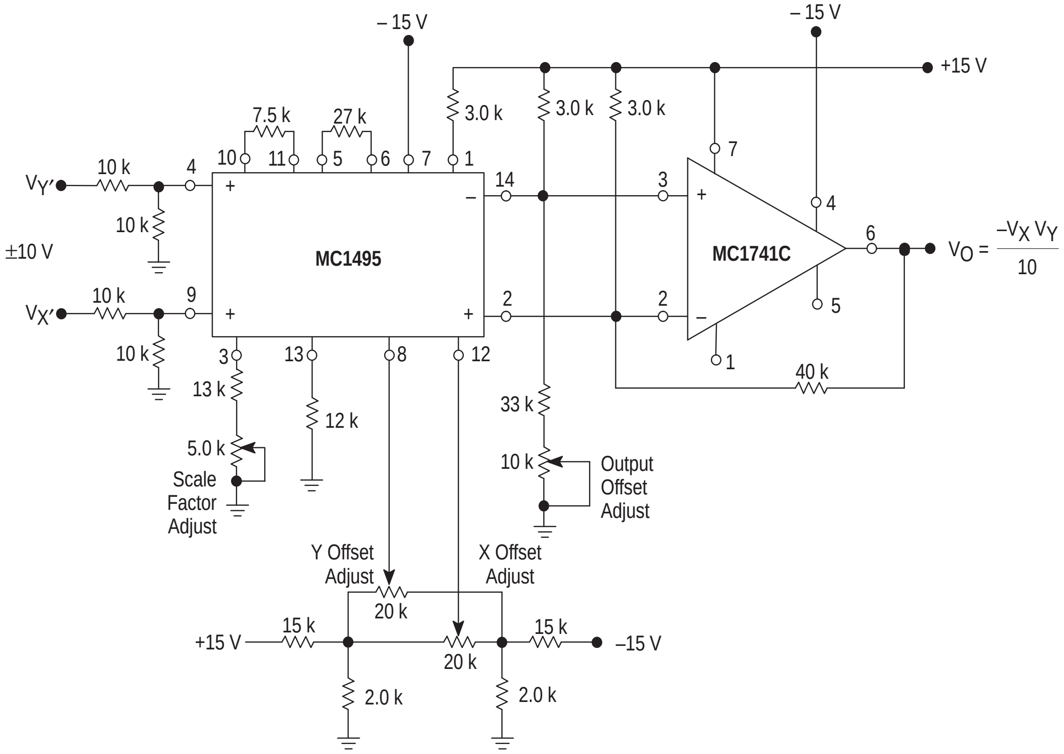
Offset Voltages

Within the monolithic multiplier (Figure 3) transistor base-emitter junctions are typically matched within 1.0 mV and resistors are typically matched within 2%. Even with this careful matching, an output error can occur. This output error is comprised of X-input offset voltage, Y-input offset voltage, and output offset voltage. These errors can be adjusted to zero with the techniques shown in Figure 21. Offset terms can be shown analytically by the transfer function:

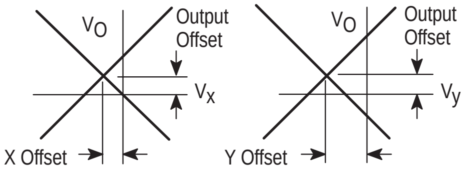
$$V_O = K[V_x \pm V_{iox} \pm V_{x(off)}]\ [V_y \pm V_{ioy} \pm V_{y(off)}] \pm V_{OO} \quad (1)$$

Where:
K = scale factor
V_x = “x” input voltage
V_y = “y” input voltage
V_{iox} = “x” input offset voltage
V_{ioy} = “y” input offset voltage
$V_{x(off)}$ = “x” input offset adjust voltage
$V_{y(off)}$ = “y” input offset adjust voltage
V_{OO} = output offset voltage.

Figure 23. Multiplier with Improved Linearity



X, Y and Output Offset Voltages



For most dc applications, all three offset adjust potentiometers (P_1, P_2, P_4) will be necessary. One or more offset adjust potentiometers can be eliminated for ac applications (see Figures 28, 29, 30, 31).

If well regulated supply voltages are available, the offset adjust circuit of Figure 13 is recommended. Otherwise, the circuit of Figure 14 will greatly reduce the sensitivity to power supply changes.

Scale Factor

The scale factor K is set by P_3 (Figure 21). P_3 varies I_3 which inversely controls the scale factor K. It should be noted that current I_3 is one-half the current through R_1. R_1 sets the bias level for Q_5, Q_6, Q_7, and Q_8 (see Figure 3). Therefore, to be sure that these devices remain active under all conditions of input and output swing, care should be exercised in adjusting P_3 over wide voltage ranges (see General Design Procedure).

Adjustment Procedures

The following adjustment procedure should be used to null the offsets and set the scale factor for the multiply mode of operation, (see Figure 21).

1. X-Input Offset
   (a) Connect oscillator (1.0 kHz, 5.0 V_{pp} sinewave) to the Y-input (Pin 4).
   (b) Connect X-input (Pin 9) to ground.
   (c) Adjust X offset potentiometer (P_2) for an ac null at the output.
2. Y-Input Offset
   (a) Connect oscillator (1.0 kHz, 5.0 V_{pp} sinewave) to the X-input (Pin 9).
   (b) Connect Y-input (Pin 4) to ground.
   (c) Adjust Y offset potentiometer (P_1) for an ac null at the output.
3. Output Offset
   (a) Connect both X and Y-inputs to ground.
   (b) Adjust output offset potentiometer (P_4) until the output voltage (V_O) is 0 Vdc.
4. Scale Factor
   (a) Apply +10 Vdc to both the X and Y-inputs.
   (b) Adjust P_3 to achieve + 10 V at the output.
5. Repeat steps 1 through 4 as necessary.

The ability to accurately adjust the MC1495 depends upon the characteristics of potentiometers P_1 through P_4. Multi-turn, infinite resolution potentiometers with low temperature coefficients are recommended.

DC APPLICATIONS

Multiply

The circuit shown in Figure 21 may be used to multiply signals from dc to 100 kHz. Input levels to the actual multiplier are 5.0 V (max). With resistive voltage dividers the maximum could be very large however, for this application two-to-one dividers have been used so that the maximum input level is 10 V. The maximum output level has also been designed for 10 V (max).

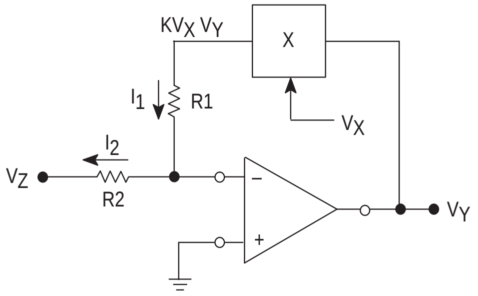
Squaring Circuit

If the two inputs are tied together, the resultant function is squaring; that is $V_O = KV^2$ where K is the scale factor. Note that all error terms can be eliminated with only three adjustment potentiometers, thus eliminating one of the input offset adjustments. Procedures for nulling with adjustments are given as follows:

A. AC Procedure:
   1. Connect oscillator (1.0 kHz, 15 V_{pp}) to input.
   2. Monitor output at 2.0 kHz with tuned voltmeter and adjust P_3 for desired gain. (Be sure to peak response of the voltmeter.)
   3. Tune voltmeter to 1.0 kHz and adjust P_1 for a minimum output voltage.
   4. Ground input and adjust P_4 (output offset) for 0 Vdc output.
   5. Repeat steps 1 through 4 as necessary.

B. DC Procedure:
   1. Set $V_X = V_Y = 0$ V and adjust P_4 (output offset potentiometer) such that $V_O = 0$ Vdc
   2. Set $V_X = V_Y = 1.0$ V and adjust P_1 (Y-input offset potentiometer) such that the output voltage is + 0.100 V.
   3. Set $V_X = V_Y = 10$ Vdc and adjust P_3 such that the output voltage is + 10 V.
   4. Set $V_X = V_Y = –10$ Vdc. Repeat steps 1 through 3 as necessary.

Figure 24. Basic Divide Circuit



Divide Circuit

Consider the circuit shown in Figure 24 in which the multiplier is placed in the feedback path of an operational amplifier. For this configuration, the operational amplifier will maintain a “virtual ground” at the inverting (–) input. Assuming that the bias current of the operational amplifier is negligible, then $I_1 = I_2$ and,

$$\frac{KV_XV_Y}{R1} = \frac{-V_Z}{R2} \tag{1}$$

$$\text{Solving for } V_Y, \quad V_Y = \frac{-R1}{R2\,K}\,\frac{V_Z}{V_X} \tag{2}$$

$$\text{If R1=R2,} \quad V_Y = \frac{-V_Z}{KV_X} \tag{3}$$

$$\text{If R1= KR2,} \quad V_Y = \frac{-V_Z}{V_X} \tag{4}$$

Hence, the output voltage is the ratio of V_Z to V_X and provides a divide function. This analysis is, of course, the ideal condition. If the multiplier error is taken into account, the output voltage is found to be:

$$V_Y = -\left[\frac{R1}{R2\,K}\right]\frac{V_Z}{V_X} + \frac{\Delta E}{KV_X} \tag{5}$$

where ΔE is the error voltage at the output of the multiplier. From this equation, it is seen that divide accuracy is strongly dependent upon the accuracy at which the multiplier can be set, particularly at small values of V_Y. For example, assume that R1 = R2, and K = 1/10. For these conditions the output of the divide circuit is given by:

$$V_Y = \frac{-10\,V_Z}{V_X} + \frac{10\,\Delta E}{V_X} \tag{6}$$

From Equation 6, it is seen that only when $V_X = 10$ V is the error voltage of the divide circuit as low as the error of the multiply circuit. For example, when V_X is small, (0.1 V) the error voltage of the divide circuit can be expected to be a hundred times the error of the basic multiplier circuit.

In terms of percentage error,

$$\text{percentage error} = \frac{\text{error}}{\text{actual}} \times 100\%$$

or from Equation (5),

$$PE_D = \frac{\dfrac{\Delta E}{KV_X}}{\left[\dfrac{R1}{R2\,K}\right]\dfrac{V_Z}{V_X}} = \left[\frac{R2}{R1}\right]\frac{\Delta E}{V_Z} \tag{7}$$

From Equation 7, the percentage error is inversely related to voltage V_Z (i.e., for increasing values of V_Z, the percentage error decreases).

A circuit that performs the divide function is shown in Figure 25.

Two things should be emphasized concerning Figure 25.

1. The input voltage ($V_{X'}$) must be greater than zero and must be positive. This insures that the current out of Pin 2 of the multiplier will always be in a direction compatible with the polarity of V_Z.
2. Pin 2 and 14 of the multiplier have been interchanged in respect to the operational amplifiers input terminals. In this instance, Figure 25 differs from the circuit connection shown in Figure 21; necessitated to insure negative feedback around the loop.

A suggested adjustment procedure for the divide circuit.

1. Set $V_Z = 0$ V and adjust the output offset potentiometer (P_4) until the output voltage (V_O) remains at some (not necessarily zero) constant value as $V_{X'}$ is varied between +1.0 V and +10 V.
2. Keep V_Z at 0 V, set $V_{X'}$ at +10 V and adjust the Y input offset potentiometer (P_1) until $V_O = 0$ V.
3. Let $V_{X'} = V_Z$ and adjust the X-input offset potentiometer (P_2) until the output voltage remains at some (not necessarily – 10 V) constant value as $V_Z = V_{X'}$ is varied between +1.0 and +10 V.
4. Keep $V_{X'} = V_Z$ and adjust the scale factor potentiometer (P_3) until the average value of V_O is –10 V as $V_Z = V_{X'}$ is varied between +1.0 V and +10 V.
5. Repeat steps 1 through 4 as necessary to achieve optimum performance.

Figure 25. Divide Circuit

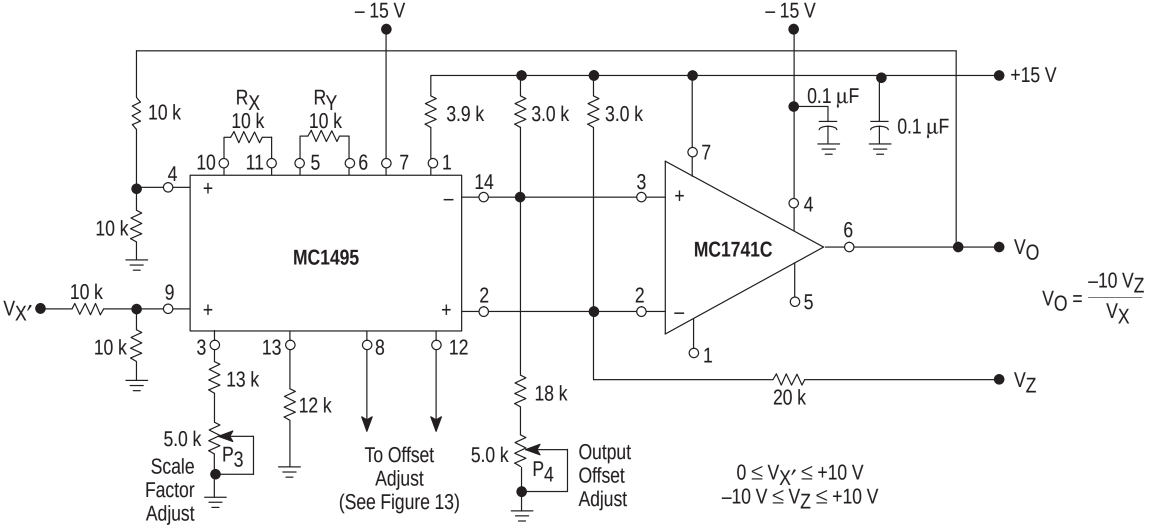
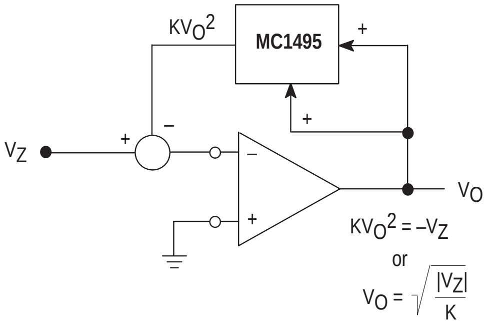


Figure 26. Basic Square Root Circuit



Square Root

A special case of the divide circuit in which the two inputs to the multiplier are connected together is the square root function as indicated in Figure 26. This circuit may suffer from latch-up problems similar to those of the divide circuit. Note that only one polarity of input is allowed and diode clamping (see Figure 27) protects against accidental latch-up.

This circuit also may be adjusted in the closed-loop mode as follows:

1. Set V_Z to –0.01 V and adjust P_4 (output offset) for V_O = +0.316 V, being careful to approach the output from the positive side to preclude the effect of the output diode clamping.
2. Set V_Z to –0.9 V and adjust P_2 (X adjust) for V_O = +3.0 V.
3. Set V_Z to –10 V and adjust P_3 (scale factor adjust) for V_O = +10 V.
4. Steps 1 through 3 may be repeated as necessary to achieve desired accuracy.

AC APPLICATIONS

The applications that follow demonstrate the versatility of the monolithic multiplier. If a potted multiplier is used for these cases, the results generally would not be as good because the potted units have circuits that, although they optimize dc multiplication operation, can hinder ac applications.

Frequency doubling often is done with a diode where the fundamental plus a series of harmonics are generated. However, extensive filtering is required to obtain the desired harmonic, and the second harmonic obtained under this technique usually is small in magnitude and requires amplification.

When a multiplier is used to double frequency the second harmonic is obtained directly, except for a dc term, which can be removed with ac coupling.

$$e_O = KE^2 \cos^2 \omega t$$

$$e_O = \frac{KE^2}{2} (1 + \cos 2\omega t).$$

A potted multiplier can be used to obtain the double frequency component, but frequency would be limited by its internal level-shift amplififer. In the monolithic units, the amplifier is omitted.

In a typical doubler circuit, conventional ± 15 V supplies are used. An input dynamic range of 5.0 V peak-to-peak is allowed. The circuit generates wave-forms that are double frequency; less than 1% distortion is encountered without filtering. The configuration has been successfully used in excess of 200 kHz; reducing the scale factor by decreasing the load resistors can further expand the bandwidth.

Figure 29 represents an application for the monolithic multiplier as a balanced modulator. Here, the audio input signal is 1.6 kHz and the carrier is 40 kHz.

Figure 27. Square Root Circuit

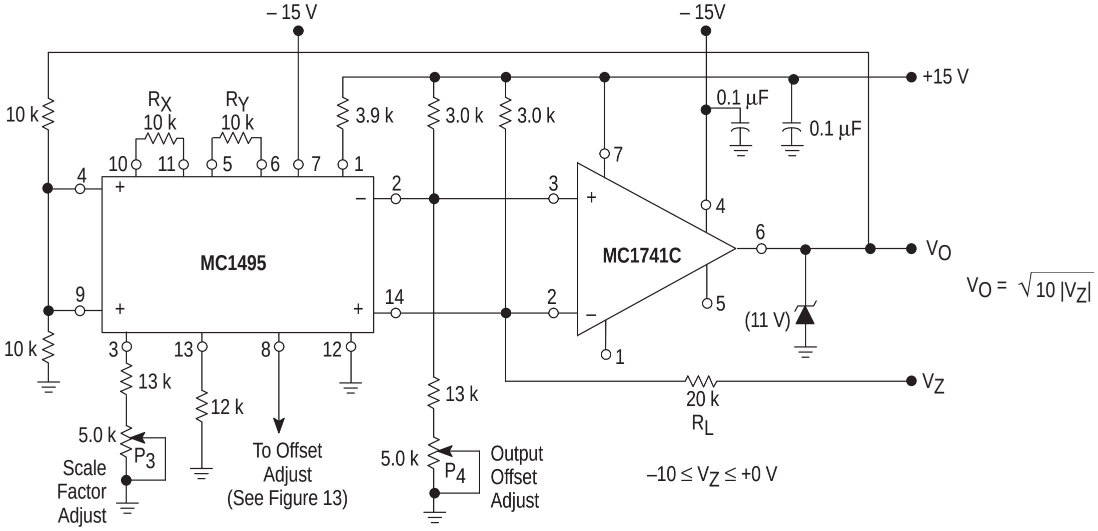
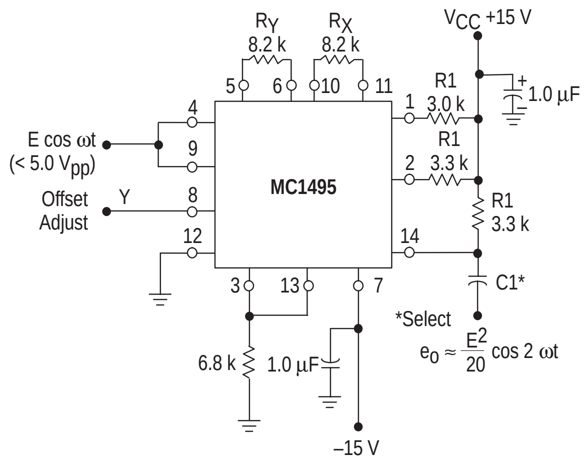
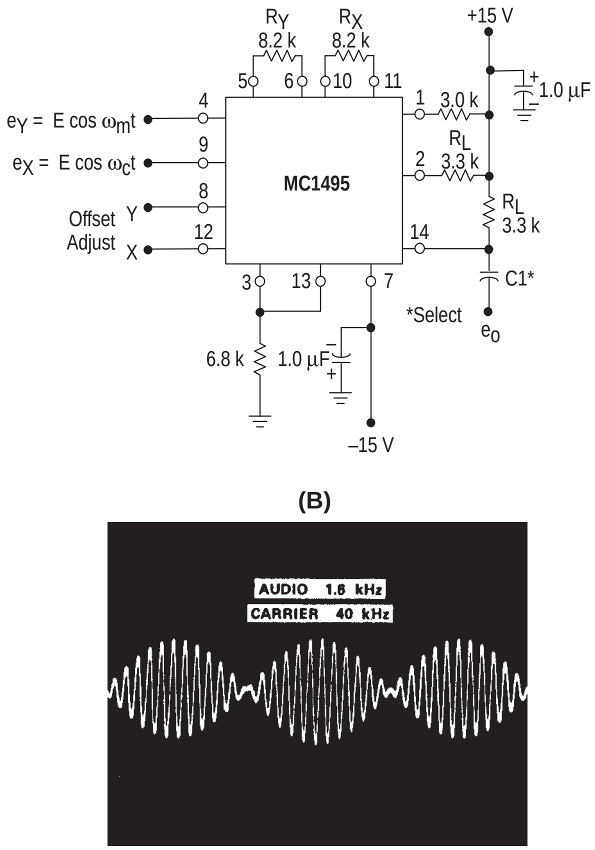


Figure 28. Frequency Doubler



When two equal cosine waves are applied to X and Y, the result is a wave shape of twice the input frequency. For this example the input was a 10 kHz signal, output was 20 kHz.

Figure 29. Balanced Modulator



(A)

(B)

The defining equation for balanced modulation is

$$K(E_m \cos \omega_m t)\,(E_c \cos \omega_c t) =$$

$$\frac{KE_c\,E_m}{2}\,[\,\cos(\omega_c + \omega_m)t + \cos(\omega_c - \omega_m)\,t\,]$$

where ω_c is the carrier frequency, ω_m is the modulator frequency and K is the multiplier gain constant.

AC coupling at the output eliminates the need for level translation or an operational amplifier; a higher operating frequency results.

A problem common to communications is to extract the intelligence from single-sideband received signal. The ssb signal is of the form:

$$e_{ssb} = A \cos(\omega_c + \omega_m)\,t$$

and if multiplied by the appropriate carrier waveform, cos ω_ct,

$$e_{ssb}e_{carrier} = \frac{AK}{2}\,[\cos(2\omega_c + \omega_m)t + \cos(\omega_c)\,t\,].$$

If the frequency of the band-limited carrier signal (ω_c) is ascertained in advance, the designer can insert a low pass filter and obtain the (AK/2) (cosω_ct) term with ease. He/she also can use an operational amplifier for a combination level shift-active filter, as an external component. But in potted multipliers, even if the frequency range can be covered, the operational amplifier is inside and not accessible, so the user must accept the level shifting provided, and still add a low pass filter.

Amplitude Modulation

The multiplier performs amplitude modulation, similar to balanced modulation, when a dc term is added to the modulating signal with the Y-offset adjust potentiometer (see Figure 30).

Here, the identity is:

$$E_m(1 + m \cos \omega_m t)\,E_c \cos \omega_c t = KE_mE_c \cos \omega_c t +$$

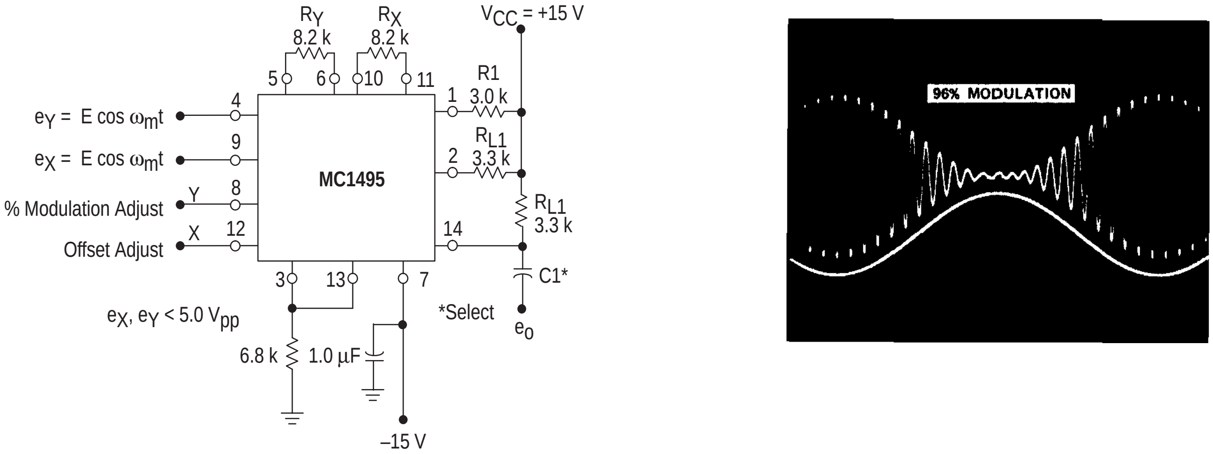
$$\frac{KE_mE_cm}{2}\,[\,\cos(\omega_c + \omega_m)t + \cos(\omega_c - \omega_m)\,t\,]$$

where m indicates the degrees of modulation. Since m is adjustable, via potentiometer P_1, 100% modulation is possible. Without extensive tweaking, 96% modulation may be obtained where ω_c and ω_m are the same as in the balanced modulator example.

Linear Gain Control

To obtain linear gain control, the designer can feed to one of the two MC1495 inputs a signal that will vary the unit's gain. The following example demonstrates the feasibility of this application. Suppose a 200 kHz sinewave, 1.0 V peak-to-peak, is the signal to which a gain control will be added. The dynamic range of the control voltage V_C is 0 V to +1.0 V. These must be ascertained and the proper values of R_X and R_Y can be selected for optimum performance. For the 200 kHz operating frequency, load resistors of 100 Ω were chosen to broaden the operating bandwidth of the multiplier, but gain was sacrificed. It may be made up with an amplifier operating at the appropriate frequency (see Figure 31).

Figure 30. Amplitude Modulation



The signal is applied to the unit's Y-input. Since the total input range is limited to 1.0 V_{pp}, a 2.0 V swing, a current source of 2.0 mA and an R_Y value of 1.0 kΩ is chosen. This takes best advantage of the dynamic range and insures linear operation in the Y-channel.

Since the X-input varies between 0 and +1.0 V, the current source selected was 1.0 mA, and the R_X value chosen was 2.0 kΩ. This also insures linear operation over the X-input dynamic range. Choosing R_L = 100 assures wide bandwidth operation.

Hence, the scale factor for this configuration is:

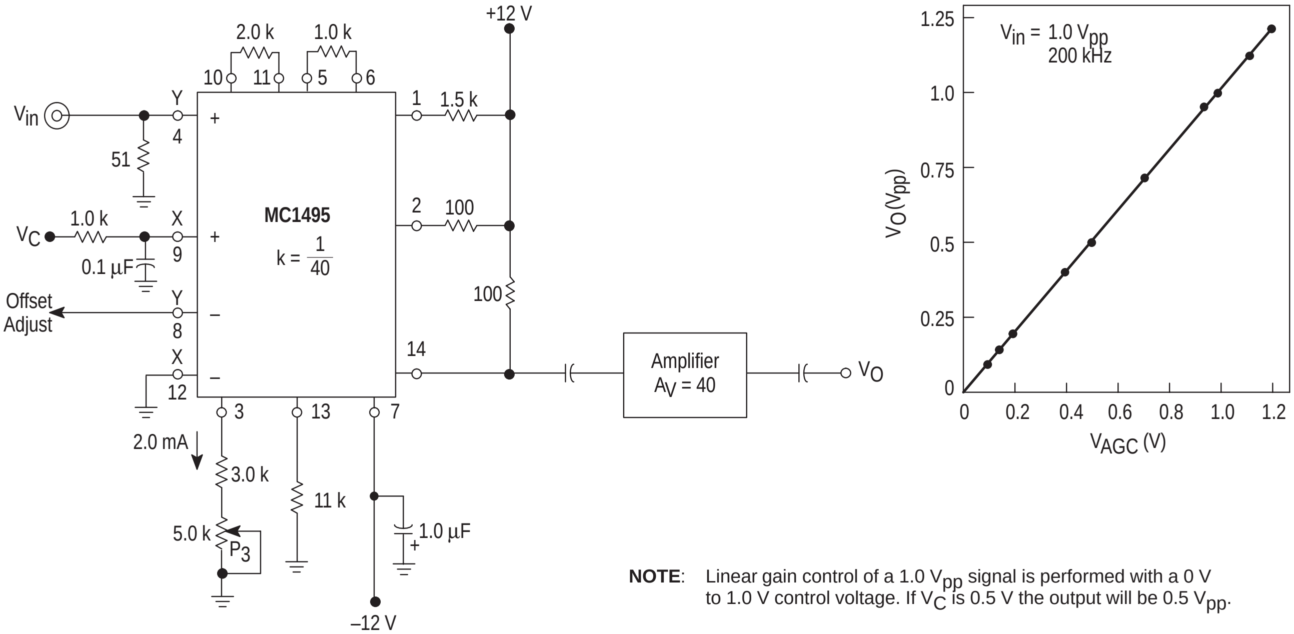
$$K = \frac{R_L}{R_X\, R_Y\, I_3}$$

$$= \frac{100}{(2\ k)\ (1\ k)\ (2 \times 10^3)}\ V^{-1}$$

$$= \frac{1}{40}\ V^{-1}$$

The 2 in the numerator of the equation is missing in this scale factor expression because the output is single-ended and ac coupled.

Figure 31. Linear Gain Control



NOTE: Linear gain control of a 1.0 V_{pp} signal is performed with a 0 V to 1.0 V control voltage. If V_C is 0.5 V the output will be 0.5 V_{pp}.

MOTOROLA

MC3456

Dual Timing Circuit

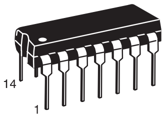
The MC3456 dual timing circuit is a highly stable controller capable of producing accurate time delays, or oscillation. Additional terminals are provided for triggering or resetting if desired. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor per timer. For astable operation as an oscillator, the free running frequency and the duty cycle are both accurately controlled with two external resistors and one capacitor per timer. The circuit may be triggered and reset on falling waveforms, and the output structure can source or sink up to 200 mA or drive MTTL circuits.

- Direct Replacement for NE556/SE556 Timers
- Timing from Microseconds through Hours
- Operates in Both Astable and Monostable Modes
- Adjustable Duty Cycle
- High Current Output can Source or Sink 200 mA
- Output can Drive MTTL
- Temperature Stability of 0.005% per °C
- Normally “On” or Normally “Off” Output
- Dual Version of the Popular MC1455 Timer

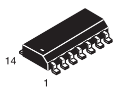
DUAL TIMING CIRCUIT

SEMICONDUCTOR
TECHNICAL DATA

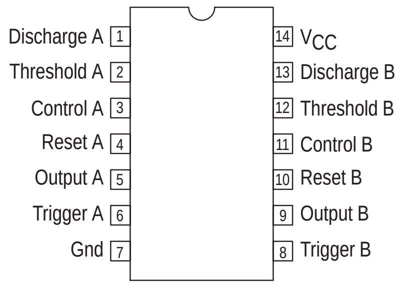
P SUFFIX
PLASTIC PACKAGE
CASE 646



D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–14)



PIN CONNECTIONS

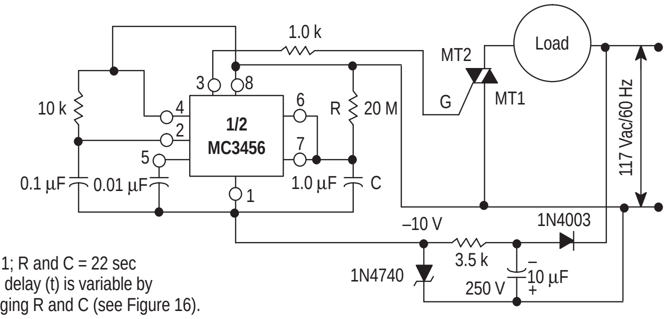


(Top View)

ORDERING INFORMATION

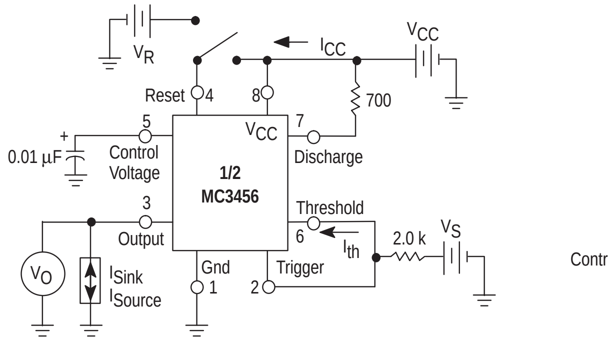
Device	Operating Temperature Range	Package
MC3456P	0° to +70°C	Plastic DIP
NE556D		SO–14

Figure 1. 22 Second Solid State Time Delay Relay Circuit



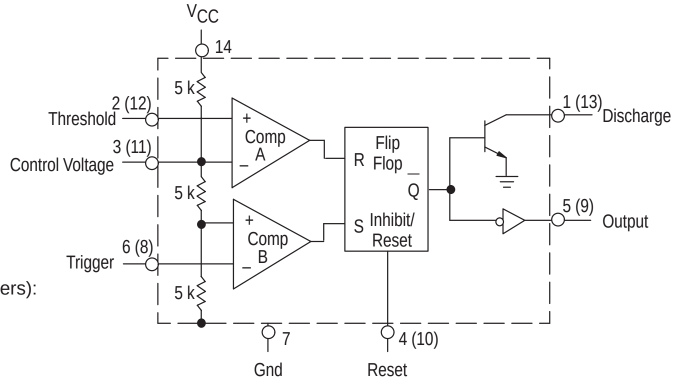
t = 1.1; R and C = 22 sec
Time delay (t) is variable by
changing R and C (see Figure 16).

Figure 3. General Test Circuit



Test circuit for measuring DC parameters (to set output and measure parameters):
a) When $V_S \geq 2/3\ V_{CC}$, V_O is low.
b) When $V_S \leq 1/3\ V_{CC}$, V_O is high.
c) When V_O is low, Pin 7 sinks current. To test for Reset, set V_O high, apply Reset voltage, and test for current flowing into Pin 7. When Reset is not in use, it should be tied to V_{CC}.

Figure 2. Block Diagram (1/2 Shown)



MAXIMUM RATINGS (T_A = +25°C, unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	+18	Vdc
Discharge Current	I_{dis}	200	mA
Power Dissipation (Package Limitation)	P_D		
P Suffix, Plastic Package, Case 646		625	mW
Derate above T_A = +25°C		5.0	mW/°C
D Suffix, Plastic Package, Case 751		1.0	W
Derate above T_A = +25°C		8.0	mW/°C
Operating Ambient Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

ELECTRICAL CHARACTERISTICS (T_A = +25°C, V_{CC} = +15 V, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	–	16	V
Supply Current	I_{CC}				mA
V_{CC} = 5.0 V, R_L = ∞		–	6.0	12	
V_{CC} = 15 V, R_L = ∞ Low State, (Note 1)		–	20	30	
Timing Error (Note 2)					
Monostable Mode (R_A = 2.0 kΩ; C = 0.1 μF)					
Initial Accuracy		–	0.75	–	%
Drift with Temperature		–	50	–	PPM/°C
Drift with Supply Voltage		–	0.1	–	%/V
Astable Mode (R_A = R_B = 2.0 kΩ to 100 kΩ; C = 0.01 μF)					
Initial Accuracy		–	2.25	–	%
Drift with Temperature		–	150	–	PPM/°C
Drift with Supply Voltage		–	0.3	–	%/V
Threshold Voltage	V_{th}	–	2/3	–	xV_{CC}
Trigger Voltage	V_T				V
V_{CC} = 15 V		–	5.0	–	
V_{CC} = 5.0 V		–	1.67	–	
Trigger Current	I_T	–	0.5	–	μA
Reset Voltage	V_R	0.4	0.7	1.0	V
Reset Current	I_R	–	0.1	–	mA
Threshold Current (Note 3)	I_{th}	–	0.03	0.1	μA
Control Voltage Level	V_{CL}				V
V_{CC} = 15 V		9.0	10	11	
V_{CC} = 5.0 V		2.6	3.33	4.0	
Output Voltage Low	V_{OL}				
(V_{CC} = 15 V)					V
I_{Sink} = 10 mA		–	0.1	0.25	
I_{Sink} = 50 mA		–	0.4	0.75	
I_{Sink} = 100 mA		–	2.0	2.75	
I_{Sink} = 200 mA		–	2.5	–	
(V_{CC} = 5.0 V)					
I_{Sink} = 5.0 mA		–	0.25	0.35	
Output Voltage High	V_{OH}				V
(I_{Source} = 200 mA)					
V_{CC} = 15 V		–	12.5	–	
(I_{Source} = 100 mA)					
V_{CC} = 15 V		12.75	13.3	–	
V_{CC} = 5.0 V		2.75	3.3	–	
Toggle Rate R_A = 3.3 kΩ, R_B = 6.8 kΩ, C = 0.003 μF (Figure 17, 19)	–	–	100	–	kHz
Discharge Leakage Current	I_{dis}	–	20	100	nA
Rise Time of Output	t_{OLH}	–	100	–	ns
Fall Time of Output	t_{OHL}	–	100	–	ns
Matching Characteristics Between Sections					
Monostable Mode					
Initial Timing Accuracy		–	1.0	2.0	%
Timing Drift with Temperature		–	±10	–	ppm/°C
Drift with Supply Voltage		–	0.2	0.5	%/V

NOTES: 1. Supply current is typically 1.0 mA less for each output which is high.
2. Tested at V_{CC} = 5.0 V and V_{CC} = 15 V.
3. This will determine the maximum value of $R_A + R_B$ for 15 V operation. The maximum total R = 20 mΩ.

Figure 4. Trigger Pulse Width

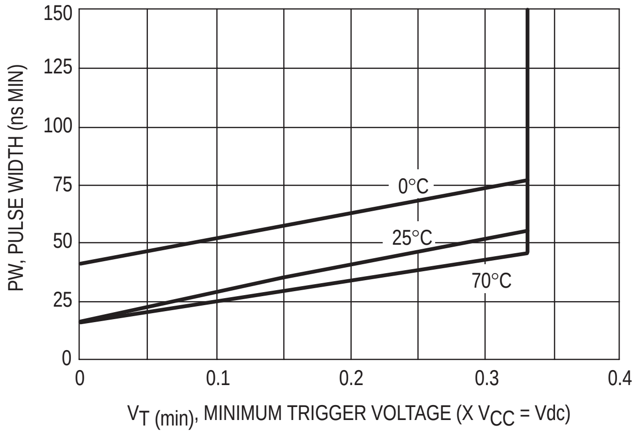


Figure 5. Supply Current

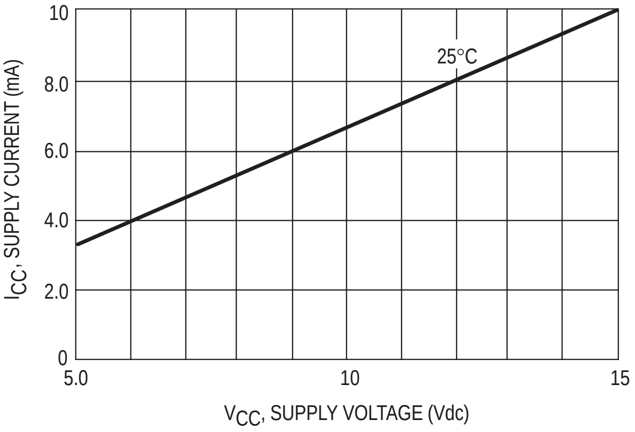


Figure 6. High Output Voltage

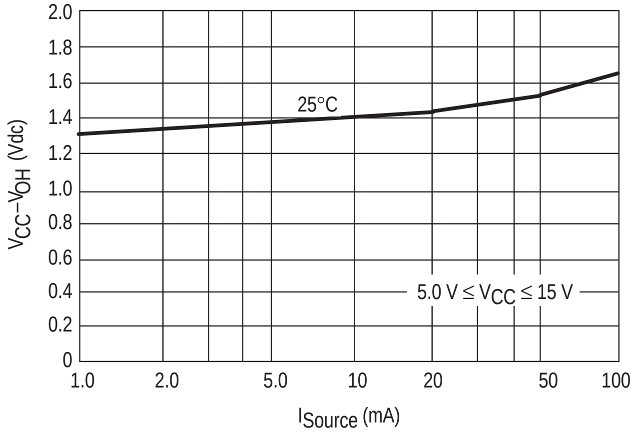


Figure 7. Low Output Voltage

(@ V_{CC} = 5.0 Vdc)

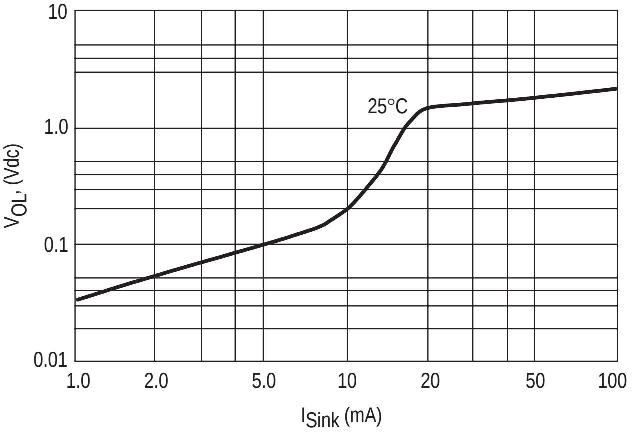


Figure 8. Low Output Voltage

(@ V_{CC} = 10 Vdc)

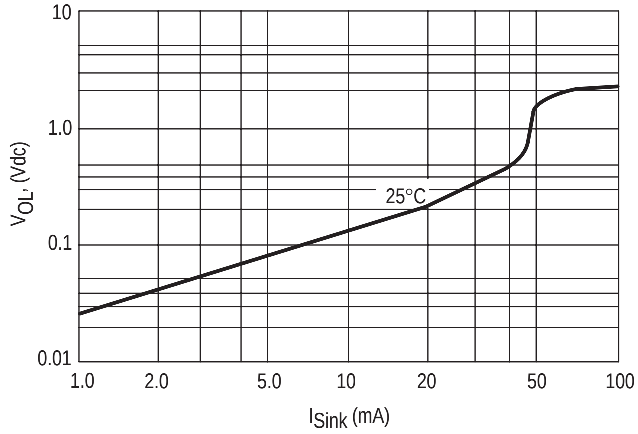


Figure 9. Low Output Voltage

(@ V_{CC} = 15 Vdc)

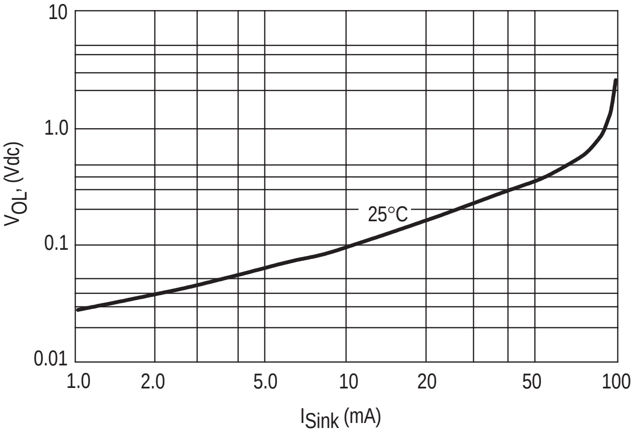


Figure 10. Delay Time versus Supply Voltage

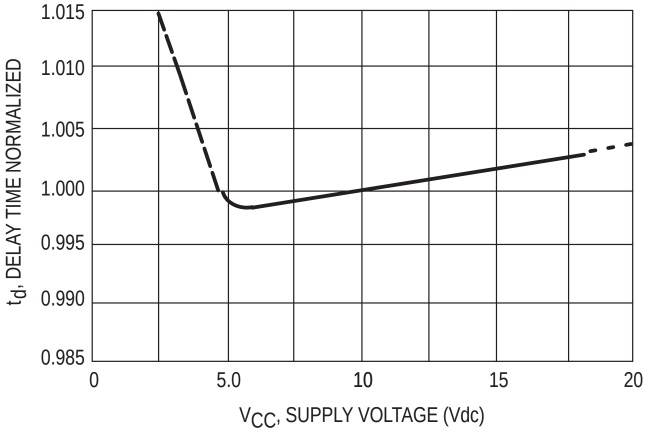


Figure 11. Delay Time versus Temperature

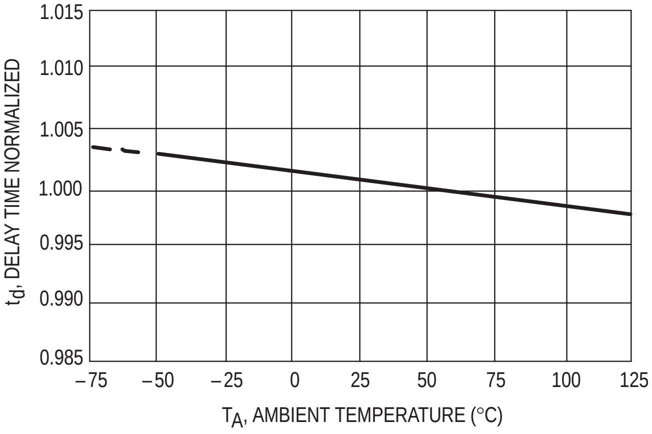
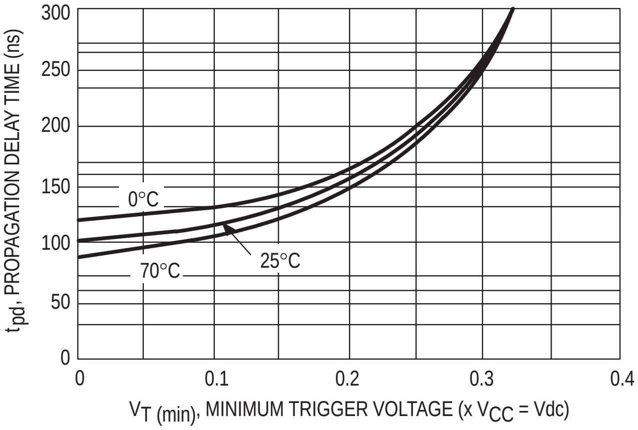


Figure 12. Propagation Delay versus Trigger Voltage



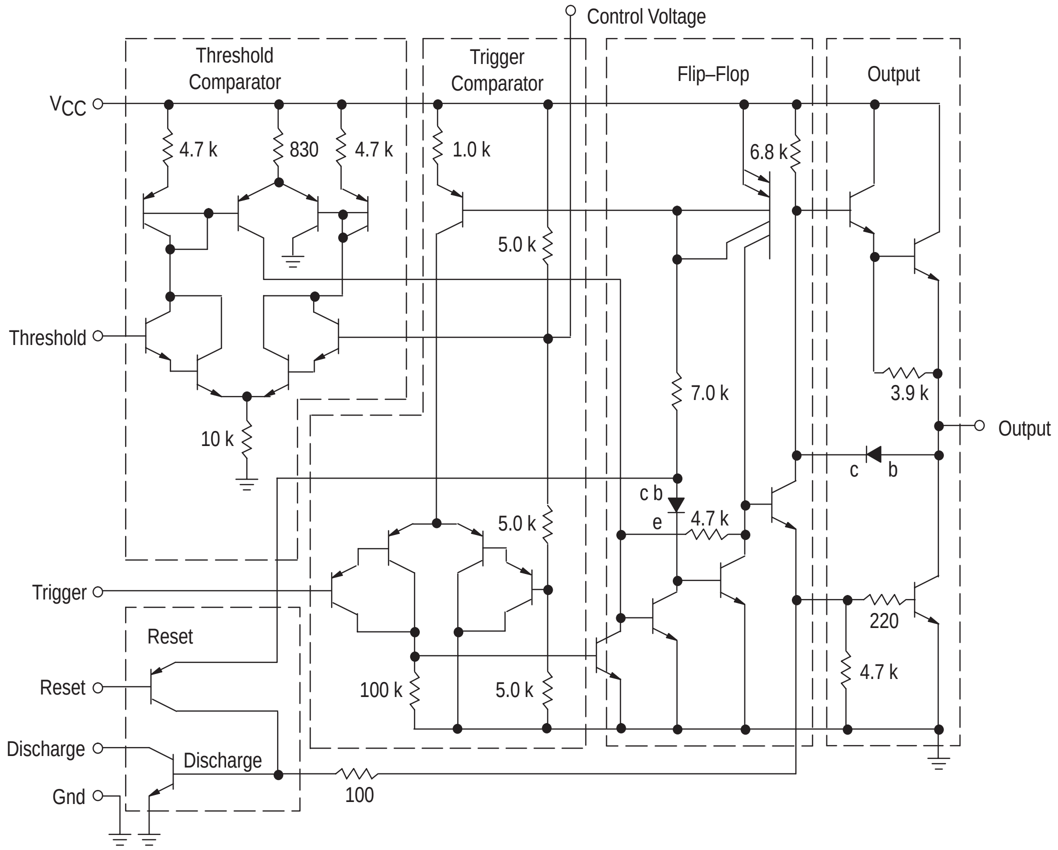


Figure 13. 1/2 Representative Circuit Schematic

GENERAL OPERATION

The MC3456 is a dual timing circuit which uses as its timing elements an external resistor/capacitor network. It can be used in both the monostable (one shot) and astable modes with frequency and duty cycle, controlled by the capacitor and resistor values. While the timing is dependent upon the external passive components, the monolithic circuit provides the starting circuit, voltage comparison and other functions needed for a complete timing circuit. Internal to the integrated circuit are two comparators, one for the input signal and the other for capacitor voltage; also a flip–flop and digital output are included. The comparator reference voltages are always a fixed ratio of the supply voltage thus providing output timing independent of supply voltage.

Monostable Mode

In the monostable mode, a capacitor and a single resistor are used for the timing network. Both the threshold terminal and the discharge transistor terminal are connected together in this mode (refer to circuit Figure 15). When the input voltage to the trigger comparator falls below 1/3 V_{CC} the comparator output triggers the flip–flop so that it's output sets low. This turns the capacitor discharge transistor "off" and drives the digital output to the high state. This condition allows the capacitor to charge at an exponential rate which is set by the RC time constant. When the capacitor voltage reaches 2/3 V_{CC} the threshold comparator resets the flip–flop. This action discharges the timing capacitor and returns the digital output to the low state. Once the flip–flop has been triggered by an input signal, it cannot be retriggered until the present timing period has been completed. The time that the output is high is given by the equation $t = 1.1\ R_A\ C$. Various combinations of R and C and their associated times are shown in Figure 14. The trigger pulse width must be less than the timing period.

A reset pin is provided to discharge the capacitor thus interrupting the timing cycle. As long as the reset pin is low, the capacitor discharge transistor is turned "on" and prevents the capacitor from charging. While the reset voltage is applied the digital output will remain the same. The reset pin should be tied to the supply voltage when not in use.

Figure 14. Time Delay

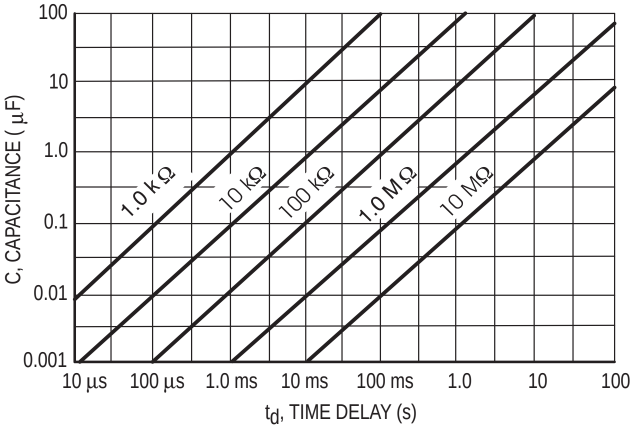
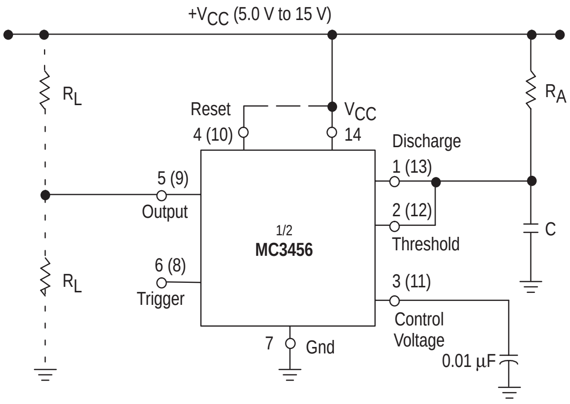
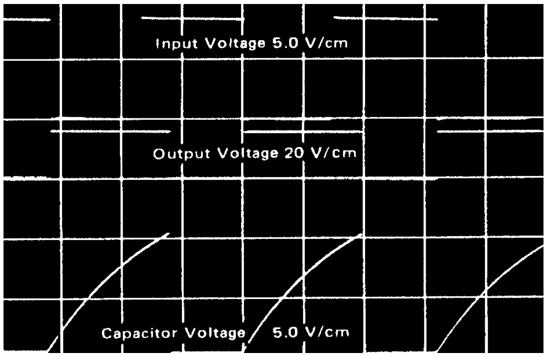


Figure 15. Monostable Circuit



Pin numbers in parenthesis ( ) indicate B–Channel

Figure 16. Monostable Waveforms



t = 50 µs/cm
(R_A = 10 kΩ, C = 0.01 µF, R_L = 1.0 kΩ, V_{CC} = 15 V)

Figure 17. Astable Circuit

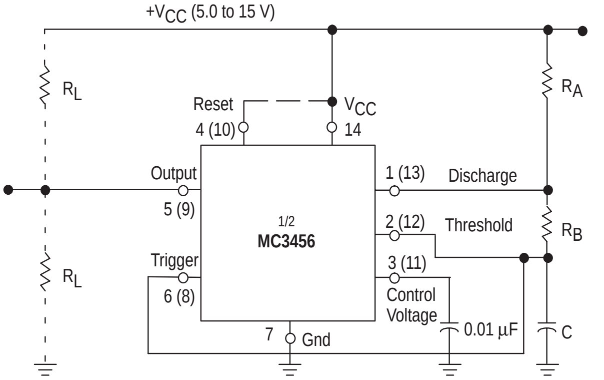
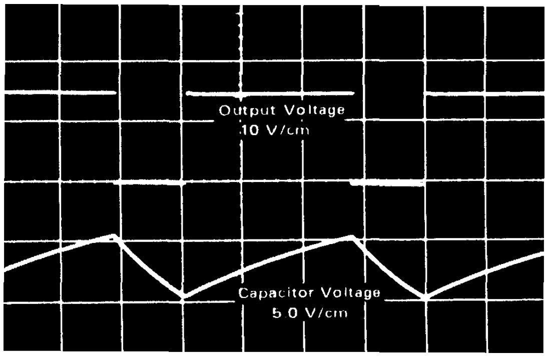


Figure 18. Astable Waveforms



t = 20 µs/cm
(R_A = 5.1 kΩ, C = 0.0 1 µF, R_L = 1.0 kΩ, R_B = 3.9 kΩ, V_{CC} = 15 V)

Astable Mode

In the astable mode the timer is connected so that it will retrigger itself and cause the capacitor voltage to oscillate between 1/3 V_{CC} and 2/3 V_{CC} (see Figure 17).

The external capacitor charges to 2/3 V_{CC} through R_A and R_B and discharges to 1/3 V_{CC} through R_B. By varying the ratio of these resistors the duty cycle can be varied. The charge and discharge times are independent of the supply voltage.

The charge time (output high) is given by:

$$t_1 = 0.695\,(R_A + R_B)\,C$$

The discharge time (output low) by:

$$t_2 = 0.695\,(R_B)\,C$$

Thus the total period is given by:

$$T = t_1 + t_2 = 0.695\,(R_A + 2R_B)\,C$$

The frequency of oscillation is then: $f = \frac{1}{T} = \frac{1.44}{(R_A + 2R_B)\,C}$

and may be easily found as shown in Figure 19.

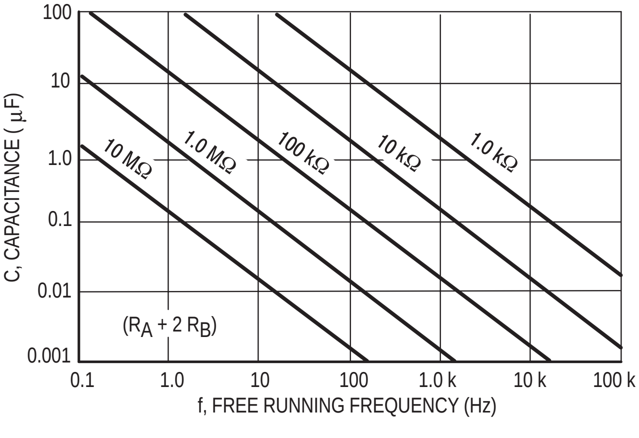
The duty cycle is given by: $DC = \frac{R_B}{R_A + 2R_B}$

To obtain the maximum duty cycle, R_A must be as small as possible; but it must also be large enough to limit the discharge current (Pin 7 current) within the maximum rating of the discharge transistor (200 mA).

The minimum value of R_A is given by:

$$R_A \geq \frac{V_{CC}\,(Vdc)}{I_7\,(A)} \geq \frac{V_{CC}\,(Vdc)}{0.2}$$

Figure 19. Free Running Frequency



APPLICATIONS INFORMATION

Tone Burst Generator

For a tone burst generator, the first timer is used as a monostable and determines the tone duration when triggered by a positive pulse at Pin 6. The second timer is enabled by the high output of the monostable. It is connected as an astable and determines the frequency of the tone.

Dual Astable Multivibrator

This dual astable multivibrator provides versatility not available with single timer circuits. The duty cycle can be adjusted from 5% to 95%. The two outputs provide two phase clock signals often required in digital systems. It can also be inhibited by use of either reset terminal.

Figure 20. Tone Burst Generator

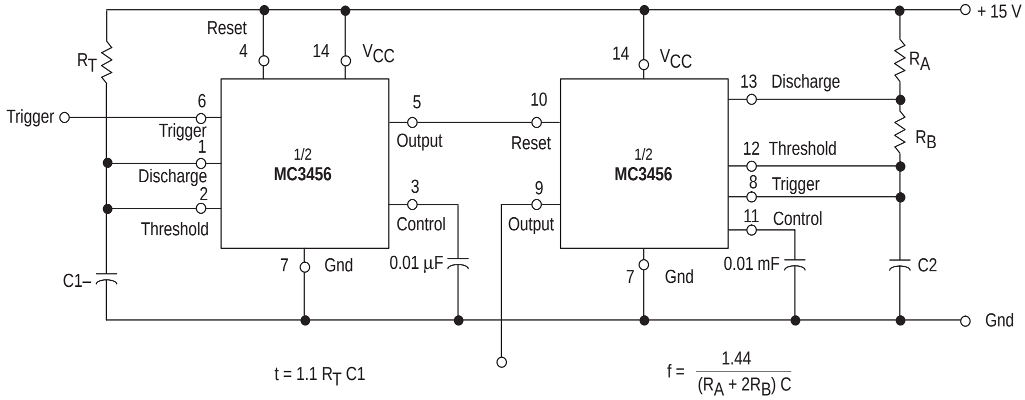
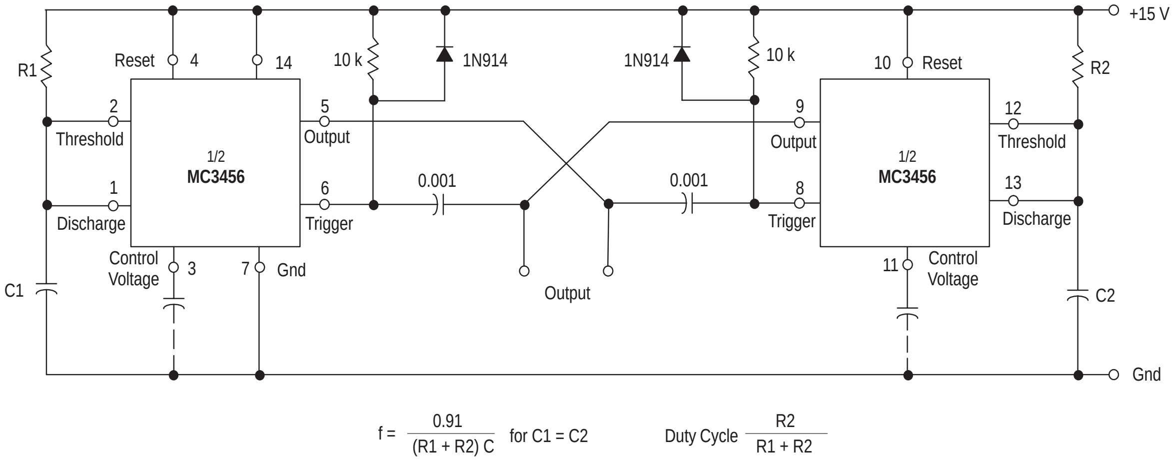


Figure 21. Dual Astable Multivibrator



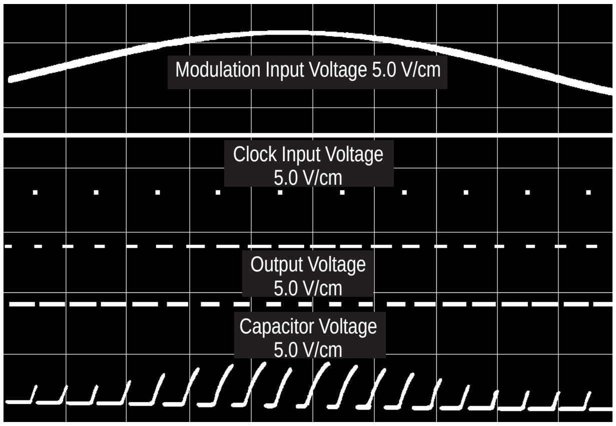
Pulse Width Modulation

If the timer is triggered with a continuous pulse train in the monostable mode of operation, the charge time of the capacitor can be varied by changing the control voltage at Pin 3. In this manner, the output pulse width can be modulated by applying a modulating signal that controls the threshold voltage.

Test Sequences

Several timers can be connected to drive each other for sequential timing. An example is shown in Figure 24 where the sequence is started by triggering the first timer which runs for 10 ms. The output then switches low momentarily and starts the second timer which runs for 50 ms and so forth.

Figure 22. Pulse Width Modulation Waveforms



t = 0.5 ms/cm
(R_A = 10 kW, C = 0.02 mF, V_{CC} = 15 V)

Figure 23. Pulse Width Modulation Circuit

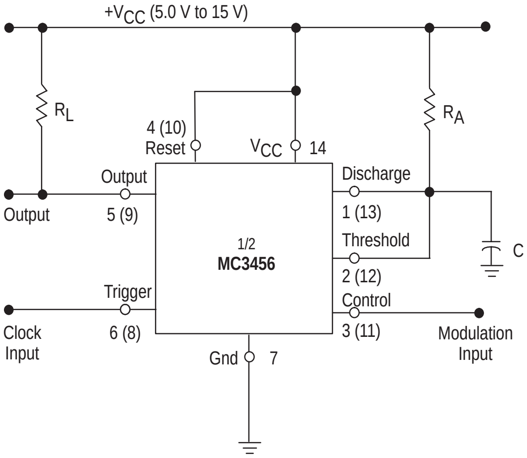
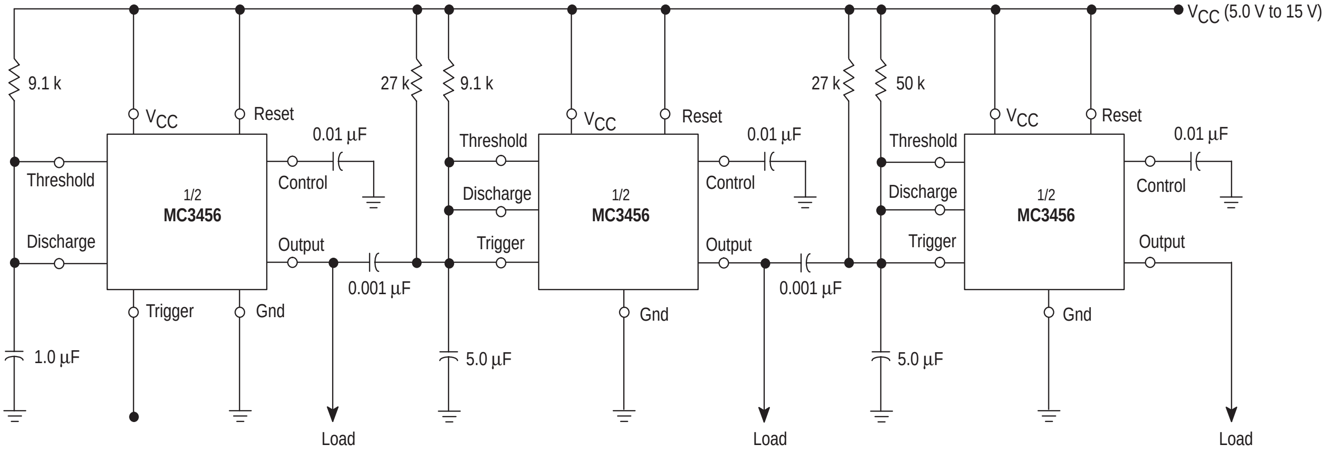


Figure 24. Sequential Timing Circuit



Tape and Reel Options

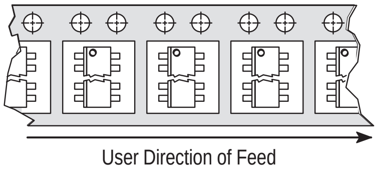
In Brief . . .

Motorola offers the convenience of Tape and Reel packaging for our growing family of standard integrated circuit products. Reels are available to support the requirements of both first and second generation pick–and–place equipment. The packaging fully conforms to the latest EIA–481A specification. The antistatic embossed tape provides a secure cavity, sealed with a peel–back cover tape.

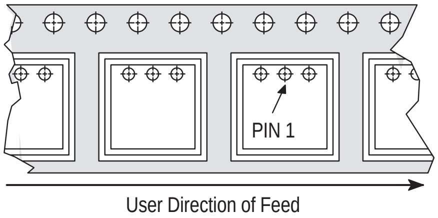
Tape and Reel Configurations

Mechanical Polarization

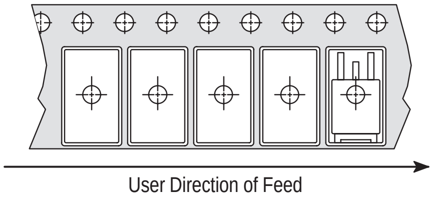
SOIC and Micro–8 DEVICES
Typical



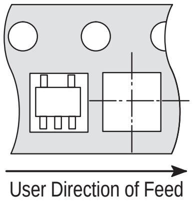
PLCC DEVICES
Typical



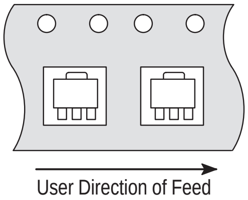
DPAK and D^{2}PAK DEVICES
Typical



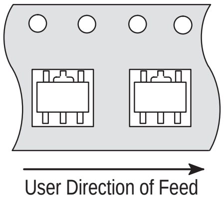
SOT–23 (5 Pin) DEVICES
Typical



SOT–89 (3 Pin) DEVICES
Typical



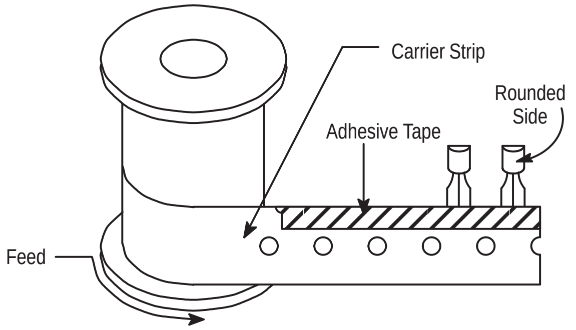
SOT–89 (5 Pin) DEVICES
Typical



Tape and Reel Configurations **(continued)**

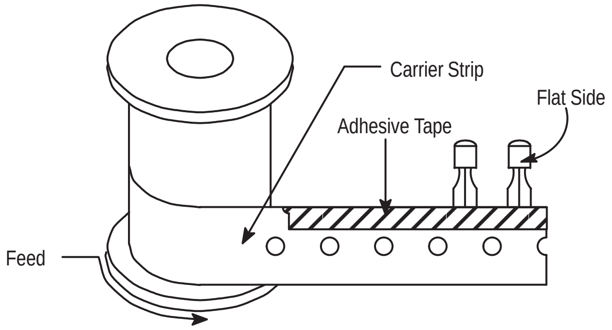
TO–92 Reel Styles

STYLE A
(Preferred)



Rounded side of transistor and adhesive tape visible.

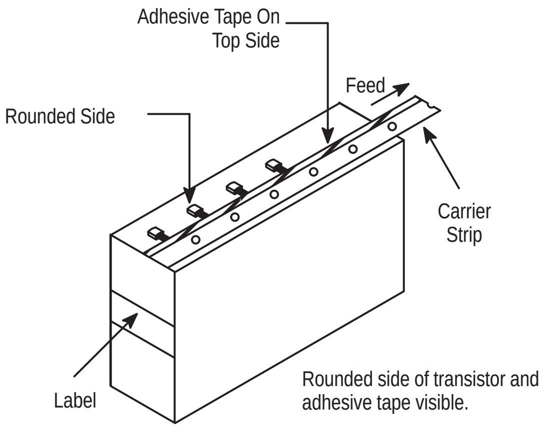
STYLE E



Flat side of transistor and adhesive tape visible.

TO–92 Ammo Pack Styles

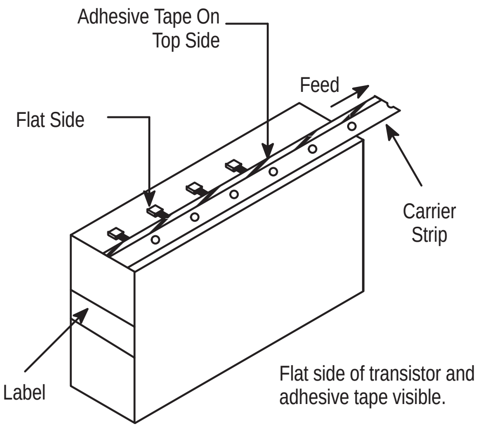
STYLE P
(Preferred)



Rounded side of transistor and adhesive tape visible.

Style P ammo pack is equivalent to Styles A and B of reel pack dependent on feed orientation from box.

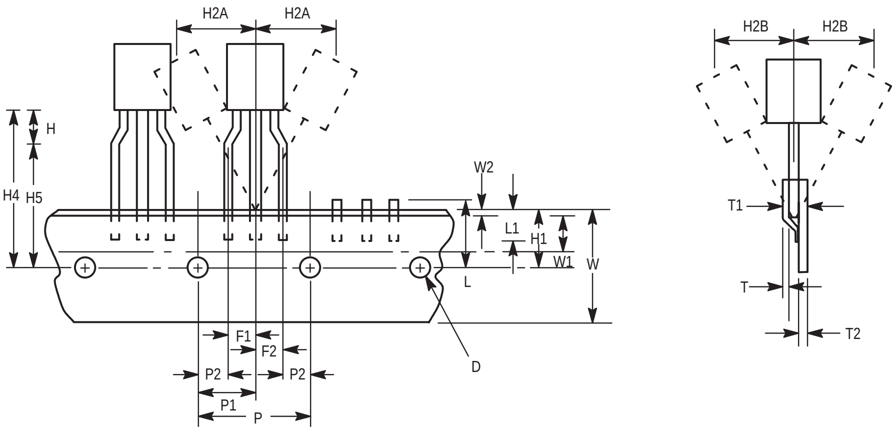
STYLE M



Flat side of transistor and adhesive tape visible.

Style M ammo pack is equivalent to Style E of reel pack dependent on feed orientation from box.

TO–92 EIA Radial Tape in Fan Fold Box or On Reel



Tape and Reel Information Table

Package	Tape Width (mm)	Devices(1) per Reel	Reel Size (inch)	Device Suffix
SO–8, SOP–8	12	2,500	13	R2
SO–14	16	2,500	13	R2
SO–16	16	2,500	13	R2
SO–16L, SO–8+8L WIDE	16	1,000	13	R2
SO–20L WIDE	24	1,000	13	R2
SO–24L WIDE	24	1,000	13	R2
SO–28L WIDE	24	1,000	13	R2
SO–28L WIDE	32	1,000	13	R3
Micro–8	12	2,500	13	R2
PLCC–20	16	1,000	13	R2
PLCC–28	24	500	13	R2
PLCC–44	32	500	13	R2
PLCC–52	32	500	13	R2
PLCC–68	44	250	13	R2
PLCC–84	44	250	13	R2
TO–226AA (TO–92)(2)	18	2,000	13	RA, RE, RP, or RM (Ammo Pack) only
DPAK	16	2,500	13	RK
D^2PAK	24	800	13	R4
SOT–23 (5 Pin)	8	3,000	7	TR
SOT–89 (3/5 Pin)	12	1,000	7	T1

(1) Minimum order quantity is 1 reel. Distributors/OEM customers may break lots or reels at their option, however broken reels may not be returned.

(2) Integrated circuits in TO–226AA packages are available in Styes A and E only, with optional “Ammo Pack” (Suffix RP or RM). The RA and RP configurations are preferred. For ordering information please contact your local Motorola Semiconductor Sales Office.

Analog MPQ Table

Tape/Reel and Ammo Pack

Package Type	Package Code	MPQ
PLCC		
Case 775	0802	1000/reel
Case 776	0804	500/reel
Case 777	0801	500/reel
SOIC		
Case 751	0095	2500/reel
Case 751A	0096	2500/reel
Case 751B	0097	2500/reel
Case 751G	2003	1000/reel
Case 751D	2005	1000/reel
Case 751E	2008	1000/reel
Case 751F	2009	1000/reel
Micro–8		
Case 846A	–	2500/reel
TO–92		
Case 29	0031	2000/reel
Case 29	0031	2000/Ammo Pack
DPAK		
Case 369A	–	2500/reel
D^{2}PAK		
Case 936	–	800/reel
SOT–23 (5 Pin)		
Case 1212	–	3000/reel
SOT–89 (3 Pin)		
Case 1213	–	1000/reel
SOT–89 (5 Pin)		
Case 1214	–	1000/reel

Packaging Information

In Brief . . .

The packaging availability for each device type is indicated on the individual data sheets and the Selector Guide. All of the outline dimensions for the packages are given in this section.

The maximum power consumption an integrated circuit can tolerate at a given operating ambient temperature can be found from the equation:

$$P_{D(TA)} = \frac{T_{J(max)} - T_A}{R_{\theta JA(Typ)}}$$

where:

$P_{D(TA)}$ = *Power Dissipation allowable at a given operating ambient temperature. This must be greater than the sum of the products of the supply voltages and supply currents at the worst case operating condition.*

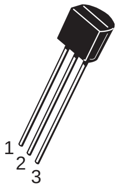
$T_{J(max)}$ = *Maximum operating Junction Temperature as listed in the Maximum Ratings Section. See individual data sheets for $T_{J(max)}$ information.*

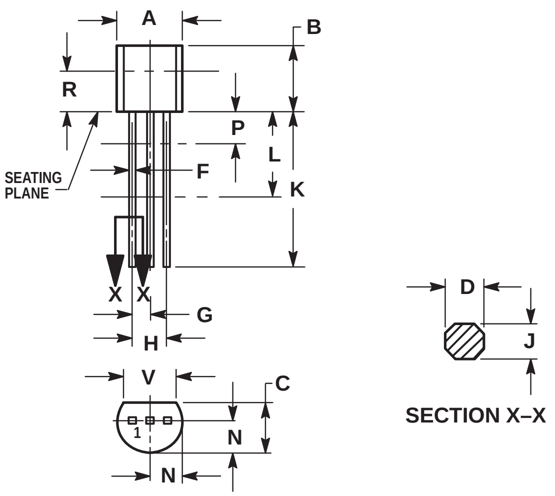
T_A = *Maximum desired operating Ambient Temperature*

$R_{\theta JA(Typ)}$ = *Typical Thermal Resistance Junction-to-Ambient*

Case Outline Dimensions

LP, P, Z SUFFIX
CASE 29-04
Plastic Package
(TO-226AA/TO-92)
ISSUE AD

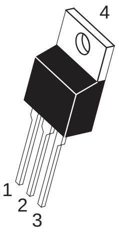


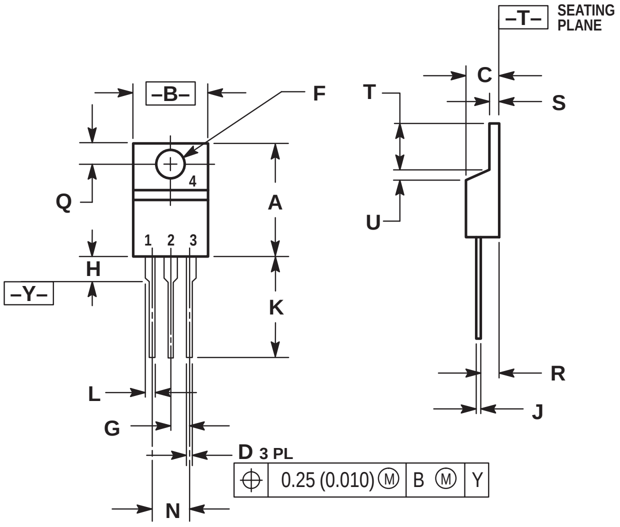


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. CONTOUR OF PACKAGE BEYOND DIMENSION R IS UNCONTROLLED.
4. DIMENSION F APPLIES BETWEEN P AND L. DIMENSION D AND J APPLY BETWEEN L AND K MINIMUM. LEAD DIMENSION IS UNCONTROLLED IN P AND BEYOND DIMENSION K MINIMUM.

	INCHES		MILLIMETERS	
DIM	**MIN**	**MAX**	**MIN**	**MAX**
A	0.175	0.205	4.45	5.20
B	0.170	0.210	4.32	5.33
C	0.125	0.165	3.18	4.19
D	0.016	0.022	0.41	0.55
F	0.016	0.019	0.41	0.48
G	0.045	0.055	1.15	1.39
H	0.095	0.105	2.42	2.66
J	0.015	0.020	0.39	0.50
K	0.500	——	12.70	——
L	0.250	——	6.35	——
N	0.080	0.105	2.04	2.66
P	——	0.100	——	2.54
R	0.115	——	2.93	——
V	0.135	——	3.43	——

KC, T SUFFIX
CASE 221A-06
Plastic Package
ISSUE Y



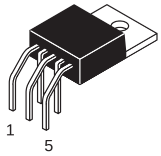


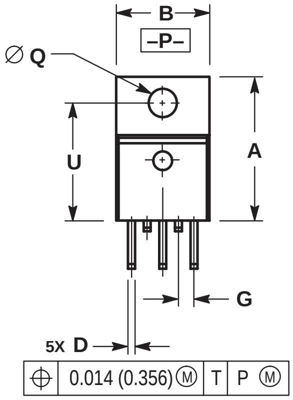
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

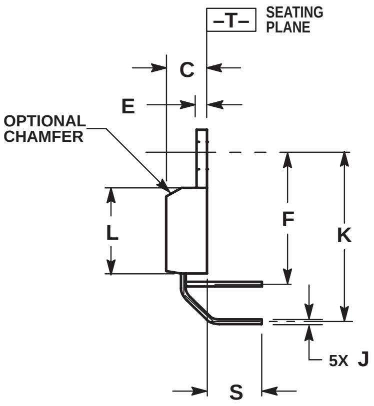
	INCHES		MILLIMETERS	
DIM	**MIN**	**MAX**	**MIN**	**MAX**
A	0.560	0.625	14.23	15.87
B	0.380	0.420	9.66	10.66
C	0.140	0.190	3.56	4.82
D	0.020	0.045	0.51	1.14
F	0.139	0.155	3.53	3.93
G	0.100 BSC		2.54 BSC	
H	——	0.280	——	7.11
J	0.012	0.045	0.31	1.14
K	0.500	0.580	12.70	14.73
L	0.045	0.070	1.15	1.77
N	0.200 BSC		5.08 BSC	
Q	0.100	0.135	2.54	3.42
R	0.080	0.115	2.04	2.92
S	0.020	0.055	0.51	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27

TH SUFFIX
CASE 314A-03

Plastic Package
ISSUE D





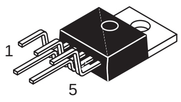


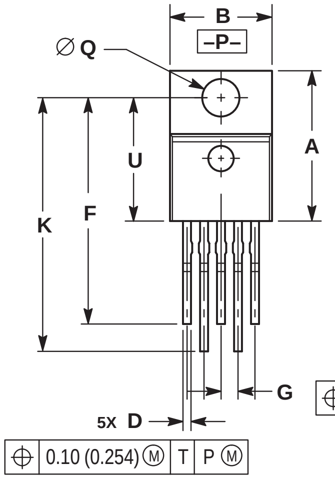
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION D DOES NOT INCLUDE INTERCONNECT BAR (DAMBAR) PROTRUSION. DIMENSION D INCLUDING PROTRUSION SHALL NOT EXCEED 0.043 (1.092) MAXIMUM.

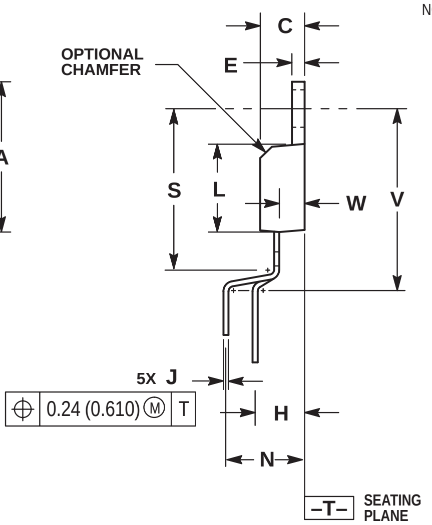
	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.572	0.613	14.529	15.570
B	0.390	0.415	9.906	10.541
C	0.170	0.180	4.318	4.572
D	0.025	0.038	0.635	0.965
E	0.048	0.055	1.219	1.397
F	0.570	0.585	14.478	14.859
G	0.067 BSC		1.702 BSC	
J	0.015	0.025	0.381	0.635
K	0.730	0.745	18.542	18.923
L	0.320	0.365	8.128	9.271
Q	0.140	0.153	3.556	3.886
S	0.210	0.260	5.334	6.604
U	0.468	0.505	11.888	12.827

T, TV SUFFIX
CASE 314B-05

Plastic Package
ISSUE J





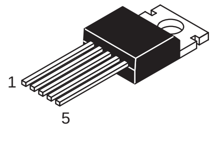


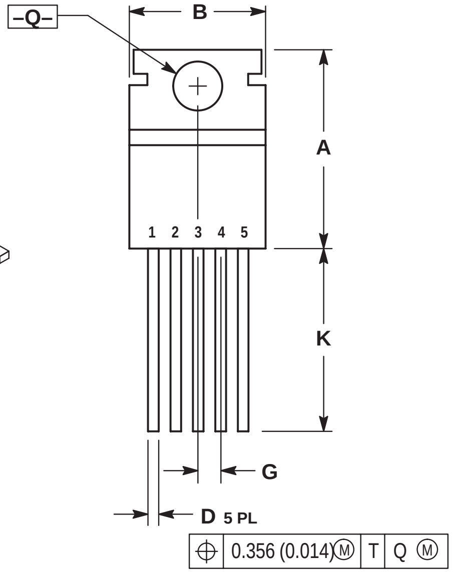
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION D DOES NOT INCLUDE INTERCONNECT BAR (DAMBAR) PROTRUSION. DIMENSION D INCLUDING PROTRUSION SHALL NOT EXCEED 0.043 (1.092) MAXIMUM.

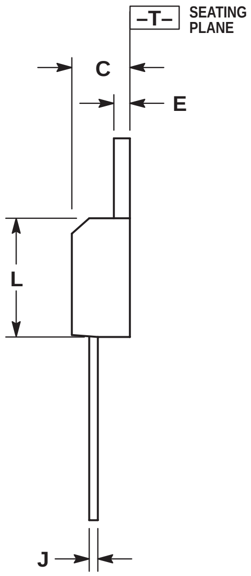
	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.572	0.613	14.529	15.570
B	0.390	0.415	9.906	10.541
C	0.170	0.180	4.318	4.572
D	0.025	0.038	0.635	0.965
E	0.048	0.055	1.219	1.397
F	0.850	0.935	21.590	23.749
G	0.067 BSC		1.702 BSC	
H	0.166 BSC		4.216 BSC	
J	0.015	0.025	0.381	0.635
K	0.900	1.100	22.860	27.940
L	0.320	0.365	8.128	9.271
N	0.320 BSC		8.128 BSC	
Q	0.140	0.153	3.556	3.886
S	—	0.620	—	15.748
U	0.468	0.505	11.888	12.827
V	—	0.735	—	18.669
W	0.090	0.110	2.286	2.794

T SUFFIX
CASE 314C–01

Plastic Package
ISSUE A



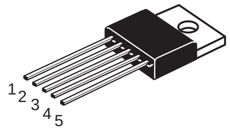


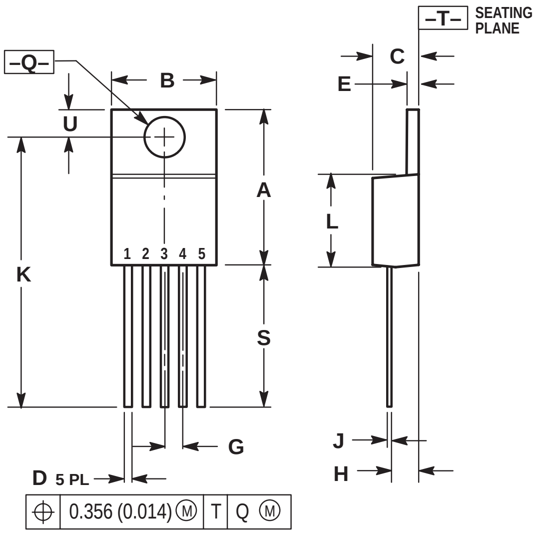


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION D DOES NOT INCLUDE INTERCONNECT BAR (DAMBAR) PROTRUSION. DIMENSION D INCLUDING PROTRUSION SHALL NOT EXCEED 10.92 (0.043) MAXIMUM.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.610	0.625	15.59	15.88
B	0.380	0.420	9.65	10.67
C	0.160	0.190	4.06	4.83
D	0.020	0.040	0.51	1.02
E	0.035	0.055	0.89	1.40
G	0.067 BSC		1.702 BSC	
J	0.015	0.025	0.38	0.64
K	0.500	—	12.70	—
L	0.355	0.370	9.02	9.40
Q	0.139	0.147	3.53	3.73

T, T1 SUFFIX
CASE 314D-03
Plastic Package
ISSUE D

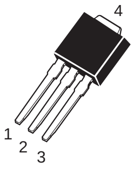


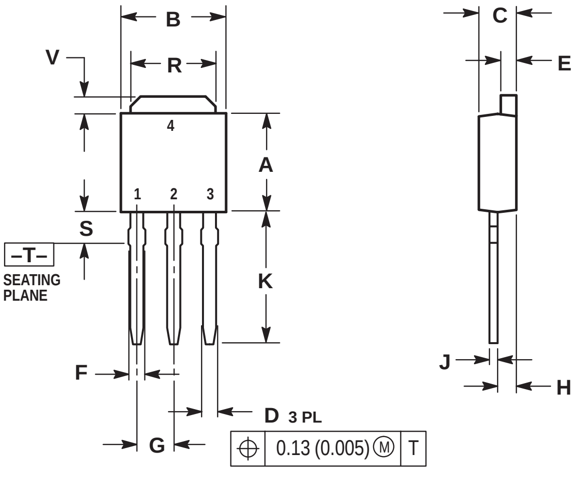


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION D DOES NOT INCLUDE INTERCONNECT BAR (DAMBAR) PROTRUSION. DIMENSION D INCLUDING PROTRUSION SHALL NOT EXCEED 10.92 (0.043) MAXIMUM.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.572	0.613	14.529	15.570
B	0.390	0.415	9.906	10.541
C	0.170	0.180	4.318	4.572
D	0.025	0.038	0.635	0.965
E	0.048	0.055	1.219	1.397
G	0.067 BSC		1.702 BSC	
H	0.087	0.112	2.210	2.845
J	0.015	0.025	0.381	0.635
K	1.020	1.065	25.908	27.051
L	0.320	0.365	8.128	9.271
Q	0.140	0.153	3.556	3.886
U	0.105	0.117	2.667	2.972
S	0.543	0.582	13.792	14.783

DT-1 SUFFIX
CASE 369-07
Plastic Package
(DPAK)
ISSUE K

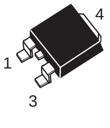


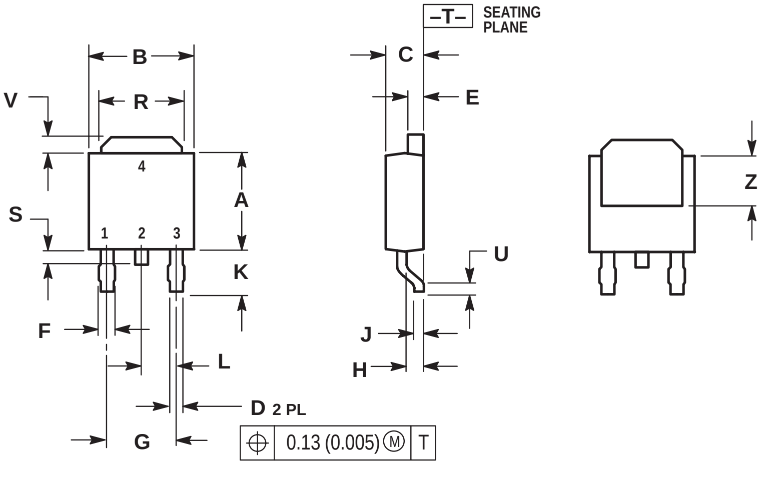


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.235	0.250	5.97	6.35
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.033	0.040	0.84	1.01
F	0.037	0.047	0.94	1.19
G	0.090 BSC		2.29 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.350	0.380	8.89	9.65
R	0.175	0.215	4.45	5.46
S	0.050	0.090	1.27	2.28
V	0.030	0.050	0.77	1.27

DT SUFFIX
CASE 369A-13
Plastic Package
(DPAK)
ISSUE Y



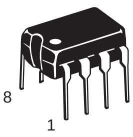


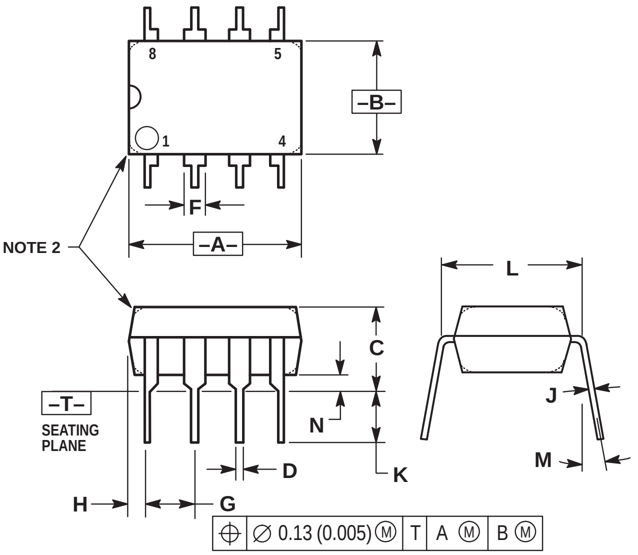
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.235	0.250	5.97	6.35
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.033	0.040	0.84	1.01
F	0.037	0.047	0.94	1.19
G	0.180 BSC		4.58 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.102	0.114	2.60	2.89
L	0.090 BSC		2.29 BSC	
R	0.175	0.215	4.45	5.46
S	0.020	0.050	0.51	1.27
U	0.020	——	0.51	——
V	0.030	0.050	0.77	1.27
Z	0.138	——	3.51	——

DP1, N, P, P1 SUFFIX
CASE 626-05

Plastic Package
ISSUE K



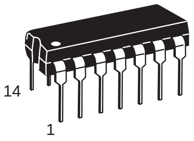


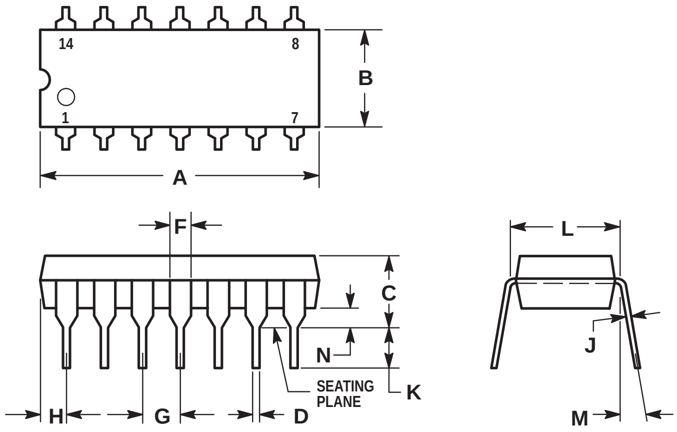
NOTES:
1. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
2. PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CORNERS).
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.40	10.16	0.370	0.400
B	6.10	6.60	0.240	0.260
C	3.94	4.45	0.155	0.175
D	0.38	0.51	0.015	0.020
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	0.76	1.27	0.030	0.050
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	—	10°	—	10°
N	0.76	1.01	0.030	0.040

N, P, N-14, P2 SUFFIX
CASE 646-06

Plastic Package
ISSUE L



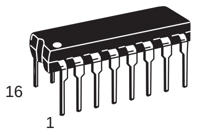


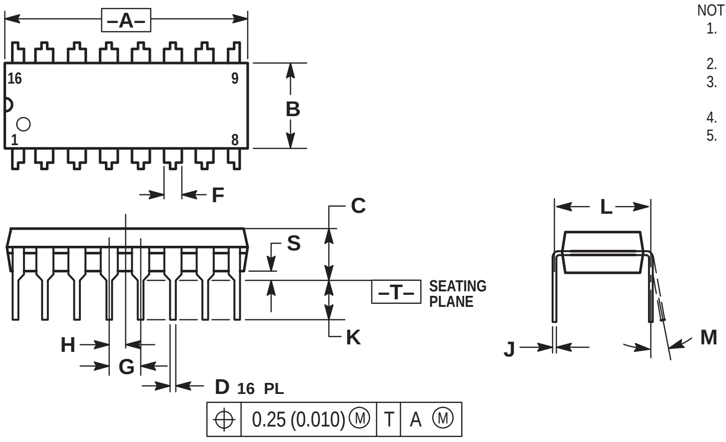
NOTES:
1. LEADS WITHIN 0.13 (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
4. ROUNDED CORNERS OPTIONAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.715	0.770	18.16	19.56
B	0.240	0.260	6.10	6.60
C	0.145	0.185	3.69	4.69
D	0.015	0.021	0.38	0.53
F	0.040	0.070	1.02	1.78
G	0.100 BSC		2.54 BSC	
H	0.052	0.095	1.32	2.41
J	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.300 BSC		7.62 BSC	
M	0°	10°	0°	10°
N	0.015	0.039	0.39	1.01

DP2, N, P, PC SUFFIX
CASE 648-08

Plastic Package
ISSUE R

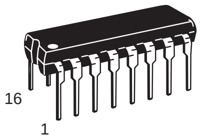


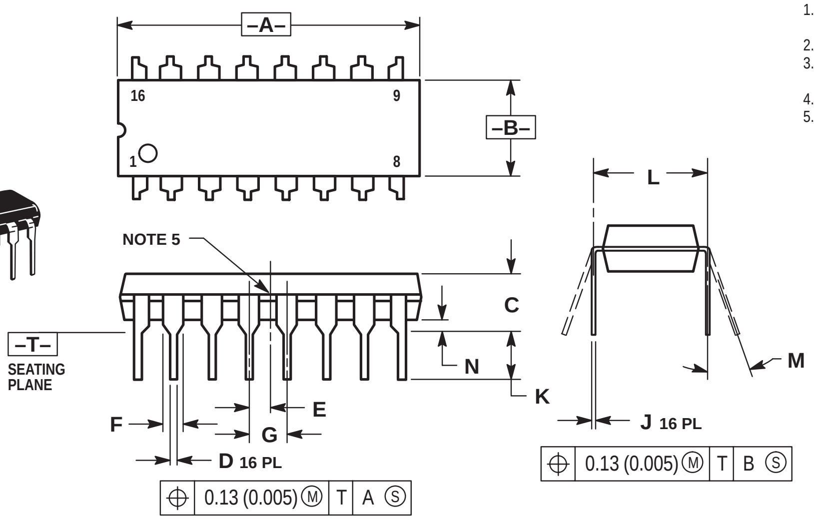


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

B, P, P2, V SUFFIX
CASE 648C-03
Plastic Package
(DIP–16)
ISSUE C

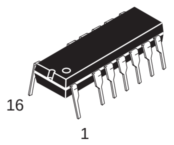


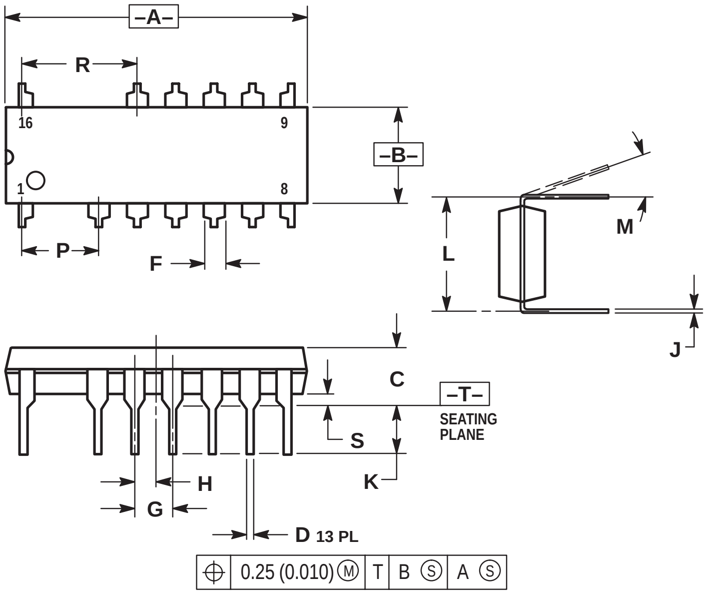


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. INTERNAL LEAD CONNECTION BETWEEN 4 AND 5, 12 AND 13.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.740	0.840	18.80	21.34
B	0.240	0.260	6.10	6.60
C	0.145	0.185	3.69	4.69
D	0.015	0.021	0.38	0.53
E	0.050 BSC		1.27 BSC	
F	0.040	0.70	1.02	1.78
G	0.100 BSC		2.54 BSC	
J	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.300 BSC		7.62 BSC	
M	0°	10°	0°	10°
N	0.015	0.040	0.39	1.01

P SUFFIX
CASE 648E–01
Plastic Package
(DIP–16)
ISSUE O

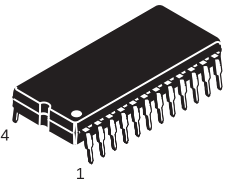


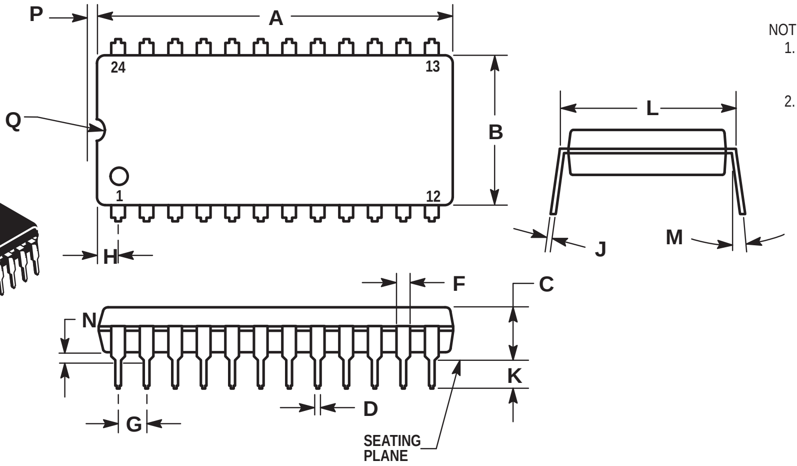


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION A AND B DOES NOT INCLUDE MOLD PROTRUSION.
5. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.25 (0.010).
6. ROUNDED CORNER OPTIONAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.740	0.760	18.80	19.30
B	0.245	0.260	6.23	6.60
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.050	0.070	1.27	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.120	0.140	3.05	3.55
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
P	0.200 BSC		5.08 BSC	
R	0.300 BSC		7.62 BSC	
S	0.015	0.035	0.39	0.88

P SUFFIX
CASE 649-03
Plastic Package
ISSUE D

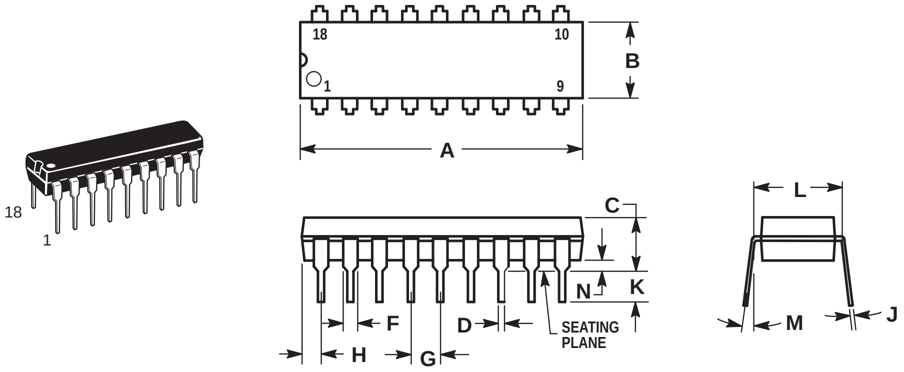




NOTES:
1. LEADS WITHIN 0.13 (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	31.50	32.13	1.240	1.265
B	13.21	13.72	0.520	0.540
C	4.70	5.21	0.185	0.205
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	14.99	15.49	0.590	0.610
M	—	10	—	10°
N	0.51	1.02	0.020	0.040
P	0.13	0.38	0.005	0.015
Q	0.51	0.76	0.020	0.030

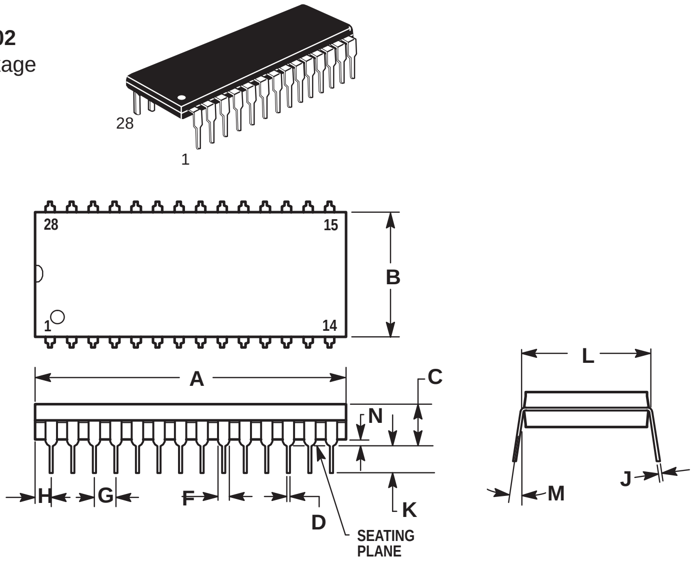
A, B, N, P SUFFIX
CASE 707-02
Plastic Package
ISSUE C



NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	22.22	23.24	0.875	0.915
B	6.10	6.60	0.240	0.260
C	3.56	4.57	0.140	0.180
D	0.36	0.56	0.014	0.022
F	1.27	1.78	0.050	0.070
G	2.54 BSC		0.100 BSC	
H	1.02	1.52	0.040	0.060
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

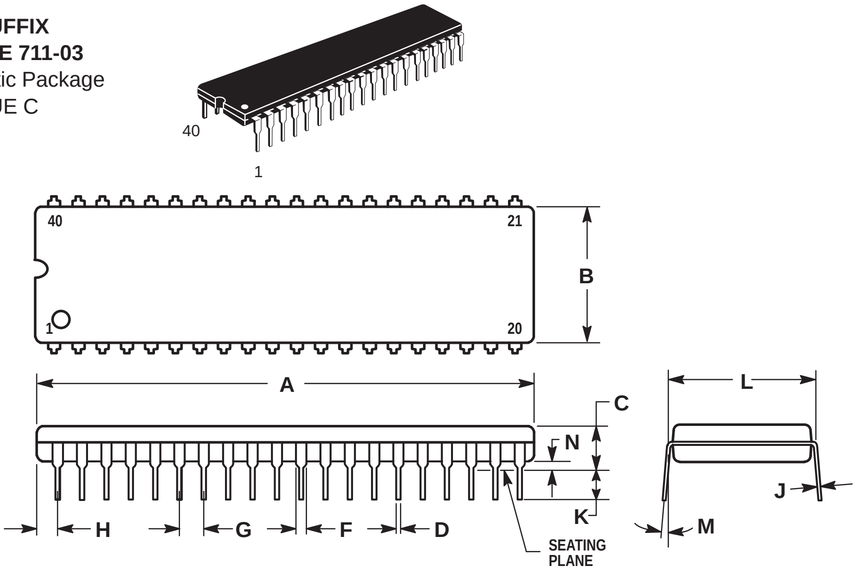
P SUFFIX
CASE 710-02
Plastic Package
ISSUE B



NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	36.45	37.21	1.435	1.465
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

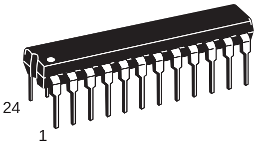
P SUFFIX
CASE 711-03
Plastic Package
ISSUE C

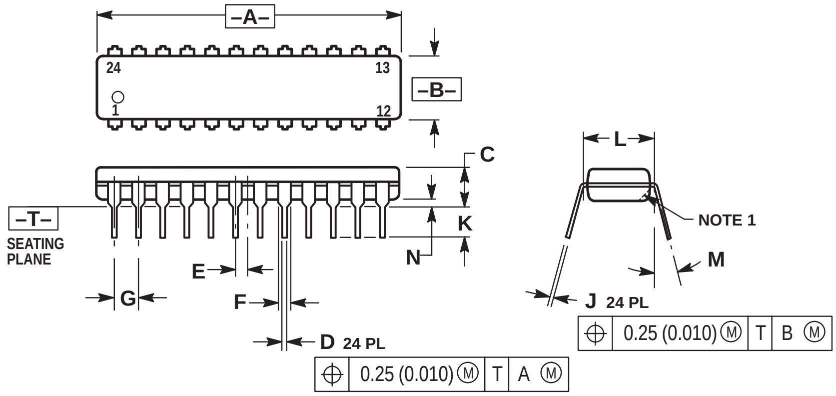


NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	51.69	52.45	2.035	2.065
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

F, P, P-3 SUFFIX
CASE 724-03
Plastic Package
(NDIP–24)
ISSUE D

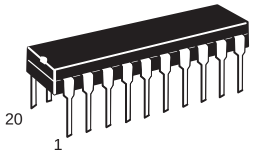


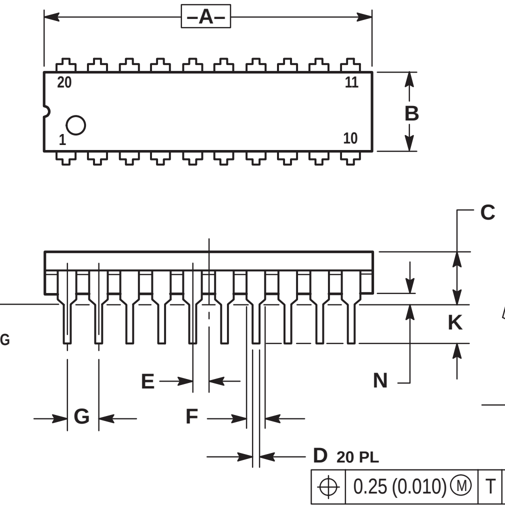


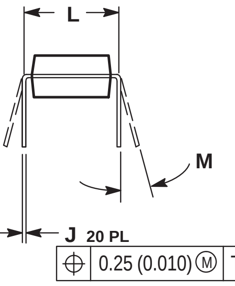
NOTES:
1. CHAMFERED CONTOUR OPTIONAL.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
4. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.230	1.265	31.25	32.13
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.020	0.38	0.51
E	0.050 BSC		1.27 BSC	
F	0.040	0.060	1.02	1.52
G	0.100 BSC		2.54 BSC	
J	0.007	0.012	0.18	0.30
K	0.110	0.140	2.80	3.55
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

H, P, DP SUFFIX
CASE 738-03
Plastic Package
ISSUE E



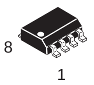


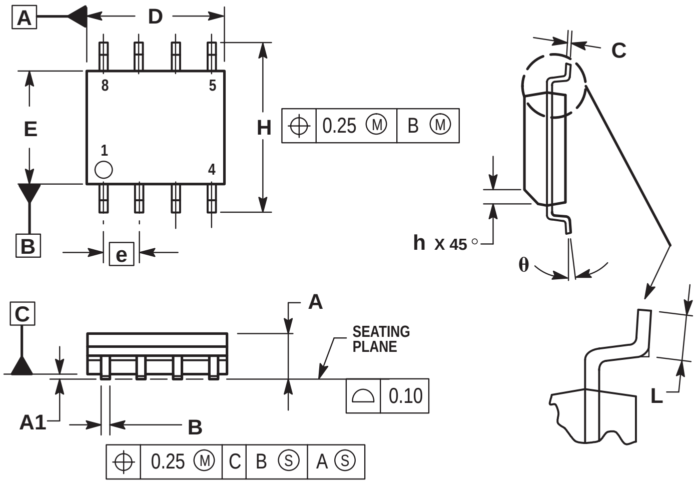


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.010	1.070	25.66	27.17
B	0.240	0.260	6.10	6.60
C	0.150	0.180	3.81	4.57
D	0.015	0.022	0.39	0.55
E	0.050 BSC		1.27 BSC	
F	0.050	0.070	1.27	1.77
G	0.100 BSC		2.54 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.140	2.80	3.55
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

D, D1, D2 SUFFIX
CASE 751-05
Plastic Package
(SO-8, SOP-8)
ISSUE R

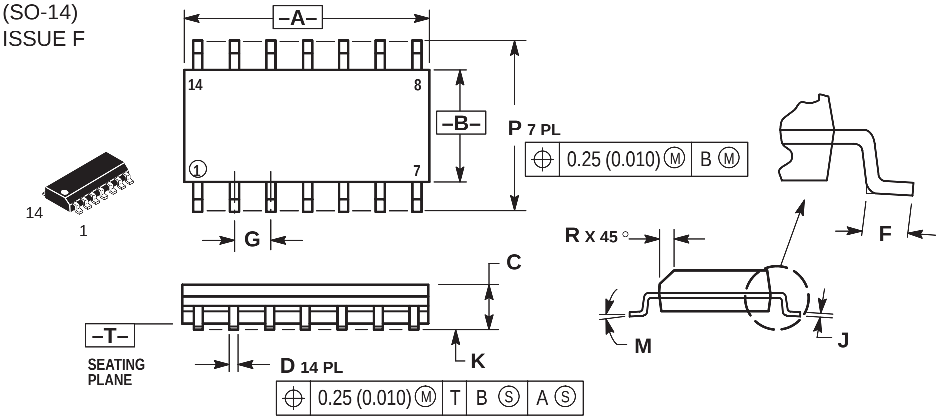




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS ARE IN MILLIMETERS.
3. DIMENSION D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS	
DIM	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
B	0.35	0.49
C	0.18	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.25
θ	0°	7°

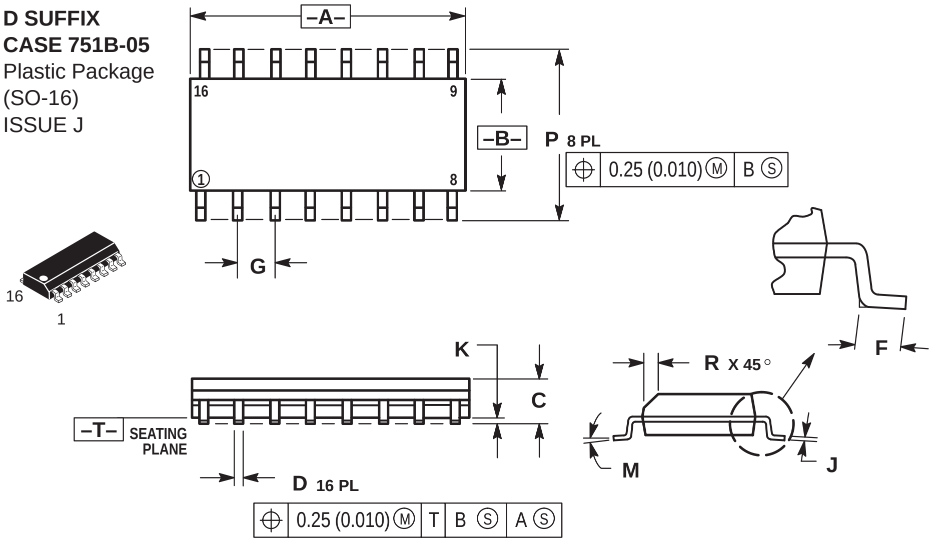
D SUFFIX
CASE 751A-03
Plastic Package
(SO-14)
ISSUE F



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

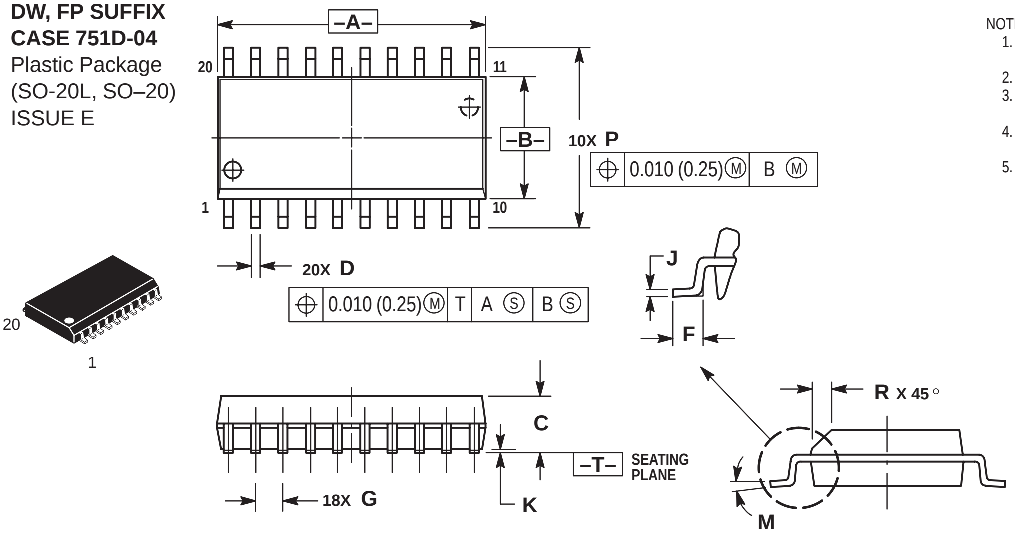
D SUFFIX
CASE 751B-05
Plastic Package
(SO-16)
ISSUE J



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

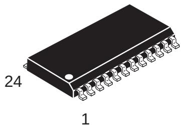
DW, FP SUFFIX
CASE 751D-04
Plastic Package
(SO-20L, SO–20)
ISSUE E

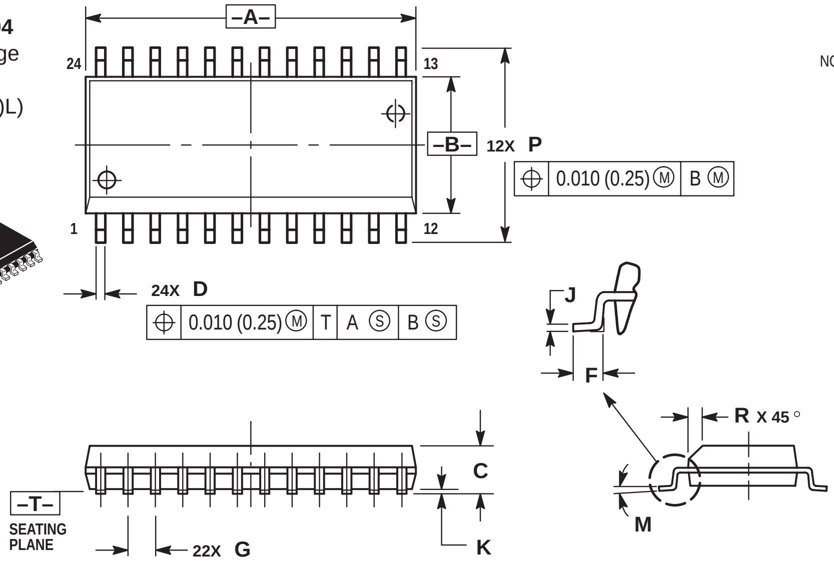


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.150 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	12.65	12.95	0.499	0.510
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

DW SUFFIX
CASE 751E-04
Plastic Package
(SO-24L,
SOP (16+4+4)L)
ISSUE E

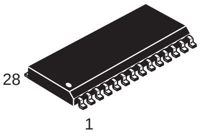


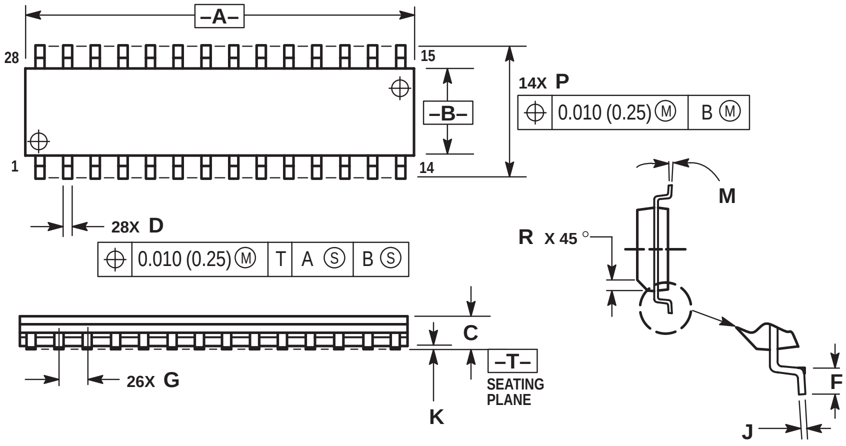


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	15.25	15.54	0.601	0.612
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.41	0.90	0.016	0.035
G	1.27 BSC		0.050 BSC	
J	0.23	0.32	0.009	0.013
K	0.13	0.29	0.005	0.011
M	0°	8°	0°	8°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

DW SUFFIX
CASE 751F-04
Plastic Package
(SO-28L, SOIC–28)
ISSUE E

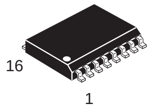


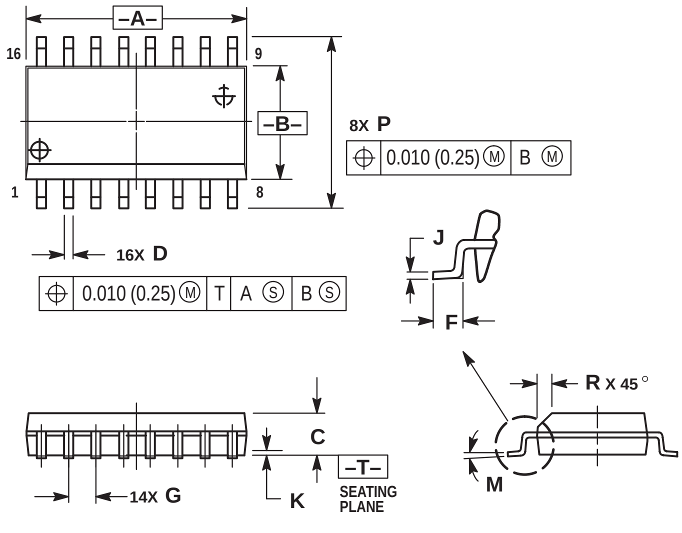


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	17.80	18.05	0.701	0.711
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.41	0.90	0.016	0.035
G	1.27 BSC		0.050 BSC	
J	0.23	0.32	0.009	0.013
K	0.13	0.29	0.005	0.011
M	0°	8°	0°	8°
P	10.01	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

DW SUFFIX
CASE 751G-02
Plastic Package
(SO-16L, SOP–16L,
SOP-8+8L)
ISSUE A

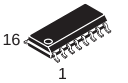


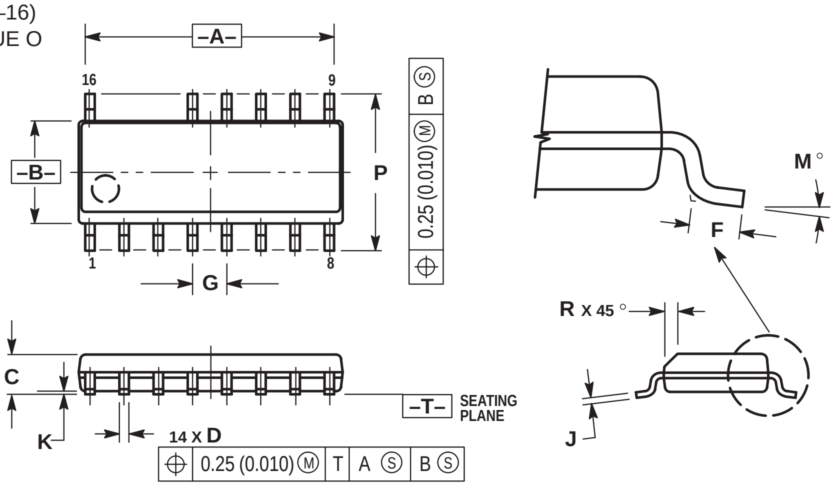


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	10.15	10.45	0.400	0.411
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

D SUFFIX
CASE 751K–01
Plastic Package
(SO–16)
ISSUE O

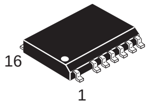


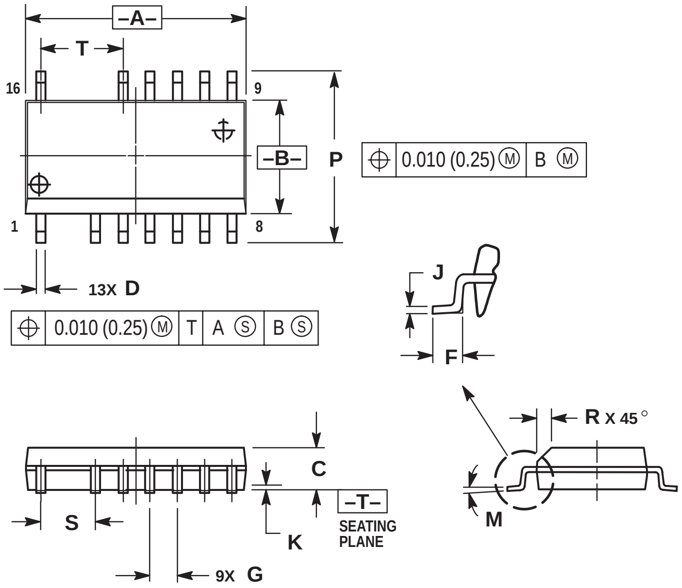


NOTES:
1 DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2 CONTROLLING DIMENSION: MILLIMETER.
3 DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4 MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5 DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	**MIN**	**MAX**	**MIN**	**MAX**
A	9.80	10.00	0.368	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

DW SUFFIX
CASE 751N–01
Plastic Package
(SOP–16L)
ISSUE O

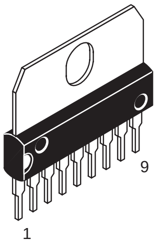


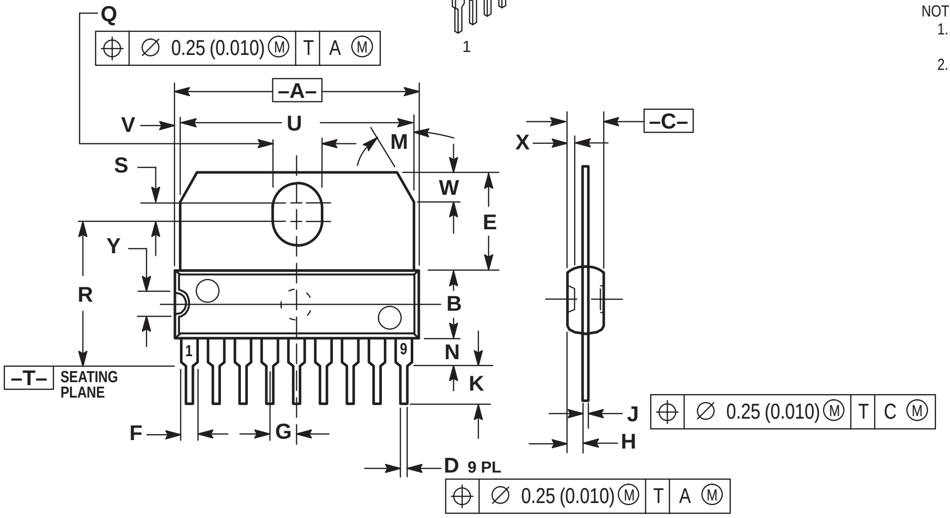


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	**MIN**	**MAX**	**MIN**	**MAX**
A	10.15	10.45	0.400	0.411
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029
S	2.54 BSC		0.100 BSC	
T	3.81 BSC		0.150 BSC	

CASE 762-01
Plastic Medium Power Package
(SIP-9)
ISSUE C

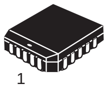


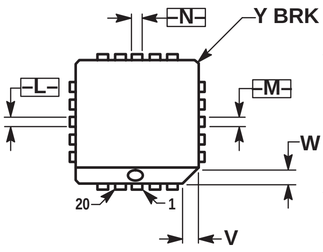


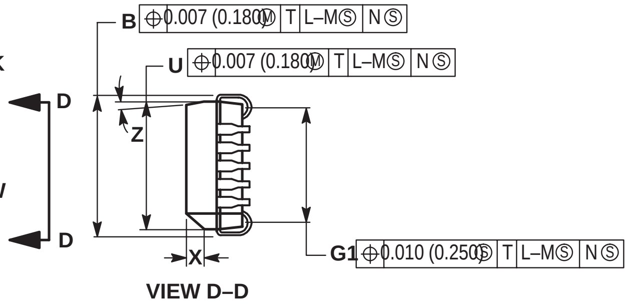
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	22.40	23.00	0.873	0.897
B	6.40	6.60	0.252	0.260
C	3.45	3.65	0.135	1.143
D	0.40	0.55	0.015	0.021
E	9.35	9.60	0.368	0.377
F	1.40	1.60	0.055	0.062
G	2.54 BSC		0.100 BSC	
H	1.51	1.71	0.059	0.067
J	0.360	0.400	0.014	0.015
K	3.95	4.20	0.155	0.165
M	30° BSC		30° BSC	
N	2.50	2.70	0.099	0.106
Q	3.15	3.45	0.124	0.135
R	13.60	13.90	0.535	0.547
S	1.65	1.95	0.064	0.076
U	22.00	22.20	0.866	0.874
V	0.55	0.75	0.021	0.029
W	2.89 BSC		0.113 BSC	
X	0.65	0.75	0.025	0.029
Y	2.70	2.80	0.106	0.110

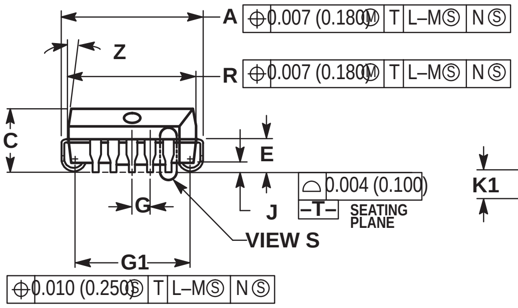
FN SUFFIX
CASE 775-02
Plastic Package
(PLCC-20)
ISSUE C

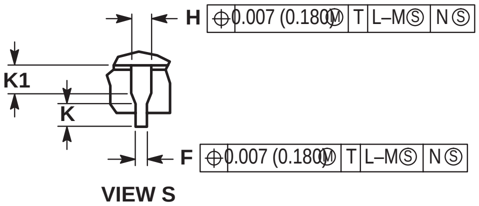






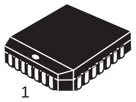
NOTES:
1. DATUMS –L–, –M–, AND –N– DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
2. DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM –T–, SEATING PLANE.
3. DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.
6. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
7. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

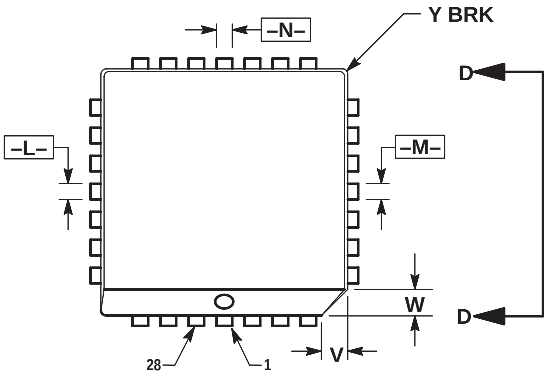


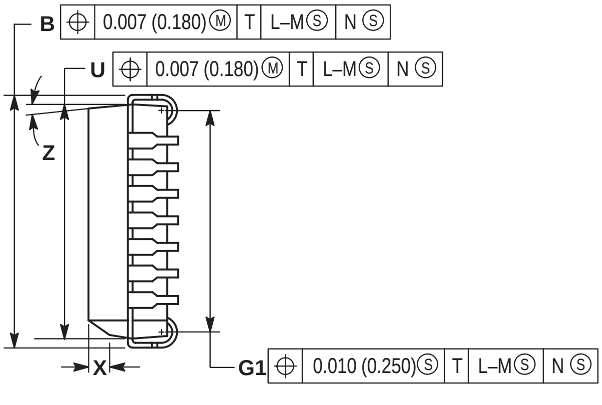


	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.385	0.395	9.78	10.03
B	0.385	0.395	9.78	10.03
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	—	0.51	—
K	0.025	—	0.64	—
R	0.350	0.356	8.89	9.04
U	0.350	0.356	8.89	9.04
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	—	0.020	—	0.50
Z	2°	10°	2°	10°
G1	0.310	0.330	7.88	8.38
K1	0.040	—	1.02	—

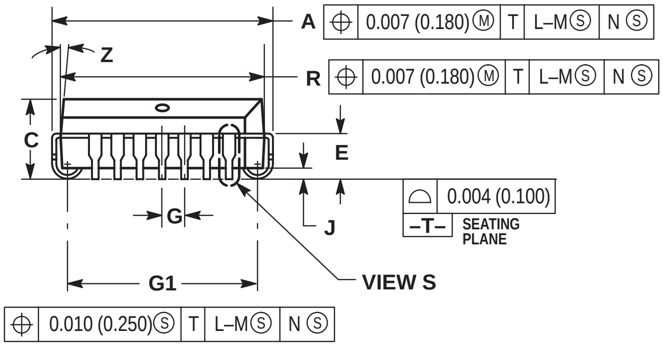
FN SUFFIX
CASE 776-02
Plastic Package
(PLCC–28)
ISSUE D

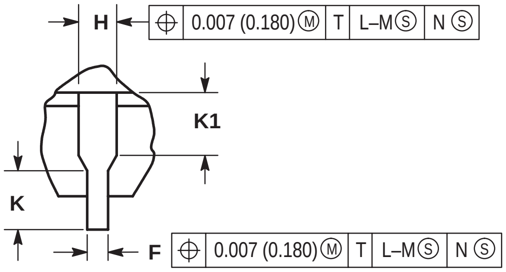






VIEW D–D



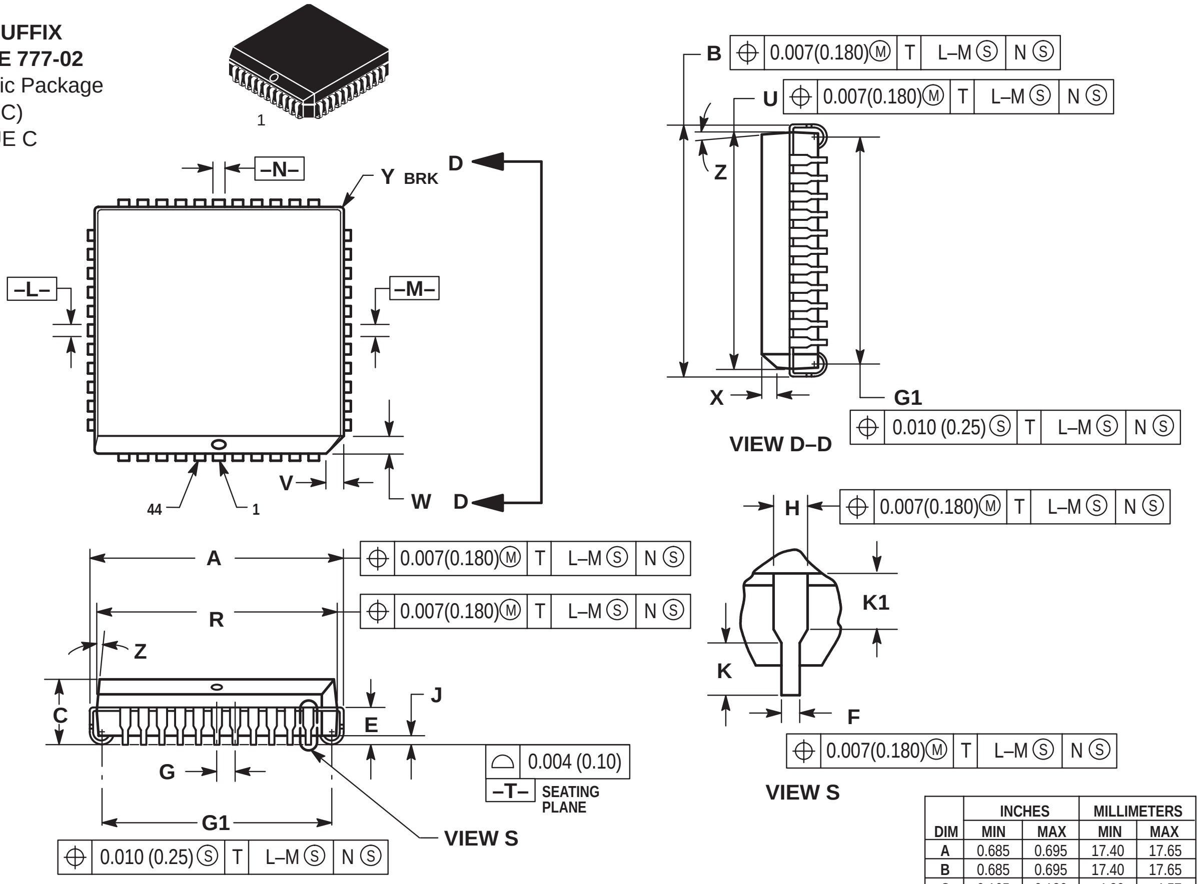


VIEW S

NOTES:
1. DATUMS –L–, –M–, AND –N– DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
2. DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM –T–, SEATING PLANE.
3. DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.
6. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
7. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.485	0.495	12.32	12.57
B	0.485	0.495	12.32	12.57
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	—	0.51	—
K	0.025	—	0.64	—
R	0.450	0.456	11.43	11.58
U	0.450	0.456	11.43	11.58
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	—	0.020	—	0.50
Z	2°	10°	2°	10°
G1	0.410	0.430	10.42	10.92
K1	0.040	—	1.02	—

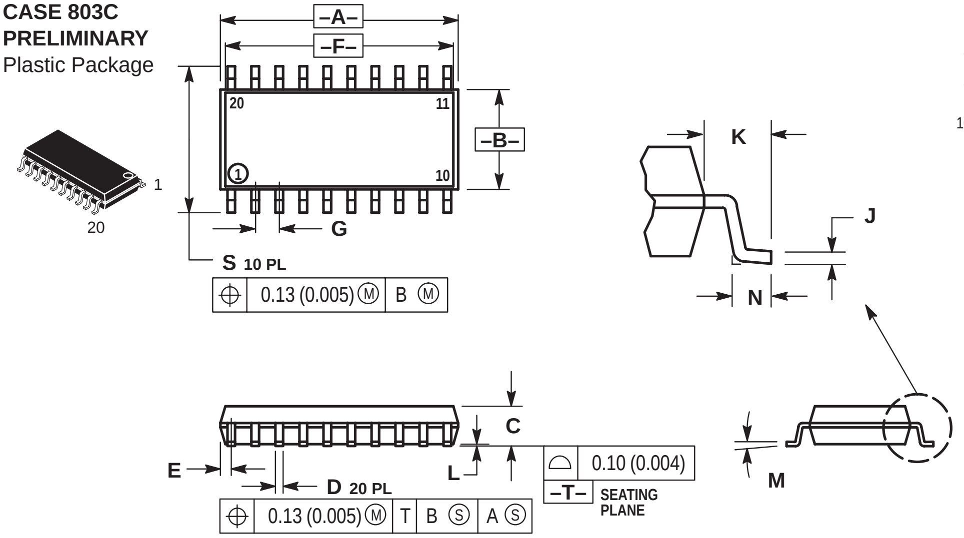
FN SUFFIX
CASE 777-02
Plastic Package
(PLCC)
ISSUE C



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.685	0.695	17.40	17.65
B	0.685	0.695	17.40	17.65
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	——	0.51	——
K	0.025	——	0.64	——
R	0.650	0.656	16.51	16.66
U	0.650	0.656	16.51	16.66
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	——	0.020	——	0.50
Z	2 °	10 °	2 °	10 °
G1	0.610	0.630	15.50	16.00
K1	0.040	——	1.02	——

NOTES:
1. DATUMS –L–, –M–, AND –N– ARE DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
2. DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM –T–, SEATING PLANE.
3. DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.25) PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.
6. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
7. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

M SUFFIX
CASE 803C
PRELIMINARY
Plastic Package



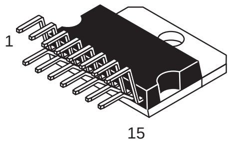
NOTES:
6. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
7. CONTROLLING DIMENSION: MILLIMETER.
8. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
9. MAXIMUM MOLD PROTRUSION 0.15 (0.008) PER SIDE.
10. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.006) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	12.35	12.80	0.486	0.504
B	5.10	5.45	0.201	0.215
C	1.95	2.05	0.077	0.081
D	0.35	0.50	0.014	0.020
E	——	0.81	——	0.032
F	12.40*		0.488*	
G	1.15	1.39	0.045	0.055
H	0.59	0.81	0.023	0.032
J	0.18	0.27	0.007	0.011
K	1.10	1.50	0.043	0.059
L	0.05	0.20	0.001	0.008
M	0 °	10 °	0 °	10 °
N	0.50	0.85	0.020	0.033
S	7.40	8.20	0.291	0.323

*APPROXIMATE

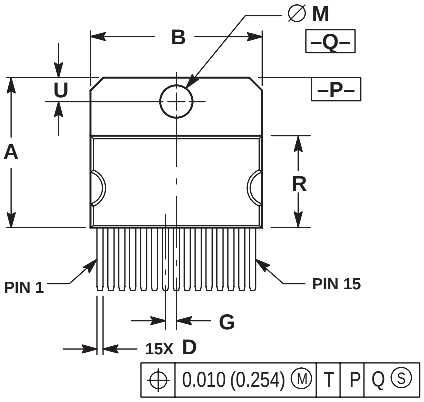
TV SUFFIX
CASE 821C-04

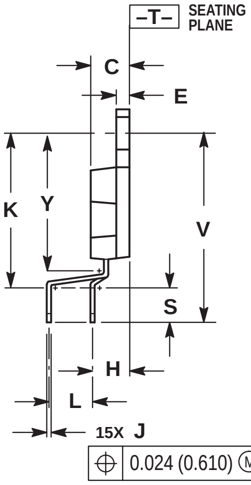
Plastic Package
(15-Pin ZIP)
ISSUE D



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION R DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
5. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.010 (0.250).
6. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.003 (0.076) TOTAL IN EXCESS OF THE D DIMENSION. AT MAXIMUM MATERIAL CONDITION.

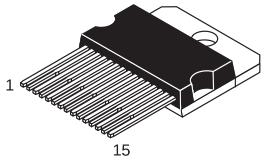




DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.684	0.694	17.374	17.627
B	0.784	0.792	19.914	20.116
C	0.173	0.181	4.395	4.597
D	0.024	0.031	0.610	0.787
E	0.058	0.062	1.473	1.574
G	0.050 BSC		1.270 BSC	
H	0.169 BSC		4.293 BSC	
J	0.018	0.024	0.458	0.609
K	0.700	0.710	17.780	18.034
L	0.200 BSC		5.080 BSC	
M	0.148	0.151	3.760	3.835
R	0.416	0.426	10.567	10.820
S	0.157	0.167	3.988	4.242
U	0.105	0.115	2.667	2.921
V	0.868 REF		22.047 REF	
Y	0.625	0.639	15.875	16.231

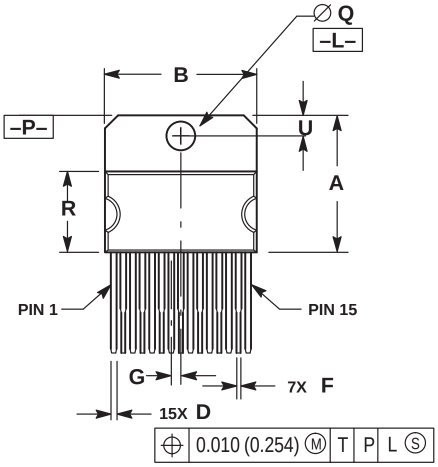
T SUFFIX
CASE 821D-03

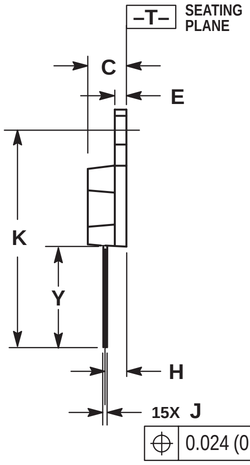
Plastic Package
ISSUE C



NOTES:

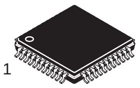
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION R DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
5. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.010 (0.250).
6. DELETED
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.003 (0.076) TOTAL IN EXCESS OF THE D DIMENSION. AT MAXIMUM MATERIAL CONDITION.

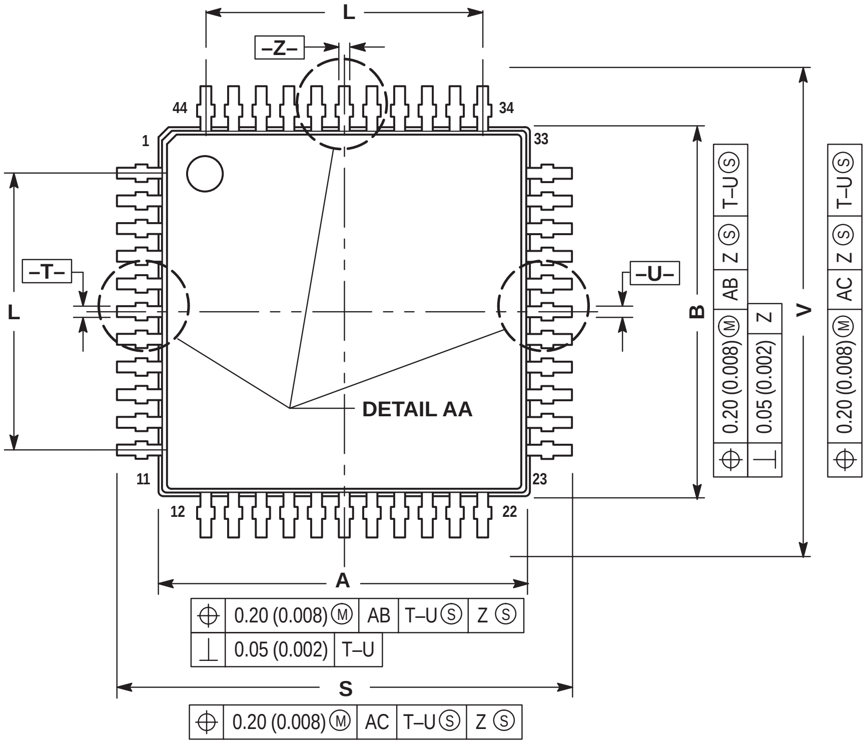


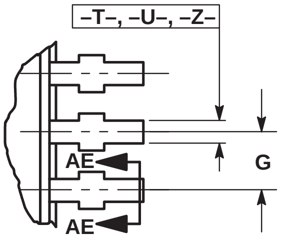


DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.681	0.694	17.298	17.627
B	0.784	0.792	19.914	20.116
C	0.173	0.181	4.395	4.597
D	0.024	0.031	0.610	0.787
E	0.058	0.062	1.473	1.574
F	0.016	0.023	0.407	0.584
G	0.050 BSC		1.270 BSC	
H	0.110 BSC		2.794 BSC	
J	0.018	0.024	0.458	0.609
K	1.078	1.086	27.382	27.584
Q	0.148	0.151	3.760	3.835
R	0.416	0.426	10.567	10.820
U	0.110 BSC		2.794 BSC	
Y	0.503 REF		12.776 REF	

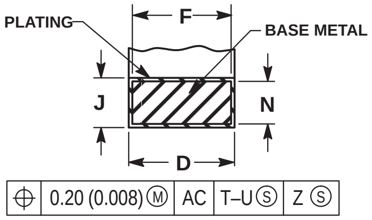
FTB SUFFIX
CASE 824D–01
Plastic Package
(TQFP–44)
ISSUE O





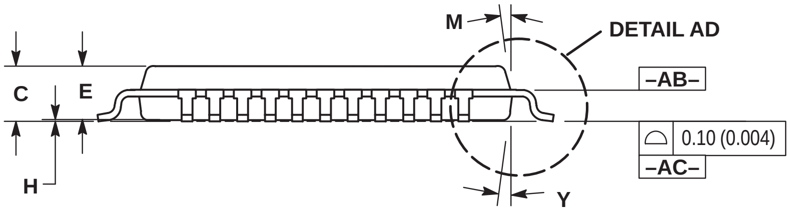


DETAIL AA

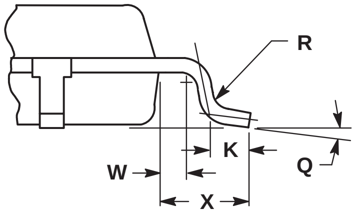


SECTION AE–AE

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE –AB– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS –T–, –U– AND –Z– TO BE DETERMINED AT DATUM PLANE –AB–.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE –AC–.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –AB–.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.530 (0.021).

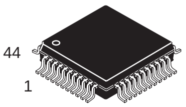


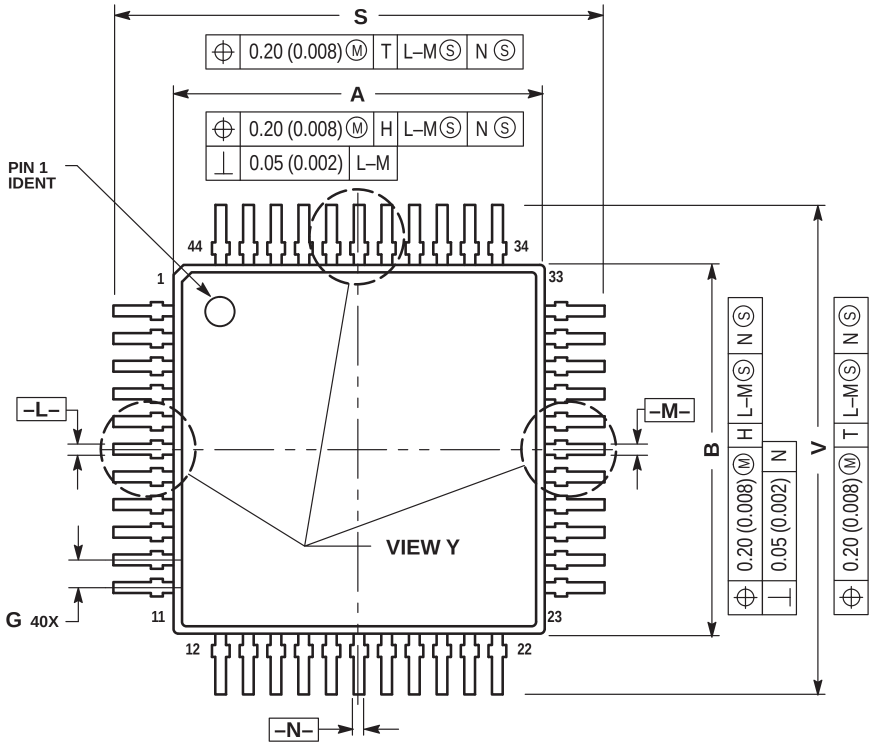
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.950	10.050	0.392	0.396
B	9.950	10.050	0.392	0.396
C	1.400	1.600	0.055	0.063
D	0.300	0.450	0.012	0.018
E	1.350	1.450	0.053	0.057
F	0.300	0.400	0.012	0.016
G	0.800 BSC		0.031 BSC	
H	0.050	0.150	0.002	0.006
J	0.090	0.200	0.004	0.008
K	0.450	0.550	0.018	0.022
L	8.000 BSC		0.315 BSC	
M	12° REF		12° REF	
N	0.090	0.160	0.004	0.006
Q	1°	5°	1°	5°
R	0.100	0.200	0.004	0.008
S	11.900	12.100	0.469	0.476
V	11.900	12.100	0.469	0.476
W	0.200 REF		0.008 REF	
X	1.000 REF		0.039 REF	
Y	12° REF		12° REF	

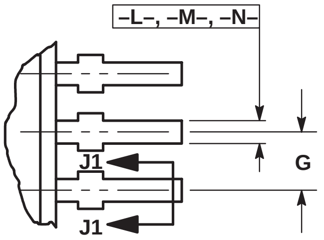


VIEW AD

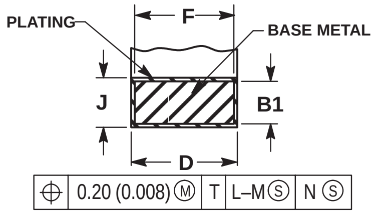
FB SUFFIX
CASE 824E–02
Plastic Package
(QFP)
ISSUE A



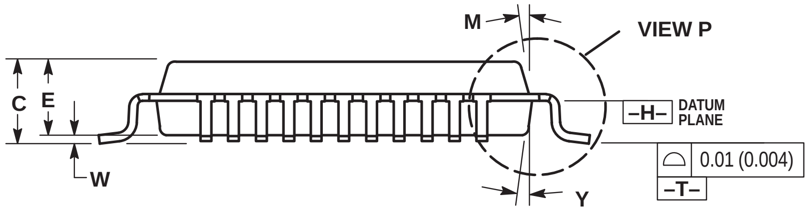


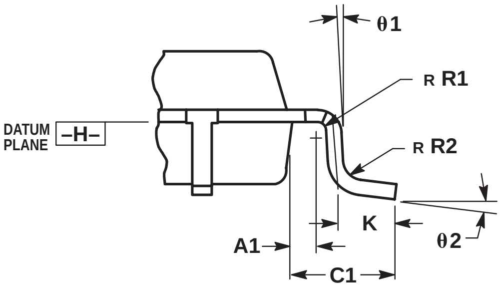


VIEW Y
3 PL



SECTION J1–J1
44 PL



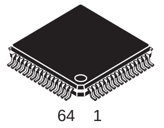


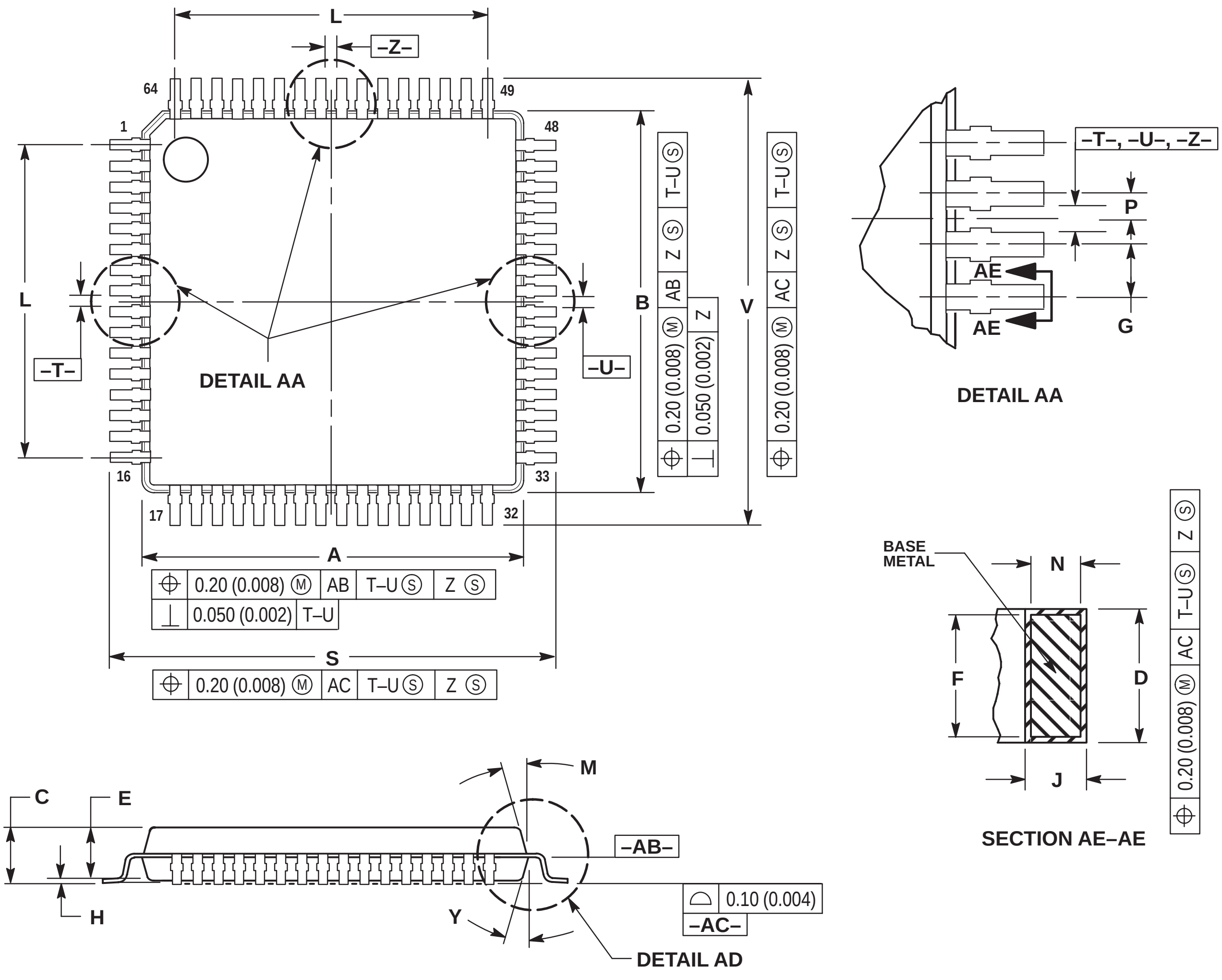
VIEW P

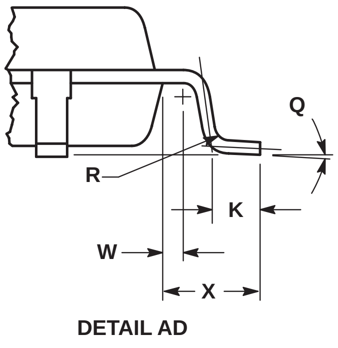
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE –H– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS –L–, –M– AND –N– TO BE DETERMINED AT DATUM PLANE –H–.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE –T–.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –H–.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.530 (0.021).

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.90	10.10	0.390	0.398
B	9.90	10.10	0.390	0.398
C	2.00	2.21	0.079	0.087
D	0.30	0.45	0.0118	0.0177
E	2.00	2.10	0.079	0.083
F	0.30	0.40	0.012	0.016
G	0.80 BSC		0.031 BSC	
J	0.13	0.23	0.005	0.009
K	0.65	0.95	0.026	0.037
M	5°	10°	5°	10°
S	12.95	13.45	0.510	0.530
V	12.95	13.45	0.510	0.530
W	0.000	0.210	0.000	0.008
Y	5°	10°	5°	10°
A1	0.450 REF		0.018 REF	
B1	0.130	0.170	0.005	0.007
C1	1.600 REF		0.063 REF	
R1	0.130	0.300	0.005	0.012
R2	0.130	0.300	0.005	0.012
θ1	5°	10°	5°	10°
θ2	0°	7°	0°	7°

FB SUFFIX
CASE 840F–01
Plastic Package
ISSUE O





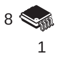


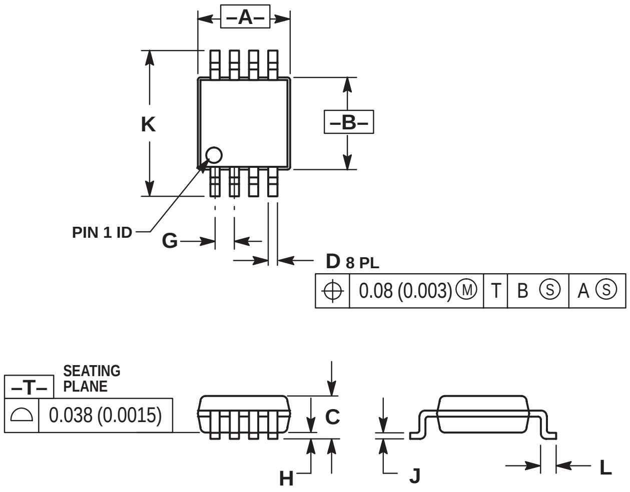
DETAIL AD

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE –AB– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS –T–, –U– AND –Z– TO BE DETERMINED AT DATUM PLANE –AC–.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE –AC–.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –AB–.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.350 (0.014).

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.950	10.050	0.392	0.396
B	9.950	10.050	0.392	0.396
C	1.400	1.600	0.055	0.063
D	0.170	0.270	0.007	0.011
E	1.350	1.450	0.053	0.057
F	0.170	0.230	0.007	0.009
G	0.500 BSC		0.020 BSC	
H	0.050	0.150	0.002	0.006
J	0.090	0.200	0.004	0.008
K	0.450	0.550	0.018	0.022
L	7.500 BSC		0.295 BSC	
M	12° REF		12° REF	
N	0.090	0.160	0.004	0.006
P	0.250 BSC		0.010 BSC	
Q	1°	5°	1°	5°
R	0.100	0.200	0.004	0.008
S	11.900	12.100	0.469	0.476
V	11.900	12.100	0.469	0.476
W	0.200 REF		0.008 REF	
X	1.000 REF		0.039 REF	
Y	12° REF		12° REF	

DM SUFFIX
CASE 846A–02
Plastic Package
(Micro–8)
ISSUE C



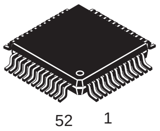


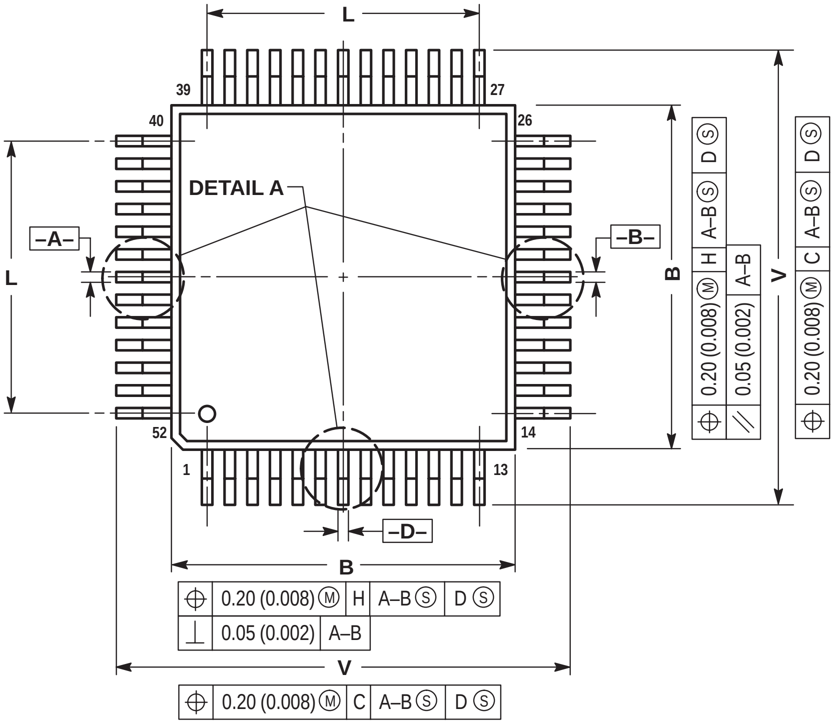
NOTES:

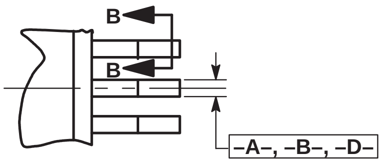
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	2.90	3.10	0.114	0.122
B	2.90	3.10	0.114	0.122
C	—	1.10	—	0.043
D	0.25	0.40	0.010	0.016
G	0.65 BSC		0.026 BSC	
H	0.05	0.15	0.002	0.006
J	0.13	0.23	0.005	0.009
K	4.75	5.05	0.187	0.199
L	0.40	0.70	0.016	0.028

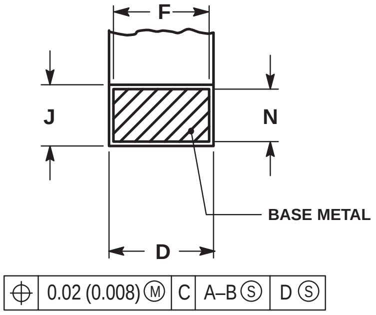
FB SUFFIX
CASE 848B-04
Plastic Package
(TQFP–52)
ISSUE C



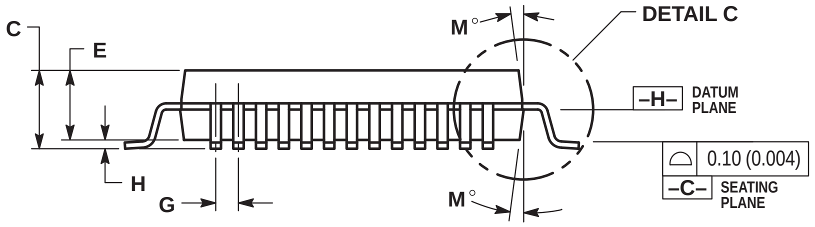


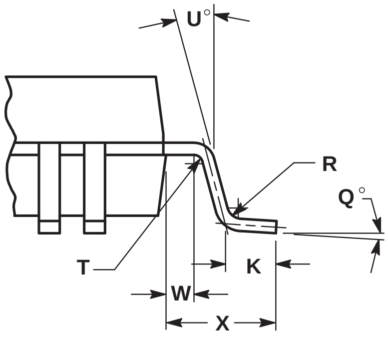


DETAIL A



SECTION B–B





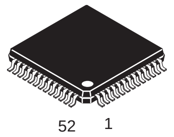
DETAIL C

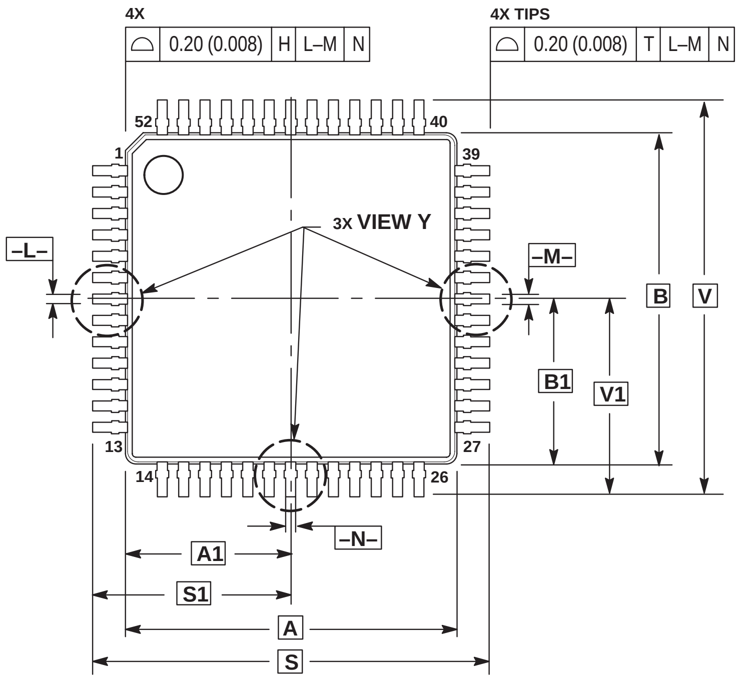
NOTES:

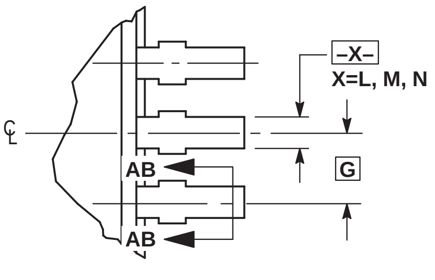
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE –H– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS –A–, –B– AND –D– TO BE DETERMINED AT DATUM PLANE –H–.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE –C–.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –H–.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.90	10.10	0.390	0.398
B	9.90	10.10	0.390	0.398
C	2.10	2.45	0.083	0.096
D	0.22	0.38	0.009	0.015
E	2.00	2.10	0.079	0.083
F	0.22	0.33	0.009	0.013
G	0.65 BSC		0.026 BSC	
H	—	0.25	—	0.010
J	0.13	0.23	0.005	0.009
K	0.65	0.95	0.026	0.037
L	7.80 REF		0.307 REF	
M	5°	10°	5°	10°
N	0.13	0.17	0.005	0.007
Q	0°	7°	0°	7°
R	0.13	0.30	0.005	0.012
S	12.95	13.45	0.510	0.530
T	0.13	—	0.005	—
U	0°	—	0°	—
V	12.95	13.45	0.510	0.530
W	0.35	0.45	0.014	0.018
X	1.6 REF		0.063 REF	

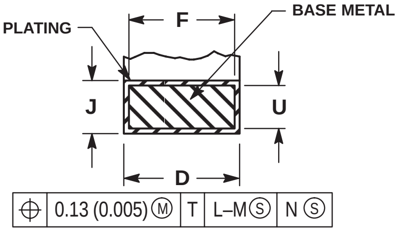
FB SUFFIX
CASE 848D–03
Plastic Package
ISSUE C



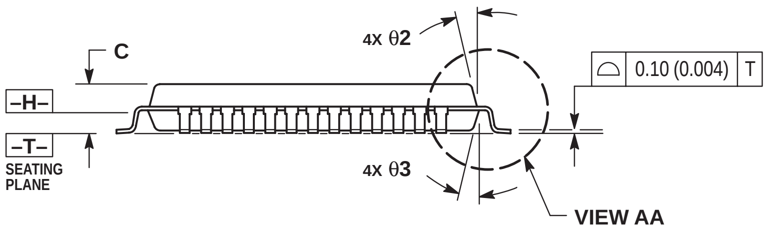


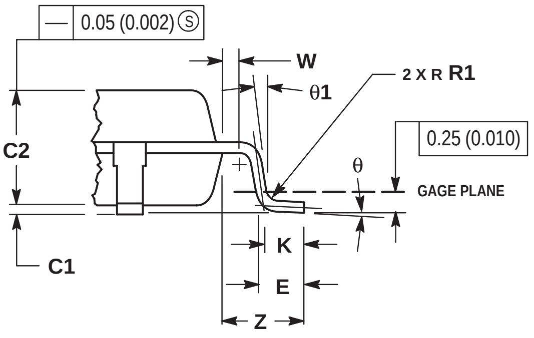


VIEW Y



SECTION AB–AB
ROTATED 90° CLOCKWISE





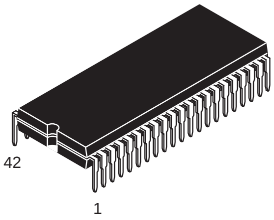
VIEW AA

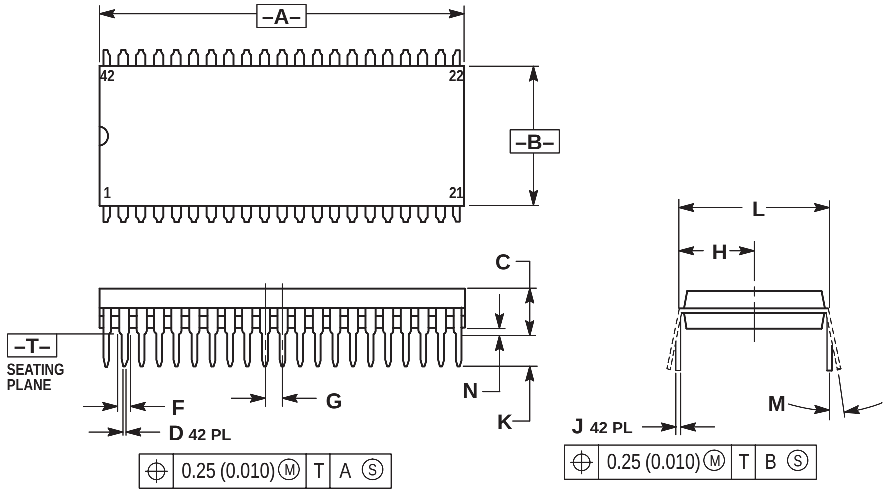
NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE –H– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS –L–, –M– AND –N– TO BE DETERMINED AT DATUM PLANE –H–.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE –T–.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.46 (0.018). MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION 0.07 (0.003).

	MILLIMETERS		INCHES	
DIM	**MIN**	**MAX**	**MIN**	**MAX**
A	10.00 BSC		0.394 BSC	
A1	5.00 BSC		0.197 BSC	
B	10.00 BSC		0.394 BSC	
B1	5.00 BSC		0.197 BSC	
C	—	1.70	—	0.067
C1	0.05	0.20	0.002	0.008
C2	1.30	1.50	0.051	0.059
D	0.20	0.40	0.008	0.016
E	0.45	0.75	0.018	0.030
F	0.22	0.35	0.009	0.014
G	0.65 BSC		0.026 BSC	
J	0.07	0.20	0.003	0.008
K	0.50 REF		0.020 REF	
R1	0.08	0.20	0.003	0.008
S	12.00 BSC		0.472 BSC	
S1	6.00 BSC		0.236 BSC	
U	0.09	0.16	0.004	0.006
V	12.00 BSC		0.472 BSC	
V1	6.00 BSC		0.236 BSC	
W	0.20 REF		0.008 REF	
Z	1.00 REF		0.039 REF	
θ	0°	7°	0°	7°
θ1	0°	—	0°	—
θ2	12° REF		12° REF	
θ3	5°	13°	5°	13°

B SUFFIX
CASE 858–01
Plastic Package
ISSUE O

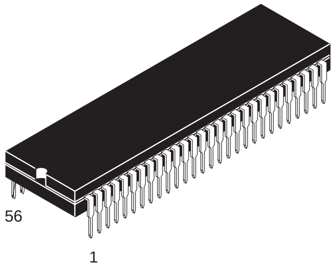


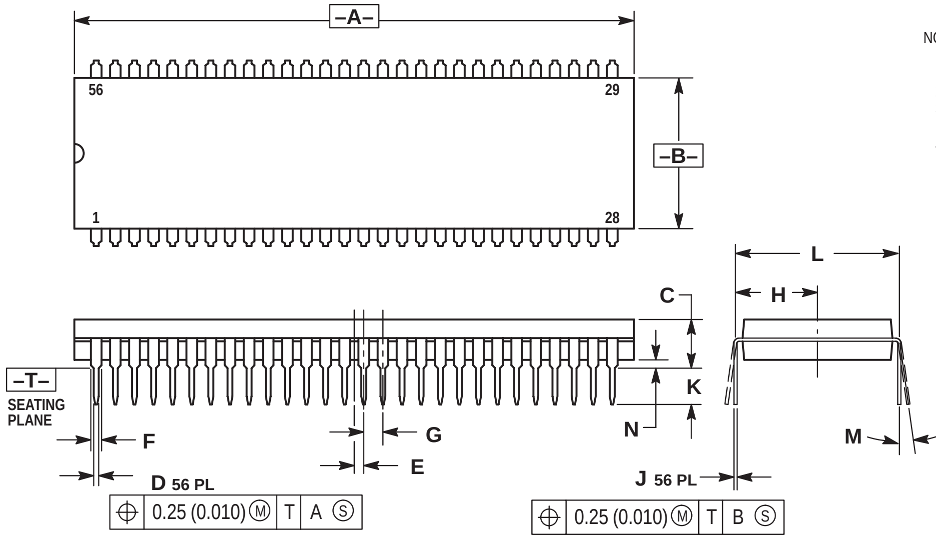


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH. MAXIMUM MOLD FLASH 0.25 (0.010).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.435	1.465	36.45	37.21
B	0.540	0.560	13.72	14.22
C	0.155	0.200	3.94	5.08
D	0.014	0.022	0.36	0.56
F	0.032	0.046	0.81	1.17
G	0.070 BSC		1.778 BSC	
H	0.300 BSC		7.62 BSC	
J	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.600 BSC		15.24 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.02

B SUFFIX
CASE 859–01
Plastic Package
(SDIP)
ISSUE O

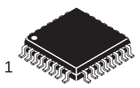


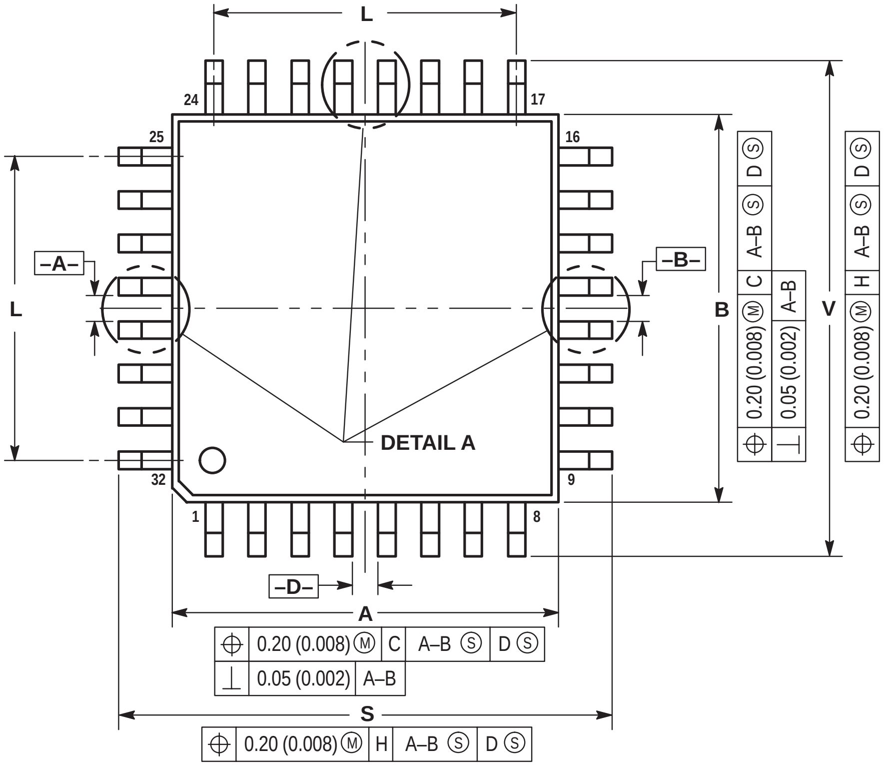


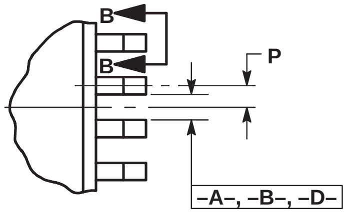
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH. MAXIMUM MOLD FLASH 0.25 (0.010)

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	2.035	2.065	51.69	52.45
B	0.540	0.560	13.72	14.22
C	0.155	0.200	3.94	5.08
D	0.014	0.022	0.36	0.56
E	0.035 BSC		0.89 BSC	
F	0.032	0.046	0.81	1.17
G	0.070 BSC		1.778 BSC	
H	0.300 BSC		7.62 BSC	
J	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.600 BSC		15.24 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.02

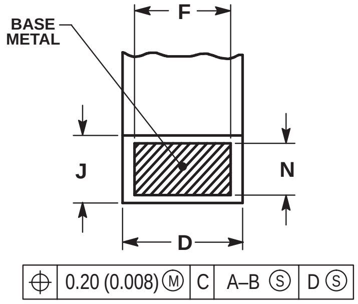
FB, FTB SUFFIX
CASE 873-01
Plastic Package
(TQFP–32)
ISSUE A



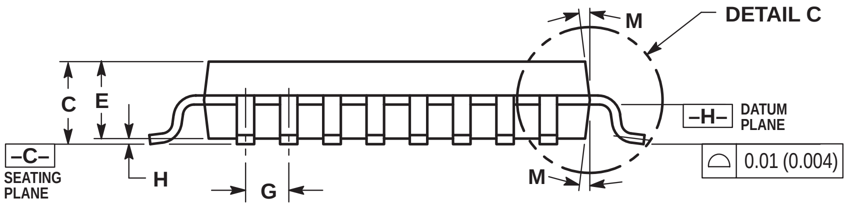


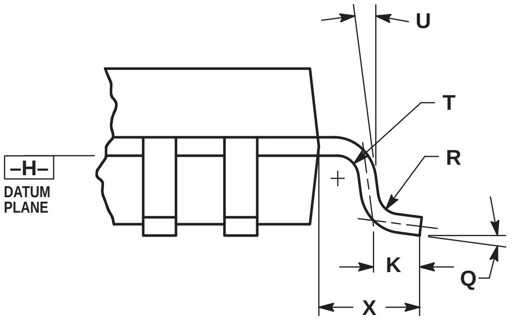


DETAIL A



SECTION B–B
VIEW ROTATED 90° CLOCKWISE





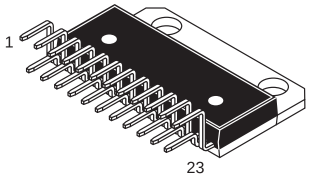
DETAIL C

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE –H– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS –A–, –B– AND –D– TO BE DETERMINED AT DATUM PLANE –H–.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE –C–.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –H–.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.

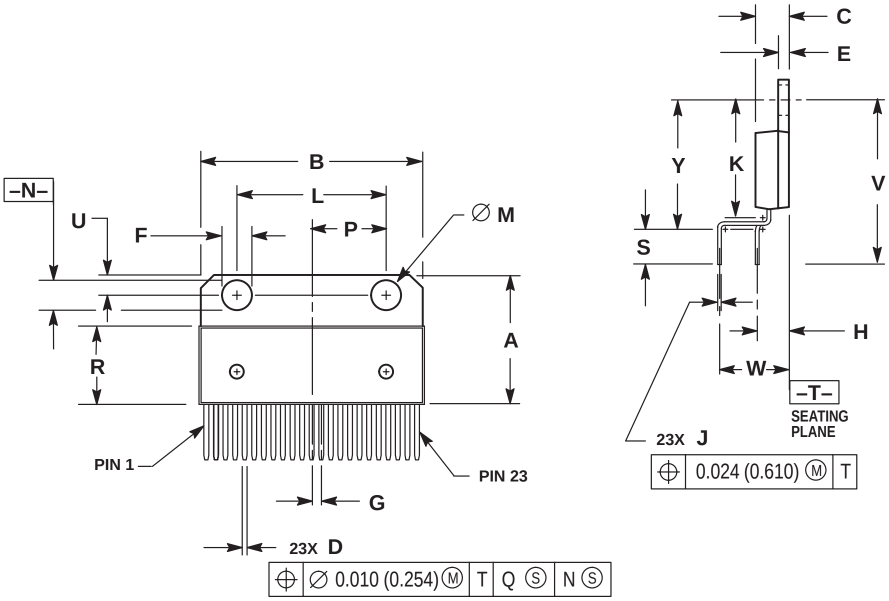
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	6.95	7.10	0.274	0.280
B	6.95	7.10	0.274	0.280
C	1.40	1.60	0.055	0.063
D	0.273	0.373	0.010	0.015
E	1.30	1.50	0.051	0.059
F	0.273	——	0.010	——
G	0.80 BSC		0.031 BSC	
H	——	0.20	——	0.008
J	0.119	0.197	0.005	0.008
K	0.33	0.57	0.013	0.022
L	5.6 REF		0.220 REF	
M	6°	8°	6°	8°
N	0.119	0.135	0.005	0.005
P	0.40 BSC		0.016 BSC	
Q	5°	10°	5°	10°
R	0.15	0.25	0.006	0.010
S	8.85	9.15	0.348	0.360
T	0.15	0.25	0.006	0.010
U	5°	11°	5°	11°
V	8.85	9.15	0.348	0.360
X	1.00 REF		0.039 REF	

T SUFFIX
CASE 894-03
Plastic Package
(23-Pin SZIP)
ISSUE B

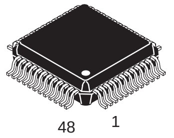


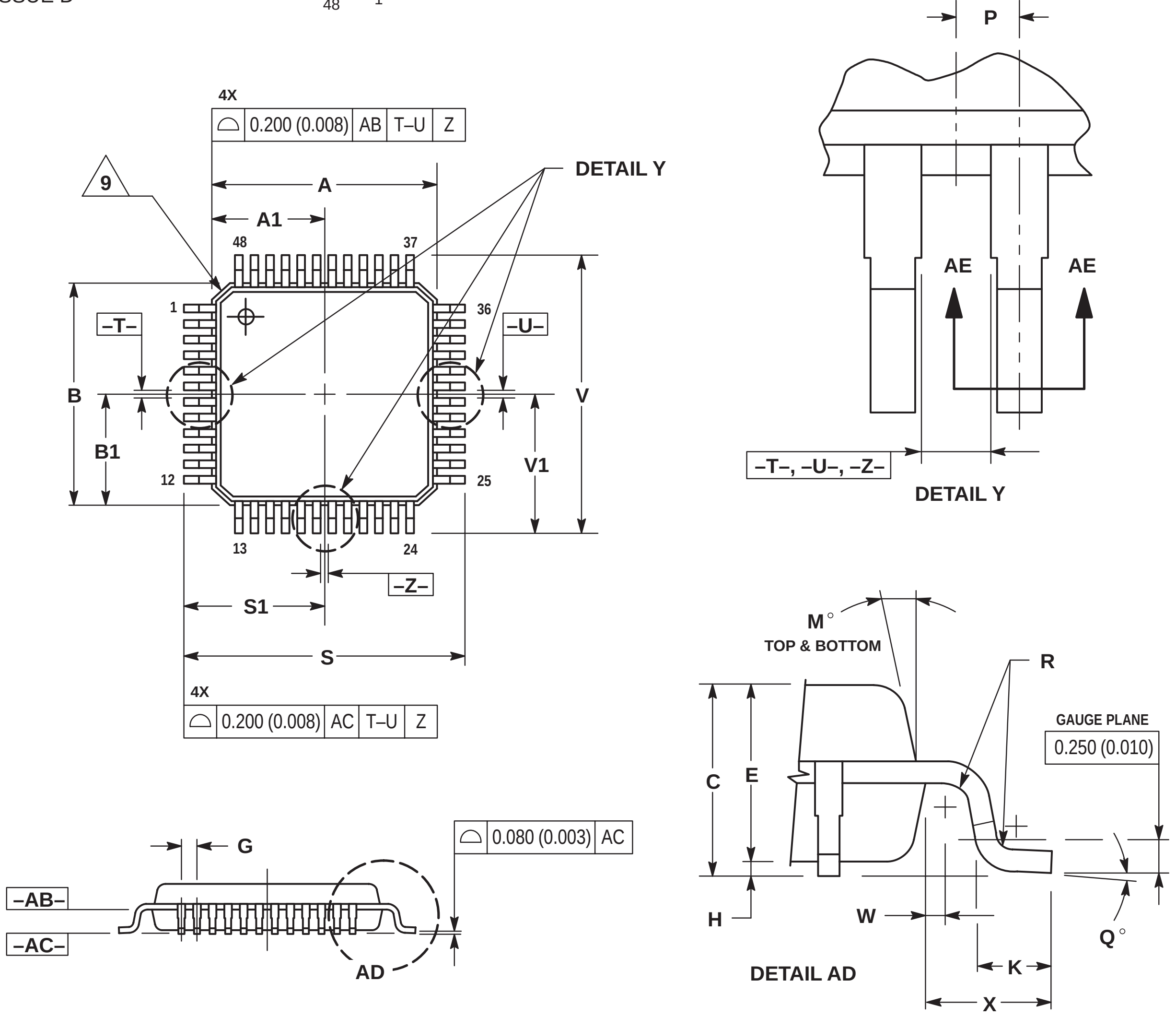
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION R DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
5. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.010 (0.250).
6. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.003 (0.076) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

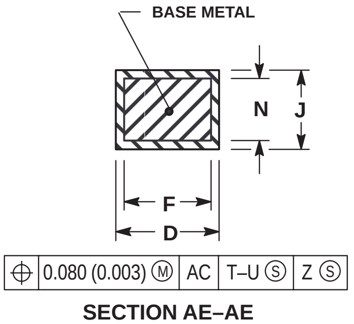
	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.684	0.694	17.374	17.627
B	1.183	1.193	30.048	30.302
C	0.175	0.179	4.445	4.547
D	0.026	0.031	0.660	0.787
E	0.058	0.062	1.473	1.574
F	0.165	0.175	4.191	4.445
G	0.050 BSC		1.270 BSC	
H	0.169 BSC		4.293 BSC	
J	0.014	0.020	0.356	0.508
K	0.625	0.639	15.875	16.231
L	0.770	0.790	19.558	20.066
M	0.148	0.152	3.760	3.861
N	0.148	0.152	3.760	3.861
P	0.390 BSC		9.906 BSC	
R	0.416	0.424	10.566	10.770
S	0.157	0.167	3.988	4.242
U	0.105	0.115	2.667	2.921
V	0.868 REF		22.047 REF	
W	0.200 BSC		5.080 BSC	
Y	0.700	0.710	17.780	18.034



FTA SUFFIX
CASE 932–02
Plastic Package
(TQFP–48)
ISSUE D





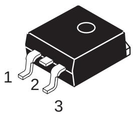


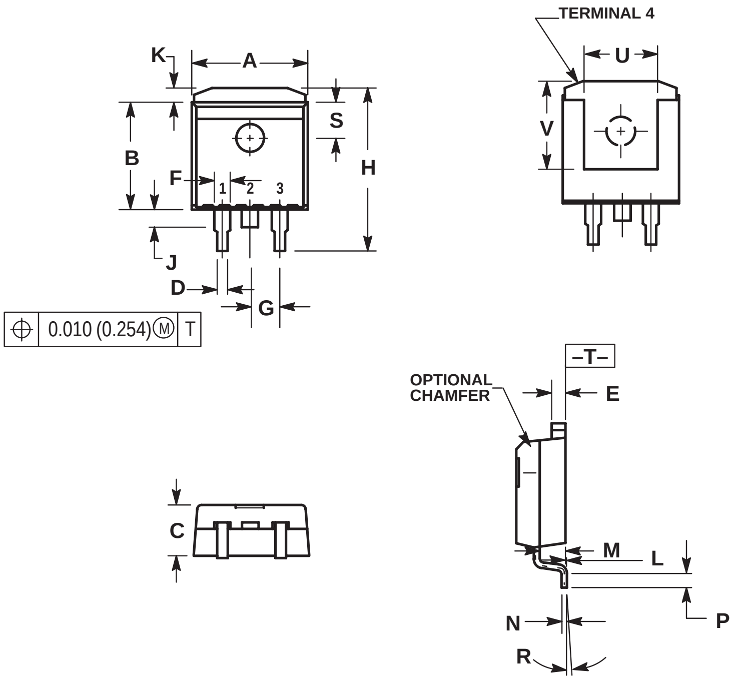
SECTION AE–AE

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE –AB– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS –T–, –U–, AND –Z– TO BE DETERMINED AT DATUM PLANE –AB–.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE –AC–.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –AB–.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.350 (0.014).
8. MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076 (0.0003).
9. EXACT SHAPE OF EACH CORNER IS OPTIONAL.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	7.000 BSC		0.276 BSC	
A1	3.500 BSC		0.138 BSC	
B	7.000 BSC		0.276 BSC	
B1	3.500 BSC		0.138 BSC	
C	1.400	1.600	0.055	0.063
D	0.170	0.270	0.007	0.011
E	1.350	1.450	0.053	0.057
F	0.170	0.230	0.007	0.009
G	0.500 BASIC		0.020 BASIC	
H	0.050	0.150	0.002	0.006
J	0.090	0.200	0.004	0.008
K	0.500	0.700	0.020	0.028
M	12 °REF		12 °REF	
N	0.090	0.160	0.004	0.006
P	0.250 BASIC		0.010 BASIC	
Q	1°	5°	1°	5°
R	0.150	0.250	0.006	0.010
S	9.000 BSC		0.354 BSC	
S1	4.500 BSC		0.177 BSC	
V	9.000 BSC		0.354 BSC	
V1	4.500 BSC		0.177 BSC	
W	0.200 REF		0.008 REF	
X	1.000 REF		0.039 REF	

D2T SUFFIX
CASE 936–03
Plastic Package
ISSUE B

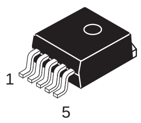


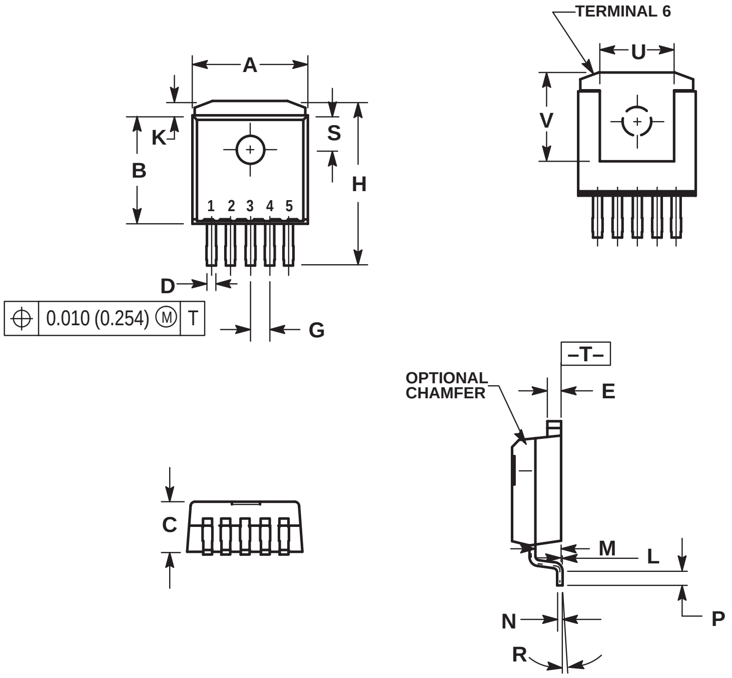


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. TAB CONTOUR OPTIONAL WITHIN DIMENSIONS A AND K.
4. DIMENSIONS U AND V ESTABLISH A MINIMUM MOUNTING SURFACE FOR TERMINAL 4.
5. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH OR GATE PROTRUSIONS. MOLD FLASH AND GATE PROTRUSIONS NOT TO EXCEED 0.025 (0.635) MAXIMUM.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.386	0.403	9.804	10.236
B	0.356	0.368	9.042	9.347
C	0.170	0.180	4.318	4.572
D	0.026	0.036	0.660	0.914
E	0.045	0.055	1.143	1.397
F	0.051 REF		1.295 REF	
G	0.100 BSC		2.540 BSC	
H	0.539	0.579	13.691	14.707
J	0.125 MAX		3.175 MAX	
K	0.050 REF		1.270 REF	
L	0.000	0.010	0.000	0.254
M	0.088	0.102	2.235	2.591
N	0.018	0.026	0.457	0.660
P	0.058	0.078	1.473	1.981
R	5° REF		5° REF	
S	0.116 REF		2.946 REF	
U	0.200 MIN		5.080 MIN	
V	0.250 MIN		6.350 MIN	

D2T SUFFIX
CASE 936A–02
Plastic Package
(D^{2}PAK)
ISSUE A

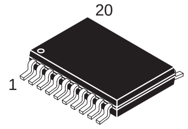


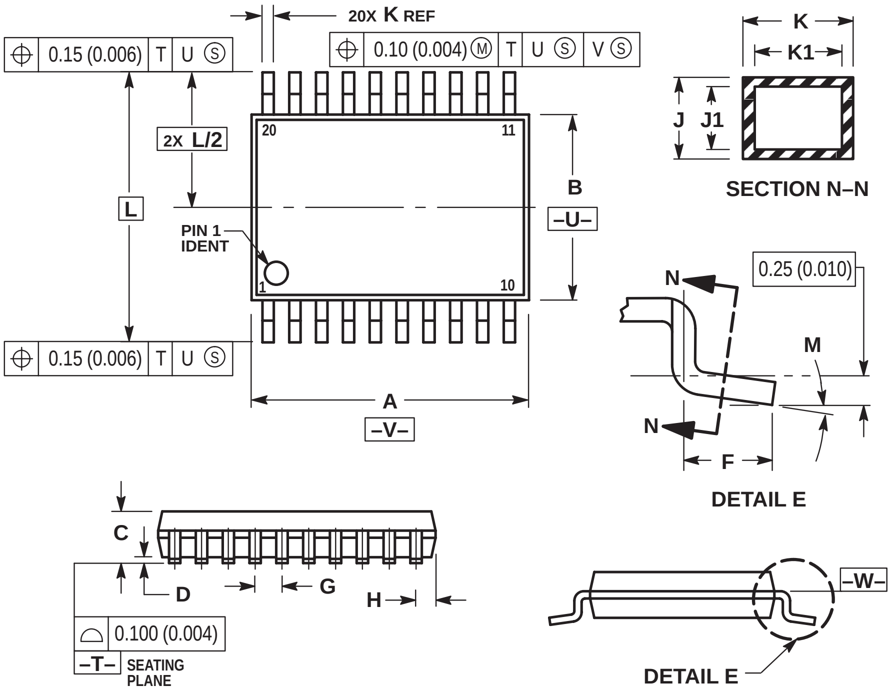


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. TAB CONTOUR OPTIONAL WITHIN DIMENSIONS A AND K.
4. DIMENSIONS U AND V ESTABLISH A MINIMUM MOUNTING SURFACE FOR TERMINAL 6.
5. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH OR GATE PROTRUSIONS. MOLD FLASH AND GATE PROTRUSIONS NOT TO EXCEED 0.025 (0.635) MAXIMUM.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.386	0.403	9.804	10.236
B	0.356	0.368	9.042	9.347
C	0.170	0.180	4.318	4.572
D	0.026	0.036	0.660	0.914
E	0.045	0.055	1.143	1.397
G	0.067 BSC		1.702 BSC	
H	0.539	0.579	13.691	14.707
K	0.050 REF		1.270 REF	
L	0.000	0.010	0.000	0.254
M	0.088	0.102	2.235	2.591
N	0.018	0.026	0.457	0.660
P	0.058	0.078	1.473	1.981
R	5° REF		5° REF	
S	0.116 REF		2.946 REF	
U	0.200 MIN		5.080 MIN	
V	0.250 MIN		6.350 MIN	

DT, DTB SUFFIX
CASE 948E–02
Plastic Package
(TSSOP–20)
ISSUE A

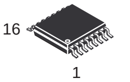


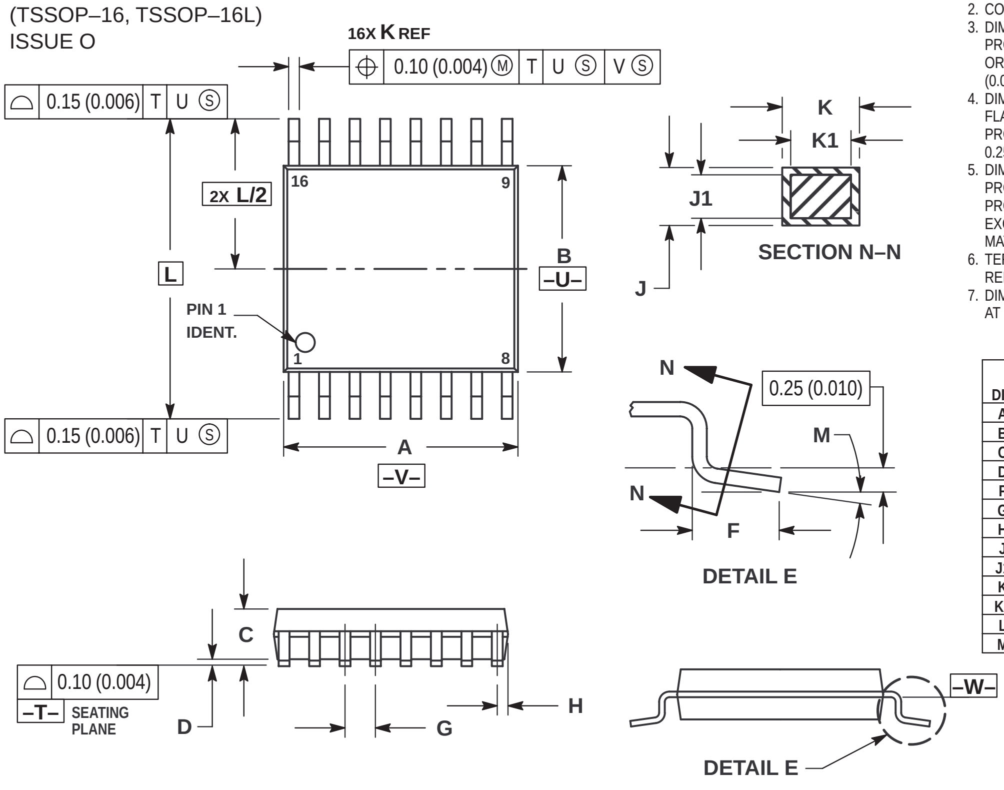


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	6.40	6.60	0.252	0.260
B	4.30	4.50	0.169	0.177
C	—	1.20	—	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

DTB SUFFIX
CASE 948F–01
Plastic Package
(TSSOP–16, TSSOP–16L)
ISSUE O

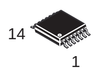


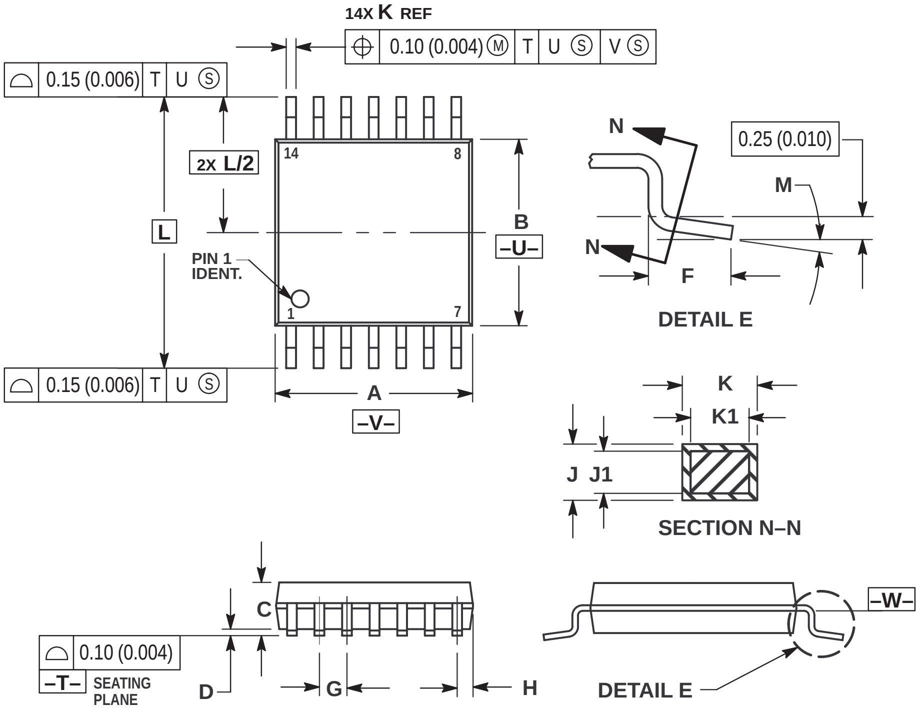


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	—	1.20	—	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

DTB SUFFIX
CASE 948G–01
Plastic Package
(TSSOP–14)
ISSUE O

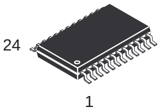


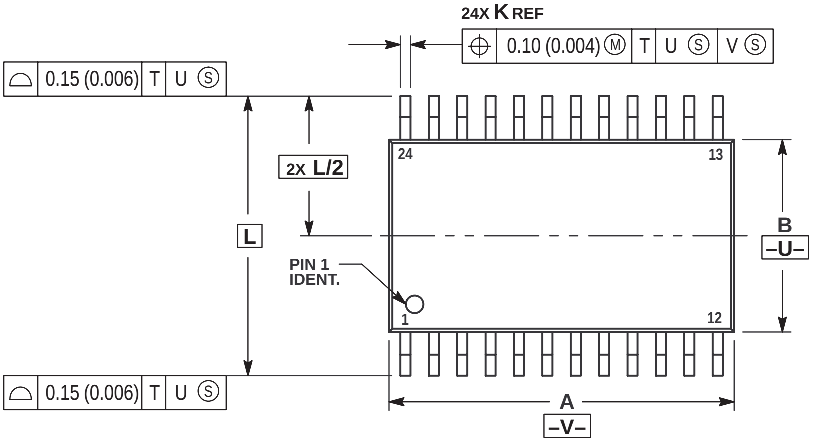


NOTES:
1 DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2 CONTROLLING DIMENSION: MILLIMETER.
3 DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4 DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5 DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6 TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7 DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

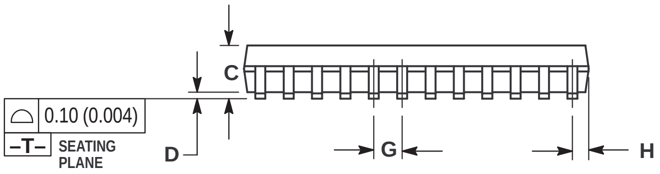
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	—	1.20	—	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

DTB SUFFIX
CASE 948H–01
Plastic Package
ISSUE O

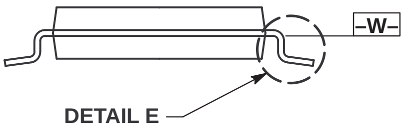


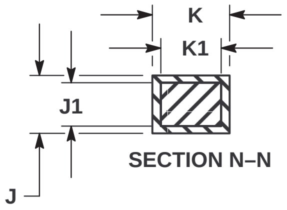


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

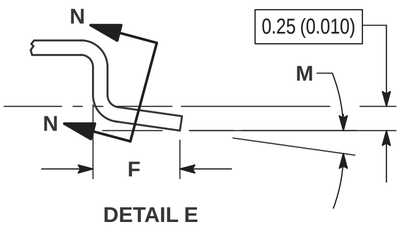


	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	7.70	7.90	0.303	0.311
B	4.30	4.50	0.169	0.177
C	—	1.20	—	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°



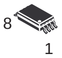


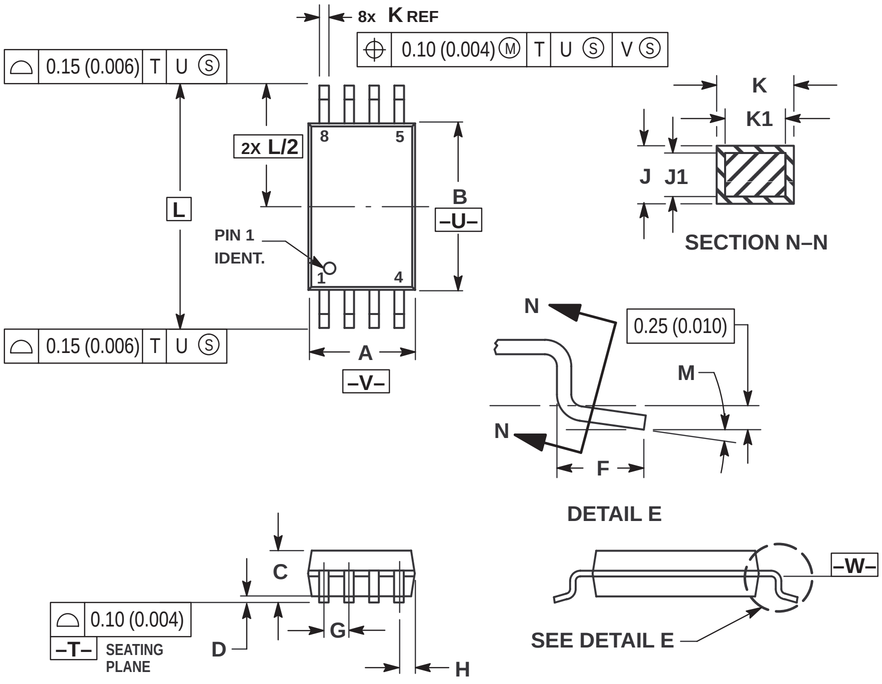
SECTION N–N



DETAIL E

DTB SUFFIX
CASE 948J–01
Plastic Package
(TSSOP–8)
ISSUE O

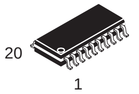


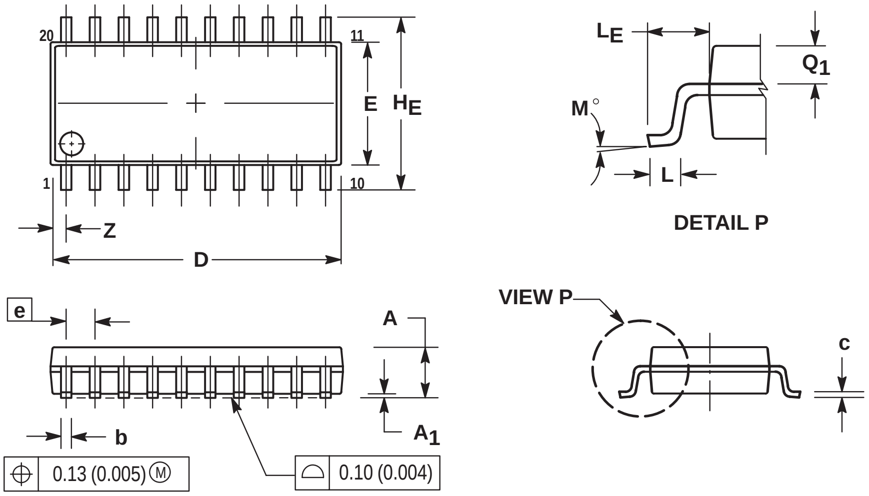


NOTES:
1 DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2 CONTROLLING DIMENSION: MILLIMETER.
3 DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4 DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5 DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6 TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7 DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	2.90	3.10	0.114	0.122
B	4.30	4.50	0.169	0.177
C	——	1.20	——	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

M SUFFIX
CASE 967–01
Plastic Package
(EIAJ–20)
ISSUE O

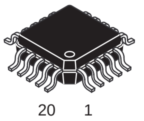




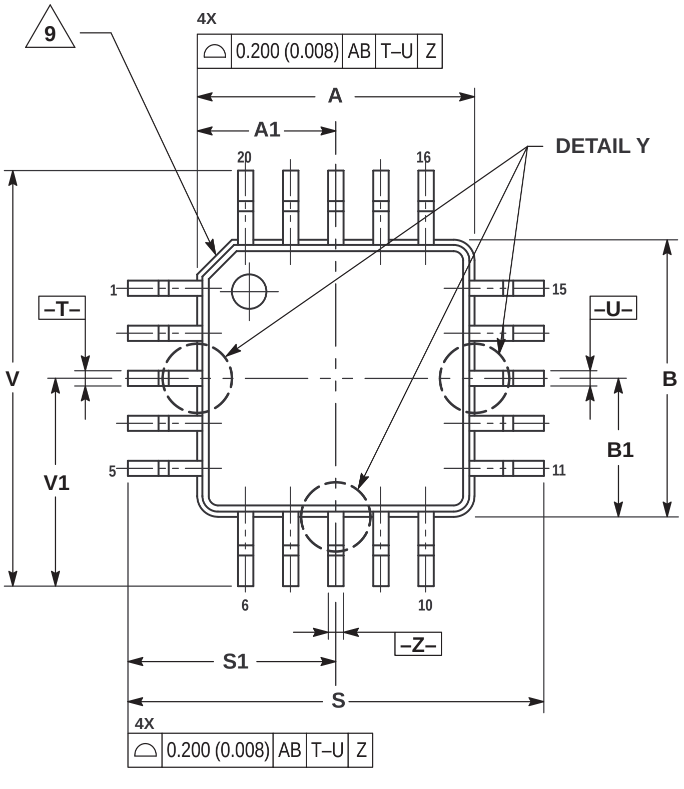
NOTES:
1 DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2 CONTROLLING DIMENSION: MILLIMETER.
3 DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4 TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5 THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	——	2.05	——	0.081
A_1	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.18	0.27	0.007	0.011
D	12.35	12.80	0.486	0.504
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
H_E	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
L_E	1.10	1.50	0.043	0.059
M	0°	10°	0°	10°
Q_1	0.70	0.90	0.028	0.035
Z	——	0.81	——	0.032

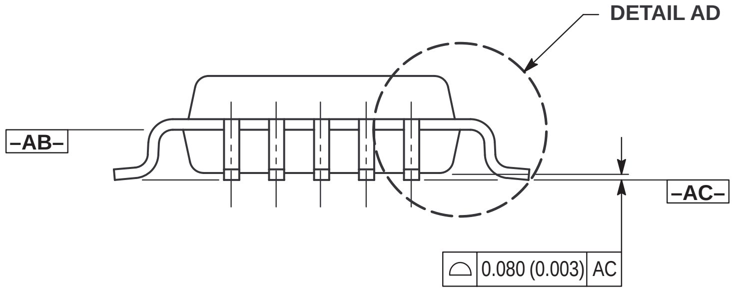
FTB SUFFIX
CASE 976–01
Plastic Package
(TQFP–20)
ISSUE O

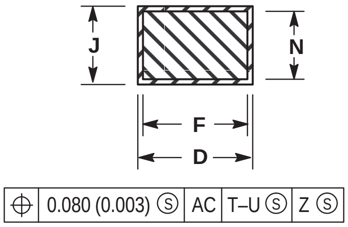


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE –AB– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS –T–, –U–, AND –Z– TO BE DETERMINED AT DATUM PLANE –AB–.
5. DIMENSIONS S AND V TO BE DETERMINED AT DATUM PLANE –AC–.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –AB–.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.350 (0.014).
8. MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076 (0.0003).
9. EXACT SHAPE OF EACH CORNER IS OPTIONAL.

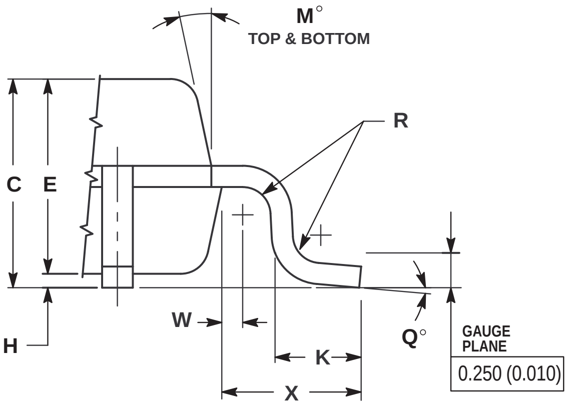


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.000 BSC		0.157 BSC	
A1	2.000 BSC		0.079 BSC	
B	4.000 BSC		0.157 BSC	
B1	2.000 BSC		0.079 BSC	
C	1.400	1.600	0.055	0.063
D	0.170	0.270	0.007	0.011
E	1.350	1.450	0.053	0.057
F	0.170	0.230	0.007	0.009
G	0.650 BSC		0.026 BSC	
H	0.050	0.150	0.002	0.006
J	0.090	0.200	0.004	0.008
K	0.500	0.700	0.020	0.028
M	12° REF		12° REF	
N	0.090	0.160	0.004	0.006
P	0.250 BSC		0.010 BSC	
Q	1°	5°	1°	5°
R	0.150	0.250	0.006	0.010
S	6.000 BSC		0.236 BSC	
S1	3.000 BSC		0.118 BSC	
V	6.000 BSC		0.236 BSC	
V1	3.000 BSC		0.118 BSC	
W	0.200 REF		0.008 REF	
X	1.000 REF		0.039 REF	

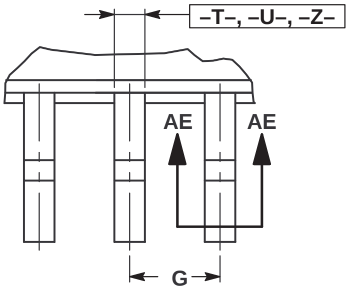




SECTION AE–AE

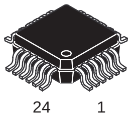


DETAIL AD



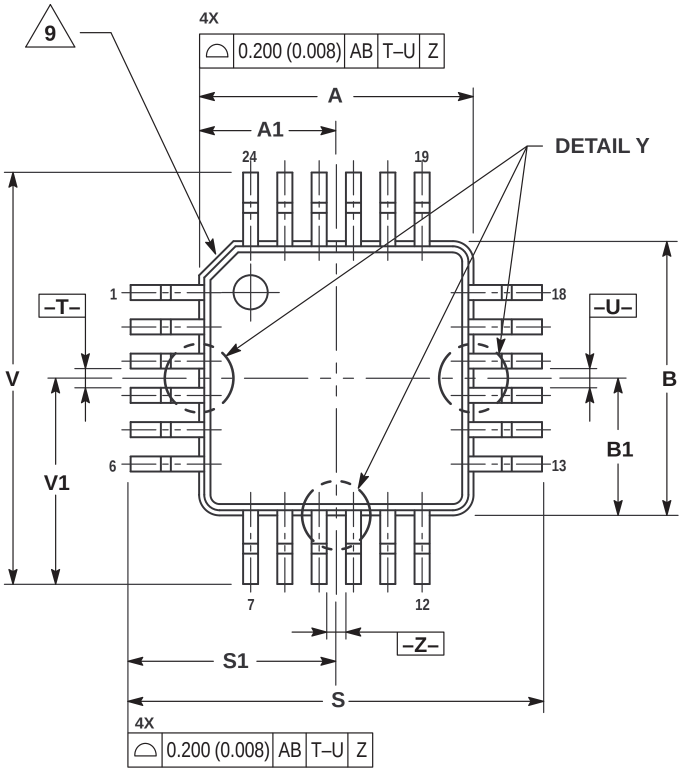
DETAIL Y

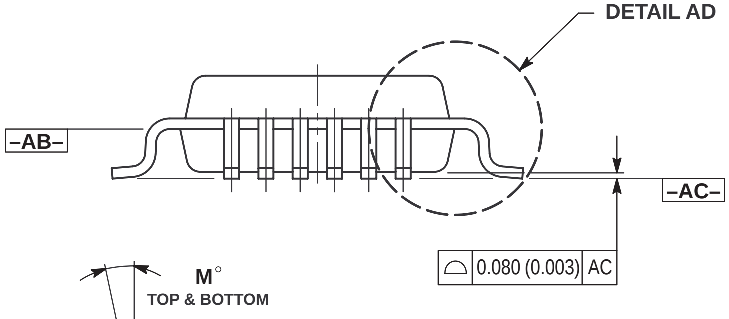
FTA SUFFIX
CASE 977–01
Plastic Package
ISSUE O

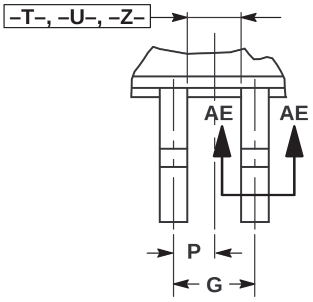


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE –AB– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS –T–, –U–, AND –Z– TO BE DETERMINED AT DATUM PLANE –AB–.
5. DIMENSIONS S AND V TO BE DETERMINED AT DATUM PLANE –AC–.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –AB–.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.350 (0.014).
8. MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076 (0.0003).
9. EXACT SHAPE OF EACH CORNER IS OPTIONAL.

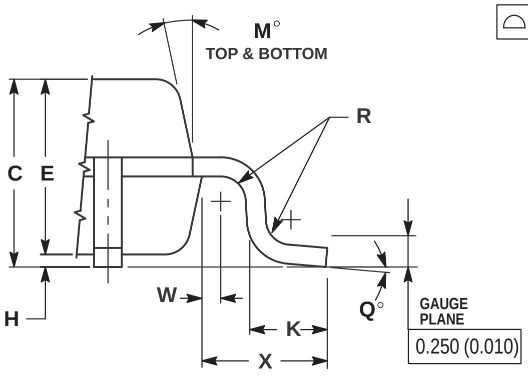
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.000 BSC		0.157 BSC	
A1	2.000 BSC		0.079 BSC	
B	4.000 BSC		0.157 BSC	
B1	2.000 BSC		0.079 BSC	
C	1.400	1.600	0.055	0.063
D	0.170	0.270	0.007	0.011
E	1.350	1.450	0.053	0.057
F	0.170	0.230	0.007	0.009
G	0.500 BSC		0.020 BSC	
H	0.050	0.150	0.002	0.006
J	0.090	0.200	0.004	0.008
K	0.500	0.700	0.020	0.028
M	12° REF		12° REF	
N	0.090	0.160	0.004	0.006
P	0.250 BSC		0.010 BSC	
Q	1°	5°	1°	5°
R	0.150	0.250	0.006	0.010
S	6.000 BSC		0.236 BSC	
S1	3.000 BSC		0.118 BSC	
V	6.000 BSC		0.236 BSC	
V1	3.000 BSC		0.118 BSC	
W	0.200 REF		0.008 REF	
X	1.000 REF		0.039 REF	



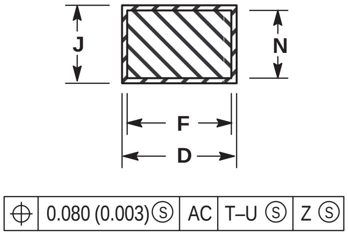




DETAIL Y

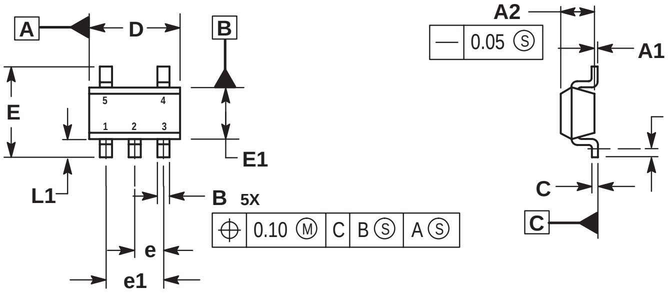


DETAIL AD



SECTION AE–AE

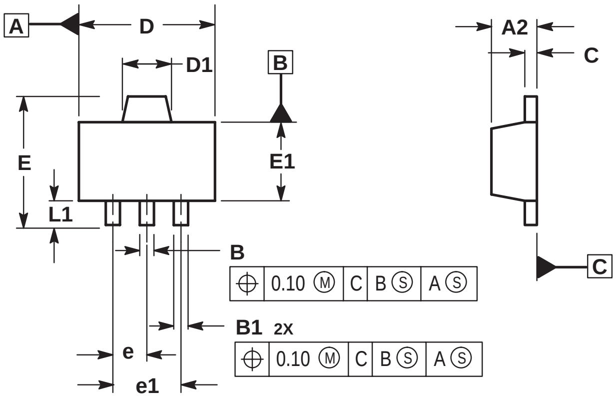
N SUFFIX
CASE 1212–01
Plastic Package
(SOT–23)
ISSUE O



NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DATUM C IS A SEATING PLANE.

	MILLIMETERS	
DIM	MIN	MAX
A1	0.00	0.10
A2	1.00	1.30
B	0.30	0.50
C	0.10	0.25
D	2.80	3.00
E	2.50	3.10
E1	1.50	1.80
e	0.95 BSC	
e1	1.90 BSC	
L	0.20	—
L1	0.45	0.75

H SUFFIX
CASE 1213–01
Plastic Package
(SOT–89)
ISSUE O



NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
3. DATUM C IS A SEATING PLANE.

	MILLIMETERS	
DIM	MIN	MAX
A2	1.40	1.60
B	0.37	0.57
B1	0.32	0.52
C	0.30	0.50
D	4.40	4.60
D1	1.50	1.70
E	—	4.25
E1	2.40	2.60
e	1.50 BSC	
e1	3.00 BSC	
L1	0.80	—

Quality and Reliability Assurance

In Brief . . .

The word quality has been used to describe many things, such as fitness for use, customer satisfaction, customer enthusiasm, what the customer says quality is, etc. These descriptions convey important truths, however, quality should be described in a way that precipitates immediate action. With that in mind, quality can be described as reduction of variability around a target, so that conformance to customer requirements and possibly expectations can be achieved in a cost effective way. This definition provides direction and potential for immediate action for a person desiring to improve quality.

The definition of quality as described above can be applied to a task, process or a whole company. If we are to reap the benefits of quality and obtain a competitive advantage, quality must be applied to the whole company.

Implementation of quality ideas company wide requires a quality plan showing: a philosophy (belief) of operation, measurable goals, training of individuals and methods of communicating this philosophy of operation to the whole organization.

Motorola, for example, believes that quality and reliability are the responsibility of every person. Participative Management is the process by which problem solving and quality improvement are facilitated at all levels of the organization through crossfunctional teams. Continuous improvement for the individual is facilitated by a broad educational program covering onsite, university and college courses. Motorola University provides leadership and administers this educational effort on a company wide basis.

Another key belief is that quality excellence is accomplished by people doing things right the first time and committed to never ending improvement. The Six Sigma (6σ) challenge is designed to convey and facilitate the idea of continuous improvement at all levels.

Page

Quality Concepts

Quality improvement for a task or a process can be quickly described in terms of the target, current status with respect to target (variability), reduction of variability (commitment to never ending improvement), customer requirements (who receives output, what are a person's requirements/ expectations) and economics (cost of nonconformance, loss function, etc.).

Application of quality to the whole company has come to be known by such names as **"Total Quality Control" (TQC); "Company Wide Quality Control" (CWQC); "Total Quality Excellence" or "Total Quality Engineering" (TQE); "Total Quality Involvement" (TQI).** These names attempt to convey the idea that quality is a process (a way of acting continuously) rather than a program (implying a beginning and an end). Nevertheless for this process to be successful it must be able to show measurable results.

"**Six Sigma** is the required capability level to approach the standard. The **standard** is **zero defects**. Our goal is to be Best-in-Class in product, sales and service." (For a more detailed explanation, contact your Motorola Representative for a pamphlet of the Six Sigma Challenge.)

Quick insight into six sigma is obtained if we realize that a six sigma process has variability which is one half of the variation allowed (tolerance, spread) by the customer requirements (i.e. natural variation is one half of the customer specification range for a given characteristic). When six sigma is achieved, virtually zero defects are observed in the output of a process/product even allowing for potential process shifts (Figure 1).

Policies, objectives and five year plans are the mechanisms for communicating the key beliefs and measurable goals to all personnel and continuously keeping them in focus. This is done at the corporate, sector, group, division, and department levels.

The Analog Division, for example, evaluates performance to the corporate goals of **10 fold improvement by 1989; 100 fold improvement by 1991** and achievement of **six sigma capability by 1992** by utilizing indices such as Outgoing Electrical and Visual Mechanical Quality **(AOQ)** in terms of PPM (parts per million or sometimes given in parts per billion); **% of devices with zero PPM ; product quality returns** (RMR); number of processes/products with specified **capability indices (cp, cpk); six sigma capability roadmaps; failure rates for various reliability tests** (operating life, temperature humidity bias, hast, temperature cycling, etc.); **on-time delivery; customer product evaluation and failure analysis turnaround; cost of nonconformance; productivity improvement and personnel development**.

Figure 2 shows the improvement in electrical outgoing quality for analog products over recent years in a normalized form. Figure 3 shows the number of parts with zero PPM over a period of time.

Documentation control is an important part of **statistical process control. Process mapping** (flow charting etc.) with documentation identified allows visualization and therefore optimization of the process. Figure 4 shows a portion of a flow chart for wafer fabrication. **Control plans** are an important part of Statistical Process Control, these plans identify in detail critical points where data for process control is taken, parameters measured, frequency of measurements, type of control device used, measuring equipment, responsibilities and reaction plans. Figure 5 shows a portion of a control plan for wafer fabrication. Six sigma progress is tracked by roadmaps based on the six sigma process, a portion of which is shown on Figure 6.

On-time delivery is of great importance, with the current emphasis on **just-in-time** systems. Tracking is done on an overall basis, and at the device levels.

Figure 1. A Six Sigma Process Has Virtually Zero Defects Allowing for 1.5σ Shift

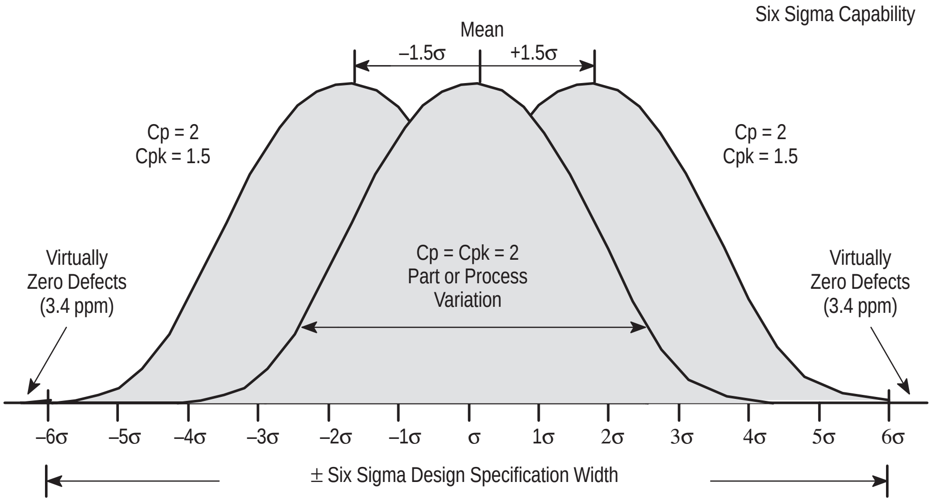


Figure 2. Motorola Logic & Analog Technologies Group Electrical AOQ

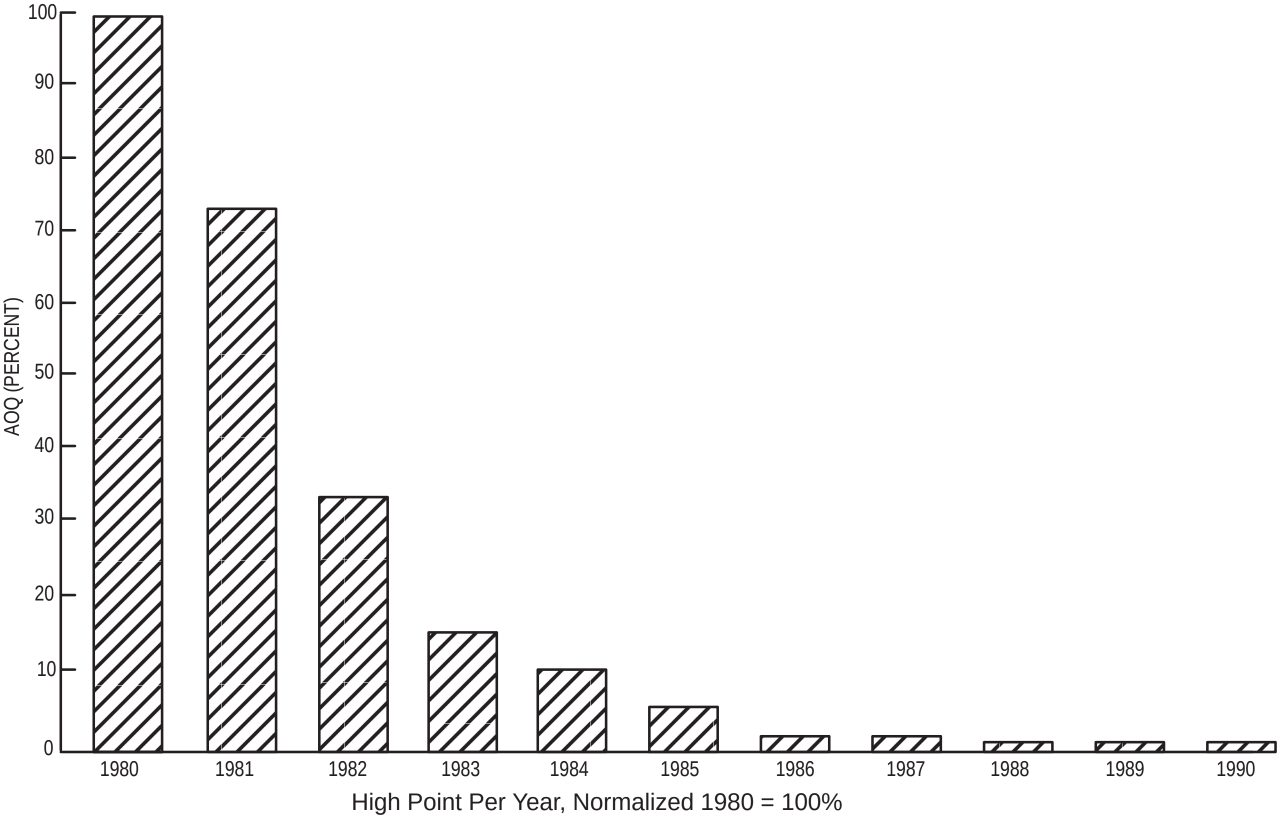


Figure 3. Percentage of Parts with Zero PPM AOQ

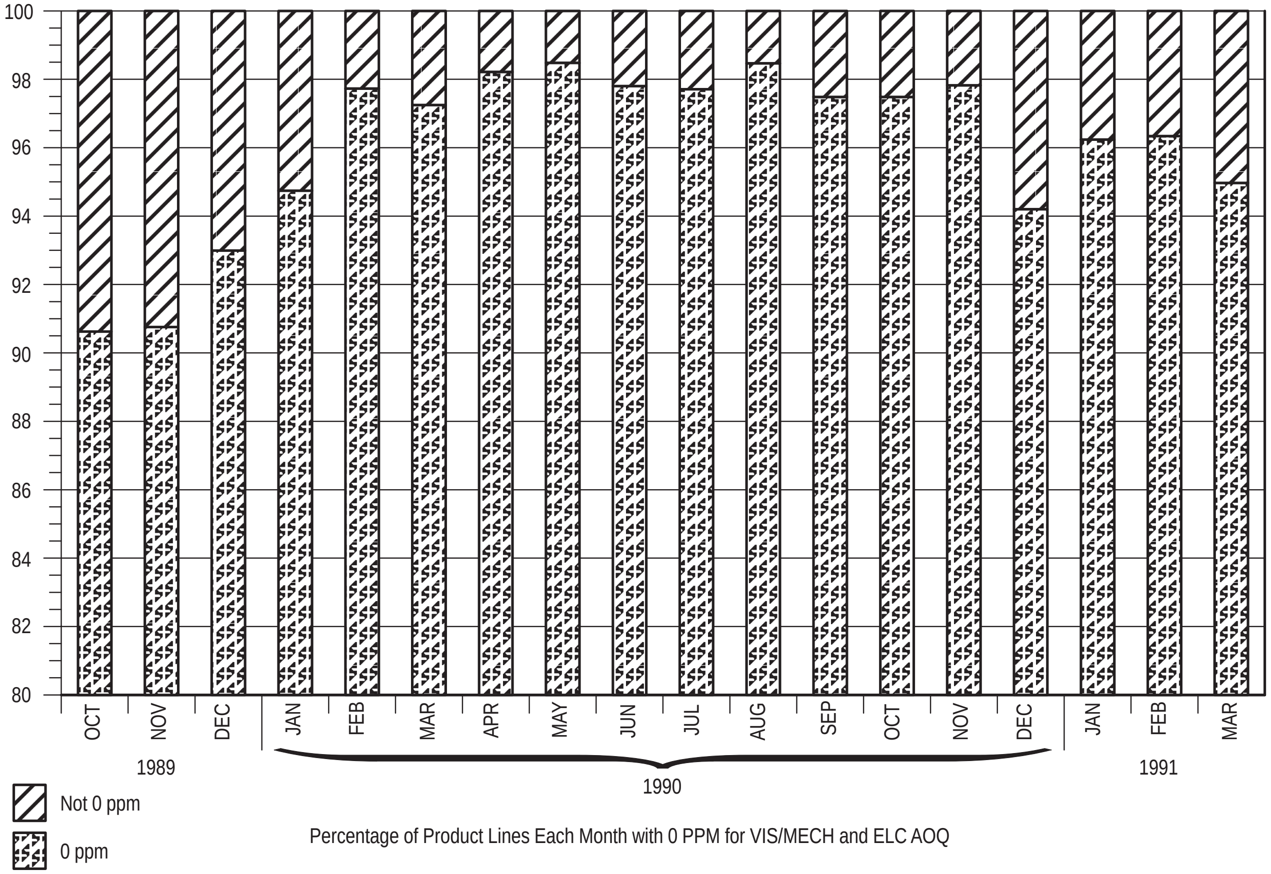
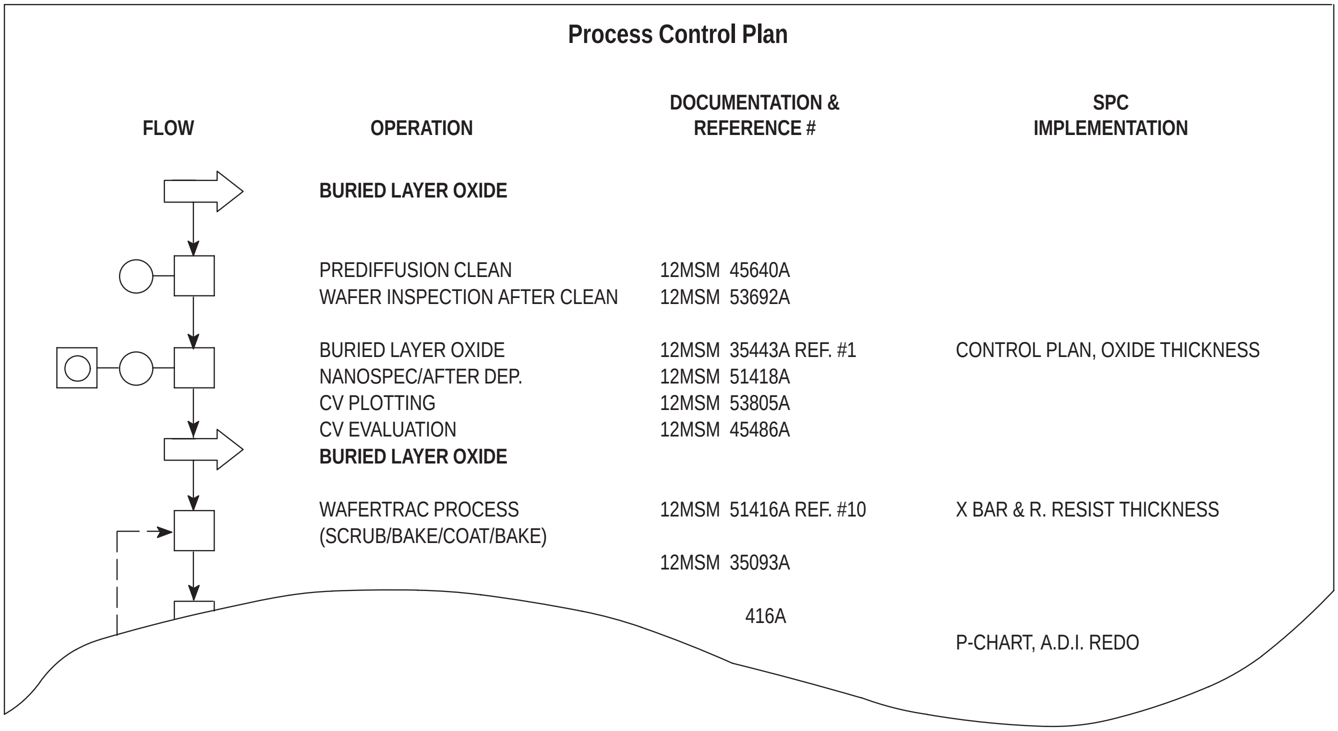


Figure 4. Portion of a Process Flow Chart From Wafer Fab, Showing Documentation Control and SPC



Process Control Plan

OPERATION	DOCUMENTATION & REFERENCE #	SPC IMPLEMENTATION
BURIED LAYER OXIDE		
PREDIFFUSION CLEAN	12MSM 45640A	
WAFER INSPECTION AFTER CLEAN	12MSM 53692A	
BURIED LAYER OXIDE	12MSM 35443A REF. #1	CONTROL PLAN, OXIDE THICKNESS
NANOSPEC/AFTER DEP.	12MSM 51418A	
CV PLOTTING	12MSM 53805A	
CV EVALUATION	12MSM 45486A	
BURIED LAYER OXIDE		
WAFERTRAC PROCESS (SCRUB/BAKE/COAT/BAKE)	12MSM 51416A REF. #10	X BAR & R. RESIST THICKNESS
	12MSM 35093A	
	416A	
		P-CHART, A.D.I. REDO

Figure 5. Part of a Wafer Fab Control Plan, Showing Statistical Process Control Details

Characteristics:

Code	Description	Code	Description
A	VISUAL DEFECTS	E	FILM SHEET RESISTANCE
B	VISUAL DEFECTS . . . MICROSCOPE	F	REFRACTIVE INDEX
C	PARTICLE . . . MONITOR	G	CRITICAL DIMENSION
D	FILM THICKNESS	H	CV PLOT

Process Location	Ref. No.	Characteristic Affected	Part/Process Detail	Measurements Method	Analysis Methods	Frequency Sample Size	Reaction Plan: Point out of Limit (3) (4)
B.L. OXIDE	1	D	OXIDE THICKNESS	NANOMETRIC	CONTROL GRAPH	EVERY RUN 3 WFR/RUN	IMPOUND LOT (1) ADJUST TIME TO CENTER PROCESS PER SPEC
EPI	2	D	THICKNESS	DIGILAB	$\bar{X}$ R CHART	EVERY RUN 5 SITES/WFR	IMPOUND LOT (1) NOTIFY ENGR.
QA		D	THICKNESS	DIGILAB	$\bar{X}$ R CHART	1WFR/SHIFT 5 SITES/WFR	IMPOUND LOT (2) NOTIFY ENGR.
		E	FILM RESISTIVITY	4PT PROBE	$\bar{X}$ R CHART	EVERY RUN 5 SITES/WFR	IMPOUND LOT (1) NOTIFY ENGR.
QA		E	FILM RESISTIVITY	4PT PROBE	$\bar{X}$ R CHART	1WFR/SHIFT 5 SITES/WFR	IMPOUND LOT (2) NOTIFY ENGR.
DEEP				4PT PROBE	MOVING R	EVERY LOT 1 CTRL WFR PER LOT	IMPOUND LOT NOTIFY ENGR.

Figure 6. Portion of Six Sigma (6σ) Roadmap Showing Steps to Six Sigma Capability

STEP	±6σ Summary
1. Identify critical characteristics	• Product Description • Marketing • Industrial Design • R&D/Developmental Engineering • Actual or Potential Customers
2. Determine specified product elements contributing to critical characteristics	• Critical Characteristics Matrix • Cause-and-Effect and Ishikawa Diagrams • Success Tree/Fault Tree Analysis • Component Search or Other Forms of Planned Experimentation • FMECA (Failure Mode Effects and Critical Analysis)
3. For each product element, determine the process step or process choice that affects or controls required performance	• Planned Experiments • Computer-Aided Simulation • TOP/Process Engineering Studies • Multi-Vari Analysis • Comparative Experiments
4. Determine maximum (real) allowable tolerance for each and process	• Graphing Techniques • Engineering Handbooks • Planned Experiments • Optimization, Especially Response Surface Methodology

Reliability Concepts

Reliability is the probability that an analog integrated circuit will succesfully perform its specified function in a given environment for a specified period of time. This is the classical definition of reliability applied to analog integrated circuits.

Another way of thinking about reliability is in relationship to quality. While **quality** is a measure of variability (extending to potential nonconformances-rejects) in the population domain, **reliability** is a measure of variability (extending to potential nonconformances-failures) in the population, time and environmental conditions domain. In brief, **reliability** can be thought of as **quality over time** and **environmental conditions**.

Ultimately, **product reliability** is a function of proper **understanding** of **customer requirements** and **communicating** them throughout design, product/process development, manufacturing and final product use. **Quality Function Deployment (QFD)** is a technique which may be used to facilitate identification of customer quality and reliability requirements and communicating them throughout an organization.

The most frequently used reliability measure for integrated circuits is the **failure rate expressed** in percent per thousand device hours (%/1000 hrs.). If the time interval is small the failure rate is called **Instantaneous Failure Rate** [λ (t)] or ‘‘Hazard Rate.” If the time interval is long (for example total operational time) the failure rate is called **Cumulative Failure Rate**.

The number of failures observed, taken over the number of device hours accumulated at the end of the observation period and expressed as a percent is called the point estimate failure rate. This however, is a number obtained from observations from a sample of all integrated circuits. If we are to use this number to estimate the failure rate of all integrated circuits (total population), we need to say something about the risk we are taking by using this estimate. A **risk** statement is provided by the **confidence level** expressed together with the failure rate. Mathematically, the failure rate at a given confidence level is obtained from the point estimate and the **CHI square** (X^2) distribution. (The X^2 is a statistical distribution used to relate the observed and expected frequencies of an event.) In practice, a reliability calculator rule is used which gives the failure rate at the confidence level desired for the number of failures and device hours under question.

As the number of device hours increases, our confidence in the estimate increases. In integrated circuits, it is preferred to make estimates on the basis of failures per 1,000,000,000 (10^9) device hours **(FITS)** or more. If such large numbers of device hours are not available for a particular device, then the point estimate is obtained by pooling the data from devices that are similar in process, voltage, construction, design, etc., and for which we expect to see the same failure modes in the field.

The environment is specified in terms of the temperature, electric field, relative humidity, etc., by an **Eyring** type equation of the form:

$$\lambda = Ae - \frac{\phi}{KT}\ \ldots e - \frac{B}{RH}\ \ldots e - \frac{C}{E}$$

where A, B, C, ϕ & K are constants, T is temperature, RH is relative humidity, E is the electric field, etc.

The most familiar form of this equation deals with the first exponential which shows an **Arrhenius type** relationship of the **failure rate** versus the **junction temperature** of integrated circuits, while the causes of failure generally remain the same. Thus we can test devices near their maximum junction temperatures, analyze the failures to assure that they are the types that are accelerated by temperature and then applying known acceleration factors, estimate the failure rates for lower junction temperatures. The Eyring or Arrhenius relationships should be used for failure rate projections in conjunction with proper understanding of failure modes, mechanisms and patterns such as infant mortality, constant failure rate (useful region) and wearout. For example if by design and proper process control infant mortality and useful period failures have been brought to zero and wearout failures do not start until, let us say, 30,000 hours at 125°C then failure rate projections at lower temperatures must account for these facts and whether the observed wearout failures occur at lower temperatures.

Figure 7 shows an example of a curve which gives estimates of failure rates versus temperature for an integrated circuit case study.

$$\text{Arrhenius type of equation:}\quad \lambda = Ae - \frac{\phi}{KT}$$

where: λ = Failure Rate
A = Constant
e = 2.72
ϕ = Activation Energy
K = Botzman’s Constant
T = Temperature in Degrees Kelvin

$$T_J = T_A + \theta_{JA} P_D \text{ or } T_J = T_C + \theta_{JC} P_D$$

where: T_J = Junction Temperature
T_A = Ambient Temperature
T_C = Case Temperature
θ_{JA} = Junction to Ambient Thermal Resistance
θ_{JC} = Junction to Case Thermal Resistance
P_D = Power Dissipation

Life patterns (failure rate curves) for equipment and devices can be represented by an idealized graph called the **Bathtub Curve** (Figure 8).

There are three important regions identified on this curve. In Region A, the failure rate decreases with time and it is generally called **infant mortality** or early life failure region. In Region B, the failure rate has reached a relatively constant level and it is called **constant failure rate** or useful life region**.** In the third region, the failure rate increases again and it is called **wearout region**. Modern integrated circuits generally do not reach the wearout portion of the curve when operating under normal use conditions.

Figure 7. Example of a Failure Rate versus Junction Temperature Curve

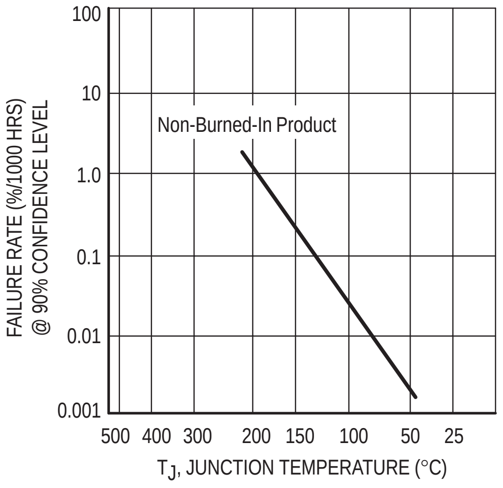
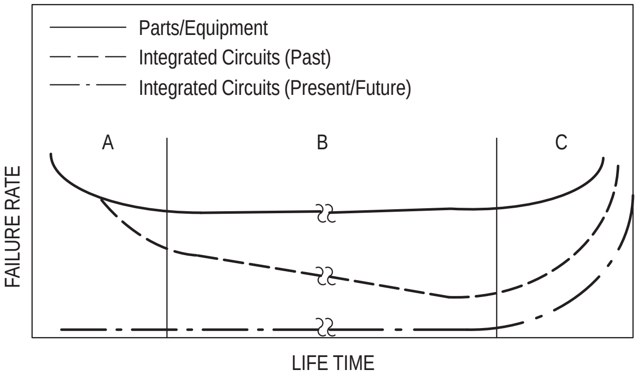


Figure 8. A Model for Failure Distribution in Time Domain Bathtub Curve Model



Decreasing Failure Rate	Constant Failure Rate	Increasing Failure Rate
Infant Mortality Burn-In	Useful Life	Wearout
Manufacturing Variations Workmanship Defects	Random (Chance) Defects (No Pattern; Occur Regularly)	Material, Design, Process Limitations
Weibull Log Normal Gamma Distribution	Weibull Exponential for Equipment Log Normal for ICs	Weibull Normal (Gaussian)

The wearout portion of the curve can usually be identified by using highly accelerated test conditions. For modern integrated circuits, even the useful life portion of the curve may be characterized by few or no failures. As a result the bathtub curve looks like continuously declining (few failures, Figure 8, Curve B) or zero infant and useful period failures (constant failure rate until wearout, Curve C).

The **infant mortality** portion of the curve is of most interest to equipment manufacturers because of its impact on customer perception and potential warranty costs. In recent years the infant mortality portion of the curve for integrated circuits, and even equipment, has been drastically reduced

(Figure 8, Curve C). The reduction was accomplished by improvements in technology, emphasis on statistical process control, reliability modeling in design and reliability in manufacturing (wafer level reliability, assembly level reliability, etc.). In this respect many integrated circuit families have zero or near zero failure patterns until wearout starts.

Does a user still need to consider burn-in? For this question to be answered properly the IC user must consider the **target failure rate** of the equipment, **apportioned** to the components used, application environment, maturity of equipment and components (new versus mature technology), the impact of a failure (i.e. safety versus casual loss of entertainment), maintenance costs, etc. Therefore, if the IC user is going through these considerations for the first time, the question of burn-in at the component level should be discussed during a user-vendor interface meeting.

A frequently asked question is about the reliability differences between **plastic** and **hermetic** packaged integrated circuits. In general, for all integrated circuits including analog, the field removal rates are the same for normal use environments, with many claims of plastic being better because of its ‘‘solid block” structure.

The tremendous decrease of failure rates of plastic packages has been accomplished by **continuous improvements** in piece parts, materials and processes. Nevertheless, differences can still be observed under highly accelerated environmental stress conditions. For example, if a bimetallic (gold wire and aluminum metallization) system is used in plastic packages and they are placed on a high temperature operating life test (125°C) then failures in the form of opens, at the gold to aluminum interface, may not be observed until 30,000 hours of continuous operating life. Packages, whether plastic or hermetic, with a monometallic system (aluminum wire to aluminum metallization) will have no opens because of the absence of the gold to aluminum interface. As a result, a difference in failure rates will be observable.

Differences in failure rates between plastics and hermetics may also be observed if devices from both packaging systems are placed in a moist environment such as 85°C, 85% RH with bias applied. At some point in time plastic encapsulated ICs should fail since they are considered pervious by moisture, (the failure mechanism being corrosion of the aluminum metallization) while hermetic packages should not fail since they are considered impervious by moisture. The reason the word ‘‘should” was used is because advances in plastic compounds, package piece parts, encapsulation processes and final chip passivation have made plastic integrated circuits capable of operating more than 5000 hours without failures in an 85°C, 85% RH environment. Differences in failure rates due to internal corrosion between plastic and hermetic packages may not be observable until well after 5000 operating hours.

The aforementioned two examples had environments substantially more accelerated than normal life so the two issues discussed are not even a factor under normal use conditions. In addition, mechanisms inherent in hermetic packages but absent in plastics were not even considered here. Improved reliability of plastic encapsulated ICs has decreased demand of hermetic packages to the point where many devices are offered only in plastic packages. The user then should feel comfortable in using the present plastic packaging systems.

A final question that is asked by the IC user is, how can one be assured that the reliability of standard product does not degrade over time? This is accomplished by our emphasis on **statistical process control, in-line reliability** assessment and **reliability auditing** by periodic and strategic sampling and accelerated testing of the various integrated circuit device packaging systems. A description of these audit programs follows.

Analog Reliability Audit Program

The reliability of a product is a function of proper understanding of the application and environmental conditions that the product will encounter during its life as well as design, manufacturing process and final use conditions. **Inherent reliability** is the reliability which a product would have if there were no imperfections in the materials, piece parts and manufacturing processes of the product. The presence of imperfections gives rise to reliability risks. **Failure Mode and Effects Analysis (FMEA)** is a technique for identifying, controlling and eliminating potential failures from the design and manufacture of the product.

Motorola uses **on-line** and **off-line** reliability monitoring in an attempt to prevent situations which could degrade reliability. **On-line** reliability monitoring is at the **wafer and assembly levels** while **off-line** reliability monitoring involves reliability assessment of the **finished product** through the use of **accelerated** environmental tests.

Continuous monitoring of the reliability of analog integrated circuits is accomplished by the **Analog Reliability Audit Program**, which is designed to compare the actual reliability to that specified. This objective is accomplished by periodic and strategic sampling of the various integrated circuit device packaging systems. The samples are tested by subjecting them to accelerated environmental conditions and the results are reviewed for unfavorable trends that would indicate a degradation of the reliability or quality of a particular packaging system. This provides the trigger mechanism for initiating an investigation for **root cause** and **corrective action**. Concurrently, in order to provide a minimum of interruption of product flow and assure that the product is fit for use, a lot by lot sampling or a non-destructive type 100% screen may be used to assure that a particular packaging system released for shipment does have the expected reliability. This rigorous surveillance is continued until there is sufficient proof (many consecutive lots) that the problem has been corrected.

The **Logic and Analog Technologies Group** has used reliability audits since the late sixties. Such programs have been identified by acronyms such as CRP (Consumer Reliability Program), EPIIC (Environmental Package Indicators for Integrated Circuits), LAPP (Linear Accelerated Punishment Program), and RAP (Reliability Audit Program).

Currently, the Analog Reliability Audit Program consists of a **Weekly Reliability Audit** and a **Quarterly Reliability Audit**. The Weekly Reliability Audit consists of rapid (short time) types of tests used to monitor the production lines on a real time basis. This type of testing is performed at the assembly/test sites worldwide. It provides data for use as an **early warning system** for identifying negative trends and triggering investigations for root cause and corrective actions.

The Quarterly Reliability Audit consists of long term types of tests and is performed at th U.S. Bipolar Analog Division Center. The data obtained from the Quarterly Reliability Audit is used to assure that the correlation between the short term weekly tests and long term quarterly tests has not changed and a new failure mechanism has not appeared.

A large data base is established by combining the results from the Weekly Reliability Audit with the results from the Quarterly Reliability Audit. Such a data base is necessary for estimating long term failure rates and evaluating potential process improvement changes. Also, after a process improvement change has been implemented, the Analog Reliability Audit Program provides a system for monitoring the change and the past history data base for evaluating the affect of the change.

Weekly Reliability Audit

The Weekly Reliability Audit is performed by each assembly/test site worldwide. The site must have capability for final electrical and quality assurance testing, reliability testing and first level of failure analysis. The results are reviewed on a continuous basis and corrective action is taken when appropriate. The results are accumulated on a monthly basis and published.

The Reliability Audit test plan is as follows:

Electrical Measurements: Performed initially and after each reliability test, consist of critical parameters and functional testing at 25°C on a go-no-go basis.

High Temperature Operating Life: Performed to detect failure mechanisms that are accelerated by a combination of temperature and electric fields. Procedure and conditions are per MIL-STD-883, Method 1015 with an ambient temperature of 145°C for 40 hours or equivalent based on a 1.0 eV activation energy and the Arrhenius equation.

Approximate Accelerated Factors

	125°C	50°C
145°C	4	4000
125°C	1	1000

Temperature Cycling/Thermal Shock: Performed to detect mechanisms related to thermal expansion and contraction of dissimilar materials, etc. Procedures and conditions are per MIL-STD-883, Methods 1010 or 1011, with ambient temperatures of –65° to +150°C or –40° to +125°C (JEDEC-STD-22-A104), for a minimum of 100 cycles.

Pressure Temperature Humidity (Autoclave): Performed to measure the moisture resistance of plastic encapsulated packages. It detects corrosion type failure mechanisms due to free ionic contaminants that may have entered the package during the manufacturing processes. Conditions are per JEDEC-STD-22, Method 102, a temperature of 121°C, steam environment and 15 psig. The duration of the test is 96 hours (minimum).

Analysis Procedure: Devices failing to meet the electrical criteria after being subjected to an accelerated environment type test are verified and characterized electrically, then submitted for failure analysis.

Quarterly Reliability Audit

The Quarterly Analog Reliability Audit Program is performed at the U.S. Bipolar Analog Division Center. This testing is designed to assure that the correlation between the short term weekly tests and the longer quarterly tests has not changed and that no new failure mechanisms have appeared. It also provides additional long term information for a data base for estimating failure rates and evaluation of potential process improvement changes.

Electrical Measurements: Performed initially and at interim readouts, consist of all standard DC and functional parameters at 25°C, measured on a go-no-go basis.

High Temperature Operating Life Test: Performed to detect failure mechanisms that are accelerated by a combination of temperature and electric fields. Procedure and conditions are per MIL-STD-883, Method 1015, with an ambient temperature of 145°C for 40 and 250 hours or equivalent, based on 1.0 eV activation energy and the Arrhenius equation.

Approximate Accelerated Factors

	125°C	50°C
145°C	4	4000
125°C	1	1000

Temperature Cycling/Thermal Shock: Performed to detect mechanisms related to thermal expansion and contraction, mismatch effects, etc. Procedure and conditions are per MIL-STD-883, Methods 1010 or 1011, with ambient temperatures of –65° to +150°C or –40° to +125°C (JEDEC-STD-22-A104) for 100, 500 and 1000 or more cycles, depending on the temperature range used. Temperature Cycling is used more frequently than Thermal Shock.

Pressure Temperature Humidity (Autoclave): Performed to measure the moisture resistance of plastic encapsulated packages. It detects corrosion type failure mechanisms due to free ionic contaminants that may have entered the package during the manufacturing processes. Conditions are per JEDEC-STD-22, Method 102, a temperature of 121°C, steam environment and 15 psig. The duration of the test is for 96 hours (minimum), with a 48 hour interim readout.

Pressure Temperature Humidity Bias (PTHB; Biased Autoclaved): This test measures the moisture resistance of plastic encapsulated packages. It detects corrosion type failure mechanisms due to free and bounded ionic contaminants that may have entered the package during the manufacturing processes, or they may be bound in the materials of the integrated circuit packaging system and activated by the moisture and the applied electrical fields. Conditions are per JEDEC-STD-22, Method 102, with bias applied, a temperature of 121°C, steam environment and 15 psig. This test detects the same type of failures as the Temperature Humidity Bias (85°C, 85% RH, with bias) test, only faster. The acceleration factor between PTHB and THB is between 20 and 40 times, depending on the type of corrosion mechanism, electrical field and packaging system.

Highly Accelerated Stress Test (HAST) is increasingly replacing the aforementioned **PTHB** test. The reason is that the **HAST** test allows control of pressure, temperature and humidity independently of each other, thus we are able to set different combinations of temperature and relative humidity. The most frequently used combination is **130°C with 85% RH**. This has been related to THB (85°C, 85% RH) by an **acceleration factor of 20** (minimum). The ability to keep the relative humidity variable constant for different temperatures is the most appealing factor of the HAST test because it reduces the determination of the acceleration factor to a single Arrhenius type of relationship. Motorola has been phasing over to HAST testing since 1985.

Temperature, Humidity and Bias (THB): This test measures the moisture resistance of plastic encapsulated packages. It detects corrosion type failure mechanisms due to free and bounded ionic contaminants that may have entered the package during the manufacturing processes, or they may be bound in the materials of the integrated circuit packaging system and activated by moisture and the applied electrical fields. Conditions are per JEDEC-STD-22, Method 102 (85°C, 85% RH), with bias applied. The duration is for 1008 hours, with a 504 hour interim readout. The acceleration factor between THB (85°C, 85% RH with bias) and the 30°C, 90% RH is typically 40 to 50 times, depending on the type of corrosion mechanism, electrical field and packaging system.

Analysis Procedure: Devices failing to meet the electrical criteria after being subjected to an accelerated environment type test(s) are verified and characterized electrically, then they are submitted for root cause failure analysis and corrective action for continuous improvement.

Applications and Product Literature

In Brief . . .

Motorola's Applications Literature provides guidance to the effective use of its semiconductor families across a broad range of practical applications. Many different topics are discussed — in a way that is not possible in a device data sheet — from detailed circuit designs complete with PCB layouts, through matters to consider when embarking on a design, to complete overviews of product families and their design philosophies.

Information is presented in the form of Application Notes, Article Reprints and detailed Engineering Bulletins.

Abstracts of all the applications documents are provided as a guide to their content; each abstract also shows the number of pages in the document, plus the origin of the article in the case of Article Reprints. Documents new to this issue are highlighted throughout.

Applications and Product Literature

*Indicates New Document

The application literature listed in this section has been prepared to acquaint the circuits and systems engineer with Motorola Linear integrated circuits and their applications. To obtain copies of the notes, simply list the publications number or numbers and send your request on your company letterhead to: Literature Distribution Center, Motorola Semiconductor Products Inc., P.O. Box 20912, Phoenix, Arizona 85036.

Application Note Abstracts

AN004E *Semiconductor Consideration for DC Power Supply Voltage Protector Circuits*

This paper addresses the requirements for the semiconductor sensing circuitry and SCR crowbar devices used in DC power supply over/under voltage protection schemes. (8pp)

AN428 *Automotive Direction Indicator with Short Circuit Detection Using the UAA1041*

Cold lamps and faulty wiring can cause false operation when using the UAA1041 Automotive Direction Indicator IC. This note provides simple solutions. (3pp)

AN531 *MC1596 Balanced Modulator*

The MC1596 Monolithic Balanced Modulator is a versatile HF communications building block. It functions as a broadband, double-sideband suppressed-carrier balanced modulator without the need for transformers or tuned circuits. This article describes device operation and biasing, and gives circuit details for typical modulator/demodulator applications in AM, SSB and suppressed-carrier AM. Additional uses as an SSB Product Detector, AM Modulator/Detector, Mixer, Frequency Doubler, Phase Detector and others are also illustrated. An appendix gives detailed AC and DC analysis. (13pp)

AN535 *Phase-Locked-Loop Design Fundamentals*

The fundamental design concepts for phase-locked-loops implemented with integrated circuits are outlined. The necessary equations required to evaluate the basic loop performance are given in conjunction with a brief design example. (12pp)

AN545A *Television Video IF Amplifier Using Integrated Circuits*

This applications note considers the requirements of the video IF amplifier section of a television receiver, and gives working circuit schematics using integrated circuits which have been specifically designed for consumer oriented products. The integrated circuits used are the MC1350, MC1352, and the MC1330. (12pp)

AN559 *A Single Ramp Analog-to-Digital Converter*

A simple single ramp A/D converter which incorporates a calibration cycle to ensure an accuracy of 12 bits is discussed. The circuit uses standard ICs and requires only one precision part — the reference voltage used in the calibration. This converter is useful in a number of instrumentation and measurement applications. (10pp)

AN569 *Transient Thermal Resistance — General Data and its Use*

Data illustrating the thermal response of a number of semiconductor die and package combinations are given. Its use, employing the concepts of transient thermal resistance and superposition, permit the circuit designer to predict semiconductor junction temperature at any point in time during application of a complex power pulse train. (16pp)

AN587 *Analysis and Design of the Op Amp Current Source*

Voltage-controlled current sources based on operational amplifiers are both versatile and accurate, yet the quality of op amps required is unimportant. This note develops general expressions for basic transfer function and output impedance, and shows that simplified equations give a very accurate description of actual circuit performance. Includes a section on analysis of the errors that result from changes in circuit parameters and temperature. (7pp)

AN703 *Designing Digitally-Controlled Power Supplies*

This application note shows two design approaches; a basic low voltage supply using an inexpensive MC1723 voltage regulator and a high current, high voltage, supply using the MC1466 floating regulator with optoelectronic isolation. Various circuit options are shown to allow the designer maximum flexibility in an application. (9pp)

AN708A *Line Driver and Receiver Considerations*

This report discusses many line driver and receiver design considerations such as system description, definition of terms, important parameter measurements, design procedures and application examples. An extensive line of devices is available from Motorola to provide the designer with the tools to implement the data transmission requirements necessary for almost every type of transmission system. (18pp)

AN719 *A New Approach To Switching Regulators*

This article describes a 24 V, 3.0 A switching mode supply. It operates at 20 kHz from a 120 V AC line with an overall efficiency of 70%. New techniques are used to shape the load line. The control circuit uses a quad comparator and an opto-coupler and features short circuit protection. (12pp)

AN740 ***The Design of an N-Channel 16k x 16 Bit Memory System for the PDP-11***

This application note describes the design and construction of a mainframe memory system with MCM6605 N-channel MOS memories. Topics included are: the interface to the PDP-11, refresh control and bookkeeping, timing control logic for the memories, memory system considerations and organization. The memory also features new integrated circuits that reduce package count and enhance memory system performance. (16pp)

AN781A ***Revised Data Interface Standards***

Revised data interface standards allow higher data rates and longer cables. This note provides an overview and comparison of the electrical and performance characteristics of RS232-C, RS422, RS423, RS449 and RS485. Includes a list of appropriate Motorola drivers and receivers with performance summaries. (6pp)

AN829 ***Application of the MC1374 TV Modulator***

The MC1374 was designed for use in applications where separate audio and composite video signals are available, which need converting to a high quality VHF television signal. It’s ideally suited as an output device for subscription TV decoders, video disk and video tape players. (12pp)

AN879 ***Monomax: Application of the MC13001 Monochrome Television Integrated Circuit***

This application note presents a complete 12″ black and white line-operated television receiver, including artwork for the printed circuit board. It is intended to provide a good starting point for the first-time user. Some of the most common pitfalls are overcome, and the significance of component selections and locations are discussed. (12pp)

AN917 ***Reading and Writing in Floppy Disk Systems Using Motorola Integrated Circuits***

The floppy disk system has become a widely used means for storing and retrieving both programs and data. A floppy disk drive requires precision controls to position and load the head as will as defined read/write signals in order to be a viable system. This application note describes the use of the MC3469 and MC3471 Write Control ICs and the MC3470 Read Amplifier which provide the necessary head and erase control, timing functions, and filtering. (16pp)

AN920 ***Theory and Applications of the MC34063 and µA78S40 Switching Regular Control Circuits***

This paper describes in detail the principle of operation of the MC34063 and µA78S40 switching regulator subsystems. Several converter design examples and numerous applications circuits with test data are included. (38pp)

AN921 ***Horizontal APC/AFC Loops***

The most popular method used in modern television receivers to synchronize the line frequency oscillator is the phase locked loop. The operating characteristics and parameters of the loops are discussed. (19pp)

AN932 ***Application of the MC1377 Color Encoder***

The MC1377 is an economical, high quality, RGB encoder for NTSC or PAL applications. It accepts RGB and composite sync inputs, and delivers a 1.0 Vp-p composite NTSC or PAL video output into a 75 Ω load. It can provide its own color oscillator and burst gating, or it can easily be driven from external sources. Performance virtually equal to high-cost studio equipment is possible with common color receiver components. (12pp)

AN954** ***A Unique Converter Configuration Provides Step–Up/Down Functions

The use of switching regulators in new portable equipment designs is becoming more pronounced over that of linear regulators. This is primarily due to the need for reductions in size and weight which dictate an ever increasing demand for higher power conversion efficiency from a battery pack. When designing at the board level it sometimes becomes necessary to generate a constant output voltage that is less than that of the battery. The step–down circuit is presented that will perform this function efficiently. However, as the battery discharges, its terminal voltage will eventually fall down below the desired output, and in order to utilize the remaining battery energy a step–up circuit is also presented.

AN957 ***Interfacing the Speakerphone to the MC34010/11/13 Speech Networks***

Interfacing the MC34018 speakerphone circuit to the MC34010 series of telephone circuits is described in this application note. The series includes the MC34010, MC34011, MC34013, and the new ‘‘A’’ version of each of those. The interface is applicable to existing designs, as well as to new designs. (12pp)

AN958 ***Transmit Gain Adjustments for the MC34014 Speech Network***

The MC34014 telephone speech network provides for direct connection to an electret microphone and to Tip and Ring. In between, the circuit provides gain, drive capability, and determination of the ac impedance for compatibility with the telephone lines. Since different microphones have different sensitivity levels, different gain levels are required from the microphone to the Tip and Ring lines. This application note will discuss how to change the gain level to suit a particular microphone while not affecting the other circuit parameters. (2pp)

AN959 ***A Speakerphone with Receive Idle Mode***

The MC34018 speakerphone system operates on the principle of comparing the transmit and receive signals to determine which is stronger, and then switching the circuit into that mode. (2pp)

AN960 ***Equalization of DTMF Signals Using the MC34014***

This application note will describe how to obtain equalization (line length compensation) of the DTMF dialing tones using the MC34014 speech network. (2pp)

AN968 ***A Digital Voice/Data Telephone Set***

This design provides standard analog telephone functions while simultaneously transmitting 9600 baud asynchronous data. It is based on Motorola's MC145422/26 UDLT family of voice/data ICs which provide 80 kbps full-duplex synchronous communication over distances up to 2 km. The circuit includes a Codec/filter, Data Set Interface and pulse/tone dialer. (7pp)

AN976 ***A New High Performance Current Mode Controller Teams Up with Current Sensing Power MOSFETs***

A new current mode control IC that interfaces directly with current sensing power MOSFETs is described. Its second generation architecture is shown to provide a variety of advantages in current mode power supplies. The most notable of these advantages is a ‘‘lossless’’ current sensing capability that is provided when used with current sensing MOSFETs. The discussion includes subtle factors to watch out for in practical designs, and an applications example. (8pp)

AN980 ***VHF Narrowband FM Receiver Design Using the MC3362 and the MC3363 Dual Conversion Receivers***

The MC3362 and MC3363 narrowband FM dual conversion receivers feature excellent VHF performance with low power drain, making them ideal for cordless telephones, narrowband voice and data receivers and RF security devices. This note provides a detailed description of the operation of the two devices, plus circuits and descriptions for four applications: a Single Channel VHF FM Narrowband Receiver; a Ten Channel Frequency Synthesized Cordless Telephone Receiver; a 256 Channel Frequency Synthesized Two-Meter Amateur Band Receiver; and a Single Chip Weather Band Receiver. (14pp)

AN983 ***A Simplified Power Supply Design Using the TL494 Control Circuit***

This application note describes the operation and characteristics of the TL494 Switchmode™ Voltage Regulator and shows its application of a 400 W offline power supply.

The TL494 is a fixed-frequency pulse width modulation control circuit, incorporating the primary building blocks required for the control of a switching power supply. (5pp)

AN1002 ***A Handsfree Featurephone Design Using the MC34114 Speech Network and the MC34018 Speakerphone ICs***

A comprehensive application note which develops a full featurephone circuit using the MC34114 Speech Network, the MC34018 Speakerphone IC and the MC145412 Dialer. Functions include 10 number memory pulse/tone dialer, tone ringer, mike mute and line length compensation for both handset and speakerphone operation. Options include line-powered circuit, line-powered circuit with booster for long lines, and external supply-powered. Includes glossary of telephone terms. (18pp)

AN1003 ***A Featurephone Design, with Tone Ringer and Dialer, Using the MC34118 Speakerphone IC***

This application note describes how to add a handset, dialer and tone ringer to the MC34118 speakerphone circuit. Although any one of several speech networks could be used as an interface between the MC34118 and the phone line this application note covers the case where simplicity and low cost are paramount. Two circuits are developed in this discussion: line-powered and supply-powered versions. (13pp)

AN1004 ***A Handsfree Featurephone Design Using the MC34114 Speech Network and the MC34118 Speakerphone ICs***

Complete designs for a featurephone providing 10 number memory, pulse or tone dialling, tone ringer, microphone muting, and line length compensation for both handset and speakerphone operation. Includes line-powered, line-powered plus long-line booster, and supply-powered versions. The MC34114 interfaces with tip and ring and provides 2-to-4 wire conversion. (18pp)

AN1006 ***Linearize the Volume Control of the MC34118 Speakerphone***

A single resistor added to the volume control potentiometer in an MC34118 speakerphone application will almost perfectly linearize the control law. (1pp)

AN1016 ***Infrared Sensing and Data Transmission Fundamentals***

Many applications need electrical isolation, remote control or position sensing. Infrared light provides an excellent solution due to its low cost, ease of use, availability of components, and freedom from the licensing and interference concerns of RF techniques. This note is a brief but informative reference on the design principles for IR systems, including a selection of receiver circuits. (6pp)

AN1019 ***NTSC Decoding Using the TDA3330, with Emphasis on Cable In/Cable Out Operation***

The TDA3330 is a Composite Video to RGB Color Decoder originally intended for PAL and NTSC color TV receivers and monitors — so its data sheet concentrates on picture tube drive. This practical application note supplements the data sheet by providing circuits for video cable drive as used in video processing, frame store and other specialized applications, and expands on TDA3330 functional details. Includes PCB artwork and layout of an evaluation board. (8pp)

AN1040 ***Mounting Considerations for Power Semiconductors***

The operating environment is a vital factor in setting current and power ratings of a semiconductor device. Reliability is increased considerably for relatively small reductions in junction temperature. Faulty mounting not only increases the thermal gradient between the device and its heatsink, but can also cause mechanical damage. This comprehensive note shows correct and incorrect methods of mounting all types of discrete packages, and discusses methods of thermal system evaluation. (20pp)

AN1044 ***The MC1378 — A Monolithic Composite Video Synchronizer***

The MC1378 provides an interface between a remote composite color video source and local RGB. On-chip circuitry can lock a local computer to the remote source, switching between local and remote signals to generate composite video overlays. This detailed note describes local and remote operation; picture-in-picture applications and the design of test fixtures to help system development. Printed circuit artwork for an evaluation board is provided. The NTSC/PAL color encoder is similar to the MC1377, discussed in detail in AN932. (13pp)

AN1046 ***Three Piece Solution for Brushless Motor Control Design (Rev. 1)***

Until recently, the design of compact but comprehensive circuits taking full advantage of the unique attributes of brushless DC motors has been difficult, while available power transistors have not always performed as well as is necessary for the application. This high-performance three-chip solution couples the rugged MPM3003 three phase MOSFET bridge (in a 12-pin power package) with the MC33035 Brushless DC Motor Adapter. Design is simplified, board area reduced. Full circuit, parts list, and discussion of practical considerations. (10pp)

AN1065** ***Use of the MC68HC68T1 Real–Time Clock with Multiple Time Bases

While this Application Note is primarily about the MC68HC68T1 clock/calendar device, it also provides an example of the application of two Motorola Analog ICs: the MC34160 Microporcessor Voltage Regulator and Supervisory Circuit and the MC34164 Undervoltage Sensing Circuit. The MC34160 provides a regulated 5.0 V supply, plus power warning and reset outputs to the MCU. The MC34164 assures that the MCU is held in reset when the supply voltage is too low for the MC34160 to operate correctly.

AN1077 ***Adding Digital Volume Control To Speakerphone Circuits***

Describes how to control speakerphone volume from UP and DOWN switches in place of the more usual potentiometer. Includes a fully annotated circuit using only three standard CMOS ICs and no critical components. (4pp)

AN1078 ***New Components Simplify Brush DC Motor Drives***

A variety of new components simplify the design of brush motor drives. One is a brushless motor control IC which is easily adapted to brush motors. Others include multiple Power MOSFETs in H-Bridge configuration, a new MOS turn-off device, and gain-stable opto level shifters. Several circuits illustrate how the new devices can be used in practical motor drives, in particular to control speed in both directions and operate from a single power supply. (6pp)

AN1080 ***External-Sync Power Supply with Universal Input Voltage Range for Monitors***

As the resolution of color monitors increases, the performance and features of their power supplies becomes more critical. EMI/RFI generated by switching power supplies can adversely affect resolution if switching frequency is not synchronized to horizontal scanning frequency. This 90 W flyback switching supply demonstrates the use of new high performance devices in a low cost design, and includes a new universal input voltage adapter. (20pp)

AN1081 ***Minimize the "pop" in the MC34119 Low Power Audio Amplifier***

Sometimes a "pop" is heard in the loudspeaker when the MC34119 audio amplifier is re-enabled. There are several possible causes, but this note offers a simple and low cost remedy to satisfy the most demanding user. (3pp)

AN1101 ***One-Horsepower Off-Line Brushless Permanent Magnet Motor Drive***

Brushless Permanent Magnet (BPM) motors (brushless DC motors) using MOSFET inverters are common in low voltage, variable speed applications such as disk drives. Higher voltage off-line applications can also use the same technology, but there have been problems in designing a reliable, low cost high side driver and understanding the more subtle effects of diode snap and PCB layout. This one-horsepower off-line BPM motor drive board uses opto-isolators and a special MOSFET turn-off IC for level translation. Includes PCB artwork and parts list, and a discussion of the theory. (10pp)

AN1108 ***Design Considerations for a Two Transistor, Current Mode Forward Converter***

This design for a 150 W, 150 kHz, two transistor, current mode forward converter illustrates solutions for noise control, feedback circuit analysis and magnetic component design — topics that often create the most problems for designers. Improved Schottky rectifiers, power MOSFETs and optocouplers — and their effects on switchmode power supply design — are also considered. Includes circuit, analysis, parts list and theoretical discussion. (11pp)

AN1122 ***Running the MC44802A PLL Circuit***

The MC44802A provides the Phase-Locked-Loop (PLL) portion of a tuning circuit intended for TV, FM radio and set-top converter applications up to 1.3 GHz; a complete tuning circuit is formed by adding a Voltage Controlled Oscillator (VCO) and mixer. The data sheet recommends use of an MCU for sending the control bytes that set the tuning frequency. This note describes a serial (I^2C) interface with an MC68HC11E9 in a tuner design — the information is sufficiently general to allow almost any MCU to be used. Includes M68HC11 program listing. (12pp)

AN1126 ***Evaluation Systems for Remote Control Devices on an Infrared Link***

The availability at low cost of remote control devices and infrared communication links provides opportunities in many application areas. This note gives information for constructing the basic building blocks to evaluate both IR links and the most popular remote control devices. Schematics and single-side PCB layouts are presented that should enable the designer quickly to put together a basic control link and evaluate its suitability for a given application in terms of data rate, effective distance, error rate and cost. Sources for special parts are also given. (10pp)

AN1203 ***A Software Method for Decoding the Output from the MC14497/MC3373 Combination***

Infrared communication is now widely used as a simple and effective means of remote control over short distances. A variety of encoding methods is used, including the biphase scheme implemented by the MC14497, a complete building block for IR data transmission. The MC3373 is a companion receiver chip to the MC14497, providing front-end processing to interface a photo detector to a TTL level. This note describes the decoding of the data at the output of the MC3373, along with software listings for the MC68HC11 and the MC68HC05. (5pp)

AN1300 ***Interfacing Microcomputers to Fractional Horsepower Motors***

In fractional horsepower motion control systems, command signals are usually now generated by a microprocessor or digital signal processor, while power is applied with MOSFETs. The interface between the two can still present difficulties; for small motors it will be, typically, 5.0 V logic to complementary P-Channel/N-Channel MOSFET H-bridges. A number of factors need to be considered, including diode snap, group bounce, noise suppression and locking out invalid inputs. The design discussed here is embodied in evaluation board DEVB103. (8pp)

AN1301 ***Interfacing Analog Inputs to Fractional Horsepower Motors***

In many types of systems it is desirable to control motor speed with an analog signal. Even in digital systems, it is often cost effective to generate an analog signal from static speed control bits or a lower frequency PWM signal than to use a more expensive MCU capable of generating a 20 kHz+ PWM signal directly. Although recent developments have simplified analog input conversion and power MOSFET outputs, the interface between signal processing circuits and power outputs is still far from simple. This note discusses the issues using the DEVB118 evaluation board as an example design. (9pp)

AN1306 ***Thermal Distortion in Video Amplifiers***

Thermal distortion is a problem in many high resolution video amplifiers. It occurs when there are instantaneous power changes in the transistor stages, and if the problem remains uncompensated, this leads to the visual effect known as smearing. This note discusses what smearing is, what causes thermal distortion, how to measure it, and how to compensate for it. (5pp)

AN1307 ***A Simple Pressure Regulator Using Semiconductor Pressure Transducers***

Semiconductor pressure transducers offer an economical means of achieving high reliability and performance in pressure sensing applications. The completely integrated MPX5100 (0 psi to 15 psi) series provides a temperature compensated, high level linear output suitable for interfacing directly with many linear control systems. This circuit illustrates how the MPX5100 can be used with a simple pressure feedback system based on the MC33033 Brushless Motor Controller to establish pressure regulation. Includes circuit diagram and PCB artwork. (7pp)

AN1315** ***An Evaluation System Interfacing the MPX2000 Series Pressure Sensors to a Microprocessor

Outputs from compensated and calibrated semiconductor pressure sensors such as the MPX2000 series devices are easily amplified and interfaced to a microprocessor. Design considerations and the description of an evaluation board using a simple analog interface connected to a microprocessor is presented here. (21pp)

AN1510 ***A Mode Indicator for the MC34118 Speakerphone Circuit***

Within the MC34118 are two comparators driven by the level detectors which are sensing the speech signals (see MC34118/D Data Sheet, Figure 24). The comparators' outputs drive the attenuator control block which sets the operating mode. (2pp)

AN1539** ***An IF Communication Circuit Tutorial

This article is intended to be a tutorial on the use of IF communication integrated circuits. The ISM band channel bandwidths and the Motorola MC13156 are used within this article as a platform for discussion. An examination of the devices topology is provided along with a discussion of the classical parameters critical to the proper operation of any typical IF device. The parameters reviewed are impedance matching the mixer, selecting the quad tank and filters and concluding with a overview of bit error rate testing for digital applications. Upon completion, the reader will have a better understanding of IF communications basics and will be able to specify the support components necessary for proper operation of these devices. (8pp)

AN1544** ***Design of Continuously Variable Slope Delta Modulation Communication Systems

Delta modulation is a simple and robust method of A/D conversion in systems requiring serial digital communications of analog signals. Delta modulation is limited by the anlaog input frequency and amplitude processed with any given circuit configuration; *i.e.*, the higher the clock frequency, the better the modulation quality (the clock frequency should be typically 9.6 kHz to 64 kHz for voice applications). Delta modulaton has the advantage that signal to noise ratios do not vary with distance in digital transmission and multiplexing, and the switching and repeating hardware is more economical than with purely analog systems. This paper is intended to give practical guidance in designing an optimum deltamod configuration for the most common voice applications using a Continuously Variable Slope Delta Modulator/Demodulator, MC34115 or MC3418, and provide some useful SNR performance information. (20pp)

AN1548** ***Guidelines for Debugging the MC44011 Video Decoder

Normally, the implementation of the MC44011 Multistandard video decoder is fairly simple in that there are no external adjustments, or critical components, to deal with. However, since this IC contains several interrelated functions and a substantial amount of programmability, debugging an improperly working circuit can sometimes be daunting. The purpose of this document is to provide a procedure for debugging and checking the operation of this IC, and an indication of what to expect at some of the various pins. (8pp)

AN1575** ***Worldwide Cordless Telephone Frequencies

This application note contains a listing of the worldwide cordless telephone frequencies by country. These tables reference application information provided in the MC13109, MC13110, and MC13111 Universal Cordless Telephone Subsystem Integrated Circuit Technical Data Sheets. Channel number, T_X channel frequency, 1st LO frequency, and T_X and R_X divider values are listed in this application note. (8pp)

ANE424 ***50 W Current Mode Controlled Offline Switch Mode Power Supply Working over 50% Duty Cycle using the UC3842A***

Switchmode power supplies based on flyback architecture and voltage-controlled PWM techniques are well established. This note describes a way of improving their dynamic characteristics using a Current Controlled PWM technique. A dedicated bipolar IC, the UC3842A Off-Line Current Mode PWM Controller, performs the current control, regulation and safety features. Full analysis of transformer and other components, plus discussion of the instability inherent in the current control mode. (27pp)

ANHK02 ***Low Power FM Transmitter System MC2831A***

This application note provides information concerning the MC2831A, a one-chip low-power FM transmitter system designed for FM communication equipment such as FM transceivers, cordless telephones, remote control and RF data link. (16pp)

Article Reprint Abstracts

AR301 ***Solid State Devices Ease Task of Designing Brushless DC Motors***

Brushless fractional-horsepower DC motors are gaining in popularity over brush type motors. Their characteristics are similar but they avoid the practical problems associated with brushes. In the past control complexity has made them less attractive, but dedicated control ICs like the MC33034, plus current-sensing power MOSFETs, mean that much of the control and protection electronics is available off the shelf. (*EDN*, 3 September 1987) (7pp)

AR323 ***Managing Heat Dissipation in DPAK Surface Mount Power Packages***

Physically smaller than a lead-formed TO-220, the DPAK was introduced to accommodate larger die than in previously available SM packages like the SOT-89. But larger die implies increased heat dissipation. New board materials and good circuit design ensure that DPAK Power MOSFETs can readily switch at their full pulse current ratings.
(*Powertechnics*, December 1988) (4pp)

AR340 ***The Low Forward Voltage Schottky***

As feature sizes are scaled down in very high density circuits, it will be necessary for the standard power supply voltage to be reduced from 5.0 V to 3.3 V within the next few years to avoid degrading performance in the new devices. Also, greater power supply efficiency will be required if the power supply is not to occupy a disproportionate amount of the total system volume. Since the major power loss in switching power supplies is in the output rectification circuits, more efficient rectifiers are needed. Schottky rectifier technology shows the greatest potential. (*Powertechnics*, May 1990) (3pp)

Engineering Bulletin Abstracts

EB27A ***Get 300 Watts EPE Linear Across 2 to 30 MHz from this Push-Pull Amplifier***

Includes circuit, PCB artwork and layout for a 300 W push-pull linear amplifier based on two MRF422s, designed to operate over the 2.0 MHz to 30 MHz band. An MC1723 voltage regulator is used as a bias supply. (4pp)

EB85A ***Full-Bridge Switching Power Supplies***

A useful selection chart presenting preferred Bipolar, power MOSFET, Rectifier and Control devices for various areas of typical 500 W to 1000 W full-bridge switching power supplies. (1p)

EB112 ***The Application of a Telephone Tone Ringer as a Ring Detector***

Telephone ringers are driven by high voltage, low frequency AC signals which are superimposed on the 48 V DC Tip-Ring feed voltage. An electronic ring detector must sense the presence of an AC signal on the line and produce a dielectrically isolated logic level to the system processor. (2pp)

EB123 ***A Simple Brush Type DC Motor Controller***

A simple and cost effective way to drive brush type DC motors is to use power MOSFETs with a Brushless DC Motor Control IC. The low cost MC33033 controller and integrated 8.0 A/100 V MPM3002 H-bridge combine to give a minimum parts count brush motor drive. (2pp)

EB124 ***MOSFETs Compete with Bipolars in Flyback Power Supplies***

Power MOSFETs with 400 V to 500 V breakdown ratings are widely used in multiple-transistor off-line power supplies. Now they can be used in flyback supplies as well, as breakdown voltages are extended to 1000 V. A discussion of the advantages and disadvantages, illustrated with typical 100 W MOSFET and Bipolar designs. (2pp)

EB126 ***Ultra-Rapid Nickel-Cadmium Battery Charger***

Charging NiCad batteries is a particular problem when their voltage exceeds the voltage of the available charging source. The ultra-fast charger presented here is capable of charging eight to twelve 1.5 V batteries at 1.2 A to 1.8 A in 30 to 45 minutes from a 10 V to 14 V source — a feat made possible by the use of new sintered electrode technology by battery manufacturers. Includes PC artwork and layout. (3pp)

EB128 ***Simple, Low-Cost Motor Controller***

This low cost DC motor controller uses the cost effective MPM3002 SENSEFET-based H-Bridge, plus the MC34060 PWM IC. It is capable of driving a 1/3 HP, permanent magnet 90 V DC motor, and includes dynamic braking and Soft-Start. (2pp)

EB142 ***The MOSFET Turn-Off Device — A New Circuit Building Block***

Technical developments have lead to a variety of discrete devices using circuit integration to reduce system cost and board space, while offering some performance improvement over conventional solutions. The first of these new components — dubbed SMALLBLOCK™ — is a building block that simplifies and reduces the component cost of an active gate-turn-off network for current-source driven MOSFETs. It is available in TO-92, SOT-23 and SOT-223 packages. (8pp)

Product Literature

DL136/D	*Telecommunications Device Data*
HB206	*Linear & Switchmode Voltage Regulator Handbook* (See Back of Chapter 3) (Out of Print)
SG56/D	*TMOS Power MOSFET Selector Guide / Cross Reference*
SG73/D	*Master Selection Guide*
SG79/D	*SWITCHMODE — A Designer's Guide for Switching Power Supply Circuits and Components*
SG96/D	*Linear/Interface ICs Selector Guide Selector Guide and Cross Reference*
SG98/D	*Linear Telecom Cross Reference*
SG127/D	*Surface Mount Products Selector Guide*
SG368/D	*Video Capture Chip Sets Selector Guide* (See Front of Chapter 9)
SG410/D	*Applications & Product Literature Selector Guide / Cross Reference*

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